A HIGHLY MODULAR GRID INTERFACE FOR UTILITY SCALE RENEWABLES: MMC WITH ISOLATED HIGH FREQUENCY LINK SUB-MODULES

A DISSERTATION
SUBMITTED TO THE FACULTY OF THE
UNIVERSITY OF MINNESOTA
BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

ADVISOR: NED MOHAN

MAY, 2017

Acknowledgements

I want to express my deepest gratitude to my advisor Professor Ned Mohan. He has always been very supportive from the moment I expressed my interest in graduate school. I'm very grateful for his guidance and support throughout my research at the University of Minnesota.

I'm thankful to Professor Wollenberg, Robbins, Dhople, and Rothman. Working as a TA for Professor Wollenberg and Dhople has made me realize how much I enjoy teaching, and has also expanded my interest in the area of power systems. Professor Robbins for his support and allowing me to teach the undergraduate labs, these are one of my fondest memories. Professor Rothman for making a statistics class genuinely interesting, and being a source of inspiration to me.

I would like to thank my lab mates Kartik, Ashis, Suvanker, Srikant, Eric, and Siddharth for always being a great group to bounce ideas off with. My thanks to Apurva, Kaushik, and Gysler, for welcoming me in the lab.

A special thanks to David, Mudita, and Santhosh for being fantastic friends (FB), and for working and developing ideas with me.

My heartfelt thanks to Fernando, Marian, Angel, Veronica, Nichole, Carmelo, Jennifer, Thomas, Landy, Lorie, Hector, Kevin, Carlos, Rebecca, Raquel, and Bernardo for being my family away from home.

This work was supported by the Office of Naval Research (ONR Grant Number N00014-11-1-0897). This financial support is gratefully acknowledged.

Dedication

This dissertation is dedicated to my family, Edna, Jose, Gustavo, Lidiannie, and Carlos whose support and love made this possible. A very special dedication goes to my fiancée Cristina; she has been my pillar of strength and my best friend throughout this process.

Abstract

A novel isolated Modular Multilevel Converter that allows low voltage DC (LVDC) to medium voltage ac (MVAC) power transmission is proposed in this dissertation. The proposed topology is composed of a primary inverter and a collection of sub-modules. Each sub-module is composed of a high-frequency transformer, a diode bridge rectifier, a capacitor, and a half-bridge cell. The sub-modules are arranged in a three phase MMC configuration where the output of each sub-module is the half-bridge cell. The inputs of all sub-modules are connected to the primary inverter via a high-frequency bus bar. Each sub-module is capable of generating its own isolated DC voltage by tapping into the high-frequency bus bar. The galvanic isolation between the MMC side and the input of the inverter, and the unidirectional power flow, is ideal for use with PV panels. The proposed solution allows for scalability with the possibility of reaching MVAC, making it an ideal converter for large scale PV power plants. With the use of high frequency transformers the proposed topology can be built small and lightweight, allowing it for other applications. One example is as a converter for wind energy systems where the reduce size and weight can allow the converter to be located in the hub of smaller wind turbines. This strategy allows the turbine to transmit high voltage power at lower current levels, hence reducing the cable thickness and the conduction losses associated with it.

In this dissertation, a detail analysis of the proposed topology, simulations and experimental results are shown. Simulations were created using the PLECS tool set in Matlab/Simulink. The hardware prototype is a proof of concept design to operate at 1kW, with an input of 100 V, and a 9-level output voltage with a ± 200 V limit. A total of 24 sub-modules were created, 8 for each phase of this three phase converter. Two alternatives for the MMC cell are proposed, a half-bridge solutions and a full-bridge solution, although only the first is developed in hardware. It is shown through simulation and experimentation that the average values of the capacitor voltages are self-balanced, and no additional balancing algorithm is needed. The simulation and experimental results confirm the overall intended operation of the proposed topology.

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1 INTRODUCTION

1.1 Grid-tied converters for Renewables

1.1.1 Motivation

Reduction in the cost of photovoltaic (PV) technologies combined with a recent study indicating that solar has the highest potential to meet the load demand of future [2] are motivating countries to add PV power plants to their energy portfolio [3]. These PV power plants are environment-friendly and can also be grid-friendly by offering voltage and power factor regulation, fault ride through, real power control (plant curtailment), and frequency control [4], [5]. Recent studies show that intermittence can be overcome as new advancements in energy storage control are proposed ([6], [7], [8]). Increasingly accurate meteorological data collection allows for improved PV power plant design to lower the financial risk and potentially allow PV participation in the energy market [9].

A typical PV power plant has the components shown in Figure 1.1. The area of interest for this dissertation is the grid interface marked as "target section". The conventional grid interface approach is to use a three phase, two level inverter combined with a filter and a line-frequency power transformer. This approach has the advantage of using technology that has been tested and understood. However, one of its limitations is the line-frequency transformer. These transformers can be heavy, expensive, and require maintenance if they need to be liquid cooled. Due to their higher power density, high frequency transformers (HFT) are smaller, lighter, and potentially cheaper, making them more attractive over line-frequency transformers [10]. The use of power electronic converters means that high frequencies are already present in the system and that a transformer can be used with virtually no drawbacks.

Injecting unwanted harmonics into the grid creates problems for other components in the system; therefore regulations have been placed in order to limit these

injections. The simplest way to comply with these regulations is to filter the undesired harmonic components out. However, as the system power increases, the filter components also increase in size and price, making them more difficult to design and build.

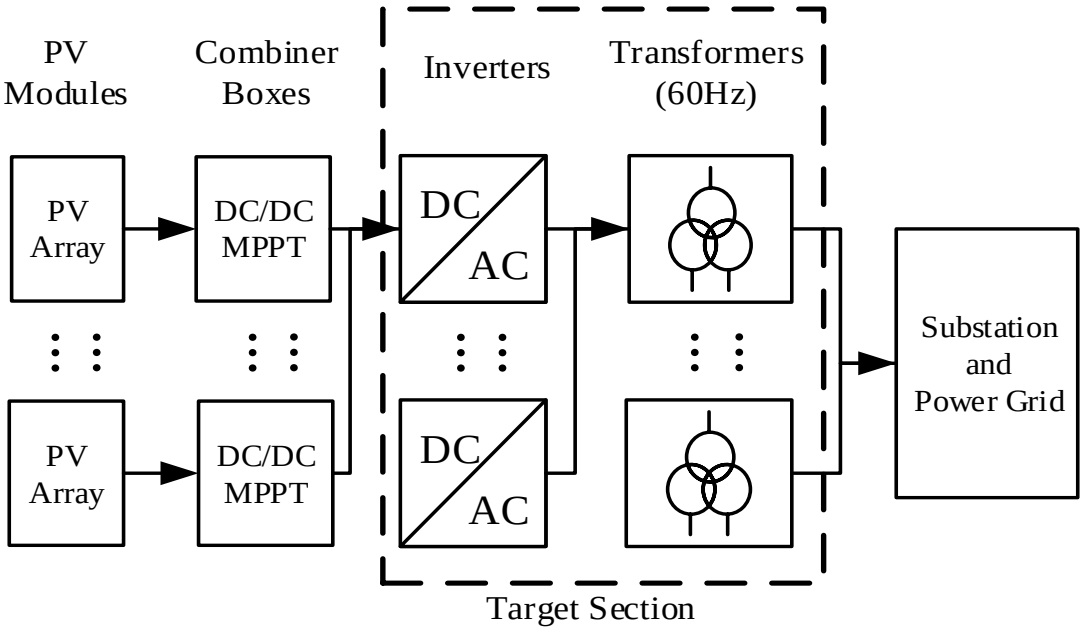


Figure 1.1: Typical PV power plant layout.

1.2 Prior art

With the increased popularity of PV power plants, many solutions for a grid interface converter have been proposed. The most common improvement is the use of HFTs to replace the line-frequency transformer. One example is to add a HFT to step up the DC link voltage to a HVDC link, but keeping a conventional DC/AC inverter topology [11]. While this approach takes advantage of the benefits of an HFT, it still suffers from harmonic distortion due to the use of two level inverters.

An ideal grid-interfaced inverter would produce a sinusoidal output voltage. However, these inverters use pulsed square voltages to synthesize the desired sinewave, resulting in unwanted harmonics. While the nature of switching converters producing square-wave voltages is unavoidable, techniques to minimize the production of unwanted harmonics are well known. If multiple cascaded square voltages are used to approximate a

sinusoidal voltage, the unwanted harmonics can be greatly reduced, such inverters are known as multilevel inverters. Depending on the number of levels, a multilevel inverter can improve the total harmonic distortion (THD) to the point where either no output filter or only a small output filter is needed. One example is a modified cascaded multilevel inverter proposed for PV applications in Europe [12]. While a 4 kV flying capacitor and series connected H-bridge [13] are finding applications in PV power plants. Another multilevel converter that can be found in PV applications is the active-clamp inverter [14]. While multilevel inverters can offer a great improvement in THD, they all suffer in terms of design, flexibility, and complex operation requirements.

A modular multilevel converter is based on the same principle of increasing the number of levels in the output to reduce the THD. As made apparent by their name, these topologies are built from cascaded "modular" circuits that are composed of lower rated components. MMC topologies offer many advantages over the non-modular variety: the system is more flexible, reliable, and repair times can be greatly reduced by having spare modules. These advantages have prompted many researchers to study MMCs over the past years [15], [16]. Different configurations of sub-modules have been proposed for different applications [17], most of them targeting HVDC lines. MMCs typically require voltage balancing to keep every sub-module at the same level [18]. For example, a modulation strategy that distributes the load of each sub-module evenly is a popular way to balance capacitor voltages (e.g. [19], [20]). If an HVDC MMC doesn't have balanced capacitors, a voltage difference between top and bottom arm leads to circulating currents [21].

The use of MMCs can also be seen in wind energy and some of these converters can be applied to PV systems as well. One example is the hybrid MMC [22], where a 7-level converter is proposed to interface to the grid. Another, more exotic example can be found in [23] where the generator coils are connected to each sub-module. The high-frequency magnetic-link medium-voltage converter for wind generation systems found in [24] offers modular inverter that can achieve high power density.

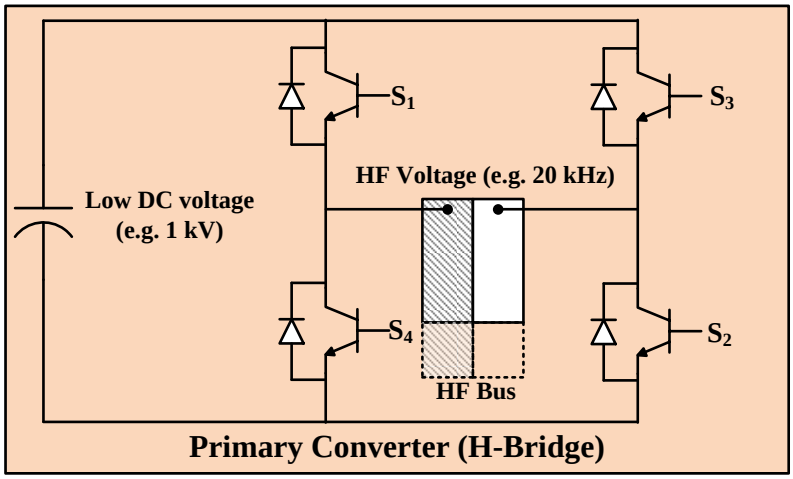
Different MMC topologies have also been proposed to act as inverters for PV systems. When different PV modules (or PV zones) are connected into different HFTs, the output

can be combined and higher voltages can be achieved [25]. Another topology that follows a similar approach is the cascaded Quasi-Z source inverter, where each PV module energizes a sub-module [26]. However, in order to achieve high voltages, numerous PV modules need to be connected in series, resulting in a system that is very susceptible to shading.

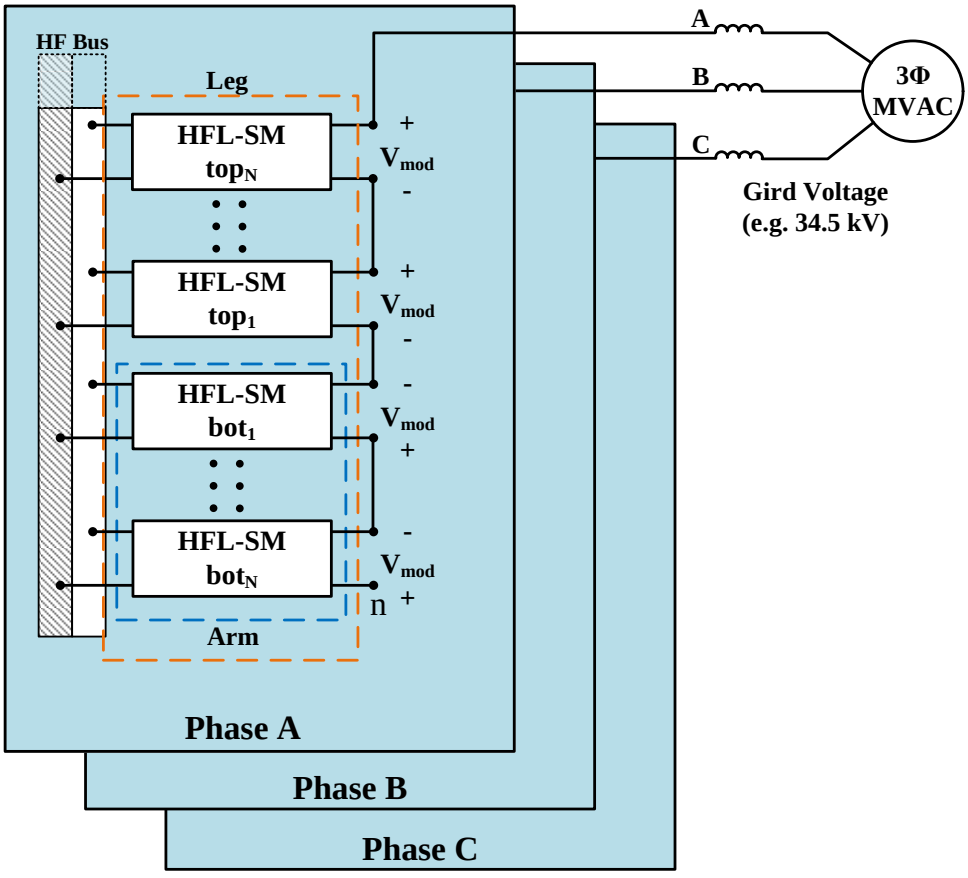
Yet another approach uses a multi-winding HFT, where multiple secondary coils are cascaded in an MMC fashion to synthesize the grid voltage as seen in [27] and [28]. While this approach offers several advantages, it suffers from the critical disadvantage of the transformer not being modular and hard to scale up. As seen in [29], the HFT design is more complicated and the number of sub-modules is limited by the number of secondary coils that can physically fit in the core.

1.3 Proposed Grid-tie inverter

A novel configuration of a MMC for a PV power plant application is proposed in this dissertation. The proposed topology has a primary converter that is electrically connected to every sub-module. Each sub-module is composed of a HFT, diode rectifier, and a conventional sub-module (e.g. half-bridge, full-bridge). Simulation results for the proposed topology have been presented in [1]. Some of the key advantages of this new topology include: a reduction in the system size and weight compared to the use of line-frequency transformers, reduced THD by having a high number of levels, eliminating the need for capacitor voltage balancing, a low input DC voltage with medium to high output AC voltage, and zero-current and zero-voltage switching in the primary inverter due to 50% duty cycle operation (also known as soft switching).



(a)



(b)

Figure 1.2: (a) Primary Converter, single H-Bridge inverter with DC input and HF square voltage output. (b) Multiple HFL-SM arranged into a 3 phase MMC.

1.3.1 **Primary Inverter (H-bridge inverter)**

The primary inverter is shown in Figure 1.2(a). The input of this inverter is a DC voltage source of around 1kV, depending on the application. The input source can also be a rectified voltage from a wind turbine or the output of a DC-DC converter. The output is a two-level square voltage with 50% duty ratio at a frequency in the range of 10 kHz-20 kHz. The duty ratio is defined in (1).

$$\text{Duty ratio [\%]} = \frac{t_{S_1,S_2}}{t_{S_1,S_2}+t_{S_3,S_4}} * 100 \qquad (1.1)$$

where t_{S_1,S_2} is the time both switch 1 and 2 are conducting in one switching cycle. Because the duty ratio is 50%, zero-voltage and zero current switching can be achieved. This can greatly improve the efficiency and, since the full power of the system goes through this inverter, is highly recommended [30]. Notice that these are the only four switches that need to be rated for the full power of the converter, whereas the sub-module switches are of lower power rating. IGBTs are already commercially available for applications of over 1 MW. For higher power levels, multiple switches can be combined or multiple H-bridges can be paralleled, however each approach presents its own challenges. Multi-switch devices need to be carefully designed so that the gate signals are applied simultaneously, which requires careful layout consideration. Paralleling multiple H-bridge converters could suffer from circulating current if there is an output voltage difference between different primary converters. With great care in the timing of the PWM signals, this effect can be mitigated, but not completely removed. Another solution would be to decouple the multiple H-bridge converter (i.e. one converter powers half of the sub-modules while another powers the other half); however, this approach requires more capacitors in the "Low DC voltage" link due to the instantaneous power not being constant. Therefore, if the power requirements can be met by a single primary converter, all of the previously mention challenges can be avoided.

1.3.2 **High Frequency Link Sub-module (HFL-SM)**

Every high frequency link sub-module (HFL-SM) connects to the primary inverter output via a high frequency bus bar as shown in Figure 1.2(b). A single HFL-SM is shown in Figure 1.3 and Figure 1.4. Notice that each HFL-SM has its own high frequency transformer. A topology in [27] uses a single transformer that serves as the high frequency link. Compared to [27], the proposed system offers a modular solution that can be scaled up with ease, as every additional sub-module needs to be connected to a bus rather than wrapped into a main transformer. During normal operation, the capacitor is constantly charged via the transformer and the diode bridge rectifier. This removes the need to balance the capacitors voltages and eliminates many of the complicated algorithms and voltage sensors typically associated with MMC balancing. The output of an HFL-SM is marked as "V_{mod}" in Figure 1.3. This voltage is controlled by IGBTs and can be either V_C or zero. This is known as a half-bridge sub-module; other configurations like the full-bridge shown in Figure 1.4 are also viable. A full-bridge sub-module can provide the additional level of ($-V_C$). The switching frequency of a HFL-SM depends on the number of sub-modules used, but it could be as low as 60Hz for a high number of sub-modules. For a 9 level converter, the switching frequency can be at least an order of magnitude smaller than the primary side (around 1 kHz to 2 kHz).

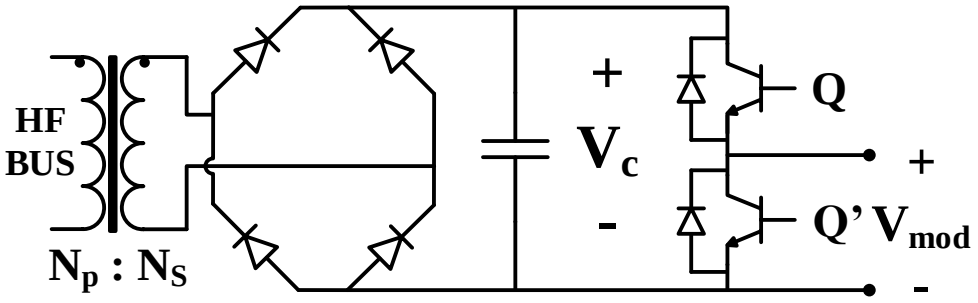


Figure 1.3: High Frequency Link Sub-module (HFL-SM) with Half-Bridge.

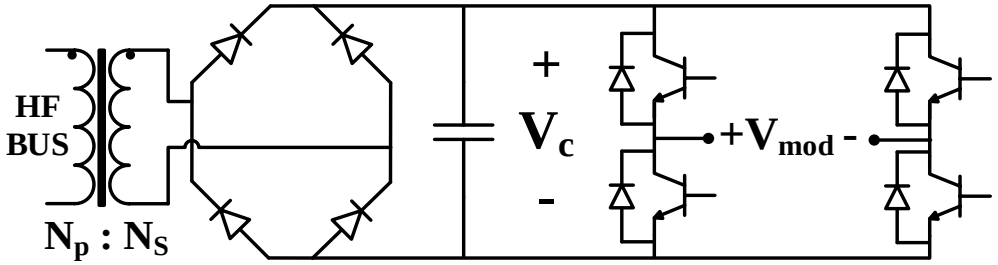


Figure 1.4: High Frequency Link Sub-module (HFL-SM) with Full-Bridge

1.3.3 **Modular Multilevel Arrangement**

Multiple HFL-SMs are connected in series. Each module provides additional voltage levels and the module levels for a half-bridge sub-module are presented in Table 1.1. An equation that dictates how many sub-modules are needed to achieve a desired number of voltage levels in the output can also be defined. Using the half-bridged sub-module, (1.2) defines the quantity required per phase for an n-level converter as

$$N_{SM} = (n_{level} - 1)\ [Sub\ Modules/Phase] \qquad (1.2)$$

Table 1.1: Half-Bridge HFL-SM Output Voltage

$[\boldsymbol{Q}, \boldsymbol{Q'}]$	$\boldsymbol{V_{mod}}$
[1 , 0]	V_C
[0 , 1]	$zero$

In Figure 1.2(b) an arrangement of half-bridge HFL-SMs for a three phase inverter is shown. The half-bridge HFL-SMs are connected in series to form an “arm”. A phase has two arms connected in series to form a “leg”; one arm provides the positive voltage levels, whereas the other provides the negative voltage levels. Notice that the HFL-SMs on the negative arm are identical to the ones in the positive arm, only the output terminals are inverted. A total of 3 legs are needed to form a 3-phase inverter. Compared to an HVDC MMC, the line connection is not where the positive and negative arm meet, instead it is at the end of each leg. There is also no need for arm inductances to limit fault currents due to the galvanic isolation between the grid and DC source. Each leg can provide a magnitude and frequency independent voltage that can be used to control the real and reactive power flow of the inverter to the grid. The output voltage can be designed to be anything from low to medium voltages (e.g. 600 V – 69 kV) depending on the number of levels, the input voltage, and the transformers turn ratio.

Increasing the number of levels increases the performance (e.g. voltage and current THD) and decreases the rating specifications for each sub-module. For a grid tied application it’s desired to select enough modules such that power quality is sufficient with a small or no output filter.

Chapter 2

2 OPERATION PRINCIPLES OF PROPOSED TOPOLOGY

A brief introduction of the proposed topology has been presented in the previous chapter; this chapter presents a more in-depth description on some of the operational aspects of the proposed converter.

2.1 First Stage

The proposed topology can be more easily explained in two stages: the first stage is a combination of the H-bridge primary converter, and a sub-module HF transformer, diode bridge stage and capacitor. Figure 2.1 describes the first stage for a single sub-module; the high frequency bus bar has been represented as an R-L element for this analysis.

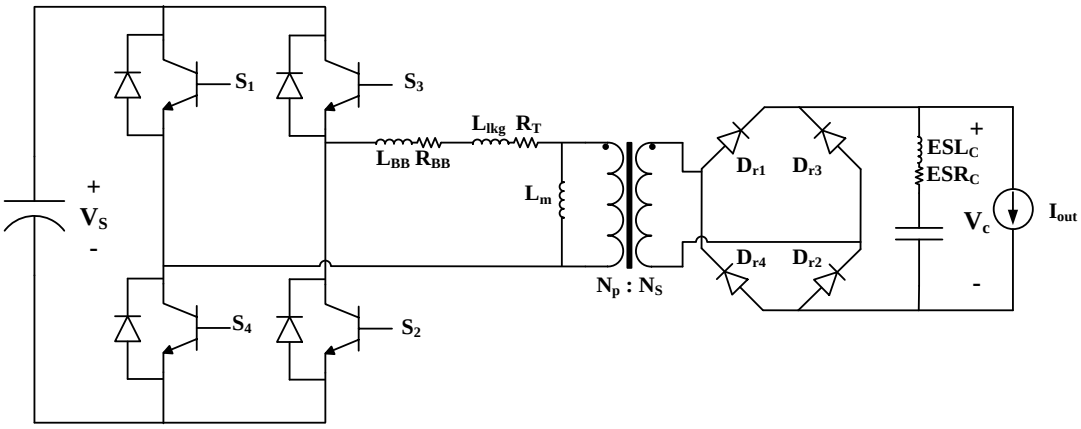


Figure 2.1: Proposed topolgy first stage conversion.

2.1.1 High Frequency Transformer Operation

In order to simplify the model, the first step taken is to set some operational boundaries. For the converter to work as desired it is necessary to have a voltage induced in the

secondary coil of the sub-module. According to Faraday's law (2.1), the voltage induced on each of the turns in the secondary coil is dependent on the changing flux.

$$V_{turn}(t) = \frac{d\Phi(t)}{dt} \tag{2.1}$$

where V_{turn} is the voltage induced on a single turn of a coil, and Φ is the flux passing through the interior of the coil.

In order to have a voltage at the secondary, a changing flux needs to be induced somehow. The primary and secondary coils are wrapped around the same core and the same flux is linking the two coils, therefore this flux can be induced by applying a voltage on the primary coil. If this voltage applied is constant, the flux will increase and eventually saturate, and once it does, there will no longer be a change in flux and the voltage across the secondary coil will decay. However, by reversing the voltage polarity on the primary, the flux change can be reversed and kept in constant change. The need of an alternating voltage sets the operational boundary of the primary H-bridge converter. The resulting voltage across the secondary will also be alternating due to the change in flux being both positive and negative. For the topology to work, it is desired to have a constant positive voltage, thus a diode bride was used to rectify the secondary voltage. With these constrains in place, the model for the first stage can be simplify to be as shown in Figure 2.2.

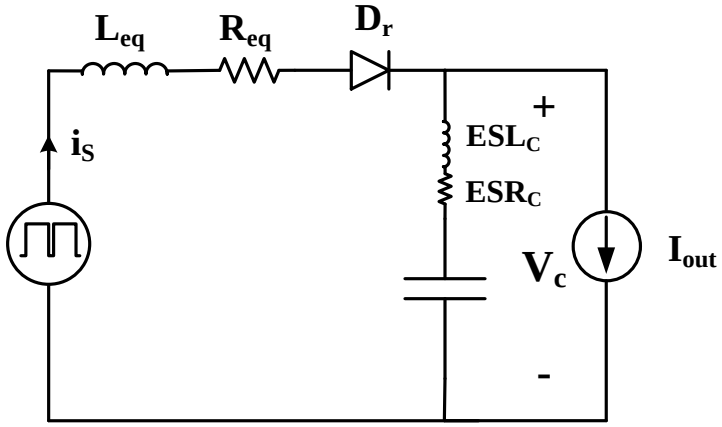


Figure 2.2: Simplify model of first stage conversion.

2.1.2 **Transient Response of Primary Stage**

Using the simplified model in Figure 2.2 we can derive a set of equations that can describe the transient response. The equivalent resistance is in the model refers to (2.2),

$$R_{eq} = 2Rs_{ON} + R_{BB} + R_T + 2Rd_{ON} + R_{misc} \tag{2.2}$$

where Rs_{ON} is the H-bridge ON resistance, R_{BB} is the bus bar resistance, R_T is the transformer equivalent resistance, Rd_{ON} is the diode ON resistance, and R_{misc} includes other non-accounted resistances (e.g. source resistance and trace resistance). Also included in the diagram is the capacitor equivalent series resistance "ESR" and inductance "ESL". The equivalent inductance is the sum of the following,

$$Leq = L_{BB} + L_{lkg} + L_{misc} \tag{2.3}$$

where L_{BB} is the bus bar inductance, L_{lkg} is the transformer leakage inductance, and L_{misc} are other non-accounted for inductances. The transient response to a voltage step can be model by a simple RLC with diode where a KVL loop yields (2.4) -(2.6),

$$V_S = R_{eq} i_s + L_{eq} \frac{di_s}{dt} + \frac{1}{C} \int i_s dt + V_c(0) \tag{2.4}$$

$$L_{eq} \frac{di_s^2}{dt^2} + R_{eq} \frac{di_s}{dt} + \frac{1}{C} i_s = 0 \tag{2.5}$$

$$\frac{di_s^2}{dt^2} + \frac{R_{eq}}{L_{eq}} \frac{di_s}{dt} + \frac{i_s}{L_{eq} C} = 0 \tag{2.6}$$

where V_S is the equivalent source voltage, i_s is the secondary current after the diode, C is the capacitance of the sub-module's capacitor, and $V_C(0)$ is the initial capacitor voltage.

The characteristic equation (2.7) can be found by applying a Laplace transformation,

$$S^2 + \frac{R_{eq}}{L_{eq}}S + \frac{1}{L_{eq}C} = 0$$

$$\alpha = \frac{R_{eq}}{2L_{eq}}$$

$$\omega_0 = \frac{1}{\sqrt{L_{eq}C}}$$

$$S_{1,2} = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2} \tag{2.7}$$

where α is the damping factor, ω_0 is the natural resonant frequency, and $S_{1,2}$ are the poles of the system.

The first thing we can identify is that in order to avoid "ringing" at the secondary side voltage, the system needs to be either critically damped or preferably slightly overdamped. In order to have an overdamped system the damping factor must be greater than the natural resonant frequency,

$$\alpha \geq \omega_0 \quad (overdamped)$$

$$\frac{R_{eq}}{2L_{eq}} \geq \frac{1}{\sqrt{L_{eq}C}}$$

$$\frac{R_{eq}\sqrt{C}}{2\sqrt{L_{eq}}} \geq 1 \tag{2.8}$$

As seen on by (2.8) this can be accomplish by various ways, however there is only one practical way. Increasing R_{eq} will of course have a negative impact on the efficiency, and as we will see later, increasing C can be costly. Therefore, reducing the equivalent inductance is the best alternative to guarantee the secondary voltage is well behaved. From (2.7) we know that a stable system is possible as both poles will be real, different and strictly on the left hand plane. It can be found that due to a relatively high capacitance, the leakage inductance is realizable and it can be large enough for a ZVS that will be discuss ahead.

2.1.3 **Steady State Operation of Primary Stage**

From the previous analysis it is clear that one of the design considerations for a well behaved system is to have a relatively small leakage inductance and bus bar inductance. As for the steady state analysis we will define the output capacitor voltage as V_C, the input voltage as V_{in}, the transformer turns ratio N_2/N_1, and the effective duty cycle d_{eff}. The equivalent function of the primary stage is that of a "Phase-Shifted Full-Bridge Converter" that has been well study and described in [34]-[37]. The transfer function for the output capacitor voltage is,

$$V_C = \frac{N_2}{N_1}\, d_{eff}\, V_{in} \tag{2.9}$$

The effective duty cycle is calculated as follow,

$$d_{eff} = \frac{t_{1,2}+t_{3,4}}{T_s} \tag{2.10}$$

where the time $t_{1,2}$ and $t_{3,4}$ are the times each pair of switches are conducting together.

2.1.4 **Zero Voltage Switching of Primary H-bridge Converter**

It is clear that Zero Voltage Switching (ZVS) has its merits as long as it can be implemented effectively. Eliminating the switching losses improves the overall converter efficiency, allows faster switching frequency operation, and simplifies the heatsink design.

As mentioned before the first stage of the proposed topology is similar in operation to a Full-Bridge converter. It is well known that a Full-Bridge converter can operate with ZVS; this particular arrangement is known as a "Phase-Shifted Full-Bridge Converter" [38]. If designed correctly, the proposed topology can be capable of a resonant tank similar to that of the Phase Shifted Full-Bridge. Figure # shows the configuration of the first stage, as mentioned in the previous sub-section, the equivalent leakage inductance is the sum of the components described in (2.3).

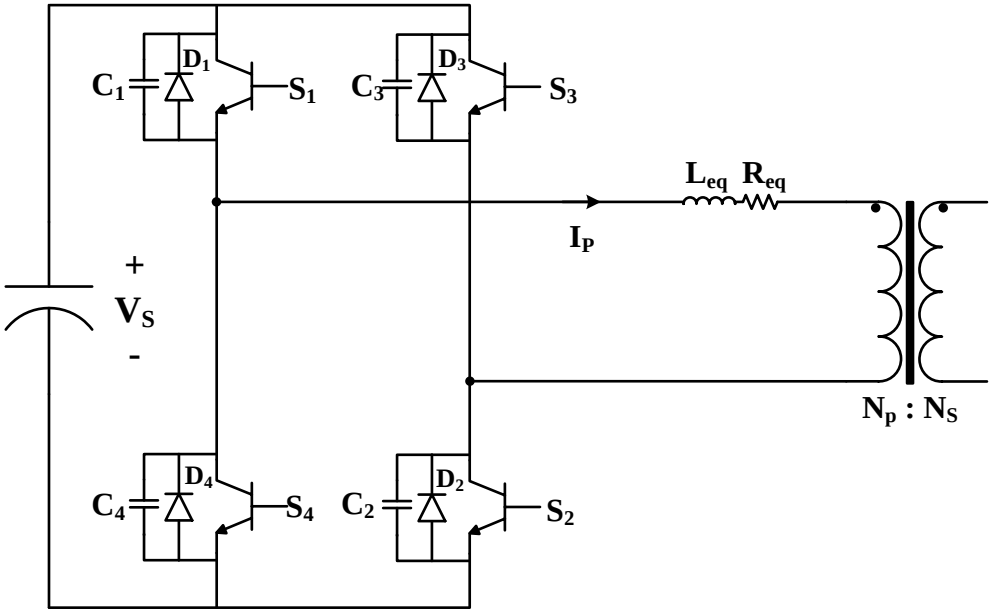


Figure 2.3: H-Bridge model for ZVS analysis.

The operation of this first stage involves applying an alternating voltage to the primary coil, therefore the power delivery states are when S_1/S_2 switch ON together or when S_3/S_4 switch ON together. ZVS will be achieved when moving from one of these states to the other. Instead of just each pair switching at the same time ZCS is achieved by adding a delay between the turn on time of S_1 and S_2 or for the other half of the cycle S_3 and S_4. The delay will depend on various parameters that will be explain in more details later on, but the resulting effect will be an apparent phase shift between S_1 and S_2, and between S_3 and S_4. A detail description of the transition from state S1/S2 to S3/S4 is presented in the following figures, the reversed transition will be similar thus it won't be discussed.

Initially the current $I_P(t_0)$ is flowing from the input, through S1, through the equivalent transformer primary, out to S2, and back to the source. At the same time a current is being induced on the secondary winding and power is being transferred.

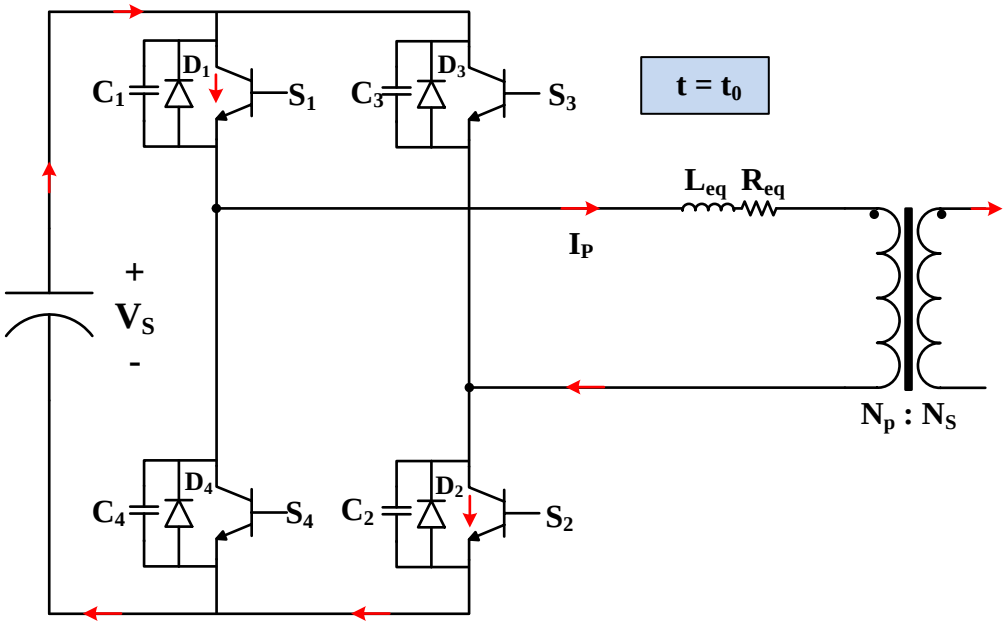


Figure 2.4: H-Bridge model for ZVS analysis ($t = t_0$).

The time t_1 marks the moment it is desired to start transition; at this moment S_2 is turned off. As a result of the switch not conducting anymore, the primary current now flows through the output capacitors C_2 and C_3. As the current passes though C_2 the capacitor is charge, and as is passes though C_3 the capacitor being discharged. Eventually the C_2 reaches the value of V_{DC} and C_3 drops to zero. As soon as this happened D_3 is now conducting all of the primary current and the S_3 is ready for a ZVS. It is now that we provide the signal to switch S3 ON, at this moment the primary current $I_P(t_1)$ is not much different from $I_P(t_0)$, as the equivalent inductance is large enough to keep the current constant during this short amount of time. During this state the top two devices S_1/S_3 are conducting, and the voltage across the transformer is zero, meaning that there is no power transfer occurring. It is important to point out that the time it takes to reach the state where S3 can be turn on depends on various factors (i.e. L_{eq}, $I_P(t_0)$, C_2, and C_3).

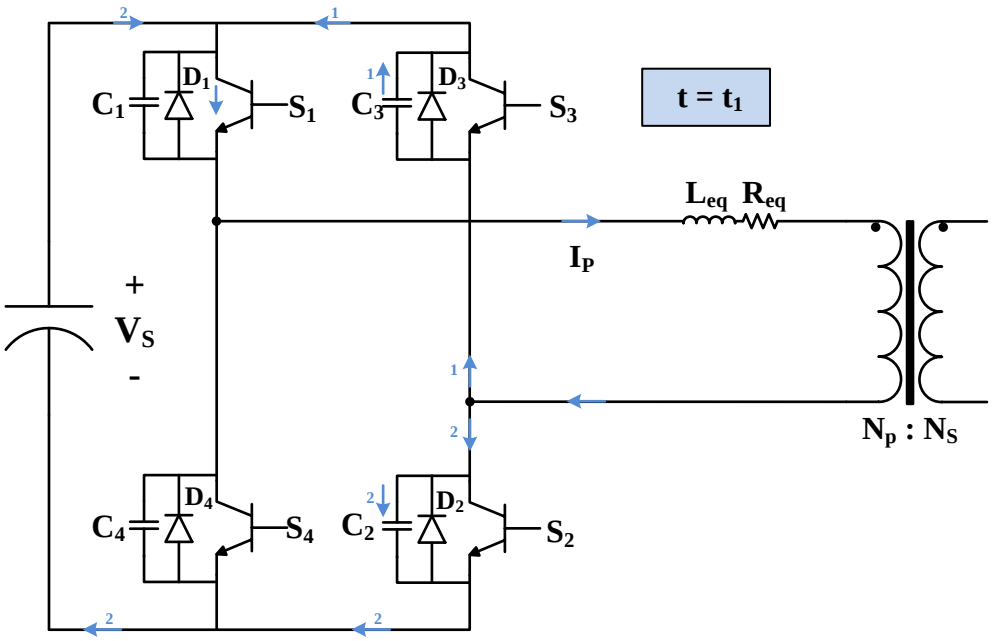


Figure 2.5: H-Bridge model for ZVS analysis ($t = t_1$).

As the current freewheels through the upper two devices, losses on the circuit cause the current to decay slowly. At time t_2 the switch S_1 will be turned off, beginning the transition between S_1 and S_4. Similarly to the previous transition the primary current $I_P(t_2)$, now lower in magnitude, goes from flowing through S_1 to now flowing through C_1 and C_4. The voltage across C_1 rises from zero to V_{DC}, whereas the voltage across C_4 drops from V_{DC} to zero. Even if the devices are identical to the previous transition, this one will take slightly more, as the commutating primary current $I_P(t_2)$ is smaller. After the switches capacitor voltages have been reveres the primary current is now flowing through the D_4 and the voltage across S_4 is now ready for a ZVS. Once the switching signal is applied to S_4, the device will start conducting and a reverse polarity voltage will be applied at the primary coil. At this moment power will start flowing again through the circuit and the transition from S_1/S_2 to S_3/S_4 has been completed.

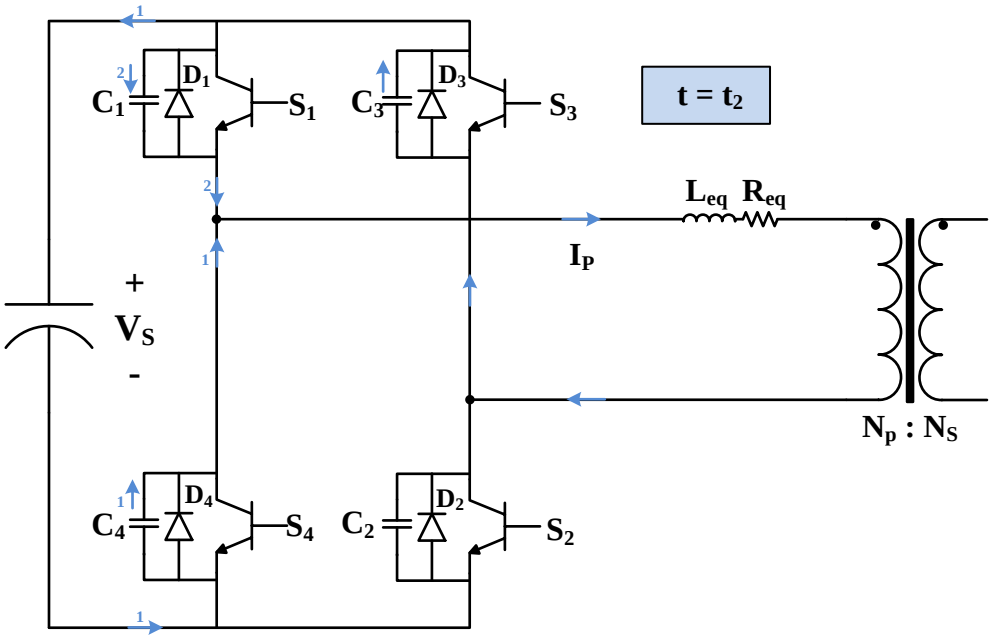


Figure 2.6: H-Bridge model for ZVS analysis ($t = t_2$).

Some assumption were made in this analysis, the first is that the primary current is constant. In reality the primary current during the commutation cycle will be the sum of both the initial primary current and a resonant current, however the resonant current is much smaller in magnitude when compared to the initial primary current. As long as we can guaranteed this the analysis can be simplify with this assumption. In the proposed topology because we use a single primary converter to power all three phases the primary current is a DC value, and it is of course larger in magnitude when compare to the resonant current. This will not always be the case in topologies that use an individual H-Bridge for each module, as the primary current will be sinusoidal.

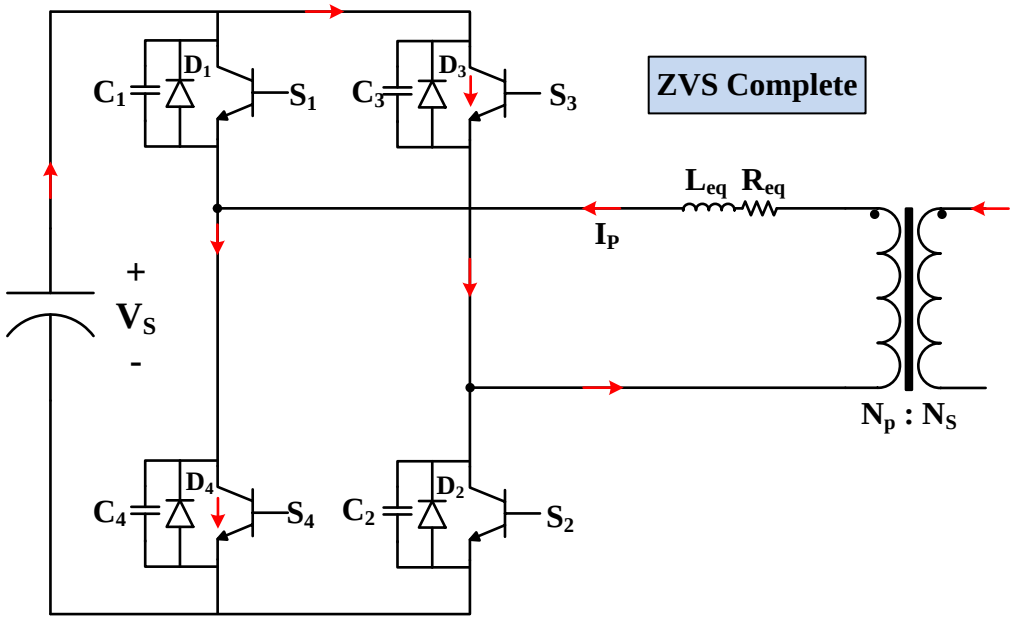


Figure 2.7: H-Bridge model for ZVS analysis (transfer completed).

2.2 Second Stage

The second stage of the proposed converter is a half-bridge cell MMC as shown in Figure 2.8, a single cell is used for every sub-module and multiple sub-modules are used to create three phase inverter.

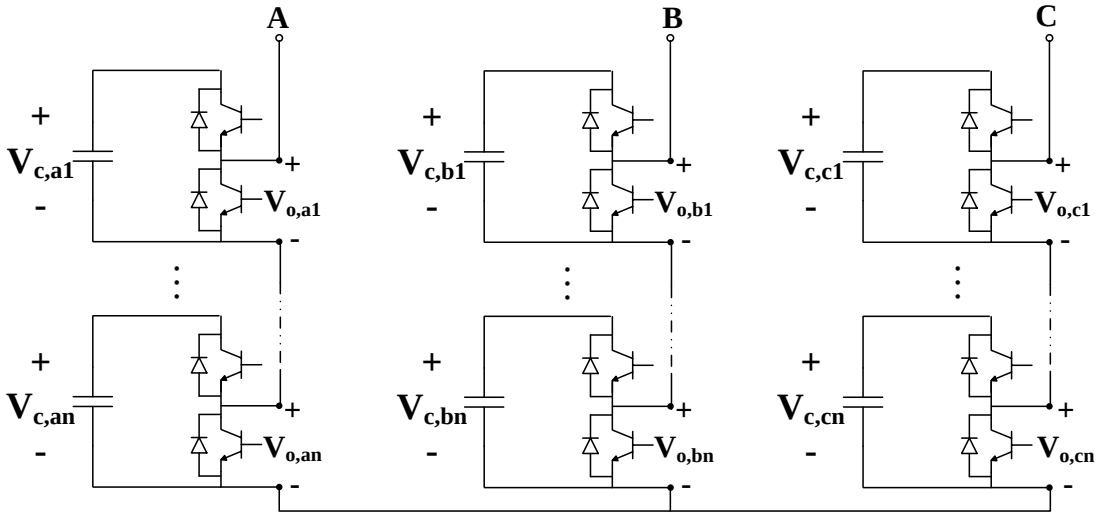


Figure 2.8: Second Stage Structure

2.2.1 **Switching State Transitions in Secondary Stage**

One of the advantages of the proposed topology is that part of the analysis of primary and secondary stage can be done independently. The switching state analysis of the secondary state doesn't depend on the transients in the primary state. For simplification purposes we can assume the sub-module's capacitance behaves as a voltage source. A single sub module second stage cell is presented in Figure 2.9. The output voltage V_O is dependent on the state of the switches Q and Q', and on the output current direction. Table 2.1 summarizes all of the possible states.

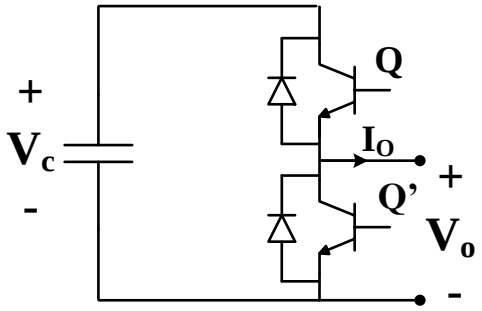


Figure 2.9: Second Stage Half-Bridge Cell

Table 2.1: Half-Bridge Cell States of Operation

State	$[\,Q\,,Q'\,]$	V_O
S1	[0 , 0]	$0^* \,/\, V_C^*$
S2	[0 , 1]	0
S3	[1 , 0]	V_C
S4	[1 , 1]	X

*: $+I_O \,/\, -I_O$

As we can see in Table 2.1, out of the four states the last is an undesirable state because it will create a short circuit for the module capacitor. This state should be avoided during operation and it is unusable. The first state is also an undesirable state because the output voltage is controlled by the current direction. However this state serves as a good transition state between states 2 and 3, but time spent on this state should be minimizes as the uncontrolled output voltages hinders our ability to control the overall

all leg voltage. States 2 and 3 will be the main operating states, on both states the output voltage can be controlled regardless of the current direction.

As mentioned before transitions between states 2 and 3 will be done through state 1, Figure 2.10 shows a state diagram that describes this behavior. Notice that there is no direct path between state 2 and 3 for safety reasons, this is because if the switching signals do not arrive at the exact time there is a possibility the system can end in state 4. When the system is on state 2 and receives a signal to turn the module ON it immediately moves to state 1. The time spent on state 1 during a transition should be controlled to allow proper turn off the semiconductor in use. Therefore, as soon as state 1 is active a timer start to count towards a pre-determined dead time value "t_d" and when it is reached it moves to state 3. The reverse transition is similar, as soon as the BYEPASS signal arrives the system moves to state 1 and after t_d it moves to state 2.

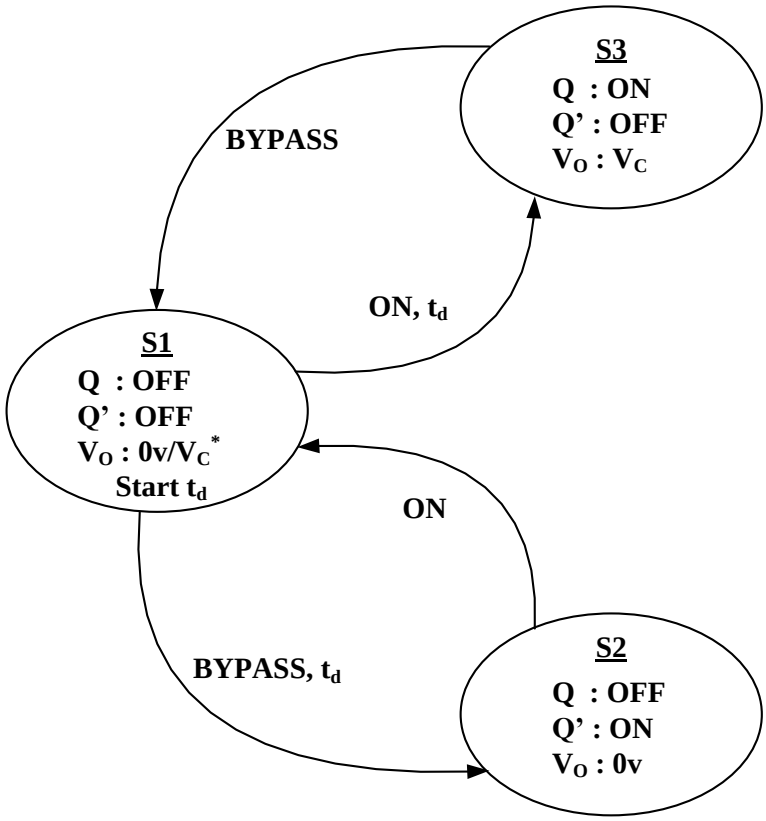


Figure 2.10: Half-Bridge Cell Operational State Flow

The losses associated with each transition are described in Figure 2.11(a) and (b). If the current is positive (as described in Figure 2.11.a) the module voltage and current are the same in state 1 and 2, except for the current flow inside the semiconductor used. If the transistor allows for bi-directional current flow then the current will be in the transistor instead of the diode. Regardless, a transition between states 1 and 2 will be a ZVS and there will be no switching losses at that moment. When changing from state 1 to state 3, Q will have turn ON losses dependent on the output capacitance of the device used. The reverse transition will incur in turn OFF switching losses for the top device as well.

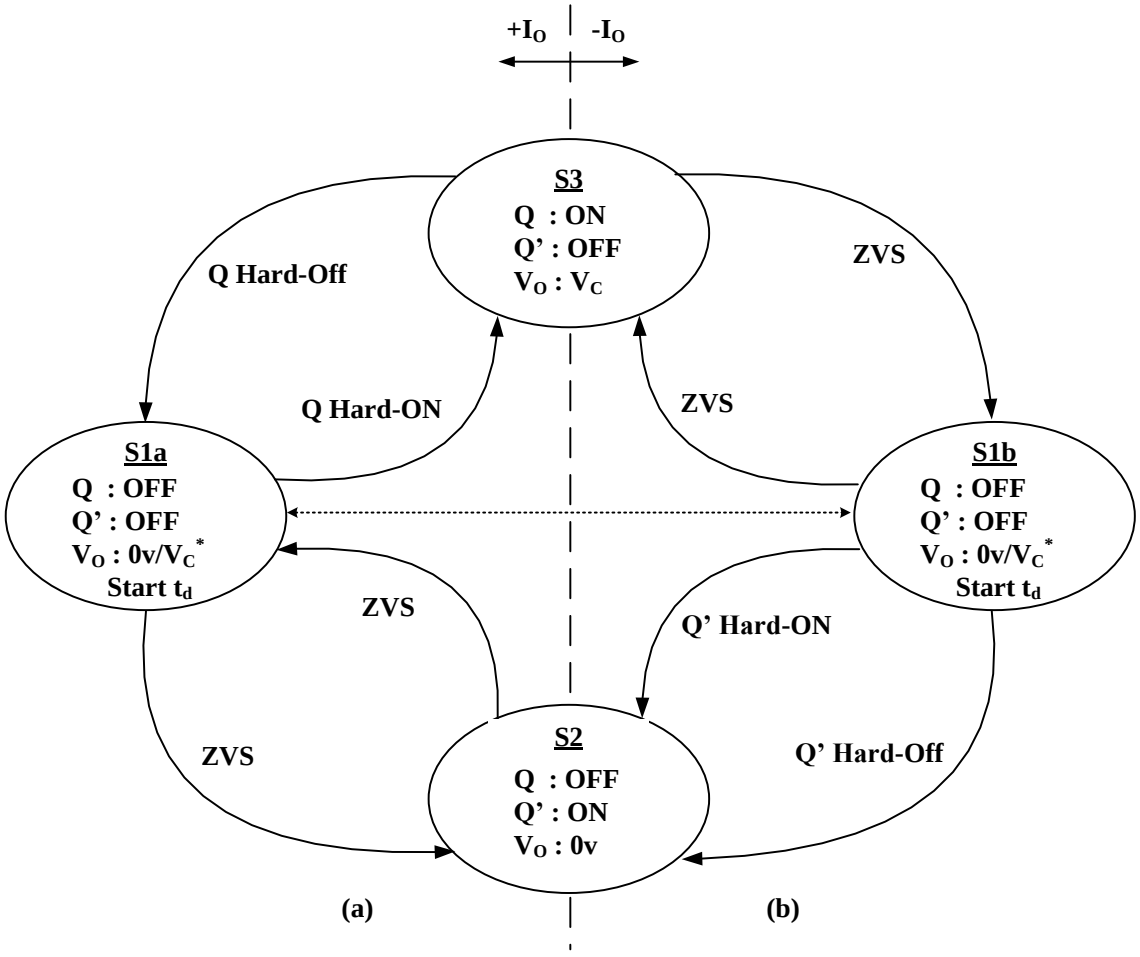


Figure 2.11: Half-Bridge Cell Operational State Flow With Switching Behavior For Positive Current (a) and Negative Current (b)

The reverse behavior can be seen when the current is negative (Figure 2.11.b), but instead of the losses being on the top device they will be on the bottom device. The proposed operation will only use the transitions for the negative current when the inverter voltage and current are out of phase (i.e. when reactive power need to be deliver to the gird). If the inverter only needs to be operated with unity power factor we can then notice that during positive current all of the switching losses will be on the top device, this is of course not ideal when using the same device for both top and bottom switch. If discrete devices are used, then selecting a device with fewer switching losses for the top switch only (e.g. SiC MOSFET) will improve the efficiency.

2.2.2 **Capacitor Balancing**

One of the most important claims of the proposed topology is that it removes the need of an active capacitor balancing scheme. In a typical MMC the capacitor voltage of each module will fluctuate depending on the capacitance of that module, the current level at the time and how long the module was ON. As different ripple voltages are seen by different modules, so does the average voltage of the capacitor change over time if no action is taken to keep them balanced. There are modulation scheme that attempt to use modules equally over a line cycle in order to moderate the unbalance, however these can't take into account the difference in capacitance between modules and a change in the load. On top of this the modulations needs to have additional switching of modules compared to a more simple modulation scheme, therefore resulting in higher switching losses. For more details on the different types of modulation please refer to Chapter 3.

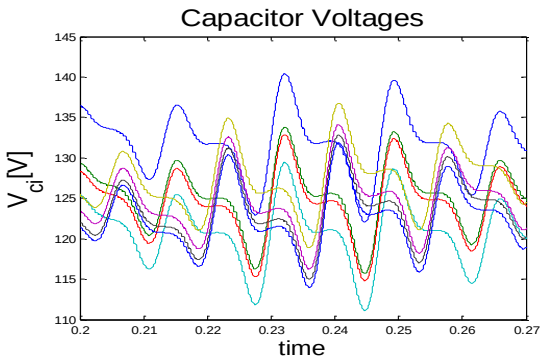


Figure 2.12: Capacitor voltage unbalance of a Typical MMC

Figure 2.12 shows how the capacitor voltages can get unbalances as time passes if there is no active control balancing the capacitors. In order to balance the capacitor voltages the sub-modules have to be switch in and out depending on their current charge state. Shown in FIGURE G are the Discharging/Charging states a module can be in depending on the switch state and current direction, and the states where the capacitor is unchanged. One of the most common strategies for voltage balancing is to use a phase shifted modulation as shown in Figure 2.13, along with the balancing algorithm shown in Figure 2.14. When one of the triangle carrier waveforms goes above the reference a module needs to be switched ON and when it goes below one of the modules needs to be bypassed. The blue and red carriers control the top arm, whereas the green and purple carriers control the bottom arm. Notice that all of the carriers are shifted so that their phases are spaced equally, with a top and bottom carrier alternating. The basic idea of the voltage balancing algorithm is to use the sub-module with the highest capacitor voltage when a sub-module needs to be switched on a discharging state, and use the sub-module with the lowest capacitor voltage when a charging state is to happen. A state flow diagram of the algorithm is shown in Figure 2.14. The arm current is then measured to know if the MMC is on a charging state or discharging state and every sub-module voltage needs to be measured to determine which has the lower/highest voltage. Using the measured information and the state flow, we can determine which module needs to be bypass or connected [39].

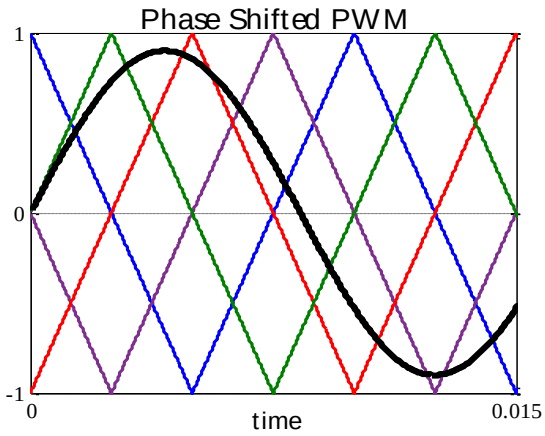


Figure 2.13: Phase Shifted Modulation for a 5-Level of a Typical MMC.

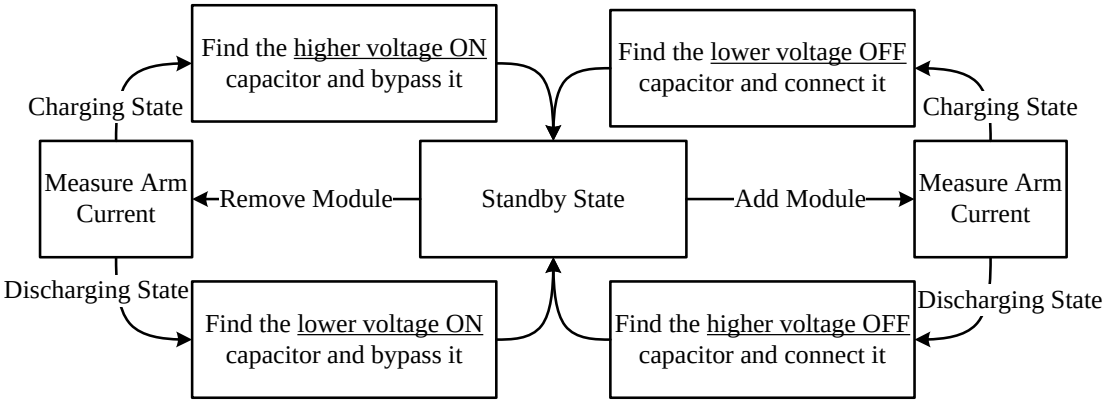


Figure 2.14: Voltage Balancing Algorithm of a Typical MMC.

As we see this process is complicated, requires the sensing and processing of many values, and incurs in additional unnecessary switching. With the proposed topology we can use a simpler modulation scheme and no capacitor voltage sensing is required.

2.2.3 **Full-Bridge Secondary Stage (Alternative Secondary Stage)**

In the previous chapters the secondary stage was discussed, this secondary stage was composed of a half-bridge sub-module. This type of sub-module was selected because of its simplicity and it is consider the basic fundamental block of an MMC. The proposed topology can also be used with different types of secondary stages, the full-bridge sub-

module is one of them (show in Figure 2.15). Operation of this sub-module is similar in principle to what has been described above, the difference being that this module has an additional level ($-V_C$). Having this additional level means that one full-bridge sub-module is effectively equivalent to one positive arm and one negative arm sub-module. The number of switches doesn't change but the capacitor, transformer and rectifier stages involved with each submodule is reduced by half. This is of course very advantageous as the overall system can be made smaller, or additional levels can be achieved with the same number of sub-modules.

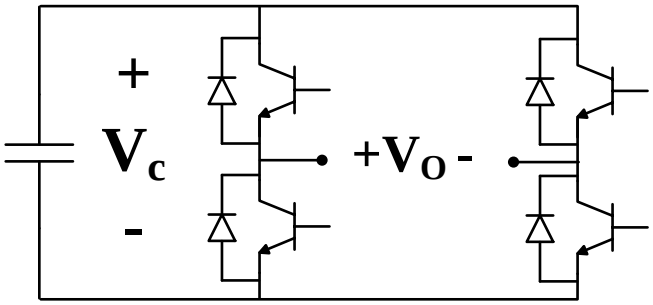


Figure 2.15: Full-Bridge Secondary Stage Cell

2.2.4 **Modular Multilevel Converter AC Voltage Synthesis**

The ideal model for the second stage is shown in Figure 2.16, each sub-module can be model as an ideal controlled voltage source and in case of the full-bridge sub-module it is capable of both positive and negative voltages. In this assumption each sub-module is capable of following a voltage reference between zero and V_C. Sub-modules on the same leg regulate their voltage as seen on Figure 2.17, such that the sum is equivalent to the desired reference ac voltage. The reference ac voltage will be determined by an active/reactive controller.

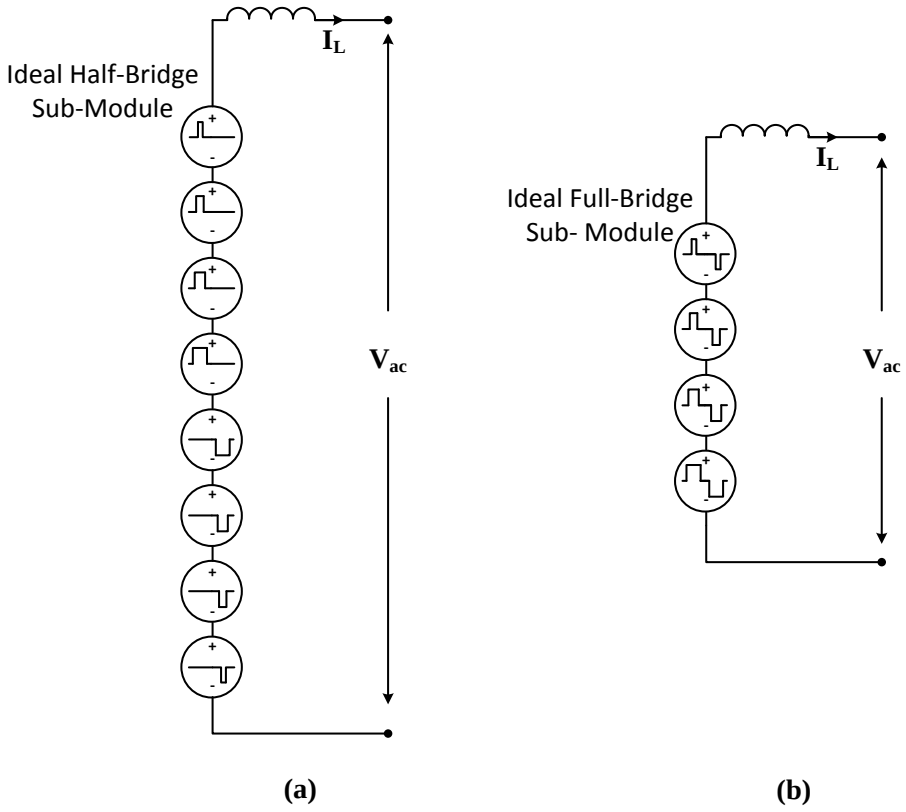


Figure 2.16: Ideal MMC Model

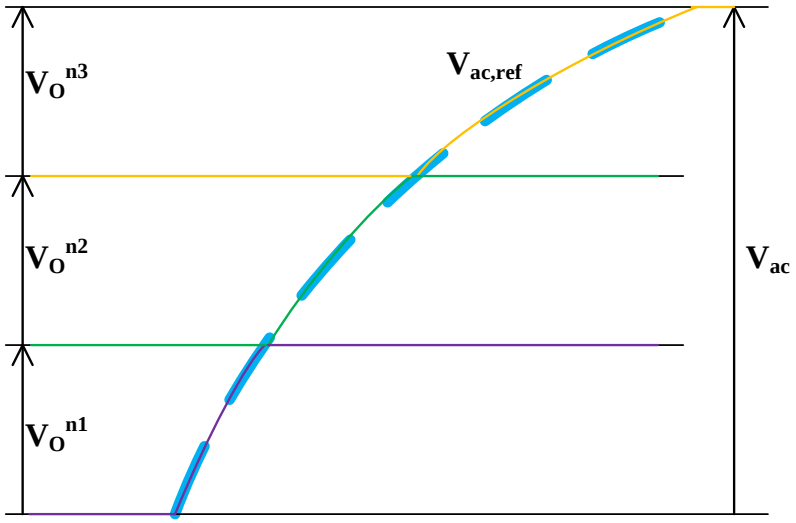


Figure 2.17: Output AC voltage composed of sum of regulated sub-module voltages

2.2.5 **Active and Reactive Power Control**

The proposed topology is a voltage source converter (VSC), therefore the ideal model of a grid interconnection is shown in Figure 2.18. The basic power flow equations are as follow;

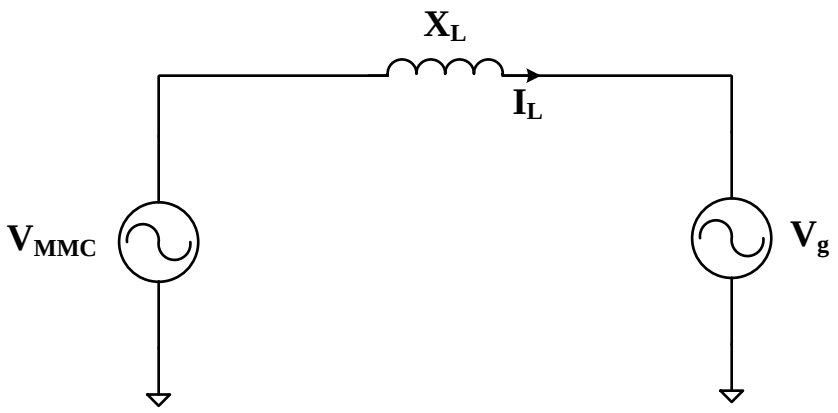


Figure 2.18: Grid Connected VSC

$$I_L = \frac{V_{MMC} - V_g \angle \alpha}{jX_L} \tag{2.11}$$

$$S_{MMC} = V_{MMC} I^* = V_{MMC} \left(\frac{V_{MMC} - V_g \angle \alpha}{-jX_L} \right) \tag{2.12}$$

$$P_{MMC} + j\, Q_{MMC} = \frac{V_{MMC} V_g \sin(\alpha)}{X_L} + \frac{V_{MMC}^2 - V_{MMC} V_G \cos(\alpha)}{-jX_L} \tag{2.13}$$

$$P_{MMC} = \frac{V_{MMC} V_g \sin(\alpha)}{X_L}, \quad Q_{MMC} = \frac{V_{MMC}^2 - V_{MMC} V_G \cos(\alpha)}{-jX_L} \tag{2.14}$$

$$V_{MMC} = \lambda\ V_g \tag{2.15}$$

$$P_{MMC} = \frac{\lambda V_G^2 \sin(\alpha)}{X_L}, \quad Q_{MMC} = \frac{V_g^2 \left(\lambda^2 - \lambda \cos(\alpha)\right)}{-jX_L} \tag{2.16}$$

where α is the phase between the grid and converter voltage, and λ is define as the ratio between the converter and grid voltage magnitude. As expected from a VSC it can be seen in (2.16) that the active and reactive power can be adjusted by controlling α and λ. In case of real power flow into the MMC, because the proposed topology is unidirectional it will cause the average voltage of the capacitors to increase. This mode of operation is not viable, and thus accurate and independent control of both active and reactive power is needed. It can also be seen that both powers depend on the grid side voltage and the line impedance, in order to independently control each quantity a close loop control is needed.

One of the most popular control techniques used is vector control, where the three phase voltages and currents are transformed using the Clark and Park transformation to be represented by only two vectors [#-#]. For the three phase voltages shown in (2.17) the Clark transformation is shown in (2.18).

$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_C \end{bmatrix} = \begin{bmatrix} V\cos(\theta) \\ V\cos(\theta - 120°) \\ V\cos(\theta + 120°) \end{bmatrix} \tag{2.17}$$

$$\underbrace{\frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}}_{Clack\ transformation} V_{abc} = \frac{2}{3}\begin{bmatrix} \frac{3}{2}V\cos(\theta) \\ \frac{3}{2}V\sin(\theta) \end{bmatrix} = V_{\alpha\beta} \tag{2.18}$$

$$\underbrace{\begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}}_{Park\ transformation} V_{\alpha\beta} = \begin{bmatrix} V \\ 0 \end{bmatrix} = V_{dq} \tag{2.19}$$

To go from the $\alpha\beta$ reference frame to the dq reference frame, Park's transformation is used as seen in (2.19). The system equation on (2.20) can be re-written as shown in (2.21). Using the transformations mentioned before, the system equation on (2.21) can be converted to the dq reference frame seen on (2.22).

$$L\begin{bmatrix}\frac{di_a}{dt}\\ \frac{di_b}{dt}\\ \frac{di_c}{dt}\end{bmatrix}=\begin{bmatrix}V_{MMC_a}\\ V_{MMC_B}\\ V_{MMC_C}\end{bmatrix}-\begin{bmatrix}V_{g_a}\\ V_{g_b}\\ V_{g_c}\end{bmatrix} \tag{2.20}$$

$$\begin{bmatrix}V_{MMC_a}\\ V_{MMC_B}\\ V_{MMC_C}\end{bmatrix}=L\begin{bmatrix}\frac{di_a}{dt}\\ \frac{di_b}{dt}\\ \frac{di_c}{dt}\end{bmatrix}+\begin{bmatrix}V_{g_a}\\ V_{g_b}\\ V_{g_c}\end{bmatrix} \tag{2.21}$$

$$\begin{bmatrix}V_{MMC_d}\\ V_{MMC_q}\end{bmatrix}=L\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}+L\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\begin{bmatrix}i_d\\ i_q\end{bmatrix}+\begin{bmatrix}V_{g_d}\\ V_{g_q}\end{bmatrix} \tag{2.22}$$

These equations can also include a line resistance model, these have been left out on this analysis. As we align the reference d-axis with the rotational phase a vector, V_{g_q} zero in steady state and we can derive the active and reactive power equations in (2.23).

$$P=\frac{3}{2}\,V_{g_d}\,i_d,\quad Q=-\frac{3}{2}\,V_{g_d}\,i_q \tag{2.23}$$

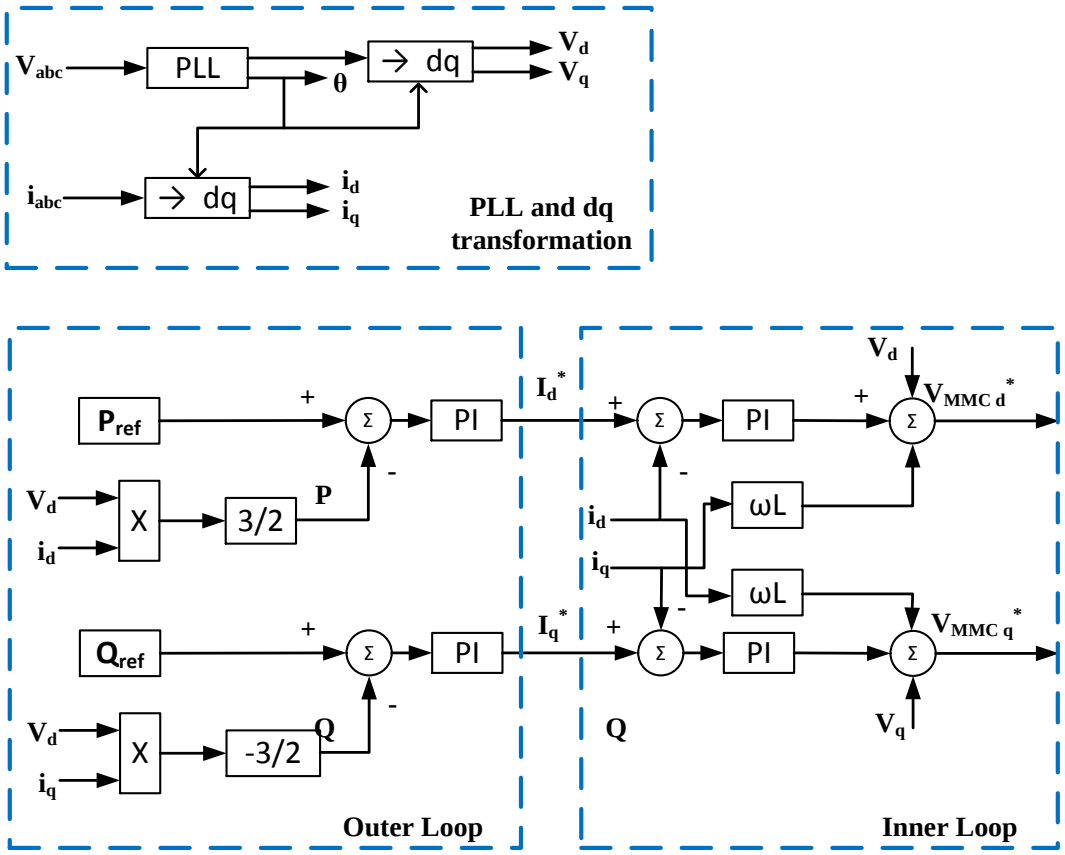


Figure 2.19: Vector Control of Active and Reactive Power

Notice that now the active and reactive power can be decouple and control independently by controlling i_d and i_q. Two PI controllers can be used to control the reference dq current values by acting on the error of P and Q. An inner loop controller made of an additional two PI controller is then used to set the currents at the reference value generated by the outer loop. The action of this controller creates the reference voltage for the sub-module PWM generation scheme. The control diagram is shown in Figure 2.19.

2.2.6 **Limitation on Reactive Power Sink/Source**

A control for the active and reactive power was proposed with the assumption that the proposed topology behaves like a VSC. It was mentioned before that active power can only flow from one the converter to the grid, but no restriction was given to the reactive power. There is in fact a restriction on the amount of reactive power that can be sink or source by the converter. This restriction is imposed by the amount of allowable voltage ripple on the sub-module capacitors. An equivalent sub-modules model is shown in Figure 2.20 with the set of equations (2.24) and (2.25).

$$\frac{d}{dt}v_{dc}(t) = \frac{\left(i_L(t) - i_{out}(t)\right)}{C} \tag{2.24}$$

$$\frac{d}{dt}i_L(t) = \frac{\left(v_{in}(t) - v_{dc} - R_{eq}i_L(t)\right)}{L_{lkg}} \tag{2.25}$$

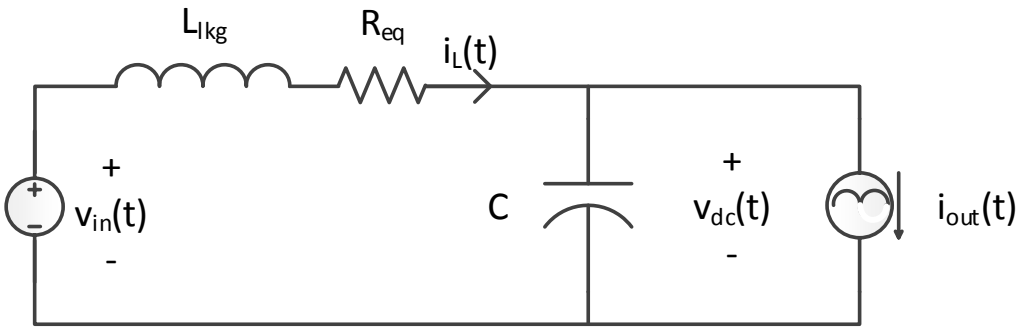


Figure 2.20: Model for analyzing capacitor voltage ripple.

Were i_L is the secondary current, C is the capacitance, and R_{eq} is the equivalent resistance between V_{in} and the capacitor. The output current i_{out} shape and magnitude is dependent on the real and reactive power. The output current shown in Figure 2.20 is for a full bridge sub-module, this will have a higher ripple compared to the half-bridge. It's also important to notice that it's assumed that the module is ON all the time. Depending on the modulation scheme, most modules are partially ON during one cycle and thus will

have a lower. To keep some generality the highest possible ripple voltage is derived using the output current shown in (2.27).

$$|S| = |V| * |I| = \sqrt{P^2 + Q^2} \tag{2.26}$$

$$|I_o| = \frac{\sqrt{P^2+Q^2}}{3\,|V_g|} \quad \rightarrow \quad i_{out}(t) = \left|\sqrt{2}\,|I_o|\sin(\omega t)\right| \tag{2.27}$$

For different values of sub-modules capacitor the voltage ripple can be calculated at different reactive power loading levels.

Figure 2.21 summarizes the voltage ripple for a specific system with various levels.

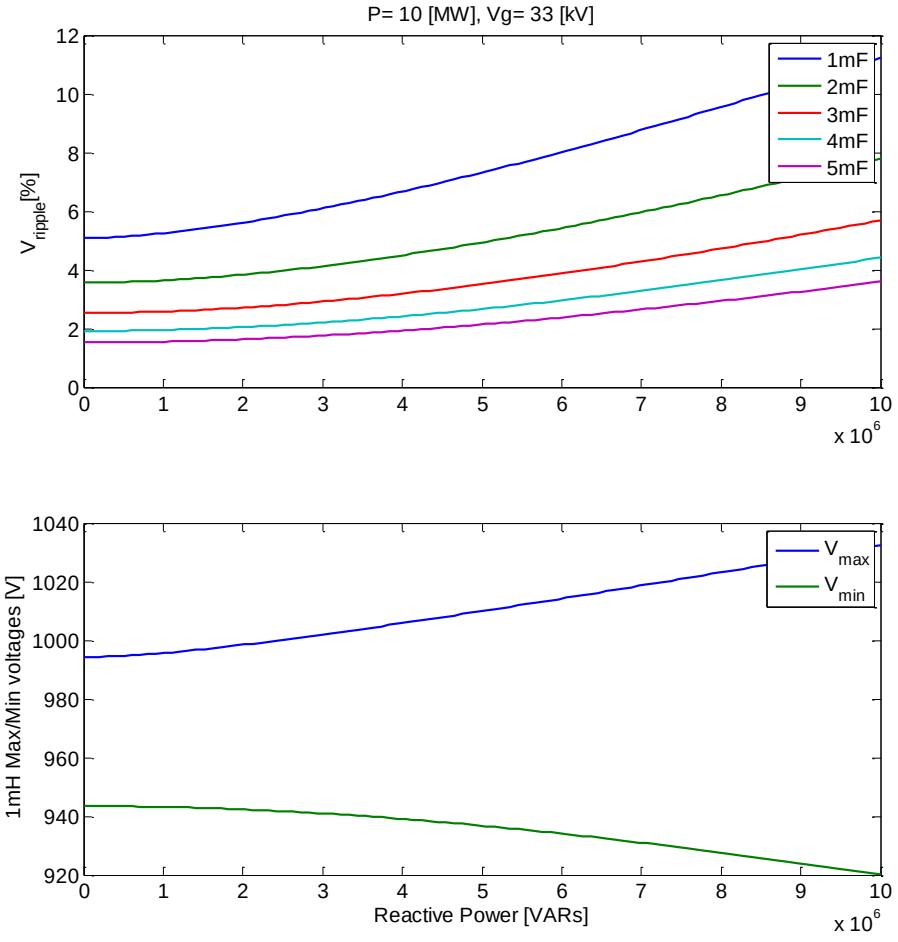


Figure 2.21: Capacitor Voltage Ripple Variation Due to Reactive Power.

Chapter 3

3 SIMULATION OF PROPOSED TOPOLOGY

A very inclusive simulation was created in order to validate the proposed topology, and to showcase higher voltage operations that are not practical to build in the laboratory. The tool used to build these simulations was a Matlab/Simulink with the PLECS circuit toolbox from Plexim. Figure 3.1 Figure 3.1: Overview of the system model shows an overview of the model, it is divided into two major sections, the model of the circuit and the control. The circuit model includes all of the components needed for a 9-level MMC, and the control section is composed of the modulation schemes for the primary converter and sub-modules.

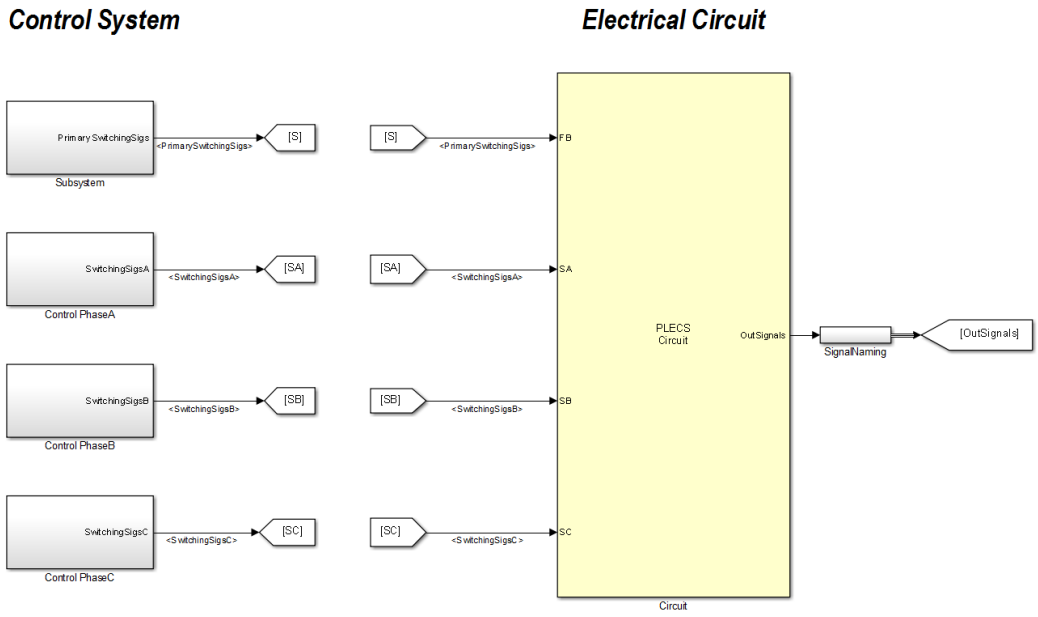


Figure 3.1: Overview of the system model

3.1 Topology Model

A HFL-SM is shown in Figure 3.2, the high frequency input is located at the left of the sub-module and it is marked as P1 and P2. For monitoring purposes voltage and current at the input of the sub-module are measured. A transformer model is connected next to input of the sub-module, this model includes leakage and magnetizing inductances. Saturation was not model in the current version of the model, inter-winding capacitance was included initially and removed. The expected inter-winding capacitance did not have a significant effect on the results, but because of it small value it slowed down the simulation considerably and it was not included in the final model. At the secondary of the transformer, a diode rectifier circuit is model, these diodes have turn-on losses and on-resistance included in the model. PLECS toolbox does provide a more detail model for diodes containing reverse recovery losses, but for the current model size it increases the simulation run time exponentially. The output of the diode rectifier is connected to a capacitance, referred to as the sub-module DC link capacitance. This capacitor is in the order of 2.2 mF, and it includes equivalent series resistance (ESR). To the right, the

IGBTs and output if the sub-module (S1 and S2) are connected. Figure 3.2 shows a half bridge configuration with two devices, it can produce two different voltage levels at the output.

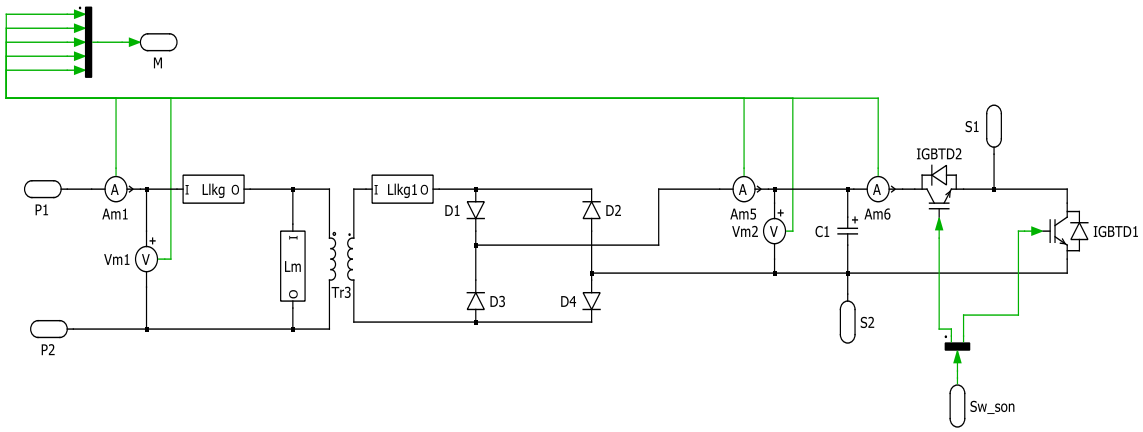


Figure 3.2:High-Frequency Link Sub-Module PLECS Model

Multiple HFL-SMs are connected in order to build a 9-level MMC as seen in the right part of FIGURE. Three phase leg, each composed of 8 HFL-SM are connected to the output to create a 3-phase inverter. Each HFL-SM has control inputs, and measurement output that can be monitored individually and with ease thanks to the use of signal bus bars in the Simulink model. Also an electrical input is shared with all the HFL-SM, this input is connected to the output of the primary converter (seen on the left side of FIGURE). The primary converter is model using 4 IGBT device models.

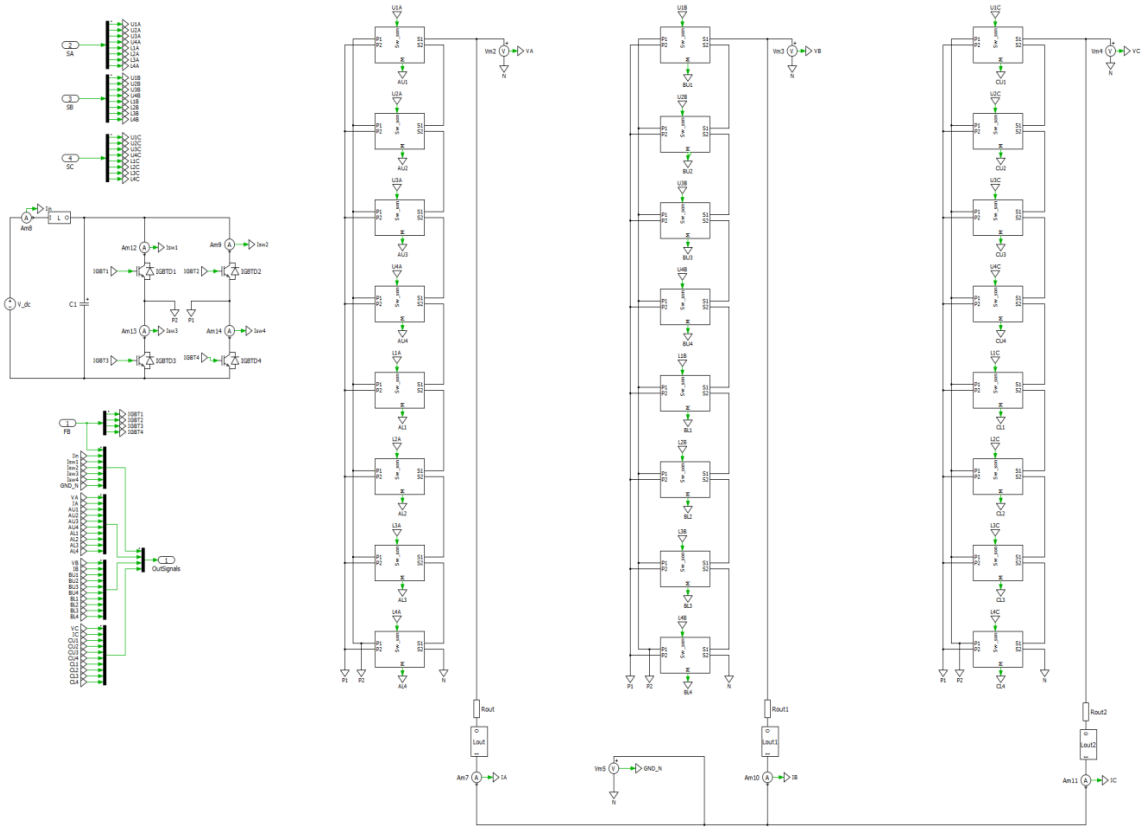


Figure 3.3: Model of MMC with High-Frequency Link Sub-Modules

3.2 Modulation

The modulation of the MMC is composed of two separate schemes, the primary converter switching signals and the sub-modules switching signal. The primary converter switching signals will be discussed in the first section, these signals are S1, S2, S3, and S4 from the IGBTs shown in Figure 3.4. Another section will describe the switching scheme that will generate the signals Q and Q' for each HFL-SM (Figure 3.5). These switching signals have to be controlled with the goal of regulating a desired output voltage and phase.

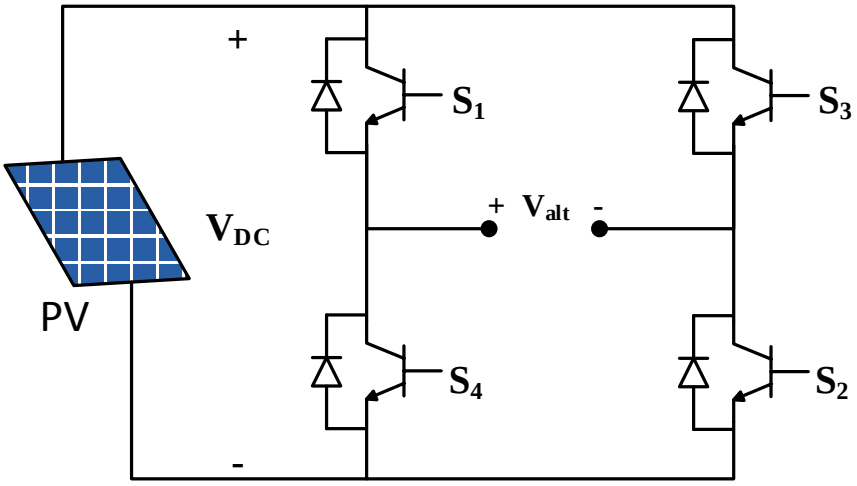


Figure 3.4: Primary Converter.

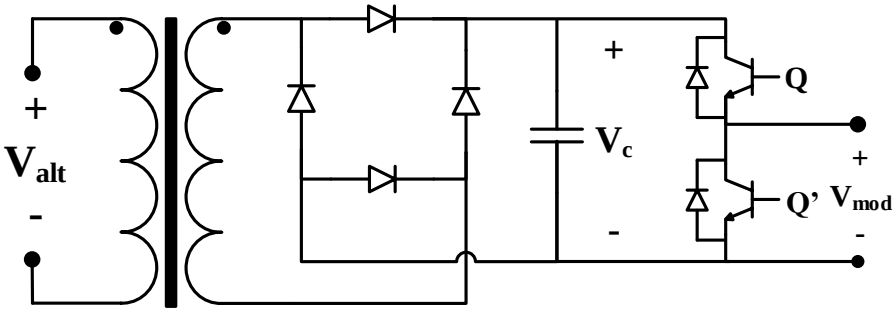


Figure 3.5: High Frequency Link Sub-module (HFL-SM).

3.2.1 **Primary Converter**

A high-frequency voltage needs to be generated by the primary converter in order to keep the transformer design as compact as possible. This primary converter generates an alternating voltage as shown in Figure 3.6. The duty cycle D of this converter is calculated using (1.1), ideally it should be around 50% duty cycle. Some "dead-time" is needed in between $+V_{DC}$ and $-V_{DC}$, however this is very small and in Figure 3.6 it has been exaggerated for display purposes only. Additional time in the zero voltage state will result in less time for power transfer, and can result in a lower module voltage. Although not studied on this thesis, an alternative configuration can involve an inductor in series with the rectifier, and purposely reducing the duty cycle in order to achieve a controllable and variable sub-module voltage. As mentioned before the frequency of this square

voltage affects the design of transformer; the higher the frequency, the size and weight of the transformer is reduced. Currently IGBT technology is practically limited to about 20 kHz, however it is possible to use lower current rated wide band gap (WBG) devices in parallel instead in order to achieve higher switching frequencies. Such devices can be GaN and SiC and they can practically switch at frequencies of up to 100 kHz, reducing the overall size and weight of the transformer.

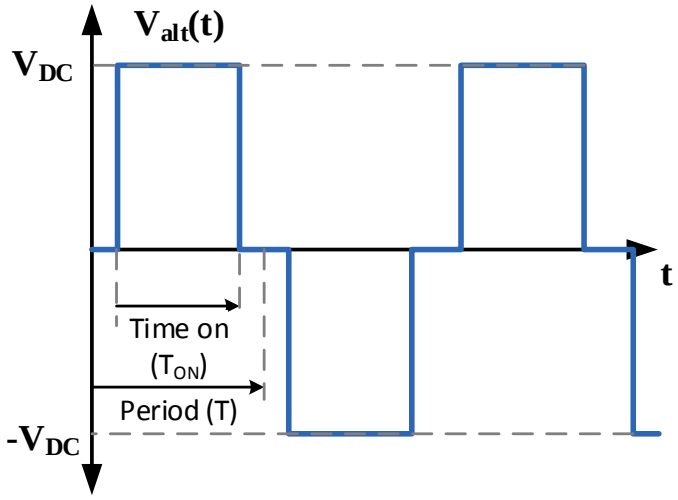


Figure 3.6: Full-Bridge theoretical output voltage.

There are various ways to generate the switching signals. In this dissertation a state flow diagram is used to represent the switching states. The state flow will have a total of 4 states (shown in Table 3.1). Each cycle of the modulation is completed by flowing from state 1 to 4. Notice that this modulation is desirable because at every state change only one switch is changing, this reduces the total switching loss of the system. Ideally the duty ratio should stay close to 50%, but if needed it can be used to adjust the capacitor voltage.

Table 3.1: Full-Bridge Converter States of Operation

State	Switches ON	V_{alt}
1	S_1, S_3	Zero
2	S_1, S_2	$+V_{DC}$
3	S_2, S_4	Zero
4	S_3, S_4	$-V_{DC}$

3.2.2 **MMC**

Consider the sub-modules to be simple half bridge sub-modules with a constant DC supply. The desired output voltage of one of the phases is shown in Figure 3.7. Notice that the vertical axis is in number of HFL sub-module voltages (V_{mod}). This example has 8 sub-modules that will allow the output voltage to be any of the 9 levels between $4 * V_{mod}$ and $-4 * V_{mod}$, (including zero). The number of levels is too small to have a low THD by just going from one level to another, so instead the strategy will use pulse width modulate (PWM) when transitioning between levels. With the goal of having the average inverter voltage match the desired AC phase voltage.

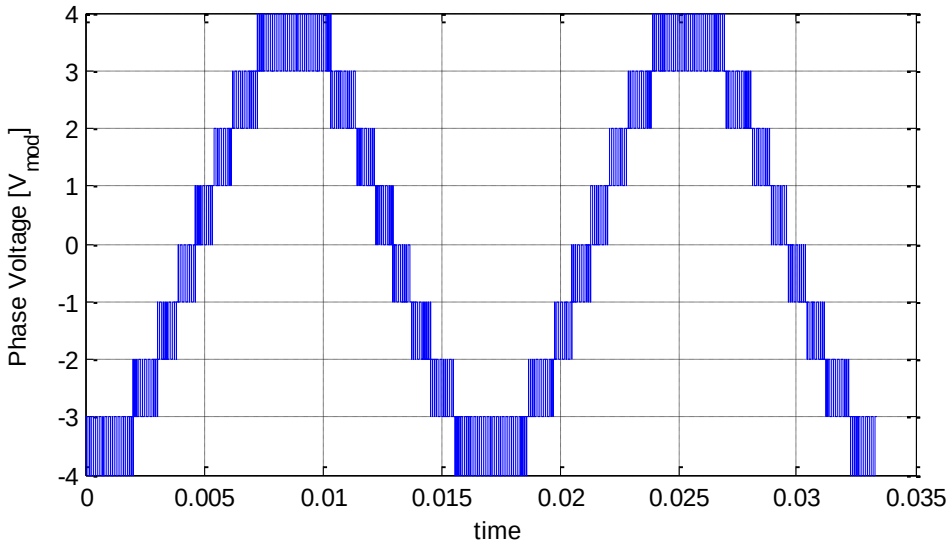


Figure 3.7: Ideal MMC phase voltage.

When it comes to generation of the switching signals for the MMC, there are two main options: level shifted and phase shifted (Figure 3.8). Both modulations schemes have triangular waveforms at switching frequency that are compared against a reference sinusoidal voltage in order to generate the switching signals. Each waveform is assign to a module and when compared to the reference voltage Q and Q' can be generated. More information on these can be found in [1].

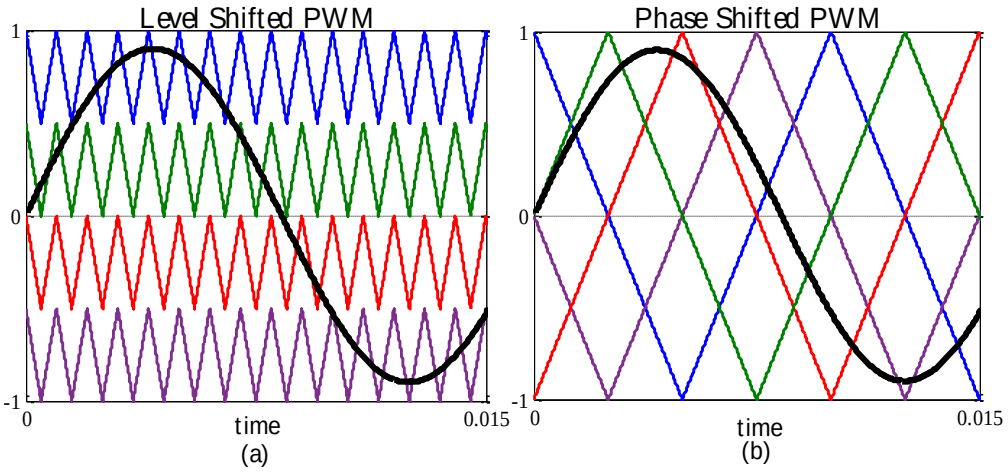


Figure 3.8: (a) Level Shifted PWM, (b) Phase Shifted PWM

Phase shifted modulation offers the advantage of using each modules equally. This is desirable because it distributes the stress equally. The presented topology uses a phase shifted modulation, however the positive and negative arms are level shifted. The triangle and reference signals for the proposed topology are as shown in Figure 3.9.

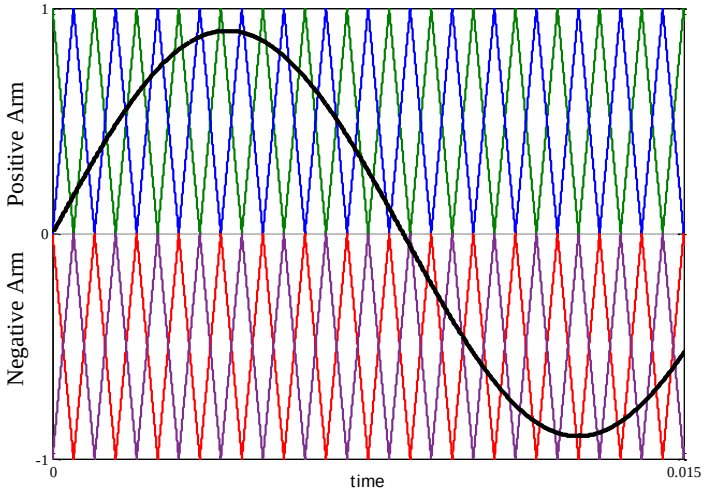


Figure 3.9: Modulation signals for one leg of the proposed topology.

Using Figure 3.9 and Table 3.2 the switching signals for the HFL sub-modules can be generated. Notice that the signals shown are for a leg with 4 sub-modules. For the example shown in Fig. 6 there should be 4 triangular waveforms on both top and bottom level, for a total of 8 signals for 8 modules.

Table 3.2: HFL sub-module switching signals

[Q , Q']	Ref. ≥ Triangular	Ref. < Triangular
Positive Arm	[1 , 0]	[0, 1]
Negative Arm	[0 , 1]	[1 , 0]

3.3 Results

As a proof of concept various simulations were created in MATLAB/Simulink. A low voltage scaled down version of the converter was created in order to test the basic concept of the proposed topology. In addition to this a high voltage inverter was simulated. Ideally a high voltage inverter would require many HFL sub-modules in order to achieve a good power quality output. To simplify the simulation only 8 modules per arm were used, this means that the capacitance needed to increase to keep a good output quality. Table 3.3 shows some of the parameter values used in both simulations.

Table 3.3: Simulation Parameters

Parameters	Low Voltage	High Voltage
Input Voltage	50V	1kV
HFL V_{mod}	50V	12.5kV
# of SM per Leg	8	8
Transformer Frequency	20kHz	15KHz
Transformer turns ratio	1:2	1:25
Duty Cycle	50%	50%
Output Voltage	120V RMS	34.5kV RMS
Output Current	3.54A RMS	1.73kA RMS
Output Frequency	60-Hz	60-Hz
3 Phase Power	1.27kW	60MW
Sub-module Capacitance	2.2mF	2.2mF
Arm Inductance	1mH-10mH	5mH

3.3.1 **Low Voltage Simulation**

One of the design parameters of the proposed topology is the arm inductance. This inductance helps maintain the output current smooth. Figure 3.10 and Figure 3.11 will help to illustrate how the output voltage is affected by the arm inductance. When 1mH was used the output current shows a perceptible ripple. If the ripple current is too high it can present potential damage to the semiconductor devices. A 10mH arm inductance is used next in order to improve this ripple current. When comparing the current on both plots the improvement in the current ripple is very clear. However when increasing the arm inductance the current will lag the voltage more, this needs to be taken into account because it will affect the capacitor voltage ripple. When the current lags the voltage the top ripple shown in Figure 3.12 will slightly increase. However this effect is very small in comparison to the effect due to the output current magnitude.

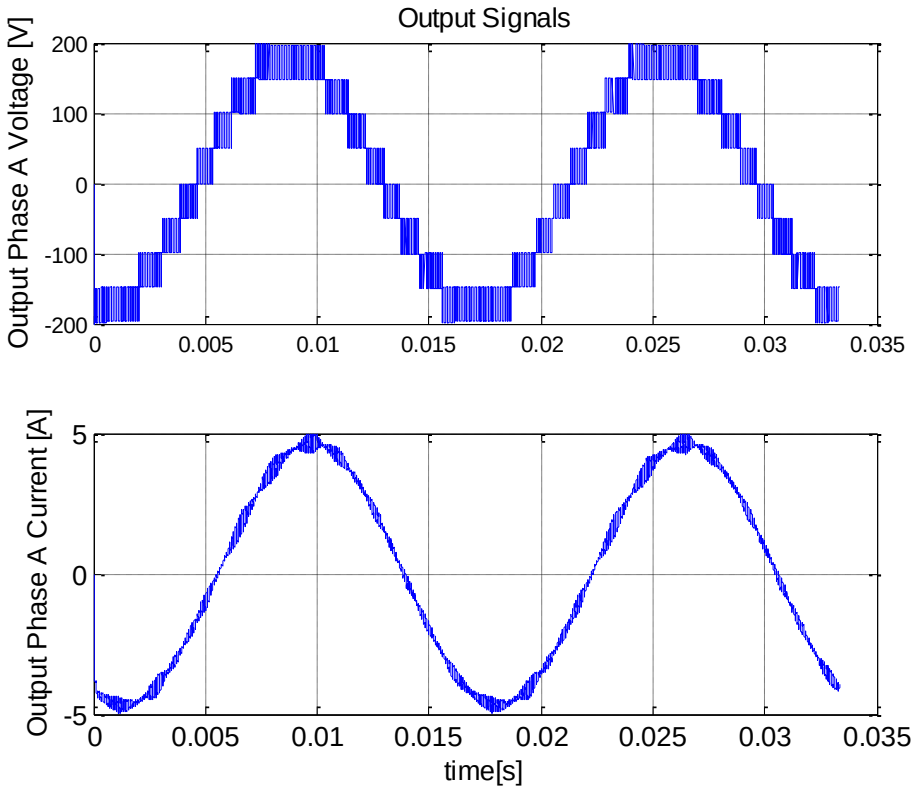


Figure 3.10: Inverter output with arm inductance of 1mH.

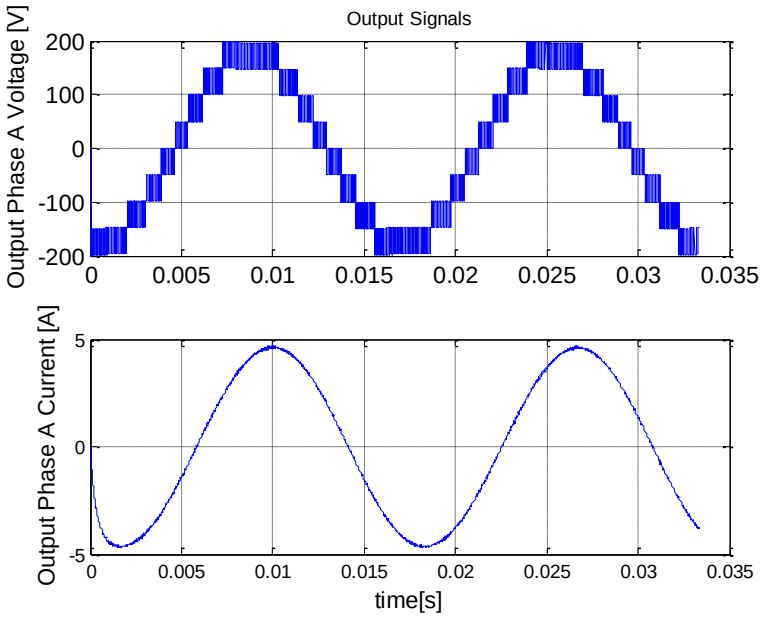


Figure 3.11: Inverter output with arm inductance of 10mH.

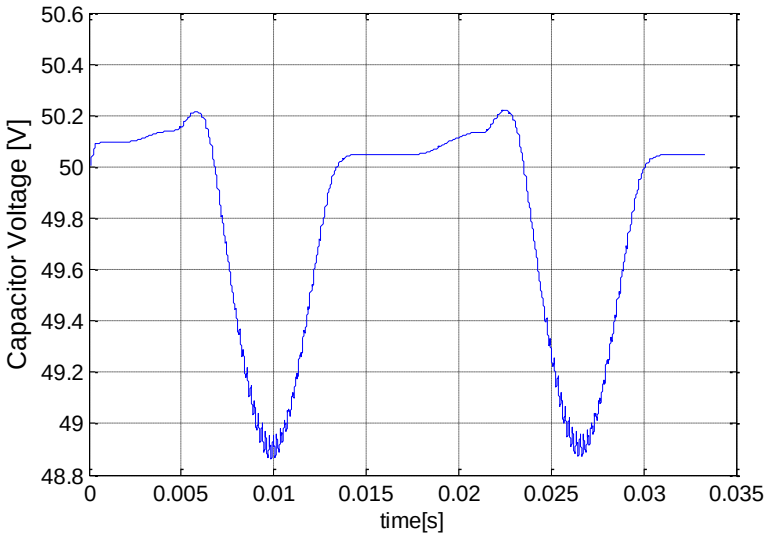


Figure 3.12: Capacitor voltage ripple.

A signal of interest is the capacitor voltage ripple. Figure 3.12 shows the capacitor voltage for the simulation result with 10mH as the arm inductance. Notice that the capacitor voltage ripple is about 2% of the total capacitor voltage. Another observation is that the ripple voltage is clearly riding on top of an average voltage; this average voltage is set by the full bridge converter. As long as the capacitor can be charged back to this

average value there is no need for voltage balancing in the proposed topology. If that was not the case and no voltage balancing is desired then either the number of sub-modules needs to be increased or the capacitance must be increased.

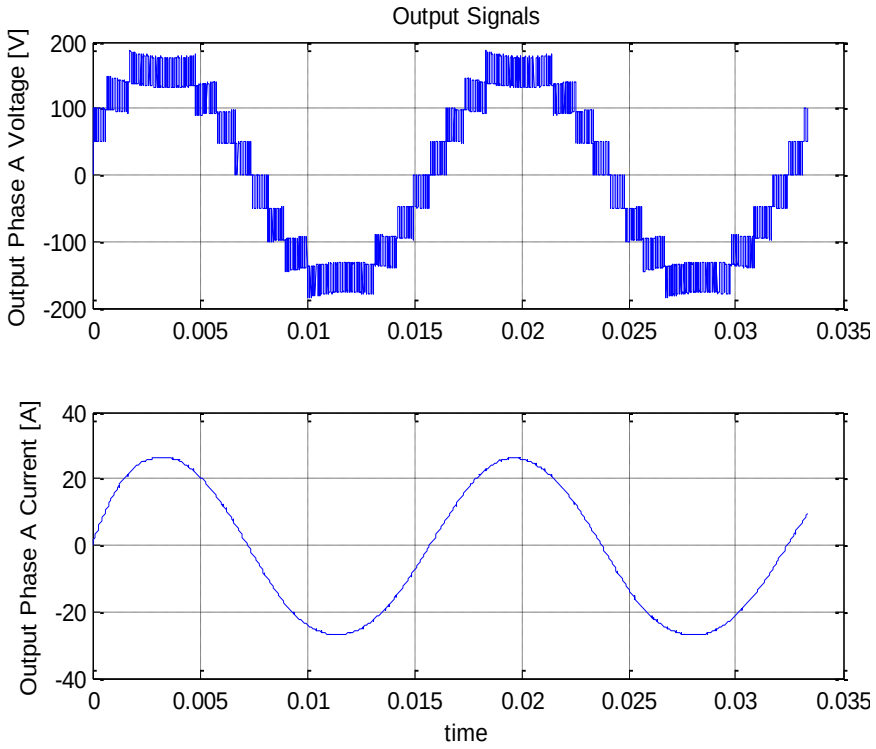


Figure 3.13: Over current output signals.

It is of interested to know what will happen when a fault on the gird side occurs. This normally will lead to an over current for the inverter. As a test Figure 3.13 shows the output signals when the output current is about four times the rated current. Notice that the main effect is the capacitor voltage ripple becoming larger. This will distort the voltage levels reducing the rated output voltage capabilities. However the inverter can operate in this state for short periods of time.

3.3.2 **High Voltage Simulation**

As mentioned previously, a good application for the proposed topology is PV power plants. PV power plants produce a large amount of power. A typical PV power plant output voltage is 34.5kV; using this output voltage a 60 MW inverter was simulated.

However for such a high voltage 8 modules per leg are too few, about 200 modules per arm are need to get reasonable results. Knowing this the simulation was still done with 8 modules due to computational resource limitations. Figure 3.14 shows the output signals for a high voltage inverter.

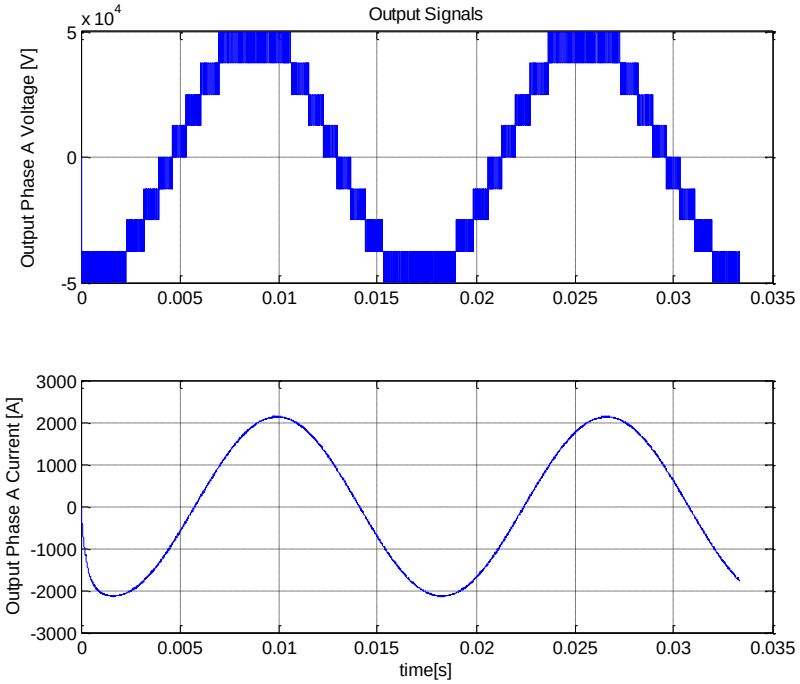


Figure 3.14: High voltage output signals.

This simulation shows that switching wise, it is possible to design an inverter that can output high voltages. The proposed topology has the advantage that it can step up the voltage in 2 different ways: transformer turns ratio, and adding more sub-modules. A combination of these two can be used to easily achieve high voltage levels.

Chapter 3

4 HARDWARE DESIGN

A 9-level prototype that validates the concept presented in this dissertation is design and tested. A 1.2 kW power supply, with a voltage of 100 V serves as the input DC source to the prototype. For simplicity and proof of concept, half-bridge sub-modules are used, although it is more practical to use full-bridge HFL-SM (shown in section 2.2.3). To reduce the prototype component cost, each HFL-SM is designed to operate at 50V (turns ratios of 2:1). This limits the output peak to peak voltage to 400 V as shown on (4.1).

$$V_{p-p} \leq \mathrm{N_{SM}} \left(\frac{N_p}{N_s}\right) V_{DC} \tag{4.1}$$

where $V_{p\text{-}p}$ is the peak to peak output voltage, N_{SM} the number of submodules used per phase, N_p and N_s the number of turns in the primary and secondary winding of each module high frequency transformer, and V_{DC} is the input DC voltage.

4.1 Primary Converter: Semiconductors

The primary inverter has to switch the bulk of the power at a switching frequency of 20 kHz. This large amount of power will result in a large amount of switching losses at the primary converter as compared to the sub modules. To reduce the switching losses soft switching (also known as zero current switching "ZCS" and zero voltage switching "ZVS) is recommended. For the proof of concept prototype avoiding these loses aren't a priority, therefore soft switching will not be implemented. To ensure the switching losses will not create any overheating problems a device module that is rated for a much higher power will be used, this will of course increase the losses more but all well within the capabilities of the module. Pair of Power-EX dual-IGBT modules (CM200DX-24S) is used as the two legs of this inverter. Each of these modules is rated for 200 A and 1200 V

this makes them extremely rugged both thermally and electrically, a desired trait to for a prototype hardware.

The estimated loss on each module can be found by adding the estimated conduction loss and the estimated switching loss as shown in (4.2);

$$P_{Loss} = P_{Cond_{loss}} + P_{SW_{loss}} \tag{4.2}$$

The switching losses include the turn ON losses, turn OFF losses, and reverse recovery losses for both the IGBT and diode as shown in (4.3)

$$P_{SW_{loss}} = (E_{ON} + E_{OFF} + E_{rr}) * f_{SW} \tag{4.3}$$

where the E_{ON} is the energy lost during turn on, E_{OFF} is the energy lost during turn off, and E_{rr} is the reverse recovery energy lost. These losses are taken from empirical measurement done by the manufacturer and are found on the modules datasheet. Notice that these are values for each switch, and thus calculations have to include the energy for both top and bottom device of a half-bridge leg. Using the equations shown above and the device parameters found on Table 4.1, we can estimate the total losses for a 1 kW and 5 kW converter to be $P_{Loss_{1kW}} = 27.78\,W$ and $P_{Loss_{5kW}} = 57.75\,W$ on each leg. The total power loss on the primary converter would be twice the amount, therefore the estimated primary converter efficiency is 94.44% for 1 kW and 97.69% for 5 kW. Using the estimated loss and the module thermal resistance found to be 0.273 °C/W from the junction to the ambient, we can estimate the module junction temperature using (4.4).

$$T_j - T_a = R_{TH,j-a}\, P_{Loss} \tag{4.4}$$

where T_j is the junction temperature, T_a is the ambient temperature, $R_{TH,j\text{-}a}$ is the half-bridge module thermal resistance from the junction to the ambient, and P_{Loss} is the power loss on one of the primary half-bridge modules. For 1 kW the expected temperature rise is about 15.2 °C, and 31.5 °C for 5 kW.

Table 4.1: Power-EX dual-IGBT module (CM200DX-24S) Parameters

Parameters	Value
Collector-Emitter Voltage	1200 V
Collector Current	200 A
Maximum Junction Temperature	150 °C
Collector-Emitter Resistance (per switch)	1.1 mΩ
Turn-on energy (adjusted for 1 kW)	340 µJ
Turn-off energy (adjusted for 1kW)	583.3 µJ
Reverse recovery energy (adjusted for 1kW)	466.7 µJ
Maximum Power Dissipation of Module HS	1500 W
Equivalent Thermal Resistance ($R_{TH,j-a}$)	0.273 °C/W

Typically a 2-leg inverter is required to have two types of capacitance connected to the DC link. One is known as the bulk capacitance, this capacitor can often be a capacitor bank and it scales up exponentially as the power of the converter increases. This capacitor serves as an energy buffer for inverters where the instantaneous input and output power do no match; this is the case for a 1ϕ inverter. By providing the energy mismatch a bulk capacitor bank keeps the DC link voltage constant when a weak source (i.e. PV panel) is used as the input. The primary converter proposed on this topology doesn't have an instantaneous power mismatch, both input and output power are constant, thus no bulk capacitor is needed. The second type of capacitance in the DC link is used as a snubber, and needs to be as close to the switched as possible. As the converter carries a high current switched at a relatively fast speed, voltage spikes can appear. This is because the cable that connects the DC source to the converter is inductive, especially more if the cable is long. A film capacitor is directly connected to the DC link of each module to provide a low impedance path for the high frequency currents, and prevent the voltage spike. These are shown along with an overall picture of the primary inverter prototype in Figure 4.1.

Figure 4.1: Primary side inverter hardware prototype.

4.2 High Frequency Bus

The high frequency bus (HF-Bus) is one of the key factors of the system and it has to be designed correctly in order to avoid voltage spikes and EMI noise. The proposed hardware prototype is designed to have 10 A switching at 20 kHz, with an expected voltage potential of 100 V between two busses. When designing the HF-Bus, it is important to minimize the skin effect, keep length to a minimum, and EMI noise to as low as possible. Using (4.5), the thickness of a rectangular conductor is calculated to be less than 0.96 mm. To keep the inductance, EMI, and losses to a minimum, multiple positive and negative bus bars are stacked, as shown in Figure 4.2. The shaded part is the negative bus and it is underneath the positive bus, represented with solid white. Each bus is cut in the form shown by the solid white but, then every other bus is flipped along the center horizontal axis such that all the tabs of the positive and negative bus line up in the areas marked with "+" and "-". For the proposed hardware prototype only one layer is needed for the relatively low power in the experimental setup. A flat wire of 0.5588mm (22mils) thickness and 50.8mm (2") width was selected due to its large cross section area

with a small thickness. The cross-sectional area of this wire is comparable to that of an AGW 6 wire, for which the recommended maximum current is 37 A. Each bus has to be isolated with Kapton tape and care must be taken so that no sharp edges puncture the tape.

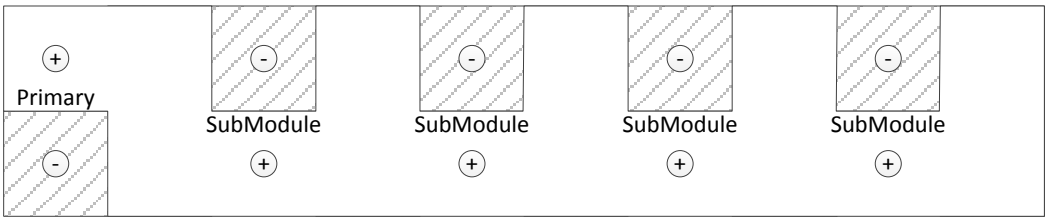


Figure 4.2: High frequency bus bar configuration.

4.3 High Frequency Link – Submodule: Transformers

The transformer design considerations are as follows: avoid core saturation, minimize the leakage inductance, minimize skin effect on the wires, and selecting the appropriate turn ratio. To ensure a minimal leakage it is advised that a toroid core should be used with the primary and secondary winding turns kept as close as possible. To assure a full usage of the cable (minimize skin effect) the wire thickness/radius should be based on (4.5) [33]

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}\ \sqrt{\sqrt{1+(\rho\omega\epsilon)^2}+\rho\omega\epsilon} \tag{4.5}$$

where δ is the distance from the surface to where the current density drops to e^{-1} times of the surface current, ω is the angular frequency of the signal in the wire, ρ is the permittivity of the wire, and μ is the permeability of the wire.

For a rectangular copper wire, the thickness of the wire should not be more than $2\delta(copper\ @20k\ Hz) \approx\ 0.92\ mm$. A flat copper cable with a thickness of 0.5 mm and width of 2 mm (AWG 17 equivalent) is selected to accommodate the previously mention restriction.

The flux density in the core should not exceed the material's saturation point (B_{sat}) for the designed switching frequencies (10 kHz - 20 kHz). Ferrite cores are among the most common core materials and come in many shapes and sizes. Compared to other high performance materials (e.g. amorphous and nanocrystalline), ferrite is very inexpensive, making it ideal for MMCs. A typical ferrite core saturates at approximately 0.35T. The first step to find an appropriate core starts by defining the peak flux density with (4.6).

$$B_{peak} = \frac{\mu\mu_0 N I_{peak}}{l_e} \tag{4.6}$$

The peak magnetizing current can be estimated using (4.7) and (4.8),

$$I_{peak} = \frac{V_{in}\Delta t}{2L_m} \tag{4.7}$$

$$L_m = \frac{N^2\mu\mu_0 A_e}{l_e} \tag{4.8}$$

Substituting (4.7) and (4.8) into (4.6) yields (4.9) where $V_{in} = 100\,V,\ and\ \Delta t = \frac{0.5}{10\ kHz}$ (half a cycle).

$$B_{peak} = \frac{V_{in}\Delta t}{2NA_e} \tag{4.9}$$

A core with $A_e = 305.9\,mm^2$ was selected to avoid core saturation. The number of primary turns is then calculated using (4.10). The parameters of the designed transformer shown inTable 4.2 and the mean and standard deviation for the 24 built transformers in TABLE 4.3. An example is shown in Figure 4.3.

$$N \geq \frac{V_{in}\Delta t}{2B_{peak}A_e} = 24\ turns \tag{4.10}$$

Table 4.2: Transformer Design Parameters

Parameter	Value	Parameter	Value
$\boldsymbol{V_{in}}$	100 V	$\boldsymbol{N_p}$: $\boldsymbol{N_s}$	50:25 turns
$\boldsymbol{L_m}$	31 mH	$\boldsymbol{l_e}$	152 mm
$\boldsymbol{A_e}$	306 mm^2	$\boldsymbol{\mu_r}$	5000

$f_{sw,min}$	5 kHz	$f_{sw,max}$	60 kHz

Table 4.3: Manually Wrapped Transformer Parameters

μ_{L_m}	σ_{L_m}	$\mu_{L_{lkg}}$	$\sigma_{L_{lkg}}$
30.29 mH	2.44 mH	5.97 μH	1.2 μH

Figure 4.3: Transformer of High Frequency Link Sub-Module.

4.4 High Frequency Link – Submodule: Capacitors

The capacitor needs to be sized correctly to keep the voltage ripple within an acceptable level. Voltage ripple in the capacitor leads to unwanted second order harmonics in an open loop system. The capacitor behavior is described using the differential equations (4.11) and (4.12).

$$\frac{d}{dt} v_c(t) = \frac{\left(i_L(t) - i_{out}(t)\right)}{C} \tag{4.11}$$

$$\frac{d}{dt} i_L(t) = \frac{\left(v_{in}(t) - v_c - R_{eq} i_L(t)\right)}{L_{lkg}} \tag{4.12}$$

where i_L is the rectified secondary current, R_{eq} is the equivalent resistance between V_{in} and the capacitor, and i_{out} is the output current of the module. For a module that is ON for

the duration of a half cycle, (4.11) and (4.12) calculate the ripple voltage with different capacitance values. The results are shown in Figure 4.4 for a constant active power of 1 kW and a variable reactive power. A capacitance of 2.2 mF is enough to keep the ripple well below 5% if the reactive power is lower than 600VAR (pf = 0.625). Note that when multiple sub-modules are used, each is only ON for a fraction of the time consider in the calculation above. Therefore this ripple represents the worst case scenario.

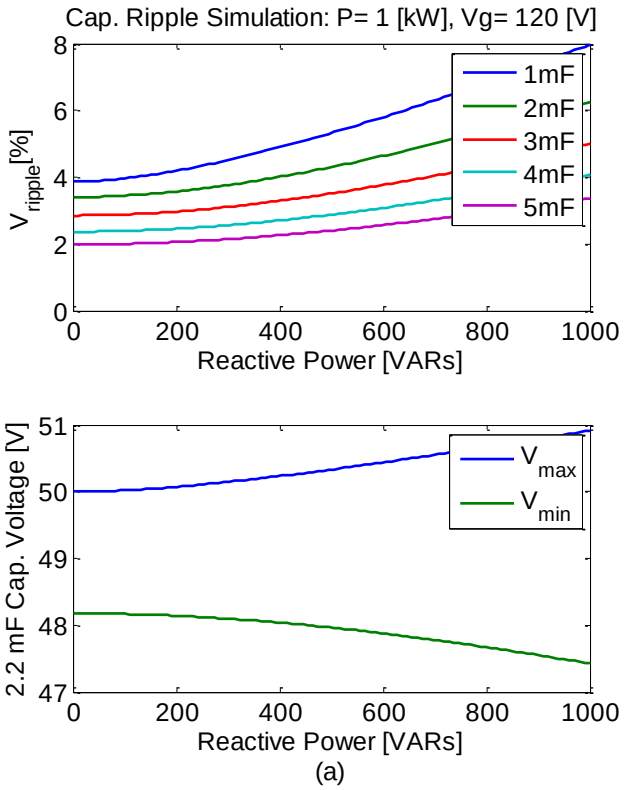


Figure 4.4: (a) Voltage ripple percentage for different capacitance values (b) envelope of the capacitor voltage for a 2.2mF capacitor.

4.5 High Frequency Link – Submodule: Semiconductors

The HFL-SM is implemented as a 9 level; three phase MMC with half-bridge sub-modules. The number of IGBTs needed can be calculated as;

$$2 * N_{SM} * 3 = 2 * (9 - 1) * 3 = 48 \text{ IGBTs} \quad (4.13)$$

Notice that if full-bridge sub-modules are used, the number of modules needed would be reduced to half but the number of switches would remain the same. A Power-EX dual-IGBT module (CM100DU-12F) was used in each HFL- SM. For the diode bridge rectifier, a general purpose fast recovery diode (TO220AC) was selected to ensure fast switching times and low reverse recovery currents to minimize the losses. Each HFL-SM is equipped with a DC-DC converter that powers the driver from the capacitor, removing the need for an external or isolated power supply. The power consumed by the driver is approximately 2.5 W and is drawn directly from the inverter, ensuring that the driver losses are included in the efficiency measurements. An example of a HFL-SM is shown in Figure 4.5.

Figure 4.5: HFL-SM hardware prototype.

4.6 FPGA Controller

The controller used in the experimental setup is a Spartan 6 FPGA board combined with a dual buffer stage (see Figure 4.6).

Figure 4.6: Signal Buffer (3.3 V to 15 V) and FPGA board (Spartan 6).

4.7 Signal Driver

The first is a bidirectional buffer stage that turns the 3.3 V switching signals from the FPGA to 5 V. Signals form an ADC can be connected to this stage for measurement purposes. The second buffer stage steps up the 5 V signals to 15 V signals that travel on CAT6-RJ45 cables to prevent noise from unintentionally turning ON a device. A Power-EX driver (VLA504-01) receives the 15V signals; these are optically isolated to maintain galvanic isolation between different HFL-SM.

4.8 Loss Estimation

4.8.1 Primary Converter Semiconductor Losses:

From section 4.1, the semiconductor losses have been estimated at $P_{Loss_{IGBT}} = 55.6\,W$.

4.8.2 Core Losses on HF Transformers:

To calculate the core losses we use (4.14) from the manufacturers datasheet.

$$P_{core} = 3.397\, f^{1.979}\, \Delta B^{2.628}\, \left[\frac{mW}{cm^3}\right] \qquad (4.14)$$

where f is the switching ripple frequency on the core in kHz, and ΔB is the peak ripple flux density. This equation includes both hysteresis losses and eddy losses for the specified core. Each HF core loss is estimated to be 2.44 W, for a total of 58.8 W for all 24 transformers.

4.8.3 **Copper loss on Transformer:**

At 20 kHz the resistance of the primary coil was measured at 24 mΩ and 12 mΩ on the secondary coil, transposed to the primary for a total of 48 mΩ. The copper loss will vary from sub-module to sub-module, as some are conducting for longer and thus draw more current. If we assume we can balance out the use sub-modules over time, then we can find the average loss on a single module using the input current divided by the number of modules as seen on (4.15).

$$P_{copper} = \left(\frac{I_{in}}{N}\right)^2 R \qquad (4.15)$$

where R is the equivalent resistance at the primary coil, and N is the total number of sub-modules. It can be found that the copper loss on each HF transformer is 8 mW, and 0.2 W in total. This is much smaller compared to the core losses, a future design could consider using a different material for the core (e.g. Sendust) with lower core losses or optimize the design more.

4.8.4 **MMC Stage Semiconductor Losses:**

The device characteristic are similar to that found on the primary converter, the difference being the voltage used is half as much. At any moment only one sub-module per phase is switching in and out, therefore the switching losses can be estimated as if only one module was doing all the switching. At a switching frequency of 20 kHz, the switching losses per phase can be calculated to be 13.83 W, for a total of 41.5 W in all.

For the conduction losses, each submodule is always conducting through one IGBT, therefore an equivalent ON-resistance can be found by multiplying the number of sub-modules with the ON-resistance of a single IGBT. In the experimental setup this is a total of 26.4 mΩ per phase. This corresponds to a total of 5.5 W in conduction losses. The losses in the semiconductors at the MMC stage are the sum of switching and conduction losses, a total of 47 W.

4.8.5 **Estimated Efficiency:**

Assuming a 1 kW output power, the efficiency for the primary converter is estimated at 94.4% and the efficiency for the MMC stage is estimated at 89.4%. The total estimated efficiency of the prototype is 84.43%. There are three big item losses on the prototype, in order these are; core losses, MMC stage switching losses, and primary stage switching losses. The switching losses can be improved by selecting lower rated devices, using wide band gap devices (e.g. SiC and GaN), and implementing a soft switching strategy on the primary converter. The core losses make up for more than 35% of the total losses and they can be reduced by selecting a different core material, however in order to maximize the efficiency the design needs to be optimized.

4.9 Hardware Results

The 1 kW prototype was programed using the system generator tool package from Xilinx. This tool allowed the use of blocks in a Simulink environment to program the FPGA (Figure 4.7). It also includes co-simulation capabilities that allow for the change of variables in real time (Figure 4.7); this was used to control the switching frequency of both primary converter and MMC, primary effective duty cycle, output frequency, and modulation index. A picture of the experimental setup is shown on Figure 4.8, each horizontal plane has 8 submodules that make up a phase leg, and the primary converter is located in the middle of the table. From left to right the top of the bench sits the input DC source, power supply for the primary converter, and oscilloscope.

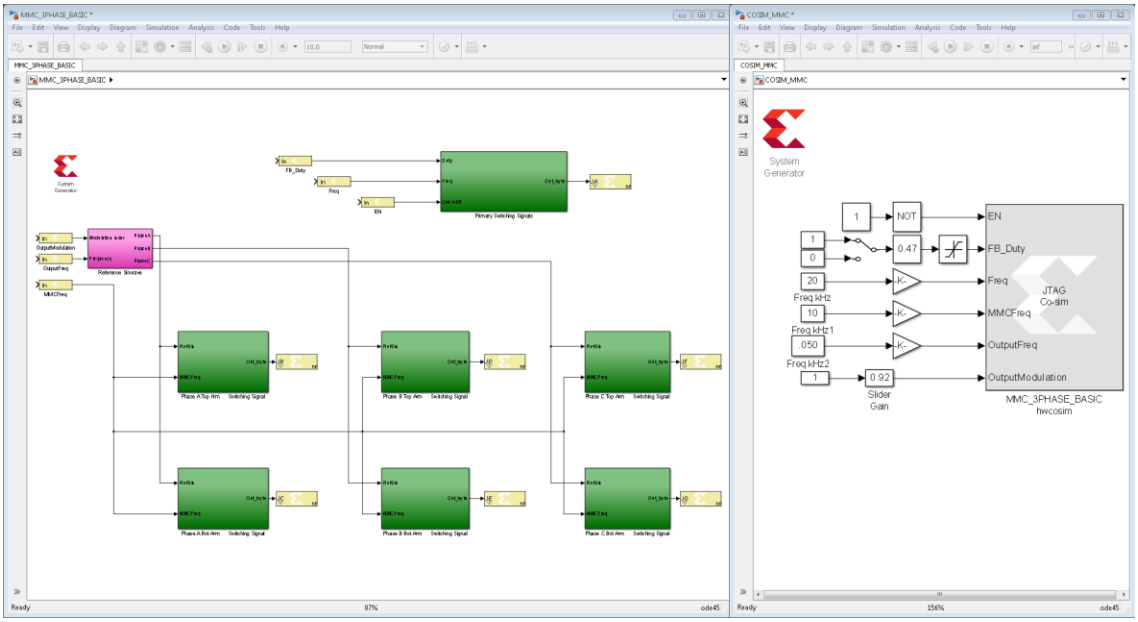


Figure 4.7: (Left) System Generator code for prototype, (Right) co-simulation environment for the experimental setup.

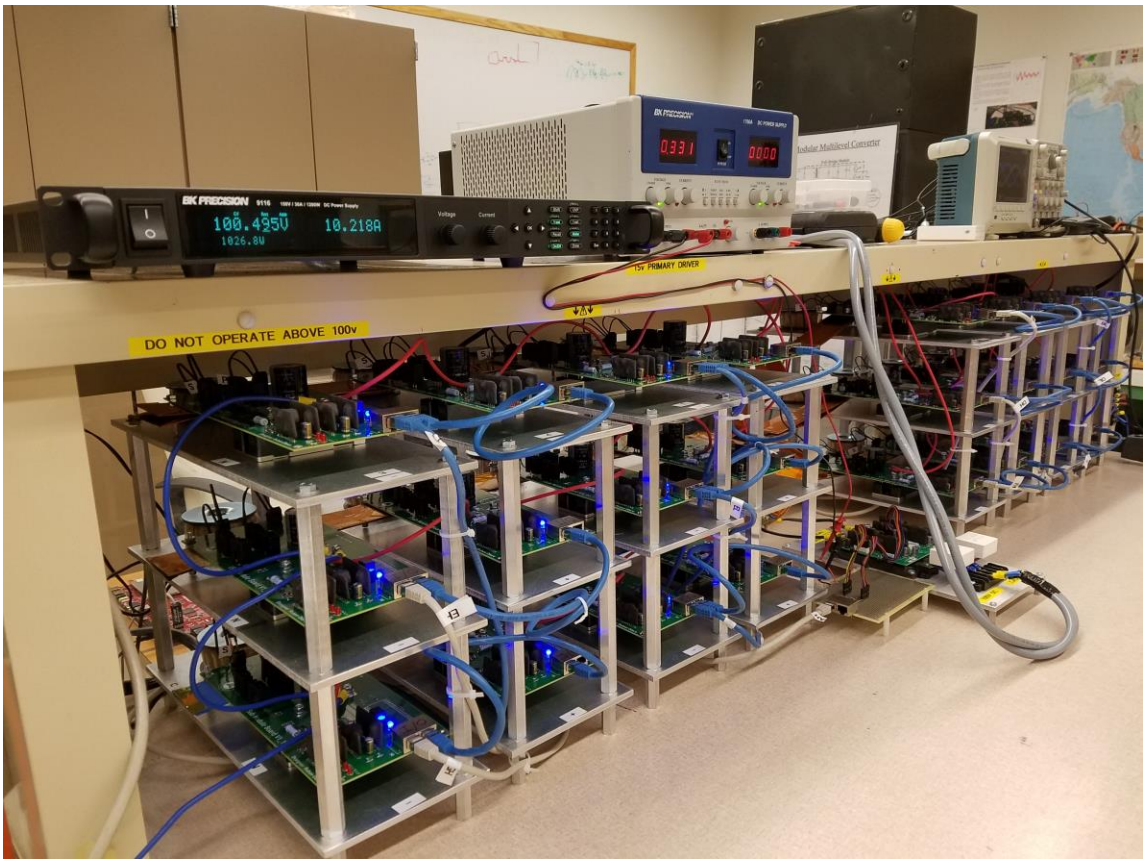


Figure 4.8: Prototype experimental setup.

4.9.1 **Operating Voltage and Current Waveform**

The voltage and current at the primary and secondary side of one of the HF transformers are shown in Figure 4.9. The phase to neutral output voltages can be seen in Figure 4.10, along with the phase-A current. Notice that each phase voltage has a total of 9 levels and each level is pulsed width modulated at 10 kHz. The load of the inverter was a three-phase resistive load of 58.6 Ω in series with a 45 mH smoothing inductance per phase. The three-phase output line currents can be seen in Figure 4.12 and the line-to-line voltages can be seen in Figure 4.11.

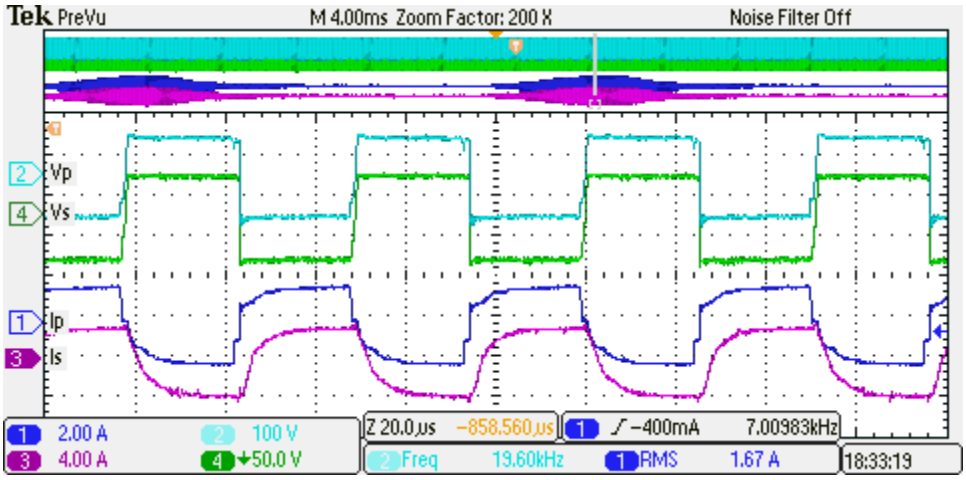


Figure 4.9: High frequency link voltage and current for 20kHz case (Primary and Secondary Voltage and Current on HF transformer).

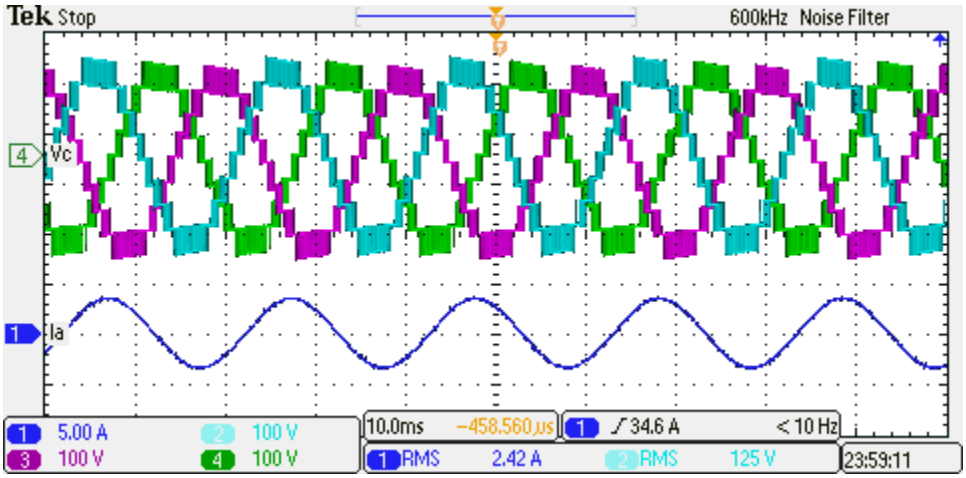


Figure 4.10: Output three phase line to neutral voltages, and line current.

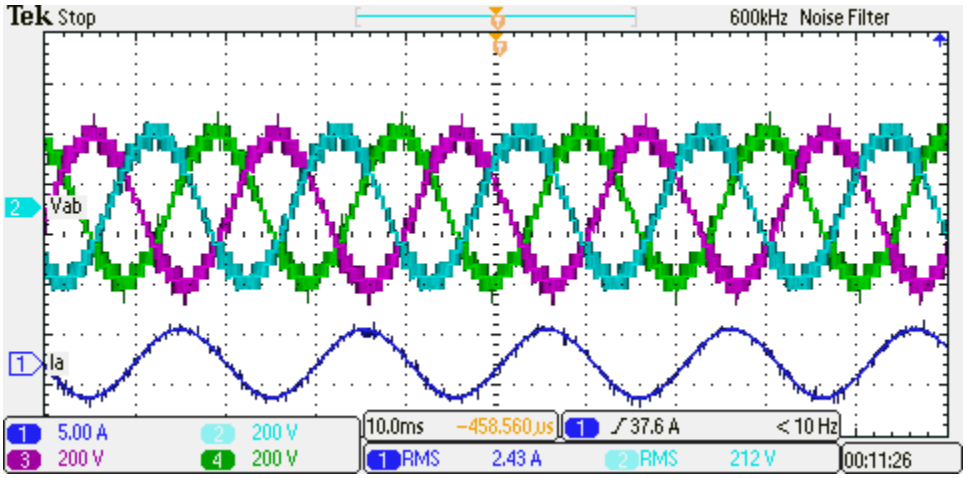


Figure 4.11: Output three phase line to line voltages, and line current.

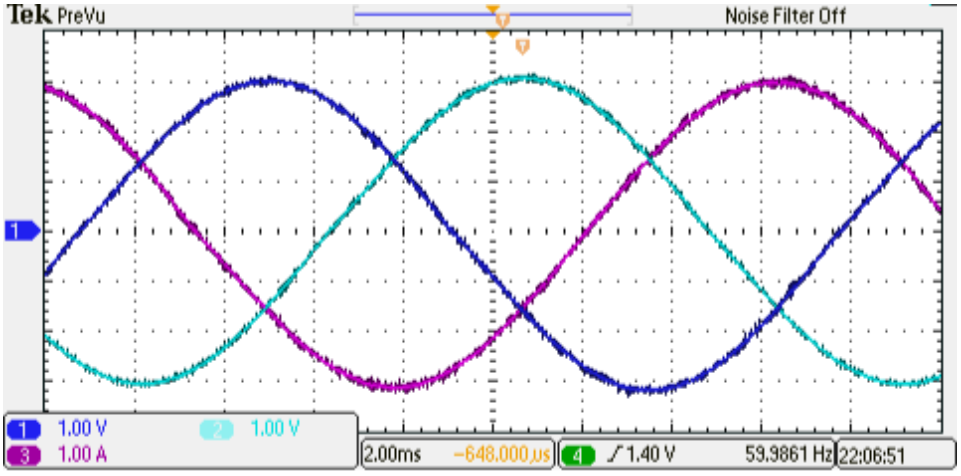


Figure 4.12: Measured line currents at the output.

4.9.2 **Capacitor Voltage Ripple**

One of the valuable claims of the proposed topology was the ability to self-balance the capacitor voltages, in the experimental setup there was no voltage balancing algorithm being performed. Figure 4.13 and Figure 4.14 show the capacitor voltage and the ripple over the average. Figure 4.13 shows a very interesting result; here one of the capacitor is sitting at a higher voltage due to a slightly different turn ratio on those modules HF-transformer. This waveform was capture after 30 mins of operation and as we see the

capacitor voltages are not diverging, this confirms that in fact the proposed topology is self-balanced. Notice the ripple difference shown in Figure 4.14, because the prototype is using a level shifted PWM some sub-modules are expected to be used more than others. This reflects to a higher ripple on that sub-module, one way to reduce the overall ripple is to implementing a phase shifted PWM. However this will require more switching, which will in turn reduce the efficiency. Another approach would be to cycle the PWM level shifted every line cycle, with this the maximum average ripple over time can be reduced.

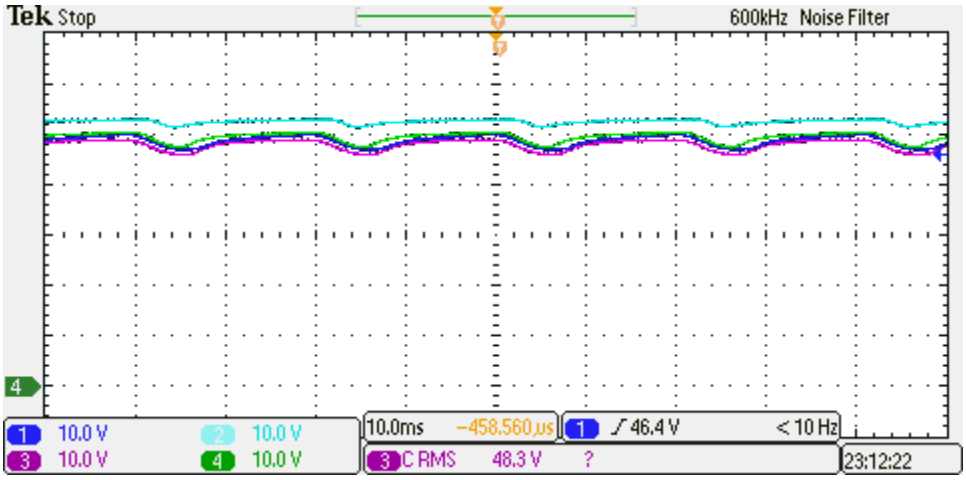


Figure 4.13: Capacitor voltage of 4 different HFL-SM (on the same arm).

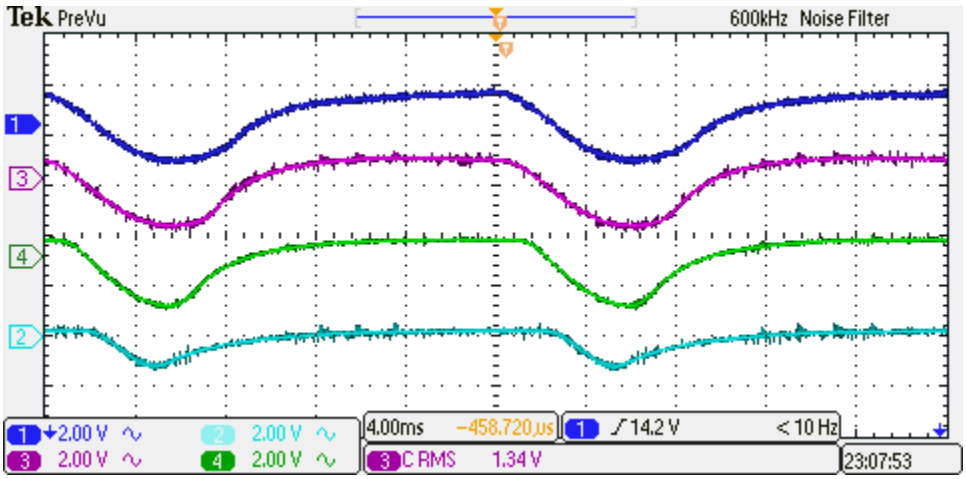


Figure 4.14: Capacitor ripple voltage of 4 different HFL-SM (on the same arm).

Total Harmonic Distortion

Figure 4.15 shows the frequency spectrum of the line-to-line voltage taken at the output of the converter. As expected, there are some peaks in the amplitude spectrum around the PWM switching frequency and its harmonics. The measured THD for the line to line voltage is 13.27%. Similarly, Figure 4.16 shows the amplitude frequency spectrum for the line currents, the THD is reduced to about 4.7%. In the current frequency spectrum, most of the harmonic distortion comes from the lower order harmonics shown in Figure 4.17. For example, the 2nd order harmonic is present due to the capacitor voltage ripple (seen in Figure 4.13) passing into the load due to open-loop control. By implementing closed-loop current control, all of the lower order harmonics can be greatly reduced.

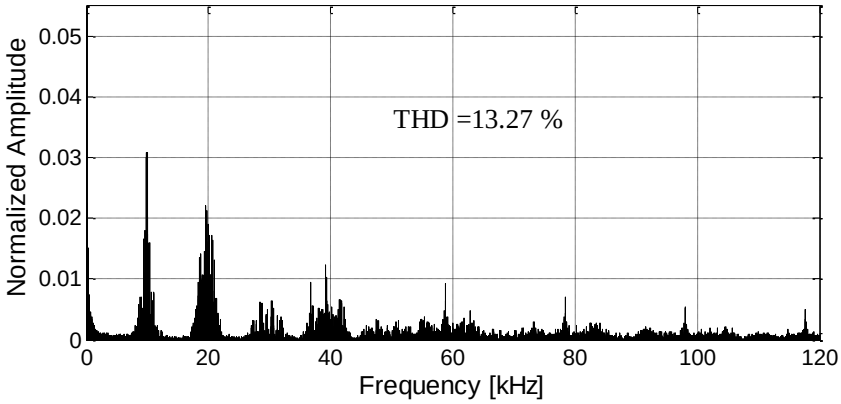


Figure 4.15: Frequency spectrum of measured VLL (High order harmonics).

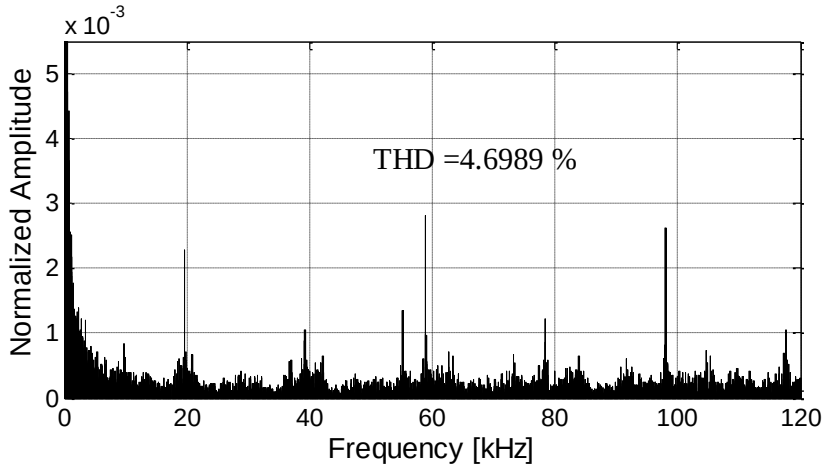


Figure 4.16: Frequency spectrum of measured IA (High order harmonics).

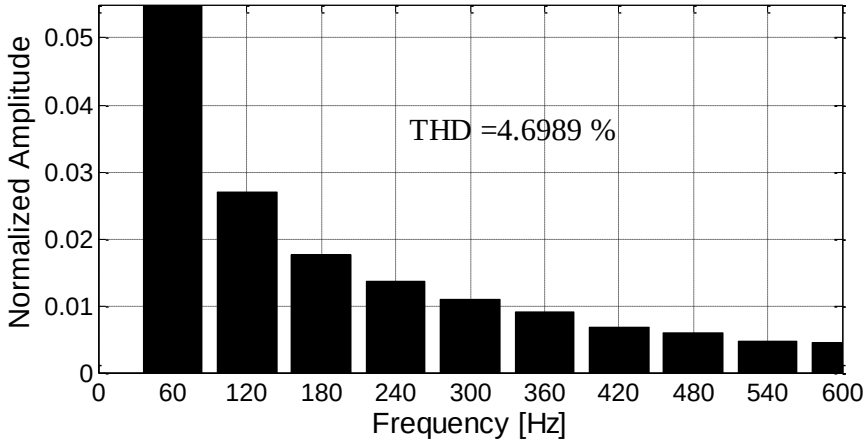


Figure 4.17: Frequency spectrum of measured IA (Low order harmonics).

4.9.3 **Efficiency and Loss Calculation**

From the FFT analysis the RMS value for the fundamental current is found to be 2.17 A with a load resistance of 58.6 Ω.

$$P_{out} = 3\,R_{load}\,(I_{60Hz,RMz})^2 \;=\; 831\,W \quad (12)$$

By measuring the high frequency bus voltage and current the power to the high frequency bus is measured at 959 W. The input power to the inverter was 1029 W (including 5 W drawn by the H-bridge drivers). Using these values, Figure 4.18 summarizes the efficiencies, where η is the calculated efficiency. For the HFL-SMs, the driver power consumption is estimated to be 15W, with the other 113 W corresponding to switching, conduction, and transformer core losses.

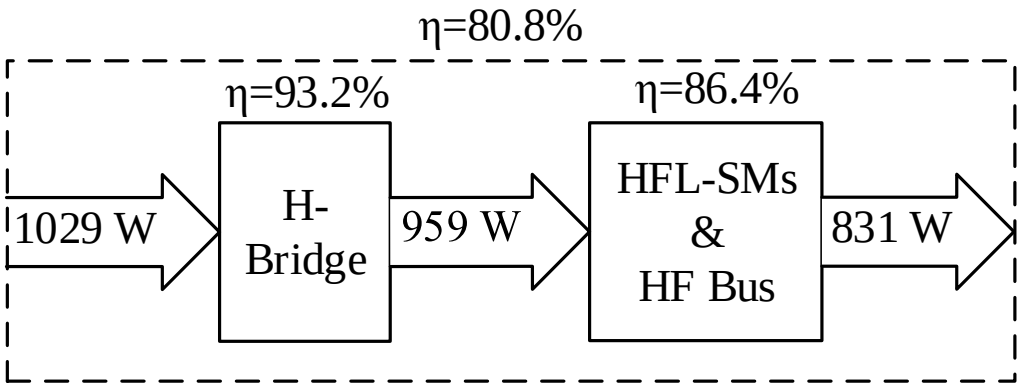


Figure 4.18: Efficiency for hardware prototype.

5 CONCLUSION

The MMC with isolated high-frequency link proposed in this dissertation offers a scalable low voltage DC to medium voltage AC grid interface connection. It has the benefits of an MMC (e.g. low THD, modularity, and scalability), without the need of implementing complicated voltage balancing methods. It also offers a unidirectional power flow and galvanic isolation, making it ideal for PV applications.

Due to the nature of the primary converter it is possible to achieve ZVS and a strategy has been proposed in order to increase the overall efficiency of the inverter. This strategy involves using the transformer leakage inductance to create a resonant transition that will allow for ZVS. Because the primary converter powers all three phases the power and current are constant, this makes the implementation of the ZVS more feasible.

As the switching losses are reduced, the high-frequency transformer core losses become more dominant; with a high number of sub-modules it will become crucial to minimize these. The current design with a ferrite core has core losses that are too high; this is mostly due to hysteresis losses. Core materials like MPP (molypermalloy) and Sendust although slightly more expensive will have fewer core losses.

The functionality of the proposed topology has been confirmed through both simulation and experimental results. An active and reactive power control strategy has been suggested, this will enable the proposed converter to actively support the grid. The MMC with isolated high-frequency link is a promising solution for medium voltage utility scale connections.

5.1 Future Work

The following are proposed as future work to improve the viability of the proposed topology;

1) Optimize the high-frequency transformer design to improve the efficiency.

2) Use wide band gap devices on the primary converter, along with a properly design ZVS resonant transition in order to maximize the primary converter efficiency.

3) For the prove of concept a half-bridge sub-module was used, however a full-bridge sub-module is recommended for future experiments due to its overall lower hardware investment.

4) Implement the proposed controlled strategy for active and reactive power flow into the grid, and confirm proper operation with the experimental setup.

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