Design and Analysis of a Four-Quadrant, High Linearity, Time-Domain, Analog Multiplier

A Thesis

SUBMITTED TO THE FACULTY OF THE UNIVERSITY

OF MINNESOTA

BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE DEGREE OF

MASTER OF SCIENCE

Professor Ramesh Harjani

May 2025

Acknowledgments

This thesis is the culmination of work since late 2023, and could not have been completed without help, encouragement, guidance, and support from many people in my life.

First, I want to thank my advisor and supervisor, Professor Ramesh Harjani. He has offered me advice on a wide variety of topics, from career advice to technical discussions to wisdom about how best to move forward through the many challenges I have come across in the research process. Under his guidance, I have developed into a far better engineer and analog designer than I was when I started. More importantly, working with him has only built my passion for this field further, and I am eternally grateful for that gift.

I would also like to thank the members of my thesis committee, Professors Ted Higman and Michel Janssen. Both of them have volunteered some of their valuable time to help me finish my degree, and I greatly appreciate it. Perhaps more than that, I have appreciated what I have learned in classes with each of them, as both are founts of knowledge gained from long experience. I would also like to thank Professors Sarah Swisher and Rhonda Franklin, whose classes helped me realize that analog circuit design is passion that I want to spend my working life on.

The other members of my research lab have also been valuable parts of my work. Yashodharma, Sanjoy, Bosi, Surya, and Yangcheng have all been good friends and colleagues, and have humored my questions at all times. I would like to specifically mention Yashodharma Parthaje, who as the

one with the desk adjacent to mine had to suffer the most interrogation from me, but has always been a fantastic help in my work.

Finally, I would like to thank my girlfriend Alyssa, who has always made it her mission to help me in the difficult times. She has never stopped cheering me on and has lifted me up when I felt down. I would also like to acknowledge my parents Heather and Brandon, and my brothers Owen and Isaac, for their love and support as I have been hard at work on this project. My mother, in particular, has always supported me and my goals my entire life, and I would not have gotten to where I am today without her.

Soli Deo gloria

Abstract

AI and communications circuits require correlation circuits that use a MAC (multiply accumulate) operation as their core. In the MAC, the multiplication circuit tends to be the most power hungry and most critical component compared to addition. Currently, digital implementations of the circuits are very power hungry. Analog circuits offer opportunities to save power, particularly for lower SNR use cases. However, in modern processes, lowering supply voltages and second-order effects have degraded the linearity and dynamic range of analog circuits. This work presents an analog multiplier capable of high linearity and range, with a maximum input magnitude of $400\,\text{mV}$ and THD% of $0.014\,\%$. This design achieves this by using a novel time-domain approach, where the input voltages are multiplied by integrating a current over a length of time. This concept offers great promise for future development and adds to the capabilities of time-domain circuits.

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List of Acronyms and Definitions

Notation	Description
DSP	Digital Signal Processing.
MAC	Multiply-and-Accumulate.
SFDR	Spurious-Free Dynamic Range.
SNR	Signal-to-Noise Ratio.
THD	Total Harmonic Distortion.
Time-Domain Circuit	A circuit that encodes the input as a time interval, rather than a voltage or current.
Time-Signal	A PWM signal, where the value is linearly proportional to the pulse width.
VLSI	Very-Large-Scale Integration.
VTC	Voltage-to-Time Converter.

Chapter 1

Introduction

In modern chip design, the greatest challenge faced is power consumption. Every area of computing is affected by the issue. In high-performance processors, the clock speed is limited by the power dissipation of the die. In mobile and Internet-of-Things applications, the lower power consumption means longer battery lives. In data centers and server farms, engineers struggle to supply high-quality power supplies for the massive loads and to remove the incredible amount of heat generated, to the point of considering placing the computers underwater or in the Arctic Circle. At the same time, more processing is always demanded, especially with the advent of massive neural networks and machine learning since 2022. Most importantly, most of the tasks done on computers do not require many bits and high precision that comes with that, which gives analog circuit design a way to improve the situation.

Analog circuits have been shown to be more efficient than digital circuits at relatively low signal-to-noise ratios [2]. This thesis aims to introduce the concept of using analog circuits to create and process signals valued in time, rather than voltage or current. By doing this, opportunities may arise to both improve linearity and decrease power consumption. This introductory chapter will discuss the motivations and goals of this research in more detail. Chapter 2 will give an

overview of many prior methods of analog multiplication that have been published. Chapter 3 will discuss the concept of time-signals and how one can make a multiplier with them. Chapter 4 will show measurements from simulations of the analog multiplier, designed in Global Foundries' GF22 process. Finally, Chapter 5 will review the measurement results and point the direction towards further improvements and development of the concept.

1.1 Development of Signal Processing

Signal processing underpins the entire modern world. Both analog and digital signal processing are part of any technology used today. High-speed communications rely on processing to extract information from the transmitted signals through noise and distortion. MRI machines, super-resolution microscopy, and digital cameras all use signal processing to construct images from the signal they receive from sensors. No matter the use case, signal processing systems are built up from certain basic building blocks, like adders, multipliers, and correlators.

At first, signal processing was done entirely in the analog domain. Addition, multiplication, filtering, and other processing needs were completed using combinations of resistors, capacitors, and operational amplifiers. These methods were the only option, as the size and cost of digital computers ruled them out for any applications that needed be portable, real-time, or mass-manufactured. At first, discrete components were used to create the circuits needed, but the introduction of the integrated circuit allowed for the circuits to be made much smaller. Until the advent of modern microcontrollers, G_m-C filters and switched capacitor circuits were at the forefront of signal processing.

Starting in the 1980s, digital methods finally became cheap and fast enough to beat analog [9]. Digital signal processing (DSP) continually increased market share, and today far more signal processing is done in digital than in analog. Digital methods came with certain advantages, like

the ability to reconfigure the system almost at-will, without having to reorder components or in the case of integrated circuits, create an expensive new chip design. For high signal-to-noise ratio (SNR) applications, digital also became more power efficient. Since then, analog signal processing has been phased out, and today is most commonly seen in the most high-speed applications, like RF and wireline transceivers. Even in these areas, DSP is being looked to to improve performance.

Though not a new idea, in recent years neural networks and artificial intelligence has developed into an entirely new market for computing. Modern large language models (LLMs) use massive neural networks to create their responses, but each neuron uses the same basic building blocks that are already used in signal processing. For example, neurons work by looking at their inputs (either from the input to the system or from the previous layer of neurons), weigh each by a factor, and then check if the result is greater than a threshold. The basic operations are just addition and multiplication, repeated over a trillion times in the largest modern LLMs. The tiniest amount of power savings per operation results in massive savings overall at such scales.

1.2 Power Issues in Modern Processing

As stated prior, the largest problem faced today in computing is power consumption. In CPUs and GPUs, the clock speeds are primarily limited by the ability of the die to dissipate heat, as losses rise linearly with frequency in digital logic. The long battery lives of mobile consumer products today are only possible through the careful use of low-power design, but they are limited in their capabilities by their need to draw as little current as possible. Scaling the semiconductor process has, for a long time, worked for helping these issues. Figure 1.1 shows the trends since the early 1970s, and shows that since 2005 the power consumption of consumer processors has stayed fairly constant. However, the performance of the processors has only improved in that time interval. This has been done primarily by the continued scaling of semiconductor processes.

In 2005, the newest node was 65 nm; in 2025, it is 2 nm. With that reduction in size has come reductions in capacitance and supply voltage, lowering the power consumption by an individual transistor. However, the improvements have begun to disappear, as the rate of scaling the metal interconnects has not kept up with the transistors themselves. This means that parasitic capacitance has become a dominant source of power loss, as the capacitance between the metal routes must also be charged and discharged with the gate of the transistor. At the same time, the shrinking of the transistor has introduced large amounts of leakage losses, due to effects such as drain-induced barrier lowering (DIBL).

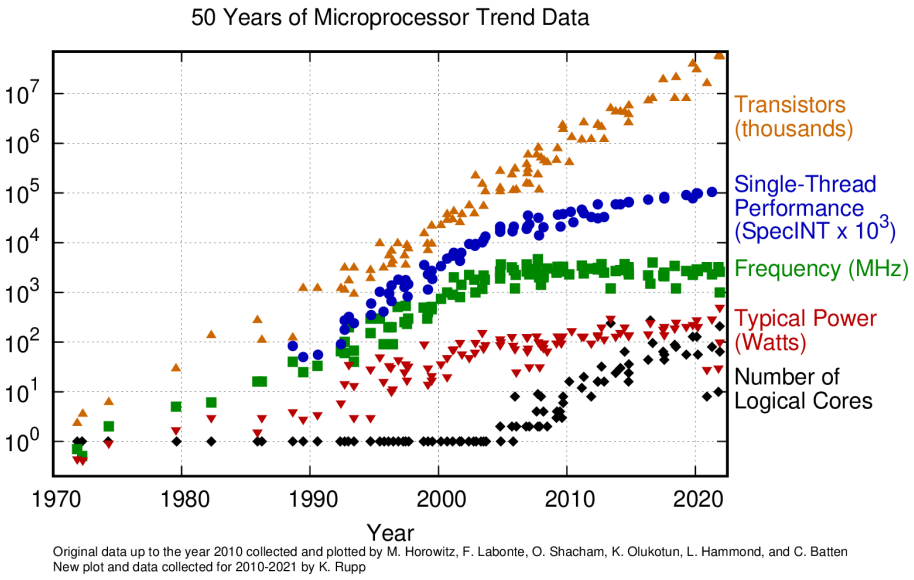


Figure 1.1: VLSI Trends Over 50 Years. Source: [1]

To reduce power consumption, new methods are being examined for use. Some ideas rely on continued technology progression and the introduction of new transistor structures or processes, like the advent of nanosheet transistors. Other methods aim to modify the digital circuits themselves, such as in adiabatic logic circuits. The method investigated in this paper is a third option, looking

to complete the same operations without any digital logic being involved. Analog methods are one of these alternative paths.

1.3 Analog Signal Processing

Analog circuits have a major advantage over digital circuits: they can run on near-zero power. At the highest level, this can be understood by realizing that an analog circuit can often work the same with a lower level of power, if everything is scaled correctly and bandwidth limitations are accepted, but digital circuits are limited by the energy cost of charging and discharging their capacitors. However, this approach ignores the practical aspects of system design, such as SNR requirements. Eric Vittoz examined the issue from that perspective. He pointed out that the power consumption of digital circuits is directly tied to the number of bits required to reach the SNR level required, while analog circuits consume power based on the intrinsic noise produced by the device. Because of this, digital circuits scale logarithmically, while analog circuits do so linearly.

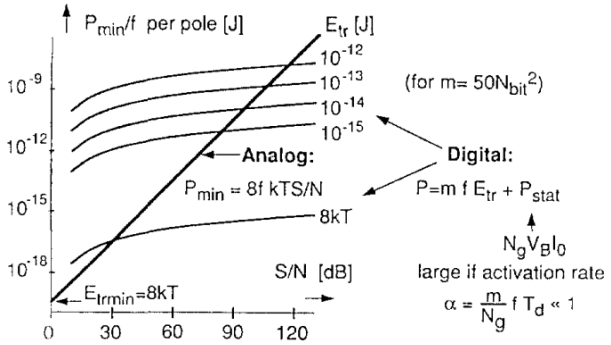


Figure 1.2: Comparing Filter Implementations [2]

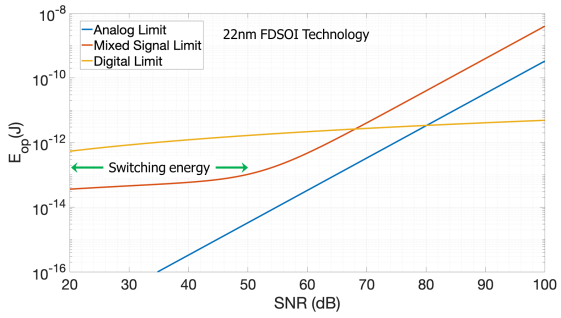


Figure 1.3: Comparing Digital to Mixed-Signal Implementations of a MAC Circuit in a 22 nm Technology [3]

In Figure 1.2, Vittoz shows that for filtering applications, analog circuits can be more power efficient, depending on the SNR requirement and the node used. The transition energy loss, E_{tr}, is

dependent on the capacitance of the transistors used. By assuming that the number of transistors needed in the digital circuit scales quadratically, the digital power consumption increases logarithmically with SNR. Analog circuits, on the other hand, are limited by the thermal noise produced by the devices, and their SNR scales linearly independently of process. This means that, up to a point, analog circuits can be more efficient than digital equivalents.

Figure 1.3 shows this comparison in a 22 nm FDSOI process. In a theoretically perfect world, analog circuits beat digital up to SNR levels around 80 dB. However, even Vittoz acknowledges that the only analog circuit to ever reach the theoretical limit is the RC filter [2]. The overhead needed to bias amplifiers, generate clocks, and other supporting functions adds power. These overheads exist in digital too, but the error is less severe compared to analog. This means that the real limit in analog may be closer to 70 dB or lower. Even accounting for that, however, analog circuits can still definitely compete in the range of low SNR applications.

What are those low SNR applications? Simply put: anything that designers can get away with. Why design for 80 dB, with the power consumption to match, when 40 dB works just as well? Many systems fit this approach. The most common today is the neural network, where in digital implementations precisions as low as 1 bit are being used. Analog neurons could easily compete with their digital equivalents, and have been investigated. Some recent results have shown power improvements by nearly 3 orders of magnitude using analog circuits in subthreshold operation [10]. Another possibility is in true low-power signal processing, such as in correlators. Analog correlators have been shown to greatly beat digital correlators in terms of their performance-to-power ratio [11].

1.4 Analog Multiplication

One of the most common operations in computing is multiplication. Multiplication is also one of the most power-hungry operations, as most implementations require a large number of successive addition operations. For example, if using an array multiplier, an N bit multiplication requires $N(N-1)$ individual 1-bit addition operations. Thus, for even just an 8-bit multiplication, an array multiplier would require 56 full adders just to generate the partial products. There are more efficient methods, but they will still be expensive and as shown in Figures 1.2 and 1.3, not necessarily needed. Though it is unlikely that all digital multiplication could be replaced (or that it would be desirable to do so, as digital has advantages of its own), modern chip design is moving towards specialization in all things. The demand for specialized performance is what has fueled the industry-wide move towards chiplets, aiming to create multiple specialized chips that create a processor or ASIC as a unit. Analog methods offer one such way to specialize.

The application of analog circuits discussed in this thesis is for the multiplication of real numbers. By representing the numbers as voltages or currents, analog multipliers can give the correct output as an analog signal, which can be converted back. To multiply complex numbers, one only needs four normal analog multipliers working in combination with each other. There are many ways to construct such a multiplier, and many of the most popular and explored options have been discussed in Chapter 2. Multiplication is a useful operation on its own, but it is especially useful when considering multiplying two signals that vary in time. If one multiplies two sine waves, the output of the multiplication results in a sum of sine waves at new frequencies:

$$cos(\omega_1 t)cos(\omega_2 t) = \frac{1}{2}(cos((\omega_1 - \omega_2)t) + cos((\omega_1 + \omega_2)t)) \tag{1.1}$$

This is the fundamental concept behind mixers in RF design, though they have different goals

from signal processing applications. The biggest distinction is that in mixers, the amplitude of the local oscillator input should not affect the output magnitude, while in multiplication that is necessary. However, testing multipliers like mixers makes it very easy to measure linearity, as the distortion causes spurs to exist at other frequencies not predicted by Equation 1.1. The methods for measuring it are discussed in Chapter 2 and will be used throughout this work.

Specifically, this work introduces a method of using lengths of time proportional to one of the multiplier inputs to complete the calculation. These lengths of time are represented as pulse widths, as the technique relies on encoding the input signal onto a pulse train via pulse-width modulation (PWM). By using the variable lengths of time to control how long a current can charge a capacitor, multiplication is achieved. The specifics of this process, as well as how the idea can be extended to multiplying both positive and negative numbers, is discussed in Chapter 3. The greatest advantage of the ”time-domain” approach is that the resolution actually improves as semiconductor nodes shrink. This is because the edges of the pulses cain more definition as circuit bandwidth increases due the lower capacitances. Furthermore, this resolution can be increased in exchange for slowing the system down by increasing the maximum length of the pulses, decreasing the effect of edge noise and distortion on the magnitude of the overall signal. Smaller nodes exhibit higher amounts of noise, but the time-domain part of the multiplication is immune to normal amounts of voltage noise, only being affected by jitter. The circuits also scale far better than other methods, as the time durations are marked only by high-low transitions, not any specific voltage or current output. This means that no matter the voltage supply, the resolution of the time-signal is unaffected.

1.5 Aims of This Work

This work aims to explore the implementation of time-domain methods in analog multiplication, creating a new structure for further exploration. I do this by first discussing the implementations

of analog multiplication that have been used before, then moving into the time-domain method. Simulation results will be shown from a 20 nm process, and the conclusions that can be drawn from those simulations will be discussed.

The goal of this work is not to show performance that is superior to prior methods. Rather, this works aims to setup future exploration of these ideas. Although some work has been done on time-domain multiplication, it has been done purely from a digital perspective [12]. This work looks to introduce a new block into the time-domain system, which can already create ADCs, PLLs, and many other circuits. In doing this, inspiration is drawn from Qian Chen's VTC paper [6], which is used to create the time-domain behavior. This work differs in important ways, however. First, this design is entirely analog, without any digital control. Secondly, this paper creates a four-quadrant multiplier, where [12] only creates a one-quadrant. Thirdly, this work prioritizes linearity and dynamic range, rather than the operating bandwidth or the power consumption (though they are both still concerns). This work will show that a time-domain multiplier is both possible and advantageous in achieving these goals, as well as identify pitfalls and offer ideas on their mitigation.

This work is limited, unfortunately. Due to time constraints, very few of the suggestions that will be discussed to mitigate issues such as delay dispersion were implemented. Similarly, layouts were not finished for the blocks simulated in this work, and there is no non-simulated measurement data. As such, this work focuses on the theory and simulation results that were achieved. Future work can build on the methods and results given here to further broaden the horizons of time-domain circuits.

Chapter 2

Prior Work in Analog Multiplication

When designing an analog multiplication circuit, several factors must be balanced against one another. Several of these, namely power consumption, speed, and area, are common issues with almost all circuit designs, while others, like linearity and noise, are specific to signal processing applications. While most signification research into analog multiplication was published prior to 2000, new methods have been developed in the last quarter of a century which allow for improvements across nearly all areas of circuit design. Some of these developments resulted from process improvements, as the continual scaling of MOS transistors has allowed power consumption, area, and speed to all improve. At the same time, new transistors structures, like silicon-on-insulator (SOI) and FinFET, have allowed for better control over the transistor's underlying physics, reducing leakage and opening up opportunities with the device body terminals.

Most of the modern developments can be applied to the older designs for analog multipliers. For example, having smaller devices reduces the net capacitance of the design, allowing for circuits to operate at lower power and in a smaller area than previously, but reach similar speed targets. Similarly, innovations with SOI have allowed for the reduction of threshold voltages by biasing the body in ways that previously would have allowed conduction of the body diode. These advantages

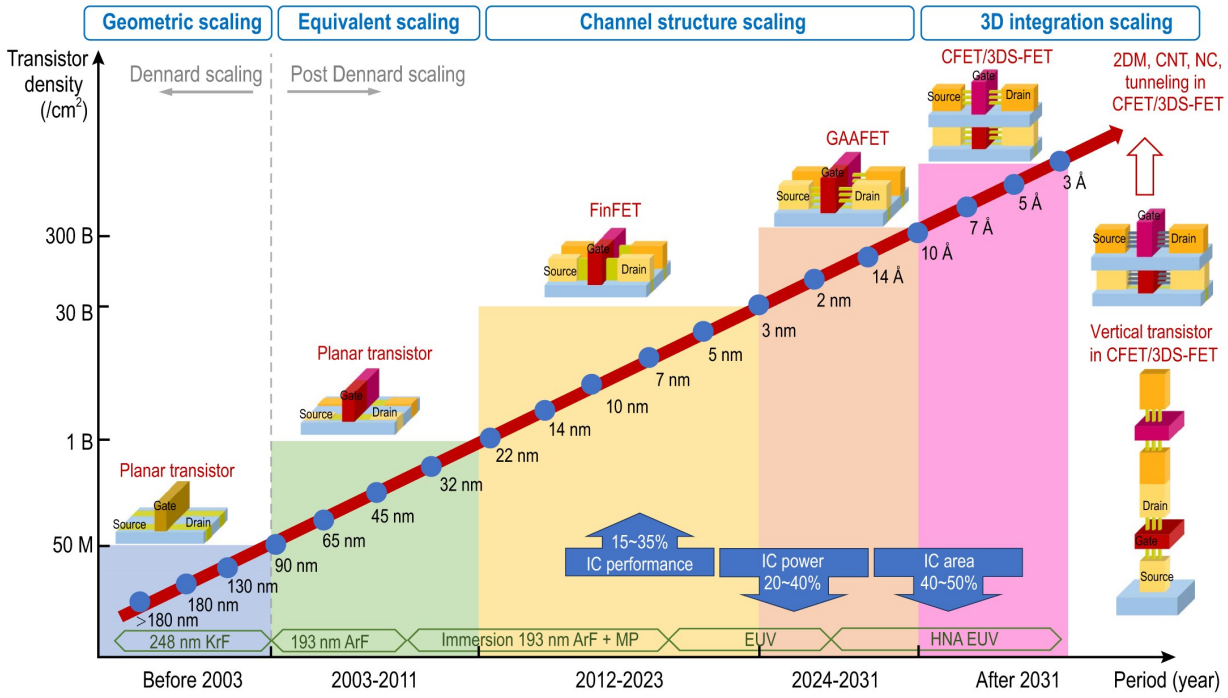


Figure 2.1: Transistor Scaling Over Time [4]

can be applied directly to older designs, without any structural changes.

However, some aspects of scaling have not benefited circuit design. The same scaling that helps reduce power and area cost introduces short-channel effects that degrade individual transistor performance. Some effects are simply worse versions of problems with long-channel technologies, such as increased leakage due to the shortening of the channel energy barrier. Lowering the voltage supply turns certain architectures impractical, as stacking of transistors is limited. Others are problems that only developed into significance as channel lengths dropped below 1 µm, such as drain-induced barrier lowering (DIBL) or velocity saturation. These new effects must be mitigated in order to see benefits with modern nodes.

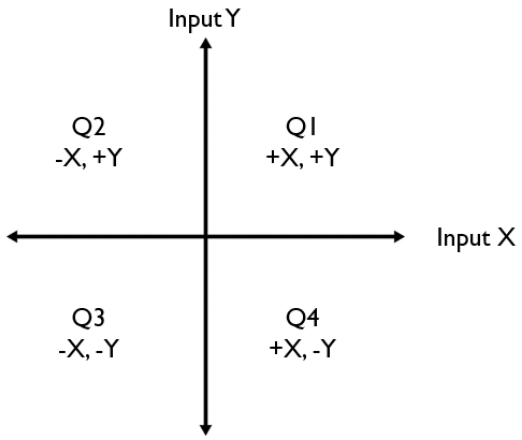


Figure 2.2: Input Regions of a Multiplier

2.1 Types of Analog Multipliers

Analog multipliers can have a variety of capabilities. The most important of these is how many quadrants the multiplier is capable of calculating for. Quadrant refers to the quadrants of a Cartesian plane like the one in Figure 2.2, where each axis represents the value of one of the inputs. A one-quadrant multiplier can only multiply within one quadrant, generally two positive values. A two-quadrant multiplier can multiply one purely positive value with one real value (positive or negative). Generally, four-quadrant multipliers are required, which can multiply any two real values. This is a requirement for signal processing, as most signals are best represented with real values.

With a four-quadrant analog multiplier, digital signal processing (DSP) operations can easily be replicated. The basic building blocks of DSP, multiply-and-accumulate (MAC) operators, can be made in analog and chained together to create both FIR and IIR filters. Techniques from switched-capacitor circuits can be used to pass the values between MACs. To make an analog multiplier that can multiply complex values, one only needs four four-quadrant multipliers to make one larger complex multiplier, which can multiply any two complex values.

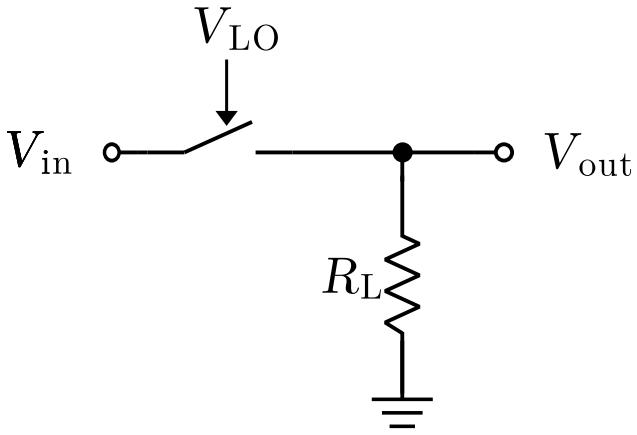


Figure 2.3: Switching Mixer

2.1.1 Comparison to Mixers

While traditional analog multipliers have not been a large topic of research for decades, RF mixers have been. Both function by multiplying two signals together, but with completely different goals. This can be easily seen by looking at the most basic mixer design, the switching mixer. As shown in Figure 2.3, a switching mixer works by modulating an input signal with a local oscillator signal (LO) that controls a switch. If the switch is on (V_{LO} is high), then V_{in} passes through, otherwise the output is 0. This can be represented as Equation (2.1).

$$V_{out} = V_{in}V_{LO} \tag{2.1}$$

At a surface level, this appears to be exactly the multiplication operation that is needed. However, this is nearly useless for signal-processing applications, because the LO input cannot carry any magnitude information. Thus, while the circuit is linear with V_{in}, it is completely nonlinear for V_{LO}. In RF, this is ideal, because the magnitude of the LO should not affect the output, only its frequency. However, for signal processing applications, magnitude is one of, if not the most, important signal characteristics. This means that multiplier circuits can be used as mixers, but not

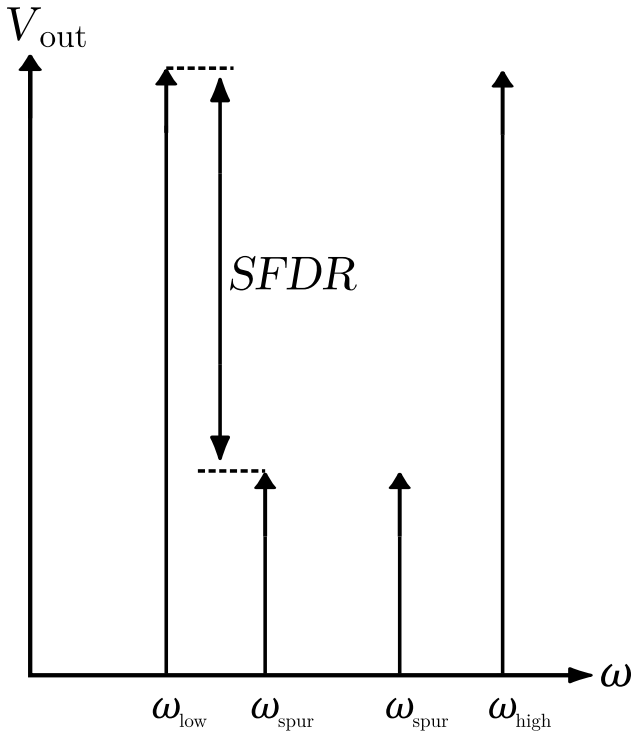


Figure 2.4: Measuring SFDR in the Frequency Domain

necessarily the other way around. The best example of this would be the Gilbert Cell, which will be introduced in Section 2.3.1.

While most mixer-based techniques can't be used for signal processing, techniques for characterizing them can be used. The most meaningful technique that can be borrowed is the concept of Spurious Free Dynamic Range (SFDR). SFDR is a frequency domain measure of distortion, giving the range from the largest desired signal component to the largest "spur" distortion in the output. This is seen in Figure 2.4. A larger SFDR value is directly related to improved linearity, a key multiplier characteristic and can be used as a performance metric. Other methods for measuring linearity exist,but generally, they either borrow concepts from data-converter analysis, like integral nonlinearity, or they measure a maximum percent error from the ideal output [13–16].

2.2 Diode-Based Methods

The first analog multiplier in published IEEE research was submitted in 1957, and used transformers and a diode rectifier to multiply RF signals [17]. The obvious drawback of this method was that it could not multiply broadband signals, as DC would not conduct through the transformers. Soon after, circuits were published that relied on the exponential behavior of diode junctions in large-signal operation. These methods do not rely on small-signal approximations for design, like the designs in Section 2.3 do, but rather work off of the fundamental properties of the PN junction.

One type of circuit uses diodes as a part of a feedback network to create log and antilog amplifiers. First, the logarithm of each circuit is taken, and then the sum is taken of the two. The antilog is then taken of this result to finish with the correct output. If the difference is taken rather than the sum, then the circuit becomes an analog divider rather than a multiplier. This has a massive flaw, however: the feedback only functions for positive inputs. This means that the log-antilog structure is just a one-quadrant multiplier, and as such not usable for most signal processing.

Another way utilizes the BJT's translinear principle. If a set of devices in a closed loop have an exponential voltage-current relationship, then the product of the currents going in one direction around the loop is equal to the product of the currents going the other direction around the loop [18]. Via manipulation of this property:

$$\prod I_{cw} = \prod I_{ccw} \tag{2.2}$$

If $I_{cw} = I_{unit} I_{out}$ and $I_{ccw} = I_x I_y$, where I_{unit} is an introduced unit current:

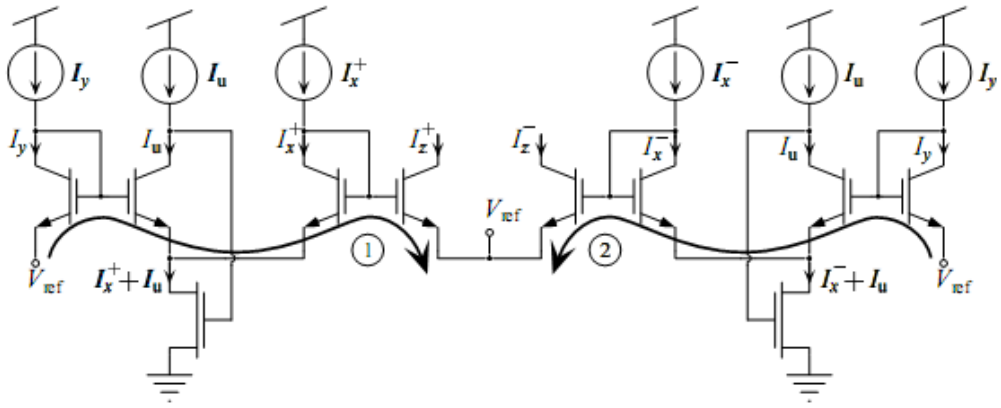


Figure 2.5: Two-Quadrant Translinear Multiplier [5]

$$\prod I_{unit} I_{out} = \prod I_x I_y \tag{2.3}$$

$$\prod I_{out} = \prod \frac{I_x I_y}{I_{unit}} \tag{2.4}$$

$$I_{out} = I_{x,norm} I_{y,norm} \tag{2.5}$$

Thus, an output current can be created that is the product of the two input currents, normalized by some unit current that is definable. This means that not only is such a circuit linear in the ideal case, it also has variable gain, if the unit current is not held at a reference. This is another benefit that earlier diode-based designs did not have. Figure 2.5 shows an basic model of such a design.

The translinear principle relies on the exponential voltage-current relationship that BJTs and diodes exhibit. It is well understood that MOSFETs, when operated in the weak-inversion region, can exhibit the same type of exponential behavior. Indeed, this exact idea was tested several times as interest in MOSFETs as the primary semiconductor device grew [18, 19]. While the principle was successfully extended to CMOS, as shown via experimental results, the scaling of transistors in modern ASICs has effectively eliminated this possibility. As transistors and supply voltages

have shrunk, the threshold voltages have shrunk with them. This means that the voltage range in which the device operates in deep weak-inversion is now less than a few hundred millivolts at most. Substantial signal magnitude reductions severely degrade the dynamic range of the circuit, as the noise and distortion components become larger relative to the signal. To maximize that range in modern CMOS designs, nearly the full supply voltage range, rail-to-rail, must be used for the input and output signals. Weak inversion designs cannot do this, and as such they fall short of the performance reached by transconductor-based methods.

2.3 Transconductor-Based Methods

In modern processes, MOSFETs have scaled very well, whereas diodes and BJTs have not. Thus, it is desirable to design with MOSFETs as much as possible, and that eliminates most diode-based methods. Using MOSFETs in weak inversion to replicate the translinear principle also does not work well, as it unnecessarily restricts the dynamic range of the multiplier. This means that new methods of multiplication must be found that do not rely on exponential properties. The basic building block in analog signal processing has been the transconductor, and so this offers a new area to explore.

As discussed by Gunhee Han and Edgar Sánchez-Sinencio [20], there are two ways to achieve four-quadrant multiplication using transconductors. The difficulty in designing multipliers is that real signals on chips have non-zero common-modes. This means that simply multiplying two voltages together can't work, as shown:

$$(X + x)(Y + y) = XY + Xy + xY + xy \tag{2.6}$$

where X,Y are the common-mode voltages and x,y are the differential signal voltages. This is

easy to see when using a multiplier as a mixer, as the output will have both the desired "mixed" frequencies ($f_x + f_y, f_x - f_y$) and the original input frequencies, which originate from the terms Xy, xY, on top of a DC offset due to the XY term in Equation 2.6. Thus, these extra terms must be canceled out, which is what is analyzed by Han and Sánchez-Sinencio [20].

The first method involves using a set of four single-quadrant multipliers. Each is fed one possible combination of the differential inputs of V_x and V_y:

$$\begin{aligned} & [(X+x)(Y+y)+(X-x)(Y-y)] \\ - \quad & [(X+x)(Y-y)+(X-x)(Y+y)] \qquad (2.7) \\ = \quad & (2XY+2xy)-(2XY-2xy) \\ = \quad & 4xy \qquad (2.8) \end{aligned}$$

Equation 2.8 shows the result is just the product of x and y, with a constant gain. In real applications, difficulties arise when ensuring complete cancellation. This requires that good matching is achieved between the four single-quadrant multipliers, as well as balanced addition and subtraction operations. These are possible and well-understood problems in analog circuit design, however, and can be solved. This method is used for implementing the time-domain multiplier, discussed in Chapter 3.

The second method faces the same problem of cancelling the additional terms, but instead can be achieved by squaring the sums and then adding/subtracting them together.

$$
\begin{aligned}
& [(X+x)+(Y+y)]^2 + [(X-x)+(Y-y)]^2 \\
- \quad & [(X+x)+(Y-y)]^2 - [(X-x)+(Y+y)]^2 && (2.9) \\
= \quad & 8xy && (2.10)
\end{aligned}
$$

This method completely avoids any multiplication operations, but does require a squaring. This is achievable in large signal from the fundamental square law of MOSFETs, where:

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{2.11}$$

Ignoring all other effects on a MOSFET, this produces a perfect squaring of an input voltage. Then, all that is needed is to produce the addition operations. However, in reality this is much more complex. Especially in short-channel devices, second-order effects corrupt the square law to the extent that even without channel length modulation, the MOSFET cannot produce a perfect square. Velocity saturation distorts the higher end of the V_{gs} range, while DIBL and leakage distorts the lower end. Including the device's finite output impedance only worsens the performance. As such, modern designs should prefer the method in Equation 2.7.

2.3.1 The Gilbert Cell Architecture

The most famous analog multiplier structure is the Gilbert cell, named after its inventor Barrie Gilbert [21]. Its design, seen in Figure 2.6, is based on the cancellation method shown in Equation 2.7, though it is hard to recognize. To gain intuition about the circuit's operation, a first step is to simplify the differential pairs into perfectly linear current steering circuits, with some transconductance G_m. The lower differential pair steers current down one side of the other, with the purpose

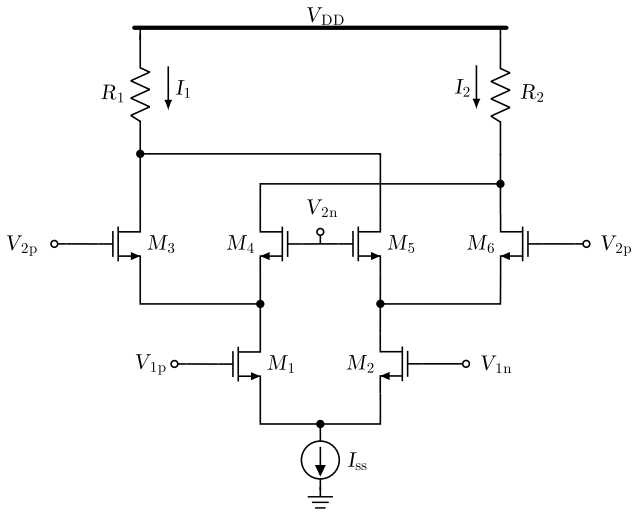


Figure 2.6: The Gilbert Cell Multiplier

of modulating the transconductance of the top differential pairs, as $G_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{tail}}$. This creates the multiplication of terms, as the tail current for the second level of differential pairs is proportional to V_1. Thus, the differential output current for the top left pair is:

$$I_{do} = G_m(V_1) * V_2 \tag{2.12}$$

Or, if examining just individual output currents rather than a differential output current:

$$I_{pp} = G_m(V_1^+) * V_2^+ \tag{2.13}$$

$$I_{pn} = G_m(V_1^+) * V_2^- \tag{2.14}$$

Similar expressions exist for the other top differential pair, giving expressions for I_{nn}, I_{np}. Looking at all the output currents in the second level of differential pairs, it can be seen that each matches with a term from Equation 2.7. For example, the currents in Equations 2.13,2.14 corre-

spond to the terms $(X+x)(Y+y)$, $(X+x)(Y-y)$, respectively. Then, these currents are summed at the output notes, creating the differential output current $I_{out} = I_1 - I_2$.

Careful reading of this work reveals an shortcoming of the concept. It is known that the G_m of a differential pair is proportional to $\sqrt{I_{tail}}$, which means that it is also proportional to $\sqrt{V_{in}}$. This means that the individual output currents are not proportional to V_1V_2, but rather $\sqrt{V_1}V_2$ in large-signal operation. A square-root is not linear, so the cancellation necessary to achieve pure multiplication is no longer perfect. For some designs, this may be tolerable, especially if small signal magnitudes are expected which keeps the square root approximately linear. The square root lowers the dynamic range of the design by increasing distortion, and the solution of lowering the input magnitude decreases SNR, lowering the range as well. Unfortunately, this tradeoff is an intrinsic part of the design.

These concepts were tested in a simulation of a SOI 20nm process. Designing with a tail current of 5uA, various structures were tested, including: the basic structure, the basic structure with resistor degeneration, a Gilbert cell with the bottom stage replaced with a feedback linearized transconductor, and combinations of these structures. The measured SFDR in simulation was not able to surpass 36dB of dynamic range as shown in Figure 2.7, due to large third-order nonlinearity-induced harmonics. Increasing the tail current would have improved the linearity, but it also would have increased power consumption. This is not tenable, as a major benefit of analog signal processing is that it is low-power. Another issue was created by forcing a limited input signal magnitude, in order to prevent the transistors in the differential pairs from entering subthreshold operation. A signal swing of just 50mV was used in order to prevent issues and keep the pairs as linear as possible, but this small of a swing is vulnerable to noise and distortion effects.

The Gilbert cell's biggest advantage is its simplicity; its most basic implementation requires just 7 transistors. This simplicity is generally conducive for high-speed operation as well, which

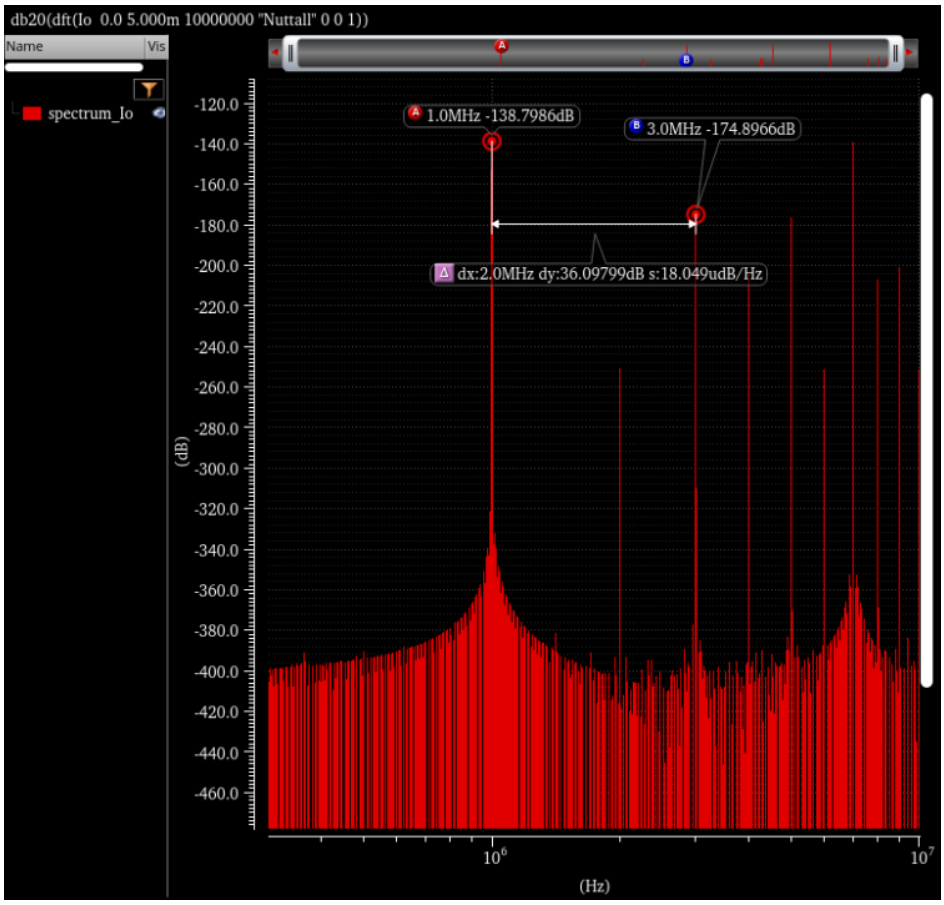


Figure 2.7: Spectrum of the Output Current of a Gilbert Cell, Designed in a 20nm Process

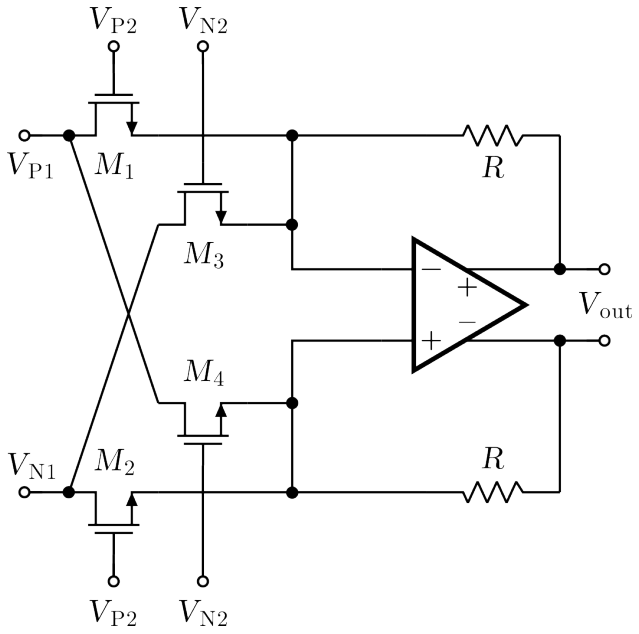


Figure 2.8: The Triode-Mode Multiplier

is another benefit. It also does not require feedback or clocking, two systems that often create new problems to solve. It's largest drawback, besides the intrinsic linearity issues, is the large voltage headroom requirement. Earlier, it was discussed that in order to maximize multiplier performance, the signal's range should cover as much of the voltage supply range as possible. The Gilbert Cell implementation in Figure 2.6 has a tolerable output swing of $V_{out} = V_{DD} - 3V_{OV}$, if the overdrive voltage is constant for all transistors and the current source. Say that $V_{DD} = 0.8V$ and $V_{OV} = 0.1V$, reasonable values for a 20nm process. This leaves the output swing limited to just 0.5V, nearly half the supply range. The situation worsens if any steps to improve linearity are taken, such as adding degeneration resistors on the differential pairs or cascoding, as these consume additional voltage. The Gilbert Cell is simply not practical in modern ASICs.

2.3.2 The Triode-Mode Architecture

Another method is based on using transistors operating in triode to create a variable gain amplifier. This is a modified version of a differential integrator published by Czarnul [22]. An input (V_1 in Figure 2.8) experiences a gain that is modulated by another input (V_2). The result is multiplication. Furthermore, the DC gain of the multiplier is easily configurable by changing the feedback resistance R. Deriving this is straightforward, as the structure of the multiplier is essentially just an inverting amplifier, oftentimes the first amplifier configuration learned by many electrical engineers.

If M1 and M2 have small-signal resistances R_p, and M3 and M4 have small-signal impedances R_n, then:

$$|V_{out}| = R(I_{top} - I_{bot}) \tag{2.15}$$

$$I_{top} = \frac{V_{1p}}{R_p} + \frac{V_{1n}}{R_n} \tag{2.16}$$

$$I_{bot} = \frac{V_{1p}}{R_n} + \frac{V_{1n}}{R_p} \tag{2.17}$$

Rearranging terms in Equation 2.15, one can reach:

$$R\left(\frac{V_{1p} - V_{1n}}{R_p} - \frac{V_{1p} - V_{1n}}{R_n}\right) = RV_1\left(\frac{1}{R_p} - \frac{1}{R_n}\right) \tag{2.18}$$

Substituting in the equation for the small-signal resistance in triode finishes with:

$$RV_1(\mu_n C_{ox}\frac{W}{L})(V_{2p} - V_{th} - (V_{2n} - V_{th})) = \mu_n C_{ox}\frac{W}{L}RV_1V_2 \tag{2.19}$$

Thus, the gain of the multiplier is equal to $\mu_n C_{ox}\frac{W}{L}R$. Unlike in the Gilbert Cell, there is no

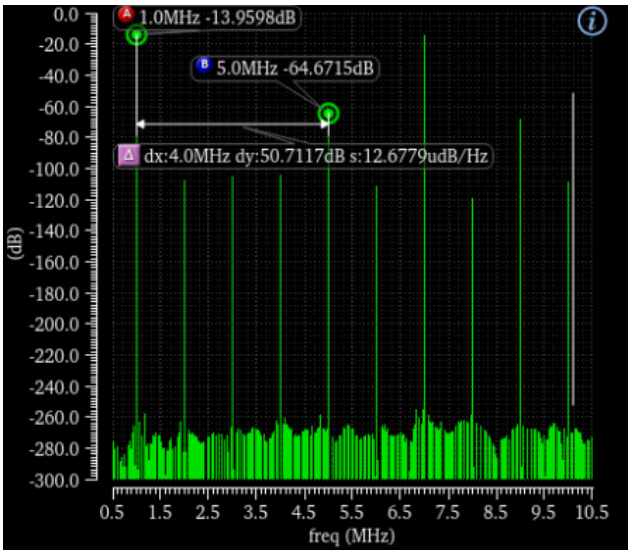


Figure 2.9: Spectrum of the Output Voltage of a Triode-Mode Multiplier, Designed in a 20nm Process

intrinsic nonlinearity built into the design. However, the reality of using of triode-mode transistors is that their resistance does not change linearly with either V_{gs}, despite the equations. While second-order effects contribute to this, especially DIBL, it is affected to a larger degree by the (ideally) large input signal pushing the transistor closer to subthreshold operation. The transition to subthreshold is not abrupt, but rather a gradual change, and this means that any signal with enough magnitude to get near the threshold will create significant distortions. This is similar to the signal magnitude limitations the Gilbert Cell has, and limits the performance of a triode-mode multiplier in the same way.

In a 20nm SOI process simulation, a triode-mode multiplier was constructed. Using just an ideal op-amp, the imperfections of the triode-mode devices limited SFDR to 53dB. In a real implementation, that would be reduced further by nonlinearity in the op-amp itself. Like with the Gilbert Cell, 50mV signal amplitudes were used, which again limits the dynamic range of the input signals. As will be seen in Chapter 3, the time-domain multiplier avoids this issue and allows near

rail-to-rail inputs and outputs.

2.4 Other Methods

Other methods have been explored in recent years, usually optimized for a certain performance metric. Since the primary benefit of analog design is a low power consumption, many designs focus on reducing it by shrinking the supply voltage or the supply current. Some rely on modifications of existing designs, like removing the current mirror from a Gilbert Cell or by adapting a flipped voltage follower [23, 24]. Others use new techniques, like square rooting circuits or cascading multiplication and subtraction stages [25, 26]. Of the designs cited, none claim a dynamic range larger than 40dB. Designs that optimize for speed have used techniques like dynamic body biasing, reaching speeds of nearly 10GHz with very small input and output magnitudes of less than 50mV [27]. Linearity-focused approaches have also used flipped voltage followers, or other kinds of feedback loops in order to linearize their designs [28]. However, large input magnitudes severely degrade the linearity, going from 64dB at 10% supply to 39dB at 75% in one specific case by Huang [29]. Finally, current-mode approaches have been investigated, which use current inputs and outputs to achieve good balances of speed, power consumption, and linearity [30, 31]. The major downside of such systems, however, is that nearly all other circuits rely on voltages, not currents, and so the benefits of the circuits may be lost when adapting them to fit in voltage-dominated signal processors.

Among the alternative designs, few are capable of handling signals larger than 15% of their supply voltage. While not explicitly stated, generally the reason why the input range is limited is to set the minimum linearity of the circuit, as generally linearity improves with smaller signal magnitudes. Many of the highest linearity multipliers published come with the most stringent input magnitude restrictions. In modern processes, however, the ever decreasing supply voltage requires

that signals possess as large of magnitude as possible, to avoid degrading SNR. This is where the circuit described later in this thesis excels. The time-domain analog multiplier is able to handle much larger signals, with high linearity, in exchange for a slower bandwidth. Other designs that have been published often must choose one, and with high power consumption as well (Huang's work in [29] used $\pm 2.5V$ supplies). The time domain will be shown to be a promising option for high-linearity, high-range applications in modern semiconductor nodes.

Table 2.1: Comparison of Multiplier Structures

Structure	Benefits	Drawbacks
Log-Antilog	- Simple design - Large dynamic range - Inputs share common-mode	- Single-ended, single-quadrant only - High power usage
Translinear	- Few devices - Wide dynamic range - Same common-mode inputs	- Hard to implement 4-quadrant - Needs BJTs for large signals
Gilbert Cell	- Few devices - 4-quadrant capable	- High VDD and overdrive needed for linearity - Inputs must differ in common-mode
Triode-Mode	- Only 4 nonlinear devices	- Input range limited by triode constraint - Device impedance highly nonlinear in modern nodes
Time-Domain	- Handles large inputs - Scales well with VDD - Same common-mode inputs - Power-bandwidth trade-off w/ maintained linearity	- Clocked: limited by Nyquist frequency - Linearity tied to Gm accuracy

Chapter 3

Theory and Implementation of the Time-Domain Analog Multiplier

The novel concept at the root of this thesis is the use of time for signal processing, rather than the usual voltages and currents. This is not a new idea, but has been primarily used in designing low-power, low-resolution analog-to-digital converters, not for general signal processing [32–36]. However, recent work in fields like machine learning have shown that for many large-scale computation applications, lower-resolutions are all that is needed. That is the space where time-domain designs offer great benefits in power-consumption and linearity.

The idea of using voltage-to-time converters to multiply numbers is similarly, not new. Work by Hong used uses a similar idea as what will be described in Section 3.1, but with digital inputs rather than analog [37]. Their work also only builds a single-quadrant multiplier, rather than a four-quadrant multiplier. This chapter will present a fully-analog, four-quadrant multiplier, which allows it to function as a general purpose analog signal processor, rather than a tool to be used in digital computation.

3.1 Fundamental Concept and Derivation

In the physics classes for any electrical engineering undergraduate, it is learned that

$$I(t) = C\frac{dV}{dt}$$

This is the core principle of how capacitors work, their own Ohm's Law. By solving the expression for $V(t)$, one can see that:

$$V(t) = \int_{t_0}^{t} \frac{I(\tau)}{C} d\tau \tag{3.1}$$

Equation 3.1 shows that a time-varying current into a capacitor results in an output voltage that is the integration of that current over the time interval. Intuitively, this expression simply represents that the output voltage is proportional to the total accumulated charge on the plates of the capacitor. If $I(t)$ is constant over the interval, then:

$$V(t) = \frac{I(t - t_0)}{C} = \frac{I\Delta t}{C} \tag{3.2}$$

Thus, the output voltage is proportional to the product of the input current I and the time that current is applied Δt. Without further definition, this basic concept could be used as a two-quadrant multiplier, where I can be either positive or negative, but Δt can only be positive (as it is not possible to have "negative" time, which would require $t < t_0$). However, clever ways of creating differential circuits can allow the time parameter to also hold a negative value, creating a true four-quadrant multiplier. This will be discussed further in Section 3.1.1.

It does not take advanced circuit knowledge to understand how this multiplication is linear. The ability to create constant currents with low error has existed for decades. The capabilities of CMOS

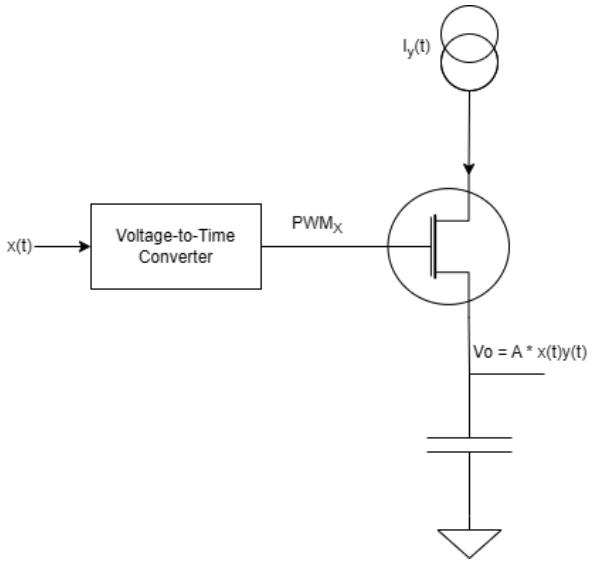


Figure 3.1: Basic Concept of Single-Quadrant Multiplier

circuits to generate tightly controlled time intervals has been developed as well, with some modern circuits exhibiting clock jitter measured in femtoseconds. The difficulties arise in making these two parameters fixed over the time interval, but also changeable proportionally to an input voltage or current between intervals. Otherwise, the multiplier would only multiply fixed constants, and there is no point in such a thing. Nonlinearity springs from the compromises that must be made to allow for varying inputs to the multiplier, and will be studied later.

3.1.1 Creating Negative Time Intervals

As the name suggests, the time component of the design is the crucial element. To create a four-quadrant multiplier with time as an input, both positive and ”negative” time are needed. When designing circuits with only a positive supply voltage, ”negative” values are generated by comparing voltages to a reference, usually the common-mode voltage of the signals. This can be done with single-ended or differentially. The same idea can be used to create negative time. Consider the pulse-width modulated (PWM) signals in Figure 3.2. With a zero input, the width of the pulse

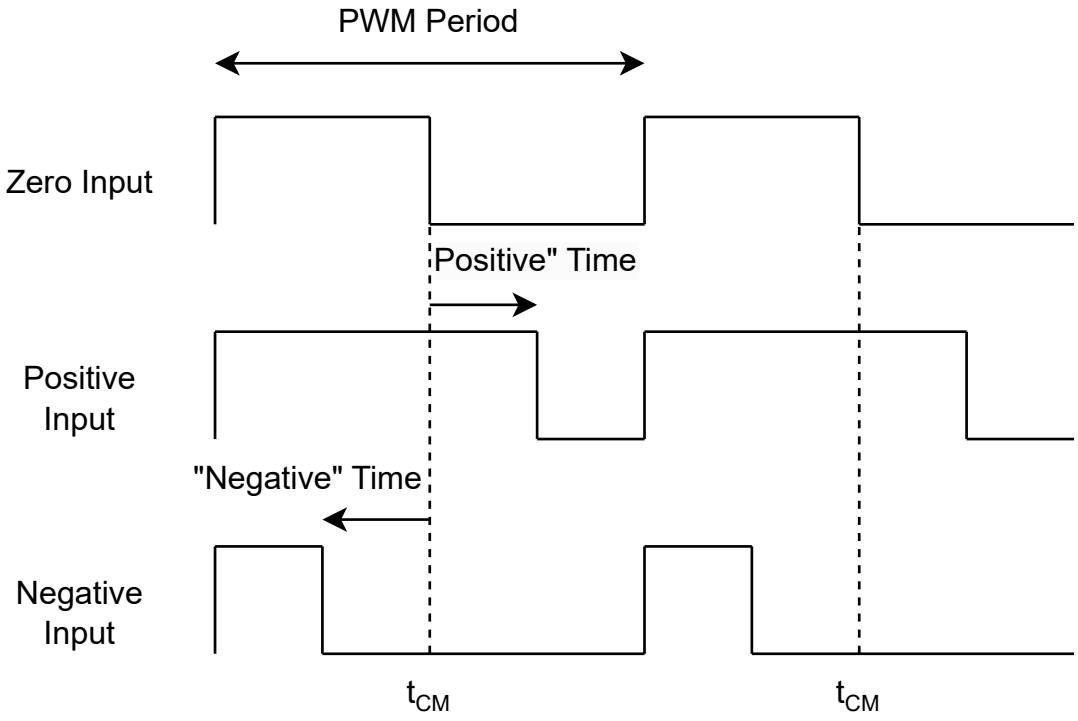


Figure 3.2: Defining Positive and Negative Time as Pulse Width Deltas

stretches to the common-mode time, t_{CM}. Adding a positive or negative input linearly changes that width by positive or negative time, respectively. This resembles the type of PWM or duty cycle control that is often used in power electronics, but with a key difference. In those systems, the pulses exist to modulate other circuits or systems as part of a control loop. In time-domain circuits, the pulse widths themselves carry information, and are are vulnerable to all the non-idealities that switching converters are not, like edge jitter.

Fortunately, the way voltage and current signals are already discussed in the field of electrical engineering can be extended to time signals as well. The magnitude of a time-signal is simply the degree to which the pulse width changes by. Notably, this is constrained by the total period of the

Table 3.1: Time-Domain Signal Magnitude and Nyquist Frequency Examples

PWM Period (ns)	**Maximum Signal Magnitude** (ns)	**Signal Nyquist Frequency** (MHz)
3	1.5	166.67
30	15	16.67
100	50	5

PWM signal. For example, if the period is 100ns, then pulse width cannot vary by more than 50ns from the common-mode level. This sets a hard limit on signal range in a unique way; voltage and current signals have limits set by the physical limitations of the devices. However, just like voltage and current signals, differential signaling effectively doubles the input range.

The frequency of a time-domain signal is similarly constrained. Frequency is directly to the period of a signal, and since the period of a time-domain signal can't be smaller than the period of the pulse train, there is a maximum frequency that can be encoded. Also, the time signal is also a discrete signal, as the pulse width deltas are delivered at the rate of the underlying pulse train. That means that, by the Nyquist Theorem, the highest frequency signal that can be reconstructed from the signal will have a period twice that of the pulse train period, in order to avoid aliasing. Thus:

$$f_{nyquist} = \frac{1}{2T_{PWM}} \tag{3.3}$$

Unlike with voltage and current signals, these limitations on magnitude and frequency are linked together. Increasing the PWM period would increase the maximum signal magnitude, but at the same time decrease the maximum signal frequency, and vice versa. Table 3.1 shows some examples of the relation.

Noise in time-domain signals manifests as jitter, directly changing the signal's magnitude. Jitter is a well-understood phenomenon, and can be studied in a similar way to how it is done in PLL,

oscillator, and clock distribution design. Time-domain signals actually have an advantage over voltage signals as voltage supplies continue to scale, which is that the SNR of the signal can stay constant no matter the supply voltage, as the time intervals and the relative jitters can stay the same. Distortion of a time-domain signal. on the other hand, is difficult. Part of it relates well to voltage signal processing, where the time signal has a systemic nonlinear effect on it that creates non-idealities just like occurs with voltages and currents in modern transistors. However, because the pulse is created by rising and falling edges, the properties of those also plays a role. If the shape of those edges changes with input magnitude, then that also may result in a distortion on the signal, as it would affect how the circuits turn on and off again, as well as charge injection, clock feedthrough, and other non-ideal effects. This is different than the noise case. Circuit noise would change the magnitude of the time signals by modifying the pulse widths, where distortion would effect the signal even if the time signals are noise-free.

3.1.2 Creating a Full Four-Quadrant Multiplier

Since negative time and negative currents can be created, can a four-quadrant multiplier be created from just Figure 3.1? No, it cannot. The reason is that, while the signal components would multiply properly, there would also be feed-through of the DC common-mode components and the original input signals. This can be shown, if X,Y are the common-mode inputs and x,y are the signal inputs, as:

$$(X + x)(Y + y) = XY + Xy + xY + xy \neq xy \tag{3.4}$$

While the DC term could be tolerated, the feedthrough input terms cannot be. They must be removed from the output. As discussed in Section 2.3, this can be done by using four separate multipliers to produce a pure four-quadrant multiplier output. The four separate multipliers are then

added and subtracted from one another to cancel out the terms. This approach requires differential inputs, however.

$$\begin{aligned} & [(X+x)(Y+y)+(X-x)(Y-y)] \\ - \quad & [(X+x)(Y-y)+(X-x)(Y+y)] \qquad (3.5) \\ = \quad & (2XY+2xy)-(2XY-2xy) \\ = \quad & 4xy \qquad (3.6) \end{aligned}$$

The subtraction operation is easy to achieve by simply using a differential amplifier, feeding one sum into each side. The addition is more complicated. The chosen method in this case is using charge sharing between capacitors to sum the voltages. Each capacitor is charged, like shown in the single-quadrant case, and then after both switches have turned off, the capacitors are linked together. The charge must be conserved, and so the final charge is simply the sum of the individual charges. If the original charges on two capacitors are $Q_1 = C_1V_1$ and $Q_2 = C_2V_2$, then if $C_1 = C_2$:

$$\begin{aligned} Q_{tot} &= Q_1 + Q_2 \qquad (3.7) \\ C_{tot}V_{tot} &= CV_1 + CV_2 \qquad (3.8) \\ (2C)V_{tot} &= C(V_1+V_2) \qquad (3.9) \\ V_{tot} &= \frac{V_1+V_2}{2} \qquad (3.10) \end{aligned}$$

This method unfortunately includes a factor of $\frac{1}{2}$, but the power savings resulting from no extra amplifiers or control circuits makes that loss worth the 6dB decrease in signal magnitude. The only

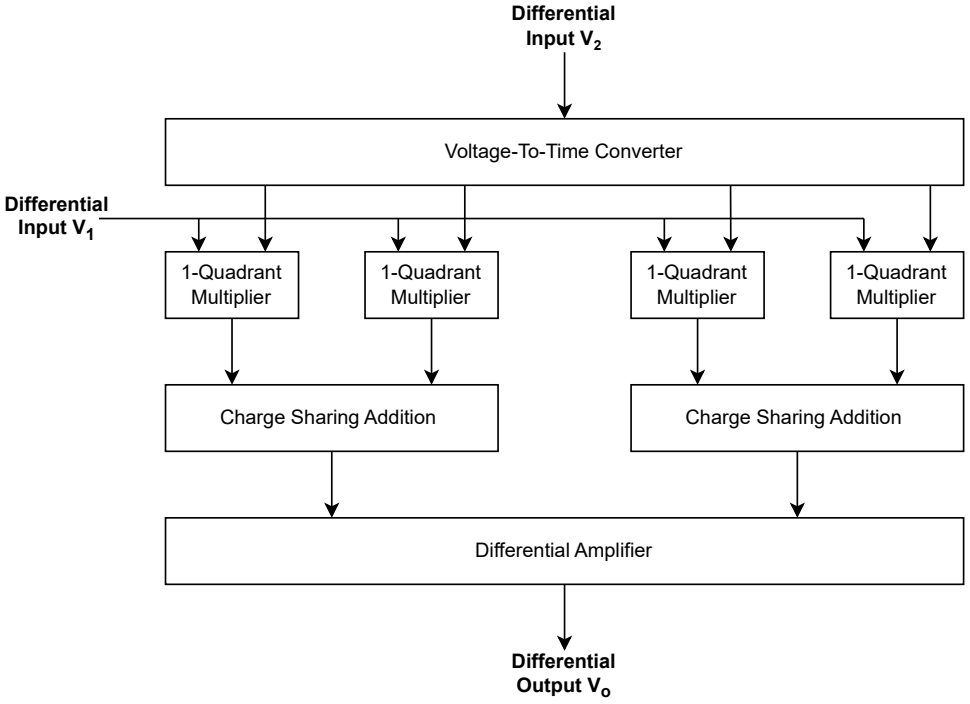


Figure 3.3: Signal Processing Flow of the Time-Domain Multiplier

additional power consumption from the addition operation is what is needed to charge the gate capacitance for the sharing switch itself, and that is negligible.

Together, the structure of the design is shown in Figure 3.3. Each ”block” will be discussed in detail in Section 3.2, as well as some details that are missing from the figure, such as the clocking of the different blocks. However, to derive the output function of the multiplier, nothing more is needed.

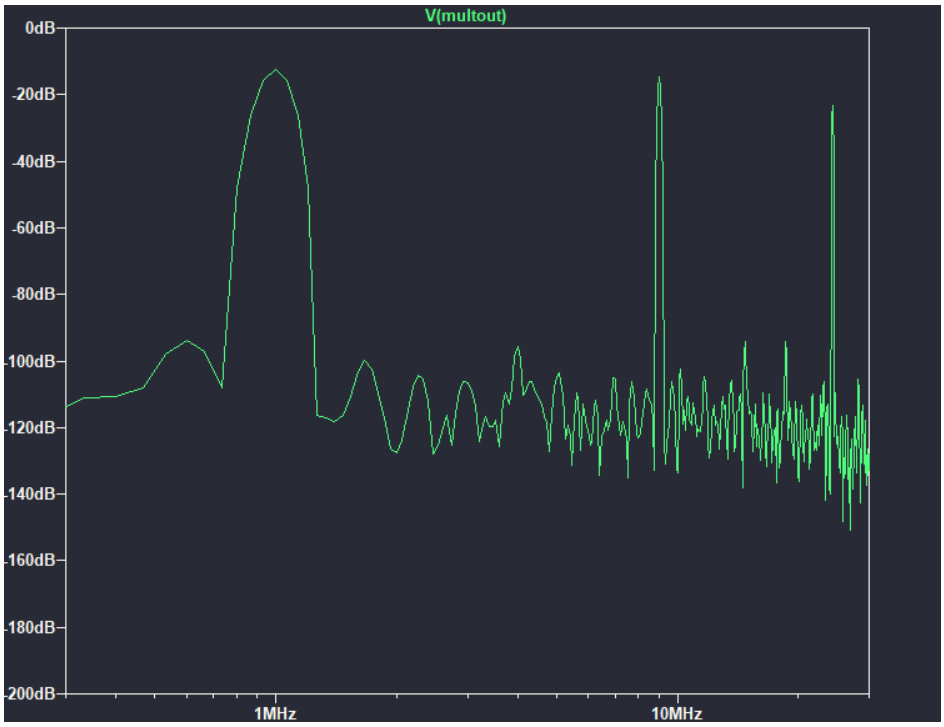


Figure 3.4: Ideal Simulation of Time-Domain Multiplier, with 4 MHz and 5 MHz Inputs. SFDR = 83 dB

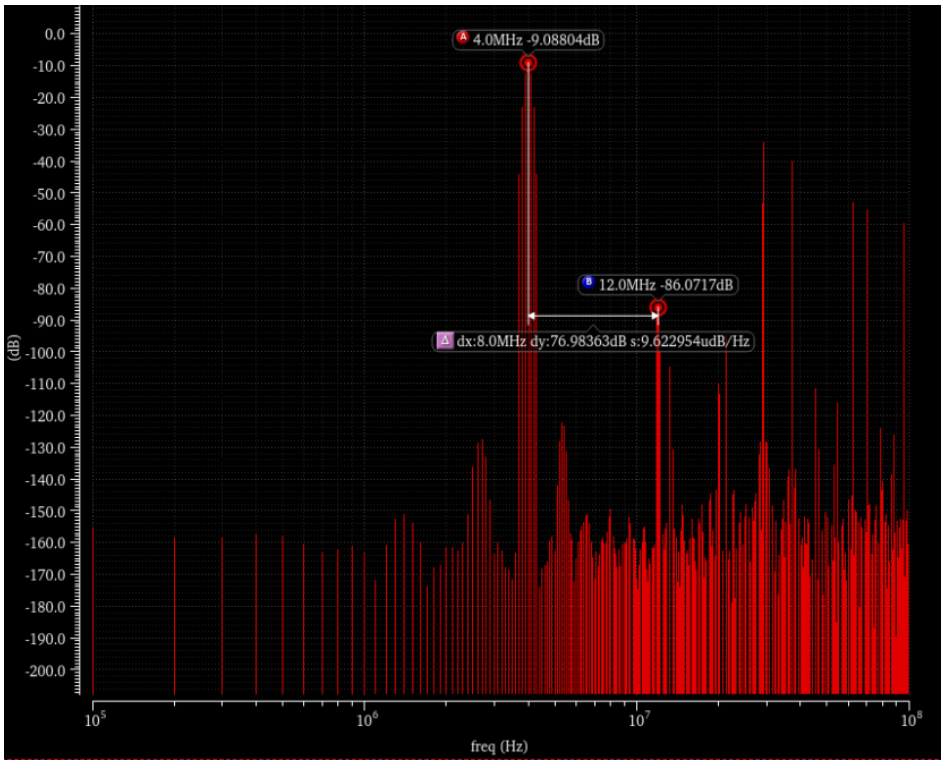


Figure 3.5: Simulation of Model with a Single Input, Real Switching Devices

Full Derivation of the Output

The full output function of the design will be derived, in its ideal form. The resulting output will have the form of a four-quadrant multiplier. First, two voltage inputs are defined as

$$(V_X + V_x), (V_Y + V_y)$$

where the capitalized terms represent the DC common mode levels of the signals and the uncapitalized terms represent the differential input magnitudes. Of the two blocks that the inputs feed into directly, the transconductor is the easier to model. Linear transconductors are characterized by their G_m value, where:

$$G_m = \frac{I_{od}}{V_{id}} \tag{3.11}$$

The transconductor also has a common mode output current I_{ocm}, around which the output currents vary. Thus, the transconductors output current, split into the two single-ended output currents that feed into each individual one-quadrant multiplier is:

$$I_o^+ = I_{ocm} + G_m V_{id}^+ = I_{ocm} + G_m V_x^+ \tag{3.12}$$

$$I_o^- = I_{ocm} + G_m V_{id}^- = I_{ocm} + G_m V_x^- \tag{3.13}$$

Note that the input common mode voltage does not matter, as the ideal transconductor's output is proportional only to the differential input. In reality, the output current does change across input common mode voltages, though the effect is much less than the differential input's effect. The output current is also affected by the output voltage, proportional to the output impedance of the transconductor. This error current is:

$$I_e = \frac{V_{DD} - V_{out}}{R_{out}} \tag{3.14}$$

The effect of this finite output impedance cannot be accurately calculated, as the output impedance changes as V_{out} changes in a nonlinear fashion. That nonlinear error current is then integrated by the capacitor to change the output voltage. This effect is best left to SPICE simulation to model, but it should be known that the output impedance of the circuit is critical.

The other block is the Voltage-To-Time Converter (VTC). VTCs have conversion gains just like transonductors do, but with units of $\frac{s}{V}$. The value of this conversion gain will be represented by A_t, and as its value is highly dependent on the topology of the converter, will be derived in Section 3.2.4 when the structure used is introduced. The time also has a common-mode value, like the current, and so the output of the VTC is:

$$T_o^+ = T_{ocm} + A_t V_{id}^+ = T_{ocm} + A_t V_y^+ \tag{3.15}$$

$$T_o^- = T_{ocm} + A_t V_{id}^- = T_{ocm} + A_t V_y^- \tag{3.16}$$

Now, the two inputs for the single-ended multiplier are defined. Given the multiplier's transfer function:

$$V_o = \frac{I_o T_o}{C} \tag{3.17}$$

Then the output of a single ended multiplier, given any combination of the single-ended outputs of the transconductor and VTC, is:

$$V_o = \frac{(I_{ocm} + G_m V_x)(T_{ocm} + A_t V_y)}{C} \tag{3.18}$$

$$= \frac{1}{C}(I_{ocm}T_{ocm} + I_{ocm}A_t V_y + T_{ocm}G_m V_x + A_t G_m V_x V_y) \tag{3.19}$$

The issues with the single-ended multiplier are clear in Equation 3.19. There is a direct feedthrough of each input to the output voltage, superposed with a constant output and the multiplication output. Combining the four one-quadrant multipliers into a single one-quadrant multiplier will resolve these issues.

First, each individual output is summed. V_p sums the two unipolar terms:

$$V_p = \frac{1}{2C}(I_{ocm}T_{ocm} + I_{ocm}A_t V_y^+ + T_{ocm}G_m V_x^+ + A_t G_m V_x^+ V_y^+ + I_{ocm}T_{ocm} + I_{ocm}A_t V_y^- + T_{ocm}G_m V_x^- + A_t G_m V_x^- V_y^-) \tag{3.20}$$

while V_n sums the two mixed terms:

$$V_n = \frac{1}{2C}(I_{ocm}T_{ocm} + I_{ocm}A_t V_y^- + T_{ocm}G_m V_x^+ + A_t G_m V_x^+ V_y^- + I_{ocm}T_{ocm} + I_{ocm}A_t V_y^+ + T_{ocm}G_m V_x^- + A_t G_m V_x^- V_y^+) \tag{3.21}$$

Then, the difference is taken using a differential amplifier:

$$
\begin{aligned}
V_p - V_n &= \frac{1}{2C}(I_{ocm}T_{ocm} + I_{ocm}A_tV_y^+ + T_{ocm}G_mV_x^+ + A_tG_mV_x^+V_y^+ \\
&\quad + I_{ocm}T_{ocm} + I_{ocm}A_tV_y^- + T_{ocm}G_mV_x^- + A_tG_mV_x^-V_y^- \\
&\quad - I_{ocm}T_{ocm} - I_{ocm}A_tV_y^- - T_{ocm}G_mV_x^+ - A_tG_mV_x^+V_y^- \\
&\quad - I_{ocm}T_{ocm} - I_{ocm}A_tV_y^+ - T_{ocm}G_mV_x^- - A_tG_mV_x^-V_y^+) \qquad (3.22)
\end{aligned}
$$

Canceling terms and grouping:

$$
\begin{aligned}
V_p - V_n &= \frac{1}{2C}(A_tG_mV_x^+V_y^+ + A_tG_mV_x^-V_y^- \\
&\quad - A_tG_mV_x^+V_y^- - A_tG_mV_x^-V_y^+) \qquad (3.23) \\
&= \frac{A_tG_m}{2C}(V_x^+(V_y^+ - V_y^-) + V_x^-(V_y^- - V_y^+)) \qquad (3.24) \\
&= \frac{A_tG_m}{2C}((V_x^+ - V_x^-)(V_y^+ - V_y^-)) \qquad (3.25) \\
&= \frac{A_tG_m}{2C}(V_xV_y) \qquad (3.26)
\end{aligned}
$$

Thus, the output of the amplifier will exhibit only the multiplication property, and all other feedthrough and constant terms cancel out. The leading term in Equation 3.26 is referred to as the multiplication gain, and it is the amount by which the pure input voltage multiplication is scaled. The value can be easily adjusted by changing C, the chargeable capacitance. An output stage could be used to further increase the magnitude of the output signal.

3.2 Implementation

3.2.1 Clocking

Unlike many other analog multiplication circuits, the time-domain multiplier is a clocked system. This is necessary for the time-domain portion to function, as the generation of the VTC edges cannot happen continuously. A generic timing scheme is shown in Figure 3.6 without numerical values. First, the reset phase resets the capacitor voltages and holds them low while the transconductor output current settles. This prevents the unpredictable settling behavior from being integrated onto the output capacitors. Then, the PWM phase occurs, though it does not have its own signal. Rather, the PWM phase is defined as the period from which the RST signal releases the capacitors to charge and when the MEAS phase starts. During that time, the VTC processes its input and cuts off the charging of the capacitor with its time-domain signal. The MEAS phase is when the now-charged capacitors are combined to create the proper output, completing the multiplication. The final phase, CAPT, is not technically a phase as it does not control part of the multiplier. Rather, it shows the time to sample the output voltage of the multiplier, after it has properly settled.

Because of the output comparator used in the VTC (as discussed further in Section 3.2.4), the VTC generates glitch edges after it has already cut off current to the chargeable capacitor. To rectify this, the VTC output (being a digital signal effectively) is processed with digital logic. The input to the VTC, carrying the time-domain signal, is subject to:

$$PWM = \overline{(\overline{VTC} + MEAS)} \tag{3.27}$$

This holds the PWM signal low while the measurement phase is underway, including while the output value is being captured.

It is also important to note that there is a finite output range for the VTC in Figure 3.6. There

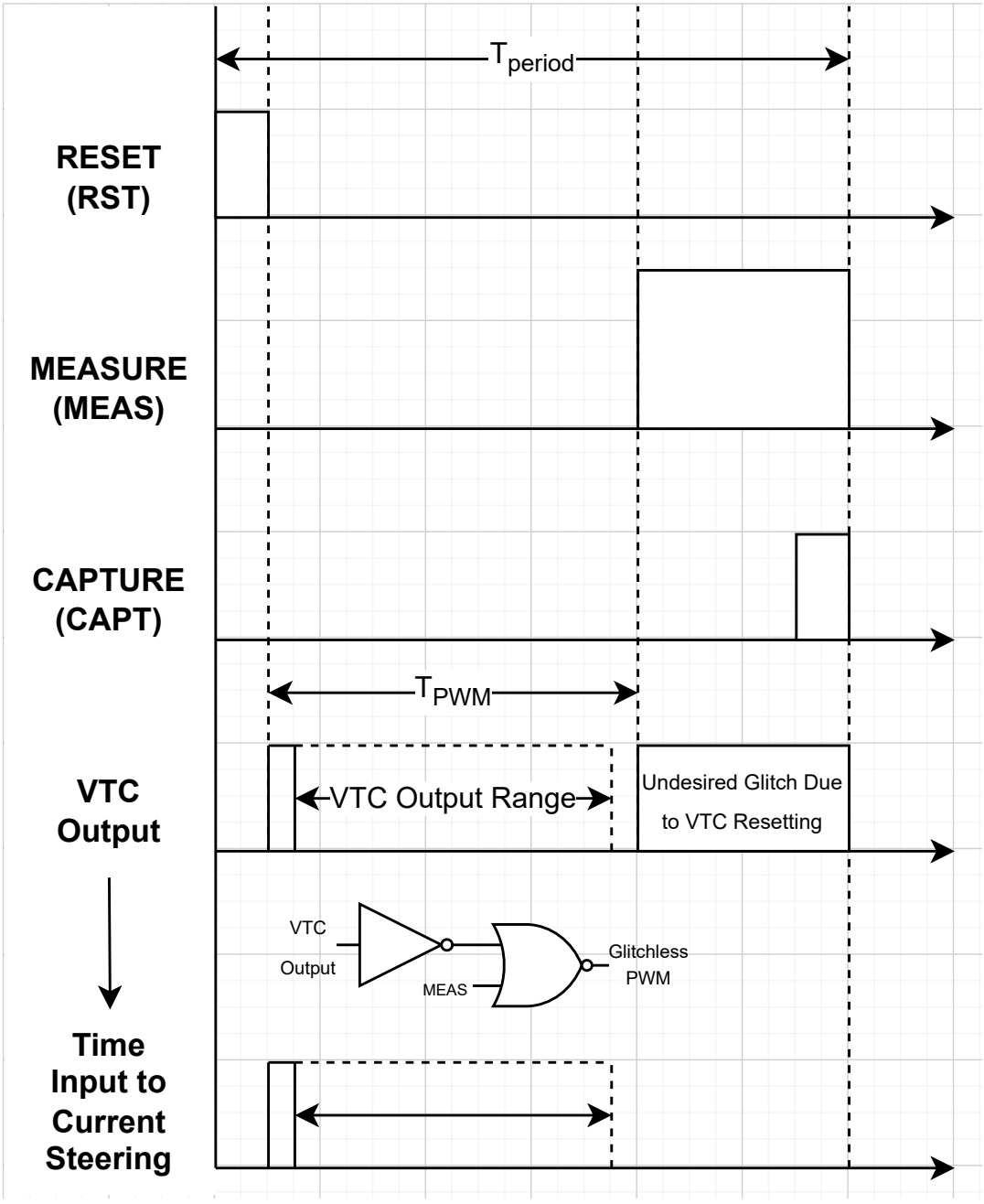


Figure 3.6: Timing Diagram of the Time-Domain Multiplier

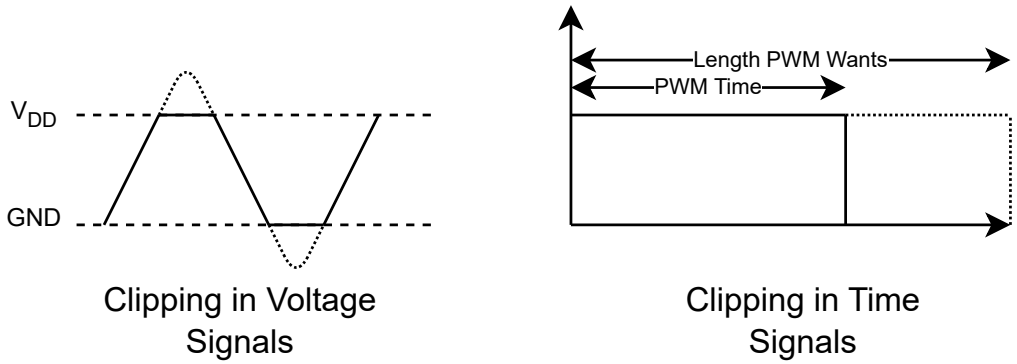


Figure 3.7: Clipping of Voltage vs. Time Signals due to Range Limitations

is a limit for the time for the low end, as the time output can't be less than 0s, and for the high end, as the time output cannot exceed the allotted PWM time, cuts off when MEAS goes high. This is a phenomenon also seen with voltage signals, where the limits are set by the supply voltages of the circuit. The similarities can be seen in Figure 3.7. Since the overall circuit is differential, the real range for the time-signal is double the allotted PWM time, just like with differential voltage signals. Best practices from voltage signals apply to time signals as well, such as leaving some headroom to make sure that the output does not clip and introduce distortion. This can be observed in Figure 3.6, where the range of the signal does not reach 0s or the full allotted PWM time.

3.2.2 Current Steering

While the basic model of the circuit shows the use of switches to control the flow of current in an on-off fashion, practical concerns require current steering instead. The most important concern is that, if the current is simply blocked, the output voltage of the transconductor rises to the rail voltage. This creates two issues once the current is allowed to flow again. First, the stored charge in the output of the transconductor, both in the parasitic capacitances and in the channel, flow out to the

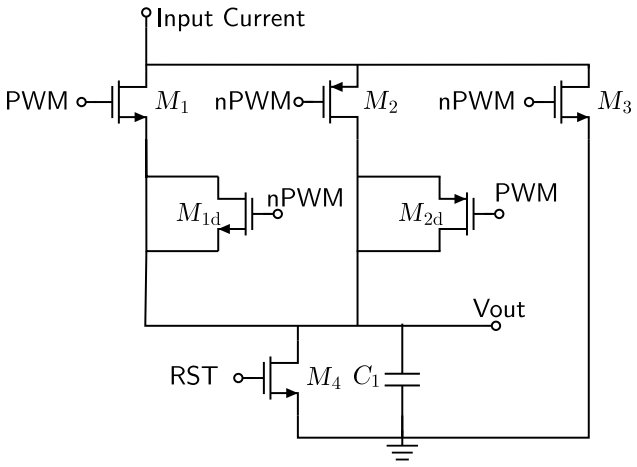


Figure 3.8: Current-Steering Block

now-connected capacitor in an attempt to equalize the voltages. This produces an uncontrollable glitch in the output voltage. Second, the output current of the transconductor requires time to recover as the output voltage descends from VDD. This settling behavior is uniquely harmful in this system, as the output current is still integrated onto the capacitor even during transient spikes.

Current steering offers a way out of the problem. By using M3 to hold sink the output current, the transconductor does not have to react at all when the capacitor is allowed to charge. The output current stays constant, and the output voltage stays at 0V on either side of the switch transition. The difference between the two methods is illustrated in Figure 3.9, where V_{out} refers to the output voltage of the transconductor, not the capacitor.

Because the input is a fixed current and not a voltage, the switch resistance does not affect the output voltage like it would with a voltage input. This is because the fixed current enters the capacitor no matter the switch resistance, while a voltage input would exhibit an RC time constant with the switch resistance as R. A transmission gate structure is used with M1 and M2 to ensure that the resistance stays low across voltage. Devices M1d and M2d are dummy devices, used to help mitigate charge injection into the output capacitor from the switches. They are sized to half that of

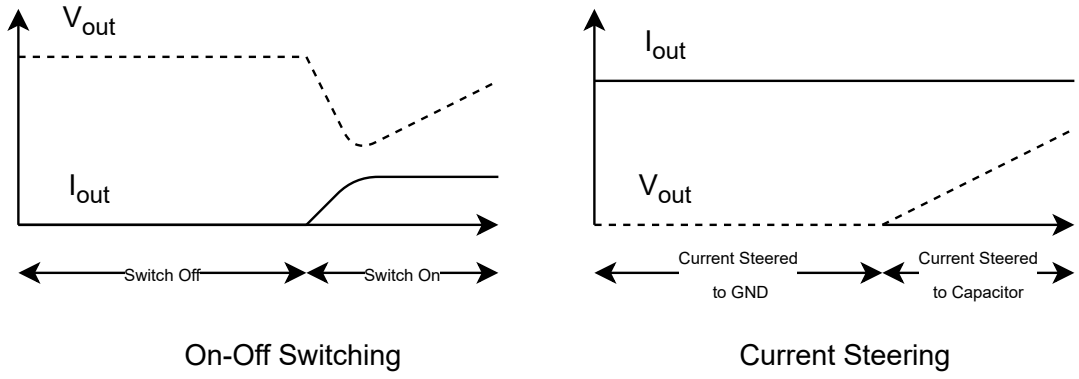


Figure 3.9: On-Off Switching vs Current Steering

the actual switches, as the charge injection is estimated to split evenly between the drain and source of the switches. This estimation is a poor one, as the real split is dependent on how fast the gate voltage switches, the capacitance at the drain and source, and various time constants [38]. As these parameters are often poorly controlled in analog circuits, it is better to assume an even split and accept the imprecision. No charge-injection compensating dummy transistors are needed for M3 or M4. For M3, charge injection does not matter, as most of the charge will exit via GND since the GND capacitance is much greater than the input capacitance of the circuit. What charge does enter the circuit may be compensated for by M1d and M2d. For M4, the reset switch, charge injection will occur but crucially only when the voltages of all output capacitors are held at 0V. This means that identical amounts of charge should be injected from each device, and the errors will cancel at the output of the multiplier. The dummy can be included if device variation is a concern, as this affects the cancellation.

The capacitor C_1 is a metal-oxide-metal (MOM) capacitor sized to 200 fF. It is sized to produce the appropriate gain in Equation 3.26. The size of the capacitor also determines noise characteristics of the circuit ($\frac{kT}{C}$ noise) and the time constant of the resetting operation, where $\tau_{rst} = R_{M_4}C$. The

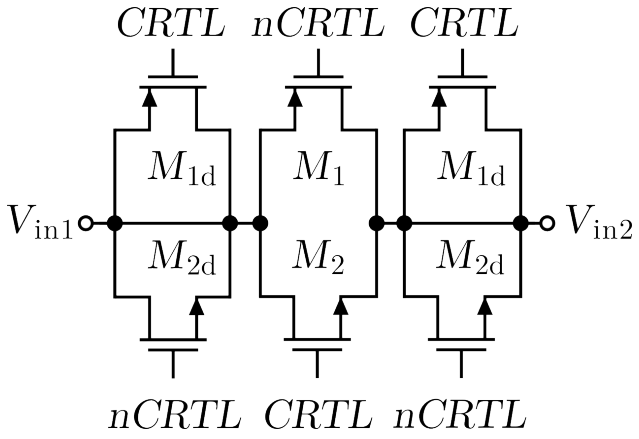


Figure 3.10: Charge Sharing Switch

sizing of the switches were tuned to balance speed against error due to charge injection. As stated above, the impedance of transistors M1-M3 does not produce error, as the use of a constant current means the capacitor charges as the same rate always. As long as the V_{ds} across the switches is small enough, the current source stays operating as desired. The reset transistor is much larger than any other, as it is the only one for which the on impedance matters and must be minimized to reduce the resetting time constant.

3.2.3 Charge Sharing Addition

To create the addition operation, the same-valued capacitors charged in the current steering blocks are put in parallel. This results in a final voltage:

$$V_{final} = \frac{V_{in1} + V_{in2}}{2} \tag{3.28}$$

This result is reliant on the capacitors being the same value. Fortunately, capacitors match very well even in modern processes. However, with mismatch, the final voltage becomes a weighted average of the two initial voltages relative to the total capacitance. If $\Delta C = \frac{C_2 - C_1}{2}$:

$$V_{final} = \frac{C_1V_1 + C_2V_2}{C_1 + C_2} = \frac{V_1 + V_2}{2} + \frac{\Delta C}{2C}(V_2 - V_1) \tag{3.29}$$

Once the transconductors are separated from the capacitors by the current steering block, the rest of the circuit is passive. This means that effects like charge injection and clock feedthrough must be treated even more carefully. For this reason, two sets of dummy transistors are used on both sides of the switch to mitigate charge injection, and the corresponding NMOS/PMOS pairs have matched widths and lengths, canceling out clock feedthrough.

The output will take time to settle after the switch is closed. The time constant is lower than it would be for a capacitor being charged from a voltage source, as both capacitor voltages will be moving towards the final value rather than just one. Circuit-wise, this can be seen by recognizing that connecting two capacitors with a switch and a common ground puts the capacitors in series with one another. This results in a time constant:

$$\tau = R_{sw}C_{tot} = R_{sw}\frac{C_1C_2}{C_1 + C_2} = \frac{R_{sw}C}{2} \tag{3.30}$$

During this settling time, the output will not be accurate. A failed experiment while developing the topology showed that failing to respect the settling behavior can have massive impact on the output. Specifically, using the outputs of the addition operations as inputs for an output transconductor, which would charge output capacitors to hold the final value, was considered. The motivation was that average power consumption may be lowered, as the output load capacitance could be charged gradually. However, a current feeding into a capacitor results in an integration, and when the idea was tested the settling behavior of the addition was integrated onto the output of the multiplier. This resulted in a feedthrough of transconductor input frequency, the magnitude of which was determined by how quickly the charge sharing settled. Moving to sampling the voltage

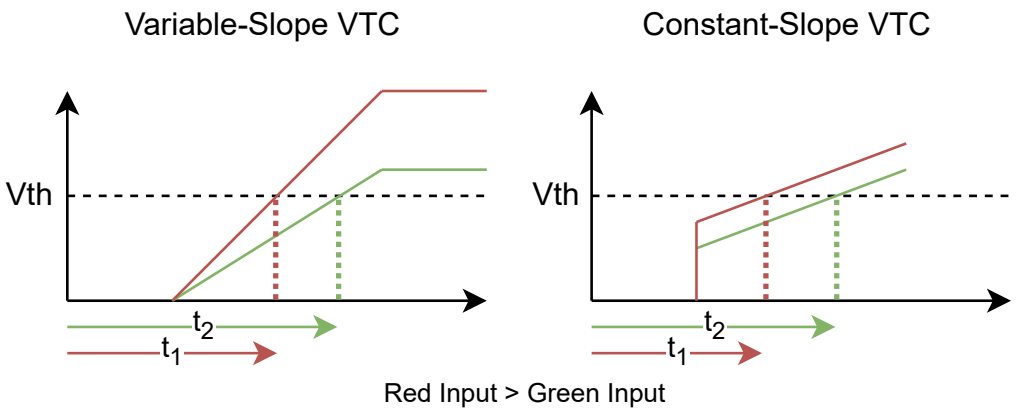


Figure 3.11: Two Types of VTC [6]

after a certain number of time constants resolved this issue.

3.2.4 Voltage-to-Time Converter

The design of the voltage-to-time converter (VTC) in this work is very similar to the design introduced by Chen et al. in 2022 [6]. The essential idea of the circuit is the same, but has been modified for slower operation, as the original design ran at 4GS/s, while this work is intended for 33MS/s. Chen's work also does not go into depth about the design of the output comparator, which was the most complicated part of the design.

As discussed in Section 3.1, the VTC linearly converts an input voltage into a pulse-width modulated signal, where the pulse width is proportional to the input voltage. This creates a time signal, where the data is encoded as lengths of time rather than magnitudes of voltage or current. This can be easily done with a comparator, waiting for a linearly increasing input to cross a reference threshold. However, the input to the VTC must be able to change when that threshold is crossed, and Figure 3.11 shows two methods for doing this that were discussed by Chen. The first type, the

variable-slope VTC, functions by changing the slope of the signal that crosses the threshold. This is easy to implement with any integrator circuit. The time signal is defined by the time from 0 to the crossing point. In Figure 3.11, the red input has a larger magnitude, so it has a larger slope and the time signal has a smaller value.

The difficulty with the variable-slope VTC is that the slope needs to be linear, and that is difficult to achieve in across a wide input range without high power consumption. An easier and more linear solution is to charge with a constant current, which means designing a constant-slope VTC. Using cascoding or gain-boosting, current sources can be made extremely linear. However, this removes the mechanism for the input to affect the point of crossing. To reintroduce the input, Chen and this work use capacitive charge redistribution to set the initial condition of the integrator to a value proportional to the input voltage. This can be seen in Figure 3.11, where the red input resulted in a higher initial condition, moving the crossing point sooner in time. The downside of this approach is that the charge redistribution is not instant, but rather takes time to settle. This limits the bandwidth of the VTC, as linearity decreases the less time the redistribution has to settle. In exchange, no transconductor is needed to change the current flowing into the integrating capacitor, greatly reducing power consumption.

The full design for the VTC is shown in Figure 3.12. The design used in this work is single-ended, requiring two identical copies of the structure in order to create a differential VTC. As discussed in Section 3.2.3, dummy transistors (labeled by the ”d” suffix) are used to mitigate the effects of charge injection on the signal. The structure of M7,M8, and M9 is also familiar; it is the current steering structure discussed in Section 3.2.2. For this reason, these two aspects of the design will not be discussed further, as all the previous statements about them still apply.

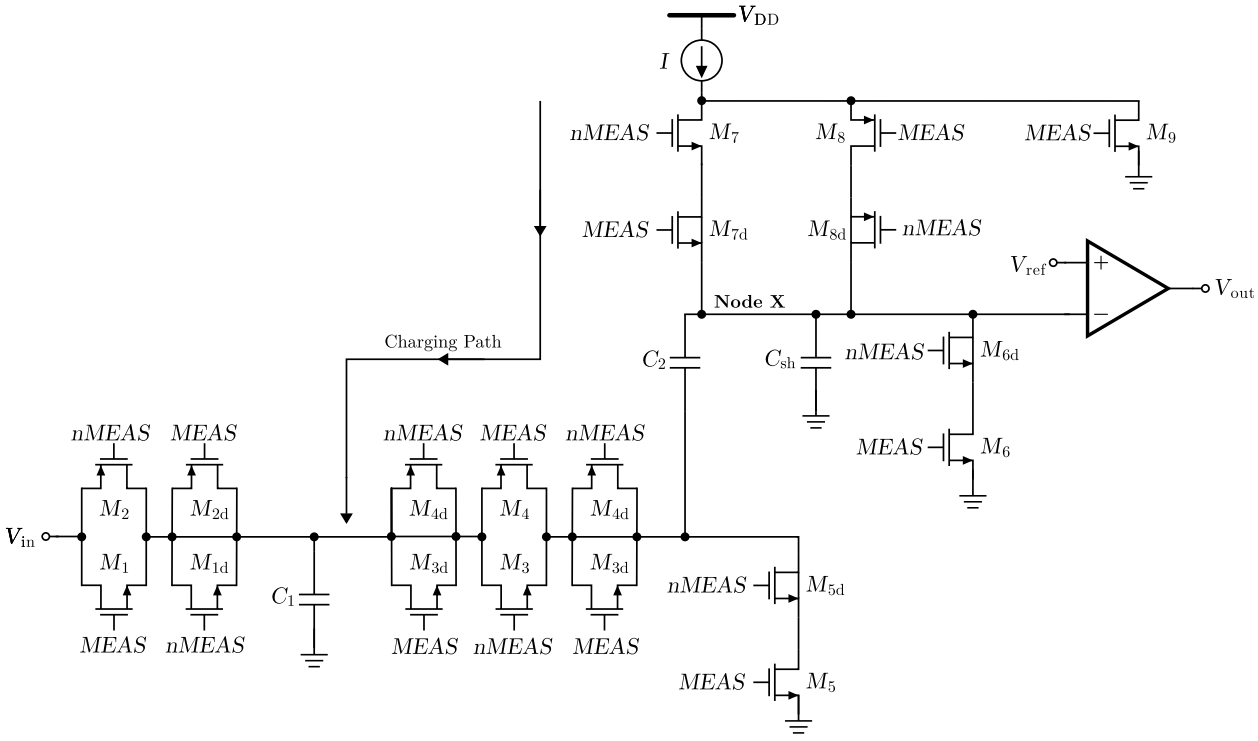


Figure 3.12: Voltage-to-Time Converter

Input-Dependent Charge Redistribution

The novel aspect of the constant-slope architecture is the use of charge redistribution to allow the input to affect the length of the output pulse. In Figure 3.12, capacitors C1, C2, and Csh (which represents the net parasitic capacitance at node X as well as any intentional capacitance added) are combined to create a voltage at node X proportional to the input voltage. This voltage, after sufficient time has been allowed for settling, is derived as follows:

$$\begin{aligned} Q_i &= C_1 V_i = Q_f = Q_{1f} + Q_{C_{2,sh}} && (3.31)\\ &\quad \text{where } C_{2.sh} = \frac{C_2 C_{sh}}{C_2 + C_{sh}} \\ C_1 V_i &= C_1 V_{C_{2,sh}} + C_{2.sh} V_{C_{2,sh}} && (3.32)\\ V_{C_{2,sh}} &= \frac{C_1 V_i}{C_1 + C_{2,sh}} && (3.33)\\ V_X &= \frac{C_2}{C_2 + C_{sh}} \frac{C_1 V_i}{C_1 + C_{2,sh}} && (3.34)\\ &= \frac{C_1 C_2}{C_1 C_2 + C_1 C_{sh} + C_2 C_{sh}} V_i && (3.35) \end{aligned}$$

This term is easily adjusted to pick a specific ratio, and because of how well capacitors match in most processes, is well controlled. The combination settles through the switch formed by M_3, M_4 when it conducts during the nMEAS ($= \overline{MEAS}$) clock period. The time constant is:

$$\begin{aligned} \tau &= R_{M_3,M_4} C_{eq} = \frac{R_{M_3,M_4}}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_{sh}}} && (3.36)\\ &= \frac{R_{M_3,M_4} C_1 C_2 C_{sh}}{C_1 C_2 + C_1 C_{sh} + C_2 C_{sh}} && (3.37) \end{aligned}$$

This settling follows the usual exponential behavior, and the number of required time constants can be calculated to reach a certain level of precision.

Comparator Design

Though the novel part of the VTC design is the charge redistribution mechanism, it is also the easiest to design. The most difficult component is the output comparator, for several reasons. Firstly, a clocked comparator cannot be used, despite their advantages. The reason for this is because clocking the comparator would discretize the value of the time signal, as the end of the pulse could only happen at specific increments. The clock speed would need to be multiple orders of magnitude larger than the operating frequency for the system for an equivalent resolution of 8-10 bits, which is far too power hungry to be practical. Instead, open-loop comparators must be used. Secondly, the comparator needs to have a very high slew rate in order to create sharp transitions and define clear time spans, but also a low propagation delay in order to prevent wasted time. High slew-rates require large transistors, which slows down the overall design. The way to reach performance targets is to increase power consumption, which is not ideal for an analog multiplier.

Thirdly, and most importantly, the propagation delay must be constant , no matter the input magnitude to the circuit. Generally, comparators exhibit a variety of propagation delays, dependent on both the input common-mode and differential input magnitudes. In Figure 3.13, the delay increases rapidly outside the VTC input range of 150-650mV. This is incredibly important, because if the delay changes depending on the input, it results in distortion in the time-signal. Suddenly, the time output for a 400mV input and a 700mV input is not linearly related by the gain A_t. This nonideality in the comparator is the main source of distortion and nonlinearity in the VTC, and has a name: delay dispersion. This has been studied in relation to slope-crossing ADCs, and techniques have been proposed for flattening the propagation delay [7, 39, 40]. These offer an opportunity for

Figure 3.13: Delay Dispersion in the Designed Comparator vs. Input to VTC

improvement, as none of these methods have been implemented in this work.

For the design discussed in Chapter 4, the comparator is a 2-stage operational amplifier with a folded cascode PMOS input stage. This was chosen to allow low common-mode input levels, which is important since the lowest common-mode input level is just $\frac{V_{th}}{2} = 125mV$. A telescopic cascode would have allowed for higher speed operation, but at the cost of common-mode range. A Class AB output stage was used, in order to allow for high slew rates in both directions.

Deriving Conversion Gain of VTC

The conversion gain A_t needs to be derived, so that it can be applied to the derivation given in Section 3.1.2, specifically Equation 3.26. The formula is given by Chen, but is not derived in his

work [6]. The gain A_t is defined as:

$$A_t = \frac{t_{out} - t_{cm}}{V_i - V_{i,cm}} \tag{3.38}$$

Assuming that the charge redistribution time constant is small compared to the VTC operating time, the conversion gain occurs in two steps. First, the voltage at node X in Figure 3.12 increases immediately by an amount proportional to the input. Second, the voltage at node X increases linearly until it crosses the threshold voltage. The amount that the node X raises by is given by Equation 3.35, though for this derivation the gain preceding V_i will be replaced by α. The time it takes for the constant-slope voltage to cross the threshold is simply:

$$\frac{dV}{dt} = \frac{I}{C} \rightarrow t_{out} = \frac{C_{eq}}{I}(V_{th} - V_{Xi}) \tag{3.39}$$

Thus, the two times given in Equation 3.38 are:

$$t_{cm} = \frac{C_{eq}}{I}(V_{th} - \alpha V_{i,cm}) \tag{3.40}$$

$$t_{out} = \frac{C_{eq}}{I}(V_{th} - \alpha V_i) \tag{3.41}$$

Solving to find the gain:

$$t_{out} - t_{cm} = \frac{\alpha C_{eq}}{I}(V_{i.cm} - V_i) \tag{3.42}$$

$$A_t = \frac{\alpha C_{eq}}{I} \tag{3.43}$$

Interestingly, the equivalent capacitance for the integration behavior is not the same as it is for

charge redistribution.

$$C_{eq} = C_{sh} + \frac{C_1 C_2}{C_1 + C_2} = \frac{C_1 C_{sh} + C_2 C_{sh} + C_1 C_2}{C_1 + C_2} \tag{3.44}$$

Substituting and canceling:

$$A_t = \frac{1}{I} \frac{C_1 C_2}{C_1 C_2 + C_1 C_{sh} + C_2 C_{sh}} \frac{C_1 C_2 + C_1 C_{sh} + C_2 C_{sh}}{C_1 + C_2} \tag{3.45}$$

$$A_t = \frac{C_1 C_2}{I(C_1 + C_2)} \tag{3.46}$$

Equation 3.46 gives the single-ended conversion gain. For a differential VTC, using two copies of the single-ended version (as is done in this work), the conversion gain is double:

$$A_{t,diff} = \frac{2C_1 C_2}{I(C_1 + C_2)} \tag{3.47}$$

Besides being useful for calculating the gain of the overall multiplier, this equation for the gain also reveals several interesting details about the VTC's properties. Firstly, though C_{sh} is used prominently to derive all the supporting equations, it has no impact on the overall gain at all. The only condition is that C_{sh} must be chosen so that the threshold is always crossed during the constant-slope portion of the VTC's operation. Secondly, the specific threshold voltage used has no impact on the gain, as long as the threshold is crossed during the constant-slope portion of operation. This also means that any offset voltage in the output comparator does not affect the conversion gain, as the offset voltage would represent as a shift in the reference threshold.

This also reveals the biggest advantage of the time-domain multiplier. A_t can be increased ,by changing C_1, C_2, to any value, without increasing I and thus increasing power consumption. In

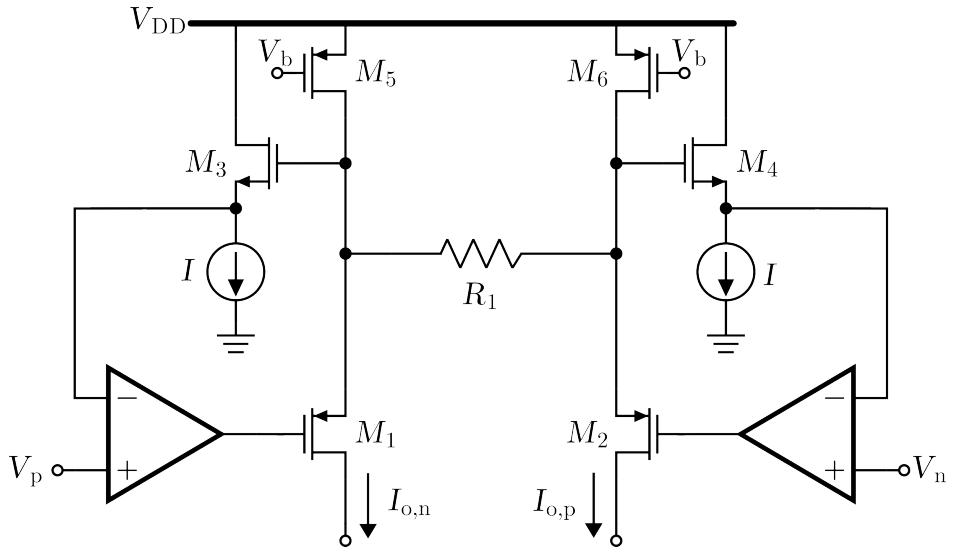


Figure 3.14: Linear Transconductor Used in Multiplier

exchange, the PWM time for the VTC must increase, but this is tolerable for many slower applications. For example, multipliers used in low-speed watchdog correlators may only need to operate below 1MHz. More importantly, increasing A_t allows for G_m of the transconductor to be decreased proportionally. Since the G_m of the transconductor relates directly to its power consumption, overall power consumption can be reduced in this way.

3.2.5 Linear Transconductor

The transconductor is the other block that accepts an input signal, but this time it converts the input voltage into a current signal rather than a time signal. Figure 3.14 shows the circuit used in this work, though other structures were examined. In an ideal world, this circuit would be a perfect transconductor. The voltages on each side of the resistor would be exactly that of the inputs, and so the output current that passes through the resistor would be simply:

$$I_o = I_{o,p} - I_{o,n} = \frac{V_p - V_n}{R_1} \tag{3.48}$$

This output current sits on top of the common-mode output current, which is set by the current sources M_5, M_6. In this design, $3\,\mu$A was used, but that value was chosen based on the period of operation for the circuit overall. First, the VTC's output range is set directly by the time that is allowed for it to operate, with an upper bound set by the operating period. Knowing that period, the maximum and minimum values of the output current can be determined. The maximum current is easiest, as it is set by the maximum voltage the circuit can tolerate across the integrating capacitor. Usually, this is set by the maximum output voltage of the transconductor itself. For example, if the maximum output voltage is $0.4\,$V, then the maximum output current will create that voltage if the VTC output is at the maximum, integrating the largest current for the longest period of time. If that maximum time is $20\,$ns and the capacitor size is $200\,$fF:

$$I_{o,max} = C\frac{V_{max}}{t_{max}} = (200fF)\frac{0.4V}{20ns} = 4\mu A \tag{3.49}$$

The minimum current, on the other hand, is less strict. The only limit is that the current must not be $0\,$A, for two reasons. Firstly, no transconductor will be linear at or approaching $0\,$A, and since linearity is a primary concern this must be avoided. Secondly, clipping may be introduced if the current can reach $0\,$A, since even a perfectly balanced design may be disrupted by mismatch and the $0\,$A point would be reached before the limit on input magnitude. As long as this is avoided, then the minimum current is set by considering both the minimum capacitor voltage to be attained for SNR purposes and how linear the transconductor needs to be, as a larger output swing will be less linear. A great benefit of this design is that the output swing of the transconductor does not need to be large, as a small change in output current will integrate into a large change in the voltage. In this design, the minimum output current was chosen to be $2\,\mu$A by balancing these concerns. The common-mode output current is then chosen halfway between the minimum and maximum, so $I_{cm} = 3\mu A$.

The structure in Figure 3.14 was chosen for its simplicity and linearity. Many other transconductor structures exist, including ones without discrete amplifiers like [41, 42], and these offer opportunities to improve the power consumption of the design. However, for this work time was a constraint, and as such a simpler design was chosen. Those who have seen the transconductor structure in Figure 3.14 may notice the addition of the source followers created by M_3 and M_4. This is not standard, and in fact degrades the linearity of the transconductor. However, it is necessary in order to allow the input common-mode of the transconductor to be the same as the input common-mode of the VTC. Without this follower, the unity feedback would attempt to directly create the input voltages on each side of the resistor, at the same common-mode voltage as the inputs. This means that with an input common-mode of $400\,\text{mV}$, and assuming a minimum $V_{DS} = 100mV$, the maximum output voltage of the transconductor would be just $300\,\text{mV}$ without any differential input whatsoever. With input, that maximum voltage falls as the input magnitude rises, and kills performance. However, with the addition of the source followers, the resistor nodes exist one V_{GS} above the inputs, increasing the maximum output voltage by V_{GS}. This does require a sufficiently high VDD level in order to allow this, so for this design the VDD is $1.2\,\text{V}$ rather than $0.8\,\text{V}$.

3.2.6 Output Amplifier

Although not discussed in this work, an output amplifier could be used to increase the output magnitude. Unlike many other multiplier designs, the output magnitude is already greater than 100 mV for larger-scale inputs, so only a small voltage gain in the range of $2 - 10\frac{V}{V}$ is required, depending on the supply voltage used. This stage can also be used to convert the differential output of the prior stages to a single-ended output. As long as the noise performance and linearity of the output stage are high, there will be negligible impact on system performance metrics such as SFDR or SNR.

Chapter 4

Time-Domain Multiplier Specifications and Measurements

4.1 Specifications for Design

In Chapter 3, references are made to the design implemented in this work. This project initially began as part of a high-speed analog correlator, targeting a multiplier bandwidth of 300 MHz. Multiple multipliers would have been used in parallel to achieve the targeted throughput targets for the system. However, it quickly became apparent that the benefits of the time domain multiplier are not speed, and so the specifications were reduced. The goal specifications are shown in Table 4.1.

The goal specifications were based on the original project. The linearity target of 72dB was roughly equivalent to 12 bits of precision, by ENOB. The clock period, 30 ns,was tied to the Nyquist frequency needed to represent a 15MHz signal without aliasing. The Nyquist frequency was30 MHz in this case, but the circuit operates at 33 MHz.

The following sections detail the measured simulation results, pre-layout, at several stages of

Table 4.1: Goal Specifications for Multiplier

Specifications	Value	Unit
Max. Power Consumption	12	µW
Min. Differential Input Range	± 400	mV
Bandwidth	15	MHz
Clock Period	30	ns
Minimum Linearity (SFDR)	72	dB

development. This was done in order to show what parts of the design degrade the specifications from the ideal values the most. These simulations were conducted using a real $20\,\text{nm}$ FDSOI process, with a $0.8\,\text{V}$ voltage supply unless stated otherwise. Simulations were ran using Cadence's Spectre SPICE engine, under the conservative preset.

4.2 Results With Ideal Transconductor and VTC

First, the circuit was simulated with ideal transconductors and VTC. The ideal VTC composed of a sawtooth generator and the input sine wave, which creates an output PWM signal that varies with the level of the sine wave. The ideal transconductor composed of ideal current inputs, copied through cascode current mirrors. The power consumption by these ideal circuits is not accurate by any measure, but they do set a baseline for linearity. A 5x ideal output amplifier is used to scale the output to large levels for easier display, but the linearity is unaffected and the stage consumes no power.

For the single input case, the differential inputs were a $4\,\text{MHz}$ sine wave with differential $400\,\text{mV}$ amplitude into the VTC and a constant $2\,\mu\text{A}$ differential output current from the ideal transconductor. The results are shown in Figures 4.1,4.2. It can be seen that the SFDR is nearly $77\,\text{dB}$. This sets an initial baseline of distortion to compare subsequent measurements to.

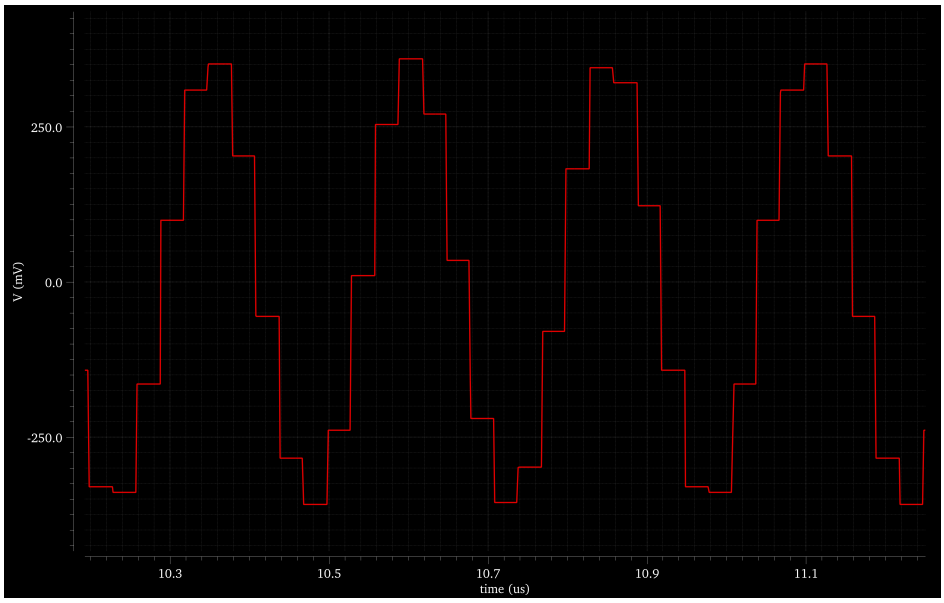


Figure 4.1: Time-Domain Output of Multiplier with Ideal VTC, Transconductor. Single Input

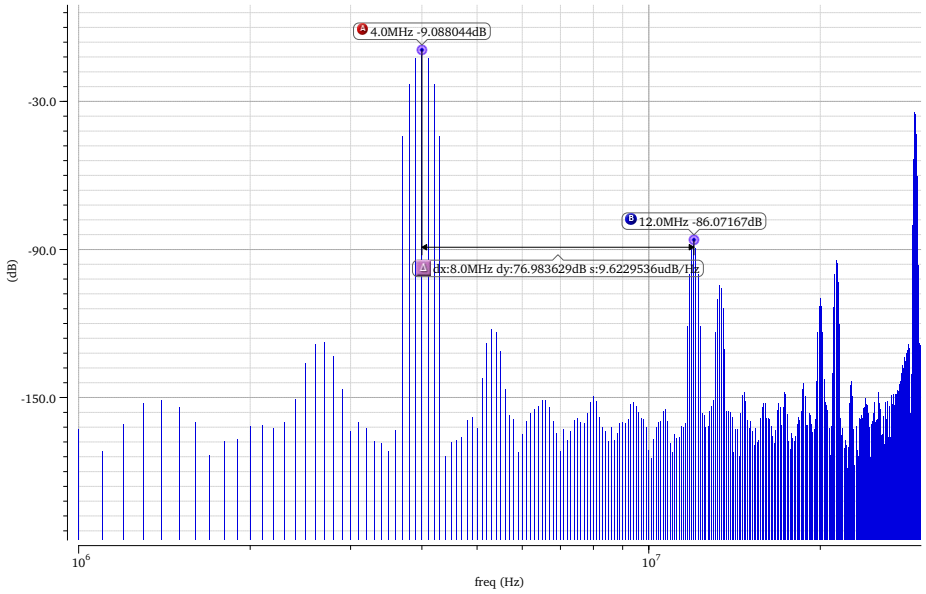


Figure 4.2: Spectrum of Multiplierwith Ideal VTC, Transconductor. Single Input

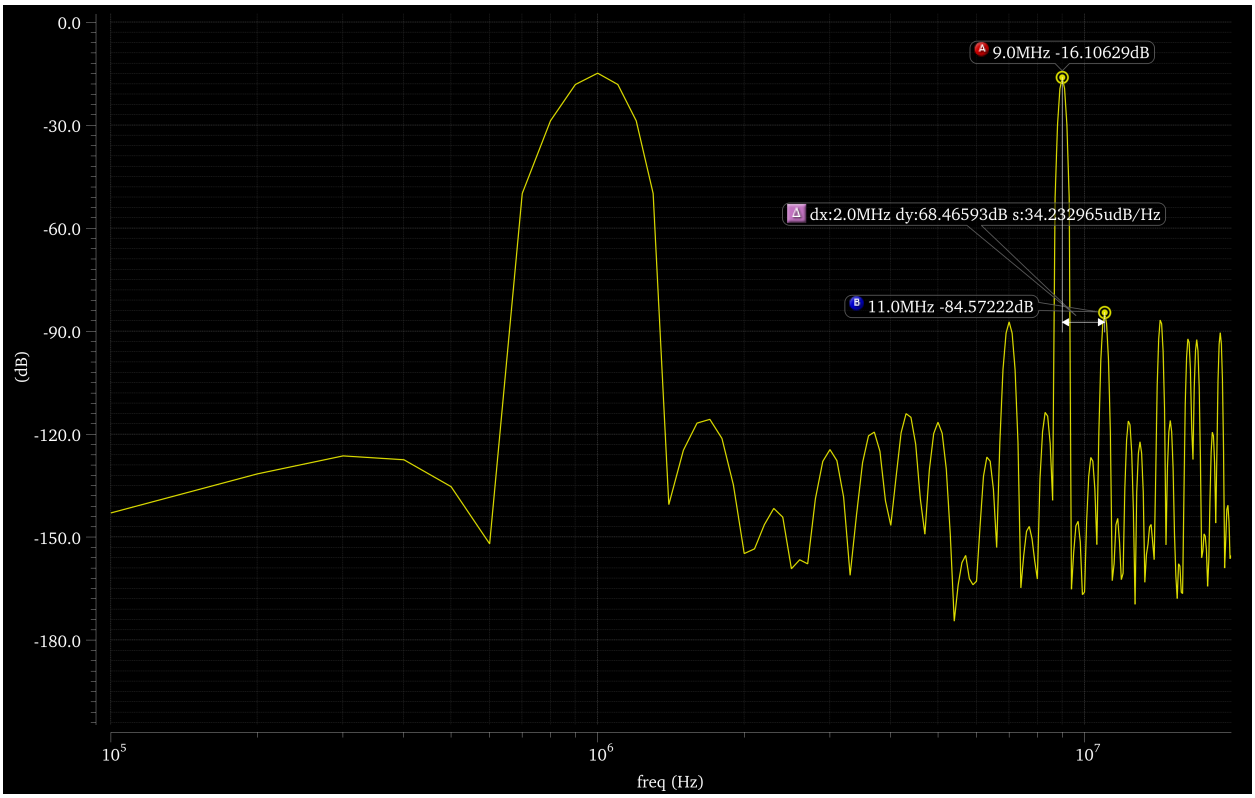


Figure 4.3: Spectrum of Multiplier with Ideal VTC, Transconductor. Two Inputs at 4 MHz and 5 MHz

For the two input case, the VTC input was the same as the single input case, but the transconductor input was now a 2 µA amplitude sine wave at 5 MHz. Due to the multiplication, the output tones of interest were at 1 MHz and 9 MHz. The resulting spectrum can be seen in Figure 4.3.

For both the single input and dual input case, the average power consumption was 30 µW. Of that, an average of 24 µW was consumed by the transconductor, either directly charging the capacitors or biasing the cascode current sources. The power consumption and linearity targets were already missed before adding the VTC and transconductor.

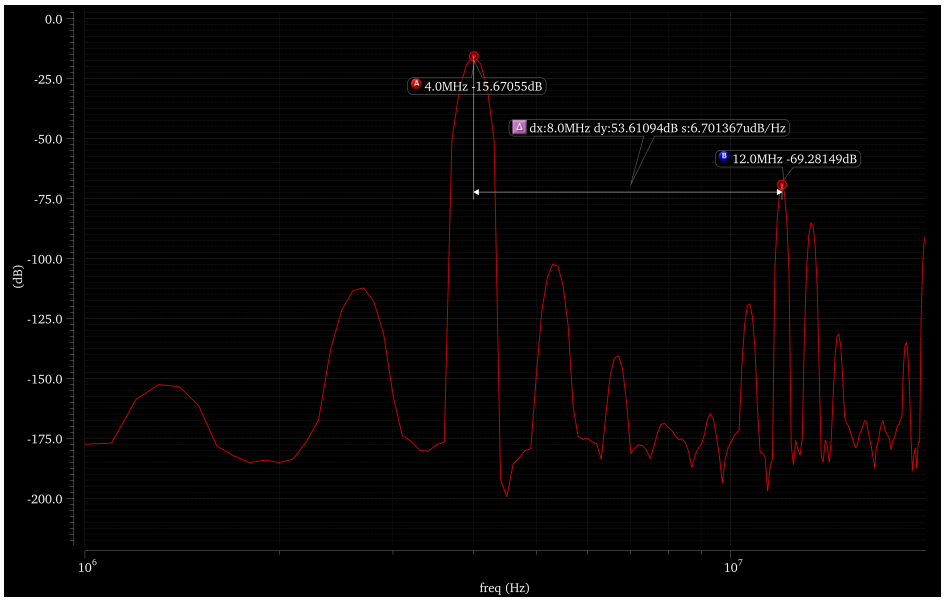


Figure 4.4: Spectrum of Multiplier with Real VTC. One Input at 4Mhz

4.3 Results with Ideal Transconductor, Real VTC

The test setup is identical to the setups given in Section 4.2, except that the VTC discussed in Chapter 3 is used instead of the ideal version. The input to the VTC is still a 400 mV differential signal.

In Figure 4.4, it can be seen immediately that the harmonics of the output have increased compared to the ideal case. Now, the SFDR=53.6 dB.

With two inputs, the SFDR is 50.8 dB (THD=0.46%) with a 400mV input. Reducing the input magnitude to 200mV increases the SFDR to 59.7 dB (THD=0.135%). This shows that the linearity of the VTC improves with a decreasing input magnitude, same as most circuits. In both cases, the average power consumption was 66 µW.

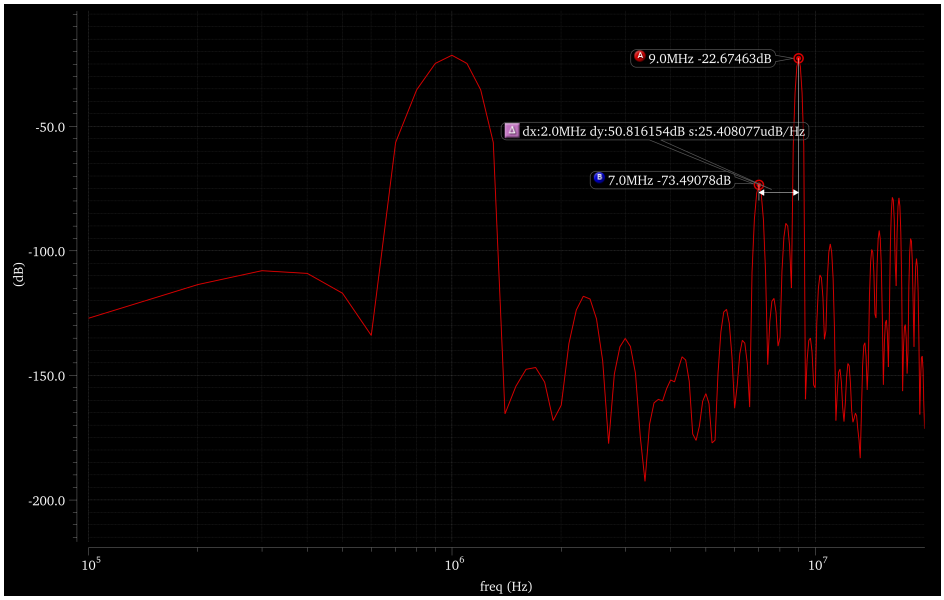


Figure 4.5: Spectrum of Multiplier with Real VTC. Two Inputs at 4 MHz and 5 MHz

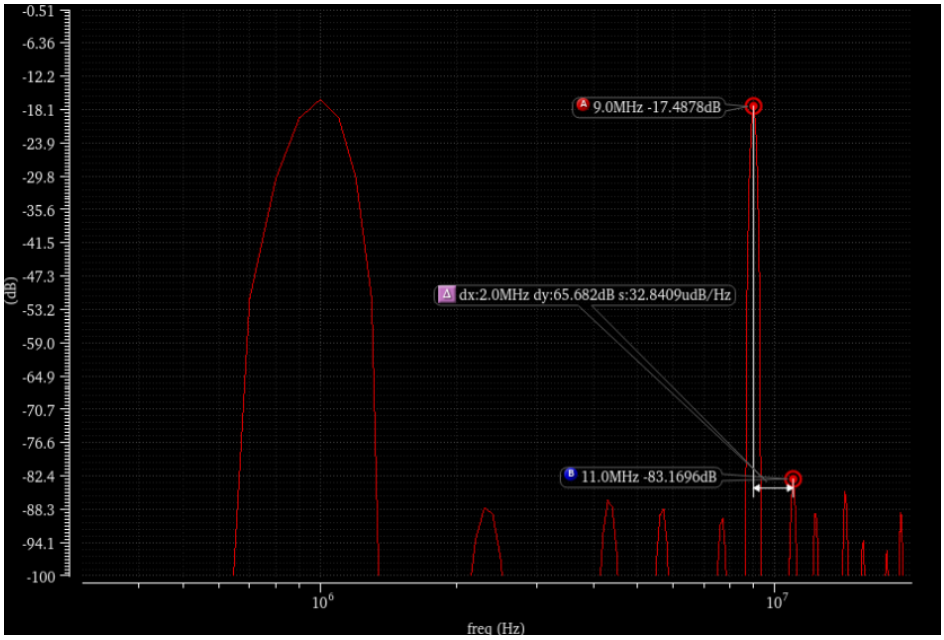


Figure 4.6: Spectrum of Multiplier with Real Transconductor. Two Inputs at 4 MHz and 5 MHz

4.4 Results of Real Transconductor, Ideal VTC

Figure 4.6 shows the results using an ideal VTC, but a real transconductor. The linearity worsened by about 8dB to an SFDR of 65.7 dB, which is significant. The THD is worse as well, due to the rise of the other harmonics in the output spectrum. The power consumption was only $28.8\,\mu$W, which shows that the VTC consumes a considerable amount of power. This power is mostly consumed in the comparator for its output.

4.5 Results of Full Implementation

With every part of the circuit implemented with the designs in Chapter 3, more measurements were taken. Tables 4.2 and 4.3 show the performance of the multiplier across input magnitude and compared to the prior stages of implementation. In each simulation, both inputs had the same magnitude, though only one input may have varied with time. This analysis reveals that the transconductor input is incredibly linear, with a THD of nearly $0.01\,\%$ with a 400 mV input. It is even more linear than the transconductor itself is at any given time, possibly due to the integration of that error and then cancellation.

On the other hand, the VTC performance needs improvement in order to reach design targets. One would expect the linearity to improve as the input magnitude shrank, but these simulations did not show that for the VTC. Furthermore, the linearity numbers don't monotonically decrease at input magnitude increases, which is definitely not a physical result. For small input magnitudes, the simulator does not accurately simulate the linearity of the VTC circuit, even with very tight simulator tolerances. The VTC also introduces spurs at evenly spaced intervals that are not harmonics of any frequency used in the design. Both issues suggest that accurately simulating the VTC needs further investigation.

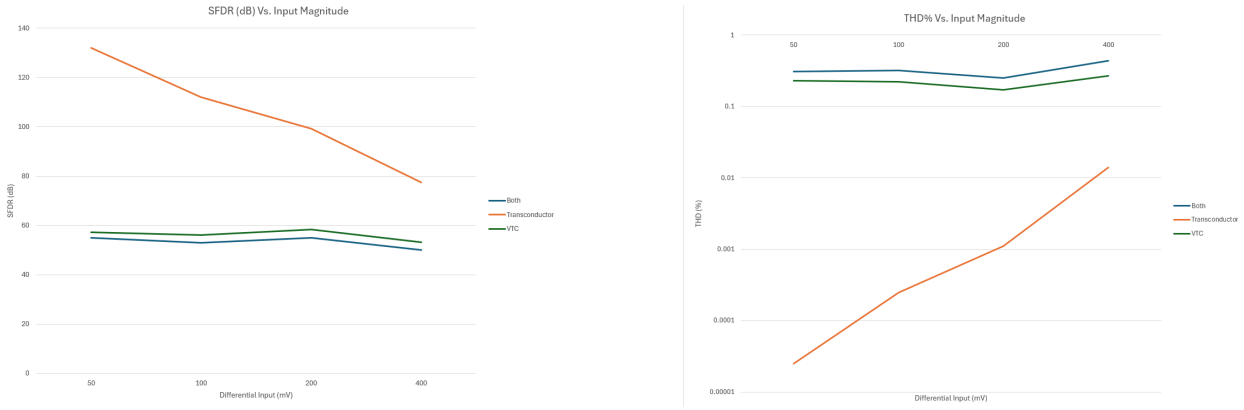


Figure 4.7: SFDR and THD Plotted Over Input Magnitude

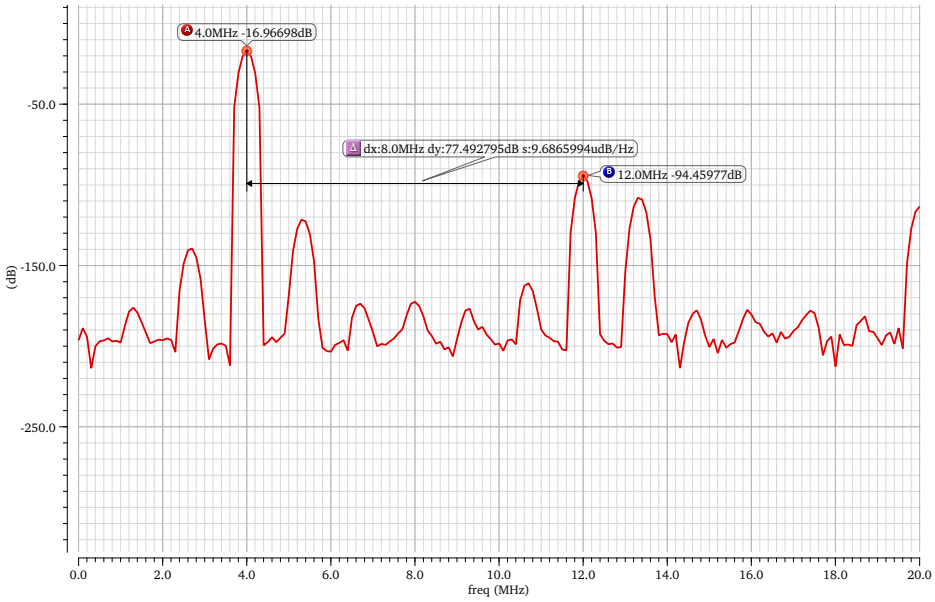


Figure 4.8: Spectrum of Fully Implemented Multiplier. Sinusoidal Transconductor Input at 400 mV, Constant 400 mV Input to VTC

Table 4.2: Linearity Measurements over Input Magnitude

	Two Sinusoidal Inputs		Sinusoidal VTC Input Other Input Constant		Sinusoidal Transconductor Input Other Input Constant	
$V_{i,diff}$ (mV)	SFDR (dB)	THD (%)	SFDR (dB)	THD (%)	SFDR (dB)	THD (%)
50	55	0.31	57.1	0.23	132	2.49e-5
100	52.9	0.32	56.1	0.22	112	2.46e-4
200	55	0.25	58.4	0.17	99.2	1.1e-3
400	50	0.44	53.2	0.27	77.5	1.4e-2

Table 4.3: Measured Results From Each Test Case of the Multiplier Circuit

Case ($V_{i,diff}$ =400 mV)	SFDR (dB)	Pdiss (uW)
Ideal Except Switches	77	30
Real VTC, Ideal Transconductor	50.8	66
Real Transconductor, Ideal VTC	65.7	28.8
Fully Implemented	50	65.5

Chapter 5

Results and Future Work

5.1 Analysis of Results

Table 4.3 shows the performance metrics obtained from the simulations of the circuit. Many other designs for analog multipliers have been published, but it is difficult to compare them as there are many different types of inputs, outputs, and definitions of linearity between them. For the purposes of this analysis, only voltage-mode multipliers will be examined, as there is no way to compare the input signal ranges of voltage- and current-mode circuits fairly. This comparison will also limit itself to comparing circuits with Total Harmonic Distortion (THD), rather than SFDR. Though SFDR makes more sense for characterizing multipliers in a two-tone test, as was done in Chapter 4, THD is the more traditional metric for analog circuits. For the same reason, the results will be compared between tests where only a single input frequency is used, and the second input is held constant.

Even with these limitations, a Figure of Merit (FoM) will be used to compare the different multipliers, as bandwidths, linearity, and power dissipation may fluctuate wildly between multipliers specialized for different tasks. This FoM is defined in this work as:

$$\text{FoM} = \frac{\text{Bandwidth (MHz)} * \text{Input Signal Range (mV)}}{\text{THD (\%)} * \text{Power Consumption } (\mu W)} \tag{5.1}$$

Unfortunately, the many papers on analog multipliers differ wildly on what they report. In published work on data converters, generally the same information is published about each design: power consumption, dynamic range, bandwidth, ENOB, etc. However, for multipliers, some papers do not even publish their power consumption values. Furthermore, the papers are often published with varying methods of defining linearity, including THD and SFDR but also by looking at a percent error from the ideal DC transfer function. This means that some papers have been excluded on this basis, rather than the basis of their performance.

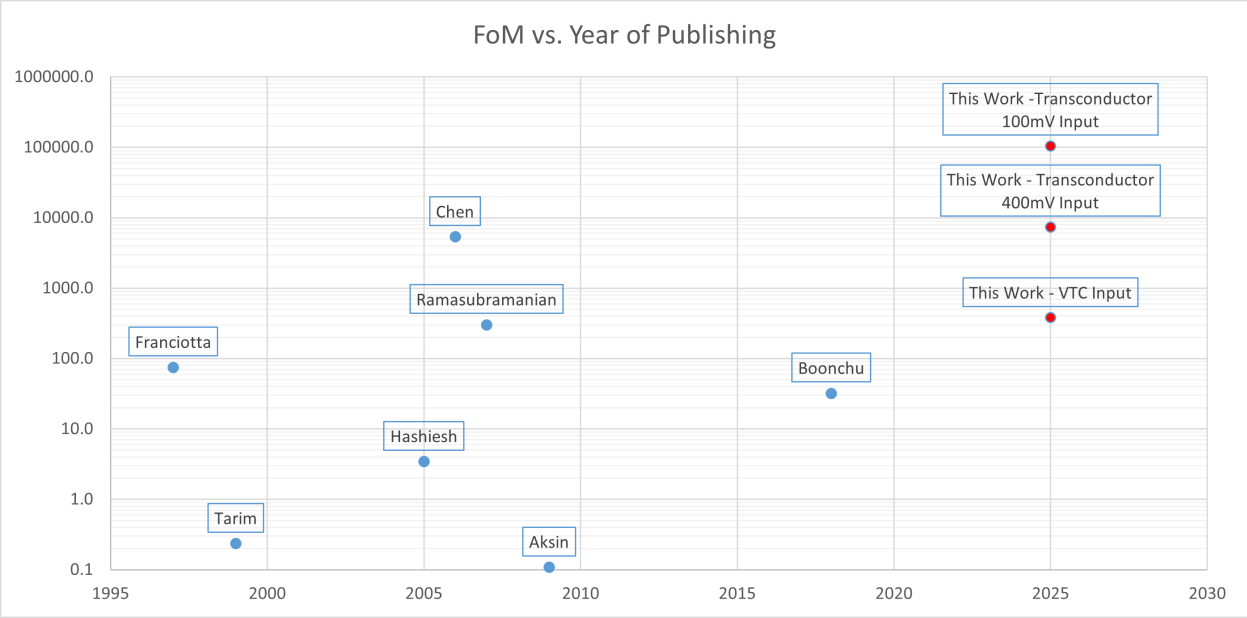


Figure 5.1: Comparing Figures of Merit with Other Published Work

The results of the analysis are shown in Table 5.1 and plotted in Figure 5.1. All results are based on the linearity of a single-tone, with the other input at a constant voltage. Some THD values were converted from dB to % in order to make them compatible. The results from this work are

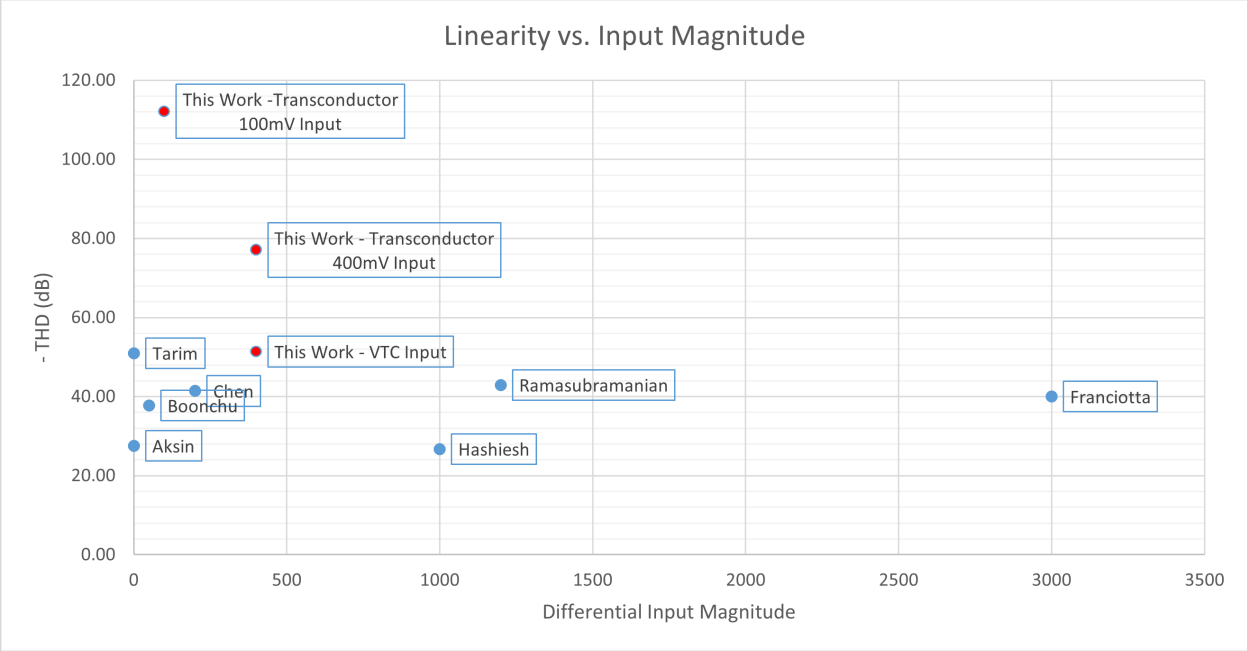


Figure 5.2: Comparing The Linearity of Multipliers vs. Input Magnitude

shown in 3 separate points, depending on the input used. The performance of the multiplier with a 100 mV input to the transconductor is significantly superior to any other voltage-mode multiplier analyzed, followed closely by the 400 mV case and the work by Chen. The performance with a VTC input does not perform as well, possibly due to the issues in simulating the VTC accurately, but its performance matches up with the work by Ramasubramanian.

The closest performing works to this one are by Chen and Ramasubramanian. Both are impressive in that they offer very good linearity performance in addition to superior performance in other areas. Chen's work offers significant speed advantages, though it was tested at 100 kHz and not the claimed 1.02 GHz bandwidth, and Ramasubramanian's work can handle input voltages 240 % greater than their supply voltage [43, 44]. However, neither is able to offer the linearity that the time-domain multiplier is capable of.

There is an argument to be made that this analysis is not useful, as it compares simulation

results to physical measurement results. While it is true that there is a disparity between the two sides of the comparison, it does not invalidate the core idea of this work. Firstly, this work is vastly superior to the other shown examples from Chapter 2, which were made with the same process, similar design targets, and simulated in the same way. Many of the designs shown in Figure 5.2 exhibit performances similar to those non-time-domain multiplier designs. While the performance of the time-domain multiplier will be worse in a physical measurement, it should still be superior to the other methods. Comparing just linearity figures, the THD of the time-domain multiplier would have to worsen by greater than 60 dB for it to just fall in line with the best competition. Losing that much performance is highly unlikely with a solid layout, using standard techniques such as common-centroid layout.

Table 5.1: Comparison to Other Published Voltage-Mode Multipliers

Multiplier Design	Year	Bandwidth (MHz)	Input Range (mV)	Linearity (THD%)	Power (μW)	FoM
This Work - 400 mV Transconductor Input	2025	16.7	400.0	1.4E-02	65.5	7271.5
This Work - 100 mV Transconductor Input	2025	16.7	100.0	2.5E-04	65.5	103456.8
This Work - VTC Input	2025	16.7	400.0	0.3	65.5	377.0
Boonchu [45]	2018	0.7	50.0	1.3	0.8	32.1
Aksin [46]	2009	70.0	0.5	4.2	76.8	0.1
Ramasubramanian [44]	2007	32.0	1200.0	0.7	179.0	301.3
Chen [43]	2006	1020.0	200.0	0.9	45.0	5333.3
Hashiesh [47]	2005	25.3	1000.0	4.6	1600.0	3.4
Tarun [48]	1999	99.4	1.0	0.3	1500.0	0.2
Franciotta [49]	1997	100.0	3000.0	1	4000.0	75.0

5.1.1 Falling Short of Goal Specifications

The performance targets in Table 4.1 were set prior to fully exploring the time-domain ideas and understanding the difficulties with their design. Though worthy goals, the requirements are not possible to reach with this topology. The largest difficulty is the power consumption relative to the

bandwidth.

The power consumption of the multiplier is unique compared to other structures in that it does not significantly affect the linearity. It does, however, affect the speed of operation, as it does other circuits. The bandwidth of operation, 16.67 MHz, is limited primarily by the settling time of the circuit. Increasing the bandwidth requires an increase in power, and due to the size of the circuit this increase in power consumption would not be outweighed by the bandwidth improvements. An operating period of 30 ns balances the two issues, though future work may find more power-efficient circuits that would allow for bandwidth increases. Some possible suggestions are discussed in Section 5.2.

5.1.2 Strengths of the Design

Despite not quite reaching the initial goals, this work does present strong advantages as well. One main motivation of investigating the time-domain was possibly linearity improvements, and those gains have been realized. Though these are just simulation results, linearity (unlike bandwidth and power consumption) is a property that does not change greatly from the simulation results. As such, even if the linearity decreases due to parasitics and mismatch, the performance should still be better than other designs that this work has been compared against.

This design is also able to handle very large input voltages for its supply of 0.8 V, and these input voltages are at the same common-mode input level. This is important, as it means that the multiplier can have its inputs used interchangeably. Most other structures, most famously the Gilbert Cell, cannot do this, and this makes them impossible to cascade easily like the structure in this work can. Also, thanks to the very flexible nature of the multiplier's gain, the output magnitude of the multiplier can reach the same level as the input magnitude, another requirement of cascading multipliers together without intermediate stages.

Finally, because the magnitude of the time signals can be lengthened to any amount of time, unlike a voltage signal, the dynamic range of the time signal can be theoretically unlimited. Practically, it is limited by the need for a usable bandwidth, as increasing the dynamic range requires increasing the operating period and reduces bandwidth, but this offers a great advantage. The integration of current onto the capacitor also reduces the noise from that source, so this design is capable of high dynamic range. Unfortunately, this is difficult to simulate as the use of the clocking requires transient noise analysis, and so demonstration of this property is not shown here.

5.2 Opportunities for Future Work

Despite falling short of the initial goals for the design, there are still many improvements that could be made that had to be skipped due to time constraints. The following are options for further improvement of the design. Some are simple, such as slowing down the design to improve performance in other areas, while others are more involved, such as minimizing delay dispersion in the VTC's comparator. However, many of the ideas have been discussed in other works, and should be implementable.

5.2.1 Structural Improvements

The largest improvement for this design may be to redesign it for a slower operating bandwidth. This work presents a multiplier operating with a 30 ns operating period. This circuit is able to deliver very impressive linearity for its input magnitude, but the main limits on its linearity are based in the limited operating time for all components to settle. The transconductor needs to settle within the allotted time at the beginning of the PWM period, when the RST signal is shunting the current to ground while the appropriate value is reached. If a longer time period is used, this settling

can take longer without losing output magnitude, as the capacitor voltage will be reached with a lower current over a longer time. The G_m of the comparator is related to that output current, but the overall gain of the multiplier could be kept the same by raising A_t to compensate for a lower G_m. A_t can be adjusted simply by changing the capacitor values, and since the capacitors are charged with a constant current and constant voltage, the power consumption would not rise. Thus, power consumption would be reduced and linearity would increase, which other multiplier designs cannot do.

The other major improvement for the structure would be the use of a differential VTC. The current design uses two copies of the VTC discussed in Section 3.2.4, one for each half of the differential input. This means that two separate comparators are needed, one for each VTC, doubling the power consumption of the VTC. Unfortunately, very few differential VTCs have been proposed at the time of this work. A "pseudo-differential" VTC was proposed by Hassan, but it in fact uses two separate VTC cores (like this work) and only has a SFDR of about 40 dB [50]. Work by Xie has also proposed a differential VTC, but it uses voltage-controlled oscillators in a feedback loop similar to a PLL, rather than PWM signals that could control current flow [51]. If a highly linear differential VTC could be created, it would be of great use in time-domain multipliers such as this design.

5.2.2 VTC Improvements

The VTC could be improved with a differential VTC, as discussed above, but to create sharp transitions a comparator is needed for most designs. In order to reduce the delay and transition time of the output, the comparator consumes a significant portion of the total power budget. Because there are two comparators that need to match up well, the comparator also needs a well controlled input offset and low delay dispersion. The comparator implemented in this work includes switchable

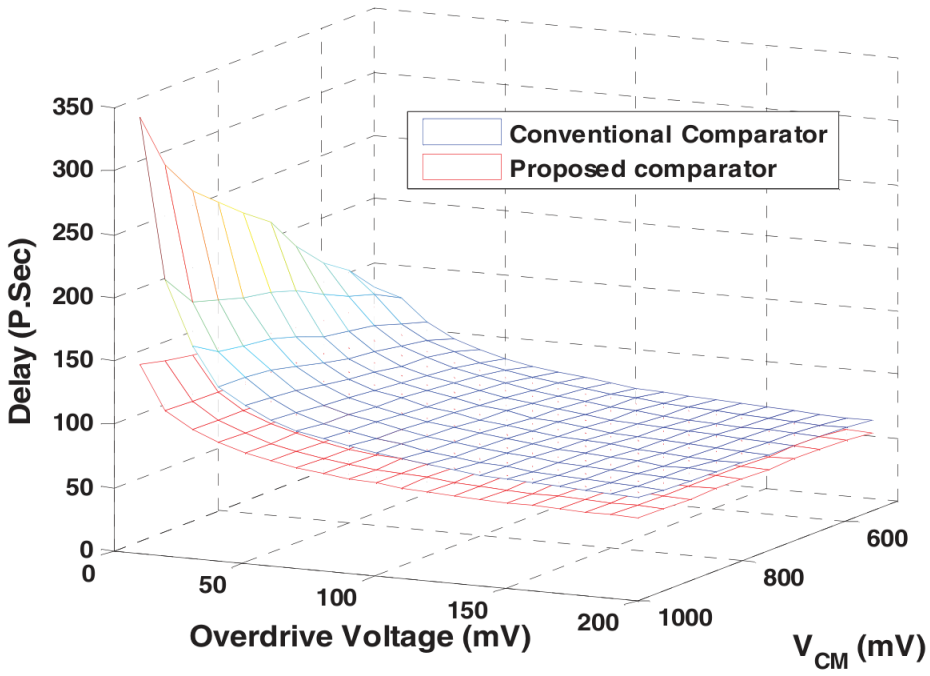
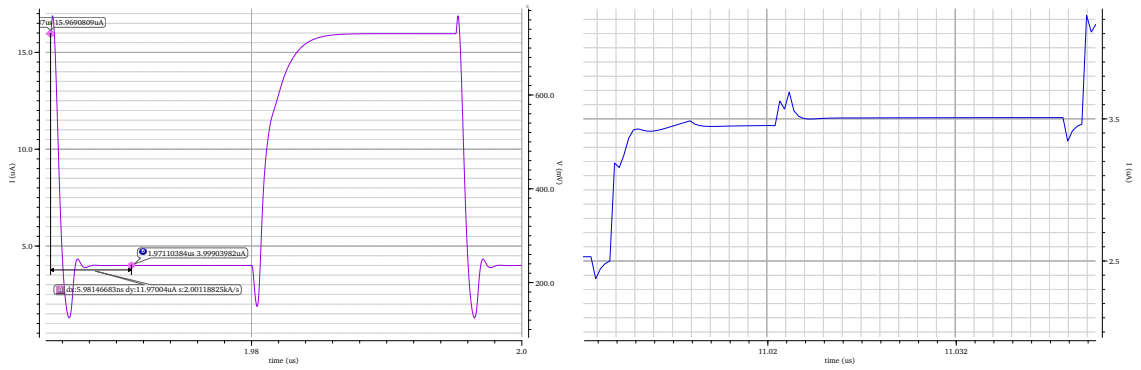


Figure 5.3: Example of Minimizing Delay Dispersion in Comparator [7]

compensation capacitance to allow for auto-zeroing of the comparator and has good delay dispersion with VTC inputs from 200 mV-600 mV, but consumes about one-sixth of the total power consumption of the design on its own.

Like with differential VTCs, the issue of delay dispersion has only been studied by a few works. However, further improvements of VTCs will require that the comparators be optimized for it. [7, 39, 40] offer opportunities to improve the design. Alternatively, [6] uses simple inverters to create the comparator, which can work well if willing to have the output transition set to roughly half of VDD, rather than a lower value to allow for larger overdrive voltages and lower charging currents.



(a) **(b)**

Figure 5.4: Examples of Slow Transconductor Settling

5.2.3 Transconductor Improvements

Transconductor design has been developed much more than VTC design, but still offers challenges in thsi use case. The transconductor contributes non-linearity in two ways. One is distortion, where the output current is not proportional to the input anymore. This issue has been well understood, and can be improved with feedback and degeneration like was done in this work. The second issue is settling of the output current. Lowering the output current means that the current available to charge and discharge the various parasitic capacitances in the transconductor is limited, slowing down settling. On top of that, the switching of the output current can result in charge injection to sensitive bias nodes, forcing every circuit connected to the node to settle at the same time. Figure 5.4b shows this behavior, where the current settles and then is disrupted when one of the output currents is steered to ground.

The slow settling behavior may be addressable via dynamic biasing. With dynamic biasing, the slew rate and bandwidth of the transconductor could be increased only during the transitions. The issue would be maintaining stability, which was why it was not attempted in this work. However, moving to dynamic biasing may allow the use of a linear transconductor structure without any operational amplifiers included, such as the circuit in Figure 5.5 from Carusone's text [8]. This

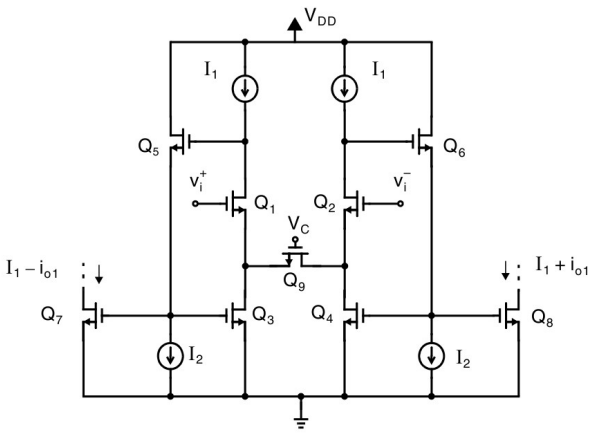


Figure 5.5: Linear Transconductor Without Amplifiers [8]

would save significant power, as the current used to generate the loop gain is also used to charge and discharge the important nodes of the transconductor. However, stability can be an issue in modern nodes, as many of the poles are of similar magnitude.

5.3 Review

As computing becomes continually cheaper, the demand for power efficient circuits has only grown. For many low SNR tasks, such as neural networks, analog circuits may offer opportunities to decrease power consumption for power-hungry digital computing tasks, such as multiplication. However, as modern semiconductor processes have shrunk, the linearity of analog circuits has degraded due to limits on supply voltages and the influence of second-order effects. New circuit topologies are necessary in order to solve these issues. This work proposed a time-domain multiplier, using a novel method of encoding the inputs, to increase linearity in a modern node.

Prior work in analog multiplication had many issues that prevented use in today's computing systems. Most dominant of these issues is that the decrease of supply voltages has limited the input and output signal ranges of analog circuits, requiring the move away from formerly-common

techniques such as stacking devices or using triode-mode devices in large signal applications. This has ruled out the use of the most basic topologies, such as the Gilbert Cell and the triode-mode multiplier. Other designs relied on techniques like the translinear principle, but the use of BJTs or MOSFETs operating in deep subthreshold does not integrate well in modern processes. Almost all designs shared limitations on input magnitude to ensure linearity, with few being able to handle inputs greater than $100\,\text{mV}$ with much larger supply voltages than today.

This work proposed a multiplier that multiplies input voltages via the use of time-signals and currents. These new values, generated by a voltage-to-time converter (VTC) and transconductor respectively, could be used by having the time-signal control how the current is integrated onto a capacitor. Combining four of these structures allows for the creation of a four-quadrant multiplier, capable of high linearity and handling large input signals.

After simulating this design in a 20nm process, the performance of the multiplier was found to be superior to the other voltage-mode multipliers examined. Impressively, the multiplier handled a $400\,\text{mV}$ input with a total harmonic distortion (THD%) of $0.014\,\%$. The design also offers great benefits in its output signal range and in operability within a larger system, as the multiplier inputs are interchangeable in all ways. This design offers great promise for future development, especially investigation into linear VTC structures and the creation of a truly differential VTC. The time-domain multiplier offers top-of-class linearity and dynamic range, and may prove to be a competitor for the future of signal processing circuits.

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