Digital Intensive Transceivers for High-Speed Serial Links

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Dedication

I dedicate this work to my family, friends, and my advisor, Prof. Chris H. Kim.

Abstract

Digital intensive circuit is gaining popularity to mixed-signal circuit design as they are friendly to technology scaling. The simple inverter-based implementation is easy to design in the new process while immune to process-voltage-temperature (PVT) variation. The growing complexity equalization technique can benefit from the robustness design to enhance the link performance. Also, as the data rate increases, accurately measurement is more challenge since there is no time-domain calibration for bit error rate (BER). The issue mentioned above motivates the in-situ measurement circuit, which enables simple testing setup and obviates the uncertainty.

Three digital intensive high speed serial link transceiver for various kinds of application is proposed in this thesis along with in-situ measurements circuit for BER and channel loss testing. First, a digital-intensive on-chip serial link achieving a 10 Gb/s data rate over a 10mm interconnect was demonstrated in a 65nm GP process. A 3-tap half-rate feed forward equalizer (FFE) was implemented for signal pre-emphasis in the transmitted block. On the receiver side, a 2-tap half-rate time-based decision feedback equalizer (TB-DFE) was employed to cancel out inter-symbol-interference (ISI) noise. A 2^{15-1} pseudo random binary sequence (PRBS) generator and an in-situ bit error rate (BER) monitor were designed for bit stream generation and convenient eye-diagram measurements. The measured energy-efficiency of the transmitter and receiver was 31.9 and 45.3 fJ/b/mm, respectively, for a data rate of 10 Gb/s. A BER less than 10^{-12} was verified for an eye width of 0.43 Unit Interval (UI).

In second work, we present an 8 Gb/s time-to-digital converter (TDC) based receiver with a time-based front-end in 65nm CMOS specifically designed for in-package serial link applications. The proposed receiver converts the channel signal to a corresponding time delay, which is amplified by a novel delay line based time amplifier. Next, a time-to-digital converter generates a 4 bit code which is used for digital equalization. The proposed design is digital intensive and hence highly resilient to voltage headroom and/or PVT issues. A bathtub curve and time-domain eye-diagram were measured by an in-situ BER monitor circuit. An energy-efficiency of 2.1 pJ/b was achieved at 8 Gb/s for a 7 mm link. The receiver area is $240\times120\mu m^2$.

Last, a single-ended digital-intensive four-level pulse amplitude (PAM-4) transceiver with a 2-tap time-based decision feedback equalization (TB-DFE) and an in-situ channel loss monitor has been demonstrated in 65nm CMOS process for high speed memory interface. A proposed differential voltage-to-time converter (DVTC) increases the linearity and dynamic range by 67% compared to prior art. The four-level signal comparison and decision feedback equalization (DFE) operation are performed entirely in the time domain using programmable delays and a phase detector (PD). The in-situ channel loss monitor was proposed to measure the channel loss in the time domain instead of measuring the S-parameter. By using the on-chip BER monitor, the proposed transceiver can achieve BER less than 10^{-12} while energy-efficiency is 0.97pJ/b for a 32Gb/s data rate. The chip area includes the transmitter and receiver is $0.009mm^2$.

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Chapter 1. Introduction

High speed input/output (I/O) playing an important role in recently highly developed technology from consumer electronics to supercomputer such as smartphones, automatic driving, virtual/augmented reality (AR/VR), and internet of thing (IoT) as they reply on multiple high speed link to communicate between subsystems. Fig. 1.1 shows the several standard data rate roadmap reported by ISSCC 2019 [1]. The data rate is increasing two times every four years. The data rate over 100 Gb/s is expected to come soon. At the same time, new packaging technology has been proposed to increase the total bandwidth by increasing the pin number. As a result, high speed I/O power consumption becomes a great portion of total chip power. Equalization techniques such as continuous time linear equalizer (CTLE) and decision feedback equalizer (DFE) have been proposed to achieve the targeting data rate while maintaining reasonable energy efficiency. However, most of this equalization technique is analog intensive approaching and usually requires high power consumption current mode logic (CML) and area hungry inductor peaking technique. Moreover, they can not take the full benefit of technology scaling and sensitive to PVT variation and low supply voltage operation.

To take full benefit of technology scaling while achieving the required data rate, digital intensive time-based circuit design techniques have been proposed to perform the equalization function and achieve comparable performance with analog intensive circuit design techniques. The proposed transceiver is targeting for the various application, including on-chip interconnect, system-in-package (SiP), and memory interface.

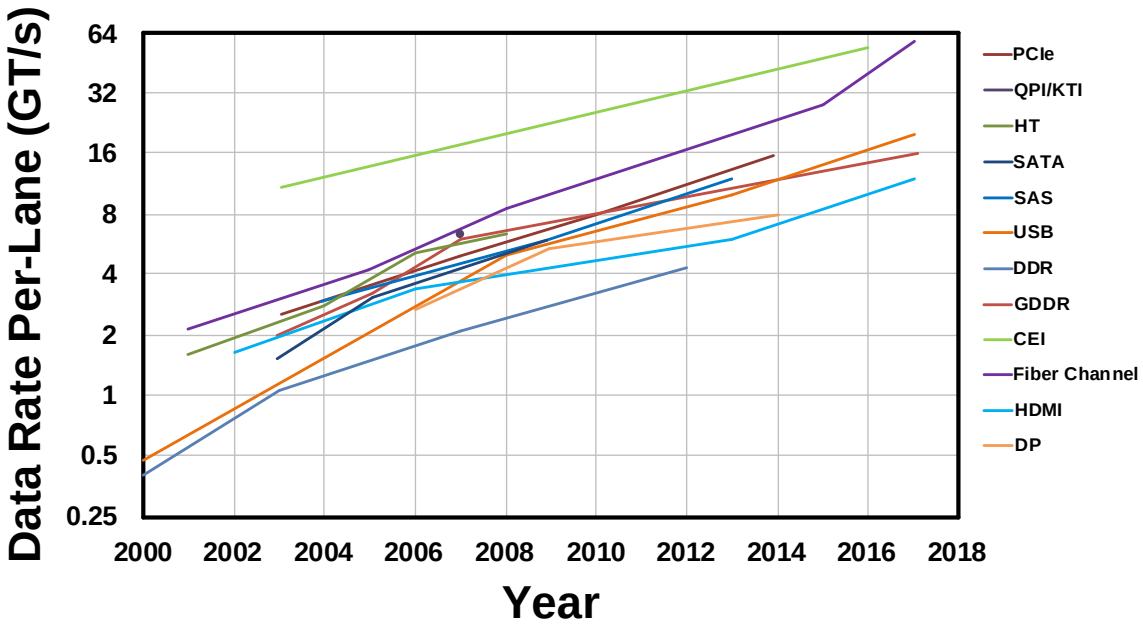


Fig. 1.1: Roadmap of data date per pin for different I/O standards [1].

1.1 Time-Based Decision feedback equalizer

Fig. 1.2 shows the road map of the processor chip area versus technology node. As shown in the figure, the chip area is not scaling with the technology node. On the contrary, chip area is even twice compared to older technology. Hence, the interconnection is longer and requires more powerful equalization technique to maintain data integrity. Decision feedback equalization (DFE) technique has been adopted in high speed off-chip serial link for a long time but has not yet used in on-chip interconnect applications. In older processor, the receiver without DFE is still working well due to the shorter interconnect length. However, when the processor becomes larger, high loss and multiple reflections will induced by longer connection. The complicated circuit design technique in conventional voltage-based DFE is not suitable for on-chip interconnect as they usually rely on current

mode logic (CML) circuits. This work proposed a time-based DFE where the equalization is performed in time delay and implemented by the inverter delay line. The simple inverter-based implementation can benefit from technology scaling and easy to scale up the DFE taps by adding the number of delay stages. Furthermore, the in-situ time-domain BER monitor is introducing to measure the time-based circuit performance. The time-based DFE and in-situ BER monitor are implemented in 65nm GP process.

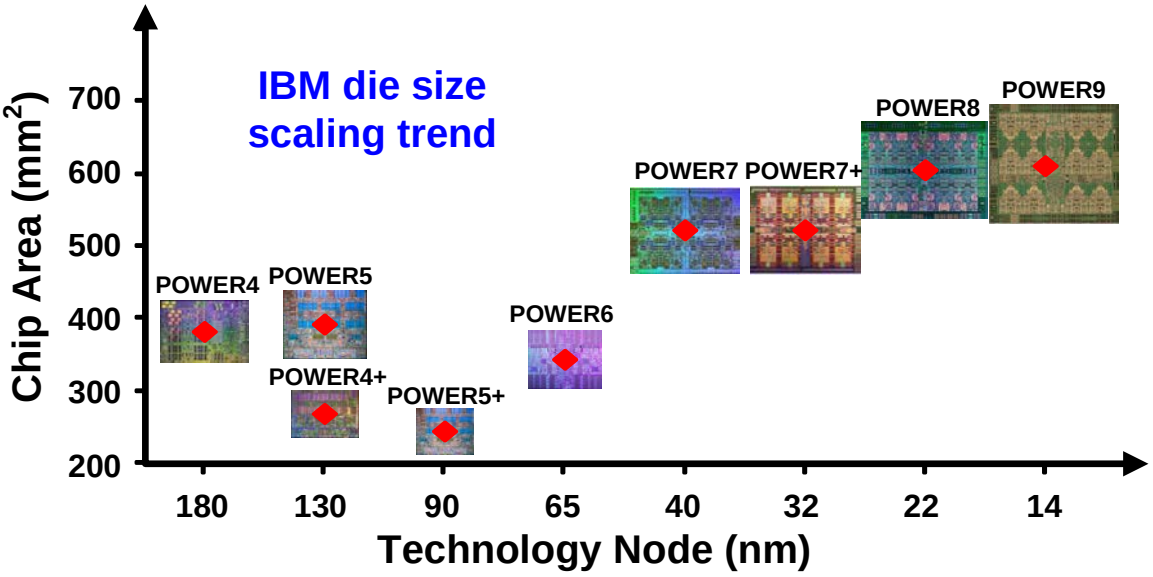


Fig. 1.2: Roadmap of processor chip area vs. technology node.

1.2 Time-to-Digital Converter Based Receiver

Multi-chip packages allow chips fabricated in disparate technologies to be integrated into a single package, reducing form factor and improving overall system performance. High speed communication circuits for such system-in-package (SiP) applications have stringent area, power, and voltage requirements compare to traditional high speed IO applications. The analog-to-digital converter (ADC) based receiver usually implemented

with conventional analog front-end (AFE) is no longer suitable for this new packaging technology. The ADC-based is gaining attention due to its powerful post-digital equalization. However, they still rely on AFE to reduce ADC design loading. The purpose of this work is to develop a highly digitalize front-end for digital-based equalization receiver. A time-to-digital (TDC) based receiver with time-based front-end is introduced where the amplification function is performed in time-domain by delay chain. The vernier line TDC will convert the amplified delay to digital code for digital post-processing. The proposed transceiver is demonstrated in 65nm GP process for 7mm in-package link.

1.3 PAM-4 Time-Based Decision Feedback Equalizer

Several modulation schemes, including pulse amplitude modulation (PAM), duo-binary, and multi-tone signals, have been proposed to increase bandwidth efficiency to improve the data rate for high speed memory interface. However, they usually involved more complicated circuit technique and require higher power consumption and chip area compare to non-return-to-zero (NRZ). To further reduce the design complexity for PAM-4 signaling, in this work, a PAM-4 time-based DFE is proposed that different signal level comparison is performed in multiple delay lines for DFE functionality. Apart from digital intensive implementation, the digital-to-analog converter (DAC) usually adopted in the voltage-based PAM-4 DFE to generate different threshold voltage for different level comparison is not required. Instead, a simple programmable delay buffer can generate the threshold delay for time-based operation. In addition to PAM-4 transceiver, in-situ channel loss monitor is proposed to measure the channel characteristic in time-domain. The proposed monitor circuit can alleviate the extensive setup for scattering parameter (S-

parameter) measurement. The circuit techniques mentioned above are also implemented in 65nm GP process.

1.4 Summary of Dissertation Contribution

Several contributions have been made in this dissertation to improve the performance of the state-of-the-art high speed serial link architectures.

To summarize the key contributions of this research: 1) a time-based DFE has been proposed, where the equalization function is performed in time delay by inverter delay line, which can take full advantage of CMOS scaling. The DFE taps can be scaled up by simply adding more delay stages degrading the throughput. 2) To alleviate the analog front-end (AFE) in receiver, time-based front-end has been introduced for TDC-based receiver. The amplification function is entirely performed in time domain by the delay line. 3) A PAM-4 transceiver is presented where PAM-4 operation is performed in time-based DFE. 4) Two in-situ measurement circuits have been demonstrated to alleviate testing setup. One is a time-domain BER monitor to test the time-based operation circuit. Another one is time-domain channel loss monitor to characterize the channel response.

The remainder of this dissertation is organized as follows. Chapter 2 presents the design of the time-based DFE in 65nm CMOS technology along with the concept of the in-situ time-domain BER measurement circuit. Chapter 3 illustrates the TDC-based with time-based front-end. Chapter 4 discusses the proposed PAM-4 transceiver with PAM-4 time-based DFE. The in-situ channel loss monitor is also demonstrated in this chapter. Chapter 5 summarizes this dissertation.

Chapter 2. A 10 Gb/s Digital-Intensive Time-Based Decision Feedback Equalizer for On-Chip Serial Link

2.1 Introduction

On-chip data buses are performance-critical circuits in modern processor systems as they are responsible for transferring a massive amount of data between various processing units and cache blocks at gigahertz frequencies. Despite the aggressive pace of transistor scaling, interconnect speed and interconnect power have not scaled proportionally due to large RC parasitics, large die size, increasing number of processing units, and higher operating frequencies [2]-[7]. When the data rate exceeds the RC time constant of an interconnect wire, significant inter-symbol-interference (ISI) may occur. Meanwhile, due to the longer interconnect length and high operating frequency, interconnect power has become a significant portion of the total chip power consumption.

A simple solution to overcome the interconnect bottleneck is adding repeater circuits to break up a long wire into shorter segments, which enhances the overall latency and throughput of the channel [8]-[9] as shown in Fig. 2.1. This method is effective and relatively straightforward to implement as synthesis tools support automated buffer insertion. However, tools may not be able to place repeaters at their desired locations due to large functional blocks underneath the interconnect path. Signals may have to be

rerouted or the chip floorplan may have to be disrupted to accommodate the repeaters. This may result in additional design time, loss in performance, and increased power consumption due to redundant repeaters [10].

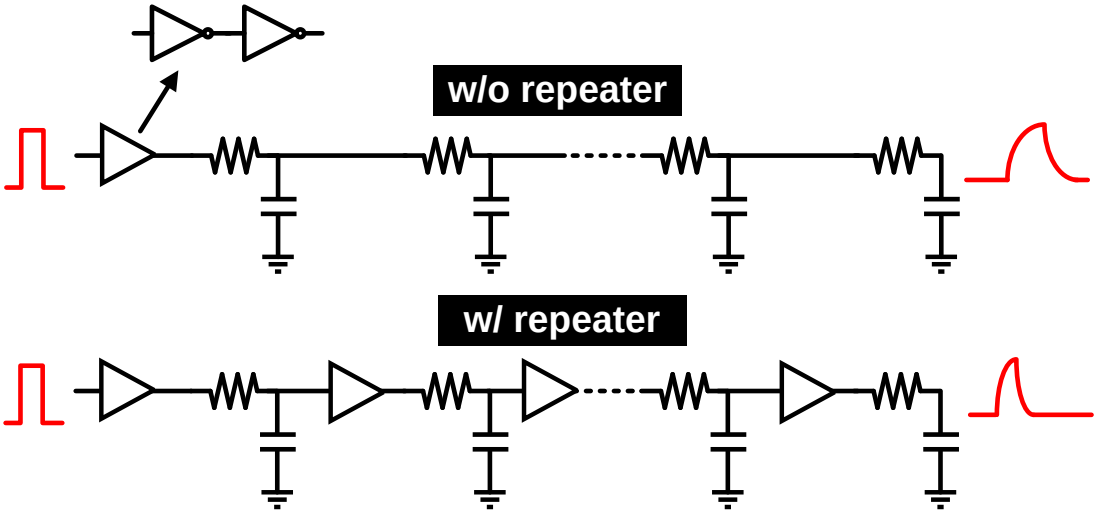


Fig. 2.1: Repeater circuits can improve the latency and throughput of on-chip interconnects.

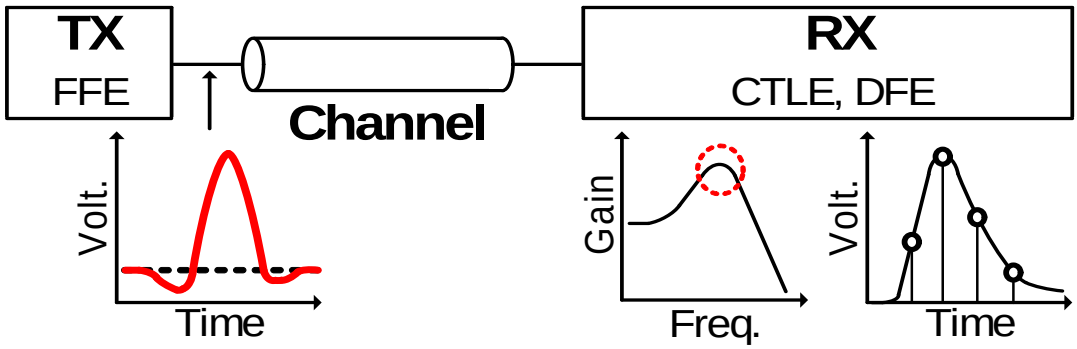


Fig. 2.2: Equalization techniques such as FFE, CTLE, and DFE have proven to be effective for high-speed IO applications.

Recently, serial links have been gaining popularity for on-chip point-to-point applications as they can achieve 10 Gb/s or higher data rates with high power efficiency without disrupting the chip floorplan. Many of them employ low-swing signaling which

can lower the power consumption but requires sophisticated transmitter (TX) and receiver (RX) circuits. Equalization techniques such as feedforward equalizer (FFE), continuous time linear equalizer (CTLE), and decision feedback equalizer (DFE) have been widely used for off-chip serial link applications as shown in the Fig. 2.2 [11]-[14]. FFE [13]-[14] is a technique implemented in the transmitter block to pre-distort the signal to compensate for the channel loss. CTLE and DFE are implemented in the receiver block. CTLE is basically an amplifier which provides a peaking gain to the signal frequency of interest [9], [11]. DFE on the other hand is used to cancel ISI noise in the incoming data stream by subtracting the ISI component estimated based on the preceding bits and proper weights [12]-[14]. The number of preceding bits and the weight values for the DFE filter are determined by the channel characteristics. Generally speaking, a channel with high loss requires a longer DFE filter. Some recent works have proposed using equalization techniques to improve the communication speed and energy-efficiency of on-chip serial links. For example, a charge-injection based FFE was proposed in [15] where capacitive coupling was used to pre-distort the TX signal [16]-[17]. In [18], a current mode transceiver with a pre-emphasis driver and an active inductor was demonstrated. However, these on-chip serial links incorporate a complex analog-intensive design style which suffers from headroom issues and process-voltage-temperature effects. Moreover, they do not take full advantage of the technology scaling benefits and require considerable re-design effort in every new technology. There has not been any report of DFE applied to on-chip links due to the complicated circuit design and large power overhead of current mode logic (CML).

In an effort to make DFE more digital-friendly and amenable to technology scaling, we propose a time-based DFE (TB-DFE) technique where the DFE operation is performed entirely in the time domain using digital circuits. Time-based circuits for DFE implementation was first proposed in [19] for off-chip links. However, their design was primarily based on analog-intensive circuits. In this work, we demonstrate a digital intensive design of time-based DFE utilizing inverters and digitally-controlled delay elements which are readily available in advanced technologies. Another key advantage of the proposed TB-DFE is that higher number of taps can be incorporated by simply adding more delay stages without affecting the DFE throughput. Our work dose not leverage this property as on-chip interconnects typically do not require more than 2-3 taps. However, we think TB-DFE can be a promising candidate for off-chip links or body channel communication (BCC) applications where large number of taps is preferred.

The remainder of this chapter is organized as follows. Section 2.2 describes conventional voltage mode DFE for comparison purpose. The proposed time-based DFE is described in section 2.3. Implementation details of an 10mm on-chip serial link with a time-based DFE are given in section 2.4. Section 2.5 provides details of the in-situ bit-error-rate (BER) monitor used to measure the time-domain BER eye diagram. Measurement results are discussed in section 2.6. Finally, conclusions are drawn in section 2.7. The conference version of this work was published in [20].

2.2 Conventional DFE Architecture

DFEs have become indispensable for off-chip links, however they have not been adopted in on-chip links due to their design complexity, and area/power overhead. For

better understanding of the proposed time-based approach, we first describe the basic operation of the conventional DFE. Voltage-based DFE filter operation can be expressed as $V_{DFE} = V_{RX}(t) + \sum_i x[n-i] \cdot w_i$ where $V_{RX}(t)$ is the incoming analog voltage, $x[n-i]$] is the i-th preceding bit, and w_i is the corresponding weight. As shown in Fig. 2.3, the summer and slicer circuits of the conventional design are implemented using CML. The weight of each DFE filter tap corresponds to the CML tail current. The operation principle is as follows. The analog voltage signal $V_{RX}(t)$ determines the pull-down current of the first CML stage. The pull-down current of the other CML stages are determined by the preceding data coupled with the appropriate weights W_1, W_2, … W_N. By subtracting the weighted sum of the preceding bits from the original analog signal, the ISI noise component can be cancelled out.

CML is a natural fit for DFE implementation. However, on-chip serial link applications cannot afford such analog-intensive circuit solutions as they have to be integrated in a complex processor. Another fundamental limitation of CML based DFE implementation is the throughput loss as the number of taps increases. This is because parasitic capacitance increases linearly with the number of CML stages connected to the output node. In addition, the common mode voltage will change with different number of CML branches affecting the gain and linearity of the summer circuit. Complex biasing circuits are needed to mitigate this issue which makes DFE less attractive for on-chip link applications. To further understand the performance limitations of CML, we simulated the unity gain frequency f_T for a CML circuit with different number of pull down branches. As shown in Fig. 2.3, the total parasitic capacitor on node VDFE is equal to $C_{Total} = C_M +$

$C_{T1} + \cdots + C_{TN}$, where C_M denotes the main tap capacitance and C_{TN} denotes the N-th post tap capacitance. Fig. 2.4 shows the simulation results of f_T versus number of taps assuming an I_{BIAS} of 2mA. The parasitic capacitance of each post tap was assumed to be 10% of the main tap capacitance. From the simulation results, we can see that increasing the number of taps degrades f_T and limits the maximum throughput of the DFE filter. The bandwidth degradation is not only caused by the increased parasitics but also by the reduced current of the main stage. The reduced main stage current also affects the common mode voltage level, necessitating the redesign and resizing of the CML circuit.

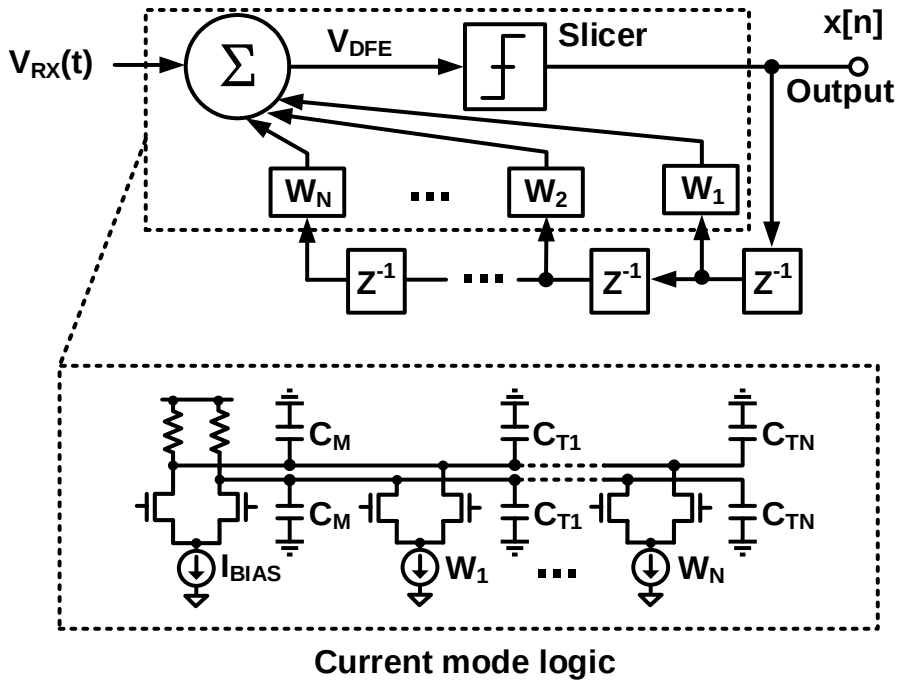


Fig. 2.3: Conventional DFE consisting of a current mode logic (CML) summer and slicer circuit. DFE filter weights (W_1, W_2, etc) are incorporated in the CML tail current.

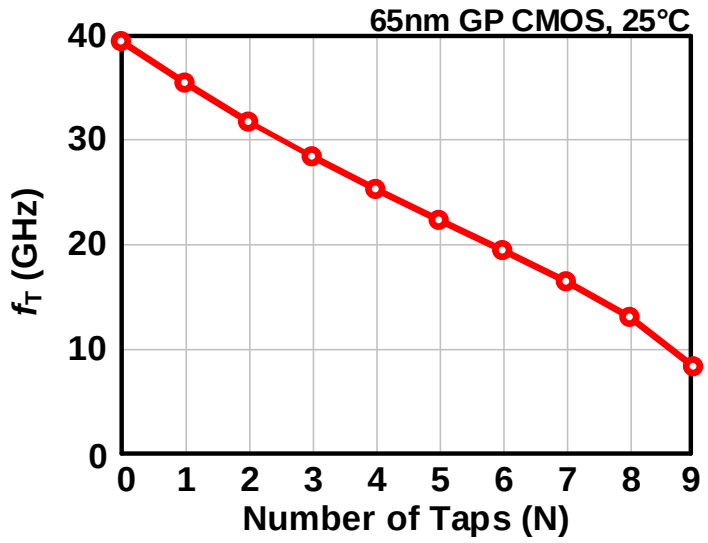


Fig. 2.4: Simulation unity gain frequency versus number of DFE taps for a conventional CML based DFE circuit. Bandwidth decreases with higher number of DFE taps.

2.3 Proposed Time-based DFE

2.3.1 Operation Principle of Time-based DFE

In this section, we describe the proposed digital intensive time-based DFE approach, where equalization is performed entirely in the time domain using digital circuits. The basic idea is to perform the time domain version of the DFE filter expressed as $T_{DFE} = T_{RX}(t) + \sum_i x[n-i] \cdot w_i$. This can be achieved by replacing the CML summer and slicer circuit with an inverter-based delay line and phase detector (PD) as shown inFig. 2.5. In conventional DFE, the weights are built into the CML tail current while in TB-DFE, the weights are incorporated in the inverter delays. The high-level operation is as follows. As shown inFig. 2.6, the input clock is fed to both the main delay line containing a voltage-to-time (VTC) stage, and the reference delay line. The incoming analog voltage signal is converted to an

analog delay by the VTC stage. For instance, data ‘1’ will result in a longer delay and vice versa. The VTC delay is then added to the delay of the later stages which are determined by the filter weights and previously sampled bits. The PD compares the delay of the main path with the delay of the reference path to generate the binary output. This is equivalent to the slicer operation in a conventional DFE, but in the time domain. The binary output is fed back to the DFE filter for the next cycle. The proposed time-based architecture has several unique advantages compared to the CML based architecture such as good scalability, good low voltage operating margin, compact area, good tuning capability for process compensation, and no throughput loss for higher number of DFE taps.

The reason why there is no throughput loss is because the number of DFE taps can be increased by simply adding more delay stages. Adding more delay stages does not affect the parasitic capacitance of the individual stage and hence the throughput remains constant regardless of the number of DFE taps. On the contrary, parasitic capacitance of the CML based implementation increases linearly with the number of DFE taps. This degrades the DFE performance as seen inFig. 2.4. The constant throughput behavior was verified by simulating the delay of the programmable delay stage. Two inverters were chained together to form a single non-inverting delay stage which is equivalent to a single DFE tap. The shift register in the feedback path does not contain any logic function and hence can operate faster than a single delay stage. To simulate the maximum operating frequency, we took the layout of a standard inverter chain and extracted the RC parasitics. Then we gradually increased the clock frequency until the inverter delay decreased by 0.2ps. This corresponds to the frequency when the signal amplitude starts to degrade. Degradation in the signal

amplitude has two detrimental effects. First, it will make the DFE delay compensation less precise. Second, the non-full swing signal will induce timing offset in the PD circuit. The maximum operating frequency was simulated while varying the number of delay stages (Fig. 2.7). For accurate timing simulations, random dynamic noise option was turned on. This captures the impact of device noise introduced by the additional delay stages on clock jitter. In our simulation setup, the maximum noise frequency was set to be 5 times higher than the maximum operating frequency while the minimum noise frequency was set to be 1/(simulation time), which is 10MHz. All other noise parameters were set to their default values. The baseline clock period without noise was set as 55ps, which corresponds to a frequency of 18.2 GHz. To account for the slight increase in jitter in the later stages, we increased the clock period by two times the maximum jitter when measuring the maximum clock frequency of a particular stage. As seen in the simulated waveforms inFig. 2.7, transient noise due to the additional delay stages results in only a modest increase in jitter and hence the maximum operating frequency remains relatively constant. For instance, only a 0.76 ps increase in clock period was necessary to account for transient noise effects in the 9th stage output. It is worth clarifying why the maximum operating frequency in Fig. 2.7 is significantly higher than the measured frequency (i.e. 10Gb/s) from the actual test chip. This discrepancy is due to the minimum capacitance configuration used in the simulation as well as the higher parasitic capacitance of the fabricated chip and the specific bit-error-rate criterion.

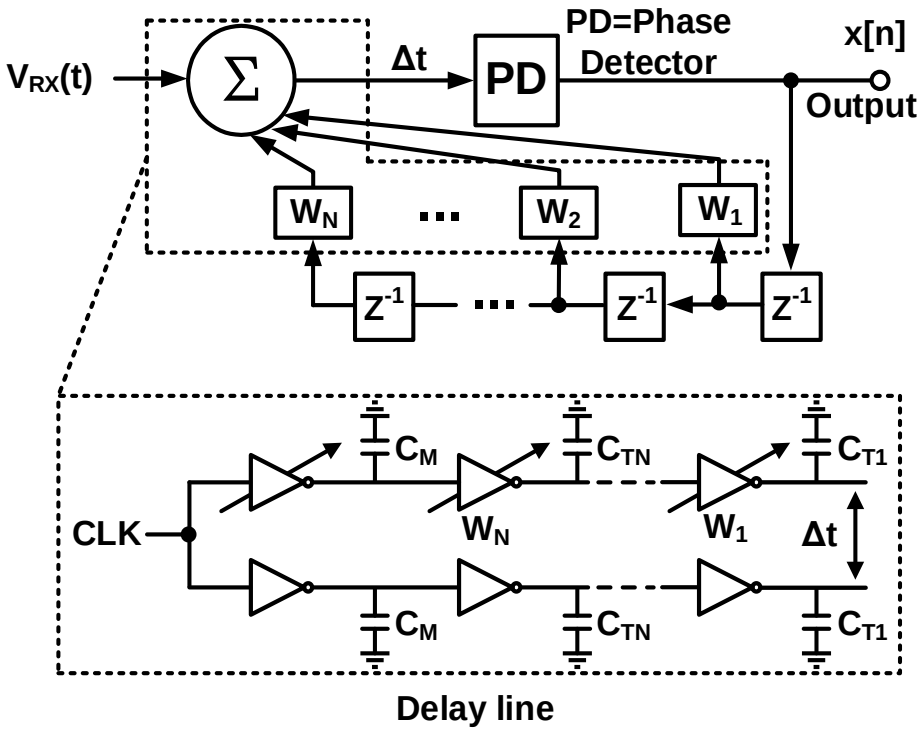


Fig. 2.5 Proposed time-based DFE architecture with two inverter based delay lines and a phase detector. DFE weights control the delay of each inverter stage.

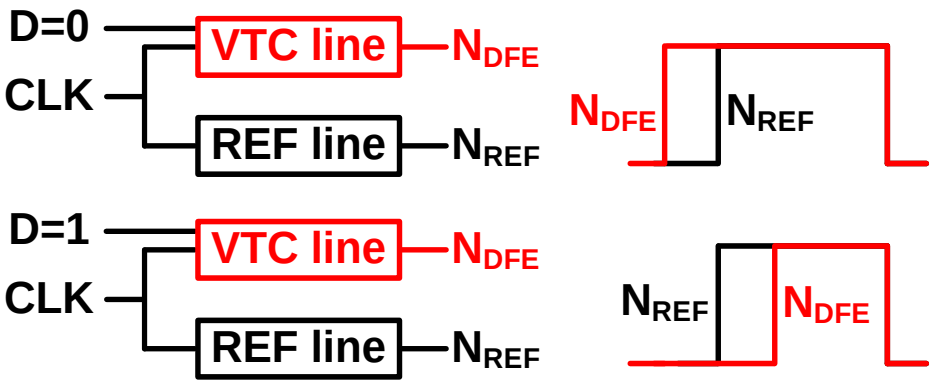


Fig. 2.6: High-level operating principle of the TB-DFE. The delay difference between the main delay line and the reference delay line determines the output bit.

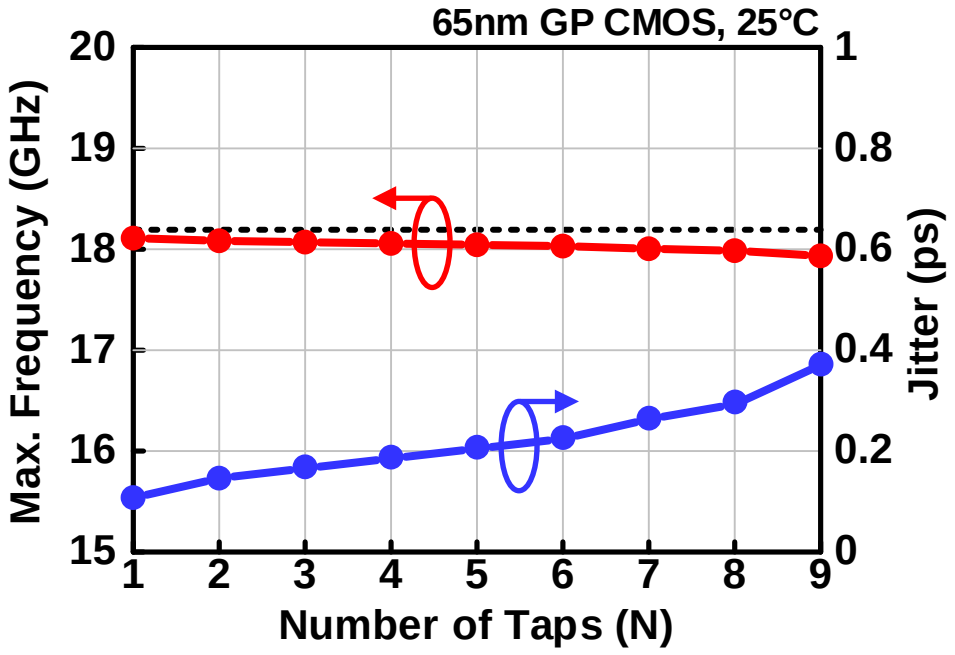


Fig. 2.7: Maximum operating frequency and jitter for each TB-DFE output stage. Transient noise option was turned on to account for the increased jitter in the later delay stages. Simulation results show that the operating frequency remains relatively constant even for a high number of DFE taps.

Fig. 2.8 shows the operation example of the TB-DFE for a bit sequence of '0100'. Due to the channel ISI, the original square waveform becomes a smoother waveform VRX(t) by the time it reaches the receiver. The delay line signals before and after the DFE operation are shown in Fig. 2.8 (middle). The distorted voltage is converted to the corresponding time delay which contains ISI noise. This results in a reduced sensing margin between the DFE path signal NDFE and the reference path signal NREF. The reduced phase difference may lead to a bit error. TB-DFE utilizes the preceding bits to expand the phase difference leading to a more reliable phase detection. The improvement in sensing window using the TB-DFE is illustrated in Fig. 2.8 (bottom).

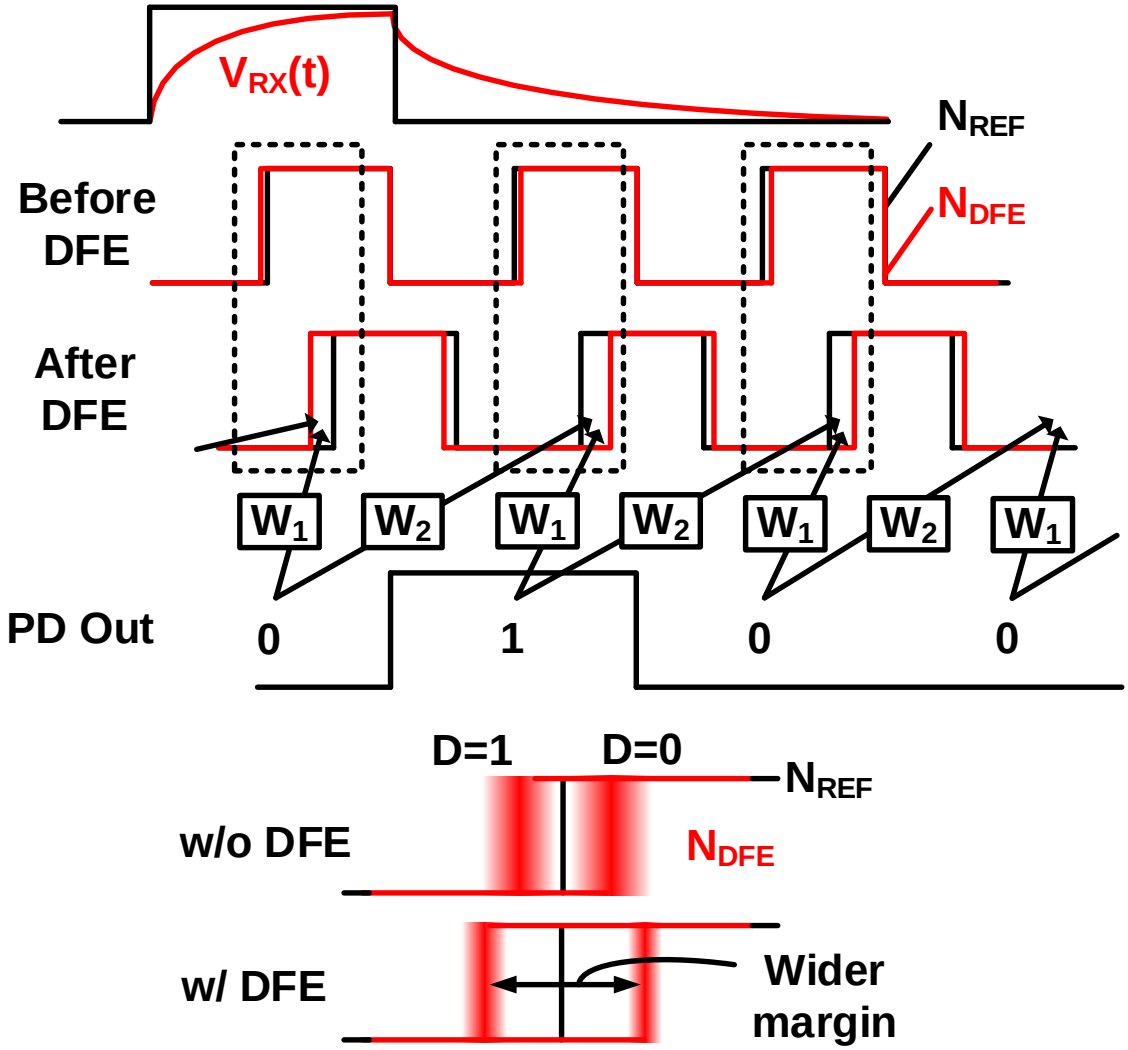
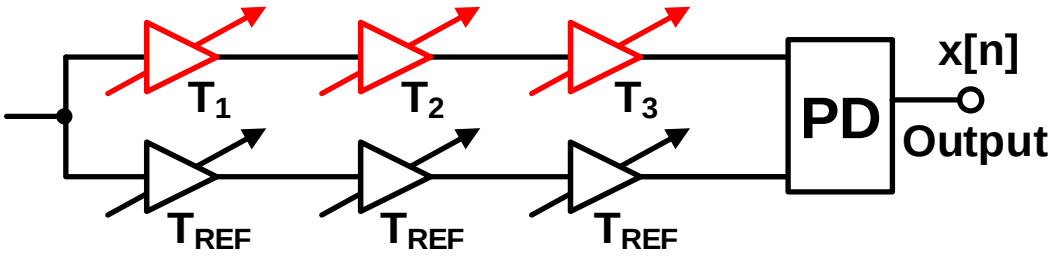
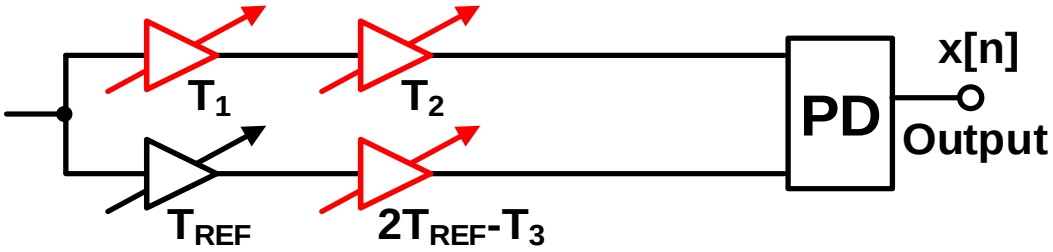


Fig. 2.8: Illustration of TB-DFE for a data pattern of '0100'. Timing margin is enhanced by the TB-DFE circuit.



(a)



(b)

Fig. 2.9: Illustration of delay transformation technique. (a) Standard implementation requires six inverters. (b) The same operation (i.e. sign(T1+T2+T3-3TREF)) can be performed using four inverters by folding inverter delay T3 to the lower path. For DFE implementations with a high number of taps, the total area and energy can be reduced by roughly 50% using this technique.

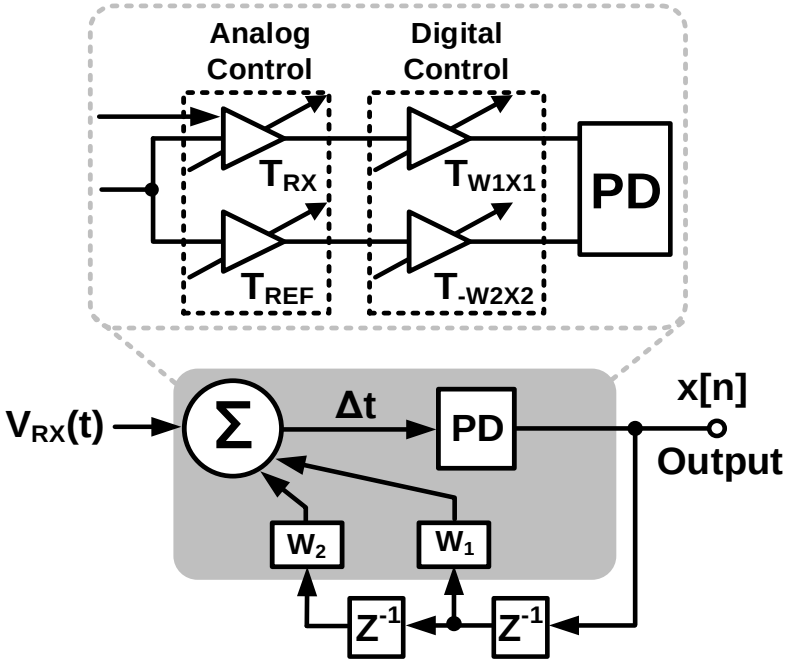


Fig. 2.10: 2-tap TB-DFE after applying the delay transformation technique described in Fig. 2.9.

2.3.2 Delay Transformation Technique

The power consumption and chip area of the TB-DFE can be further reduced by folding half of the DFE delay line to the reference delay line. Fig. 2.9 shows a simplified example of a three stage TB-DFE with the proposed delay transformation technique. Delays T_1, T_2, and T_3 of the upper delay line are controlled by the current input signal, preceding bits, and the DFE weights. Delay of the lower reference delay line is fixed. The PD compares the two delays $T_1+T_2+T_3$ and $3T_{REF}$ to determine the output bit. If we move T_3 to the lower delay line but with a negative polarity and positive delay offset (i.e. $2T_{REF}-T_3$) as shown in Fig. 2.9(b), the phase comparison result remains the same as the original implementation. That is, the same DFE function can be realized with fewer delay stages which translates into a lower power consumption and smaller chip area. For long delay lines, the power and area can be cut down by almost 50% using this technique. An important point to note is that all delay stages including the one denoted by $2T_{REF}-T_3$ can be implemented using the same exact circuit. This is possible is because the delay ranges for T_1, T_2 and $2T_{REF}-T_3$ are the same when the nominal values of T_1, T_2, and T_3 are equal to T_{REF}. This can be explained using the following example. Suppose delays T_1, T_2, and T_3 are all centered around TREF with a programmable delay range of $\pm\Delta T$.

$$\max(T_1, T_2, T_3) = T_{REF} + \Delta T$$
$$\min(T_1, T_2, T_3) = T_{REF} - \Delta T$$

Then the range of $2T_{REF}-T_3$ can be calculated as follows.

$$\begin{aligned}\max(2T_{REF} - T_3) &= 2T_{REF} - \min(T_3) \\ &= 2T_{REF} - (T_{REF} - \Delta T) \\ &= T_{REF} + \Delta T\end{aligned}$$

$$\min(2T_{REF} - T_3) = 2T_{REF} - \max(T_3)$$
$$= 2T_{REF} - (T_{REF} + \Delta T)$$
$$= T_{REF} - \Delta T$$

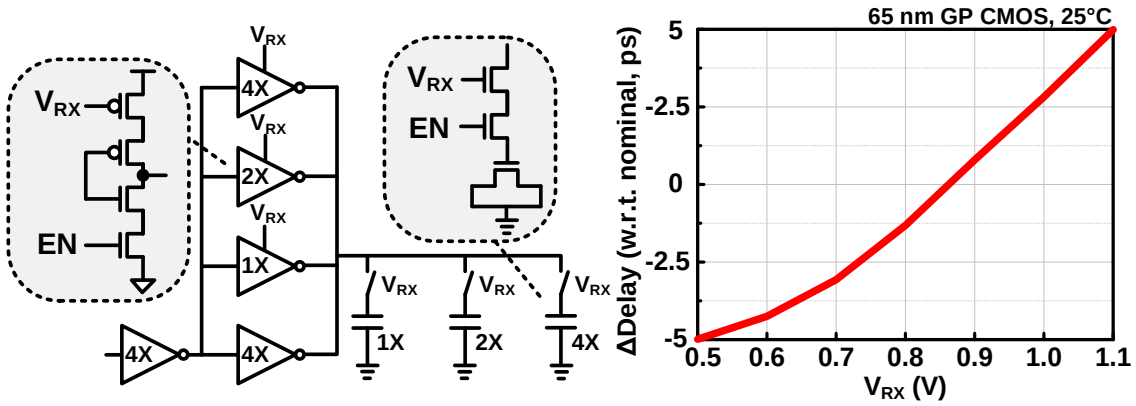
As shown in these simple equations, the new delay stage (i.e. $2T_{REF}$-T_3) has the same delay range as other three delay stages T_1, T_2 and T_3. This allows us to utilize the same circuit for all delay stages which ensures a uniform layout with minimum delay mismatch. The output of the PD circuit is determined by the arrival time difference between the two inputs rather than the absolute delay value of each delay line. So the TB-DFE is inherently tolerant to voltage and temperature drifts or noise affecting both delay lines equally. Another subtle but important point is that with the proposed delay transformation, the number of delay stages required for an N-tap DFE is just N/2. In contrast, an N-tap DFE operation using CML requires N (not N/2) pull-down paths. So, when comparing the results in Fig. 2.4 and Fig. 2.7, we must account for the 2x difference in the number of taps. For instance, an 8 tap delay in Fig. 2.4 corresponds to a 4 tap delay in Fig. 2.7, and so on. This makes TB-DFE even more attractive compared to CML based DFE for large N values.

Implementation of a 2-tap TB-DFE using the proposed delay transformation technique is shown in Fig. 2.10. One of the two digital controlled delay stages is folded into the reference delay path with a complementary weight, which serves as a DFE tap. The first delay stage in each line is an analog controlled delay stage serving as a VTC. The incoming analog signal from the channel is connected to the VTC of the upper delay line. The input voltage to the bottom VTC is hardwired to half VDD. The symmetric configuration between the upper and lower delay lines minimizes layout mismatch and common-mode noise issues.

2.3.3 Analog and Digital Delay Stages

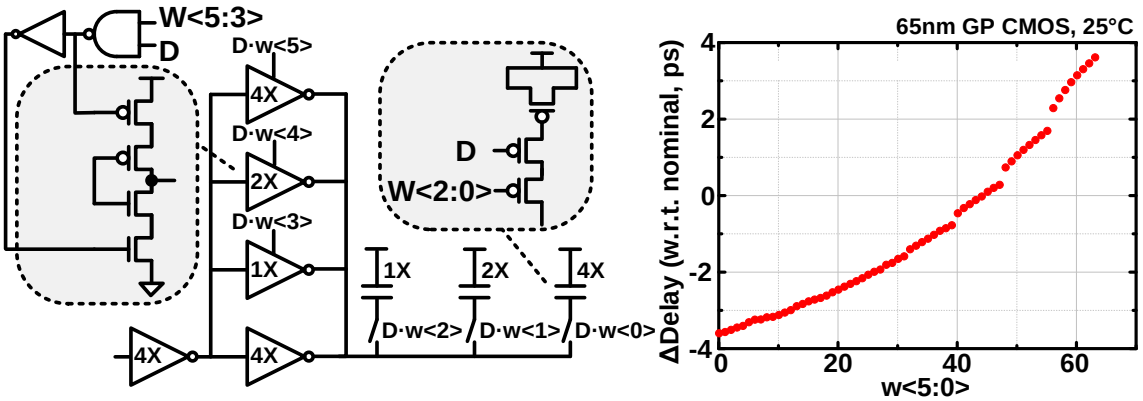
Fig. 2.11(a) shows the detailed implementation of the analog delay control stage which consists of four parallel tri-state inverters (including one always-on inverter) and three MOS capacitors. The control signals of the parallel inverters and capacitors are directly connected to the incoming analog voltage to maximize delay range. Fig. 2.11(b) shows the delay change versus input RX voltage relationship. Non-linearity of the VTC transfer curve will affect the TB-DFE operation since the voltage to delay conversion will be distorted. To get around this issue, we utilized the linear portion of the VTC transfer curve (i.e. from 0.5V to 1.1V) by appropriately sizing the inverter's pull-up and pull-down devices. As shown in Fig. 2.11 (b), the delay range corresponding to this input voltage range is 10ps. Fig. 2.12 (a) shows the detailed implementation of the digital delay control stage for positive delay compensation. The circuit is almost identical to the analog delay stage except that the capacitor is connected to VDD rather than ground for a wider delay range. The delay is controlled by the feedback data D and a 6-bit weight w<5:0>. Signal D determines whether or not the weight is applied to the delay stage. The 6-bit weight determines how many inverters and capacitors are turned on. The implementation of negative delay compensation is verbatim, with the exception of using a complementary digital code. Fig. 2.12 (b) shows the difference between the actual delay and the reference delay versus different configurations. To achieve both positive and negative compensation, the delay of the reference line is set near the average between the D=0 and D=1 delays. With a 6-bit control, we were able to program the weights to their desired values with sufficient accuracy. Hence, non-linearity of the delay curve is not a critical concern for

proper TB-DFE operation.



(a) (b)

Fig. 2.11: (a) Circuit implementation of delay stage with analog control (i.e. VTC stage). (b) Delay change versus RX voltage.



(a) (b)

Fig. 2.12: (a) Circuit implementation of delay stage with 6-bit digital control. (b) Delay change versus weight.

2.4 Circuit Design

Fig. 2.13 shows the overall block diagram of the 10mm on-chip transceiver system we implemented in a 65nm GP process. It contains an on-chip clock generator which can provide a 5GHz differential clock for TX and RX circuits. Channel data is generated by an on-chip PRBS circuit. A 3-tap half-rate FFE was implemented in the TX block to de-emphasize the output signal and transmit the data over a 10 mm by 2μm M9 channel. 2μm is the minimum metal width of M9 metal layer in this technology. An inverter based transimpedance amplifier (TIA) followed by a 2-tap half-rate TB-DFE was designed for the RX block. On-chip monitoring circuits for in-situ bathtub and BER eye-diagram measurements were included. A 2-tap DFE was found to be sufficient for a 10 mm channel for our target frequency. This was also verified by experimental data shown in section V. For on-chip serial link applications, the system clock is available everywhere inside the chip so there is no need for separate clock and data recovery circuits. BER data in section IV captures non-ideal effects such as clock jitter as we have implemented the clock generator inside the test chip.

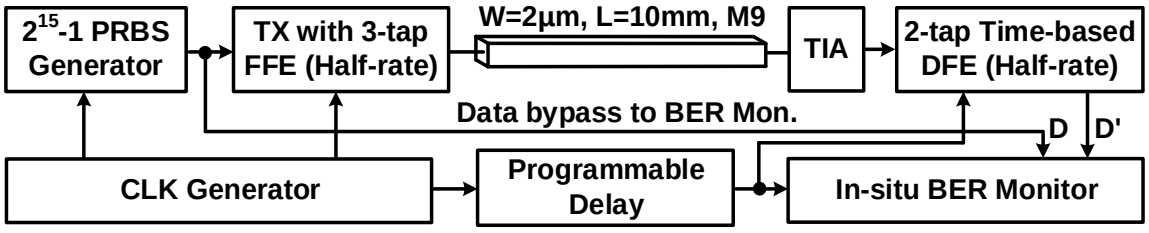


Fig. 2.13: Block diagram of 65nm test chip.

2.4.1 Transmitter

Fig. 2.14 shows the detailed implementation of the 3-tap half-rate FFE. The data stream was generated by two independent PRBS units each operating at 5Gb/s. The two bit streams were fed to two separate data paths. Different PRBS algorithms were implemented to ensure good randomness in the combined 10 Gb/s data. The differential 5 GHz clock samples the two data streams in an alternating manner achieving half-rate operation. Three flip-flops drive the per-cursor, main-cursor, and post-cursor, respectively, to support a 3-tap FFE operation. The multiplexer (MUX) after the third flip-flop stage combines the two data streams into a single 10 Gb/s data stream. A voltage mode output driver operating at 10 Gb/s is implemented using a bank of inverters and two shared output resistors for TX impedance matching [21]. 4-bit FFE weights determine the de-emphasis level.

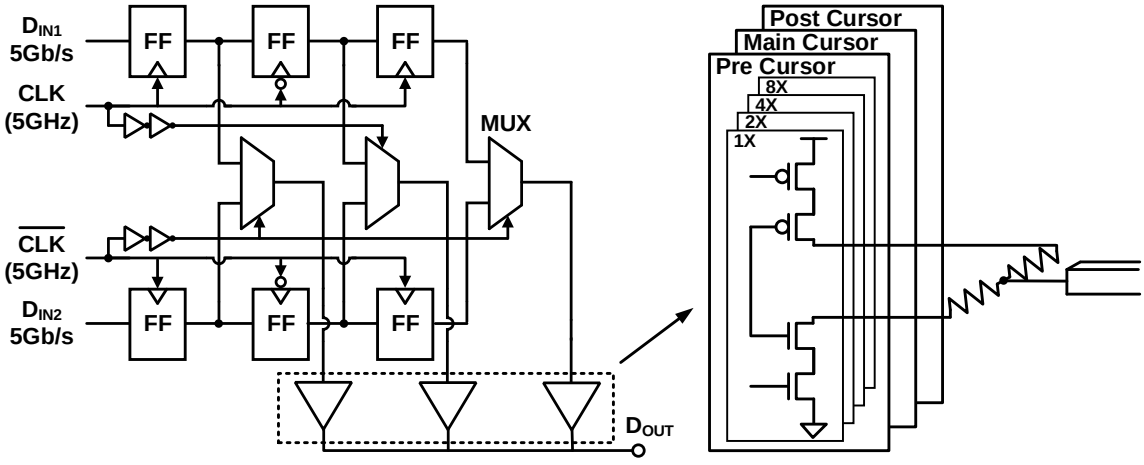


Fig. 2.14: Detailed implementation of 3-tap half rate FFE on transmitter side.

2.4.2 Receiver

Details of the receiver are shown in Fig. 2.15. An inverter based TIA with a 4-bit programmable transmission gate bank ensures good RX impedance matching. The simulated bandwidth of the TIA was 4.2-9.9 GHz depending on the transmission gate configuration. A differential 5 GHz clock drives two parallel DFE paths achieving a combined data rate of 10 Gb/s. After the TIA, the voltage signal is converted to time delay T_{RX} by the VTC. T_{REF} is tunable in our test chip and was fixed to roughly the average of data '1' and '0' delays. The second delay stage is a digital delay stage controlled by the feedback data and the appropriate weights. With the delay transformation technique described in section III. B, the second tap can be moved to the bottom delay line. A third programmable delay stage was added for testing purposes (i.e. eye-diagram measurements). We will discuss time domain eye diagram measurements in section V.

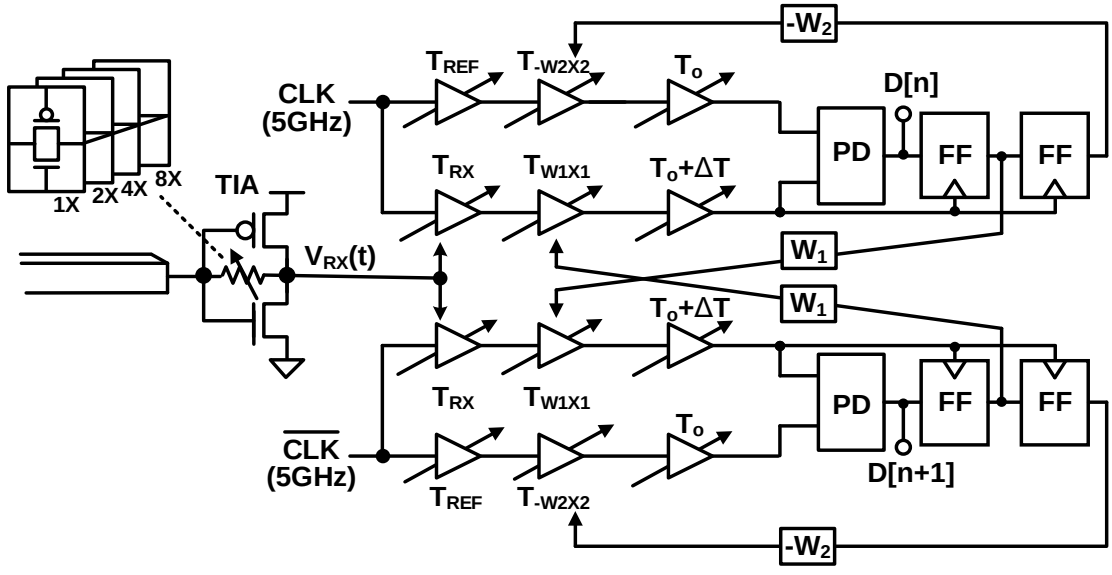


Fig. 2.15: Detailed implementation of receiver block including TIA and 2-tap half rate TB-DFE.

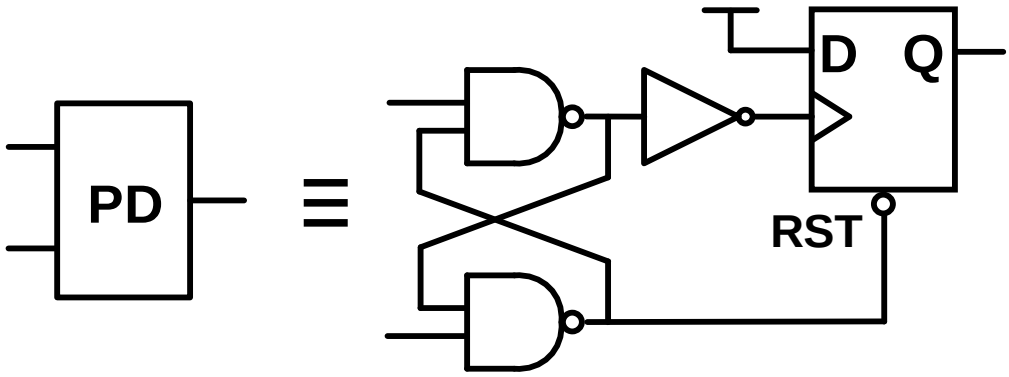


Fig. 2.16: Zero-offset aperture phase detector circuit adopted in this work [22].

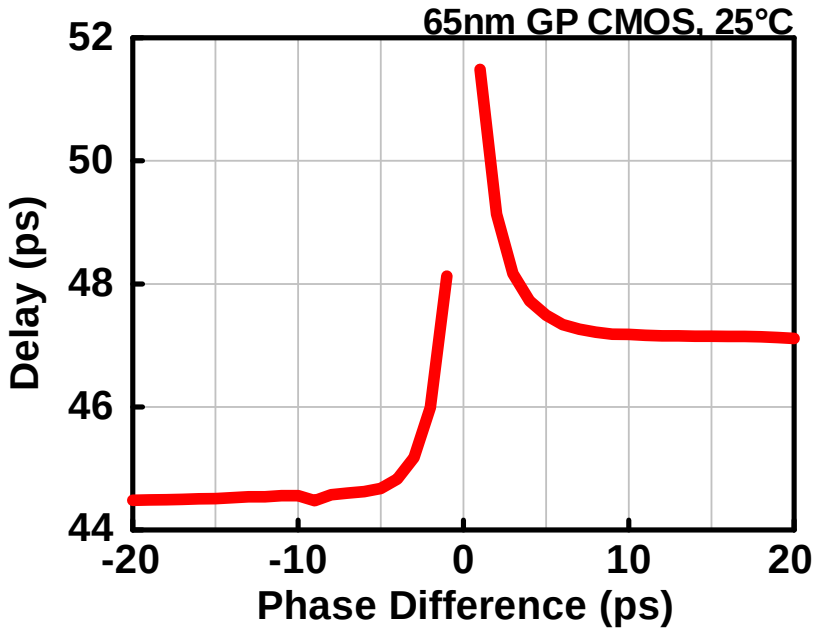


Fig. 2.17: Zero-offset aperture phase detector simulation results.

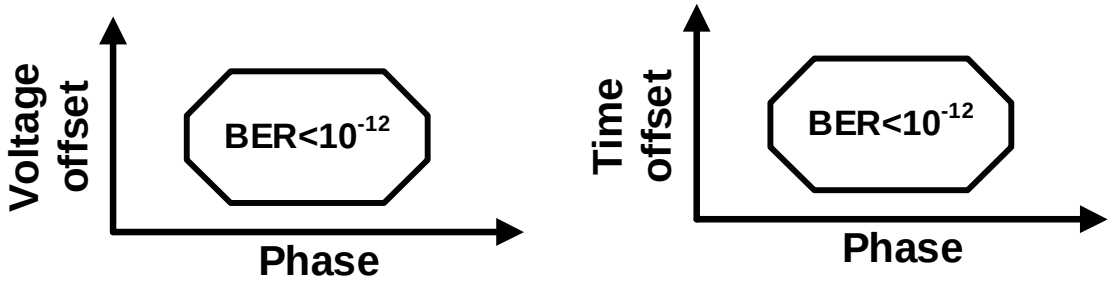
A zero-offset aperture PD shown in Fig. 2.16, composing of a Set-Reset-latch and a flip-flop, was adopted in our design [22]. Simulation results of the zero-offset aperture PD are shown in Fig. 2.17. The x-axis represents the arrival time difference between the two input signals and the y-axis represents the delay between the early input signal and the PD output. When the upper input signal arrives earlier, then the flip-flop will sample a '1', and

vice versa. If the two inputs fall within the aperture time window, then the PD delay increases which can eventually result in a metastable output response. This is not a concern in our design as the input phase difference is sufficiently large compare to the aperture time window.

2.5 In-Situ BER Eye Diagram Measurements

High-speed serial links are traditionally characterized using off-chip equipment such as bit-error-rate-tester (BERT), gigahertz clock generator, and high frequency probes/cables. High-speed serial link measurements can be easily corrupted by any non-ideal connection between the test equipment and I/O pad. Ever-increasing clock frequencies and rising test costs have motivated designers to adopt on-chip BER measurement solutions. This testing approach has several advantages over off-chip equipment based testing such as simpler setup, lower cost, ease of test automation, higher resolution, and reduced noise. This is particularly true for on-chip serial links as they are embedded deeply inside a processor chip with no connection to the outside world. In this work, we designed in-situ BER and eye-diagram measurement circuits as part of the 65nm test chip. Before we discuss the detail implementation of measurement circuit, we first introduce the concept of a “time domain” eye-diagram. Fig. 2.18(a) shows a typical BER eye-diagram for voltage-mode circuits which are obtained by sweeping the sampling time point (x-axis) and the offset voltage (y-axis). Such a voltage-versus-time BER eye-diagram does not apply to our proposed TB-DFE as the voltage is immediately converted to time. So instead, we propose a time domain BER eye-diagram where the y-axis is the delay offset as shown in Fig. 2.18(b). The delay offset was implemented using a separate delay stage

in the delay lines.



(a) (b)

Fig. 2.18: (a) Conventional BER eye diagram is plotted in the voltage-versus-time domain. (b) Time domain BER eye-diagram is plotted in time-versus-time domain.

Fig. 2.19 displays the overall block diagram of the in-situ BER and eye-diagram measurement circuit. The left most box denoted by "Phase Delay" is used to sweep the x-axis. This programmable phase delay allows the clock to sample data over a 2 unit interval (UI) range allowing BER eye measurement across two cycles. The box denoted by "ΔT", which is the third stage in the delay line, is for the delay offset representing the y-axis. Each programmable delay has a 6-bit control. The BER monitor compares the data from the 2^{15}-1 PRBS data D with the DFE output data D' using a 2-input XOR gate. The error signal increments the 11-bit error counter. Finally, the error count is periodically read out for a given x-y configuration and the BER is computed based on the total number of cycles and the error count. By sweeping phase delay and time offset, we can obtain the BER bathtub and BER eye-diagram.

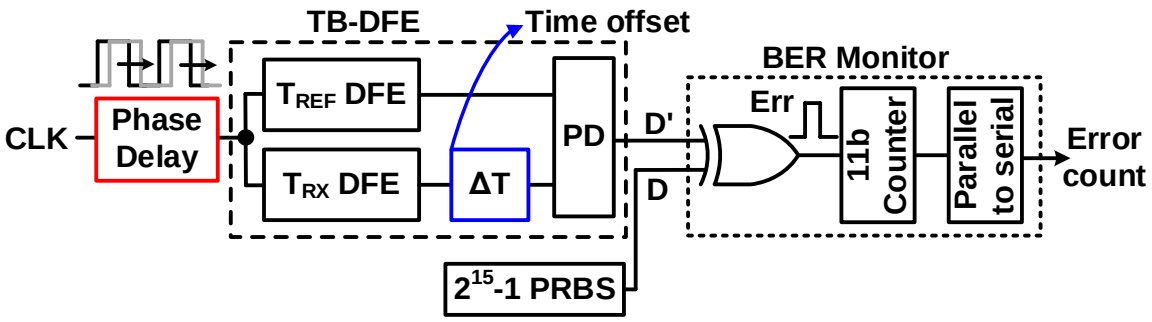


Fig. 2.19: In-situ bathtub and BER eye-diagram measurement circuits.Single-layer digit recognition application for proof-of-concept.

2.6 Measurements Results

In this section, we present the bathtub and time domain BER eye-diagrams measured using the proposed on-chip circuits. Fig. 2.20 shows the BER bathtub while sweeping the phase delay for 1-tap and 2-tap DFE configurations. BER down to 10^{-10} was measured. No noticeable improvement in BER was seen by increasing the DFE length from 1-tap to 2-tap. So, it can be concluded that for the 10mm channel implemented in our test chip and for our target frequency, a 1-tap DFE is enough to remove ISI noise. Fig. 2.21 shows the bathtub curves with and without TB-DFE down to a BER of 10^{-12}. Without the TB-DFE, the lowest BER we could achieve was only 10^{-10}. After applying the TB-DFE, a BER less than 10^{-12} can be achieved while maintaining an eye width of 0.43 UI. Fig. 2.22 shows the time domain BER eye-diagram for two consecutive bits. The time offset can be controlled with 6-bit precision, so 64 codes are shown in the y-axis. To save test time, BER down to 10^{-11} was measured for the eye-diagram. Results show that a BER less than 10^{-11} was achieved for an eye width of 0.5 UI. Fig. 2.23 displays the energy-efficiency and data rate measured at different supply voltages. The purpose of this figure is to verify good low

voltage performance of the TB-DFE. The data point at 1.2V is based on a BER criteria of 10^{-12} while the other data points are for a BER of 10^{-9} due to test time limitations.

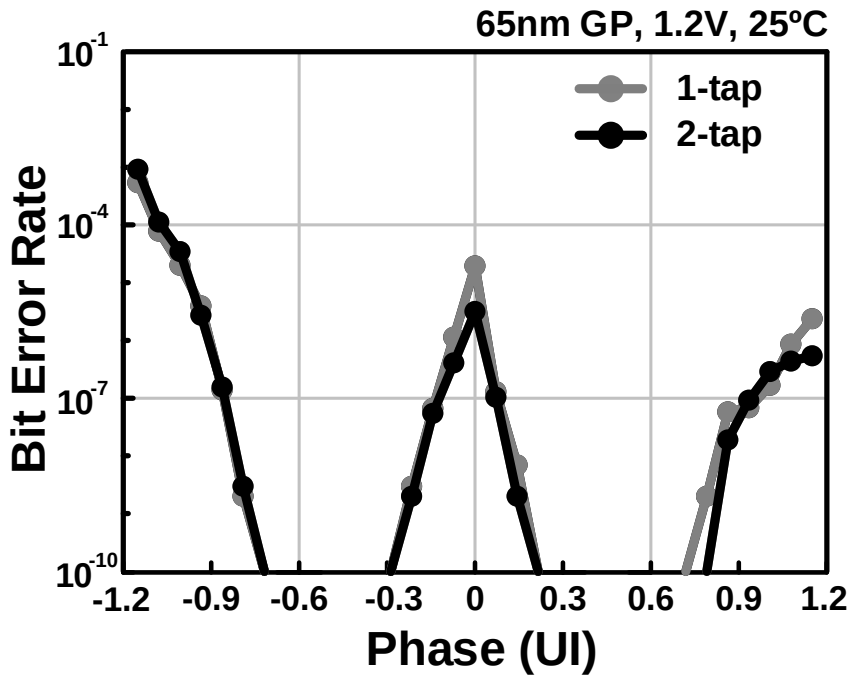


Fig. 2.20: Measured BER bathtub curves (<10^{-10}) for 1-tap and 2-tap DFE. BER is plotted for two consecutive bits. For our target application, a 2-tap DFE offers marginal improvement in BER compared to a 1-tap DFE.

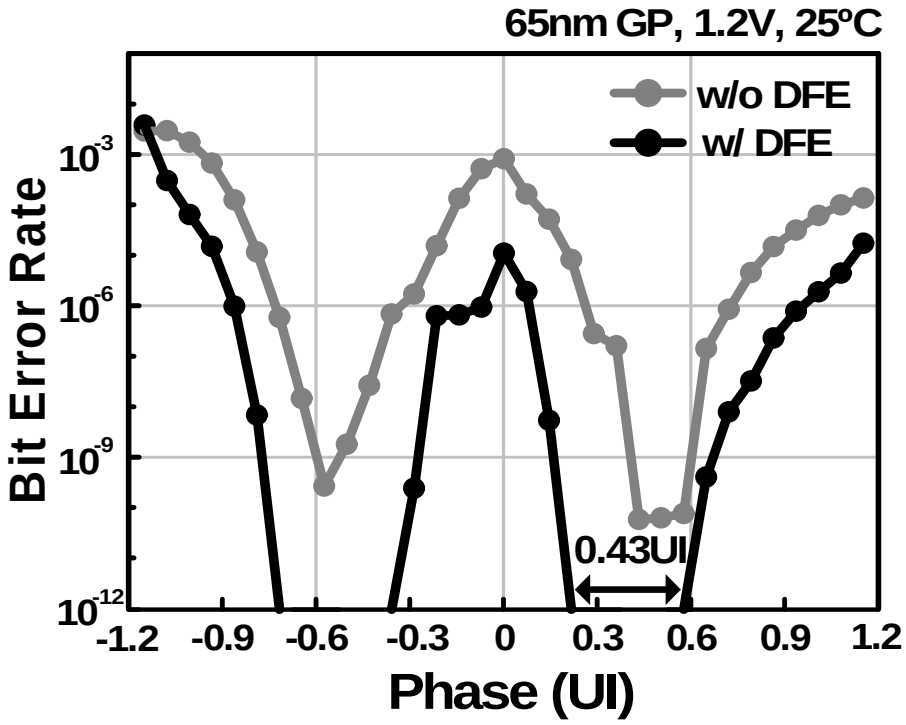


Fig. 2.21: Measured BER bathtub curves (<10^{-12}) with and without TB-DFE for two consecutive bits.

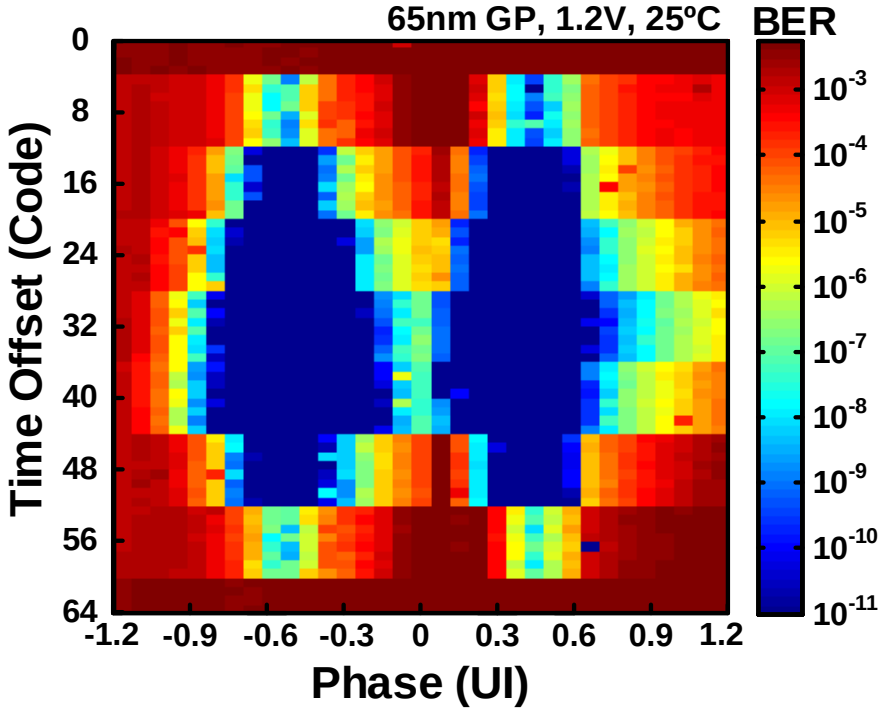


Fig. 2.22: Measured BER eye diagram for two consecutive bits.

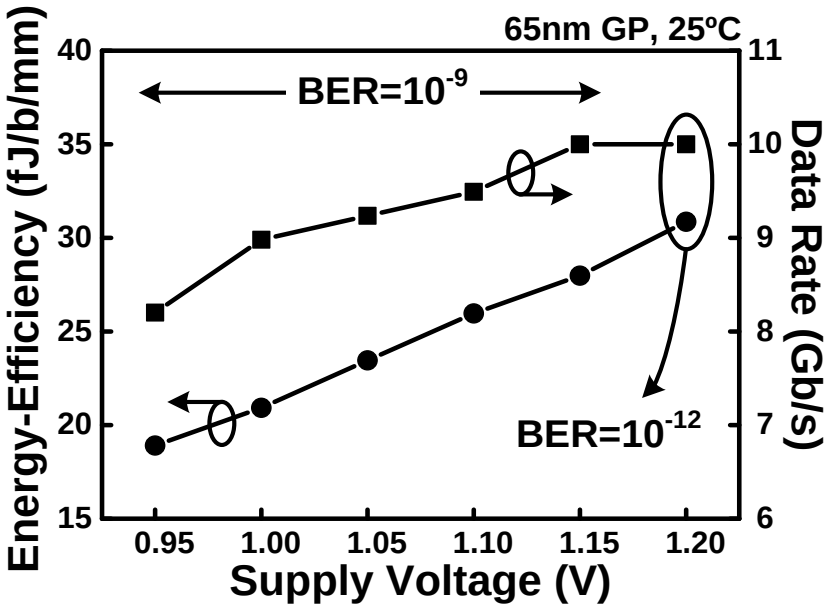
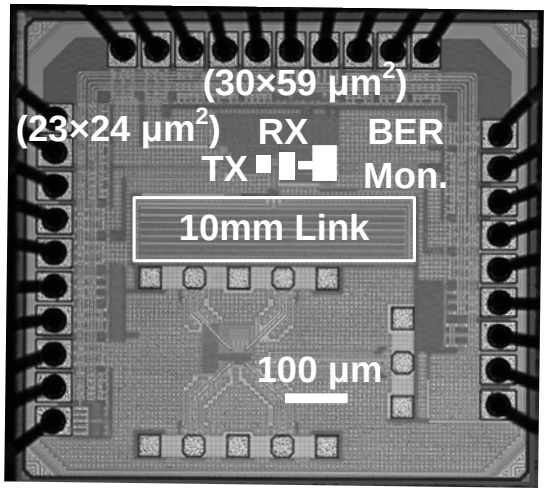


Fig. 2.23: Supply voltage versus data rate and energy-efficiency.

The die photo and summary table are shown inFig. 2.24. The transmitter and receiver blocks occupy a chip area of 23×24μm2 and 30×59μm2, respectively. One thing to note is that the receiver area includes test circuits such as the delay offset stage, which occupies about 1/3 of the receiver circuit area so that the actual circuit area will be significantly smaller. The throughput per channel 2 Gb/s/um for a data rate of 10 Gb/s and a channel length of 10 mm. The energy-efficiency of the transmitter and receiver (not including BER monitor) blocks are 31.9 and 45.3 fJ/b/mm, respectively, at 1.2V, 10 Gb/s. Fig. 2.25 compares the proposed design with other state-of-the-art on-chip links. This work represents the first on-chip serial link with a time-based DFE utilizing digital-intensive circuits.



Technology	65nm GP CMOS
Core Size	TX : 23μm x 24μm
	RX : 30μm x 59μm
VDD	1.2V
Data Rate	10Gb/s
Channel Length	10 mm
BER	$< 10^{-12}$
Throughput	2 Gb/s/μm
Energy Efficiency	TX : 31.9 fJ/b/mm
	RX : 45.3 fJ/b/mm

Fig. 2.24: Die photo and feature summary table.

	ISSCC'09 [14]	ISSCC'10 [15]	ISSCC'12 [16]	ISSCC'13 [17]	VLSI'15 [8]	This work	
Technology	90nm	90nm	65nm	65nm	65nm	65nm	
TX and RX	Charge Injection FFE+TIA	Capacitively driven	Capacitively driven+sense amp.	Current mode transceiver	CTLE-based repeater	Voltage mode driver+TIA	
Features	No DFE	No DFE	No DFE	No DFE	No DFE	2-tap TB-DFE	
Data Rate	4Gb/s	4.9Gb/s	10Gb/s	3Gb/s	4Gb/s	10Gb/s	
Throughput (Gb/s/μm)	2	4.4	2.56	0.75	4	2	
Link Length	10mm	5mm	6mm	10mm	2.5mm+2.5mm	10mm	
BER Bathtub	< 10E-6	< 10E-10	< 10E-12	< 10E-12	< 10E-12	< 10E-12	
BER Eye	Yes (< 10E-6)	No	No	Yes (< 10E-12)	No	Yes (< 10E-11)	
Eye Width	0.5UI* @BER=10E-6	N/A	N/A	0.48UI* @BER=10E-12	0.48UI** @BER=10E-12	0.43UI** @BER=10E-12	
Energy Efficiency (fJ/b/mm)	35.6	68	174	9.5	48.4	TIA	14.4
						DFE	30.9
						FFE	31.9

*Eye width **Bathtub width

Fig. 2.25: Comparison with previous on-chip serial links.

2.7 Conclusions

In this chapter, an inverter-based 2-tap half-rate TB-DFE is demonstrated on a 10 mm on-chip serial link in a 65nm GP process. Our proposed TB-DFE leverages digital-intensive circuits for good scalability, good low voltage operation, low power, compact implementation, short design time, and digital programmability. Higher number of taps can be incorporated without incurring any throughput loss by simply adding more delay stages. This could be particularly beneficial for serial link applications requiring a longer DFE filter. The concept of time domain BER eye-diagram was introduced along with in-situ BER measurement circuits for reduced test effort and improved test accuracy. Circuit performance was verified using in-situ BER measurement circuits. Experimental data from the 65nm test chip shows that the proposed digital-intensive serial link can be a viable option for future on-chip interconnect applications.

Chapter 3. An 8 Gb/s TDC-Based Receiver with Time-Based Front-end for In-Package Serial Link

3.1 Introduction

The ever-increasing bandwidth requirement for chip-to-chip connection has pushed high speed input/output (I/O) circuits up to tens gigabit per second. The total throughput for next-generation memory-to-processor links is targeting at 8 Tb/s [23]. To achieve this data rate, the pin density and date rate per lane should be increased at the same time. While the CMOS scaling can benefit the high speed I/O circuit performance and energy efficiency, the pins count is not growing at the same rate. The physical size of electronic devices also limited the pin count. To solve the problem, emerging packaging technologies such as system-in-package (SiP), 2.5D integration, through-silicon-via based 3D ICs, and silicon interposers were proposed to enable ultra-small form factors [23]-[29]. These packaging technology, as shown in Fig. 3.1 also allows heterogeneous technologies to be integrated into the same chip package [24]. Design consideration of high speed I/O for in-package applications must be more compact, energy-efficient, and digital friendly compared to their chip-to-chip counterparts. In this work, we will focus on low power and

compact size digital intensive I/O design, especially for in-package communication.

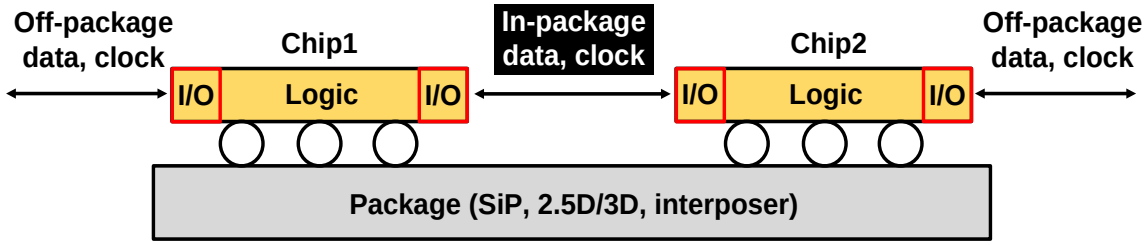


Fig. 3.1: Illustration of system-in-package technology.

Equalization technique has been widely used for serial link communication. The conventional analog front-ends (AFE) usually contain analog-intensive circuits such as continuous linear equalizer (CTLE), variable gain amplifier (VGA), and current-mode-logic (CML) based decision feedback equalizer (DFE). These circuits have proven to be highly effective for high speed off-chip applications. However, they are not suitable for in-package links as they suffer from voltage headroom and process-voltage-temperature (PVT) variation issues, and are typically powered by a separate high power supply. The complicated analog intensive design also makes these topologies less attractive to in-package link. Recently ADC-based receivers have been drawing attention as they can provide more powerful and efficiency equalization scheme in the digital domain by DSP unit [30]-[34]. While ADC-based receivers can operate at a lower voltage than their analog counterparts, and hence take full advantage of technology scaling, they still rely on AFE circuits such as CTLE for high frequency gain peaking to reduce the ADC design challenges. A digital friendly approach such as a time-based DFE has been proposed for the signal equalization [35]. The basic concept of time-based operation transfers the voltage

signal into time delay and utilizing an inverter-based delay line. The equalization is done by different programming delay on each delay cell. The delay information after equalization will be sum up naturally in delay line, and final output data will be read out by phase detector. This approach is implemented only simple delay cell which can significantly reduce the circuit complexity while achieving performance levels comparable to the previous analog approach.

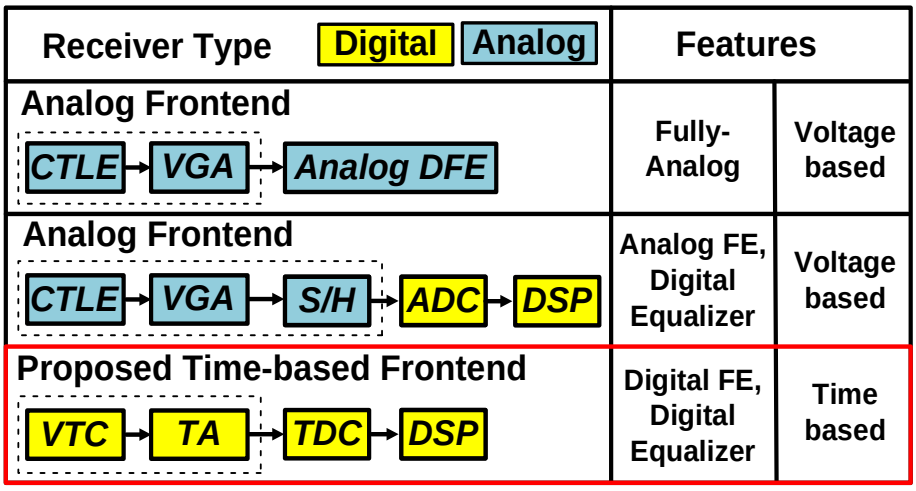


Fig. 3.2: Comparison between the proposed time-based front-end design with conventional RX designs.

To achieve both digital friendly and advanced equalization, we combine the time-based and ADC-based design concepts and present a time-to-digital converter (TDC) based receiver with a digital-intensive time-based front-end (TBFE) [36]. Compare to AFE, the TBFE perform the signal amplification totally in time delay by inverter. In AFE, analog amplification is done by CTLE and VGA. While in TBFE, analog amplification is perform in voltage-to-time converter (VTC) and delay line based time amplifier (TA). The VTC

converts the channel signal to a time delay. A Vernier-line based TDC is added to converts the amplified delay difference to a 4 bit digital code for digital equalization. Fig. 3.2 shows the comparison of different receiver approach and our proposed time-based receiver. Compare to the previous solution, the proposed architecture is based on digital circuits and is hence resilient to PVT issues. The entire front-end circuit can operate at the same supply voltage as the DSP block, making it suitable for in-package links. Another advantage is that the proposed TBFE obviates the need for a sample and hold (S/H) circuit as the VTC converts the instantaneous voltage seen by the passing signal edge to a corresponding delay.

The remainder of the paper is organized as follows. Chapter 3.2 discusses the design and implementation of TBFE including implementation details of VTC, TA, TDC, and DSP unit. The block diagram of the full transceiver design is described in chapter 3.3. Measurement setups and in-situ bit error rate (BER) monitor are shown in chapter 3.4. Chapter 3.5 presents the 65nm test chip measured results. Conclusions are given in chapter 3.6.

3.2 Time-Based Receiver Design

As shown in Fig. 3.3, time-based receiver has four stages. The first stage is VTC used to convert the voltage signal into time delay. The channel inter-symbol-interference (ISI) will induce the jitter at the clock rising edge. The second stage TA will amplify the delay and fed into the third stage TDC for signal digitalizing. Finally, the ISI will filter out by last stage digital equalization and output the recover data. Each block will introduce in the following.

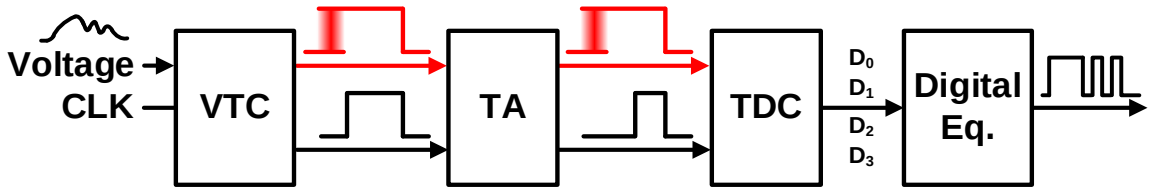


Fig. 3.3 Operating principle of the time-based receiver.

3.2.1 Voltage to Time Converter

The circuit implementation and operation of the VTC is shown in Fig. 3.4 [35]. The VTC has two input signal, input voltage signal and clock. The voltage signal will modulate the clock delay with its corresponding amplitude and generate two different phase output clock. The VTC is composed of an always-on inverter connected in parallel with a programmable tri-state inverter. The channel signal is connected to the PMOS of tri-state inverter to change the pull up strength and produce the corresponding time delay. The clock will enter two identical VTCs, generating the reference and RX clock signals. The delay difference between the VTC circuits is determined by the channel voltage V_{RX} and the reference voltage V_{REF}. For example, A low channel voltage (=data '0') induces a larger delay difference, and vice versa. The reference delay path is fixed to the longest delay to ensure it is always slower than the RX path delay for TDC operation. ISI noise distorts the delay of the RX clock path which will filtered out later by digital equalization.

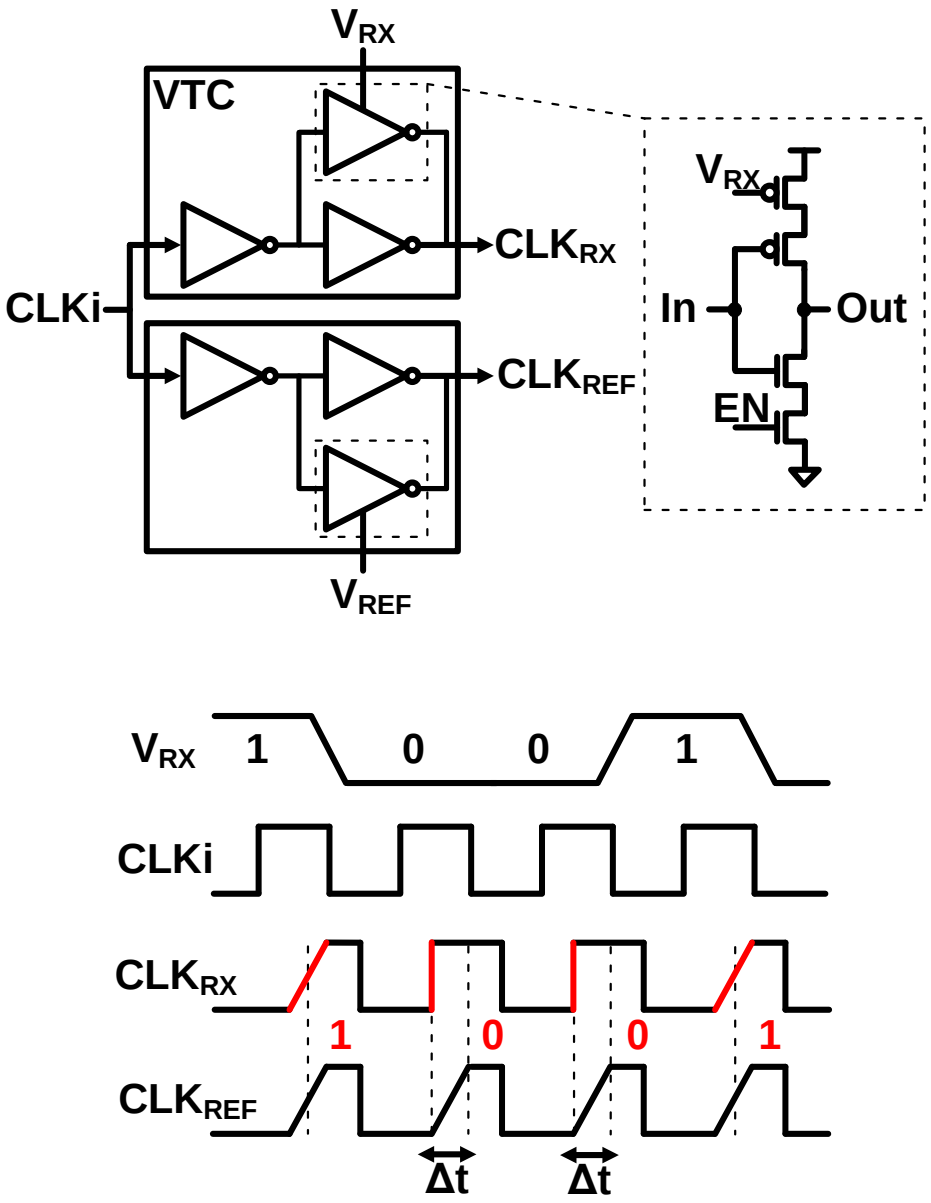


Fig. 3.4 Voltage to time converter (VTC) circuit implementation and timing diagram for a data pattern of '1001'.

3.2.2 Proposed Delay Line Based Time Amplifier

TA has been used in many mixed-mode circuits like all-digital phase lock loop (ADPLL), analog-to-digital converter (ADC), and TDC. Three types of TA have been proposed and compared in [37]. The first two are SR-latch and discharging time control TA. Both two configurations can achieve high gain. However, the linearity is very sensitive due to metastability mechanism, which requires extra gain calibration circuits. The third one is based on a ring oscillator (ROSC) configuration as shown in Fig. 3.5. It consists of two identical NAND gate based switched ring oscillator. Each one with 1X and NX unit connected in parallel. The timing diagram is shown in Fig. 3.6. The ROSC will be trigger by incoming signal. In the beginning, the ROSC is driving by (N+1)X parallel NAND gate and operating at max oscillation frequency, equivalent to min clock period. The ROSC phase different is same as delay different of coming signal. The EN signal will disable the NX unit NAND gate and reduce the ROSC frequency which is equivalent increase the clock period by N+1. The time difference is then N+1 times longer. This structure shows good linearity and high gain stability for wide range operation. However, the speed is limited by ROSC operation frequency, which is not suitable for high speed design. Furthermore, a NAND gate based implementation was required to ensure circuit oscillation.

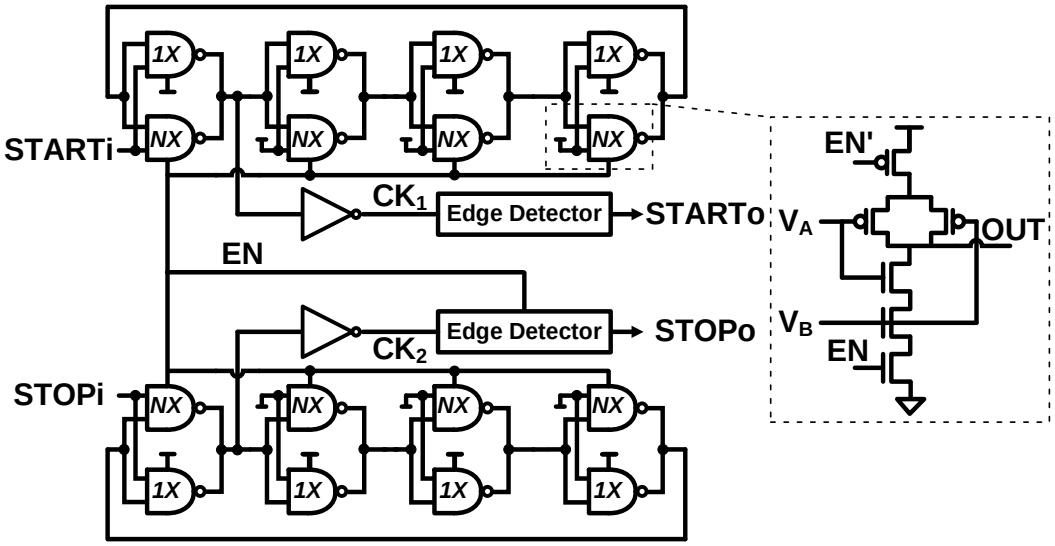


Fig. 3.5: Schematic of ROSC based time amplifier (TA) with close-loop configuration

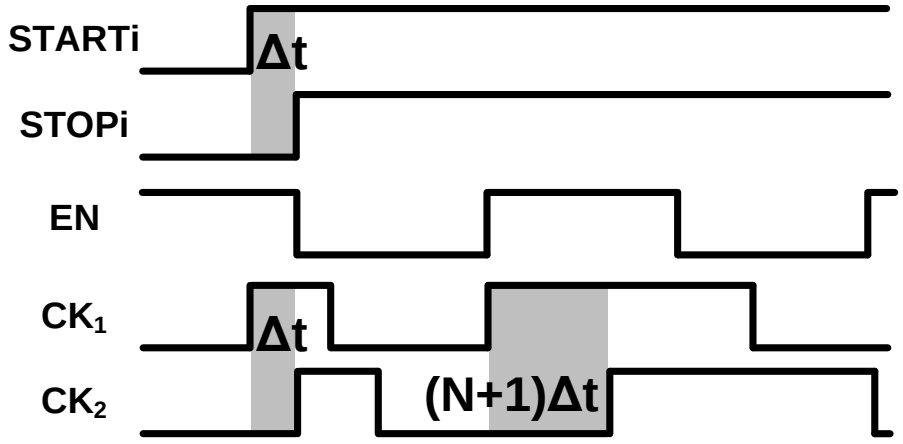


Fig. 3.6: Timing diagram of ROSC based time amplifier.

To increase the TA operating speed, in this work, we employed an open-loop delay line configuration utilizing tri-state inverters rather than NAND gates, as shown in Fig. 3.7. The proposed open-loop TA circuit consists of two identical tri-state inverter-based delay lines. Each stage is driven by two parallel tri-state inverters with 1X and NX sizing,

respectively. The operation principle of the proposed TA is shown in Fig. 3.8. Initially (i.e. STARTi=0, STOPi=0), the enable signal EN is high which activates all the NX tri-state inverters. Since a total of (N+1)X tri-state inverters are driving the output, the rising edge of STARTi experiences a short propagation delay. Once the STARTi signal arrives, EN is set to low after a fixed delay T_d upon which the parallel NX tri-state inverters are disabled. The delay line is now driven only by the 1X tri-state inverters. The EN signal is asserted after a fixed delay, so a longer propagation delay will be seen by the STOPi signal. Since the STARTi edge travels faster than the STOPi edge, an (N+1) times longer delay difference appears at the end of the delay line. The relationship of amplification can be expressed in mathematical formula as follow. Suppose when delay line turn on both of NX and 1X, the signal can travel in the speed of (N+1)S. And if delay line only turns on 1X inverter, the signal can only travel in speed of 1S. We assume the T_d is the number larger than Δt, which can be expressed as $\Delta t+\Delta t_d=T_d$. Before the EN turn off the NX inverter, STARTi will travel for the distance of $(N+1)\cdot T_d$ while STOPi will travel for $(N+1)\cdot \Delta t_d$. After EN turn off the NX inverter, both STARTi and STOPi will travel at the same speed hence the propagate the distance. So the distance different is $(N+1)\cdot T_d-(N+1)\cdot \Delta t_d=(N+1)\cdot \Delta t$. As the result, the delay has been amplified by (N+1) times.

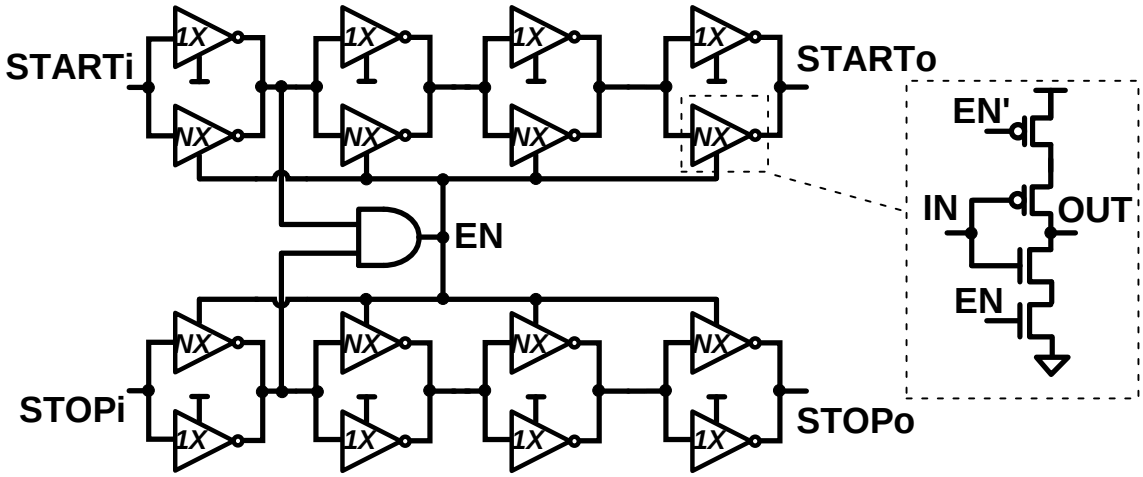


Fig. 3.7: Schematic of delay line based time amplifier (TA) with open-loop configuration.

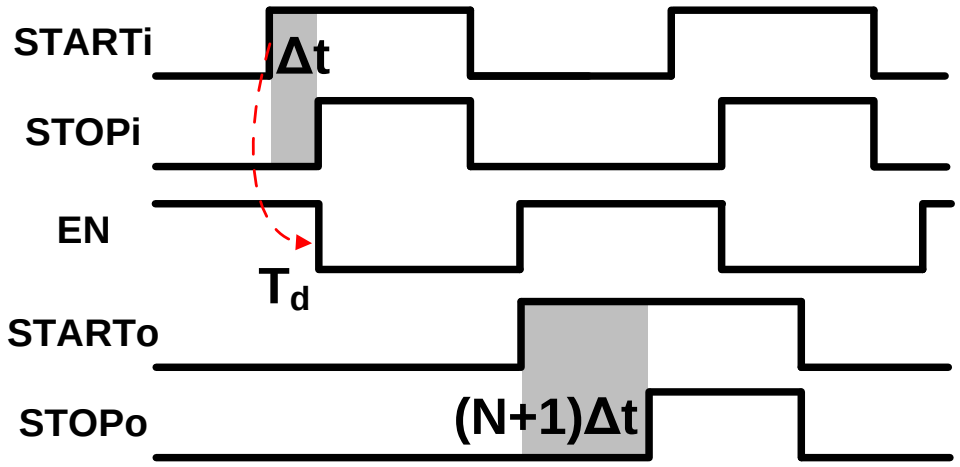


Fig. 3.8: Timing diagram of the proposed TA.

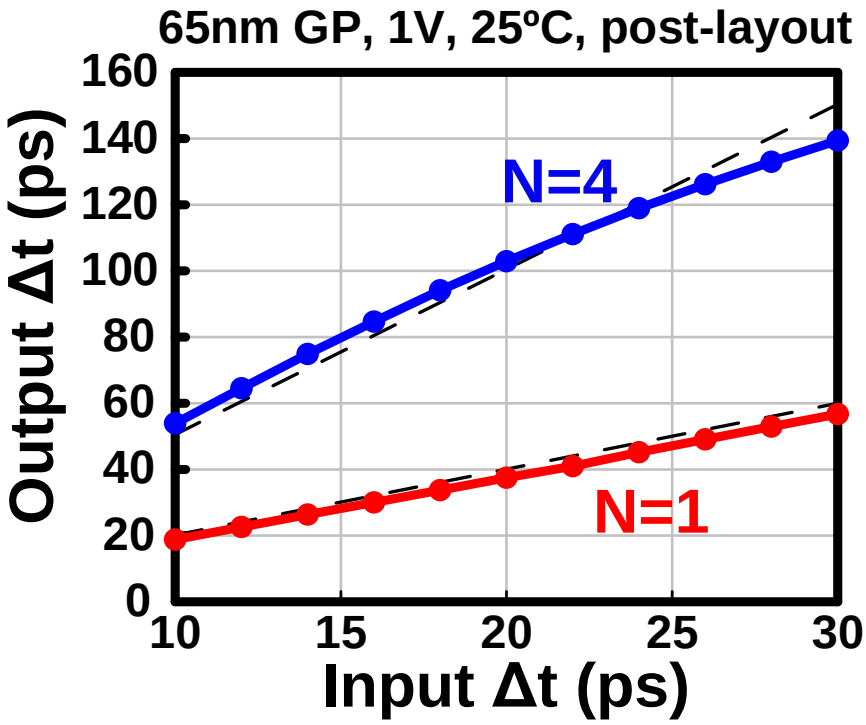


Fig. 3.9: Post layout gain simulation results for N=1 and 4 (Gain=2 and 5).

The function of TA in TBFE is the same as the voltage amplifier in conventional AFE, so the linearity is a vital performance to avoid signal distortion. For good linearity, few points need to be carefully designed. First, to maintain a constant gain of (N+1), the fixed delay of EN signal T_d should larger than the input delay difference Δt. From previous equation, if the fixed delay T_d is shorter than the Δt, the distance different after amplification is only $(N+1)\cdot T_d$ which is smaller than $(N+1)\cdot\Delta t$ and hence reduce the gain ratio. Second, the delay line stages should be large enough that both STARTi and STOPi can simultaneously propagate in the delay line. It means the total delay of delay line should larger than input dynamic range Δt. Third, since the EN signal needs to drive number of delay line stages multiply by 2NX loading. The EN signal fan-out should be large enough.

Otherwise, EN signal can not turn off the NX inverter sharply which will affect the produced delay and hence affect the gain ratio. However, too large fan-out will reduce energy efficiency. The last one is data dependent noise where EN signal might turn off the NX inverter at any time of clock rising. Different shutdown time will affect the total delay and lead to a small discrepancy of amplifying delay. This one performs as and data dependent noise in time domain. Each factor is related to one; for example, if T_d is large, since $T_d > \Delta t$, the number of the stage of delay line should be increased. As the result, EN signal fan-out should also be increased which degrades energy efficiency.

In our implementation, the VTC will generate delay difference about 25ps. The four stages delay line is enough to cover the input dynamic range. The sizing ratio has two options N=1 and 4 in this design. Under this condition, EN signal needs to drive the fan-out of 32X, so EN signal is designed to be 8X for fan-out of 4. The reason for N=4 relates to TDC design parameter. We will discuss this part in next section. Post-layout simulation results of the proposed TA with size N=1 (red line) and 4 (blue line) in Fig. 3.9 shows highly linearity between the input delay and output delay. The black dash represents the ideal case. The N=1 is well matched to the (N+1) gain ratio. However, N=4 has small discrepancy. The reason might be the high loading of 4X device size of the delay line and the data dependent signal which will randomly turn off the NX inverter. One thing worth to mention is that the proposed TBFE, VTC, and delay line based TA is inverter-based implementation, which can reduce the circuit complexity while canceling out voltage and temperature-induced delay shifts in the delay lines.

3.2.3 Time to Digital Converter

After the TA, the amplified delay difference will be converted to 4 bit digital code by TDC for digital processing. The Vernier-line based TDC is adopted in our design. Since the TDC should convert the delay information into digital code in one unit interval, hence the TDC resolution is direct trade of data rate. To reduce the circuit complexity while ensuring an 8 Gb/s data rate, the quarter rate operation and 4 bit resolution i chosen which provided a good balance between operation speed and resolution. Under this condition, TDC needs to convert the data in 500ps. The implementation of Vernier-line based TDC is shown in Fig. 3.10, which consists of four cascaded delay units with each unit having four delay buffers and four arbiters, total of 16 delay stages and arbiters. Each stage's delay is designed to around 20 ps, which ensures TDC can finish the data conversion in one unit interval. A 16 bit thermometer code generated by the Vernier-line is converted to a 4 bit binary code using a thermometer-to-binary (T2B) decoder.

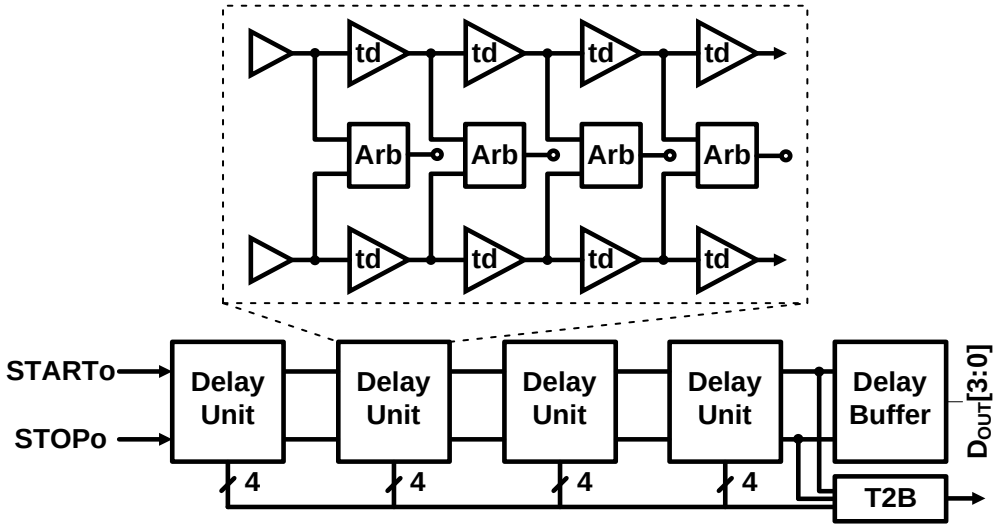


Fig. 3.10: Implementation of 4-bit Vernier-line based TDC.

3.2.4 Digital Equalization

The 4-bit output digital code from the TDC will be fed into the DSP for digital equalization. The digital equalization can adopt both FFE and DFE [38]. In this work, the digital equalization is implemented in 4-tap loop unroll DFE as shown in Fig. 3.11. The digital equalization consists of one 16:1 digital MUX and sixteen 4-bit digital comparators. A bank of 4-bit digital comparators in the DSP compares the new TDC output with predetermined weights w0000, w0001, etc. The correct result from the comparator is selected based on the previous decision results D1-D4. A 16:1 digital MUX outputs the final RX data to the BER monitor circuits.

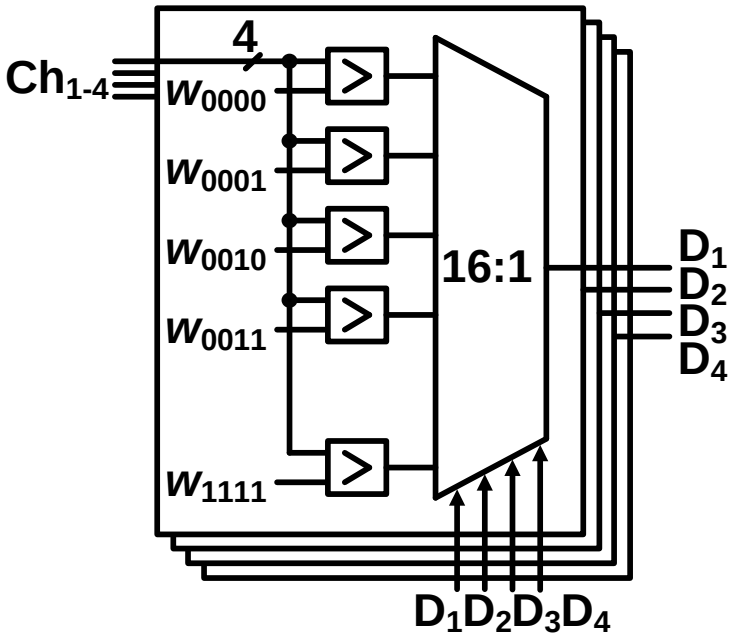


Fig. 3.11: DSP for digital equalization.

3.3 Time-Based Transceiver Implementation

The block diagram of the proposed transceiver system, including a 2^{15}-1 pseudo random bit generator (PRBS), a voltage mode transmitter, a 1/4 rate time-based receiver, and an in-situ BER monitoring circuit, is shown in Fig. 3.12. Since all the links are connected in the small package, we did not add any termination to minimize the package size and adopt the source synchronize architecture in the transceiver. The single-ended data will be transmitted via 7mm in-package link. The transmitter is half-rate operation; the 4 GHz clock is used to generate the random bit data stream and data sampling for FFE operation. This 4 GHz clock will also transmit to receiver for source synchronize. On the receiver side, 4 GHz clock need to divide to 2 GHz and generate four phase clock for time-based receiver quarter rate operation. To four phase 2 GHz clock, divider and single-to-differential (S-D) converter are added on the receiver side clock path. The programmable delay is included for measurements purpose. A PRBS, implemented by shift register, is used to generate a random bit stream while the in-situ BER monitor circuit was implemented to obtain the bathtub curves and time domain eye-diagrams. The measurement part will introduce in next section. The transmitter is based on a 3-tap half-rate FFE with an inverter-based driver. The design details of transmitter can refer to [35]. The receiver contains four lanes of TBFE+TDC circuits, followed by a DSP for digital equalization. Each lane operates at 2 Gb/s.

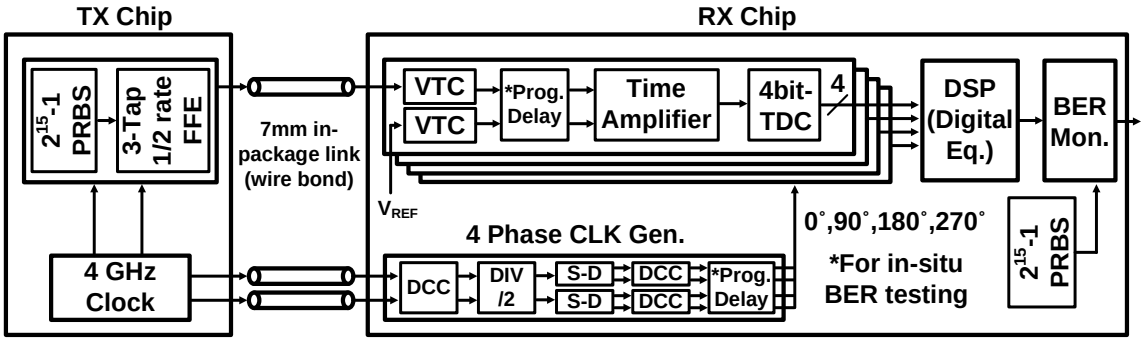


Fig. 3.12: Block diagram of the proposed digital-intensive time-based transceiver.

3.4 Measurement Setup

To verify the performance of the proposed transceiver for SiP application, two dies were integrated into a single package to mimic the link behavior of an SiP system as shown in Fig. 3.13. An SiP prototype containing both TX and RX circuits. A single-ended data signal and a differential clock signal are sent from the TX chip to the RX chip. The 7mm is the longest distance we can achieve in the QFN-100 package.

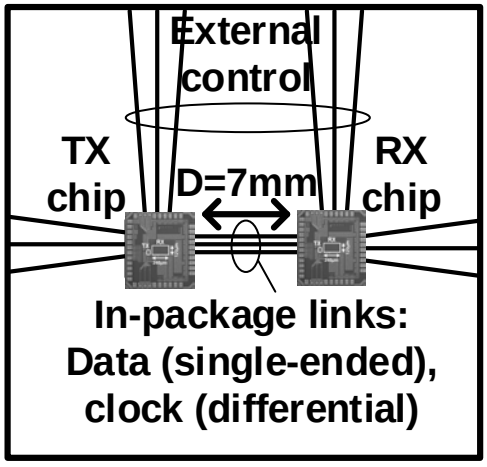


Fig. 3.13: Test package with TX and RX chips for in-package link demo.

The on-chip time-domain BER monitor is included to measure the BER, as shown in Fig. 3.14. Two programmable delay was implemented to check the bathtub and eye-diagram. One is used as phase delay in the red box to sweep the clock phase for data sampling up to one unit interval (UI). By sweeping the phase delay, we can get the bathtub. VTC will generate the delay depend on different clocking phase and add with another delay. This extra delay represents as delay offset shown in blue box, which is corresponding to voltage offset in voltage-based receiver. To get the time-domain BER eye-diagram, we swept the two programmable delays at the same time, corresponding to the x and y axis. The total delay will go through TA and digital equalization to generate the output data. The output data from RX will compare with the original data in BER monitor. To have the correct data pattern in RX chip, we implemented the PRBS, identical to the one in the TX chip, and clocked using a delayed clock from TX chip to generate the ground-truth data. The output from RX will compare with the ground-truth data by XOR gate. An 11 bit BER counter increments whenever an error is detected. The error count is serially read out using a scan chain circuits. The data should read out in certain amount of period to avoid counter overflow. With the on-chip monitor, we don’t need the high cost equipment to measure the bathtub and eye diagram.

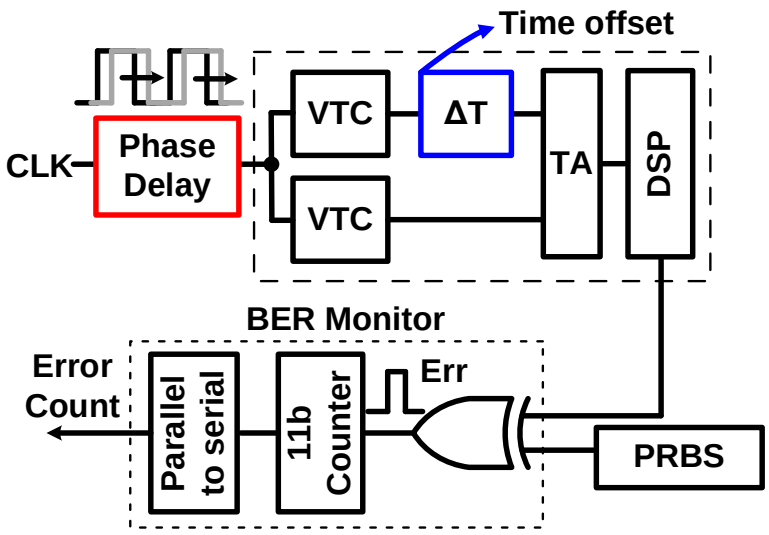


Fig. 3.14: In-situ bathtub and BER eye diagram measurement circuits.

3.5 Measurement Results

Using the above mentioned setup. We first sweep the phase delay in the red box to measure the bathtub with and without equalization, as shown in Fig. 3.15. Without the equalization, the BER can almost achieve 10^{-12}. The reason might due to the short in-package link. After applying the equalization, the results improve and show the timing margin of 0.12 UI for a BER criterion of 10^{-12} for a 7mm communication distance. By sweeping both delay in red and blue box, we got the time-domain eye-diagram, as shown in Fig. 3.16. To save the measurement time, BER down to 10^{-11} is reported in BER eye-diagram. Lower BER values such as 10^{-12} or 10^{-13} can be measured using the same setup. Fig. 3.17 shows the die photo performance summary. Fig. 3.18 shows the comparison with previous link designs. When operating at a data rate of 8 Gb/s, the proposed system achieves an energy-efficiency of 2.1 pJ/b (including TX, RX, and DSP power) at 1V. The

circuit areas of the time-based receiver (including TBFE, TDC) and DSP are 0.0192mm^2 and 0.0096mm^2, respectively

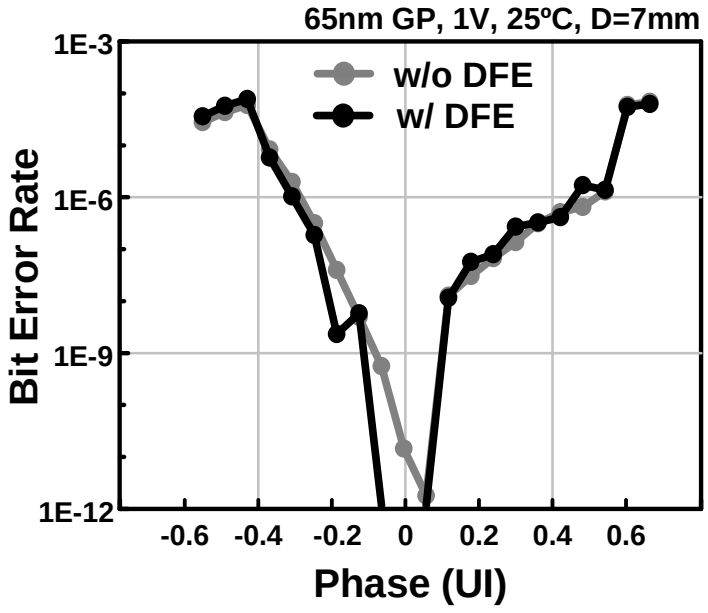


Fig. 3.15: Measured BER bathtub.

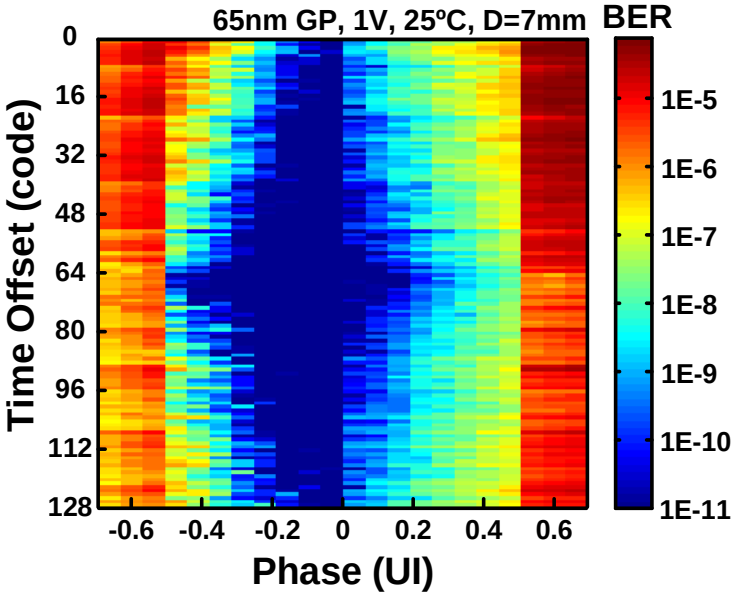
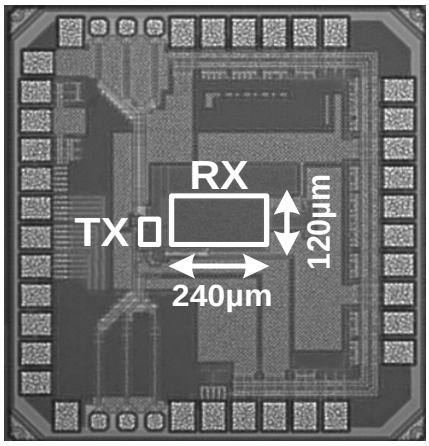


Fig. 3.16: Measured BER eye-diagram.



Technology	65nm GP CMOS
RX Size	240µm x 120µm
VDD	1V
Data Rate	8 Gb/s
Link Length	7 mm
BER	$< 10^{-12}$
Architecture	TBFE+TDC
Resolution	4 bit
Energy Efficiency	2.1 pJ/b

Fig. 3.17: Die photo and feature summary table.

	JSSC'12 [8]	JSSC'13 [9]	JSSC'14 [10]	JSSC'15 [11]	JSSC'16 [12]	This work
Application	Off Chip	Off Chip	Off Chip	Off Chip	Off Chip	SiP
RX Architecture	4x Flash ADC	4x Flash ADC	64x SAR ADC	4x Flash ADC	32x SAR ADC	4x TDC
Front-end Type	Voltage-Based (CTLE +VGA)	Voltage-Based (VGA)	Voltage-Based (T/H)	Voltage-Based (VGA)	Voltage-Based (Analog FFE)	Time-Based (VTC+TA)
Data Rate	10 Gb/s	10.3125 Gb/s	10 Gb/s	8.5-11.5 Gb/s	10 Gb/s	8 Gb/s
Technology	65nm	40nm	65nm	40nm	65nm	65nm
Voltage	1.1V	0.9V	1.1/0.9V	1V	1V	1V
Resolution	4 bit	6 bit	6 bit	6 bit	6 bit	4 bit
BER	<1E-9	<1E-12	<1E-9	<1E-12	<1E-10	<1E-12
RX Area (w/o DSP)	0.288 mm^2	0.27 mm^2	0.52 mm^2	0.82 mm^2	0.38 mm^2	0.0192 mm^2
Power Efficiency (pJ/b)	8.1 (RX only)	15.1 (RX only)	7.9 (RX only)	18.9 (RX, includes Clock)	7.9 (RX only)	2.1 (TX+RX, includes DSP power)

Fig. 3.18: Comparison with previous on-chip serial links.

3.6 Conclusion

In this work, a TDC based receiver with TBFE is presented on in-package serial link in 65nm GP process. To our best knowledge, this is the first TDC based receiver with TBFE. A highly linear delay line based TA is proposed to amplify the small time difference generated from VTC. The detail implementation and design consideration of delay line based TA are also provided in the paper. A BER less than 10^{-12} is verified using the in-situ measurement circuits. Our proposed TBFE is highly digitalized, low voltage operation, and has good compatibility with post digital circuit. The compact size and high energy efficiency show that the proposed time-based receiver is promising for SiP applications.

Chapter 4. A 32 Gb/s PAM-4 Transceiver for High Speed Memory Interface

4.1 Introduction

Advanced semiconductor technology has enabled the high performance computing application from consumer electronic to cloud storage and big data centers such as smartphones, virtual/augmented reality (AR/VR), and internet of thing (IoT). At the same time, the high quality data had pushed the signal transmission volume increasing ever before and required high aggregate throughput of memory interface [39]. Either increase the pin count or the data rate per pin to push the overall bandwidth to achieve the next generation Tera-Byte application for processor to memory link [23]. Different package technology has been proposed to increase the pin count [36]. The single-ended transmission is another main trend to reduce the pin number compare to the differential signal. In circuit architecture, serial link input/output (I/O) bandwidth is targeting 16 Gb/s in sixth-generation double data rate (GDDR). To meet the ever-growing demands of future memory interfaces, this chapter will focus on single-ended transceivers that can deliver high data rates at reduced supply voltages.

Most of the serial link transceiver in now day is based on the non-return-to-zero (NRZ) modulation scheme where low voltage represents logic ‘0’ and high voltage

represent logic ‘1’. NRZ. This simple modulation scheme is working well in low speed operation where the voltage comparator or slicer can detect the signal threshold and decode the data. However, when data rate is increased to a certain level, high channel loss induced severe inter-symbol-interference (ISI) noise will limit the performance and hence increase the (BER). Even with the help of advanced equalization techniques in circuits design, like continuous time linear equalization (CTLE) and (DFE), can provide acceptable signal integrity, the limitation is arising when the data rate is up to 30 Gb/s or beyond [40]. Also, the circuits design, area, and power consumption are quite challenging on high speed design. To solve the problem of channel induced bandwidth limitation, modulation scheme has been proposed to increase the bandwidth efficiency [41]-[45]. In [41] and [42], duobinary can take advantage of the ISI and provide higher signal amplitude. Nevertheless, the pin efficiency is the same as NRZ. The multi-tone signaling is another option that can split the frequency dependent channel into small segments with higher frequency independent loss property to alleviate the equalization challenge at receiver [43]-[44]. In [44], the self-equalization was proposed to avoid any equalization circuits. However, , complicated RF circuit design technique should be adopted, including up/down frequency conversion mixer. The frequency band should be properly chosen for flat frequency response. Recently, multi-level pulse amplitude modulation, like (PAM-3, PAM-4) [41], [44]-[45], were proposed to increase bandwidth efficiency with the cost of reducing signal-to-noise ratio (SNR). In particular, PAM-4 signaling utilizes four signal levels to send 2 bits per unit interval at the expense of complex TX and RX circuits resulting in higher power consumption and larger chip area. If the application is targeting at muti-reflection

[47] or higher loss which requires more number of DFE taps, the hardware overhead will even worse. While this approach has been gaining popularity for ultra high speed (e.g. >50Gb/s) links [45]-[47], a more compact implementation is needed for memory interface applications. Table 4-1 Summarize the feature of previous mentioned signal modulation scheme. Basically, NRZ, PAM-3 and PAM-4 scheme are tradeoff between data rate and SNR. Duo-binary can achieve higher transmitted signal amplitude in same data rate. The data rate of multi-tone modulation depends on number of frequency bands and type of communication modulation to be adopted. It is not straight forward to compare the SNR in multi-tone with other types of modulation. In general, bandwidth efficiency is relatively higher than other types of scheme if several bands and modulation techniques are incorporated. However, the complicated RF circuit design makes less friendly to technology scaling. To achieve low energy efficiency and high scalability for multiple DFE taps for high speed memory interface, we propose a digital-intensive PAM-4 receiver targeted for memory interfaces utilizing fully time-based circuits for DFE.

TB-DFE has been proposed in [19], [35]. The basic concept of time-based operation is shown in Fig. 4.1. The voltage signal will be converted to time delay by voltage-to-time converter (VTC) and generated two delay, data dependent delay T_{Data} and reference delay T_{REF}. These two delays will go through the delay line, and each delay stage can program to different delays with its corresponding weight. Finally, the phase detector (PD) will detect the total delay at the end of delay chain and output the data. Unlike traditional current mode logic, time-based circuits can be realized using simple inverters and programmable loads, making them ideally suited for low voltage energy-efficient memory interfaces.

Since these two works are NRZ signaling, so the linearity and dynamic range are not addressing in the VTC design. To make PAM-4 suitable for time-based operation, we proposed the DVTC which can enhance the linearity and dynamic range without any hardware overhead [49]. Also, the differential delay line along can provide two times of DFE taps efficiency and immune the common node noise in single-ended operation. Also, we proposed an in-situ channel loss monitor to measure the loss in time domain instead of S-parameter in frequency domain. The chip area and power consumption of the loss measurement circuit are negligible.

Table 4-1: Summarize of modulation scheme and its feature.

Signal Type	Pin Efficiency	CLK Frequency	SNR
NRZ	1X	1X	1X
Duo-Binary	1X	X/2	X/2
Muti-Band	NX	X/N	--
PAM-3	1.5X	X/3	X/2
PAM-4	2X	X/2	X/3

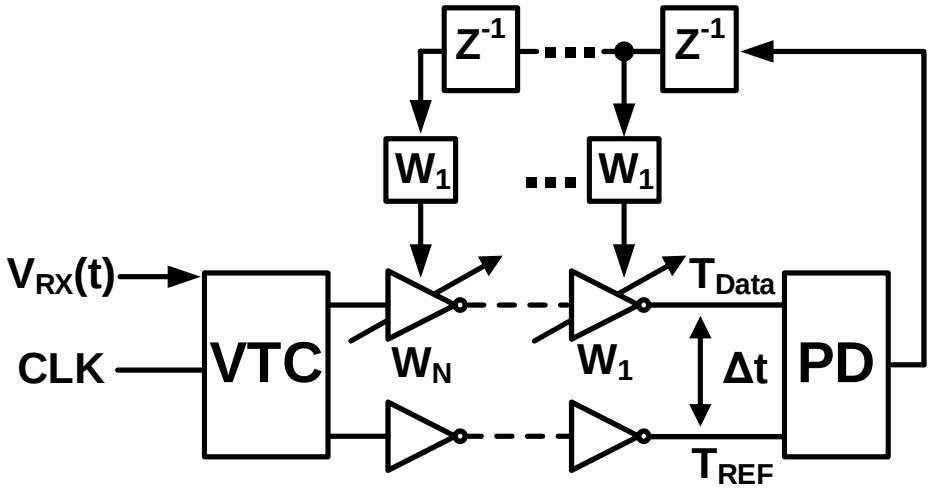


Fig. 4.1: Architecture of TB-DFE.

The remainder of this paper is organized as follows. Chapter 4.2 describes PAM-4 in time-based. The proposed DVTC is described in chapter 4.3. We compare the performance between DVTC and prior art VTC. Implementation details of single-ended PAM-4 transceiver with a 2-tap TB-DFE are given in chapter 4.4. Chapter 4.5 provides details of the in-situ channel loss monitor. Measurement results are discussed in chapter 4.6. Finally, conclusions are drawn in chapter 7.

4.2 Time-Based PAM-4 Signal

Two-level amplitude modulation (PAM-2, NRZ) is the most common use architecture in wireline communication system as they are relatively simple to design. As shown in Fig. 4.2(a), two-level V_1 and V_0 are used to represent the logic '1' and '0', and the threshold voltage is $V_{TH,M}$. The voltage comparator can used to detect the signal to determine the data. In NRZ time-based operation, the (VTC) need to be adopted to convert the voltage amplitude to time delay. The two amplitude signal is mapping into two different time delay information T_1 and T_2. The PD can use to detect the early edge T_1 or late edge T_2 and

determine the data one or zero. In time domain, threshold delay $T_{TH,M}$ is set in the middle of T_1 and T_2. In both cases, since voltage comparator and PD can inherently determine the threshold level, the DFE operation only needs one voltage comparator for voltage-based and one PD for time-based. To overcome the bandwidth limitation and increase bandwidth efficiency, the four-level modulation has been proposed and shown in Fig. 4.2(b). The PAM-4 can transmit two symbols in one unit interval (UI) by representing the data in four different voltage amplitudes shown as V_{11}, V_{10}, $V_{01,}$ and V_{00}. Due to four-level amplitude, PAM-4 requires three voltage comparator to detect three threshold $V_{TH,H}$, $V_{TH,M}$ and $V_{TH,L}$ plus a decoder to determine the data. The three different thresholds are usually implemented by digital-to-analog converter (DAC). All of these make PAM-4 design more challenging than NRZ. For example, if half-rate architecture is adopted and DFE requires a bunch of taps, the signal routing will introduce another parasitic and limit the DFE performance. To alleviate the hardware loading in PAM-4 signaling, we proposed the time-based PAM-4 operation shown in Fig. 4.2(b). The four-level voltage signal convert to time delay will generate four different delays T_{11}, T_{10}, T_{01} and T_{00} with three threshold delay $T_{TH,H}$, $T_{TH,M,}$ and $T_{TH,L}$. The PAM-4 linearity is more important than NRZ, so the VTC should be carefully designed. The VTC for NRZ can not be used directly in PAM-4. We will discuss this part in next session. Same as voltage-based, time-based operation requires three PD and decoder for data detecting. However, the DAC is not required in the time-based operation. The different threshold can be implemented by simple programmable delay which is equivalent to digital-to-time converter (DTC) as shown in Fig. 4.3. In NRZ, the threshold is controlled by reference delay inside the VTC and the delay difference is

$\Delta t = T_{Data} - T_{REF}$. After adding another delay stage to changing the threshold, the delay difference will change to $\Delta t = T_{Data} - (T_{REF} + T_{TH})$ where the four level delay can be detected by PD.

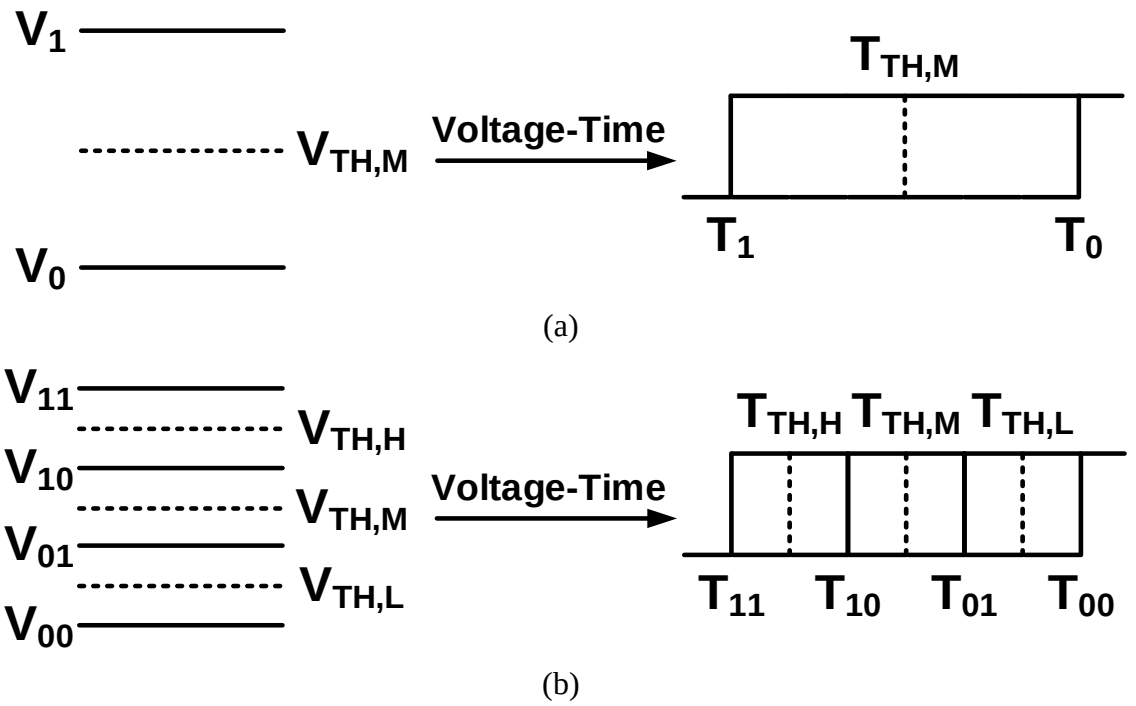


Fig. 4.2: Waveform of (a) two-level and (b) four-level signals in voltage-based and time-based.

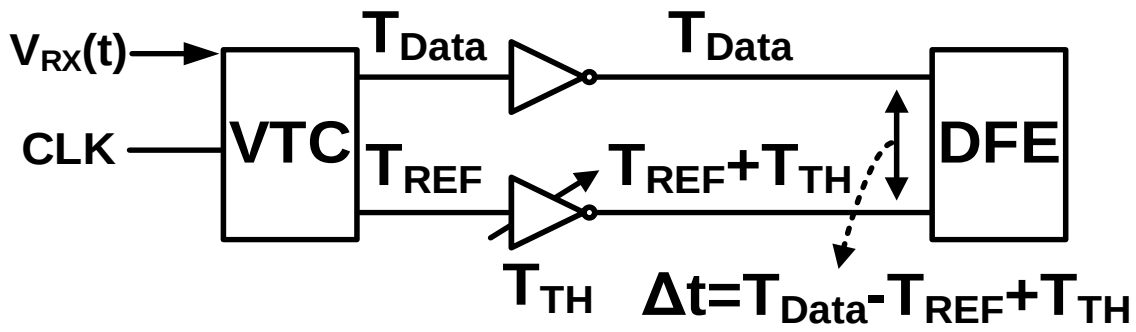


Fig. 4.3: Block diagram of DTC implementation for four-level delay comparison.

4.3 Proposed Differential Voltage to Time Converter

The VTC is required in the first stage for time-based operation. Compare to NRZ, linearity and dynamic range are two important considerations in PAM-4 receiver designs because of the multi-level signaling requirement. In particular, accurate mapping of the four voltage levels to the corresponding time delays is a critical requirement for a TB-DFE. Two types of VTCs have been used in previous works [19]-[35]. [19] utilizes the clock-to-q delay of a voltage comparator biased in a metastable condition. The offset voltage of the metastable voltage comparator is tuned by adjusting the source degeneration resistance. The source degeneration can also reduce the comparator transconductance to increase the VTC conversion gain. Since this work is targeting low TX swing around 200mV, the large gain and good linearity are reported under this range. However, this is not suitable for PAM-4 signaling, which usually requires large TX swing for better SNR and high linearity at RX. Moreover, the analog-intensive design technique is sensitive to PVT variation.

In [35], a current starved inverter stage is used where the pull-up delay is controlled by the input voltage, as shown in Fig. 4.4(a). It consists of two delay lines fed with same clock. Each delay line has two stages inverter. One delay line is data dependent and controlled by Vin, where the Vin is connected to second stage tri-state inverter PMOS. Another delay line is reference delay and usually bias at middle of D=0 and D=1. The operational waveform is shown in Fig. 4.4(b). Different voltage level signals will change the PMOS pull-up strength and change the delay. The voltage signal will modulate on the delay line RX, and the data can be read out by comparing the phase difference between RX and REF. The details implementation is introduced in Chapter 2. The inverter-based design

is more simple compare in [19]. However, the voltage-to-time gain is smaller. The transfer curve in Fig. 4.4(c) shows that the performance of linearity is an issue when the input range is increasing and makes it not suitable for PAM-4 signaling.

To achieve high sensitivity, good linearity, and robust operation, we propose the DVTC circuit in Fig. 4.4(d) where the incoming analog voltage Vin is connected to the PMOS header of the upper inverter as well as the NMOS footer of the lower inverter. Prior art VTC only modulates the signal in one delay line. Here we take advantage of the reference delay line and change the reference delay at the same time but in opposite polarity. Since the PD is rising edge detection, if we want to change the rising edge on reference delay line at opposite polarity, the Vin should be connected to NMOS footer in first stage inverter. As illustrated in the timing diagram in Fig. 4.4(e), RX_P delay, and RX_N delay have opposite polarities due to the same Vin voltage controlling the pull-up and pull-down delays of the two paths. For instance, when the data is high, the RX_P delay increases while the RX_N delay decreases and vice versa. This operation is similar to differential pair amplifiers. In ideally, the proposed DVTC can achieve two times of gain and produce the delay difference twice as large as prior art. The differential operation can also cancel out the non-linearity in the two delay paths, enabling good linearity and increase the operational range. The post-layout is shown in Fig. 4.4(f). The dash line RX_P is equal to the VTC where Vin only connected to PMOS on upper delay line. The dash line RX_P is equal to the VTC where Vin only connects to PMOS on upper delay line. Dash line RX_N represents the delay only use lower delay line, and Vin connect to NMOS. The PD will compare the phase difference between these two, and the difference is shown in black line.

This unique configuration expands the delay range from 42ps to 70ps over the entire voltage range, from VSS to VDD. The simulation result shows that the generated delay difference is less than expected. The reason is that the non-symmetric of PMOS on RX_P delay line and NMOS on RX_N delay line. Higher mobility of NMOS generates more current and decrease the delay. As shown in Fig. 4.4 (f), RX_N has smaller delay, and the phase difference has discrepancy compare to ideal case. This issue can be solved by tuning the device ratio to match the two line.

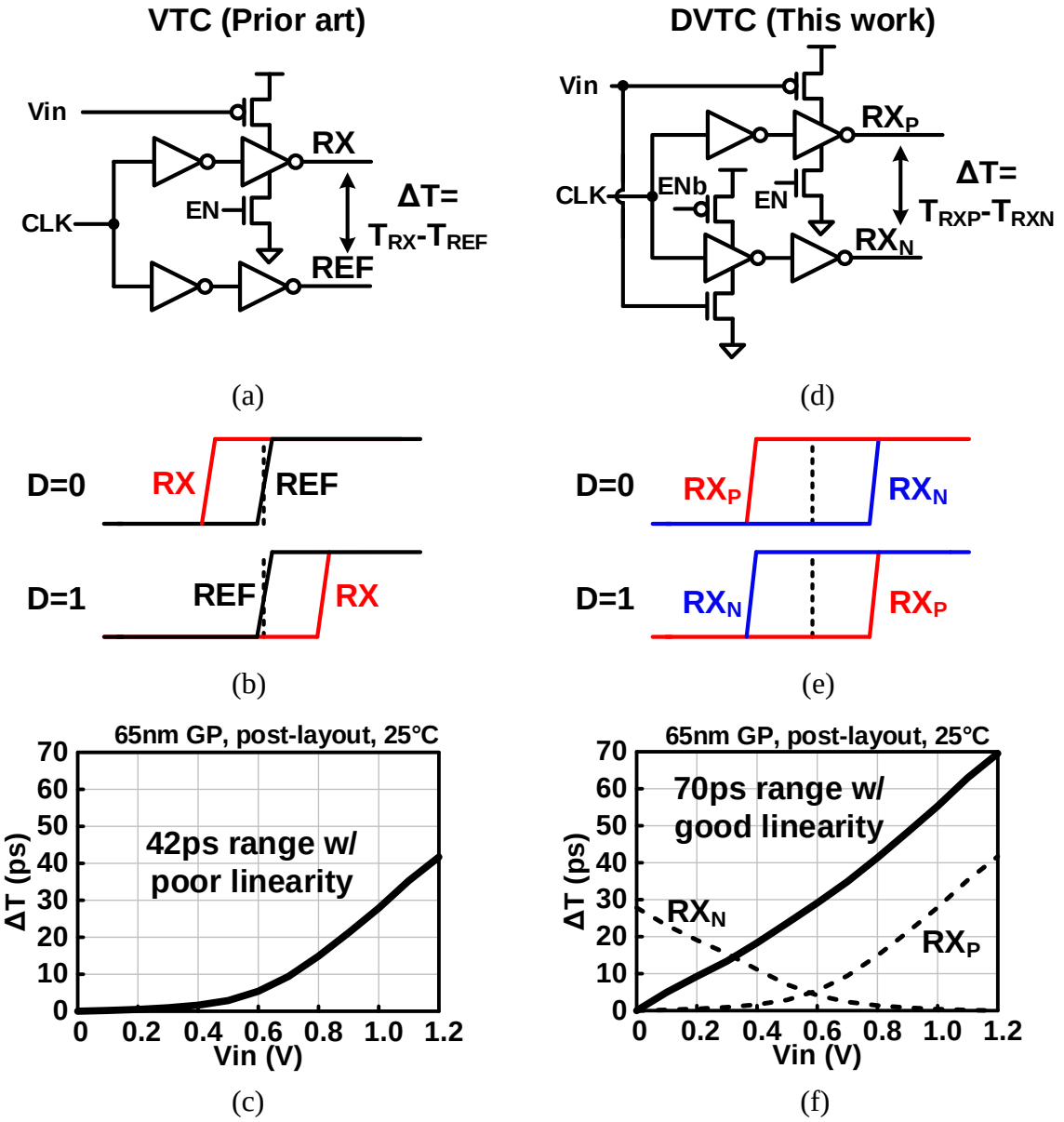


Fig. 4.4(a) Schematic, (b) operating principle, timing diagram and (c) post-layout simulation results of the inverter-based VTC [35]. (d) Proposed DVTC schematic. DVTC takes advantage of two delay lines. (e) The timing diagram of proposed DVTC. RX_P and RX_N will shift at the same time but in different polarities. (f) The post-layout simulation result shows that the linearity and dynamic range are significantly improved.

4.4 PAM-4 Time-Based DFE Circuit Design

The full PAM-4 transceiver system block diagram is shown in Fig. 4.5. In the TX part, we adopted the 3-tap half-rate feed forward equalizer (FFE) and parallel voltage-mode drivers. The on-chip pseudo random bit sequence (PRBS) generator is included to generate the data stream and also for measurement purposes. On the RX side, it includes the proposed DVTC, a half-rate 2-tap TB-DFE, a PAM-4 decoder, and a BER monitor. In-situ channel loss monitors (ICLM) were implemented on both the TX and RX sides to characterize the channel condition. We will discuss ICML in next session.

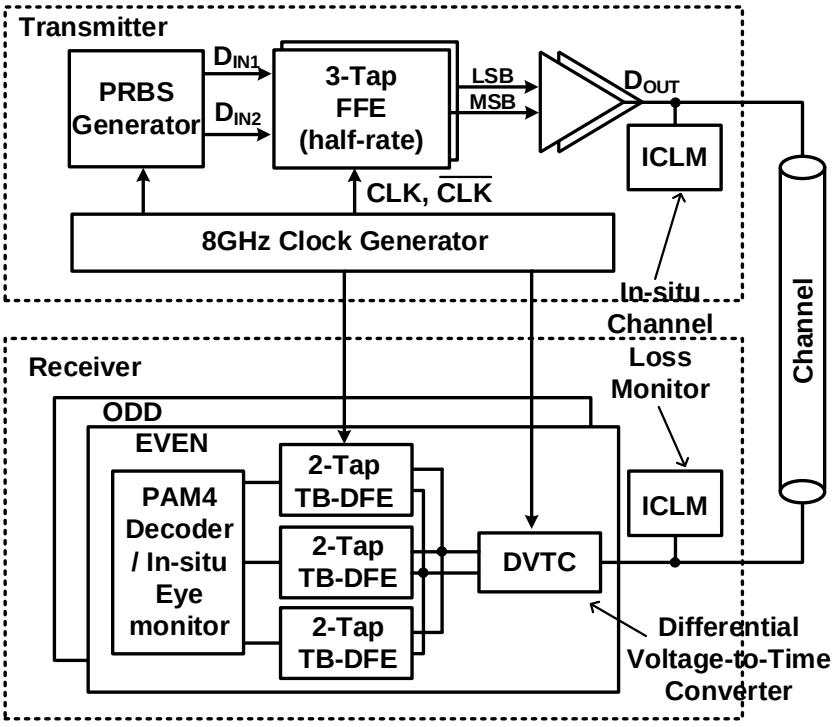


Fig. 4.5 Block diagram of proposed PAM-4 transceiver.

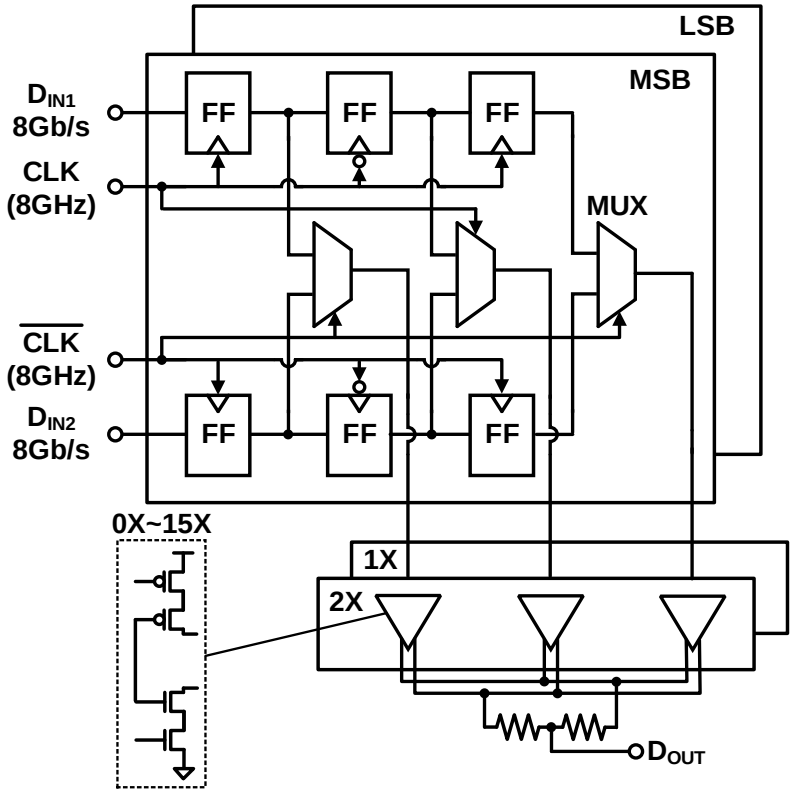


Fig. 4.6: Block diagram of the proposed PAM-4 transceiver.

The detailed implementation of the 3-tap half-rate FFE and output combiner are shown in Fig. 4.6. It consists of two paths of FFE, MSB and LSB, respectively. The 8 Gb/s bit stream is fed to the half-rate FFE for signal pre-emphasis. Two voltage mode drivers with 2X and 1X driving capability will combine two data paths and drive the same resistor load to create PAM-4 signal. The output combiner has 4-bit programmability to support different pre-emphasis levels. The detail of FFE and voltage driver can refer to Chapter 2 or [35]. Fig. 4.7 shows the implementation of the fully time-based PAM-4 DFE along with the signal waveforms for each delay stage. Differential output signals RX_N and RX_P from the odd and even DVTCs are fed to the time-based DFE block. The delay difference between RX_N and RX_P contains the signal information. The four delay levels

corresponding to voltage levels V_{00}, V_{01}, V_{10}, and V_{11} must be compared with three threshold delays $T_{REF,H}$, $T_{REF,M}$, and $T_{REF,L}$. This operation is performed by the three delay chain blocks denoted H, M, and L. Each block contains two separate delay paths for RX_N and RX_P signals, respectively. The first buffer stage performs the delay comparison while the second buffer stage performs the 2-tap DFE operation. The length of the delay chain was reduced by implementing the 6-bit DFE weights w1 and w2 in the upper and lower paths, respectively. To support half-rate operation, a total of 6 delay chain blocks with 12 delay paths and 6 PDs are implemented in our design. A notable advantage of our proposed time-based implementation is the absence of any DAC circuits for generating reference voltages $V_{TH,H}$, $V_{TH,M}$, and $V_{TH,L}$. These analog voltages are required in conventional voltage-based PAM-4 designs to detect the different voltage levels. In our time-based implementation, simple programmable delay stages are used in lieu of DACs which significantly reduces the design complexity and circuit area. The timing waveforms in the bottom of Fig. 4.7 shows how the delay signals are manifested in each delay stage. Signals RX_N and RX_P have different relative delays depending on the four signal levels. These delays are compared with different reference delays in the first delay stage. ISI noise is canceled out in the second delay stage, and the delay polarity is sampled by a PD circuit. The results generated by the PD are decoded by a PAM-4 decoder, and the BER is measured using an on-chip monitor circuit.

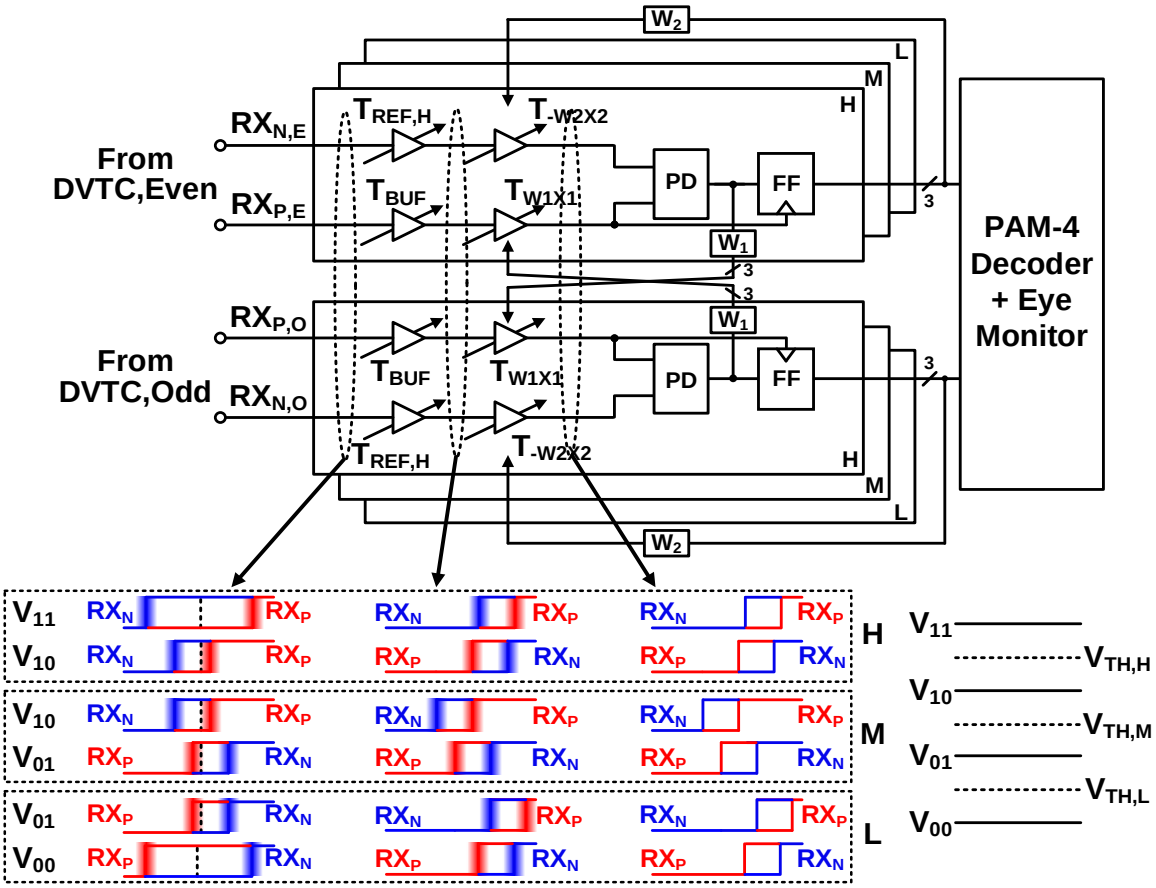


Fig. 4.7 Block diagram of proposed time-based PAM-4 DFE. The timing diagram illustrates how the delay difference is manifested after each delay stage pair for the four PAM-4 signal levels. Apart from the low voltage friendly design, our time-based approach obviates the need for DAC typically used in PAM-4 systems for generating threshold levels $V_{TH,H}$, $V_{TH,M}$, $V_{TH,L}$.

4.5 In-Situ Channel loss Monitor

Scattering parameter (S-parameter) is the de-facto measure of channel loss. The S-parameter is measured in power and use this quantity to calculate the insertion loss S_{21}. Fig. 4.8 illustrates the S-parameter setup and measurement principle. Z_S and Z_S represent the source and load impedance. By measuring the available power to the channel P_A and deliver power to the load P_D we can calculate the insertion loss from the formula shown in

the figure. However, this measurement requires an extensive test setup, including a high frequency sinusoidal signal source, network analyzer, and high frequency cables.

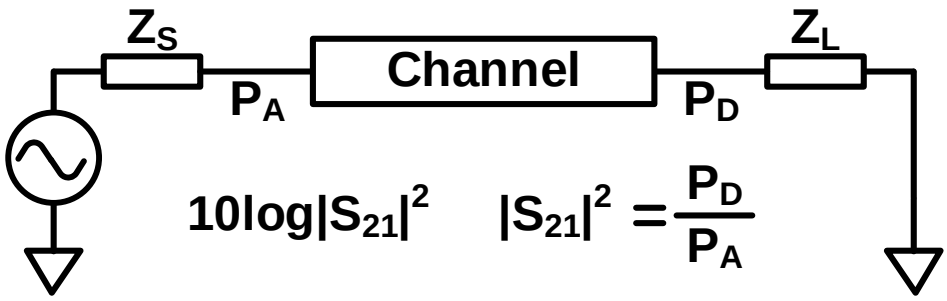
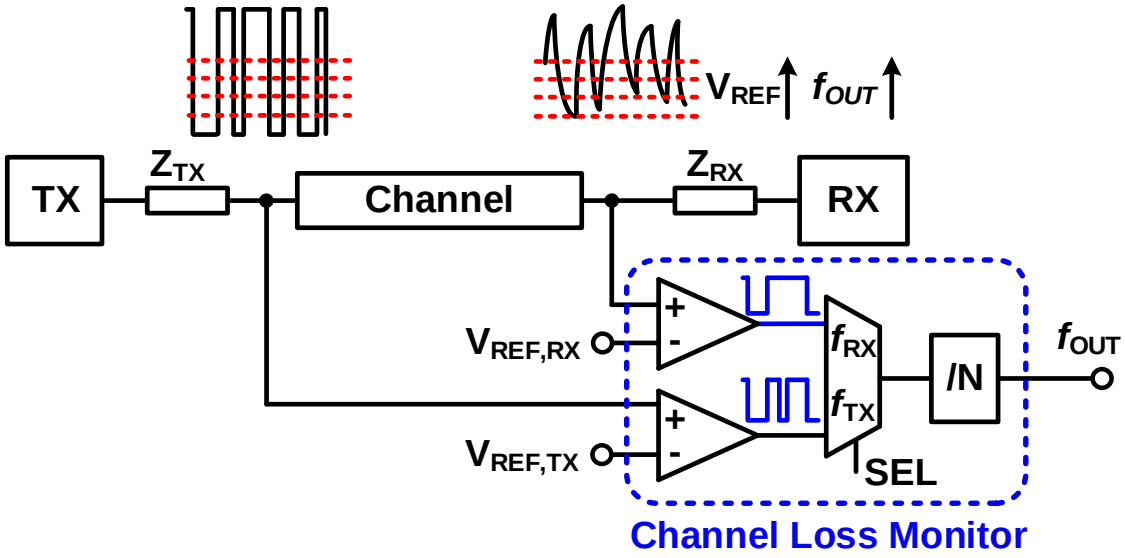


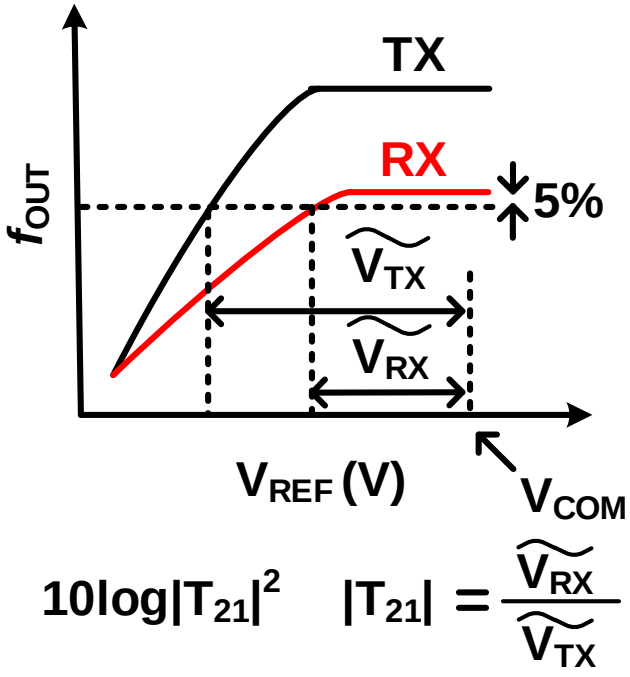
Fig. 4.8: Illustration of S-parameter measurement principle and insertion loss formula.

In this work, we designed an in-situ monitor that can indirectly measure the channel loss in time-domain by sensing the signal swings of the TX and RX signals for a random bit sequence. The proposed ICLM is shown in Fig. 4.9 (a). Z_{TX} and Z_{RX} represent the TX impedance and RX impedance, respectively. In TX side, the signal is supposed to close idea square waveform. If we set a reference voltage and measure the frequency, the frequency should be the maximum at any voltage level. On the RX side, due to the ISI, some bit cannot achieve full swing, and the frequency will change at different voltage levels. With this observation, the frequency is a function relative to reference voltage level which can help us understand the signal decay after the channel. This architecture also helps us reuse the signal from TX without any signal generator circuitry. The proposed monitor is shown in blue dash box. It included two voltage comparators, one MUX, and one frequency divider. The two voltage comparator is implemented on RX side and TX side. MUX is used to choose which frequency to be measured. The voltage comparator will

compare the TX and RX signal levels with a known reference voltage V_{REF}. By sweeping the V_{REF} and we can measure the average toggling frequency at the comparator output using a divider circuit. Fig. 4.9(b) shows how the signal swings are extracted from the measured frequency versus reference voltage data. The X-axis is the reference voltage, and Y-axis is the average frequency after divider. The frequency is expected to be low when reference is at low level. When voltage increase, the average frequency will also increase as reference voltage touch more signal swing. Due to the ISI, RX frequency is expected to be lower than the TX frequency. We also introduce a channel loss parameter $T_{21,}$ which is the ratio between the TX and RX signal swings. We first set a common mode voltage where both TX and RX reach the saturate frequency. Then we gradually lower the reference voltage until the RX frequency decrease 5%. The voltage difference between common voltage and 5% frequency decreasing reference voltage is the average swing at the RX part. The same frequency is used to find the reference voltage at the TX and get the average swing at the TX part. The frequency response can be derived by comparing two average swings. The proposed ICLM can extract the signal swing information without extensive setup. The area and power consumption of the proposed channel loss monitor are negligible.



(a)



(b)

Fig. 4.9: (a) Proposed in-situ channel loss monitor and (b) methodology for extracting channel loss parameter from the monitor output.

4.6 Measurement Results

In this section, we show the measurement results of the proposed transceiver along with ICLM. A PAM-4 test chip featuring the aforementioned techniques was implemented in a 65nm GP process. The test setup is shown in Fig. 4.10. Due to the in-situ BER monitor circuits and proposed ICML, we do not need high frequency equipment. The test chip packaged in QFN-100 is sitting in the customized PCB board. The PXI is used to scan in the control signal and reads out the data, which is already divided into low frequency. Fig. 4.11 shows the frequency data from the ICLM. The red line shows the frequency of 1GHz, and blue line is at 7GHz. The average frequency of the TX and RX comparator outputs has small discrepancy at low voltage and reaches the same level at 1GHz. The reason is due to the relatively small loss. As the frequency increases to 7GHz or higher, the RX comparator frequency saturates early due to the severe channel loss while the TX comparator frequency continues to rise. The discrepancy is also larger than 1GHz. From the frequency versus voltage plot, we calculated the loss parameter defined in Fig. 4.9(b) and compared the results with S-parameter values obtained from electromagnetic simulations as shown in Fig. 4.12. The small discrepancy can be attributed to the non-sinusoidal random bit stream used for the channel characterization. The error rate of PAM-4 line was measured using an on-chip BER monitor adopt from the previous work [35]. The bathtub curves in Fig. 4.13 shows PAM-4 TB-DFE enabling an operating window with a BER less than 10^{-12}. A time-domain (i.e. time versus time) BER eye-diagram is shown in Fig. 4.14 down to BER rates of $<10^{-9}$.

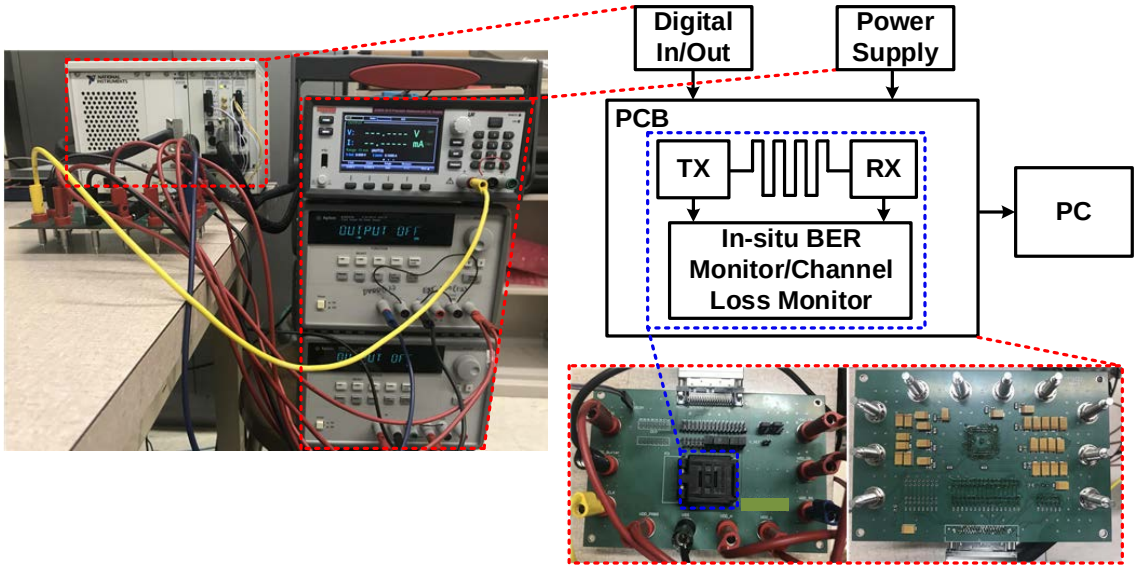


Fig. 4.10: Measurement setup. A low frequency test interface is used owing to the in-situ measurement circuits. The setup consists of a custom PCB with a QFN-100 socket holding the packaged chip, power supplies, and a PXI system.

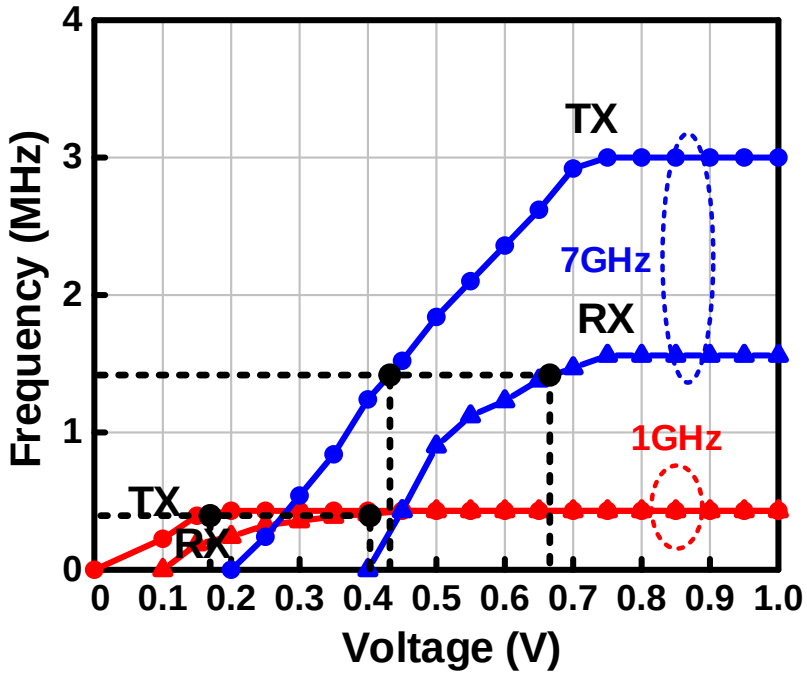


Fig. 4.11: Frequency data measured by proposed ICLM.

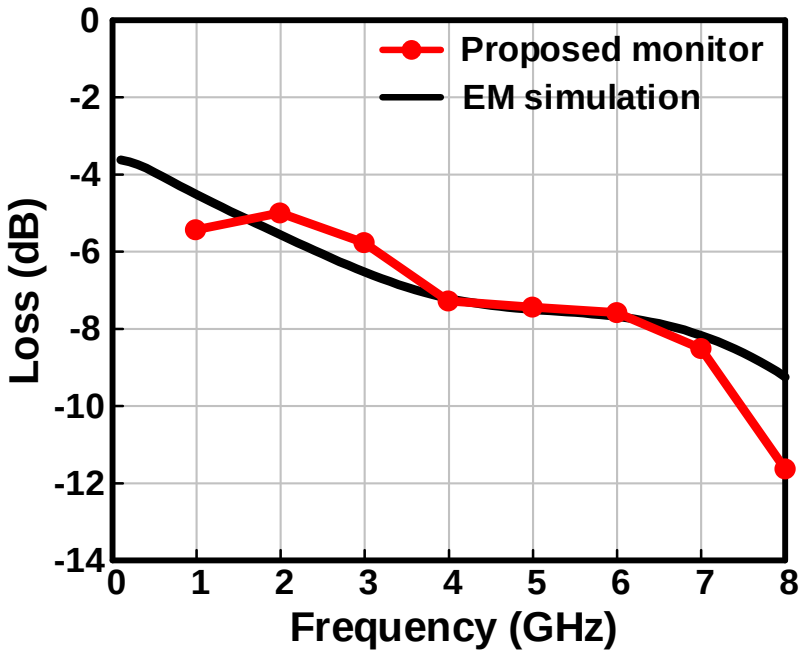


Fig. 4.12: The reconstructed channel characteristics used the data from Fig. 4.11.

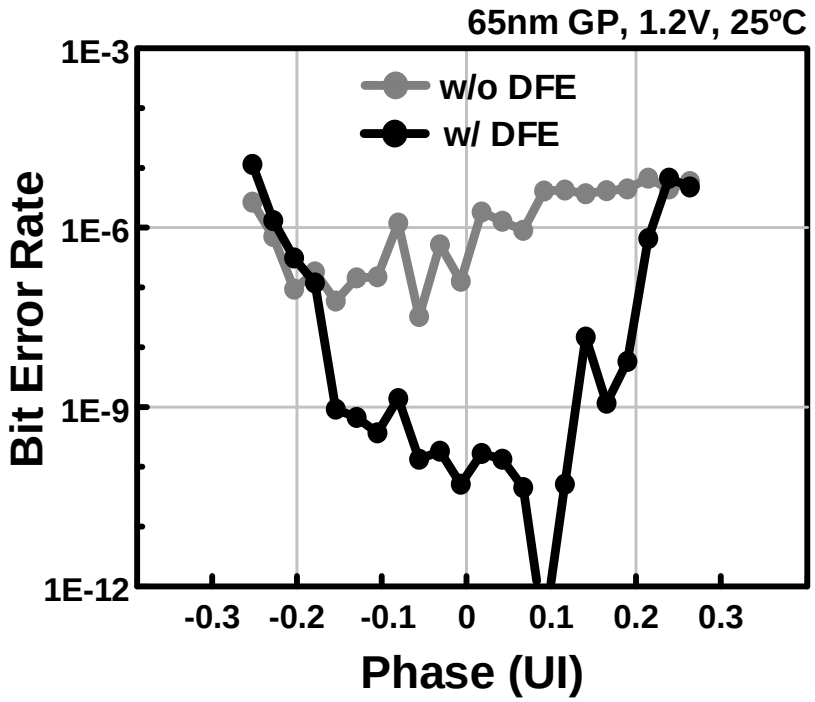


Fig. 4.13: Measured BER bathtub curves (<10^{-12}) with and without TB-DFE.

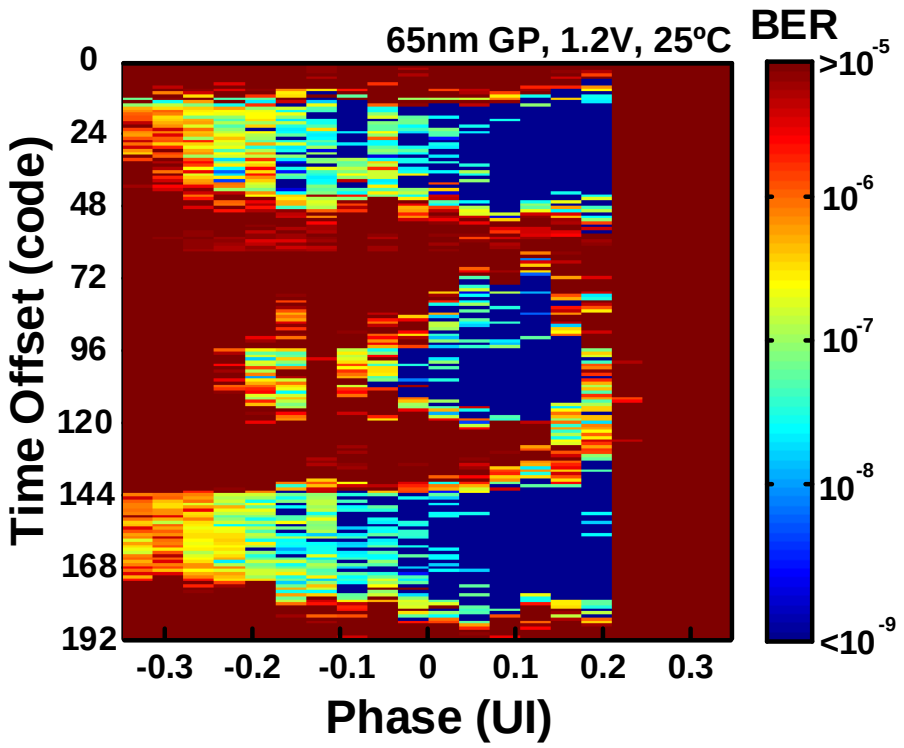
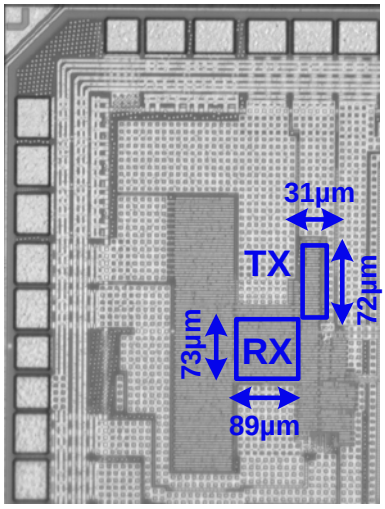


Fig. 4.14: Measured BER eye-diagram (<10^{-9}).

Fig. 4.15 shows the test chip die photo and summary table. The TX occupy a chip area of 31×72 μm^2 while RX side occupies 73×89 μm^2. The channel loss is 11.6 dB at 8 GHz measured by proposed ICLM. The PAM-4 transceiver operates at is 32 Gb/s data rate. The total energy-efficiency of the transceivers is 0.97 pJ/b at 1.2V supply voltage while BER can achieve 10^{-12}. Fig. 4.16 compares the proposed design with various types of signaling for high speed memory interface. The proposed design has a competitive performance



Technology	65nm CMOS
Circuit Area	TX: 31x72µm^2
	RX: 89x73µm^2
VDD	1.2V
Data Rate	32 Gb/s
Channel Loss	11.6dB@8GHz
BER	<10^{-12}
Power Efficiency	0.97 pJ/b

Fig. 4.15: Die photo and feature summary table.

	JSSC'14 [1]	ISSCC'19 [2]	ISSCC'16 [3]	JSSC'18 [4]	This work
Signaling	Duobinary	PAM-3	Muti-Band	NRZ	PAM-4
Single/Differential	Single-Ended	Single-Ended	Differential	Single-Ended	Single-Ended
RX Circuit Type	Voltage-Based	Voltage-Based	Voltage-Based	Time-Based	Time-Based
RX Equalization	1-Tap DFE	1-Tap DFE	Self-Equalization	2-Tap DFE	2-Tap DFE
Data Rate	7 Gb/s	27 Gb/s	10 Gb/s	12.5 Gb/s	32 Gb/s
Technology	65nm	28nm	28nm	65nm	65nm
Voltage	1.05V	0.6V	1.2V	0.8V	1.2V
Channel Loss	0.8dB@3.5GHz	20mm	6dB@6GHz	14dB@6.25GHz	11.6dB@8GHz
BER	<10E-12	<10E-12	<10E-12	<10E-12	<10E-12
TRX Area	0.0333 mm^2	0.0135 mm^2	0.01 mm^2	0.0094 mm^2	0.009 mm^2
TRX Power Efficiency	0.56 pJ/b	1.03 pJ/b	0.95 pJ/b	0.49 pJ/b	0.97 pJ/b

Fig. 4.16: Comparison with previous high speed memory interface.

4.7 Conclusions

In this chapter, we demonstrate a single-ended digital-intensive PAM-4 time-based transceiver for high speed memory interface. The digital intensive circuit technique is friendly to CMOS scaling and robust to PVT variation. The simple inverter-based implementation can reduce the design overhead with complicated PAM-4 design. With singled-end data transmission, the proposed structure can also immune the common noise with differential operation features of DVTC and delay line. The time-domain channel noise monitor used random bit sequence was introduced to characterize the channel loss. The performance of 65nm test chip was verified by on-chip BER monitor. The results show that the proposed PAM-4 transceiver has comparable performance with prior art while offering the unique benefits of a time-based design like digital-intensive, low voltage operation, and good scalability, which is a potential option for advanced memory interface.

Chapter 5. Summary

In this thesis, three digital intensive time-based high speed transceiver is proposed for high speed link, including on-chip interconnect, system in package (SiP) link and memory interface. In addition, in-situ time-domain bit error rate (BER) monitor and channel loss monitor are introduced to verify the performance without any extensive testing setup. The proposed transceiver along with on-chip measurement circuits are implemented in TSMC 65nm GP process.

Chapter 2 presents the time-based decision feedback equalizer (DFE) for on-chip interconnect. The time-based DFE can perform the DFE function in time-domain by the inverter delay line. The differential operation of the delay line can cancel out the variation between two delay lines. Also, the inverter-based implementation and delay transformer technique allows the high scalability of DFE taps without affecting the throughput. The 65nm test chip is verified with proposed on-chip monitor. The result shows that the proposed transceiver can achieve BER less than 10^{-12} while operates 10 Gb/s data rate for 10mm interconnect. The total energy efficiency is 77.2 fJ/b/mm under 1.2V supply voltage and total chip area for transmitter and receiver is $23\times24\mu m^2$ and $30\times59\mu m^2$, respectively.

A time-to-digital converter (TDC) based receiver with time-based front-end is introduced in Chapter 3 for system in package (SiP) link. The amplification function can perform in a delay line based circuit instead of analog front-end (AFE). The Vernier line TDC enables the post-digital equalization with the highly digitalize time-based front-end. By using the proposed time-domain BER monitor, the proposed transceiver can achieve

8Gb/s data rate with 7mm in-package link with the BER less than 10^{-12}. The total energy efficiency is 2.1 pJ/b under the 1V supply voltage. The occupy chip area is 0.0192mm^2.

Chapter 4 demonstrates a PAM-4 transceiver for high speed memory interface. The proposed transceiver utilizes the time-based DFE to reduce the design complexity for PAM-4 operation. The digital-to-analog converter (DAC) is not required. Instead, the different delay threshold can be implemented by a simple delay buffer. The time-domain in-situ channel loss monitor (ICLM) is proposed to measure the channel characteristic. The proposed 32 Gb/s PAM-4 transceiver is measured by on-chip BER monitor and ICLM. The result shows that the transceiver can achieve BER less than 10^{-12} with 1.2 supply voltage. The total energy efficiency is 0.97 pJ/b with the chip area of 0.009mm^2. The channel loss is 11.6 dB at 8GHz.

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