Graphene Point Junctions: A Potential Platform for Achieving Valley Polarization

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Introduction

Traditional electronic devices such as transistors and capacitors utilize the charge and motion of electrons to achieve their task. Next-generation electronic devices that take advantage of electron's spin and valley degrees of freedom, known as spintronic and valleytronic devices respectively, have the potential to improve upon these traditional electronics [1]. We study one such valleytronic device, the valley polarizer, implemented using a PN point junction. This device could serve as a building block for more complex next-generation valleytronic devices.

Background

The band structure of bilayer graphene (BLG) contains local energy extrema in momentum space known as valleys. BLG has two distinct valleys labeled K and K' at the corners of the first Brillouin zone [2]. A valley polarized current occurs when states associated with one valley are populated over those associated with the other.

Bilayer graphene has a bandgap tunable by external perpendicular displacement fields, effectively allowing for control over whether it is zero-bandgap, P-doped, or N-doped [3]. Local gates can be used to take advantage of this, creating gate-defined nanostructures.

One such nanostructure is a point-junction (PJ), a narrow conductive region surrounded by insulating regions [4]. When the PJ is formed, we expect some conductivity due to electrons tunneling through the barrier. In configurations where the displacement field changes its sign between the insulating regions, theory predicts the existence of symmetry-protected conductive states known as valley-chiral states. These states carry K or K' electrons depending on the current direction, making the PJ a promising candidate for creating valley-polarized currents [5-6].

Trivial and Non-Trivial Configurations

In the trivial configuration, the D-field does not change its sign between the two insulating regions. In the non-trivial case, the D-field does change its sign.

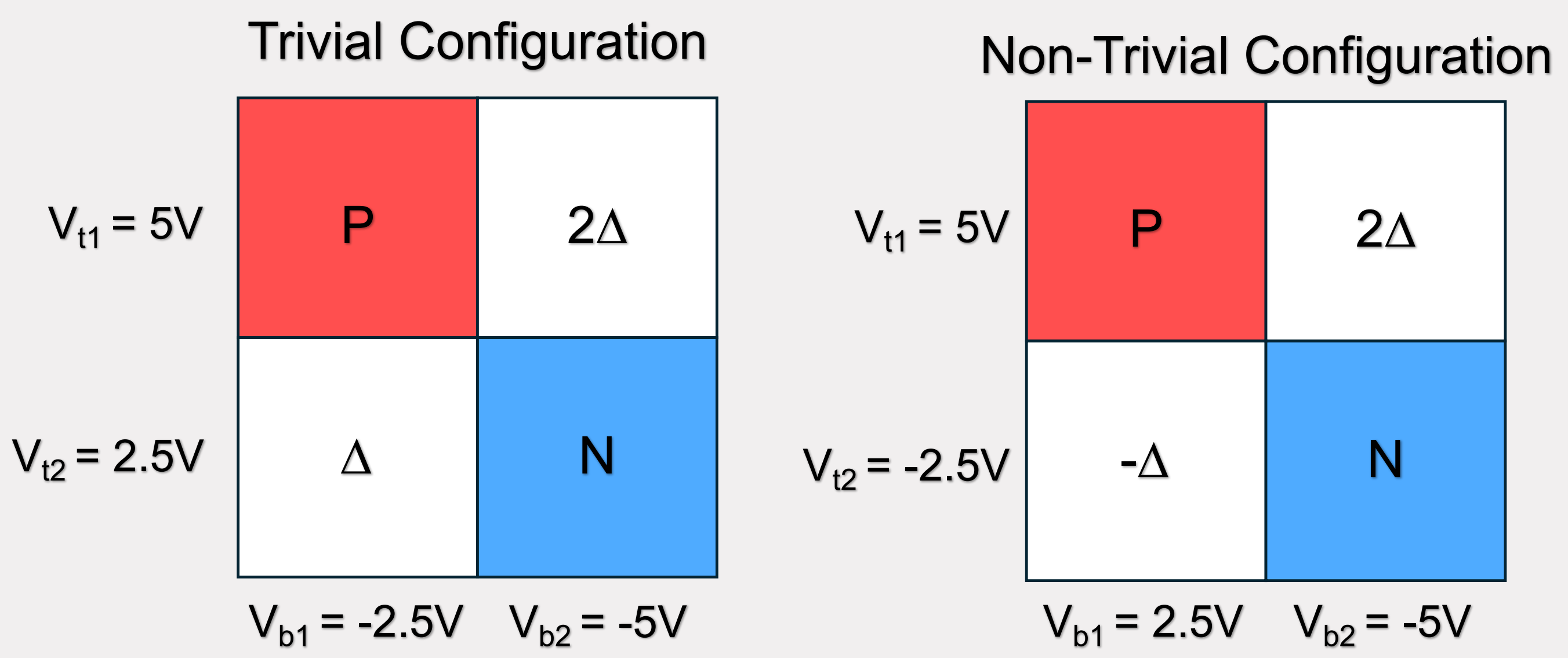

Fig 1. Gate Voltages and resulting device structure for trivial and non-trivial configurations. $V_{t1,2}$ and $V_{b1,2}$ refer to top and bottom gate voltages.

In the trivial case, we expect tunneling through the junction to be responsible for the device's conductivity. In the non-trivial case, theory predicts the changing sign of the displacement field (and thus changing valley Chern number) results in valley-chiral states through the PJ. The existence of these states increase device conductivity and allow the non-trivial configuration to function as a valley-polarizer.

Methods

To fabricate the device, we begin by stacking mechanically exfoliated bilayer graphene (BLG) and hexagonal boron nitride (hBN). A top and bottom hBN serve as insulators between orthogonal top and bottom pairs of metal gates and the BLG. The stack is transferred to a SiO_2 wafer with pre-deposited metal gates. Top metal gates and electrical contacts are deposited using electron beam lithography and metal deposition. The final geometry of the device is defined using lithography and reactive-ion etching.

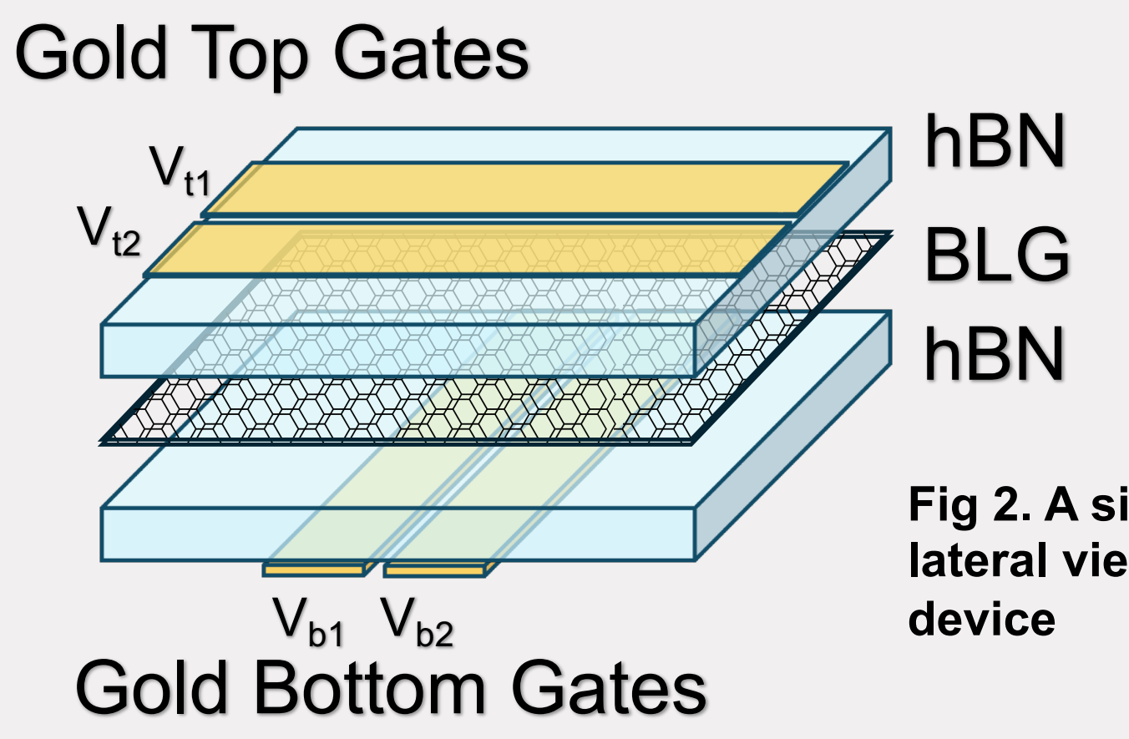

Fig 2. A simplified lateral view of the device

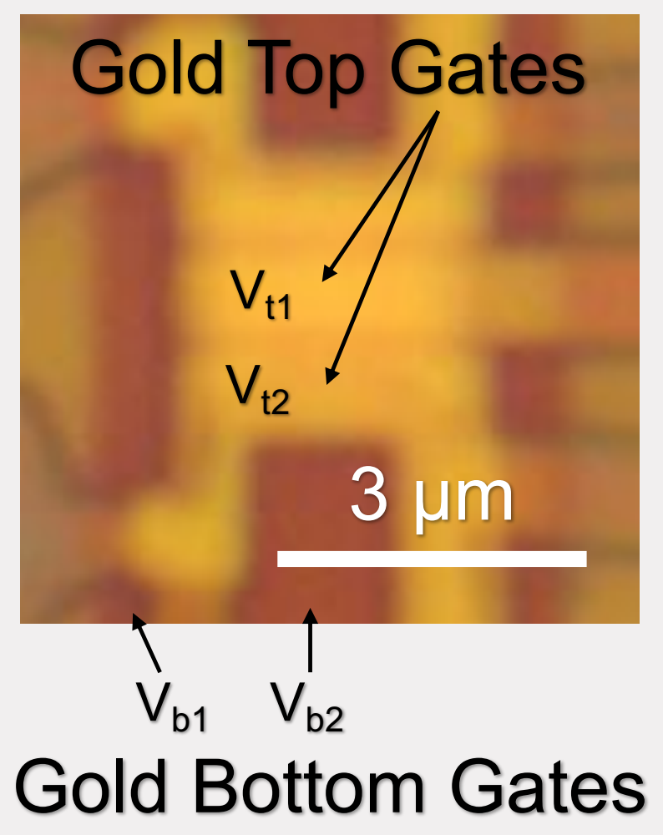

Fig 3. The final device under an optical microscope

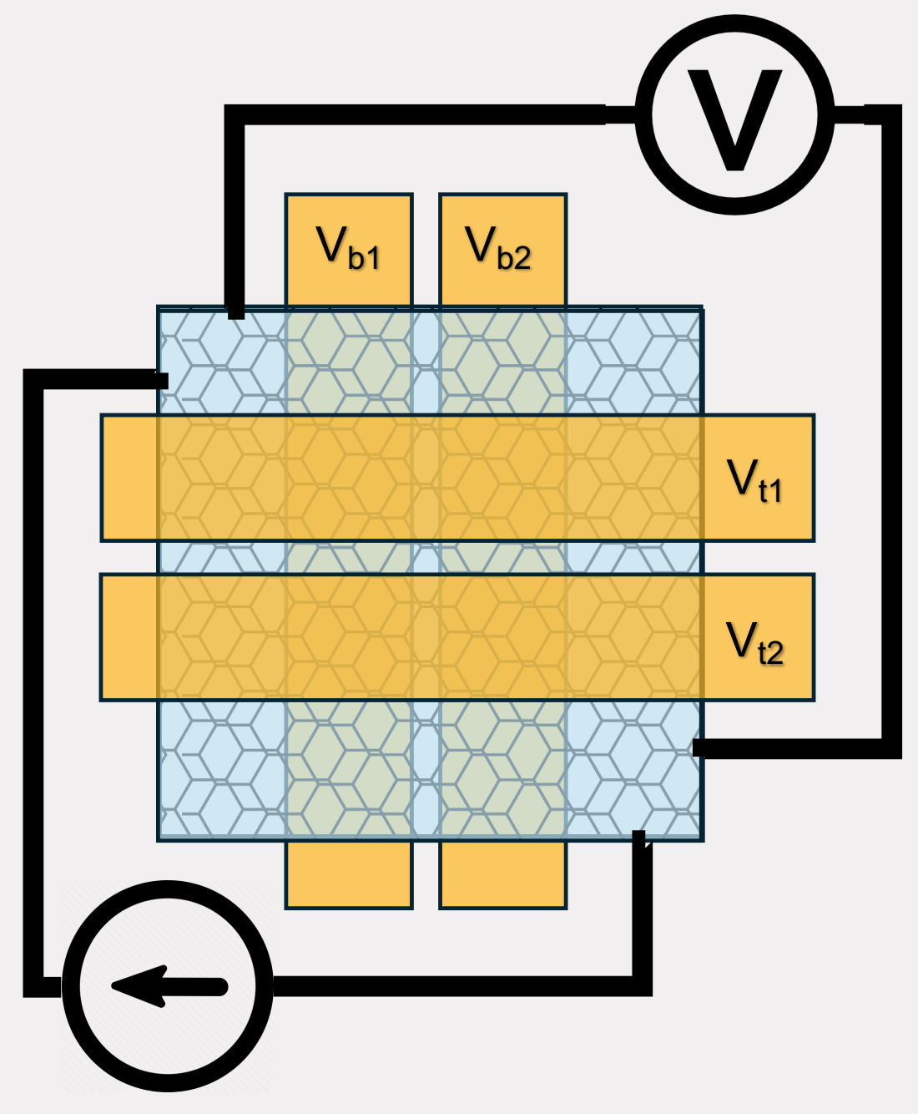

Fig 4. A diagram of the measurement setup

The device was configured in the trivial and non-trivial cases as defined in Fig 1. Measurements were taken in a cryostat at a temperature of 4.2K. The gate voltages (V_{b1}, V_{b2}) were varied, and the resulting device resistance was measured. Resistance was plotted as a function of ΔV_{b1} and ΔV_{b2} (Fig 5), where each ΔV_b is the difference between the gate voltage and the ideal gate voltage for point junction formation, as defined in Fig 1.

Results

In both trivial and non-trivial configurations, we observe a resistance peak which suggests a point junction has formed. The trivial and non-trivial configurations display peak resistances of 9.82 kΩ and 2.09 kΩ respectively. The lower resistance in the non-trivial configuration can be attributed to the existence of valley-chiral states through the junction.

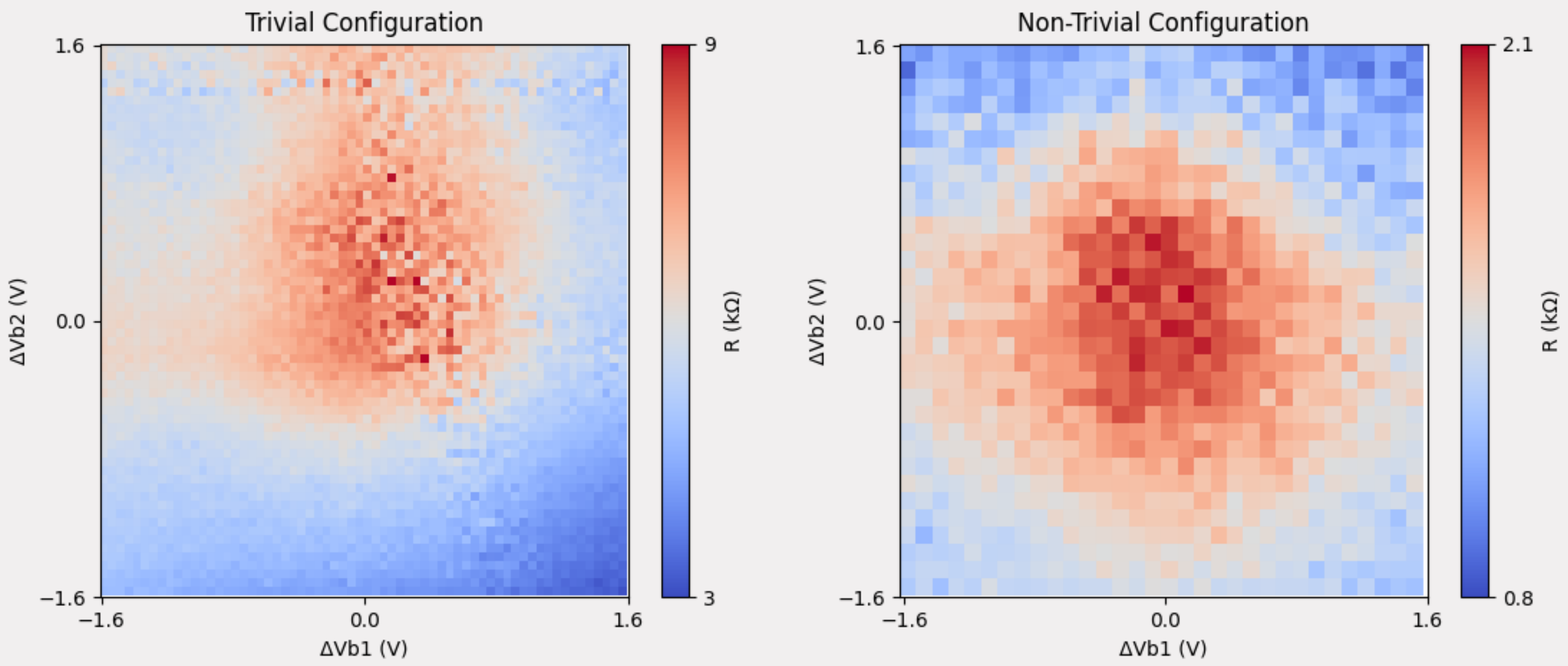

Fig 5. Device resistance as a function of bottom gate voltages. The origin represents the formation of a point junction.

The additional valley-chiral states in the non-trivial case have a predicted resistance of $h/4e^2$ Ω (~6.45kΩ). We denote this resistance R_V. The measured resistance in the non-trivial configuration is notably less than R_V, since there is a parallel resistance R_T due to valley unpolarized tunneling through the junction.

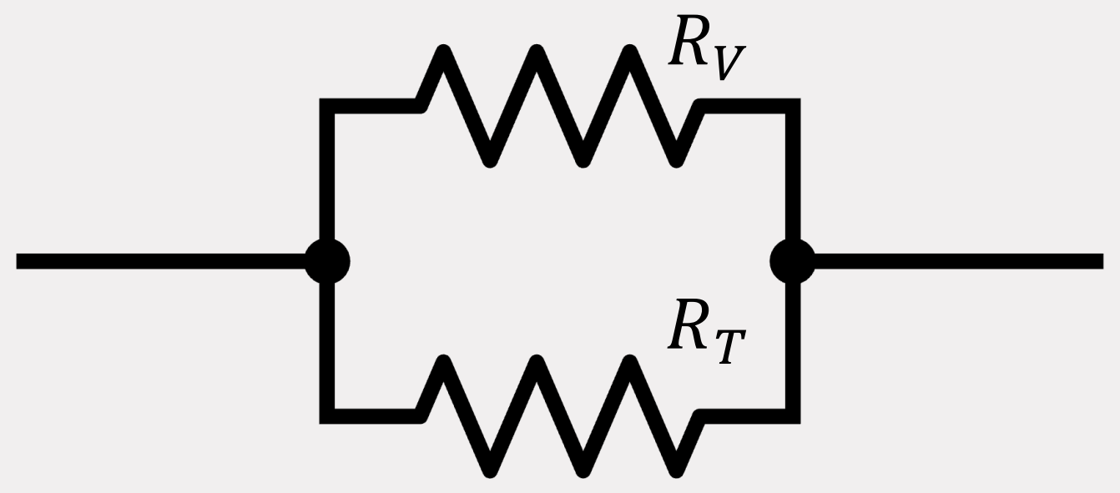

Fig 6. A model for the non-trivial point junction configuration considering the tunneling resistance along with valley-chiral states.

Overall, the decrease in resistance from trivial to non-trivial configurations provides some evidence for the existence of valley-chiral states through the junction. This would suggest that current flow in the non-trivial case is partially valley-polarized. Further research could attempt to enhance the polarization by reducing tunneling, either by increasing displacement fields (and thus bandgap) or by applying a perpendicular magnetic field.

References

[1] J. R. Schaibley, H. Yu, G. Clark, P. Rivera, J. S. Ross, K. L. Seyler, W. Yao, and X. Xu, *Valleytronics in 2D Materials*, Nat Rev Mater **1**, 1 (2016).

[2] E. McCann and M. Koshino, *The Electronic Properties of Bilayer Graphene*, Rep. Prog. Phys. **76**, 056503 (2013).

[3] Y. Zhang, T.-T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen, and F. Wang, *Direct Observation of a Widely Tunable Bandgap in Bilayer Graphene*, Nature **459**, 7248 (2009).

[4] Konstantin Davydov, Xi Zhang, Wei Ren, Matthew Coles, Logan Kline, Bryan Zucker, Kenji Watanabe, Takashi Taniguchi, Ke Wang, *Easy-to-Configure Zero-Dimensional Valley-Chiral Modes in a Graphene Point Junction*, Science Advances (in press).

[5] J. Li, K. Wang, K. J. McFaul, Z. Zern, Y. Ren, K. Watanabe, T. Taniguchi, Z. Qiao, and J. Zhu, *Gate-Controlled Topological Conducting Channels in Bilayer Graphene*, Nature Nanotech **11**, 1060 (2016).

[6] I. Martin, Ya. M. Blanter, and A. F. Morpurgo, *Topological Confinement in Bilayer Graphene*, Phys. Rev. Lett. **100**, 036804 (2008).