UNIVERSITY OF MINNESOTA TWIN CITIES

DOCTORAL THESIS

Modular Multilevel Converter (MMC) with High-Frequency Link and Natural Capacitor Balancing for Grid-Interfacing of Renewables

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A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

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This dissertation is dedicated to my family

Prince Kumar

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Abstract

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Doctor of Philosophy

Modular Multilevel Converter (MMC) with High-Frequency Link and Natural Capacitor Balancing for Grid-Interfacing of Renewables

by Prince Kumar

This thesis presents an isolated modular multi-level architecture designed to interface low/medium DC voltage sources (such as renewable energy sources) to medium-voltage transmission/distribution system levels. The architecture uses isolated high-frequency links with full-bridge sub-modules. Due to its structure, it has natural capacitor self-balancing properties and all the three phases can be operated independently on a single phase basis.

The proposed topology consists of one primary H-Bridge converter and several identical sub-modules. Each sub-module consists of a high-frequency transformer, a full-bridge diode rectifier, a capacitor, and a full-bridge output-stage converter. The output of the primary H-Bridge is connected to a high-frequency bus. All sub-modules draw power from this bus. Sub-module outputs are connected in series on a per-phase basis, to generate large multi-level voltage outputs. Since each module produces an isolated, bipolar, switching AC voltage, modules are inserted or bypassed to synthesize the desired AC voltages level. This thesis presents a novel hybrid pulse-width-modulation (PWM) method for this topology which combines the benefits of level-shifted PWM (low switching losses) with the benefits of phase-shifted PWM (equal module utilization). This is achieved through a re-assignment of carriers, resulting in negligible computational overhead.

The thesis also includes a new variant of this topology with a combination of wide-bandgap (WBG) and silicon (Si) devices; along with the associated PWM scheme. Here, one sub-module (SM) in each phase employs Gallium Nitride (GaN) devices and switches at high frequency to produce a switching output

voltage, while the rest of the sub-modules consist of traditional Si devices operating at low switching frequency. This combination reduces the overall converter cost while also yielding high efficiency. The proposed schemes are validated by simulation and experimental results with a nine-level H-Bridge multilevel converter hardware.

Acknowledgements

I want to express my deepest gratitude to my advisor Professor Ned Mohan for giving me this opportunity. He have always been very supportive of me since the moment I expressed my interest in graduate school. I'm very grateful for their guidance and support throughout my research at the University of Minnesota. I can't thank enough to Dr. Abhijit Kshirsagar, for all the valuable guidance and support throughout my school. He was always there for any small or challenging task I faced during my work. The ideas and lessons learned from him really helped me to succeed in my research.

I want to express my gratitude to Professors Robbins, Dhople, and Hemati. Professor Dhople and Mohan gave me the opportunity to TA for their perspective classes which helped me realize how much I enjoy teaching. This also expanded my interest in the area of power systems. Professor Robbins gave me the opportunity to teach undergraduate labs which gave me one of the best memories and or experiences in my graduate-level career. I would also like to thank Professor Hemati for all the support he's provided me during my time as a graduate student at the University of Minnesota. Last but not least, I would like to thank my lab mates Venkat, Manikanta, Jeyaram, Sreekant, Kundan, Ruben, and Siddarth for their support and technical expertise.

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List of Abbreviations

MMC	**M**odular **M**ulti-level **C**onverter
THD	**T**otal **H**armonic **D**istortion
PV	**P**hoto **V**oltaic
PWM	**P**ulse **W**idth **M**odulation
NLM	**N**eareast **L**evel **M**odulation
FFT	**F**ast **F**ourier **T**ransform
IGBT	**I**nsulated **G**ate **B**ipolar **T**ransistor
WBG	**W**ide **B**and **D**evices
GaN	**Ga**llium **N**itride
CHB	**C**ascaded **H**-**B**ridge

Chapter 1

INTRODUCTION

1.1 Grid-tied converters for Renewables

1.1.1 Motivation

Rapid development in power electronics is the vehicle in which the United States electric grid is transitioning into the 21^{st} century. This has allowed greater use of renewable and has reduced our dependence on fossil fuels. Distributed Energy Resources (DER) sources such as photovoltaics (PVs) are connected to the grid via so-called grid-interactive inverters. Conventionally, PV or wind farms are connected to the grid via three phase inverters, filters, and line frequency transformers as shown in Fig.1.1 [1] [2]. Although this system is well tested, robust and reliable, it suffers from many shortcomings. The inverters are usually three-level inverters, which need bulky line frequency transformers and filters. Also, since most collection voltages for utility-scale generation are 34.5 kV or higher, a line frequency step-up transformer is required, which is also large and heavy.

Multilevel converters with high frequency transformers have the potential to overcome many of these drawbacks. Modular multilevel converters (MMCs)

have a scalable, modular structure due to the use of several identical submodules which can be easily replaced in case of failures, resulting in very low down time [3][4][5][6], and has been used in several other applications [7][8][9].

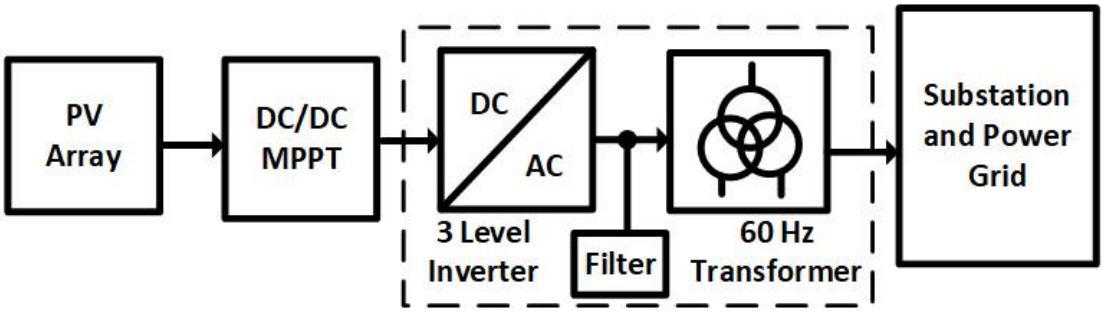

FIGURE 1.1: Traditional Grid Connection

The modular topology in [10] replaces the traditional 60 Hz transformer with multiple compact, lightweight, high frequency transformers. It produces multi-level output voltages, following the sinusoidal waveform, which lead to lower total harmonics distortion (THD). This topology can generate high voltage output suitable for direct connection to a 34.5 kV collection grid. Since the power and voltage stresses are distributed across sub-modules of the multi-level converter, lower rated components can be used to achieve the desired high voltage and power levels. Previous work on modulation schemes for this high-frequency link MMC includes a level-shifted carrier-based approach, which is computationally simple but results in vastly unequal stresses in the different modules. Alternatively, phase-shifted PWM can equalize module stresses, but this results in much higher switching losses. This paper proposes a modified PWM technique based on the level-shifted carrier approach, which equalizes the module stresses without increasing switching losses.

1.2 Prior Art

Falling costs of renewable energy components have aided the push for cleaner energy sources. This has driven the need for improved power electronic topologies for grid connection of renewable energy sources.

Traditional methods of connecting renewables to grid employed two- or three-level power electronic converters and line frequency (60 Hz) transformers. The emergence of high-frequency transformers to replace line-frequency transformers provided major improvents such as reduced weight and footprint. However, existing two- or three-level power converters were not very much suited for grid connection at higher voltage level (34.5 kV), due to high harmonic content and the need for line-side filtering. The use of pulsed squared voltage also resulted in issues due to large dV/dt transitions. Multi-level converters were proposed to increase the number of levels in the output waveform, which reduced the output harmonics to a significantly lower level. Depending on the voltage level, a multilevel converter can reduce the harmonics to a point where a very small or even no output filter is necessary. Several topologies and configurations of multilevel converters have been proposed: one example in Europe for PV application uses a cascaded multilevel converter [10]. Other multi-level converter topolgies for PV application include active-clamp inverters[11] and flying-capacitor and series connected H-Bridge[12]. Several multilevel topologies have been proposed specifically for grid connected renewables with low total harmonic distortion (THD) in the output voltage. However, many suffer in terms of complex design, low flexibility, and difficult operational requirements. Modular multilevel converters (MMC) have emerged as the solution for the drawbacks presented in the traditional multilevel converters. MMCs work in a similar fashion to traditional multilevel converters,

except more levels are easily added to reduce the THD. MMCs have a modular structure which makes them very flexible, reliable, easy to design & repair. This thesis presents a modular multilevel converter with high frequency transformers that is suitable to replace the target area (the doted window) in Fig.1.1.

1.3 MMC Topology

The MMC topology [8] consists of a primary H-Bridge and several identical sub-modules whose outputs are connected in series to give multilevel output voltage. The input to the topology (primary H-Bridge) can come from PV/wind system, after converting it to suitable DC voltage. The H-Bridge consists of high-frequency switches which operate at 20kHz and produce a high frequency alternating voltage V_{alt} as shown in Fig.1.2. The output, V_{alt}, is then connected to a high frequency bus which connects to the primaries of several high frequency transformers, whose secondaries are connected to a diode full bridge rectifier, followed by DC capacitor and a full bridge converter. The sub-module arrangement is shown in Fig.1.3. Multiple sub-modules can be stacked together to produce the required number of levels across the output. Fig.1.4 shows the per phase arrangement for four such modules. The overall circuit, design attributes, advantages, and trade offs are explained in the following section.

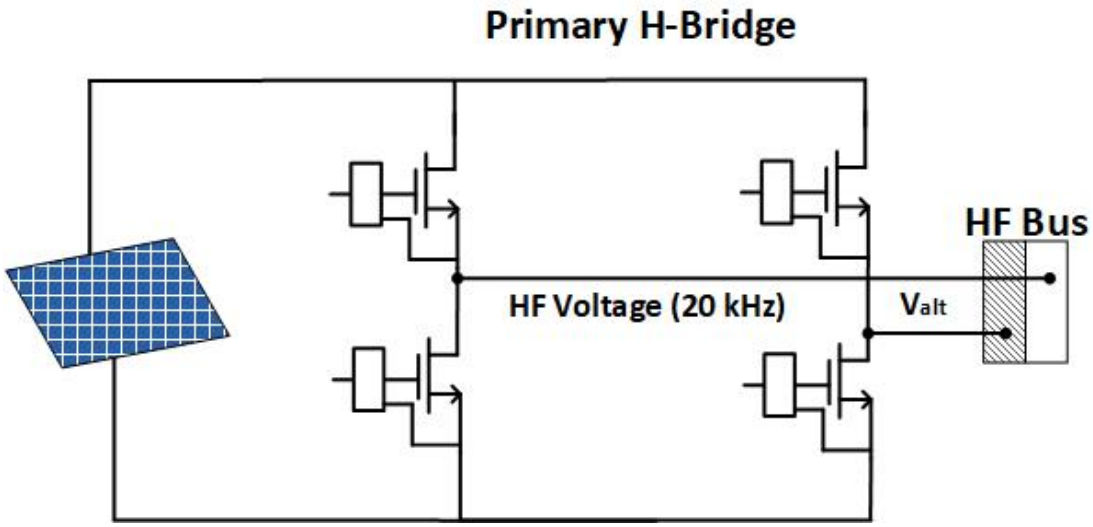

FIGURE 1.2: Primary H-Bridge

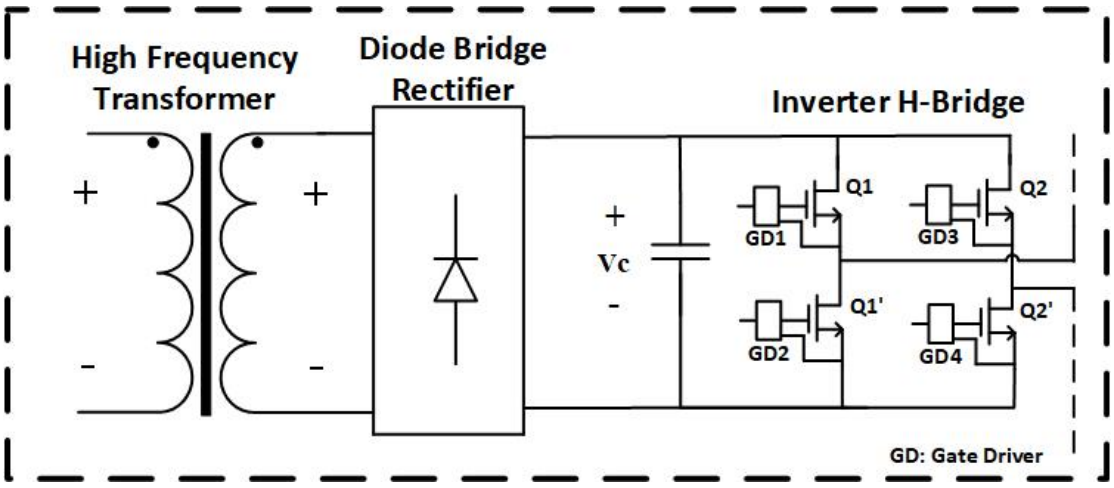

FIGURE 1.3: Sub-Modules Topology

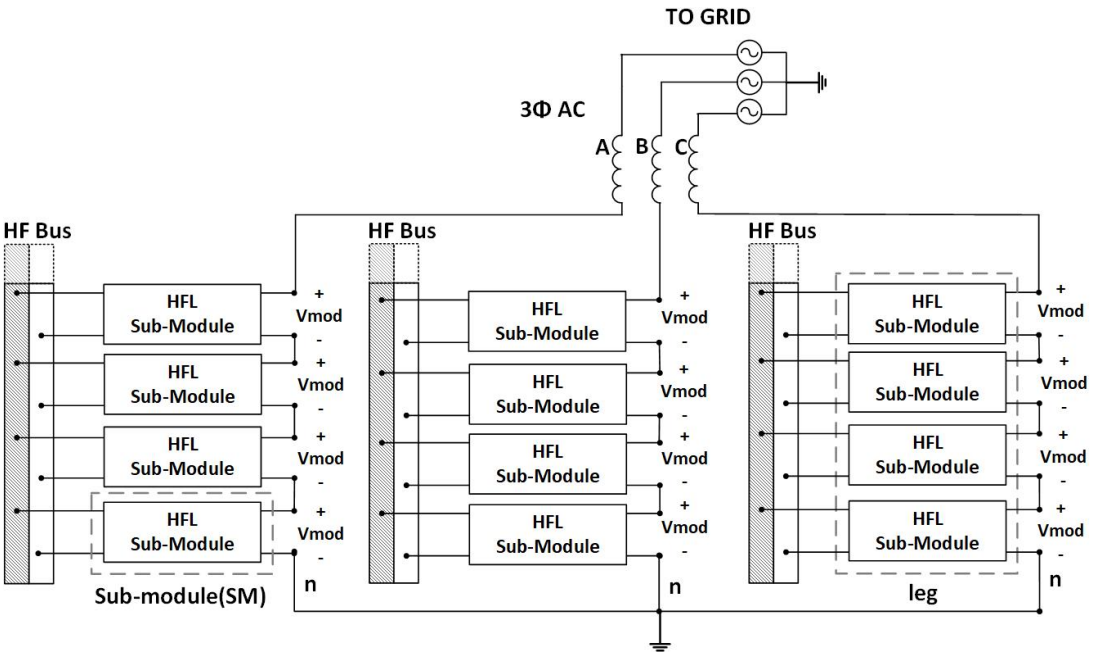

FIGURE 1.4: MMC Topology

For the present analysis and simulation studies, each phase is taken to consist of four sub-modules. Therefore, each pole-voltage can have 9-levels, including the zero level. The carrier wave frequency considered for PWM is 10kHz for the sub-modules. The primary H-Bridge is driven at 20 kHz at a duty cycle of 50 percent. The effects of variable duty cycle and/or phase-shift modulation in the H-bridge are beyond the scope of this thesis.

The output of the PV after a DC to DC converter (or AC to DC in case of wind) acts as input for the topology, and is given to the primary H-Bridge. The H-Bridge converts the DC input to a high frequency AC (20 kHz in this case) shown in Fig.1.5. This signal is given to each sub-module individually, where it passes through the high frequency transformer and diode bridge to provide a DC signal to the H-Bridge of the sub-modules. Gate signals to the H-Bridge (that is to the switches Q1, Q1 ', Q2, and Q2') of the sub-modules can be generated by any of the MMC PWM techniques (discussed later) such that the

output voltage follows the desired sinusoidal waveform. The higher the number of sub-modules, the closer it follows the desired sinusoidal output voltage waveform, and thus reducing the output filter requirement. There is a design trade off between reducing harmonics (filter requirement) and the cost of additional sub-modules. This thesis considers four sub-modules for all simulation purposes. Output voltage for the topology (four sub-modules) is as shown in Fig.1.6. The relationship between the number of sub-modules and the number of voltage levels is as defined in equation1.1. Where N_{SM} is the number of sub-modules required per phase, while n_{level} is defined as the desired number of levels in the voltage.

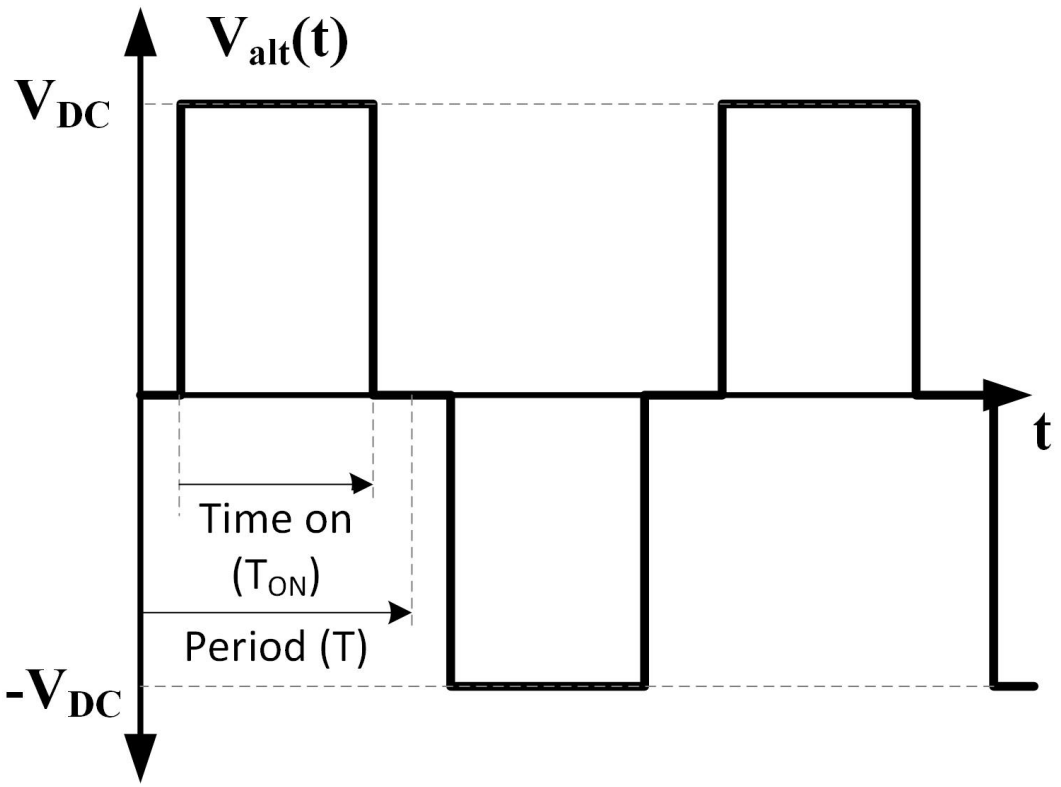

FIGURE 1.5: Primary Output Voltage

$$N_{SM} = (n_{level} - 1)/2 \tag{1.1}$$

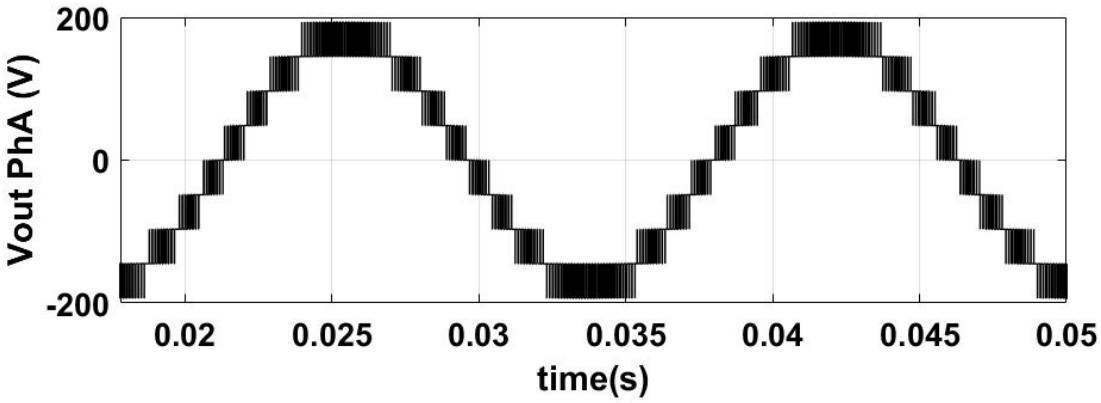

FIGURE 1.6: Expected Output Voltage for 9 level MMC

The output voltage of the sub-modules can be controlled by giving gate pulses as represented in table 1.1. The same is shown in figure 1.7.

TABLE 1.1: Sub-Module Full Bridge Voltage Output

Q1 Q1′ Q2 Q2′	Vsub-modules
1 0 0 1	Vc
0 1 1 0	-Vc
1 0 1 0	zero
0 1 0 1	zero

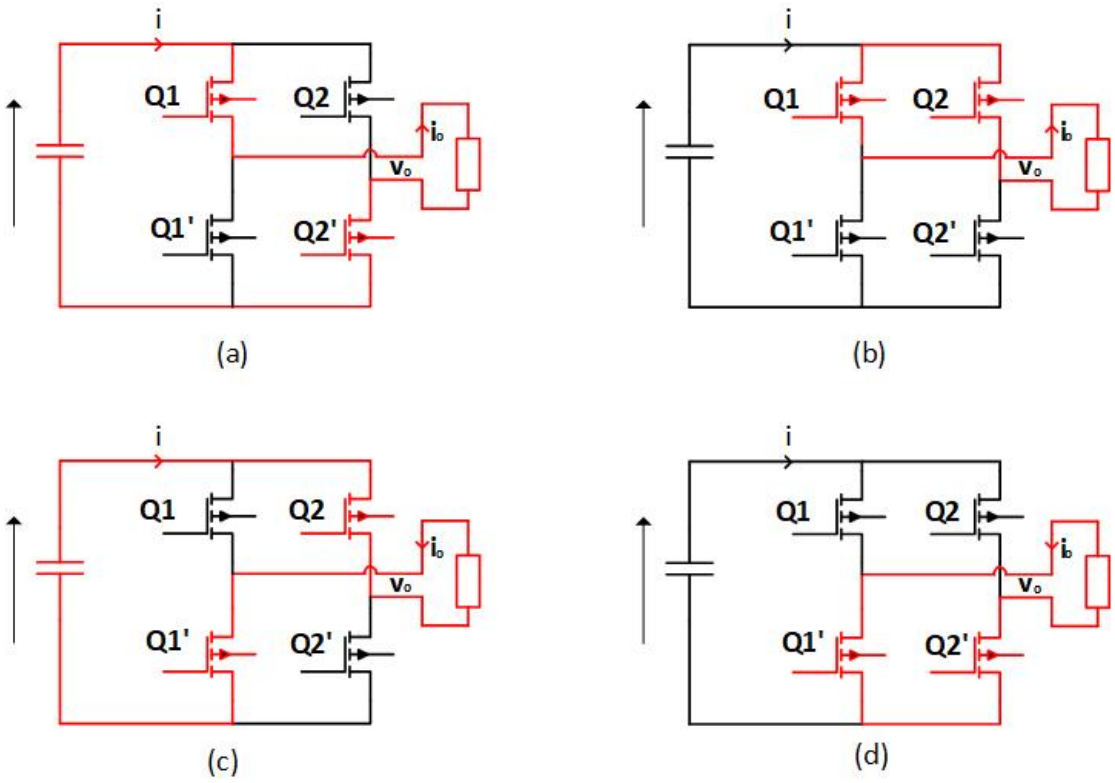

FIGURE 1.7: H Bridge Operation (a) Q1 and Q2′ ON (b) Q1 and Q2 ON (c) Q2 and Q1′ ON (d) Q1′ and Q2′ ON

1.4 Capacitor Balancing

There is no need for active capacitor balancing for this topology. This MMC topology has natural capacitor balancing properties, which results in fewer controls and reduced complexity when compared to other multi-level inverters with additional controls for voltage balancing.

Many traditional multi-level converters require an active voltage balancing scheme. The capacitance voltage of capacitors used in multi-level converters fluctuates depending on the current level, capacitance, and duration for which the capacitor was used in the cycle. There are different capacitor balancing schemes proposed in such multi-level converters, which make control difficult

and complex. The proposed topology doesn't need any such control for capacitor balancing and thus has less complex control.

1.5 Thesis Organization

Chapter one briefly describes the motivation and introduces the proposed MMC topology. Chapter two explains the various PWM techniques used for MMC and proposed a new PWM scheme. Chapter three shows all the simulation results of different PWM techniques and compares them with the proposed scheme. Chapter four explains the hardware used for verification of all the PWM techniques and presents all the hardware results. Chapter five introduces new hardware and PWM scheme that uses a combination of WBG and Si switches in the topology. Chapter six gives a brief comparison of the pros and cons of increasing and decreasing the number of sub-modules in the topology. Chapter seven concludes the thesis and discusses potential future work.

A significant part of this thesis is taken from my published work [13][14].

Chapter 2

PWM Techniques

There have been several PWM schemes proposed for multilevel converter in the literature. Most of these PWM schemes are based on sinusoidal pulse width modulation. In PWM for MMC, multiple carrier waves (triangular) are compared with a reference signal, generally sinusoidal, to generate gate pulses. Each carrier signal generates a gate pulse for a switch. When the reference signal is greater than the carrier signal, the switch is ON; otherwise, it is OFF. The complementary of that gate pulse is given to the complementary switch of the H-Bridge. Few of the several PWM schemes for MMC are nearest level modulation(NLM)[15][16] [17], Level Shifted PWM [18] [19] and Phase Shifted PWM [20]. These PWM techniques are briefly compared in the following sections. This chapter also presents a new PWM scheme[13] based on the level shifted PWM that will be introduced and compared at the end of the chapter. The PWM schemes are discussed as under:

2.0.1 Nearest-Level Modulation (NLM)

A staircase-like waveform with multiple output voltage levels can be synthesized to approximate a sine wave using the Nearest-Level Modulation (NLM) scheme. When the number of possible voltage levels is very high, NLM is a

quick and computationally easy way to generate the switching signals. It is useful when the number of sub-modules is very large, such as for high-voltage MMCs. The underlying principle of NLM is to simply use the nearest avialable (discrete) voltage level to generate the desired output voltage. When the desired output voltage is sinusoidal, the two levels adjacent to the desired output voltage are applied for different periods of time [16]. In such cases of sinusoidal output voltages, there is only one voltage transition (from one voltage level to the next) as opposed to the multiple transitions seen with level- or phase-shifted carrier modulation. As a result, it has much lower switching losses. However, as seen in Fig.2.1, during a particular half cycle, the modules are not equally utilized (SM1 and SM2 are used for longer time intervals compared to SM3 and SM4). Thus, it has the problem of some sub-modules being operated for a longer time and some for a shorter duration of time [17]. This can lead to unequal utilization of sub-modules, leading to unpredictable failures of some sub-modules, thereby demanding frequent maintenance.

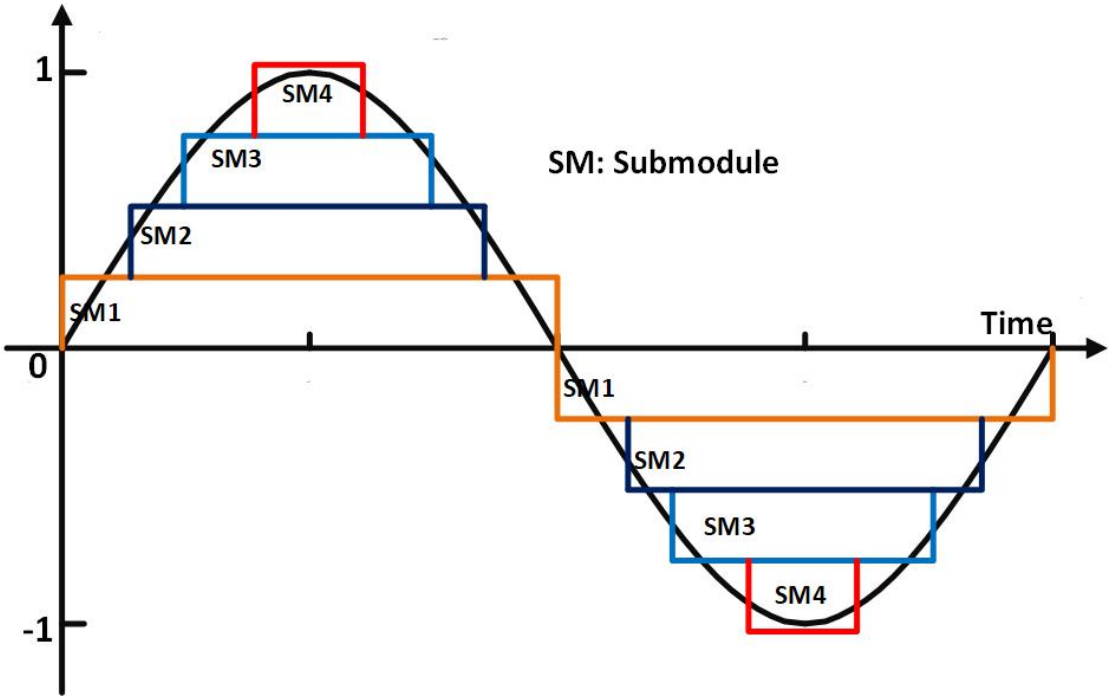

FIGURE 2.1: Nearest-Level Modulation

2.0.2 Level-Shifted PWM

Level-shifted PWM consists of multiple carrier waves displaced across different voltage levels [18] . Depending on how these carrier waves are displaced there are different types of level-shifted PWM modulation schemes available [19]. The carrier wave position is determined by addition or subtraction of amplitude of other carrier waves, as shown in Fig.2.2 where the 4 carrier waves are displaced and when these carrier waves are compared with the reference signal, then the corresponding sub-module is operated. This PWM technique has the disadvantage of unequal stress distribution of the switches across the sub-modules.

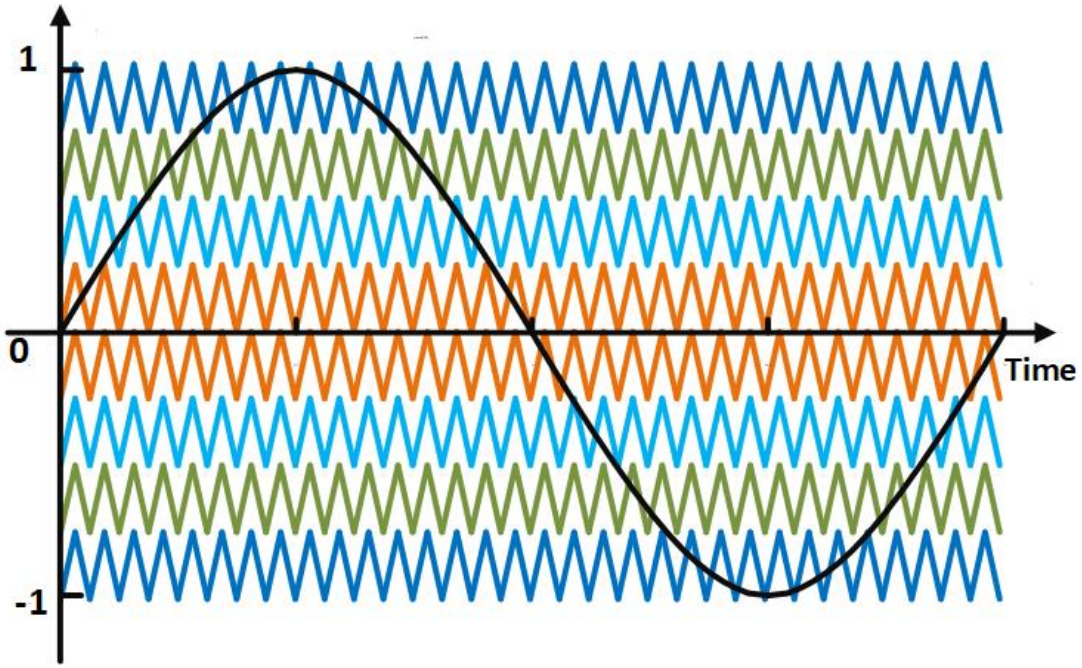

FIGURE 2.2: Level-Shifted Modulation

2.0.3 Phase-Shifted PWM

Phase-shifted PWM consists of carrier waves differing between the amplitude of ± 1 as shown in Fig.2.3. Each of these carrier waves is phase-shifted by an angle equal to (360/N) degrees, where N is the number of sub-modules in an arm [20]. In this case N is equal to 4 and all the carriers are phase-shifted by an angle of 90°. Unlike the other two above mentioned PWM schemes, this scheme has the advantage of equally distributing the switching stress across all the sub-modules. However, if we compare this with a level shifted or Phase shifted PWM in a fundamental cycle, the sub-modules switch throughout the time period as can be seen from Fig.2.3. Hence these sub-modules experience switching loss throughout the fundamental cycle hence contributing to a larger switching loss compared to other modulation techniques.

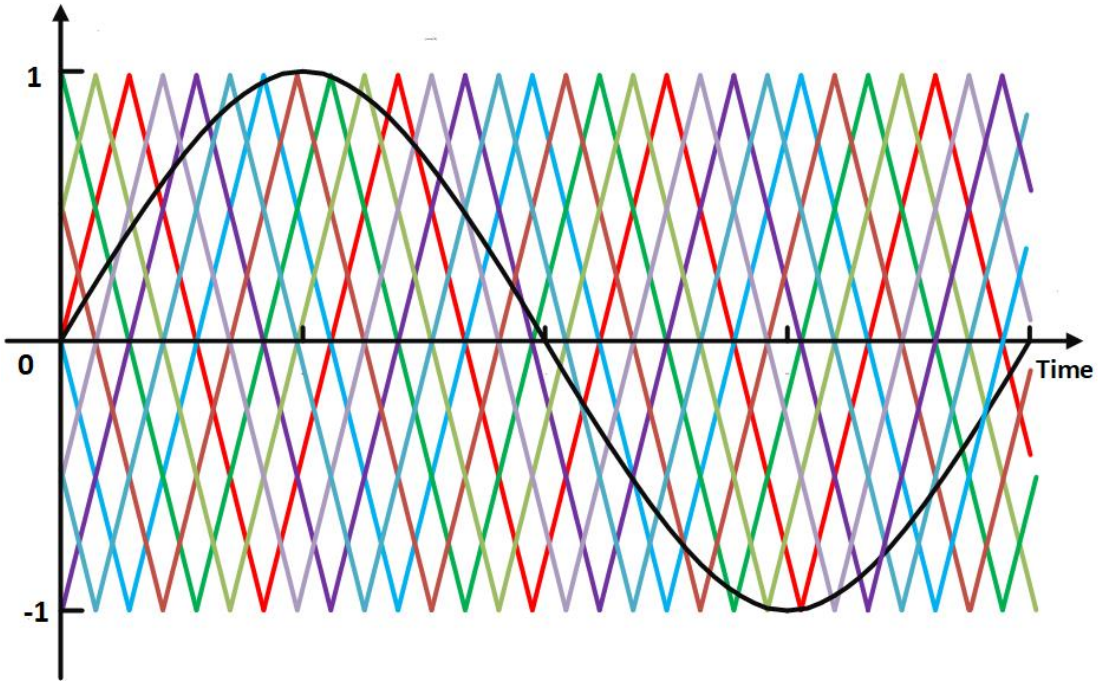

FIGURE 2.3: Phase Shifted Modulation

2.0.4 Hybrid PWM

Hybrid modulation schemes[21] use a combination of level and phase-shifted carriers. Carriers are divided into groups. Carriers within groups are at the same level, and each group is level-shifted. Carriers within each group are phase-shifted from each other. Fig.2.4 shows hybrid PWM with two groups of four carriers each. Hybrid PWM provides a trade-off between level and phase-shifted PWM in terms of loss, capacitor ripple, and equalization of module stress.

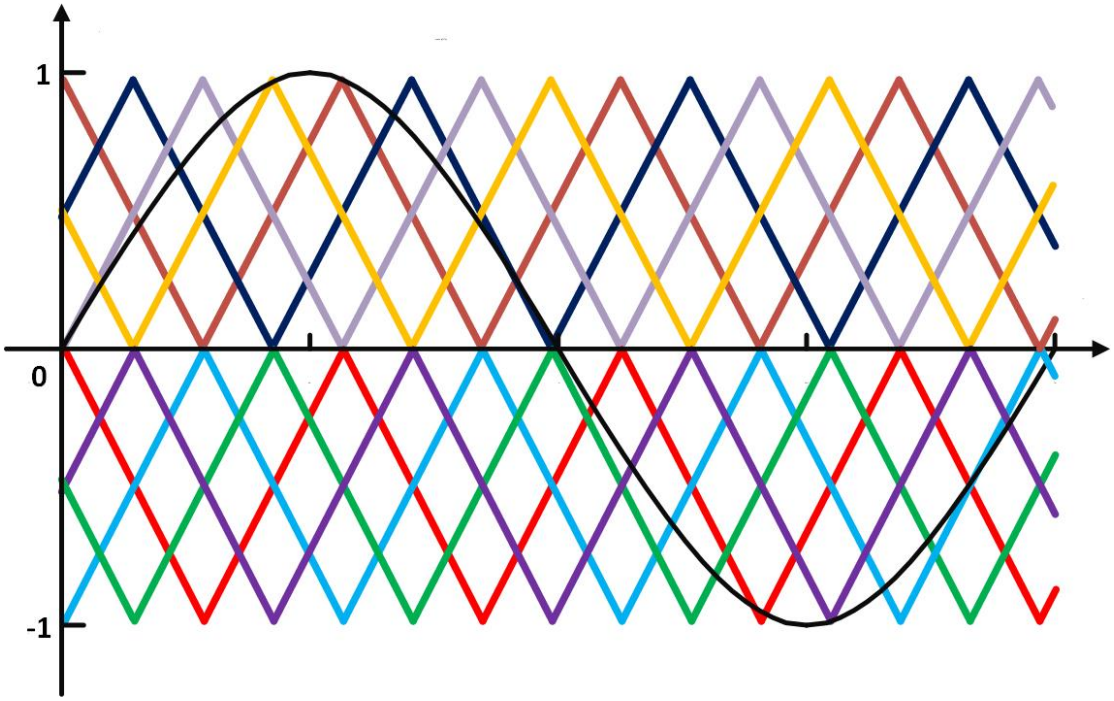

FIGURE 2.4: Hybrid PWM Modulation

2.1 Proposed PWM Scheme

In the proposed PWM scheme, level-shifted carriers are used, but carriers are re-assigned to modules after every quarter cycle to equalize module stresses without increasing switching loss. This ensures that the module which is turned 'on' first in the fundamental period is turned off first, in a "FIFO" approach. Gate signal reassignment is as shown in Fig.2.5. Since all the carriers are phase-aligned, this can be done without causing the output voltage to glitch.

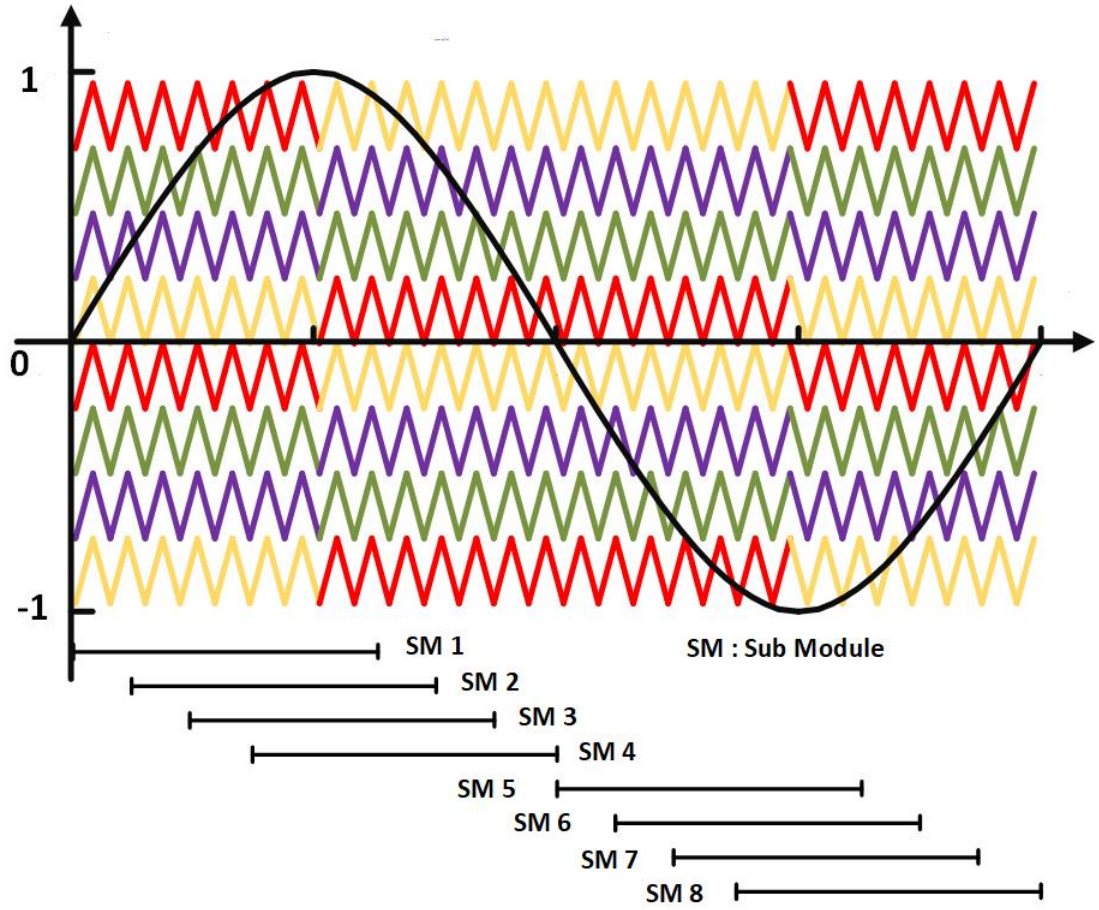

FIGURE 2.5: Proposed PWM Modulation

Fig.2.5 shows all the sub-modules being nearly equally utilized. The power flow in each sub-modules becomes very close with the increase in the number of sub-modules. In a realistic system with a high number of sub-modules, the power flow in each sub-modules are almost equal. This scheme makes the topology truly modular, as the module structure and the power flow are the same, thus avoiding any uneven failures of the sub-modules. The proposed PWM scheme is being verified in simulation as well as in the hardware in the following chapters.

Chapter 3

Simulation Results

3.1 Simulation Details

This chapter presents simulation results of all the PWM techniques discussed in the previous chapter. The simulation was done using MATLAB/Simulink. This chapter also briefly analyzes the losses across the power switches between different PWM schemes. Fig.3.1 shows the top-level block diagram of the simulation. In the figure, all the PWM gate pulses are coming from the control system blocks shown on the left side of the diagram. Fig.3.2 shows the overall topology for the three phase system. The left side of the figure shows the primary H-Bridge, receiving power from DC voltage source (PV/wind in a real system), while the rest of the system consists of sub-modules connected in series in each phase for the multi-level output voltage. Fig.3.3 shows the sub-module, which consists of a high frequency transformer, diode bridge rectifier, output H-Bridge, and gate & data collection signals. The simulation parameters are results are shown in the following sub-sections.

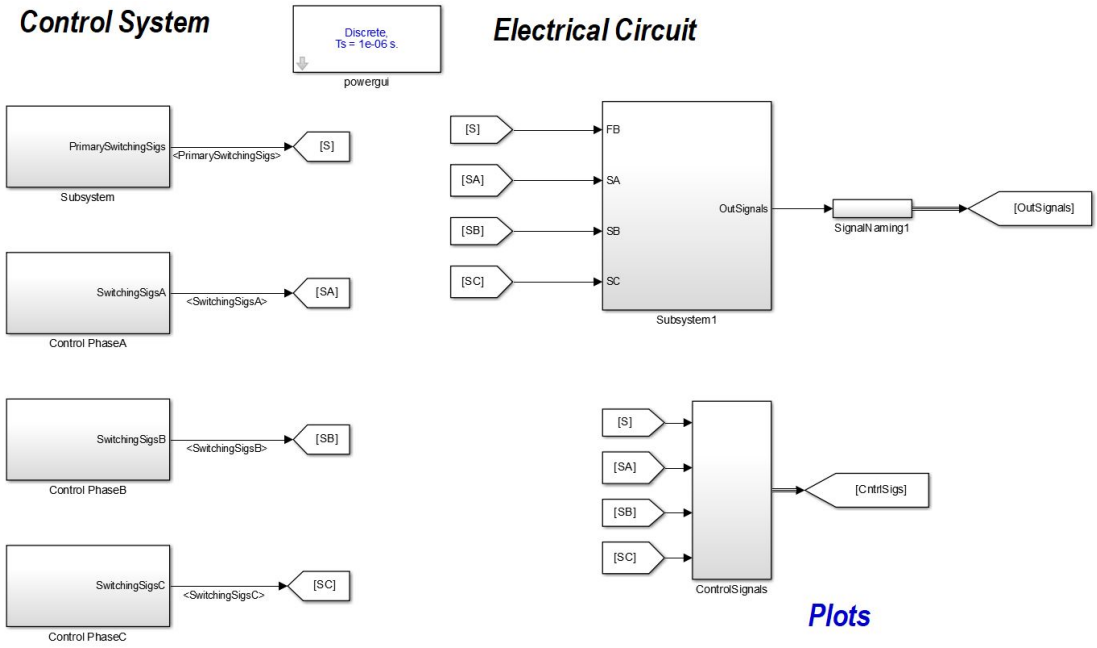

FIGURE 3.1: Top Level Simulation Diagram in Simulink

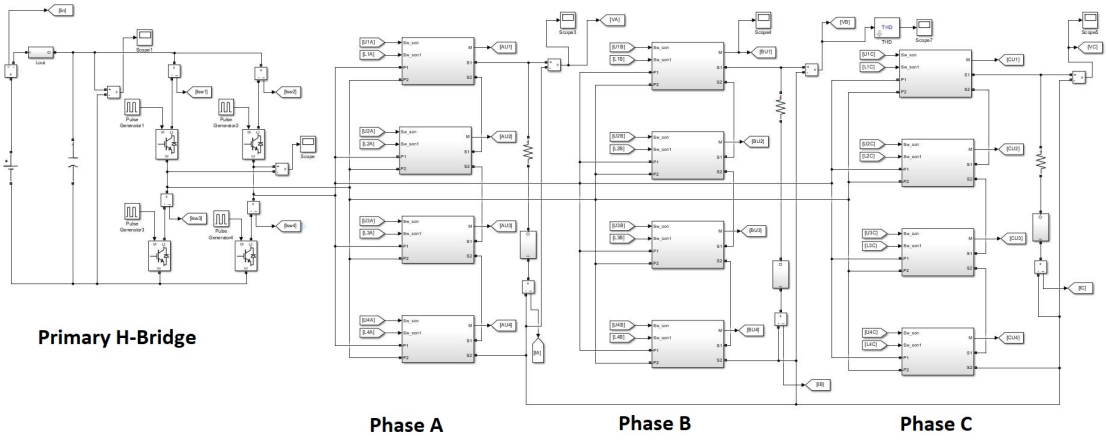

FIGURE 3.2: Simulation Overview: Electrical Circuit

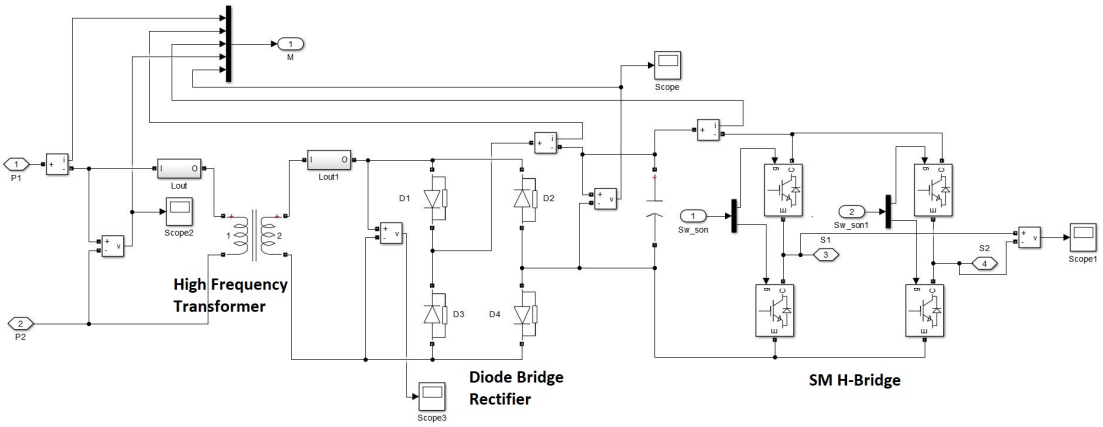

FIGURE 3.3: Simulation Sub-modules

Table 3.1 shows the simulation parameters used to determine the capacitor voltage ripple. It should be noted that capacitor voltage ripple for a modulation technique depends on various parameters, like capacitance value, arm inductance, number of sub-modules in a leg. The effect of different PWM techniques on the MMC with respect to output voltage, capacitor ripple, harmonics, and losses are discussed in the following subsections. The carrier frequency for the sub-module H-Bridge is 10 KHz.

TABLE 3.1: Simulation Parameters

Parameters	Values
No. of Sub-module per leg	4
Transformer frequency	20kHz
Transformer turns ratio	1:1
Duty Cycle	50%
Output frequency	60Hz
3 Phase power	1.27kW
Sub-module Capacitance	2.2mF
Arm Inductance	10mH
Input Voltage	50V
HFL Vmod	50V

3.1.1 Output Voltage and Current

Fig.3.4 and Fig.3.5 show the capacitor voltage V_c for the sub-modules, output voltage V_{out}, and the current I_{out} for phase A in the proposed PWM scheme, level-shifted, phase-shifted, and hybrid PWM.

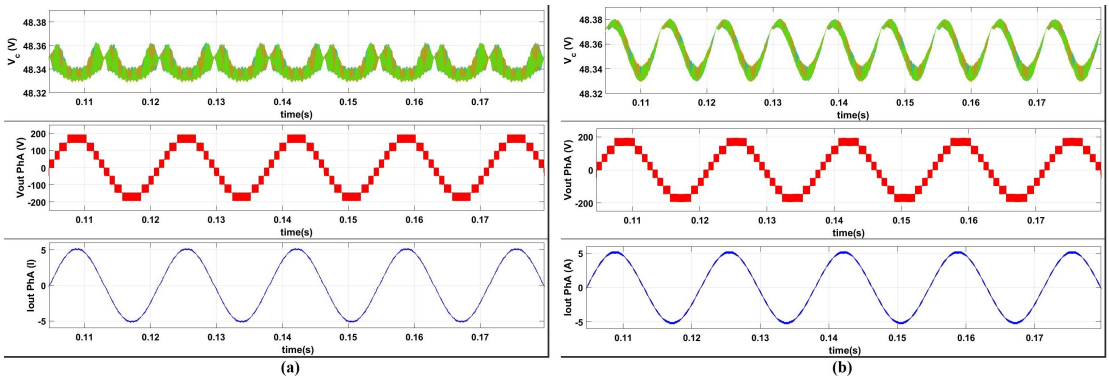

FIGURE 3.4: Simulation results for PWM schemes for the MMC showing sub-module capacitor voltage ripple (top trace), A-phase pole voltage (middle trace) and phase current (bottom trace): (a) Phase-shifted PWM (b) Hybrid PWM

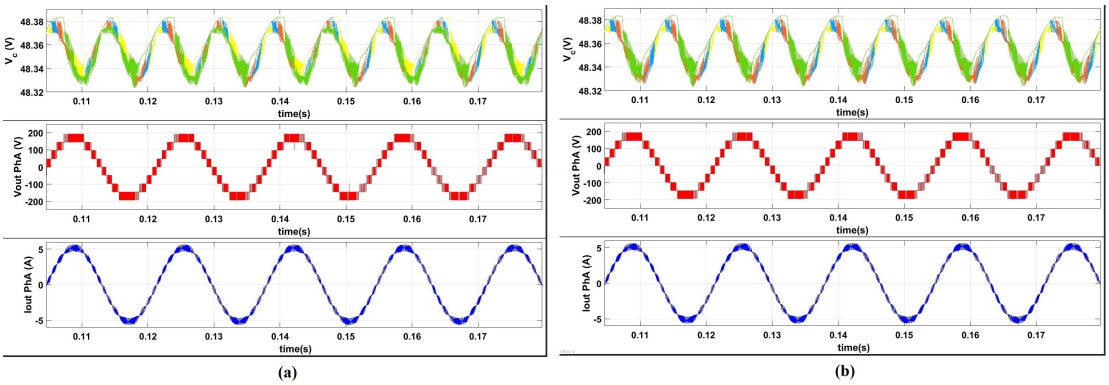

FIGURE 3.5: Simulation results for PWM schemes for the MMC showing submodule capacitor voltage ripple (top trace), A-phase pole voltage (middle trace) and phase current (bottom trace): (a) Proposed PWM scheme (b) Level-shifted PWM

3.1.2 Capacitor Voltages

Fig.3.6 and Fig.3.7 show the DC-link capacitor voltage of phase A for all sub-modules for different modulation types. The voltage ripple for phase-shifted PWM is minimum while that of the Modified level-shifted or level-shifted PWM is maximum.

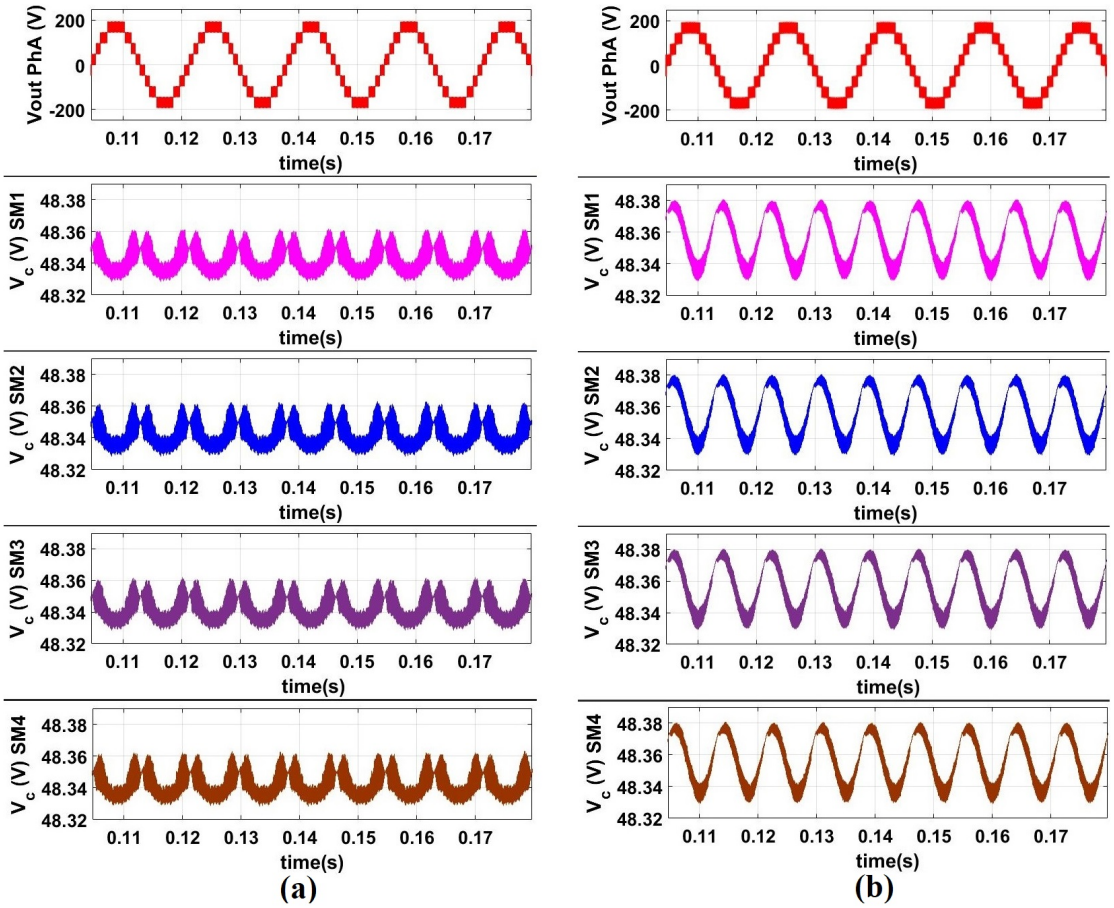

FIGURE 3.6: Simulation results for PWM schemes for the MMC showing submodule A-phase pole voltage (top trace), capacitor voltage ripple SM1-SM4 (Lower four trace respectively): (a) Phase-shifted PWM (b) Hybrid PWM

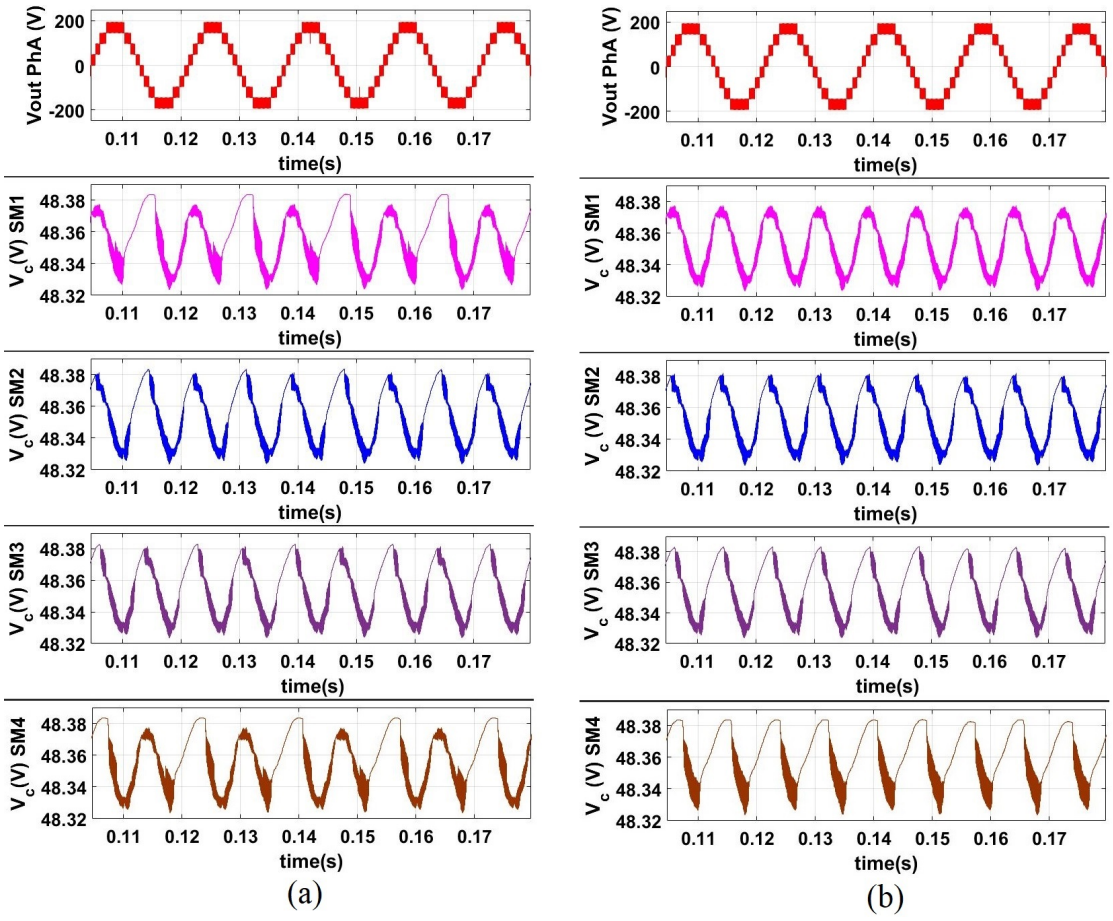

FIGURE 3.7: Simulation results for PWM schemes for the MMC showing submodule A-phase pole voltage (top trace), capacitor voltage ripple SM1-SM4 (Lower four trace respectively): (a) Proposed PWM scheme (b) Level-shifted PWM

3.1.3 NLM Modulation

The nearest level modulation shows the basic principles behind the operation of a multilevel converter. The NLM is the building block for several PWM schemes for multi-level converters.

3.1.4 Level-Shifted PWM

The gate pulses for the level-shifted PWM scheme is generated by 8 different carrier signals at 10 kHz. All the carrier signals switch at different times, thus the output voltage has a switching frequency of 10 kHz. The FFT analysis of the output voltage for the level-shifted PWM shows the signals at 10 kHz and its harmonics, as shown in Fig.3.8.

3.1.5 Phase-Shifted PWM

The gate pulses for the phase-shifted PWM scheme is generated by 8 different carrier signals at 10 kHz. All the carrier signals switch at the same time making the affecting output voltage switching signals as 8 times (for 4 sub-modules) that of the carrier frequency, thus the output voltage has a switching frequency of 80 kHz. The FFT analysis of the output voltage for the level-shifted PWM shows the signals at 80 kHz and its harmonics, as shown in Fig.3.8.

3.1.6 Hybrid PWM

The hybrid PWM is hybrid of the level and phase-shifted PWM as explained in chapter 2. For a four sub-module system, the effective switching will be four times that of the carrier frequency signal. FFT analysis of the output voltage for the hybrid PWM shows the signals at 40 kHz and its harmonics, as shown in Fig.3.8.

3.2 Proposed PWM Scheme

As explained in chapter 2, the proposed PWM scheme is similar to the level shifted PWM with the carriers being re-assigned to modules after every quarter cycle to equalize module stresses. Thus the effective PWM signal for the output voltage remains the same at 10 kHz, as that of the level shifted PWM. The FFT analysis of the Output voltage for the proposed PWM scheme shows the signals at 10 kHz and its harmonics, as shown in Fig.3.8.

3.3 Harmonics and FFT Analysis of Output MMC Voltage

Fig.3.8 shows the FFT analysis for the output voltage with different PWM techniques. The phase-shifted PWM technique has the lowest sub-harmonic content of all the PWM techniques discussed here.

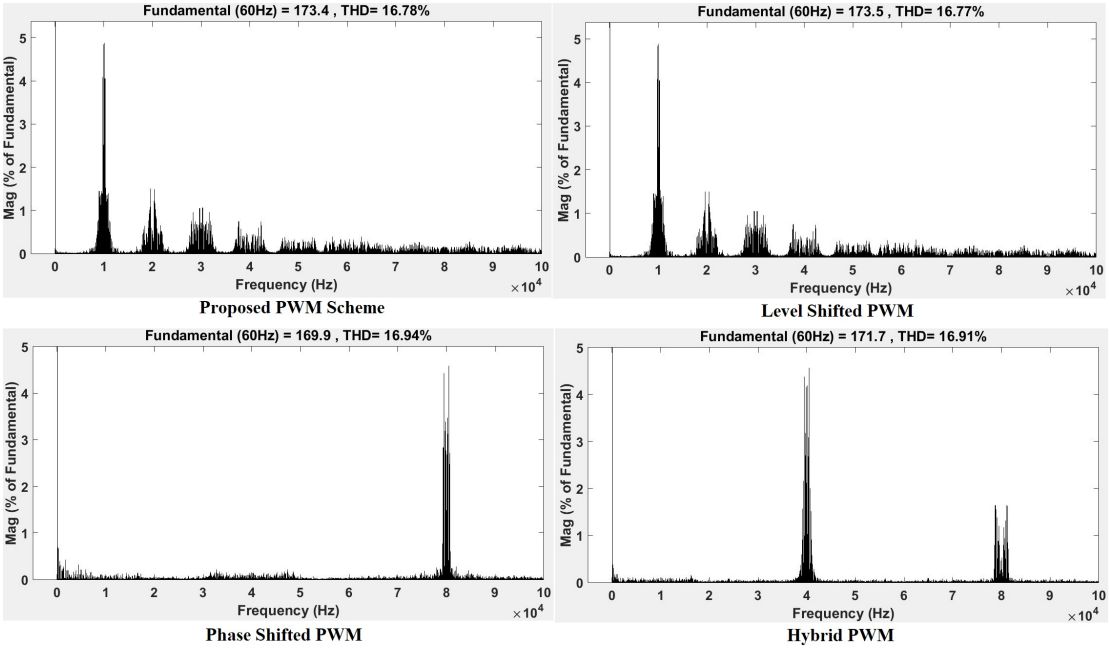

FIGURE 3.8: Output Voltage FFT Analysis 100k Hz window

3.4 Switching Losses

The two components of the losses in the switch are conduction (turn-on) loss and switching loss. Conduction loss is independent of the PWM techniques while switching loss depends greatly on the selected PWM technique. The switching loss is observed to be the highest in phase-Shifted PWM followed by hybrid PWM technique and the least in level-Shifted & modified level-shifted PWM.

Loss analysis is done using SIMULINK as described previously [22] and the obtained losses are shown in table 3.2 and compared in Fig. 3.9. The model consists of IGBT and Diode losses. IGBTs losses include switching and conduction loss, while diode losses consist of reverse recovery and conduction loss. The obtained losses are the sum of all the losses incurred in the switches of the sub-modules of MMC. The losses incurred in the primary converter is not considered in the analysis as it is equal in all PWM techniques and is mainly due to conduction loss of switches. The total output power of the three-phase converter in the simulation was 1.36 kW.

TABLE 3.2: Losses for Different PWM Techniques

PWM Technique	Semiconductor losses over all the sub-modules (W)
NLM	50
Level-shifted	70
Phase-shifted	210
Proposed PWM Scheme	70

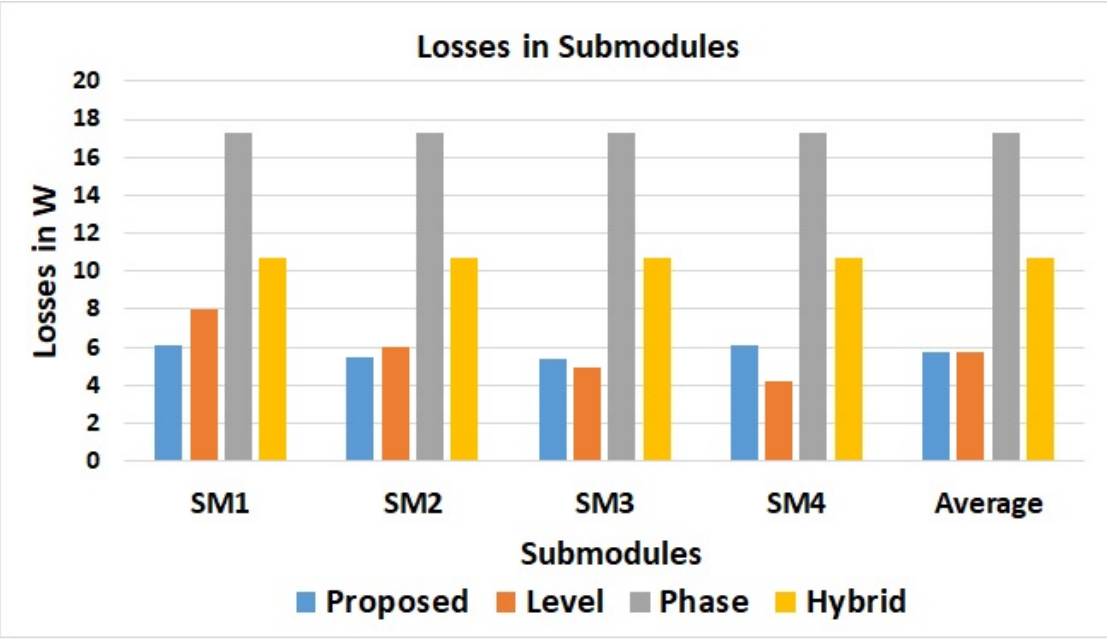

FIGURE 3.9: Losses for different PWM Modulation

Chapter 4

Hardware Results with the Proposed-PWM Scheme

4.1 Hardware Details

This chapter gives a detailed description of the hardware to support the simulation results for the proposed PWM along with the other PWM techniques. To verify the PWM techniques, the hardware is similar to 9-level cascaded H-Bridge multilevel converter for the lab test as shown in Fig.4.1. The hardware consists of four H-Bridges with their output connected in series. The input to each H-bridge is given by an isolated DC power supply as shown. It is really important that all the DC power supplies and the gate drives remain isolated from each other.

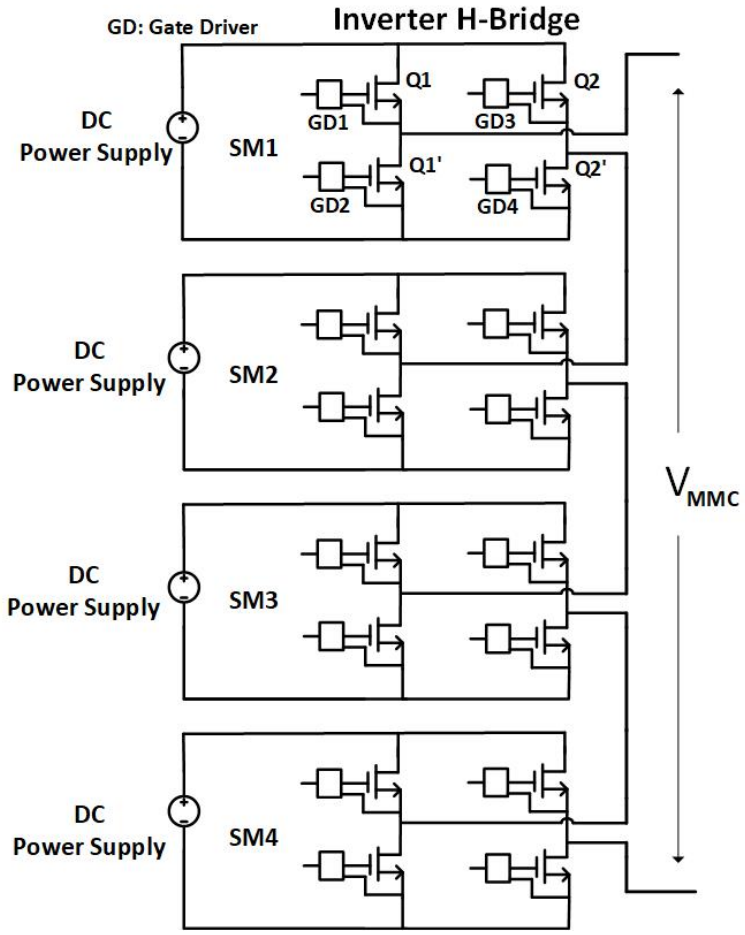

FIGURE 4.1: Hardware Setup Block Diagram

The DC-link input to the four H-Bridges is supplied by four isolated DC power supply as shown in Fig.4.2. Fig.4.3 shows the gate pulses board and one of the H-bridge from the top. The hardware results are presented and discussed in the upcoming sub-sections.

Overall Setup *CHB inverter*

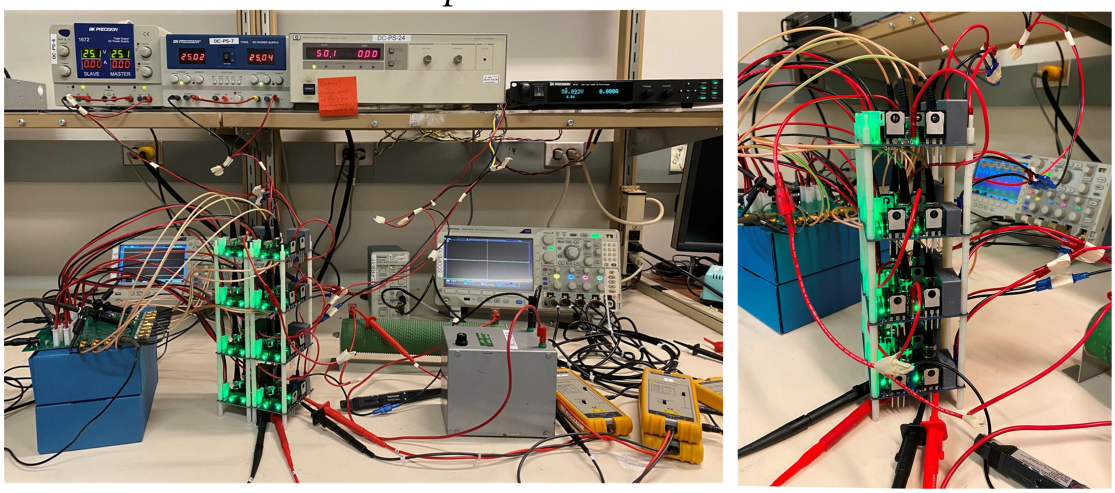

FIGURE 4.2: Hardware Setup of 9-level CHB inverter

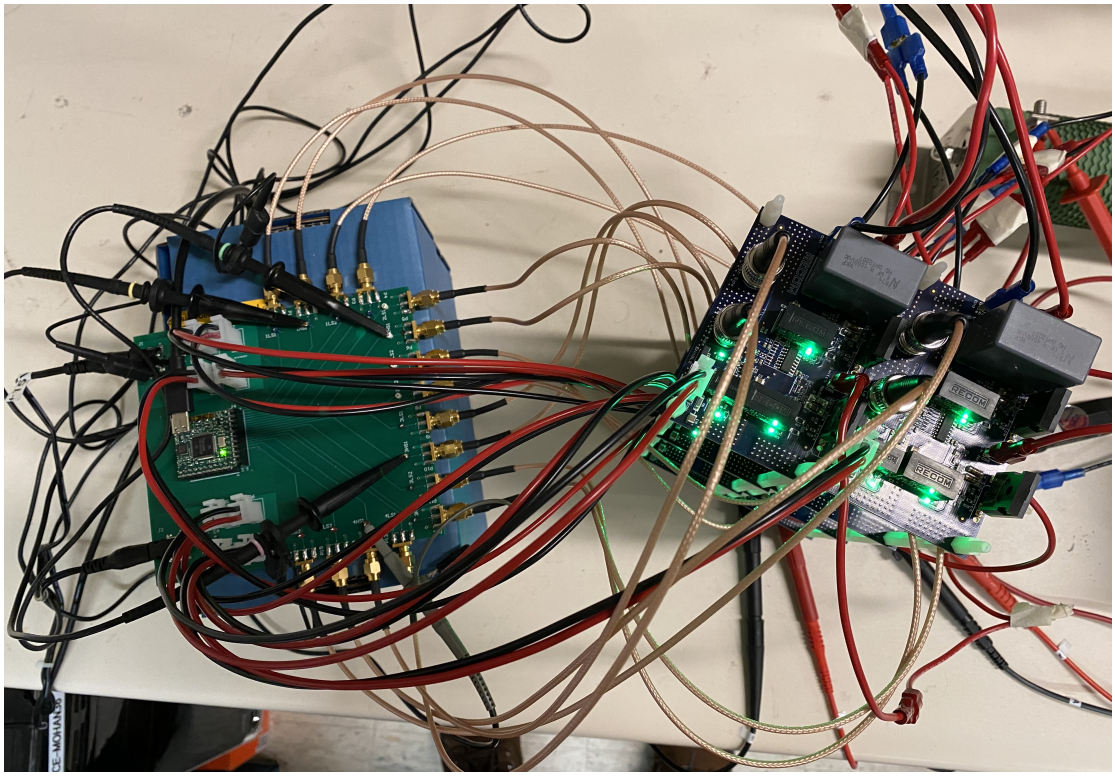

FIGURE 4.3: Hardware Setup of Gate Pulses

4.1.1 NLM Modulation

Nearest Level Modulation shows the basics of multilevel converter operation. Fig. 4.4 and Fig.4.5 show the gate pulses for top side switches for the positive half of the output signal. Fig.4.6 and Fig4.7 show the output voltage and current, along with gate pulses for one of the sub-modules.

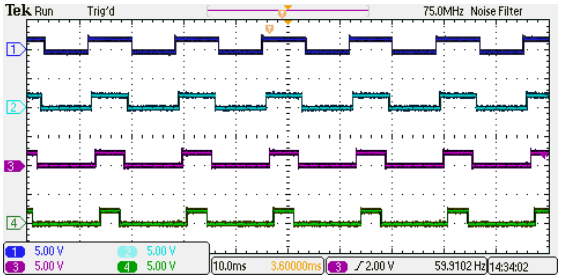

FIGURE 4.4: NLM Gate Pulses

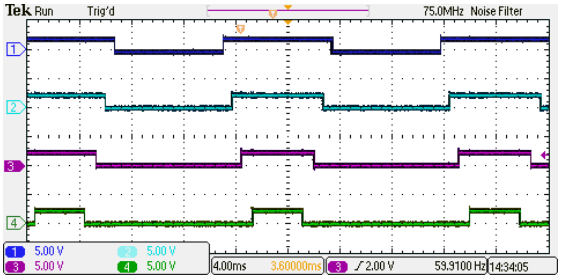

FIGURE 4.5: NLM Gate Pulses Zoomed

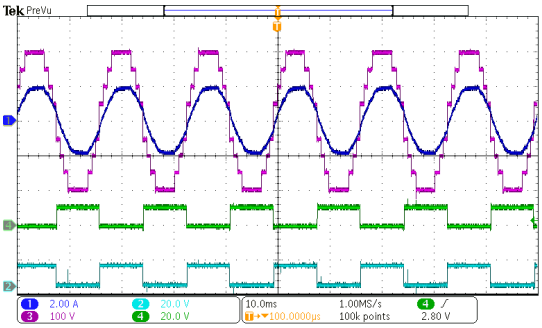

FIGURE 4.6: NLM Output

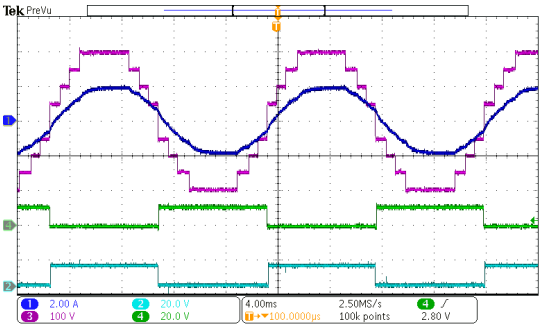

FIGURE 4.7: NLM Output Zoomed

4.1.2 Level-Shifted PWM

Level-Shifted Modulation looks similar and comparable to the 3-level PWM switching, except it has multiple carriers depending on the number of levels required. Fig. 4.8 and Fig.4.9 show the gate pulses for top side switches for the positive half of the output signal. Fig.4.10 and Fig 4.11 show the output voltage and current, along with the gate pulses for one of the sub-modules.

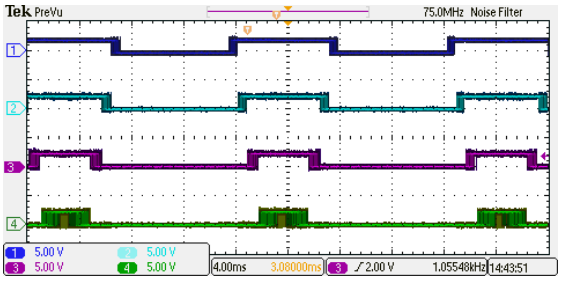

FIGURE 4.8: Level-Gate Pulses

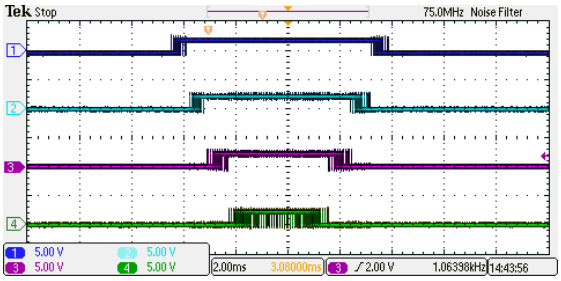

FIGURE 4.9: Level-Gate Pulses Zoomed

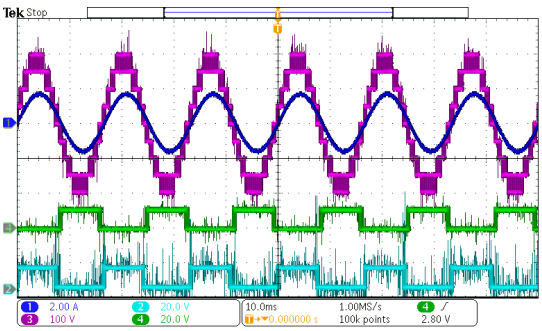

FIGURE 4.10: Level-Shifted Output

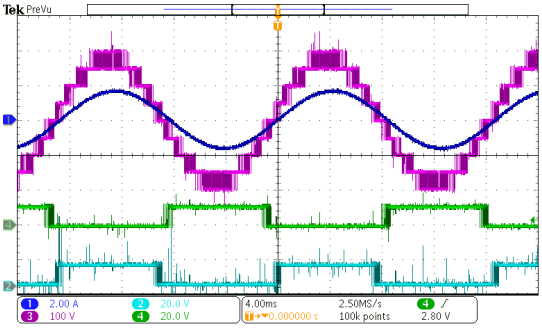

FIGURE 4.11: Level-Shifted Output Zoomed

4.1.3 Phase-Shifted PWM

Phase-Shifted Modulation has their carrier pulses going from zero to one, with their carriers phase shifted depending on the number of levels required. Fig.4.12 and Fig.4.13 show the gate pulses for top side switches for the positive half of the output signal. Fig.4.14 shows the output voltage and current, along with gate pulses for one of the sub-modules.

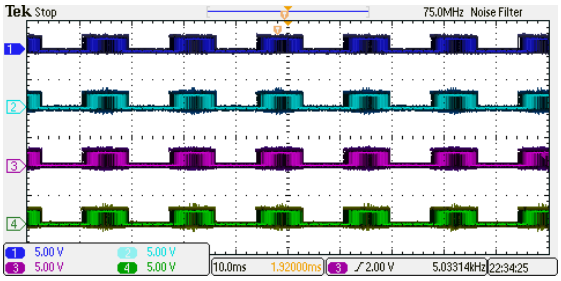

FIGURE 4.12: Phase-Gate Pulses

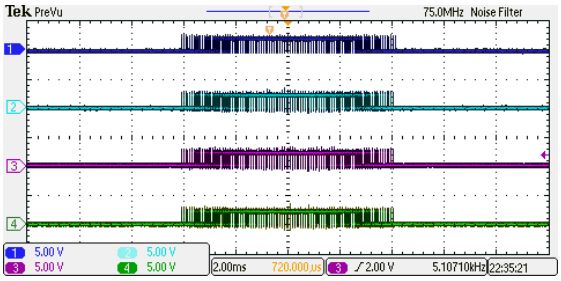

FIGURE 4.13: Phase-Gate Pulses Zoomed

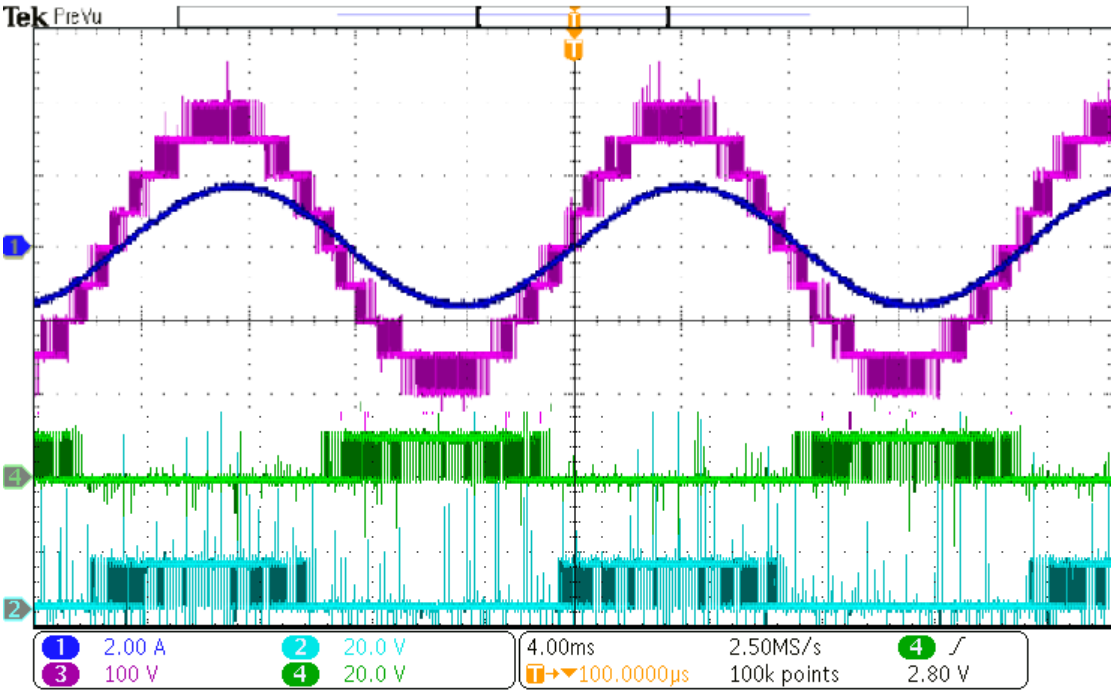

FIGURE 4.14: Phase-Shifted Output

4.2 Proposed PWM Scheme

Proposed Modulation uses a concept similar to that of level shifted, except it works in FIFO (first in, first out) fashion. The sub-module which starts conducting first, stops first. Fig.4.15 and Fig.4.16 show the gate pulses for top side switches for the positive half of the output signal. Fig.4.17 and Fig.4.18 show

the output voltage and current, along with the gate pulses for one of the sub-modules.

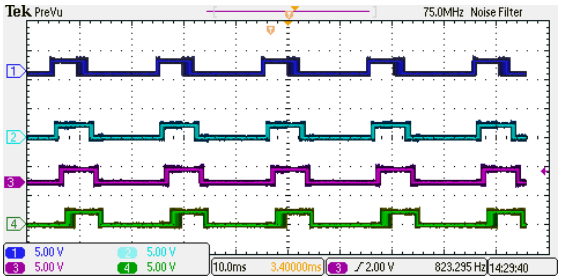

FIGURE 4.15: Proposed Gate Pulses

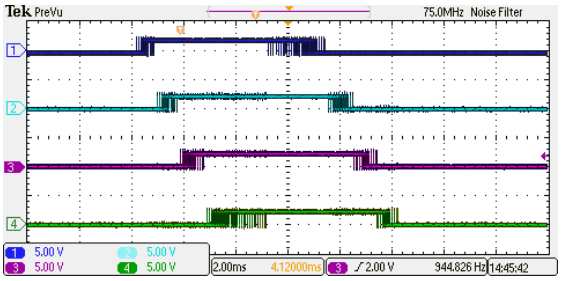

FIGURE 4.16: Proposed Gate Pulses Zoomed

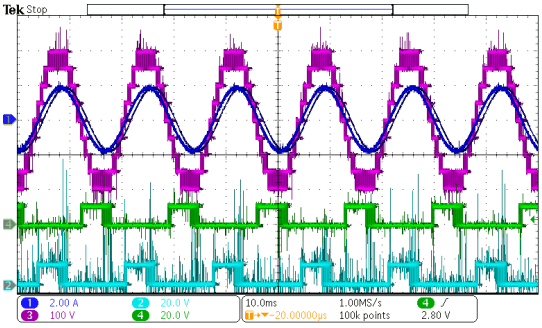

FIGURE 4.17: Proposed PWM Output

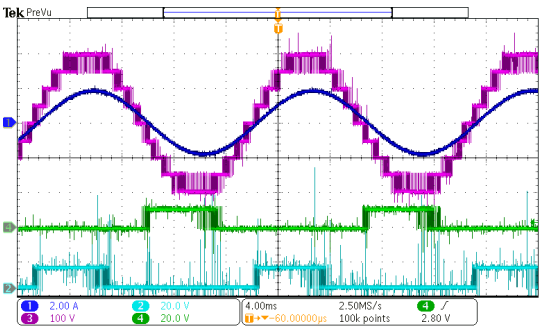

FIGURE 4.18: Proposed PWM Output Zoomed

Chapter 5

Hardware and PWM Scheme for WBG+Si System

This chapter proposes an new hardware topology along with it's corresponding PWM scheme for WBG+Si based system.

5.1 WBG+Si based proposed MMC

In the proposed MMC topoloy one of sub-modules switches are replaced with WBG (SiC/GaN) switches, while the remaining sub-modules still have traditional 'Si' switches as shown in Fig.5.1. The SiC/GaN sub-module switches all the time with a carrier switching frequency of 10 kHz while the 'Si' sub-modules are switched at line frequency (at 60 Hz) similar to the NLM based approach. However, compared to the traditional NLM based PWM scheme this modified approach makes sure all the sub-modules are equally utilized [13]. This ensures that almost all switching happens in SiC/GaN devices. Since the switching losses in these devices are low, the total switching loss in the system is less. Also, as only one sub-module is replaced with the SiC/GaN switches the cost of the overall system remains the same. The gate signal for the SiC/GaN

and 'Si' sub-modules are as shown in Fig.5.2. The figure is a time representation of all the gate pulses given to the sub-modules of one of the phases. The gate pulses are placed on top of other gate pulses in the same sequence as it affects the output phase voltage.

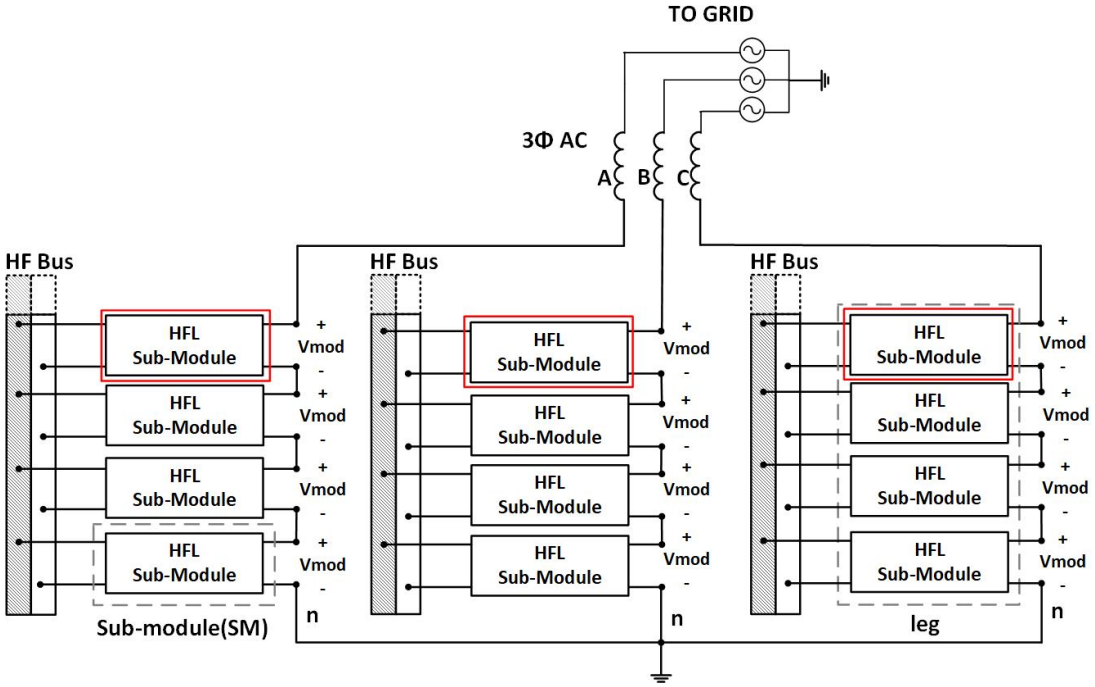

FIGURE 5.1: Proposed Modulation

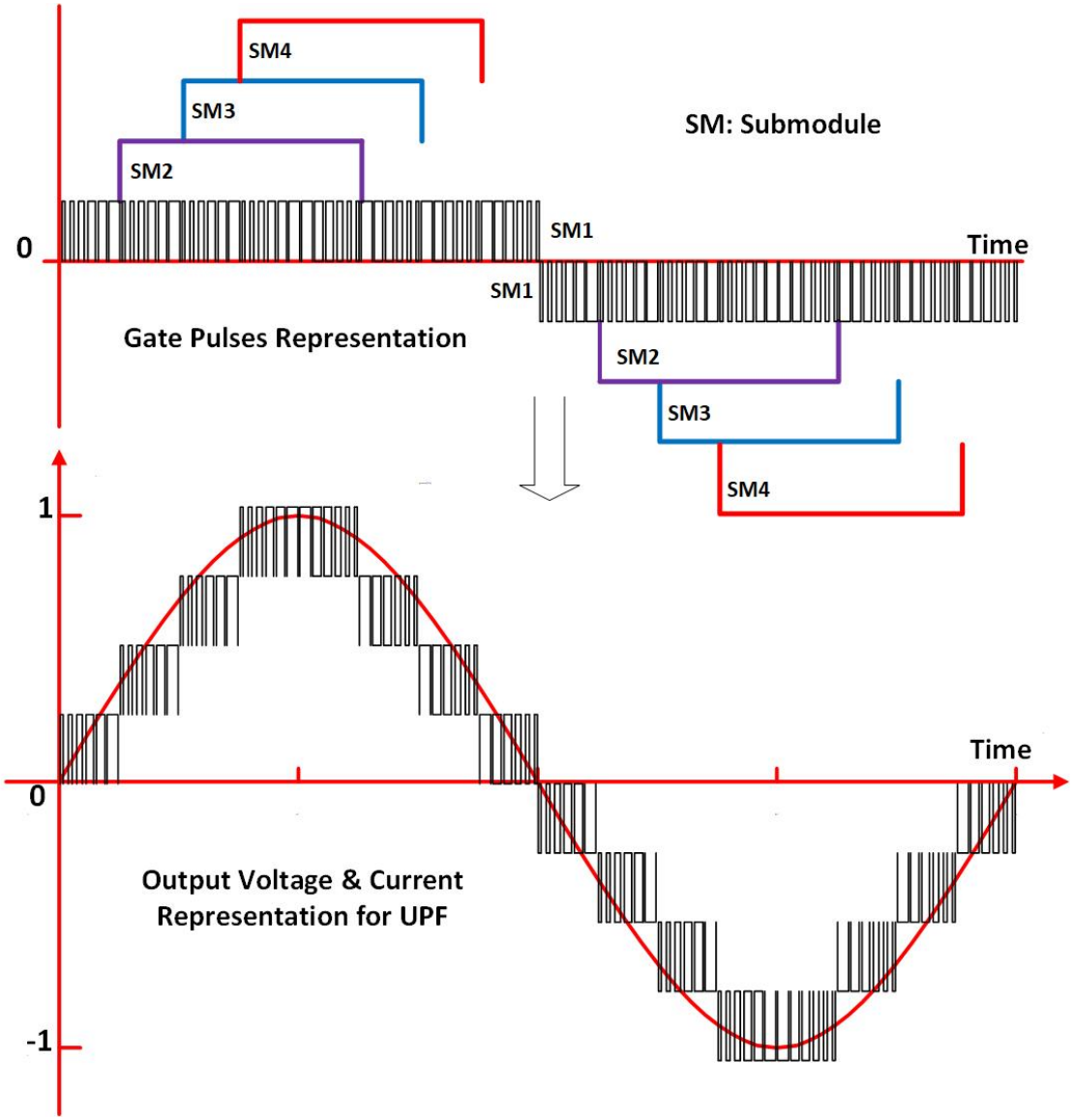

FIGURE 5.2: Proposed Modulation for GaN+Si Topology

5.1.1 Proposed PWM Scheme for WBG+Si

In the proposed PWM scheme[14] for WBG+Si, a composite reference signal is given to the SM-1 with the GaN devices while driving the rest of the sub-modules (SM-2 to SM-4) with low frequency quasi-square wave gate pulses,

as shown illustratively in Fig.5.2. The composite signal for the GaN SM is created by combining several quarter-wave sinusoid as shown in Fig.5.3, such that the final average output waveform is a sinusoid of the fundamental frequency. Note that the modulation signal has quarter-wave as well as half-wave symmetry, and hence, defined only for the interval $[0, \pi/2]$ as below:

$$d_1 = \begin{cases} 4m\sin\theta, & 0 \le \theta \le \theta_1 \\ 4m\sin\theta - 1, & \theta_1 \le \theta \le \theta_2 \\ 4m\sin\theta - 2, & \theta_2 \le \theta \le \theta_3 \\ 4m\sin\theta - 3, & \theta_3 \le \theta \le \pi/2 \end{cases} \qquad \theta_x = \begin{cases} \theta_1 = \sin^{-1}\left(\frac{0.25}{m}\right) \\ \theta_2 = \sin^{-1}\left(\frac{0.5}{m}\right) \\ \theta_3 = \sin^{-1}\left(\frac{0.75}{m}\right) \end{cases} \tag{5.1}$$

$$d_2 = \begin{cases} 1, & \theta_1 \le \theta \le \pi - \theta_3 \\ 0, & \text{elsewhere} \end{cases} \quad d_3 = \begin{cases} 1, & \theta_2 \le \theta \le \pi - \theta_2 \\ 0, & \text{elsewhere} \end{cases} \quad d_3 = \begin{cases} 1, & \theta_3 \le \theta \le \pi - \theta_1 \\ 0, & \text{elsewhere} \end{cases} \tag{5.2}$$

Also, it is worth noting that all the sub-modules with 'Si' devices are pulsed to have equal power utilization.

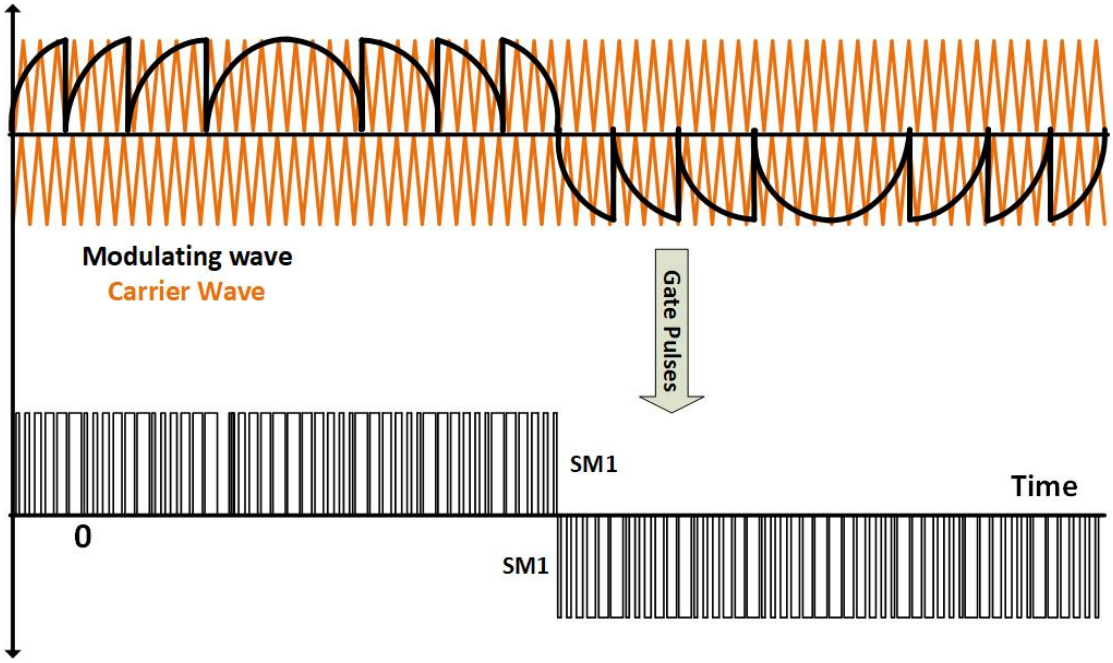

FIGURE 5.3: Proposed Modulation for GaN Sub-module

5.1.2 Hybrid CHB Inverter

In the proposed power stage [14], one of the sub-modules in the topology is being replaced by GaN devices while the remaining SMs use Si devices. In the proposed PWM scheme, detailed in the previous section, the HF PWM will be given to the sub-module with GaN devices, while the remaining sub-modules will see line frequency switching. To verify the hardware and PWM topology for WBG+Si based system, cascaded H-Bridge system explained in Chapter 4 is modified as shown in Fig.5.5. This will increase the efficiency of the system, as GaN has less switching and on-state losses as compared to 'Si' devices. The overall hardware considered in the work has 4 sub-modules, with one sub-module carrying GaN devices as shown in Fig.5.4 and Fig.5.5.

Overall Setup *CHB inverter*

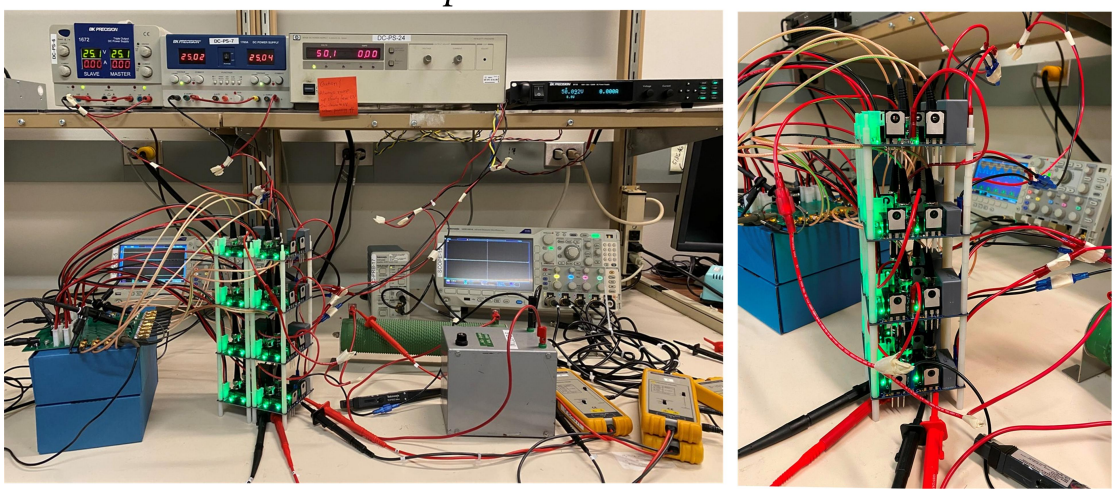

FIGURE 5.4: Hardware Setup of 9-level CHB inverter

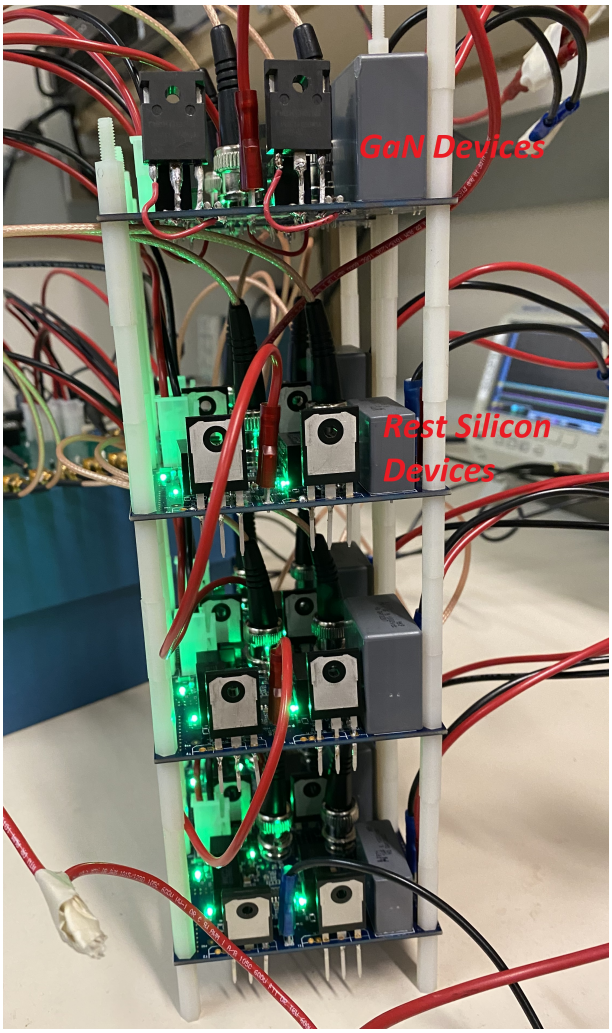

FIGURE 5.5: Sub-Modules with GaN

5.2 Simulation & Hardware Results

The simulation for the proposed CHB inverter topology for WBG+Si was done using Matlab/Simulink. Fig.5.8 shows the output voltage for a nine level converter. The parameters for the simulation are shown in Table 3.1. A hardware prototype for a single phase is developed to verify the simulation and the PWM concept as shown in Fig.5.4. Hardware is similar to a 9-level cascaded H-Bridge multi-level converter for the lab test. The DC-link input to the four H-Bridge

is supplied by four isolated DC power supply as shown in Fig.5.4. The CHB inverter in Fig.5.5 shows all the H-Bridges connected and stacked together to give multi-level voltage output. An RL load with the resistance of 100 ohms and inductance of 100 mH was used for the phase. The gate pulses for the high side switches for the positive half cycle and the output voltage and current are shown in Fig.5.7. The hardware results of the proposed gate pulses are shown in Fig.5.9 and Fig.5.10. The output voltage and current for the proposed PWM scheme for GaN+Si hardware are as shown in Fig.5.11 and Fig.5.12.

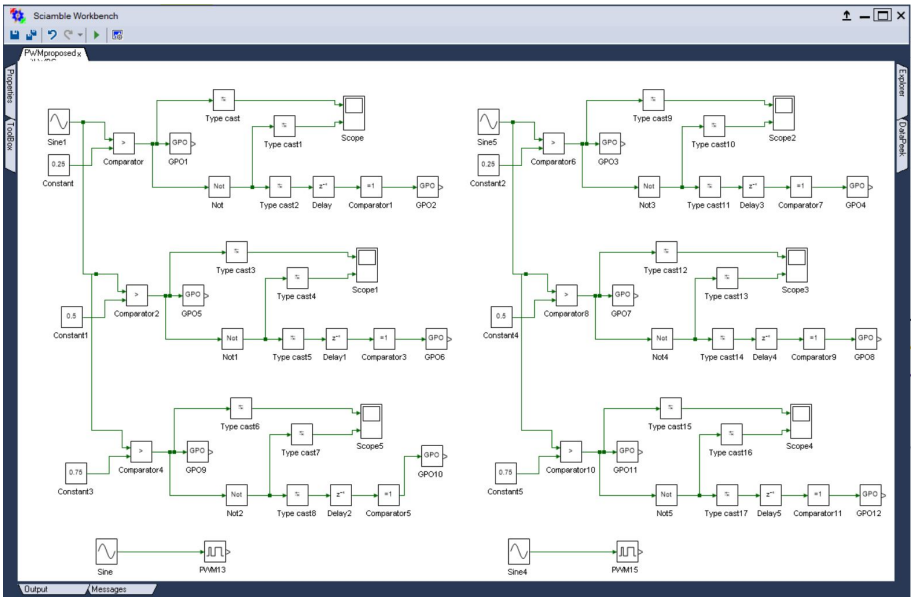

FIGURE 5.6: Gate Pulse Generation through Sciamble

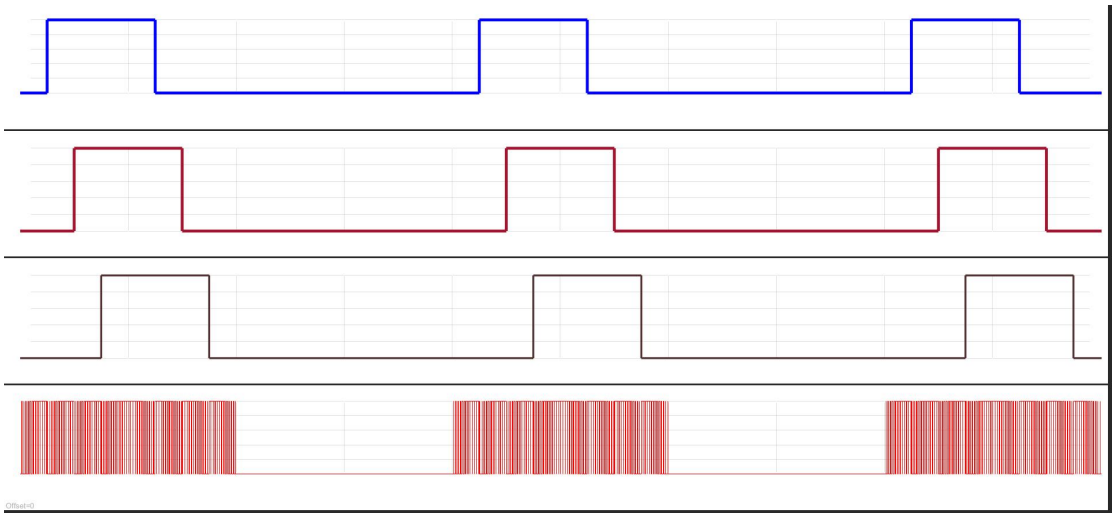

FIGURE 5.7: Simulation: Gate Pulses for Hybrid GaN+Si devices

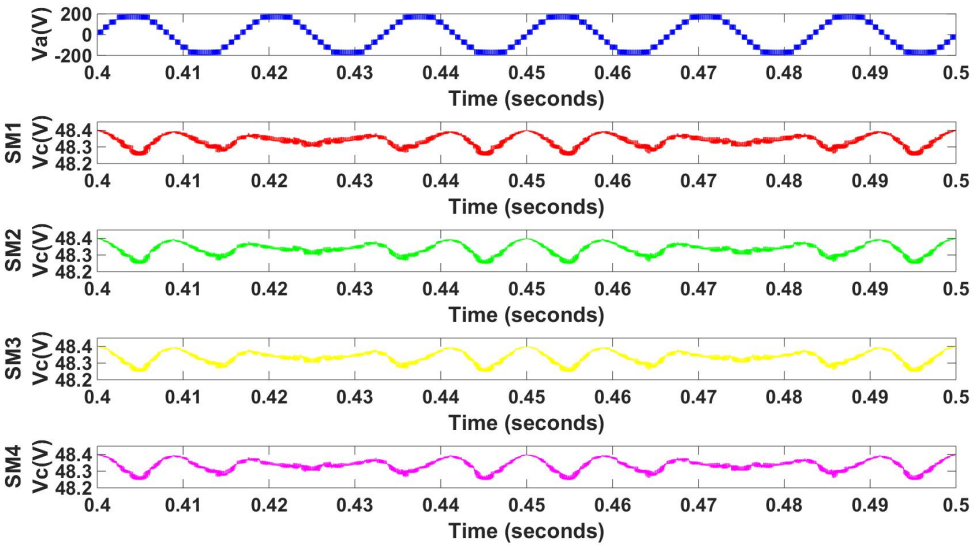

FIGURE 5.8: Simulation results for Proposed PWM Scheme for GAN+Si MMC showing sub-module A-phase pole voltage (top trace), capacitor voltage ripple SM1-SM4 (Lower four trace respectively)

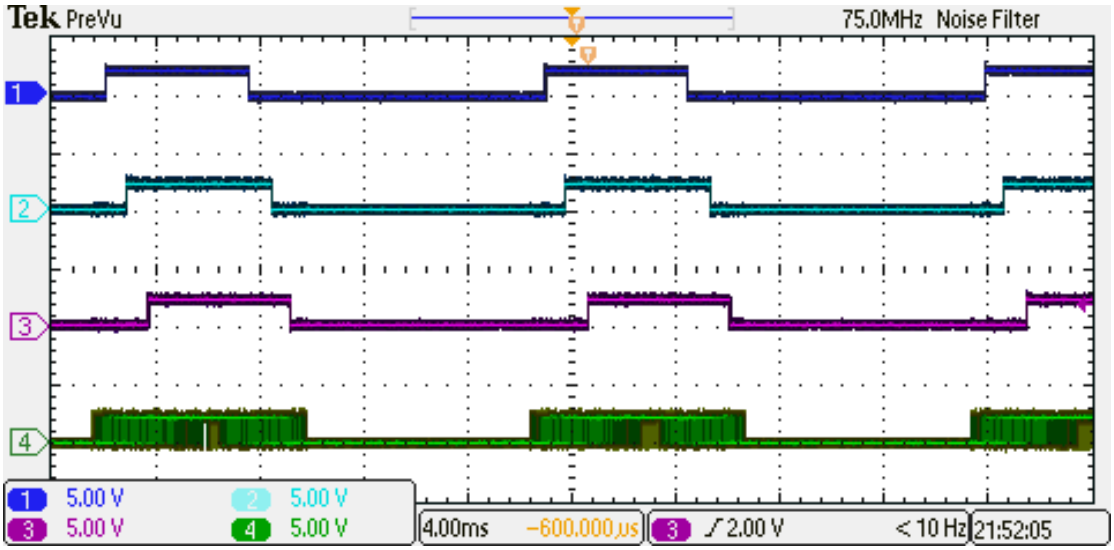

FIGURE 5.9: Proposed Pulses WBG+Si Gate Pulse

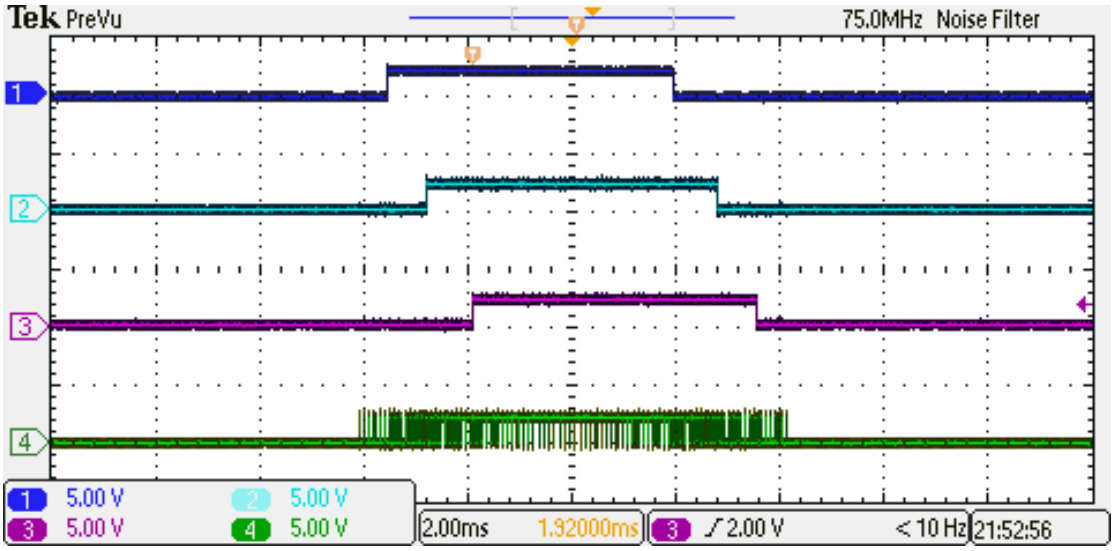

FIGURE 5.10: Proposed Pulses WBG+Si Gate Pulse Zoomed

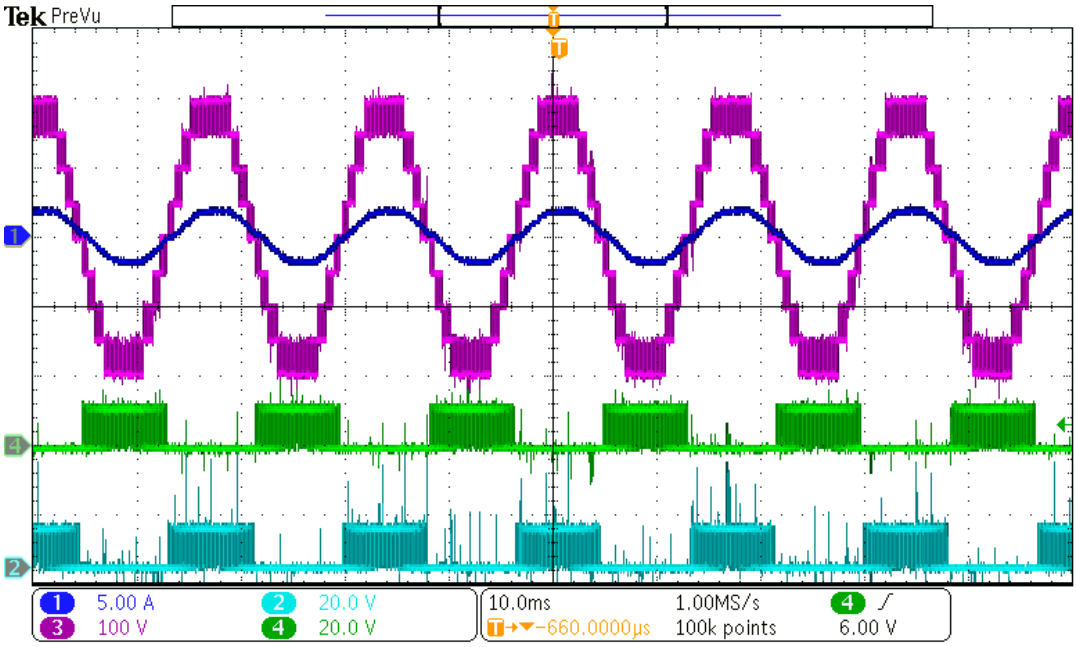

FIGURE 5.11: Proposed Pulses WBG+Si Output

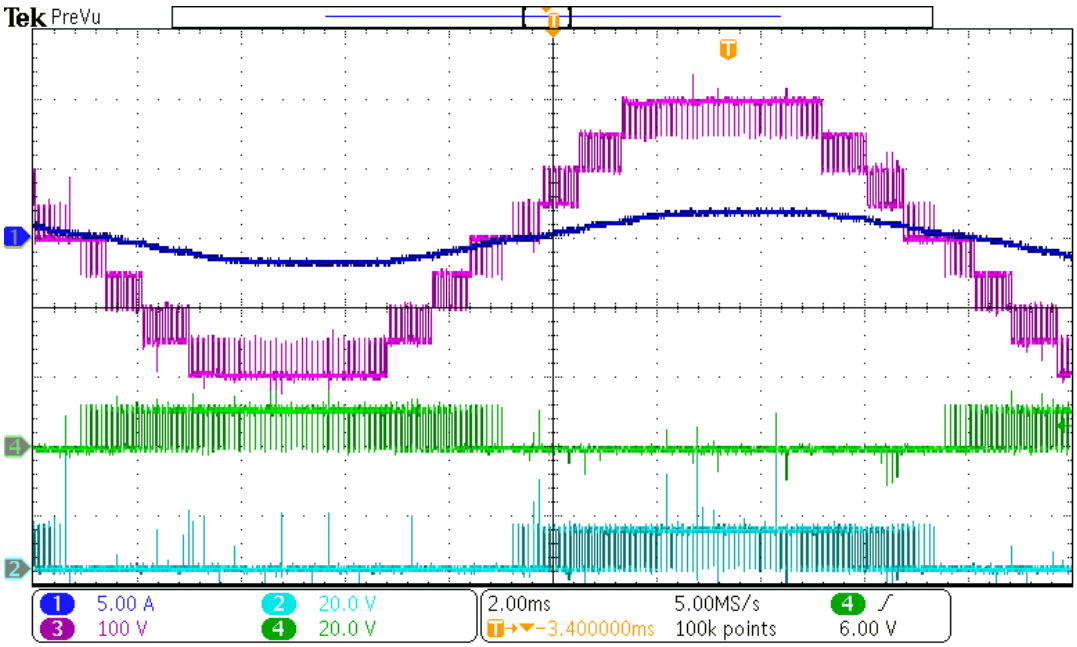

FIGURE 5.12: Proposed Pulses WBG+Si Output Zoomed

5.3 Switching Lossess

WBG devices has different structure and material composition compared to traditional 'Si' devices. It has larger breakdown field strength, which enables faster switching with lower losses. So WBG devices offer lower switching and turn-on losses compared to traditional Si switches. As all the high speed switching happens on the sub-modules with WBG switches, the switching losses of the overall system remains low. The switching losses become significant for very high switching frequency for WBGs.

Chapter 6

MMC topologies with different number of sub-modules

This chapter describes the effect of changing the number of output voltage levels by changing the number of sub-modules. The first part of the chapter introduces the terms/calculations required for the comparison. The second part briefly explains the effects of changing the number of sub-modules in the system.

6.1 Active and Reactive Power

Let V_{MMC} be the single phase output voltage of the system. An MMC with 'n' number of sub-modules will have voltage equal to V_{MMC}/n across each sub-modules when they are all ON. The current I_L (I_{MMC}) is the current flowing across the MMC and has value 1 pu. Current flowing through each sub-module is equal to I_{MMC} as each of them is connected in series.

The active and reactive power for a voltage source converter (VSC) is explained in this section. The topology acts as VSC, and can be controlled to

supply active and reactive power within the power limits. The single phase equivalent model for the grid connection of this MMC is as shown in Fig 6.1.

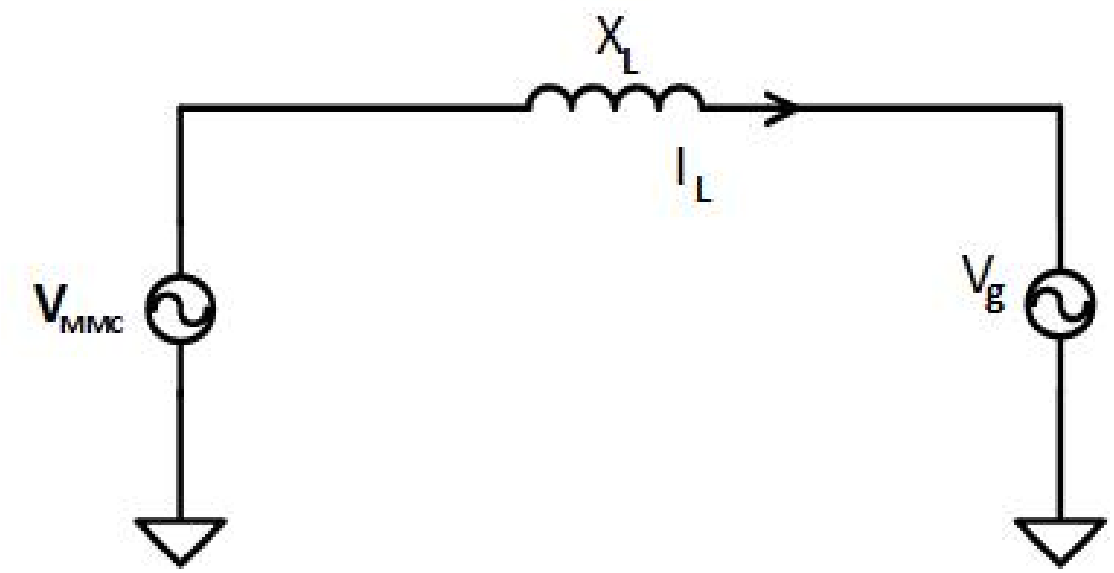

FIGURE 6.1: MMC power flow to the grid

The current flowing into the grid as shown in Fig. 6.1 is given as:

$$I_L = \frac{V_{MMC} - V_{g\angle\alpha}}{jX_L} \tag{6.1}$$

The apparent power is given as:

$$S_{MMC} = VI^* = V_{MMC} \cdot \left(\frac{V_{MMC} - V_{g\angle\alpha}}{jX_L} \right) \tag{6.2}$$

$$P_{MMC} + jQ_{MMC} = \frac{V_{MMC} \cdot (V_g \sin \angle\alpha)}{X_L} + \frac{(V_{MMC})^2 - V_{MMC} V_g \cos \angle\alpha}{-jX_L} \tag{6.3}$$

$$P_{MMC} = \frac{V_{MMC} \cdot (V_g \sin \angle\alpha)}{X_L} \tag{6.4}$$

$$Q_{MMC} = \frac{(V_{MMC})^2 - V_{MMC} \cdot V_g \cos \not{\alpha}}{-jX_L} \tag{6.5}$$

where α is the phase angle between the converter(V_{MMC}) and grid(V_g) voltage. The reactive and active power can be controlled by changing α and the voltage magnitude across the line.

Let's say the P_{MMC} and Q_{MMC} are 1 pu and 1 pu respectively. V_{MMC} is the summation of voltages across the individual sub-modules connected in series to give the multi-level output voltage. Let's call that voltage 1 pu.

6.2 Capacitance in Sub-modules

Fig. 6.2 shows DC to AC converter with DC link capacitor voltage 'V'.

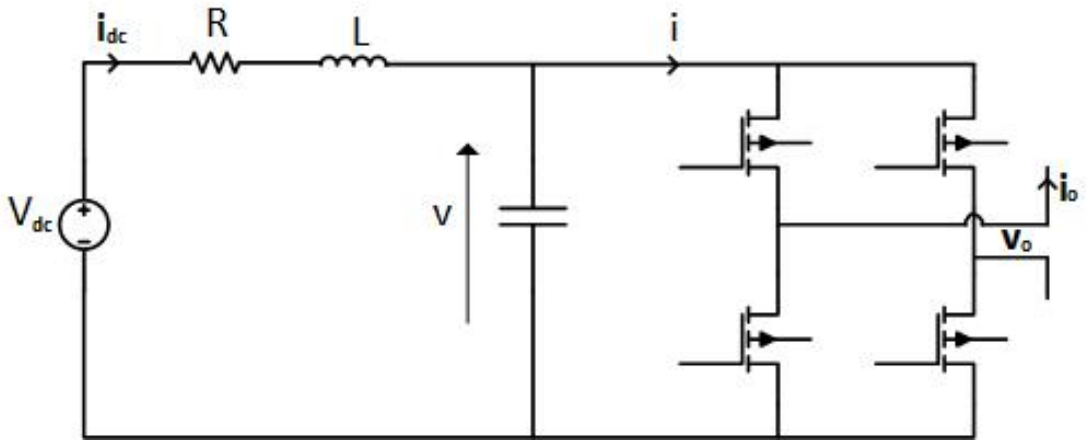

FIGURE 6.2: Capacitor Value Calculation

Expression for the output ac voltage and current are given respectively as under:

$$v_o = V_o * \sin \gamma \tag{6.6}$$

$$i_o = I_o * \sin(\gamma - \theta) \tag{6.7}$$

where γ is the voltage reference angle and θ is the output current phase. The input current 'i' going to the inverter H-Bridge will have a DC component, an AC double fundamental frequency component and the switching frequency component. In an ideal situation, all the DC current component should come form the DC voltage. While the AC double fundamental frequency component and switching frequency component would be sourced from the DC capacitor. The current 'i' can be further written as:

$$i(t) = I_{dc} + \bar{i}(t) + \Delta i(t) \tag{6.8}$$

where, I_{dc} is the dc current, $\bar{i}(t)$ is the double fundamental frequency of the ac current and, $\Delta i(t)$ is switching frequency component

Further expansion for the current is as shown in the following equations [23]:

$$I_{dc} = \frac{m * I_o * cos\theta}{2} \tag{6.9}$$

$$\bar{i}(t) = \frac{-m * I_o * cos(2\gamma - \theta)}{2} \tag{6.10}$$

$$\Delta i(t) = I_o * sin(\gamma - \theta)(1 - m * sin\gamma) \tag{6.11}$$

And the peak to peak amplitude of DC link capacitor is given by the following equation:

$$\Delta v_{pp}(t) = \frac{I_o * T_s * m * |sin\gamma * sin(\gamma - \theta) * (1 - m * sin\gamma)|}{C} \tag{6.12}$$

where, T_s is the time period of the switching frequency, C is the capacitance of the DC link capacitor.

The DC link capacitor is designed such that the capacitor can supply the switching frequency ripple and the double fundamental frequency ripple. For the majority of the cases, including this, the capacitor value for the double frequency ripple is much higher than the capacitance for the switching frequency component. So, the capacitor value is selected accordingly. The DC link capacitor value when calculated for the double fundamental frequency is given by [23]:

$$C = \frac{m * I_o^{max}}{2} * \frac{1}{2 * \omega * V_{rpp}} \tag{6.13}$$

where 'm' is the modulation index, V_{rpp} is the DC link voltage ripple, and 'ω' is the angular frequency of the fundamental frequency. The above equation can be used to design the capacitance value for the DC link.

6.3 MMC with different number of sub-modules

Modular multilevel converters are convenient when it comes to the connection or removal of a sub-module to increase or decrease voltage levels on the output voltage waveform. In the proposed topology adding or removing a sub-module can change the output voltage by two levels. This section discusses the advantages and disadvantages of increasing or decreasing the sub-modules in the proposed topology. For convenience, topology with 4 and 8 sub-modules are compared and discussed in the following section. Fig. 6.3 - Fig. 6.10 shows the structure, output and capacitor voltages for the topology with four and eight sub-modules system.

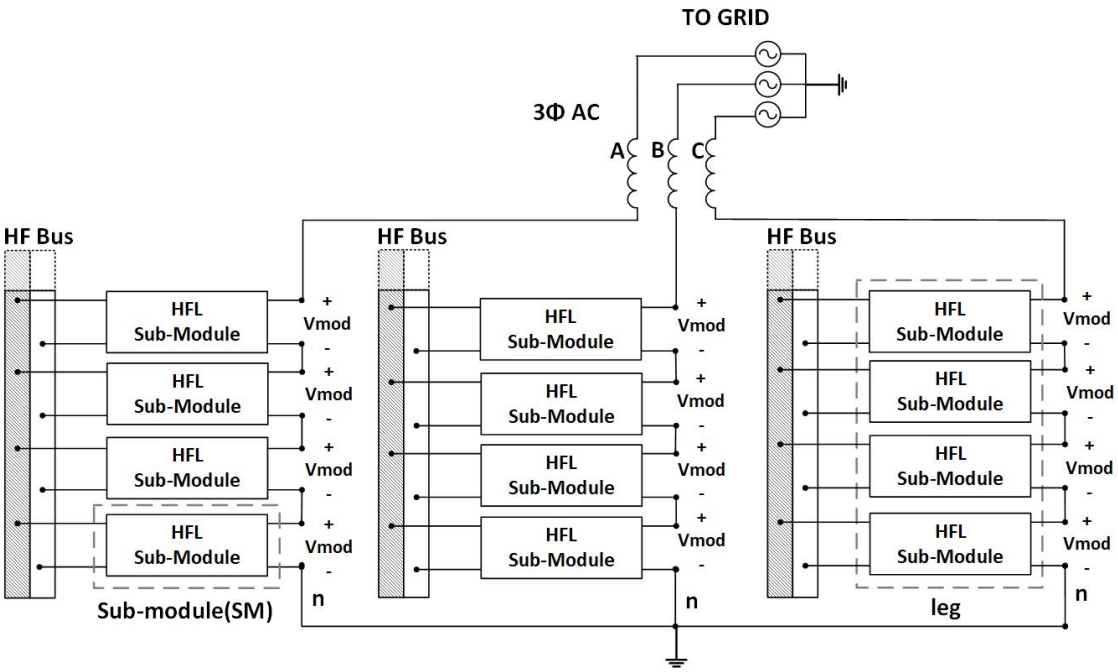

FIGURE 6.3: MMC topology under consideration with 4 sub-modules

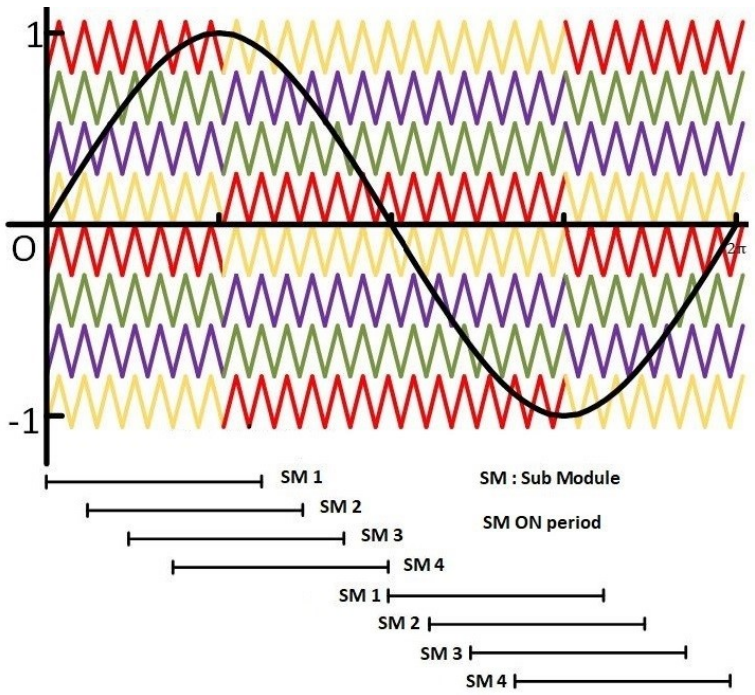

FIGURE 6.4: PWM scheme for 4 sub-modules

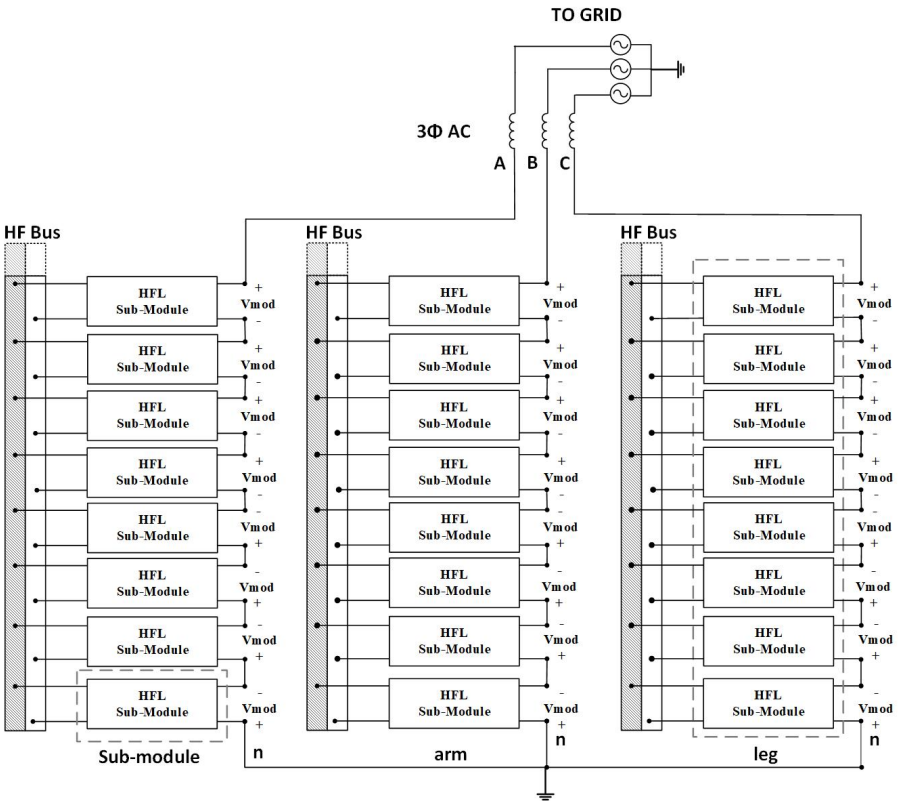

FIGURE 6.5: MMC topology under consideration with 8 sub-modules: Topology indicating the High-frequency bus and connection to the grid

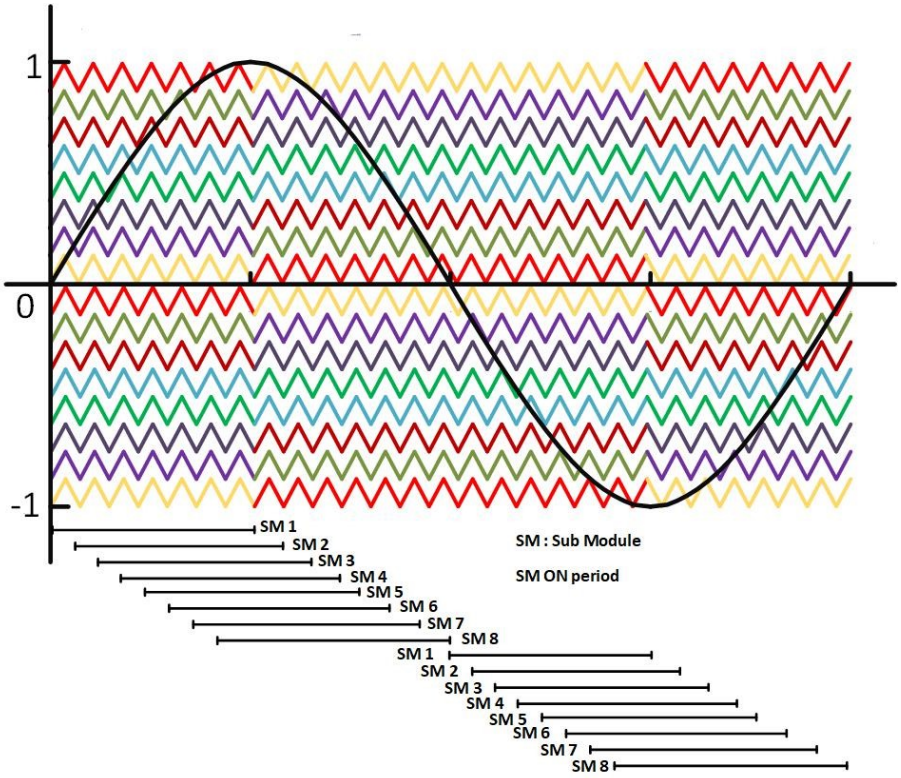

FIGURE 6.6: MMC topology under consideration with 8 sub-modules: New PWM scheme for the PWM

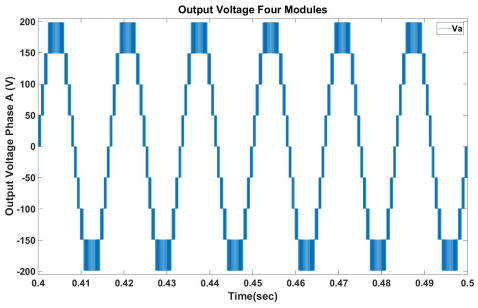

FIGURE 6.7: Output Voltage: 4 Sub-modules

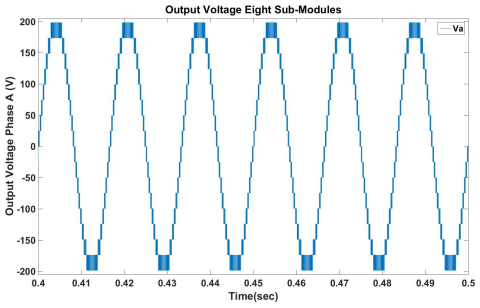

FIGURE 6.8: Output Voltage: 8 Sub-modules

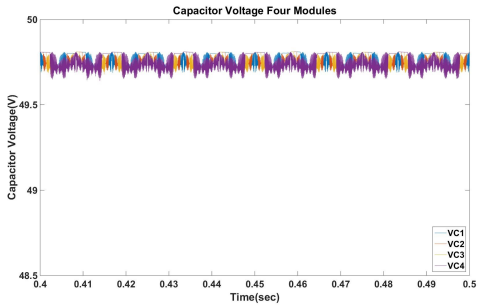

FIGURE 6.9: Capacitor Voltages: 4 Sub-modules

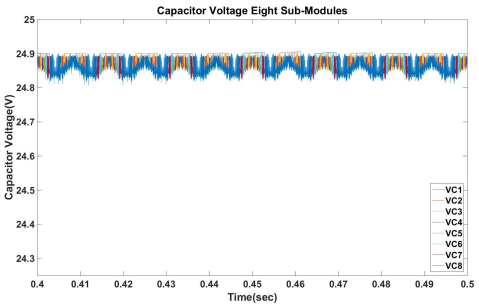

FIGURE 6.10: Capacitor Voltages: 8 Sub-modules

6.3.1 Effects with changing the different number of modules

One of the noticeable cons is the additional cost of increased sub-modules. However, we will look in detail for various other effects of changing the number of sub-modules in the system. In general, changing the number of modules has advantages like reduction in filter size, harmonics, $\frac{dv}{dt}$ stress, EMI, and a lower rated device can be used.

In the following sub-section a comparison for the MMC topology with 4 and 8 sub-modules are done. For comparison, the 4 sub-modules topology output voltage is taken as the reference at 1p.u.

Cost

Increasing the number of sub-modules increases the cost of the overall system. In the presented topology each sub-module has a cost associated with the cost of high frequency transformer, capacitor, diode bridge, and H-Bridge converter.

Harmonics

With the increase in sub-modules, the output harmonics goes down. This can reduce the overall filter requirements, and thus the additional filter cost.

Switch Voltage Rating

The voltage rating of the switch with twice the sub-modules is half that of the original system.

Size and Weight

Increasing the number of sub-modules increases the size and weight of the overall system. Although it might of much importance for the PV/wind system if the system is placed on earth. However, the system is commonly placed in the nacelle of the wind turbine, and it is desirable to have a smaller size and weight. In particular, it becomes very crucial for offshore wind farms due to limited installation area, and this is where the size & weight of the turbine play a big factor.

Gate Pulse control Complexity

The fewer number of sub-modules means there will be few switches to control. This reduces the gate pulse complexity. A topology with four sub-modules needs only 16 gate pulses for all the sub-modules, while the eight sub-modules will need 32 gate pulses. This increases the gate control complexity and thus cost.

Equal Utilization of sub-modules

Power distribution among the sub-modules depends on the type of PWM technique used. The phase shifted modulation equalizes the power flow across all the sub-modules irrespective of the number of the sub-modules. However, on the proposed PWM scheme, an increase in the number of sub-modules, improves the power distribution among the sub-modules.

6.4 Output Voltage Ripple and Energy Stored

Changing the number of sub-modules will have different impact on energy storage, output voltage ripple of the sub-modules. Here, we will consider two different options: a)capacitance value of the of the sub-modules are same. b) output voltage ripple remains same.

6.4.1 Same Capacitance Value for the sub-modules

If the sub-modules in both the systems are identical:

Energy Storage

Energy stored in capacitors with 'x' sub-modules E_x can be given as

$E_x = 0.5 * C * V^2 * (numberofsubmodules) = 0.5 * C * V^2 * n.$

So energy stored with 4 sub-modules:

$$E_4 = \frac{C * V^2}{2} \tag{6.14}$$

$$E_4 = 1pu \tag{6.15}$$

and energy stored with 8 sub-modules:

$$E_8 = 4 * \frac{C * (V/2)^2}{2} \tag{6.16}$$

$$E_8 = 0.5pu \tag{6.17}$$

Energy Stored in the Capacitor of the sub-modules reduces to half when we double the number of sub-modules. Energy stored in the sub-modules plays a vital role in fast recovery from faults in the system or in case of voltage sag or swell.

Capacitor Ripple

With a change in the number of modules, the overall system capacitor ripple changes. With 4 sub-modules (with capacitor voltage equals 50 V), let us say the capacitor voltage ripple as 1 p.u.

The capacitor ripple is given by the following equation:

$$V_{rpp} = \frac{m * I_o^{max}}{2} * \frac{1}{2 * \omega * C} \tag{6.18}$$

With change in the number of sub-modules, without changing the capacitor value in the sub-module the capacitor ripple for the sub-modules remains the same. Considering the capacitor ripple of each sub-modules be 1 pu. Overall system capacitor ripple with four sub-modules becomes

$$V_{rpp_4} = 4pu \tag{6.19}$$

Overall system capacitor ripple becomes with eight sub-modules

$$V_{rpp_8} = 8pu \tag{6.20}$$

With the increase in sub-modules without changing the capacitance value (but changing the sub-module voltage to generate the same output MMC voltage), the capacitance ripple of the overall system increases.

6.4.2 Equal Output Voltage capacitance ripple

As the voltage across the capacitors becomes half with double the number of sub-modules, to maintain the same output voltage ripple the capacitance value for each sub-modules should double.

So energy stored with 4 sub-modules:

$$E_4 = \frac{C * V^2}{2} \tag{6.21}$$

$$E_4 = 1pu \tag{6.22}$$

and energy stored with 8 sub-modules:

$$E_8 = 4 * \frac{2 * C * (V/2)^2}{2} \tag{6.23}$$

$$E_8 = 1pu \tag{6.24}$$

Energy Stored in the Capacitor of the sub-modules remains the same for double the number of sub-modules and increase the sub-modules capacitance value to two times. The percentage ripple of the capacitors for each sub-modules

also remains the same. Energy stored in the sub-modules plays a vital role in fast recovery from faults in the system or in case of voltage sag or swell.

Increase or decrease in the number of sub-modules can have have significant chance in the the size and complexity of the system. The actual number of sub-modules should be evaluated and considered case-by-case depending on the application.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

The thesis presents a modular multi-level converter that can act as an interface between renewable and the modern grid. It proposes a new PWM scheme for a high-frequency link based MMC converter for the grid integration of PV and wind. The proposed PWM technique has almost equal module thermal stress with low switching losses, thereby including the benefits of both level-shifted and phase-shifted techniques. A detailed analysis of the various PWM techniques is presented. This also includes a comparison of switching losses and capacitor ripple with analytical models SIMULINK simulation.

In addition, proposed a hybrid GaN + Si based CHB inverter and a corresponding PWM technique for improved efficiency of the system without a significant increase the overall cost of the system. This thesis presents the simulation and the hardware results to demonstrate the proposed hardware and PWM schemes on a 9-level CHB inverter.

7.2 Future Work

The topology has significant advantages compared to the traditional grid connection and can be used in future smart grid implementations. The following future work will help:

1. Detailed analysis of energy storage in the system.
2. Connection of the topology to the grid.
3. Real and reactive power compensation.
4. Fault ride through capability.

Chapter 8

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