Modeling, Analysis, Design and Control of a Power Electronic Transformer using Back-to-Back Connected MMCs for Grid Integration of Renewables and Storage

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Dedication

To Prof. Ned Mohan... for providing me with an opportunity to work under him and being with me till the end.

Abstract

Utility-scale renewables, wind and solar, are already becoming cheaper than power from the conventional fossil-fuel sources. Their further penetration for achieving the goal of 100% carbon-free electricity will be stalled unless their cost and efficiencies are further improved. Power electronic interfaces enabling their grid integration should provide ancillary services to keep the grid stable. In addition, it has become the norm to be able to integrate multiple heterogenous forms of energy through a common interface scheme and thus achieve higher power densities. The power electronic interface in this research serves these purposes for the integration of renewables and storage to the medium voltage grid between $5\,kV - 34.5\,kV$.

A Power Electronic Transformer (PET) topology involving direct back-to-back connection of Modular Multilevel Converters (MMCs), where one of the MMCs is connected to the grid and the other called High-Frequency MMC (HF-MMC) is connected to a step-down HF transformer, is studied in this dissertation. The low-voltage (LV) side of the HF transformer is connected to another back-to-back arrangement of two-level voltage source converters (2L-VSCs) for extracting power from renewables such as wind.

The proposed interface is based on a modular topology to render it highly reliable, in conjunction with a high-frequency transformer which can be lighter in weight by a factor of 150 compared to the line-frequency transformer. It can provide ancillary services and control flexibility to offer "smart" solutions to maintain grid stability even when the penetration of renewables begins to approach conventional sources.

Specifically, the contributions of the dissertation in making the interface deployable in the industry are as stated below.

The modeling, design, control, and operation of the proposed interface scheme have been presented and validated through OPAL-RT-based Hardware-In-Loop simulations, MATLAB/ SIMULINK simulations, and results from the experimental hardware prototype. The PWM switching ripples across the dc link have been quantitatively characterized and investigation of their propagation in the dc-link control schemes has been performed. Harmonic analysis and online optimization-based control schemes to improve the efficiency of power transfer across the high-frequency link have been presented. The

DC side model of the HF-MMC which unveils the sensitivity of HF-MMC to voltages at frequencies other than dc being injected at the dc link is developed. The potential for virtual inertia with the proposed PET interface has been identified along with formulating associated control schemes for inertial support to the grid. Finally, an invention of a power converter topology employing several modular high-frequency transformers with drastically reduced voltage stresses and with multiple parallel power transfer paths has been made to improve on the initial architecture under study. This novel power conversion architecture achieves the critical objective of unifying dispatchable forms of power such as storage and the highly intermittent forms of energy such as wind and solar.

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Introduction

With the looming climate crisis becoming ever more pressing by the day, the necessity to curtail the presence of greenhouse gases has become one of the most urgent ones among the landscape of global risks in the coming ten years as shown in Fig.1.1[1].

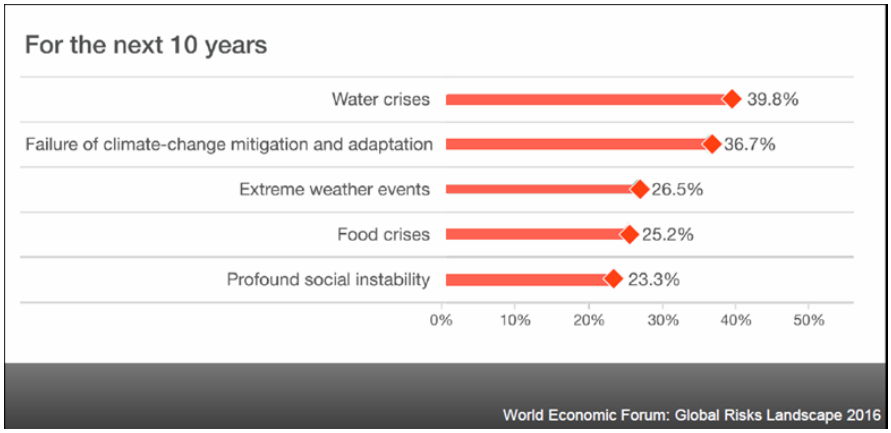


Figure 1.1: Global Risks Landscape [1]

The actual global temperature rise closely follows the trend under the influence of green house gases alone as shown in Fig.1.2[2].

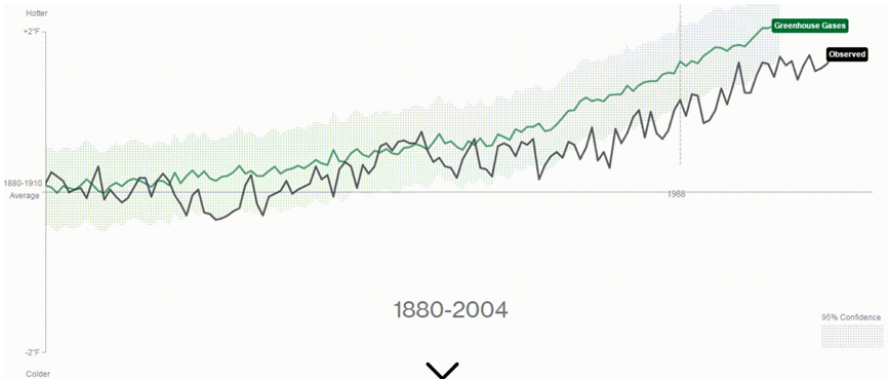


Figure 1.2: Global average temperature rise under the influence of greenhouse gases[2]

Fortunately, renewable energy sources such as wind and solar power present a solution. Levelized Cost of Energy (LCOE) trends of these energy sources clearly indicate an equally optimistic alternative path for mitigating humanity's energy crisis as observed from Fig.1.3[3].

Plant type	Capacity factor (%)	Levelized capital cost	Levelized fixed O&M	Levelized variable O&M	Levelized transmission cost	Total system LCOE	Levelized tax credit[1]	LCOE including tax credit
Dispatchable technologies								
Coal with 30% CCS[2]	85	84.0	9.5	35.6	1.1	130.1	NA	130.1
Coal with 90% CCS[2]	85	68.5	11.0	38.5	1.1	119.1	NA	119.1
Conventional CC	87	12.6	1.5	34.9	1.1	50.1	NA	50.1
Advanced CC	87	14.4	1.3	32.2	1.1	49.0	NA	49.0
Advanced CC with CCS	87	26.9	4.4	42.5	1.1	74.9	NA	74.9
Conventional CT	30	37.2	6.7	51.6	3.2	98.7	NA	98.7
Advanced CT	30	23.6	2.6	55.7	3.2	85.1	NA	85.1
Advanced nuclear	90	69.4	12.9	9.3	1.0	92.6	NA	92.6
Geothermal	90	30.1	13.2	0.0	1.3	44.6	-3.0	41.6
Biomass	83	39.2	15.4	39.6	1.1	95.3	NA	95.3
Non-dispatchable technologies								
Wind, onshore	41	43.1	13.4	0.0	2.5	59.1	-11.1	48.0
Wind, offshore	45	115.8	19.9	0.0	2.3	138.0	-20.8	117.1
Solar PV[3]	29	51.2	8.7	0.0	3.3	63.2	-13.3	49.9
Solar thermal	25	128.4	32.6	0.0	4.1	165.1	-38.5	126.6
Hydroelectric[4]	64	48.2	9.8	1.8	1.9	61.7	NA	61.7

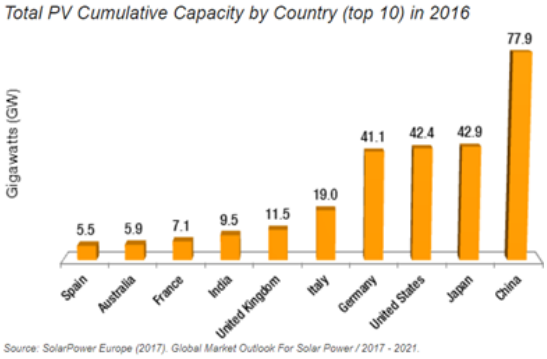
Figure 1.3: Estimated levelized cost of electricity (unweighted average) for new generation resources entering service in 2022 (as of 2017 in $/MWh)[3]

The increasing penetration of these green energy sources into the grid and shown in Fig.1.4 make it apparent that they are sparking off a revolution in the energy sectors of the nations all over the world[5].

Country	End 2016	Net New 2017	End 2017	Change
China	168,732	19,500	188,232	11.6%
USA	82,060	7,017	89,077	8.6%
Germany	50,019	6,581	56,132	12.2%
India	28,700	4,148	32,848	14.5%
Spain	23,075	96	23,170	0.4%
UK	14,602	4,270	18,872	29.2%
France	12,065	1,694	13,759	14.0%
Brazil	10,741	2,022	12,763	18.8%
Canada	11,898	341	12,239	2.9%
Italy	9,227	252	9,479	2.7%
Turkey	6,091	766	6,857	12.6%
Sweden	6,494	197	6,691	3.0%
Poland	6,355	41	6,397	0.7%
Denmark	5,230	342	5,476	4.7%
Portugal	5,316	-	5,316	0.0%
Australia	4,312	245	4,557	5.7%
Netherlands	4,328	81	4,341	0.3%
Mexico	3,527	478	4,005	13.6%
Japan	3,230	177	3,400	5.3%
Ireland	2,701	426	3,127	15.8%
World Total MW	487,657	52,573	539,581	10.6%

Source: Global Wind Energy Council (GWEC)

(a)



(b)

Figure 1.4: Installations of wind and solar power across different countries as of 2017 [4]

In the United States for example, Xcel energy has recently embarked upon building a 600MW wind facility in Colorado which would meet 55% of the state's energy needs[6]. This is in addition to other new wind energy projects proposed for construction in the southern parts of Minnesota and in North and South Dakota which totals to about 3700 MW of additional wind installations in the next 4 years[6]. With such a drastic addition of installation of these renewable energy sources, there is still a need to provide a reliable and cost-effective infrastructure to tap their full potential. MIT Technology Review has observed that the "Renewables are outgrowing their grids" in Germany and China[7]. It has been reported that China has been adding solar power installations so fast that it can't make use of as much as 50 percent of the energy being generated in some provinces[7]. Thus, storage plays a crucial role in the realm of wind and solar energy going forward. In addition, grid stability and other ancillary services that their power converters are required to provide to support the grid have driven a major research effort by power engineers to make energy sustainability a reality.

As seen above, utility-scale renewables, wind and solar, are already becoming cheaper than power from the conventional fossil-fuel sources. Their further penetration for achieving the goal of 100% carbon-free electricity will be stalled unless their cost and efficiencies are further improved. They should provide ancillary services to keep the grid stable. In addition, it has become the norm to be able to integrate multiple heterogenous forms of energy through a common interface scheme and thus achieve higher power densities. The power electronic interface in this research serves these purposes for the integration of renewables and storage to the medium voltage grid between $5\,kV - 34.5\,kV$. The power conversion architectures presented achieve the critical objective of unifying dispatchable forms of power such as storage and the highly intermittent forms of energy such as wind and solar.

1.1 Background

1.1.1 Present Interfaces using a 60-Hz Transformer

The present methods of interfacing renewables, based on 60-Hz transformers are discussed below in wind, PVs and battery-storage applications.

Wind-Turbine Interface

To illustrate this, consider Fig.1.5 which shows a typical arrangement of components, for example, in a 2.3 MW wind turbine from Siemens[8, 9]. It shows a low-voltage 690-V generator in the nacelle that produces variable-frequency voltages and currents depending on wind speeds, where over two-thousand amperes of current flows through nearly a 100m long cable, thick enough to handle this current. These variable-frequency voltages/currents are converted by the power electronics converter, shown in Fig.1.9 by its block-diagram, at the base of the tower to constant amplitude (700 V) and 60-Hz sinusoidal voltages that are boosted to 34.5 kV by a 60-Hz transformer weighing nearly 7 tons at these power levels.

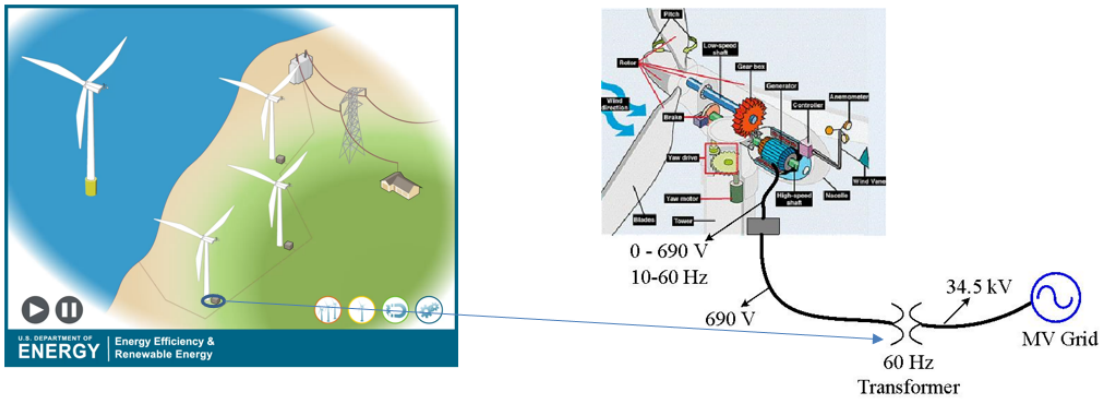


Figure 1.5: Typical grid interface of wind turbines

In a wind plant, now as large as 800 MW[10], hundreds such wind turbines are connected to an underground collection grid at a voltage of 34.5 kV, which has become a de facto collection grid voltage level. Subsequently, another transformer boosts this voltage to 161 kV, for example, for transmission purposes. Some companies are now opting to put the power electronics converter and the 60-Hz transformer in the nacelle so that only a small amount of current needs to be carried by the 100m long cable. But it requires a heavy 7 ton transformer to be located in the nacelle, putting additional burden on the tower structure and the foundation and thus increasing their cost.

Photovoltaic Applications

Fig.1.6 shows a typical topology for a 550 MW PV plant built by First Solar, Inc[11]. It shows that power from a large array of PV modules, each operating at their maximum power point (MPP), is collected at 1,000 V (dc) which is interfaced through a power electronics converter and a 60-Hz transformer to the grid voltage of 34.5 kV.

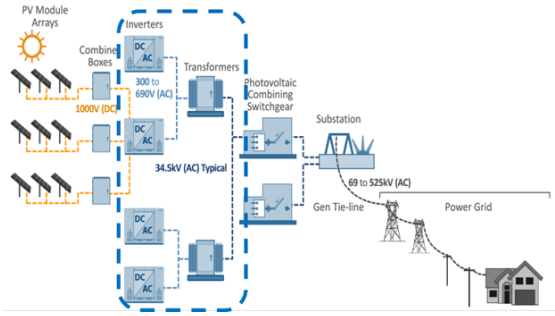


Figure 1.6: First Solar Inc.'s 550 MW PV Plant

Battery-Storage Application

An interface, similar for wind and PVs, but with bi-directional power-flow capability, is used for large-scale battery storage facilities, e.g., Xcel Energy's 1 MW, 7.2 MWh battery facility built in Lavern, MN[12] and shown in Fig.1.7.

Figure 1.7: Xcel Energy battery facility

1.1.2 High-Frequency (HF) Transformers versus 60-Hz Transformers

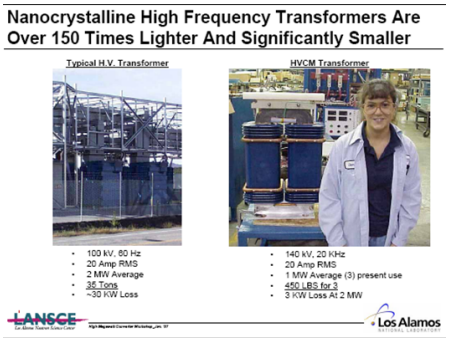


Figure 1.8: High Frequency versus a 60-Hz Transformer[4]

Compared to 60-Hz transformers, high-frequency (HF) transformers operating at 20 kHz, for example, can be significantly smaller and lighter by a factor of 150[4], as

depicted in Fig.1.8. This size reduction also implies a significant reduction in the amount of copper and the core material needed. The core of HF transformers is made up of a nano-crystalline material such as FINEMET[13] that is ideal because of its high permeability, high saturation flux-density, and very low core-loss at frequencies of 20 kHz or so at which these transformers are likely to operate at high power-levels. The cost of such material will reduce in large-volume production since no exotic material is required. It is important to note that the losses shown in Fig.1.8 in the HF transformer (3 kW) are only one-tenth of those in a comparable 60-Hz transformer (30 kW). Therefore, it is expected that the overall losses, including those in power electronic converters needed on both sides of the HF transformer, will be lower than in a 60-Hz transformer.

1.1.3 A cost-effective and novel solution for the Utility-Scale Integration of Wind/Solar:

Present wind turbine integration schemes use a 60-Hz transformer to interface the generator and the power electronic converter at voltages around 1 kV to the collection grid with voltages of 34.5 kV as shown in Fig.1.9.

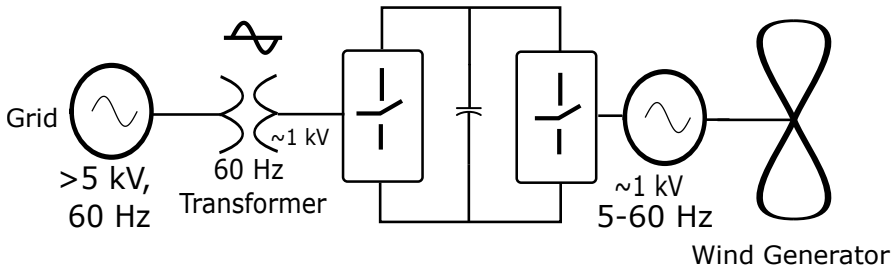


Figure 1.9: Present Grid Interface Scheme of Wind Turbines

This scheme results in high currents of the order of kilo-Amperes in the long cables from the nacelle to ground where the power electronic converter and the heavy 60 Hz transformer are located[8, 9]. To reduce the weight of the transformer by a factor of one-hundred or more[4] so that it can be placed in the nacelle along with the converter, thus avoiding the losses in cables 300 meters or so in length, a novel scheme employing power electronic transformer (PET), as shown fig. 2 has been proposed[14, 15, 16, 17, 18].

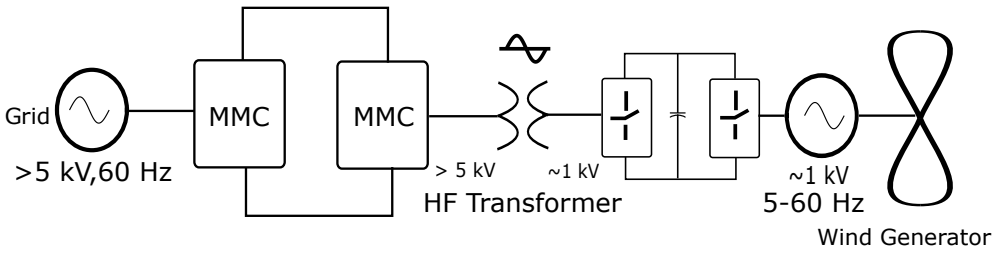


Figure 1.10: The proposed Back-to-Back MMC-PET based Interface

This solution based on Modular Multilevel Converters(MMCs) involves modular cascaded connection of solid-state devices which reduces the high-frequency transformer dv/dt stresses, has very low harmonic content in the output voltages and is more reliable and cheaper, particularly at grid voltage levels beyond 10 kV, compared to the prior state-of-the-art technology for power electronic transformers involving a direct series connection of IGBT devices and lossy snubber circuits for equal voltage sharing. The reduction in the heavy copper losses in the droop cables, core losses by about ten times due to transformer size reduction and the cost of the wind turbine tower support structure, makes the proposed interface scheme for wind and solar achieve significant cost reduction. Minimizing the burden on the tower and foundation of the wind turbines assumes paramount importance in off-shore wind farms where the cost and technology limitations of the floating platforms on the sea-bed results in off-shore wind power to cost in excess of $110/MWh[19], as for example, in the New York's NYISO grid.

1.1.4 Proposed Renewable Energy Interface as a Power Buffer:

In existing wind turbine systems, to provide inertial support in case of step load changes, the stored kinetic energy in the rotating turbine is utilized. In doing this, the wind turbine is continuously operated at higher speeds so that there is additional stored kinetic energy which can be dispatched on demand. However, these higher speeds are not optimal for the maximum power point- the speed where the maximum possible wind power gets transferred on to the turbine and subsequently to the grid. The interface in this research presents an alternative means of providing inertia using the stored energy in the virtual dc link across the back-to-back MMCs and can ensure that additional power due to inertia is always provided while simultaneously extracting the maximum

power available from the wind[17]. In order to comply with requirements such as a ramp rate of less than 10% of the PV plant capacity, a large number of battery storage units would be required, and the repeated charge/discharge cycles further reduce their useful lives[20]. The proposed interface scheme can be designed in an economically feasible way to ensure that the PV cluster associated with the interface provides a more uniform power output across different one-minute intervals thus reducing the magnitude of the ramp rate violations. This, in turn, reduces the battery energy storage that needs to be installed to meet the technical requirements for PV projects. Further, a frequency stable and constant AC power output can be supplied even from a small cluster of PV panels connected through the interface under research even when not connected to the grid or other energy sources. About 127 GW of coal and nuclear plant generators have retired since 2005. This land area with the power lines already in place, could be ideal for installing solar panels and batteries, integrated with the utility grid by employing the interface in this research.

1.2 Novel Contributions towards making the interface practical:

The following are the major contributions of this dissertation and research on the interface:

1. Design, control, and operation of the proposed interface Scheme.
2. Quantitatively characterising the PWM switching ripples across the dc link and investigation of their propagation in the dc link control schemes.
3. Harmonic analysis of the high frequency link currents and online optimization-based control schemes to improve the efficiency of power transfer across the high-frequency link.
4. DC side modeling of the HF-MMC which unveils the sensitivity of HF-MMC to voltages at frequencies other than dc being injected at the dc link.
5. Invention of a power converter topology employing several modular high-frequency transformers with drastically reduced voltage stresses.

6. Identifying the potential for virtual inertia with associated control schemes for inertial-control from the PET.

Accordingly the rest of the dissertation is organized as follows:

Chapter 2 introduces the MMC-PET interface in detail along with its advantages and provides a comparison with other HF-link topologies. The operation and control of the back-to-back MMC based power electronic transformer are demonstrated for the voltage control of the back-to-back MMC dc link voltage, power-factor control on the grid side, grid-independent reactive power sourcing on the load side and under conditions of grid voltage unbalances and faults in Chapter 2. The various modulation schemes at the grid side MMC, high-frequency link MMC, high-frequency link voltage source inverter, the wind turbine side converter outlined in Fig.1.11.

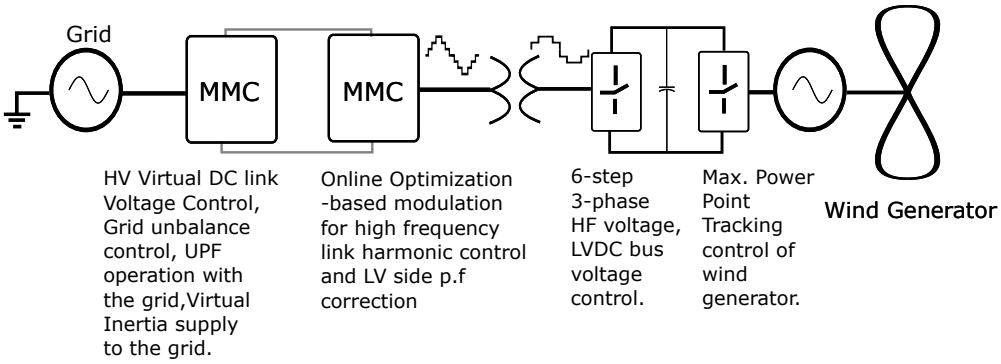


Figure 1.11: Overall Control Allocation to the converters in the back-to-back MMC based PET interface of the wind turbine

Further, Chapter 2 quantitatively characterizes PWM switching ripples in the dc link across the back-to-back MMCs and derives analytical expressions for their magnitude at each stage during their propagation through the control loop. It also presents a scheme to control the voltage across during grid voltage unbalances making sure grid current quality does not get affected at all operating scenarios.

Chapter 3 presents an online non-linear optimization technique to optimize the switching angles in the nearest-level-modulated waveform at the high-frequency link resulted in reduction in harmonic distortion of the high-frequency link currents by as

much as 60% while at the same time ensuring unity displacement power factor operation. It also validates the proposed control schemes at the high-frequency link involving the control of the two-level converter dc link and efficient power transfer across the link.

Chapter 4 discusses the mathematical modeling of the dc side of the HF-MMC and uncovers the mechanism that causes its sensitivity to certain frequency voltage injections at the its dc link. A mathematical framework predicts these sensitive frequencies as a function of the MMC parameters and operating frequency.

Chapter 5 discusses some design considerations at the high-frequency link which ensures soft-switching at the HF-link two-level converter, unity displacement power factor operation and keep the current THD within limits for the required rated power transfer.

Chapter 6 presents an invention of a power-converter topology called Distributed-Phase-MMC (DP-MMC) to further reduce the high-frequency transformer voltage stresses. Further, the topology is rendered even more modular with multiple parallel power transfer paths by employing N high-frequency transformers with reduced voltage ratings as shown in Fig.1.12.

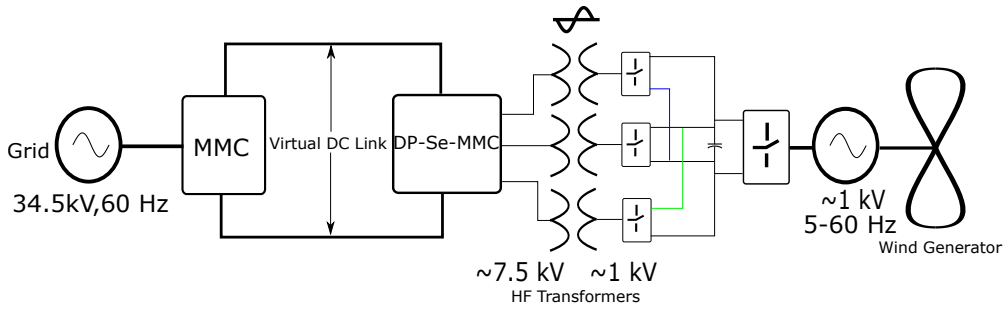


Figure 1.12: Utility-Scale Interface for renewables and storage with the proposed DP-MMC topology

DP-MMC ensures that each transformer withstands (1/N) th of the voltage of that when using a conventional MMC and with similar current ratings, where N is the number of three-phase transformers.

Chapter 7 identifies the potential for virtual inertia. The virtual dc link across the back-to-back MMCs is at voltages of the order of twice the collection grid voltage which results in a large stored potential energy in it. A novel control scheme for providing

inertia using the back-to-back MMCs in the PET used for grid interface of renewables and storage is discussed.

Chapter 8 concludes the dissertation by summarizing the results presented validating the above claims.

Chapter 2

A Modular Multi-Level Converter based Power Conversion Architecture and Operating Scheme for Grid-Integration of Wind Energy Systems

Traditional power conversion schemes for grid interfacing of wind energy systems (WES) typically employ a line frequency transformer and back-to-back connected PWM power converters. Such a scheme is heavy, bulky and expensive. In this paper, a new power conversion architecture is proposed that is particularly well suited for grid integration of WES at medium voltage (MV) level in the distribution network. The proposed power-circuit consists of back-to-back connected Modular Multilevel Converters (BB-MMCs), a high-frequency (HF) transformer and back-to-back connected two-level converters. Such a scheme has several advantages over traditional architectures such as reduced transformer size and weight due to HF operation. This enables housing the entire system in the wind turbine nacelle. An operating mechanism for the overall system is proposed that facilitates high-frequency operation and the corresponding size reduction.

A Fourier series based method is employed for quantitatively characterizing the

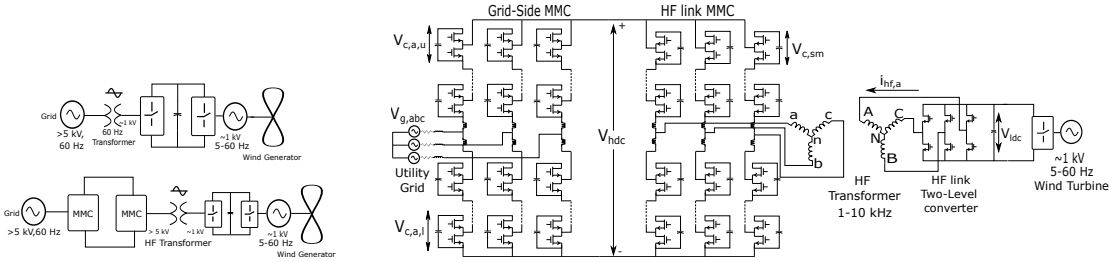
propagation of the BB-MMC DC link switching ripples through its voltage control loop. The designed DC-link voltage controller ensures fast dynamic performance as well as injection of high quality grid current even with unbalanced grid voltages. Validations of the proposed PWM and control schemes on the overall architecture are performed using simulations of the full-order model in MATLAB/Simulink and with real-time hardware-in-loop (HIL) simulations in OPAL-RT.

2.1 Introduction

Wind energy systems (WES) are widely being deployed today due to the increased spur towards renewable power generation. In Germany wind energy contributes to 25% of all power generation today [21] and the budget is to increase it to 50% by 2050[22]. Similarly in the US, wind penetration, which is the share of annual end-use electricity demand, has a trajectory of 10% ,20% and 35% by 2020, 2030 and 2050 respectively[23]. Such a wind dominated power generation landscape necessitates increasing the efficiency of WES and making its generation cost achieve even greater gaps with conventional energy sources, thereby addressing the demand for an ever-decreasing cost curve of overall power generation[24].

As shown in Fig.2.1a(top), present wind turbine integration schemes use a 60-Hz transformer to interface generator and the power electronic converter at voltages around 1 kV to the grid with voltages of 5 kV and above, upto collection grid voltages of 34.5 kV. This scheme results in high currents of the order of kAs in the long cables from the nacelle to ground where the power electronic converter and the heavy 60 Hz transformer are located[25].

To reduce the weight of the transformer by a factor of one-hundred or more[26] so that it can be placed in the nacelle along with the converter, thus avoiding the losses in cables 300 meters or so in length, the topology under study in this dissertation shown in Fig. 2.1a (bottom), is a possible solution.



(a) (b)

Figure 2.1: (a). Present grid interface scheme for wind turbines (top) and Proposed BB-MMC PET based wind turbine interface scheme (bottom) (b). Detailed circuit diagram of the proposed BB-MMC PET architecture

The proposed approach in Fig.2.1b consists of Back-to-Back connected Modular Multi-Level Converters (BB-MMCs)[14, 15, 16] of which the Grid-Side MMC (GS-MMC) synthesizes line frequency PWM voltages to control the currents drawn from the grid and the High-Frequency MMC (HF-MMC) synthesizes a nearly sinusoidal stepped-waveform of voltages and currents associated with the high-frequency (HF) transformer.

It serves to increase the efficiency and cost of such WES as follows. Winding and core losses in the transformer scale with its size[4] and thus, these losses are tremendously reduced. Next, since the voltages are stepped up to the grid voltage level by the HF-transformer at the nacelle itself, the losses in the droop cables running down the wind turbine tower are reduced by the square of the transformer turns ratio. Further, the power smoothing function of the single large dc link capacitor of the two level converters in Fig.2.1a(top) is performed by the distributed sub-module capacitors of the BB-MMCs in Fig.2.1b.

Unlike the MMCs employed in VSC-HVDC systems[27, 28, 29] where a thousand sub-modules are cascaded to reach the transmission voltage levels of 400 kV and above, the BB-MMCs in the proposed architecture contain reduced number of sub-modules to reach the level of the medium voltage grid. The distributed capacitance of the transmission lines make the dc link of the VSC-HVDC system act like a rigid dc voltage source. However, in the proposed topology, there is a much lower effective dc bus capacitance presented by the sub-module capacitors. Since megawatts of power from the

wind turbine are being processed through such a low capacitance dc link, the bandwidth of the dc bus control loop should be sufficient to the reject the variations in wind power at this scale.

A premise for such a dc bus controller is provided next. In case of HVDC lines, the leg energy of the MMC is controlled through circulating current control schemes[30, 31]. Whereas for medium voltage grid integration, railway traction and some motor drive applications, the dc bus voltage control across the direct back-to-back connected (not through HVDC lines) MMC arrangement have been reported in [32, 33, 34, 35, 36]. In these cases, the dc bus voltage is regulated by an outer voltage control loop which provides a grid current reference command that is tracked by the inner output AC current control loop. Further, the dc bus voltage that is used for feedback is obtained by directly measuring the leg voltages across the BB-MMCs with or without processing this feedback signal through a low-pass filter[32, 33, 34, 35, 36, 37]. Since these leg voltages are formed by the PWM output of the cascaded half-bridge modules, sensing them for feedback purposes causes switching ripple propagation through the control loops which is quantitatively characterized in this paper. This ripple propagation is in turn shown to cause associated degradation in the injected grid current quality. In [38], the leg energy is controlled by sensing the average of the sub-module capacitor voltages in a leg. In [39], the sub-module capacitor voltages are averaged across the three-phases for arm voltage reference generation, but the signal was not used for closed loop control of the dc link voltage. Under unbalanced grid conditions, the zero sequence second harmonic oscillation was extracted through a resonant filter for feed-forward cancellation in the arm voltage reference. In this paper, a similar processing of the sub-module capacitor voltages is carried out for generating the dc bus voltage feedback signal. Further the zero sequence second harmonic voltage feed-forward cancellation under unbalanced grid conditions is carried out by estimating this ripple without utilizing any form of filter for processing the voltage signal in the feedback path.

Next, a comparison with other power conversion architectures is provided to bring out the unique aspects of the proposed circuit. Cascaded converter topologies to interface power sources at voltage levels of about 1 kV to the medium voltage grid at voltages of 5 kV-34.5 kV are increasingly being studied upon [40, 41, 42, 43, 44, 45].

These interfaces involve a power electronic transformer to match the difference in voltage levels and for isolation purposes. In [40] and [41], there are multiple windings acting as the secondaries of the high frequency transformer in each module of the cascaded converter. In [41], the H-bridge sub-module capacitor voltage is fixed at the PV maximum-power-point(MPP) voltage which does not allow inertial power support to the grid or smoothening out of PV power variations. Also in [42, 43], other topologies for medium voltage applications with a H-bridge connected to each of the sub-module dc capacitors followed by a high frequency transformer and an active rectifier are discussed.

In comparison, the topology studied in this paper[14, 15, 16, 17, 18, 46, 47] shown in Fig.2.1b, employs a single high-frequency (HF) transformer without multiple secondaries. This renders the topology less prone to transformer failures since only one transformer's insulation is subjected to voltage stresses of the medium voltage grid with respect to the grid ground. This is unlike the case of a HF transformer in each of the sub-modules [42, 43] of the cascaded converter where each transformer's insulation is subjected to such voltage stresses.

In [44], a switched mode rectifier is used in the high frequency link of the cascaded sub-modules instead of a passive rectifier as in [41]. Combined phase shift and frequency modulation techniques in the dual-active-bridge(DAB) operated high frequency link in [44] allow for reducing the size of the sub-module capacitor. With a reduced sub-module capacitance, dedicated energy storage units are required to be interfaced through the cascaded sub-modules for providing inertial support to the grid. Also, there is increased control complexity as each sub-module will have to be controlled independently depending on the power available from the PV arrays through dedicated control loops at the sub-module level. In contrast, with the current topology, only one single parameter, namely, the dc link voltage across the back-to-back connected modular-multilevel-converters (MMCs) needs to be controlled to provide frequency regulation to the grid through a simple control scheme[48, 17].

Modular multilevel converter based medium voltage grid integration topologies in [49] integrate PV and batteries directly into the half-bridge sub-modules along with their associated dc-dc converters. This topology is not especially suited for wind turbines unlike the one studied in this paper.

DC-DC transformers based on MMCs have been proposed in [50, 51, 52] to transfer power between high-voltage-direct-current (HVDC) lines at different voltages or between a low voltage dc source and a medium voltage dc source. However, they do not consider a direct back-to-back connected MMC for renewable energy interface with the utility grid. The back-to-back connected MMC topology was also studied in [53, 32]. In these cases, a HF-MMC was not involved.

Other direct AC-AC medium voltage interface topologies are based on modular-multilevel-matrix-converter [54] with the advantage of reducing the total switch count and an extension of the work in [44] to have unfolding bridges and AC sources at both input and output[45]. However, both these topologies lack a controllable high voltage dc link with inherent energy storage.

2.2 Proposed Power Conversion Architecture

2.2.1 Power Circuit

The detailed circuit diagram of the proposed power circuit is shown in Fig. 2.1b. It is to be noted that the HF-MMC and the GS-MMC are directly connected as shown and that its not a HVDC line. The entire BB-MMC, the HF-Transformer and the BB-2LVSC are to be housed in the wind turbine nacelle. The HF-transformer is Y-Y connected and the zero sequence currents under grid voltage unbalance cannot flow since the transformer neutral is floating[55]. The end application of the topology targets the use of Silicon Carbide devices and so the total number of modules required to reach up to the medium voltage grid level is accordingly reduced.

2.2.2 PWM Schemes for Subsystems

The GS-MMC sub-modules are modulated using phase-shifted carrier sine-triangle PWM(PSC-PWM) ensuring minimum carrier frequency harmonics in the output voltage. PSC-PWM is especially suited when the number of sub-modules in the MMC are small as is the case here. The effective switching frequency harmonics in the output voltage is at $2N$ times the switching frequency of each sub-module. The HF-MMC is modulated

using nearest level modulation and the output waveform is a sinusoidal stepped waveform. The switching frequencies of the both the HF-MMC and HF side 2l-VSC are the same as the output voltage fundamental frequency across the transformer. The HF side 2L-VSC operates in six-step mode since there are six steps in every fundamental cycle of its line-neutral voltage waveform. Both the sides of the HF transformer don't see PWM waveforms to limit the dv/dt stresses involved if carrier frequency at 10 times the HF link frequency is used for modulation.(show typical waveforms)

2.2.3 Overall System Operation

The GS-MMC controls the currents drawn from the grid for V_{hdc} control, reactive power support to the grid, operation during grid unbalance and faults, virtual inertia support to the grid for frequency regulation and other grid ancillary services. The HF-MMC ensures minimum conduction losses in the HF-link by current harmonic control and controlling the currents to be at unity displacement power factor with the HF-2LVSC. The HF-2LVSC maintains the low voltage dc link at the commanded reference value and the WT-2LVSC is involved in tracking the wind turbine's maximum power point.

2.2.4 Summary of Advantages

The various advantages of the proposed topology mentioned thus far are summarized below:

1. Transformer weight reduction by more than 100 times in WES compared to the line-frequency transformer, so it can be placed in naccelle.
2. Conduction loss in the 300m long droop cables are reduced by T^2 times for a transformer turns ratio of T.
3. A single controllable high-voltage dc link which can be used for grid ancillary services such as frequency regulation.
4. The topology can also be extended to interface PV, energy storage systems and other LV power sources.
5. The possibility to connect multiple MMCs across the same dc link and make it more power dense.

6. A simple control scheme because of uniform modulating signal for all modules of each MMC arm.

7. Increased reliability compared to using a HF transformer in each module such as when energy sources are integrated through dc-dc converters at the sub-module level. This is because only one HF transformer insulation sees MV stresses compared to the case of each HF transformer in the individual sub-modules.

2.3 Analysis of BB-MMC DC-link Voltage

$$V_{aN} = \frac{V_c}{2} + \frac{V_c}{2} M \cos(\omega_m t + \theta_m) + A_F + B_F \tag{2.1}$$

where,

$$A_F = \frac{2V_c}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_o \left(m \frac{\pi}{2} M \right) \sin \left(\frac{m\pi}{2} \right) \cos m(\omega_c t + \theta_c) \tag{2.2}$$

$$B_F = \frac{2V_c}{\pi} \sum_{\substack{n=-\infty \\ n\neq 0}}^{\infty} \sum_{m=1}^{\infty} \frac{1}{m} J_n \left(m \frac{\pi}{2} M \right) \sin \left(\frac{(m+n)\pi}{2} \right) \cos(m(\omega_c t + \theta_c) + n(\omega_m t + \theta_m)) \tag{2.3}$$

Eq. (2.1)-Eq. (2.3) give the harmonic components of a half bridge module's output voltage with respect to the negative of its dc bus[56] with double update sine-PWM. Here, m and n are harmonic orders of the carrier frequency and fundamental frequency voltage components respectively. The pictorial representation of the frequency components in the sub-module output voltage in Fig.2.2 follows from Eq. (2.1)-Eq. (2.3). The terms in A_F result in frequency components at the carrier frequency and its multiples and the terms in B_F give rise to frequency components at the various sidebands around the carrier frequency harmonics.

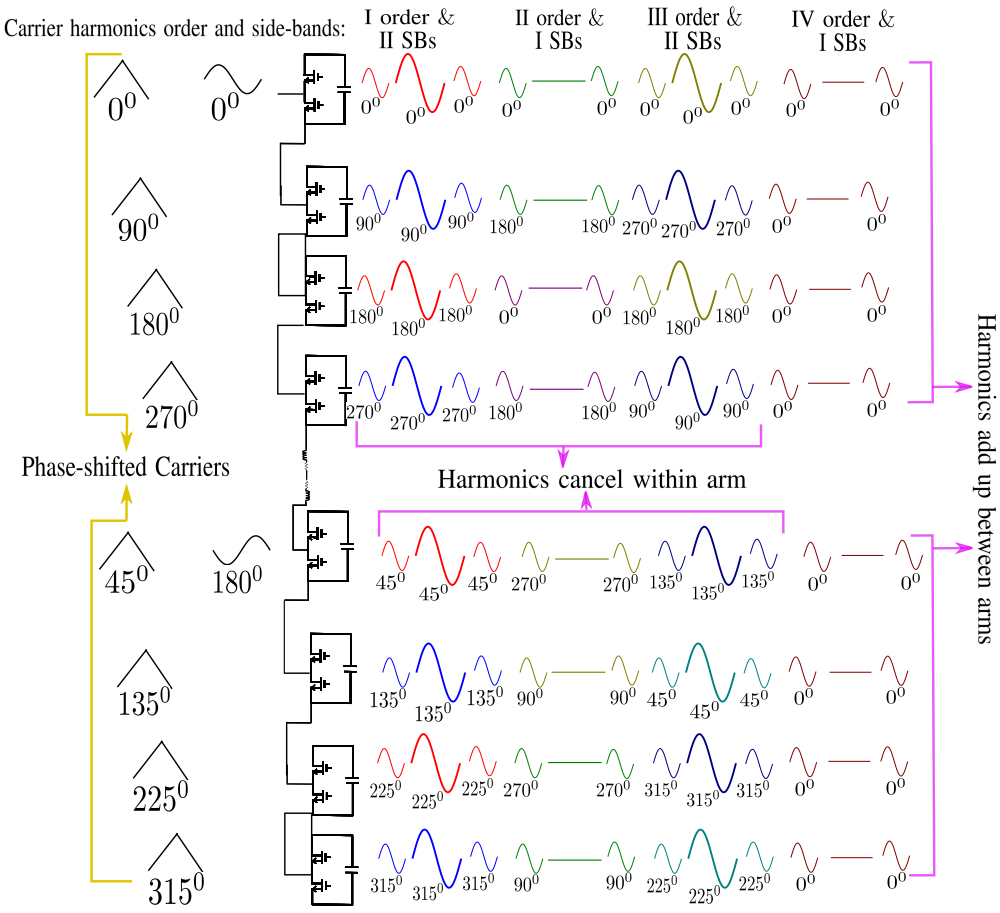


Figure 2.2: Pictorial representation of carrier frequency harmonics and their side-bands that are produced at the output of the half-bridge sub-modules as a result of sin-triangle modulation.

In Fig.2.2, the carrier phase shifts for the lowest harmonic content in the AC output voltage of the MMC, in the case of 8 modules per leg are shown. Also, the various carrier frequency harmonics and their sidebands considering the differential mode component of the modulating signal can be observed. These carrier harmonics and their sidebands cancel in pairs if a 180^0 counterpart is available within the arm as in the case of the I carrier harmonic and its sidebands[57]. They also cancel in pairs if a 0^0 counterpart is available between the two arms as in the case of the IV order carrier harmonic and its sidebands.

It is seen from Fig.2.2 that upon adding the sub-module output voltages in the upper and lower arms from top to bottom, dc bus switching ripples result at a frequency of the sidebands of the IV order carrier harmonic. For N submodules per arm, the switching ripple in fact, contains the sidebands of all odd multiples of Nf_{sw} where, f_{sw} is the grid-side MMC module switching frequency. Between the three phases of the MMC, only the zero-sequence sidebands at third harmonic of the fundamental frequency add up and the magnitude and frequency of the net dc link switching ripple around Nf_{sw} is as shown in Eq. (2.4).

$$\begin{aligned} f_{swr} &= mf_{sw} \pm 3pf_m, \\ \sum V_{sm}^{swr}\Big|_{f_{swr}} &= \frac{4NV_c}{\pi}\sum_n\sum_m \frac{1}{m}J_n\left(m\frac{\pi}{2}M\right) \\ p\,\epsilon\,\mathbb{N}, m &= N(2p-1), n = \pm 3p \end{aligned} \tag{2.4}$$

As an example, with $f_m = 50Hz$ and $f_{sw} = 4\,kHz$, the switching ripple occurs at $15850\,Hz$ and $16150\,Hz$ for $n = 1$ and $N = 4$.

2.4 DC-link Voltage Control Design

2.4.1 Sensing the leg voltage and switching ripple propagation

In Fig.2.3a, the control schematic for the voltage control of the high voltage dc link is shown in case the dc link voltage across the back-to-back connected MMCs is sensed directly. Here, the switching ripples add on to $V_{hdc} = NV_{c,avg}$.

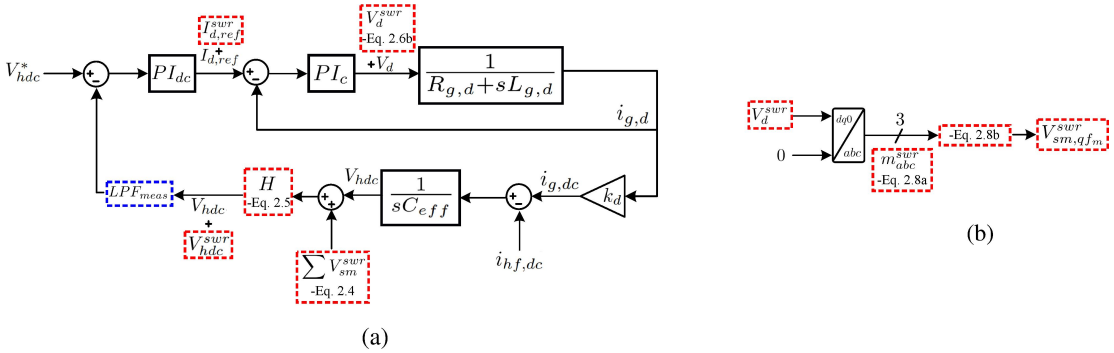


Figure 2.3: (a).PWM switching ripples from the output of cascaded sub-modules propagate through the dc link voltage control loops. (b).Production of even harmonic voltages at the sub-module outputs from the propagated switching ripple voltage components.

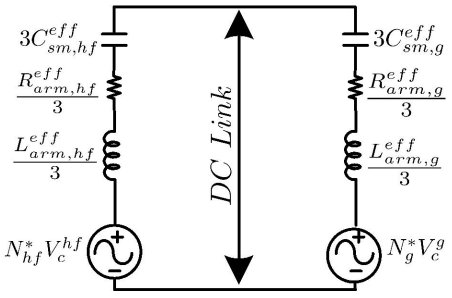


Figure 2.4: BB-MMC equivalent circuit to obtain transfer function of the switching ripple magnitudes from the sub-module outputs to the dc link.

The switching ripple in each leg of the GS-MMC marked as ΣV^{swr}_{sm} or $N^*_g V_{c,g}$ in Fig.2.4 transfer on to the dc link through the voltage transfer function H as shown in Eq. (4.1). N^*_g and N^*_{hf} is the instantaneous number of sub-modules turned on in a phase-leg of the GS-MMC and HF-MMC respectively. An $(N+1)$ modulation is employed at the HF-MMC for the circuit operation in Fig.2.1b and so N^*_{hf} instantaneously stays

constant at N. Thus all the switching ripple originates from the GS-MMC.

$$\begin{aligned} Z_{hf} &= \frac{1}{s\,C^{eff}_{sm,hf}} + R^{eff}_{arm,hf} + s\,L^{eff}_{arm,hf}, \\ Z_g &= \frac{1}{s\,C^{eff}_{sm,g}} + R^{eff}_{arm,g} + s\,L^{eff}_{arm,g} \\ C^{eff}_{sm,g} &= \frac{C_{sm,g}}{N}, C^{eff}_{sm,hf} = \frac{C_{sm,hf}}{N} \\ H &= \frac{Z_{hf}}{Z_{hf}+Z_g} = \frac{V^{swr}_{hdc}}{\Sigma V^{swr}_{sm}} \end{aligned} \tag{2.5}$$

The arm resistances and inductances have been grouped into an effective inductance and resistance in each phase leg and the effective capacitance in the phase leg of the GS-MMC and HF-MMC are $C^{eff}_{sm,g}/N$ and $C^{eff}_{sm,hf}/N$ for switching ripples at frequencies much larger than the HF-link frequency.

$$I^{swr}_d = V^{swr}_{hdc}(LPF_{meas})(PI_{dc}) \tag{2.6a}$$

$$V^{swr}_d = I^{swr}_d(PI_c) \tag{2.6b}$$

$$\begin{aligned} f^{abc}_{swr} &= mf_{sw} \pm (3p \pm 1)f_m, \\ m &= (2p-1)N, p\,\epsilon\,\mathbb{N} \end{aligned} \tag{2.7}$$

$$M^{swr}_{abc}\Big|_{mf_{sw}\pm(3p\pm1)f_m} = \frac{V^{swr}_d}{V_{hdc}}\frac{1}{2}\sqrt{\frac{2}{3}}\left(\frac{2}{V_M}\right) \tag{2.8a}$$

$$V^{swr}_{sm,qf_m} = \frac{2V_c}{\pi}\sum_m \frac{1}{m}J_{-1}\left(m\frac{\pi}{2}M^{swr}_{abc}\right) \tag{2.8b}$$

$$I^{qfm}_{arm} = \frac{V^{swr}_{sm,qfm}}{2R_{arm} + j\omega_{qf_m}\,2L_{arm}} \tag{2.8c}$$

$$q = 3p \pm 1, m = (2p-1)N, p\,\epsilon\,\mathbb{N}$$

Switching ripples thus reaching the dc link voltage through the transfer function H, pass through voltage control loop to create the corresponding components in $V_{d,swr}$,$m_{abc,swr}$ and V^{swr}_{sm,qf_m} as shown in Fig.2.3a and Fig.2.3b and in Eq. (2.6b),Eq. (2.8a) and Eq. (2.8). The output voltages of the half-bridge sub-modules contain even order harmonics similar to the production of sidebands of IV order carrier harmonics in Fig.2.2 due to this propagation. This manifests as common mode voltages between the top and bottom arms and create significant even harmonic circulating currents over and above the the magnitude of such currents due to single phase power absorption.

2.4.2 Proposed DC link voltage Extraction Scheme

The power absorbed by the upper arm of phase a in the MMC is as shown in Eq. (2.9) [58], where I_{dc} is the dc current drawn into each phase-leg from the dc link, V_s is the amplitude of the Grid-side MMC output voltage and I_s is its output AC current.

$$\begin{aligned} P_u = 0.5V_{hdc}I_{dc} - I_{dc}V_s\cos(\omega_g t) + 0.25I_s\,V_{hdc}\cos(\omega_g t - \phi) \\ -0.5I_sV_s\cos(\omega_g t)\cos(\omega_g t - \phi) \end{aligned} \tag{2.9}$$

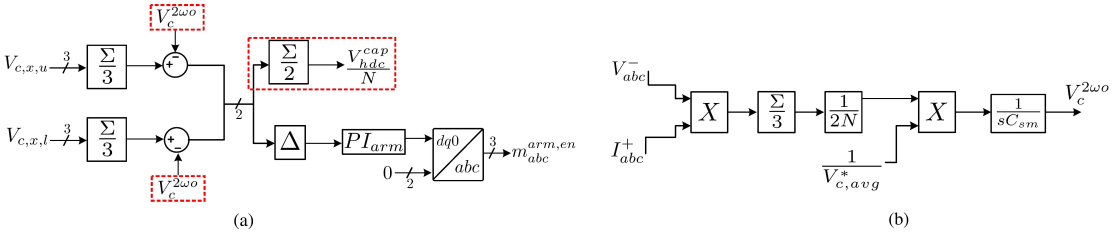


Figure 2.5: (a).Feed-forward cancellation of zero sequence $2\omega_g$ voltage oscillations in the processing of sub-module capacitor voltages to form V^{cap}_{hdc}.(b)Estimation of zero sequence $2\omega_g$ voltage oscillations in the sub-module capacitor voltages under grid voltage unbalance.

In order to use the sub-module capacitor voltages for dc bus voltage control only their dc values are needed and the fundamental frequency and second harmonic voltage

ripples produced due to the last three power terms in Eq. (2.9) need to be canceled out. As shown in Fig.2.5a and Eq. (2.10), towards this, a sample of the sub-module capacitor voltage from each phase of the upper arm are summed and averaged resulting in cancellation of single phase power 2ω voltage oscillations and fundamental frequency voltage ripple. The same is also done with a sample of lower arm sub-module voltage in each phase. In Fig.2.5a, subscript x represents each phase of the MMC and u, l represent upper and lower arms.

$$V_{hdc}^{cap} = \frac{4}{6} \sum_{j=u,l} \sum_{x=a,b,c} V_{c,x,j} \tag{2.10}$$

However, under the case of a grid voltage unbalance, this operation does not eliminate the voltage ripple due to zero sequence 2ω power absorbed in the three phases shown in Eq. (2.11)[59].

$$p_{2\omega o} = 0.5 V_p^+ I_p^- \cos(2\omega_g t + \theta_k^+ + \phi_k^-) + 0.5 V_p^- I_p^+ \cos(2\omega_g t + \theta_k^- + \phi_k^+) \tag{2.11}$$

Eq. (2.11) is used to estimate this zero sequence voltage oscillations in the sub-module capacitors as shown in Fig.2.5b. Here, only the second term contributes to zero sequence power since I^- is controlled to zero by the negative sequence grid current controller. The power due to the second term in Eq. (2.11) in terms of instantaneous phase quantities can be expressed as shown in Eq. (2.12).

$$\begin{aligned}
V_a^- I_a^+ &= (V_p^- \cos(\omega_g t + \theta_k^-)) I_p^+ \cos(\omega_g t + \phi_k^+) \\
&= \frac{V_p^- I_p^+}{2} (\cos(2\omega_g t + \phi_k^+ + \theta_k^-) + \cos(\phi_k^+ - \theta_k^-) \\
V_b^- I_b^+ &= (V_p^- \cos(\omega_g t + \theta_k^- + \frac{2\pi}{3})) I_p^+ \cos(\omega_g t + \phi_k^+ - \frac{2\pi}{3})) \\
&= \frac{V_p^- I_p^+}{2} (\cos(2\omega_g t + \phi_k^+ + \theta_k^-) + \cos(\phi_k^+ - \theta_k^- - \frac{4\pi}{3})) \\
V_c^- I_c^+ &= (V_p^- \cos(\omega_g t + \theta_k^- - \frac{2\pi}{3})) I_p^+ \cos(\omega_g t + \phi_k^+ + \frac{2\pi}{3}) \\
&= \frac{V_p^- I_p^+}{2} (\cos(2\omega_g t + \phi_k^+ + \theta_k^-) + \cos(\phi_k^+ - \theta_k^- + \frac{4\pi}{3}))
\end{aligned} \tag{2.12}$$

Taking the sum of each of the three phase instantaneous powers in Eq. (2.12), the dc quantity cancels out and rest of the power distributes equally to all the $2N$ sub-modules in each phase leg of the MMC. In response, to maintain power balance in the

sub-module dc side, a current flows through the sub-module capacitance which is used to estimate the zero sequence 2ω voltage ripple as shown in Eq. (2.13). $V^*_{c,avg}$ is the reference value of the average capacitor voltages obtained from V^*_{hdc}/N. $V_c^{2\omega o}$ is then fedforward and decoupled from the sensed capacitor voltages as shown in Fig.2.5a and Fig.2.5b.

$$V_c^{2\omega o}(t) = \frac{1}{C_{sm}} \int \frac{V_p^- I_p^+}{4\,N\,V^*_{c,avg}} (\cos(2\omega_g t + \phi_k^+ + \theta_k^-)\,dt \tag{2.13}$$

In Fig.2.5, the processed capacitor voltages are fed to the dc bus voltage control loop and arm energy balancing controller[60].

The effect of not filtering out the zero sequence $2\omega 0$ ripple from capacitor voltages can be explained as follows. Since $2\omega_s$ is close to the bandwidth of the dc bus PI controller, $I_{d,ref}$ signal contains this ripple of amplitude $I_d^{2\omega_g}$ reflected from V_{hdc}^{cap} through the dc bus PI controller. Since $I_{q,ref} = 0$ under grid-side unity power factor operation, the corresponding grid side currents under stationary $\alpha - \beta$ coordinates can be written as shown in Eq. (2.14).

$$\begin{aligned} I_\alpha &= I_d^{2\omega_g} \cos(2\omega_g t)\cos(\omega_g t) \\ &= \frac{1}{2} I_d^{2\omega_g} (\cos(\omega_g t) + \cos(3\omega_g t)) \\ I_\beta &= I_d^{2\omega_g} \cos(2\omega_g t)\sin(\omega_g t) \\ &= \frac{1}{2} I_d^{2\omega_g} (\sin(-\omega_g t) + \sin(3\omega_g t)) \end{aligned} \tag{2.14}$$

$$\begin{aligned} I_a &= I_\alpha \\ I_b &= -\frac{1}{2} I_\alpha + \frac{\sqrt{3}}{2} I_\beta \\ I_c &= -\frac{1}{2} I_\alpha - \frac{\sqrt{3}}{2} I_\beta \end{aligned} \tag{2.15}$$

When converted to three-phase currents using Eq. (2.15), we see that a fundamental frequency negative sequence component results in three-phase output currents.

2.5 Results

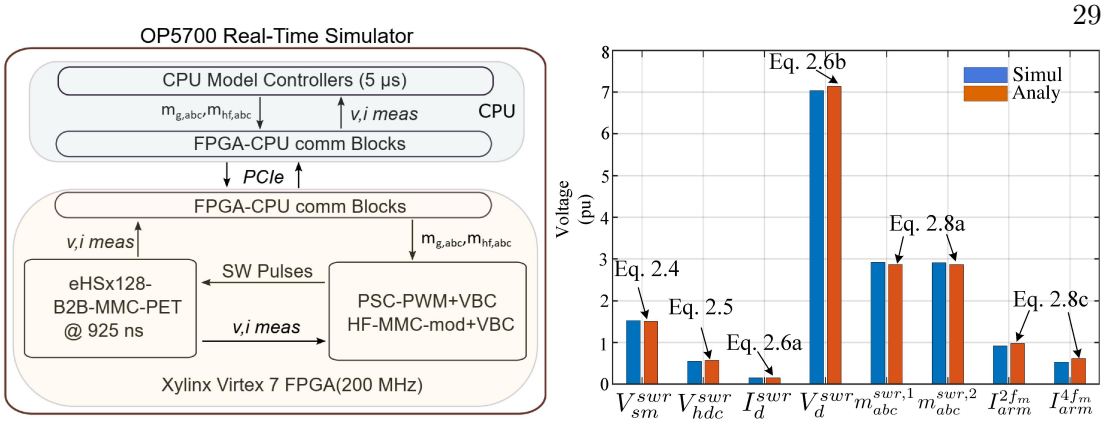
In this section, real-time HIL simulations on OPAL-RT and MATLAB/SIMULINK simulations using the full-scale switching model are conducted and the analytical results

obtained in Section 2.3 and Section 2.4 are verified. Further, the overall operation of the proposed power conversion architecture in Fig. 2.1b is validated. The wind turbine in Fig. 2.1b is emulated by an ideal three-phase AC voltage source.

2.5.1 Circuit and ratings

In the MATLAB/SIMULINK model, both the GS-MMC and the HF-MMC contain eight half-bridge sub-modules per leg with their dc link capacitances being $C_{sm,g} = 5$ mF and $C_{s,hf} = 250\,\mu$F respectively. Their respective arm inductances and resistances are $L_{arm,g} = 4$ mH, $L_{arm,hf} = 200\,\mu$H, $R_{arm,g} = R_{arm,hf} = 0.1\,\Omega$. The GS-MMC and HF-MMC module switching frequencies are 4 kHz and 1 kHz respectively. The grid interface and wind trubine interface R-L filters respectively are $L_g = 16.58$ mH, $R_g = 0.1\,\Omega$, $L_{wind} = 0.35$ mH, $R_{wind} = 0.01\,\Omega$. The rated line-line RMS voltages of the grid and the AC source emulating the wind turbine are 6.1237 kV and 400 V respectively.

In the OPAL-RT based HIL model, the BB-MMCs contain four sub-modules per leg to limit the switch count and reduce the computational burden on OPAL-RT's proprietary real-time power electronic circuit solver block called electrical hardware solver(eHS). Further, to limit overruns on the OP5700 CPU subystem in Fig.2.6a, for the current case of two cores being activated, the BB-2LVSC and the ideal AC source are altogether replaced by an R-L load with a nominal power rating of 250 kW. The minimum possible eHS time step of 925 ns for this circuit was chosen. All other eHS circuit parameters were the same as used in the SIMULINK model.



(a) (b)

Figure 2.6: (a). Block diagram of OP5700 Real-Time simulator with its subsystems (b). Quantitative validation of magnitude of propagated switching ripple at various stages in the control loop.

The eHS and the PWM generation blocks run on the Virtex 7 FPGA of OP5700 at a 200 MHz clock cycle. The PWM blocks were implemented on the FPGA using the RT-XSG toolbox and Xilinx System Generator by creating a custom bitstream. The PI controllers, park transformation blocks and other computations required to generate the modulating signals run on the two Intel CPU cores of OP5700. A block diagram showing the communication between different subystems in OP5700 is shown in Fig.2.6a.

2.5.2 Overall operation

Fig.2.7 validates the overall operation of the power conversion architecture. In Fig.2.7a, a step change in load at the AC source emulating the wind turbine from 600 kW to 720 kW happens at 0.8 sec and the three-phase currents drawn from this source, the HF-link currents and the grid currents undergo a corresponding change in amplitude. Fig.2.7b shows a load change of 250 kW to 300 kW in the OPAL-RT HIL real-time simulation circuit and the associated waveforms. In Fig.2.7c, comparison between grid currents and $I_{d,ref}$ currents with and without the proposed feed-forward estimation and cancellation of the zero-sequence sub-module capacitor voltages are shown. A gird current unbalance of 5% is corrected with the proposed method. Fig.2.7d, shows balanced grid currents being drawn despite using V_{hdc}^{cap} containing the zero-sequence capacitor voltage oscillations, for feedback in the dc bus voltage control loop through

the real-time HIL simulation.

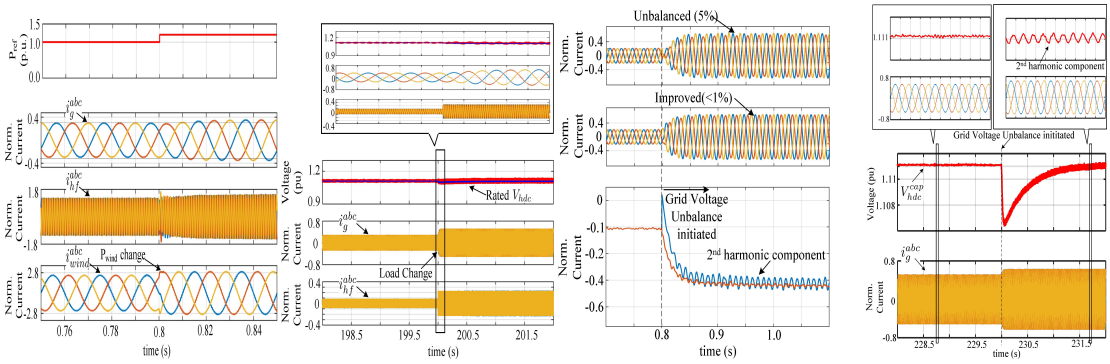


Figure 2.7: (a).Load change at the wind turbine end from 600 kW to 720 kW in the MATLAB/SIMULINK based model(b)Load change at the wind turbine end from 250 kW to 300 kW in the OPAL-RT HIL real-time simulation model(c)Operation under grid unbalance - comparison of three-phase grid currents(top) and $I_{d,ref}$ command(bottom) with and without feed-forward cancellation of $2\omega_g$ voltage oscillations(d) Operation under grid voltage unbalance in the OPAL-RT HIL model, showing balanced three-phase grid currents and $2\omega_g$ capacitor voltage oscillations before feed-forward cancellation

2.5.3 Switching ripple propagation

To ascertain the mechanism of switching ripple propagation, an experiment was conducted with the back-to-back MMCs where the HF MMC was operated with no load connected to its AC output while the Grid-Side MMC remained connected to the grid as shown in Fig.2.8. Operating at no load prevents the single phase power induced second harmonic ripples in the capacitor voltages and i_{cir} containing even harmonics due to switching ripple propagation i.e., $i^{swr}_{cir,2n\omega}$ can be clearly observed. The controller gains for the voltage control loop are $K^{hdc}_p = 0.3685$ and $K^{hdc}_i = 0.0819$ and similarly for the inner current control loop they are $K^c_p = 47.08$ and $K^c_i = 456.6$.

A modulation index of 0.2736 was observed at the grid-side MMC from the simulation of Fig.2.8 for triangular carriers between 0 and 1. Using this and the equations in Section 2.3, the magnitudes of switching ripple propagated at various stages of the

control loop from the simulation are compared with the theoretically expected values as shown in Fig.2.6b. A measurement filter of $15.9kHz$ cut-off filter was used for this experiment and the circulating current is seen to contain even harmonics at no-load as shown in Fig.2.9a. Circulating currents due to PWM ripple propagation are 2.28 times their value without such propagation even at full load condition as seen from the comparison of Fig.2.9a and Fig.2.9b. These currents cause additional capacitor voltage oscillations and in turn deteriorate grid current quality as shown in Section 2.5.4. The circulating currents under no load become negligible with a measurement filter of a low enough cut-off frequency as shown in Fig.2.9b. These results are also validated through real-time HIL simulations as shown in Fig.2.9c and Fig.2.9d.

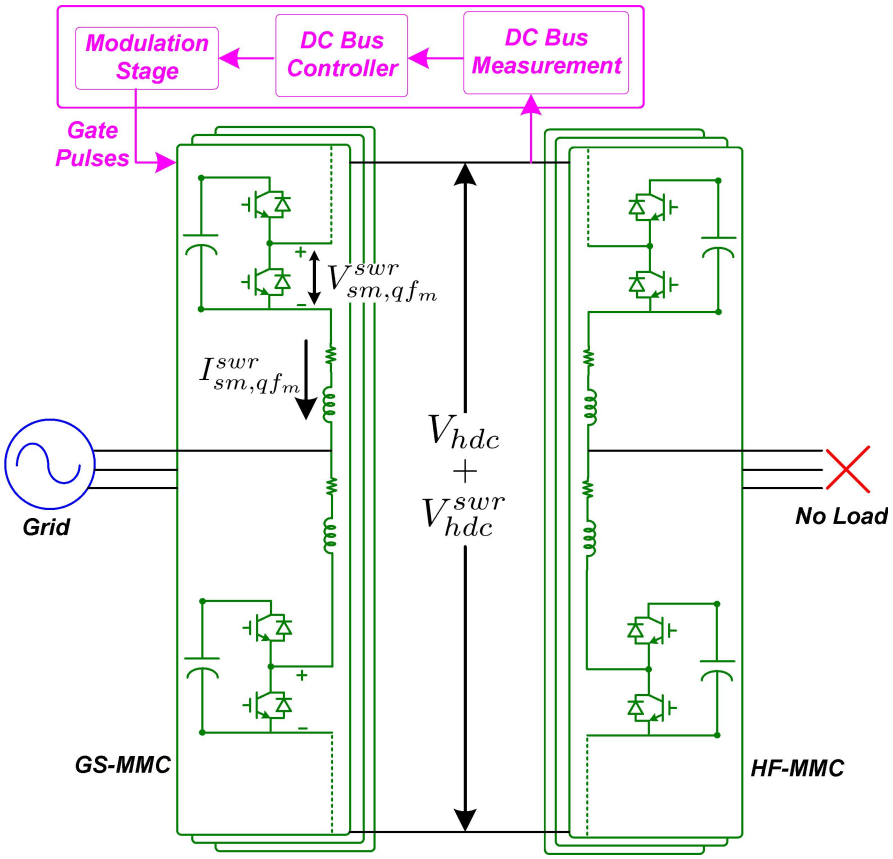


Figure 2.8: Experimental circuit to confirm the flow of I^{swr}_{sm,qf_m} due to switching ripple propagation in the control loops

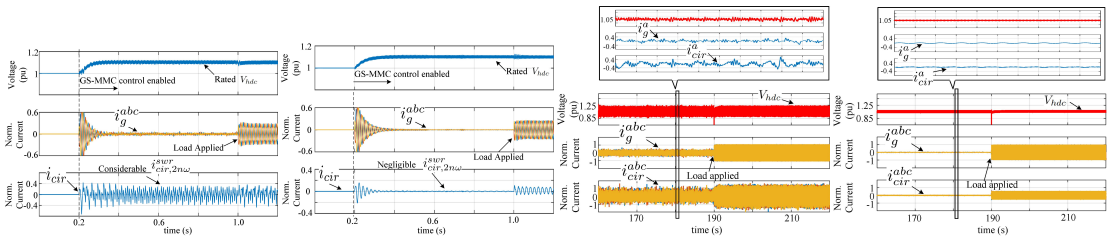
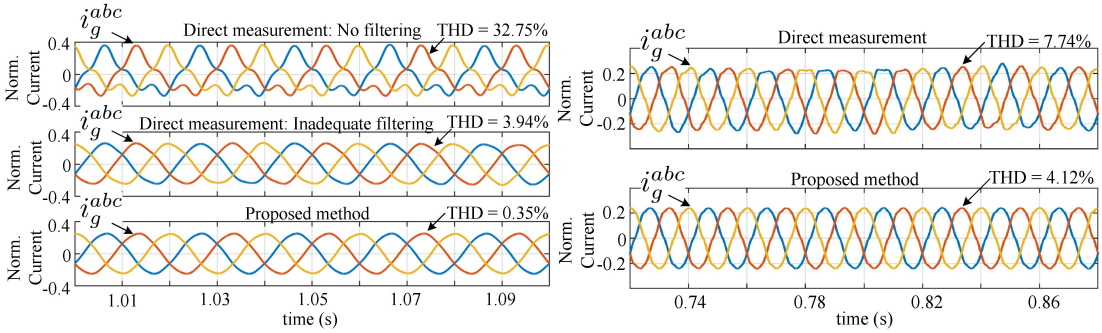


Figure 2.9: (a).Propagated switching ripple in the dc link voltage control loop causes significant even harmonic circulating current under no load -MATLAB/SIMULINK result (b)The same experiment in (a) repeated with sufficient filtering of measured dc link voltage shows negligible even harmonic circulating current under no load (c) Repeat of (a) in the OPAL-RT based HIL real-time simulations (d) No circulating currents under no load with the proposed dc link voltage control - OPAL-RT HIL real-time simulations

2.5.4 Grid current quality

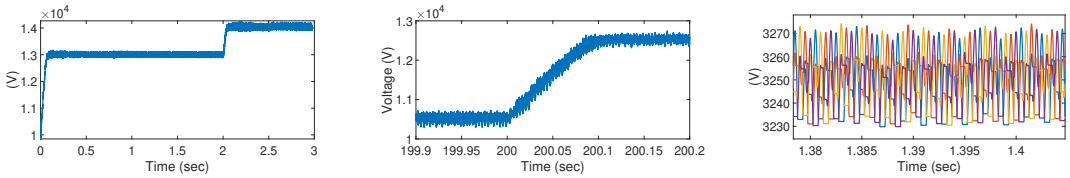
The PWM outputs of the cascaded half-bridges form the leg voltages and the in turn the dc link voltage of the BB-MMC. Using this voltage for feedback purposes in the dc link voltage control loop cause grid current quality to deteriorate even with the use of a suitable measurement filter as shown in Fig.2.10a. For a 4% dead-time for the GS-MMC sub-modules, the grid currents with a $100Hz$ cut-off mesurement filter and the proposed method are shown. Since the PWM outputs contain spurious baseband harmonics due to the effect of deadtime, these harmonics propagate through the dc link voltage control loop and cause additional grid current harmonics as shown in Fig.2.10a. Fig.2.10b shows the comparison of grid side currents for the case of no dead-time and different levels of filtering the measured voltage with the proposed control scheme.



(a) (b)

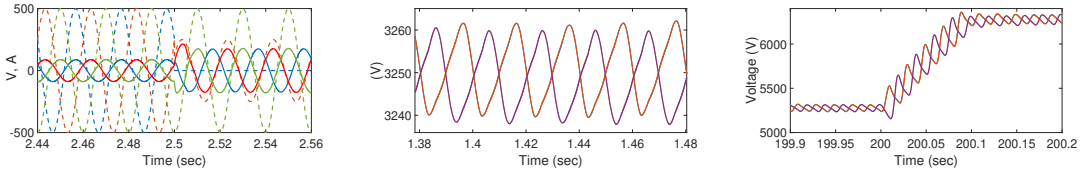
Figure 2.10: (a).Grid currents under the case of directly measuring the dc link voltage (top and middle) and proposed method of dc link voltage control(bottom)(b).Grid currents with 4% deadtime included in the modulation of the half-bridge sub-modules

2.6 DC link voltage control, Current Unbalance Control and Capacitor voltage balancing



(a) (b) (c)

Figure 2.11: (a).DC link voltage waveform across the back-to-back connected MMCs tracks the reference command of 13 kV at the start and a reference command change from 13 kV to 14 kV at 2 sec. -MATLAB/SIMULINK result (b) Repeat of (a) in the OPAL-RT based HIL real-time simulations - step change in dc bus voltage at 200 sec, causes it to increase from 10.5 kV to 12.5 kV. (c)HF link MMC sub-module capacitor voltages in the upper arm of phase-c -MATLAB/SIMULINK results



(a) (b) (c)

Figure 2.12: (a).The grid currents are balanced even after a line-ground fault in phase c and a 50% voltage sag in phase b occurs at 2.5 sec. The grid phase currents are in phase with the grid phase voltage (shown as scaled by 0.1) both before and after the grid unbalance.-MATLAB/SIMULINK result (b)Grid side MMC sub-module capacitor voltages in the upper and lower arms of phase c showing action - MATLAB/SIMULINK results(c) Repeat of (b) in the OPAL-RT based HIL real-time simulations - Grid side-MMC upper and lower arm capacitor voltages are shown to respond to a step change in the reference command for dc bus voltage and changes from 5250 V before 200 sec and at 6250 V after 200.1 sec

The high-voltage dc link voltage is seen to track the step change in reference at 2 sec from 13 kV to 14 kV in Fig.2.11a. The same is repeated in the OPAL-RT HIL simulation in Fig.2.11b. The HF-link MMC capacitor voltages and are shown in Fig.2.11c. The grid voltage undergoes a line-ground fault in phase c and a 50% voltage sag in phase b at 2.5 sec. During this disturbance the grid side currents are maintained to be balanced and at unity power factor with the grid in Fig.2.12a. The Grid-side MMC capacitor voltages are shown in Fig.2.12b and Fig.2.12c from the MATLAB/SIMULINk and OPAL-RT HIL simulations respectively. Arm energy balancing controller ensures the upper and lower arm capacitor voltages vary together and the second harmonic capacitor circulating current controller ensures a predominant fundamental ripple voltage component in the grid side capacitor voltages.

2.7 Summary

The frequency components in the DC link voltage across the back-to-back connected MMCs in the PET was analyzed. Further their magnitude as they propagate through

the control loops were quantitatively characterized. A dc link voltage sensing and control scheme was presented which ensures grid current quality does not deteriorate due its implementation. Ancillary servies to the grid such as load independent power factor control on the grid side, operation under grid voltage unbalance and control of the dc link voltage across the back-to-back connected MMCs have been demostrated. A brief comparison of the studied topology with other medium voltage grid integration topologies was presented. MATLAB/SIMULINK and OPAL-RT based HIL simulation results confirmed the designed control schemes of the back-to-back connected MMC based PET operation.

Chapter 3

An Online Optimization-Based Control Scheme for the High-Frequency link in a Back-to-Back Connected MMC-based Power Conversion Architecture for Wind Energy Systems

In Chapter 2, the effect of dc bus switching ripples on the grid-side MMC control schemes was discussed and a comparison of this topology with other medium voltage grid integration topologies was provided.

A summary of the novel contributions of this chapter are as follows:

1). The control schemes of the HF-MMC and the 2L-VSC connected across the HF transformer in Fig.3.1 to enable controlled and efficient power transfer are presented.

2). An online optimization based modulation scheme for the HF link MMC is developed to minimize the net root-mean-squared (rms) value due to the harmonics in the high-frequency link currents. In addition, this modulation scheme allows control of the MMC output voltage fundamental magnitude which has been employed in closed loop to achieve unity displacement power factor with the low voltage side converter.

The optimization problem is based on coordinate gradient descent method and it optimizes the switching angles in the output voltage of the HF-MMC. Detailed simulation results verifying the analysis and control are presented in MATLAB/SIMULINK. Further verification of the designed control schemes for power transfer through the topology is achieved through OPAL-RT based hardware-in-loop (HIL) real-time simulations and hardware experimental results.

3.1 Introduction

In [52], a single MMC based power electronic transformer was studied but losses in HF link resistance was not considered and the application was for power transfer from a low voltage dc source to a medium voltage dc source. Minimization of the fundamental component of the link current or its harmonics was not considered which cause associated conduction losses in the winding resistance[61, 62].

[63, 64] show minimization of voltage harmonics in the MMC output voltage waveform through the Selective Harmonic Elimination (SHE) method. However, only a particular harmonic component, example, 5th harmonic of the MMC output voltage waveform is targeted to be minimized. Other works on reduced frequency modulation of MMCs involve improvements in capacitor voltage balancing schemes[52] and circulating current supression [65]. In [66, 67], a nearest level PWM method for an MMC connected to the medium voltage grid was presented which showed improvement in both the output current harmonics and in the MMC output voltage. However, there is PWM occurring at each level which causes higher dv/dt stresses on the high-frequency transformer as opposed to a simple staircase waveform employed in this paper.

In [68, 69], the switching angles of the mutlilevel waveform were optimized based on Newton's method to improve the voltage harmonic profile subject to a fundamental

magnitude constraint. To address the convergence sensitivity of Newton's method to starting points of the switching angles, particle swarm optimization (PSO) algorithms were used in [70]. In [71], genetic algorithms were used to solve the transcendental non-linear equations offline, for zero voltage harmonics in the output and the solutions were stored in look-up tables. In [72], a universal formulation showing various alternative algorithms at the different stages of the optimization process was presented. In [73], gradient descent based optimization of the switching angles are discussed but not used for closed-loop operation and also did not employ the full gradient equations.

In contrast to the work mentioned above, the focus in this paper is on output current harmonic control instead of control of the harmonics in the output voltage, with simultaneous output fundamental voltage magnitude control for closed loop unity displacement power factor operation. This minimizes the conduction losses due to kAs of current through the HF transformer and the low voltage side converter. The harmonic minimization technique is different from SHE since it can include any number of harmonics in the objective function to be minimized. Moreover, it solves for the minimum possible value of the resultant harmonic rms value rather than an absolute zero value of each harmonic as in SHE, for which solutions may not exist as more harmonics are included for all operating conditions. Also, a different converter interface where the MMC is injecting current through a high-frequency transformer against the six-step voltage waveform presented by the two-level converter is considered. The online optimization problem framework dynamically reacts to changes in load angle, magnitude reference command and changes in the high voltage dc link voltage across the back-to-back connected MMCs to output an optimum set of switching angles. The optimization formulation is such that computational burden on the solver can be adjusted by the iteration number k within each CPU time-step to suit the available processing power.

A standard sine wave is used as the modulating signal and it avoids the need for generating a special modulating signal to achieve harmonics minimation using multiple PI/PIR controllers[74, 75]. This is because this objective is captured in optimization cost function and the resulting control of the switching angles of the MMC output voltage waveform.

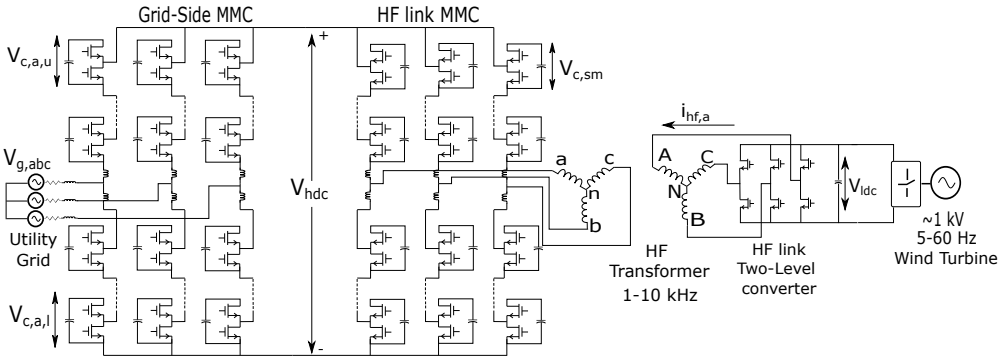


Figure 3.1: Detailed circuit diagram of the proposed BB-MMC PET architecture

The detailed circuit diagram of the PET interface is shown again in Fig.3.1 for convenience. Circuit topology, overall operation and the basic introduction to PWM schemes of the different converters involved are provided in Chapter 1.

3.2 Proposed Low-Voltage side DC-bus Control

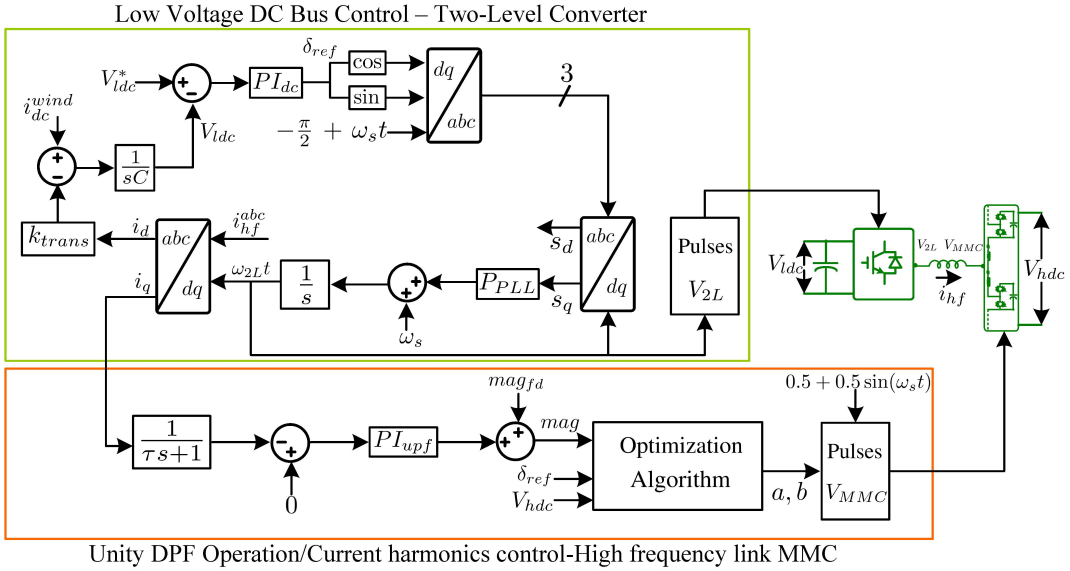


Figure 3.2: High frequency link control schematic - low voltage dc bus control by the HF-link 2L-VSC and the unity displacement power factor control and HF-link current harmonics control by the HF-MMC.

The dc bus of the 2L-VSC at the high frequency link is controlled by adjusting the phase angle of its six-step output voltage waveform with respect to the staircase voltage waveform of the MMC. As shown in Fig.3.2, a dc bus PI controller generates a reference load angle, δ in response to the error in the voltage of the low voltage dc link from a set reference voltage. Taking cosine and sine of this load angle generates arbitrary d and q component signals. Since the MMC is fed a constant modulating signal as shown in Fig.3.2, these d-q components are transformed to a three-phase signal using instantaneous phase angle of the HF-MMC modulating signal space vector, $\omega_s t$. This three-phase signal will now be at a load angle δ with respect to the MMC output voltage. A PLL tracks this three-phase signal forming a two-loop control scheme with a slower dc bus voltage control loop generating the load angle and the inner PLL loop tracking this reference load angle. The phase angle tracked by the PLL is used to synthesize the six-step waveform of the two level converter.

3.3 Control of HF-Link Current and Power Flow

In the conventional nearest level modulation scheme, the switching angles in the staircase waveform are produced when the modulating signal such as a sine wave varying between 0-1 crosses constant values chosen in the same range. For an example of 4 modules per arm, the modules of the bottom arm of the HF-MMC that are inserted, N_{ON} is determined according to Eq. (4.34) by this scheme[76].

$$\begin{aligned} m_a = 0.5 + 0.5\,(m_{hf})\,sin(\omega_s t), 0 \leq m_{hf} \leq 1 \\ N_{ON} = round_{0.5}(N m_a) \\ m_a \geq 0.875, \text{ all 4 modules ON} \\ 0.875 > m_a \geq 0.625, \text{ 3 modules ON} \\ 0.625 > m_a \geq 0.375, \text{ 2 modules ON} \\ 0.375 > m_a \geq 0.125, \text{ 1 modules ON} \\ 0.125 > m_a \geq 0, \text{ 0 modules ON} \end{aligned} \tag{3.1}$$

Although, closed loop control of the magnitude of the fundamental component of the output voltage by adjusting the magnitude of this sine wave is possible, this scheme may not fully utilize the complete range of magnitude control available. This can be

seen from Eq. (3.3), where the maximum magnitude of the fundamental component is $\frac{4\,V_c}{\pi}\,\frac{N}{2}$. For $N = 4$, this is $\frac{4\,V_c}{\pi}\,2$. In comparison for the maximum modulation index of $m_{hf} = 1.15$ in Eq. (4.34) made possible with the injection of a three-phase common mode signal to m_a, the corresponding magnitude of the fundamental is $\frac{4\,V_c}{\pi}\,1.88$. Moreover, the resulting switching angles in the MMC output voltage are not optimized to minimize the magnitude of the current harmonics flowing out of the MMC AC terminals.

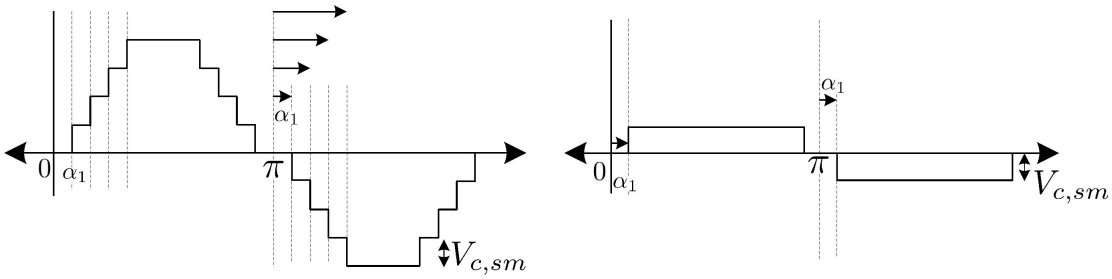


Figure 3.3: Typical MMC output voltage with respect to its dc bus midpoint in case of 8 modules per arm(left) and its first quasi-square wave component corresponding to the first switching angle(right).

A typical nearest level modulated voltage waveform with respect to the dc bus midpoint of the MMC is shown in Fig.3.3 alongside its first quasi square wave component. It can be seen that the voltage waveform in on the left can be viewed as a sum of many such quasi square wave components each with a different phase shift α_i. Also, each of these components is symmetric about a half-cycle and its Fourier series expansion consists of only the odd harmonic sinusoidal terms with their amplitude given by Eq. (3.2). An $N + 1$ modulation scheme is employed here, where $N + 1$ is the number of levels in the output voltage and N is the number of sub-modules per arm. In this scheme, the upper and lower arm modules are switched complementary to each other. The number of independent switching angles is equal to half the total number of sub-modules in an arm of the MMC owing to the symmetry in the positive and negative halves of the output AC waveform.

$$b_p = \frac{4V_{c,sm}}{(2p-1)\,\pi} cos((2p-1)\alpha_i),\; i = 1,..\frac{N}{2},\; p\,\epsilon\,\mathbb{N} \tag{3.2}$$

Using Eq. (3.2), amplitude of the k^{th} harmonic in the Fourier expansion of the resultant staircase waveform is as shown in Eq. (3.3).

$$b_k, NLM = \sum_{i=1}^{\frac{N}{2}} \frac{4V_{c,sm}}{k\pi} cos(k\alpha_i),\ k\ =\ 1, 3, 5.. \tag{3.3}$$

In Fig.3.4, the pole voltages of the MMC and the 2L-VSC with respect to the imaginary midpoints of their dc buses (dashed-dotted lines) and with respect to the transformer neutral points (solid lines) are shown.

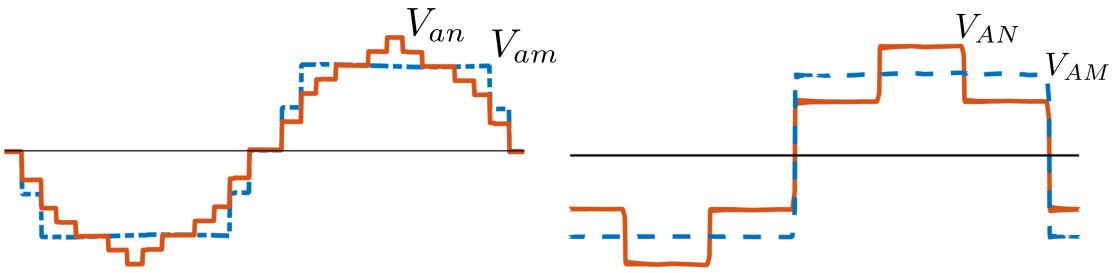


Figure 3.4: HF-MMC output voltage with respect to transformer neutral V_{an},its dc bus midpoint V_{am}, 2L-VSC output voltage with respect to transformer neutral V_{AN}, and its dc bus midpoint V_{AM}

To form the minimization objective function in terms of the current harmonics, only voltages of either converters with respect to their virtual dc bus mid-points i.e., V_{am} and V_{AM} are required. This is due to the fact that voltages with respect to the neutral point of the transformer are only improved in terms of the third harmonic component and other triplen harmonics of these voltages. For example, the $5^{th}, 7^{th}$ and 11^{th} harmonic components in V_{AN} are the same as in V_{AM}. The same is true of the MMC voltages V_{an} and V_{am}. The neutral point on the MMC side of the transformer is left floating to avoid zero sequence currents from the grid during grid unbalance [77] and these triplen

harmonic currents also cannot flow.

$$\begin{aligned} V_{AM} &= \sum_{k=1,3,5,..} \frac{4\,V_{ldc}/2}{k\pi} sin\, k(\omega t + \delta) \\ V_{am} &= \sum_{k=1,3,5,..} b_{k,NLM}\, sin\, k(\omega t) \end{aligned} \tag{3.4}$$

Assuming the six-step waveform of the two-level converter to lead the MMC voltage by an angle δ, V_{AM} and V_{am} in Fig.3.4, can be written as shown in Eq. (3.4).

The optimization function can now be formed to minimize the HF-link current harmonics as shown in Eq. (3.6)-Eq. (3.7). $V_{cm}^{'}$ is the MMC sub-module voltage at the nominal value of V_{hdc} referred to the transformer low voltage side as shown in Eq. (3.5). V_{MMC} in Eq. (3.7) is the fundamental component of the MMC voltage referred to the low voltage side. X_{hf} is the leakage reactance at the fundamental frequency of the HF-link in Eq. (3.5) and T_r is the transformer turns ratio.

$$V_{c,sm}^{'} = \frac{V_{hdc,nom}}{NT_r},\; X_{hf} = 2\pi f_s\, L_{hf} \tag{3.5}$$

$$min\, f = \sum_{n=5,7,11} \frac{1}{2\,X_{hf}^2\, n^4} (\sum_i \frac{4V_{c,sm}^{'}}{\pi} cos(n\alpha_i) - \frac{4V_{ldc}/2}{\pi} cos(n\delta))^2 \tag{3.6}$$

subject to the constraint,

$$\sum_i \frac{4V_{c,sm}^{'}}{\pi} cos\, \alpha_i = V_{MMC} \tag{3.7}$$

Note that the $cos(k\,\omega t)$ terms in V_{AM} of Eq. (3.4) have been dropped since they are in quadrature to the HF-MMC voltage and cannot be minimized through the choice of switching angles α_1, α_2.

Eq. (3.6) and Eq. (3.7) have been further modified using Eq. (3.8) for feeding into the designed algorithm as shown in Eq. (3.9), where a and b are now the switching angles.

$$\begin{aligned} k_f &= \frac{0.5 V_{ldc}}{V_{c,sm}^{'}}, \\ mag &= \frac{V_{MMC}}{\frac{4V_{c,sm}^{'}}{\pi}} \end{aligned} \tag{3.8}$$

The minimization of Eq. (3.9) is equivalent to the minimization of the function in Eq. (3.6).

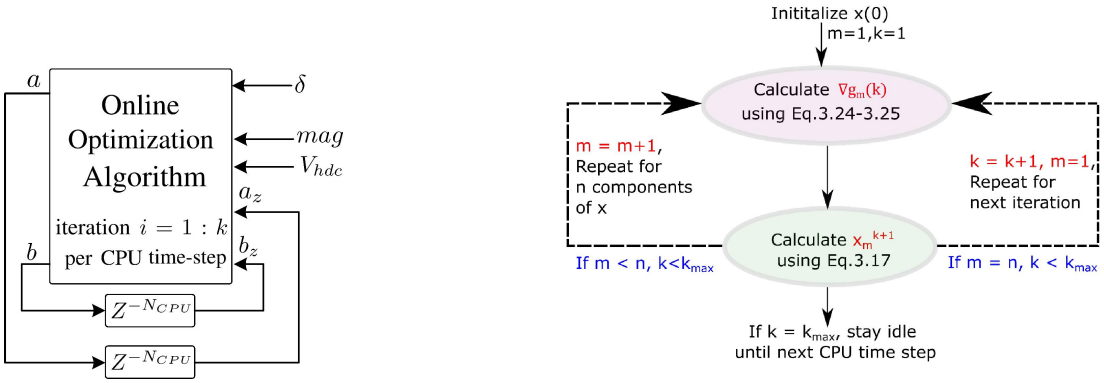


Figure 3.5: A block diagram of the designed online optimization algorithm (left) and Progression of coordinate descent algorithm implemented at each iteration(right).

$$\begin{aligned} min\ f = \sum_{n=5,7,11} \frac{1}{2\,n^4}\Big(\sum_i cos(n\alpha_i) - (k_f)cos(n\delta)\Big)^2 \\ s.t.\ \sum_i cos(\alpha_i) - mag = 0 \end{aligned} \tag{3.9}$$

Forming the Lagrangian for the current optimization problem [78, 79], Eq. (3.10) is obtained.

$$L(x,\lambda) = \sum_{n=5,7,11} \frac{1}{2\,n^4}\Big(\sum_i cos(n\alpha_i) - (k_f)cos(n\delta)\Big)^2 + \lambda\,\Big(\sum_i cos(\alpha_i) - mag\Big) \tag{3.10}$$

In addition to the constraint on MMC fundamental voltage magnitude in Eq. (3.9), it is also possible to view the optimization problem with inequality constraints on the switching angles, $0 \leq \alpha_i \leq \pi/2$. However, it is observed that these inequalities are almost always inactive meaning that the optimal solutions don't exist at the boundaries of these inequalities and they can be discarded.

In order to apply the Karush-Kuhn-Tucker Necessary conditions (KKT conditions) for a minimum [79] with the Lagrangian in Eq. (3.10), the gradients of the lagrangians in Eq. (3.11) should be set to zero.

$$\begin{aligned}\nabla_{\alpha_i} L = A_L(-sin(11\alpha_i)) + B_L(-sin(5\alpha_i)) + \\ C_L(-sin(7\alpha_i)) + \lambda(-sin(\alpha_i)) \\ \nabla_\lambda L = \sum_i cos(\alpha_i) - mag\end{aligned} \tag{3.11}$$

where A_L, B_L and C_L are as defined in Eq. (3.12).

$$\begin{aligned}A_L = \frac{1}{11^3}\,(\sum_i cos(11\alpha_i) - k_f\, cos(11\delta)) \\ B_L = \frac{1}{5^3}\,(\sum_i cos(5\alpha_i) - k_f\, cos(5\delta)) \\ C_L = \frac{1}{7^3}\,(\sum_i cos(7\alpha_i) - k_f\, cos(7\delta))\end{aligned} \tag{3.12}$$

These gradients $\nabla_{\alpha_i} L$ and $\nabla_\lambda L$ are set to zero by forming another optimization problem as shown in Eq. (3.13).

$$min\, g = \frac{1}{2}||\nabla||^2, \nabla = \Big(\nabla_{\alpha_1} L, \nabla_{\alpha_2} L, ., ., \nabla_\lambda L\Big)' \tag{3.13}$$

This minimization problem is solved using coordinate gradient descent method[80, 81] described below. Each optimization variable is updated as per Eq. (3.14) where the step sizes β_i and the partial derivatives of the cost g, $\nabla_i g$ are used to update the components x_i. Note that the value of the component, say x_1, at the $(k+1)^{th}$ iteration is used to calculate $\nabla_2 g$ for updating the next component x_2[80].

$$\begin{aligned}x_1^{k+1} = x_1^k - \beta_1\, \nabla_1 g(x_1^k, x_2^k, .., x_m^k) \\ x_2^{k+1} = x_2^k - \beta_2\, \nabla_2 g(x_1^{k+1}, x_2^k, ..x_m^k)\end{aligned} \tag{3.14}$$

For the current problem, with 4 sub-modules per arm $\beta_3 = 0.5$, $\beta_1 = \beta_2 = 0.01$ were for the three optimization variables, $\lambda, \alpha_1, \alpha_2$ respectively by observing the values of the hessians. Constant step sizes chosen according to Eq. (3.15) gurantees convergence to a stationary point and Eq. (3.16) holds[81]. In Eq. (3.15), ϵ is a small number greater than zero and L_1 and L_2 are the bounds on the values of the hessians $\nabla_1^2 g$ and $\nabla_2^2 g$.

Termination condition depends on the range of size of the gradients for the optimization problem, and for the current problem the termination condition of $log(norm(\nabla g_m)) =$

-40 was experimentally found to be satisfactory.

$$\begin{aligned} \epsilon \leq \beta_1 \leq \frac{2-\epsilon}{L_1}, \\ \epsilon \leq \beta_2 \leq \frac{2-\epsilon}{L_2}, \\ \epsilon, L_1, L_2 > 0 \end{aligned} \tag{3.15}$$

$$g(x_1^{k+1}, x_2^k, x_3^k) \leq g(x_1^k, x_2^k, x_3^k) \tag{3.16}$$

Thus, the update of each of the components at iteration $k+1$ of the optimization vector $x = \{\alpha_1, \alpha_2, .., \lambda\}$ can be written as shown in Eq. (3.17), where the subscript m denotes the m^{th} optimization variable. The progress of the coordinate descent algorithm is represented pictorially in Fig.3.5. At the end of T_{cpu}, the values of the optimization variables reached thus far are fed back with a delay of N_{CPU} time steps to repeat calculation of the gradients and update of the optimization variables. N_{CPU} is chosen to slow down the response of the optimization block in relation to the control loop around it.

$$x_m^{k+1} = x_m^k - \beta_m \nabla_m g(k) \tag{3.17}$$

The cost function shown in Fig.3.6, formed by the weighted sum of harmonic components of the HF-link current is not convex, and a significant change in the shape of this surface plot might require a new set of starting points for the optimal solution. For example, for the case of 4 sub-modules per arm and two switching angles a, b, the surface plot for $0 < \delta < \pi/25$ is shown on the right in Fig.3.6. The cost surface for $\pi/25 < \delta < \pi/2$ is shown on the left and the starting points a, b were chosen to be $0, \pi/3$ and $\pi/6, \pi/3$ respectively for these two regions of operation. With this choice of starting points, the minimum values of the cost obtained by the algorithm have been observed to be similar to that obtained by the semi-definite programming based MATLAB optimization function, $fmincon$.

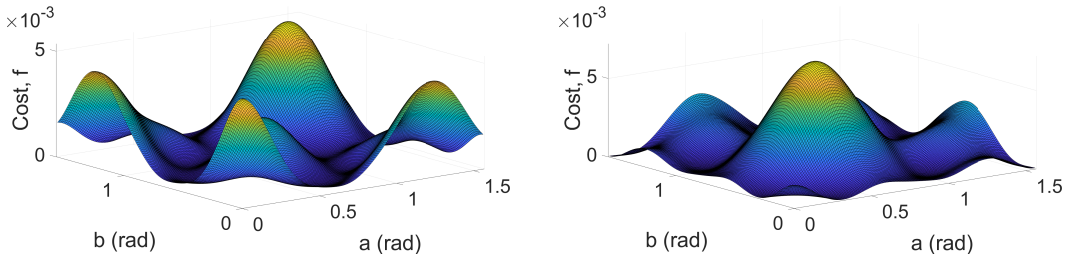


Figure 3.6: (a)Optimization cost surface for higher load angles ($\delta = \pi/4$). (b)Optimization cost surface for low load angles ($\delta = \pi/30$)

A note about the computational complexity of the algorithm is given next. For the calculation of every gradient $\nabla_m g$ corresponding to m^{th} optimization variable in Eq. (3.24), it takes l multiplications and additions, where l is the number of optimization variables. Since there are l different $\nabla_m g$ to be calculated at every iteration, the order of complexity per iteration of the algorithm is $O(l^2)$. The inputs to the optimization formulation namely, the load angle δ, magnitude reference command of V_{MMC} and V_{hdc} are required to not change over the number of cycles required to arrive at the optimum cost of the f in Eq. (3.9). Since these inputs depend on actual power values from renewable energy sources or the grid, the time over which they change are quite large compared to the rate of decrease of cost objective.

3.3.1 Low voltage side Unity Displacement Power Factor operation

Unity displacement power factor (DPF) operation is motivated by the need for the minimum value of the fundamental component of the HF-link current for a given real power transfer. [1]

[1] The fundamental component of the current could also have been absorbed into the minimization objective in Eq. (3.6). This was not done since without a constraint on V_{MMC}, there would be sudden changes in its values for different switching angles solved by the algorithm.

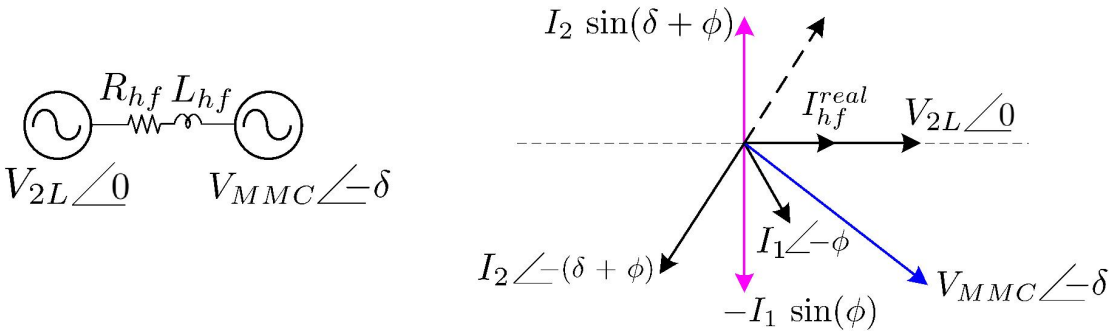


Figure 3.7: (a)Simplified voltage representation across the HF link. (b)Phasor diagram showing the condition for unity displacement power factor operation at the high-frequency link

Using Fig.3.7, the fundamental component of current through the HF link is given by Eq. (3.18).

$$I_{hf} = \frac{V_{2L}\angle 0 - V_{MMC}\angle -\delta}{R_{hf} + jX_{hf}} \tag{3.18}$$

The current through the HF link can be re-written as shown in Eq. (3.19) following from Eq. (3.18). A phasor diagram showing this current with its real and imaginary components is shown in Fig.3.7 where the reference axis is along V_{2L}.

$$\begin{aligned} I_{hf} = I_{real} + jI_{imag} = \\ I_1 cos(\phi) - I_2 cos(\delta+\phi) \\ +j(-I_1 sin(\phi) + I_2 sin(\delta+\phi)) \\ I_1 = \frac{V_{2L}}{\sqrt{R_{hf}^2 + X_{hf}^2}} \\ I_2 = \frac{V_{MMC}}{\sqrt{R_{hf}^2 + X_{hf}^2}} \\ \phi = tan^{-1}(\frac{X_{hf}}{R_{hf}}) \end{aligned} \tag{3.19}$$

Setting I_{imag} of I_{hf} to zero in Eq. (3.19), we get the condition for unity displacement

power factor as shown in Eq. (3.20).

$$V_{2L} = V_{MMC}(cos(\delta) + \frac{R_{hf}}{X_{hf}} sin(\delta))$$
$$V_{MMC} = \frac{V_{2L}}{(cos(\delta) + \frac{R_{hf}}{X_{hf}} sin(\delta))} \tag{3.20}$$

The real power transferred across the HF link through the fundamental voltage components under unity DPF is given by Eq. (3.21). This is derived using $V_{2L}I_{real}$ and substituting for V_{MMC} from Eq. (3.20). The combined effects of harmonic impedance and low harmonic content in the MMC voltage result in negligible power transfer through the voltage harmonics at either end of the HF-link.

It is noted that the $cos(\phi)$ term in Eq. (3.21) is the power loss occurring in the HF link resistance. $\delta + \phi > 90^o$ for power transfer out of V_{2L} and the minimum δ for this is given by $90 - \phi$. As the load angle δ increases making $\delta + \phi$ increase towards 180^o, the power transferred while ensuring unity DPF seems to increase without bound. The maximum power that can be transferred then depends on the maximum value that V_{MMC} can increase to, ensuring unity DPF as per Eq. (3.20).

$$P_{upf} = \frac{V_{2L}^2}{\sqrt{R_{hf}^2 + X_{hf}^2}}(cos(\phi) - sin(\phi)cot(\delta + \phi)) \tag{3.21}$$

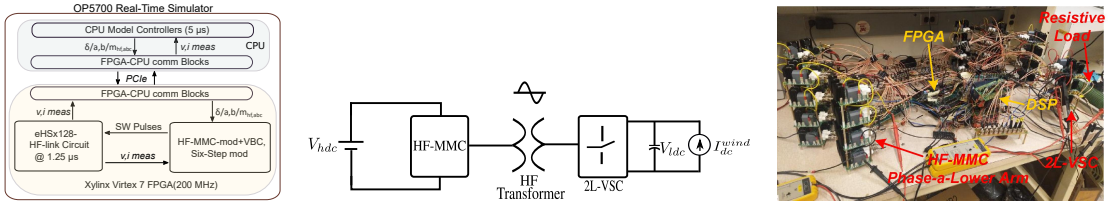
In order to determine how the magnitude of V_{MMC} should be adjusted to control I_{imag} to zero, the q axis component of the current with the d-q frame synchronized to V_{2L} is considered. It is seen that $I_q > 0$ if $I_2\, sin(\delta+\phi)$ is more than $I_1\, sin(\phi)$ and V_{MMC} is decreased to reduce I_q to zero. In decreasing V_{MMC}, delta increases to maintain power flow and this in turn further reduces $I_2\, sin(\delta + \phi)$ since $\delta + \phi$ is more than 90^o, thus ensuring unity DPF. Similarly, if the term due to $I_1 sin(\phi)$ is larger, $I_q < 0$ and V_{MMC} is increased to maintain I_q at zero. The load angle, δ decreases to maintain the same power flow which further increases $I_2 sin(\delta + \phi)$. Thus, the q axis current component of the HF-link current is fed to a PI controller as in Fig.3.2 which in turn outputs a magnitude reference command for the online optimization algorithm.

3.4 Results

In this section, results from the real-time HIL simulations on OPAL-RT, MATLAB/SIMULINK simulations using the full-scale switching model and the experimental hardware setup are presented and the proposed control schemes in Section 3.3 are verified. Further, the overall operation of the proposed power conversion architecture in Fig. 3.1 is validated.

3.4.1 Circuit and Ratings

In the MATLAB/SIMULINK model, both the GS-MMC and the HF-MMC contain eight half-bridge sub-modules per leg with their dc link capacitances being $C_{sm,g} = 5$ mF and $C_{s,hf} = 250\,\mu$F respectively. Their respective arm inductances and resistances are $L_{arm,g} = 4$ mH, $L_{arm,hf} = 200\,\mu$H, $R_{arm,g} = R_{arm,hf} = 0.1\,\Omega$. The GS-MMC and HF-MMC module switching frequencies are 4 kHz and 1 kHz respectively. The grid interface and wind trubine interface R-L filters respectively are $L_g = 16.58$ mH, $R_g = 0.1\,\Omega$, $L_{wind} = 0.35$ mH, $R_{wind} = 0.01\,\Omega$. The rated line-line RMS voltages of the grid and the AC source emulating the wind turbine are 6.1237 kV and 400 V respectively.



(a) (b) (c)

Figure 3.8: (a).Block diagram showing the functions performed by the subsystems of OP5700 real-time simulator (b) Circuit implemented for HF-link control schemes validation through HIL simulation (c)Setup of laboratory-scale experimental hardware prototype

In the OPAL-RT based HIL model, the GS-MMC was removed and the dc link was connected to a fixed voltage source of $13kV$to limit the switch count and reduce the computational burden on OPAL-RT's proprietary real-time power electronic circuit solver block called electrical hardware solver(eHS). Also, the wind turbine and its converter are replaced by a current source connected to the low voltage dc link as shown

in Fig.3.8. The minimum possible eHS time step of 750 ns for this circuit was chosen. All other eHS circuit parameters were the same as used in the SIMULINK model.

The eHS and the PWM generation blocks run on the Virtex 7 FPGA of OP5700 at a 200 MHz clock cycle. The PWM blocks were implemented on the FPGA using the RT-XSG toolbox and Xilinx System Generator by creating a custom bitstream. The PI controllers, park transformation blocks, the optimization algorithm and other computations required to implement the PWM run on the two Intel CPU cores of OP5700. A block diagram showing the communication between different subystems in OP5700 is shown in Fig.3.8. To suit the processing power of the solver used, the number of iterations per time step in Fig.3.5 can be any number ≥ 1. For MATLAB/SIMULINK based simulations the number of iterations per CPU time step was $k = 200$ for a simulation time step of $1.25\mu s$. However, for the OPAL-RT based real-time simulations $k = 1$ was used to reduce the computational burden on the CPU core in OP5700 real time simulator.

The hardware experimental setup consists of a resistive load of $10\,\Omega$ replacing the current source in Fig.3.8. A load change is implemented using a circuit breaker which completes path to another resistive load of 47Ω connected in parallel. The HF-transformer is replaced by a three-phase R-L branch of $330\mu H$ and 0.1Ω. The rated MMC dc link voltage is 75V and the low voltage dc bus is controlled to be 40V. A 2L-VSC dc link capacitance of $3.3mF$. The HF-MMC arm inductors and sub-module capacitors are of values $26\mu H$ and $80\mu F$ respectively. The operating frequency of the HF-link is $1111\,Hz$. The voltage balancing algorithm and the PWM pulses for the MMC sub-modules are implemented on the Zynq7000/Zedboard FPGA platform while the optimization block, the PLL and the PI controllers in Fig.3.2 are implemented on two TMS320F28335 experimenter boards. The required signals for synchronization between the three controller boards are exchanged through GPIO pin-outs. Photographs of the experimental setup is provided in Fig.3.8c and also in Section A.0.1.

3.4.2 Overall operation

The functioning of the HF-link control scheme can be observed from Fig.3.10. Unity displacement power factor operation starts at 0.2 sec when it can be seen that the q axis HF-link current drops to zero from a value of 313.5 A. A positive q-axis current means

that the MMC fundamental voltage magnitude at the feed-forward value of $mag = 1.8$ was more than required to maintain unity DPF and accordingly its value was reduced to the required value of 1.4 by the V_{mmc} magnitude PI controller and the optimization block. Upon the onset of unity DPF, the peak value of fundamental current decreased from 709.4 A to 606.6 A in Fig.3.9c. In response to a decrease in mag to maintain unity DPF, the load angle δ increases from 0.5046 rad to 0.5682 rad to settle to a new operating point for transferring the given power at 0.2 sec. The decrease of V_{MMC} and increase of δ both complement decrease of I_{hf} from a positive value to zero as explained in Section3.3.1. mag and δ obey Eq. (3.20) during unity DPF operation for this new value of δ of 0.5682 rad.

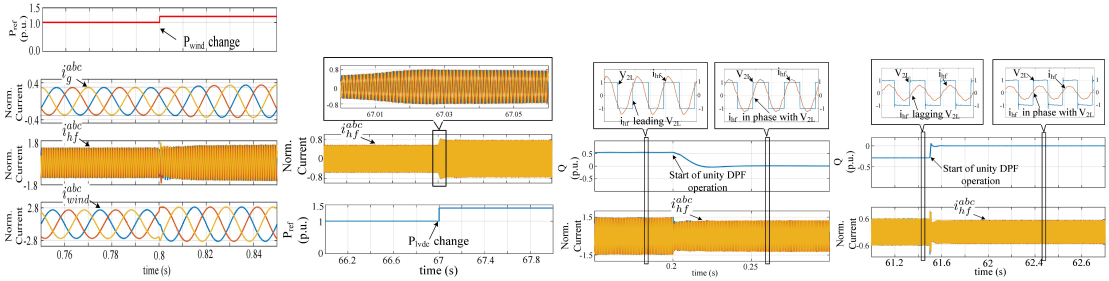


Figure 3.9: Load change implemented with the (a).MATLAB/SIMULINK simulation.(b)OPAL-RT HIL simulation.Unity DPF operation on the (c). MATLAB/SIMULINK model.(d) OPAL-RT HIL model

At 0.8 sec there is a step change in power input from the AC source emulating the wind turbine, from $3 * 200kW$ to $3 * 240kW$ as seen from the the currents in Fig.3.9a changing from a peak amplitude of 1222 A to 1470 A. In response to the step change in wind power at 0.8 sec, the load angle δ also increases from 0.5682 rad to 0.6464 rad to transfer more power resulting in higher values of three-phase HF-link currents with a fundamental magnitude of about 720 A as seen from Fig.3.9a. The mag command reference also increases to 1.493 as per Eq. (3.20) at this load change.

The low voltage dc link is regulated to be at 1000V through all these changes in operation with a peak-to-peak ripple of 20 V. At 2 sec, the high-voltage dc link value

is given a step change in reference from 13 kV to 14 kV and accordingly, the *mag* command now decreases from 1.493 to 1.385 to maintain unity DPF in Fig.3.10. The load angle is observed to not change at 2 sec since the power transferred from the wind turbine end is not changing and the resultant V_{MMC} presented by the combined effects of increase of V_{hdc} and decrease of *mag* does not change.

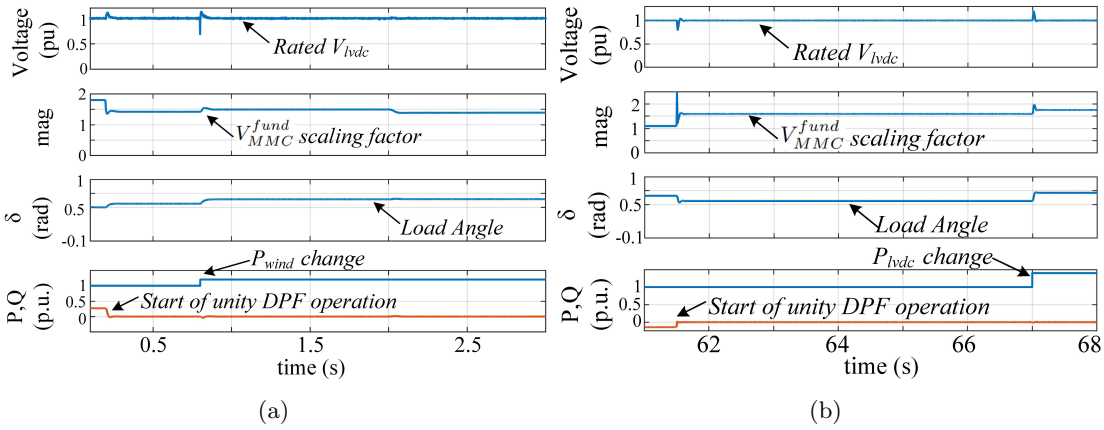


Figure 3.10: HF-link control scheme verification on (a).MATLAB/SIMULINK model (b).OPAL-RT HIL model

In the OPAL-RT HIL simulations, the three-phase HF-link currents decrease from a peak amplitude of 293 A to 260 A in response to the start of unity displacement power factor operation at 61.5 sec as shown in Fig.3.9d. In Fig.3.9b, a step change in load from 83.33 kW per phase (low voltage dc-link input current of 250 A) to 116.67 kW per phase (dc-link input current of 350 A) at 67 sec causes an increase of the peak fundamental amplitude of the current from 260 A to 365 A.

In Fig.3.10, the various HF-link control schemes in Fig.3.2 are verified through OPAL-RT real-time HIL simulations. The control variables δ, *mag* and the HF-link q axis current $I_{hf,q}$ are shown. It observed that *mag* increases from a feed-forward value of 1.1, to 1.595 at 61.5 sec upon enabling unity DPF operation to control a negative $I_{hf,q}$ to zero. To maintain the same power transfer, δ correspondingly changes from 0.6598 rad to 0.5656 rad at 61.5 sec following Eq. (3.20). It increases from 0.5656

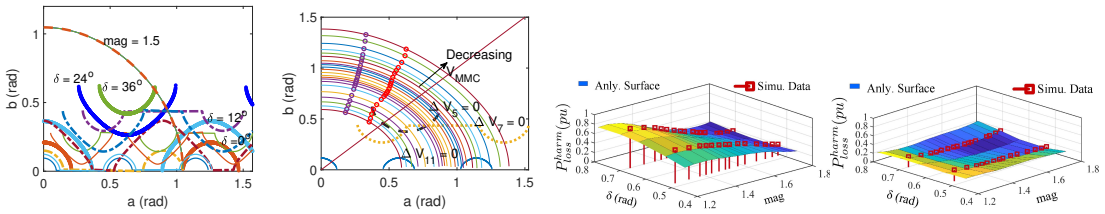
rad to 0.7122 rad responding to step change in power input at 67 sec to maintain the low voltage side dc bus at 1000 V. Correspondingly, *mag* increases again at 67 sec from 1.595 to 1.754 obeying Eq. (3.20).

In Fig.3.10, the low voltage side dc bus voltage is controlled to a constant value at 1000 V quickly rejecting the disturbance due to start of unity DPF at 61.5 sec and the load change disturbance at 67 sec.

3.4.3 Switching Angle Trajectory

In Fig.3.11b, the switching angle contours a vs b along zero values of $5^{th}, 7^{th}$ and 11^{th} harmonic voltages across the HF link for various values of load angles as a parameter are shown. The zeros of the harmonics lie on solutions of Eq. (3.22). k_f defined in Eq. (3.8) is a factor that depends on the ratios of V_{ldc} and V_{hdc} voltages.

$$cos(na) + cos(nb) - (k_f)cos(n\delta) = 0 \tag{3.22}$$



(a) (b) (c) (d)

Figure 3.11: (a)Zero harmonics contours for the case of two switching angles.(b)Comparison of switching angles solutions under conventional and proposed modulation schemes.(c)Surface plot of harmonics rms values with conventional modulation scheme.(d)Surface plot of harmonics rms values with proposed modulation scheme.

For a given voltage magnitude of the MMC output AC voltage, switching angles simultaneously satisfying the magnitude constraint and closest to the zero harmonic voltage contours are chosen by the optimization algorithm. This is illustrated in Fig.3.11a where the zero harmonic voltage contours have been plotted considering an example load

angle of $\pi/6$. The magnitude contours closer to the origin correspond to higher MMC fundamental voltage magnitudes and they have been plotted as solutions of Eq. (3.23), for various values of mag.

$$cos(a) + cos(b) = mag \tag{3.23}$$

The red circles indicate the switching angles solved by the proposed optimization algorithm. Note that the switching angles are all towards the top of the $x = y$ line indicating that b, the second switching angle is more than a, the first switching angle.

3.4.4 HF-link current harmonics reduction

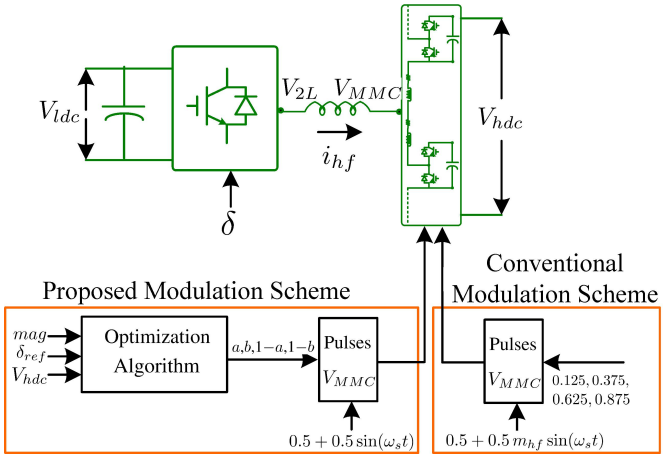


Figure 3.12: Simulation circuit to compare rms-squared values of HF-link current with the conventional and proposed HF-MMC modulation schemes.

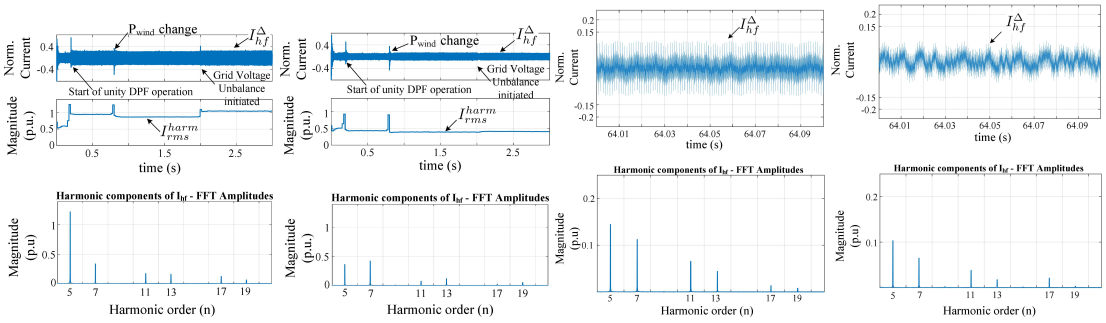


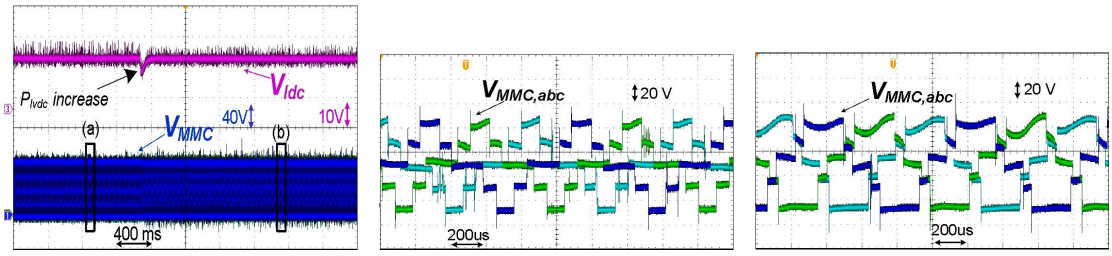
Figure 3.13: HF-link harmonic ripple current from the MATLAB/SIMULINK simulation for (a)Conventional modulation. (b)Proposed modulation. HF-link harmonic ripple current from OPAL-RT HIL simulation for (a)Conventional modulation. (b)Proposed modulation

The rms current squared is seen to show an improvement by more than three times for certain MMC voltage fundamental magnitudes as shown in Fig.3.11c and Fig.3.11d. For example, for $\delta = 2\pi/9$ and $V_{MMC} = (6521/11)\,V$ ($mag = 1.4$), the rms value of the current harmonics have been found to be 58.47 A with the conventional modulation (Eq. (4.34)) as compared to 26.49 A with the optimization scheme, an improvement by 54.69%, for the same fundamental current amplitude of 561 A. At very high values of mag, the modules need to be inserted quite early in the sinusoidal portion of the modulating signal in both the conventional and the proposed switching schemes. Due to this, the difference between the rms current values of the harmonics in the two schemes decreases. Similarly in Fig.3.13a-Fig.3.13b, the rms value of the current harmonics are observed to be consistently lower by about 60% in MATLAB/SIMULINK model and by 25% in the OPAL-RT HIL simulation under all operating conditions marked in the figure.

3.4.5 Hardware results

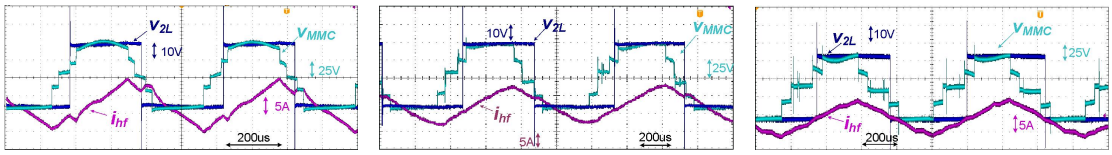
In Fig.3.14, a load increase at the lvdc link is performed from 160 W to 195 W and the lower MMC arm voltages under unity DPF operation at low load and high loads are

shown. An increase in load angle requires the MMC fundamental voltage to increase for unity DPF. In Fig.3.15, MMC modulated with conventional switching angles, the proposed optimization based harmonic control with a fixed feed-forward value of MMC fundamental voltage, and under unity DPF operation with harmonic control are shown. With proposed online optimization scheme, and a load of 10% of the rated load, an efficiency of 87% was observed which was an improvement over conventional modulation scheme by 7.5%.



(a) (b) (c)

Figure 3.14: (a).Load increase and its effect on the 2L-VSC dc link voltage and the three-phase MMC arm voltages, Zoomed MMC arm voltages at:(b).light load (c)increased load



(a) (b) (c)

Figure 3.15: MMC arm voltage,2L-VSC pole voltage and the HF-link current under (a)Conventional modulation scheme (b)Proposed modulation scheme without unity DPF and only harmonics control (c)Proposed modulation scheme with Unity DPF and harmonics control

3.5 Summary

An online optimization based modulation scheme for the HF-MMC to achieve closed-loop unity DPF operation and HF link current harmonic control was formulated. Along with this, the low voltage side dc bus control scheme acts in tandem for power transfer through the high-frequency link. It was observed that the harmonics in the HF-link current reduce by as much as 60% with the proposed control schemes and the unity DPF operation helped to reduce the fundamental current amplitude by as much as 15% under certain operating conditions. MATLAB/SIMULINK, OPAL-RT based HIL simulation results and hardware experimental results confirmed the designed control schemes at the HF link of the power electronic transformer topology.

3.6 Appendix

In Eq. (3.24) and Eq. (3.25), the subscripts 'L' on A_L, B_L and C_L have been dropped and the gradients are written for two switching angles a, b for the sake of clarity.

$$\begin{aligned}
&\nabla_a g = \\
&(A\,sin(11a) + B\,sin(5a) + C\,sin(7a) + \lambda\,sin(a)) \\
&\big[A\,cos(11a)(11) + B\,cos(5a)(5) + C\,cos(7a)(7) + \lambda\,cos(a) - \\
&\frac{sin^2(11a)}{11^2} - \frac{sin^2(5a)}{5^2} - \frac{sin^2(7a)}{7^2}\big] - \\
&(A\,sin(11b) + B\,sin(5b) + C\,sin(7b) + \lambda\,sin(b)) \\
&\big[\frac{sin(11a)sin(11b)}{11^2} + \frac{sin(5a)sin(5b)}{5^2} + \frac{sin(7a)sin(7b)}{7^2}\big] \\
&-(cos(a) + cos(b) - mag)\,sin(a)
\end{aligned} \tag{3.24}$$

$$\begin{aligned}
&\nabla_\lambda g = \\
&(A\,sin(11a) + B\,sin(5a) + C\,sin(7a) + \lambda\,sin(a))sin(a) \\
&+(A\,sin(11b) + B\,sin(5b) + C\,sin(7b) + \lambda\,sin(b))sin(b)
\end{aligned} \tag{3.25}$$

3.7 Acknowledgements

I would like to thank Prof. Mingyi Hong, Electrical and Computer Engineering Department, University of Minnesota, for offering the course - Introduction to Nonlinear Optimization and for his valuable comments about the optimization based control that was presented.

Chapter 4

DC-side Modeling of the High-Frequency-link MMC in a Back-to-Back Connected MMC-based Power Electronic Transformer

The DC-side model of the High Frequency link-MMC (HF-MMC) to study its response to an excitation in the dc link is presented in this chapter. The model is derived using a simplified equivalent circuit that excellently captures its behavior in this regard. Theoretical basis for the observed resonant peaks in the frequency response of the sum of the sub-module output voltages and closed form expressions for these resonant frequencies are provided. The developed model is validated through extensive simulation results from MATLAB/SIMULINK. OPAL-RT based Hardware-In-Loop real time simulations are used to further verify the presented model.

4.1 Introduction

Unlike in the case of MMCs connected through HVDC lines, direct back-to-back connection of MMCs calls for the frequency domain modeling of the High-Frequency MMC (HF-MMC) phase legs especially when the dc link contains injected excitation voltages with frequencies of the same order as the output fundamental frequency of the HF-MMC as shown in this paper. Such a model can then be used to design the control schemes, switching frequency and the component level parameters of the direct back-to-back connected MMCs with a common dc link.

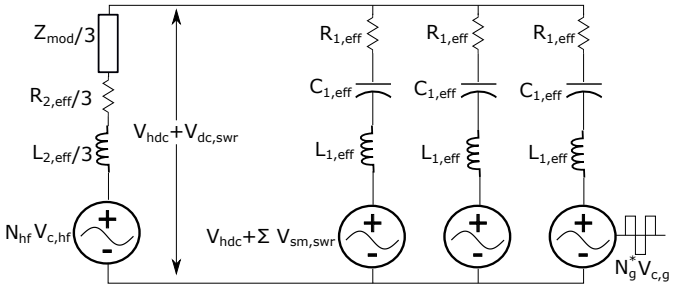


Figure 4.1: Circuit schematic to find the transfer function of an excitation voltage in the MMC phase legs to the dc link across the back-to-back connected MMC.

AC admittance modeling of the MMC was extensively studied in [82, 83, 84, 27, 28]. But the dc side impedance modeling of the MMCs needs special consideration when the dc link voltage cannot be assumed to be constant and ripple free.

In fig. 4.1, the arm resistances and inductances have been grouped into an effective inductance and resistance in each phase leg. The switching ripple with frequency components around carrier harmonics and its multiples result in each leg due to the sum of the sub-module PWM output voltages in the grid side MMC as explained in Chapter 2. They are marked as $\Sigma V_{sm,swr}$ or $N_g^* V_{c,g}$ in fig. 4.1 and transfer on to the dc link as V_{hdc}^{swr} through the voltage transfer function H as shown in Eq. (4.1). N_g^* is the instantaneous number of sub-modules turned on in a phase-leg of the grid-side MMC.

With the output fundamental frequency of 60 Hz at the grid-side MMC (GS-MMC), the excitation frequencies in the dc link are much greater in comparison. Thus, in the GS-MMC, the terminal model of the sub-module output voltages behave like a simple

capacitance of value $C_{g,sm}/N$ as explained in section 4.2. The three legs of the HF-MMC are represented by the branch containing the impedance $Z_{mod}/3$ in this paper. Here, Z_{mod} is the terminal impedance model of HF-MMC submodules.

$$\begin{aligned} Z_{hf} &= Z_{mod} + R_{2,eff} + s\,L_{2,eff}, \\ Z_g &= \frac{1}{s\,C_{1,eff}} + R_{1,eff} + s\,L_{1,eff} \\ H &= \frac{Z_{hf}}{Z_{hf}+Z_g} = \frac{V_{hdc}^{swr}}{\Sigma V_{sm}^{swr}} \end{aligned} \tag{4.1}$$

It is observed that with a sinusoidal excitation in the dc link at a frequency equal to that of the HF link frequency, this excitation could be amplified by a factor of more than 10 times in the sum of the sub-module output voltages causing severe capacitor voltage variations and large phase-leg currents as shown in Fig.4.7. In order to theoretically justify such a behaviour and to find out which excitation frequencies in the dc link are favourable, the following analysis is performed. This is useful in multi-converter configurations with a common dc link such as in Chapter 6 to design the individual HF-link frequencies of the converters.

Finally, it is shown below that the equivalent circuit in Fig.4.2, produces a resonant peak at the switching frequency of the half-bridges, independent of the variation in $2L_{arm}$ and C_{sm}/N. This aspect could prove useful in applications requiring resonance at the same frequency irrespective of change in leakage inductances such as wireless power transfer [85, 86].

In [87] and more recently in [88, 89] the concept of a switch controlled capacitor was used to implement a tunable capacitance for applications in resonant power converters. Instead of a single switch in parallel with the capacitor thus shorting it out or inserting it as in [88, 87], two half-bridge controlled capacitors results out of the high-frequency link MMC operation. The main difference is that the sub-module capacitor is bypassed without resetting the capacitor voltage to zero. Also, there always remains one of the two capacitors inserted in the resulting R-L-C circuit in this case.

4.2 DC side Modeling of the HF-MMC phase legs

In Fig.4.2, the equivalent circuit of the high-frequency side MMC (HF-MMC) phase legs to study the effect of the dc link switching ripple is shown. The half-bridge capacitors

are precharged to half the dc link voltage, V_{hdc} in Fig.4.2 and the capacitor voltages being shaped by the sinusoidal excitation voltage in the dc link, are assumed to vary around zero by removing the dc operating point voltages in the circuit.

For sufficiently high modulation indices, for example, $m_a > 0.875$ or $m_{hf} > 0.75$ in Eq. (4.34)[76], all submodules in the upper arm are inserted in one half-cycle of the switching frequency. Likewise in the next half, all submodules in the lower arm are inserted. Accordingly, the sub-module capacitors in the upper and lower arms of the MMC are lumped into an equivalent capacitance of value C_{sm}/N at the dc side of the two half bridges and the arm inductances and resistances are lumped together as shown. In the analysis below, $L = 2L_{arm}$ and $C = C_{sm}/N$.

Each of the half-bridges in Fig.4.2 receive a square pulse at a frequency f_s, the frequency of the AC output voltage of the HF-MMC. The switching frequency square pulse to the half-bridges can be written as shown in Eq. (4.2) with $m_{hf} = \frac{4}{\pi}$ to the first fundamental approximation.

$$m_{sq} = 0.5 \pm m_{hf}\,(0.5) sin(\omega_s t) \tag{4.2}$$

In the HF-MMC, m_{hf} can be atmost equal to 1.15 with a common mode voltage component such as a third harmonic added to the three phase modulating signals. In this case, the half-bridges receive a nearest-level-modulated(NLM) waveform following a rule such as in Eq. (4.34), instead of this square pulse thus eliminating the dv/dt stresses of the transformer and improving the voltage harmonic content.

The model in Fig.4.2 becomes more exact when modulation index is high. However, it has been observed that some key characteristics of the frequency response of the dc link impedance model remain the same at lower modulation indices as seen in Section 4.3.

To start with the analysis, it is observed that in each half-cycle of the switching frequency f_s, the circuit in Fig.4.2 reduces to an R-L-C circuit. The Laplace transform of the voltage equation of such an R-L-C circuit is shown in Eq. (4.3).

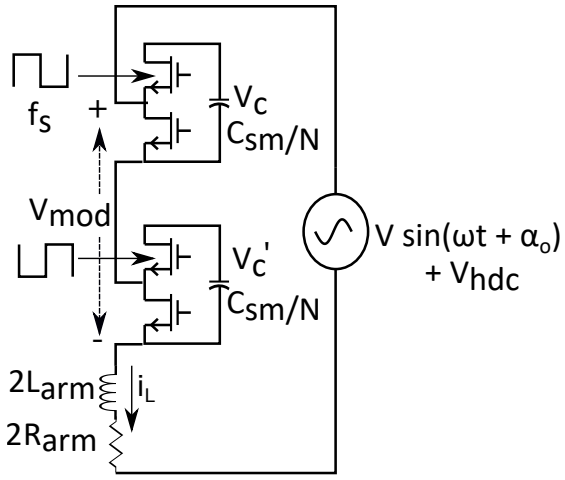


Figure 4.2: Equivalent circuit to model the frequency response of the HF-MMC phase legs to an excitation voltage in the dc link.

$$V\frac{\omega cos(\alpha) + s\, sin(\alpha)}{(s^2+\omega^2)} = L\, sI(s) - L\, I_{Lo} + I(s)\, R + \frac{1}{C}\frac{I(s)}{s} + \frac{V_{co}}{s} \tag{4.3}$$

The equation considers an initial condition on the capacitor voltage, V_{co} and the inductor current, I_{Lo} and a phase angle offset of α in the external sinusoidal voltage at the start of a time period under consideration. The external sinusoidal voltage source in the dc link has an amplitude, V and a frequency,f in Hz or ω in rad/sec and its instantaneous phase angle is denoted by $x = \omega t + \alpha_o$, where α_o is the phase angle offset between the modulating signal in Eq. (4.2) and the sinusoidal excitation in the dc link.

Then, the inverse laplace transform of the capacitor voltage and inductor current, not considering the series resistance in Eq. (4.3) is as shown in Eq. (4.4) and Eq. (4.5). The capacitor voltages of the upper and lower half-bridges as a function of x are denoted by $V_c(x)$ and $V_c'(x)$ respectively. Eq. (4.18) and Eq. (4.17) are damped versions of Eq. (4.5) and Eq. (4.4) and are used to numerically obtain $I_{L,k}$, $V_{c,k}$, $I_{L,k}^{'}$ and $V_{c,k}^{'}$ in fig. 4.3. $V_{c,k-1}$ and $V_{c,k-1}^{'}$ are the capacitor voltages of the upper and lower half-bridges at the beginning of their corresponding half-cycles i.e., the first and second half-cycles, in the k^{th} cycle of the switching frequency waveform. Similarly, $I_{L,k-1}$ and $I_{L,k-1}^{'}$ are the inductor currents respectively, at the beginning of the first and second half-cycles

in the k^{th} cycle of the switching frequency waveform.

$$V_c(x) = V_{co}\,cos(\frac{x-\alpha}{\omega\sqrt{LC}}) + \sqrt{\frac{L}{C}}\,I_{Lo}\,sin(\frac{x-\alpha}{\omega\sqrt{LC}}) - \frac{V}{\omega^2 LC-1}\,sin(x) + \frac{V}{\omega^2 LC-1}(cos(\frac{x-\alpha}{\omega\sqrt{LC}})\,sin(\alpha) + \omega\sqrt{LC}\,cos(\alpha)\,sin(\frac{x-\alpha}{\omega\sqrt{LC}})) \tag{4.4}$$

$$i_L(x) = I_{Lo}\,cos(\frac{x-\alpha}{\omega\sqrt{LC}}) - \sqrt{\frac{C}{L}}\,V_{co}\,sin(\frac{x-\alpha}{\omega\sqrt{LC}}) - \frac{V\omega C}{\omega^2 LC-1}\,cos(x) + \frac{V}{\omega^2 LC-1}(\omega\,C\,cos(\frac{x-\alpha}{\omega\sqrt{LC}})\,cos(\alpha) - \sqrt{\frac{C}{L}}\,sin(\alpha)\,sin(\frac{x-\alpha}{\omega\sqrt{LC}})) \tag{4.5}$$

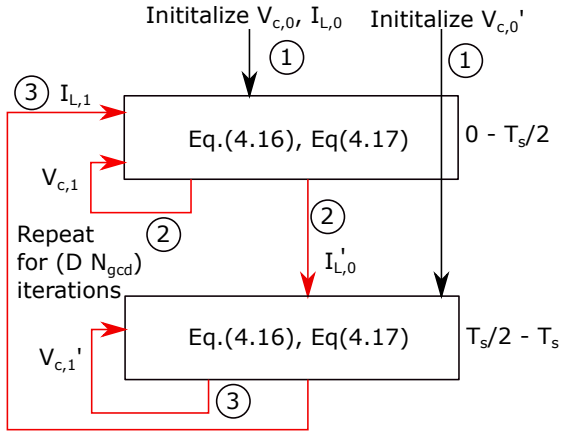


Figure 4.3: Numerical calculation of the initial conditions on $V_{c,0}, V'_{c,0}$ and $I_{L,0}$ at the beginning of a cycle of V_c and i_L. After N_{gcd} applications of Eq. (4.17) and Eq. (4.18), a cycle completes and V_c and i_L reach the same initial conditions as at the beginning. It takes D such iterations for the solutions to converge starting from an arbitrary initialization of $V_{c,0}, V'_{c,0}$ and $I_{L,0}$, where D is a large number such as 1000. Here, $I'_{L,0} = i_L(\frac{T_s}{2}), I_{L,1} = i_L(T_S).V_{c,1} = v_c(\frac{T_s}{2}) = v_c(T_s)$, since the upper capacitor is bypassed in the interval $\frac{T_s}{2} - T_s$ and its voltage does not change during this time. Similarly between T_s and $T_s + T_s/2$, the lower capacitor is bypassed and its voltage at the end of T_s is preserved till beginning of $T_s + T_s/2$. Hence, $V'_{c,1} = v'_c(T_s) = v'_c(T_s + \frac{T_s}{2})$. After these D iterations, the 2 N_{gcd} values of the inductor current and capacitor voltages are used for calculation in Eq. (4.7).

The operation of the equivalent circuit in fig. 4.2 is such that the capacitors of the two half-bridges swap each other in forming the series R-L-C circuit every half cycle of

the high-frequency link fundamental period, T_s. Evaluating Eq. (4.4) and Eq. (4.5) at the end of each of these half cycles eqs. (4.35) to (4.38) are obtained. In these equations, h is the fraction of the instantaneous phase angle of the external voltage spanned within a time interval of $0.5T_s$ and can be written as $h = \frac{0.5T_s}{T}2\pi$. $\alpha_{2k} = \alpha_o + 2\,k\,h$, is the angle spanned by the external voltage thus far till the beginning of the first half of the $(k+1)^{th}$ switching cycle. The quantity v in these equations is defined in Eq. (4.8).

When the sub-module capacitances of either of the half-bridges is swapped out, its voltage does not change. For example, $V_c(\alpha_{2k-1})$ at the end of the first half of the k^{th} switching cycle is equal to $V_c(\alpha_{2k}) = V_{c,k}$ at the beginning of the first half of the $(k+1)^{th}$ switching cycle, as also explained in fig. 4.3.

To model the terminal behaviour of the two half-bridge controlled capacitors, the Fourier component of V_{mod} in fig. 4.2, at the frequency of the driving voltage source is obtained. This is derived using Eq. (4.4), without considering the series resistance to keep computations tractable and in aiding insights into the operations of the circuit. By hitting the upper and lower capacitor voltages given by Eq. (4.4), with $cos(x)$ and $-jsin(x)$, in their respective half cycles and taking the average over a period of each of the sub-module's output voltage, Eq. (4.7) is derived. This is shown in Eq. (4.6).

$$V_{mod} = \frac{2}{N_f\,(2\pi)} \sum_{k=0}^{N_{gcd}-1} \Big[\int_{\alpha_o+2\,k\,h}^{\alpha_o+(2\,k+1)h} V_c(x)e^{-jx}dx + \int_{\alpha_o+(2\,k+1)h}^{\alpha_o+(2\,k+2)h} V_c^{'}(x)e^{-jx}dx \Big] \quad (4.6)$$

The capacitor voltages complete a period after N_{gcd} number of cycles of the switching frequency, f_s as shown in fig. 4.4. In this period of repetition, there are N_f number of cycles of the driving voltage where N_f and N_{gcd} are defined in Eq. (4.8). The total integral over this period is broken down into N_{gcd} pairs of smaller integrals as shown in Eq. (4.6), with integration duration of h.

$$V_{mod} = \frac{1}{N_f \pi}\Big[F_a(j\, N_{gcd}\, h) + B \sum_{k=0}^{N_{gcd}-1} (V_{co,k} + V'_{co,k} e^{-jh}) e^{-jk2h} + A \sum_{k=0}^{N_{gcd}-1} (I_{o,k} + I'_{o,k} e^{-jh}) e^{-jk2h} + \sum_{m=0}^{2N_{gcd}-1} (F_1\, cos(\alpha_o + mh) + F_2\, sin(\alpha_o + mh))\, e^{-jmh}\Big] \tag{4.7}$$

$$\begin{aligned} F_1 = \frac{A\,(\omega C)\,V}{\omega^2 LC - 1}, F_2 = \frac{B\,V}{\omega^2 LC - 1}, F_a = \frac{V}{\omega^2 LC - 1} \\ N_{gcd} = \frac{f_s}{GCD(f, f_s)}, N_f = \frac{f}{GCD(f, f_s)} \\ h = \frac{0.5\,T_s}{T} 2\pi = \frac{\pi N_f}{N_{gcd}}, v = \frac{0.5\,T_s}{\sqrt{LC}} \end{aligned} \tag{4.8}$$

$$\begin{aligned} A = (\frac{e^{-j\alpha_o}\omega L}{(\omega^2 LC - 1)})[-1 + e^{-j\,h}(cos(v) + j\omega\sqrt{LC} sin(v))] \\ B = (\frac{e^{-j\alpha_o}\omega\sqrt{LC}}{\omega^2 LC - 1})[-j\,\omega\,\sqrt{LC} - e^{-j\,h}\,(-j\omega\sqrt{LC}\, cos(v) + sin(v)] \end{aligned} \tag{4.9}$$

In calculating the Fourier series component at the frequency of the external driving voltage in Eq. (4.7), a total of $2N_{gcd}$ pairs of initial capacitor voltages and inductor currents, from the start of each half-cycle of f_s are required. As an example, fig. 4.7 show the waveforms of the sum of the sub-module output voltages, the two capacitor voltages and the current drawn from the external source when $f = f_s = 10$ kHz. We observe that V_c, $V_c^{'}$ and I_L complete a period after $N_{gcd} = 1$ cycle of f_s and accordingly the corresponding capacitor voltage and the inductor current, at the start of the first and second half-cycles of f_s are required. Similarly, for $f = 4.5$ kHz and $f_s = 10$ kHz, $V_c(t)$ is shown in fig. 4.4 and here $N_{gcd} = 20$ (20 cycles of f_s) when the capacitor voltage completes a period. The general numerical formulation for the calculation of all the initial conditions required for the evaluation of the Fourier series component in Eq. (4.7) is shown in fig. 4.3.

In Eq. (4.7), the term with the factor F_a is just the voltage component if both the half bridges were together replaced with a capacitor of value C_{sm}/N. This is because $\frac{N_{gcd}\,h}{N_f\,\pi} = 1$ and what remains of the term is $\frac{j\,V}{\omega^2 LC - 1}$ which is just the voltage across the

capacitor in an L-C circuit excited with a sinusoidal voltage source. The rest of the terms in Eq. (4.7) contain the factors A or B in Eq. (4.9). A and B both go to zero under the following conditions:

$$f = 2\,p\,f_s, f_s = \frac{1}{2\pi\sqrt{LC}}\frac{1}{2q}, p, q\,\epsilon N \qquad f \neq \frac{1}{2\pi\sqrt{LC}} \tag{4.10}$$

For example, this means that if the resonant frequency formed by L_{arm} and C_{sm}/N is 20 kHz, then for $f_s = 10$ kHz and $f = 40$ kHz, the half-bridges behave like a simple capacitance of value C_{sm}/N.

From fig. 4.13, the blue dotted line represents the magnitude response of this voltage component and it can be seen that at very low and very high frequencies of excitation voltage compared to $\frac{1}{\sqrt{L\,C}}$, the two half-bridges asymptotically follow the response of a simple capacitance of value C_{sm}/N. Further interpretation of Eq. (4.7) is deferred until after the investigation into the trend of the initial inductor current and capacitor voltages $V_{c,k}, V_{c,k}^{'}$ and $I_{L,k}, I_{L,k}^{'}$ of Eq. (4.7) which is provided next.

4.2.1 Initial Inductor Current And Capacitor Voltage In Each Half-cycle

The initial values of the inductor current and the two capacitor voltages at the beginning of the half-cycles in the Eq. (4.7) heavily influence the shape of the frequency response of V_{mod} to the excitation voltages at the dc link.

It is observed from the magnitude plots of V_{mod} in fig. 4.14 for various excitation frequencies that there is always a peak at the link frequency i.e., the frequency of switching of the two half-bridges. In addition there is also a resonant peak at a lower frequency and together these form the two major resonant peaks and which we call, the bigger sister (BS) and the smaller sister (SS) peaks. The other resonant peaks after the first two in the higher frequency range in fig. 4.13 are called the daughter peaks.

First, an attempt is made below to understand the two sister peaks. In Eq. (4.11), eqs. (4.35) to (4.38) are rewritten in matrix form to give the initial values of the state

variables at the beginning of a cycle as a function of the initial values at the beginning of the previous cycle i.e., before two half-cycles. The last three terms in each of the equations eqs. (4.35) to (4.38) which depend on the external voltage applied are abstractly grouped into J_o. The matrix P remains the same through every cycle of f_s and there are N_{gcd} such cycles before a period of the capacitor voltages or inductor current is complete. In Eq. (4.12), a similar matrix equation is written considering the starting point to be $I_{Lo}^{'}$ and $V_{co}^{'}$ in fig. 4.3 and accordingly the external applied voltage functions in eqs. (4.35) to (4.38) would have advanced by an angle h.

$$\underbrace{\begin{pmatrix} I_{L,1} \\ V_{c,1} \\ V_{c,1}^{'} \end{pmatrix}}_{W_1} = \underbrace{\begin{pmatrix} cos^2(v) & -\frac{y}{2}sin(2v) & -ysin(v) \\ \frac{1}{y}sin(v) & cos(v) & 0 \\ \frac{1}{2y}sin(2v) & -sin^2(v) & cos(v) \end{pmatrix}}_{\mathrm{P}} \underbrace{\begin{pmatrix} I_{L,o} \\ V_{c,o} \\ V_{c,o}^{'} \end{pmatrix}}_{W_o} + J_o \tag{4.11}$$

$$y = \sqrt{\frac{C}{L}}$$

$$\underbrace{\begin{pmatrix} I_{L,1}^{'} \\ V_{c,1}^{'} \\ V_{c,1} \end{pmatrix}}_{W_1^{'}} = P \underbrace{\begin{pmatrix} I_{L,o}^{'} \\ V_{c,o}^{'} \\ V_{c,o} \end{pmatrix}}_{W_o^{'}} + J_o e^{j\,h} \tag{4.12}$$

Since Eq. (4.7) contains the sum of the initial condition terms such as $V_{c,k} + V_{c,k}^{'} e^{-j\,h}$, a new initial condition vector as shown in Eq. (4.13) is synthesized by adding Eq. (4.11) and Eq. (4.12) multiplied by $e^{-j\,h}$.

$$\begin{aligned} U_n = W_n + W_n^{'} e^{-jh},\ Q_n = 2J_n,\ n = 0, 1, 2... \\ U_1 = P\,U_o + Q_o \end{aligned} \tag{4.13}$$

It is interesting to note that in Eq. (4.13), $Q_n = 2J_n$ and this means that $W_n + W_n^{'} e^{-jh}$ is just equal to $2W_n$. This has been verfied from simulations that $I_{L,n} + I_{L,n}^{'} e^{-jh} = 2I_{L,n}$ and $V_{c,n} + V_{c,n}^{'} e^{-jh} = 2V_{c,n}$. For example, at $f = f_s$, $h = \pi$ and it is seen from fig. 4.7 that $I_{L,0} + I_{L,0}^{'} e^{-j\pi} = 2I_{L,0}$.

The general form for the vector U_n in Eq. (4.13) can be written as a series as shown in Eq. (4.14) and Eq. (4.15).

$$\begin{aligned} U_{n+1} = P\,U_n + Q_n &= P\,(P\,U_{n-1} + Q_{n-1}) + Q_n \\ &= P^2\,U_{n-1} + P\,Q_{n-1} + Q_n \end{aligned} \tag{4.14}$$

After $(n+1)$ cycles, the initial conditions complete a period and return to the same values as at the start at the beginning of the $(n+2)^{th}$ cycle as shown in Eq. (4.15). Later $(n+1) = N_{gcd}$ will be used. For example, in fig. 4.4, $N_{gcd} = 20$ and a period completes starting from 0.4 sec at 0.402 sec. At the beginning of the 21^{st} cycle at 0.402 sec, the capacitor voltage returns to the same value as at 0.4 sec.

$$U_o = U_{n+1} = P^{n+1}U_o + \underbrace{\sum_{i=0}^{n} P^i Q_{n-i}}_{R_n} \tag{4.15}$$

The terms dependent on the external applied voltage formed by the summation in Eq. (4.15) is denoted by R_n corresponding to the vector at the $(n+1)^{th}$ cycle with the maximum index of the summation to be n.

The time domain equations in Eq. (4.4) and Eq. (4.5) are in a convenient form to analyze the circuit passing through multiple loops with separate initital conditions in each half-cycle. The usual time domain equations for analysing an R-L-C circuit are shown in Eq. (4.16), where f_{forced} is the forced response of the state variable in steady state and the other two terms represent the natural response [90, 91].

$$\begin{aligned} i_L &= K_1\, e^{s_1\, t} + K_2\, e^{s_2\, t} + f_{forced} \\ s_1, s_2 &= -\beta \pm \sqrt{\beta^2 - \omega_o^2} \\ \beta &= \frac{R}{2\,L}, \omega_o = \frac{1}{\sqrt{LC}} \end{aligned} \tag{4.16}$$

For a small damping resistance R, $\beta^2 << \omega_o^2$, $s1, s2 \simeq -\beta \pm j\omega_o$. Comparing with all the $e^{\pm j\omega_o}$ terms in Eq. (4.4) and Eq. (4.5), an additional factor of $r(t) = e^{\frac{-Rt}{2L}}$ multiplies these terms to impart damping to the system as shown in Eq. (4.17) and Eq. (4.18).

$$\begin{aligned} V_c(x) = r(t)\, V_{co}\, cos(\frac{t}{\sqrt{LC}}) + r(t)\sqrt{\frac{L}{C}}\, I_{Lo}\, sin(\frac{t}{\sqrt{LC}}) - \frac{V}{\omega^2 LC - 1}\, sin(\omega t + \alpha_o) + \\ \frac{V\, r(t)}{\omega^2 LC - 1}(cos(\frac{t}{\sqrt{LC}})\, sin(\alpha_o) + \omega\sqrt{LC}\, cos(\alpha_o)\, sin(\frac{t}{\sqrt{LC}})) \end{aligned} \tag{4.17}$$

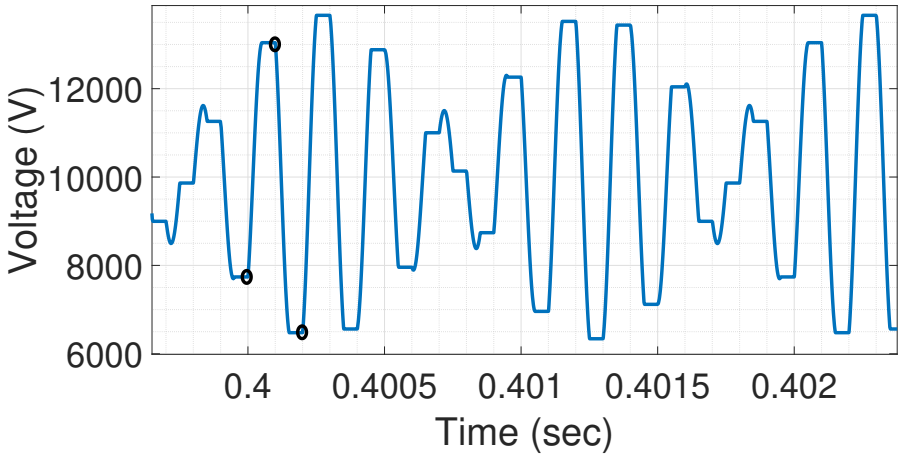


Figure 4.4: Upper half-bridge capacitor voltage $V_c(t)$ in fig. 4.2 for a dc side excitation voltage of 250 V at 4500 Hz - It takes $N_{gcd} = 20$ cycles of $f_s = 10kHz$ for a period of $V_c(t)$ to complete-e.g.,0.4-0.402 sec. The first three initial values $V_{c,k}$ for $k = 0, 1, 2$ out of a total of 20 within a period, starting from 0.4 sec are marked as black ellipses.

$$i_L(x) = r(t)\, I_{Lo}\, cos(\frac{t}{\sqrt{LC}}) - r(t)\sqrt{\frac{C}{L}}\, V_{co}\, sin(\frac{t}{\sqrt{LC}})\, \frac{V\omega C}{\omega^2 LC - 1}\, cos(\omega t + \alpha_o) + \frac{V\, r(t)}{\omega^2 LC - 1}(\omega\, C\, cos(\frac{t}{\sqrt{LC}})\, cos(\alpha_o) - \sqrt{\frac{C}{L}}\, sin(\alpha_o)\, sin(\frac{t}{\sqrt{LC}})) \tag{4.18}$$

Accordingly, the matrix considering the damping resistance is shown as P_R in Eq. (4.19), where $r(t)$ is being evaluated at the end of every half cycle at $t = 0.5T_s$.

$$P_R = r \begin{pmatrix} rcos^2(v) & -r\frac{y}{2}sin(2v) & -ysin(v) \\ \frac{1}{y}sin(v) & cos(v) & 0 \\ \frac{r}{2y}sin(2v) & -rsin^2(v) & cos(v) \end{pmatrix} \qquad r = e^{-\frac{RT_s}{4L}} \tag{4.19}$$

The matrices P and P_R are diagonalized in Eq. (4.20). The eigen values of P are the roots of its characteristic equation in Eq. (4.21) and these are shown in diagonal elements of the matrix $\wedge$ in Eq. (4.20). The exact eigen values of the matrix P_R have a complicated form and the values of r inside the elements of the matrix P_R is approximated by 1. As an example, for a 10 kHz HF link, $(4L)/R >> T_s$ for $L = 2L_{arm} = (2)(28\mu H)$ and $R = (2)0.1\Omega$ and so $r = e^{-\frac{RT_s}{4L}} = 0.92 \simeq 1$ is used within the elements of the matrix

P_R.

$$P = T \wedge T^{-1},\ P_R \simeq T \wedge_R T^{-1}$$

$$\wedge = \begin{pmatrix} 1 & & \\ & e^{j\theta} & \\ & & e^{-j\theta} \end{pmatrix},\ \wedge_R = \begin{pmatrix} r & & \\ & r\,e^{j\theta} & \\ & & r\,e^{-j\theta} \end{pmatrix} \tag{4.20}$$

$$e^{\pm j\theta} = \frac{1}{4}\left[q \pm \sqrt{-16 + q^2}\right]$$

$$\left[2\lambda^2 - \underbrace{\left(cos(2v) + 4cos(v) - 1\right)}_{\mathrm{q}}\lambda + 2\right](\lambda - 1) = 0 \tag{4.21}$$

The eigen values of the matrix P_R are as shown by the elements of the matrix $\wedge_R$ in Eq. (4.20). Note that θ depends only on the L and C values in the discussion above. Eq. (4.22) can then be written from Eq. (4.15) with P replaced by P_R and R_n replaced by $R_{r,N_{gcd-1}}$ to account for the inclusion of the factor r in the external voltage dependent terms.

$$U_o = (I_d - P_R^{N_{gcd}})^{-1} R_{r,N_{gcd-1}} \tag{4.22}$$

Next, $R_{r,N_{gcd-1}}$ is written in terms of the eigen vectors of the matrix P_R since they form a basis in $\mathbb{R}^3$ and U_o can be expressed as shown in Eq. (4.23).

$$\begin{aligned} U_o &= \gamma_1 (I_d - P_R^{N_{gcd}})^{-1} E_1 + \gamma_2 (I_d - P_R^{N_{gcd}})^{-1} E_2 + \gamma_3 (I_d - P_R^{N_{gcd}})^{-1} E_3 \\ U_o &= \gamma_1 \frac{1}{1 - (r)^{N_{gcd}}} E_1 + \gamma_2 \frac{1}{1 - (r\,e^{j\theta})^{N_{gcd}}} E_2 + \gamma_3 \frac{1}{1 - (r\,e^{-j\theta})^{N_{gcd}}} E_3 \end{aligned} \tag{4.23}$$

Here $\gamma_1, \gamma_2, \gamma_3$ are the magnitudes of $R_{r,N_{gcd-1}}$ along the eigen vector directions. Although we don't have a closed form expression for these γ values, the structure of U_k still reveals some important characteristics as shown below. Moreover, the exact values of the magnitude response at any frequency can still be calculated using the numerical iterative formulation for calculating initial values of the capacitor voltages and inductor currents in Fig.6 and using them in Eq.31.

Using the equation for U_o in Eq. (4.23) and substituting it in the general form for U_n in Eq. (4.15), U_k can be written as shown in Eq. (4.24).

$$U_k = \gamma_1 \frac{r^k}{1 - (r)^{N_{gcd}}} E_1 + \gamma_2 \frac{r^k\,e^{jk\theta}}{1 - (r\,e^{j\theta})^{N_{gcd}}} E_2 \gamma_3 \frac{r^k\,e^{-jk\theta}}{1 - (r\,e^{-j\theta})^{N_{gcd}}} E_3 + R_{r,k-1} \tag{4.24}$$

Now applying the equation for U_k in Eq. (4.7), the first two terms of U_k when taken inside the summation in Eq. (4.7), result in Eq. (4.25) and Eq. (4.26) by the formula for the sum of a geometric series. Since $2\,h = \frac{T_s}{T} 2\pi$, using $N_{gcd} = \frac{f_s}{GCD(f, f_s)}$ and

$N_f = \frac{f}{GCD(f,fs)}$, we get $2\,h = \frac{2\pi N_f}{N_{gcd}}$.

$$\frac{\gamma_1 E_1}{1-(r)^{N_{gcd}}} \sum_{k=0}^{N_{gcd}-1} r^k e^{-jk2h} = \begin{cases} \frac{\gamma_1 E_1}{1-r}, f = nf_s, n\,\epsilon\,\mathbb{N} \\ \frac{\gamma_1 E_1}{1-r\,e^{-j\frac{2\pi N_f}{N_{gcd}}}}, \text{otherwise} \end{cases} \tag{4.25}$$

$$\frac{\gamma_2 E_2}{1-(re^{j\theta})^{N_{gcd}}} \sum_{k=0}^{N_{gcd}-1} r^k\, e^{jk(\theta-2h)} = \begin{cases} \frac{\gamma_2 E_2}{1-r}, \theta = 2\,h \text{ or } \Delta = n\,2\pi, n\,\epsilon\,\mathbb{N} \\ \frac{\gamma_2 E_2}{1-r\,e^{j\Delta}}, \Delta \neq m\,2\pi, \theta N_{gcd} = m\,2\pi, m\,\epsilon\,\mathbb{Z} \\ \frac{\gamma_2 E_2}{1-(re^{j\theta})^{N_{gcd}}}\left(\frac{1-(r\,e^{j\Delta})^{N_{gcd}}}{1-r\,e^{j\Delta}}\right), \text{otherwise} \end{cases}$$

$$\Delta = \theta - 2\,h \tag{4.26}$$

Eq. (4.25) suggests that for r tending to 1, the summation of U_k terms in Eq. (4.7) tends to a huge value at $f = nf_s$, where $N_f = nN_{gcd}$ at such frequencies. Also, for $f = n\,f_s$, $N_{gcd} = 1$. For example, if $f_s = 10kHz$ and $f = 30kHz$, $N_{gcd} = 1$ and $N_f = 3$. The first case in Eq. (4.25) can be viewed as obtained by setting $N_f = nN_{gcd}$ in the more general formula in case two of the equation.

For the case of $N_{gcd} = 1$ and $f = n\,f_s$, the expression for the single required initital condition for calculation of Eq. (4.7), $I_{L,0}$ and $V_{c,0}$ are provided in Eq. (4.33). $I'_{L,0}$ and $V'_{c,0}$ are negative of these as explained before. It is seen that for frequencies that are odd multiples of f_s, there is a peak as captured in Eq. (4.30) and specifically, $f = f_s$ is the major peak, since for other odd multiples, the factor $\omega^2 LC - 1$ in the denominator is much bigger for $\omega >> \frac{1}{\sqrt{LC}}$. Thus the BS peak occurs at a frequency f_{BS} given by Eq. (4.27). It is also observed from Eq. (4.33) that for even multiples of f_s, the resonant peak does not exist and this is due to the effect of γ_1 which also influences the magnitude of U_k as mentioned before.

$$f_{BS} = f_s \tag{4.27}$$

Also, it is seen from Eq. (4.33) that for $\alpha_o = 0$, the magnitudes of $I_{L,0}$ and $V_{c,0}$ are not significant and the magnitude plot of V_{mod} for $\alpha_o = 0^o$ and $f_s = 10kHz$ is shown in fig. 4.13. There is indeed a sharp notch at f_s but at frequencies very close to f_s, the peaking is as much as the case for $\alpha_o = 90^o$.

It is interesting to note that the presence of a resonant peak at f_{BS} is insensitive to changes in values of L and C. It has been observed that the extent of increase of L that can be supported by the BS peak depends on the value of the dc link voltage,V_{hdc} in fig. 4.2. A large value of V_{mod} at $f = f_s$ occurs due to splitting of the upper and lower half-bridge capacitor voltages as shown in fig. 4.7. In the limits, the lower capacitor voltage touches zero. To achieve resonance at $f = f_s$, the impedance presented by the terminal model of the half-bridges, $Z_{mod} = -sL$ should be satisfied. This can be observed for $f = f_s$ when $V_{mod} >> V$ and using $R << sL$ from Eq. (4.28) and verified in fig. 4.5. At large values of L, the splitting of the two capacitor is not large enough to create the same voltage drop as that across sL while allowing a current limited only by the resistance in the circuit.

$$Z_{mod} = \frac{R(\frac{sL}{R} + 1)}{\frac{V}{V_{mod}} - 1} \tag{4.28}$$

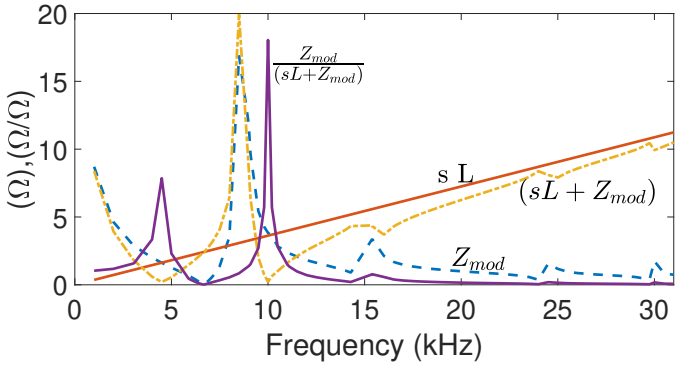


Figure 4.5: Magnitude plot of the effective impedance offered by the MMC sub-modules (blue dotted lines), the arm inductors (solid red line), the net impedance formed by the sum of the two (dashed-dotted yellow line) and the ratio $Z_{mod}/(Z_{mod} + s\,L)$for a $10kHz$ HF link fundamental frequency. The net impedance(yellow dashed-dotted line) goes to very low values at the BS and SS frequencies producing a resonance and at high frequencies the curve asymptotically follows the impedance of the inductor.

Similarly, from Eq. (4.26), it is observed that the summation of U_k terms in Eq. (4.7) blow up to a large value at $\theta = 2h$, where θ is the angle of the complex pair of eigen values of the matrix P or P_R. In other words, the resonance occurs at that frequency

f_{SS} shown in Eq. (4.29).

$$f_{SS} = \frac{\theta f_s}{2\pi} \tag{4.29}$$

The case 3 of Eq. (4.26) contains the general formula in the RHS and can be used to obtain cases 1 and 2 of the equation by applying the corresponding conditions shown in the equation. Taking an example, at $f_s = 10$ kHz, for L and C values as listed in table 4.2, $\theta \simeq \frac{9}{20}2\pi$ using Eq. (4.20). For $f = 4500$ Hz, $2\,h$ is also $\frac{9}{20}2\pi$ using Eq. (4.8). This gives, $\Delta = 0$ and the first case in Eq. (4.26). Thus $f_{SS} = 4500$ Hz for these values of arm inductance, sub-module capacitance and HF-link frequency as can be verified from Eq. (4.29). Note that, for these values of L and C and $f = 4500Hz$, $\theta\, N_{gcd} = 2\pi$ in the term outside the summation in the LHS of Eq. (4.26).

Even for other frequencies such as 500 Hz,1500 Hz, 3500 Hz etc, $N_{gcd} = 20$, (ΔN_{gcd}) and (θN_{gcd}) are multiples of 2π, but this only results in case 2 in Eq. (4.26). Only for $\Delta = 0$ or $\Delta = n2\pi$, case 1 holds. Note that $\theta N_{gcd} = 2\pi$ is automatically satisfied for $\theta = 2\,h$ in case 1 of Eq. (4.26).

From the magnitude response plot in fig. 4.13, in addition to the first two sister peaks, there are a number of resonant peaks in the higher frequency range. When $2nf_s - f = \pm f_{BS}$ and $2nf_s - f = \pm f_{SS}$, daughter peaks(DP) corresponding to BS and SS respectively are produced as shown in Eq. (4.30).

$$f_{DP} = (2\,n\,f_s \pm f_{BS,SS}),\ n\,\epsilon\,\mathbb{N} \tag{4.30}$$

This can be explained as follows: Using $\theta = \frac{2\pi T_s}{T_{ss}}$ from Eq. (4.29), $T_{DP} = \frac{1}{2nf_s + f_{SS}}$ and $2h = \frac{2\pi T_s}{T_{DP}}$, we get $\Delta = \theta - 2h$ to be a multiple of 2π and case 1 of Eq. (4.26) holds. A similar result can be obtained from the third term of U_k in Eq. (4.24) when $\Delta^{'} = \theta + 2h$ becomes a multiple of 2π for $T_{DP} = \frac{1}{2nf_s - f_{SS}}$. The general condition on the excitation voltage frequency for Δ or $\Delta^{'}$ to be a multiple of 2 π is given by Eq. (4.31).

$$f_\Delta = pf_s \pm f_{SS}, p\,\epsilon\,\mathbb{N} \tag{4.31}$$

It is observed from the numerical calculation of initial conditions using fig. 4.3 and Eq. (4.7) that there is an actual observed peak only for even values of p in Eq. (4.31) and this is captured in Eq. (4.30). Unlike for $N_{gcd} = 1$, the general closed form expression for the initial values of the capacitor voltages and inductor currents such as in Eq. (4.33), for the smaller sister or its daughter peaks involve looping through Eq. (4.18) and Eq. (4.17) multiple times (example, $N_{gcd} = 20$ for $f = 4500$ Hz).

The two degree-of-freedom model in Eq. (4.32) is seen to mimic the model in Eq. (4.7) as shown in fig. 4.17 for the case of fs = 10 kHz. The constants d_1 and d_2 are obtained from the magnitudes of V_{mod}, M_1 and M_2, at ω_{BS} and ω_{SS} using Eq. (4.7) and fig. 4.3, and by setting the dc gain to be unity. Since Eq. (4.7) is dominated by capacitive term at high and low frequencies, $\omega << \frac{1}{\sqrt{LC}}$ and $\omega >> \frac{1}{\sqrt{LC}}$, a similar second order term such as in Eq. (4.32) also captures this behaviour in these frequency ranges. In the region near the resonant sister peaks,the resonant terms in Eq. (4.32) dictate the frequency response of V_{mod}.

$$\begin{aligned} \frac{V_{mod,2DOF}}{V} &= \frac{d_1\left(\omega_{BS}^2\right)}{s^2+\omega_{BS}^2} + \frac{d_2\left(\omega_{SS}^2\right)}{s^2+\omega_{SS}^2} \\ \frac{d_1\left(\omega_{BS}^2\right)}{d_2\left(\omega_{SS}^2\right)} &= \frac{M_1}{M_2} \\ d_1 + d_2 &= 1 \end{aligned} \tag{4.32}$$

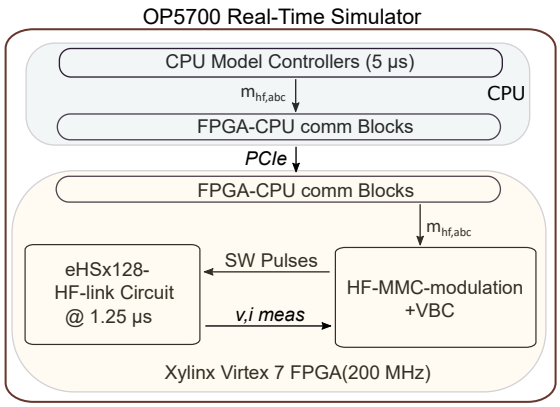
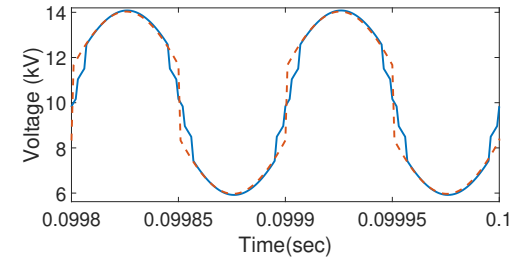
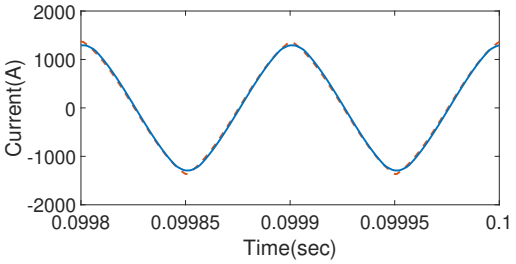


Figure 4.6: Block diagram of HIL real-time simulation implementation on OPAL-RT- The FPGA consists of two main blocks- eHSx128 and the PWM generation block. The eHSx128 is OPAL-RT's electrical hardware solver block which models the circuit in hardware. In the PWM generation block, HF-MMC modulation scheme is implemented. Capacitor Voltage Balancing logic is designed in the FPGA to balance the MMC sub-module capacitors. Communication of control signals such as the HF-MMC modulating signals $m_{hf,abc}$, from the CPU to the FPGA are exchanged through Peripheral Interconnect Express cables (PCIe).

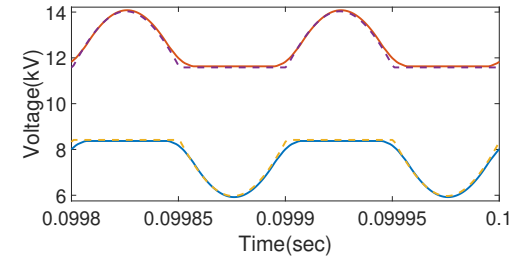
4.3 Results



(a)



(b)

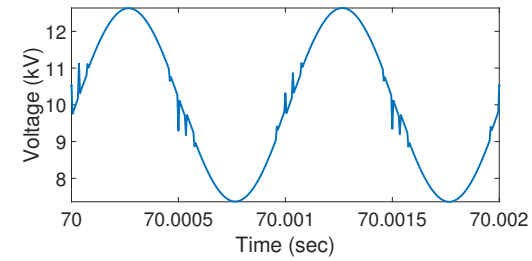


(c)

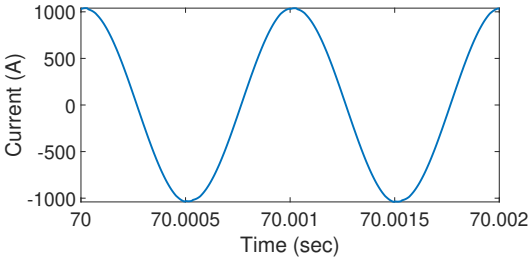
Figure 4.7: Comparison of time-domain waveforms of the equivalent circuit in fig. 4.2(dashed red lines) and the MMC in fig. 4.9(blue solid lines) in response to a dc side excitation voltage at $f = f_s = 10\ kHz$ and an amplitude of 250 V.

$$I_{L,0} = \frac{V}{\omega^2 LC - 1}\Big(- \omega\, C\, cos(\alpha_o) - \frac{2\, r}{r^2 - 1}\sqrt{\frac{C}{L}} sin(\alpha_o) sin(v)\Big)\Big|_{\omega=(2n+1)\omega_s} \qquad I_{L,0} = \frac{-V\omega C cos(\alpha_o)}{\omega^2 LC - 1}\Big|_{\omega=(2n)\omega_s}$$

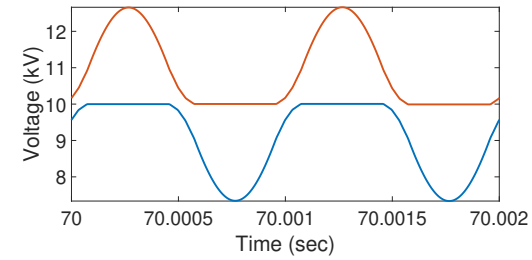
$$V_{c,0} = \frac{-V}{\omega^2 LC - 1}\frac{1 + r^2 + 2\, r cos(v)}{r^2 - 1} sin(\alpha_o)\Big|_{\omega=(2n+1)\omega_s} \qquad V_{c,0} = \frac{-V sin(\alpha_o)}{\omega^2 LC - 1}\Big|_{\omega=(2n)\omega_s} \tag{4.33}$$



(a)



(b)



(c)

Figure 4.8: Hardware-In-Loop Real time simulation waveforms of the MMC in fig. 4.9 in response to a dc side excitation voltage at $f = f_s = 1\ kHz$ and an amplitude of 250 V.

In Fig.4.7 are shown the time domain waveforms from the MATLAB/SIMULINK simulation of HF-MMC circuit and the equivalent circuit in Fig.4.2 with a modulation index of $m_{hf} = 1.15$ made possible with third harmonic injection. These waveforms have been obtained for a 10 kHz HF link with circuit parameters as in table 4.1. It can be observed that the waveforms almost overlap with each other showing the validity of the equivalent circuit for high modulation indices.

In fig. 4.6, the block diagram of the HIL implementation on OPAL-RT for verification of the presented model is shown. Voltage balancing of the sub-module capacitors and switching pulses for the HF-MMC are generated by custom created FPGA logic block. The switched model of the MMC circuit in fig. 4.9 is implemented on the electrical Harware Solver Block on the FPGA. The modulating signals for the HF-MMC are sent to the FPGA from the CPU cores in OPAL-RT. The time domain waveforms for a HF-link frequency of 1 kHz and other parameters as in table 4.1, using HIL real-time simulations from OPAL-RT are shown in Fig.4.8 and a similar trend can be observed.

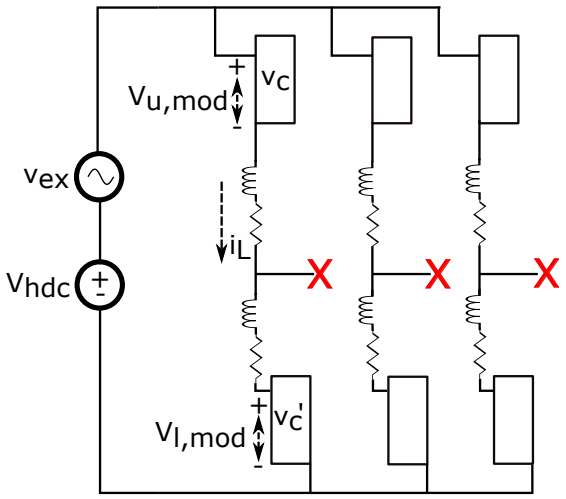


Figure 4.9: Experimental HF-MMC circuit to compare time domain waveforms and frequency response of the HF-MMC phase legs with the equivalent circuit in fig. 4.2 and the analysis expression for V_{mod} in Eq. (4.7).

Parameter	Value
V_{hdc}	10 kV
V_{ex}	250 V
MMC-	1 kHz - 200 μH, 0.1 Ω, 250 μF
L_{arm}, R_{arm},C_{sm}	10 kHz - 28.847 μH, 0.1 Ω, 31.831 μF
	50 kHz - 3.988 μH, 0.1 Ω, 10.61 μF

Table 4.1: Simulation parameters for the circuit in Fig.4.9. The arm inductances and sub-module capacitances are chosen to limit the sub-module capacitor voltage ripple to within 1% of its dc value and second harmonic circulating currents to within 2% of the maximum fundamental output current of 200 A.

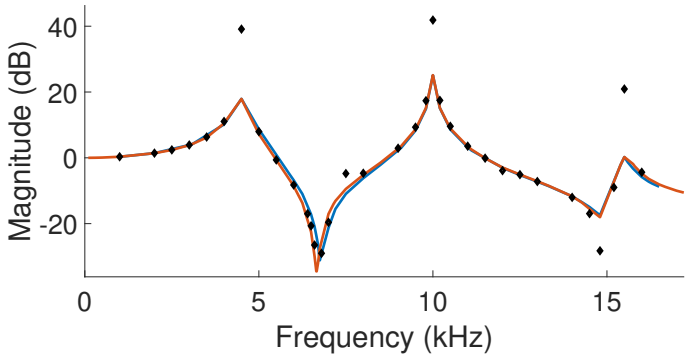


Figure 4.10: Magnitude plot at $f_s = 10kHz$, of the sum of upper and lower arm sub-module output voltages from the MMC circuit in Fig.4.9(blue solid lines), V_{mod} in the equivalent circuit in Fig.4.2(red solid lines) and the magnitude response as calculated from Eq. (4.7) with required initial conditions on I_L, V_c and$V_c^{'}$ obtained numerically as per fig. 4.3(black diamonds).

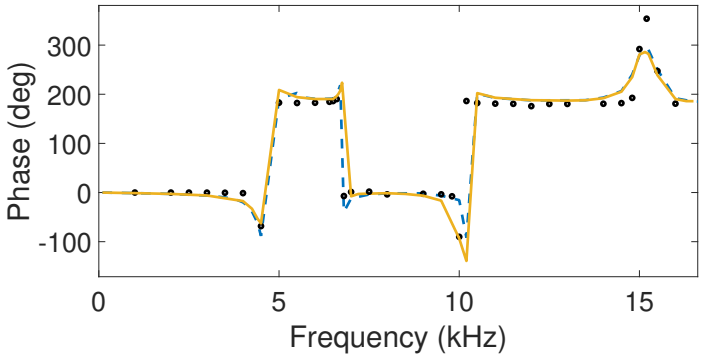


Figure 4.11: The phase plot corresponding to the magnitude response in fig. 4.10 from the MMC circuit in fig. 4.9(yellow solid lines), from fig. 4.2 (blue dashed lines) and from the analysis as explained in fig. 4.10(black circles).

The magnitude plots of V_{mod} as a function of frequency extracted from fig. 4.9 and fig. 4.2 for a HF link frequency of 10 kHz and circuit parameters as in table 4.1, are shown as the blue and red solid lines respectively in fig. 4.10. In fig. 4.11, their corresponding phase plots are also shown and they once again almost superimpose each other. The magnitude and phase of V_{mod} are plotted as black diamonds in fig. 4.10 and fig. 4.11 using Eq. (4.7), and fig. 4.3 for the calculation of the initial values in Eq. (4.7). The frequency response from the simulation and those from the analysis are observed to match well with each other. At close to resonant frequency of $\frac{1}{\sqrt{LC}}$ and at the two sister peak frequencies, there is an error from the experimental results in fig. 4.10 due to Eq. (4.7) not considering the series resistance. It is interesting to note that the phase of V_{mod} in fig. 4.11 alternates between almost 0^o and almost 180^o every time a resonant frequency is crossed. This can be understood from the general partial fraction expansion form such as in Eq. (4.32) for a multiresonant system[92].

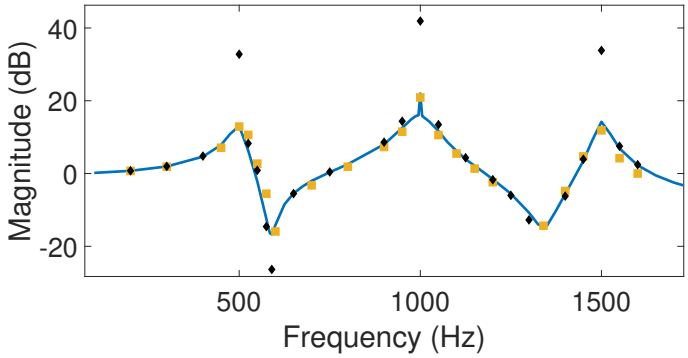


Figure 4.12: Magnitude response plot of V_{mod} from OPAL-RT HIL simulation (yellow squares), using Eq. (4.7) and numerical calculation of intitial conditions with fig. 4.3 (black diamonds), MATLAB/SIMULINK simulation results (solid blue line).

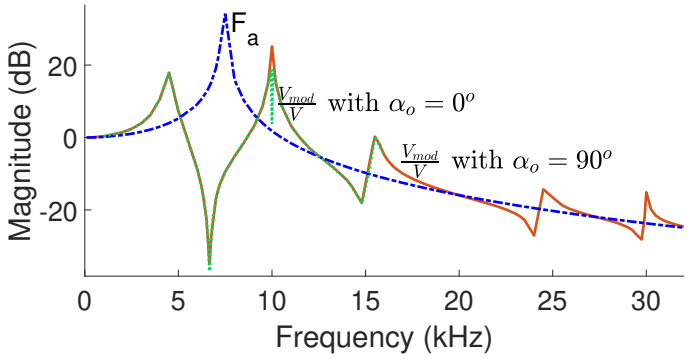


Figure 4.13: Magnitude response of V_{mod} in fig. 4.2 with $f_s = 10\,kHz$, to the excitation voltage V at the dc link(red solid lines) with $\alpha_o = 90^o$, with $\alpha_o = 0^o$ (green dotted line). It is observed that there is a notch at f_{BS} with $\alpha_o = 0^o$ as per Eq. (4.33) and Eq. (4.7). The magnitude reponse of a capacitor of value C_{sm}/N (blue dashed-dotted lines) is also shown and V_{mod} asymptotically follows the capacitor's response at very high and very low frequencies.

For a 1 kHz HF link and circuit parameters in table 4.1, the magnitude plots of the sum of upper and lower sub-module output voltages in fig. 4.9, from OPAL-RT based HIL simulation are shown in fig. 4.12 for $m_{hf} = 1.15$. In the same figure, the magnitude plot of V_{mod} using the analytical expression in Eq. (4.7) and MATLAB/SIMULINK simulations of fig. 4.2 are shown. Once again, a good match is observed between the

three plots.

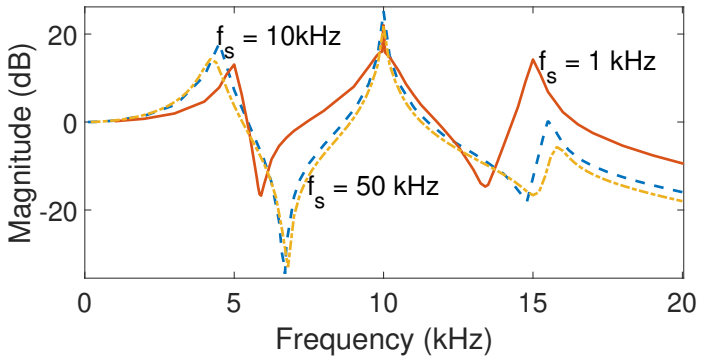


Figure 4.14: Magnitude plots of the frequency reponse of the circuit in fig. 4.2 at $f_s = 1kHz$-solid line, $50kHz$-dashed-dotted line, with frequency axis scaled by 10 times and 0.2 times respectively, and at $f_s = 10kHz$-dotted line, shown in the same plot. The BS peaks always lie at the link frequencies and the SS peaks follows the values in table 4.2.

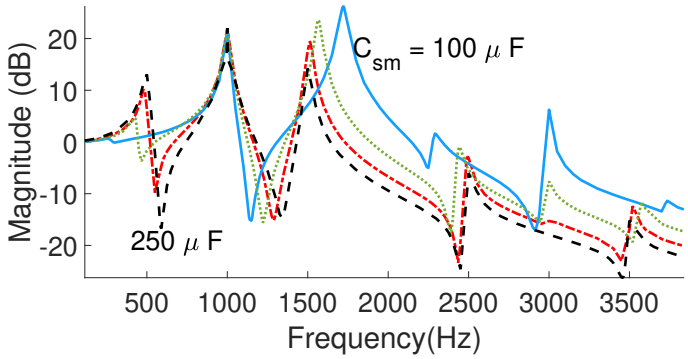


Figure 4.15: Magnitude response plot of V_{mod} using the equivalent circuit model in fig. 4.2 for the link frequency of 1 kHz and $C_{sm} = 100\mu F, 150\mu F, 200\mu F$ and $250\mu F$ with $L_{arm} = 200\mu H$. The peaks in the plot have been tabulated in table 4.2.

The frequencies of the resonant peaks in fig. 4.13, fig. 4.14 and fig. 4.15 have been tabulated in table 4.2. Also, the expected values of f_{SS} using Eq. (4.29) and the angle of the complex pair of eigen values in Eq. (4.20) have been tabulated for various values of HF-link frequencies, sub-module capacitances and arm inductance values. The first

daughter peak in the last three rows using Eq. (4.30) for the frequencies of f_{SS} tabulated in table 4.2, are at 1512.2 Hz, 1565.9 Hz and 1721.8 Hz. At these frequencies it can be verified that $\theta + 2\,h = 4\pi$, for the corresponding θ values in table 4.2. Also, DP exist only at even numbers p in Eq. (4.31) as mentioned before.

It is seen that the observed frequencies of the smaller sister peak and the daughter peaks as per Eq. (4.30) in table 4.2 are within a maximum error of 2% from the theoretical values. Also, the magnitude of observed V_{mod} at the theoretical f_{SS} and observed f_{SS} are within a maximum margin of 4%. The daughter peaks of the BS peak always occur when the dc link excitation is at odd multiples of the link frequencies from Eq. (4.30), and the values of the intitial currents for these frequencies at the beginning of each half-cycle of f_s follow Eq. (4.33).

It is interesting to observe that the expected daughter resonant peak at 3 kHz for a sub-module capacitance value of $C_{sm} = 250\mu F$ is absent for the HF link at 1 kHz as tabulated in table 4.2 and observed in fig. 4.15. This can be explained by observing that the resonant frequency formed by the $2L_{arm}$ and $0.25\,C_{sm}$ for $C_{sm} = 250\mu F$ and $L_{arm} = 200\mu H$ is at the HF link frequency of 1 kHz. Substituting for $T_s = 2\pi\sqrt{LC}$ in v of Eq. (4.33) and $\omega = 3\omega_s$, reveals that the numerators of the terms dependent on r in $I_{L,0}$ and $V_{c,0}$ are almost zero in case the HF-link is at the resonant frequency. However, even in this case, the BS peak still exists because the denominator of these terms tend to zero faster than the numerator and there is a needle-peak at f_{BS}, specially for this case as observed from fig. 4.12.

For other values of C_{sm}, a predominant peak at $3f_s$ can be observed from fig. 4.15. It is also observed that for lower values of C_{sm}, the smaller sister peak is smaller in magnitude. This can be explained from the fact that, at low values of SS peak frequencies and far away from the resonant frequency formed by L and C, the numerator of the coefficient A and B in Eq. (4.9) is so small that it does not amplify the U_k terms in Eq. (4.7) sufficiently. In these cases the corresponding daughter peaks are quite significant in amplitude as seen from fig. 4.15.

In fig. 4.14, the magnitude responses of fig. 4.2 at HF link frequencies of 10 kHz, 1 kHz and 50 kHz for C_{sm} and L_{arm} as tabulated in table 4.1 are shown. The frequency axis for the 1 kHz plot has been scaled by 10 times and that of the 50 kHz plot has

been scaled by 0.2 times to show in the same plot. The SS peak frequencies follow the expression obtained from the analysis as seen from table 4.2 and the BS peak remains fixed at the link frequency.

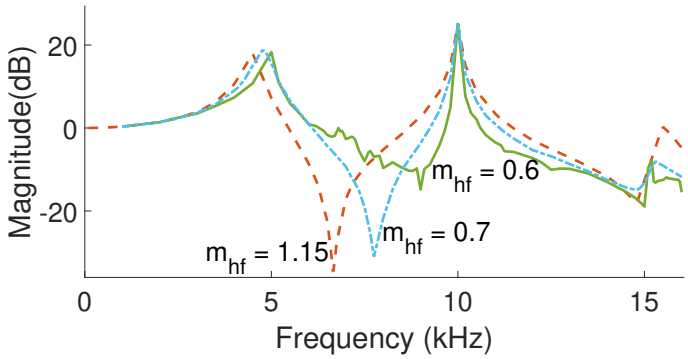


Figure 4.16: Magnitude plot of the frequency response of the MMC circuit in fig. 4.9 at $f_s = 10kHz$ to a dc link excitation voltage for varying values of modulation index.

In fig. 4.16 are shown, the magnitude response plots from fig. 4.9 for $m_{hf} = 0.7$ and $m_{hf} = 0.6$ respectively in the blue dashed-dotted line and the green solid line. For comparison, the magnitude response plot for the case of modulation index of 1.15 is also shown by the red dotted line in fig. 4.16. It is seen that the SS peak shifts slightly to the right while the BS peak remains at the link frequency of f_s. Also, there are a number of micro-resonances occurring between the two sister peaks as seen from the green solid line for lower modulation index of 0.6. Although at lower modulation indices such as 0.6 the total number of modules inserted per phase leg is still N, they are composed of (N-1) in one of the arms and 1 in the other for most of the time as against N and 0 for higher modulation indices. Since the capacitor voltages of these (N-1) and 1 capacitors are balanced in two different groups they cannot be considered as a single capacitor anymore.

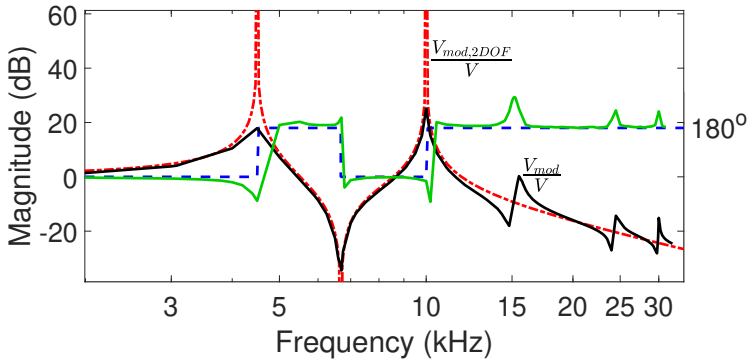


Figure 4.17: Comparison of magnitude and phase plot vs frequency from Eq. (4.32)(red dashed-dotted and blue dotted lines) and from the equivalent circuit in fig. 4.2(black solid and green solid lines), for $f_{BS} = 10kHz$ and $f_{SS} = 4.5kHz$. $d_1 = 0.3180$ and $d_2 = 0.6820$ was used in Eq. (4.32).

In the magnitude response plots, it has been repeatedly observed that there is an antiresonant dip between any two resonant peaks. This can again be explained as following from the partial fraction expansion form for a general multiresonant system such as shown in Eq. (4.32) [92]. If the coefficients d_1 and d_2 are of the same sign then there is an antiresonant dip between ω_{BS} and ω_{SS} since the denominators are of opposite sign at a frequency between the two resonant frequencies. In fig. 4.17, the comparison of the magnitude response from Eq. (4.32) and from the equivalent circuit in fig. 4.2 for $f_s = 10$ kHz is shown.

$f_s(kHz)$	$L(\mu H)$ -$2L_{arm}$	$C(\mu F)$ -$0.25C_{sm}$	$\theta(rad)$ -Eq. (4.20)	$f_{SS,t}(kHz)$ -Eq. (4.29)	$f_{SS,o}(kHz)$ -Observed	$V_{mod}(V)$ -$f_{SS,t}$	$V_{mod}(V)$ -$f_{SS,o}$	DP(kHz)-Observed
10	57.7	7.96	2.8312	4.506	4.5	1960	1964	15.5, 24.5, 30
50	7.9	2.65	2.7055	21.529	21.3	1314	1324	79, 121.53 150
1	400	62.5	3.1414	0.499	0.495	1137	1147	1.5, 2.5, -, 3.5
1	400	50	3.0650	0.4878	0.480	771.5	803.6	1.515, 2.495, 3, 3.520
1	400	37.5	2.7277	0.4341	0.425	382.6	427.2	1.565, 2.445, 3, 3.575
1	400	25	1.7478	0.2782	0.270	259.5	267.6	1.721, 2.290, 3, 3.730

Table 4.2: Resonant peaks in the frequency response of the HF-MMC phase legs designed for various fundamental link frequencies, f_s. The BS peak always lies at the link frequency and is not shown separately. The SS peak follows the prediction in Eq. (4.29) and the daughter peaks follow Eq. (4.30).

4.4 Summary

The dc side modeling of the HF-MMC phase legs was performed and it was shown that the frequency response of the sum of sub-module output voltages is dominated by resonant peaks at frequencies called as the two sister peaks and several associated daughter peaks. Correspondingly closed form expressions of the frequencies of these peaks were presented. It was observed that the major resonant peak lies at the link frequency or the switching frequency of the HF-MMC. This resonant peak is largely insensitive to the changes in the inductance and capacitance values forming the series R-L-C network. Through the simulation results from MATLAB/SIMULINK and Hardware-In-Loop simulation results from OPAL-RT, the magnitude and phase response plots from the model was observed to match closely with the experimental results.

4.5 Appendix

$$
\begin{aligned}
m_a = 0.5 + 0.5\,(m_{hf})\,sin(\omega_s t), 0 \leq m_{hf} \leq 1 \\
N_{ON} = round_{0.5}(Nm_a) \\
m_a \geq 0.875, \text{ all 4 modules ON} \\
0.875 > m_a \geq 0.625, \text{ 3 modules ON} \\
0.625 > m_a \geq 0.375, \text{ 2 modules ON} \\
0.375 > m_a \geq 0.125, \text{ 1 modules ON} \\
0.125 > m_a \geq 0, \text{ 0 modules ON}
\end{aligned}
\tag{4.34}
$$

$$
\begin{aligned}
V_{c,k} = V_{c,k-1}cos(v) + \sqrt{\frac{L}{C}} I_{L,k-1} sin(v) - \frac{V}{\omega^2 LC - 1} sin(\alpha_{2k-1}) \\
+ \frac{V}{\omega^2 LC - 1}(cos(v)sin(\alpha_{2k-2}) + \omega\sqrt{LC}cos(\alpha_{2k-2})sin(v))
\end{aligned}
\tag{4.35}
$$

$$
\begin{aligned}
I_{L,k} = I^{'}_{L,k-1}cos(v) - \sqrt{\frac{C}{L}} V^{'}_{c,k-1} sin(v) - \frac{V\omega C}{\omega^2 LC - 1} cos(\alpha_{2k}) + \\
\frac{V}{\omega^2 LC - 1}(\omega C cos(v)cos(\alpha_{2k-1}) - \sqrt{\frac{C}{L}} sin(\alpha_{2k-1})sin(v))
\end{aligned}
\tag{4.36}
$$

$$
\begin{aligned}
V^{'}_{c,k} = V^{'}_{c,k-1}cos(v) + \sqrt{\frac{L}{C}} I^{'}_{L,k-1} sin(v) - \frac{V}{\omega^2 LC - 1} sin(\alpha_{2k}) \\
+ \frac{V}{\omega^2 LC - 1}(cos(v)sin(\alpha_{2k-1}) + \omega\sqrt{LC}cos(\alpha_{2k-1})sin(v))
\end{aligned}
\tag{4.37}
$$

$$
\begin{aligned}
I^{'}_{L,k-1} = I_{L,k-1}cos(v) - \sqrt{\frac{C}{L}} V_{c,k-1} sin(v) - \frac{V\omega C}{\omega^2 LC - 1} cos(\alpha_{2k-1}) + \\
\frac{V}{\omega^2 LC - 1}(\omega C cos(v)cos(\alpha_{2k-2}) - \sqrt{\frac{C}{L}} sin(\alpha_{2k-2})sin(v))
\end{aligned}
\tag{4.38}
$$

Acknowledgment

I would like to sincerely thank Prof. Bernardo Cockburn, Mathematics Department, University of Minnesota, for the fruitful discussions and for helping out with the formulation of the problem in section 4.2.1.

Chapter 5

Design Considerations at the High Frequency Link

HF-transformer design based on area-product method[93] and design for maximizing the number of HF-MMC sub-modules that undergo soft-switching as in [94] yield accurate design values of the transformer leakage inductance. In this chapter, some design equations for the transformer turns ratio and the effect of variation of the HF-link leakage inductance over a chosen range on some of the parameters discussed so far is presented. It assumes a 2kV margin of voltage variation on V_{hdc} to provide frequency regulation and inertial power support to the grid.

The resistance of the HF link depends upon the asymmetries in the mutual coupling between the primary and secondary windings and is taken to be 0.03Ω at 1 KHz corresponding to that of a mega-watt level HF-transformer [95]. Nominal value of V_{hdc} is 13 kV and N is the number of sub-modules per arm and is set to 4 in the following equations. The HF link is designed to operate at 1 KHz.

5.0.1 Conditions for Soft switching at the HF-link low voltage side converter

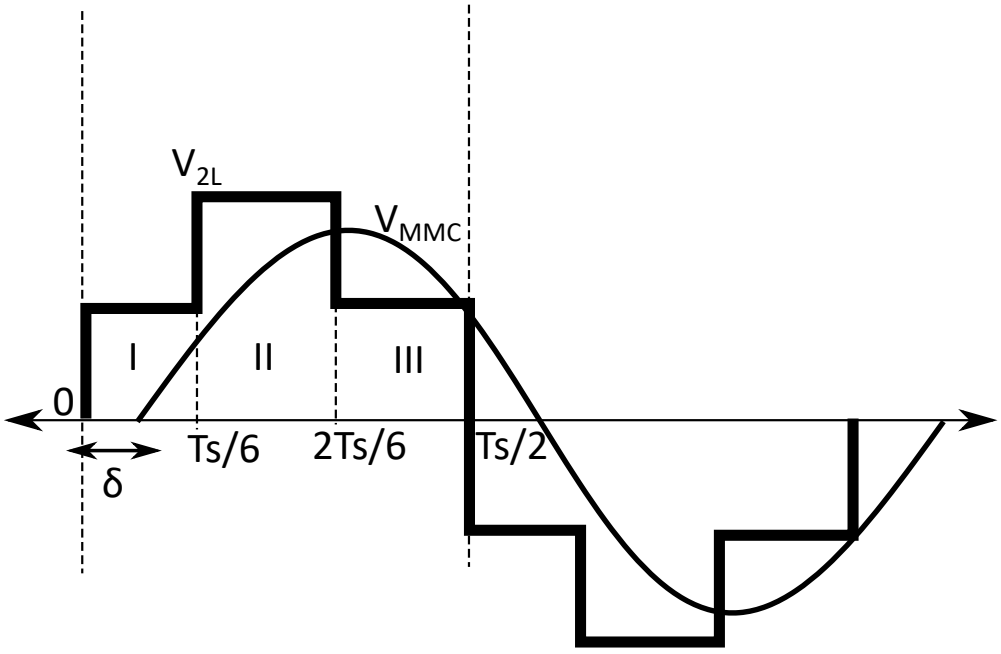


Figure 5.1: The stepped down MMC voltage waveform with only its fundamental frequency component and the six-step voltage waveform produced by the HF-link 2L-VSC

Usually, the current available for soft-switching is found by writing piece-wise current equations for every change in voltage across the HF transformer [96, 52]. Since the MMC voltage consists of a number of levels in its voltage waveform, writing piecewise equations for every change in the MMC voltage can become tedious [52]. In [97], analysis of the HF-link waveforms by expressing both the applied voltages and the link current using trigonometric Fourier series cofficients was suggested. Here, only the MMC side voltage is analysed using Fourier series coefficients and the analysis provided below yields a general expression for the soft-swtiching current available for any such number of harmonics and for all load angles, δ. The NLM waveform created by the MMC is assumed to be sinusoidal to start with in the analysis presented. Later, the exact expression for the soft-switching current by adding the k^{th} harmonic to the MMC voltage is presented. Also, the analysis incorporates the high-frequency link resistance

in contrast to the usual case of considering just the leakage inductance of the HF-link. $V_{2L,n}$ and $V_{MMC,N}$ are the voltages with respect to the transformer neutral points in fig. 3.1b, referred to the low voltage side. The distinct voltage levels in the six-step voltage waveform of the two-level converter are denoted as $V_1 = \frac{V_{ldc}}{3}$ and $V_2 = \frac{2V_{ldc}}{3}$. V_{an} in fig. 3.1b is assumed to be of the form $V_{MMC}\, sin(\omega_s t - \delta)$ lagging V_{AN} by an angle δ. The time domain voltage equations across the high frequency link during intervals I, II and III in fig. 5.1 are shown in Eq. (5.1). R_{hf} and L_{hf} are the leakage inductance and resistance of the HF-link.

$$\begin{aligned} i\,R_{hf} + L_{hf}\frac{di}{dt} &= V_1 - V_{MMC}\, sin(\omega_s t - \delta), \\ 0 \le t \le \frac{T_s}{6},\ i(0) &= I_o \\ i\,R_{hf} + L_{hf}\frac{di}{dt} &= V_2 - V_{MMC}\, sin(\omega_s t - \delta + \frac{\pi}{3}), \\ \frac{T_s}{6} \le t \le \frac{2T_s}{6},\ i(\frac{T_s}{6}) &= I_{o2} \\ i\,R_{hf} + L_{hf}\frac{di}{dt} &= V_1 - V_{MMC}\, sin(\omega_s t - \delta + 2\pi/3), \\ \frac{2T_s}{6} \le t \le \frac{T_s}{2},\ i(\frac{2T_s}{6}) &= I_{o3} \end{aligned} \tag{5.1}$$

The Laplace transform of the voltage equation across the R-L impedance of the high frequency link assuming an initial value of current, I_o is shown in Eq. (5.2).

$$I(s)R_{hf} + L_{hf}(s\,I(s) - I_o) = V_{2L,N}(s) - V_{MMC,n}(s) \tag{5.2}$$

Intervals marked as I, II and III in fig. 5.1 extend for one-sixth of a cycle and the Laplace transform equation of the current in interval I in shown in Eq. (5.3a). The subscript hf for R and L has been dropped for the rest of the analysis to keep the equations short. At the beginning of interval II in fig. 5.1, the initital current through the link is denoted as I_{o2} and the the MMC voltage would have advanced by 60^o. The next level in the two-level inverter's voltage is V_2. Using this, the Laplace transform equation of the current during the second interval is shown in the second equation in Eq. (5.3b). With further advance of the MMC voltage by 60^o, using an initial current I_{o3} and the level V_1 again for the six-step waveform in interval III we have the third equation in Eq. (5.3c).

Taking inverse laplace transforms of the equations in Eq. (5.3), the currents at the end of interval I, II and III are equated to I_{o2}, I_{o3} and back to I_o respectively for steady

state operation and are shown in eqs. (5.4) to (5.6). Substituting for I_{o2} and I_{o3} from these equations in Eq. (5.6), we get Eq. (5.7). Note that the time durations for interval I, II and III are equal to $\frac{1}{6\,f_s}$ and this value was set as t_s at the end of each interval to get expressions for currents I_{o2} and I_{o3}.

Following a similar process, it is found that the error terms in the soft switching current due to each additional harmonic in the MMC voltage is given by the general formula for $I_{o,error,k^{th}}$ in Eq. (5.8). Z_k and ψ_k are the magnitude and impedance angle of the HF-link R-L impedance at the k^{th} harmonic of the MMC voltage.

The final expression for the current available for soft switching is shown in Eq. (5.9) where, the relation $V_2 = 2V_1$ was used to eliminate the V_2.

$$I(s) = \frac{V_1}{s(sL+R)} - V_{MMC}\frac{\omega_s\, cos(\delta) + s\, sin(-\delta)}{(s^2+\omega_s^2)(sL+R)} + \frac{I_o}{s+R/L} \tag{5.3a}$$

$$I(s) = \frac{V_2}{s(sL+R)} - V_{MMC}\frac{\omega_s\, cos(\frac{\pi}{3}-\delta) + s\, sin(\frac{\pi}{3}-\delta)}{(s^2+\omega_s^2)(sL+R)} + \frac{I_{o2}}{s+R/L} \tag{5.3b}$$

$$I(s) = \frac{V_1}{s(sL+R)} - V_{MMC}\frac{\omega_s\, cos(\frac{2\pi}{3}-\delta) + s\, sin(\frac{2\pi}{3}-\delta)}{(s^2+\omega_s^2)(sL+R)} + \frac{I_{o3}}{s+R/L} \tag{5.3c}$$

$$I_{o2} = \frac{V_1}{R}(1-e^{-\frac{Rt_s}{L}}) + I_o\, e^{-\frac{Rt_s}{L}} + \frac{e^{-\frac{Rt_s}{L}} V_{MMC}\, sin(-\delta-\psi_1)}{Z_1} - \frac{V_{MMC}\, sin(\omega_s t_s - \delta - \psi_1)}{Z_1} \tag{5.4}$$

$$I_{o3} = \frac{V_2}{R}(1-e^{-\frac{Rt_s}{L}}) + I_{o2}\, e^{-\frac{Rt_s}{L}} + \frac{e^{-\frac{Rt_s}{L}} V_{MMC}\, sin(\frac{\pi}{3}-\delta-\psi_1)}{Z_1} - \frac{V_{MMC}\, sin(\omega_s t_s + \frac{\pi}{3} - \delta - \psi_1)}{Z_1} \tag{5.5}$$

$$I_o = \frac{V_1}{R}(1-e^{-\frac{Rt_s}{L}}) + I_{o3}\, e^{-\frac{Rt_s}{L}} + \frac{e^{-\frac{Rt_s}{L}} V_{MMC}\, sin(\frac{2\pi}{3}-\delta-\psi_1)}{Z_1} - \frac{V_{MMC}\, sin(\omega_s t_s + \frac{2\pi}{3} - \delta - \psi_1)}{Z_1} \tag{5.6}$$

$$-I_o = e^{-3Rt_s/L} I_o + \frac{V_1}{R}(1 - e^{-Rt_s/L} + e^{-2Rt_s/L} - e^{-3Rt_s/L}) + \frac{V_2}{R}(e^{-Rt_s/L} - e^{-2Rt_s/L}) - \frac{V_{MMC}}{Z} sin(\delta + \psi)(1 + e^{-3Rt_s/L}) + I_{o,error,k^{th}} \tag{5.7}$$

$$I_{o,error,k^{th}} = -\frac{^{k}V_{MMC}}{Z_k}(sin(k\,\delta + \psi_k))(1 + e^{-3Rt_s/L}) \tag{5.8}$$

$$-I_{soft} = \frac{V_1}{R}\frac{(1 + e^{-Rt_s/L} - e^{-2Rt_s/L} - e^{-3Rt_s/L})}{(1 + e^{-3Rt_s/L})} - \sum_{k=1,3,5,..} \frac{^{k}V_{MMC}}{Z_k} sin(k\,\delta + \psi_k)$$
$$= G\,V_1 - \sum_{n=1,3,5,..} \frac{^{k}V_{MMC}}{Z_k} sin(k\,\delta + \psi_k)$$
$$t_s = \frac{1}{6\,f_s}, V_1 = \frac{V_{ldc}}{3} \tag{5.9}$$

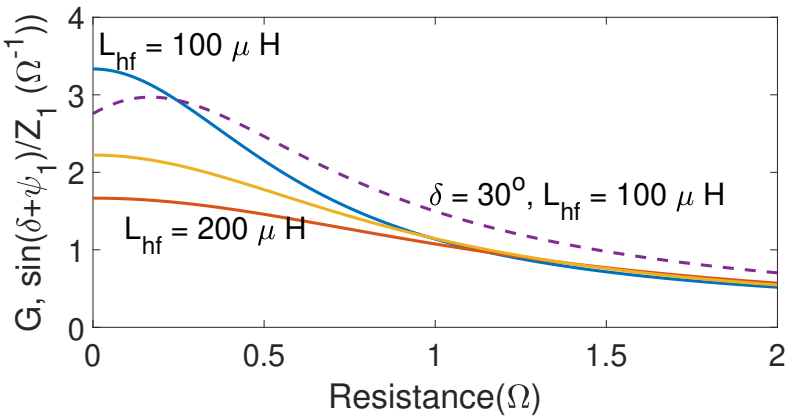


Figure 5.2: Plot of G in Eq. (5.9)(solid lines) with HF-link resistance on the x-axis for HF-link inductance values of $L_{hf} = 100\mu H, 150\mu H$ and $200\mu H$. Also shown is the dependence of the coefficient of the MMC voltage fundamental component(dotted line) on the link resistance for $\delta = 30^o$.

The soft-switching current using Eq. (5.9) is plotted against variation of *mag* defined

in Eq. (3.8), in fig. 5.3. ${}^{k}V_{MMC}$ in Eq. (5.9) is given by Eq. (3.3) and the switching angles are determined acoording to the online optimization scheme. This optimization algorithm is run offline to yield the switching angles for fixed values of load angle δ and mag and the data are plotted as solid lines in fig. 5.3 and fig. 5.4. The simulation data is also plotted using the circuit schematic in fig. 3.12 for various values of mag in fig. 5.3 for a load angle of $\pi/6$ and for various values of δ in fig. 5.4 with $mag = 1.6$. ${}^{k}V_{MMC}$ in Eq. (5.9) could be positive or negative depending on the switching angles $alpha_1$ and $alpha_2$ in Eq. (3.3). The impedance angle of the fundamental ψ_1 is almost 90^o thus implying that increase in δ should favour soft-switching. However, if ${}^{5}V_{MMC}$ or ${}^{7}V_{MMC}$ are positive and $k\,\delta + psi_k$ is around an angle such as 45^o, this trend may depart depending on the magnitudes of these harmonics. In fig. 5.3 and fig. 5.4, a negative current implies current is available to discharge the top switch of the HF-link 2L-VSC. As mag increases, this current generally decreases in these plots and similarly increase in load angle δ generally increases it for the magnitudes plotted in fig. 5.4. It is interesting to note the cross over of the lines for $\delta = 0$ and $\delta = \pi/6$ at higher values of mag and this is not surprising considering the dominance of the MMC voltage harmonics in Eq. (5.9) in these regions. The expression in Eq. (5.9) is further used to ensure sufficient current for soft-switching at the two-level converter switches under unity displacement power factor operation, by the appropriate design of the HF-link in this chapter. A plot of the factor G in Eq. (5.9) is shown in fig. 5.2 and it is seen that for the link resistance varying from 0.01 to 0.2 Ω, it varies from 3.35 to 3.05 and the factor $2\frac{sin(\delta+\psi)}{Z}$ for $\delta = 30^o$ varies from 2.76 to 2.97. This implies that the soft-switching current should decrease with increase in resistance as shown in fig. 5.5. Also, for other values of L_{hf} namely 150 μH and 200 μH, G in the same range of resistance values decreases to a peak value of 2.22 and 1.68 respectively as shown in fig. 5.2. The overall dependence of I_{soft} on increase in HF-link inductance in given in Section 5.0.3 under unity DPF operation.

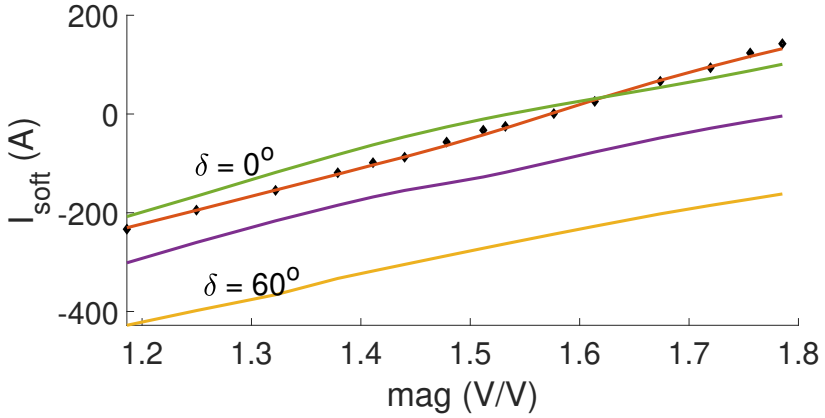


Figure 5.3: I_{soft} plotted against varying magnitude of V_{MMC} and δ as a parameter

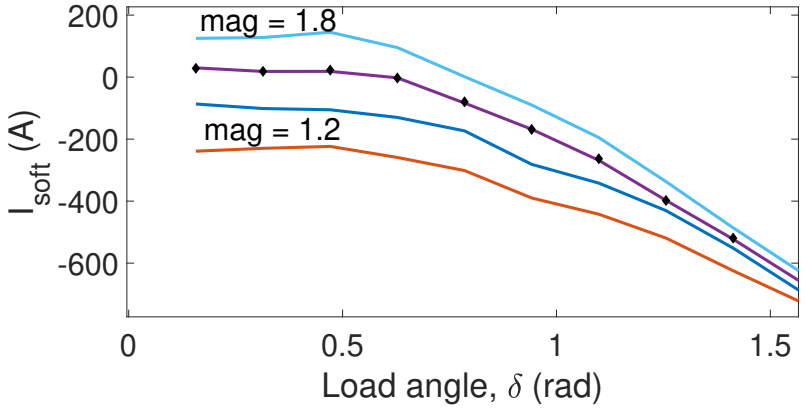


Figure 5.4: I_{soft} plotted against varying load angle and *mag* as a parameter.

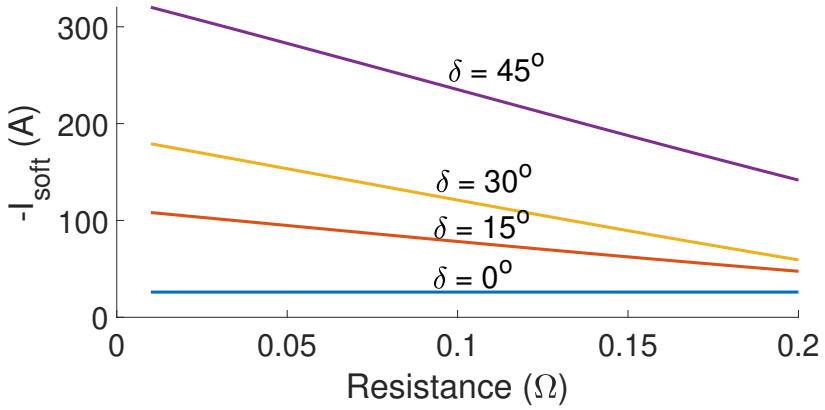


Figure 5.5: I_{soft} plotted against varying link resistance with load angle δ as a parameter for $mag = 1.5$ and $L_{hf} = 112.5\mu H$

5.0.2 Transformer Turns Ratio

The maximum turns ratio $1 : T_{max}$ of the transformer, from the low voltage side to the high voltage side is obtained by ensuring that Eq. (3.20) is satisfied i.e., V_{MMC} is of sufficiently large magnitude, atleast at the maximum value of mag defined in Eq. (3.8). This is depicted in Eq. (5.10a) and T_{max} can be written as shown in Eq. (5.10b). The term dependent on δ_m in Eq. (5.10b) keeps increasing with increase in delta thus reducing T_{max}. Beyond a certain load angle, δ_m, T_{max} decreases below T_{min} given in Eq. (5.10d) and this is the limiting load angle δ_m.

T_{min} is given by the lowest turns ratio, so that atleast at the minimum value of mag, the required lowest value of V_{MMC} for unity DPF is attained i.e., Eq. (5.10c) holds good. The maximum value of $cos(\delta) + \frac{R}{X}sin(\delta)$ is given by $1/cos(tan^{-1}\frac{R}{X})$ and using this we get Eq. (5.10d).

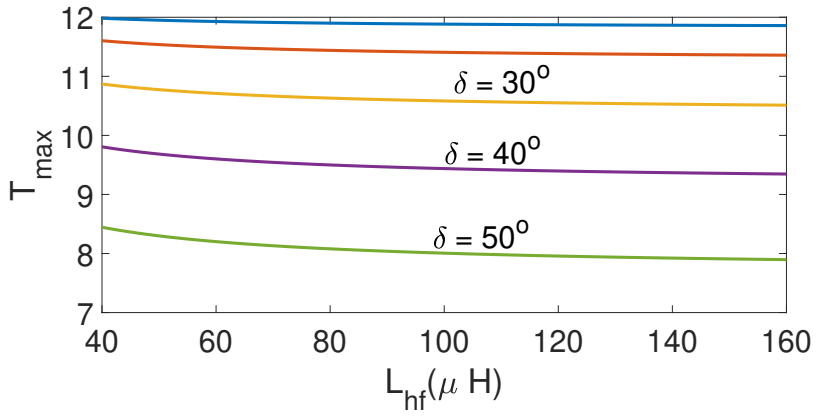


Figure 5.6: Variation of T_{max} with increase in L_{hf} with load angle, δ as a parameter. The limiting load angle $\delta_m = 50^o$ here, is obtained when T_{max} decreases below T_{min}.

$$\frac{4}{\pi}\frac{V_{hdc,min}}{NT}mag_{max} \geq \frac{4}{\pi}\frac{V_{ldc}}{2}\frac{1}{cos(\delta)+\frac{R}{X}sin(\delta)} \tag{5.10a}$$

$$T_{max} = \frac{V_{hdc,min}(mag_{max})}{N\frac{Vldc}{2}(\frac{1}{cos(\delta_m)+\frac{R}{X}sin(\delta_m)})} \tag{5.10b}$$

$$\frac{4}{\pi}\frac{V_{hdc,max}}{NT}mag_{min} \leq \frac{4}{\pi}\frac{V_{ldc}}{2}\frac{1}{cos(\delta)+\frac{R}{X}sin(\delta)} \tag{5.10c}$$

$$T_{min} = \frac{V_{hdc,max}(mag_{min})}{N\frac{Vldc}{2}cos(tan^{-1}\frac{R}{X})} \tag{5.10d}$$

5.0.3 Soft switching

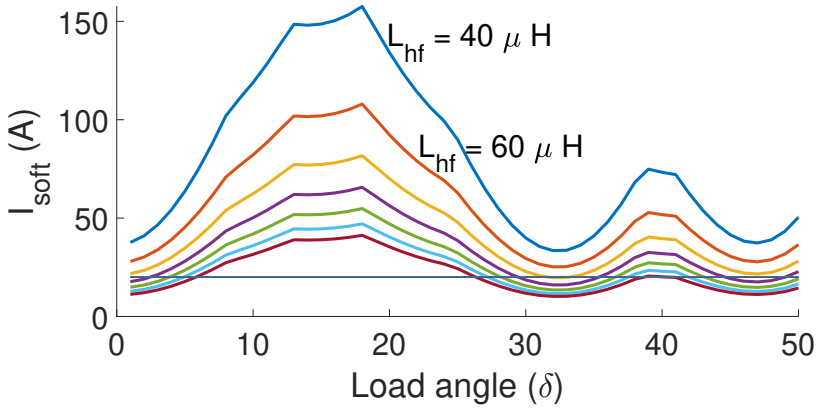


Figure 5.7: Variation of worst-case current available for soft switching with load angle in degrees on x-axis and Lhf as a parameter under unity DPF operation.

The condition for soft-switching at the HF link two level converter switches is shown in Eq. (5.11), where I_{soft} is the minimum magnitude of current required during 0-1 transitions of the switches. Only the magnitude of current is considered here and a positive current refers to current available to discharge the switch capacitances.

$$\frac{V_1}{R}\frac{1+e^{-x}-e^{-2x}-e^{-3x}}{1+e^{-3x}} - \frac{V_{MMC}}{Z}sin(\delta+\psi) - \sum_{k=5,7,11}\frac{{}^{k}V_{MMC}}{Z_k}\,sin(k\,\delta+\psi_k) > |I_{soft}| \tag{5.11}$$

As described in section 5.0.1, ${}^{k}V_{MMC}$ in Eq. (5.11) depends on cosine functions of switching angles as per Eq. (3.3) and it could be positive or negative. Also, depending on the load angle, $sin(k\,\delta+\psi_k)$ could be postive or negative. ${}^{k}V_{MMC}$ is atmost $1/k$ times V_{MMC} and thus, in order to find the worst case current available for soft switching, ${}^{k}V_{MMC} = V_{MMC}/k$ and $|(sin(k\delta+\psi_k))|$ is substituted for the terms inside the summation in Eq. (5.11). V_{MMC} in Eq. (5.11) is written using the condition for unity DPF in Eq. (3.20) thus extracting I_{soft} while maintaining unity DPF operation. The resulting equation is plotted for variation in load angle δ on the x-axis, with L_{hf} as a parameter. It is observed that I_{soft} decreases with increase in L_{hf}.

For the IGBT output capacitance of $100\,nF$ at the HF link two-level converter and deadtime of $10us$[98], the current required to discharge the low voltage dc bus value of

1000V on a top device in the two-level converter is found to be -20 A. Actually, the output capacitance of the device is a highly non-linear function of the collector-emitter voltage[98] and the highest value of this capacitance during the switch state transition is used here. Here, the effective capacitance is taken to be $2 * 100nF$ since the top and bottom device output capacitances come in parallel during the switch state transition. It is observed from fig. 5.7 that for any L_{hf} value $\leq 80\mu H$ which is the third line from the top in fig. 5.7, this condition is satisfied for all load angles in the range 0 to 50 degrees. Considering another instance of $L_{hf} = 100\mu H$, the fourth line from the top in fig. 5.7, the worst case condition for soft switching is not satisfied in the load angle range of 30 to 35 degrees and also for very low load angles less than 2 degrees.

5.0.4 % THD

The % THD is designed using empirically obtained maximum cost values from the optimization problem. $max(f_{min})$ was observed to be 0.0085 for a load angle $\delta < \delta_m$ of 45^o and for $mag = 1.95$. The % of RMS current due to harmonics from Eq. (5.12) was found to be 17.5% of the fundamental for $V_c^{'}$ corresponding to the lowest value of $V_{hdc} = 12kV$ and the nominal value of HF link current $I_{fund} = 500$ A corresponding to 160 kW per phase. The value of L_{hf} was readjusted to $100\,\mu H$ to reduce the THD to within 15% to a value of 14%. The soft-switching current condition seemed to be easily met since the value of V_n, for $n = 5, 7, 11$, was not simultaneously the maximum value of $1/n$ and positive at any time.

$$\%RMS_{har} = 100\sqrt{(\frac{4V_c^{'}}{\pi})^2 \frac{max(f_{min})}{X^2 I_{fund}^2}} \tag{5.12}$$

5.0.5 Maximum Power Transfer

Finally, the maximum power transfer possible for a limiting load angle of $\delta_m = 50^o$ and ensuring unity DPF for an $L_{hf} = 100\,\mu H$ is found using Eq. (3.21) to be $370.4\,kW$ per phase. Here, a V_{2L} of $\frac{4V_{ldc}/2}{\sqrt{2}pi}$ was used as the RMS value of the low voltage side fundamental voltage. The parameters designed in this section are summarized in cloumn 1 of table 7.1.

Parameter	MATLAB/SIMULINK	OPAL-RT, HF-link circuit	OPAL-RT, BB-MMC PET
Nominal DC bus voltage	13 kV	13 kV	11 kV
Module Capacitor Precharge voltage	2500 V	2500 V	5000 V
Nominal Grid Phase voltage, frequency	5000 V,50 Hz	-	4000 V, 50 Hz
Module Capacitor-Grid side,HF side	5 mF, 250μF	-,250 μF	5 mF, 250 μF
Arm Inductor-Grid side, HF side	4mH,200μH	-, 200 μH	4mH,200μH
Arm Resistance	0.1 Ω	0.1 Ω	0.1 Ω
MMC Module Switching frequency- Grid side, HF side	4000 Hz, 1000 Hz	-, 1000 Hz	4000 Hz, 1000 Hz
No. of Modules per Leg- Grid side, HF side	8,8	-,8	4,4
Grid Interface R-L filter	R = 0.1 Ω, L=16.58mH	-	R = 0.1 Ω, L=16.58mH
HF transformer turns ratio	8	9	8
HF-link impedance referred to low voltage side	R = 0.03 Ω, L = 100 μH	R = 0.2 Ω, L = 200 μH	R = 0.1 Ω, L = 100 μH
Low voltage DC bus voltage	1000 V	1000 V	-
Low voltage side DC bus capacitance	4 mF	4 mF	-
Wind turbine side AC source voltage(L-L,rms)	400 V	-	-
Wind turbine side converter filter	R = 0.01 Ω, L = 0.35 mH	-	-
HF side R-L load	-	-	R = 0.5 Ω, L = 1 μH

Table 5.1: Simulation Parameters for SIMULINK model in Chapter 2 and Chapter 3-column 1, and OPAL-RT HIL simulations in Chapter 3-column 2 and Chapter 2- column 3.

5.1 Summary

An analytical expression for the current available for soft-switching at the low-voltage side two-level converter in the topology under research was obtained. Design equations involving soft-switching condition at the HF link 2L-VSC, condition for unity DPF, maximum power transferred under unity DPF and percentage rms value of harmonics in the HF link current were used to arrive at the transformer turns ratio and HF link leakage inductance values.

Chapter 6

A Multi-port Modular Multilevel Converter Architecture with Decoupled Power Flow Control for Grid Integration of Heterogeneous Renewable Energy Resources

Recent surge in the adoption and grid-integration of renewable distributed energy resources (DERs) at utility scale has spurred the interest in power-electronic architectures for interface at medium-voltage (MV) grid. The constant endeavor to achieve higher power densities has brought forth the need for multi-port converter topologies capable of integrating heterogeneous energy resources through a common interface scheme. In this paper, a novel high-frequency link transformer based multi-port power converter termed Distributed-Phase-MMC (DP-MMC) is proposed for the grid-integration of DERs at MV level. The topology has several advantages such as modularity at sub-module as well as sub-system level, decoupled/independent power flow through its input ports and

reduced voltage stresses in the HF-transformer windings. A simplified equivalent circuit and a phasor-based analysis are proposed for the system, which provide qualitative and quantitative insights into the power transfer mechanism across different ports. In addition, a control scheme is proposed based on this analysis that ensures stable operation of the system while injecting the required active/reactive power to the grid. The proposed scheme achieves the critical objective of unifying dispatchable storage systems with intermittent renewable energy systems at MV-level. Detailed MATLAB-Simulink results validate the overall operation and control of the proposed multi-port DP-MMC architecture.

6.1 Introduction

Integration of utility-scale distributed energy resources (DERs) and energy storage systems (ESS) to the medium voltage grid through cascaded power-converter topologies have gathered significant attention [42, 43, 40, 41]. These cascaded converters typically aim to interface DERs at about 1 kV to the MV grid between 5 kV - 34.5 kV [44, 45].

To match the difference in voltage levels and for isolation purposes, these interfaces usually involve a PE high-frequency transformer [44, 99, 45, 40, 41]. A major setback in most of these prior-art topologies is that each submodule of the cascaded converter is required to employ a HF-transformer, which is of single-phase type rendering the system bulky in size and weight. In particular, the power-circuit topology in [44, 99, 45] demands equal power sharing between the cascaded sub-modules (SMs). This is a challenge, especially when the DER is a PV source tracking the maximum power point (MPP). In this case, equal power sharing is not feasible without having a dedicated battery storage system integrated through an appropriate port. In [100], a three-phase HF-transformer based stacked-converter topology is considered, yielding size reduction. This topology is also multi-port in nature, but it does not allow decoupled bidirectional power flow at the AC ports. In other such cascaded multi-port topologies proposed in [41, 40], exclusive closed-loop control-systems are required at sub-module level to regulate SM-capacitor voltages, that allows grid-interactive ancillary services.
Modular-multilevel converter (MMC) based topologies have the major advantage of requiring only a single three-phase HF transformer for the grid-interface [14, 15, 16].

Reference [94] proposes a variant in the form of a three-phase series connected MMC topology that offers the benefit of reduced number of sub-modules for processing given power. However, the downside in these topologies is that the transformer terminal-to-terminal winding voltage stresses at the high voltage side and the primary to secondary voltage stresses are notably high (as high as MV level) [17, 18, 52]. Also, these architectures are not multi-port and do not contain parallel power-transfer paths through the HF-link.

In order to address the concerns existing in these prior-art topologies, a novel MMC based multi-port converter architecture with HF-links is proposed in this chapter, that allows integration of heterogeneous renewable DERs and battery storage systems. The salient features and advantages of this topology are: (a) the intra- and inter-winding voltage stresses on the HF transformer are reduced by a factor equal to the number of AC-ports, (b) customizable number of HF-transformers chosen based on AC-port count and winding stress, but independent of total SM-count (that is needed to reach MV level), (c) bidirectional and decoupled power flow at each port without requiring battery storage, that allows for power exchange between these AC ports as required, and (d) multiple MMC based converters can be interfaced to a central grid-side converter via a common dc-link, (e) capability to offer grid-interactive ancillary services via control of the single common dc-link voltage across the cascaded converters.

We refer to this topology as a distributed-phase (DP)-MMC, as the SMs of the cascaded converter (of each phase) are distributed into various groups corresponding to the multiple AC-ports.

A simplified equivalent circuit and a phasor-based analysis are proposed for the DP-MMC, based on which the power transfer mechanism across various ports is studied qualitatively and quantitatively. A control scheme is proposed for operation of the DP-MMC that ensures stability and tracks the power commands at the input/output ports. Detailed switched model results in MATLAB/Simulink are presented that validate the overall operation and control of the proposed multi-port DP-MMC architecture.

6.2 Proposed Power Circuit Architecture

The detailed circuit diagram of the proposed Distributed-Phase MMC for the case of two output ports is shown in Fig.6.1b. The sub-modules of each phase of the MMC is distributed into as many groups as the number of output ports. The phase legs contain one upper arm, one lower arm and an intermediate arm between every pair of three-phase AC ports. The exists a HF transformer at each of the output ports and the number of such ports can be customized to be two or more. The transformer neutrals are left floating. With N_g groups or output ports, the transformer terminal-to-terminal voltage stress is limited to $(\frac{1}{N_g})^{th}$ of that in [14, 15, 16, 17, 18, 52] and the transformer turns ratio required to match the low voltage side is also reduced correspondingly. Each port allows power to be drawn in, sent out or to draw zero power from the low voltage side source independent of the other output ports. The grid side converter is the regular MMC without any transformer in connecting to the medium voltage grid.

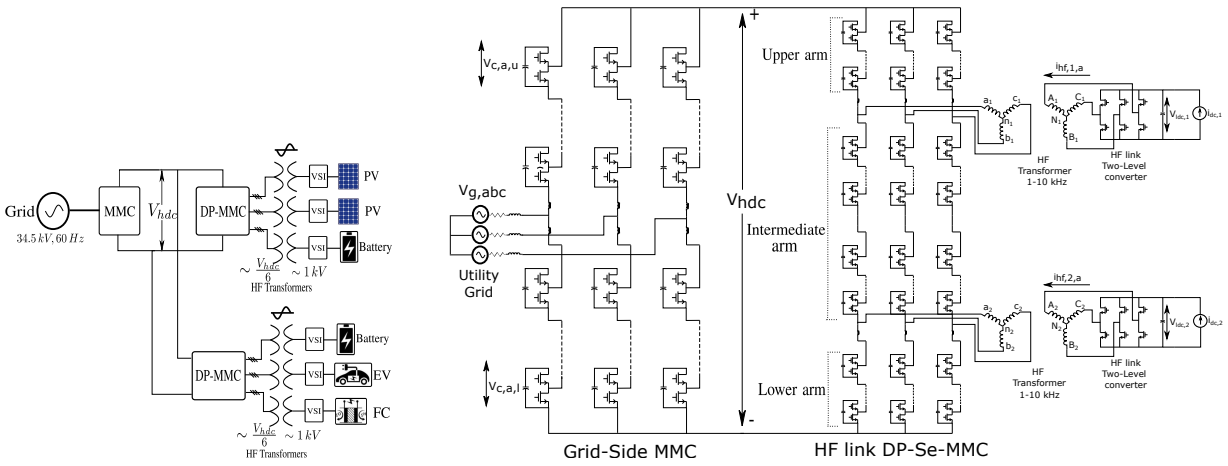


Figure 6.1: (a). A block diagram of the presented DP-MMC topology in a multi-converter configuration with a common dc link interfacing PV arrays, electric vehicle charging stations, storage units and fuel cells. (b). Detailed circuit diagram of the proposed DP-MMC based PET architecture

6.3 Operating Scheme

The GS-MMC controls the currents drawn from the grid and performs the functions of V_{hdc} control, providing reactive power support to the grid, operation during grid unbalance and faults, virtual inertia support to the grid for frequency regulation and providing other grid ancillary services. The GS-MMC sub-modules are modulated using phase-shifted carrier sine-triangle PWM(PSC-PWM) ensuring minimum carrier frequency harmonics in the output voltage. PSC-PWM is especially suited when the number of sub-modules in the MMC are small as is the case here. The effective switching frequency harmonics in the output voltage is at $2N$ times the switching frequency of each sub-module.

The HF-DPMMC ensures minimum conduction losses in the HF-links by current harmonic control and controlling the currents to be at unity displacement power factor with the HF-2LVSCs. The HF-2LVSCs maintains the low voltage dc links at the commanded reference value. The switching frequencies of both the HF-DPMMC and HF side 2L-VSC at each of the output ports are the same as the output voltage fundamental frequency across the transformers. The HF side 2L-VSCs operate in six-step mode since there are six steps in every fundamental cycle of its line-neutral voltage waveform. Both the primary and the secondary sides of the HF transformers don't see PWM waveforms thus avoiding the dv/dt stresses involved if a carrier frequency at 10 times the HF link frequency is used for modulation.

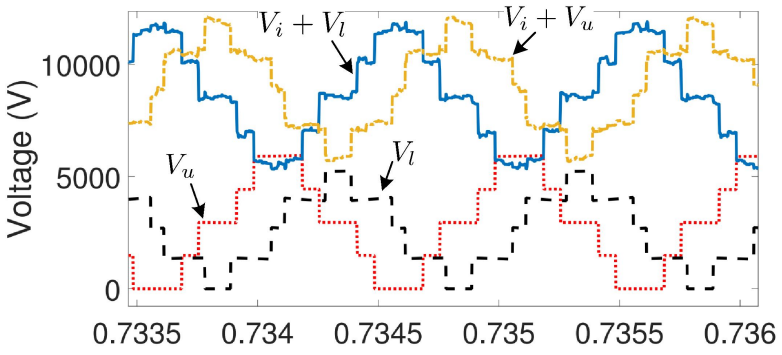


Figure 6.2: Comparison of DP-MMC arm-voltages (Phase-A)

6.4 DP-MMC PWM and Voltage Balancing Controls

The PWM scheme of the DP-MMC is such that the voltage at the phase poles corresponding to each output port is formed as a result of voltages in the arms connecting to the negative of the dc bus and the voltage in the arms connecting to the positive of the dc bus. For example, with two output ports in the DP-MMC, the pole voltages in the upper port is formed by the upper arm voltage and the sum of the intermediate arm and lower arm voltages. Similarly the pole voltages at the lower port is formed as a result of the lower arm voltage and sum of the upper arm and intermediate arm voltages. These voltages for phase a are shown in Fig.6.2. This operating mechanism leads to the HF transformer neutral points of the upper port and lower port to be at dc voltages of value $\frac{3V_{hdc}}{4}$ and $\frac{V_{hdc}}{4}$ respectively.

The number of sub-modules to be inserted in the intermediate arm are determined as $N_2^* + N_3^*$ and shown in Fig.6.3. The modulating signal in-phase with the output voltage at the upper port which similar to the lower arm modulating signal in a conventional MMC, and the one out of phase with the voltage at the lower port are used to generate N_2^* and N_3^*. The sub-modules of the intermediate arm are sorted and balanced together. Similarly, the number of sub-modules to be inserted in the upper arm and lower arm of the DP-MMC are obtained as N_1^* and N_4^* shown in Fig.6.3. The voltage balancing of the sub-modules is performed among the respective modules in these arms.

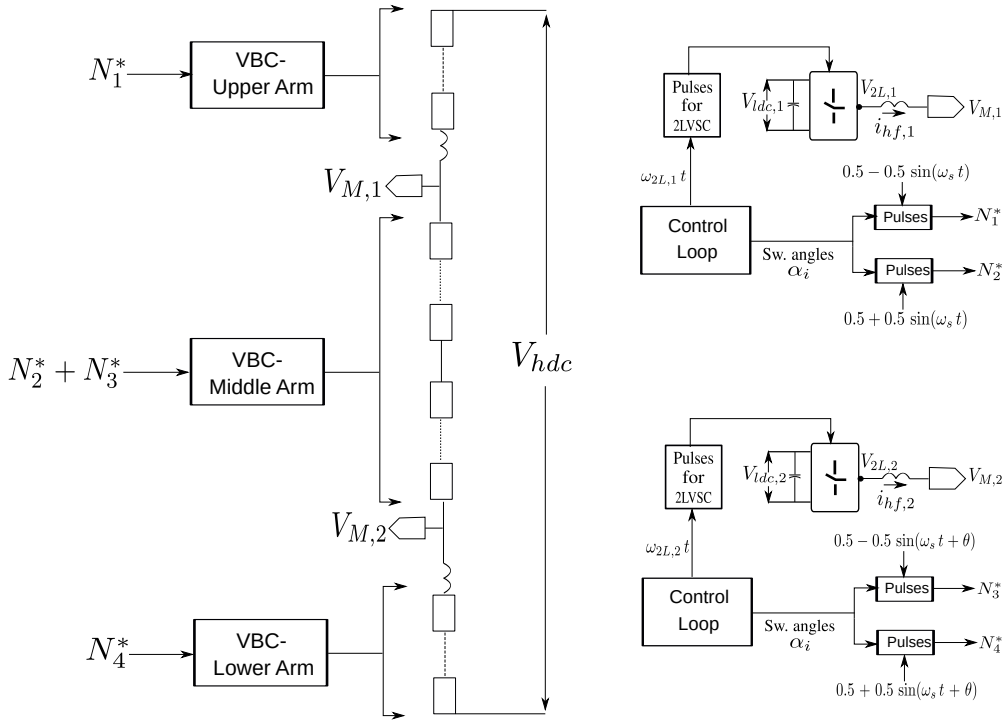


Figure 6.3: Overall voltage balancing, gate pulse generation and control scheme for the DP-MMC sub-modules

6.5 Simplified Equivalent Circuits

The overall equivalent circuit of the DP-MMC operation is depicted in Fig.6.4a. The HF-links are current controlled for the required power transfer. They are at unity displacement power factor with the 2L-VSC voltage. Thus, the 2L-VSC voltage and the link impedance can be replaced by constant current sources of magnitudes given by Eq. (6.1) and shown in Fig.6.4c.

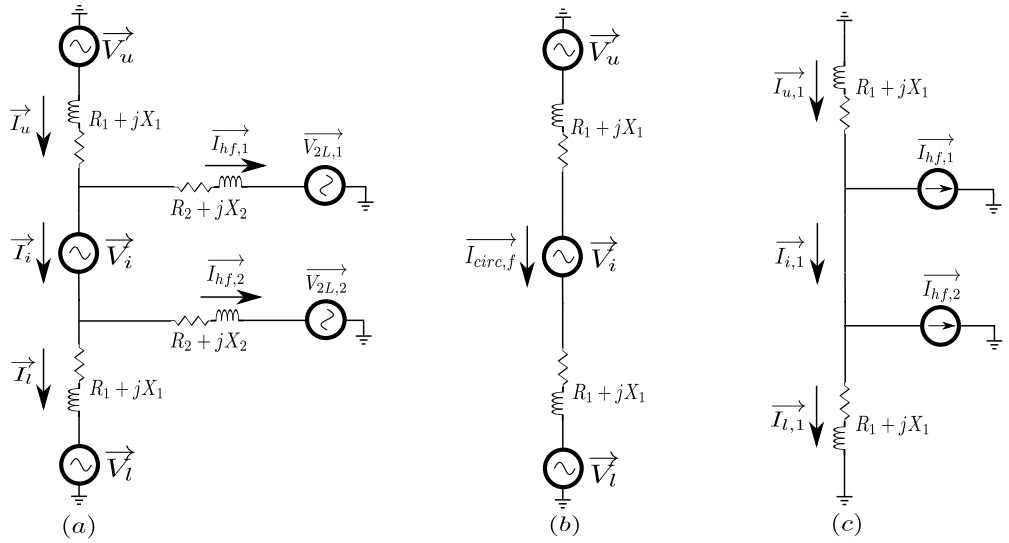


Figure 6.4: (a) DP-MMC equivalent circuit at HF-link fundamental frequency, (b) equivalent circuit for circulating current $I_{cir,f}$, and (c) equivalent circuit for output currents from AC-ports.

The rest of the analysis assumes that the phase angle of $\overrightarrow{V_{M,1}}$ to be zero i.e., the reference vector. Also, since the drop across the arm inductance and arm resistances are small, the phase angle of $\overrightarrow{V_u}$ is assumed to be 180^o i.e., it is exactly out of phase with $V_{M,1}$.

$$V_{2L,1} = \frac{4}{\pi} V_{ldc,1}, V_{2L,2} = \frac{4}{\pi} V_{ldc,2}$$

$$I_{hf,1} = \frac{P_1}{V_{2L,1}}, I_{hf,2} = \frac{P_2}{V_{2L,2}},$$

$$\overrightarrow{I_{hf,1}} = I_{hf,1} \angle -\delta_1, \overrightarrow{I_{hf,2}} = I_{hf,2} \angle -\delta_2, \tag{6.1}$$

$$\overrightarrow{V_{2L,1}} = V_{2L,1} \angle -\delta_1, \overrightarrow{V_{2L,2}} = V_{2L,2} \angle -\delta_2$$

$$\delta_1 = \angle(V_{2L,1} + I_{hf,1}\, Z_2), \delta_2 = \angle(V_{2L,2} + I_{hf,2}\, Z_2) + \theta$$

The pole voltages of the converter at each of the output ports can then be written using

the 2L-VSC voltage and drop across the link impedance as shown in Eq. (6.2).

$$\begin{aligned} \overrightarrow{V_{M,1}} &= \overrightarrow{V_{2L,1}} + \overrightarrow{I_{hf,1}}\, Z_2 \\ \overrightarrow{V_{M,2}} &= \overrightarrow{V_{2L,2}} + \overrightarrow{I_{hf,2}}\, Z_2 \end{aligned} \tag{6.2}$$

The DP-MMC arm currents are obtained as superpositions of currents from Fig.6.4c and Fig.6.4b and shown in Eq. (6.3),Eq. (6.4) and Eq. (6.5).

$$\begin{aligned} \overrightarrow{I_{u,1}} &= 0.5\,\overrightarrow{Ihf,1} + 0.5\,\overrightarrow{I_{hf,2}} \\ \overrightarrow{I_{i,1}} &= -0.5\,\overrightarrow{Ihf,1} + 0.5\,\overrightarrow{I_{hf,2}} \\ \overrightarrow{I_{l,1}} &= -0.5\,\overrightarrow{Ihf,1} - 0.5\,\overrightarrow{I_{hf,2}} \end{aligned} \tag{6.3}$$

$$I_{circ,f} = \frac{\overrightarrow{V_u} + \overrightarrow{V_i} + \overrightarrow{V_l}}{2\,\overrightarrow{Z_1}} \tag{6.4}$$

$$\begin{aligned} \overrightarrow{I_u} &= \overrightarrow{I_{u,1}} + \overrightarrow{I_{circ,f}} \\ \overrightarrow{I_i} &= \overrightarrow{I_{i,1}} + \overrightarrow{I_{circ,f}} \\ \overrightarrow{I_l} &= \overrightarrow{I_{l,1}} + \overrightarrow{I_{circ,f}} \end{aligned} \tag{6.5}$$

The pole voltages $V_{M,1}$ and $V_{M,2}$ at the output ports is written in terms of the arm voltages and 2L-VSC voltages in Eq. (6.6).

$$\begin{aligned} \overrightarrow{V_{M,1}} &= (\overrightarrow{V_l} - \overrightarrow{V_u})\, A + (\overrightarrow{V_{2L,1}} + \overrightarrow{V_{2L,2}})\, B + \overrightarrow{V_i}\, C \\ \overrightarrow{V_{M,2}} &= (\overrightarrow{V_l} - \overrightarrow{V_u})\, A + (\overrightarrow{V_{2L,1}} + \overrightarrow{V_{2L,2}})\, B - \overrightarrow{V_i}\, C \end{aligned} \tag{6.6}$$

The quantities A,B,C are given in Eq. (6.7).

$$A = \frac{(Z_2||Z_1)||Z_2}{(Z_2||Z_1)||Z_2 + Z_1}$$

$$B = \frac{(Z_1||Z_2)||Z_1}{(Z_1||Z_2)||Z_1 + Z_2} \tag{6.7}$$

$$C = 0.5$$

The intermediate arm voltage is expressed in terms of $V_{M,1}$ and $V_{M,2}$ as shown in Eq. (6.8).

$$\overrightarrow{V_i} = \overrightarrow{V_{M,1}} - \overrightarrow{V_{M,2}} \tag{6.8}$$

Since, $V_{M,1}$, $V_{M,2}$, $V_{2L,1}$ and $V_{2L,2}$ are known the upper and lower arm voltages are solved using Eq. (6.6) and Eq. (6.8) as shown in Eq. (6.9) and Eq. (6.10).

$$\overrightarrow{V_{lu}} = \overrightarrow{V_l} - \overrightarrow{V_u} = \frac{1}{A}(0.5(\overrightarrow{V_{M,1}} + \overrightarrow{V_{M,2}}) - B(\overrightarrow{V_{2L,1}} + \overrightarrow{V_{2L,2}})) \tag{6.9}$$

$$\begin{aligned} \overrightarrow{V_u} &= -Re[\overrightarrow{V_{lu}}] + \frac{Im[\overrightarrow{V_{lu}}]}{tan(\theta)} + j0 \\ \overrightarrow{V_l} &= \frac{Im[\overrightarrow{V_{lu}}]}{tan(\theta)} + jIm[\overrightarrow{V_{lu}}] \end{aligned} \tag{6.10}$$

Ignoring the losses in the converter, the dc current drawn from the high voltage dc link can be expressed as shown in Eq. (6.11).

$$I_{dc} = \frac{Re[1.5\,(\overrightarrow{V_{2L,1}}\overrightarrow{I_{hf,1}}^* + \overrightarrow{V_{2L,2}}\overrightarrow{I_{hf,2}}^*)]}{V_{dc}} \tag{6.11}$$

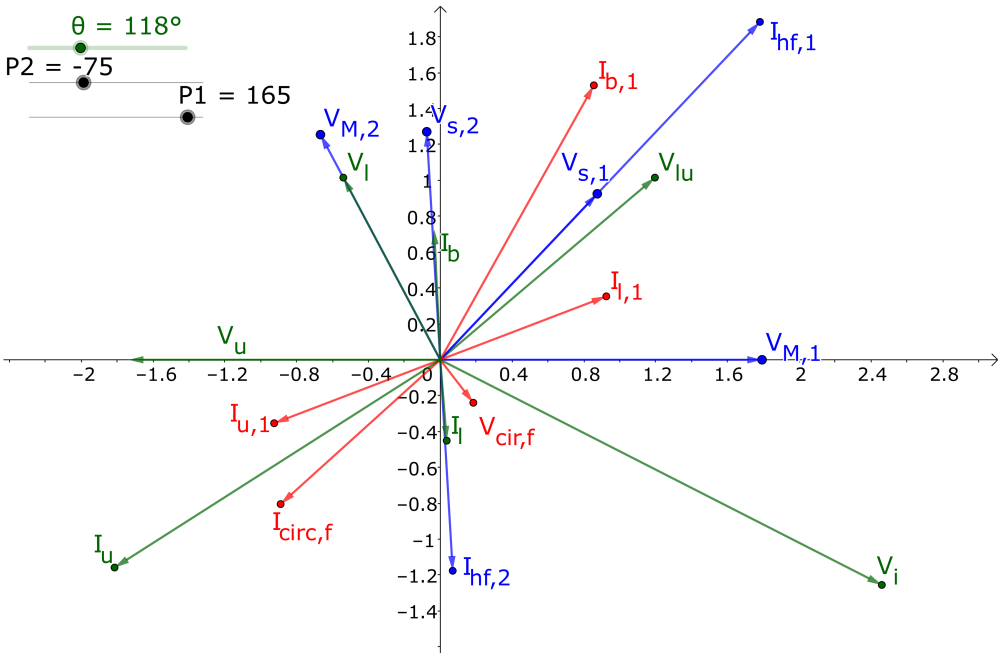


Figure 6.5: Phasor diagram showing relationship between key quantities as a function of power at the three-phase ports and the phase shift between DP-MMC groups

6.5.1 Selection of θ

To obtain the sub-module capacitor voltages in the DP-MMC arms, the system of equations in Eq. (6.12) are solved for the five unknown variables $m_1, m_2, V_{c,1}, V_{c,2}$ and $V_{c,3}$ as a function of the parameter θ.

$$\begin{aligned} 4\,m_1\,V_{c,1} &= -V_u, \\ 4\,m_1\,V_{c,2} - 4\,m_2\,V_{c,2}\,cos(\theta) &= Re[V_i], \\ 4\,m_2\,V_{c,2}\,sin(\theta) &= -Im[V_i], \\ 4\,m_2\,V_{c,3}\,sin(\theta) &= Im[V_l] \end{aligned} \tag{6.12}$$

$$0.5\,(4\,V_{c,1} + 8\,V_{c,2} + 4\,V_{c,3}) + \frac{2\,I_{dc}}{3}\,R_1 = V_{dc}$$

The resulting expressions for the capacitor voltages are provided in Eq. (6.13),

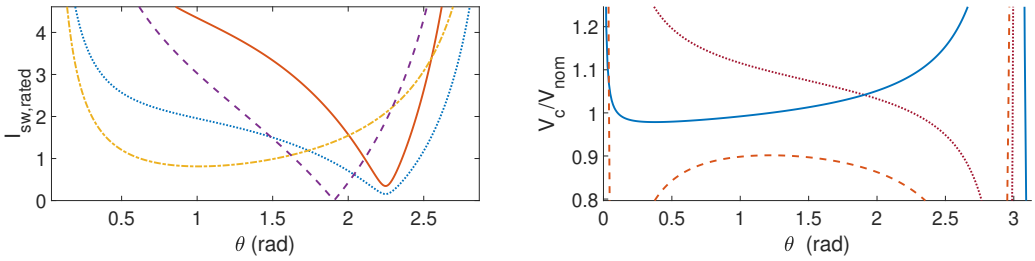
$$\begin{aligned} V_{c,1} &= \frac{E\left(-V_u\, Im[\overrightarrow{V_i}] sin(\theta)\right)}{D} \\ V_{c,2} &= \frac{E\left(-Im[\overrightarrow{V_i}]\right)\left(cos(\theta) Im[\overrightarrow{V_i}] - sin(\theta) Re[\overrightarrow{V_i}]\right)}{D} \\ V_{c,3} &= \frac{E\left(Im[\overrightarrow{V_l}]\right)\left(cos(\theta) Im[\overrightarrow{V_i}] - sin(\theta) Re[\overrightarrow{V_i}]\right)}{D} \end{aligned} \tag{6.13}$$

where D and E are given by,

$$\begin{aligned} D{=}(-V_u\, Im[\overrightarrow{V_i}] + 2 Im[\overrightarrow{V_i}] Re[\overrightarrow{V_i}] - Im[\overrightarrow{V_l}] Re[\overrightarrow{V_i}])\, sin(\theta) \\ - 2\, Im[\overrightarrow{V_i}]^2\, cos(\theta) + Im[\overrightarrow{V_i}]\, Im[\overrightarrow{V_l}]\, cos(\theta) \end{aligned} \tag{6.14}$$

$$E = 0.5\left(V_{dc} - 2\, I_{dc}\, R_1\right) \tag{6.15}$$

Fig.6.5 shows a phasor diagram showing the relationship between the fundamental components of various converter quantities as a function of θ and power absorbed at the output ports in case of two such three-phase outputs. It is observed that the value of θ that minimizes converter arm currents and capacitor voltage ratings depends on the value of powers absorbed at the output ports. Fig.6.6 shows the arm current and capacitor voltage over-ratings as a function of θ, plotted using Eq.6.13 and Eq.6.5, for the case of $P_1 = 1$ MW and $P_2 = 450$ kW.



(a) (b)

Figure 6.6: Over-ratings of : a). semiconductor currents and b).sub-module capacitor voltages, as a function of θ

6.6 Results

6.6.1 Circuit Ratings

Table 6.1: Ratings and system parameters

Parameter	MATLAB-Simulink
Nominal DC-bus voltage	13 kV
Nominal Grid voltage, frequency	5000 V(p)k,50 Hz
SM Capacitance - Grid side, HF side	5 mF, 500μF
Arm Inductance-Grid side, HF side	4mH,200μH
Arm Resistance	0.1 Ω
MMC f_{sw}- Grid side, HF side	4000 Hz, 1000 Hz
N_{SM}- Grid side, HF side	8,16
Grid Interface R-L filter	R = 0.1 Ω, L=16.58mH
HF transformer turns-ratio	4
HF-link impedance (LV side)	R = 0.03 Ω, L = 50 μH
LV DC-bus	1000 V
LV DC-bus capacitance	4 mF

In this section, simulation results from MATLAB/SIMULINK demonstrating the operation of the circuit topology in Fig.6.1b are provided.

The DP-MMC sub-module capacitances and arm inductances were chosen to be 500 μF and 200 μH respectively to limit the sub-module capacitor ripple to within 5% of its nominal value. The HF transformer turns ratio was chosen to be 4 at both the ports. The number of modules per leg of the DP-MMC was chosen to be 16. The circuit parameters of the overall topology are provided in table 6.1.

6.6.2 Overall Operation

Fig.6.7a-Fig.6.7b show the three-phase currents at the two ports due to a step change in power from 1 MW to 600 kW and from 450 kW to 1 MW occurring at 1 sec at the two ports.

Fig.6.7c show the phase change in the three-phase grid currents due to resultant power direction reversal at the grid side.

Fig.6.7d-Fig.6.7e show the phase relationship of the phase-a HF link currents at the two ports and at the grid side with the pole voltages of the 2L-VSC and grid voltage respectively. The power is flowing into the port 1 as observed from Fig.6.7d and out of port 2 in Fig.6.7e and the power direction at the grid reverses in Fig.6.7f at 1 sec.

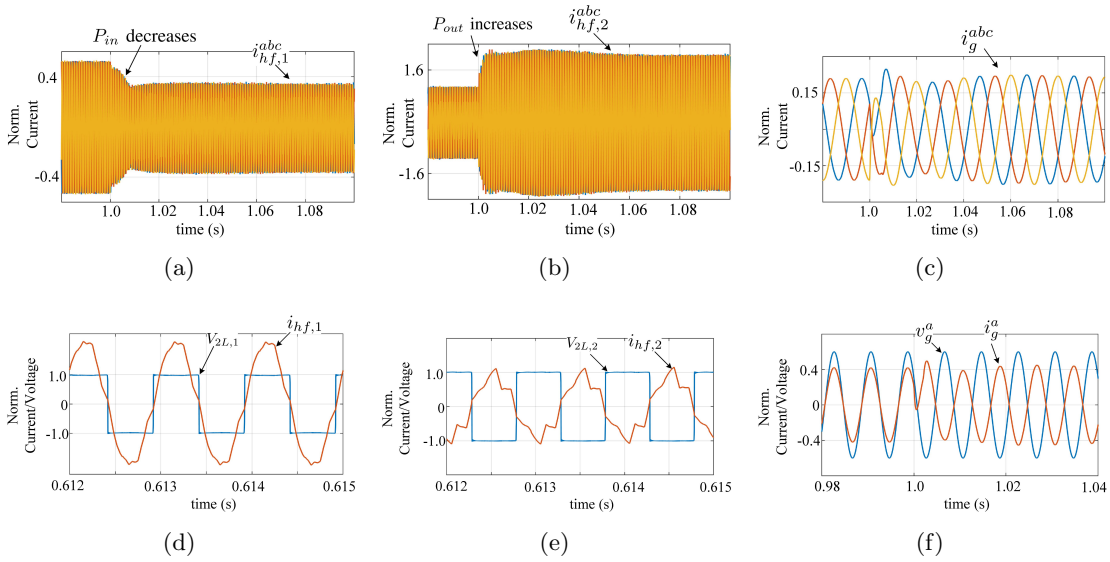
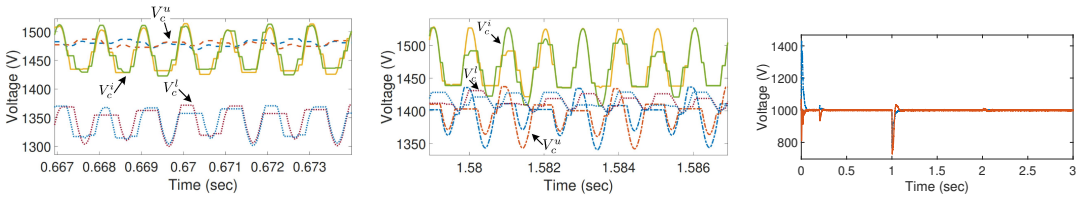


Figure 6.7: (a). HFAC port 1 three-phase currents - power into the port decreases from 1MW to 600 kW at 1 sec (b). HFAC port 2 three-phase currents - power out of the port increases from 450kW to 1 MW at 1 sec (c). Grid currents change phase relationship with grid voltage to transition from power being delivered to the grid to power being absorbed from the grid (d). Zoomed version of (a) with phase a current and 2L-VSC pole voltage (e). Zoomed version of (b) with phase a current and 2L-VSC pole voltage (f).Single phase version of (c) with phase a grid current and voltage



(a) (b) (c)

Figure 6.8: (a) Arm capacitor voltages prior to 1 sec (b) Repeat of (a) after 1 sec (c). The two HF-link 2L-VSC dc bus voltages

The sub-module capacitor voltages of the three arms before and after the step change in power occurs at the two ports is shown in Fig.6.8a and Fig.6.8b. The low voltage side dc link voltage at the two ports is also shown in Fig.6.8c and is regulated to be constant at 1000V.

6.7 Conclusion

In this paper, a novel multi-port power converter termed Distributed-Phase-MMC is proposed for the integration of heterogeneous DERs to MV grid. The overall operation is analyzed using an appropriate equivalent circuit and phasor analysis. An appropriate control scheme is presented that achieves bidirectional as well as decoupled power flow at each of its AC-ports. The arm current and sub-module capacitor voltage expressions as a function of power and phase-shift angle are analytically evaluated, which aids sizing and rating of semiconductor devices. The operation of the DP-MMC is demonstrated using a full-order switched model simulation in MATLAB-Simulink for various power-command changes. The results verify the bidirectionality and decoupled power flow capability of the DP-MMC. The proposed scheme achieves the critical objective of unifying dispatchable storage systems with intermittent renewable energy systems at MV-level voltage.

Chapter 7

A Novel Proposal and Control Scheme for Virtual Inertia

The increasing penetration of renewable energy sources into the grid has brought upon the need for synthetic inertia. This is to be meted out by the corresponding power electronic interfaces integrating these Distributed Energy Sources into the grid. In particular, a novel interface scheme using back-to-back MMCs to integrate wind turbines to the collection grid at voltages of 34.5kV has been shown to possess substantial potential for virtual inertia in this chapter. The large stored potential energy in the virtual dc link between the MMCs is used to emulate the characteristics of a synchronous generator in case of step load changes. Inertial parameters of the back-to-back MMC has been derived enabling comparison with a synchronous generator connected to the grid. A control scheme to provide additional power to emulate the inertial characteristics of a synchronous generator has been developed. The corresponding over-ratings of currents and voltages to support this function have been quantitatively described. Frequency response characteristics due to step load changes in a weak grid has been considerably improved with the proposed interface scheme as verified by simulation results.

7.1 Introduction

The back-to-back MMC proposed here has a virtual dc link which is created by an appropriately chosen modulation scheme[18]. The effective capacitance here, is trivially

small compared to the effective capacitance in between the MMCs in case of a HVDC transmission line[60, 58] where the DC bus is a rigid DC source irrespective of the number of modules inserted in each leg of the MMCs. This virtual dc link is at voltages of the order of twice the collection grid voltage which results in a large stored potential energy in it.

In existing wind turbine systems, to provide inertial support in case of step load changes, the stored kinetic energy in the turbine is utilized which results in slowing down of the wind turbine and deviation from its MPPT operating point[101]. Also, the duration of this additional power is limited depending upon the inertia of the wind turbines and the extent to which they can be slowed down. After this additional power due to inertia stops, the wind turbine has to be brought back up to speed of the MPPT operating point[101]. This requires that only a fraction of the available power, even at these non-optimal speeds of the wind turbine is available to feed to the grid. This results in not extracting the maximum power available from the wind during this speed excursion away from the MPPT. In this paper, an alternative means of providing inertia using the stored energy in the virtual dc link in the back-to-back MMC is proposed which can ensure that additional power due to inertia can be provided for a longer time while simultaneously extracting the maximum power available from the wind at all times.

7.2 System Topology Considered for Analysis

The system topology considered for the analysis of the performance of inertial control of the back-to-back MMC is shown in fig. 7.1. Since the focus of this paper is to investigate the control of back-to-back MMCs in the PET, the wind turbine and its associated converter in fig. 3.1 have been replaced by a ideal three-phase high frequency ac source for simulation purposes. The back-to-back MMC, is connected to a 3 phase HF AC source through a HF, Y-Yg 1:1 transformer on the load side. Also, the detailed circuit diagram of the back-to-back MMCs forming the virtual dc link and the overall control schemes employed for the grid connected operation of the MMC has been described in [18].

The relevant parameters and ratings of the various components in the system topology are given in table 7.1. Load 1 in fig. 7.1 is switched ON to simulate a step load change and Load 2 remains connected throughout. Also, the nomenclature of some

variables used in the analysis is provided in table 7.2.

7.3 Equivalent Swing-Equation Small Signal Model of the MMC

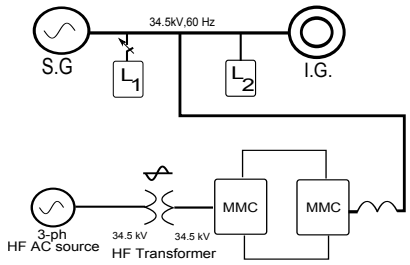


Figure 7.1: System topology considered for studying inertial characteristics of the MMC

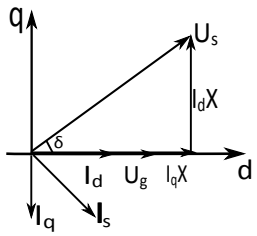


Figure 7.2: Phasor diagram involving MMC's output phase voltage, phase current and the grid voltage

The power balance equation of a synchronous generator is as shown in Eq. (7.1), where P_{in} is the power input from the governor as per Eq. (7.2). The rate of change of kinetic energy stored in the rotor, $\frac{d(\frac{1}{2}J\omega_m^2)}{dt}$ results in the term due to inertia of the rotor in Eq. (7.1). In heavy rotors, a large inertia, J of the machines, results in the required $\frac{d\omega_m}{dt}$ of the machines to be small for a given step load change. Using $P_{out} = \frac{EV_{out}\sin(\delta)}{X_s}$, and linearizing Eq. (7.1) about the nominal operating point δ, in p.u. basis and assuming no change in P_{in}, we get Eq. (7.3). Replacing the coefficients in Eq. (7.3) by T_j, T_s and T_D, we get Eq. (7.4). Eq. (7.4) has been represented in the form of a schematic in fig. 7.3[102], which is the small signal model of the swing equation of the synchronous generator.

$$P_{in} - P_{out} = J\omega_m \frac{d\omega_m}{dt} + D(\omega_m - \omega_g) \tag{7.1}$$

$$P_{in} = K_p(\omega_o - \omega_m) + P_o \tag{7.2}$$

$$H\frac{d\Delta\omega_{m,pu}}{dt} = \frac{-EV_{out}cos(\delta)}{S_B\, X_s}\,\Delta\delta - (D\,\omega_s/S_B)\,\Delta\omega_{m,pu} \tag{7.3}$$

$$T_j \frac{d\Delta\omega_{m,pu}}{dt} = -T_s\,\Delta\delta - T_D\,\Delta\omega_{m,pu} \tag{7.4}$$

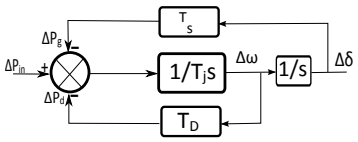


Figure 7.3: Small signal linearized model of the swing equation of the Synchronous generator

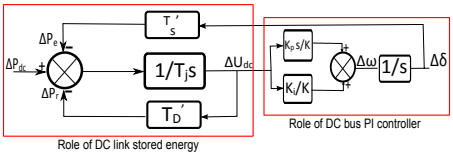


Figure 7.4: Equivalent small signal linearized model of the swing equation of the MMC

The equivalent small signal model of a voltage source converter(VSC) emulating the synchronous generator's swing equation has been derived in [102]. This model has been analyzed in two parts showing the role of the DC bus voltage controller (A) and the role of stored electrostatic potential energy in the DC link (B) to bring out the effect of the large energy stored as described below.

7.3.1 Role of DC bus voltage controller in the emulated swing equation

The phasor diagram involving the grid side MMC's output phase voltage(U_s) and phase current(I_s), and the grid phase voltage(U_g) is shown in fig. 7.2. From fig. 7.2, we see that $I_d = \frac{U_s}{X}\,sin(\delta)$. Here the d-q axis is aligned along the grid voltage and so real power is controlled by controlling I_d as can be seen by setting $V_q = 0$ in Eq. (7.5)[103]. Thus we have Eq. (7.6). Linearizing about the nominal operating point δ , we obtain Eq. (7.7). Noting that $s\,\Delta\delta = \Delta\omega$, we get Eq. (7.8).

$$\begin{aligned} P &= V_d I_d + V_q I_q \\ Q &= -V_d I_q + V_q I_d \end{aligned} \tag{7.5}$$

$$\frac{U_s}{X}\,sin(\delta) = -(K_p + \frac{K_i}{s})(U_{dc} - u_{dc}) \tag{7.6}$$

$$s(\frac{U_s\,cos(\delta)}{X})\,\Delta\delta = (s\,K_p + K_i)\Delta U_{dc} \tag{7.7}$$

$$\Delta\omega = \frac{1}{K}(sK_p + K_i)\Delta U_{dc} \tag{7.8}$$

This part of the emulated swing equation is represented in the second half of the schematic in fig. 7.4[102].

7.3.2 Role of the DC link stored energy in the emulated swing equation

The first part of fig. 7.4 involves stored energy in the dc link. The power balance equation of the dc link in the back-to-back MMCs is as shown in Eq. (7.9). The damping resistor power term in Eq. (7.9) takes into account the equivalent parasitic resistance in parallel at the dc link. However, since parasitic resistances of the module capacitors is quite large, its effect is negligible. Later on, to provide damping due to absolute change in frequency, a separate control scheme will be discussed. Replacing $E_k = \frac{CU_{dc}^2}{2}$, $P_{out} = \frac{U_s U_g sin(\delta)}{X}$ and $P_{damp} = \frac{u_{dc}^2}{R}$ in Eq. (7.9) we get Eq. (7.10). Comparing Eq. (7.1) and Eq. (7.10), we see that instead of the large moment of inertia, J of the machines associated with heavy rotors, in case of the back-to-back MMC, u_{dc} being large results in rate of change of the dc bus voltage required to be small. In other words, a change in voltage of 1 kV around 20kV releases much larger energy compared to a change in 1kV around 3 kV. Converting Eq. (7.10) on a pu basis and replacing C in Eq. (7.10) by $\frac{2E_k}{U_{dc}^2}$, we have Eq. (7.11). Linearizing about the nominal operating point, and assuming no change in dc input power which is actually the power output from the wind turbine, we get Eq. (7.12).

$$\frac{dE_k}{dt} = P_{dc} - P_{out} - P_{damp} \tag{7.9}$$

$$C\, u_{dc} \frac{du_{dc}}{dt} = P_{dc} - \frac{U_s U_g sin(\delta)}{X} - \frac{u_{dc}^2}{R} \tag{7.10}$$

$$\frac{2\,E_k}{S_B}\,\frac{du_{dc}^*}{dt} = \frac{P_{dc}}{S_B} - \frac{U_s U_g sin(\delta)}{S_B\, X} - \frac{u_{dc}^2}{S_B\, R} \tag{7.11}$$

$$\frac{2\,E_k}{S_B}\frac{d\Delta u_{dc,pu}}{dt} = -\frac{U_s U_g cos(\delta)}{S_B\, X}\Delta\delta - \frac{2\,U_{dc}^2}{S_B\, R}\,\Delta u_{dc,pu} \tag{7.12}$$

Replacing the various coefficients in Eq. (7.12) we get,

$$T_j^{'}\frac{d\Delta u_{dc}}{dt} = -T_s^{'}\Delta\delta - T_D^{'}\Delta u_{dc} \tag{7.13}$$

where, $T_s^{'} = \frac{U_s\, U_g}{S_B\, X} cos(\delta)$, $T_D^{'} = \frac{2U_{dc}^2}{S_B\, R}$ and $T_j^{'} = \frac{2E_k}{I_B U_{dc}}$. Eq. (7.13) is represented in the first half of the schematic in fig. 7.4. From Eq. (7.13), we see that the rate of change

of dc bus voltage for a particular increase in power on the RHS is small due to a large value of $T_j^{'}$.

7.4 Quantitative Analysis of Required Over-ratings

Defining the inertia constant of the MMC along the same lines as that of a synchronous generator, as the ratio of the stored potential energy to the base rating of the MMC, we have,

$$\frac{2E_k}{S_{MMC}} = H_{MMC} = \frac{C\,U_{dc}^2}{S_B} \tag{7.14}$$

where, S_{MMC} = Rated Power of a typical Wind Turbine = 60 kW(say). Since in this paper, every leg of the MMC contains 8 modules, at any instant half this number i.e., 4 modules are switched on[18]. Further, since there are 3 legs in each of the wind turbine side MMC and the grid side MMC, the net capacitance at the dc link is given by,

$$C = C_{net,hf} + C_{net,lf} = 3\,\frac{C_{mod,hf}}{4} + 3\,\frac{C_{mod,lf}}{4} \tag{7.15}$$

Using values for $C_{mod,hf} = 100\mu F, C_{mod,lf} = 1mF$, we have $C = 0.825mF$. Plugging in values of $C = 0.825mF$ and $U_{dc} = 21kV$ into Eq. (7.14), we have $H_{MMC} = 6.0637$ secs. The over-ratings of the different components of the back-to-back MMC is calculated for the cases of a three-phase fault and for a step load change as follows.

In case of a three phase to ground fault on the grid side, no power can be fed to the grid. In this situation, the wind turbine is typically shut down until the fault clears. However, with the back-to-back MMC in place, this energy from the wind turbine during the fault could be stored in the virtual dc link for some time. Substituting the rated power of the wind turbine(in p.u.) in the RHS of Eq. (7.13), and using $T_j^{'} = 6.0637$ secs, we get $\frac{d\Delta U_{dc}}{dt} = 3.4629\,kV/sec$ which implies that if the MMC is designed to sustain an over-voltage of 5kV, the fault could be sustained for 1.44 secs without having to shut down the wind turbine. Since 1 pu change in power is not accurately applied in the small-signal linearized equations, the actual time for a change in dc link voltage of 5kV is 1.27 secs. However, the above analysis serves to illustrate the application of derived equations for smaller changes in power. This over-voltage is to be shared between (N/2) modules in each leg of the MMC[18]. Thus, the percentage over-voltage rating of each module is smaller by (N/2) times.

When there is a step load increase on the grid, assuming a 100% increase in rated

power to emulate inertia and going through the analysis along similar lines as before results in a drop of 5 kV if the additional power is provided for 1.44 secs. Also, every module of the grid side MMC has to be over-rated for current by 100%.

Since the grid side MMC feeds current to the high voltage grid of the order of 34.5 kV, the actual increase in current ratings is small. To allow for a 5kV drop in dc link voltage during a step load increase, the dc link should be designed for a 5kV over-voltage room above twice the grid voltage. This can be seen from the filter design equation, Eq. (7.16), targeting a 3% THD in phase current and Eq. (7.17). In Eq. (7.16), the filter inductance required in case of the MMC is quite small with the harmonic voltages of the order of 0.1% of the fundamental at (N/2) times switching frequency of each module[18].

$$\frac{0.1\, V_{ph,MMC}}{X_{L,HF}} = 0.03\, I_{ph} \tag{7.16}$$

$$V_{ph,MMC} = I_{ph}\, X_L + V_{ph,grid} \tag{7.17}$$

In addition any over-voltage design for fault sustainability discussed earlier comes on top of this voltage.

7.5 MMC Control Schemes for Virtual Inertia

In Eq. (7.4), a step load increase on the grid causes the slowing down of the synchronous machines and the resulting $\frac{d\Delta\omega}{dt}$ causes a change in load angle, δ of the machines on the RHS of Eq. (7.4). However, in case of the MMC, a change in load does not cause any parameter of the MMC to vary inherently analogous to speed in case of synchronous machines. Thus, corresponding to a frequency deviation in case of step load changes, an appropriate controller has to designed for the MMC such that it can cause an additional power output emulating inertia. This controller causes a change in load angle, δ at the MMC output which in turn results in a $\frac{d\Delta u_{dc}}{dt}$ in Eq. (7.13). This implies that the cause is in the RHS of Eq. (7.13) in contrast to the cause being in the LHS in Eq. (7.4).

The controller for providing virtual inertia is implemented as follows: The first controller changes the DC bus voltage reference in proportion to the absolute change in frequency as shown in Eq. (7.18). Corresponding to this change in dc bus voltage reference, a change in d axis current ΔI_{dM} (in p.u.) is brought about by the dc bus PI controller and from Eq. (7.12),ignoring the term due to damping resistor, and again using

$I_d = \frac{U_s}{X}\, sin(\delta)$ we have Eq. (7.19). Substituting for E_k, and $\Delta u_{dc,M}$ from Eq. (7.18) we get Eq. (7.20). This implies that changing the dc bus voltage reference in proportion to absolute change in frequency of the grid is equivalent to increasing the power output in proportion to the rate of change of frequency of the grid[104]. Similarly for additional power due to absolute change in frequency, a change in the additional DC bus voltage reference due to K_D is provided in Eq. (7.18) and from a similar analysis as above we get, Eq. (7.21). It is of interest to note that once the dc link voltage reference has settled to a constant value, due to the action of either absolute change in frequency or the integral of change in frequency, the back-to-back MMC is called upon only to maintain this new dc link voltage. This means that the back-to-back MMC does not provide any additional power in steady state after the frequency of the grid has settled down to a steady state value and provides to the grid only what is extracted or available from the wind in steady state. $M_{SG} = J\,\omega_s$, is the coefficient responsible for power due to rate of change of frequency for a synchronous generator as seen from Eq. (7.1). Comparing the controller equations with Eq. (7.1), we have M_{MMC} and D_{MMC} as shown in Eq. (7.22). The control schematic implementing the above described controller is shown in fig. 7.5.

$$K_M \Delta f = \Delta u_{dc,M}, K_D \frac{\Delta f}{s} = \Delta u_{dc,D} \tag{7.18}$$

$$2E_k\, s\Delta u_{dc,M} = U_g\, \Delta I_{dM} \tag{7.19}$$

$$\begin{gathered} \frac{U_g\, \Delta I_{dM}}{s\, C_{MMC} U_{dc}^2} = \Delta u_{dc,M} \\ K_M\, CU_{dc}^2\, s\Delta f = U_g\, \Delta I_{dM} \end{gathered} \tag{7.20}$$

$$K_D\, CU_{dc}^2\, \Delta f = U_g\, \Delta I_{dD} \tag{7.21}$$

$$M_{MMC} = K_M\, CU_{dc}^2, D_{MMC} = K_D\, CU_{dc}^2 \tag{7.22}$$

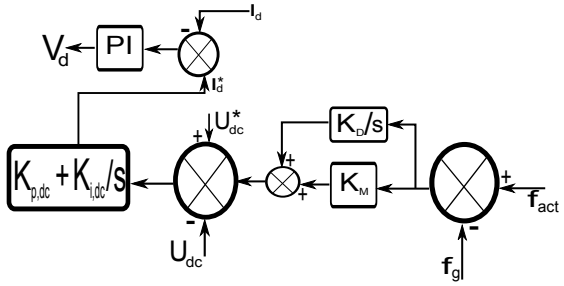


Figure 7.5: Control Scheme for implementing virtual inertia by the MMC

7.5.1 Design of the MMC inertial parameters

The design of the inertial parameters of the MMC has been done for the simulation setup in fig. 7.1. The frequency response of the grid to a step load change, not considering the secondary frequency control characteristics of the synchronous generators, is captured in the state space equations, $\dot{x} = Ax + Bu$ where,

$$\begin{aligned} A &= \begin{pmatrix} -D_{eff}\, M_{eff}^{-1} & M_{eff}^{-1} \\ -R_{eff}\tau^{-1} & \tau^{-1} \end{pmatrix}, \\ B = \begin{pmatrix} M_{eff}^{-1} & 0 \\ 0 & \tau^{-1} \end{pmatrix}, X &= \begin{pmatrix} \Delta\omega \\ \Sigma P_{G,g}^{m} \end{pmatrix}, U = \begin{pmatrix} \Delta P_{load} \\ \Sigma P_{G,g}^{r} \end{pmatrix} \end{aligned} \tag{7.23}$$

Finding the transfer function from change in frequency to change in load, we have,

$$\frac{\Delta\omega(s)}{\Delta P_{load}(s)} = \frac{-M_{eff}^{-1}\,(s + \frac{1}{\tau})}{s^2 + s\,(\frac{1}{\tau} + M_{eff}^{-1} D_{eff}) + \frac{1}{\tau} M_{eff}^{-1}(R + D_{eff})} \tag{7.24}$$

$$\begin{aligned} \omega_n &= \sqrt{\frac{D_{eff} + R_{eff}}{\tau\, M_{eff}}} \\ \zeta &= \frac{M_{eff} + \tau D_{eff}}{2\sqrt{\tau\, M_{eff}\,(D_{eff} + R_{eff})}} \end{aligned} \tag{7.25}$$

The time domain solution of frequency to a step load change is shown in Eq. (7.26).

$$\begin{aligned} \Delta\omega(t) = \frac{-1}{R + D_{eff}}\, \Delta P_{load}\, u(t) + \\ \frac{M_{eff}^{-1}\,(\frac{1}{\tau} - p_1)}{p_1\,(p_2 - p_1)}\, \Delta P_{load}\, e^{-p_1 t} + \frac{M_{eff}^{-1}\,(\frac{1}{\tau} - p_2)}{p_2\,(p_1 - p_2)}\, \Delta P_{load}\, e^{-p_2 t} \end{aligned} \tag{7.26}$$

where, $p_1 = -\zeta\omega_n + \omega_n\sqrt{\zeta^2 - 1}$ and $p_2 = -\zeta\omega_n - \omega_n\sqrt{\zeta^2 - 1}$. The transfer function helps to determine the frequency response curve when settling to the new steady state

frequency without correction by the secondary control characteristics of the synchronous machines. The zero of the transfer function depends on the time constant of governor of the synchronous machine. The inertial parameters, M_{MMC} and D_{MMC} have been designed using Eq. (7.24) to shape the time domain frequency response of the grid to a step load change, using the *sisotool* of MATLAB. By increasing M_{eff} of the grid the amplitude of the exponentials causing the transients in frequency excursion have been minimized. The frequency response of the system for various values of M_{eff} and D_{eff} as brought about by the presented control scheme for virtual inertia has been described under Section VI.

7.6 Results

The simulation parameters and ratings of various components in the simulation have mentioned in table 7.1. The simulation setup is shown in fig. 7.1. The mechanical power input to the I.G. remains constant and to that of the S.G. changes according to governor action in response to frequency deviations. Load 2 remains of 1 MW remains connected from the beginning of the simulation and Load 1 is connected at 7 secs to simulate a step load change of 1.5 MW. The initial mechanical power input to the synchronous generator is set to meet the no load condition. The frequency response of a weak grid with under three different conditions of inertial support provided by the back-to-back MMC is shown in fig. 7.7. In fig. 7.7a, inertial control loops of the back-to-back MMC are disabled and a constant power emulating that available from the wind turbine is fed to the grid. In this case, it is seen that upon the start of simulation, due to almost negligible mechanical power input to the synchronous generator, the grid frequency drops to about 0.95 p.u., before it settles back to the steady state value due to secondary control characteristics of the synchronous generator. Similarly, at t = 7secs, the grid frequency again dips to about 0.98 p.u. The virtual dc link voltage of the back-to-back MMC in this case, is controlled to be the contant reference value of of 21 kV by the dc bus voltage control of the grid side MMC. M_{eff} and D_{eff} in this case are only due to the inherent values of the machines connected to the grid and are 8700 and 0 respectively. In fig. 7.7b, an aggressive inertial support provided by the inertial control loops of the back-to-back MMC results in the grid frequency to be

maintained at close to 1 p.u. throughout the simulation. Here, $M_{eff} = 3.4276 * 10^5$ and $D_{eff} = 3.3406 * 10^4$. This leads to the dc bus voltage to drop as low as 10 kV from its nominal value of 21 kV and in such an aggressive control action, the nominal dc bus voltage may have to be rated much higher than the grid voltage. In fig. 7.7c, a balance between the drop in dc link voltage and deviation of the grid frequency during step changes in load, is achieved. In this case, the maximum dip in grid frequency is about 0.99 pu and the dc link voltage drops to a minimum value of 18 kV. $M_{eff} = 5.0791 * 10^4$ and $D_{eff} = 5.0109 * 10^3$, in this case. Thus, with the proposed back-to-back MMC based interface, the frequency response characteristics during the transient period is considerably improved. This is due to additional inertia provided by the back-to-back MMCs acting like a virtual synchronous generator during step load changes. Also, the net change in load at steady state is met solely by the synchronous generator in all three cases. A comparison between fig. 7.7a and fig. 7.7c is provided in the same plot in fig. 7.6.

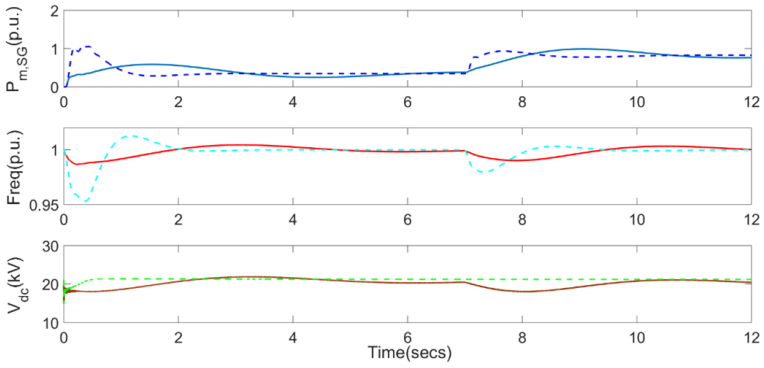
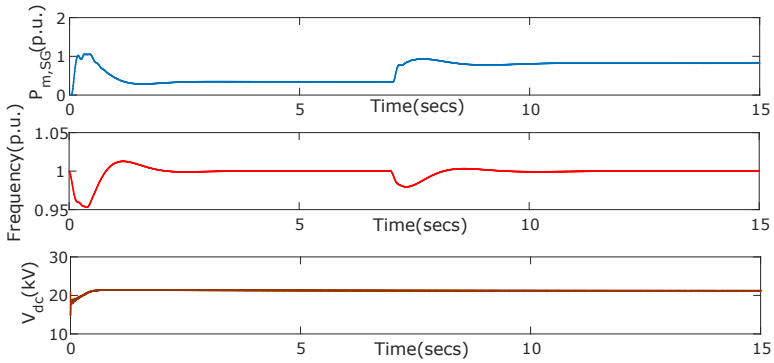
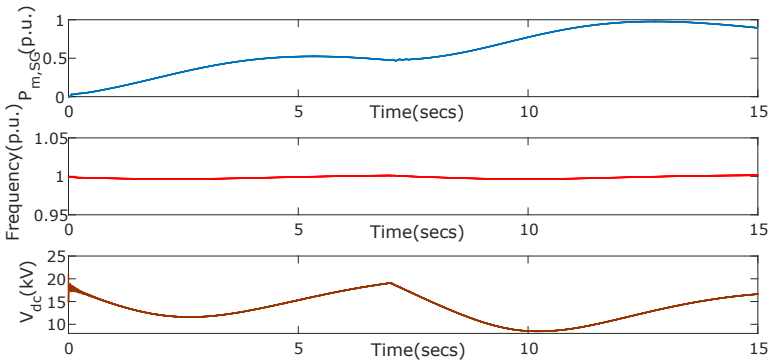


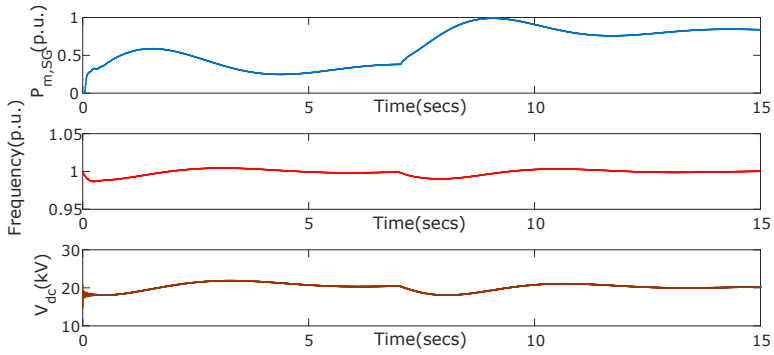
Figure 7.6: Resultant waveforms showing virtual inertia provided by the back-to-back MMCs for grid frequency regulation (top to bottom): Mechanical power input to SG in p.u., Frequency of the grid in p.u., and Virtual dc link voltage under the cases of no inertial control by the back-to-back MMCs(dashed lines) and with Inertial control achieving grid frequency regulation with frequency deviation limited to about 0.01 p.u (solid lines).



(a)



(b)



(c)

Figure 7.7: Resultant waveforms for varying inertia provided by the back-to-back MMC(top to bottom):Mechanical power input to SG in p.u., Frequency of the grid in p.u., and Virtual dc link voltage under the cases of(a)No inertial control by the back-to-back MMC, Meff =8700, Deff = 0 (b)Large inertia provided by the back-to-back MMC, Meff =3.4276e5, Deff=3.3406e4 and (c)Inertial control achieves reasonable tradeoff between dc link voltage drop and grid frequency deviation, Meff =5.0791e4, Deff = 5.0109e3

Parameter	Value
Nominal DC bus voltage	21 kV
Module Capacitor Precharge voltage	5000 V
Nominal Grid Phase voltage, frequency	5000 V,60 Hz
Module Capacitor-Grid side,Load side	10 mF, 100μF
Arm Inductor-Grid side, Load side	4mH,50μH
Arm Resistance	0.1 ohms
Module Switching frequency	1000 Hz
No. of Modules per Leg	8
Grid Interface R-L filter	R = 0.1 Ω,L=16.58mH
Nominal HF side voltage, frequency	5000V, 4000 Hz
S_{SG},S_{IG}	3.125 MVA, 1.6785 MVA
H_{SG},H_{IG}	1.07 secs, 0.0541 secs
L_1,L_2	1 MW, 1.5MW
S_B	1 MW

Table 7.1: Simulation Parameters for the circuit topology in fig. 7.1

P_{in}, P_{out}	SG power input,output
J, ω_m, ω_s	Moment of Inertia of SG, speed of rotor, grid frequency
K_d, P_o	Droop coefficient, Nominal power of governor
H, H_{SG}	Inertia constant of SG
U_s	Output per phase voltage of MMC
U_g	Per phase grid voltage
Udc	Nominal dc link voltage
u_{dc}	Actual dc link voltage
$P_{dc}, P_{out,MMC}$	Input dc power from WT, Power fed to the grid by MMC
$C, C_{net,hf}/C_{net,lf}$	Net capacitance of dc link, HF/Grid frequency side capacitance
τ, R	Governor time constant, governor regulator gain
ω_n, ζ	Natural frequency, damping ratio
S_B	Rated Power of MMC/WT

Table 7.2: Nomenclature

7.7 Summary

A novel control scheme for providing inertia using the back-to-back MMCs in the PET used for grid interface of renewables and storage is discussed. The large stored energy in the virtual DC link is exploited for providing additional power for inertia rather than extracting power from the kinetic energy of the wind turbines. The equations for the inertial parameters of the MMC have been derived and they have been designed along the same lines as that of a synchronous generator. It has been shown that the frequency response of a weak grid can be considerably improved by using the back-to-back MMCs with the virtual DC link.

Chapter 8

Conclusions

The control and operation of a back-to-back connected Modular Multilevel Converter based Power Electronic Transformer architecture to interface renewables and storage at less than 1 kV to the medium voltage grid between 5 kV -34.5 kV has been performed in this dissertation. To make the architecture ready to deployed in the industry, analysis of the converter and its control schemes under the various practical scenarios have been taken up and its operation optimized.

To minimize the conduction losses in the high-frequency link, an online optimization-based coordinated modulation of the converters ensured minimum magnitudes of the fundamental component of the current and its harmonics for a given power transfer. It was observed that the harmonics in the HF-link current reduce by as much as 60% with the proposed control schemes and the unity DPF operation helped to reduce the fundamental current amplitude by as much as 15%. The online optimization algorithm is employed in closed-loop and it dynamically reacts to changes in load angle, magnitude reference command and changes in the high voltage dc link voltage across the back-to-back connected MMCs to output an optimum set of switching angles. Its formulation is such that computational burden on the solver can be adjusted to suit the available processing power. A 720 kW SIMULINK model, 350 kW OPAL-RT HIL simulation and a 320 W hardware experimental results were used to validate the modulation of the different converters.

The voltage control of the virtual dc link, power-factor control on the grid side, grid-independent reactive power sourcing on the load side and operation under conditions

of grid voltage unbalances and faults have been demonstrated. It was ensured that the grid current quality is not affected due to the control loops involved and a Fourier series based analysis of the dc link voltage showed the mechanism by which the grid quality may deteriorate with certain types of control schemes.

Another important ancillary service to the grid namely, controlled inertial response, is naturally provided by traditional fossil-fuel driven generation sources. At high levels of penetration, electricity generated by renewables must also be able to provide these services for system stability and to make renewable sources economically competitive with traditional generation sources. The challenge with renewable-interfaced generation is the lack of mechanical inertia. A novel control scheme for providing inertia using the back-to-back MMCs in the PET used for grid interface of renewables and storage is discussed. The large stored energy in the virtual DC link is exploited for providing additional power for inertia rather than extracting power from the kinetic energy of the wind turbines. The equations for the inertial parameters of the MMC have been derived and they have been designed along the same lines as that of a synchronous generator. It has been shown that the frequency response of a weak grid can be considerably improved by using the back-to-back MMCs with the virtual DC link.

As renewable energy sources are starting to become the mainstay of the electrical grids across the world, it has become the norm to be able to integrate multiple heterogenous forms of energy through a common inteface scheme and thus achieve higher power densities. Such power conversion architectures also achieve the critical objective of unifying dispatchable forms of power such as storage and the highly intermittent forms of energy such as wind and solar. One such multi-port interface was invented in the dissertation enabling the connection of heterogenous energy sources to the medium voltage grid with unique advantages such as decoupled power flow between these three-phase AC ports and increased reliability due to reduced risks of high-frequency transformer voltage insulation failure. Analysis and simulation results were presented to understand its operating principle and control schemes.

To improve power densities, multiple MMC-based converters can be connected across their common dc link. In doing so, the PWM scheme of these converters inject certain frequency components in this common dc link. A model and equivalent circuit of the dc side of the HF-MMC was presented which unveils the sensitivity of HF-MMC to these

voltages at frequencies other than dc being injected at the dc link. A mathematical framework predicted these sensitive frequencies as a function of the MMC parameters and operating frequency within an accuracy of 2%.

8.1 Future work

The following future work as a continuation of the aspects covered in the dissertation remain:

- Coordinated Virtual Inertia from both the wind turbine and the proposed interface: Wake interaction control schemes in a wind farm result in the bigger wind turbines upstream of the wind flow to operate at higher speeds away from the maximum power point. This ensures that there is inertial power on offer from these turbines while the uncaptured power from the wind by these turbines is fully captured by the smaller wind turbine downstream of the wind flow. A coordinated inertial control scheme involving robust control design of the inertial controllers of the wind turbine and the proposed power electronic transformer should be designed.

- Implementation of the DP-MMC topology in hardware: The hardware setup already built for the HF-MMC should be modified as the proposed Distributed-Phase MMC to yield additional output three-phase AC ports. The control algorithms in simulation presented here are yet to be transferred to the hardware prototype.

- Use of SiC devices in the MMC sub-modules: This will ensure the number of sub-modules required to reach up to the medium voltage grid is small and the weight of the PET due to the sub-module capacitors is minimized when placing the interface in the wind turbine naccelle. Also, soft-switching of the MMC sub-modules is hard to be attained under all operating conditions because of the dc circulating current through the MMC arms and the wide range of power factor control required at the converters. The semiconductor loss analysis while employing SiC devices is to be done. The gate drivers for the sub-modules are to be designed with their

reference voltage at the level of the negative of the sub-module's dc link. Voltage isolation of the ICs in the gate-driver circuit where the reference voltage is at level of the medium voltage grid itself is to be investigated.

- High Frequency Transformer insulation design and voltage stresses: The quantitative analysis of the probability of transformer insulation failure due to reduced terminal-to-terminal voltage stresses within the primary winding and between the primary and secondary windings in the novel DP-MMC topology is to be carried out.

References

[1] World economic forum. Online. URL: https://www.weforum.org/agenda/2016/01/what-are-the-top-global-risks-for-2016/, 2016.

[2] Nasa goddard institute of space studies. Online. UR: https://www.bloomberg.com/graphics/2015-whats-warming-the-world/, 2015.

[3] Us energy information administration. Online. URL: https://www.eia.gov/outlooks/aeo/pdf/electricity_generation.pdf.

[4] W. A. Reass, D. M. Baca, and R. F. Gribble. Components and technologies for high frequency and high average power converters. Online. URL: https://www.nist.gov/system/files/documents/pml/high_megawatt/Reass.pdf, Apr 2008.

[5] Forecast international's energy portal. Online. URL: http://www.fi-powerweb.com/Renewable-Energy.html.

[6] Rush creek wind project, xcel energy. Online. URL: https://www.xcelenergy.com/company/rates_and_regulations/filings/rush_creek_wind_project.

[7] Mit technology review 2016. Online. URL: https://www.technologyreview.com/s/602647/in-china-and-germany-renewables-are-outgrowing-their-grids/.

[8] Siemens hvdc plus. Online. URL:www.energy.siemens.com/us/en/power-transmission/hvdc/hvdc-plus/, 2017.

[9] How a wind turbine works. Online. URL: https://www.energy.gov/eere/wind/animation-how-wind-turbine-works.

[10] Oregon green energy guide, wind farms in oregon. Online. URL: https://portlandgreenenergy.wordpress.com/wind-farms-in-oregon/.

[11] Topaz solar farm. Online. URL: http://www.firstsolar.com/en/About-Us/Projects/Topaz-SolarFarm.aspx.

[12] Sodium sulfur battery energy storage and its potential to enable further integration of wind. Online. URL: https://www.smartgrid.gov/files/documents/Sodium_Sulfur_Battery_Energy_Storage_Its_Potential_To_Enable_201006.pdf.

[13] Nanocrystalline soft magnetic material finemet. Online. URL: http://www.hilltech.com/pdf/hl-fm10-cFinemetIntro.pdf.

[14] A. K. Sahoo and N. Mohan. A power electronic transformer with sinusoidal voltages and currents using modular multilevel converter. In *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pages 3750–3757, May 2014.

[15] A. K. Sahoo and N. Mohan. High frequency link multi-winding power electronic transformer using modular multilevel converter for renewable energy integration. In *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, pages 4642–4648, Oct 2014.

[16] Ashish Sahoo. Modular converter with multilevel submodules. Online. URL: https://patents.google.com/patent/US20150124506.

[17] V. N. Vipin, A. Kshirsagar, and N. Mohan. Utility scale interface for renewables and storage using a power electronic transformer with back-to-back mmcs: A novel proposal and control scheme for virtual inertia. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–5, Sep. 2018.

[18] V. N. Vipin, A. Kshirsagar, D. Opila, and N. Mohan. Utility scale interface for renewables and storage using a power electronic transformer with back-to-back mmcs: A novel control scheme. In *2017 North American Power Symposium (NAPS)*, pages 1–6, Sep. 2017.

[19] Is offshore wind about to hit cost-competitiveness? Online. URL: https://www.forbes.com/sites/energyinnovation/2018/05/02/is-offshore-wind-about-to-hit-cost-competitiveness-in-new-york-and-new-england/?sh=7bcc610d6720.

[20] Solar energy forecasting and resource assessment. Online. URL: https://www.elsevier.com/books/solar-energy-forecasting-and-resource-assessment/kleissl/978-0-12-397177-7.

[21] Energy-charts. Online. URL: https://energy-charts.info/?l=en&c=DE.

[22] Transformation of europe's power system. Online. URL: https://www.mckinsey.com/~/media/mckinsey/dotcom/client_service/epng/pdfs/transformation_of_europes_power_system.ashx.

[23] Wind vision. Online. URL: https://www.energy.gov/sites/prod/files/wv_chapter3_impacts_of_the_wind_vision.pdf.

[24] Renewables increasingly beat even cheapest coal competitors on cost. Online. URL: https://www.irena.org/newsroom/pressreleases/2020/Jun/Renewables-Increasingly-Beat-Even-Cheapest-Coal-Competitors-on-Cost.

[25] Sie. Siemens wind turbines. Online. URL: http://www.energy.siemens.com/us/pool/hq/powergeneration/renewables/wind-power/wind%20turbines/Siemens%20Wind%20Turbine%20SWT-2.3-108_EN.pdf.

[26] W. A. Reass, D. M. Baca, and R. F. Gribble. Multi-megawatt high frequency polyphase nanocrystalline transformers. Online. URL: https://www.nist.gov/system/files/documents/pml/high_megawatt/2007_Reass-II.pdf, Jan 2007.

[27] J. Lyu, X. Zhang, X. Cai, and M. Molinas. Harmonic state-space based small-signal impedance modeling of a modular multilevel converter with consideration of internal harmonic dynamics. *IEEE Transactions on Power Electronics*, 34(3):2134–2148, March 2019.

[28] J. Lyu, X. Cai, and M. Molinas. Frequency domain stability analysis of mmc-based hvdc for wind farm integration. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(1):141–151, March 2016.

[29] R. Vidal-Albalate, H. Beltran, A. Rolán, E. Belenguer, R. Peña, and R. Blasco-Gimenez. Analysis of the performance of mmc under fault conditions in hvdc-based offshore wind farms. *IEEE Transactions on Power Delivery*, 31(2):839–847, April 2016.

[30] Lennart Harnefors, Antonios Antonopoulos, Staffan Norrga, Lennart Angquist, and Hans-Peter Nee. Dynamic analysis of modular multilevel converters. *IEEE Transactions on Industrial Electronics*, 60(7):2526–2537, 2013.

[31] Julian Freytes, Samy Akkari, Pierre Rault, Mohamed Moez Belhaouane, François Gruson, Frédéric Colas, and Xavier Guillaud. Dynamic analysis of mmc-based mtdc grids: Use of mmc energy to improve voltage behavior. *IEEE Transactions on Power Delivery*, 34(1):137–148, 2019.

[32] M. Vasiladiotis, S. Kenzelmann, N. Cherix, and A. Rufer. Power and dc link voltage control considerations for indirect ac/ac modular multilevel converters. In *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, pages 1–10, Aug 2011.

[33] R. Picas, J. Pou, S. Ceballos, J. Zaragoza, G. Konstantinou, and V. G. Agelidis. Optimal injection of harmonics in circulating currents of modular multilevel converters for capacitor voltage ripple minimization. In *2013 IEEE ECCE Asia Downunder*, pages 318–324, June 2013.

[34] Xiaoqiong He, Jun Peng, Pengcheng Han, Zi Liu, Shibin Gao, and Peng Wang. A novel advanced traction power supply system based on modular multilevel converter. *IEEE Access*, 7:165018–165028, 2019.

[35] Kei Sekiguchi, Pracha Khamphakdi, Makoto Hagiwara, and Hirofumi Akagi. A grid-level high-power btb (back-to-back) system using modular multilevel cascade converters withoutcommon dc-link capacitor. *IEEE Transactions on Industry Applications*, 50(4):2648–2659, 2014.

[36] Mingrui Li, Xiaoqian Li, Yunzhi Lin, Yingdong Wei, Chao Lu, Zhuoxuan Shen, Ziming Li, and Zengqin Li. Four-port modular multilevel ac/ac converter in continuous co-phase traction power supply application. In *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1477–1481, 2020.

[37] Binbin Li, Junlin Hu, Shaoze Zhou, and Dianguo Xu. Hybrid back-to-back mmc system for variable speed ac machine drives. *CPSS Transactions on Power Electronics and Applications*, 5(2):114–125, 2020.

[38] M. Hagiwara and H. Akagi. Control and experiment of pulsewidth-modulated modular multilevel converters. *IEEE Transactions on Power Electronics*, 24(7):1737–1746, July 2009.

[39] Qingrui Tu, Zheng Xu, Yong Chang, and Li Guan. Suppressing dc voltage ripples of mmc-hvdc under unbalanced grid conditions. *IEEE Transactions on Power Delivery*, 27(3):1332–1338, 2012.

[40] M. R. Islam, Y. Guo, and J. Zhu. A high-frequency link multilevel cascaded medium-voltage converter for direct grid integration of renewable energy systems. *IEEE Transactions on Power Electronics*, 29(8):4167–4182, Aug 2014.

[41] M. R. Islam, A. M. Mahfuz-Ur-Rahman, M. M. Islam, Y. G. Guo, and J. G. Zhu. Modular medium-voltage grid-connected converter with improved switching techniques for solar photovoltaic systems. *IEEE Transactions on Industrial Electronics*, 64(11):8887–8896, Nov 2017.

[42] B. Zhao, Q. Song, J. Li, and W. Liu. A modular multilevel dc-link front-to-front dc solid-state transformer based on high-frequency dual active phase shift for hvdc grid integration. *IEEE Transactions on Industrial Electronics*, 64(11):8919–8927, Nov 2017.

[43] B. Zhao, Q. Song, J. Li, X. Xu, and W. Liu. Comparative analysis of multilevel-high-frequency-link and multilevel-dc-link dc–dc transformers based on mmc and dual-active bridge for mvdc application. *IEEE Transactions on Power Electronics*, 33(3):2035–2049, March 2018.

[44] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Q. Huang. Research on voltage and power balance control for cascaded modular solid-state transformer. *IEEE Transactions on Power Electronics*, 26(4):1154–1166, April 2011.

[45] Q. Zhu, L. Wang, A. Q. Huang, K. Booth, and L. Zhang. 7.2-kv single-stage solid-state transformer based on the current-fed series resonant converter and 15-kv sic mosfets. *IEEE Transactions on Power Electronics*, 34(2):1099–1112, Feb 2019.

[46] V. N. Vipin and N. Mohan. Dc-side modeling of the high-frequency-link mmc in a back-to-back connected mmc-based power electronic transformer. *Journal Of Emerging And Selected Topics In Power Electronics*, submitted.

[47] V. N. Vipin and N. Mohan. Control of the high-frequency link in a back-to-back connected mmc-based power electronic transformer. *Journal Of Emerging And Selected Topics In Power Electronics*, submitted.

[48] K. Ilves, S. Norrga, L. Harnefors, and H. Nee. On energy storage requirements in modular multilevel converters. *IEEE Transactions on Power Electronics*, 29(1):77–88, Jan 2014.

[49] H. Bayat and A. Yazdani. A hybrid mmc-based photovoltaic and battery energy storage system. *IEEE Power and Energy Technology Systems Journal*, 6(1):32–40, March 2019.

[50] I. A. Gowaid, G. P. Adam, A. M. Massoud, S. Ahmed, D. Holliday, and B. W. Williams. Quasi two-level operation of modular multilevel converter for use in a high-power dc transformer with dc fault isolation capability. *IEEE Transactions on Power Electronics*, 30(1):108–123, Jan 2015.

[51] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams. Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage dc-dc transformers. *IEEE Transactions on Power Electronics*, 30(10):5439–5457, Oct 2015.

[52] J. Zhang, Z. Wang, and S. Shao. A three-phase modular multilevel dc–dc converter for power electronic transformer applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(1):140–150, March 2017.

[53] L. Bessegato, K. Ilves, L. Harnefors, S. Norrga, and S. Ostlund. Control and admittance modeling of an ac/ac modular multilevel converter for railway supplies. *IEEE Transactions on Power Electronics*, pages 1–1, 2019.

[54] M. Diaz, R. Cardenas, M. Espinoza, F. Rojas, A. Mora, J. C. Clare, and P. Wheeler. Control of wind energy conversion systems based on the modular multilevel matrix converter. *IEEE Transactions on Industrial Electronics*, 64(11):8799–8810, Nov 2017.

[55] Maryam Saeedifard and Reza Iravani. Dynamic performance of a modular multilevel back-to-back hvdc system. *IEEE Transactions on Power Delivery*, 25(4):2903–2912, 2010.

[56] D.G. Holmes and T.A. Lipo. *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE Press Series on Power Engineering. John Wiley & Sons, 2003.

[57] K. Ilves, L. Harnefors, S. Norrga, and H. Nee. Analysis and operation of modular multilevel converters with phase-shifted carrier pwm. *IEEE Transactions on Power Electronics*, 30(1):268–283, Jan 2015.

[58] D. Jovcic and K. Ahmed. *High Voltage Direct Current Transmission: Converters, Systems and DC Grids*. Wiley, 2015.

[59] M. Guan and Z. Xu. Modeling and control of a modular multilevel converter-based hvdc system under unbalanced grid conditions. *IEEE Transactions on Power Electronics*, 27(12):4858–4867, Dec 2012.

[60] K. Sharifabadi, L. Harnefors, H.P. Nee, S. Norrga, and R. Teodorescu. *Design, Control, and Application of Modular Multilevel Converters for HVDC Transmission Systems*. Wiley - IEEE. Wiley, 2016.

[61] W. G. Hurley, E. Gath, and J. G. Breslin. Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms. *IEEE Transactions on Power Electronics*, 15(2):369–376, March 2000.

[62] *Winding Resistance at High Frequencies*, chapter 5, pages 265–382. 2013, https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781118717806.ch5.

[63] A. Pérez-Basante, S. Ceballos, G. Konstantinou, J. Pou, J. Andreu, and I. M. de Alegría. (2n+1) selective harmonic elimination-pwm for modular multilevel converters: A generalized formulation and a circulating current control method. *IEEE Transactions on Power Electronics*, 33(1):802–818, Jan 2018.

[64] K. Ilves, A. Antonopoulos, S. Norrga, and H. Nee. A new modulation method for the modular multilevel converter allowing fundamental switching frequency. *IEEE Transactions on Power Electronics*, 27(8):3482–3494, Aug 2012.

[65] Y. Deng, M. Saeedifard, and R. G. Harley. An improved nearest-level modulation method for the modular multilevel converter. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1595–1600, March 2015.

[66] Y. Wang, C. Hu, R. Ding, L. Xu, C. Fu, and E. Yang. A nearest level pwm method for the mmc in dc distribution grids. *IEEE Transactions on Power Electronics*, 33(11):9209–9218, Nov 2018.

[67] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li. Improved nearest-level modulation for a modular multilevel converter with a lower submodule number. *IEEE Transactions on Power Electronics*, 31(8):5369–5377, Aug 2016.

[68] Q. Li, Z. He, and G. Tang. Investigation of the harmonic optimization approaches in the new modular multilevel converters. In *2010 Asia-Pacific Power and Energy Engineering Conference*, pages 1–6, March 2010.

[69] Y. Liu, H. Hong, and A. Q. Huang. Real-time calculation of switching angles minimizing thd for multilevel inverters with step modulation. *IEEE Transactions on Industrial Electronics*, 56(2):285–293, Feb 2009.

[70] K. Shen, D. Zhao, J. Mei, L. M. Tolbert, J. Wang, M. Ban, Y. Ji, and X. Cai. Elimination of harmonics in a modular multilevel converter using particle swarm optimization-based staircase modulation strategy. *IEEE Transactions on Industrial Electronics*, 61(10):5311–5322, Oct 2014.

[71] B. Ozpineci, L. M. Tolbert, and J. N. Chiasson. Harmonic optimization of multilevel converters using genetic algorithms. *IEEE Power Electronics Letters*, 3(3):92–95, Sep. 2005.

[72] A. Pérez-Basante, S. Ceballos, G. Konstantinou, J. Pou, I. Kortabarria, and I. M. d. Alegría. A universal formulation for multilevel selective-harmonic-eliminated pwm with half-wave symmetry. *IEEE Transactions on Power Electronics*, 34(1):943–957, Jan 2019.

[73] A. Al-Judi, H. Bierk, and E. Nowicki. Selective harmonic power optimization in multilevel inverter output. In *2011 IEEE Vehicle Power and Propulsion Conference*, pages 1–5, Sep. 2011.

[74] Xiaoming Yuan, W. Merk, H. Stemmler, and J. Allmeling. Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions. *IEEE Transactions on Industry Applications*, 38(2):523–532, 2002.

[75] David Campos-Gaona, Rafael Peña-Alzola, Jose Luis Monroy-Morales, Martin Ordonez, Olimpo Anaya-Lara, and William E. Leithead. Fast selective harmonic mitigation in multifunctional inverters using internal model controllers and synchronous reference frames. *IEEE Transactions on Industrial Electronics*, 64(8):6338–6349, 2017.

[76] P. Hu and D. Jiang. A level-increased nearest level modulation method for modular multilevel converters. *IEEE Transactions on Power Electronics*, 30(4):1836–1842, April 2015.

[77] M. Saeedifard and R. Iravani. Dynamic performance of a modular multilevel back-to-back hvdc system. In *2011 IEEE Power and Energy Society General Meeting*, pages 1–1, July 2011.

[78] D.P. Bertsekas. *Nonlinear Programming*. Athena scientific optimization and computation series. Athena Scientific, 2016.

[79] W. Forst and D. Hoffmann. *Optimization—Theory and Practice*. Springer Undergraduate Texts in Mathematics and Technology. Springer New York, 2010.

[80] Stephen J. Wright. Coordinate descent algorithms. *Math. Program.*, 151(1):3–34, June 2015.

[81] Amir. Beck and Luba. Tetruashvili. On the convergence of block coordinate descent type methods. *SIAM Journal on Optimization*, 23(4):2037–2060, 2013, https://doi.org/10.1137/120887679.

[82] L. Bessegato, L. Harnefors, K. Ilves, and S. Norrga. A method for the calculation of the ac-side admittance of a modular multilevel converter. *IEEE Transactions on Power Electronics*, 34(5):4161–4172, May 2019.

[83] L. Bessegato, K. Ilves, L. Harnefors, and S. Norrga. Effects of control on the ac-side admittance of a modular multilevel converter. *IEEE Transactions on Power Electronics*, 34(8):7206–7220, Aug 2019.

[84] J. Sun and H. Liu. Sequence impedance modeling of modular multilevel converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 5(4):1427–1443, Dec 2017.

[85] A. Ahmad, M. S. Alam, and R. Chabaan. A comprehensive review of wireless charging technologies for electric vehicles. *IEEE Transactions on Transportation Electrification*, 4(1):38–63, 2018.

[86] J. Choi, J. Xu, R. Makhoul, and J. M. R. Davila. Implementing an impedance compression network to compensate for misalignments in a wireless power transfer system. *IEEE Transactions on Power Electronics*, 34(5):4173–4184, 2019.

[87] Wen-Jian Gu and K. Harada. A new method to regulate resonant converters. *IEEE Transactions on Power Electronics*, 3(4):430–439, Oct 1988.

[88] A. S. Jurkov, A. Radomski, and D. J. Perreault. Tunable impedance matching networks based on phase-switched impedance modulation. In *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 947–954, Oct 2017.

[89] A. S. Jurkov, A. Radomski, and D. J. Perreault. Tunable matching networks based on phase-switched impedance modulation1. *IEEE Transactions on Power Electronics*, 35(10):10150–10167, 2020.

[90] Chaniotakis and Cory. Sinusoidal steady state response of linear circuits. High Megawatt Power Converter Workshop, NIST, Gaithersburg, MD, Spring 2006.

[91] S.T. Karris. *Circuit Analysis II: With MATLAB Applications*. Orchard Publications, 2003.

[92] D.J. Ewins. *Modal Testing: Theory and Practice*. Engineering dynamics series. Wiley, 1984.

[93] W. G. Hurley, W. H. Wolfle, and J. G. Breslin. Optimized transformer design: inclusive of high-frequency effects. *IEEE Transactions on Power Electronics*, 13(4):651–659, July 1998.

[94] Q. Hao, B. Ooi, F. Gao, C. Wang, and N. Li. Three-phase series-connected modular multilevel converter for hvdc application. *IEEE Transactions on Power Delivery*, 31(1):50–58, Feb 2016.

[95] R. Wang, F. Xiao, Z. Zhao, Y. Shen, and G. Yang. Effects of asymmetric coupling on winding ac resistance in medium-frequency high-power transformer. *IEEE Transactions on Magnetics*, 50(11):1–4, Nov 2014.

[96] H. Wang, K. Yan, Z. Ling, and J. Gan. Switching strategy for isolated dual-active-bridge converter. *IET Power Electronics*, 10(1):29–37, 2017.

[97] J. Everts, G. E. Sfakianakis, and E. A. Lomonova. Using fourier series to derive optimal soft-switching modulation schemes for dual active bridge converters. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 4648–4655, Sep. 2015.

[98] 3300 v, 2000 a single switch igbt module. Online. URL: `https://www.infineon.com/dgdl/Infineon-FZ2000R33HE4-DataSheet-v02_01-EN.pdf?fileId=5546d4626eab8fbf016ed15a9df22af8`.

[99] Modeling and control of single-phase single-stage isolated ac/dc converter. Online. URL:`http://www.lib.ncsu.edu/resolver/1840.20/33491`, 2016.

[100] M. Nikouie, O. Wallmark, L. Jin, L. Harnefors, and H. Nee. Dc-link stability analysis and controller design for the stacked polyphase bridges converter. *IEEE Transactions on Power Electronics*, 32(2):1666–1674, Feb 2017.

[101] J. Morren, S. W. H. de Haan, W. L. Kling, and J. A. Ferreira. Wind turbines emulating inertia and supporting primary frequency control. *IEEE Transactions on Power Systems*, 21(1):433–434, Feb 2006.

[102] L. Xiong, F. Zhuo, F. Wang, X. Liu, Y. Chen, M. Zhu, and H. Yi. Static synchronous generator model: A new perspective to investigate dynamic characteristics and stability issues of grid-tied pwm inverter. *IEEE Transactions on Power Electronics*, 31(9):6264–6280, Sept 2016.

[103] Krishna Vasudevan. Modelling and analysis of electric machines. NPTEL Courses, 2017.

[104] E. Waffenschmidt and R. S. Y. Hui. Virtual inertia with pv inverters using dc-link capacitors. In *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, pages 1–10, Sept 2016.

Appendix A

Experimental Hardware Setup

A.0.1 Experimental hardware setup for testing the HF-link control schemes

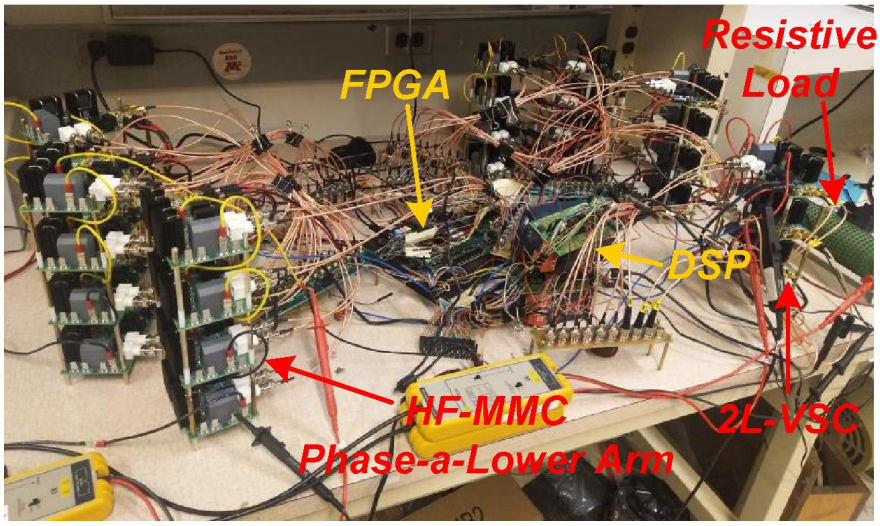


Figure A.1: Hardware setup overall view-1

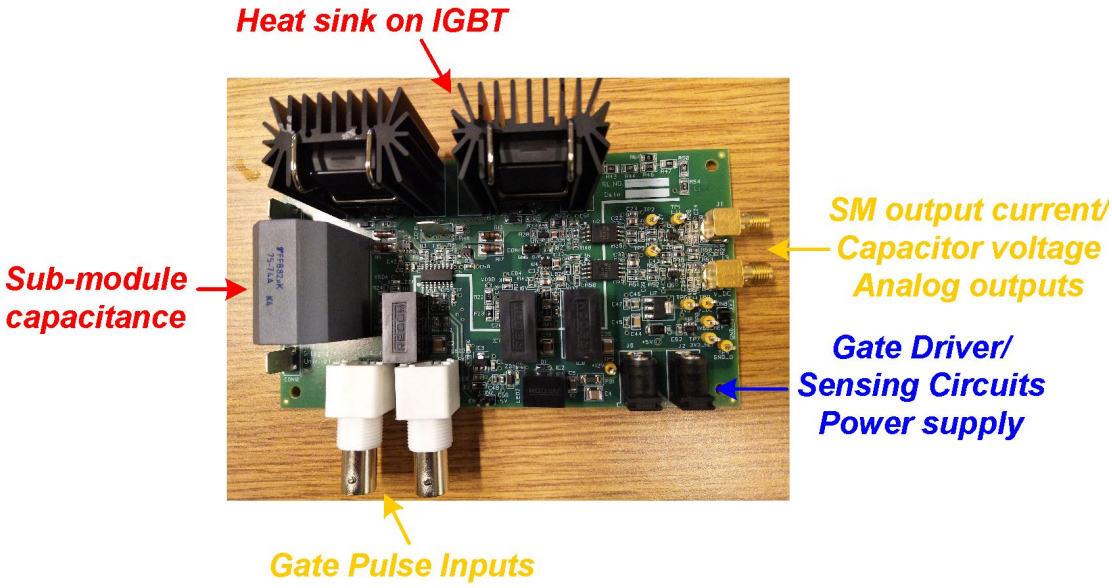


Figure A.2: Half-Bridge Submodule which are cascaded to form the MMC arms

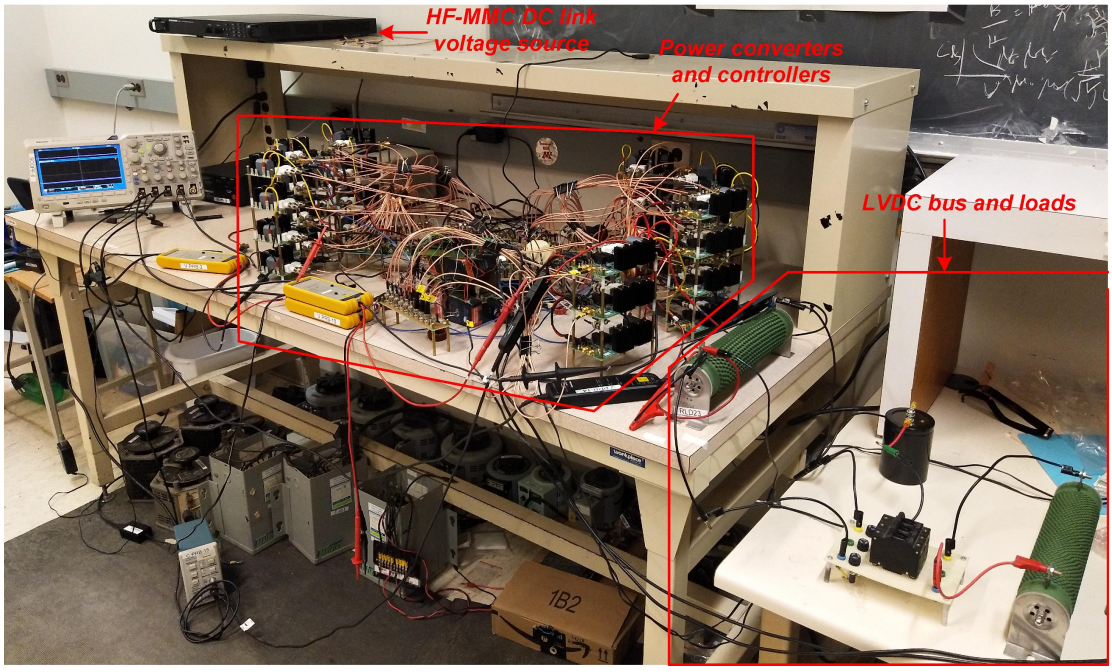


Figure A.3: Hardware setup overall view-2

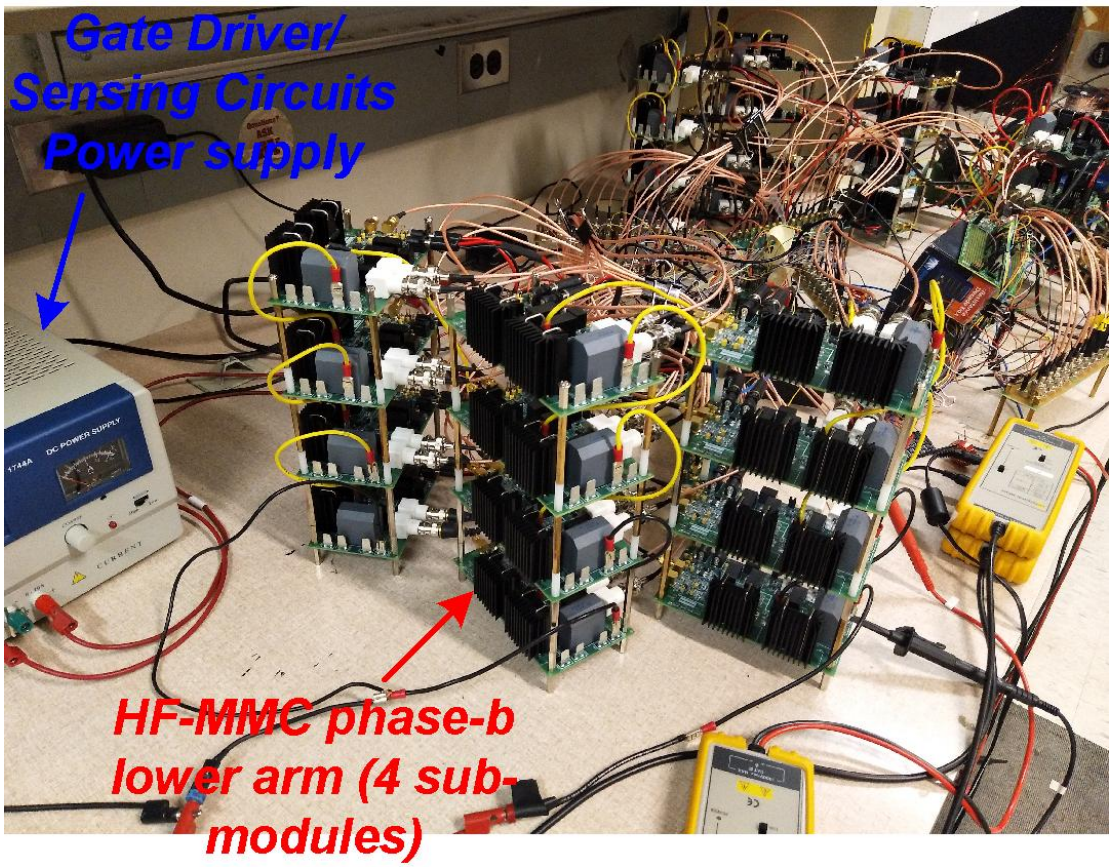


Figure A.4: Lower arms of the MMC from the three phases