Design of a Delta-Sigma Fractional-N PLL Frequency Synthesizer at 1.43GHz

A THESIS

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Abstract

PLL-based frequency synthesis is a common method for developing highly stable oscillators.The need for this type of synthesizer that can operate at non-integer multiples of a reference oscillator is growing. Delta-sigma modulators used to control the division ratio in PLL-based fractional-N frequency synthesizers help to meet the growing need for synthesizers operating at non-integer multiples. A PLL-based fractional-N frequency synthesizer using a delta-sigma modulator to control the division ratio was analyzed at the system level and implemented at transistor level. The system level analysis consisted of understanding the effect of the delta-sigma modulator on spurious tone reduction in the synthesizer output. Circuit blocks were then designed individually at transistor level. Results of the delta-sigma output and the overall synthesizer were then discussed. The synthesizer achieved a start-up speed of 4μsec. The in-band phase noise performance was -82 dBc/Hz at 3 MHzoffset from the carrier.

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Chapter 1: Introduction

The ever increasing rate of data transmission has resulted in a continual need for low-noise clock generation. Growth in the number of applications and useable frequency bands has brought about the need for new techniques in the design of low-noise clocks. This is due to the inherent phase noise of high frequency (HF) (i.e. greater than 1GHz) oscillators. Low phase noise, or period jitter in the time domain, is needed for HF applications due to the growing number of closely spaced frequency bands along with the standards set forth in the field of wireless communications.At the same time, the size constraint for synthesizers is becoming more stringent. With this size constraint brings the push for integrating more components on the same chip. Along those lines, highly stable HF crystal oscillators are not realistic for mass production integrated circuit fabrication.

Fractional-N frequency synthesis (FS) (i.e. the generation of a HF stable oscillator based on the stability of a low frequency reference signal at non-integer multiples) was first implemented in analog systems though was not able to achieve multiple closely spaced steps all on one integrated chip [1]. With the onset of HF closely spaced channels the technique of fractional-n FShas become widely used. The first fractional-n synthesizers concerning the topic of this thesis used an accumulator that periodically changed the input to a multi-modulus divider (MMD). The average division ratio in the phase-locked loop (PLL) would then be a fraction. The fractional-n approach introduces interference aside from phase noise in the form of spurious in-band tones. Spurious tone reduction in fractional-n frequency synthesis has become one of the central topics of synthesizer design. Many techniques have been introduced to solve this with the most common being delta-sigma modulation of the fractional input control. Delta-sigma modulation, used here in an all-digital form, allows for noise shaping of a bit stream around a certain frequency. Originally designed for use in a switched capacitor scheme to address quantization noise in analog to digital converters, the noise shaping property can be manipulated to reduce in-band spurious tones in the output of a fractional

frequency synthesizer. The input to the delta-sigma can be adjusted to provide an average input to the MMD giving an overall division ratio. Delta-sigma control also allows for a wider synthesizer bandwidth compared to accumulator control and thus provides faster locking speeds. Fast locking speeds allow for use in multiple frequency systems and those requiring frequency sweeping. Addressing the concerns of HF low-noise clock generation outlined here along with the need for fast locking speeds, a delta-sigma modulated fractional-n PLL-based frequency synthesizer is designed.

1.1Background on PLL- based Frequency Synthesis

In designing a phase locked loop based frequency synthesizer, an adequate study of background material is required. Provided here is a brief introduction to phase locked loops and how they are used in frequency synthesis. The fractional-n approach will then be discussed along with the delta-sigma control. Most of the mathematical models will be left for Chapter 2. Circuit design issues will be discussed in Chapter Three.

A phase-locked loop (PLL) is a feedback system designed to synchronize an oscillator output (usually a voltage controlled oscillator (VCO)) with a reference signal [2]. There are many applications of PLLs while this writing only covers frequency synthesis. When implemented using a PLL, an FS is designed to match the phase or frequency of a higher frequency signal (i.e. the VCO output) with a low-noise reference signal. In this way, the phase or frequency can be filtered rather than a voltage or a current. The resulting output signal has lower amounts of in-band phase noise as will be discussed further on in this section. A simple PLL is shown in Figure 1.1.1 to illustrate the feedback system inherent in its design.The phase detector output reflects the phase difference between the VCO output and the reference signals. The loop filter provides a smooth transition from the detected phase difference (i.e. the output of the phase detector). The VCO converts the output of the loop filter into a frequency. The system order can be found by using the transfer function of the overall loop.

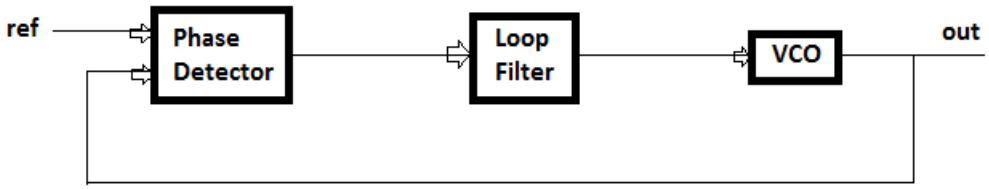


Figure 1.1.1 Simple phase-locked loop

PLL based FS is implemented by placing a divider block in the feedback path of the PLL illustrated in Figure 1.1.2.The divider block allows the synthesis of a frequency higher than the reference frequency. The simplest form being the divide-by-integer or integer-N approach. The output then equals

$$Out = ref \times N$$

This allows a stable low frequency reference signal to be used for the synthesis of a high frequency output.As shown in the above equation, the output frequency divides down to the reference frequency level. The signal after the divider is the output signal at the lower frequency level. This way the output phase can be compared to the reference. Similar to the simple loop, the output of the phase detector is filtered by the loop filter. Also similar to the simple loop in Figure 1.1.1, the output of the loop filter is used to control the VCO, except the center frequency of the VCO is N times the center frequency of the reference signal.

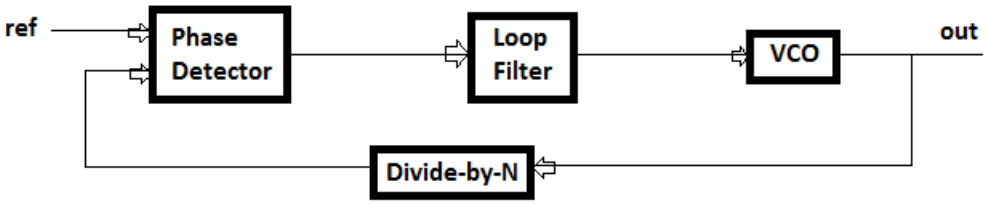


Figure 1.1.2 Integer-N PLL frequency synthesizer

The integer-N technique can be adapted to develop a fractional-N technique. The basis of the fractional-N FS is to have a divider that can be programmed to divide at different values, called a multi-modulus divider (MMD). An example would be a divider that can both divide by 8 and divide by 9. The goal of the fractional-N FS is then to synthesize a frequency at a fractional multiple of the reference frequency

(e.g. reference = 1MHz and the output equals 8.1MHz). The simple approach for controlling the input to the MMD is to toggle it at a periodic rate. Otherwise known as an accumulator, the divider control will stay at one divider rate for a certain number of cycles and then switch to another divider rate for one or more predetermined cycles.

Another method for controlling the divider ratio for fractional-N synthesis is to use a delta-sigma modulator (DSM). The concept of delta-sigma modulation is to reduce the tones that occur near the synthesizer output frequency as a result of the periodic toggling of the divider input. This is accomplished in the DSM using a concept called noise shaping. Noise shaping moves the quantization noise associated with the output of the DSM to a frequency offset from the divider rate outside of the loop bandwidth.With delta-sigma control, the divider control is no longer toggled at a periodic rate while the average division ratio remains constant. Through this process a sort of randomization occurs of the divider control. The noise that is placed outside of the bandwidth is filtered out. This concept is illustrated in Figure 1.1.3.

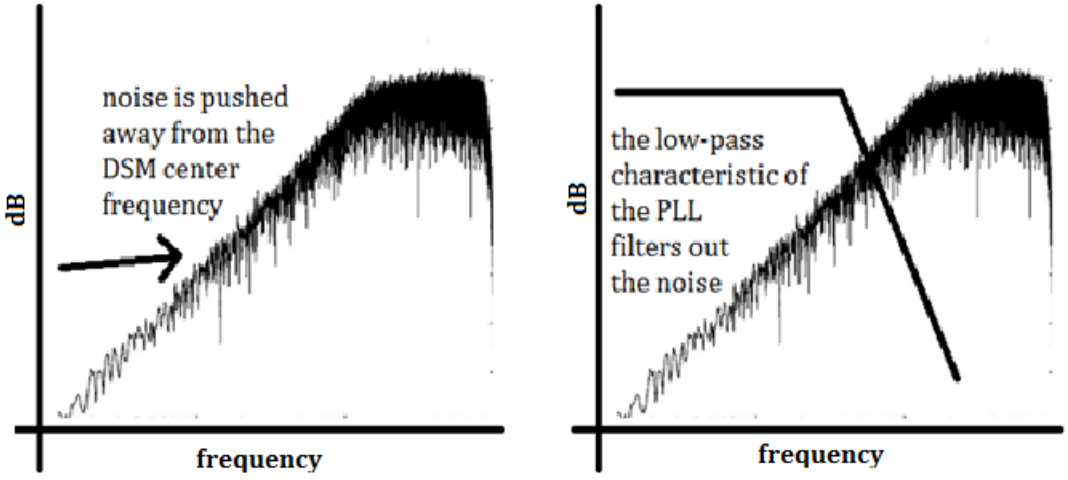


Figure 1.1.3 Noise shaping and filtering

Figure 1.1.4 depicts the synthesizer output spectrum showing the unwanted in-band spurs.These unwanted tones near the carrier frequency are what the DSM works to reduce.

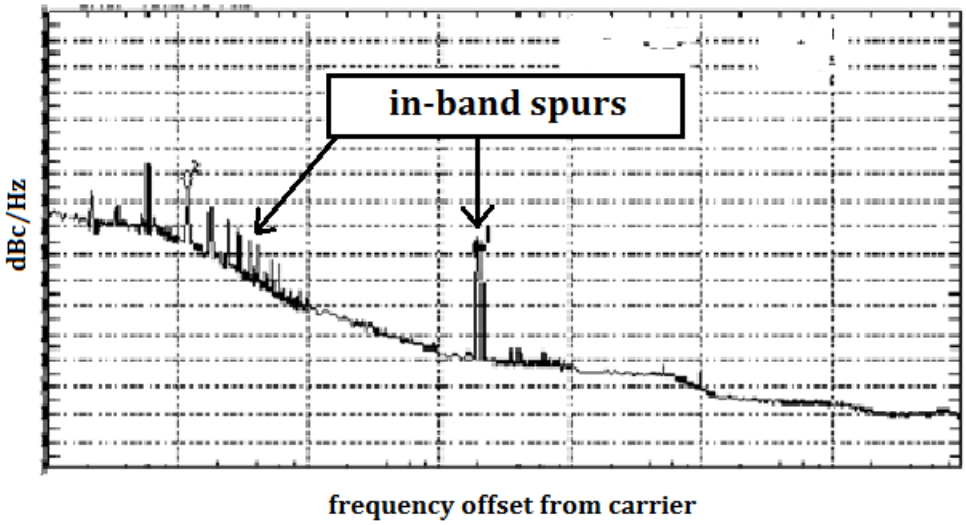


Figure 1.1.4 Unwanted in-band spurs to be reduced

1.2Choice of Architecture

A PLL-based delta-sigma modulator controlled fractional-n frequency synthesizer using an analog VCO and loop filter along with a digital phase detector and MMD was employed with a single-ended output. The type of PLL used in this FS is otherwise referred to as a digital PLL (DPLL) due to the digital nature of the phase detector. Other types of PLLs and methods for frequency synthesis are an all-digital PLL (ADPLL)[3], direct digital frequency synthesis (DDFS)[4], delay-locked loop (DLL) and direct analog FS among others. Reasons for choosing the DPLL and the overall features are now discussed. A VCO was selected for its ability to operate at high frequencies (i.e. above 1 GHz) with relative ease. The input voltage can be filtered to achieve a high level of stability. The loop filter uses a tri-state mode voltage output to efficiently transfer the phase detector output to the VCO. A phase frequency detector was used in place of the phase detector to allow both forward and reverse adjustments of phase. This allows the system to become more robust with its ability to lock the phases of the input and output signals with a start phase position of either the input leading or the output leading.

Other design choices include the delta-sigma modulator used for the divider control, the type of VCO, the specific loop filter, the type of digital components and

reason for using the CMOS technology. A feed-forward 3rd-order all-digital delta-sigma modulator with a single-bit quantizer was chosen. This DSM uses only a single-stage topology and yet achieves adequate noise shaping of the quantizer error. The single-bit output of the DSM is selected for simplicity and to easily coordinate with the MMD. The MMD uses a simple state machine approach and is the cascade of multi lower-division stages, namely divide by 2-and-3 stages. The MMD has three digital inputs set so that when the output of the DSM is "low" it divides by 14 and when the output of the DSM is "high" it divides by 15. The signal to be divided is the output of the VCO, which is made of a cross-coupled RLC tank. The RLC tank allows for the high frequency in excess of 1 GHz and the cross-coupled approach amplifies and provides the negative feedback necessary for oscillation. A widely used technique for controlling the VCO is the charge pump [5]. The charge pump would require a specific type of loop filter whose input is current as opposed to voltage. Here, for simplicity, the VCO is driven by the loop filter which was made of four cascaded first-order stages with single-ended operational amplifiers after each stage. The operational-amplifier design is shown in this thesis and is placed in the loop filter to buffer each stage. Finally, the integrated circuits designed herein use the CMOS IBM 0.13μm technology. CMOS technology was chosen for its ease of use and the growing availability in modern fabrication of integrated circuits. The IBM 0.13μm technology allows for accurate simulations using Cadence© software and is still being used for high production integrated circuits.

1.3 Literature Review

A brief review will be performed on the field of delta-sigma frequency synthesis[6, 7] to show that delta-sigma frequency synthesis is a relevant subject for a thesis concerning integrated circuits.

Study #1: Delta-sigma modulation in fractional-n frequency synthesis[6]

A fundamental read when studying delta-sigma frequency synthesis, this paper introduces the concept of using delta-sigma noise shaping in fractional-n frequency

synthesizers. The main claim is that second-order or higher DSM control of the division ratio in a fractional-n FS will allow the concepts of noise shaping in over-sampling data converters to reduce noise in the output spectrum. First-order DSM is not sufficient in randomizing the quantization error due to the zero being removed when integration is applied to convert frequency to phase. Each additional integrator stage introduces a zero at the originand thus provides noise shaping. A model for the phase noise at the output of the MMD is developed in the mathematical portion of this paper followed by an evaluation of the effects of quantization noise on the overall output of the FS.

A second-order example of a delta-sigma modulator is next introduced. A block diagram showing an implementation of the modulator is given in Figure 1.3.1 adapted from Fig. 6 of [6]. The location of the noise shaping ability is in the integrators (accumulators in this digital implementation). In this example, they are

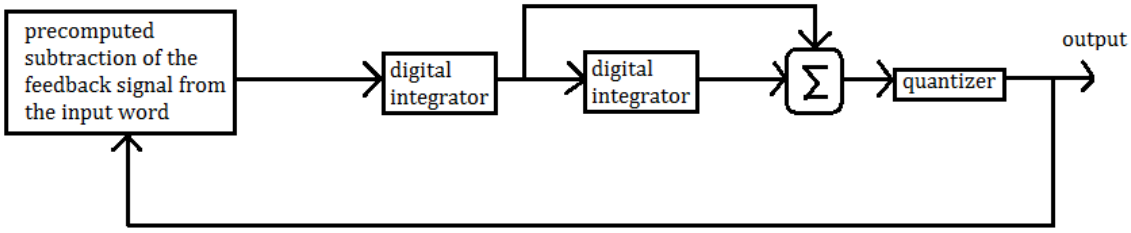


Figure 1.3.1 Block diagram of a second-order all-digital delta-sigma modulator

constructed using 13-bit adders and registers. The final summing point uses fourteen bits and the quantizer is a 1-bit and can be implemented by taking the most significant bit of the final summing point. The feedback line is also one bit and is made into a multi-bit line consisting of all ones or all negative ones while the number of bits fed back is chosen based on system constraints.A rough sketch of the DSMoutput is shown in Figure 1.3.2, adapted from Fig. 8 of [6],which shows notching around the center frequency indicating that noise shaping is occurring.

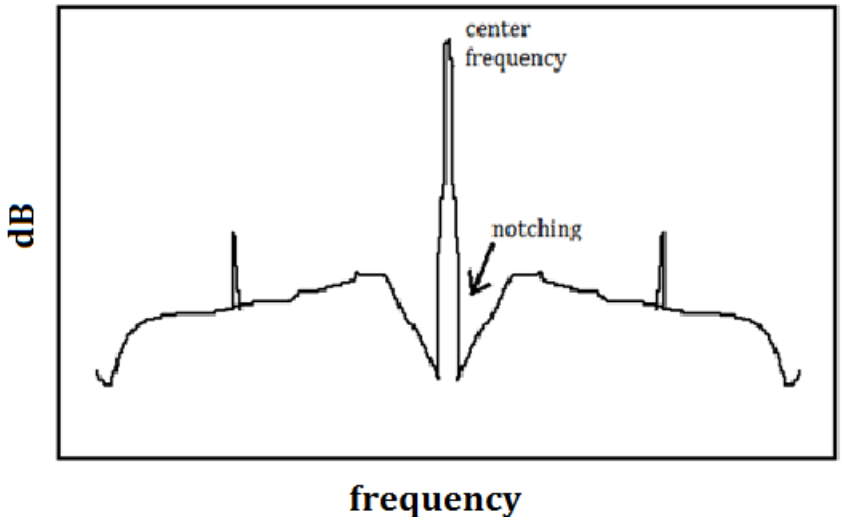


Figure 1.3.2 Spectrum of the second-order delta-sigma modulator

A third-order DSM was also constructed in this study using a structure similar to Figure 1.3.1 except with an added integrator and gain blocks to position poles. This was simulated in a fractional-n synthesizer and was found to reduce some of the noise introduced by the fractional-n technique.

Study #2: A 1.1 GHz CMOS fractional-n frequency synthesizer with a 3bit 3rd order delta sigma modulator[7]

This paper is one of the early publications in integrated circuit design of delta-sigma frequency synthesis. Bandwidth requirements of PLL-based frequency synthesizers along with constraints put in place by the delta-sigma approach are considered covering their relation to phase noise. A delta-sigma noise transfer function is discussed to obtain tradeoffs for different topologies and orders of modulators. A brief IC design of a synthesizer is shown in the study which they use for a comparison of different delta-sigma modulator topologies. Finally, experimental results for multiple types of delta-sigma modulators were compared on the fabricated chip. The results show that the proposed multi-bit quantizer approach to a non-MASH type modulator provides a better spurious tone reduction.

In the forthcoming equations an attempt is made to show the intent of this paper's author in deriving the bandwidth of a frequency synthesizer that has a

certain integrated phase error (θ_{rms}) requirement.If one assumes that the majority of the in-band phase noise of the synthesizer is limited within a certain frequency bandwidth f_c, the integrated frequency noise Δf_n is approximately

$$\Delta f_n \cong \sqrt{\tfrac{2}{3}A_n} \cdot {f_c}^{3/2}.$$

With A_n being from the phase noise equation $10 \log A_n$ measured in dBc/Hz.For various reasons, the dynamic range of the Lth-order delta sigma modulator should be constrained by

$$\frac{3}{2} \cdot \frac{2L+1}{\pi^{2L}} \cdot (OSR_{eff})^{2L+1} > (\frac{f_{PD}}{\Delta f_n})^2$$

where OSR_{eff} is the oversampling ratio of the delta-sigma and is dictated by

$$OSR_{eff} = \frac{f_{PD}}{2f_c}$$

while f_{PD} is the frequency of the phase detector. From the previous equations f_c should be constrained by

$$f_c < [A_n \cdot \frac{L+0.5}{(2\pi)^{2L}}]^{(\frac{1}{2L}-2)} \cdot {f_{PD}}^{(2L-\frac{1}{2L}-2)}.$$

Integrated phase error is given by

$$A_n = (\frac{\theta_{rms}}{\sqrt{2}})^2 \cdot {f_c}^{-1}.$$

An upper bound on the bandwidth of the system can be obtained from the previous equations

$$f_c < [\left(\frac{\theta_{rms}}{\sqrt{2}}\right)^2 \cdot \frac{L+0.5}{(2\pi)^{2L}}]^{\left(\frac{1}{2L}-1\right)} \cdot f_{PD}.$$

With a modulator order and target θ_{rms} chosen, the above equations can be used to find an upper bound for the band width of the synthesizer.

Using higher-order modulators, as the number of quantizer levels increase (i.e. having a multi-bit output from the DSM rather than 1-bit) the out of band noise increases as well. In this thesis, a 1-bit quantizer was used for simplicity although adding bits to the output is possible since a third-order modulator is used. The corner frequency can also increase, according to this paper, with the rising number of quantizer bits. For 2-bit, 3-bit and 4-bit quantizers, the corresponding corner frequencies become $0.13f_s$, $0.19f_s$ and $0.24f_s$, respectively, where f_s is the frequency of operation. The topology used is shown in Figure 1.3.3, adaptedfrom Fig. 3 of the

study, which is similar to that used in this thesis although only a 1-bit quantizer is used and the gain blocks are different. Comparisons are then made to a MASH

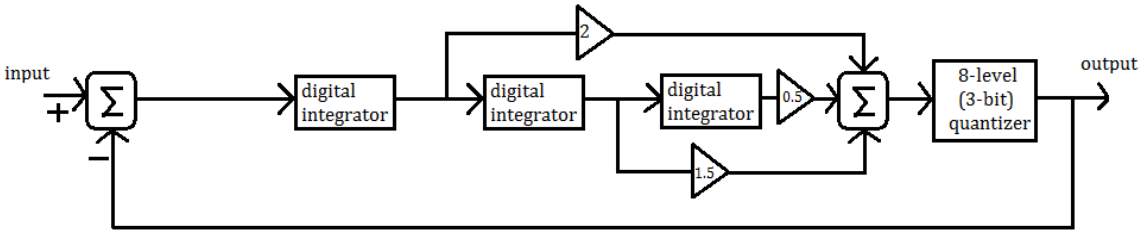


Figure 1.3.3 Third-order $\Delta\sum$ modulator with 3-bit quantizer

(multi-stage noise shaping) modulator which is another popular DSM topology. The MASH is shown to provide better shaping but has the negative effect of being more sensitive to noise coupling from the substrate. A simulated output spectrum is shown in Figure 1.3.4, adapted from Fig. 7 of the study and is as predicted.

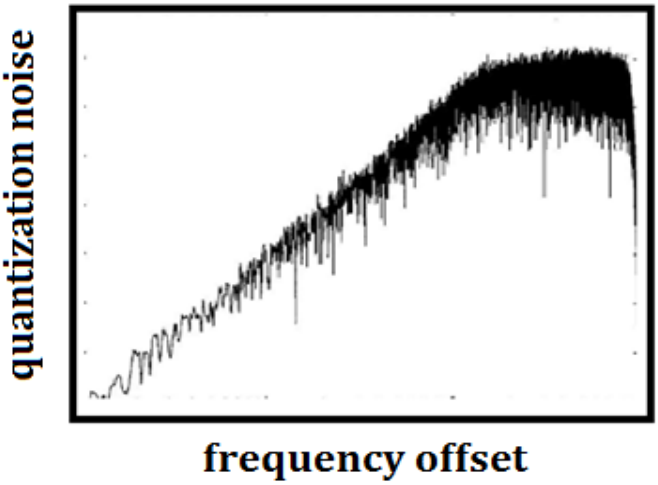


Figure 1.3.4 FFT of the Noise Transfer Function of a 3-bit third-order modulator

1.4 Design Goals and Justification

Frequency synthesizer design requires a specific set of goals along with justification prior to embarking on construction. The main reason is that frequency synthesizers can be used for a wide range of applications with each requiring a different set of specifications. With design goals in hand, the architecture and individual components can be chosen. Table 1.4.1 shows the core set of design goals for the FS detailed in this writing. The general specifications in Table 1.4.1 are

considered appropriate for a FS used in wireless communication. These specifications allow for the FS designed here to be adapted towards a direct modulation scheme such as in [8]. The phase noise target value chosen here is of moderate quality and will be sufficient for building and testing a DSM control. The following specifications were adapted from Table 1.3 of [9]. The in-band spur reduction of >15dB was chosen to be on the order of some of the current studies. The third-order delta-sigma modulator (DSM) should be able to reduce the spurs by at least 15dB. The system bandwidth of 1 MHz was selected to allow fast locking speed on the order of 1μsec. With a locking speed around 1μsec, the system would be able to handle direct modulation around 1Mbits/sec.

Design Goal	**Value**
Reduced phase noise	< -115 dBc/Hz@ 3 MHz offset
Reduced in-band spurs	>15dB reduction
Exact center frequency	1.43 GHz
Wide bandwidth	1Mhz

Table 1.4.1 Frequency Synthesizer Design Goals

Chapter 2: System Level Analysis

A system level understanding for the design of a delta-sigma fractional-n frequency synthesizer will be presented. Overall methods will be discussed to provide a basis for the design. The design will be covered in steps of increasing complexity beginning with an integer-n synthesizer. The fractional-n approach follows which leads to the technique of delta-sigma control of the fractional-n synthesizer. Finally, the entire system will be presented.

PLLs can be complicated structures consisting of trade-offs and complications between bandwidth, locking speed, system order, tuning range, output phase noise and stability. The best way to understand performance trade-offs is to use mathematical models as will be presented here. Implementing the system level design using a state-space approach is one possibility. This approach would require the entire synthesizer be viewed as a linear system [10]. In order to implement the state-space technique, much additional knowledge would need to be gathered and through which the depth of the models move beyond the goals of this thesis. Using a simple mathematical model, though, allows for the system to be viewed as a control system, thus classical control parameters can be discussed. Many books and studies on PLL synthesizers provide in-depth discussions on the mathematical models of such a system [2, 11-13]. Provided here is a brief overview of some major considerations. Due to limited access of modeling software for the topic of this thesis, system level simulations were not performed. Extensive models exist, however, such as the models demonstrated by [14] which use the Simulink and Matlab© programs to account for non-idealities. Cadence© software provides an adequate amount of system type simulations for the purpose of this thesis. Circuit blocks constructed in Cadence© consisting of transistor level implementations provide a model of how the circuit will behave due to the use of IBM© technology models.

2.1 PLL-based integer-n Frequency Synthesis

Variables in a PLL can be represented as phase or frequency when considering the mathematical model. Phase variables were chosen here for simplicity in that it can be easier to comprehend the reduction of a phase error as opposed to a frequency error regarding PLLs. The mathematical model using frequency variablesis similar to the phase version except the integral term is moved in the block diagram.This is due to the relationship between frequency (ω) and phase(φ)

$$\varphi = \int \omega \, dt.$$

Figure 2.1.1 shows the block diagram of a simple PLL in control system terms adapted from [11]. The summing point and K_p represent the phase detector,φ_{ref} is the reference frequency, the $K_{LF}F(s)$ block is the loop filter and gain, K_v is the VCO gain and$\frac{1}{s}$ (integrator) converts the VCO output frequency to phase. The integrator block is added to the mathematical model to allow phase to be a variable as described earlier. This block is not directly included in the circuit implementation but adds to the order of the system. The system equation is solved as

$$\varphi_{out} = \varphi_e K_p K_{LF} F(s) K_v \frac{1}{s}$$

$$\varphi_e = \varphi_{ref} - \frac{\varphi_{out}}{N}$$

where N is the integer that φ_{ref} is multiplied by to synthesize φ_{out}. Then it can be shown that

$$\varphi_{out}\left(1 + \frac{K_p K_{LF} F(s) K_v}{Ns}\right) = \varphi_{ref} K_p K_{LF} F(s) K_v \frac{1}{s}$$

$$\varphi_{out} = \frac{\varphi_{ref} N K_p K_{LF} F(s) K_v}{Ns + K_p K_{LF} F(s) K_v}$$

where the overall gain is defined as

$$K = K_p K_{LF} K_v$$

and

$$\frac{\varphi_{out}}{\varphi_{ref}} = \frac{NKF(s)}{Ns + KF(s)}$$

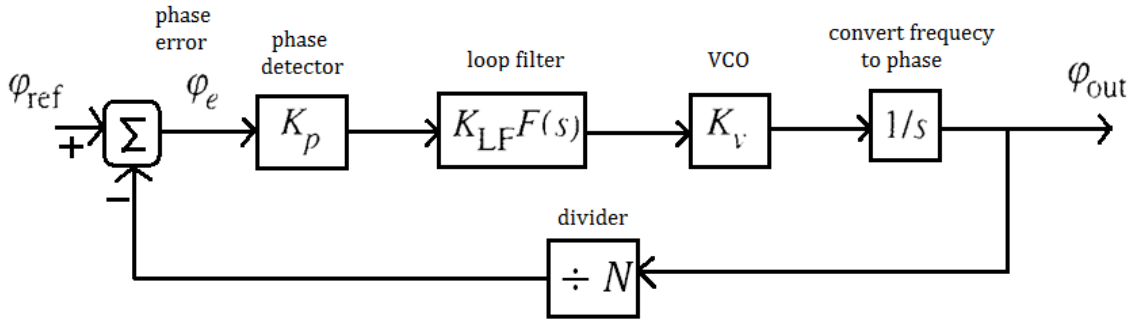


Figure 2.1.1 PLL-based FS block diagram

This equation will vary if the output phase is taken after the divider [12]. The portion of the circuit that dictates the system order is the loop filter (LF). Using a simple low pass fourth-order filter as shown in Figure 2.1.2, $F(s)$ becomes

$$F(s) = \frac{1}{(s-\frac{1}{RC})^4}.$$

The overall system then becomes a fifth-order PLL.Choosing appropriate R and C values will give the bandwidth of choice for an ideal operational amplifier.

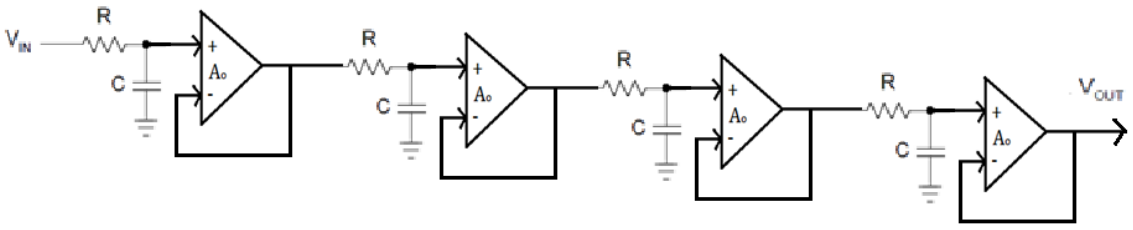


Figure 2.1.2 Simple fourth-order low-pass filter

2.2 PLL-based Fractional-n Frequency Synthesis

In classic fractional-n synthesis the N divisor is toggled in a periodic fashion. The goal is to obtain an overall average divisor value that is a fraction rather than an integer. An example of this method is if the desired average divisor value is 8.1 and the two available integer divisor values in the MMD are 8 and 9 then an accumulator would be programmed to output the control signal to divide by 8 for nine cycles and 9 for one cycle giving

$$\frac{(8 \times 9) + (9 \times 1)}{10} = 8.1 .$$

The output of the frequency synthesizer then becomes 8.1 times the reference frequency. The negative effect is the added phase noise introduced in the form of unwanted spurious tones at various offsets from the fundamental. A visual in-band spurs is shown in Figure1.2.4.These spurs become part of the output since the loop bandwidth is often at a distance greater than the spur offset. In order to minimize the spurs with the accumulator approach, the loop bandwidth has to be small, this is why locking speeds tend to be slow.

2.3 Delta-Sigma control of fractional-n frequency synthesis

Delta-sigma control of the division ratio is a special case of fractional-N frequency synthesis. The use of delta-sigma noise shaping provides a method to reduce the spurs introduced in fractional-n synthesis. The delta-sigma will produce frequency content placed at a distance from the reference frequency (i.e. the operating frequency of the PFD). This is desirable in that, ideally, an average division ratio can be achieved without introducing an exact tone. Avoiding the production of a certain tone in the control of the division ratio will remove or at least reduce the spurious tones in the output. The “noise” or otherwise thought of as higher energy frequency content of the quantization error is moved to higher frequencies which can then be filtered out by the loop filter. The concept of moving the noise to higher frequencies i.e. noise-shaping is illustrated in Figure 2.3.1. This concept, as stated earlier, was first used to shape noise in data converters to allow higher resolution withoutextremely precise(and expensive) analog circuitry

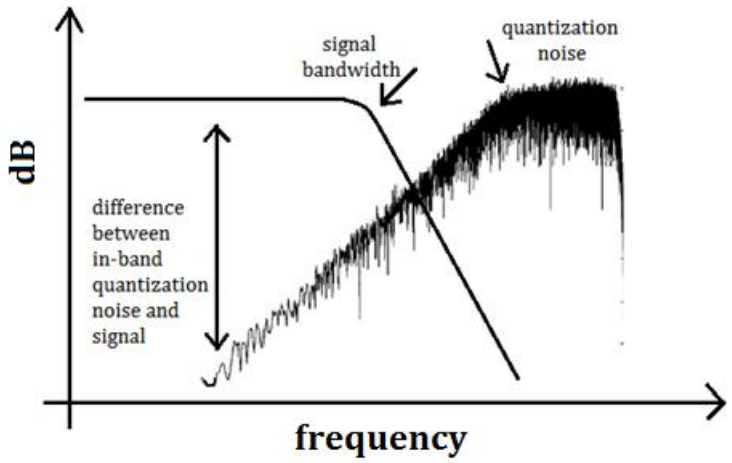


Figure 2.3.1 Noise Shaping Illustration in Data Converters

[15, 16]. The difference between the signal bandwidth and the in-band noise, in terms of data converters, dictates the resolution available for the particular converter. Generally speaking, the order of modulator decides the shape of the noise plot. The higher the order, the lower the in-band noise level and the higher the out-of-band noise level becomes. This concept is illustrated in Figure 2.3.2.

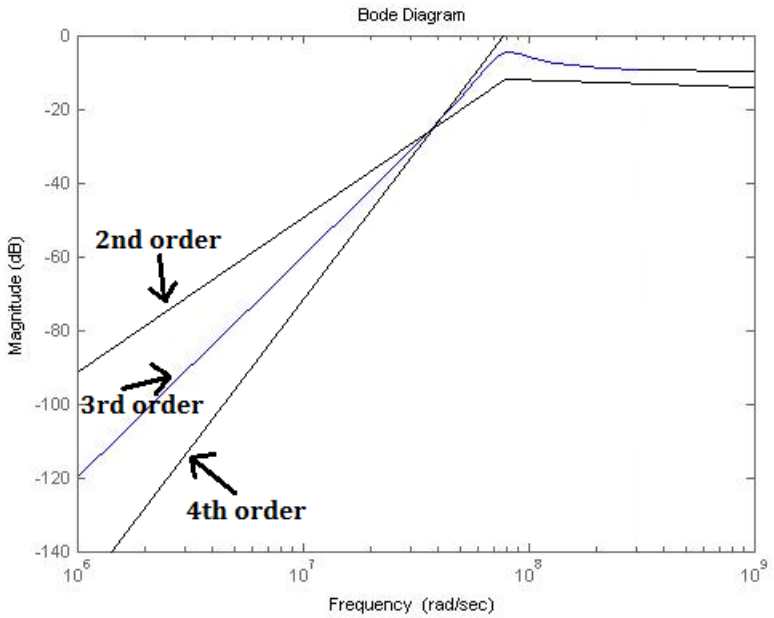


Figure 2.3.2 Noise shaping based on modulator order

The type of DSM used here is an all-digital version constructed of purely digital components. This version allows for both a digital input and a digital output providing the ability to set the average of the output.Different types of modulator topologies can be used to achieve specific noise-shaping characteristics [12]. Modulator topologies can be developed from scratch and are still being developed by many researchers. The modulator used here, shown in Figure 2.3.3 at block level, was chosen for its simplicity and was adapted from[12]. This is a third-order feed-forward modulator with a delay element in the feedback path. Solving for the transfer function gives

$$H(s) = \frac{output}{input} = \frac{(1-z^{-1})^3+(1-z^{-1})^2+(1-z^{-1})+1}{2(1-z^{-1})^3+(1-z^{-1})^2+(1-z^{-1})+1}.$$

The noise transfer function, on the other hand, is the transfer of the quantization noise to the output. The quantizer is implemented by taking the most significant bit of the last addition. The removal of the remainder of the output byte is modeled by adding a noise term. In this model it is assumed that the quantization noise is random i.e. spread over the spectrum evenly and considered as white noise. Although quantization (i.e. taking only the most significant bit at the output in this case) is a non-linear effect in the time domain, it can be treated as a random process in the frequency domain thus allowing the use of linear noise model[17]. The noise transfer function is then

$$H_{noise}(s) = \frac{output}{quantizer\ \ noise} = \frac{(1-z^{-1})^3}{2(1-z^{-1})^3+(1-z^{-1})^2+(1-z^{-1})+1}.$$

This transfer function provides the high pass characteristic capable of moving the noise away from the operating frequency of the DSM.

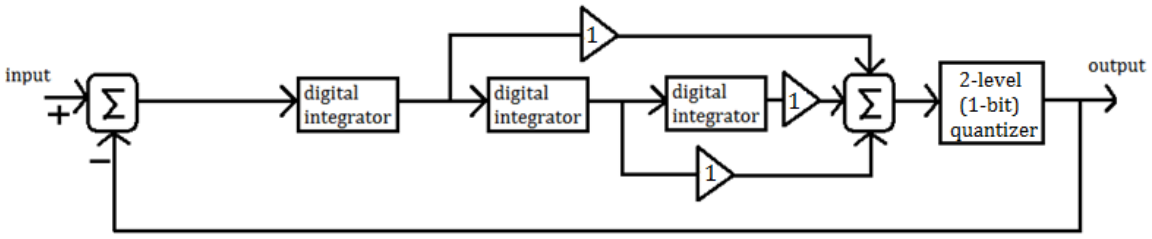


Figure 2.3.3 Modulator Block Level

2.4 PLL-based Delta-Sigma Modulator ControlledFractional-n Frequency Synthesis

The effect of moving the quantization noise away from the operating frequency of the DSM is that spurious tones at the output of the synthesizer and inside the bandwidth of the loop filter are reduced. A 15dB reduction of in-band noise can be achievedwith this topology. For further analysis of noise, the reader is referred to [18], [19]. An illustration of the effect noise shaping has on the system is shown in Figure 2.4.1. The noise shaping at the output of the DSM allows for a wider bandwidth of the loop filter. The loop filter must have an order greater than or equal to the order of the DSM to adequately attenuate the out of band noise [7].

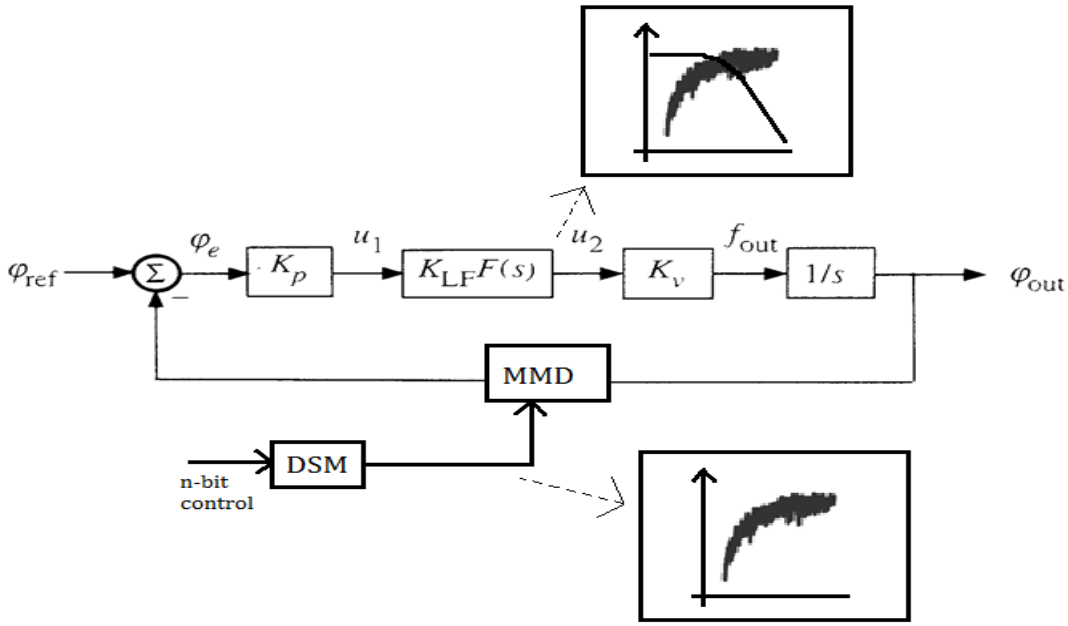


Figure 2.4.1 Illustration of noise shaping throughout the FS.

Chapter 3: Circuit Design

Design techniques and considerations for each circuit block will be addressed in this chapter. The chapter will start with general topics in the use of CMOS integrated circuits, particularly geared toward the IBM 0.13μm technology. Circuit design of the voltage controlled oscillator (VCO) consisting of a RLC tank topology will be covered next. The main design tasks will be the single ended output circuitry, impedance matching and the circuit quality factor (circuit Q). A digital implementation of the phase frequency detector (PFD) will be discussed addressing speed considerations. Following the output of the PFD is the active loop filter. Justification for the loop filter order will be presented along with the implementation of the single-ended operational amplifier at the core of the filter. The design of the multi modulus divider will cover speed considerations and its state machine style of implementation. The section on delta-sigma modulator circuitry will cover adder and register design along with speed considerations. Finally, the circuit implementation of the system as a whole will be discussed.

3.1 Overall Circuit Design Considerations

A general overview of integrated circuit design along with fundamental building blocks will be given. The technology used is the CMOS IBM 0.13μm and was chosen considering its use in modern fabricated circuits. An analog view of a transistor (nmos in this case) is shown in Figure 3.1.1 with biasing voltages. The following notes apply in general to pmos devices as well. In order for the transistor to operate properly (i.e. region 1, 2 or 3) in a particular circuit, it has to be biased properly. At the core of its operation is the threshold voltage. This voltage is set by a number of properties of the transistor including the length, width, type of substrate and voltage source level. For the NMOS to turn on

$$V_{gate} - V_{source} > V_{th}.$$

The difference between the left and right side of the above equation

$$\left(V_{gate} - V_{source}\right) - V_{th} = V_{gs} - V_{th}$$

is called the overdrive voltage or simply overdrive. The value of the overdrive is important since it largely influences both the peak current I_d and the voltage swing of the transistor where I_d at its peak is defined as

$$I_d = \frac{1}{2}\mu_n c_{ox} \frac{w}{l}\left(V_{gs} - V_{th}\right)^2.$$

μ_n is defined as the electron mobility in an n-channel device and c_{ox} is defined as the capacitance of the gate oxide per unit area. $I_d$is the current through the device and affects many design choices including power consumption and speed. The speed of the device is another important design choice which relies mainly on the channel length and the width of the device along with the power supply voltage.

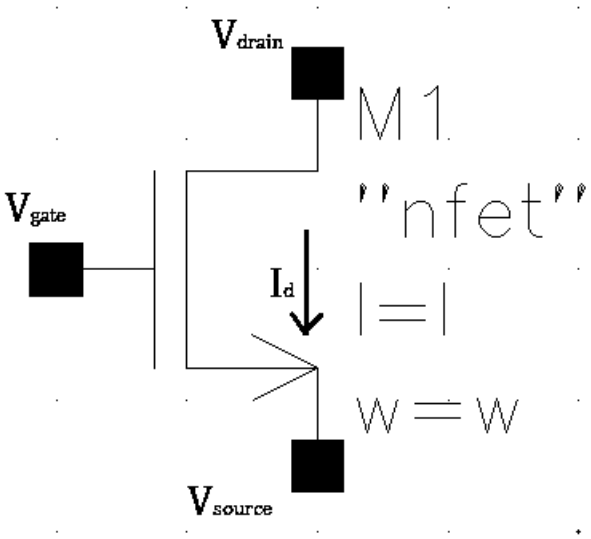


Figure 3.1.1 NMOS transistor.

A brief discussion on the building blocks of the digital circuits used begins with an inverter[20]. The sizing is the only design choice available in this case while the voltage supply was already chosen based on the needs of the analog portions of the overall design. The sizing alone, in this case, dictates the crossover voltage where the hysteresis region is minimized. The technique forbuilding the logic gates is shown using the NAND gate structure inFigure 3.1.2. This structure is adapted to construct the AND, OR and XOR gates where varying numbers of inputs can be added as needed.

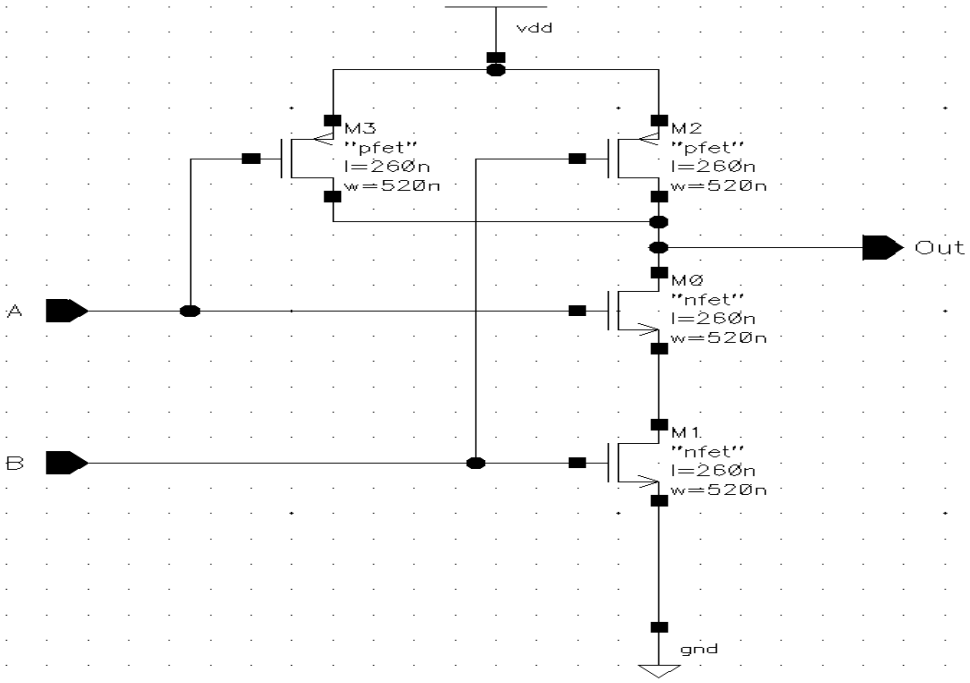
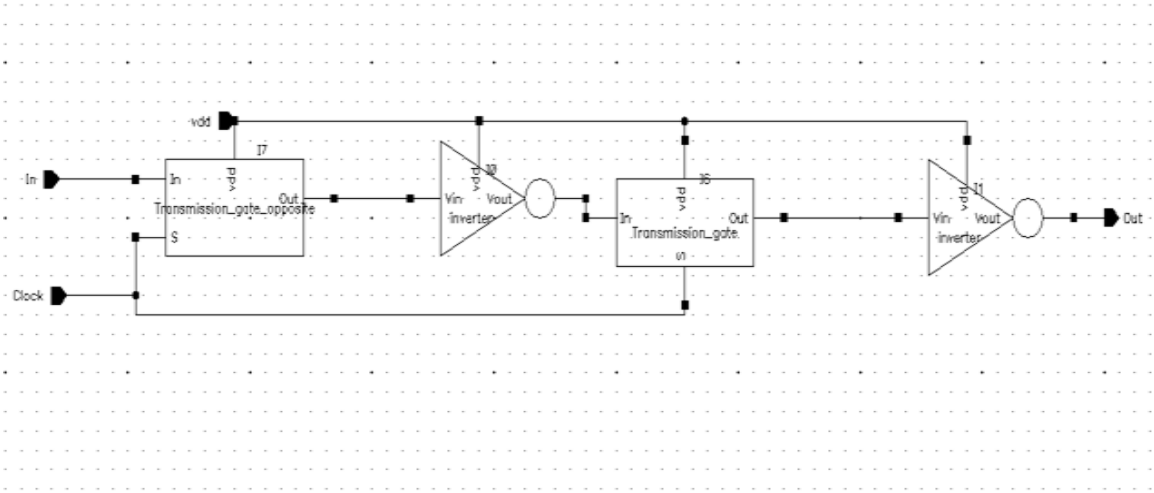
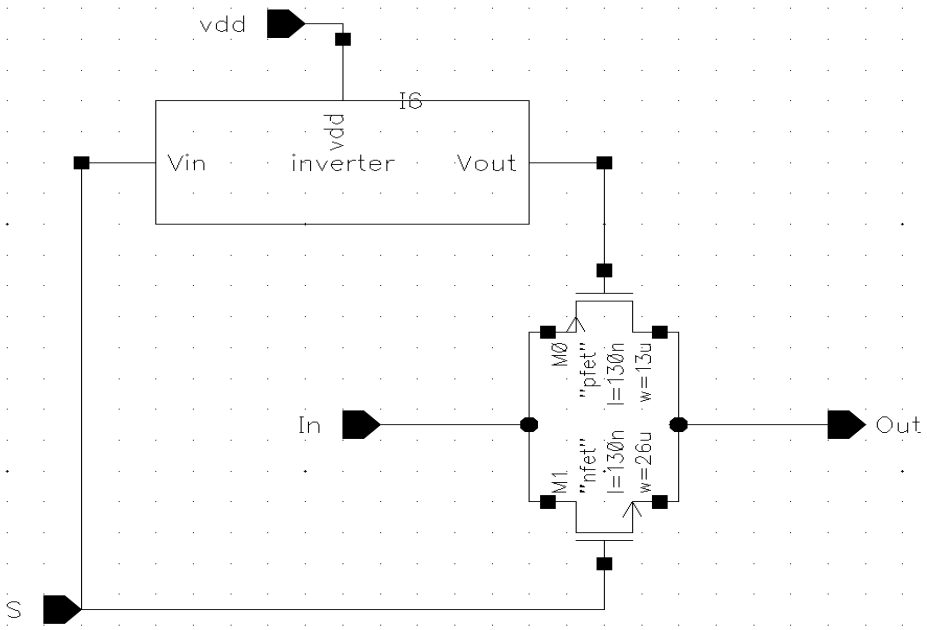


Figure 3.1.2 NAND gate

Flip-flops were required for clocked circuitry; Figure 3.1.3 shows the dynamic version of the D-type flip-flop that was built. The dynamic version was needed to prevent level sensitive inputs for the registers in the DSM. Also shown in Figure 3.1.3 is the transmission gate employed in the D-type flip-flop. These are used to control the timing of data throughout the device.



(a)



(b)

Figure 3.1.3 Clocked circuits (a) D-type flip-flop (b) transmission gate.

3.2 Circuit Design of the Voltage Controlled Oscillator

An in depth study of voltage controlled oscillators (VCO)s is beyond the scope of this thesis. An intermediate level of background is necessary, however, in RLC tank circuits for an understanding of this material. For an in-depth study of VCOs and RFIC topics the reader is referred to [21]and [22].

The oscillator used here is an RLC crossed-coupled VCO, shown in Figure 3.2.1. The RLC topology was chosen due to the high frequency requirements of the synthesizer. Resonator circuits are better for high frequency oscillators compared to other topologies such as the ring oscillator [21, 23]. Further, the RLC allows for a devoted frequency control rather than a frequency control that concurrently adjusts the output amplitude. This so called devoted frequency control consists of replacing the capacitors on the tank portion of the oscillator with varactor diodes, implemented here using diodes with the cathodes connected to separate nodes. The voltage control is placed on the anode side of the diodes and combined into one node. Varying the voltage adjusts the capacitance of the diode to AC ground in turn adjusting the resonant frequency of the tank and thus the output frequency. The

tuning range of the VCO is linear to a degree as shown in Figure 3.2.2. The maximum frequency in the voltage range that was swept is 1.61 GHz and the minimum is 1.34 GHz which is sufficient for this synthesizer. One inductor between the two output nodes, instead of one each to AC ground, results in a smaller size, which makes it easier to integrate.

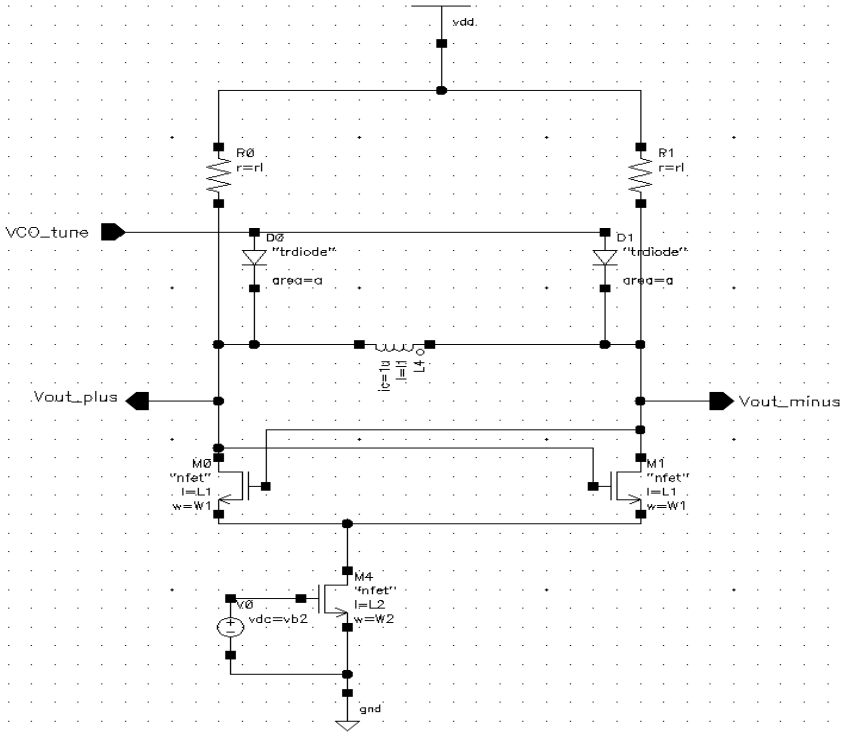


Figure 3.2.1 Crossed-coupled RLC VCO.

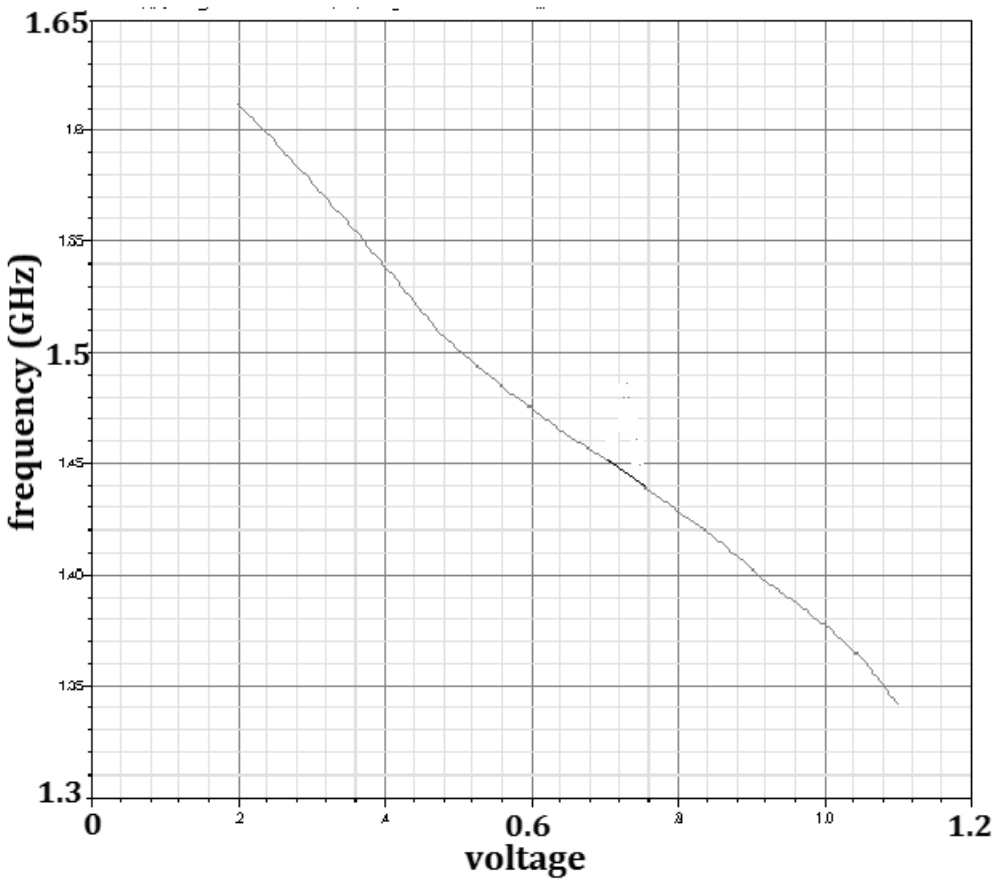


Figure 3.2.2 VCO tuning curve

The VCO had a differential output as shown in Figure 3.2.1. The frequency synthesizer in this thesis, however, requires a single-ended design. To accomplish this, a simple differential to single-ended converter with reduced output impedance was constructed as shown in Figure 3.2.3**.** The decreased output impedance allows for the VCO output power to more effectivelytransfer to the next stage, preventing the amplitude from decreasing. This topology can increase the overall system phase noise but is sufficient for this frequency synthesizer.

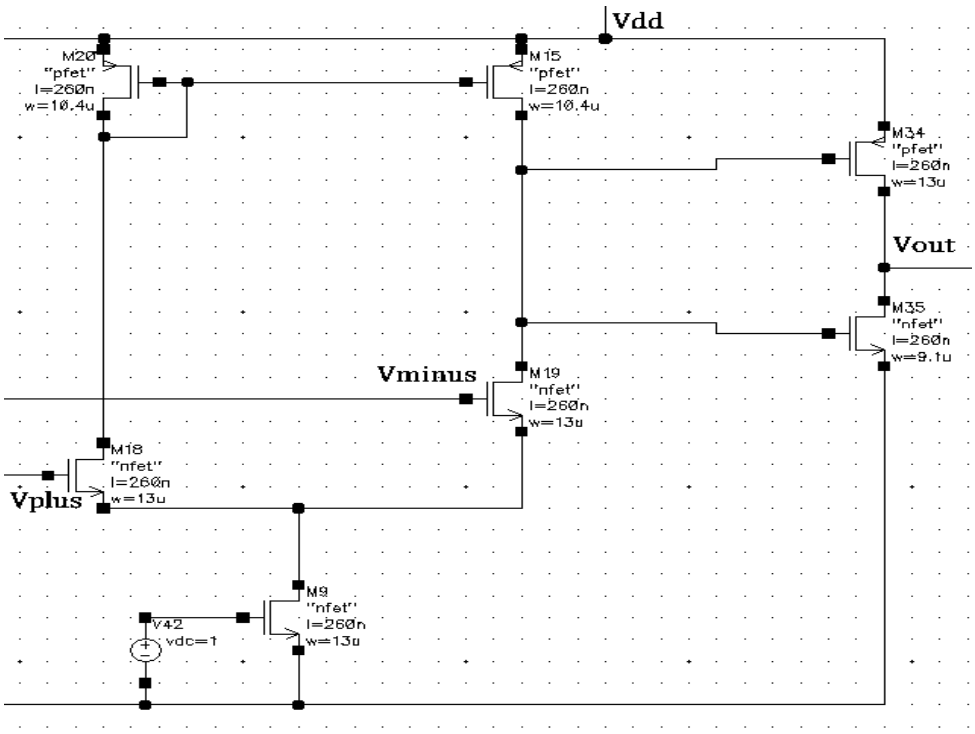


Figure 3.2.3 VCO single-ended output circuitry.

One of the drawbacks of this overall VCO topology is the low circuit quality factor (circuit Q or Q). The quality factor is a measurement used in systems that undergo sinusoidal excitation. It is a measure of the energy stored per average power dissipated whereas a higher Q value is desirable [22]. The poor circuit Q in the VCO used here is due to the series combination of the resistors with the inductor, adding to the parasitic resistance of the inductor [21].

3.3 Circuit Design of the Phase Frequency Detector

At the core of the frequency synthesizer is the measurement of the phase difference between the divider output (f_{div}) and the reference oscillator (f_{ref}). In order to measure how far out of phase f_{div} is from f_{ref},a phase detector (PD) can be employed. The PD is a digital circuit with its simplest form being a single XOR logic gate. If f_{div} begins to lag f_{ref}, shown in Figure 3.3.1, the output of the PD will be high with increasing widths. This signal runs the loop filter which in turn signals the VCO to increase the frequency.

Figure 3.3.1 Sample Output of XOR PD: vertical axis is 500mV/div for Out and 250mV/div for Ref and Div, horizontal axis is 2nsecs/div.

The simplicity and noise rejection of the XOR PD [24] make it a suitable candidate for IC PLLs. With the advent of multi-frequency PLL-based frequency synthesizers a more robust technique for phase comparison is required. This requirement makes the XOR PD less suitable given that one of the main restrictions is to have the center frequency in an exact location in order to allow the system to lock [24]. This restriction is not feasible for multi-frequency systems in that pre-tuning of the VCO and divider is not a trivial task. A solution is the more desirable phase frequency detector (PFD), implemented in this thesis. The PFD is able to detect the phase difference between f_{div} and f_{ref} along with showing which signal is leading. This technique allows the system to correct both for f_{div} is slower than $f_{\text{ref}} and f_{\text{ref}}$ being slower than f_{div}. A typical PFD is shown in Figure 3.3.2 consisting of two D-flip-flops and one AND gate. An "UP" signal indicates that f_{ref} is faster than f_{div} while a "DOWN" signal indicates the opposite.

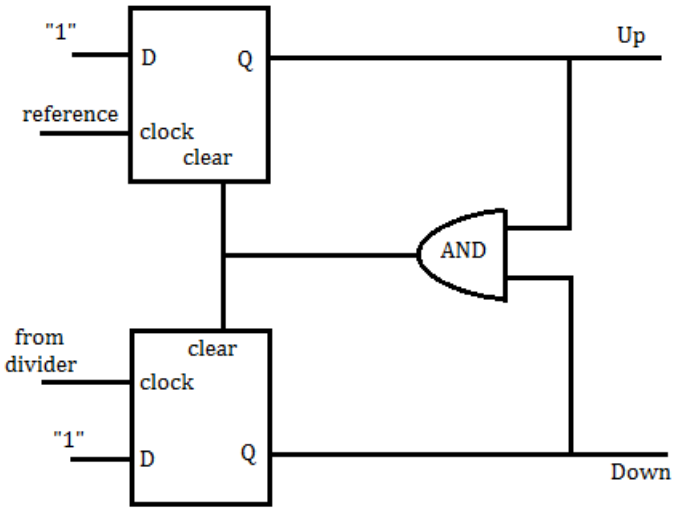


Figure 3.3.2 Typical PFD

To implement the PFD technique, the circuit shown in Figure 3.3.3 was constructed and uses only NAND gates and inverters. The topology was adapted from[24], although a custom digital design of each logic gate was completed for this thesis. A sample output is given in Figure 3.3.3 as well to show the operation of this PFD.

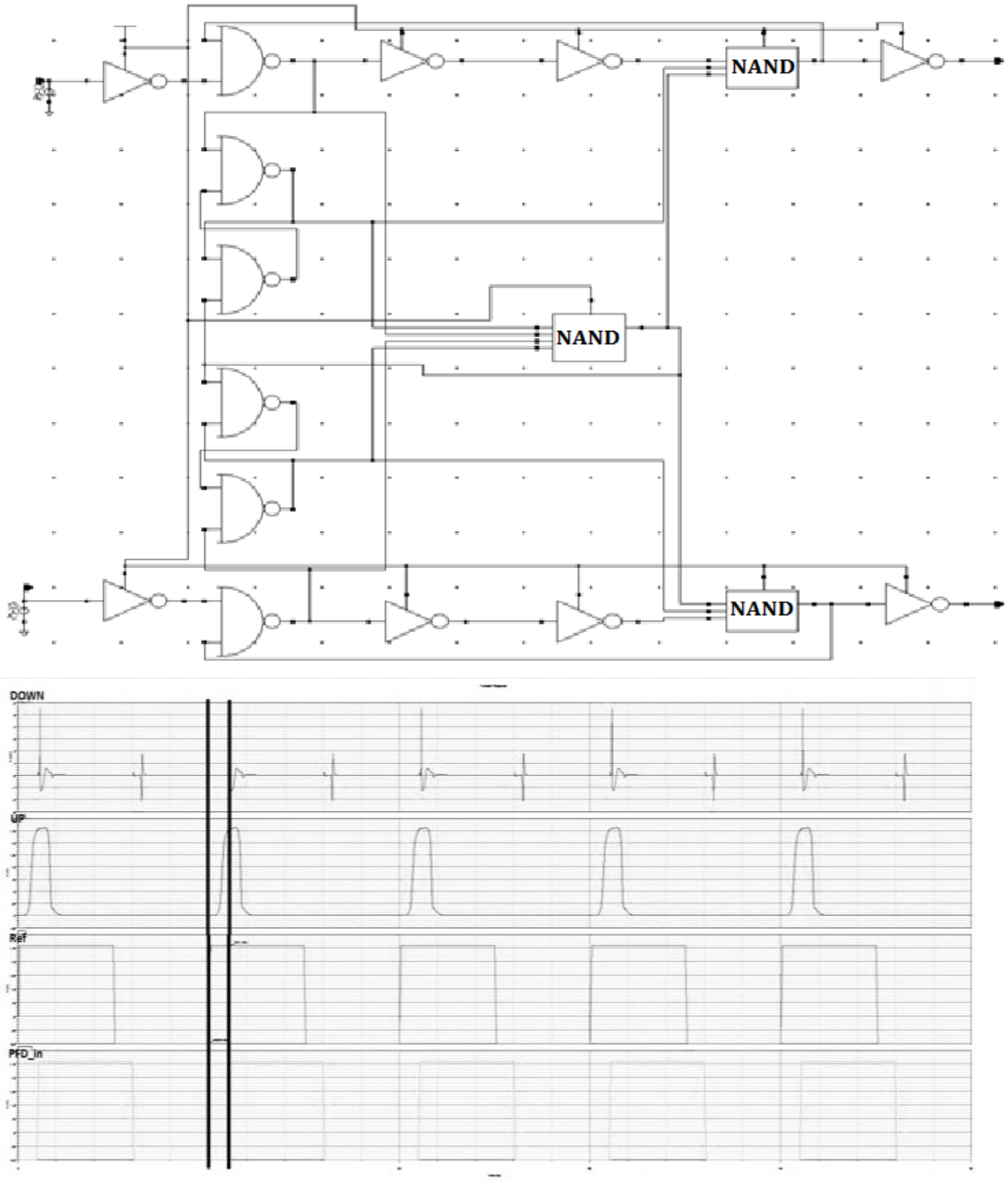


Figure 3.3.3 PFD Circuit and Sample Output: vertical axis is 250mV/div for UP, Ref and 1mV/div for DOWN, horizontal axis is 2nsecs/div.

Digital circuit timing issues are addressed by way of the inverter chains. This provides signal clarity at the decision points in the circuit. Another issue to address is the dead zone that occurs for small differences in phase difference of the PFD inputs. Increasing the speed at which the logic gates make a decision can reduce the

size of the dead zone. Even with the dead zone in place, the PLL can theoretically "lock" f_{div} and f_{ref} in the sense that their phases are not varying. Some transient ringing will still occur though if the dead zone with either signal leading is large enough to cause an error that propagates through the loop. This error will show up as additional phase noise at the output of the synthesizer. The effect of the dead zone on the phase noise for higher frequency systems is one reason why high frequency PLL-based frequency synthesizers are difficult to build.

3.4 Circuit Design of the Active 4th-order Loop Filter

A fourth order active low-pass loop filter is built at the circuit level. A fourth order filter was chosen considering the order of the DSM. The filter order must meet or exceed the order of the DSM in order to sufficiently attenuate the higher frequency components attributed to the higher order DSM [7]. An active loop filter was chosen over a passive version in order to allow a constant phase error in the PLL. The system can still achieve "lock" with a constant phase error. When the PLL is constructed with a passive filter some minor corrections to the phase can disappear since the filter is without a mechanism for adjustment. With an active filter those adjustments can be held due to the gain of the operational amplifiers (opamps) in the design.

Shown in Figure 3.4.1 is the fourth order active loop filter (capacitance values vary with eventual tuning) implemented using four cascaded first-order stages. A 1 MHz bandwidth was chosen to allow fast locking speed on the order of 1μsec. The low-pass characteristic of the filter is shown in Figure 3.4.2 along with the out of band roll-off in dB/decade. Also shown in Figure 3.4.2 is the transient response to a sinusoidal input. The output shows a smooth transition, ending on the average of the sinusoidal input. The axis values were left out intentionally.

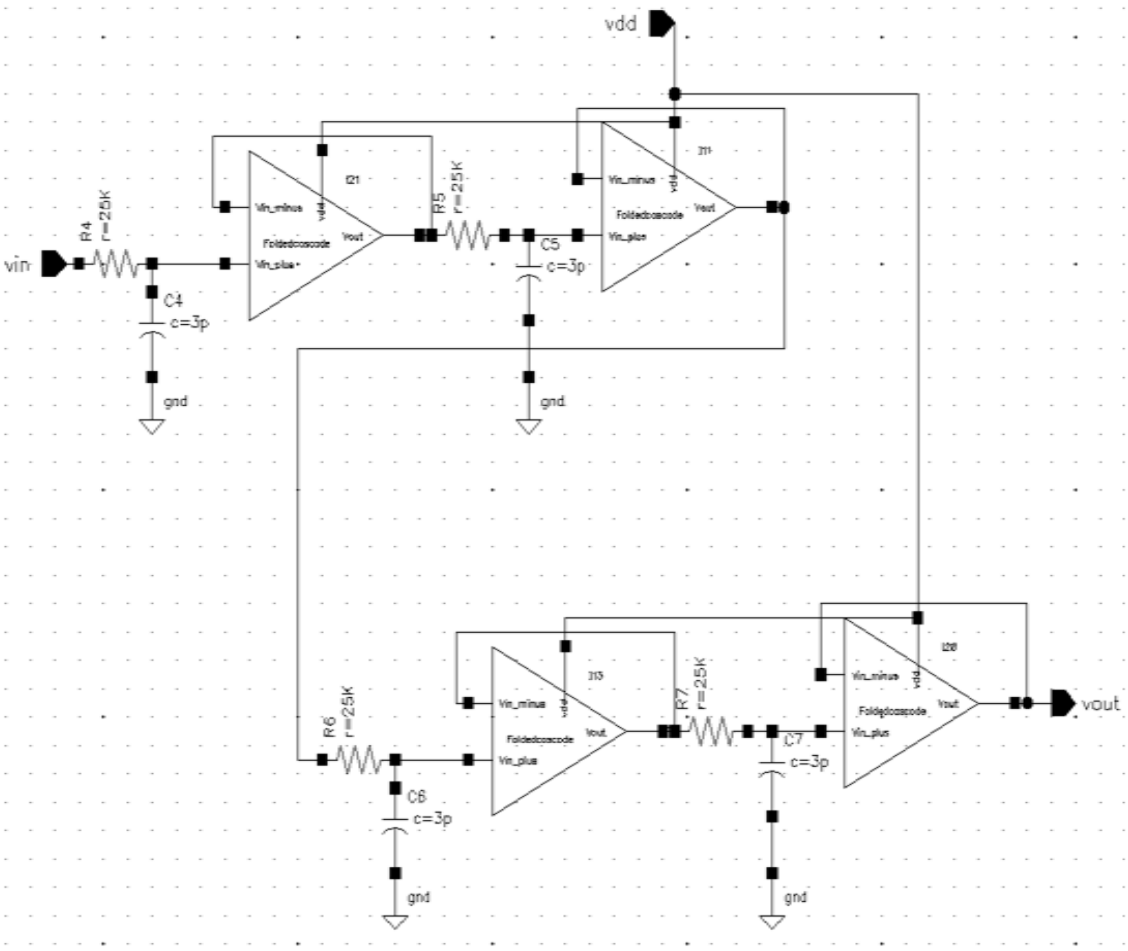
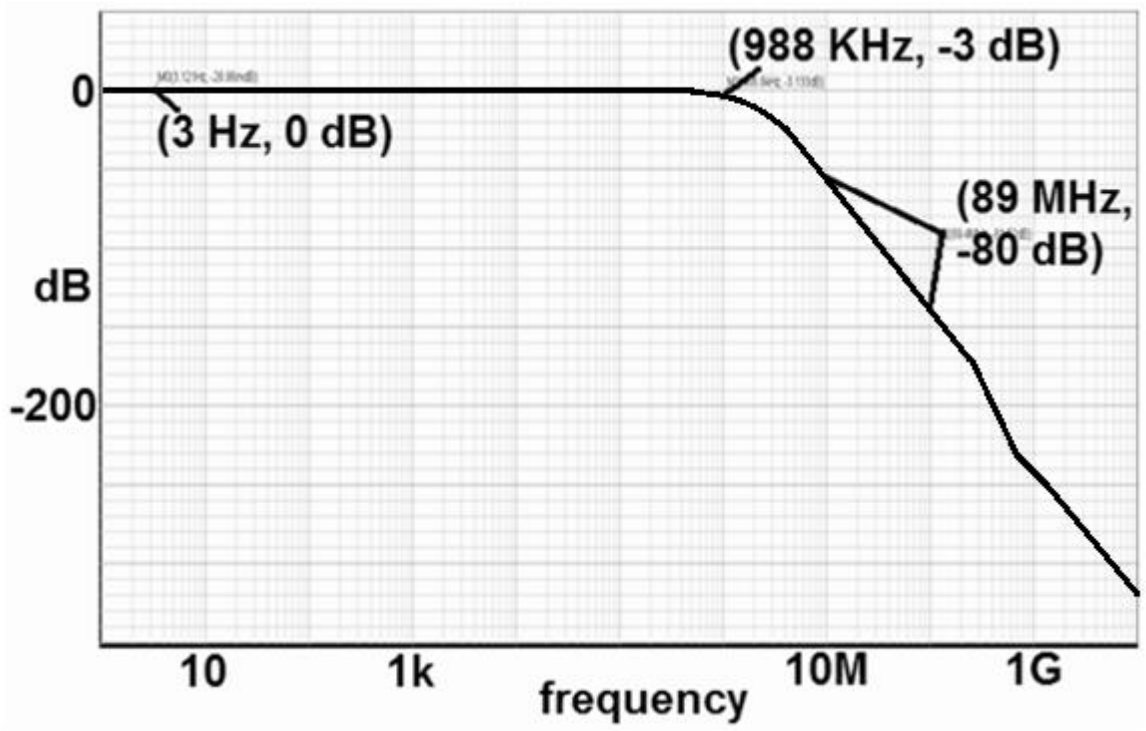
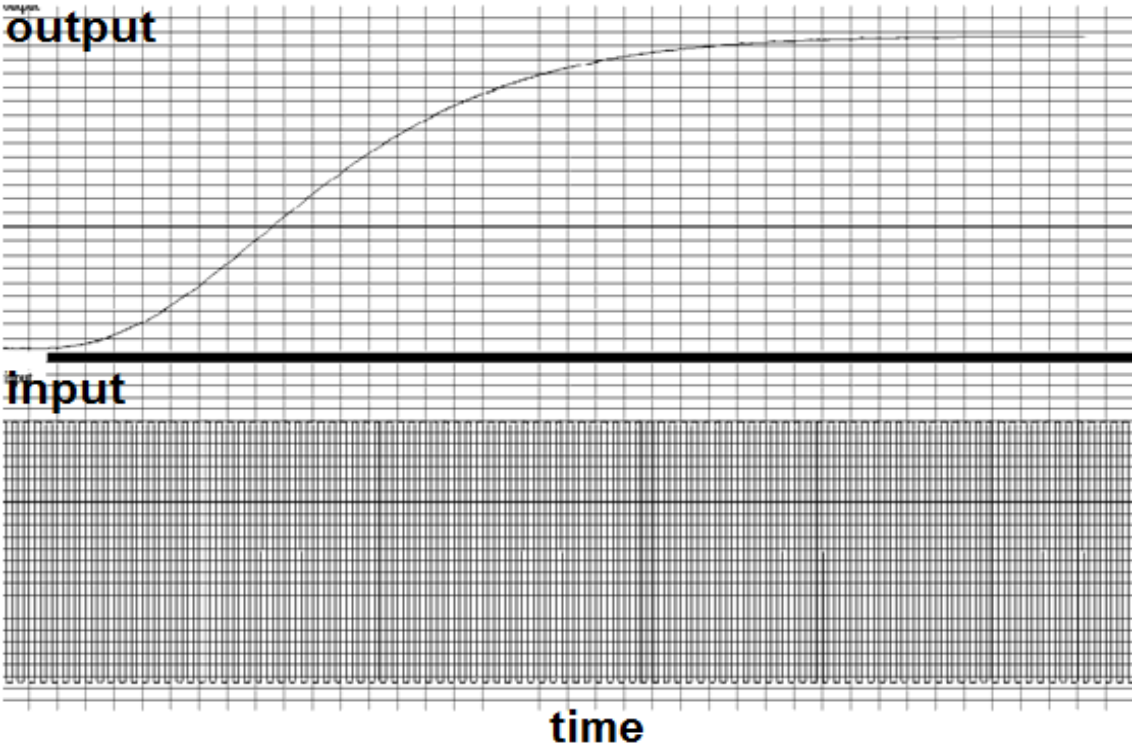


Figure 3.4.1 Fourth-order active loop filter for a 1 Mhz bandwidth



(a)



(b)

Figure 3.4.2 (a) frequency domain of the fourth-order filter (b) transient output of the fourth-order filter

The active filter is based on the cascade of four first order stages with unity gain buffers placed throughout. The chosen opamp topology was a folded cascode input stage and two extra stages of amplification. This was chosen for the high gain and the single-ended output. The third stage is in place to achieve simultaneous high output swing and low output impedance.The design of the opamp used for the unity gain buffer is the biggest challenge of the filter design. This challenge can be detailed using Table 3.4.1. The design of opamps is a core topic of many texts [25], [24], [21], [26], making it common ground for analog integrated circuit designers. This is due in large part to opamps being the fundamental building block for many types of circuits all of which requirestringent specifications. Most important of these specifications is the open loop gain A_o. A large value of A_o minimizes the gain error in the closed-loop form. This large open loop gain also provides what is needed to minimize the gain error when connected in feedback as follows, using the variables from Figure 3.4.3(b) the closed loop gain is

$$\frac{Y}{X} = \frac{A_o}{1+A_o H}$$

where H is the feedback factor. To achieve a gain error less than 0.1% of the desired gain $\frac{1}{H}$,A_o must be greater than 1000, as shown by

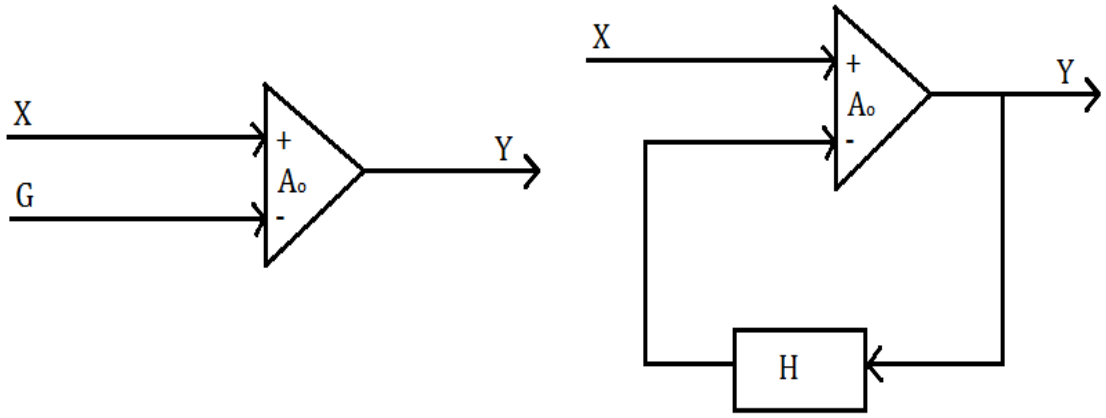
$$\frac{Y}{X} = \frac{A_o}{1 + A_o H} = \frac{1}{H}\frac{A_o}{\frac{1}{H} + A_o}$$

if A_o is much greater than 10, then $\frac{Y}{X}$ is approximated by

$$\frac{Y}{X} = \frac{1}{H}(1 - \frac{1}{H}\frac{1}{A_o})[21]$$

greater than 60dB dc gain
greater than 60° phase margin
high output swing
low rms noise level
low power consumption
small size
low output impedance
single-ended output

Table 3.4.1 Opamp requirements

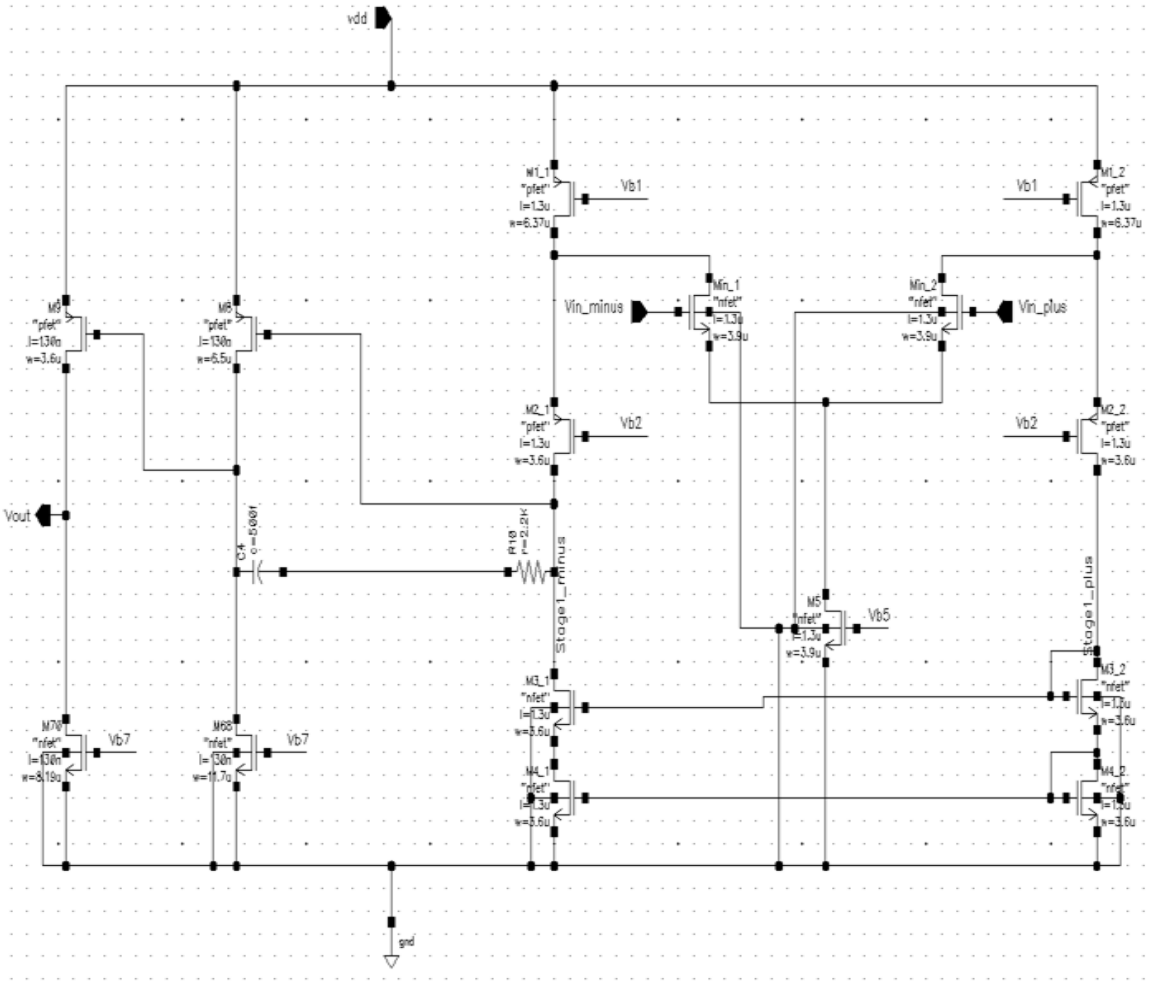


(a) (b)

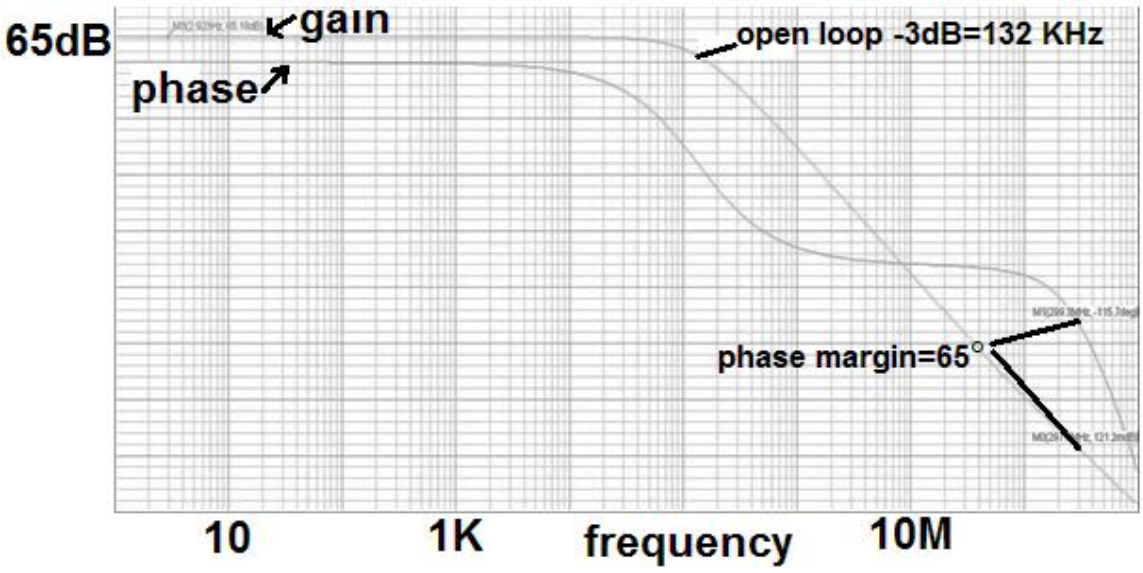
Figure 3.4.3 Opamp Shown in (a) open loop and (b) feedback setup.

The tradeoff paradigm associated with opamp design consists of all items listed in Table 3.4.1 and others not listed here. The high gain comes at the cost of lower initial phase margin and generally higher noise levels, primarily low frequency noise or flicker noise [25], [27]. Compensation is thus required and lowers the open loop bandwidth. High output swing requires small biasing margins among the output transistors. However, low output impedance is desired for voltage amplifiers. Small biasing margins above the threshold voltages make it difficult to have low resistance in these transistors and thus low output impedance. On another level, both low

amounts of noise and small area are desired at the same time. However,decreasing the size of transistors will increase the noise inherent in the opamp.Noise inherent in transistors is a complicated topic, the reader is referred to [27] for further understanding. These tradeoffs along with many others make opamp design very challenging. Shown in Figure 3.4.4 is the opamp at transistor level along with the AC analysis and DC gain verification. The DC gain is verified over a large swing to show there is an adequate amount of gain at the voltages required by the filter. The gain is higher over a smaller area centered at 900mV.



(a)



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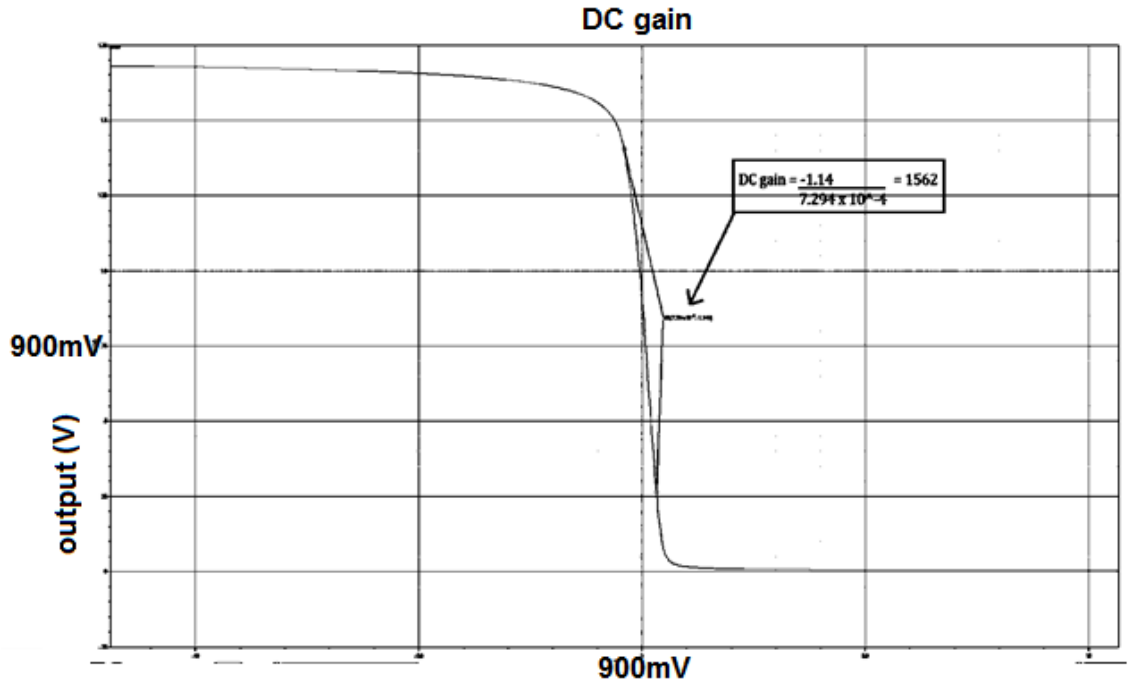

(c)

Figure 3.4.4 (a) Opamp circuitry (b) AC analysis (c) DC gain

3.5 Circuit Design of the Multi-Modulus Frequency Divider

The circuit used for the MMD is shown in Figure 3.5.1 and was adapted from [12]. The idea behind the design is to use a state machine that produces a pulse after

a certain number of input cycles. The divider is made from three cascaded divide-by-two-or-three stages. The overall combination gives a divisor of anywhere from 8 to 15 based on a 3-bit control signal.

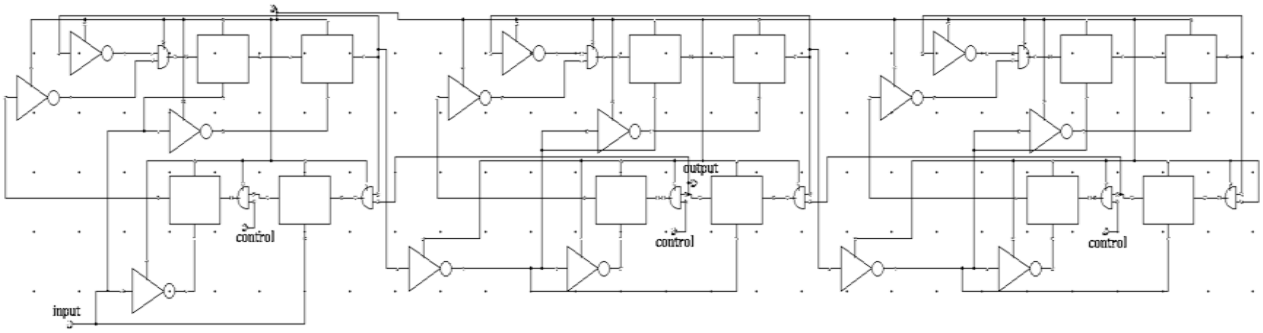

Figure 3.5.1 Divider Circuit (squares are d-type flip-flops)

3.6 Circuit Design of the Delta-Sigma Modulator

The all-digital delta-sigma modulator used was a feed-forward 20-bit topology with a single-bit output. The overall circuit is shown in Figure 3.6.1 with the overall design choices discussed in Chapter One. The input selection circuitry allows for a pre-computed value to enter the DSM based on the output. Registers used for the integrators (digital accumulators [28]) were built using dynamic D-type flip-flops. The 20-bit adders of the three integrators were used in 19-bit fashions in order from left to right so as to avoid losing information in the most significant bits.

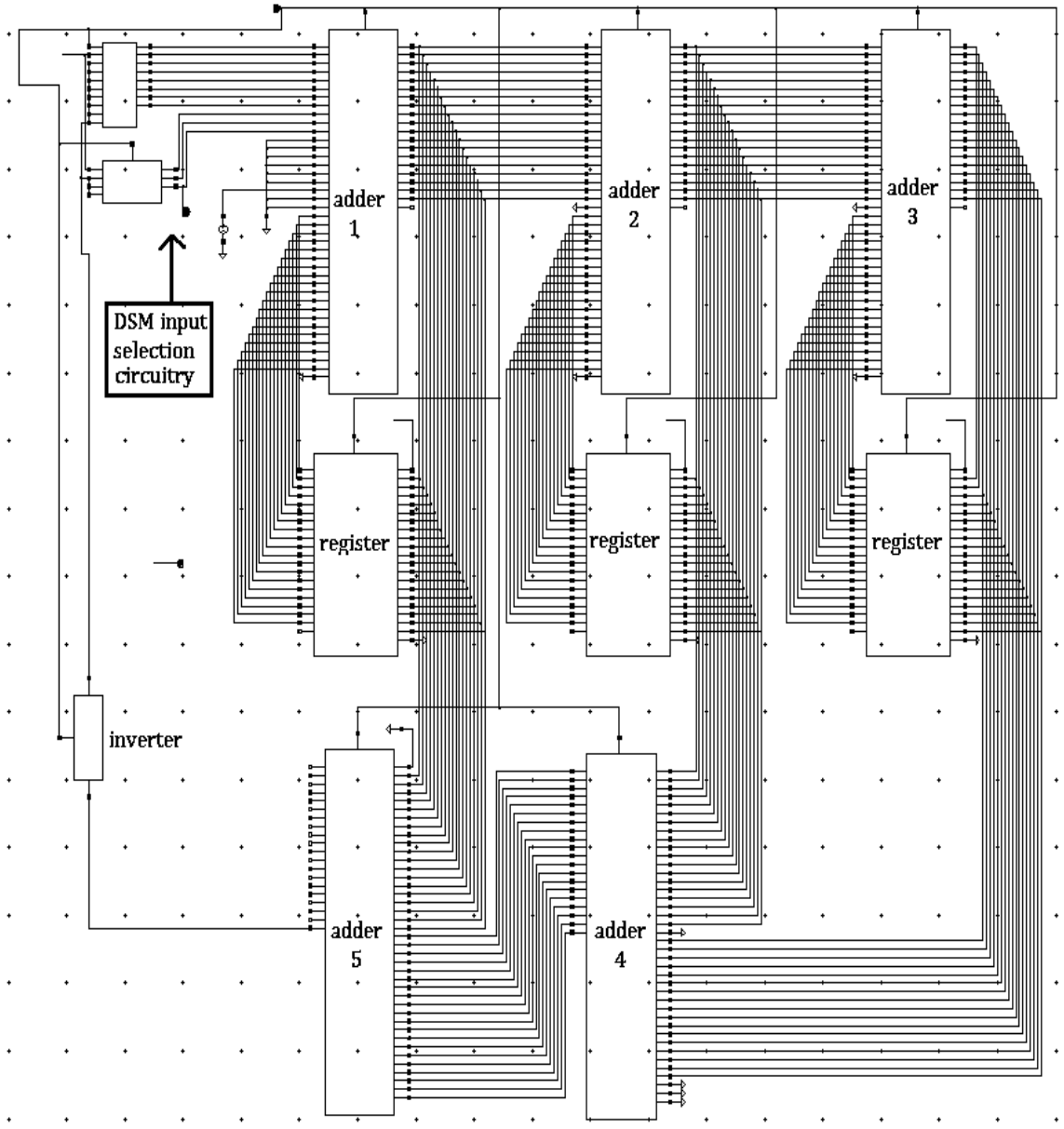

Figure 3.6.1 20-bit 3rd-order feed-forward all-digital delta-sigma modulator

Adder 4 uses the output from the third integrator divided by four. The 20-bit adders were built using a radix-2 Kogge-Stone carry-look-ahead (CLA) adder design, the CLA adder tree is shown in Figure 3.6.2[20]. This type of adder was chosen for its high speed being that the DSM has to keep up with the PFD frequency of 100 MHz. The initial stage (top row of dots) requires the production of both propagation and generation signals, the following stages use a dot operator specific to radix-2

designs. The 20-bit and 3rd-order combination,within the DSM, is near the maximum allowable for 100 MHz operation. If either the order or the number of bits increased, adder 5 would not receive both values at the same time for proper addition.

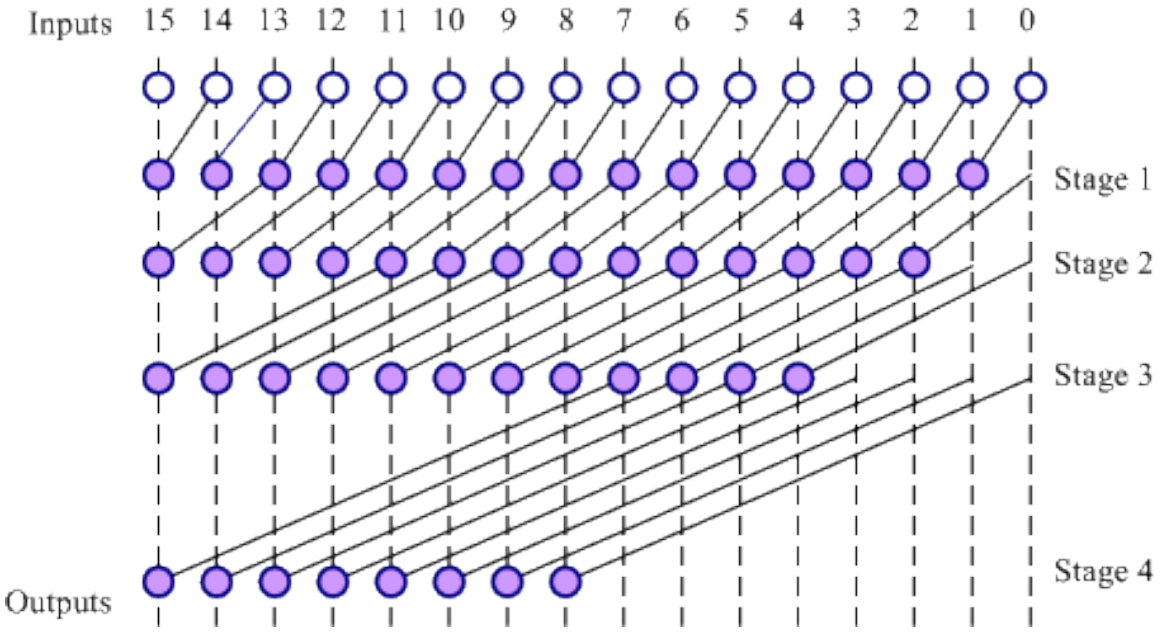

Figure 3.6.2 4-bit CLA adder.

Chapter 4: Testing and Results of the Delta-Sigma Frequency Synthesizer

4.1 Delta Sigma Modulator Results

In order to understand the results of the entire system an overview of the delta-sigma modulator output is provided. The purpose of the delta-sigma is to produce a "random" number sequence around a certain frequency with the lowest power level being at the center. This section verifies that the output of the delta-sigma modulator is random in its time domain appearance and that the power spectrum shows significant noise shaping around the center frequency. All simulations were performed using Cadence Spectre analysis software.

The transient analysis was achieved using a ramp-up approach. The ramp-up was needed in order to find initial conditions with as large of a circuit as the DSM. The length of time for the DSM to operate was 1.75µsec as this would show a sufficient number of cycles since the DSM ran at 100 MHz clock speed. The transient result is shown in Figure 4.1.1 to provide a visual of the randomization property.

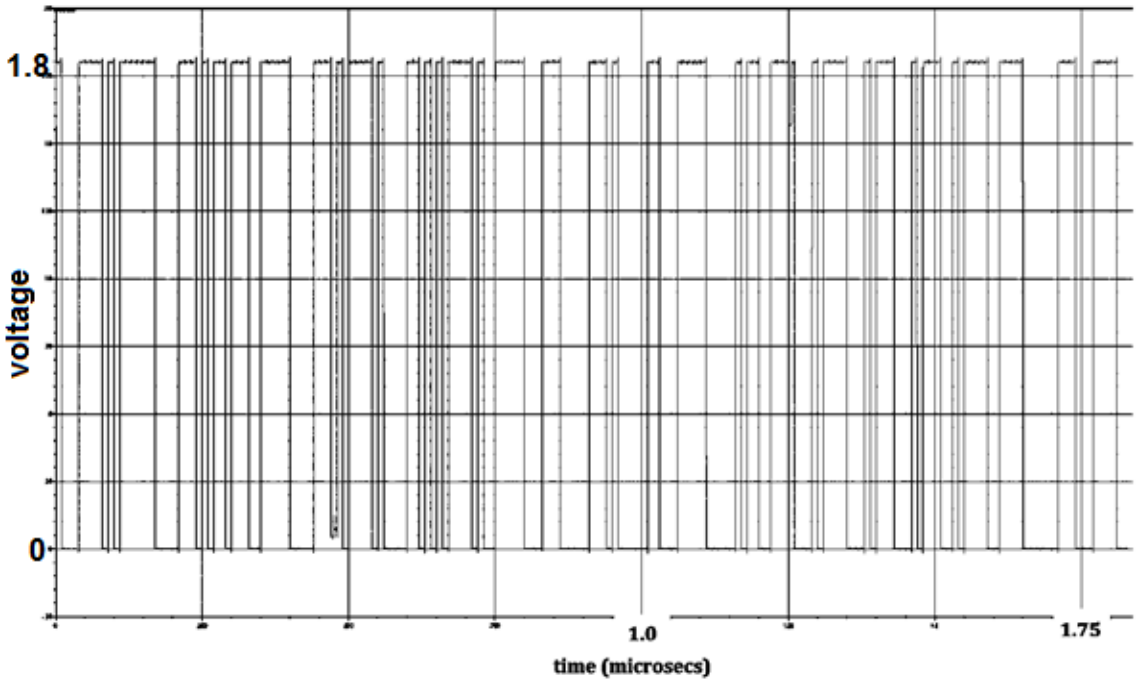

Figure 4.1.1 Transient to 1.75µsec

The noise shaping ability is the fundamental operation of the DSM. To check the noise shaping performance a power spectral density (PSD) was found using Cadence Spectre for the DSM output and the clock for comparison. Figure 4.1.2 shows the noise shaping ability over a wide range to give a broad perspective. The DSM output power clearly decreases in the region around the center frequency of 100 MHz. As expected the DSM output shows a decrease of power around the 100 MHz center (approx. -45dB) and an out of band increase in power (approx. 16dB at 25MHz offset from the center).

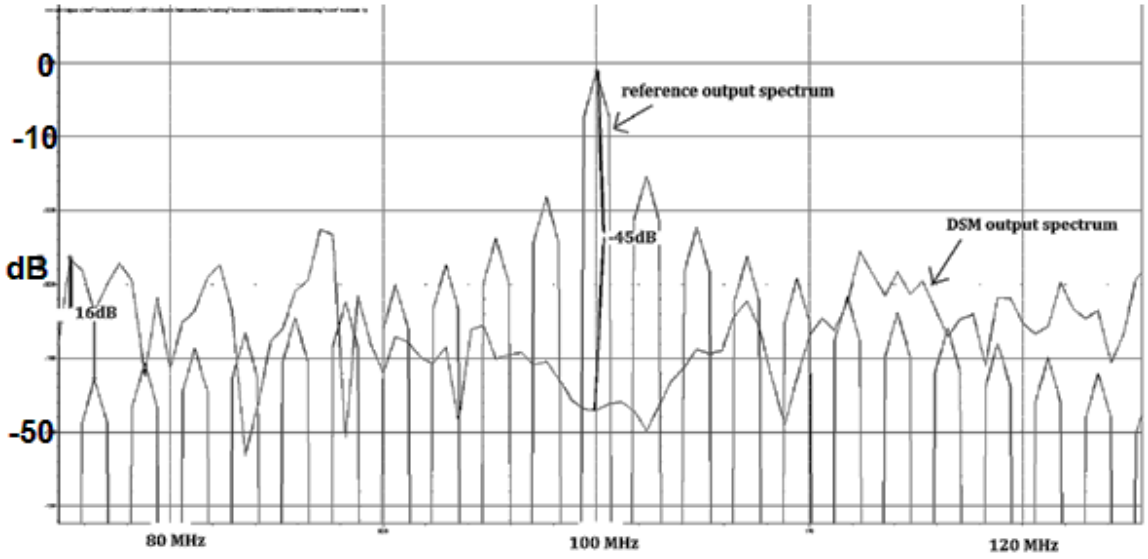

Figure 4.1.2 Spectrums of the DSM and the reference

4.2 Overall Frequency Synthesizer Results

Transient Testing, Results and Tuning of the Overall System

Many simulations of the entire FS were performed in the time domain, each taking multiple days to complete. Each simulation required a modification of the circuit parameters. The circuit was adjusted outside of the initial system level parameters to account for non-ideal effects inherent in transistor level designs. The system level approach was needed to provide a starting point, each building block was then made to adhere while tuning was performed along the way.

An example of a transient result that indicated circuit tuning was required is shown in Figure 4.2.1. The length of this simulation was two days to achieve less than 2μsec of running time. The exact values are not important in this example, only the characteristics of the plot. At the center of the plot it can be seen that VCO_control (i.e. the control voltage of the VCO) is leveled out. This voltage level input to the VCO provided the average necessary to achieve the desired frequency. The problem is that after this point the DSM signal (through correct operation) provided a larger number of "ones". This signaled the divider to divide by 15 more than 14 which in turn caused PFD_in to further lag ref and the Up signal to occur with greater duration. The larger widths of the Up signal caused the LF to adjust downward thus increasing the VCO output due to the negative gain of the VCO. Since the bandwidth of the loop was too large, this process occurred too fast thus providing a large change in the VCO_control. The DSM then provided (correctly) a larger number of "ones" again. The process continued to make the signals move too far out of phase. The other problem is that the VCO signal was traveling back through the varactor diodes to the VCO_control line making it oscillate, shown by the wide VCO_control line.The indication is that the system could not handle the variations in the DSM control line. To attempt to fix these problems the LF bandwidth needed to be decreased and a capacitor was added to the VCO_control line.

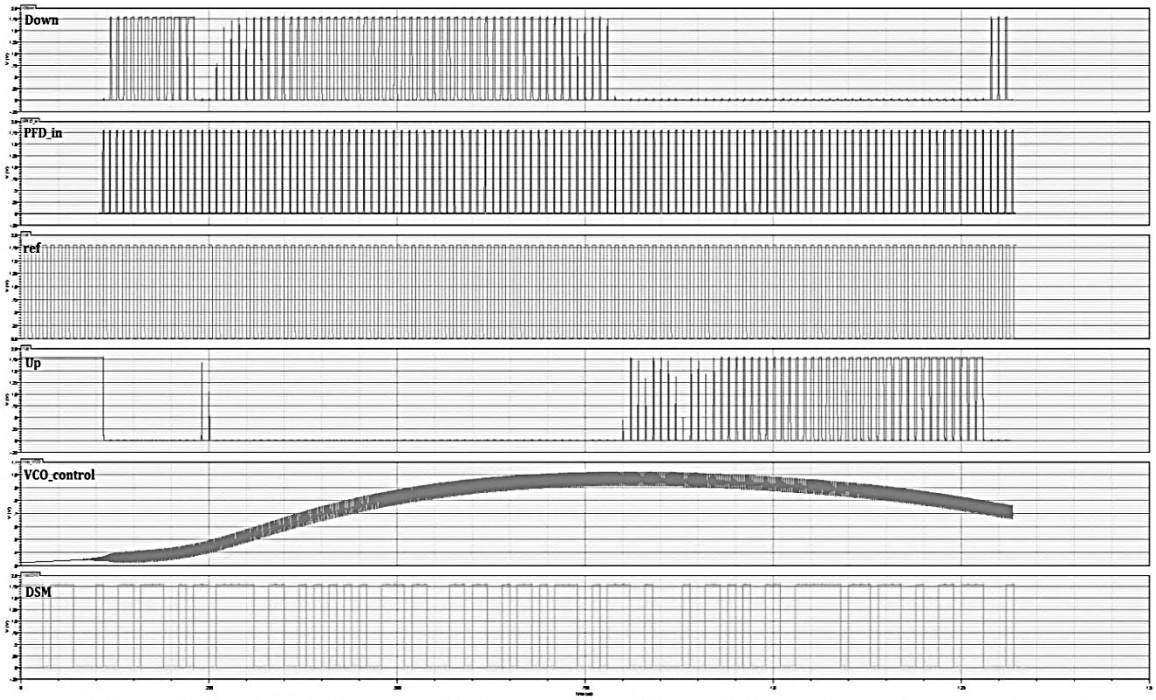

Figure 4.2.1 Transient Test.

Further transient testing revealed an important tuning tradeoff within the system. The reference frequency and thus the operating frequency of the DSM must run at a much higher level (approximately 10 times greater) than the bandwidth of the overall system. If the system bandwidth is too large relative to the DSM operating frequency the system will make too large of adjustments when the large delays of the DSMs random signal occur. The concept is illustrated in Figure 4.2.2. When a logic “high” or “low” value is held for a large duration the system places a large emphasis on the short term average of the DSM, neglecting the long term average. The long term average (i.e. the average for the entire DSM signal) plays a crucial role since this is what defines the overall system frequency.

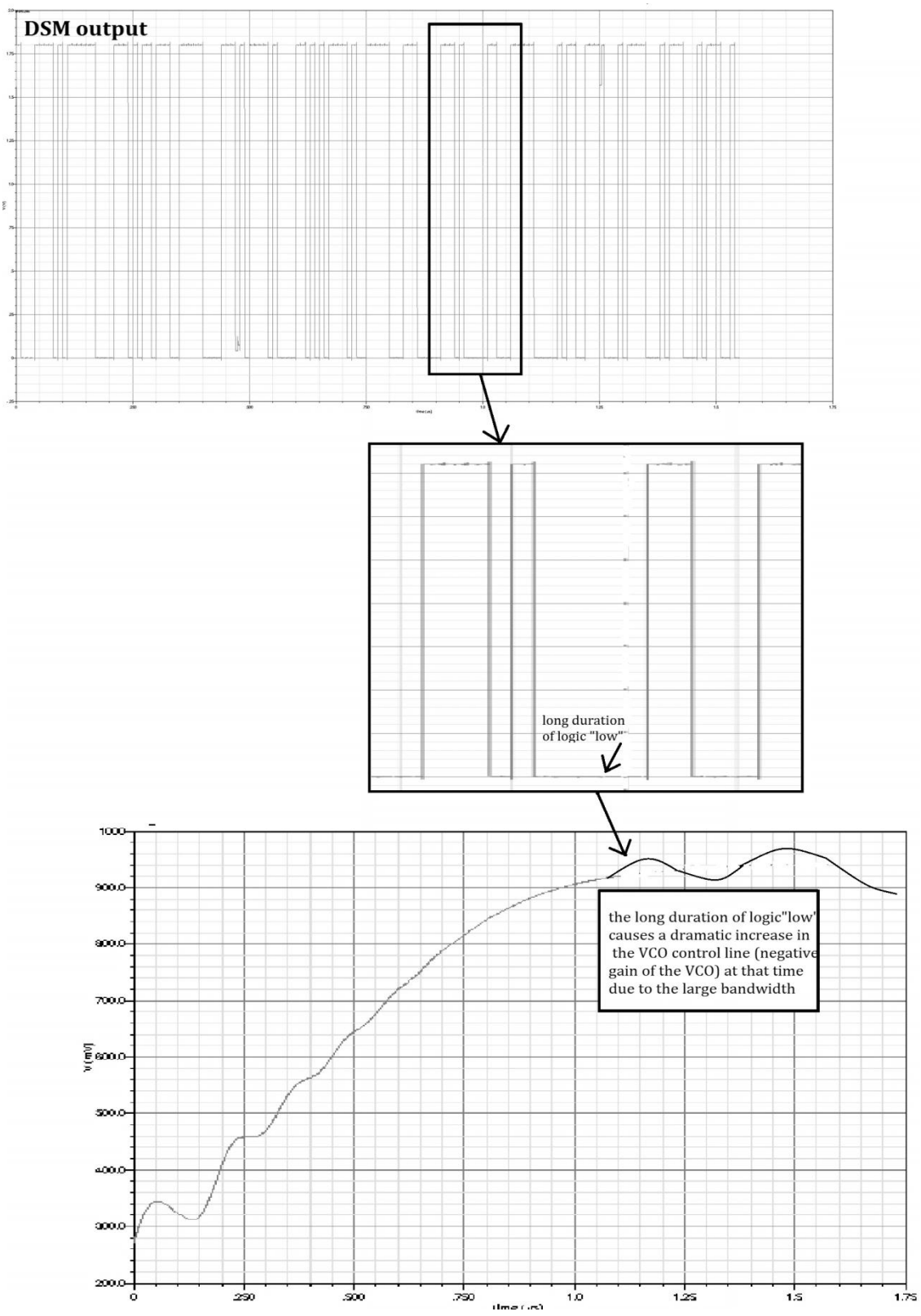

Figure 4.2.2 Effect of long duration logic “Low” in the DSM output on the VCO control line

After extensive testing and tuning of the overall system, the synthesizer achieved "lock" as shown in Figure 4.2.3. The final adjustment was that the division ratios in the MMD were changed to 58 and 59 rather than 14 and 15. This allowed for the system to make fewer decisions within the simulation time period. The reference frequency was then changed to 24.57 MHz to achieve the desired frequency. Changing the reference frequency did not affect the randomization property of the DSM. The time it takes for the system to settle, i.e. start-up time, is approximately 4μs as shown in Figure 4.2.3.

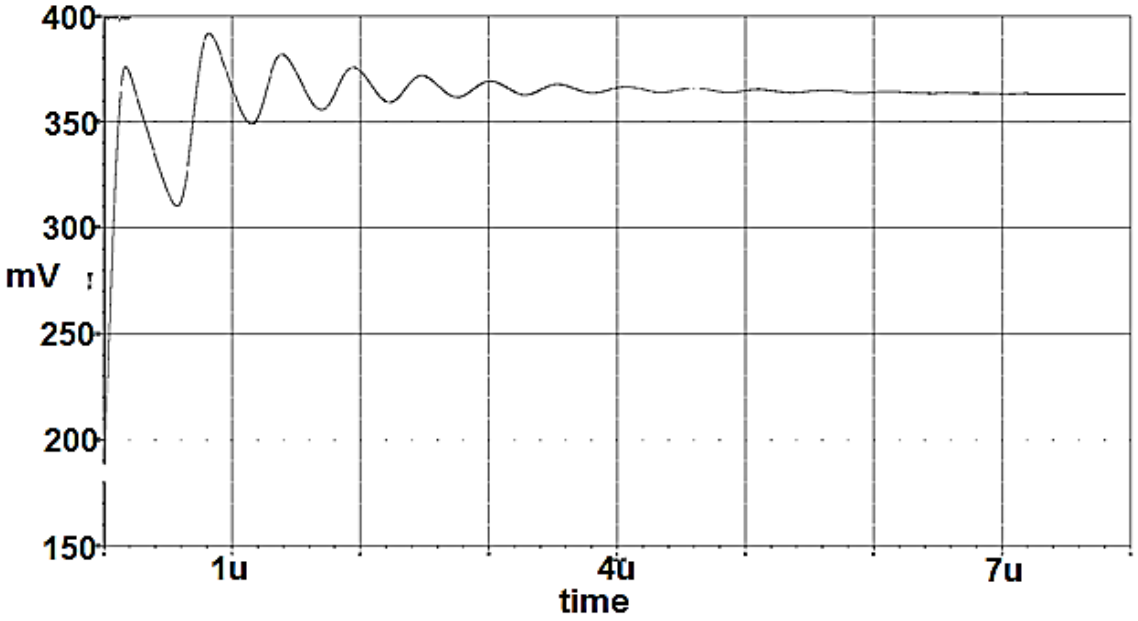

Figure 4.2.3 VCO control transient waveform

Phase Noise and the Power Spectrum

A PSD was generated for the output of the synthesizer to verify that the center frequency is as desired. The PSD of the synthesizer output gives 1.43 GHz as the center frequency. To check if the center frequency is correct, the average output of the DSM is calculated and found to be 0.678. To find the desired output frequency we first find the average division ratio as

$$\frac{0.678}{1.8} \cong 0.37667$$

$$0.37667 \times 59 = 22.223$$

$$1 - 0.37667 = 0.62333$$

$$0.62333 \times 58 = 36.15314$$

$$22.223 + 36.15314 = 58.376$$

$$58.376 \times 24.57\ MHz = 1.4343\ GHz$$

closely matching the actual output center frequency of 1.43 GHz.

Many methods exist for measuring phase noise in simulated circuits [29-31]. The method used here was developed by the Cadence© design team. The idea is to include a PLL noise measurement within a transient analysis, viewing the synthesizer as an oscillator. This way the phase noise is extracted from the transient output rather than simulating phase noise of each system block separately and combining the results. The drawback to the method used here is the time required to obtain low frequency offset measurements from the carrier. This drawback is the reason that in-band spurious tones were not measured. The limit for the lower offset measurement is dictated by the length of simulation. In order to obtain smaller offsets, the simulation time has to be extended. For example, if the closest phase noise measurement is desired to be 10KHz, the simulation time has to be 400μs. A simulation of this duration would take two weeks to complete. Shown in Figure 4.2.4 is the phase noise plot of the DSM controlled fractional-N frequency synthesizer. The simulation time, of the transient noise measurement, was chosen to be 2μs to allow for the measurement ofat least the 3 MHz offset phase noise. Phase noise was found to be -82 dBc/Hz at 3 MHz offset.

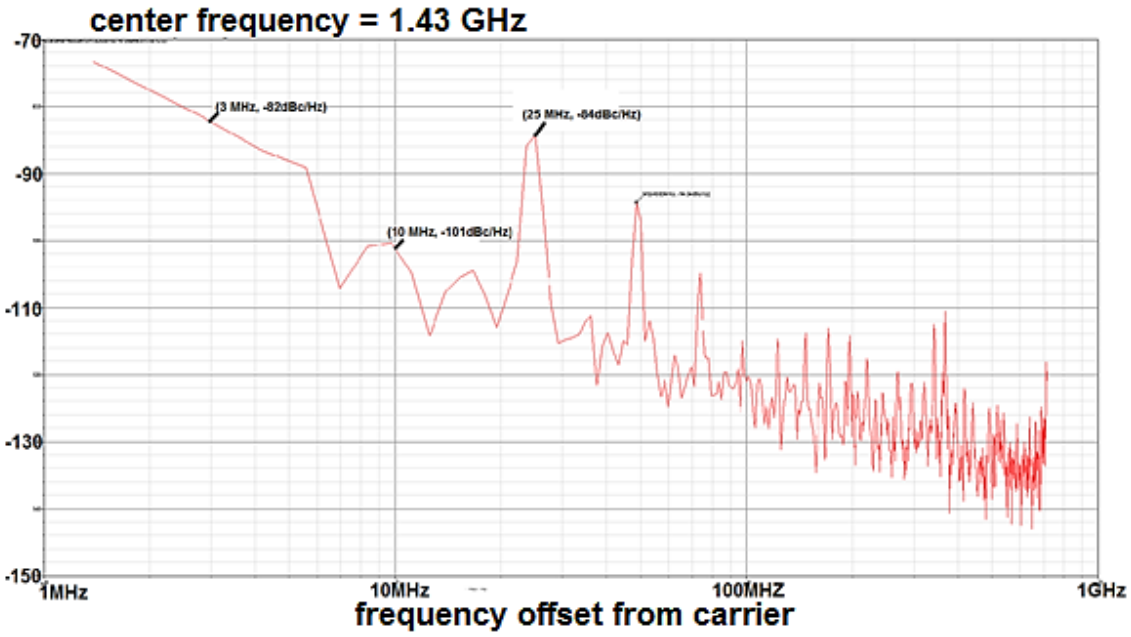

Figure 4.2.4 Phase noise plot of the DSM controlled fractional-N frequency synthesizer

Chapter 5: Future Improvements

PLL-based delta-sigma fractional-n frequency synthesizers can be improved in many ways. This chapter discusses multiple ways to make improvements on such systems. The idea of this chapter is to provide a review of current studies in the field of frequency synthesizers and how they can be used to improve the function of the device in this thesis. Alternate methods for cancelling different types of noise in the system will be presented first. Types of noise sources to be addressed include that which is associated with the delta-sigma control of the MMD along with the overall system output phase noise. A look at the architecture of the DSM design in this thesis is next, addressing the possibilities for increasing the noise shaping ability. Next, a wider bandwidth of the system is discussed which makes way for a discussion on using the FS for direct modulation. A higher center frequency of the overall synthesizer is then considered. Lastly, a system allowing a wider tuning range using coarse pre-tuning is then covered.

5.1 Other Noise Cancellation Techniques

The noise shaping properties of delta-sigma modulation can be used to reduce in-band spurious tones in a way other than controlling only the MMD. The method proposed in [32]utilizes a noise cancellation technique similar to MASH DSM where low-order stages are cascaded and later stages cancel the noise of the earlier stages. An accumulator is used initially instead of a DSM for the control of the MMD. The residue of the accumulator output is fed to a DSM whose output is used to cancel noise in the hybrid PFD/DAC. Including the cancellation circuitry in the PFD allows for the inherent noise to be cancelled.

Another method for reducing noise in fractional-N frequency synthesizers is by including a noise filter as presented in [33]. This method places a noise filter in the feedback path that is based on an integer-N FS. Out-of-band quantization noise introduced by the DSM is thus reduced. Folded noise due to nonlinear effects in the PFD can also be reduced with this noise filtering technique.

5.2 Higher-order Delta-Sigma Modulation and Alternate Topologies

Increasing the order of the DSM will increase the noise shaping ability of the modulator and thus further reduce the in-band spurs of the overall synthesizer output [ref]. The effectiveness of increasing the order to achieve better performance will decrease with larger orders of modulators. Increasing the order will also require more circuitry in the loop filter in that the order of the filter will need to increase as well. Instead of increasing the order of a single stage modulator an alternate method for DSM can be used. One alternate method is known as multi-stage noise shaping (MASH) delta-sigma modulation [19]. With the MASH approach, lower-order stages are cascaded to achieve increased out-of-band noise. Each successive stage shapes the noise of the previous stages. A drawback of the MASH topology is that the output bit pattern is more susceptible to substrate noise coupling [7].

5.3 Wider System Bandwidth

A wide bandwidth of the overall synthesizer is desirable. With a wider bandwidth there are a large number of design issues. If the system bandwidth is too large without addressing additional noise issues, there can be additional phase noise due to noise folding. Many current studies address the issue of increasing the system bandwidth. One method is to include a cancellation mechanism for mismatch-induced errors [34]. Through this method, phase error cancellation occurs at the output of the PFD.Controlling noise at the PFD can be done in different ways included that which was performed by[35]. Another method would be to implement a differential system to allow for phase error cancellation similar to that used in [36] and [37]. Tuning of the VCO at high enough speed to account for additional bandwidth is important as well and could be addressed similar to what was used in[38]. The method introduced is a feedback system within the VCO to quickly and accurately find the correct frequency. Fast switching of the system from one frequency to another for use in direct modulation could be approached from another angle. Placing the desired frequencies at a small percentage of the PLL

capture range would allow faster switching time being that the frequency change is smaller [39].

5.4 Higher Synthesized Frequency

As CMOS and other technologies are able to handle higher frequencies the ability to develop fully integrated frequency synthesizers at these frequencies is growing. Several studies show the development of synthesizers above 2.5GHz [40], [41], [35]. One method that could be adapted for future designs is that shown in[42]. This method uses analog mixers along with PLLs to achieve a multiple step approach to frequency synthesis. The mixer brings the signal down to a frequency level that can be interpreted by an integrated PLL. Another alteration to achieve a higher frequency would be to use a newer technology, such as deep sub-micron CMOS technology, which has demonstrated operation above 60 GHz [43]. A reason for pursuing a higher frequency is the large amount of bandwidth available [37].

5.5 Wider Tuning Range

The idea of integrating the entire synthesizer on a single chip (i.e. the PLL *with* the loop filter, VCO and DSM) serves the mobile application industry and other highly-integrated systems such as digital tuners [44]. An extension to full integration is to empower the system to cover a large tuning range. This would allow a number of applications on a mobile device to be used with a single frequency synthesizer covering multiple bands. Most studies concerning a wide tuning range start with a wide tuning VCO [45-49]since it is most often the main limitation. One method to develop a VCO with a wide tuning range uses a coarse tuning method by selecting from an array of capacitors as shown in [49]. The coarse selection pre-tunes the VCO to the appropriate range and the VCO is further tuned in a feedback loop to achieve the correct frequency. Adjusting the capacitance in the VCO is more efficient due to the size. It is not feasible to adjust the inductance due to size [21]. Another method for adjusting the capacitance of the VCO is to use a transmission line approach [37]. Switch-capacitor units are cascaded to form a transmission line whose overall capacitance can be digitally adjusted using the

cascaded units. This provides a coarse pre-tuning similar in concept to the study previously mentioned in this section. Yet another method for increasing the tuning range starts with reducing the noise in the divider [41].

Chapter 6: Conclusions

A PLL-based delta-sigma fractional-n frequency synthesizer was designed and implemented at transistor level. A system level approach was used to develop the initial design. This allowed for the specific types of circuits to be chosen. The PFD was constructed out of a proven topology to allow for fast operation, with the final choice for a reference frequency being 24.57 MHz. A tri-state selector was used in place of a charge pump for simplicity. The loop filter was constructed out of four cascaded first-order filter stages with the active portion being a single-ended opamp. The opamp design was based on the specifications outlined in Table 3.4.1. These specifications were chosen to allow high-speed operation along with high gain. An RLC-tank oscillator was used for the VCO to achieve a high frequency with low noise. The final version of the divider was implemented by cascadingfive divide by 2-or-3 stages that are made of simple state machines to allow for the divider ratio to toggle between 58 and 59.

Simulating the overall circuit began with ensuring the correct operation of the DSM. Transient results of the DSM were discussed and showed the randomization property as in Figure 4.1.1. The PSD of the DSM output was also discussed. The output of the DSM verified the noise shaping ability around the reference frequency as shown in Figure 4.1.2. Next was a discussion of how the overall frequency synthesizer was tuned. Multiple trials were attempted to show the methods used to adjust the system performance, with the main goal being to achieve “lock”. Results for such trials are shown in Figures 4.21 and 4.2.2. The overall frequency synthesizer achieved a simulated phase noise performance of -82 dBc/Hz at 3 MHz offset with a center frequency of 1.43 GHz. The difference between the actual performance and the desired performance outlined in Table 1.4.1 is due primarily to the system not achieving perfect “lock”. Further tuning of the overall frequency synthesizer would allow for a better lock condition. A short simulation time also played an important role in the performance measurement of the system. As discussed in the phase noise portion of section 4.2, the length of simulation must be

large for precise results. Considering the difficulty in designing and building a DSM fractional-N PLL frequency synthesizer, this design is sufficient in that it achieves "lock" at a frequency close to the desired value.

Bibliography

[1] L. R. Ulrich and P. N. David, *RF/Microwave Circuit Design for Wireless Applications*: John Wiley & Sons Inc., 2000.

[2] W. F. Egan, *Phase-Lock Basics*: Wiley-Interscience, 2007.

[3] W. Khalil, S. Shashidharan, T. Copani, S. Chakraborty, S. Kiaei, and B. Bakkaloglu, "A 700-µA 405-MHz All-Digital Fractional-N Frequency-Locked Loop for ISM Band Applications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp. 1319-1326, 2011.

[4] Y. Ching-Yuan, W. Jun-Hong, and C. Hsuan-Yu, "A 5-GHz Direct Digital Frequency Synthesizer Using an Analog-Sine-Mapping Technique in 0.35-µm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 2064-2072, 2011.

[5] F. Gardner, "Charge-Pump Phase-Lock Loops," *Communications, IEEE Transactions on,* vol. 28, pp. 1849-1858, 1980.

[6] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "DELTA-SIGMA-MODULATION IN FRACTIONAL-N FREQUENCY-SYNTHESIS," *IEEE Journal of Solid-State Circuits,* vol. 28, pp. 553-559, May 1993.

[7] W. Rhee, B. S. Song, and A. Ali, "A 1.1-GHz CMOS fractional-N frequency synthesizer with a 3-b third-order delta-sigma modulator," *IEEE Journal of Solid-State Circuits,* vol. 35, pp. 1453-1460, 2000.

[8] G. Xueyang, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "24-Bit 5.0 GHz Direct Digital Synthesizer RFIC With Direct Digital Modulations in 0.13µm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 944-954, 2010.

[9] C. Quemada, G. Bistué, and I. Adin, *Design Methodology for RF CMOS Phase Locked Loops*: Artech House, 2009.

[10] C. T. Chen, *Linear System Theory and Design*: Oxford University Press, 1999.

[11] W. F. Egan, *Advanced Frequency Synthesis by Phase Lock*: John Wiley & Sons, 2011.

[12] J. W. M. Rogers, C. Plett, and F. Dai, *Integrated circuit design for high-speed frequency synthesis*: Artech House, 2006.

[13] A. Carlosena and A. Manuel-Lazaro, "Design of High-Order Phase-Lock Loops," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 54, pp. 9-13, 2007.

[14] S. Brigati, F. Francesconi, A. Malvasi, A. Pesucci, and M. Poletti, "Modeling of fractional-N division frequency synthesizers with SIMULINK and MATLAB," in *The 8th IEEE International Conference on Electronics, Circuits and Systems, 2001. ICECS 2001.*, 2001, pp. 1081-1084 vol.2.

[15] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*: IEEE Press, 2005.

[16] S. R. Norsworthy, R. Schreier, G. C. Temes, I. Circuit, and S. Systems, *Delta-Sigma data converters: theory, design, and simulation*: IEEE Press, 1997.

[17] B. Widrow and I. Kollár, *Quantization Noise: Roundoff Error in Digital Computation, Signal Processing, Control, and Communications*: Cambridge University Press, 2008.

[18] K. Shu and E. Sánchez-Sinencio, *Cmos Pll Synthesizers: Analysis And Design*: Springer, 2005.

[19] M. Kozak and I. Kale, "Rigorous analysis of delta-sigma modulators for fractional-N PLL frequency synthesis," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 51, pp. 1148-1162, 2004.

[20] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits, 2/e*: Pearson Education, 2003.
[21] *Design Of Analog Cmos Integrated Circuits*: Tata McGraw-Hill, 2002.
[22] T. H. Lee, *The Design of Cmos Radio-Frequency Integrated Circuits*: Cambridge University Press, 2004.
[23] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proceedings of the IEEE 1998Custom Integrated Circuits Conference, 1998.*, 1998, pp. 555-558.
[24] R. J. Baker, *Cmos: Circuit Design, Layout, and Simulation*: John Wiley & Sons, 2010.
[25] P. R. Gray, *Analysis and Design of Analog Integrated Circuits*: John Wiley & Sons, 2009.
[26] D. Johns and K. W. Martin, *Analog integrated circuit design*: John Wiley & Sons, 1997.
[27] M. Von Haartman and M. Östling, *Low-Frequency Noise In Advanced Mos Devices*: Springer, 2010.
[28] A. V. Oppenheim and R. W. Schafer, *Discrete-time signal processing*: Prentice Hall, 2010.
[29] K. Young Wan and Y. Jae Du, "Phase Noise Model of Single Loop Frequency Synthesizer," *IEEE Transactions on Broadcasting,* vol. 54, pp. 112-119, 2008.
[30] H. Arora, N. Klemmer, J. C. Morizio, and P. D. Wolf, "Enhanced phase noise modeling of fractional-N frequency synthesizers," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 52, pp. 379-395, 2005.
[31] F. Herzel, S. A. Osmany, and J. C. Scheytt, "Analytical Phase-Noise Modeling and Charge Pump Optimization for Fractional-N PLLs," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, pp. 1914-1924, 2010.
[32] S. E. Meninger and M. H. Perrott, "A 1-MHZ bandwidth 3.6-GHz 0.18-mu m CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE Journal of Solid-State Circuits,* vol. 41, pp. 966-980, Apr 2006.
[33] H. Chao-Ching and L. Shen-Iuan, "A Noise Filtering Technique for Fractional-N Frequency Synthesizers," *IEEE Transactions onCircuits and Systems II: Express Briefs,* vol. 58, pp. 139-143, 2011.
[34] M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, "A Wideband 3.6 GHz Digital delta-∑; Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 627-638, 2011.
[35] H. Hedayati and B. Bakkaloglu, "A 3GHz wideband ∑-delta; fractional-N synthesizer with voltage-mode exponential CP-PFD," in *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, 2009, pp. 325-328.
[36] F. Plessas, F. Gioulekas, and G. Kalivas, "Phase noise performance of fully differential sub-harmonic injection-locked PLL," *Electronics Letters,* vol. 46, pp. 1319-1321, 2010.
[37] D. Murphy, Q. J. Gu, W. Yi-Cheng, J. Heng-Yu, X. Zhiwei, A. Tang*, et al.*, "A low phase noise, wideband and compact CMOS PLL for use in a heterodyne 802.15.3c TRX," in *2010 Proceedings of theESSCIRC*, 2010, pp. 258-261.
[38] S. Jaewook and S. Hyunchol, "A Fast and High-Precision VCO Frequency Calibration Technique for Wideband Delta-Sigma Fractional-N Frequency Synthesizers," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 57, pp. 1573-1582, 2010.
[39] V. Manassewitsch, *Frequency synthesizers: theory and design*: Wiley, 2005.
[40] G. Xueyang, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "24-Bit 5.0 GHz Direct Digital Synthesizer RFIC With Direct Digital Modulations in 0.13μm SiGe BiCMOS Technology," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 944-954, 2010.
[41] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 2.9-4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-fs(rms) Integrated

Jitter at 4.5-mW Power," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 2745-2758, Dec 2011.

[42] Z. Xu, Q. J. Gu, Y.-C. Wu, H.-Y. Jian, and M.-C. Frank, "A 70-78-GHz Integrated CMOS Frequency Synthesizer for W-Band Satellite Communications," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp. 3206-3218, Dec 2011.

[43] B. Razavi, "Gadgets gab at GHz," *IEEE Spectrum,* vol. 45, pp. 46-+, Feb 2008.

[44] Y. Yu-che, L. Fang-ting, and L. Shey-shi, "A Single-VCO Fractional-N Frequency Synthesizer for Digital TV Tuners," in *Microwave Symposium, 2007. IEEE/MTT-S International*, 2007, pp. 1545-1548.

[45] P. Dongmin and C. SeongHwan, "Design Techniques for a Low-Voltage VCO With Wide Tuning Range and Low Sensitivity to Environmental Variations," *IEEE Transactions on Microwave Theory and Techniques,* vol. 57, pp. 767-774, 2009.

[46] J. Heng-Yu, X. Zhiwei, W. Yi-Cheng, and M. C. F. Chang, "A Fractional-N PLL for Multiband (0.8–6 GHz) Communications Using Binary-Weighted D/A Differentiator and Offset-Frequency Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 768-780, 2010.

[47] L. Shuenn-Yuh and C. Ching-Yi, "Analysis and Design of a Wide-Tuning-Range VCO With Quadrature Outputs," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 1209-1213, 2008.

[48] X. Jiangtao, C. E. Saavedra, and G. Chen, "An Active Inductor-Based VCO With Wide Tuning Range and High DC-to-RF Power Efficiency," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 58, pp. 462-466, 2011.

[49] S. Yuanfeng, Q. Jian, Y. Xueyi, R. Woogeun, P. Byeong-Ha, and W. Zhihua, "A Continuously Tunable Hybrid LC-VCO PLL With Mixed-Mode Dual-Path Control and Bi-level Delta-Sigma Modulated Coarse Tuning," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 58, pp. 2149-2158, 2011.