60GHz Integrated On-chip Antenna on Silicon for High Speed Applications

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Abstract

The recent release of the unlicensed 60 GHz band tackles the increasing demand for more bandwidth in the wireless consumer electronics market. In order to meet the cost requirements of this market, many research groups have worked towards 60 GHz front-end electronics in mainstream silicon technologies, i.e., CMOS and BiCMOS. However, the technology choice for suitable antennas has not been as unitary and is controversially discussed. While there is a wide consensus that the antenna should be integrated in the same package with the front-end integrated circuit (IC), there are three main approaches on the realization. First, there is the Antenna-in- Package approach, in which the antenna is implemented in the IC's packaging technology. Second, there is the Antenna-on-Chip approach, in which the antenna is directly implemented in the back-end of the IC. Finally, the third approach can be considered as a hybrid of Antenna-on-Chip and Antenna-in-Package, in which the feed-point of the antenna is implemented on-chip while the radiating element itself is realized off-chip.

This thesis focuses Antenna-on chip main integration strategies. Its goal is to explore the challenges and potentials of this technology with respect to millimeter-wave antenna integration. For this, integrated antenna concepts for the 60 GHz band are developed using mainstream technologies. This restriction is necessary in order to achieve cost-effective solutions for the highly price-competitive wireless consumer electronics market. The main challenge of antenna design in a planar technology is the trade-off between radiation efficiency and bandwidth. To obtain a large bandwidth, a relatively thick dielectric layer is needed. However, a thicker dielectric layer introduces more losses due to surface-wave excitation in the dielectric. Silicon with low resistivity substrates also introduce special challenges for high efficiency millimeter wave on-chip antennas. First, their low resistivity of 0.1-20 Ω-cm results in high dielectric loss and significantly reduces the antenna efficiency. Second, TE and TM surface waves are easily triggered in 200-500 μm thick silicon substrates and can have serious detrimental effects on the antenna pattern and efficiency. A lot of work has been done to improve the radiation efficiency of planar antennas while maintaining a large bandwidth. Particularly, the use of electromagnetic band gap (EBG)

materials that suppress the surface-wave excitation has received a lot of attention. However, EBG materials are either difficult to manufacture, or too large to be used in planar array configurations. Another approach to improve the radiation efficiency is presented in literatures, where a superstrate antenna is used. This solution shows good performance. But careful consideration reveals that most designs are not readily amenable to mass production and many purposed structures are very inefficient. Some designs which are efficient require extra process steps such as trenching. This extra process hinders to achieve truly low fabrication cost. The fabrication process should be fully compatible with current substrate processing technology.

To tackle these challenges, antenna on chip (AOC) structures, named virtual loop antenna (VLA) structures, were studied and utilized for low profile Si CMOS on-chip antenna design and realization. The concept proposed in this work avoids the extra steps but provides for comparable good antenna efficiency. We propose the design of this antenna for use on CMOS ICs technology that promises to integrate a complete 60GHz system on single chip that combines a good performance in both bandwidth and radiation efficiency. The resulting design is completely planar, and the use of vias is avoided. This result in inherently low fabrication cost, light weight, and low volume antenna. Its design is essentially a joint optimization of bandwidth and power efficiency. The design of this integrated loop antenna for use on 60GHz CMOS receivers was based on silicon substrates of low resistivity that varies from 5- 20Ω-cm. The design was based on intensive electromagnetic simulations using HFSS software package. The width and length of the antenna is less than half a free-space wavelength, such that the antenna can be readily used for the realization of a planar beam-forming array. The designed antenna was fabricated and the measurement results agree with those of simulation results

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Chapter 1 Introduction

1.1 Context and general background of the thesis

1.1.1 Societal context

The trend in the consumer electronics sector towards wireless products has led to numerous advancements in our everyday lives. The existence of a wireless local area network (WLAN) in a cafe, public building, or private home, for example, is often taken for granted. Similarly, the use of satellite navigation using the global positioning system (GPS) to get to a destination has largely substituted the use of printed maps. If none of the two options are available, one may still browse the internet for an online-map on a smartphone, or call a friend using a hands-free headset that is connected to a mobile phone via bluetooth. All those advancements, however, have also led to a congested microwave frequency spectrum, i.e., below 30 GHz. Future applications that require wireless high-data-rate communication in the Gb/s-range can, therefore, not be accommodated for in this frequency range due to an insufficient amount of available bandwidth. Hence, the consumer electronics industry has laid an eye on the millimeter-wave (mm-wave) spectrum, i.e., 30 GHz to 300 GHz. especially the unlicensed 60 GHz band with a large worldwide overlap seems an attractive option here, see, for example, [1, 2].

1.1.2 Brief review of 60 GHz wireless communication

The interest of the wireless consumer electronics industry in mm-wave frequencies is currently mainly focused on the 60 GHz band. Here, a large bandwidth of unlicensed spectrum is available worldwide, with a large frequency overlap between different countries and regions. In Europe, for example, the 60 GHz band covers all frequencies from 57 GHz up to 66 GHz, i.e., a bandwidth of 9 GHz, for which the European Telecommunications Standards Institute (ETSI) released a harmonized European standard in early 2012, see [3]. A nice overview of the regulations in other parts of the world can be found in [2].

Prior to those regulations, many researchers had already studied some possibilities and challenges for the development of wireless consumer products operating around 60 GHz, see, for example, [1, 2, 4, 5, 6, 7, 8]. Various application scenarios were mentioned in this respect. The three top applications according to [4] are high definition (HD) video streaming, file transfer, and wireless Gigabit Ethernet. Here, HD video streaming includes, for example, uncompressed video/audio streaming from a portable media player, laptop, or personal data assistant (PDA) to a HD television (HDTV) or projector. The file transfer scenario covers applications such as communication between a personal computer (PC) and a printer, a digital camera, or similar. A further possible application mentioned is a ”kiosk in a store” that sells audio and video contents by directly uploading the product to a customer’s portable device. In addition, the authors of [5] also envision a replacement of wired connections inside PCs by 60 GHz wireless interconnects.

In order for above stated applications to be successful, products have to be developed that can compete on the highly cost-driven consumer electronics market. Hence, from the technology perspective, standard low-cost fabrication processes are preferred. One of the early publications on the exploitation of the 60 GHz band for consumer applications, [1], already briefly discusses technologies for wireless front-ends in this respect. For the antenna in particular, an implementation into the semiconductor technology is suggested in order to avoid significant interconnection losses. For cost reasons, the author advises to use silicon-germanium based semiconductor technologies. Nowadays, there indeed seems to be a wide consensus among 60 GHz research groups that silicon- or silicon-germanium-based technologies, i.e., CMOS or BiCMOS, should be used for the electronics of the wireless front-end. This is, for example, also outlined by the authors of [6], published in 2009, who compare two different integration strategies for the antenna. They distinguish the Antenna-on-Chip (AoC) solutions, i.e., (Bi-) CMOS integrated antennas, from the Antenna-in-Package (AiP) solutions, i.e., antennas that are integrated in the package technology of the integrated circuit (IC). From this comparison, they conclude that on-chip antennas are less favorable than in-package antennas for 60 GHz applications. They support their conclusion with the argument that AoCs only achieve radiation efficiencies of less than 12 % unless non-main-

stream processing steps are added, which would increase the cost of the solution accordingly. In contrast, the authors of [5] claim only a year later that AoCs offer the cheapest solution and suggest that more research should be conducted in order to increase their gain values to meet those of their AiP counterparts.

1.1.3 Motivation

With respect to 60 GHz antennas it is commonly accepted that the antenna should be located as close as possible to the mm-wave front-end electronics in order to keep interconnect losses at a minimum. Here, ’close’ refers to the electrical distance of the antenna to the front-end IC, i.e., measured in terms of the operating wavelength. The free space wavelength, λ_0, at 60 GHz is 5 mm and, hence, the antenna should preferably be inside the IC package. Such an antenna is called an integrated antenna throughout this thesis. Moreover, since the considerations are limited to antennas for the mm-wave range, such an antenna is more specifically called integrated mm-wave antenna, whereas both expressions are interchangeable.

Although there is a wide consensus regarding the integration of the antennas, the choice for the integration technology does not appear to be as unitary, as outlined in the previous section. On one hand, one of the main reasons for this controversy can be found in the vast variety of process technologies in the semiconductor industry. Many ”classical” antenna engineers simply do not know or have no access to the full spectrum of semiconductor processes and, as a consequence, cannot exploit their full capabilities. Furthermore, IC processes have hardly ever been characterized with respect to antenna parameters, which poses difficulties for a proper antenna design. On the other hand, IC design engineers, who have good insights in various semiconductor process technologies, often do not have a very broad antenna-engineering background and, therefore, might not always come up with as well-designed integrated antenna solutions. An extreme example of such a questionable antenna design was published in [9], where an on-chip metallic patch over a ground plane is simultaneously used as a high-Q resonator, for which typically low losses are desired, and as an antenna, for which (radiation) loss and a low-Q behavior are key characteristics.

As a consequence of this technologically complex field of engineering, in which strict company confidentialities within the semiconductor industry pose additional difficulties in obtaining a thorough overview, two main opinions have emerged in the mm-wave society. First, there is the group of people that do not believe in a success of the AoC approach. Their opinion is largely motivated by the problems with the lossy silicon substrate and the associated low radiation efficiency. Furthermore, it is often argued that possible processing steps that would enhance the radiation efficiency are non-standard and, therefore, too expensive. On the contrary, the second major group is mostly searching for cost-effective alternative ways to improve the radiation behavior of on-chip antennas rather than excluding this approach once and for all. Their efforts are strongly supported by successfully integrated on-chip antenna designs in the terahertz band (0.3 THz - 3 THz) at which the AoC approach can be considered largely superior to the AiP approach, see, for example, [10].

The obvious question that arises from the above sketched controversy is the following: ”Which integration technology will ultimately be the best choice for mm-wave antennas in the consumer market?” For this, beside the two main integration approaches, a third concept can be distinguished and should also be taken into consideration. This third approach can be understood as a hybrid between AiP and AoC concept, which is further described in Chapter 3. Finally, another interesting question that needs to be answered is that of the frequency limits of the concepts, i.e., ”at what frequency range is the AiP, AoC, or hybrid solution superior to the other two approaches?”

1.2 Objectives, research approach and outline

The objective of this thesis is to answer above raised questions based on mainstream technologies. This is done in a unified approach by investigating the AiP, AoC, and hybrid integration approach in an equal manner. The general outline of this thesis, shown in Figure 1.1, adopts the structure of this research approach. First, a brief review of the most important aspects of electromagnetic theory and antenna modeling is provided in Chapter 2.

Antenna specifications for the 60 GHz band are then derived in Chapter 3, where also an overview of typical state-of-the-art antenna concepts for AiP, AoC, and hybrid solutions is given. Based on those studies, integrated mm-wave Virtual Loop antenna (VLA) on chip concepts were developed, which are presented in Chapters 4. Here, since this study is focused on the effect of the integration technology, basic antenna topologies were chosen for the investigations, i.e. loop antennas. In Chapter 5, the measurement setups that were used for the characterization of the antenna prototypes are described. Since, eventually, antenna arrays will be required for many mm-wave applications, respective considerations in this direction are summarized in Chapter 6. Finally, a comparison of all three antenna concepts with respect to their performance is also provided in Chapter 6, where also general conclusions and future works are drawn. Here, special emphasis is also laid on the suitability of the concepts for the major application areas as identified in [4, 5], i.e.

a) HD video streaming and wireless Gigabit Ethernet,

b) File transfer,

c) Wireless interconnects.

Note that the designated goal of this thesis is an assessment of those process technologies that are nowadays widely considered as standard for the consumer market. Therefore, the

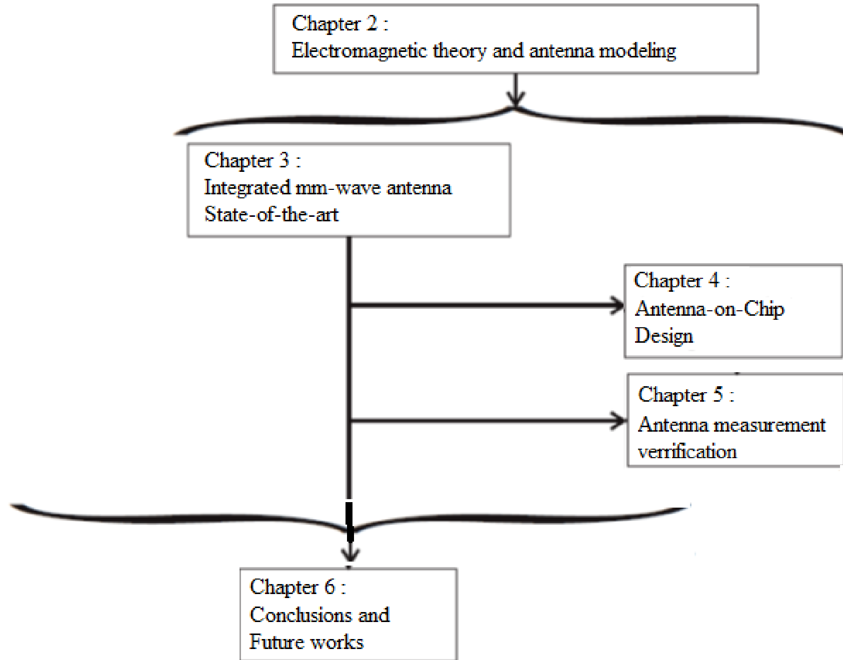


Fig.1.1 General outline of thesis

drawn conclusions reflect the general requirements of this market and exclude antenna designs in more advanced or more costly technologies. For example, the considerations are limited to silicon-based IC technologies. There are, however, also research groups that focus on, for example, gallium-arsenide based IC processes. Due to the typically much lower losses in those semiconductor substrates, on chip antennas with significantly higher efficiencies could be accomplished. Gallium arsenide is more expensive than silicon, however, and, therefore, those solutions are generally considered as less competitive on the consumer electronics market.

1.3 Contribution of thesis

The main challenge of antenna design in a planar technology is the trade-off between radiation efficiency and bandwidth. To obtain a large bandwidth, a relatively thick dielectric layer is needed [56]. However, a thicker dielectric layer introduces more losses due to surface-wave excitation in the dielectric. A lot of work has been done to improve the radiation efficiency of planar antennas while maintaining a large bandwidth [57, 58]. Particularly, the use of electromagnetic band gap (EBG) materials that suppress the surface-wave excitation has received a lot of attention [59, 60, 61]. However, EBG materials are either difficult to manufacture, or too large to be used in planar array configurations. Another approach to improve the radiation efficiency is presented in [62], where a superstrate antenna is used. This solution shows good performance, but is more complicated to realize, since the superstrate antenna is a separate component that has to be placed partly on top of the integrated circuit. As an alternative, a virtual loop antenna (VLA) is proposed here.. The concept proposed in this work avoids the extra steps but provides for good antenna efficiency. We propose the design of this antenna for use on CMOS ICs technology that promises to integrate a complete 60GHz system on single chip that combines a good performance in both bandwidth and radiation efficiency. The design is based on assumptions that conductor and conductive pad are imaged in ground plane to form a loop antenna. The resulting design is completely planar, and the use of via is avoided. This result in inherently low fabrication cost, light weight, and low volume antenna. Its design is essentially a joint optimization of bandwidth and power efficiency. The design of this integrated loop antenna

for use on 60GHz CMOS receivers was based on silicon substrates of low resistivity that varies from 5- 20Ω-cm. The design was based on intensive electromagnetic simulations using HFSS software package. The width and length of the antenna is less than half a free-space wavelength, such that the antenna can be readily used for the realization of a planar beam-forming array.

Chapter 2

Electromagnetic theory and antenna modeling

The multidisciplinary field of integrated mm-wave antennas caught the attention of not only the antenna society but also, for example, of the solid-state circuits and electron devices societies. Since the latter two do not naturally deal directly with antenna problems, it is meaningful to summarize some basic principles of antenna theory that are essential for the understanding of the remainder of this thesis. For this, a brief review of basic electromagnetic theory is first of all given in Section 2.1. Here, a link is also made between a substrate's electric resistivity, which is a commonly used parameter in the semiconductor industry, and the material's loss tangent, which is used in general microwave engineering. Due to their importance for developed integrated mm-wave antenna concepts, some basic properties of confined substrate modes and their respective cut-off frequencies are also presented in this section. An overview of Full-wave Electromagnetic Field Simulation software (HFSS) that was used for the solution of electromagnetic problems throughout this thesis is then given in Section 2.2, followed by a review of important antenna parameters in Section 2.3. These above described theoretical foundations are put into practice by the technique of image theory for a virtual loop antenna which also plays a major role for the modeling approach of the integrated antenna concept in Chapter 4.

2.1 Electromagnetic fields in dielectric media

2.1.1 The Maxwell equations

The relation between electromagnetic fields and their electric and magnetic sources is given by Maxwell's equations,

$$\nabla \times \vec{H} = \frac{\partial \vec{D}(\vec{r})}{\partial t} + \vec{J}(\vec{r}) \qquad (2.1)$$

$$\nabla \times \vec{E}(\vec{r}) = -\frac{\partial \vec{B}(\vec{r})}{\partial t} - \vec{M}(\vec{r}) \qquad (2.2)$$

$$\nabla \cdot \vec{D}((\vec{r})) = \rho_e(\vec{r}) \quad (2.3)$$

$$\nabla \cdot \vec{B}(\vec{r}) = 0 \quad (2.4)$$

with the magnetic field strength $\vec{H}(\vec{r})$, the electric field strength $\vec{E}(\vec{r})$, and the electric-flux density and magnetic-flux density $\vec{D}(\vec{r})$ and $\vec{B}(\vec{r})$, respectively. Furthermore, $\rho_e(\vec{r})$ describes the electric charge density, $\vec{J}(\vec{r})$ the electric, and $\vec{M}(\vec{r})$ the magnetic1 current densities, see, for example, [11]. The coordinate vector to the observation point is denoted by $\vec{r}$. Assuming harmonic time dependence, i.e., all field quantities are proportional to $e^{j\omega t}$, where t is the time and ω is the angular frequency, (2.1) to (2.4) can be written as

$$\nabla \times \vec{H}(\vec{r}) = j\omega\vec{D}(\vec{r}) + \vec{J}(\vec{r}) \quad (2.5)$$

$$\nabla \times \vec{E}(\vec{r}) = -j\omega\vec{B}(\vec{r}) - \vec{M}(\vec{r}) \quad (2.6)$$

$$\nabla \cdot \vec{D}(\vec{r}) = \rho_e(\vec{r}) \quad (2.7)$$

$$\nabla \cdot \vec{B}(\vec{r}) = 0 \quad (2.8)$$

For homogeneous and isotropic media, the relation between the electric-flux density and electric field strength as well as the relation between the magnetic-flux density and the magnetic field strength is given by the following constitutive relations:

$$\vec{D}(\vec{r}) = \epsilon\vec{E}(\vec{r}) = \epsilon_o\epsilon_r\vec{E}(\vec{r}) \quad (2.9)$$

$$\vec{B}(\vec{r}) = \mu\vec{H}(\vec{r}) = \mu_o\mu_r\vec{H}(\vec{r}) \quad (2.10)$$

With $\epsilon_0 = 8.854 \times 10^{-12} As/Vm$ the permittivity and the permeability of $\mu_0 = 4\pi \times 4\pi^{-7} Vs/Am$ vacuum, respectively. The factors

$$\epsilon_r = \epsilon_r' - j\epsilon_r'' \quad (2.11)$$

$$\mu_r = \mu_r' - j\mu_r'' \quad (2.12)$$

denote the relative permittivity and relative permeability of the medium with respect to vacuum. Both factors are, therefore, dimensionless. In particular, for most dielectric media it holds that $\boldsymbol{\mu_r = 1}$. In case of an infinite resistivity of the medium, $\boldsymbol{\epsilon_r''}$ accounts for polarization losses, i.e., damping of the vibrating dipole moments in the material, see [13]. Instead of stating the imaginary value, however, material suppliers usually characterize the losses of a dielectric by its loss tangent, defined as

$$\tan(\delta) = \frac{\epsilon_r''}{\epsilon_r'} \qquad (2.13)$$

2.1.2 Effect of finite electric resistivity

For a medium that exhibits an electric resistivity ρ, the electric-current density in Equation (2.5) can be decomposed in two parts, i.e.

$$\vec{J}(\vec{r}) = \vec{J}_{conduct}(\vec{r}) + \vec{J}_{imposed}(\vec{r}) \qquad (2.14)$$

see [11]. The first component is the conduction current density,

$$\vec{J}_{conduct}(\vec{r}) = \frac{\vec{E}(\vec{r})}{\rho} \qquad (2.15)$$

which describes the current due to an electric field strength acting on the conductive medium. The other term in Equation (2.14), $\vec{J}_{impsed}$ is the imposed current density and represents a source term of the electromagnetic fields.

Equation (2.5) for homogeneous and isotropic media can be re-written with the aid of Equations (2.9), (2.11), (2.14), and (2.15) to

$$\nabla \times \vec{H}(r) = j\omega\epsilon_o\left(\epsilon_r' - j\epsilon_r'' - j\frac{1}{\rho\omega\epsilon_o}\right)\vec{E}(\vec{r}) + \vec{J}_{imposed} \qquad (2.16)$$

Hence, the electric resistivity contributes as ohmic losses to the imaginary part of the relative permittivity, i.e.

$$\boldsymbol{\epsilon_r = \epsilon_r' - j\left(\epsilon_r'' + \frac{1}{\rho\omega\epsilon_o}\right) = \epsilon_r' - j\tilde{\epsilon}_r''} \qquad (2.17)$$

and has the same effect as polarization losses. Since both loss mechanisms are indistinguishable, see [13], the loss tangent (2.13) for materials with finite resistivity is given by

$$\boldsymbol{\tan(\delta) = \frac{\tilde{\epsilon}_r''}{\epsilon_r'} = \frac{\rho\omega\epsilon_o\epsilon_r'' + 1}{\rho\omega\epsilon_0\epsilon_1'}} \qquad (2.18)$$

As an example, Figure 2.1 provides the relation between the resistivity of a doped silicon substrate with $\boldsymbol{\epsilon_r' = 11.9}$ and its resulting loss tangent at 60 GHz under the assumption of low polarization losses, i.e. ,$\boldsymbol{\epsilon_r'' = 0}$.

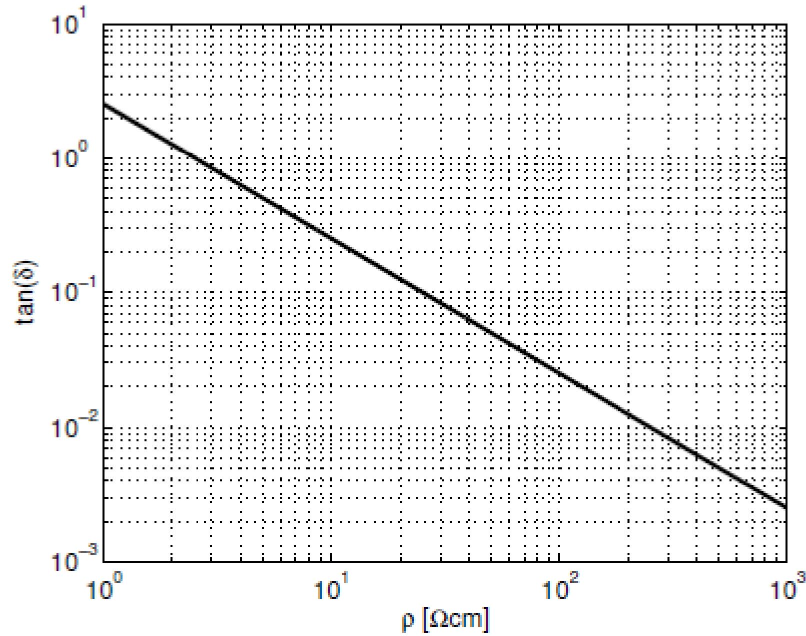


Figure 2.1. Relation between the resistivity, ρ, of a doped silicon substrate with $\epsilon_r' = 11.9$ and its resulting loss tangent at 60 GHz (low polarization losses assumed, i.e. $\epsilon_r'' = 0$).

Finally, since the resistivity can be considered as part of the relative permittivity of a medium, the term $\vec{\boldsymbol{J}}(\vec{\boldsymbol{r}})$ implies the imposed current density $\vec{\boldsymbol{J}}_{\boldsymbol{imposed}}(\vec{\boldsymbol{r}})$ only throughout the remainder of this thesis.

2.1.3 Vector potentials

As mentioned in [14], it is possible to calculate the electromagnetic fields directly from the source term $\vec{\boldsymbol{J}}(\vec{\boldsymbol{r}})$, but it is often much simpler to calculate the fields from auxiliary functions, known as vector potentials. The two most commonly used vector potentials are the magnetic vector potential, $\vec{\boldsymbol{A}}(\vec{\boldsymbol{r}})$, and the electric vector potential, $\vec{\boldsymbol{F}}(\vec{\boldsymbol{r}})$. The following paragraph summarizes the derivation of the magnetic vector potential under the assumption that only electric currents are present, i.e. $\vec{\boldsymbol{M}}(\vec{\boldsymbol{r}}) = \boldsymbol{0}$, and that the medium is homogeneous and isotropic.

The magnetic field is solenoidal, i.e.

$$\boldsymbol{\nabla} \cdot \vec{\boldsymbol{H}}(\vec{\boldsymbol{r}}) = \boldsymbol{0} \qquad (\boldsymbol{2.19})$$

Therefore, the magnetic field can be represented as the curl of a vector field,

$$\vec{\boldsymbol{H}}(\vec{\boldsymbol{r}}) = \boldsymbol{\nabla} \times \vec{\boldsymbol{A}}(\vec{\boldsymbol{r}}) \qquad (\boldsymbol{2.20})$$

with $\vec{\boldsymbol{A}}(\vec{\boldsymbol{r}})$ the magnetic vector potential. Using this result and Equation (2.10) in (2.6) yields

$$\boldsymbol{\nabla} \times \left(\vec{\boldsymbol{E}}(\vec{\boldsymbol{r}}) + \boldsymbol{j\omega\mu}\vec{\boldsymbol{A}}(\vec{\boldsymbol{r}})\right) = \boldsymbol{0} \qquad (\boldsymbol{2.21})$$

This implies that the vector field, given by $\left(\vec{\boldsymbol{E}}(\vec{\boldsymbol{r}}) + \boldsymbol{j\omega\mu}\vec{\boldsymbol{A}}(\vec{\boldsymbol{r}})\right)$, is irrotational and can therefore be represented by the gradient of a scalar field $\boldsymbol{\Phi}(\vec{\boldsymbol{r}})$, i.e.

$$\vec{E}(\vec{r}) + j\omega\mu\vec{A}(\vec{r}) = -\nabla\Phi(\vec{r}) \quad (2.22)$$

Using this result, Equation (2.10), and (2.9) in (2.5) results in

$$\nabla \times \nabla \times \vec{A}(\vec{r}) - k^2\vec{A}(\vec{r}) = -j\omega\epsilon\nabla\Phi(\vec{r}) + \vec{J}(\vec{r}) \quad (2.23)$$

where $k = \omega\sqrt{\varepsilon\mu}$ is the wave number of the medium. This equation can be re-written using the Laplace operator, defined as

$$\nabla^2\vec{A}(\vec{r}) = \nabla\nabla \cdot \vec{A}(\vec{r}) - \nabla \times \nabla \times \vec{A}(\vec{r}) \quad (2.24)$$

to arrive at

$$\nabla^2\vec{A}(\vec{r}) + k^2\vec{A}(\vec{r}) = \nabla\left(j\omega\epsilon\Phi(\vec{r}) + \nabla \cdot \vec{A}(\vec{r})\right) - \vec{J}(\vec{r}) \quad (2.25)$$

The scalar function Φ(r) can be freely chosen and is set to satisfy

$$j\omega\varepsilon\Phi(\vec{r}) = -\nabla \cdot \vec{A}(\vec{r}) \quad (2.26)$$

in order to simplify Equation (2.25) to the vectorial Helmholtz-equation

$$\nabla^2\vec{A}(\vec{r}) + k^2\vec{A}(\vec{r}) = -\vec{J}(\vec{r}) \quad (2.27)$$

Equation (2.26) is known as the Lorentz gauge. It can be shown that the solution of (2.27) is generally given by

$$\vec{A}(\vec{r}) = \frac{1}{4\pi}\iiint \frac{\vec{J}(\vec{r}')}{R(\vec{r}-\vec{r}')} e^{-jkR(\vec{r}-\vec{r}')} dV' \quad (2.28)$$

in which $\vec{r}'$ denotes the coordinate vector to a source point, V' the volume that contains the source points, $\vec{r}$ the coordinate vector to an observation point, and $R(\vec{r}-\vec{r}') = |\vec{r}-\vec{r}'|$denotes the distance between source and observation point, see also [14]. Note that the kernel of (2.28) exhibits a singularity at $\vec{r} = \vec{r}'$, which poses a challenge for the exact evaluation of the integral. After the magnetic vector potential is calculated, the magnetic

field strength in an observation point can be computed by Equation (2.10). The electric field strengths can be obtained from

$$\vec{E}(\vec{r}) = \frac{1}{j\omega\epsilon}\left(k^2\vec{A}(\vec{r}) + \nabla\nabla\cdot\vec{A}(\vec{r})\right) \quad (2.29)$$

where Equation (2.16) was used in conjunction with Equation (2.11).

Similarly, the electric vector potential can be derived from the magnetic current distribution $\vec{M}(\vec{r})$. For this, only magnetic current densities are considered, i.e., $\vec{J}(\vec{r}) = 0$ The result for the electric vector potential is then given by

$$\vec{F}(\vec{r}) = \frac{1}{4\pi}\iiint \frac{\vec{M}(\vec{r}')}{R(\vec{r}-\vec{r}')} e^{-jkR(\vec{r}-\vec{r}')} dV' \quad (2.30)$$

From this, the electric and magnetic fields can be determined by equating

$$\vec{E}(\vec{r}) = -\nabla \times \vec{F}(\vec{r}) \quad (2.31)$$

And

$$\vec{H}(\vec{r}) = \frac{1}{j\omega\mu}\left(k^2\vec{F}(\vec{r}) + \nabla\nabla\cdot\vec{F}(\vec{r})\right) \quad (2.32)$$

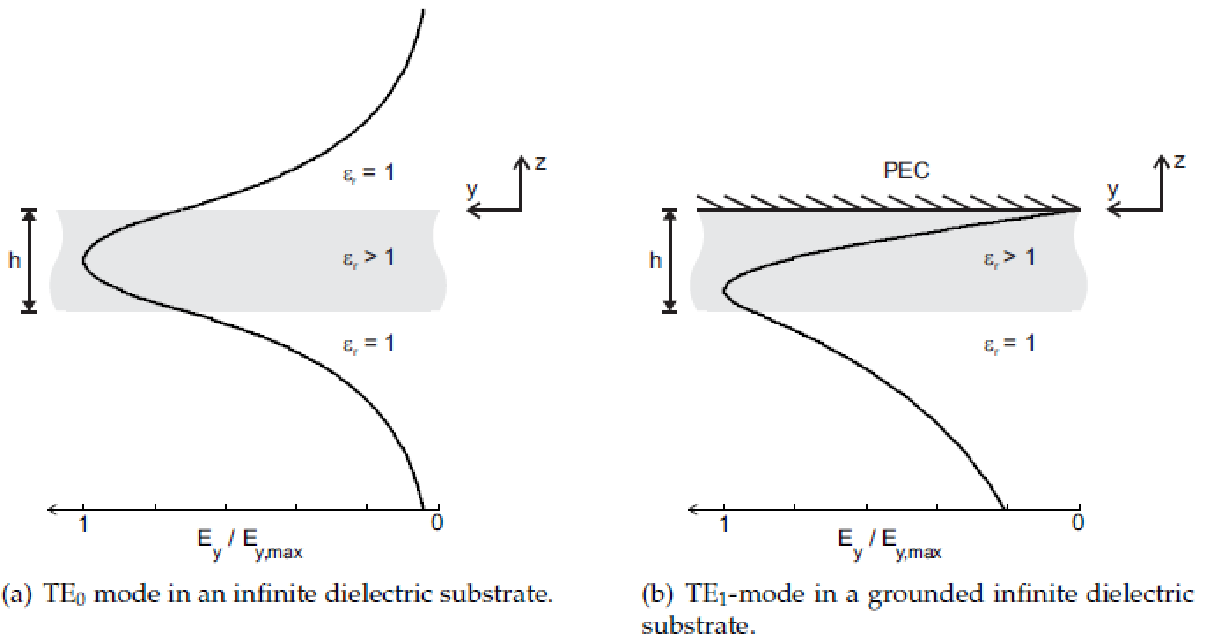
respectively.

2.1.4 Confined substrate modes

The integrated mm-wave concepts that are presented in this thesis are directly located on top of dielectric substrates. As explained in [11, 15], a dielectric substrate can confine and guide electromagnetic energy. Since this mechanism is often unwanted and can pose additional challenges to an antenna design, it is important to understand under what circumstances this can occur. As explained in [11], the confinement of the electromagnetic energy inside an infinite substrate is due to total reflections at its top and bottom surface. Those reflections result in a standing wave pattern inside the substrate as shown in Figure 2.2(a).

As known from basic electromagnetic theory, a total reflection at a dielectric interface results in an evanescent field on the opposite side of the interface, see, for example, [13]. Therefore, the shown electric field strength in Figure 2.1(a) decays exponentially for $z < -h$ and $z > 0$. The amount of confined energy inside the slab depends on its thickness, h, its permittivity, ε, as well as the permittivity of the surrounding medium, usually air. The fields inside the substrate can be subdivided into two fundamentally different field configurations, namely transverse-electric (TE) and transverse-magnetic (TM), with transverse referring to the orientation of the electric and magnetic field vectors with respect to the direction of propagation. For both cases, TE and TM propagation, several modes can exist in the substrate. The lower cut-off frequencies for those modes are given by [15] as

$$\boldsymbol{f_c = \frac{nc_o}{2h\sqrt{\epsilon_r' - 1}}}, \qquad (2.33)$$



(a) TE_0 mode in an infinite dielectric substrate.

(b) TE_1-mode in a grounded infinite dielectric substrate.

Figure 2.2.Examples of electric field distributions inside infinite silicon substrates of thickness h.

with n the mode number, c_0 the speed of light in vacuum, h the thickness, and ε_r the relative permittivity of the substrate. The modes are then named as TMn and TEn, respectively. A striking characteristic of the TM_0 and TE_0 mode is that their cut-off frequency is 0 Hz, i.e., they can always propagate.

Another important configuration that shall be considered here is the case in which the substrate is covered with a metallic plate as shown for the lowest order TE-mode in Figure 2.1(b). Here, the tangential electric field at the top surface has to be zero at all times. The cut-off frequencies of this configuration are given by [15] as

$$\boldsymbol{f_c = \frac{nc_o}{4h\sqrt{\epsilon_r' - 1}}} \qquad (2.34)$$

with $\boldsymbol{n = 0, 2, 4,...}$ for the TM modes and $\boldsymbol{n = 1, 3, 5,...}$ for the TE modes. Hence, the lowest-order TE mode has a non-zero cut-off frequency for this configuration.

2.2 Overview of full-wave electromagnetic field simulations

Analytical closed form solutions to the wave equation are only available for simple radiating structures. The accurate calculation of fields for more complex radiating structures, such as planar antennas, requires Maxwell's equations to be solved numerically. Commercially available full-wave solvers are based on the finite element method (FEM), finite difference (FD) method, finite integration (FI) method and the method of moments (MoM) in both time and frequency domains [16, 17]. The solver used in this work is based on the FEM in the frequency domain, which is implemented in the commercially available software suite High Frequency Structure Simulator (HFSS™) from Tansy's (formerly Ansoft). The FEM in the frequency domain solves the inhomogeneous vector wave equation for the electric field obtained from substituting the first two of Maxwell's equations (1) and (2) assuming time harmonic fields.

$$\boldsymbol{\vec{\nabla} \times \left[\frac{1}{\mu}\,\vec{\nabla} \times \vec{E}\right] - j\omega\vec{E} + j\omega\vec{J} = 0} \qquad (2.35)$$

The material constants can be set complex to account for dielectric and magnetic losses. The matrix equation is derived such that the residual is minimized for the entire domain. For this purpose, (2.35) is multiplied with a vector weighting function $\boldsymbol{\vec{G}_i}$ and integrated over the entire domain $\boldsymbol{V}$ to form the weighted residual equation $\boldsymbol{F(\vec{E})}$.

$$F(\vec{E}) = \iiint \left(\vec{\nabla} \times \left(\frac{1}{\mu}\vec{\nabla} \times \vec{E}\right) - j\omega\vec{E} + j\omega\vec{J}\right)\vec{G}_t dV = 0 \qquad (2.36)$$

Commonly tetrahedral elements $T_k$are used as finite elements to discretize the computation domain because they can be naturally fitted to many geometrical shapes. The interpolating functions $\vec{N}_n^k$ for each finite element T_k are chosen so that the electric field inside the element can be described.

$$\vec{E}^k = \sum_{n=1}^{6} \vec{N}_n^k \vec{E}_n^k \qquad (2.37)$$

n references the edges of the tetrahedron, which are connected through the four vertices. Two and three tangential components of the electric field are stored at the edges and vertices, respectively, yielding a total of 24 complex values per tetrahedron.

Antennas are considered an open boundary problem. Solving differential equations, however, requires the specification of boundary conditions. Reflection-free truncation of the computation volume is an inevitable measure to reduce the computational cost that would be necessary to simulate an open boundary problem with conventional boundary conditions such as perfect electric conductor (PEC) or perfect magnetic conductor (PMC) boundaries. These enforce surfaces with a reflection coefficient of 100%. They would have to be placed at a large distance away from the radiating structure to ensure that the reflected wave is attenuated enough to not disrupt the field configuration of the simulated structure. Therefore, a perfectly matched boundary condition (PML) is implemented in FEM solvers to provide reflection-free terminations of the computation volume. The complex anisotropic material of the PML is chosen to ensure reflection-free matching of the PML to the free space impedance for all incident angles, polarizations and frequencies [18].

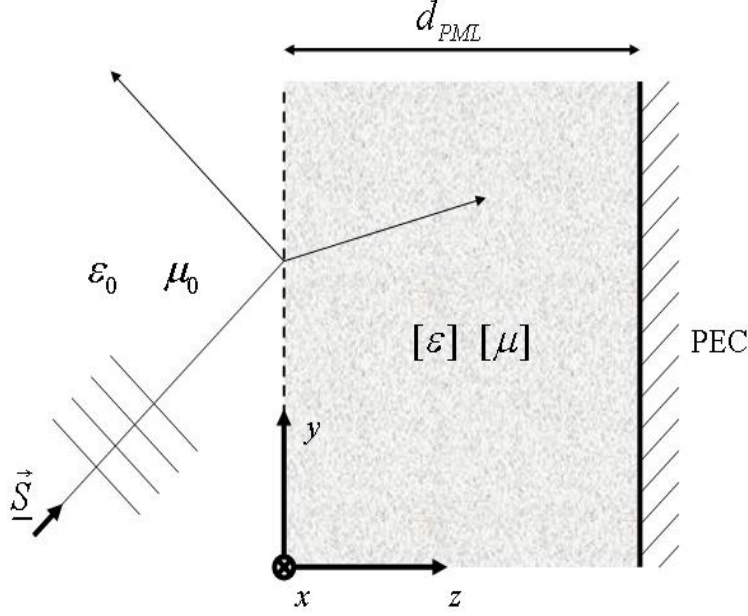


Fig. 2.3: Concept of PML boundary conditions at the sides of the computational domain to provide low reflections absorbing boundaries

A PML configuration is matched to a vacuum with the matching condition:

$$\frac{\boldsymbol{\mu_o}}{\boldsymbol{\varepsilon_o}} = \frac{[\boldsymbol{\mu}]}{[\boldsymbol{\varepsilon}]} \tag{2.38}$$

The anisotropy of the permeability and permittivity are described with tensors, $[\mu]$ and $[\varepsilon]$, in order to ensure impedance matching and attenuation in z direction.

$$[\boldsymbol{\varepsilon}] = \boldsymbol{\varepsilon_o}[\Lambda] \tag{2.39}$$

$$[\boldsymbol{\mu}] = \boldsymbol{\mu_o}[\Lambda] \tag{2.40}$$

The tensor entries must obey the following condition,

$$[\Lambda] = \begin{bmatrix} \boldsymbol{s} & \boldsymbol{0} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{s} & \boldsymbol{0} \\ \boldsymbol{0} & \boldsymbol{0} & \boldsymbol{s^{-1}} \end{bmatrix} \tag{2.41}$$

Furthermore, the entries are complex to ensure attenuation

$$\boldsymbol{s} = \boldsymbol{a} - \boldsymbol{jb} \tag{2.42}$$

The imaginary part b is used to model the electric and magnetic conductivities i.e., the losses, and the real part a models the phase of the wave propagation in the PML. The PMLs are truncated by either PECs or PMCs and must be thick enough to ensure high attenuation

of the reflected wave. It is interesting to note that the imaginary parts of the *z* components of the above tensors are negative (different leading sign to the *x* and *y* components) implying the existence of electric $-k_e E_z$and magnetic $-k_m H_z$sources within the PML materials.

The radiating structure is surrounded by a 3D box. Additional PML edge elements are introduced at the edges and sides to ensure a complete reflection-free outer box surface. The impedance matching condition (2.38) is also applied to these elements. Figure 2.4 shows a possible 2D configuration comprising one corner element.

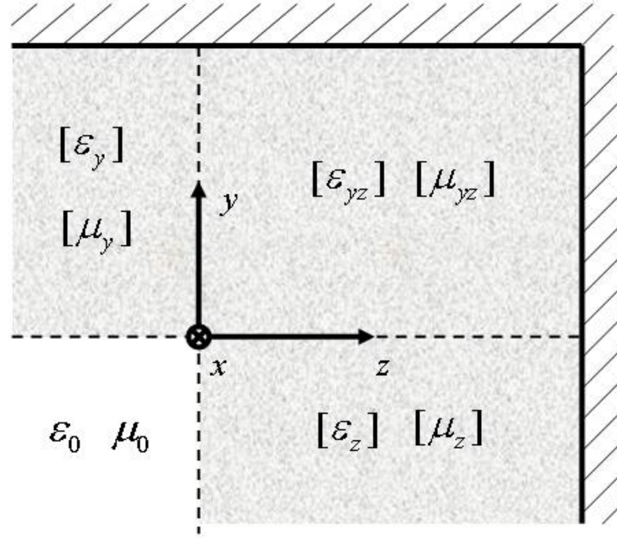


Figure 2.4: Concept of PML edge elements at the corner of the box.

High frequency models are excited by applying an exciting field distribution somewhere inside or on the surface of the computation domain. For practical applications the excitation (source) is a microstrip or coaxial mode on a transmission line. Since these modes are boundary conditions for the source regions, they must be computed before the field distribution inside the computational volume is solved. In the frequency domain, a harmonic time dependency is assumed. The electric field pattern for mode *n* is described as: $\sim e^{jwt}$ is assumed. The electric field pattern for mode *n* is described as:

$$\vec{E}_n(x, y, z, \omega) = \vec{E}_n(x, y) e^{-\alpha z - j\beta z} \quad (2.43)$$

The computation of the S-parameters requires an accurate determination of the time averaged power density $\vec{S}(x, y, z)$ propagating in and out of the port for each desired mode.

Hence, a high accuracy of the 2D port field solution $\vec{E}_n(x, y)$ is vital. The time averaged total complex power *P* of the mode can be evaluated at the cross section of the port.

$$\boldsymbol{P} = \iint \vec{\boldsymbol{S}}(\boldsymbol{x}, \boldsymbol{y}, \boldsymbol{z} = \boldsymbol{z_o})\, \boldsymbol{dxdy} \tag{2.44}$$

Concerning the stability of the computed field solution of the FEM, an adaptive mesh refinement is employed in the field solver. The simulation process is divided into a number of steps. First, a geometrical model of the antenna is set up with the 3D modeler. Material parameters, boundaries and excitations are defined. A solution setup is created with a solution frequency corresponding to the expected resonance frequency of the antenna. Next, a frequency sweep is defined covering the entire frequency range of analysis.

After the simulation is started, the field patterns that exist on the defined cross section of the ports are solved with a 2D full-wave solver. These patterns are used as boundary conditions for the excitation. Then the initial mesh is seeded in the computational domain and the field quantities and S-parameters are computed when the structure is excited with the solution frequency. To obtain a stable solution, the mesh is refined, and the solution is computed again. The maximum change ΔS is calculated:

$$\Delta \boldsymbol{S} = \boldsymbol{max}\left[\left(\boldsymbol{S}_{ij}^{N} - \boldsymbol{S}_{ij}^{N-1}\right)\right] \tag{2.45}$$

From here on, the mesh is refined after each pass until a convergence criterion is met. Once a stable solution is found, the sweep is executed, which extrapolates the field solution at the solution frequency over the desired frequency range.

2.3 Antenna parameters

2.3.1 Field regions

The space around an antenna can be subdivided into three regions, see [14]. The direct vicinity of the antenna, called the reactive near-field region, is electromagnetically dominated by the reactive fields of the antenna. This region exists until approximately $0.63\sqrt{D^3/\lambda_0}$ from the antenna surface, where λ_0 is the considered wavelength and D is the largest dimension of the antenna. The region between this boundary and up to a distance

of approximately $2D^2/\lambda_0$ is called the radiating near-field or Fresnel region. Here, the radiating fields predominate, but the angular field distribution depends on the distance from the antenna. As stated in [14], this region may not exist for antennas whose largest dimension D is not large as compared to the wavelength. The region beyond the $2D^2/\lambda_0$-boundary is called the far-field or Fraunhofer region at which the angular field distribution is essentially independent of the distance from the antenna.

2.3.2 Input impedance and radiation efficiency

From a circuit point of view, an antenna can be described, just as any other load, by means of an impedance

$$\boldsymbol{Z_{ant}(f) = R_{ant}(f) + jX_{ant}(f)} \qquad (2.46)$$

or, alternatively, as an admittance

$$\boldsymbol{Y_{ant}(f) = G_{ant}(f) + jB_{ant}(f)} \qquad (2.47)$$

where both the imaginary as well as the real part are a function of the frequency f. From an electromagnetic perspective, the imaginary part of the antenna impedance (or admittance) is determined by the reactive fields of the antenna and, thus, by its near-field. The resistive part of the impedance can be split into two different components,

$$\boldsymbol{R_{ant} = R_{rad} + R_{loss}} \qquad (2.48)$$

with the radiation resistance R_{rad} and the loss resistance R_{loss} of the antenna. For a loss mechanism in parallel, the admittance model can more easily be used, with

$$\boldsymbol{G_{ant} = G_{rad} + G_{loss}} \qquad (2.49)$$

Here, R_{rad} and G_{rad} are associated with the power loss due to radiation and can, therefore, be linked to the far-field of the antenna. R_{loss} , and G_{loss} then describe the conductor and dielectric losses inside the antenna.

Since antennas obviously exhibit undesired losses, the radiation efficiency of an antenna, defined as the ratio of the radiated power to the input power, see [11], is a vital performance parameter. From the lumped antenna models (2.46) and (2.47) in combination with (2.48) and (2.49), respectively, the radiation efficiency of the antenna can be calculated according to

$$\eta_{rad} = \frac{P_{rad}}{P_{in}} = \frac{R_{rad}}{R_{rad} + R_{loss}} \tag{2.50}$$

Note that Equations (2.50) exclude losses due to a mismatch between the source, for example an amplifier, and the antenna. Therefore, the radiation efficiency is a circuit independent parameter, which makes it an ideal figure of merit for the comparison of antenna concepts in different technologies and with different input impedance specifications. Hence, it plays an important role in the antenna concept chapter 4.

2.3.3 Gain, polarization, and radiation pattern

In most cases, a communication antenna is used to bridge larger distances. Therefore, the radiation properties of an antenna as seen from its far-field are of major importance. For example, it is crucial to know the directional properties of an antenna, like

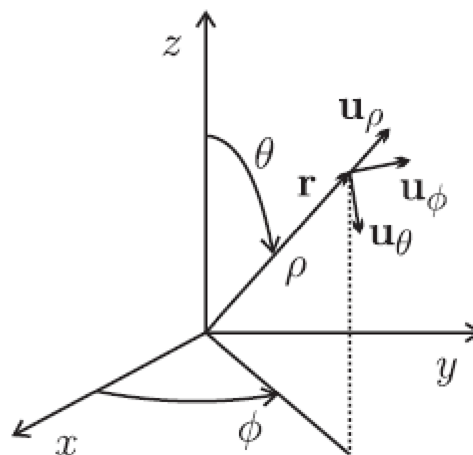


Figure 2.5. Definition of spherical coordinates.

the amount of power radiated into each direction, i.e., with respect to θ and ϕ of a spherical coordinate system as shown in Figure 2.5. For this, an isotropic radiator is considered as starting point here. Such a (hypothetical) antenna radiates the same amount of power in all directions. Thus, one can determine its radiation intensity U, defined as the radiated power per unit solid angle, simply by

$$\boldsymbol{U_0 = \frac{P_{rad}}{4\pi}} \qquad (2.51)$$

In the general case, however, the radiation intensity of an antenna is a function of direction, i.e., $U = f(\theta, \phi)$, for which the following relation always holds:

$$\boldsymbol{P_{rad} = \int_0^{2\pi} \int_0^{\pi} U(\theta, \Phi) \sin(\theta)\, d\theta\, d\Phi} \qquad (2.52)$$

Equation (2.51) simply states that the integration of the radiation intensity over all directions is equal to the total radiated power. Usually, $U = f(\theta, \phi)$, of a considered antenna is described with respect to the isotropic radiator, i.e.

$$\boldsymbol{D(\theta, \Phi) = \frac{U(\theta, \Phi)}{U_0} = \frac{4\pi U(\theta, \Phi)}{P_{rad}}} \qquad (2.53)$$

where D is known as the directivity of the antenna. This relation, however, excludes any antenna losses since only the radiated power is considered. In practice, one is usually more interested in the amount of power that is radiated in a certain direction with respect to the total input power. For this, the radiation efficiency, defined in (2.50), can be used to obtain the gain of the antenna,

$$\boldsymbol{G(\theta, \Phi) = \eta_{rad} \frac{U(\theta, \Phi)}{U_0} = \eta_{rad} D(\theta, \Phi)} \qquad (2.54)$$

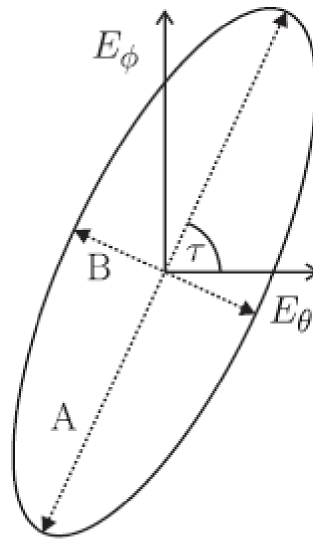


Figure 2.6. General polarization ellipse.

where it is assumed that the isotropic radiator does not exhibit any losses.

Another important far-field parameter is the polarization of an antenna, which is defined as the polarization of its radiated wave along its direction of propagation. Here, the polarization of an electromagnetic wave is further defined as the time-dependent direction and relative magnitude of the electric-field vector. Since the polarization of the radiated wave might vary with the observation direction, the polarization is usually taken to be in the direction of maximum gain, see [14]. Note, however, that although antennas are designed to radiate in a specified polarization, they always also radiate a certain amount of power in the orthogonal polarization. The component of the field that is radiated in the intended polarization is commonly referred to as co-polarization component and the orthogonal component is then referred to as cross-polarization component. A fundamental article on the possible different definitions of co- and cross-polarization was published by A.C. Ludwig in 1973, see [19]. In the outline of this thesis, however, both components coincide with either the θ or ϕ direction of the observation coordinate system, respectively. They are denoted accordingly, such that no further elaboration on this topic shall be undertaken here.

Moreover, in the far-field of an antenna, its radiated electromagnetic wave can be split into two orthogonal components, which superimpose to a general polarization ellipse as shown in Figure 2.6. For such an ellipse, the axial ratio (AR),

$$\boldsymbol{AR = \frac{A}{B} = \frac{\left|\vec{E}_\theta u_\theta + \vec{E}_\Phi u_\Phi\right|_{max}}{\left|E_\theta u_\theta + \vec{E}_\Phi u_\Phi\right|_{min}}} \tag{2.55}$$

can be defined, which indicates whether the wave is mainly linearly, elliptically, or circularly polarized. For a perfectly linearly polarized antenna, for example, the axial ratio (2.55) is infinite. For a perfectly circularly polarized antenna, the axial ratio is AR = 1. This case is of particular importance for the array considerations in Chapter 4.

Finally, the radiation characteristics of an antenna as a function of space coordinates are often represented in a plot, known as radiation pattern. If the gain of an antenna is shown, one also denotes it as power pattern since it describes the radiated power per unit solid angle. A power pattern could, however, also show the directivity or radiation intensity and is, therefore, not uniquely defined. Therefore, throughout this thesis the term gain pattern is used to indicate that the gain of the antenna is shown. Furthermore, radiation patterns are often normalized with respect to its maximum value, which is then denoted as normalized radiation pattern. In this thesis, these patterns are accordingly referred to as normalized gain patterns. Since the gain can be independently determined for co-polarization and cross-polarization components, the radiation patterns might show the results for one of the two polarizations only. If nothing is mentioned, however, the gain pattern is taken to be the absolute gain of the antenna in that direction. Furthermore, for linearly-polarized antennas it is common practice to limit the patterns to their two principle planes, i.e., E-plane and H-plane. In general, the E-plane is defined as the plane containing the electric field vector and the direction of maximum radiation. The H-plane is defined accordingly for the magnetic field vector and, since in the far-field the electric and magnetic field vectors are orthogonal to each other, the H-plane is orthogonal to the E-plane.

2.3.4 Friis transmission equation

Figure 2.7 shows a sketch of a general wireless communication scenario between a transmitter and a receiver. As known from Section 1.3.3, the transmitting antenna, in general, radiates power into all directions. Hence, not all the radiated power can be captured by the receiving antenna. The power density at the location of the receiving antenna can be calculated by

$$\boldsymbol{W_0 = \frac{P_{in} G_t(\theta_t, \Phi_t)}{4\pi R^2}} \qquad (2.56)$$

with G_t the gain of the transmitting antenna in the direction of the receiving antenna, specified by θ_t and ϕ_t and with R the distance between both antennas. The receiving antenna captures the portion

$$\boldsymbol{P_r = A_r(\theta_r, \Phi_r) W_0} \qquad (2.57)$$

of the radiated power. In (2.57) $A_r(\theta_r, \phi_r)$ denotes the effective aperture of the receiving antenna in the direction of the transmitting antenna, which is related to its gain according to

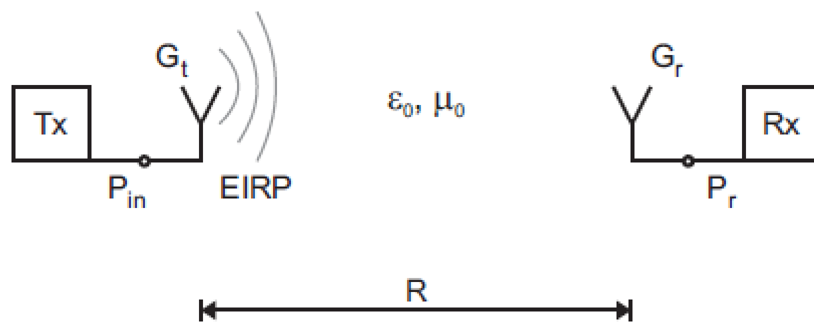


Figure 2.7. Free space wireless link between a transmitter (left) and a receiver (right) located at a distance R.

$$A_r(\theta_r, \Phi_r) = G_r(\theta_r, \Phi_r)\frac{{\lambda_0}^2}{4\pi} \qquad (2.58)$$

Using this relation and substituting (2.57) into (2.56) yields

$$\frac{P_r}{P_{in}} = \left(\frac{\lambda_0}{4\pi R}\right)^2 G_t(\theta_t, \Phi_t)G_r(\theta_r, G_r) \qquad (2.59)$$

which is known as the Friis transmission equation. The term, $1/4\pi R^2$, in (2.59) is called the free-space path loss since it takes into account the losses in the wireless link due to the spherical spreading of the radiated power.

Chapter 3

3 Integrated millimeter-wave antennas

As a starting point for the integrated mm-wave antenna concepts that were developed in the framework of this thesis, it is meaningful to first give a brief overview of the state-of-the-art. For this, some general requirements of antennas for the 60 GHz band are, firstly, summarized in Section 3.1 since these are common for all concepts. Next, brief overviews of typical state-of-the-art Antenna in Package (AiP), Antenna on Chip (AoC), and hybrid designs are given in Sections 3.2 to 3.4. The findings of the state-of-the-art overviews then serve as the motivation for the technology choices and antenna concepts that follow in subsequent chapters.

3.1 Antenna requirements for 60 GHz communications

It was already pointed out in Chapter 1 that an integrated antenna is preferred at mm-waves in order to keep the interconnect losses as low as possible. To obtain sufficient link for Gb/s transmission over 10 meters distance, an antenna should feature low fabrication cost, readily amenable to mass production, light weight, low volume, easy to integrate with monolithic integrated circuits (MMIC) RF front end-end circuitry, sufficient bandwidth and sufficient antenna directivity.

Furthermore, the antenna should exhibit a high, constant gain at a high radiation efficiency over the entire frequency band, as pointed out in [2]. If this requirement is not met, the overall signal-to-noise ratio (SNR) in the receiver is affected and, as a consequence, the communication distance would be severely compromised and/or the battery lifetime of portable devices unnecessarily shortened. Moreover, since high gain comes at a cost of a narrow beam-width, the antenna beam should be automatically adjustable in its direction. Therefore, switched-beam or phased arrays are typically suggested, see, for example, [2, 4, 5, 7, 8].

The antenna gain should be high; however, a motivated quantification of the gain requirement is hardly ever stated in the literature. Hence, this issue shall briefly be tackled here based on the Friis transmission equation (2.59), which relates the total received power to the total input power of a radio link in free space. For this, the worst case receiver sensitivity specification from IEEE standard 802.15.3c-2009, see [24], is used as minimum acceptable receiver input power level, Pr. According to this specification, a power level of at least -46dBm is the minimum requirement. For the transmitter, the maximum equivalent isotropic radiated power (EIRP), which is the product of transmit power and transmit antenna gain, is in Europe limited to a maximum of 40dBm, see [3]. Using this value and the worst case receiver sensitivity from above in (2.59), the minimum required receive antenna gain for 60 GHz can be determined to be Gr = 2dBi for a communication distance of up to R = 10 m. The respective system assumptions for this scenario are summarized as case #1 in Table 3.1. Here, a single transmitter chip like the one published in [25] is assumed that exhibits a maximum output power of PIC = 10dBm (= Pin in (2.59) for this case). As shown in the table, the resulting transmit antenna gain Gt has to be 30dBi in this case in order to achieve the maximum EIRP. Such high gain is difficult to achieve with a single integrated antenna, however, which makes this system approach rather impractical.

Another possibility of achieving a high EIRP is by increasing the transmit power. This could be done, for example, by building an array of antennas whereas every antenna is fed by an individual transmitter chip. By this, the output powers of the ICs are combined ”in the air”, as described in [4, 7]. Hence, the total transmit power is then as high as Pin = NPIC, with N the total amount of antenna array elements. Furthermore, this array approach leads to a larger overall antenna gain, with an overall gain increase of approximately the same factor N. Using this approach and assuming that the single antenna element of the array is a patch antenna, which typically exhibits a gain of Gt, single = 6dBi, and is fed by the same 10dBm transmitter chip, the total amount of transmit antennas has to be approximately 16, see case #2 in Table 3.1.

In order to reduce the transmit antenna array size, one can use another antenna array of size M on the receiver side. When choosing M = N and assuming once again that the single

antenna elements exhibit a gain of 6dBi on both sides, two 6-element arrays would easily satisfy the minimum input power requirement for a communication distance of up to R = 10 m, as shown as case #3 in Table 3.1. Note that in this configuration the maximum EIRP does not even have to be fully exploited, such that even larger distances can be reached by this approach.

For the file transfer at a ”kiosk in a store” and the wireless interconnect scenario, much shorter communication distances R are required. For a file transfer application, for example, a maximum distance of 1 m may already be sufficient. For this, a small array could be implemented in the kiosk terminal and a single antenna in the customer’s portable device. Using a 4-element patch-antenna array in the kiosk terminal, the receiver’s antenna gain can then be as low as -6dBi, shown as case #4 in Table 3.1.

Case #5 shows a possible wireless interconnect scenario. Here, only a single antenna is assumed on both sides of the radio link, which is a feasible assumption for a chip-to-chip interconnect, for example. If also for this scenario a 1 m communication distance is assumed, antennas with at least 6dBi gain are acceptable.

Finally, irrespective of the application scenario, in order to be accepted on the wireless consumer market, the cost of the complete module and, thus, of the antenna should be as low as possible, see [1, 2, 7]. For this, not only the materials and fabrication processes should be low-cost, the solution should also be flexible in order to cover as many application scenarios as possible in order to achieve high production volumes.

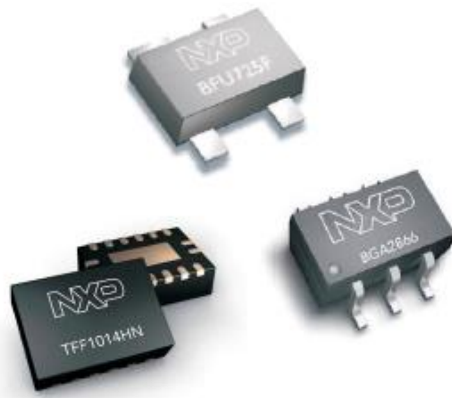
Hence, in summary, an integrated mm-wave antenna for the 60 GHz range should exhibit

- A small size and light weight, low cost
- Easy to integrate with monolithic microwave integrated circuits (MMIC)
- High radiation efficiency and gain over the entire bandwidth, e.g.
  - >6dBi for general purpose antennas,
  - > -6dBi for file transfers on the customer side,
- Beam forming capabilities,

Readily amenable to mass production.

Table 3.1. Possible antenna system configurations that satisfy the IEEE standard 802.15.3c-2009 ([24]) at 60 GHz using the transmitter chip from [25] with an output power of PIC = 10dBm.

case #	$G_{t,single}$ [dBi]	Tx array size (N)	G_t [dBi]	$P_{in} = NP_{IC}$ [dBm]	EIRP [dBm]	R [m]	$\left(\frac{\lambda_0}{4\pi R}\right)^2$ [dB]	$G_{r,single}$ [dBi]	Rx array size (M)	G_r [dBi]	P_r [dBm]
1	30	1	30	10	40	10	-88	2	1	2	-46
2	6	16	18	22	40	10	-88	2	1	2	-46
3	6	6	13.8	17.8	31.6	10	-88	6	6	13.8	-42.6
4	6	4	12	16	28	1	-68	-6	1	-6	-46
5	6	1	6	10	16	1	-68	6	1	6	-46



(a) Overmolded plastic-packages (OMP-packages).

(b) High-power ceramic-packages.

Figure 3.1. Typical high frequency packages from NXP Semiconductors, see [26] (courtesy of NXP).

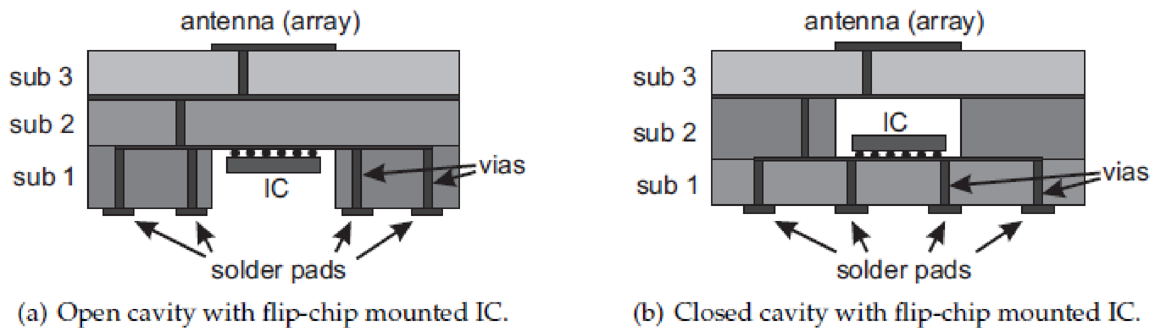
3.2 Antenna-in-Package

3.2.1 Definition

An Antenna-in-Package is here defined as an antenna that is integrated in the packaging technology of the IC. Furthermore, the antenna requires a physical interconnect to the on-chip electronics, which can be clearly distinguished from the rest of the antenna structure.

3.2.2 Review of typical IC packaging technologies

Before going into detail about state-of-the-art packaging technology concepts for future mm-wave front-end modules, it is meaningful to first briefly review typical IC packaging technologies of already existing high-frequency products. Figure 3.1 shows some typical examples of high-frequency IC packages from NXP Semiconductors, see [26]. The most



(a) Open cavity with flip-chip mounted IC.
(b) Closed cavity with flip-chip mounted IC.

Figure 3.2. Conceptual drawings of typical multilayer AiP concepts.

low-cost type is an over molded plastic-package (OMP packages), of which examples are shown in Figure 3.1(a). In its essence, it consists of a metallic lead-frame, on which the IC is placed. In order to connect the on-chip electronics to the lead-frame, standard low-cost wire-bond technology is usually used. For frequencies in the higher microwave range, however, the chip is often also placed up-side-down in order to connect the top-side of the chip directly to the leads of the package. This kind of chip assembly is commonly known as flip-chip technique.

Afterwards, the chip is then over molded with a plastic compound such that the chip is protected from external hazards, like moisture, but the metallic leads are still accessible from the outside and can be used to solder the package onto a larger system PCB.

For high power applications, ICs often produce too much heat in order to use plastic as packaging material. Here, ceramic is used instead. Figure 3.1(b) shows two examples of such packages. Compared to plastic, ceramic packaging has the disadvantage of being rather costly and is, therefore, only used if the design specifications cannot be met otherwise.

3.2.3 State-of-the-art

3.2.3.1 Low-temperature co-fired ceramic packages

One of the most often reported packaging technologies for AiP designs is known as low-temperature co-fired ceramics (LTCC), see [27]. Typical examples of AiP concepts in this technology are, for example, published in [28, 29, 30]. As explained in [29], LTCC is already a popular packaging technology in the high-frequency industry since it offers low-loss dielectrics, which can be easily stacked to create multiple metal layers for dense routing. Furthermore, open and closed cavities can be created in the multilayer stack, which can be used for integrating the IC here, as shown in Figure 3.2. Hence, using LTCC for the mm-wave range seems a natural choice. And indeed, most reported AiP designs in this technology achieve excellent performances. Some key results of references [28, 29, 30] are summarized in Table 3.2. The stated radiation efficiencies, however, often exclude the insertion loss of the chip-to-package interconnect, such that lower values can be expected in practice. Furthermore, since LTCC is a ceramic packaging technology like the ones shown in Figure 3.1(b), it is often considered as too costly for the consumer electronics market.

3.2.3.2 Printed circuit board packages

In order to reduce the costs of a solution according to Figure 3.2, some research groups have proposed to use the same multi-layer approach with less costly high frequency circuit

materials, like the RO3000-series and RO4000-series from Rogers Corporation, see [31, 32], or liquid-crystal-polymer substrates, see, for example, [33]. Good examples of such designs can, for instance, be found in [34, 35] and a very recently published AiP design that even uses a multilayer FR4-package, can be found in [36]. An overview of the key figures of all three PCB-based designs are also summarized in Table 3.2. From this, it is evident that these materials exhibit similar electric parameters to LTCC and that AiP designs in those technologies achieve comparable performances. However, a problem with the alignment accuracy of multilayer PCB substrates was presented in [37]. Although this does not appear to be a commonly experienced issue, this potential problem should be considered very seriously since it might result in an insufficient yield in high volume production.

Table 3.2. Overview of typical state-of-the-art Antenna-in-Package designs.

ref.	package technology	size [mm^2]	feed topology	interconnect technology	impedance bandwidth [GHz]	ϵ_r	$\tan(\delta)$	η_{rad} [%]	gain [dBi]	cost (relative)
[28]	LTCC	100	single-ended	wire-bond	6 @ 60 GHz	5.9	0.002	94	9.5	medium
[29]	LTCC	-	single-ended	flip-chip	-	3.9	0.006	-	8	high
[30]	LTCC	4.84	single-ended	flip-chip	9 @ 60 GHz	5.8	0.004	-	6	high
[34]	PCB	-	differential	flip-chip	10 @ 60 GHz	-	-	-	8	low
[35]	PCB	16	differential	flip-chip	9 @ 60 GHz	3.28-3.74	0.0018-0.0044	80	8	low
[36]	PCB	54	single-ended	-	9 @ 60 GHz	3.54-3.59	0.012	76	4.1	low

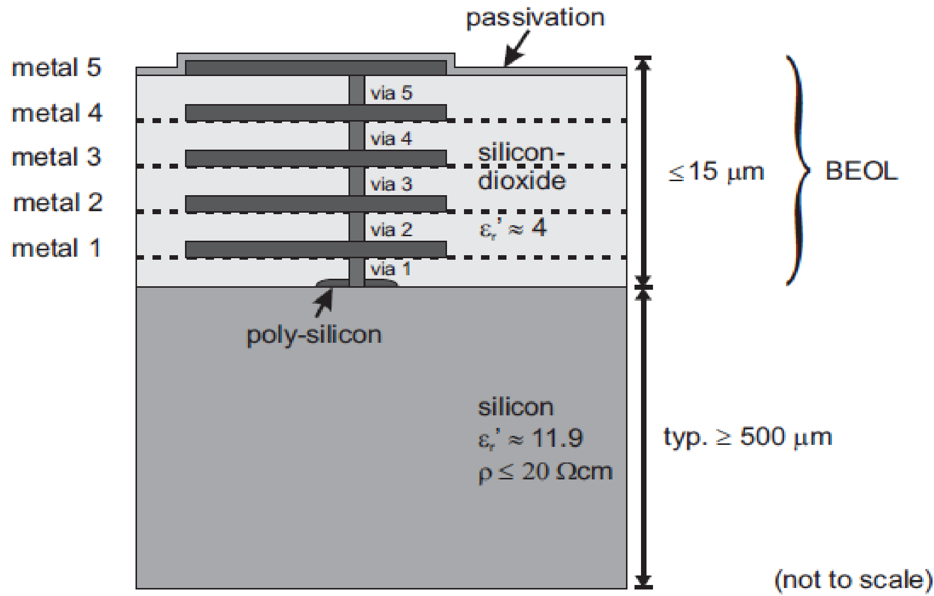


Figure 3.3. Sketched cross-section of a typical silicon IC.

3.3 Antenna-on-Chip

3.3.1 Dentition

Throughout this thesis, an Antenna-on-Chip is defined as an antenna that is integrated in the back-end of an IC, i.e., using a monolithic on-chip metallization process.

3.3.2 Review of typical silicon IC technologies

In order to understand above definition of an AoC, it is necessary to know some basics about typical silicon IC processes. Therefore, a sketched cross-section of such an IC including typical material parameters is provided in Figure 3.3. At the bottom it shows the core material of every CMOS and BiCMOS technology, namely the silicon substrate. On the top side of this usually about 750μm thick (for state-of-the-art high-frequency wafer sizes) silicon bulk, the active components are created by locally adding dopants into the silicon lattice. In the following process step, a stack of silicon-dioxide layers is added on

top of the active components. After each of those layers, metal can be deposited in order to create traces for horizontal interconnects.

Moreover, vertical interconnects (vias) that connect these metal layers can be implemented, as also indicated in Figure 3.3. Finally, the last metal layer (”metal 5” in the figure) is covered by a thin passivation layer that protects the top metal traces from external hazards, such as moisture. The complete stack of silicon-dioxide, metal, and passivation layer is usually not more than 10μm to 15μm thick. Since it is created in a ”back-end-of-line (BEOL) process”, this stack is often generally referred to as BEOL or simply as back-end of the IC. Finally, as a standard post-processing step, the silicon substrate can be ground down in order to reduce its thickness. A typical minimum silicon thickness after grinding is 200μm.

For high-frequency applications, passive components, like inductors, are often implemented in the back-end. Since the whole silicon bulk is usually pre-doped, however, it exhibits a low substrate resistivity of typically 10Ω-cm to 20Ω-cm. Thus, the losses in on-chip inductors are typically quite high, see also Section 2.1.2 on the relation between resistivity and loss tangent. Regardless of this drawback, pre-doping is necessary in order to prevent problems with active device parasitics.

3.3.3 State-of-the-art

As outlined in the previous section, it is common in high frequency IC designs to integrate passive components, like inductors, in the back-end. Hence, for frequencies at which the wavelength is comparable to the size of a complete silicon chip, it appears natural to also integrate the antenna here. The inherent advantage of this approach is that the antenna can be directly connected to the amplifier without the need for a mm-wave chip-to-off-chip interconnect. On one hand, this can minimize interconnect losses, see [1]. On the other hand, similar as for on-chip inductors, the low electric resistivity of the silicon substrate also introduces significant losses to the antenna. Those dielectric losses even have a more severe impact on on-chip antennas since, in contrast to inductors, their electric fields are

not mainly concentrated directly around the antenna but also penetrate deep into the silicon substrate. Hence, the radiation efficiency and, consequently, the gain are significantly affected by this. The on-chip Yagi-antenna in a 0.18 m CMOS technology published in [38], for example, only achieved a radiation efficiency of 10 % and a gain of -8dBi. A suggestion that is often brought up with respect to the lossy silicon substrate, is to shield it from the antenna by implementing a metal plate in the lowest metal layer of the IC's back-end ("metal 1" in Figure 3.3). A popular antenna example that is commonly mentioned in this regard is a patch antenna. As stated in [14], the distance between patch and ground plane should be between $0.003\lambda_0$ and $0.05\lambda_0$ for this antenna type. And although a back-end thickness of 15µm is right at the lower edge of this range, a significantly larger distance would be required in order to meet the bandwidth and radiation efficiency demands of the 60 GHz band, as a study on a basic patch antenna configuration in [39] indicates. An interesting consideration of an on-chip dipole with its resonance at 77 GHz, which is implemented in a 15µm thick back-end with a ground plane in the lowest metal layer, is presented in [40]. Here, the authors mainly focus on the radiation efficiency of the antenna. Their conclusion is that due to the ohmic loss in the metal traces, the radiation efficiency of this configuration is as low as 5 %. Even at higher frequencies, this approach seems to remain troublesome since a 140 GHz slot antenna design with ground shield only achieved a maximum gain of -2dBi, see [41]. Finally, the use of frequency selective surfaces, including electromagnetic band-gap (EBG) structures and artificial magnetic conductors (AMC), as proposed by [5], have been reported. Examples of such designs were published in [42] and [43]. The 60 GHz antenna design on a 17.5Ω-cm silicon substrate from [42], however, only achieved a radiation efficiency of 19.6 % and a maximum gain as low as -2.1dBi. The design presented in [43] does not specify any silicon parameters, but the reported maximum gain of -3.7dBi indicates a similarly low efficiency.

It shall be pointed out here, however, that besides the radiation efficiency issue with this antenna integration technology, all mentioned AoC designs achieved acceptable performances as the key figures in Table 3.3 indicate. Note, however, that the broad impedance bandwidth, for example, might also be caused by significant substrate losses.

Hence, achieving a satisfactory result in terms of bandwidth and radiation efficiency in a standard CMOS or BiCMOS process appears to be a major challenge. However, there are several techniques that can enhance the performance of an on-chip antenna. Since they all require additional processing steps after the usual IC fabrication, those techniques are commonly referred to as post-processing techniques. But although those steps have proven to enhance the performance of on-chip antennas, the semiconductor industry is still reluctant to incorporate them into their standard portfolio. A reason often given for this is the increase in fabrication costs and, therefore, the worries of losing competitiveness on the market. Despite those worries, typical post-processing techniques will be briefly summarized in the following, in order to present all currently available, most important options here. For comparison, the key parameters of all following antenna designs are also provided in Table 3.3.

Table 3.3. Overview of typical state-of-the-art Antenna-on-Chip designs.

ref.	ρ [Ωcm]	silicon thickness [μm]	post-proc. technology	size [mm^2]	feed topology	impedance bandwidth [GHz]	η_{rad} [%]	gain [dBi]	cost (relative)
[38]	-	-	none	1.045	differential	10 @ 60 GHz	10	-8	low
[41]	12.5	275	none	0.72	single-ended	5 @ 140 GHz	-	-2	low
[42]	17.5	300	none	1.222	differential	-	19.6	-2.1	low
[43]	-	-	none	3.24	single-ended	71 @ 70 GHz	-	-3.7	low
[44]	-	250	superstrate	0.702	single-ended	10 @ 95 GHz	44-62	0 - 2	medium
[45]	13.5	300	resonator	2.09	single-ended	3 @ 34.5 GHz	59	1.06	medium
[40]	-	100	lense	-	differential	-	-	2	medium
[46]	20	250	lense	-	differential	100 @ 220 GHz	50	17.8	medium
[47]	11-70	300-400	micromach.	12.96-20.2	both	-	-	1 - 1.5	high
[48]	-	-	MEMS	-	single-ended	12 @ 60 GHz	25	-6.75	high
[49]	10	-	proton implantation	0.83	single-ended	7 @ 46.5	-	6.4	high

3.3.3.1 Superstrates, resonators, and lenses

One possible method to improve the off-chip radiation of an antenna is to add an additional dielectric on top of the IC's back-end. Possible options for this are a simple superstrate, a resonator, and a lens. A 90 GHz design using a superstrate, for example, achieved a radiation efficiency of 44-62 %, see [44]. At nearly a third of that frequency, a 35 GHz slot

antenna design with metal shield in the lowest metal layer of the back-end and dielectric resonator on top of the slot achieved an efficiency of 59 %, see [45]. On-chip antennas including lenses were, for example, presented in [40, 46]. In both cases the lens was attached at the bottom of the chip. Hence, the electromagnetic wave first has to penetrate the low resistive BiCMOS substrates. Therefore, the 77 GHz antenna design from [40] only achieved a maximum gain of 2dBi, which is rather low for a lens antenna. The design presented in [46], however, achieved 17.8dBi at 180 GHz with a stated radiation efficiency of 50 %.

3.3.3.2 Micromachining

Since the presence of lossy silicon is the core problem of the low radiation efficiencies of on-chip antennas, a typically used post-processing method is to locally remove the silicon substrate around the antenna. This technique is generally known as micromachining. One of the earlier works in this direction was published by Öjefors et al. in [47]. According to this reference, a 30 GHz on-chip full-loop antenna achieved a gain of 1.5dBi. Unfortunately, an estimation of the radiation efficiency is not given, but in comparison to the above mentioned 60 GHz results without any post-processing, this gain indicates a rather good efficiency.

3.3.3.3 MEMS

Micro-electro-mechanical-systems (MEMS) are an up-to-date research topic on its own in the microwave and mm-wave communities. Also for on-chip antennas this technology offers promising possibilities. The authors of [48], for example, present a MEMS-based on-chip monopole antenna that stands perpendicularly on top of the IC. For this, the residual stress in a polymer based MEMS-process is used to create warping in the polymer during curing, resulting in the desired upright orientation of the monopole. Such an antenna configuration allows the implementation of a metal plate in the back-end without sacrificing bandwidth or radiation efficiency. Unfortunately, no simulated radiation efficiency or gain is given in the reference and no gain pattern measurements are shown. From a transmission

measurement between two of those antennas, the authors estimated the efficiency to be 25 %. This value seems rather low for this structure, however, which might be a result of the low signal to-noise-ratio of the transmission measurement, which is presented in the reference. Moreover, destructive interference with reflected waves from, for example, the probe station may have affected the measurement and caused this low result. Hence, in general, better efficiencies may be expected from such an antenna structure.

3.3.3.4 Proton implantation

Owing to the fact that the low radiation efficiency of on-chip antennas is mainly due to the pre-doped and, thus, low resistive silicon substrate, one might seek for a method to increase the resistivity in the vicinity of the antenna. One technique that can be used to achieve this is known as proton implantation. Already in 2003 the authors of [49] showed that by locally increasing the resistivity from 10Ω-cm to 106Ω-cm, a gain of 4.2dBi could be achieved for a 40 GHz printed monopole antenna, which indicates an excellent efficiency. Also the achieved bandwidth of about 15 % would be sufficient for operation in the 60 GHz band.

3.4 Hybrid integrated mm-wave antenna

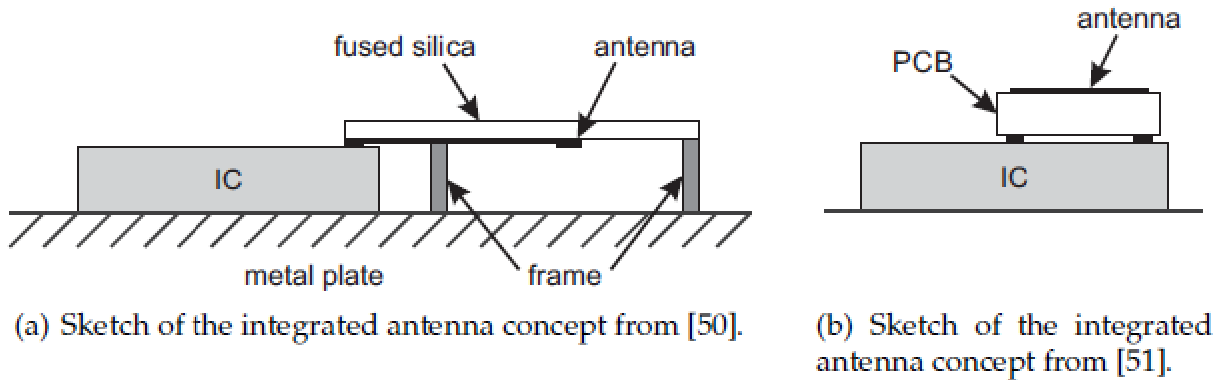
3.4.1 Definition

An antenna that is integrated in the same package with the front-end IC, but is neither implemented in the packaging technology nor in the back-end of the chip, shall here be referred to as hybrid integrated mm-wave antenna concept, or in short simply as hybrid concept.

3.4.2 State-of-the-art

Besides the AiP and AoC concept, several designs were published in recent years that cannot be uniquely assigned to one of the two categories since the antenna is neither integrated

in the back-end of the IC nor in the IC packaging technology. One of the first of those designs was published in [50]. Here, a dipole antenna on a fused silica substrate was mounted half on-chip and half off-chip, such that the antenna could be directly connected to the on-chip electronics, see Figure 3.4(a). The bandwidth of this antenna concept covers the full 60 GHz band and the reported gain is 6dBi to 8dBi at a radiation efficiency of larger than 90 %, see Table 3.4. However, the fabrication process appears to be rather complex. A slightly different antenna concept was published three years later in [51]. Here, a patch antenna in standard PCB technology was directly connected to the back-end of the IC by a flip-chip technique, see Figure 3.4(b). By mounting a small



(a) Sketch of the integrated antenna concept from [50].

(b) Sketch of the integrated antenna concept from [51].

Figure 3.4. Examples of hybrid integrated mm-wave antenna concepts.

PCB onto the chip rather than mounting the chip up-side-down onto a PCB, low-cost plastic packaging and bond-wire chip-top package interconnects could still be used. In the reference, the maximum achieved radiation efficiency including flip-chip interconnect is given as 60 % to 72 %, which results in a gain of 2dBi to 3.5dBi. Finally, even generic bond-wires can be used as antennas as shown in references [52, 53], which was even patented, see [54]. While in [52] the bond-wires are used as short monopoles (wire length of $0.144\lambda_0$) and only achieve a radiation efficiency of 15 % to 30 %, the authors of [53] use half-circular bond-wires for building a Yagi-Uda array with a simulated efficiency of 74.6 % to 90 % and a maximum gain of 6dBi to 8dBi. Also here, all key figures are provided in Table 3.4. From this, it can be concluded that hybrid integrated mm-wave antenna concepts seem to be an attractive alternative to pure AiP or AoC concepts.

Table 3.4. Overview of typical state-of-the-art hybrid integrated antenna designs.

ref.	technology complexity	size [mm^2]	feed topology	impedance bandwidth [GHz]	η_{rad} [%]	gain [dBi]	cost (relative)
[50]	high	12.6	differential	9 @ 60 GHz	90	6 - 8	high
[51]	low	-	single-ended	9 @ 60 GHz	60-72	2 - 3.5	low
[52]	very low	0.0036	single-ended	9 @ 60 GHz	15-30	-4 - 0.4	very low
[53]	very low	-	single-ended	3 @ 40 GHz	51-84	6 - 8	very low

3.5 Discussion

From the state-of-the-art overview in this chapter one can conclude that all three integration approaches can be used to design antennas that match the specifications of the 60 GHz band. The AoC approach, however, falls behind the AiP and hybrid approach in terms of radiation efficiency and gain. AiP and hybrid approach designs, on the other hand, may not be able to compete with the AoC in terms of cost due to their normally rather complex multi-layer packaging structure. Moreover, AiP concepts require an additional chip-to-off-chip interconnect that requires extra design effort and introduces additional losses to the system. Therefore, the hybrid solution seems, at first glance, the best solution here. However, for frequencies beyond 60 GHz the structure size and fabrication accuracy of typical hybrid but also AiP technologies might be insufficient. This problem does not exist for the AoC approach, which was already very successfully tested in the terahertz band, see, for example, [10].

Hence, instead of focusing on three integration approaches, the antenna on chip (AOC) option was investigated in the outline of this thesis. It shall be pointed out here, however, that besides the radiation efficiency issue with this antenna integration technology, all mentioned AoC designs achieved acceptable performances as the key figures in Table 3.3 indicate. Since they all require additional processing steps after the usual IC fabrication, those techniques are commonly referred to as post-processing techniques. But although those

steps have proven to enhance the performance of on-chip antennas, the semiconductor industry is still reluctant to incorporate them into their standard portfolio. A reason often given for this is the increase in fabrication costs and, therefore, the worries of losing competitiveness on the market. In this thesis, competitive antenna design concepts for this integration approach were developed to avoid these problems. Those concepts are based on basic antenna theories and types in order to focus the consideration on the antenna performance with respect to the integration technology and the antenna topology. The concepts for antenna on chip element are presented in the following chapter, where special emphasize is placed on the radiation efficiency. The problem of achieving sufficiently high gain values and beam-steering are then tackled in Chapter 6, which deals with considerations for antenna arrays.

Chapter 4

Design and Analysis of Virtual loop antenna (VLA)

4.1 Introduction

The performance of planar antennas can be evaluated with the modeling method that is presented in previous chapter. To determine which antenna topology is most suited for the transceiver system, a number of requirements should be taken into account in the design. The most important requirements can be listed as follows:

• The antenna should have sufficient bandwidth to cover the available unlicensed frequency band at 60 GHz. The available bandwidth is regulated differently in Europe, United States (US) and Japan. However, 5 GHz of unlicensed bandwidth is available throughout the world.

• The antenna has to be integrated with active electronics and therefore the integration of the antenna and the radio-frequency integrated circuit (RFIC) should be given consideration. Integration between antenna and RFIC improves the performance of the system, since this type of integration reduces loss significantly, has the ability to reject common-mode disturbances, and is easier to realize [55]. Therefore, an integrated antenna with a proper feed is required.

• Since it is difficult to realize sufficiently high transmit power, it is important that the antenna element has high radiation efficiency such that losses are minimized.

• The transceiver should be low-cost and therefore a standard planar manufacturing technology needs to be used for the realization of the antenna. A planar technology allows for a simple integration with the RFIC as well.

• To fulfill the link budget requirements for multiple gigabit-per-second (Gbps) transmission, front-ends with several power amplifiers are needed to generate the required transmit

power at 60 GHz. Additionally, antennas are needed that have sufficient gain and that support beam-forming. To obtain sufficient gain and to realize beam-forming, antenna arrays are needed. Therefore the antenna element needs to be suited for integration in array configurations.

• The antenna should have a well-defined feed that is low-loss and does not influence the performance of the antenna element. Moreover, the antenna topology should support a feed network that is able to feed an antenna array as well.

To summarize, an integrated antenna is needed that has a high radiation efficiency and sufficient bandwidth. Moreover, this antenna needs to be suited to be placed in array configurations and has to be realized in a low-cost planar manufacturing technology.

The main challenge of antenna design in a planar technology is the trade-off between radiation efficiency and bandwidth. To obtain a large bandwidth, a relatively thick dielectric layer is needed [56]. However, a thicker dielectric layer introduces more losses due to surface-wave excitation in the dielectric. A lot of work has been done to improve the radiation efficiency of planar antennas while maintaining a large bandwidth [57, 58]. Particularly, the use of electromagnetic band gap (EBG) materials that suppress the surface-wave excitation has received a lot of attention [59, 60, 61]. However, EBG materials are either difficult to manufacture, or too large to be used in planar array configurations. Another approach to improve the radiation efficiency is presented in [62], where a superstrate antenna is used. This solution shows good performance, but is more complicated to realize, since the superstrate antenna is a separate component that has to be placed partly on top of the integrated circuit.

As an alternative, a virtual loop antenna (VLA) is proposed here.. The concept proposed in this work avoids the extra steps but provides for good antenna efficiency. We propose the design of this antenna for use on CMOS ICs technology that promises to integrate a complete 60GHz system on single chip that combines a good performance in both bandwidth and radiation efficiency. The design is based on assumptions that conductor and conductive

pad are imaged in ground plane to form a loop antenna. The resulting design is completely planar, and the use of via is avoided. This result in inherently low fabrication cost, light weight, and low volume antenna. Its design is essentially a joint optimization of bandwidth and power efficiency. The design of this integrated loop antenna for use on 60GHz CMOS receivers was based on silicon substrates of low resistivity that varies from 5- 20Ω-cm. The design was based on intensive electromagnetic simulations using HFSS software package. The width and length of the antenna is less than half a free-space wavelength, such that the antenna can be readily used for the realization of a planar beam-forming array.

The selection of technology is discussed in detail in Section 4.2, whereas design effort of antenna element on silicon substrate is discussed in Section 4.3. Antenna configuration and modelling is considered in Section 4.4. Another aspect that is of importance with electromagnetically-coupled virtual loop antenna (EMC-VLA) is antenna quality factor which is investigated in Section 4.5. Optimization of the antenna is investigated in section 4.6. The design of electromagnetically-coupled virtual loop antenna (EMC-VLA) and probe fed virtual loop antenna (PF-VLA) is investigated in section 4.7 and 4.8. Surface wave analysis is performed in Section 4.9. Here, the effect of a finite-sized dielectric on the radiation pattern is investigated as well. Ground plane configurations are discussed in Section 4.10 To simplify the modeling of the antenna, sometimes the effect of the metal thickness and finite conductivity are not included in the model. The effects of this assumption are discussed in section 4.11. Finally, electromagnetic interference is discussed to improve the accuracy of the model in section 4.12.

4.2 Technology choice

Based on the results of the literature study in Section 3.3, an AoC concept was developed in standard IC fabrication technology. For this, NXP's CMOS process Qubic4X was chosen as integration technology due to its relatively high substrate resistivity of about 20 ohm-cm, see [63]. Qubic4X features an approximately 10μm thick back-end with five metal layers, see also Figure 3.3. Moreover, NXP grinds down their wafers to a minimum silicon

thickness of 200 m as a standard processing step. Similar to the micromachining post-processing technique described in Section 3.3, substrate thinning is used here to increase the radiation efficiency of the on-chip antenna design. In contrast to micromachining, however, the used grinding process is a standard technique in the semiconductor world and does not significantly increase the fabrication costs. With respect to the antenna type, an on-chip planar structure was chosen to realize virtual loop antenna since, just like for the AOC design from the preceding chapter, a single-fed antenna topology is preferred that can be implemented in the electrically thin back-end of the IC.

4.3 Design Efforts on silicon substrate

Silicon substrates introduce special challenges for high efficiency millimeter wave on-chip antennas. First, their low resistivity of 0.1-20 Ω-cm results in high dielectric loss and significantly reduces the antenna efficiency. Second, TE and TM surface waves are easily triggered in 200-500μm thick silicon substrates and can have serious detrimental effects on the antenna pattern and efficiency [64, 65]. In the past few years, a lot of work has been done on on-chip antennas. A 24 GHz transmitter with on-chip zigzag dipole with a measured gain around -12 dB is presented in [66]. Zhang et al. presented on-chip inverted-F and quasi-Yagi antennas with gains of -19 dB and -12.5 dB at 61 GHz and 65 GHz, respectively [67]. A 60 GHz millimeter-wave on-chip dipole antenna with a gain of -10 dB in a 0.18μm CMOS process is presented in [68]. Hsu et al. presented a 60 GHz CPW-fed on-chip Yagi-Uda antenna with a measured gain of -10 dB [69]. A 140 GHz receiver with -25 dB gain on-chip antenna is presented in [70]. A triangular loop antenna adjacent to a lossy silicon substrate is presented in [71]; the antenna has a simulated gain of -0.4 dB at 60 GHz and a measured gain of 0.9 dB using a scaled model at 2GHz. A Yagi-Uda array of wire-bond antennas with a measured gain of 8 dB at 40 GHz is presented in [72]. This antenna occupies a large space on wafer, and is not suitable for dense integrated circuits. Wu et al. also presented 60 GHz bond-wire antennas with >30% efficiency [73]. Hirokawa et al. presented a dipole antenna on a thick resin layer on the back of a silicon chip with a gain of 3.1 dB at 60 GHz [74]. Except for the bond wire and the thick resin layer antenna, all integrated circuit antennas have low gain and low efficiency at mm-wave frequencies. As

an alternative, an antenna design is proposed here that is named virtual loop (VLP) antenna. The concept proposed in this paper avoids the extra steps but provides for good antenna efficiency. We propose the design of this antenna for use on CMOS ICs technology that promises to integrate a complete 60GHz system on single chip that combines a good performance in both bandwidth and radiation efficiency. The design is based on assumptions that conductor and pad are imaged in ground plane to form a loop antenna. The resulting design is completely planar, and the use of vias is avoided. This result in inherently low fabrication cost, light weight, and low volume antenna. This antenna can be suited to be placed in array configurations and has to be realized in a low-cost planar manufacturing technology to obtain sufficient gain and to realize beam-forming, antenna arrays

4.4 Antenna configuration and Modelling

Popular strategy for making antennas electrically smaller and lowering their profiles is to use ground planes and short circuits. The principle can be easily explained by the well known example of the monopole compared to the dipole. A dipole has a length of roughly

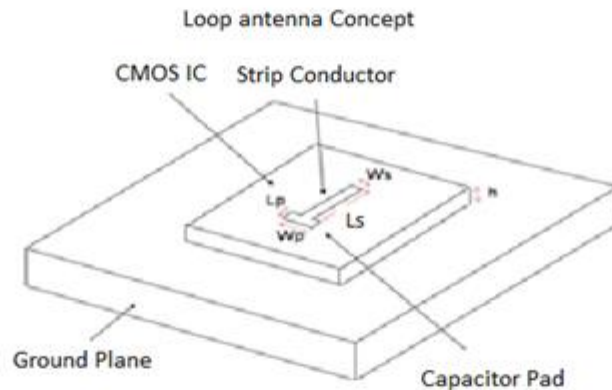


Fig. 4.1: Virtual loop antenna configuration

half a wavelength at resonance. This dipole height can be halved by replacing one dipole arm with a ground plane, which will, in turn, create a virtual dipole arm, according to image theory [75]. The principle can also be extended to planar printed antennas by adding short circuits to the ground planes. The proposed antenna configuration, as shown in Fig. 4.1, is

a loop antenna where half of it is due to the image in the ground plane and the loop is completed not by a continuous conductor but by a capacitance realized by a conductive pad and whose rf impedance is low enough to be essentially a short circuit. The figure shows that a rectangular strip and a capacitor pad are printed on the top plane of silicon substrate of thickness of h=0.25mm and a relative dielectric constant of ε_r=11.9 and substrate resistivity of 10-20Ω-cm. The design is based on assumptions that conductor and pad are imaged in ground plane to form a virtual current loop antenna. This result in inherently low fabrication cost, lightweight, and low volume antenna. For design studied here using HFSS software package, the following dimensions related to structure are determined as length of antenna l_a=0.48mm, width of antenna w_a= 0.05mm, length of pad l_p=0.12mm, width of pad w_p= 0.15mm and substrate thickness h_s=0.25mm as baseline dimensions. The antenna length chosen was approximately quarter wave length at 60GHz.

The antenna is first analyzed with aid of finite element method approach. To reduce the computational effort that is needed to analyze the performance of the antenna, the approach does not include the effect of the finiteness of the dielectric layers. For normal board sizes, the finiteness of the dielectric does not affect the impedance matching of the antenna. At the edges of the finite dielectric, the surface waves scatter and distort the radiation pattern. As a result of this, a ripple will be superimposed on the radiation pattern [45]. This effect will be analyzed separately and is discussed in Section 4.9.

The metal layers have also been modeled as perfect electric conductors with zero thickness. This approximation reduces the complexity of the model since it treats the metal layers as two-dimensional structures. Therefore, less time and computation are needed to analyze the performance of the antenna. The effect of finite conductivity and metal thickness is evaluated in future Section. The feed structure below the ground plane using probe fed and the antenna structure plane above the ground plane using microstrip line can be analyzed separately.

4.4.1 AOC electrical circuit Model

Figure 4.1 above shows the layout of a planar microstrip antenna on chip (AOC). The first metal layer, the routing layer, is sandwiched between two insulating layers. In this work,

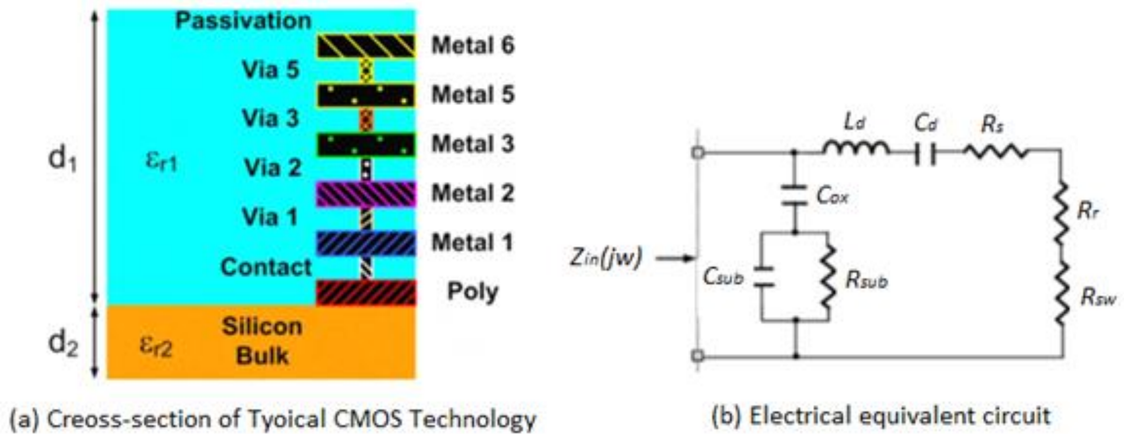


Fig. 4.2: Equivalent circuit model of an AOC with an off-chip ground

silicon dioxide is used as the insulation layer. In order to efficiently identify the optimal antenna layout and account for its parasitic in circuit simulations, an accurate equivalent model is required. A few equivalent electrical models for microstrip antenna are available that de

scribe the antenna behavior in a wide range of frequencies [76-83]. The simplest model is shown in Fig. 4.2 (b), where *L, C and R* represent the inductance, capacitance and resistance of the antenna and is computed using either of the equations discussed in this section.

The AoC solution features the integration of antennas or arrays together with other front-end circuits on the same chip in mainstream silicon technologies such as SiGe or CMOS. It should be mentioned that the AoC is not simply a matter of straightforward copy of integrated antennas developed in GaAs, for instance, via-to-ground can be easily realized through the substrate in standard GaAs, but not in a standard silicon process. Fig. 4.2 (a) shows the cross section of a silicon chip. Note that multiple metal layers are embedded between insulator layers on the substrate. In a standard silicon process, the thickness of metal layers ranges between 0.2 to 4μm and the insulator layers between 0.2 to 1μm. The number of metal layers is currently 6–8 and the separation from the top to bottom metal

layers rarely exceeds 15μm. The thickness of the substrate is typically 500–750μm. The metal is either aluminum or copper. The insulator is SiO_2 or its variations with ε_r =2.2–4. The substrate is silicon with and is doped to exhibit low resistivity ρ=10Ω-cm, which is substantially smaller than that of GaAs substrates ($\rho = 10^7$-10^9 Ω-cm).

The largest die size of the current 60-GHz radio in silicon is about 6.4mm^2.Considering the possibility of integrating more circuits such as the baseband processor on the same chip, one can expect that the die size may increase to tens of mm^2. Consequently, more area may be available to integrate more antenna elements in an array format. Nevertheless, we believe that high-directivity AoC is not practical at 60-GHz with the expected die size. The key parameters for the AoC thus become input impedance bandwidth and radiation efficiency [84].

Fig.4.2 (b) shows an AoC equivalent circuit model. In the model, the series branch comprises R_r, R_c, R_{sw}, L_d and C_d. Resistances R_r, R_c and R_{sw} account for the radiation, conductor, and surface-wave losses of the AoC, respectively. And L_d and C_d are the inductance and capacitance of the AoC, respectively. The shunt branch consists of C_{ox}, C_{sub}, and R_{sub}. C_{ox} represents the oxide capacitance between the AoC and the silicon substrate. C_{sub} and R_{sub} are the silicon substrate capacitance and resistance, respectively.

The input impedance of the AoC can be written from the equivalent circuit model as, shown in fig. (4.2) above,

$$Z_{in}(j\omega) = \frac{1-\omega^2(C_dC_sR_dR_s + C_dL_d)] + j\{\omega[(C_dR_d + C_sR_s(1-\omega^2C_dL_d))]\}}{[-\omega^2C_dC_s(R_d+R_s)] + j[\omega(C_d + C_s - \omega^2C_dC_sL_d)]} \quad (4.1)$$

Where

$$R_d = R_c + R_r + R_{sw} \quad (4.2)$$

$$R_s = \frac{R_p}{1+\omega^2R_p^2C_p^2} \quad (4.3)$$

And

$$C_s = C_p\left[1 + \frac{1}{\omega^2 R_P^2 c_P^2}\right] \quad (4.4)$$

With

$$R_p = \frac{1 + \omega^2 C_{sub}^2 (C_{sub} + C_{ox})^2}{\omega^2 R_{sub} C_{ox}^2} \quad (4.5)$$

And

$$C_p = \frac{\omega C_{ox} + \omega^2 R_{sub}^2 C_{sub} (C_{sub} + C_{ox}) C_{ox}}{1 + \omega^2 R_{sub}^2 (C_{sub} + C_{ox})^2} \quad (4.6)$$

The radiation efficiency of the AoC can be expressed as

$$\eta = \frac{R_r}{Re[Z_{in}(j\omega_d)]} \quad (4.7)$$

Where $Re[Z_{in}(j\omega_d)]$ is the real part of the input impedance of the AoC at the resonance angular frequency

$$\omega_d = \frac{1}{\sqrt{L_d C_d}} \quad (4.8)$$

Note that from $R_p \propto R_{sub}$ from (4.5) and $R_s \propto 1/R_p$ from (4.3), this leads to

$$R_s \propto \frac{1}{R_{sub}} \propto \frac{1}{\rho} \quad (4.9)$$

It is found numerically from (4.7) that the silicon substrate of low resistivity results in poor radiation efficiency.

Virtual rectangular loop antenna has been used in the AoC designs on silicon substrate with resistivity of 10 ohm-cm. The antennas are designed for the 60-GHz band. Fig. 4.3 shows

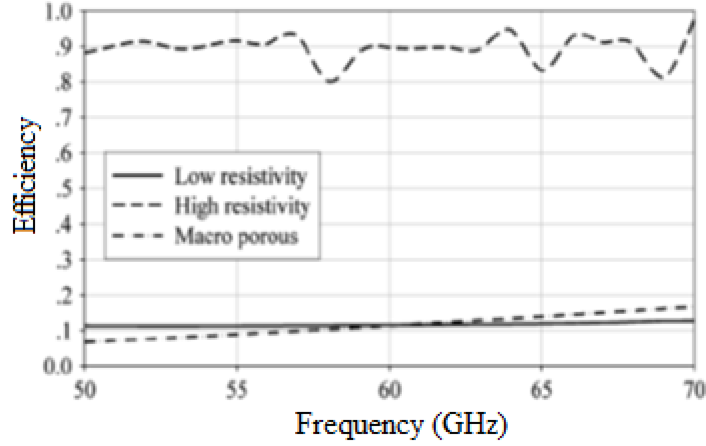


Fig. 4.3: Simulated AOC efficiency results with off-chip ground

the HFSS simulated efficiency of the designed AoC with an off-chip ground shield. The AoC is an on-chip virtual loop that has an arm size of 480µm x 50µm x 5µm and is placed away from the edge of a die size of 5mm x 5mm x 0.25mm by 100µm. The AoC is assumed to be realized using the top metal (copper) supported by a 9µm SiO_2 layer on a 250µm Si substrate of low resistivity ρ=10Ω-cm. Note that the simulated efficiency of the AoC is poor, only 11.5% at 60 GHz. This is expected from the combined effect of the low resistivity and high permittivity of the silicon substrate. The low resistivity causes loss due to heating in the presence of an electric field in the substrate and the high permittivity causes loss due to power trapped in surface-wave modes in the substrate. To improve the AoC efficiency, it is important to know which is the major contributor to the poor AoC efficiency, the low resistivity, or the high permittivity. Fig. 3 also shows the HFSS simulated AoC efficiency results for both high resistivity and macro porous Si, respectively. For the case of high resistivity Si, the resistivity is increased to ρ=1000Ω-cm; while for the case of macro porous Si, ε_r=2.2 for the SiO_2 layer and ε_r=6 for the Si substrate are assumed. It is evident from the figure that the low resistivity is the dominant factor to poor AoC efficiency [85].

4.4.2 Antenna Model Parameter Extraction

4.4.2.1 Series Resistance

The current density in a conductor strip is uniform at dc. However, as frequency increases, the current density becomes non-uniform due to the formation of eddy currents. The eddy current effect occurs when a conductor is subjected to time-varying magnetic fields and is governed by Faraday's law [86, 87]. Eddy current manifest itself as skin and proximity effects. According to the Lenz's law, eddy currents produce their own magnetic fields to oppose the original field. In the case of the skin effect, the time varying magnetic field due to the current flow in a conductor induces eddy currents in the conductor itself. The proximity effect takes place when a conductor is under the influence of a time-varying field produced by a nearby conductor carrying a time-varying current. In this case, eddy current is induced whether or not the first conductor carries current. If the first conductor does carry a time-varying current, then the skin-effect eddy current and the proximity-effect eddy current superpose to form the total eddy current distribution. Regardless of the induction mechanism, eddy currents reduce the net current flow in the conductor and hence increase the ac resistance. Since the antenna is designed on multi-conductor layer structure, eddy currents are caused by both proximity and skin effects.

The distribution of eddy currents depends on the geometry of the conductor and its orientation with respect to the imposing time-varying magnetic field. The most critical parameter presenting the skin effect is the skin depth. The skin depth is also known as the "depth of penetration" since it describes the degree by which the electromagnetic field penetrates into the thickness of a conductor at high frequencies. The severity of the skin effect is determined by the ratio of skin depth to the conductor thickness. The eddy current effect is negligible only if the depth of penetration is much greater than the conductor thickness (e.g., at frequencies close to dc).

Current distribution in a conductor is strongly dependent on the location of the ground plane. In case of the isolated conductor, at low frequencies where the skin depth is in the

order of the strip thickness, the current distribution is almost uniform across the thickness of the conductor. If this condition is satisfied, the ac resistance of the conductor per unit length can be calculated from:

$$R_{ac,f\to 0} = R_{dc} = \frac{1}{\sigma w t} \qquad t \leq 2\delta \tag{4.10}$$

Where $\sigma$the metal conductivity, and w and t is are the conductor width and thickness, respectively.

At high frequencies however, when the skin depth is much smaller than the strip thickness (say $t > 4\delta$), a nearly exponential penetration of the electric field distribution in the conductor can be observed. This behavior of the current distribution is used to find the approximate formula for the ac resistance of an isolated strip [88].

$$R_{ac,f\to\infty} = k\frac{l}{2\sigma\delta(w+t)} \qquad t \geq 4\delta \tag{4.11}$$

where l, w *and* t are the conductor length, width and thickness, respectively. σ is the conductivity of the strip, and $\delta$is the metal skin depth. k is the correction factor, which depends on w and t.

On the other hand, for a microstrip line with large w/h ratio, current recedes to the bottom surface of the conductor [89-92]. The w and h are the width of the conductor and the

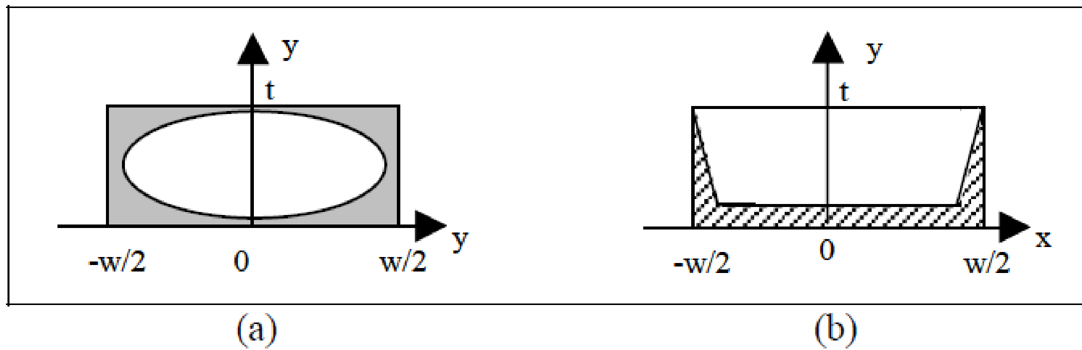


Fig. 4.4: Effective area of current flow at high frequencies where (a) $w/h \to 0$ and (b)$w/h \to \infty$.

thickness of the substrate (distance of the antenna structure to the ground plane), respectively. The current distribution is otherwise almost uniform across the height of the conductor. Figure 4.4 compares the current density distribution for two extreme cases of w/h ratio. For microstrip conductors at high frequencies the effective thickness can then be approximated by

$$t_{eff} = \delta\left(1 - e^{-t/\delta}\right) \tag{4.12}$$

And as a result, the series resistance, $R_s$can be expressed as

$$R_s = \frac{\rho l}{w t_{eff}} \tag{4.13}$$

Based on Eq. 4.13, resistance of a microstrip line does not decrease by increasing its thick ness in excess of 5$\times$skin depth. On the contrary, having an isolated strip structure for the antenna allows reduction of the series resistance by increasing the thickness of the conductor, even in excess of 5$\times$skin depth. To take advantage of this phenomenon, antenna structures used in this thesis are microstrip with distant ground, knowing that microstrip structures with distant ground behave like isolated strips. Therefore, the equivalent series resistance can be calculated from:

$$R_s = \sqrt{\left(\frac{l}{\sigma w t}\right)^2 + \left(\frac{kl}{2\sigma\delta(w + l)}\right)^2} \tag{4.14}$$

SONNET simulation results also confirm that for microstrip antenna with distant ground, current also flows on the top surface of the conductor. The verification of this fact is shown

in Fig. 4.5 (red color shows the highest current density). At 60GHz the current is confined closer to the metal walls, showing the effect of the skin depth.

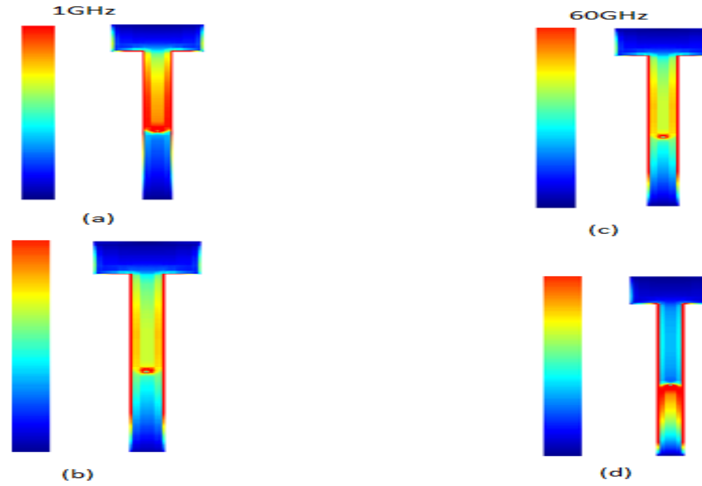


Fig. 4.5: Current density of a microstrip antenna at 1 GHz and 60 GHz (a) and(c) at the top surface of metal, (b) and (d) at the bottom surface of metal.

4.4.2.2 Series Capacitance and Substrate Parasitic

As it was previously mentioned, C_s represents the feed-through effect as well as the side-wall parasitic capacitances. The contribution of sidewall parasitic is negligible due to the insignificant voltage difference between the two adjacent strips, and C_s can be calculated from:

$$C_s = \frac{\varepsilon_{dilectric} A_{overlap}}{d} = nw^2 \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{4.15}$$

The high frequency loss of Si substrate is represented in C_{si} and R_{si}. Specifically, R_{si} is originated from the creation of eddy currents in the low resistivity S The high frequency loss of Si substrate is represented in C_{si} and R_{si}. Specifically, R_{si} is originated from the creation of eddy currents in the low resistivity Si substrate and C_{si} models the high fre-

quency capacitive effect occurring in the semi-conductors. To extract the substrate characteristic, dummy structures should be included on the substrate. Assume a rectangular dummy pad to have a measured impedance of Z_{pad}. R_{si} and C_{si} can be approximated by:

$$Z_{pad} = R_{pad} + \frac{1}{j\omega C_{pad}} \tag{4.16}$$

$$R_{si} = R_{pad} \times \frac{pad\ area}{total\ inductor\ area} \tag{4.17}$$

$$R_{si} = R_{pad} \times \frac{total\ antenna\ area}{pad\ area} \tag{4.18}$$

4.5 Antenna Quality Factor

The quality factor is a figure of merit that is representative of the antenna losses. Typically these are radiation, conductors (ohmic), dielectric and surface wave losses.

The general expression for the quality factor is:

$$Q = \frac{energy\ stored}{energy\ lost} \tag{4.19}$$

For antennas, the only undesirable sources of storing energy are magnetic and electric fields and hence any source of storing electric and energy such as capacitances and inductors are considered as a parasitic. As a result, Q of an antenna can be simplified as follow:

$$Q = 2\pi f_0 \frac{peak\ stored\ electric\ energy}{Energy\ dissipated\ per\ cycle\ of\ oscillation} \tag{4.20}$$

The frequency at which the peaks of electric and magnetic energies are equal is called the self-resonance frequency (*SRF*). Quality factor becomes zero at *SRF*. At frequencies higher

than *SRF*, the antenna does not behave as an antenna anymore. The total quality factor Q_r is influenced by all of these losses mentioned above and is, in general, written as by (Appendix A)

$$\frac{1}{Q_r} = \frac{1}{Q_{rad}} + \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_{sw}} \qquad (4.21)$$

Where

Q_r=total quality factor
Q_{rad}=quality factor due to radiation (surface wave) losses
Q_c= quality factor due to conduction (ohmic) losses
Q_d= quality factor due to dielectric losses
Q_{sw}=quality factor due to surface waves

4.5.1 Metal and Substrate loss quality factor

Metal loss is due to the finite conductivity of the metal conductors together with the skin and proximity effects presented at high frequencies. R_s in the equivalent circuit model represents the metal loss. In this work, metal loss is reduced by electroplating thick Cu (~20μm) and eliminating the effect of ground plane by increasing the signal to ground distance in the antenna layout. The thickness of routing metal (first metal) and the insulating SiO_2 layers are said by processing constrains. To alleviate the effect of routing layer on the overall Q, the length of this layer must be kept as short as possible.

At RF frequencies, induced currents in the Si substrate limit the Q by converting the electromagnetic energy into heat. Equations 4.22 and 4.23 show components of the induced current in the substrate at the presence of electromagnetic fields [93].

$$\nabla \times H = j\omega\varepsilon' E + \omega E' tan\delta E + \sigma E \qquad (4.22)$$

$$\nabla \times E = -j\omega\mu H, \qquad J = \sigma E \qquad (4.23)$$

where $\sigma$and $tan\delta$ represent the substrate conductivity and loss tangent, respectively; ω is the angular frequency, ε' and ε'' are the real and imaginary part of the substrate permittivity and μ is the permeability. For low-resistivity substrates such as CMOS-grade Si, the electrically induced current (σE) dominates over the dipole loss ($\omega\varepsilon' tan\delta E$). However, for high-resistivity substrates the dipole loss is the determining loss mechanism. At higher frequencies, creation of the magnetically induced eddy current in low-resistivity substrates (Eq.4.23) also limits Q.

These two sources of loss are independent and the unloaded Q can be expressed by [120]:

$$\frac{1}{Q} = \frac{1}{Q_d} + \frac{1}{Q_c} \tag{4,24}$$

Where Q_d and Q_c represent quality factor of substrate loss and the ohmic loss of metal strips, respectively. At very low frequencies, the DC series resistance of the metal layers is

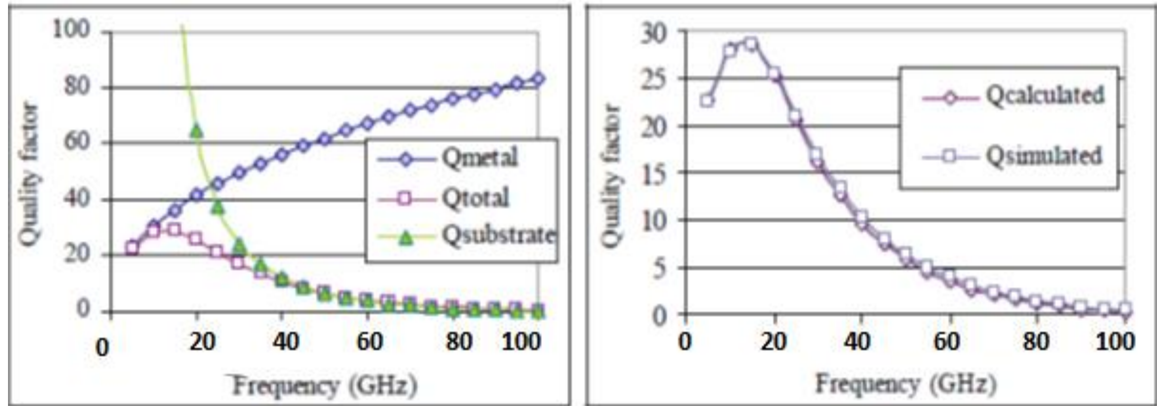


Fig. 4.6: (Left) Quality factor vs. frequency for a virtual loop antenna and (right) Comparison of the calculated Q (by Eq.4-24) and simulated Q (antenna length=500μm, antenna width=50μm, and metal thickness=5μm. ρ=10Ω.cm).

the dominant mechanism for determining the Q. At higher frequencies, skin effect and proximity effects reduce the effective area of current flow and thus further limits the Q. At even higher frequencies, loss mechanisms present in the substrate settles the lower limit on the Q. To investigate the validation of Eq. 4.24 and to better understand the contribution of

each loss-mechanism in Q, SONNET simulations were carried out. Two sets of simulation were performed to study the effect of each source of loss. Metal loss was determined by assuming that the antenna is elevated in vacuum. On the other hand, the substrate loss was considered by using ideal metal conductors. By using thin substrate (h « λ_0), the losses due to surface waves are very small and can be neglected. Figure 4.6 illustrates the SONNET simulation results. As can be seen, metal loss is the dominant loss mechanism at low frequencies, while the substrate loss sets the lower limit on the Q at higher frequencies. To obtain high efficiency antenna, the effect of both the substrate and the metal loss has been effectively suppressed

4.6 Optimization of the antenna physical dimensions

The quality factor is antenna figure-of-merit which is interrelated to antenna physical dimensions, and there is no complete freedom to independently optimize each one. There is always a trade-off between them in arriving at an optimum antenna performance. In order to obtain the highest possible efficiency for antennas fabricated on low resistivity Si, all physical dimensions of antenna are optimized based on quality factor using SONNET simulation tool. Optimization is based on minimizing ohmic, dielectric and surface wave losses To find the optimized value of each parameter, all other parameters are kept constant. The optimized parameters are:

4.6.1 Metal thickness

SONNET calculates the total surface impedance, impedance per unit area, of a thick metal by [104]:

$$Z_s = \frac{(1+j)\rho}{1 - e^{\frac{(1+j)t}{N\delta}}} \tag{4.25}$$

where ρ is the metal resistivity, δ is the skin depth, t is the metal thickness and N is the number of conductor sheets that SONNET requires to estimate the thickness of the metal.

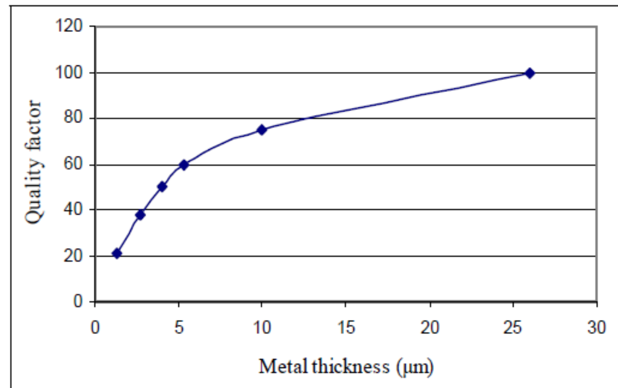


Fig. 4.7: Q vs. metal thickness using SONNET thick metal model N= 5 for 6µm metal

By increasing t, surface resistance drops exponentially and therefore Q increases. Figure 4.7 illustrates the dependency of the Q on the metal thickness. Simulation results confirm the Q improvement with metal thickness in excess of $5\times\delta$

4.6.2 Oxide thickness

Optimum value for the oxide thickness cannot be obtained by SONNET simulation tool as it is computationally intensive. To have an estimate of the required oxide thickness, simulations were done assuming the substrate is covered with a thick oxide layer. SONNET simulations indicate an increase in the antenna Q with oxide thickness up to 50µm for 60GHz antenna (Fig. 4.8). The optimum value of the dioxide thickness could be close to 50µm but needs to be obtained experimentally.

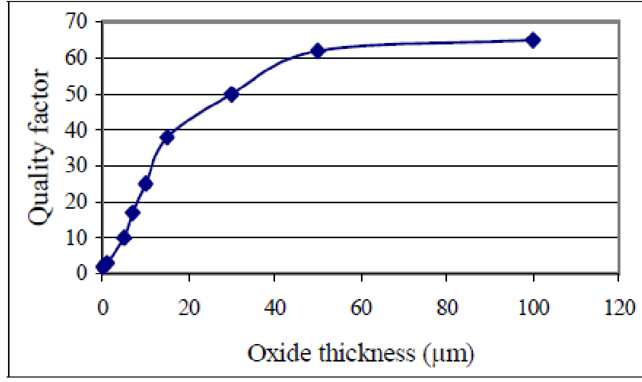


Fig. 4.8: Q vs. oxide thickness (metal thickness=7µm, antenna width=50µm, antenna length=480µm)

4.6.3 Substrate thickness

A study of integrated microstrip dipoles in GaAs shows that optimum radiation efficiency can be obtained when the substrate thickness is chosen at the cutoff thickness of the surface-wave TE_0 mode given by $\lambda_g/4$ where λ_g is the guided wavelength in the substrate [94]. This choice is appropriate for GaAs, but not for silicon substrates because they have very low resistivity resulting in significant ohmic losses that cannot be neglected. A careful investigation of radiation and propagation mechanisms shows that the AoC efficiency can be improved by thinning silicon substrates. According to mode theory, substrate thinning to less than $\lambda_g/4$ cuts off all surface-wave modes except TM_0. This mode contributes constructively to the directly radiated field through reflection at the ground plane and refraction at the substrate-air interface, thus improving the radiation efficiency.

The TM_0 surface-wave mode is an approximate plane wave because the *E*-field component is quite weak in the mode propagation direction. It undergoes large attenuation over the propagation in the substrate of low resistivity. To have a smaller attenuation, the substrate should be chosen much thinner than the thickness *T* given by

$$T = \left[\omega\sqrt{\frac{\mu_r\mu_0\varepsilon_r\varepsilon_0}{2}}\left(\sqrt{1+\left(\frac{1}{\omega\rho\varepsilon_r\varepsilon_0}\right)}-1\right)\right]^{-1} \tag{4.26}$$

where the symbols have their usual meaning. As an example, consider a silicon substrate with ε_r=11.9 and ρ=10Ω-cm, we find T to be 1.3 mm at 60 GHz. Choosing a thickness 5 times thinner than this value yields 260μm, which happens to be around the wafer thickness, thinned before dicing. HFSS simulation shows that the efficiency of the AoC on a 250μm Si substrate can be doubled to 23% at 60 GHz. Further thinning is possible, but more mechanical and reliability issues arise. In addition to substrate thinning, other approaches are available in a volume process such as placing the antenna nearest to the chip edge or furthest to the substrate which can also improve the AoC efficiency.

4.6.4 Dielectric Truncation

As discussed in previous section, the existence of a dielectric layer over a conducting ground plane in microstrip antennas is responsible for the excitation of surface waves along the air-dielectric interface. Neglecting dielectric losses, these waves propagate without attenuation in a direction parallel to the interface while, in the normal direction, they decay

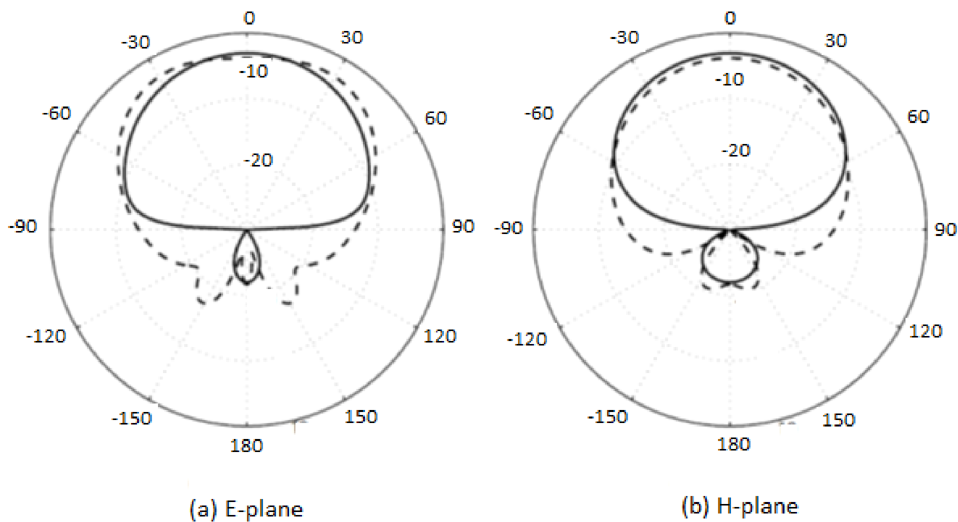


Fig. 4.9: the effect on radiation pattern due to truncation of Substrate. (a) E-plane infinite dielectric (solid line), Finite (dotted line (b) H-plane infinite dielectric (solid line) finite dielectric (dotted line)

exponentially without propagation. In most practical applications the conducting ground plane is sufficiently large and may be assumed as having infinite dimensions. For various

reasons the dielectric layer is smaller than this plane and cannot always be considered as having infinite dimensions. In other words, in many cases the dielectric should be considered as truncated after a certain distance from the conducting structure that constitutes the antenna. It is known [l] that the surface waves radiate some of their energy as they reach a discontinuity and that the electromagnetic fields from this radiation add to the space wave fields to produce the total radiated fields from the structure. The effect on the radiation patterns of the antenna due to changes in the size of the truncated dielectric will be shown in fig. 4.9. The main assumption made is that the distance between the antenna edge and the edge of the truncated dielectric is sufficiently large so that the position of truncation occurs in a far field region.

To investigate the effect of the surface-wave scattering at the edges of the dielectric, the simulated radiation patterns for an infinite and finite dielectric are compared. The radiation pattern for the infinite case has been analyzed by Method of Moment Implementation (SONNET), whereas the radiation pattern for the finite dielectric layers has been analyzed with Finite Element Method (HFSS). In Fig. 4.9, the radiation pattern is shown for the finite and infinite dielectric. Here, the size of the dielectric layers is chosen arbitrarily as 4mm $\times$ 4 mm.

4.6.5 Metal width

Variation of the conductor width (w) affects the Q in several ways. The primary consequence of increasing w is reduction of the conductor's series resistance. On the other hand,

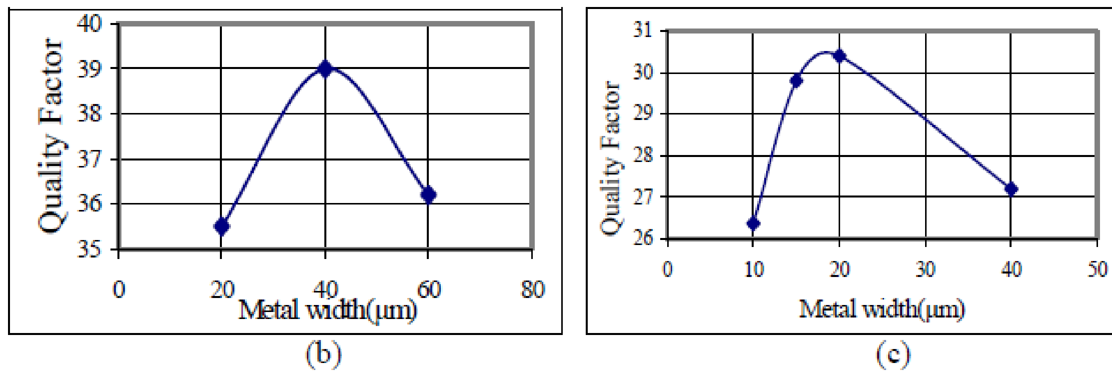


Fig. 4.10: Q vs. conductor width for (a) antenna length La=480µm), and (b) antenna length La=500 µm)

increasing the conductor width has a negative effect on the Q due to the simultaneous enlargement of the substrate parasitic capacitance. Metal width has an optimum value that must be designed for each specific antenna. Figure 4.10 shows the change in Q as a function of w for two different antennas. As will be shown in future section, another consequence of increasing the metal width is reduction of the *SRF* given that the substrate capacitance increases accordingly.

4.6.6 Size of the ground plane

Ground plane has less effect on the current distribution in the signal line compared to the ground plane underneath the antenna even when the ground plane is patterned. To minimize the effect of ground plane, the signal to ground distant must be increased. Nonetheless, the ground plane presents an important metallic area, so the ground plane dimensions must be optimized for minimal metallic losses while maintaining good antenna behavior.

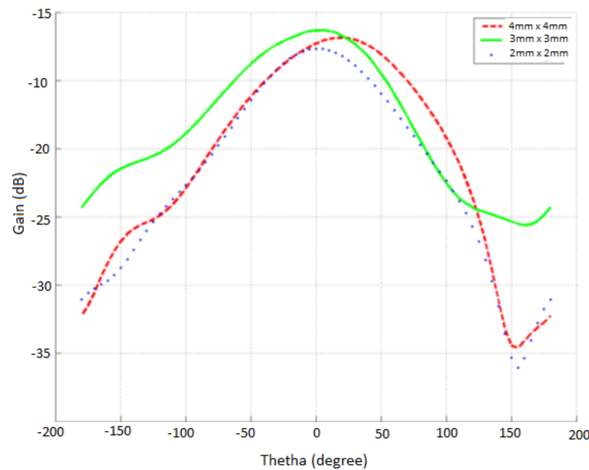


Fig. 4.11: Effect of the length of the ground plane on antenna radiation

Fig.4.11 illustrates the effect of ground plane dimensions on the radiation pattern; the antenna gain decreases not only with a large ground plane (because of metallic losses) but also with small one (Antenna S11 degradation). The design of the antenna thus involved a trade-off on the ground plan area (7.5mm²) to have better radiation and matching.

4.7 Linearly-Polarized electromagnetically-Coupled (EMC) Antenna

Gap coupling is a very important exciting method for microstrip printed antennas. A microstrip antenna and a feeding line or a feeding network are placed on single dielectric layer sharing a ground plane and are electromagnetically coupled together through a small gap between them. This configuration has many advantages over aperture coupled fed antennas. It allows use of same substrate for the feed structure and antenna. Although it doesn't offer shielding of a microstrip antenna from spurious feed radiation, this radiation in the back direction caused by the microstrip feed line and the coupling gap is undesirable. In practice, a ground plane located below the feed layer can be used to eliminate this radiation. On the other hand, there is no need of shielding structure or extension of ground plane that makes the antenna structure thicker and more complicated for the fabrication process.

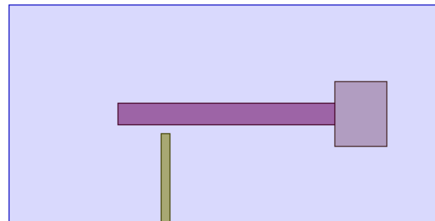


Fig. 4.12: Structure of electromagnetically-coupled microstrip antenna fed by microstrip line.

At higher frequencies especially in the mm-wave band, transmission losses in microstrip lines become significant. This feeding approach eliminates the problem of spurious radiation of the feed line in the backward direction and allows feeding microstrip antenna more efficiently in the mm-wave band. In addition, using aperture coupled antenna is complicated for integrating such an antenna structure with other passive and active PCB components of an antenna system. With respect to integrating an antenna with other planar components, using gap coupled configuration seems to be a better solution.

4.7.1 Antenna With feed Structure

A linearly-polarized electromagnetically-coupled microstrip antenna fed by microstrip line is proposed in this section. The rectangular microstrip antenna of width wa and length l_a is placed on the top surface of the substrate layer with relative permittivity ε_r and thickness h_s. A ground plane of the microstrip antenna is created at the bottom surface of this substrate layer. The microstrip antenna is shorted by a printed capacitive pad with length l_p and width w_p. The microstrip antenna is fed by microstrip line with width of w_f and length of l_f printed on the substrate layer. In order to simplify the antenna model, the antenna and ground plane is approximated by perfect electric conductor. This approach reduces computational time of the simulation runtime without loss of accuracy.

4.7.2 Simulation results

The EMC-VLA fed by microstrip line shown in Fig. 4.12 was simulated in ANSYS HFSS at 60 GHz. For the antenna design, we chose high permittivity dielectric silicon materials in order to achieve a wide operating bandwidth. Table 4.1 summarizes the design parameters of the antenna structure. In the simulation model, the metal plates are perfectly conducting and infinitely thin.

Tab. 4.1: Parameters of EMC-VLA fed by microstrip line.

Symbol	Value	description
l_a	0.48mm	Antenna length
w_a	0.05mm	Antenna width
l_p	0.12mm	Pad length
w_p	0.15mm	Pad width
h_s	0.25mm	Substrate height
w_s	5mm	Substrate width
l_s	5mm	Substrate length
w_g	5mm	Ground plane width

l_g	5mm	Ground plane length
y_f	0.2mm	Feed line distance from the center of the antenna
g_f	0.005mm	Feed line end gap to antenna

Figure 4.13 and 4.14 depicts the simulation results of the EMC-VLA fed microstrip line. The antenna has one resonance at 60 GHz and its reflection coefficient is lower than –10

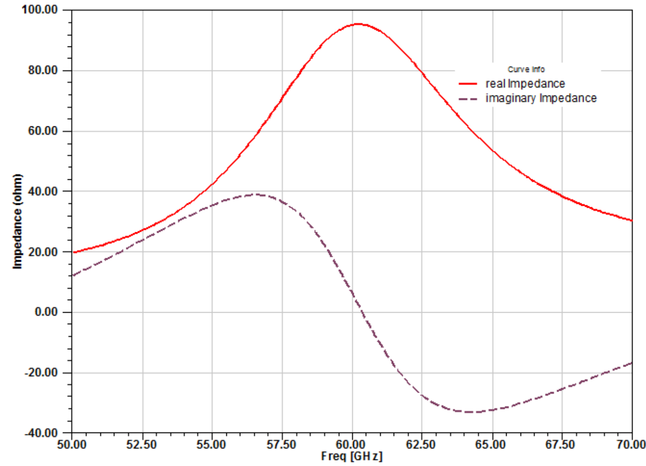


Fig. 4.13: Impedance of EMC-VLA fed by microstrip line

dB in the band from 56.8 GHz to 64.4 GHz which corresponds to a 12.6% impedance bandwidth. The radiation pattern of the antenna is simulated in the E-plane and H-plane for co-polarization (co-pol) and cross-polarization (x-pol) at 60 GHz (see fig, 4.15). From fig. 4.16, the EMC-VLA fed by microstrip line has a very low x-pol level in the main-lobe direction lower than –50 dB for both planes. The simulated gain of the antenna is -2.8dB.

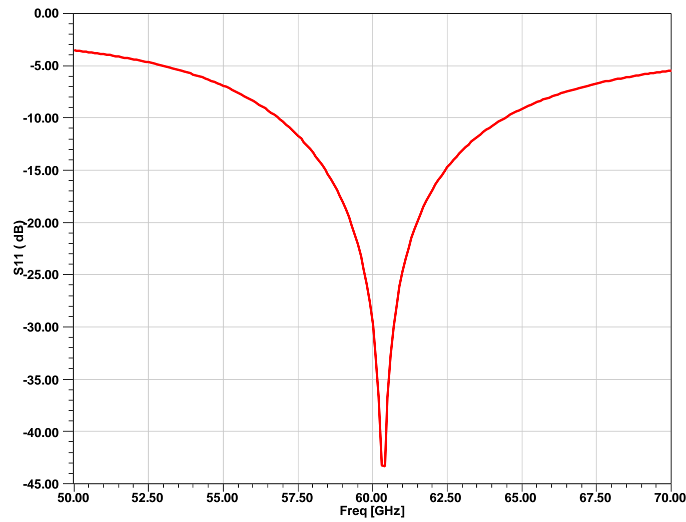


Fig. 4.14: Reflection coefficient of EMC-VLA fed by microstrip line.

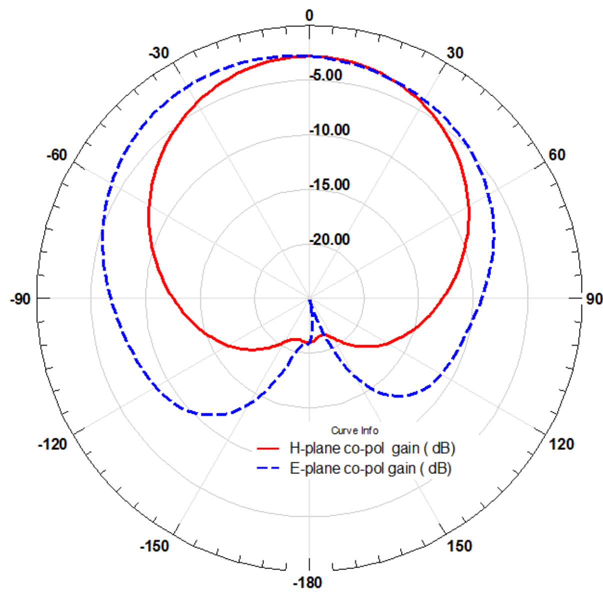


Fig. 4.15: Radiation pattern (Co-polarization) of EMC-VLA at 60 GHz (resistivity=20ohm_cm)

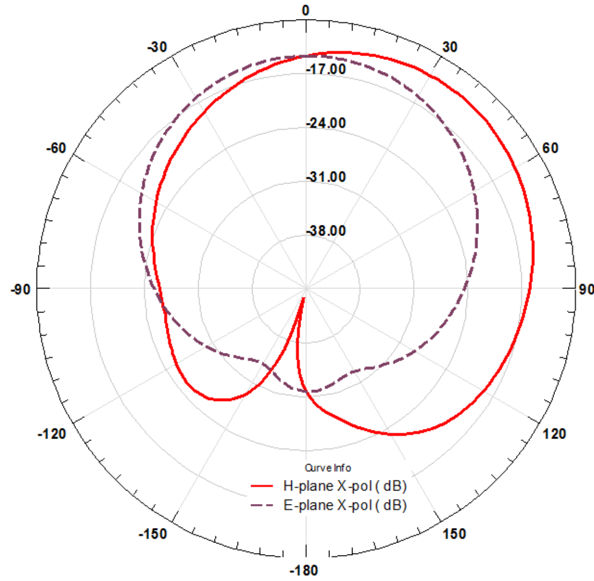


Fig. 4.16: Radiation pattern (cross-polarization) of EMC-MA at 60 GHz (resistivity=20ohm-cm)

4.7.3 Parametric study

The parametric study is usually more useful for practical antenna design thanks to the better understanding of the antenna behavior. By varying the main antenna parameters, we describe their effect on the reflection coefficient at the antenna input. The parametric study is carried out for the EMC-VLA structure fed by microstrip line shown in Fig. 4.12 with initial parameters summarized in Table 4.1.

4.7.3.1 Feed line Parameters

The size and position of the microstrip feed line and gap size are described using four parameters (l_f, w_f, y_f,l_g). In order to excite the microstrip antenna with maximum power, the feed line position y_f should be designed carefully. Therefore this parameter is included in the parametric study.

The effect of varying gap length l_g on the reflection coefficient of the EMC-VLA fed by microstrip line is depicted in Fig. 4.17. The gap l_g controls the amount of coupling energy

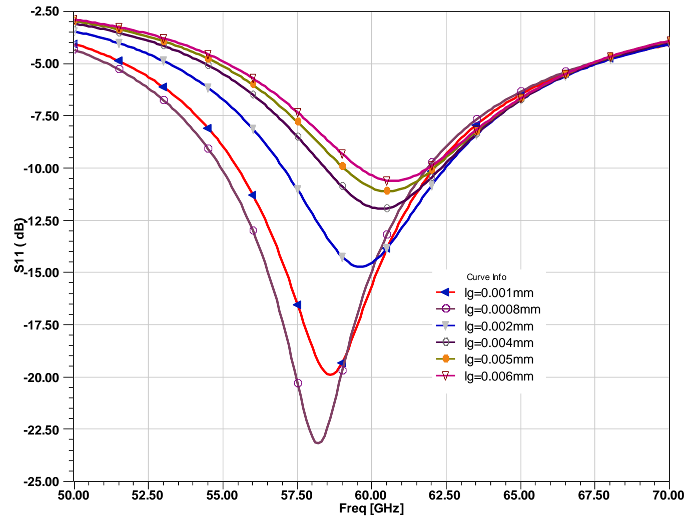


Fig. 4.17: Effect of gap length l_g on reflection coefficient of EMC-VLA fed by microstrip feed line.

between the microstrip feed line and the microstrip antenna. The coupling increases with the smaller gap l_g while the resonant frequency of the antenna increases, and vice versa. In the case where the gap size l_g is smaller or larger than the initial value, the microstrip antenna is under-coupled or over-coupled. This terminology is used in the description of the antenna design procedure.

Figure 4.18 shows the effect of varying feed line position y_f on the reflection coefficient of the EMC-VLA fed by microstrip line. Increasing y_f leads to increasing the resonant

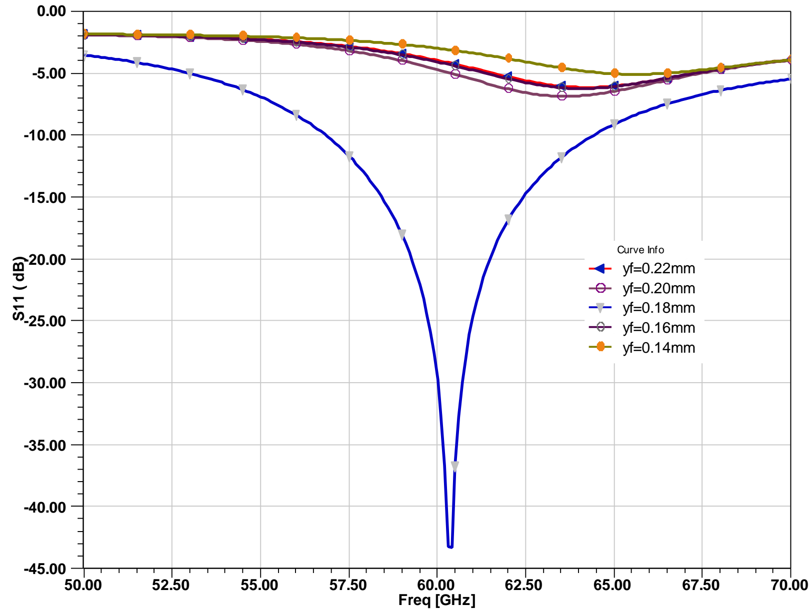


Fig. 4.18: Effect of feed line position y_f on reflection coefficient of EMC-VLA fed by microstrip line

frequency while retaining good Impedance matching. The resonant frequency of the antenna depends simultaneously on the antenna length l_a and feed line position. Obviously, the EMC-VLA fed by microstrip line can resonate with various sets of y_f and $l_a$at the same frequency. This assumption is proved in the next section.

4.7.3.2 Antenna parameters

As shown above, the resonant frequency of the EMC-VLA fed by microstrip line changes with the feed line position l_f. However, the resonant frequency also depends on the resonant length of the antenna l_a. As a first step, the effect of antenna length l_a, on the impedance is considered. All the parameters of the virtual current loop antenna as described earlier is kept the same, only the an antenna length is varied starting from 0.40 mm to 0.56 mm and the simulations were carried out. From Fig. 4.19, it can be seen that the resonant frequency shifts to higher values and the impedance decreases as antenna length decreases.

In addition, it is found that as antenna length decreases, the bandwidth becomes wider and the impedance matching gets better within most of frequency range. From these results, it suggests in proper design that the optimum length for given resonant frequency could be determined.

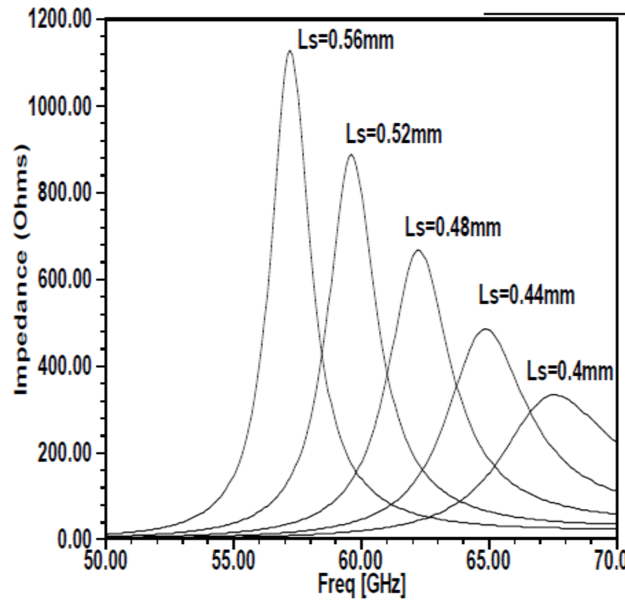


Fig. 4.19: Real impedance vs. frequency for different antenna lengths

Next, the effect of the width of the antenna on the impedance was studied. Here various width of antenna are chosen from 0.01 to 0.09 mm, and all other parameters of the antenna as described earlier is kept the same The typical simulation results for various widths are shown in Fig. 4.20. It can be seen from fig.4.20 that as antenna width increases, the resonant frequency shifts to the higher values and the real impedance decreases. The band width becomes wider as antenna width increases. Therefore, it can be balanced between the band width and impedance matching in the proposed design of virtual current loop antenna by controlling the width of antenna

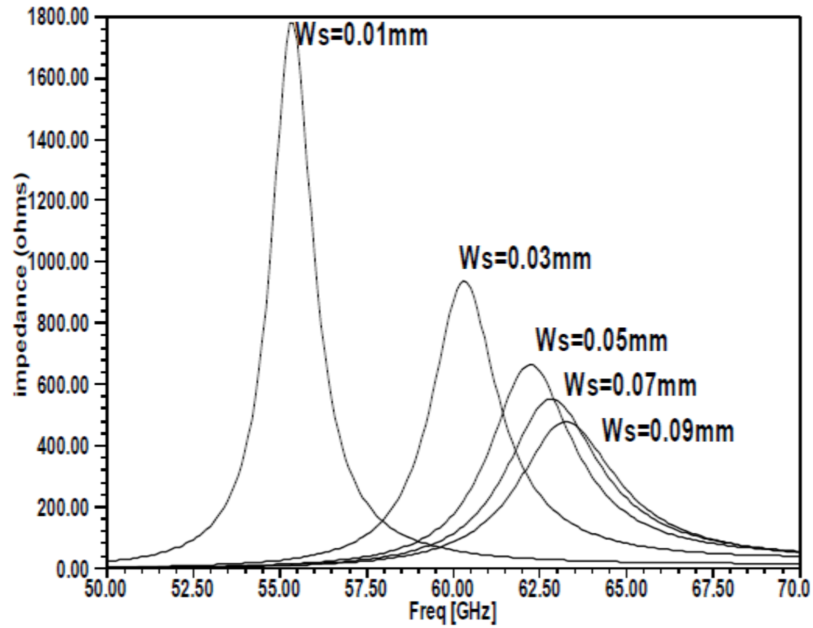


Fig. 4.20: Real impedance vs. frequency for different antenna

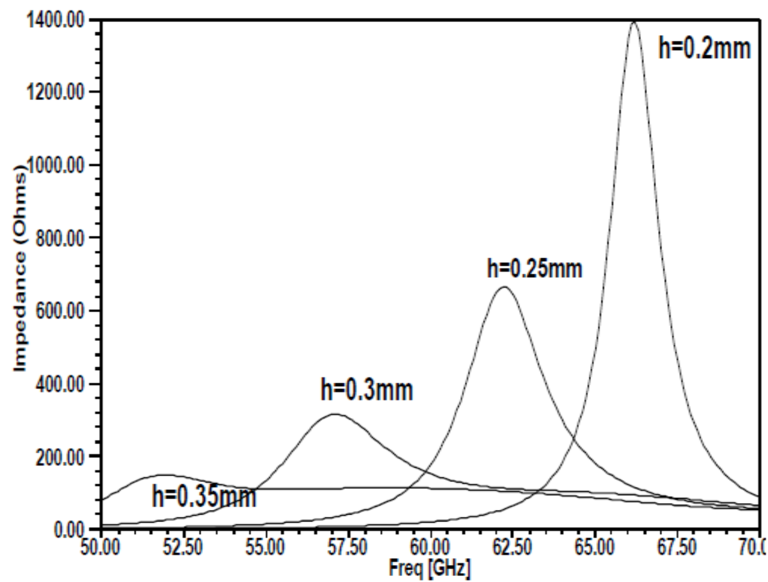


Fig. 4.21: Real impedance vs. frequency for different thickness

Third, the effect of the thickness of the substrate on the impedance was studied by choosing various thickness values. All others parameter are kept constant. As shown in Fig. 4.21, when the substrate thickness varies from 0.2 to 0.35 mm, it is found that the thickness of substrate affects resonant frequencies, bandwidth. Referring to Fig. 4.21, the better value for the substrate thickness can be selected for bandwidth enhancement. Substrate thickness

here was to to be determined 0.25mm from practical consideration. By observing the influence of the above three parameters on the antenna performance, it can be concluded that the length, the width of the antenna and substrate thickness control not only the resonant frequency but also impedance and bandwidth. The above parametric study of the antenna will be of immense help in the design of proposed antenna.

4.7.3.3 Dielectric substrate parameter

The impedance bandwidth behavior of the antenna is investigated for utilizing dielectric materials for the supporting layer with different resistivities and substrate thicknesses. We consider materials with resitivities (ρ = 5, 10, and 20ohm-cm) which are usually applied in antenna technique. In order to compare impedance bandwidth of EMC-VLAs fed by microstrip line designed on variable dielectric materials resistivities of the substrate layer, it is desirable to reach such a result that varies only in the investigated parameters substrate thickness h_s and resistivity ρ. Therefore, resonant frequency of the antenna was 60 GHz for all investigated values ρ and every EMC-VLA fed by microstrip line was optimized for the best impedance matching at 60 GHz can be achieved by changing the feed line position y_f and the gap length l_g. For the given resistivities ρ = 5, 10, and 20hm-cm, the length of the antenna corresponds to 0.48 mm, 0.50 mm, and 0.52mm, respectively. For reasons of comparison, the other antenna design parameters such as the antenna width w_a, substrate height h_s etc., remained at the initial size.

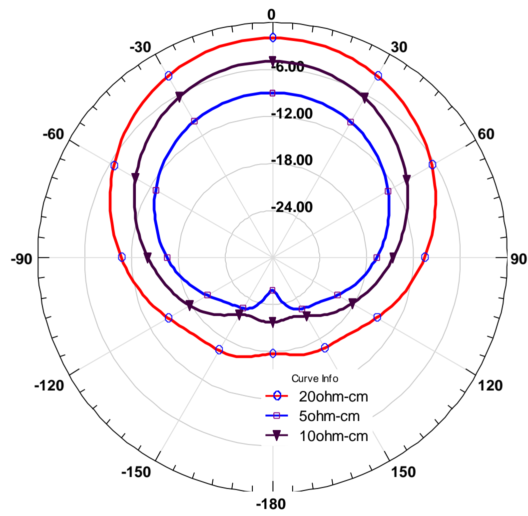


Fig. 4.22: Radiation pattern of EMC-VLA fed by microstrip line for varying resistivity ρ of substrate layer.

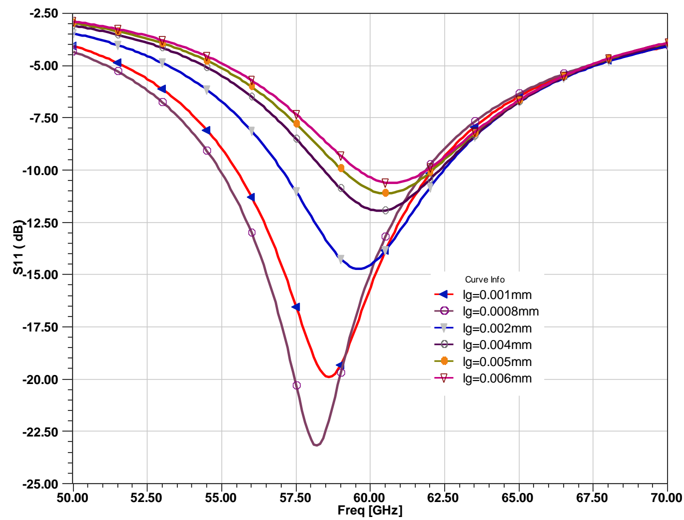


Fig. 4.23: Variation of impedance bandwidth for different gap length lg with resistivity ρ 20ohm-cm of Substrate layer.

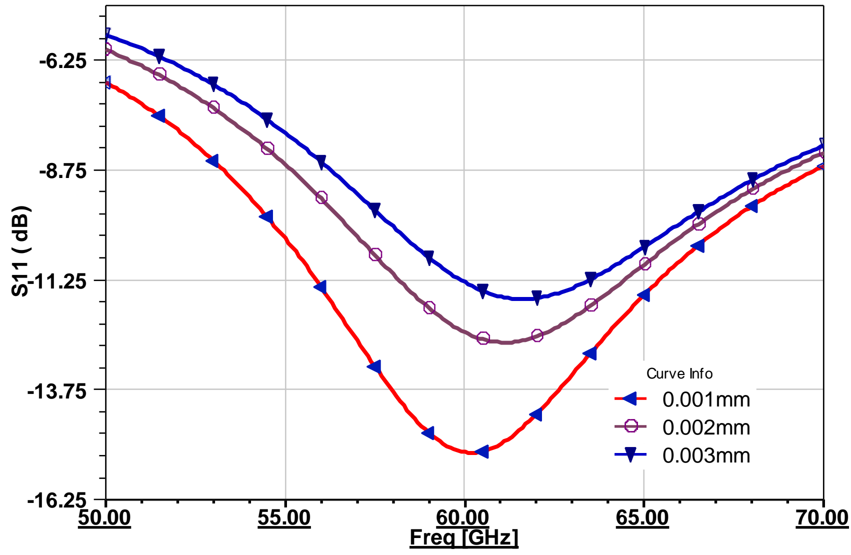


Fig. 4.24: Variation of impedance bandwidth for different gap length lg with resistivity ρ 10ohm-cm of Substrate layer.

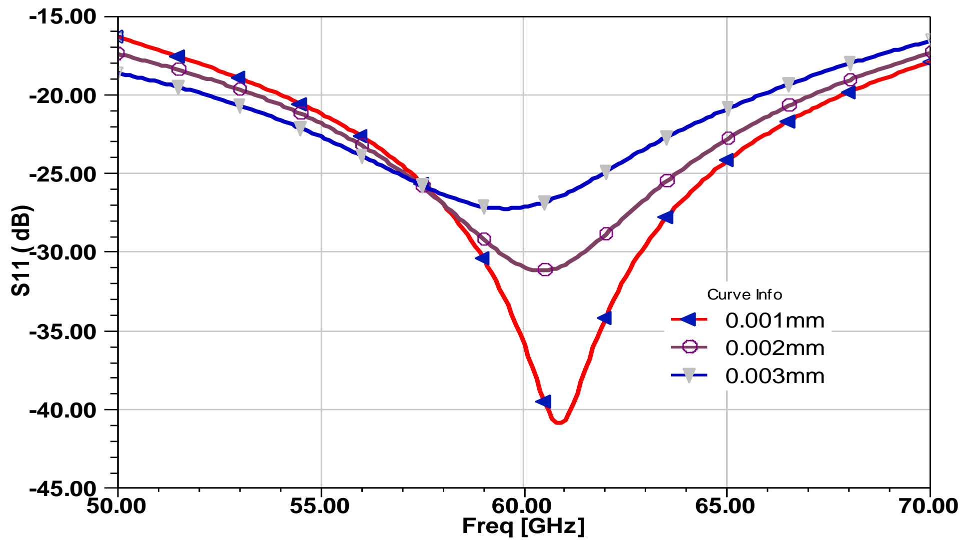


Fig. 4.25: Variation of impedance bandwidth for different gap length lg with resistivity ρ 5ohm-cm of Substrate layer.

The effect of the gap length and the resistivity ρ of the Substrate layer on the impedance bandwidth is investigated. Figures 4.23-4.25 show that wider impedance bandwidth is

achieved for a lower gap length with given resistivity of the substrate layer. Obviously, the impedance bandwidth slightly decreases with increasing gap length. In the case of using a higher permittivity material for the Substrate layer, a thicker material should be used.

Different virtual loop antennas have been designed for different frequencies on a low resistivity silicon substrate and simulated using HFSS software package. Fig. 4.26 shows that the antenna efficiency can reach more than 75% within the interested frequency range.

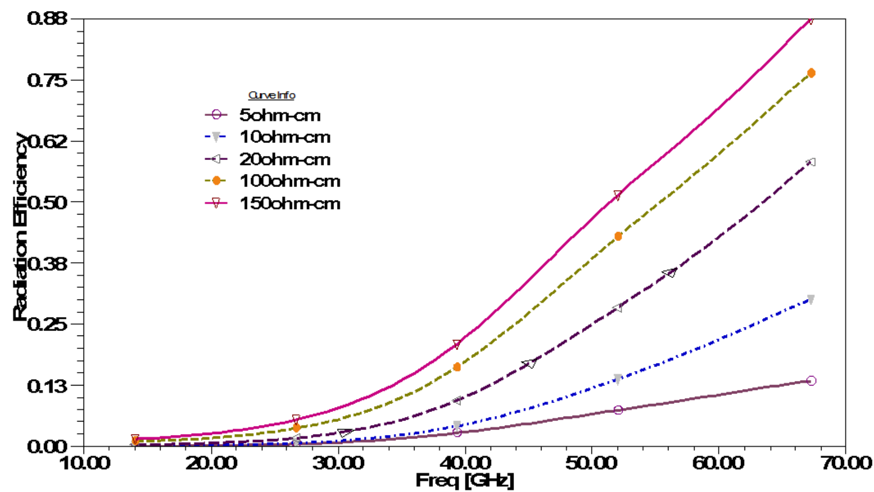


Fig. 4.26: shows efficiency versus frequency for various resistivities

4.7.4 Design Procedure

On the basis of the previous parametric study, we propose the following antenna design procedure:

1. The selection of the dielectric materials should be considered at the start of the antenna design according to electrical (impedance bandwidth, gain, etc.) and mechanical (antenna size, etc.) design requirements. Furthermore, the suitability of the

dielectric materials on the fabrication process should also be taken into consideration. The effect of material parameters used for the substrate layer was investigated in Fig. 2.9.

2. The initial antenna length la is calculated using conventional design equations considering a non-magnetic material [95]

$$l_a = \frac{\lambda_{eff}}{4} \tag{4.27}$$

where λ_{eff} is the effective wavelength given by

$$\lambda_{eff} = \frac{\lambda_0}{\varepsilon_{eff}} \tag{4.28}$$

where ε_{eff} is the effective dielectric constant

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} \tag{4.29}$$

A more accurate calculation of the initial antenna size is not required because as it was shown in the previous section, the resonant frequency of the EMC-MA fed by microstrip line depends on the resonant antenna length l_a and the feed line position y_f. Additionally, the antenna width w_a depends on the gap length l_g

3. In order to simplify the antenna model, the antenna is approximated by perfect electric conductor.

4. Selection of the position of microstrip feed line y_f and gap length l_g is a key step of the design procedure. The feed line position y_f from antenna end is given by [96]

$$y_f = \frac{\lambda_g}{4} = \frac{0.25}{\sqrt{\epsilon_r}} \cdot \frac{\lambda_0}{\sqrt{1 - \left(\frac{\lambda_0}{\lambda_c}\right)^2}} \tag{4.30}$$

Where λ_g is the guide wavelength at the operating frequency, λ_0 is the wavelength in free space at the operating frequency, and λ_c is the cutoff wavelength of the antenna. On the basis of the parametric study, the feed line position y_f should be chosen near the center of the antenna in order to reach the maximum impedance bandwidth and gain.

The gap length λ_g controls the amount of coupling to the microstrip antenna. But the coupling can also be controlled by the change of the antenna width w_a. Therefore, the choice of the initial size of the gap l_g is relatively complicated and depends particularly on the used materials and the initial antenna width w_a. It is suitable to try out several sets of l_g and w_a values. Then, the aim is to find out a starting impedance response that is not confined to the edge of the Smith chart. Once the input impedance of the antenna has a purely real part, the next step is optimizing the resonance to the required frequency by modification of the antenna length l_a and the amount of coupling by modification of the gap length l_g. In the case where the gap tends to overlap the antenna end, the antenna is under-coupled and its width w_a should be reduced. Note that the antenna width w_a also has a slight effect on the operating bandwidth. The feed line width w_f does not have a significant effect on the antenna performance so it can be varied for example between one tenth and one twentieth of the antenna length l_a.

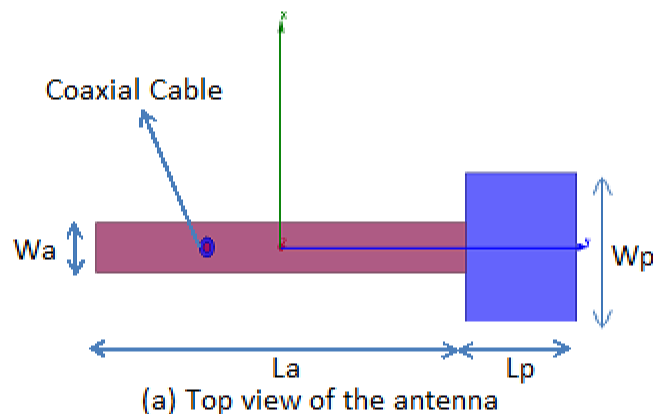
4.8 Linearly-Polarized Probe-Fed Virtual loop Antenna

Probe feeding, often referred to as a coaxial feeding, is one of the most utilized excitation methods for microstrip antennas [95]. It is usually performed using an inner conductor of

a coaxial line extended through a ground plane and connected to an antenna conductor. However, in the case of antenna arrays, a coaxial line is not suitable for the design of a feeding network. This feeding method can also be performed using a metal wire connected to the antenna and a microstrip line located under a ground plane of an antenna. The second scheme allows isolating filters or a feeding network consisting of power dividers and phase shifters from the radiating antenna via a ground plane. Nevertheless, additional shielding for a feeding line and PCB components is required which makes an antenna structure thicker and more complicated for the fabrication process. This can be avoided using microstrip technology for the design of components of a feeding network which are electrically shielded and also simpler for fabrication. In this section, a probe feed method technology for exciting a microstrip antenna is proposed in order to combine the benefits of microstrip antennas with the advantages of microstrip technology. The obtained results of this antenna have been published in [97].

4.8.1 Antenna Structure

The structure of the probe-fed virtual loop antenna (PF-VLA) is depicted in Fig. 4.27. The antenna system with overall dimensions length l_s and width w_s consists of dielectric layer, a capacitive pad of length l_p and width w_p and a ground plane of length l_g and width w_g. The antenna of width w_a and length l_a is placed on the top surface of the layer with



(a) Top view of the antenna

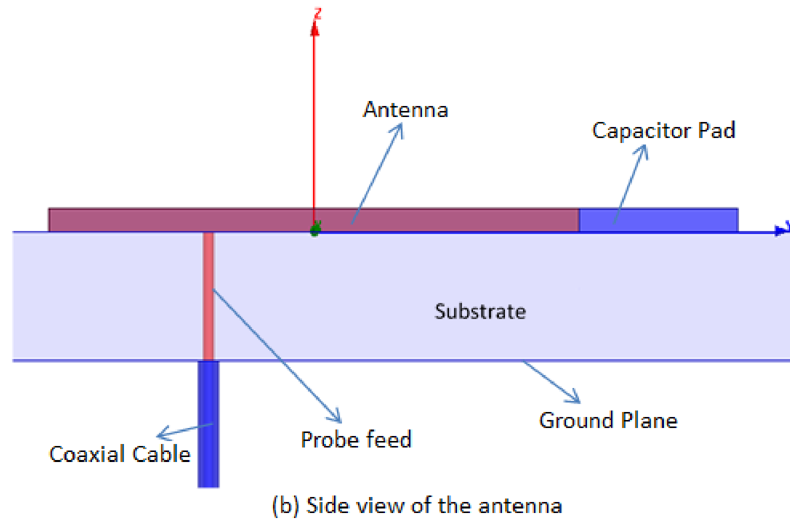


Fig. 4.27: Structure of probe-fed virtual loop antenna fed by coaxial line.

relative permittivity ε_r and thickness h_s. The ground plane of the microstrip antenna is assumed by the electric perfect conductor. The microstrip antenna is fed by a coaxial cable with relative permittivity $\varepsilon_r = 1$ and diameter. d_c In order to simplify the antenna model, the antenna structure is assumed by an electric perfect conductor and the coaxial cable consisting of perfect conductor solid walls. The port on the on the coaxial cable excites the fundamental TEM mode.

The microstrip antenna is excited from the coaxial line by a current probe composed of a metal wire with diameter d_p. The probe goes through the circular hole with diameter d_h etched in the dielectric substrate layer and is electrically connected to the bottom surface of the antenna at a distance x_p and y_p and to the antenna at a distance gap g_f. The detail of the feeding configuration is depicted in Fig. 4.27b.

4.8.2 Simulation results

The PF-VLA fed by coaxial cable shown in Fig. 4.27 was simulated in ANSYS HFSS at 60 GHz. We chose the same dielectric substrates for the antenna layers as in the case of the

EMC-VLA fed by microstrip line in Section 2.1. The coaxial cable operates in the fundamental mode TEM with the cutoff frequency 0 GHz. The design parameters of the antenna structure are listed in Table 4.2.

Tab. 4.2: Parameters of PF-VLA fed by coaxial line.

Symbol	Value	description
l_a	0.48mm	Antenna length
w_a	0.05mm	Antenna width
l_p	0.12mm	Pad length
w_p	0.15mm	Pad width
h_s	0.25mm	Substrate height
w_s	5mm	Substrate width
l_s	5mm	Substrate length
w_g	5mm	Ground plane width
l_g	5mm	Ground plane length
x_p	0mm	Probe feed distance from x-axis
y_p	0.2mm	Probe feed distance from y-axis
g_f	0.1mm	Feed line end gap distance to antenna

The simulation results of the antenna structure are depicted in Fig. 4.28 and 4.29. The reflection coefficient is lower than –10 dB in the band from 55.9 GHz to 61.7 GHz which

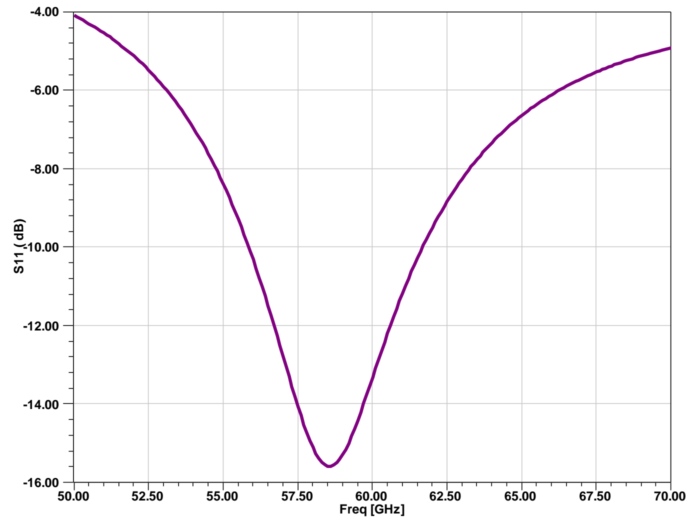


Fig. 4.28: Reflection coefficient of PF-VLA fed by coaxial cable.

corresponds to a 9.9% impedance bandwidth. In Fig. 4.28, the radiation pattern of the antenna is depicted in the

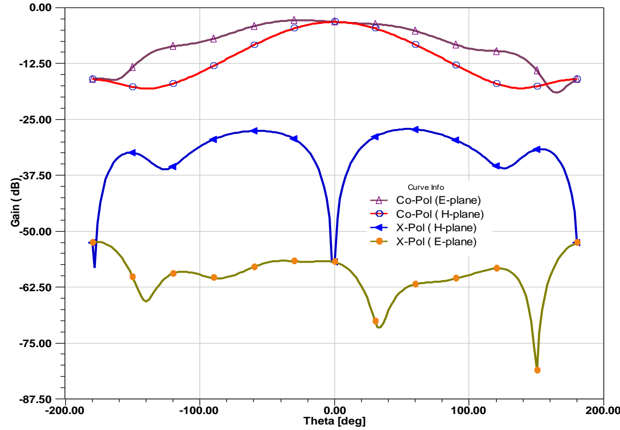


Fig. 4.29: Radiation pattern of PF-VLA fed by coaxial cable at 60 GHz (ρ=20ohm-cm)

E-plane and H-plane for co-pol and x-pol at 60 GHz. In the E-plane, the main lobe of the radiation pattern is slightly distorted due to the spurious radiation of the feeding probe. The antenna has a low x-pol level in the broadside direction (in the direction of the *z*-axis) about –33 dB in both planes. The simulated broadside gain is -2.68 dB.

4.8.3 Parametric Study

The parametric study is carried out for the antenna structure shown in Fig. 4.27 with the design parameters summarized in Table 4.2. By varying the probe parameters, we describe their effect on the reflection coefficient at the antenna input. The effect of varying probe

diameter d_p is investigated in Fig. 4.30. The figure depicts the reflection coefficient of four PF-VLAs fed by coaxial cable designed for the operating frequency 60 GHz. The investi-

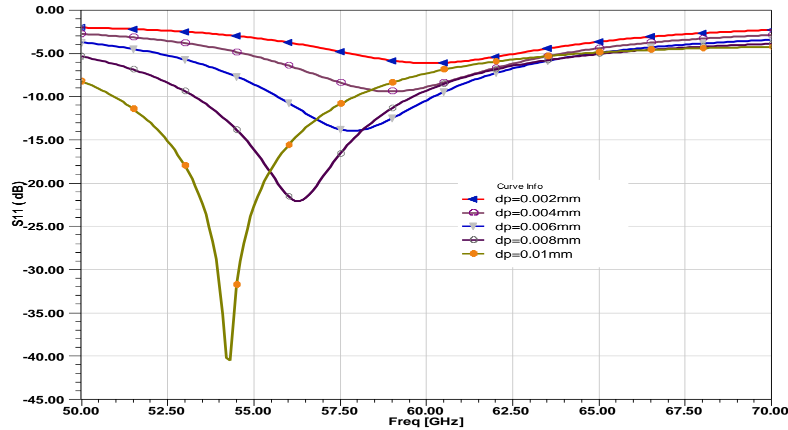


Fig. 4.30: Effect of varying probe diameter d_p on reflection coefficient of PF-VLA fed by coaxial cable

gated antennas varying in d_p within the range of 0.002mm to 0.01mm have an impedance bandwidth of range 7.7% to 12.6 %, respectively. The impedance bandwidths are varied significantly but the minimum and maximum frequency of the impedance band grows with decreasing d_p.

The next probe parameters are l_g and y_p. The effect of these parameters on the reflection coefficient response is investigated. In Fig. 4.31, the change of probe gap length in antenna

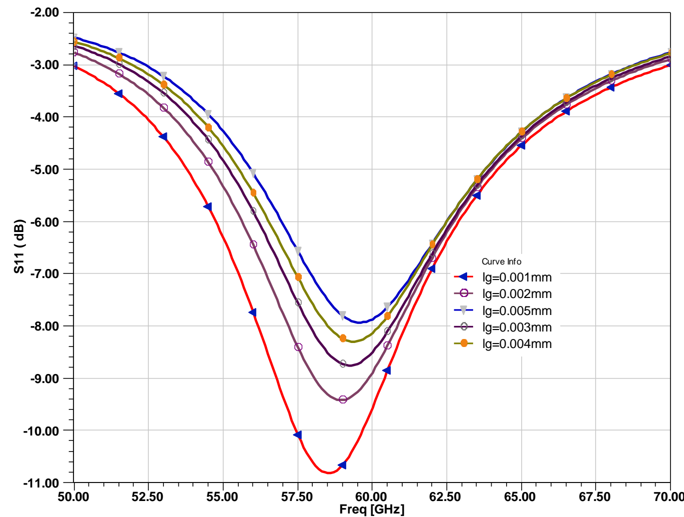


Fig. 4.31: Effect of varying probe gap length l_g on reflection coefficient of PF-VLA

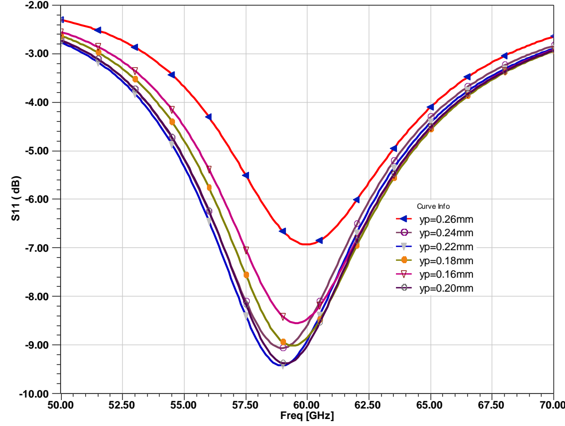


Fig. 4.32: Effect of varying probe position y_p on reflection coefficient of PF-VLA fed by coaxial cable

l_g has the effect of increasing or decreasing the resonance frequency and the amount of coupled energy from the coaxial line to the antenna. Further, the amount of coupled energy is controlled by changing probe position y_p in the probe, as shown in Fig. 4.32. Besides this, the change of probe position y_p has a considerable effect on the impedance bandwidth.

4.8.4 Design procedures

We propose the design procedure for the antenna in this order:

1. The selection of the dielectric materials for the antenna layers should be considered at the start of the antenna design according to electrical (impedance bandwidth, gain, etc.) and mechanical (antenna size, etc.) design requirements. Furthermore, the suitability of the dielectric materials on the fabrication process should also be taken into consideration.

2. The antenna structure shown in Fig. 4.27 is split into the antenna design and the coaxial cable and probe design. The antenna is designed in the same way as a conventional microstrip antenna fed by a coaxial probe. The initial antenna length can be calculated using equations (4.27), (4.28), and (4.29). This microstrip antenna is fed by a coaxial probe consisting of the inner pin with diameter d_p and the outer shielding with diameter d_c. Note that there is coaxial line and port is placed in the

plane of the end of coaxial line. This structure is optimized for the minimum reflection coefficient at the desired frequency by changing the antenna length l_a and the probe position y_p.

3. The coaxial line and probe is assumed as electric perfect conductor. The model consists of a air-filled coaxial line and a probe with the same size as the excitation

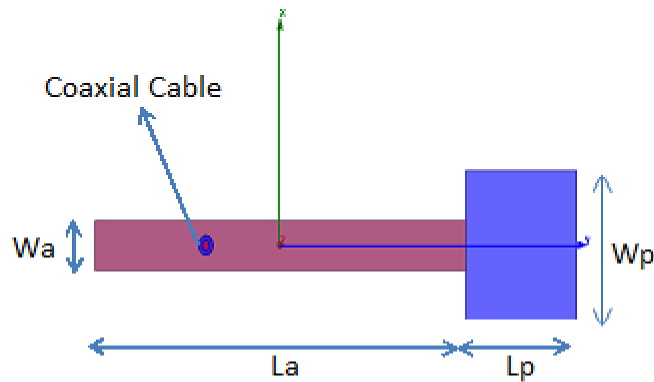


Fig. 4.33: PF-VLA design procedure – model of antenna layer.

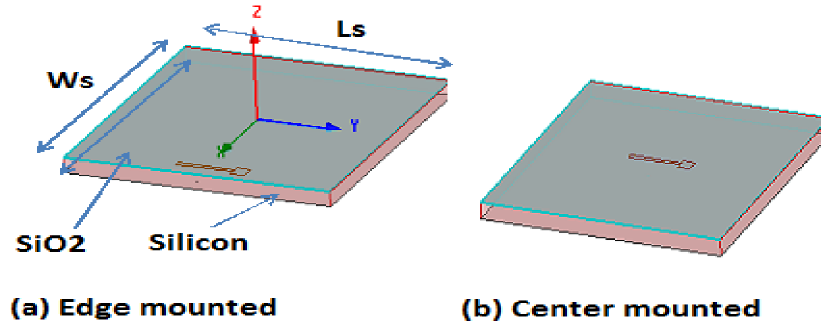
probe of the VLA in Fig. 4.33. The background of the model is defined to be a perfect electric boundary. In order to achieve a correct reflection coefficient response, the characteristic impedance of port is set to 50ohm. In this configuration, the reflection coefficient at port is optimized by changing the probe position y_p. The initial value of x_p *and* y_p is at the center line of the coaxial line and one quarter guide wavelength from the coaxial end wall, respectively

4. The antenna and feed line structures designed in the previous steps are put together and the reflection coefficient of the antenna structure is optimized. As mentioned in Section 4.8.3, the resonance frequency and the amount of coupling energy can be changed by l_a and l_g, respectively.

5. Finally, the feed line and the antenna structure is simulated. Some final simulation and optimization of the antenna structure due to a small change of the reflection coefficient after the conversion usually has to be performed.

4.9 Surface wave suppression in the silicon substrate

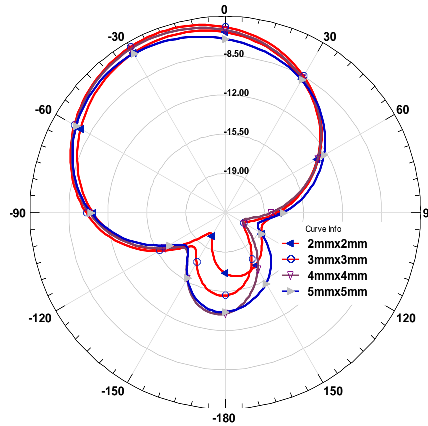
In general, any dielectric substrate can guide electromagnetic energy, as introduced in Section 2.1.4. The cut-off frequencies of the individual modes can be calculated from Equation



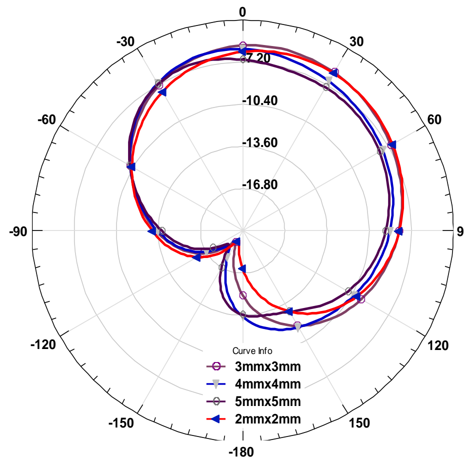
4.34: Considered antenna integration scenario for analyzing the chip size impact on the radiation characteristics

(2.34). From this, the 0th order TM mode can be determined to have a 0 Hz cut-off frequency and, consequently, can always get excited. The amount of energy that is launched in those mode by an antenna depends on the specific antenna type, its location and orientation with respect to the substrate, but also on the dielectric contrast between the substrate and the surrounding medium, usually air. The larger the permittivity of the substrate material, the more energy is confined in it. Since the real part of the dielectric constant of silicon, ε_r = 11.9, is rather large in comparison with typical microwave materials, like RO4003 with ε_r = 3.55, this topic requires special attention for a AoC design. This holds in particular for the doped silicon of typical (Bi-) CMOS processes since a significant portion of that confined electromagnetic energy will simply get dissipated into heat here. Furthermore, since silicon chips are of finite size, the excited substrate waves get partly reflected and partly radiated at the chip's edges. The radiated part superimposes with the waves that are directly radiated from the antenna and, hence, strongly affects the antenna's radiation pattern. Therefore, the exact overall pattern depends to a large extent on the dimensions of the chip. Figure 4.35 illustrates this relation. It shows the simulated gain patterns at 60 GHz of an integrated virtual loop antenna on CMOS chips of different dimensions l_s and w_s,

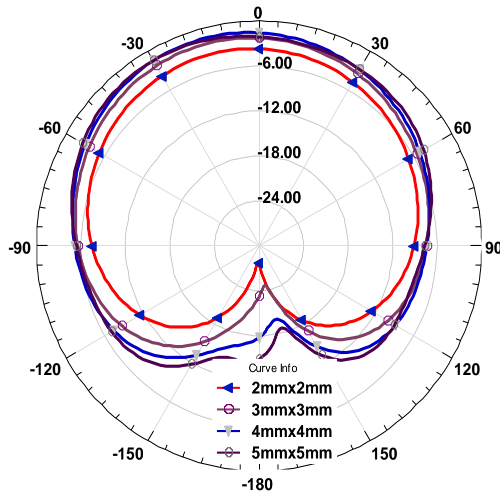
see Figure 4.34 for both configurations edge and center mounted. In order to reduce the amount of lossy silicon around the antenna, they were placed at a distance of 50μm from the edge of the silicon substrate, which has a thickness of 250μm and electric resistivity of 20Ω-cm. Also shown in table 4.3 are the simulated radiation efficiencies for each chip size. Since, generally, in a larger chip more energy is dissipated in the silicon substrate before it gets radiated from the chip's edge, a larger chip achieves a lower efficiency.



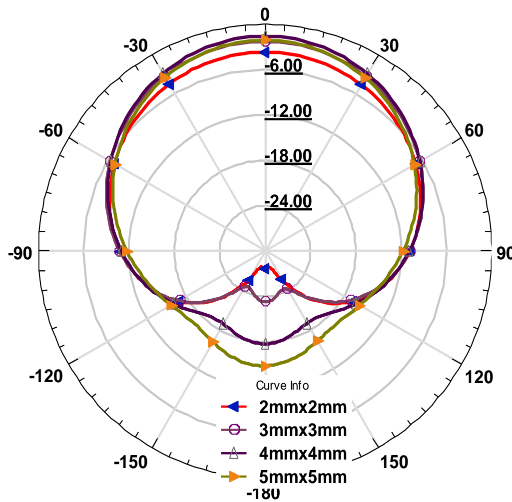
(a) E-plane Radiation pattern for edge mounted antenna (50μm from the edge)



(b) H-plane radiation pattern for edge mounted antenna (50μm from the edge)



(c) E-plane radiation pattern for center mounted antenna



d) H-plane radiation pattern for centered mounted antenna

Fig. 4.35: Considered antenna integration scenario and its simulated gain patterns for different chip sizes.

Table 4.3 shows the effect of ground layer on efficiency

Area	Edge mounted	Center mounted
l_s x $w_s mm^2$	Efficiency	Efficiency

$2 \times 2mm^2$	58.74%	22.53%
$3 \times 3mm^2$	55.33%	21.67%
$4 \times 4mm^2$	52.6%	22.37%
$5 \times 5mm^2$	44.2%	23.8%

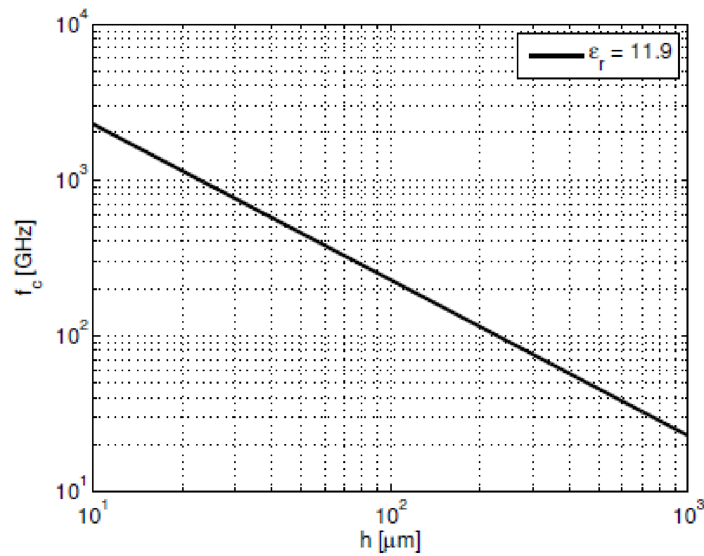


Fig. 4.36: Cut-off frequency, f_c, versus the thickness of a silicon substrate, h, according to Equation (2.34).

In order to enhance the radiation properties of the on-chip virtual loop antenna, a metal plate on top of the silicon can be implemented. By this simple measure, the substrate can be considered as a grounded dielectric slab, also known as surface waveguide, with corresponding surface-waveguide modes, see Section 2.1.4. The cut-off frequencies of its modes can be obtained from Equation (2.34). From this, the lowest-order TM mode (TM_0-mode)

can be determined to exhibit its cut-off frequency at 0 Hz, i.e., it can still always get excited. The lowest-order TE-mode (TE_1-mode), however, exhibits a non-zero cut-off frequency. Hence, for frequencies below cut-off, all guided TE-modes are suppressed. For a 60 GHz antenna design, for example, the thickness of the silicon substrate needs to be below 350µm

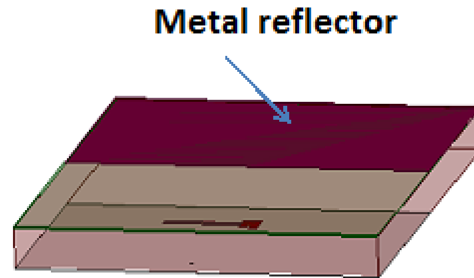


Fig. 4.37 Considered antenna integration scenario for analyzing the chip size impact on the radiation characteristics with metal top.

in order to avoid the propagation of TE-modes up to 66 GHz, as shown in Fig. 4.36.

Figure 4.38 shows the radiation patterns and efficiencies of the on-chip virtual loop antennas from Figure 4.24 when a rectangular metal plate is implemented at a distance of 650 m

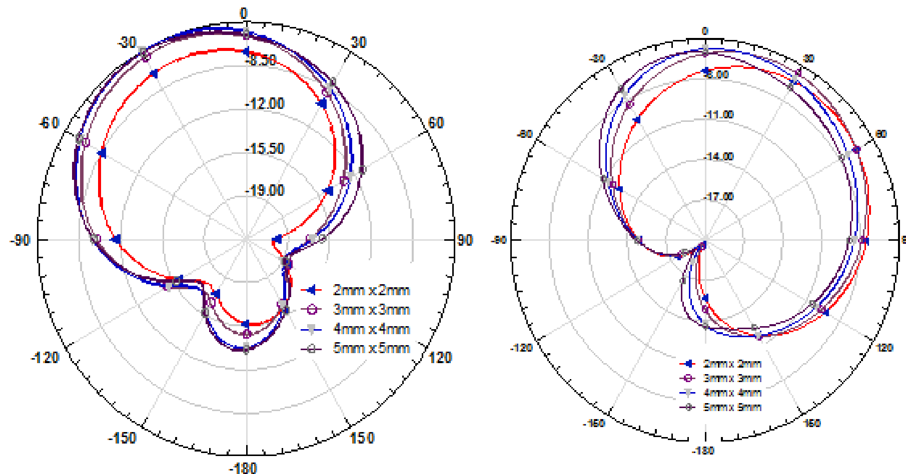


Fig. 4.38 Improved radiation characteristics of the antenna from by implementing a metal plate in the lowest layer of the IC’s back-end.

from the antenna, see Figure 4.37. By this, the plate also acts as a reflector with a length l_s while suppressing the TE-modes behind the reflecting edge. Therefore, the design can be understood as a rudimentary on-chip Yagi-antenna, see [66]. Comparing the results presented in Figure 4.37 with the ones from Figure 4.34, it is evident that the simulated radiation efficiencies are significantly improved. The radiation pattern still changes with varying chip size, however, but the sensitivity of its shape to the chip's dimension is reduced. The remaining chip size dependence might be caused by the TM_0-mode or the varying reflector length l_s.

Table 4.4 shows the effect of size of ground layer on efficiency with top metal

Area	efficiency
$2\ X2\ mm^2$	66.67%
$3\ X\ 3\ mm^2$	66.32%
$4\ X4\ mm^2$	60.09%
$5\ X\ 5\ mm^2$	53.66%

4.10 Ground plane configuration to implement on chip VLA

4.10.1 Radiating from topside without ground shield

The most obvious choice for on-chip antennas is to implement them as metal lines on top of the substrate and radiate upward into the air. In this subsection, we show why this may not be an effective solution by looking at a dipole antenna placed at the boundary of semi-infinite regions of air and dielectric (Fig. 4.39). Although this over-simplified configuration

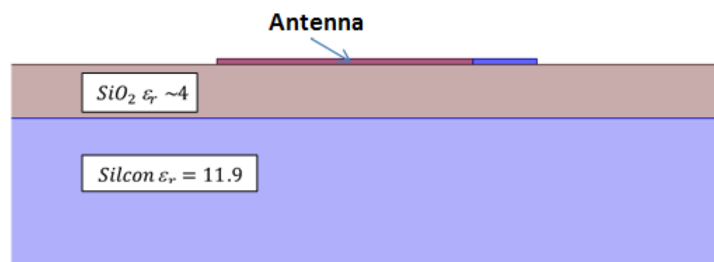


Fig. 4.39: Radiating from top side without ground shield

does not correspond to the practical setting, it guides us to better understand the effects of silicon high dielectric constant on antenna radiation pattern and efficiency. For a dipole antenna seeing the vacuum (or air) on one side and a dielectric on the other side, the ratio of the power coupled into air to the total radiated power is approximated3 by [99], [100]

$$\frac{P_{air}}{P_{total}} = \frac{1}{\varepsilon^{3/2}} \tag{4.31}$$

where P_{air} is the radiated power into air,P_{total}1 is the total accepted power and is the dielectric constant. From this formula for silicon dielectric, ε_r~11.9 a very small portion of the power radiates into the air (about 3%) and the rest of it couples into silicon. This demonstrates that without any mechanism to reroute the power coupled into silicon substrate, it is not possible to implement a high efficiency antenna on silicon this way.

4.10.2 Radiating from topside with on-chip ground shield

Another possible option is to incorporate an on-chip ground shield and trying to reflect the radiated energy upward, thus preventing it from coupling into silicon, as shown in Fig. 4.40. In this case, the on-chip antenna and the ground shield have to be placed inside the

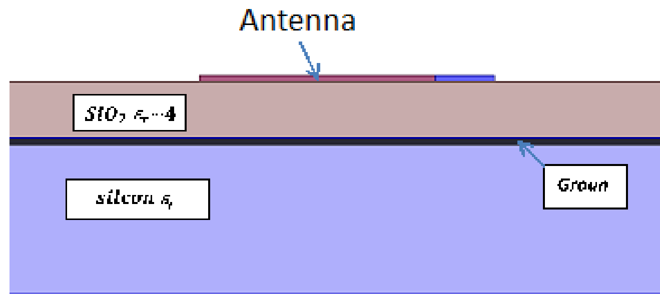


Fig. 4.40: Radiating from top side with on-chip ground shield

SiO_2 due to process limitations. For such a configuration, the distance of the antenna and the ground shield affects the antenna-ground coupling and determines the radiation resistance [101], [102]. Unfortunately, the distance between the bottom of the top metal layer and the top of the lowest metal layer rarely exceeds 15µm today's process technologies. This small antenna-ground spacing causes a strong coupling between the antenna and the

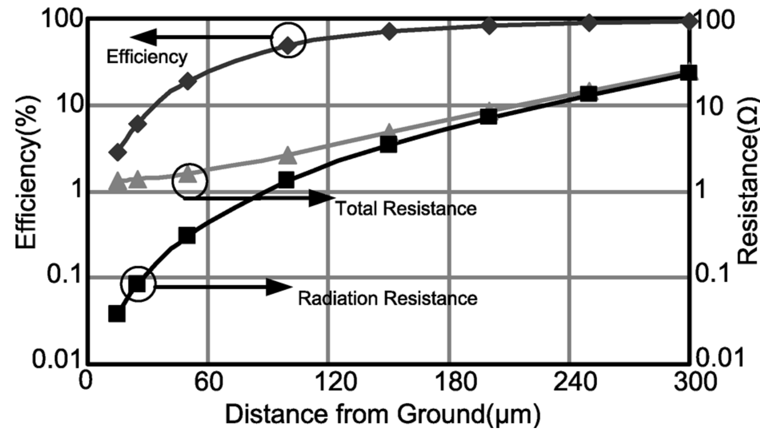


Fig. 4.41: radiation resistance and efficiency (antenna with on chip ground plane)

ground layer which lowers the all-important radiation resistance. Fig. 4.41 shows the results of the electromagnetic simulations of a copper virtual loop antenna (VLA) placed over a metal ground plane with a SiO_2 dielectric, sandwiched in between. The antenna dimensions are 5μmx50μ mx480μm The antenna-length is equal to a length of a resonant length at 60GHz which is placed in the boundary of semi-infinite regions of air and SiO_2. Based on this simulation, Fig. 41 shows that,for a spacing of 15μm between the antenna and the ground layer, the radiation resistance is very small (less than 0.1ohm) hence the total resistance is dominated by the ohmic loss of the copper resulting in a radiation efficiency of less than 5%. An option to increase the efficiency of the antenna seems to be the implementation of an off-chip ground shield to increase the distance between the antenna and its ground layer. We will discuss this case in the next sub-section.

4.10.3 Radiating from topside with off-chip ground shield

As shown in Fig. 4.42, an off-chip ground shield can be placed underneath the silicon substrate. In this case, the silicon substrate thickness is much larger than the SiO_2 layer and

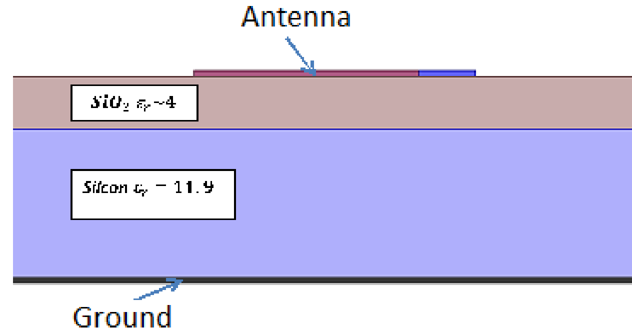


Fig. 4.42. Radiating from top side with off-chip ground shield.

effectively we are dealing with a high dielectric constant substrate (ε_r= 11.9). Unfortunately, because of the high dielectric constant of silicon and the large substrate thickness

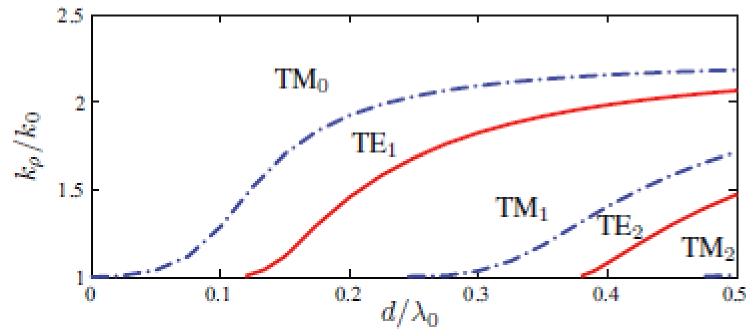


Fig. 4.43 TMx and TEx modes of Surface wave

(100 µm or more), most of the power gets absorbed into surface-wave power [99]–[104]. HFSS simulation was done. The results shown in fig. 4.43. Both TE and TM surface waves can be excited on a grounded dielectric substrate. The cutoff frequency of these mode is given by [106].

$$f_c = \frac{nc}{4d\sqrt{(\varepsilon_r - 1)}} \tag{4.32}$$

where c is the speed of light, and $n = 0$, 1, 2,3, for the TM_0,TE_1, TM_1,TE_2, … surface mode. Note that the TM_0 mode has a zero cutoff frequency, so that it can be generated for any substrate thickness d. As shown in fig. 4.43, as the substrate becomes electrically thicker, more surface modes can exist and the coupling to the lower order modes can become

stronger. For thin substrates (***d*** $< 0.01\lambda_0$) surface wave excitation is generally not important. For thicker substrates surface waves may have a detrimental effect on the antenna performance. Surface wave power launched in an infinitely wide substrate would not contribute to the main bean1 radiation and so can be treated as a loss mechanism. **A** radiation efficiency can then be defined as

$$e = \frac{P_{rad}}{P_{rad} + P_{sw}} \tag{4.33}$$

where P_{rad} is the power radiated via space wave (direct main beam power), and P_{sw} is the power coupled into surface waves. $P_{rad} + P_{sw}$ is then the total power delivered to the printed antenna element. Dielectric loss is ignored here. The effect of a finite-sized substrate would

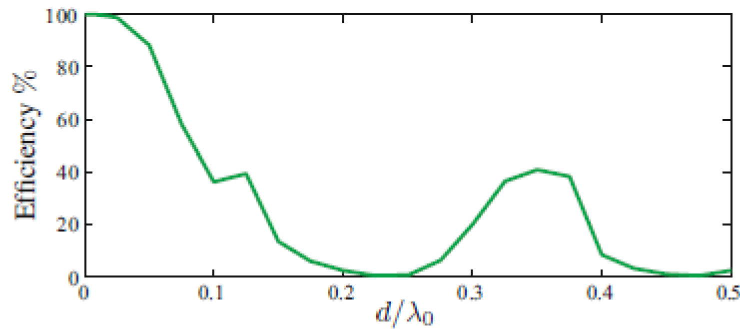


Fig. 4.44 efficiency vs substrate thickness

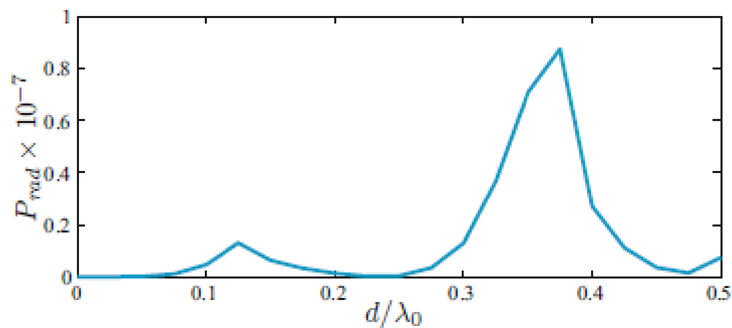


Fig. 4.45: radiated power for a grounded VLA

be to diffract the surface waves from the substrate edges, possibly causing undesirable effects on side lobe level, polarization, or main beam shape. Surface waves could also be diffracted by or coupled to feed lines or components on the substrate. Fig. 4.44 shows simulation results of efficiency **(e)** versus substrate thickness *d* for designed antenna, for ε_r =

11.9. Observe that *e* approaches 1.0 as *d* decreases 0, since surface wave excitation is negligible for very thin substrates. As *d* gets larger the TM_0 surface mode becomes stronger, reducing efficiency *e*. However, the radiated power becomes greater as *d* increases, so that *e* levels off and starts to increase for d > $0.1\lambda_0$. At d = $0.2\lambda_0$, the next surface mode (TE_1) starts to propagate, causing a slope discontinuity in *e* and a decrease in *e* as this mode becomes more strongly coupled. This type of slope discontinuity is also seen in related dielectric covered antenna problems [107] If we assume the thickness of SiO_2 is negligible compared to that of silicon, then the surface-wave power can be simulated in HFSS. Based on these results, radiated power and surface-wave power are plotted in Fig. 4.45 and Fig. 4.46, respectively. As is shown in Fig. 4.46, at 60 GHz the maximum radiated power, which occurs at the silicon substrate thickness of $0.14\lambda_0$ and $0.37\lambda_0$ However, at this substrate thicknesses, the power in all the surface wave modes is more than radiated power (Fig. 4.46), which indicates that even in the case of lossless silicon substrate, the power wasted

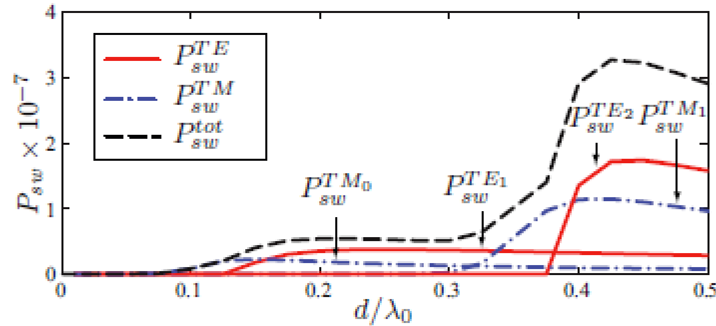


Fig. 4.46. Surface wave power for a grounded VLA

in the surface wave modes is 2.7 times greater than the useful radiated power. It is important to realize that for a lossy and finite-dimensional substrate, the surface-wave power is either dissipated due to the substrate conductivity or radiated from the edge of the chip and that often results in an undesirable radiation pattern

4.11 Effect of finite conductivity and metal thickness

The model that is introduced in Section 3.3 assumes that the metal can be approximated as a perfect electric conductor with zero thickness. In this section, the effects of finite conductivity and metal thickness are analyzed to verify the validity range of this assumption.

The antenna is modelled with copper in Ansoft Hfss to investigate the effect of finite conductivity and these results are compared with the results of the PEC antenna. The input

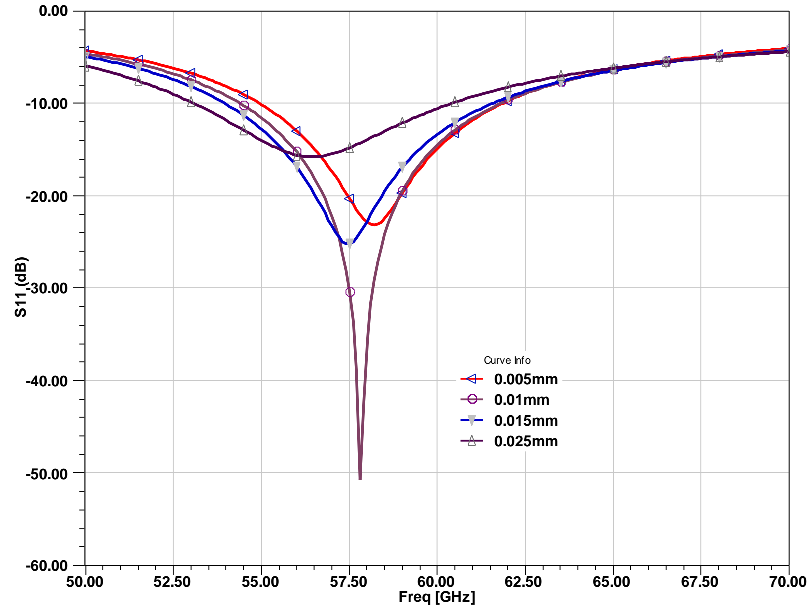


Fig. 4.47: Reflection coefficient of the VLA for different metal thicknesses.

impedance, reflection coefficient, directivity and gain of both antennas were almost identical and therefore it is concluded that the effect of finite conductivity is not important as long as well-conducting materials are used like copper, silver or gold. Note that in this comparison, the feed line of the antenna has not been incorporated. A long feed line with finite conductivity introduces additional losses that should be accounted for. However, the use of metal with a finite conductivity in the antenna itself does not affect the input impedance significantly.

The input impedance of the antenna is sensitive for changes in metal thickness t_m. Especially the thickness of the feed has an impact on the input impedance and therefore also on the reflection coefficient of the antenna. The reflection coefficient S_{11} is related to the input impedance as

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.34}$$

where Z_0 is the characteristic impedance of the transmission line that is connected to the antenna. Here, the feed line should be designed for a characteristic impedance Z_0=50Ω.The reflection coefficient is compared for different thicknesses of the metal layers, where the thickness is defined in section 4.4.2. To obtain a fair comparison, the thickness of the ground plane is not considered, since it is not incorporated in the models. Fig. 4.47 shows the results for metal thicknesses of 0, 5, 15 and 25µm. It is shown that the metal thickness affects the reflection coefficient and therefore the assumption that the metal can be modelled as if it has zero thickness is not always valid.

Close examination of the influence of metal thickness has shown that the thickness of the antenna feed and antenna have dominant effect on the reflection coefficient. In comparison, the finite thicknesses of the ground plane do not affect the reflection coefficient much. From this observation, it is tried to improve the accuracy of the HFSS model by positioning the zero thickness feed layer of this model at the top of the actual feed. Since the field is mostly confined between the top of the feed and the bottom of the ground plane, the currents on the top of the feed are the strongest. Therefore, this feed position improves the accuracy of the model. It is observed that the adjusted feed position of the zero-thickness feed improves the accuracy of the HFSS model indeed.

4.12 ELECTROMAGNETIC INTERFERENCE

A major concern with AoC solutions is electromagnetic interference (EMI), which causes mutual coupling and affects the proper operation of the antenna and circuits. An understanding of the coupling mechanisms, impact of the process technology, grounding effects, guard rings, shielding, filtering, and decoupling is necessary to reduce EMI.

For the AoC solution, the circuits, especially their power lines, inductors, and capacitors will detune the antenna and affect its radiation patterns. Hence, the layout of the antenna

should be kept away from them as far as possible [105]. On the other hand, the antenna couples to the circuits, especially the sensitive low noise amplifier, may degrade their performance. Two major coupling mechanisms are known, one is the substrate coupling and the other is the power-line coupling. The use of differential topology in the antenna and circuits can mechanism can be effectively prevented by using filtering and decoupling techniques implemented with the power lines

Chapter 5 Measurement and Verification

5.1 Antenna chip fabrication

The antennas for the experimental studies in this work were fabricated in nano fabrication center lab at the University of Minnesota, with the generous help from various professors and students associated with the lab.

The antenna chips are built on Boron doped p-type, (100) oriented, 4-inch silicon wafers. The resistivity of one type of wafers is 10Ω-cm, which represents the normal wafers used for CMOS IC fabrication. That for the other type is greater than 10k Ω-cm, which represents the higher end of the silicon wafers available for IC fabrication. The metal used for building the antenna structure is Aluminum, which is sputtered and later patterned using photolithography. Its thickness is varied for some wafers in order to study the effects of the thickness on the antenna performance.

The whole antenna chip fabrication process can be roughly divided into 9 steps.

Step 1: First, checking the quality of the surface (surface should be smooth and bright, without mechanical injury), and then using the 1st liquid (27% NH_4OH: $30\%H_2O_2$:deionized water = 1:2:5) and the 2nd liquid (37% HCl: $30\%H_2O_2$: deionized water = 1:2:8) wafer cleaning was done. The SiO_2 with thickness 1.1 μm was performed at 10 min of dry oxygen and 45 min wet oxidation, and the last 10 min of dry oxygen at a temperature of 1100°C oxygen flow 500 mL/min.

Step 2: Deposit aluminum film using sputtering

In this step, we deposit an aluminum foil on top of the silicon wafer using DC sputtering.

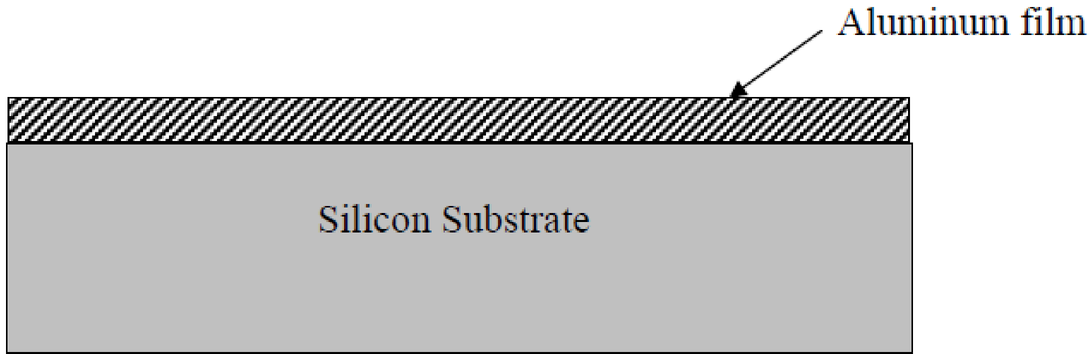


Fig. 5.1: The wafer structure after step 1

The sputtering system available in the lab is model ISE-OE-PVD-3000 from Innovative Systems Engineering, Inc. It has one deposition chamber and one manual load lock chamber. The deposition is done with one of the two available DC guns. The process gas used for the deposition is Argon at the pressure of 5mtorr. At a DC power level of 40W and room temperature, the deposition rate is around 1Angtrom/sec.

After the deposition, the wafer should be covered by a uniform aluminum film as shown in Figure 5.1.

Step 3: Spin coat the wafer with photoresist

In this step, we apply a layer of photoresist on top of the aluminum foil.

The photoresist (PR) used in this fabrication is Microposit SC-1805 positive photoresist manufactured by Shipley, Inc. It was applied with a model RC-8 spin coater from Karl Suss. The obtained film thickness was about 0.5µm when the wafer was spun for 30 sec at a speed of 3500rpm. In order to increase the uniformity of the PR film, the adhesion promoter, HMDS, was first applied on the wafer with the same process prior to the application of the PR.

After this step, the wafer should have a structure as shown in Figure 5.2.

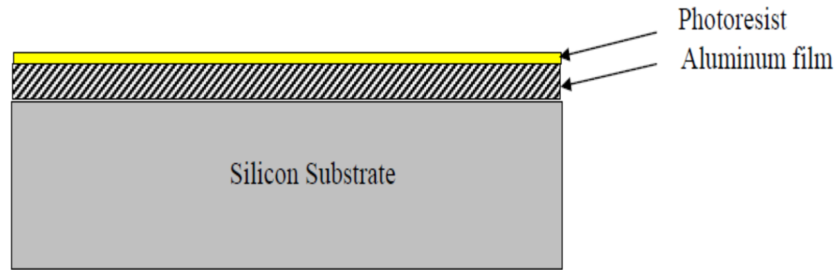


Fig. 5.2: Wafer structure after step 2

Step 4: Soft bake the photoresist

The PR is required to go through a soft baking process before it is exposed, which can be done with either a hot plate or a convection oven. In this fabrication, a convection oven was used to bake the wafer at 95°C for 30 minutes.

Step 5: Expose the photoresist to UV light

After soft baking, the PR is exposed to UV light using a Karl Suss model MA6 mask aligner. The UV source has a light intensity of 35.5mW/cm2 at a wavelength of 365nm. The best exposure time was experimentally found to be 4sec. The soft contact exposure mode was used in this fabrication.

The photo mask was manufactured by Adtek Photomask, Inc. It was a clean field mask since positive photoresist was used for this fabrication. The mask uses an anti-reflective Chrome coating on a 4×4 in^2 square soda lime glass plate. It has a minimal feature size of 10μm and critical dimension tolerance of ±1.0μm.

Step 6: Develop the photoresist

The exposed photoresist layer was developed using the MF-319 developer. At room temperature, the wafer was immersed in the developer for 60 sec. The wafer structure after developing is shown in Figure 5.3.

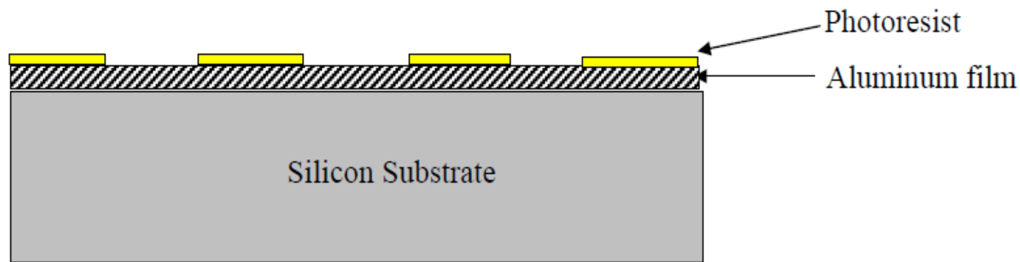


Fig. 5.3: Wafer structure after PR developing

Step 7: Hard bake the photoresist

The PR went through a hard baking process after it was developed. This was achieved by putting the wafer in a convection oven at 120°C for 30 minutes.

Step 7: Etch the aluminum film

In this step, the unwanted aluminum is removed from the wafer using a wet etching process. The etchant is a mixture of Phosphorous acid, Nitric acid, Acetic acid, and water with a ratio of 16:1:1:4.

The wafer is immersed in the etchant and consistently agitated for about 2 minutes at a temperature of 40°C. It is rinsed thoroughly with de-ionized (DI) water right after the immersion.

The wafer structure after etching is shown in Figure 5.4.

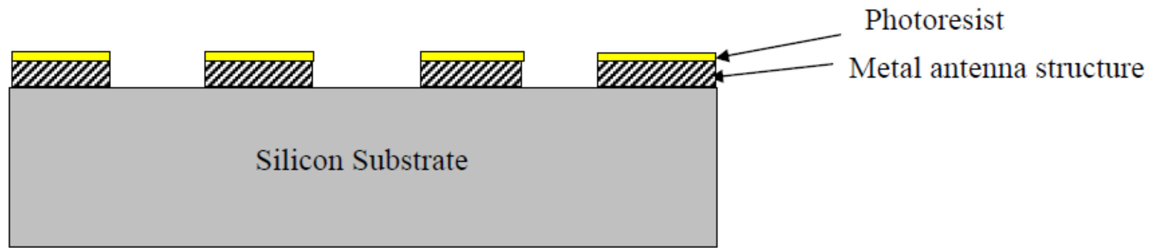


Fig. 5.4 Wafer structure after etching

Step 8: Remove the unexposed photoresist

In this step, the unexposed photoresist remaining on top of the aluminum structure is removed using Acetone.

After this step, the desired antenna structures are available on top the silicon substrate. The finished wafer structure is shown in Figure 5.5.

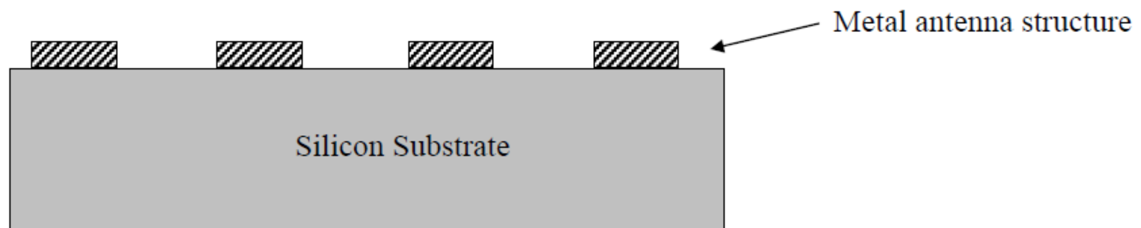


Figure 5.5 Wafer structure after step 9

Step 9: Measure the aluminum thickness and cut the wafer into antenna chips

The aluminum layer thickness is measured with a Veeco Dektak3 ST surface profiler. After the measurement, the wafer is cut into chips with a diamond saw or a glass scriber.

5.2 Measurement of antennas on CMOS ICs

Measurement is necessary to prove that the specific requirements of an antenna, which are designed to conform to the specifications, are satisfied. All the antenna performance parameters listed in section 2.3, i.e. radiation pattern, gain, efficiency, polarization, and input

impedance, deserve serious measurement efforts. But accurate measurement of most parameters for antennas on CMOS chips is generally difficult partly because the absolute values of the results are often small due to their small sizes and thus more vulnerable to systematic or random errors. One may say, the smaller the antenna size, the harder it is to determine its performance [108]. The most common problems with small antenna measurement include the coupling of nearby materials, the existence of unbalanced currents on the connecting cables, limited accuracy of the equipment, and so on. Even particular considerations are given to the measurement of small antennas, there may still be some cases where no effective method can be found [108].

Other than being extremely small, an antenna on CMOS IC is supposed to work by itself, which means no cable or wire connection of any form is made to it while it is in the working environment. When we try to connect it to the standard equipment using wires or cables, the field and the current distributions on the antenna are easily distorted. Consequently, the accuracy of the measurement may become comprised, or even nonexistent.

The accurate measurement of some of the parameters, such as the radiation pattern, requires fairly sophisticated equipment like antenna chambers or antenna ranges, which are not available in the departmental lab or readily available at other facilities. On the other hand, the figure of merit that is most important for the antennas on chips (AOC), its available power under given condition, is extremely difficult to measure using standard equipment because of the cable connection problem mentioned earlier. As a result, certain unconventional method must be developed in order to get meaningful measurement results for the on-chip antennas in this research.

5.2.1 Measurement Setups

Generally speaking, the ideal measurement setup for the antennas on CMOS ICs should satisfy the following three conditions:

1. The feeding to the antenna should be the same as that in its actual use. The use of wire or cable connections should be avoided if possible.

2. The measurement should be accurate and stable.

3. The measured data should be easy to collect and analyze.

Since the maximum available power is most important for an on-chip antenna, the setups we are going to discuss next are primarily for its accurate measurement. Some key antenna parameters, such as antenna directivity pattern, can be measured easily once the available power can be determined accurately.

5.2.2 Measurement Using Standard Equipment

Most RF measurement equipment, such as the vector network analyzer and the power meter, use coaxial cables to connect the devices under test (DUT). Because the on-chip antennas do not use probe feed, there is the problem of getting it connected to the cable.

In order to overcome the problems associated with the close proximity of the probe to the AoC, an extended feed line for the antenna was required. Since the die size should meet the size of the final chip, an extension of the feed line on chip was no option. As a consequence, the feed line had to be extended off chip. Furthermore, the die had to be placed on a defined support to achieve insensitivity of the AoC's input impedance to its placement in the measurement setup. One way to achieve both goals is the placement of the chip on a printed circuit board (PCB). While the PCB area around the antenna should be designed not to affect greatly the radiation pattern and to some extent also the input impedance, the on-chip feed line can be connected to an on-PCB line to obtain the necessary distance of the probe to the radiating element.

The solution requires to design microstrip line transition to use an available station, which is commonly utilized in the testing and measuring of impedance for integrated circuits. It works by using a bond wire to make contact microstrip line with the DUT. The bond wire and its connection to the microstrip line can be calibrated following standard procedures. Therefore, a station often offers high accuracy even in the frequency range of tens of GHz. However, while using the station, as mentioned above the DUT must be mounted on a printed circuit board (PCB), which acts as a feeding structure and a large ground plane for the antenna and the bottom side of the antenna chip is shorted to ground plane of the feeding structure via wires so it only has a ground plane underneath the feeding line and no metal ground plane behind the antenna structure itself. The setup for measurement used in this

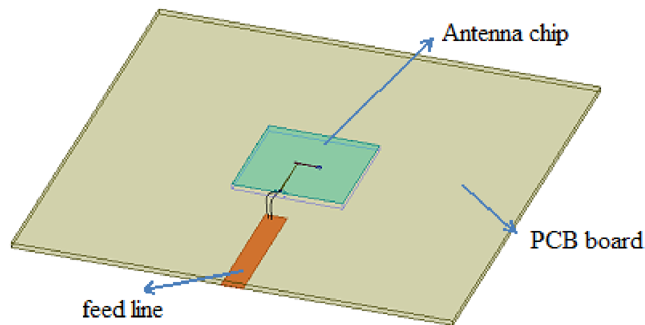


Fig. 5.6: Measurement setup with feed line

research is shown in Figure 5.6. The antenna chip is mounted on a printed circuit board (PCB) made from duroid with a thickness of 0.5 mm and a relative permittivity of 10.2. A 1.8mm connector is soldered to the front of the board. Its center pin is connected to microstrip line and the outside terminal of microstrip line is connected the input of antenna with a bond wire while its ground shield is in contact with the small ground plane on the upper layer of the board via wires. It has been suggested in [109] that the use of two parallel bond wires help to reduce the inductance of bond wire. In [110], it was shown that reducing the elevation of the bond wire from the ground plane helps to minimize its radiation effects. These suggestions were followed in this research.

An interconnect from a chip to a PCB at 60 GHz is not a trivial task and a matter of discussion itself in the mm-wave community [111]. The two standard options for the interconnect are, first, the bond-wiring technique and, second, the flip technique. Though flip-chipping is seen to be superior to the bond-wiring technique with respect to return loss

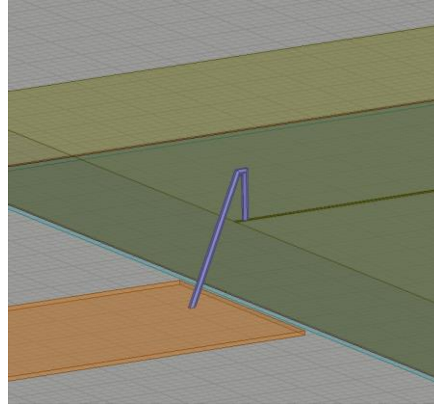


Fig. 5.7: Simulation setup (HFSS) of bond interconnect between PCB transmission line and on-chip load.

[111], it requires the chip to be mounted upside down with the antenna facing the PCB on one side and the silicon substrate on the other side. This does not resemble the targeted mounting of the AoC Therefore, the bond-wire interconnect was chosen. As described in [111], a bond-wire is commonly considered to be a non-negligible inductance at mm wave frequencies. Instead of looking at the bond wire as a parasitic element, however, we considered an alternative approach by creating a half-wavelength (λ/2) bond-wire transmission line at 60 GHz. A simulation with the commercial full-wave solver HFSS [112] revealed that a configuration of wire with a diameter of 38µm which is embedded in air environment ($\varepsilon_r = 1$) exhibits a characteristic impedance of 50Ω order to obtain a λ/2 ine, the required wire length is 2.5mm. Using these values, the simulation setup as depicted in Fig. 5.7 was made. It shows the bond-wire transmission line that connects on-chip 50Ω load to a microstrip transmission line on PCB board. Its length was designed to be $\lambda_g/2$ (1.66mm). The PCB itself has a thickness of 0.5 mm and a relative permittivity of 10.2. The resulting on-

PCB transmission line has a characteristic impedance of 50Ω. The on-chip landing structure has a pitch of 125µm between the bond-wire pad and ground pad. The two ground

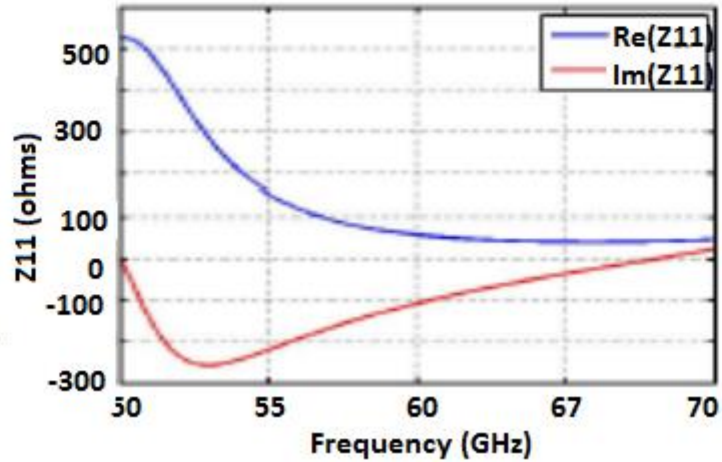


Fig. 5.8: Simulated input Impedance vs. frequency

pads were connected to the ground system. The resulting input impedance of the overall structure from fig.5.7 is depicted in Fig. 5.8. The input impedance at 60 GHz does not exactly show a value of 50Ω. This difference is seen to be the result of the discontinuity of

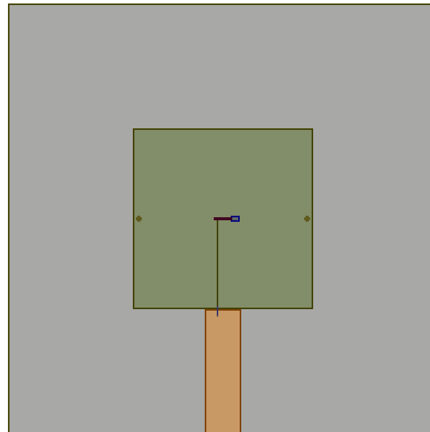


Fig. 5.9: Layout of the used measurement package with assembled AoC.

the on-chip probe pads together with their non ideal transmission line routing as well as the additional discontinuity on the PCB transmission line.

In order to not directly place the chip on the PCB, a cut-out in a large metal area on the top side of the PCB was introduced (bottom side was completely metalized). The width of the

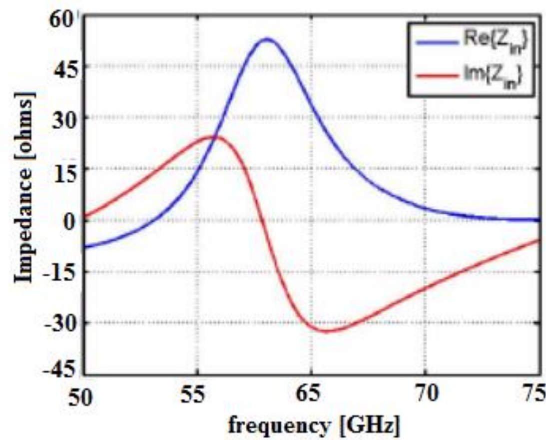


Fig. 5.10 Simulated input impedance of AoC assembled on the measurement package

resulting cavity has the same width as the chip (1.5 mm). Its length was chosen such that the edge of the plate on the chip [81] coincides with the edge of the cavity when the antenna is centered over the cavity. Note that, due to the thickness of only the fundamental parallel plate mode, i.e., the transvers electromagnetic (TEM) mode, can propagate between the plates. The energy excited in this mode, however, is considered to be small due to the field distribution associated with the antenna. The resulting input impedance of the AoC (without bond-wires, etc.) is depicted in Fig. 5.10.

5.3 Measurement of Impedance

The setup shown in Figure 5.6 used in the measurement of input impedance of the antennas. A short open load through (SOLT) calibration is performed for impedance measurements. An absorber is placed below the chip to avoid the ground plane effect from the metal chuck. Fig. 5.11 and 5.12 shows the comparison between the measured and the Simulated, S_{11}, versus the frequency for the antenna in the position. The antenna is matched for both 60GHz. It can be seen that, generally, the measured results follow the same trend as the

simulated curve, except for a small shift towards the higher frequencies. This can be explained as follows. Major issue with the fabricated modules is the non-uniform Si substrate thickness. This non-uniformity is because of the deep reactive ion etching (DRIE) of the silicon wafer to reduce its thickness from 500 m to 250 µm. The DRIE technique enabled to reduce this large Si thickness from the backside of the wafer but at the cost of large non-

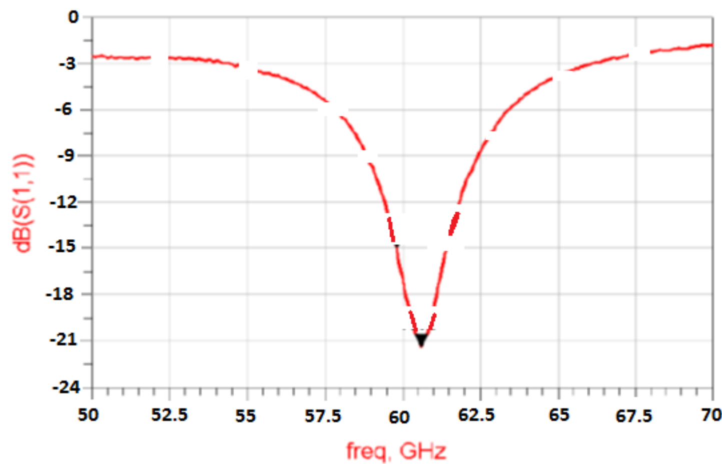


Fig. 5.11: Simulated S_{11} versus frequency for the antenna

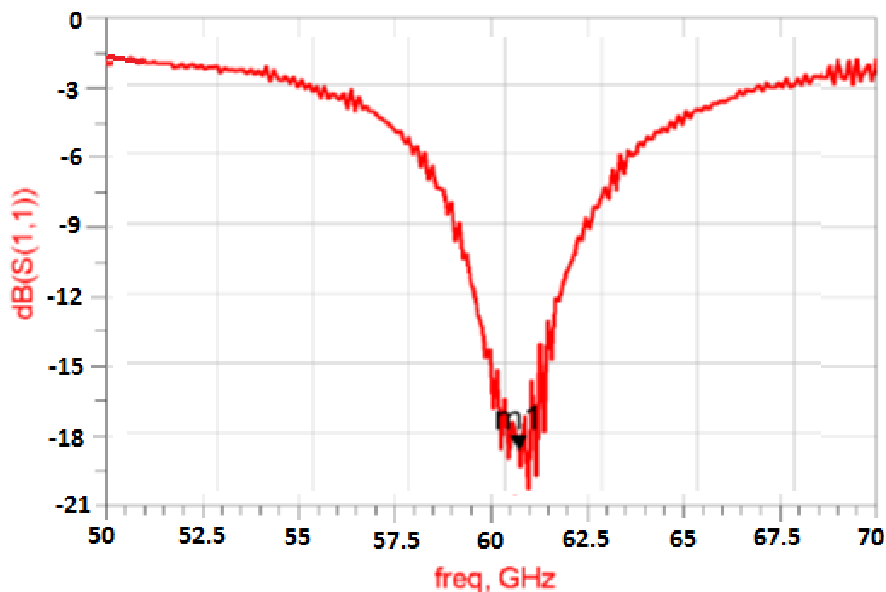


Fig. 5.12: Measured S11 versus frequency for the antenna

uniformity of the backside surface. It is hard to model this large non-uniformity in simulations, however trying different substrate thicknesses indicates that the silicon thickness affects the spacing between the resonances and in particular has a larger impact on the higher resonance. It can be responsible for the slight shift of resonances in measurements, as can be clearly seen at 60 GHz.

5.4 Measurement of the Gain Pattern

The setups and the technique discussed in the above two sections are primarily for the measurement of reflection coefficients of an on-chip antenna. It can be easily adapted to measure the gain pattern of the antenna. Although such a measurement will not be as ac-

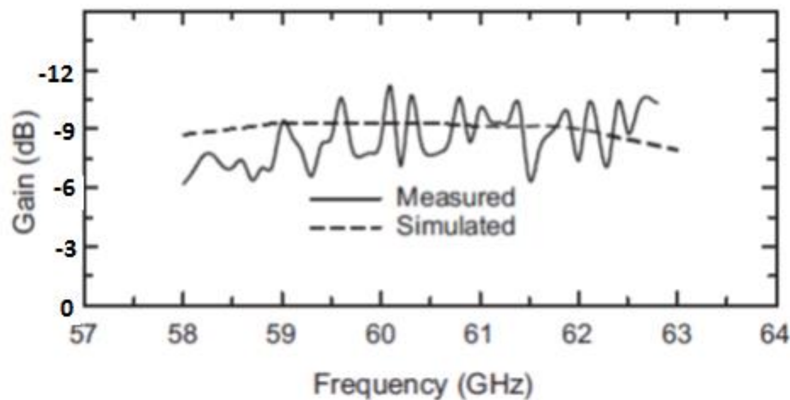


Fig. 5.13: Measured and simulated gain of the 60 GHz antenna

curate as one with sophisticated equipment, it at least gives us an estimation of the directive property of the antenna. On the other hand, even with the sophisticated equipment, the accuracy of the measurement may still be questionable due to the reasons given in the beginning of this chapter.

As discussed in previous section, the input impedance of the antenna with feed structure is deigned to be 50Ω by adjusting feed line position and gap. Measurements of the available power from the antenna are taken while the orientation of the antenna is varied. Since the transmitting antenna we are using is highly linearly polarized, the gain pattern we obtain is the partial gain of the corresponding polarization.

On-chip antenna gain and radiation pattern measurements are affected by parasitic radiations of bond wire and scattered energy from the metallic parts on the probe station. In addition, as it has been shown in previous Section, the thickness of the substrate below the antenna is critical for gain and radiation performance. Typically, the chip is glued on a PCB board which would result in surface waves excitation. These elements affect the gain measurement and must be taken into consideration in the test setup.

The gain of the antenna is measured with the absolute gain method. The absolute gain of the 60 GHz on-chip antenna is measured with a network analyzer (Agilent PNA network analyzer E8361A) using the gain transfer method. Two identical standard gain (horn) antennas are first connected to the two ports of the network analyzer and $S_{21}$is measured. The gain of the standard gain horn antennas is calculated from the measured S_{21} using the Friis transmission formula. One horn antenna is then replaced by the 60 GHz on-chip antenna and the gain of the 60 GHz antenna is obtained from the difference in the measured S_{21} in both cases. The measured gain of the 60 GHz antenna is shown in Fig. 5.13. The losses of the microstrip line and the 1.8mm mm connectors were measured separately. The measured loss of the microstrip line is ~0.8 dB/cm while the connector has a loss of ~0.9 dB at 60 GHz. The ripples in the measured gain are mainly due to scattering effects from the connector which was not covered by absorbers during the gain measurements. The measured gain of the on-chip antenna is > -6 to -10dB from 58 to 63 GHz. From the measurement of the transmission obtained with a vector network analyzer (S_{21}), the antenna gain can be estimated using Friis equation.

$$2.G(\theta,\varphi) = 10.lOG\left[10^{\left(\frac{S_{21}}{20}\right)}\right] - 20.lOG\left[\frac{\lambda}{4.\pi.R}\right] \tag{5.1}$$

where $G(\theta,\varphi)$ is the gain of a single antenna in the direction (θ,φ) and λ is the wavelength at the frequency of interest. The gain in the maximum radiation is measured using the method described above. The measured gains at 60 GHz is found to be -10.2dB.

5.5 Radiation Pattern

Typically, radiation pattern is measured in anechoic chamber with connectors and probe feeding is not common practice. On-chip antennas are small in size and mostly fed through RF connectors adding challenges to these measurements. A specific and precise test fixture is required for accurate antenna measurements. Figures 5.14 – 5-19 show the simulated radiation patterns in E-/H-planes and the measured gain of the on-chip antenna in both positions at 58, 60 and 62GHz. As can be seen, the radiation pattern for H-plane is wider and quasi-omnidirectional in comparison to that of the E-plane. It is worth mentioning here that not all the angles and cuts for the complete E and H-plane radiation characterization are possible in this setup. An acceptable agreement between the simulated radiation pattern and the measured points exist. The discrepancies can be attributed to the error in manual placement and alignment of the two antennas in these challenging on-wafer mm-wave measurements

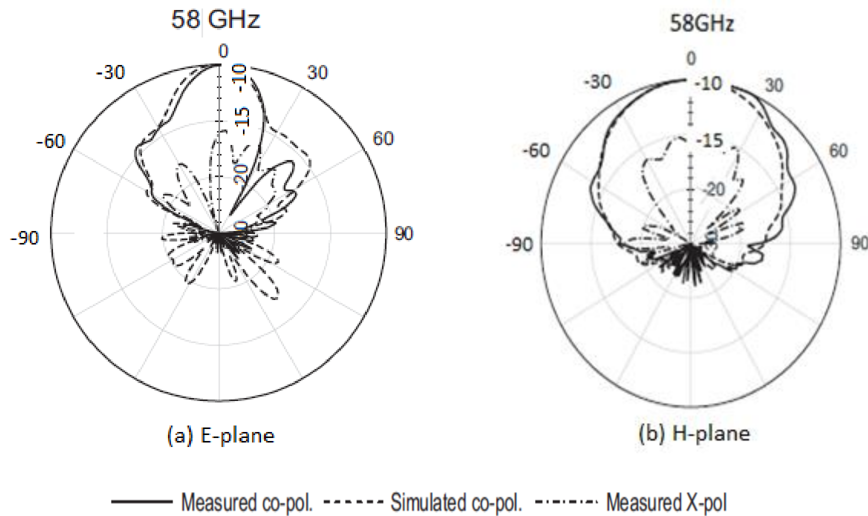


Fig. 5.14: simulated and measured radiation patterns at 58GHz for antenna chip mounted on PCB for measurement (a) E-plane, (b) H-plane

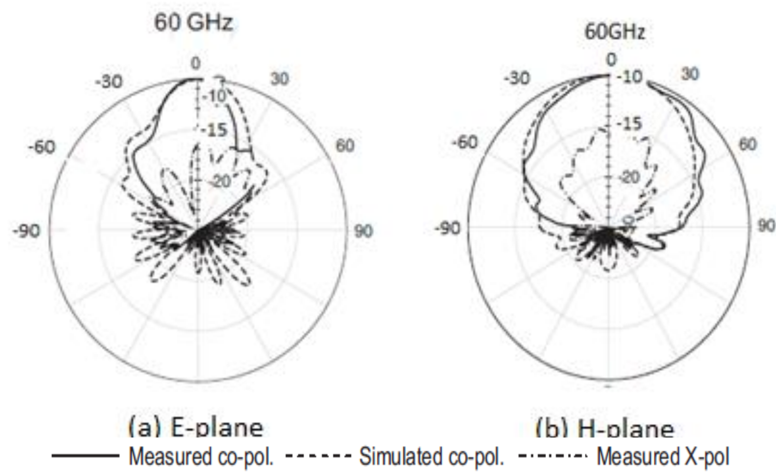


Fig. 5.15: simulated and measured radiation patterns at 60GHz for antenna chip mounted on PCB for measurement (a) E-plane, (b) H-plane

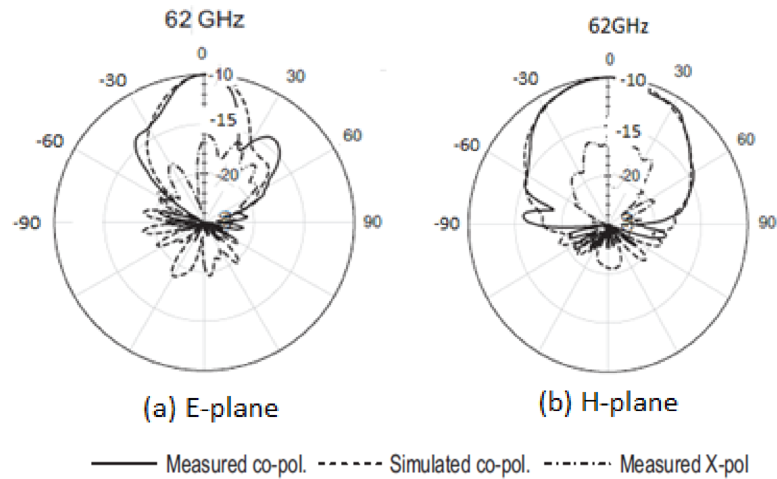


Fig. 5.16 simulated and measured radiation patterns at 62GHz for antenna chip mounted on PCB for measurement (a) E-plane, (b) H-plane

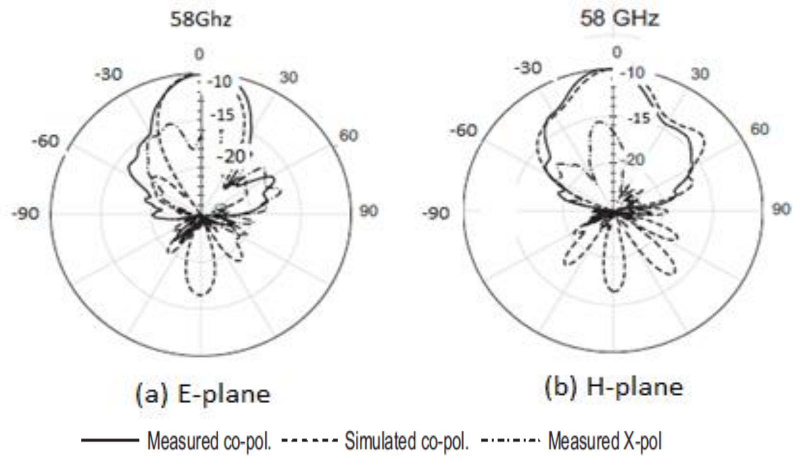


Fig. 5.17: simulated and measured radiation patterns at 58GHz for antenna with probe measurement (a) E-plane, (b) H-plane

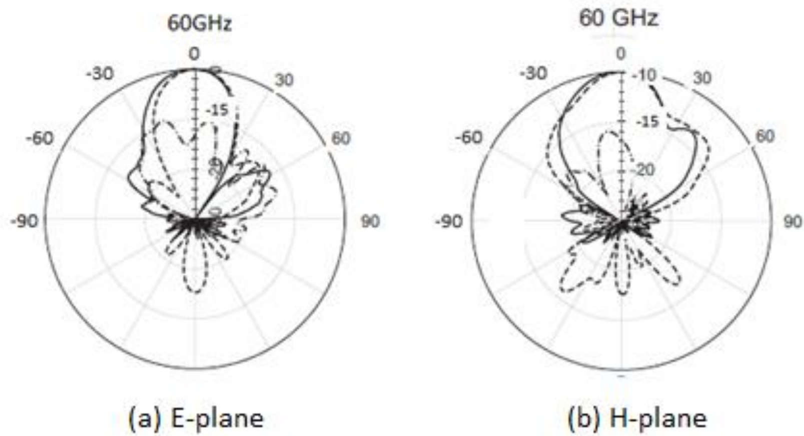


Fig. 5.18 simulated and measured radiation patterns at 60GHz for antenna with probe measurement (a) E-plane, (b) H-plane

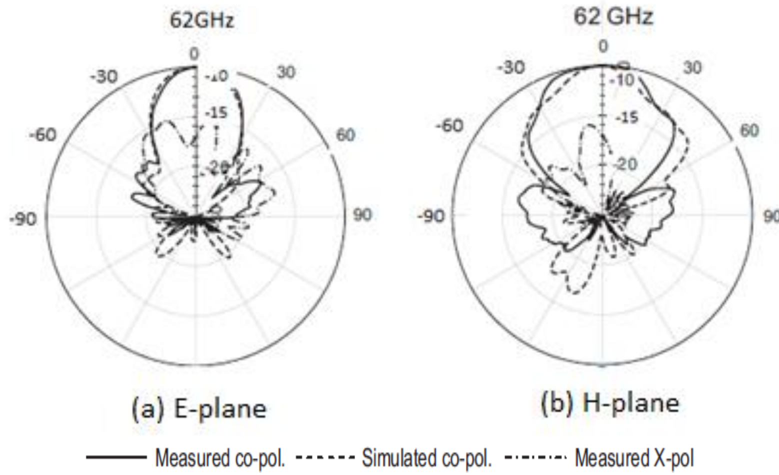


Fig. 5.19: simulated and measured radiation patterns at 62GHz for antenna with probe measurement (a) E-plane, (b) H-plane

5.6 Measurement of Antenna Efficiency

There are a number of methods for measuring antenna efficiency in the antenna literature, such as Wheeler's cap method, the Q factor method, and the directivity/gain method [113][114], among which, the Wheeler's cap method is the easiest to carry out and requires the least measurement set-ups. It was the only choice for the measurement of antenna efficiency with the available equipment.

The Wheeler's cap method is based on H. A. Wheeler's suggestion in [115] that enclosing the antenna with a conducting sphere with a radian length (λ/2π) in radius will eliminate the radiation resistance R_r from the input impedance without significantly changing the loss resistance R_L. So if we measure the input impedance of the test antenna with and without the cap. The efficiency of the antenna can then be calculated as

$$\eta = \frac{R_r}{R_r + R_L} = \frac{R_1 - R_2}{R_1} \tag{5.2}$$

where R_1 is the real part of the measured input impedance without the cap, R_2 is the real part of the part of the measured input impedance with the cap. However, this is the case

when the loss of the antenna occurs in series with the radiation. For antennas with losses that occur in parallel with the radiation, the following equation should be used,

$$\eta = \frac{R_r//R_L}{R_r} = \frac{R_1}{R_1 - R_2} \tag{5.3}$$

The experimental setup of Wheeler's cap method is shown in figure 5.18, which consists of the test antenna on a ground plane that can be completely enclosed by a metallic hemisphere. It was stated in [114] that the shape of the cap is not very important as long as it totally encloses the antenna structure. But it was found in [116] that good contact between the cap and the ground plane, as well as centering the cap over the test antenna, was important.

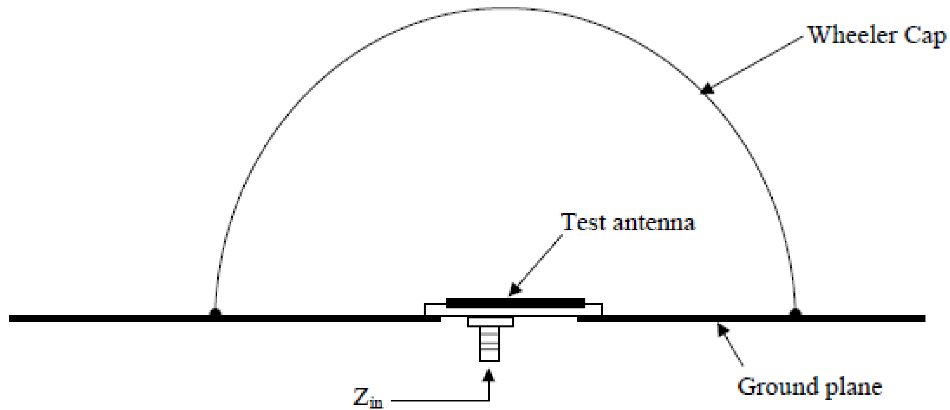


Figure 5.20 Test set-up of Wheeler cap method measurement (after D. M. Pozar [116]])

Although the Wheeler's cap method was found to be of quite good accuracy in [114], there are at least two concerns for its accuracy when applied to the measurement of antennas. One is the inevitable problem of using bonding wires and connectors. The other is the complicated loss mechanism in the antennas on CMOS chips, which makes the equivalent circuit neither a series resistance-inductance-capacitance (RLC) nor a parallel RLC circuit. However, as mentioned previously, the Wheeler's cap method is the best measurement method with the currently available equipment, and was the method of choice for antenna efficiency measurements in this research. The efficiency of the antenna was obtained 11.29% which agrees with simulated result.

Chapter 6 Conclusions and Future Works

6.1 Conclusions

From the state-of-the-art overview in chapter 3 one can conclude that all three integration approaches can be used to design antennas that match the specifications of the 60 GHz band. The AoC approach, however, falls behind the AiP and hybrid approach in terms of radiation efficiency and gain. AiP and hybrid approach designs, on the other hand, may not be able to compete with the AoC in terms of cost due to their normally rather complex multi-layer packaging structure. Moreover, AiP concepts require an additional chip-to-off-chip interconnect that requires extra design effort and introduces additional losses to the system. Therefore, the hybrid solution seems, at first glance, the best solution here. However, for frequencies beyond 60 GHz the structure size and fabrication accuracy of typical hybrid but also AiP technologies might be insufficient. This problem does not exist for the AoC approach, which was already very successfully tested in the terahertz band, see, for example, [10].

Hence, instead of focusing on three integration approaches, the antenna on chip (AOC) option was investigated in the outline of this thesis. It shall be pointed out here, however, that besides the radiation efficiency issue with this antenna integration technology, all mentioned AoC designs achieved acceptable performances as the key figures in Table 3.3 indicate. Since they all require additional processing steps after the usual IC fabrication, those techniques are commonly referred to as post-processing techniques. But although those steps have proven to enhance the performance of on-chip antennas, the semiconductor industry is still reluctant to incorporate them into their standard portfolio. A reason often given for this is the increase in fabrication costs and, therefore, the worries of losing competitiveness on the market. In this thesis, competitive antenna design concepts for this integration approach were developed to avoid these problems. Those concepts are based on basic antenna theories and types in order to focus the consideration on the antenna performance with respect to the integration technology and the antenna topology. The concepts for antenna on chip element were presented in chapter 4, where special emphasize is placed

on the radiation efficiency. The problem of achieving sufficiently high gain values beam-steering are then tackled which deals with considerations for antenna arrays.

In chapter 4, an AoC concept in standard IC technology is proposed. A virtual loop antenna (VLA) is designed here. The concept proposed in this work avoids the extra steps but provides for comparable good antenna efficiency. We propose the design of this antenna for use on CMOS ICs technology that promises to integrate a complete 60GHz system on single chip that combines a good performance in both bandwidth and radiation efficiency. The design is based on assumptions that conductor and conductive pad are imaged in ground plane to form a loop antenna. The resulting design is completely planar, and the use of via is avoided. This result in inherently low fabrication cost, light weight, and low volume antenna. Its design is essentially a joint optimization of bandwidth and power efficiency. The design of this integrated loop antenna for use on 60GHz CMOS receivers was based on silicon substrates of low resistivity that varies from 5- 20Ω-cm. The design was based on intensive electromagnetic simulations using HFSS software package. The width and length of the antenna is less than half a free-space wavelength, such that the antenna can be readily used for the realization of a planar beam-forming array.

The simulation results of the prototypes were largely confirmed by experiments and are summarized in Table 6.1. In comparison with the state-of-the-art, see Table 3.3, it can be

Table 6.1 . Key figures of proposed AoC concept

ρ [Ωcm]	20
silicon thickness [μm]	250
post-proc. technology	none
size [mm^2]	1.02
feed topology	electromagetically coupled Probe-fed sysyem
impedance bandwidth [GHz]	12.6 @ 60GHz (section 4.7.2)
η_{rad} [%]	22.53 - 58.74 (Table 4.3)
cost (relative)	Very low

concluded that this approach achieves an excellent performance with respect to other AoC designs without post-processing technologies. Compared to reference designs in which post-processing techniques were applied, the proposed approach achieves comparable results. However, since only standard processes were used for the concept presented in this chapter, it is seen to exhibit a clear cost advantage.

Therefore, especially at the 60GHz band of the spectrum. VLA on-chip antenna might come into play again since they offer a much higher design flexibility. Hence, a single low-cost integration technology that is superior throughout the entire frequency band does not seem to emerge from this consideration. Therefore, rather than trying to find the best compromise of the three solutions, one should rather make use of the existing technology diversity and choose an approach that fits best to the given specifications of a target application. For this, a general guideline with respect to the operating frequency is provided in sections 4.7.4 and 4.84, which is based on above considerations with respect to performance and producibility of the individual antenna concepts. At the upper end of the mm-wave spectrum, the AoC approach is seen to be superior, which is also in line with the successful use of on-chip antennas in the terahertz band, see, for example, [10]. The hybrid approach can then be understood as a bridge-technology that comes into play when both other approaches turn out to be insufficient.

The general recommendation from sections 4.7.4 and 4.8.4 are nice starting points for choosing a suitable antenna design parameters. However, it does not state any general corner frequencies at which one approach becomes superior to the others. For this, specific requirements for the antenna would be necessary. Due to the vast amount of possible applications throughout the mm-wave band, such definite transition points cannot be given here. Furthermore, at a single frequency band with different application scenarios, VLP on-chip antenna integration approaches may be a valid choice. In view of the three major application areas stated in Chapter 1, this integration concept is seen to be most suitable for the file transfer scenario. Here, the small size of an AoC solution allows a dense integration in hand-held devices while its gain is sufficiently large. In conclusion, we designed, simulated and built antenna on chip AOC) on silicon substrate with resistivity of 10 ohm-

cm. From initial measurements, the fabricated antenna achieves comparable results which agree well with simulated results. It indicates that these on-chip antennas on silicon substrate with resistivity of 20 ohm-cm and using standard technology process are working excellently with better efficiency. Since only standard and low cost materials and processes are used for the fabrication, these antennas are applicable for mass-employment in, for example, short-range industrial applications. Therefore, this antenna technology can be used for implementation in future high speed wireless communication products

6.2 Future Works

6.2.1 Antenna Modelling

With respect to the proposed VLA on chip antenna modeling approach, a thorough investigation of the bond-pad model will be conducted since this is seen to be the cause of the deviation between the radiation efficiency obtained with HFSS and the model. Furthermore, a mm-wave prototype of the mutual coupling experiment, will be presented in future, should be fabricated. The measurement results of this experiment can then be used to gain further insights in the validity and boundaries of the proposed modeling approach. Lastly, the VLA-model from Chapter 4 is limited to rectangular metal shapes. In order to increase the flexibility of the model and, thus, to provide the antenna designer with more freedom, the model should be extended to arbitrary shapes.

6.2.2 Antenna Array Consideration

Antenna arrays are of particular interest in 60Ghz mm-wave band since they offer high antenna gain, which is, for example, necessary for communicating over the maximum targeted distance of 10 m at 60 GHz, (see Chapter 3). For this, arrays with a fixed amplitude and phase distribution are often considered in the literature. Especially for mobile applications, however, the antenna array must exhibit the capability to align its narrow beam in the direction of the strongest signal. Otherwise, the full capacity and/or communication distance of the system can hardly ever be exploited. Hence, an antenna array with beam-

steering capability is imperative, see [2, 4, 5, 7, 8]. Such a solution for linear and circular polarization based on the AOC concept from Chapter 4 will be investigated in the future. Furthermore, a method for improving the axial ratio over the whole scan range of circularly polarized arrays be will considered. Finally, an extension of the computational model for the VLA from Chapter 4 will be introduced in future. and design procedures regarding antenna arrays in the mm-wave range will be drawn.

6.2.3 60GHz millimeter wave Measurement

The conclusions, drawn in Section 6.1., are based on the findings and conclusions of the previous chapters. Here, a strong emphasis is placed on the simulation results. The simulated radiation efficiency of the antenna concept could not be verified directly, however. In order to be able to perform direct efficiency measurements, it is recommended here to extend the radiation pattern measurement setup.to include complete hemispherical scans. By this, the total radiated power of an antenna can be determined. Furthermore, the input power that is accepted by the AUT has to be known for this, such that Equation (2.50) can be applied directly. This input power can, for example, be measured with a power meter or by a measurement of a reference antenna with known efficiency. For this, a standard gain horn could be used, for which the radiation efficiency may be assumed to be 100 %. The resulting accuracy of this assumption remains to be shown, however. Furthermore, the radiation pattern of the on-chip VLA could not be measured since the probe could not be adequately landed on the on-chip bond-pads. Therefore, the radiation pattern measurement setup needs to be extended to allow the probe to be tilted around its longitudinal axis.

6.2.4 Antenna on chip (AOC) feed and Sensitivity

Antenna on chip (AOC) feed network should also be supported by standard silicon technology process. The accuracy of the manufacturing process is especially important for the mm-wave antenna feed since, in general, the smallest features are used in the mm-wave feed. Tolerances on the width of the RF feed directly correspond to changes in the characteristic impedance of the RF feed and this results in undesired reflections and mismatch.

The silicon dielectric thickness should be selected carefully to obtain an RF feed network with a well-defined impedance and low radiation losses. It is advantageous to have a ground plane at a well-defined distance that is relatively close, in terms of wavelength, to the RF feed. In this way the radiation losses of the feed are minimized. Moreover, the package should be designed such that the feed-line interconnections are as short as possible to minimize the associated losses. Design and analysis of AOC feed structure will be investigated.

In this work, AOC element has been modelled, designed and measured. The antenna shows relatively good performance regarding radiation efficiency and antenna bandwidth. However, before the antenna element is realized, it is important to investigate the effect of manufacturing tolerances on the performance. This is especially important since the antenna is realized in a standard, low-cost, planar manufacturing technology in which tolerances can be relatively large. Therefore, the sensitivity of the antenna structure for manufacturing tolerances will be analyzed.

Bibliography

[1] P. Smulders, "Exploiting the 60 GHz band for local wireless multimedia access: prospects and future directions," IEEE Communications Magazine, vol. 40, no. 1, pp. 140 – 147, Jan. 2002.

[2] S. K. Yong and C.-C. Chong, "An Overview of Multigigabit Wireless through Millimeter Wave Technology: Potentials and Technical Challenges," EURASIP Journal on Wireless Communications and Networking, vol. Volume 2007 Issue 1, pp. 50–50, 2007.

[3] "Broadband Radio Access Networks (BRAN); 60 GHz Multi-GigabitWAS/RLAN Systems; Harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive," ETSI EN 302 567 v.1.2.1 (12-01), January 2012.

[4] N. Guo, R. C. Qiu, S. S. Mo, and K. Takahashi, "60-GHz Millimeter-Wave Radio: Principle, Technology, and New Results," EURASIP Journal on Wireless Communications and Networking, vol. 2007, no. 1, 2007.

[5] R. Daniels, J. Murdock, T. Rappaport, and R. Heath, "60 GHz Wireless: Up Close and Personal," IEEE Microwave Magazine, vol. 11, no. 7, pp. 44 –50, Dec. 2010.

[6] Y. Zhang and D. Liu, "Antenna-on-Chip and Antenna-in-Package Solutions to Highly Integrated Millimeter-Wave Devices for Wireless Communications," IEEE Transactions on Antennas and Propagation, vol. 57, no. 10, pp. 2830–2841, Oct. 2009.

[7] P. Smulders, H. Yang, and I. Akkermans, "On the Design of Low-Cost 60-GHz Radios for Multigigabit-per-Second Transmission over Short Distances [Topics in Radio Communications]," IEEE Communications Magazine, vol. 45, no. 12, pp. 44 –51, December 2007.

[8] R. Daniels and R. Heath, "60 GHz wireless communications: emerging requirements and design recommendations," IEEE Vehicular Technology Magazine, vol. 2, no. 3, pp. 41 –50, sept. 2007.

[9] K.-K. Huang and D. Wentzloff, "A 60GHz antenna-referenced frequency-locked loop in 0.13 um CMOS for wireless sensor networks," in 2011 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), feb. 2011, pp. 284 –286.

[10] E. Ojefors, U. Pfeiffer, A. Lisauskas, and H. Roskos, "A 0.65 THz focal-plane array in a quarter micron cmos process technology," IEEE Journal of Solid-State Circuits, vol. 44, no. 7, pp. 1968 –1976, July 2009.

[11] T. Simpson, "The Magnetostatic Frill Source," IEEE Transactions on Antennas and Propagation, vol. 59, no. 9, pp. 3313 –3317, sept. 2011.

[12] H.-G. Unger, Elektromagnetische Theorie f ¨ur die Hochfrequenztechnik - Teil I: Allgemeine Gesetze und Verfahren, Antennen und Funk¨ ubertragung, planare, rechteckige und zylindrische Wellenleiter, 2nd ed. Dr. Alfred H¨ uthig Verlag GmbH Heidelberg, 1988.

[13] D. M. Pozar, Microwave Engineering, 3rd ed. New York: John Wiley & Sons, Inc., New York. 2005.

[14] C. A. Balanis, Antenna Theory - Analysis and Design, 3rd ed. John Wiley & Sons, Inc., 2005.

[15] R. F. Harrington, Time-Harmonic Electromagnetic Fields, ser. on Electromagnetic Wave Theory, D. G. Dudley, Ed. IEEE Press, John Wiley & Sons, Inc., 2001.

[16] Field Computation by Moment Methods, ser. on Electromagnetic Waves, D. G. Dudley, Ed. IEEE Press, John Wiley & Sons, Inc., 2000.

[17] A. Taflove and S. C. Hagness, Computational Electrodynamics: The Finite-Difference Time-Domain Method, 3rd ed. Artech House Inc., 2005.

[18] (2012, December) EMPIRE XCcel. IMST GmbH. [Online]. Available: http://www.empire.de

[19] A. Ludwig, "The definition of cross polarization," Antennas and Propagation, IEEE Transactions on, vol. 21, no. 1, pp. 116–119, 1973.

[20] J. E. Storer, "Impedance of Thin Wire Loop Antennas," Craft Laboratory, Harvard University, Cambridge, Massachusetts, Tech. Rep. 212, May 1955.

[21] M. C. van Beurden, "Integro-differential equations for electromagnetic scattering – Analysis and computation for objects with electric contrast," Ph.D. dissertation, Eindhoven University of Technology, 2003. [Online]. Available: http://w3.tue.nl/en/services/library/digilib/ publications from tue/dissertations/

[22] M. C. van Beurden and A. G. Tijhuis, "Analysis and Regularization of the Thin-Wire Integral Equation With Reduced Kernel," IEEE Transactions on Antennas and Propagation, vol. 55, no. 1, pp.120 –129, Jan. 2007.

[23] (2012, December) Matlab website. Math Works, Inc. [Online]. Available: www.mathworks.com/ products/matlab/

[24] "IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements. Part 15.3: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for High Rate Wireless Personal Area Networks (WPANs) Amendment 2: Millimeter-wave-based Alternative Physical Layer Extension," IEEE Std 802.15.3c-2009 (Amendment to IEEE Std 802.15.3-2003), pp. c1 –187, December 2009.

[25] S. Reynolds, B. Floyd, U. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, “A silicon 60-ghz receiver and transmitter chipset for broadband communications,” Solid-State Circuits, IEEE Journal of, vol. 41, no. 12, pp. 2820 –2831, Dec. 2006.

[26] RF Manual - Application and design manual for High Performance RF products, 16th ed., NXP Semiconductors, June 2012. [Online]. Available: http://www.nxp.com

[27] (2012, December) LTCC @ IMST. IMST GmbH. [Online]. Available: http://www.ltcc.de

[28] Y. Zhang, M. Sun, K. Chua, L.Wai, and D. Liu, “Antenna-in-Package Design for-Wirebond Interconnection to Highly Integrated 60-GHz Radios,” IEEE Transactions on Antennas and Propagation, vol. 57, no. 10, pp. 2842–2852, Oct. 2009.

[29] D. G. Kam, D. Liu, A. Natarajan, S. Reynolds, H.-C. Chen, and B. Floyd, “LTCC Packages With Embedded Phased-Array Antennas for 60 GHz Communications,” IEEE Microwave and Wireless Components Letters, vol. 21, no. 3, pp. 142 –144, march 2011.

[30] W. Hong, A. Goudelev, K. Baek, V. Arkhipenkov, and J. Lee, “24-Element Antenna-in-Package for Stationary 60-GHz Communication Scenarios,” IEEE Antennas and Wireless Propagation Letters, vol. 10, pp. 738 –741, 2011.

[31] “RO3000 Series Circuit Materials - RO3003, RO3006 and RO3010 High Frequency Laminates,” Datasheet, December 2012. [Online]. Available: http://www.rogerscorp.com

[32] “RO4000 Series - High Frequency Circuit Materials,” Datasheet, December 2012. [Online]. Available: http://www.rogerscorp.com

[33] “ULTRALAM 3000 Liquid Crystalline Polymer Circuit Material,” Datasheet, December 2012. [Online]. Available: http://www.rogerscorp.com

[34] D. G. Kam, D. Liu, A. Natarajan, S. Reynolds, and B. Floyd, “Organic Packages With Embedded Phased-Array Antennas for 60-GHz Wireless Chipsets,” IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 1, no. 11, pp. 1806 –1814, Nov. 2011.

[35] D. Liu, I. Akkermans, H.-C. Chen, and B. Floyd, “Packages with Integrated 60-GHz Aperture- Coupled Patch Antennas,” IEEE Transactions on Antennas and Propagation, vol. PP, no. 99, p. 1, 2011.

[36] W. Hong, K. Baek, and A. Goudelev, “Multilayer Antenna Package for IEEE 802.11ad employing Ultra-low Cost FR4,” IEEE Transactions on Antennas and Propagation, vol. PP, no. 99, p. 1, 2012.

[37] M. I. Kazim, M. H. A. J. Herben, and M. D. Huang, "Half truncated icosahedral passive electromagnetic deflector for the 60 GHz band," in 2010 Proceedings of the Fourth European Conference on Antennas and Propagation (EuCAP), April 2010, pp. 1 –5.

[38] S.-S. Hsu, K.-C. Wei, C.-Y. Hsu, and H. Ru-Chuang, "A 60-GHz Millimeter-Wave CPW-Fed Yagi Antenna Fabricated by Using 0.18-m CMOS Technology," IEEE Electron Device Letters, vol. 29, no. 6, pp. 625 –627, June 2008.

[39] A. B. Smolders, "Microstrip Phased-Array Antennas: A Finite-Array Approach," Ph.D. dissertation, Eindhoven University of Technology, 1994. [Online]. Available: http://w3.tue.nl/ en/services/library/digilib/publications from tue/dissertations/

[40] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Receiver and Antennas," IEEE Journal of Solid- State Circuits, vol. 41, no. 12, pp. 2795 –2806, dec. 2006.

[41] S. Pan and F. Capolino, "Design of a CMOS On-Chip Slot Antenna with Extremely Flat Cavity at 140 GHz," IEEE Antennas and Wireless Propagation Letters, vol. 10, pp. 827 –830, 2011.

[42] K. Kang, F. Lin, D.-D. Pham, J. Brinkhoff, C.-H. Heng, Y. X. Guo, and X. Yuan, "A 60-GHz OOK Receiver With an On-Chip Antenna in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 45, no. 9, pp. 1720 –1731, sept. 2010.

[43] X.-Y. Bao, Y.-X. Guo, and Y.-Z. Xiong, "60-GHz AMC-Based Circularly Polarized On-Chip Antenna Using Standard 0.18-m CMOS Technology," IEEE Transactions on Antennas and Propagation, vol. 60, no. 5, pp. 2234 –2241, may 2012.

[44] Y.-C. Ou and G. Rebeiz, "On-Chip Slot-Ring and High-Gain Horn Antennas for Millimeter-Wave Wafer-Scale Silicon Systems," IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 8, pp. 1963 –1972, Aug. 2011.

[45] M.-R. Nezhad-Ahmadi, M. Fakharzadeh, B. Biglarbegian, and S. Safavi-Naeini, "High-Efficiency On-Chip Dielectric Resonator Antenna for mm-Wave Transceivers," IEEE Transactions on Antennas and Propagation, vol. 58, no. 10, pp. 3388 –3392, Oct. 2010.

[46] M. Neshat, D. Hailu, M. Nezhad-Ahmadi, G. Rafi, and S. Safavi-Naeini, "Gain Measurement of Embedded On-Chip Antennas in mm-wave/THz Range," IEEE Transactions on Antennas and Propagation, vol. 60, no. 5, pp. 2544 –2549, may 2012.

[47] E. Ojefors, H. Kratz, K. Grenier, R. Plana, and A. Rydberg, "Micromachined Loop Antennas on Low Resistivity Silicon Substrates," IEEE Transactions on Antennas and Propagation, vol. 54, no. 12, pp. 3593 –3601, dec. 2006.

[48] A. Mahanfar, S.-W. Lee, A. Parameswaran, and R. Vaughan, “Self-Assembled Monopole Antennas With Arbitrary Shapes and Tilt Angles for System-on-Chip and System-in-Package Applications,” IEEE Transactions on Antennas and Propagation, vol. 58, no. 9, pp. 3020 –3028, sept. 2010.

[49] K. Chan, A. Chin, Y. Lin, C. Chang, C. Zhu, M. Li, D. Kwong, S. McAlister, D. Duh, and W. Lin, “Integrated antennas on Si with over 100 GHz performance, fabricated using an optimized proton implantation process,” IEEE Microwave and Wireless Components Letters, vol. 13, no. 11, pp. 487 –489, Nov. 2003.

[50] U. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. Floyd, and S. Reynolds, “A chip-scale packaging technology for 60-GHz wireless chipsets,” IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 8, pp. 3387 –3397, Aug. 2006.

[51] G. Felic and S. Skafidas, “Flip-Chip Interconnection Effects on 60-GHz Microstrip Antenna Performance,” IEEE Antennas and Wireless Propagation Letters, vol. 8, pp. 283 –286, 2009.

[52] H.-T. Wu et al., “Bond Wire Antenna/Feed for Operation near 60 GHz,” IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 12, pp. 2966 –2972, dec. 2009.

[53] R. Willmot et al., “A Yagi-Uda Array of High Efficiency Wire-Bond Antennas for On-Chip Radio Applications,” IEEE Transactions on Microwave Theory and Techniques, no. 12, pp. 3315 –3321, 2009.

[54] B. P. Gaucher, D. Liu, U. R. R. Pfeiffer, and T. M. Zwick, “Apparatus and methods for constructing antennas using wire bonds as radiating elements,” U.S. Patent 7,295,161, Nov. 13, 2007.

[55] T. H. Lee, The design of CMOS radio-frequency integrated circuits. Cambridge: Cambridge University Press, 2nd ed., 2004

[56] N. Alexopoulos, P. Katehi, and D. Rutledge, “Substrate optimization for integrated circuit antennas,” IEEE Trans. Microwave Theory Tech., vol. 83, pp. 550– 557, July 1983.

[57] D. Jackson, J. Williams, A. Bhattacharyya, R. Smith, S. Buchheit, and S. Long, “Microstrip patch designs that do not excite surface waves,” IEEE Trans. Antennas Propagat., vol. 41, pp. 1026–1037, August 1993.

[58] G. Gauthier, A. Courtay, and G. Rebeiz, “Microstrip antennas on synthesized low dielectric-constant substrates,” IEEE Trans. Antennas Propagat., vol. 45, pp. 1310–1314, August 1997.

[59] A. Weily, L. Horvath, K. Esselle, B. Sanders, and T. Bird, “A planar resonator antenna based on a woodpile EBG material,” IEEE Trans. Antennas Propagat., vol. 53, pp. 216–223, January 2005.

[60] F. Yang and Y. Rahmat-Samii, “Reflection phase characterizations of the EBG ground plane for low profile wire antenna applications,” IEEE Trans. Antennas Propagat., vol. 51, pp. 2691–2703, October 2003.

[61] N. Llombart, A. Neto, G. Gerini, and P. de Maagt, “Planar circularly symmetric EBG structures for reducing surface waves in printed antennas,” IEEE Trans. Antennas Propagat., vol. 53, pp. 3210–3218, October 2005.

[62] T. Zwick, D. Liu, and B. Gaucher, “Broadband planar superstrate antenna for integrated millimeter wave transceivers,” IEEE Trans. Antennas Propagat., vol. 54, pp. 2790–2796, October 2006.

[63] P. Deixler, A. Rodriguez, W. De Boer, H. Sun, R. Colclaser, D. Bower, N. Bell, A. Yao, R. Brock, Y. Bouttement, G. Hurkx, L. Tiemeijer, J. Paasschens, H. Huizing, D. Hartskeerl, P. Agrarwal, P. Magnee, E. Aksen, and J. Slotboom, “QUBiC4X: An fT/fmax = 130/140GHz SiGe:CB iCMOS manufacturing technology with elite passives for emerging microwave applications,” Bipolar/BiCMOS Circuits and Technology, 2004. Proceedings of the 2004 Meeting, pp. 233 – 236, sept. 2004.

[64] G. M. Rebeiz, \Millimeter-wave and terahertz integrated circuit antennas," *Pro- ceedings of the IEEE*, vol. 80, pp. 1748{1770, Nov. 1992.

[65] N. G. Alexopoulos, P. B. Katehi, and D. B. Rutledge, Substrate optimization for integrated circuit antennas," *IEEE Trans. Microwave Theory and Techniques*, vol. 31, no. 7, pp. 550{557, July 1983.

[66] C. Cao, Y. Ding, X. Yang, J.-J. Lin, H. Wu, A. Verma, J. Lin, F. Martin, and K. K. O, \A 24 GHz transmitter with on-chip dipole antenna in 0.13-m CMOS," *IEEE J. Solid-state Circuits*, vol. 43, no. 6, pp. 1394{1402, June 2008.

[67] Y. Zhang, M. Sun, and L. Guo, \On-chip antennas for 60 GHz radios in silicon technology," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1664{1668, July 2005.

[68] J. Akkermans, R. van Dijk, and M. Herben, “Millimeter-wave antenna measurement,” in Proceedings of the 2007 European Microwave Conference (EuMC 2007), October 2007.

[69] S. Hsu, K. Wei, C. Hsu, and R. Chuang, \A 60-GHz Millimeter-wave CPW-fed Yagi antenna fabricated by using 0.18-m CMOS technology," *IEEE Electron Device Lett*, vol. 29, pp. 625{627, June 2008.

[70] S. T. Nicolson, A. Tomkins, K. Tang, A. Cathelin, D. Belot, and S. P. Voinigescu, \A 1.2 V, 140 GHz receiver with on-die antenna in 65 nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 229 { 232, 2008.

[71] Y. Tsutsumi, M. Nishio, S. Sekine, H. Shoki, and T. Morooka, \A triangular loop antenna mounted adjacent to a lossy Si substrate for millimeter-wave wireless PAN," *IEEE Antennas and Propagation Society International Symposium*, pp. 1008{1011, June 2007.

[72] R. Willmot, D. Kim, and D. Peroulis, \Yagi-Uda array of high-efficiency wire-bond antennas for on-chip radio applications," *IEEE Trans. Microwave Theory Tech-niques*, vol. 57, no. 12, pp. 3315{3321, Dec. 2009.

[73] H. Wu, M. Tekle, C. Nallani, N. Zhang, and K. K. O, \Bond-wire antenna/feed for operation near 60 GHz," *IEEE Trans. Microwave Theory Techniques*, vol. 57, no. 12, pp. 2966{2972, Dec. 2009.

[74] J. Hirokawa, K. Kimishima, M. Ando, and Y. Hirachi, \Dipole antenna on thick resin layer on the back side of silicon chip at 60 GHz," *Proceedings of the 39th European Microwave Conference*, vol. 57, no. 12, pp. 528{531, 2009.

[75] G.-Y. Chen and J.-S. Sun, "A printed dipole antenna with microstrip tapered balun," *Microw. Opt. Tech. Lett.*, vol. 40, no. 4, pp. 344–346, Feb. 2004

[76] Jan Craninckx and Michiel S. J. Steyaert, "A 1.8-GHz Low-Phase-Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J. Solid-State Circuits*, vol. 32, No. 5, May 1997, pp.736-744.

[77] C. Patrick Yue, S. Simon Wong, "Design Strategy of On-Chip Inductors for Highly Integrated RF Systems," *Proceeding on Design Automation Conference*, June 1999, pp. 982-987.

[78] Paolo Arcioni, et al., "An Improved Lumped-Element Equivalent Circuit for on Silicon Integrated Inductors," *IEEE Radio and Wireless Conference RAWCON*, Aug. 1998, pp 301-304.

[79] Paolo Arcioni, et al., "An Innovative Modelization of Loss Mechanism in Silicon Integrated Inductor," *IEEE Tran. on Analog and Digital Signal Processing*, vol. 46, No. 12, Dec. 1999.

[80] Ali M. Niknejad, Robert G. Meyer, "Analysis, Design and Optimization of Spiral Inductors and Transformers for Si RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, No. 10, Oct. 1998, pp. 1470-1481.

[81] Joachim N. Burghatz, Behzad Rajaei, "On the Design of RF Spiral Inductors on Silicon," *IEEE Trans. On Electron Devices*, vol. 50, No. 3, Mar. 2003, pp 718-729.

[82] William B. Kuhn, Naveen K. Yanduru, "Spiral Inductor Substrate Loss Modeling in Silicon RFICs," *IEEE RAWCON Proceeding*, Jan. 1998, pp. 305-308.

[83] H. M. Greenhouse, “Design of planar rectangular microelectronic inductors,” *IEEE Transactions on Parts, Hybrids, and Packaging*, vol. 10, Issue: 2, Jun 1974, pp.101 - 109.

[84] C. Karnfelt, P. Hallbjorner, H. Zirath, and A. Alping, “High gain active microstrip antenna for 60-GHzWLAN/WPAN applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 6, pp. 2593–2603, Jun. 2006.

[85] Y. J. Yoon and B. Kim, “A new formula for effective dielectric constant in multi-dielectric layer microstrip structure,” in *Proc. IEEE Electrical Perform. Electronic Package.* Scottsdale, AZ, Oct. 23-25, 2000,
pp. 163–167.

[86] H. A. Wheeler, “Formulas for the skin effect,” *in Proc. I. R. E.*, vol. 30, Sept. 1942,
pp. 412–424.

[87] J. A. Tegopoulos and E. E. Kriezis, Eddy Currents in Linear Conducting Media, New York, NY: Elsevier, 1985.

[88] R. Faraji-Dana, Y. Chow, “Edge condition of the field and a.c. resistance of a rectangular strip conductor,” *IEE Proceeding on Microwaves, Antennas and Propagation*, vol. 137, No.2, April 1990, pp. 133-140.

[89] Y. Eo and W. R. Eisenstadt, “High-speed VLSI interconnect modeling based on Sparameter measurements,” *IEEE Trans. Components, Hybrids, and Manufacturing Technology*, vol. 16, Issue 5, Aug. 1993, pp. 555–562.

[90] R. A. Pucel, D. J. Massé, and C. P. Hartwig, “Losses in microstrip,” *IEEE Trans. MTT*, vol. 16, June 1968, pp. 342–350.

[91] R. Faraji-Dana and Y. L. Chow, “The current distribution and ac resistance of a microstrip structure,” *IEEE Trans. MTT*, vol. 38, pp. 1268–1277, Sept. 1990.

[92] James C. Routio, “An Investigation of Microstrip Conductor Loss,” *IEEE Microwave Magazine*, Dec. 2000, pp. 60-67.

[93] D.M. Pozar, *Microwave engineering*, Amherst, MA: John Wliley & Sons, 1998.

[94] N. G. Alexopoulos, P. B. Katehi, and D. B. Rutledge, “Substrate optimization for integrated circuit antennas,” *IEEE Trans. Microw. Theory Tech.*, vol. 31, no. 7, pp. 550–557, Jul. 1983

[95] WATERHOUSE, R.B. *Microstrip patch antennas: a designer’s guide*. Boston (US-MA), 2003.

[96] MARCUVITZ, N. *Waveguide handbook*. London (GB), 1986.

[97] MIKULASEK, T., LACIK, J. Two feeding methods based on substrate integrated waveguide for microstrip patch antennas. Submitted for publication in *Journal of Electromagnetic Waves and Applications*.

[98] Y. Zhang, M. Sun, and L. Guo, “On-chip antennas for 60-GHz radios in silicon technology,” IEEE Transactions on Electron Devices, vol. 52, no. 7, pp. 1664–1668, July 2005.

[99] D. B. Rutledge *et al.*, “Integrated-circuit antennas,” in *Infrared and Millimeter-Waves*. New York: Academic, 1983, pp. 1–90.

[100] N. Engheta and C. H. Papas*,* *Radio Sci.*, vol. 17, pp. 1557–1566, 1982.

[101] T. Al-Attar, A. Hassibi, and T. H. Lee, “A 77 GHz monolithic IMPATT transmitter in standard CMOS technology,” in *Proc. IEEE MTT-S Int. Microwave Symp.*, Jun. 12–17, 2005, pp. 1571–1574.

[102] T. Al-Attar and T. H. Lee, “Monolithic integrated millimeter-wave IMPATT transmitter in standard CMOS technology,” *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 11, pp. 3557 3561, Nov. 2005.

[103] MoM-Based Electromagnetic Simulator (IE3D). [Online]. Available:http://www.zeland.com

[104] H. Kogelnik, “Theory of dielectric waveguides,” in *Integrated Optics*, T. Tamir, Ed. New York: Springer-Verlag, Ch. 2.

[105] M. R. N. Ahmadi, S. N. Safieddin, and L. Zhu, “On-chip antennas for 24, 60, and 77 GHz single package transceivers on low resistivity silicon substrate,” in *Proc. IEEE Antenna Propag. Symp.*, Honolulu, HI, Jun. 10-15, 2007, pp. 5059–5062.

[108] K. Hirasawa, M. Haneishi, Analysis, design, and measurement of small and low-profile antennas, Artech House, Boston, 1992

[109] D. Singh, C. Kalialakis, P. Gardner, and P. S. Hall, “Small H-shaped antennas for MMIC applications,” IEEE Trans. on Antennas and Propagation, Vol. Ap-48, 2000, pp.1134-1141

[110] H. Y. Lee, “Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits,” IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-43, 1995, pp. 63-68

[111] Y. Zhang, D. Liu, "Antenna-on-Chip and Antenna-in- Package Solutions to Highly Integrated Millimeter- Wave Devices for Wireless Communications", *IEEE Transactions on Antennas and Propagation*, Vol. 57, No. 10, pp. 2830-2841, October 2009.

[112] www.ansoft.com/products/hf/hfss/, Ansoft, HFSS website

[113] U. Johannsen, A.B. Smolders, R. Mahmoudi, and J.A.G. Akkermans, "Substrate Loss Reduction in Antenna-on-Chip Design," *Antennas and Propagation Society International Symposium, 2009. APSURSI '09.* IEEE 2009, pp. 1-4

[114] E. H. Newman, P. Bohley, and C. H. Walter, "Two methods for the measurement of antenna efficiency," IEEE Trans. on Antennas and Propagation, Vol. Ap-23, 1975, pp.457-461

[115] D. M. Pozar and B. Kaufman, "Comparison of three methods for the measurement of printed antenna efficiency," IEEE Trans. on Antennas and Propagation, Vol. Ap-36, 1988, pp.136-139

[116] H. A. Wheeler, "The radian sphere around a small antenna," Proc. IRE, 1959, pp.1325-1331

[117] J. Bouvier, Y. Thorigne, S. A. Hassan, S.A.; M. J. Revillet, P. Senn, "A smart card CMOS circuit with magnetic power and communication interface," Digest of Technical Papers, IEEE International Solid-State Circuits Conference, 44th ISSCC, pp. 296 –297, 474, 1997

[118] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, pp. 743–752, May 1998

[119] S. Ramo, J. R. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics, 3rd ed*. New York: Wiley, 1994.

[120] Paolo Arcioni, et al., "An Innovative Modelization of Loss Mechanism in Silicon Integrated Inductor," *IEEE Trans. Circuit and Systems*, vol. 46, No.12, Dec. 1999, pp.1453-1460.

Appendix A

A.1 Q-FACTOR DEFINITIONS FOR TRANSMISSION LINES

Analogous to the case for lumped inductors [118], there are many different definitions for Q of a transmission line, where the applicability depends upon the intended function of the transmission line in the circuit.

A.2. Resonator quality factor

The most commonly used definition is the Q of the line when used as a resonator (Q_{res}),

$$Q_{res} = \frac{\omega_0(Avg.\ energy\ Stored)}{avg.\ power\ loss} = \frac{\omega_0(W_m + W_e)}{P_L} \qquad (A.1)$$

where ω_0 is the resonance frequency, W_m and W_e are the average magnetic and electric energy stored, and P_L is the average power dissipated in the line. Q_{res} can be related to the quantities by [119]

$$Q_{res} \approx \frac{\beta}{2\alpha} = \frac{\pi}{\alpha\lambda_g} = \frac{\pi\sqrt{\varepsilon_{eff}}}{\alpha\lambda_0} \qquad (A.2)$$

where λ_0 is the free-space wavelength and ε_{eff} is the effective dielectric constant. Since ε_{eff} is determined mostly by the dielectric properties, and not the transmission line structure or dimensions, maximizing Q_{res} is roughly equivalent to minimizing the attenuation constant α. Q_{res} can be related very simply to the parameters by

$$\frac{1}{Q_{res}} \approx \frac{1}{Q_L} + \frac{1}{Q_c} \qquad (A.3)$$

A.3 Net quality factor

If the line is designed to behave as an equivalent inductor, storing mostly magnetic energy, it is more appropriate to consider the power dissipated for a given amount of *net* reactive energy stored in the line, as opposed to the *total* stored energy [118].

$$Q_{net} \equiv \frac{2\omega_0(net\ energy\ stored)}{avg.\ power\ loss} = \frac{2\omega_0(W_m - W_e)}{P_R + P_G} \qquad (A.4)$$

where ω_0 is the resonance frequency, W_m and W_e are the average magnetic and electric energy stored, and P_R and P_G are the average power dissipated in the resistance and conductance, respectively. If Q_L and Q_C are expressed as

$$Q_L = \frac{2\omega_0 W_m}{P_G} \qquad (A.5)$$

$$Q_c = \frac{2\omega_0 W_e}{P_G} \qquad (A.6)$$

it is straightforward to show that

$$\frac{1}{Q_{net}} = \frac{1}{\eta_L Q_L} + \frac{1}{\eta_C Q_C} \qquad (A.7)$$

Where

$$\eta_L = 1 - \frac{W_e}{W_m} \qquad (A.8)$$

$$\eta_C = \frac{W_m}{W_e} - 1 \qquad (A.9)$$

A.4 Q-FACTOR OF A SHORTED TRANSMISSION LINE

For a shorted transmission line (Fig. A.1), Q_{net} is simply the single-ended port Q, which is

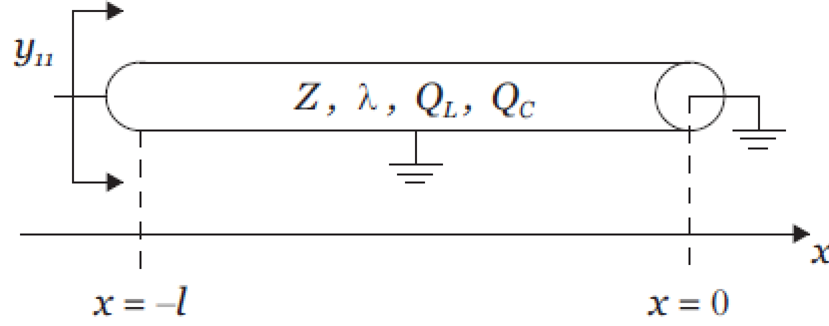


Fig. A.1: Shorted transmission line.

To derive the expression for Q_{net}, the equations for W_m and W_e must first be analytically derived. Then the results of (A.7)–(A.9) can be used to determine the scaling factors η_L and η_C. If the location of the short is at $x = 0$ (Fig. A.1), then for an ideal lossless line, the voltage and current phasors on the line, as a function of position x, are [119]

$$V = -2jV_+ \sin(\beta x) \qquad (A.10)$$

$$I = 2\frac{V_+}{Z_0}\cos(\beta x) \qquad (A.11)$$

where V_+ is the voltage in the positively traveling wave. The time origin is selected such that V_+ is real.

For a low-loss transmission line of length l, if we assume that the current and voltage are not significantly affected by the losses on the line, then the average stored magnetic and electric energy are

$$W_m = \int_{-l}^{0} \frac{L|I|^2}{4} dx \approx \frac{L{V_+}^2 l}{2Z^2}\left(1 + sinc\left(\frac{4l}{\lambda}\right)\right) \qquad (A.12)$$

$$W_e = \int_{-l}^{0} \frac{C|V|^2}{4} dx \approx \frac{1}{2} C {V_+}^2 l \left(1 - sinc\left(\frac{4l}{\lambda}\right)\right) \qquad (A.13)$$

Where

$$Sinc(t) \equiv \frac{\sin(\pi t)}{\pi t} \qquad (A.14)$$

Substituting (2.45) and (2.46) into (2.40) and (2.41), we find

$$\frac{1}{Q_{net}} = \frac{1}{\eta_L Q_L} + \frac{1}{\eta_C Q_C} \qquad (A.15)$$

Where

$$\frac{1}{\eta_L} = \frac{1}{2sinc(\frac{4l}{\lambda})} + \frac{1}{2} \qquad (A.16)$$

$$\frac{1}{\eta_C} = \frac{1}{2sinc(\frac{4l}{\lambda})} - \frac{1}{2} \qquad (A.17)$$

For transmission lines that are much shorter than a wavelength, the shorted stub looks inductive, $\eta_C >> \eta_L$, and Q_C can often be neglected. For example, if $l < 0.1\lambda$ then $\eta_C > 7.2\eta_L$.