Characterization of Analog and Mixed-Signal Circuit Reliability Issues Using On-Chip Monitors

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Dedication

This thesis is dedicated to my parents and family members, and true friends who are always there for me when they'd rather be anywhere else.

Abstract

As CMOS technology continues scaling down, reliability issues have become more challenging with each technology node. With this trend, the reliability on devices and digital gates have been well studied and characterized. However, despite the growing interest in analog/mixed-signal (AMS) circuit reliability, the reliability characterization in AMS circuits has not be widely reported due to complexity of the circuit and the difficulty in measuring subtle performance shifts. It is as such more sophisticated and difficult to characterize and understand as compared to the reliability of a simple transistor and a digital logic. Off-chip measurements for AMS reliability characterization can be considered using several off-chip components such as high-speed probes, off-chip drivers (OCDs), and a spectrum analyzer. But, it requires sophisticated interconnecting cables, packages, or connectors which needs expensive design effort. Also, each of these components can introduce inaccuracy in the measurement. This is critical for the aging testing of the noise sensitive AMS systems. To this end, we propose several on-chip in-situ monitoring circuits enable noise immune and high precision aging testing.

In the first part of this thesis, we explore the impact of device aging on the frequency and phase noise degradation in an all-digital phase locked loop (ADPLL), which is a key building block for processor clock generation and wireless communication. This work presents frequency and phase noise degradation data measured from a standard ADPLL circuit fabricated in a 65nm process, using simple on-chip monitoring circuits. Our study shows that precise measurement of aging-induced timing shifts in ADPLLs is possible using digital circuits such as counters, flip-flops, and a programmable delay line. The

proposed approach does not require an extensive test setup and allows automated testing using a simple serial interface. Experimental data shows that ADPLL phase noise degrades with aging even though the output frequency is maintained constant due to the ADPLL feedback operation. Results show that applying high temperature annealing can recover most of the phase noise degradation while natural recovery alone was not enough to fully recover the phase noise due to permanent hot carrier injection (HCI) and bias temperature instability (BTI) damage. In certain high-reliability applications where parts cannot be easily replaced and a long lifetime must be ensured (e.g. space electronics), annealing using an on-chip heat source may be a viable option.

In addition to that, in this thesis, we experimentally explore reliability of an analog-to-digital converter (ADC). A counter based measurement circuit is proposed for in-situ ADC non-linearity measurements such as differential non-linearity (DNL) and integral non-linearity (INL). An array of counters collects the histogram of the ADC output codes for a triangular input voltage. Since the ADC operation and data transfer operation are separated in time, the DNL and INL results are immune to noise in the measurement setup. Using the proposed measurement method, we studied short-term BTI effects in a successive-approximate-register (SAR) ADC under different operating conditions. The test chip was fabricated in 65nm CMOS. Results confirm that subtle DNL shifts can be accurately measured using the proposed method.

Next, an on-chip reliability odometer based on a ring oscillator array with dual power rails is proposed for the first time, which is capable of characterizing all four types of BTI modes at a single system. These four BTI stress can be occurred in either digital or analog

building blocks in a system. Thus, it enables to fully characterize the degradation of all the digital and analog circuit components caused by four different BTI stress in the system. Stressed ring oscillators with independent dual power rails are implemented in which odd and even stages of an inverter chain are subject to different stress voltage configurations. An on-chip beat frequency detection circuit with 3 reference ring oscillators achieves a frequency measurement resolution as low as 0.01% with a short measurement interruption time of 1μs. Extensive BTI data collected from a 65nm ROSC array is presented for different stress conditions.

Lastly, in this thesis, an Op-AMP reliability odometer using an on-chip monitor, on-chip signal generator, and an on-chip heater is proposed for the first time in 65nm CMOS process. A comparator and a counter are implemented to monitor the Op-AMP output before and after the stress. Two monitoring methods are employed: (i) monitoring output transient response for a square wave input, and (ii) monitoring output transient for power/load transition. The proposed on-chip heater enables the precise on-chip temperature control. Also, the on-chip monitor and signal generator achieve accurate aging dynamics characterization for the Op-AMP transient response.

To sum up, several simple on-chip monitoring circuits are proposed to characterize circuit reliability aspects in the AMS systems such as ADPLL, SAR-ADC, and Op-AMP. Also, we propose the new BTI odometer for sensing all four BTI stress effects at a single system. Their performance are verified with the measurement results obtained from working test chips implemented in 65nm LP and GP CMOS technologies. Moreover, in-

situ measurement schemes employed in these circuits enable accurate measurement without requiring sophisticated measurement setup for the noise sensitive AMS systems.

Table of Contents

List of Figures

Chapter 1. Introduction

With the continued scaling of CMOS technology, the detrimental impact of device failures or parametric shifts have become more severe. While the impact of device aging on digital logic or memory circuits for different stress mechanisms such as hot carrier injection (HCI) and bias temperature instability (BTI) have been relatively well studied, their impact on analog and mixed-signal circuit performance have yet to fully understand. Recently, mixed-signal applications are increasingly relying on digital circuits since they now include many digital-intensive or all-digital circuit blocks which play crucial roles in the overall performance. Therefore, the negative impact of the device aging on the digital circuit blocks not only affect digital logic performance, but also degrade the performance of mixed-signal systems incorporating them. Thus, these trends warrant further investigation of aging issues in critical mixed-signal building blocks. The device aging data for process characterization is mostly obtained through device probing experiments. The external equipment used in those tests can be expensive, and testing individual device takes long experiment times. Several on-chip systems have recently been proposed to monitor circuit aging. However, no method has been presented to characterize the reliability effects on the mixed-signal systems. The off-chip measurement for the mixed-signal systems can be done using several off-chip components such as high-speed probes, off-chip drivers (OCDs), and a spectrum analyzer. But, it requires sophisticated high-speed probes, packages, or connectors which needs expensive design effort. Also, each of these components can introduce inaccuracy in the measurement. This is critical for the aging

testing of the noise sensitive mixed-signal systems. In this thesis, among several mixed-signal systems, reliability of an all-digital PLL (ADPLL) and a successive-approximate-register analog-to-digital converter (SAR ADC) were experimentally studied. Furthermore, we proposed simple on-chip monitoring circuits enable noise immune aging testing. The proposed approach does not require an extensive test setup and allows automated testing using a simple serial interface.

Additionally, for the first time, the on-chip monitor capable of sensing the four different BTI induced aging effects is proposed in a single system. These four BTI stress can be occurred in both digital and analog building blocks in a system. Thus, it enables to fully characterize the degradation of all the digital and analog circuit components caused by four different BTI stress in the system.

Our proposed designs are demonstrated in working test-chips implemented in 65nm low-power (LP) and general purpose (GP) CMOS technology and the on-chip monitoring circuits enable to fully characterize the aging effects on the mixed-signal systems.

1.1 All-Digital PLL Reliability Study Using On-chip Monitors

Hot carrier injection (HCI) and bias temperature instability (BTI) are the two major front-end-of-line aging mechanisms in advanced CMOS technologies. Fig. 1.1 illustrates HCI and BTI induced aging occurring in individual transistors and a standard inverter. While the effects of aging and recovery on devices and digital gates have been well studied, aging-induced shifts in mixed-signal circuits have not be widely reported due to the complexity of the circuit block and the difficulty in measuring subtle performance shifts

using external test equipment. Recent design trends toward digital intensive mixed-signal implementations (e.g, all digital PLL (ADPLL), time-based ADC, digitally-controlled voltage regulators), warrant further investigation of aging issues in mixed-signal building blocks. The purpose of this work is to understand the impact of device aging on frequency and phase noise degradation of an ADPLL circuit. For precise measurements, we employ on-chip monitors based on standard digital circuits such as counters, flip-flops, and a variable delay line. The proposed approach allows accurate measurements using a simple serial interface without requiring an extensive test setup.

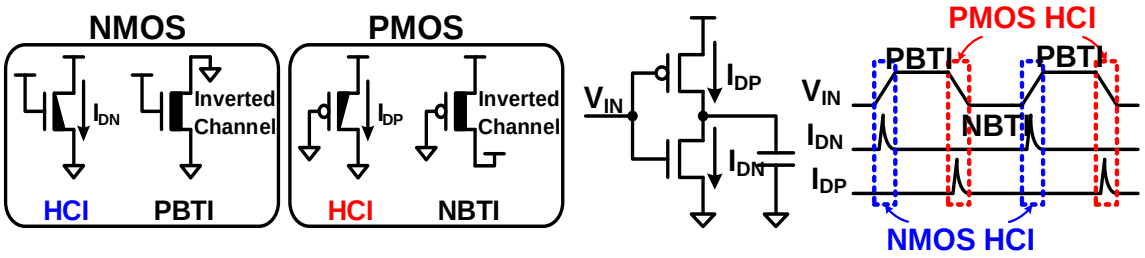


Fig. 1.1: HCI and BTI degradation occurring in NMOS and PMOS devices (left) and an inverter circuit (right).

1.2 SAR-ADC Reliability Study with In-situ Monitors

Despite the growing interest in analog circuit reliability, very few experimental results have been reported on this issue. In an effort to gain a deeper understanding on fast degradation and recovery effects in analog circuits, we design and fabricate the dedicated test chips including a SAR-ADC and in-situ non-linearity measurement circuits. Bias temperature instability (BTI) is a major reliability mechanism that can cause the transistor

Vth to degrade or recover within a few microseconds. When a voltage comparator circuit is exposed to two very different input voltages, the asymmetric BTI aging experienced by the two input transistors can lead to a time-dependent offset voltage. This issue can be detrimental to the linearity and resolution of SAR-ADCs even for a fresh chip. In this work, we design a test chip specifically to study the impact of short-term BTI aging on SAR-ADCs.

We study the effect of (i) duty cycle, (ii) frequency of ADC clock, and (iii) different type of comparator input pairs on short-term BTI effects in SAR-ADC. The most important part of this work is noise immune measurement to detect subtle parameter shifts in ADC due to short-term BTI effects.

The new in-situ integral nonlinearity (INL) / differential nonlinearity (DNL) measurement circuitry is implemented to pick up any subtle changes in ADC linearity. The circuit consists of decoders and a counter bank connected to the SAR-ADC output, and basically counts the number of times the ADC produces a particular output code. The counts are then scanned out for INL/DNL analysis. To further reduce the area of the large counter block, we propose a measurement method based on repetitive ramp up ramp down tests. After repetitive voltage sweeps, we will stitch the partial distributions together to construct the full count distribution. This technique provides a number of important benefits over traditional ADC measurement methods such as higher accuracy, lower noise, simpler test setup, and reduced readout data volume.

1.3 All BTI On-chip Odometer

The parametric shifts or circuit failures caused by negative and positive bias temperature instability (NBTI and PBTI) have become more severe with device scaling. While PMOS NBTI and NMOS PBTI have been understood well, only few studies exist for PMOS PBTI and NMOS NBTI. Particularly, the prior studies show PMOS input transistors in analog circuits such as op-amp can be exposed to PBTI in power down mode. In addition to device probing experiments, several on-chip systems have been proposed to monitor circuit BTI effects. However, no method has been proposed to characterize all four types of BTI mechanisms in a single system. In this thesis, we demonstrate for the first time, an on-chip beat frequency based monitor circuit capable of characterizing frequency shifts caused by all four BTI modes with a high frequency measurement precision (>0.01%). The main innovation is a ring oscillator (ROSC) circuit with dual power rails offering different BTI stress modes. Unwanted device recovery during stress interruptions can be suppressed by the ultra-short stress interrupt time (>1μs).

1.4 Op-AMP Reliability Odometer

Unlike in digital gates where transistors are subject to the full supply voltage or 0V, an Op-AMP consists of a number of transistors with their own bias condition (e.g. different Vgs and Vds). Thus, it is a big challenging to apply the stress and accelerate aging mechanism. If we simply increase the supply voltage for the stress, it does not apply the same aging acceleration effect to all devices in the Op-AMP. To overcome this issue, we

manipulate temperature using an on-chip heater. By applying the same temperature to all the devices in the Op-AMP at the same time, the same amount of acceleration effect can be reflected. Additionally, measuring the aging induced subtle performance shift and fast transient response of Op-AMP is extremely challenging. Practically, it would be impossible to accurately detect the subtle shift in fast transient response of Op-AMP without data loss using the conventional off-chip testing. Therefore, in this thesis, we propose an on-chip monitoring circuit for precise characterization of Op-AMP reliability issues for the first time.

1.5 Summary of Dissertation Contribution

Several contributions have been made in this thesis to characterize circuit reliability effect on analog/mixed signal circuit and system. Proposed techniques are applied in three different types of applications: all digital PLL, analog-to-digital converter, and all BTI odometer.

To summarize the key contributions of this research: (1) all-digital PLL frequency and phase noise are characterized for the first time using on-chip monitors. (2) Counter based measurement circuit is demonstrated for precise characterization of ADC DNL and INL. Using the proposed method, short-term BTI is studied in a 10-bit SAR-ADC in 65nm CMOS. Subtle DNL shifts can be accurately measured using the proposed method. (3) An on-chip reliability monitor capable of characterizing all four types of BTI stress modes is proposed for the first time. (4) An Op-AMP reliability odometer using an on-chip monitor and an on-chip heater is proposed for the first time in 65nm CMOS process

The remainder of this thesis is organized as follows. Chapter 2 illustrates the all-digital PLL reliability study using simple on-chip monitoring circuits. Chapter 3 presents a counter based ADC non-linearity measurement circuits and its application to reliability testing. An all BTI (PMOS NBTI, PMOS PBTI, NMOS NBTI, and NMOS PBTI) odometer based on a dual power rail ring oscillator array is described in chapter 4. Chapter 5 describes the Op-AMP reliability odometer. Finally, chapter 6 provides a summary of the thesis.

Chapter 2. All-Digital PLL Reliability Measurement Using On-Chip Monitors

2.1 Introduction

While the effects of aging and recovery on devices and digital gates have been well studied, aging-induced shifts in mixed-signal circuits have not be widely reported due to the complexity of the circuit and the difficulty in measuring subtle performance shifts. Recent design trends toward digital intensive mixed-signal implementations (e.g, all digital PLL (ADPLL) [1]-[3], time-based ADC [4]-[6], digitally-controlled voltage regulators [7]-[9]), warrant further investigation of aging issues in critical mixed-signal building blocks. Typically, off-chip measurement can be done using several components such as high-speed probes, off-chip drivers (OCDs), and a spectrum analyzer, as shown in Fig. 2.1. However, it requires sophisticated high-speed probes, packages, or connectors which needs expensive design effort. Also, each of these components can introduce inaccuracy in the measurement.

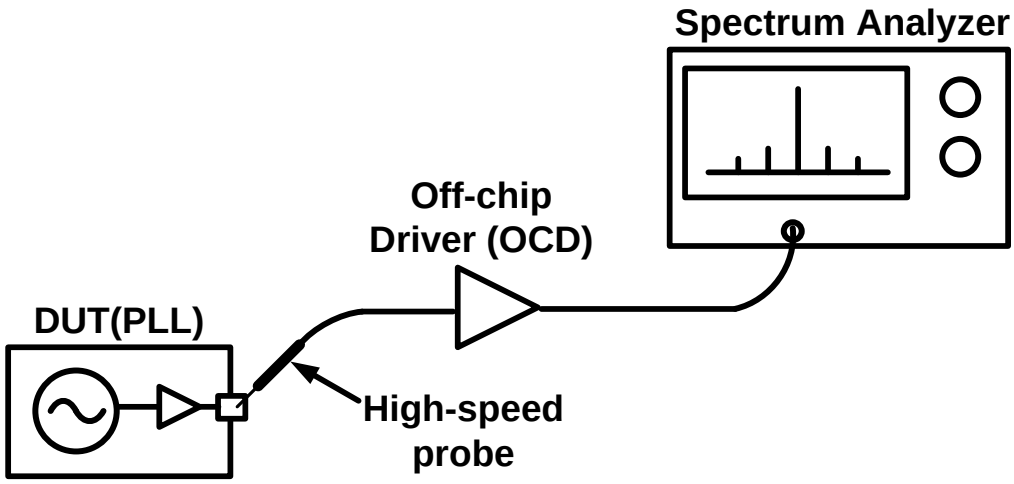


Fig. 2.1: Conventional off-chip measurement.

Among several mixed-signal circuits, our target circuit in this work is ADPLL (Fig. 2.2). Phase locked loop (PLL) is a key building block and widely employed for clock generation, wireless communication, and other electronic applications. PLL can be implemented as either analog or digital circuits. Recently, design trend towards to ADPLL with scaling down technology. The ADPLL is a digital control system that generates an output signal whose phase is related to the phase of the reference input signal. Also, ADPLL is used for making an output signal whose frequency is faster than the frequency of the reference input signal. It consists of several digital circuit components such as a phase detector, a PI controller, a digitally controlled oscillator (DCO), and a frequency divider in the feedback loop. The DCO generates a periodic signal, and its frequency is divided by the frequency divider. Then, the frequency divider output signal is fed back to the phase detector. The phase detector compares the phase of the feedback signal with the phase of the reference input signal. According to comparing results, the output of the phase detector and the PI controller are generated, which are utilized for adjusting the oscillator

to keep the phases matched. Keeping the phases of the input and the feedback signal in this condition also implies keeping frequencies of the input and the feedback signal the same. Despite the recent trend of digital intensive PLL design, no experimental studies have been reported for reliability of ADPLL, which directly have a negative impact on the performance and life time. Since we study on reliability of ADPLL for the first time, we defined frequency and phase noise as a reliability figure-of-merit of ADPLL, because these two factors are main performance parameter of frequency synthesizer such as PLL system. For example, if frequency gets much degraded, ADPLL can get into unlock condition. Also, an increase of phase noise can cause phase impurity in wireless communication by inducing channel interference to adjacent signals.

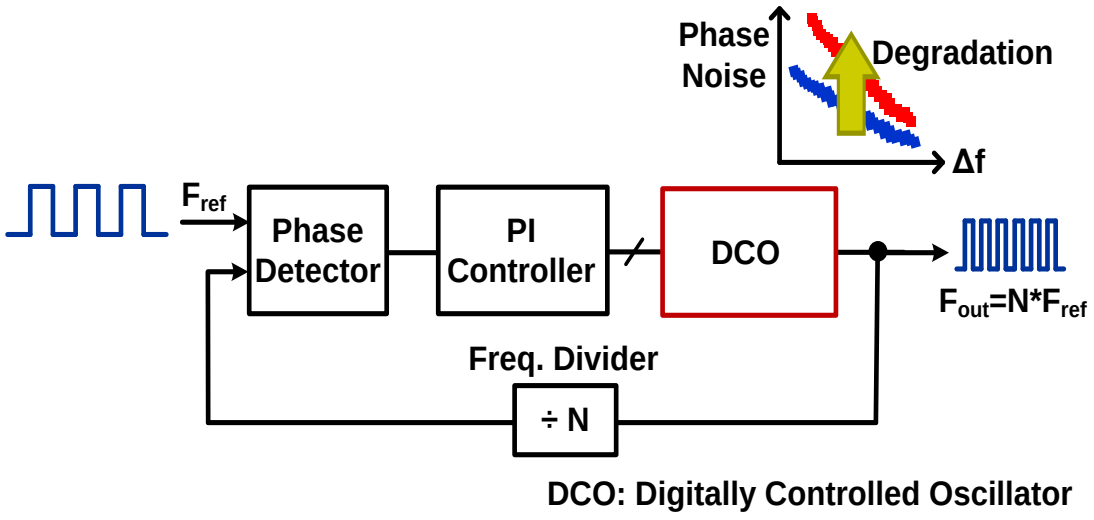


Fig. 2.2: Target circuit: all-digital phase locked loop (ADPLL) and ADPLL reliability figure-of-merit.

Since the DCO generates the output of ADPLL, the frequency and the phase noise degradation of the DCO can significantly affect to overall ADPLL reliability. Therefore, we characterize the frequency and phase noise degradation not only in open-loop DCO (i.e. open-loop) but also in ADPLL including the DCO (i.e. closed-loop with feedback). It implies that how much degradation of the DCO impact on ADPLL performance and reliability is explored.

To this end, this paper presents frequency and phase noise degradation data measured from a standard ADPLL circuit fabricated in a 65nm process, using simple on-chip monitoring circuits. Our study shows that precise measurement of aging-induced timing shifts in ADPLLs is possible using digital circuits such as counters, flip-flops, and a variable delay line. The proposed approach does not require an extensive test setup and allows automated testing using a simple serial interface. Detailed frequency and phase noise window data under various stress, recovery, and annealing conditions are presented.

In this work, using simple on-chip monitoring circuits, we precisely characterized the impact of hot carrier injection and bias temperature instability on frequency and phase noise degradation of a 65nm all-digital PLL circuit. Experimental data shows that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. Results show that applying high temperature annealing can recover most of the phase noise degradation.

2.2 Test Structure and Experiment Flow

2.2.1. DCO and PLL Test Structure

The ADPLL test chip with on-chip monitors for measuring the frequency and phase noise degradation is shown in Fig. 2.3. The PLL itself contains a digitally controlled oscillator (DCO) with capacitor banks, a bang-bang phase frequency detector (BB PFD), a digital loop filter, and a frequency divider. During stress mode, a supply of 2.4V is applied to the stress DCO while the fresh reference DCO is powered off. The stressed DCO oscillates at its natural oscillation frequency inducing HCI and BTI. In measurement mode, the supply voltages of both DCOs are switched to the nominal voltage of 1.2V. On-chip LDOs are implemented for fast power supply transition between stress and measurement modes. We also employed on-chip monitor circuits to measure subtle frequency and phase noise shifts induced by device aging.

2.2.2. Experiment Flow

We measured the frequency and phase noise degradation (indirectly) which are critical performance parameters of a PLL system. To fully understand the aging implications on these parameters, we tested the ADPLL in both open loop and closed loop configurations.

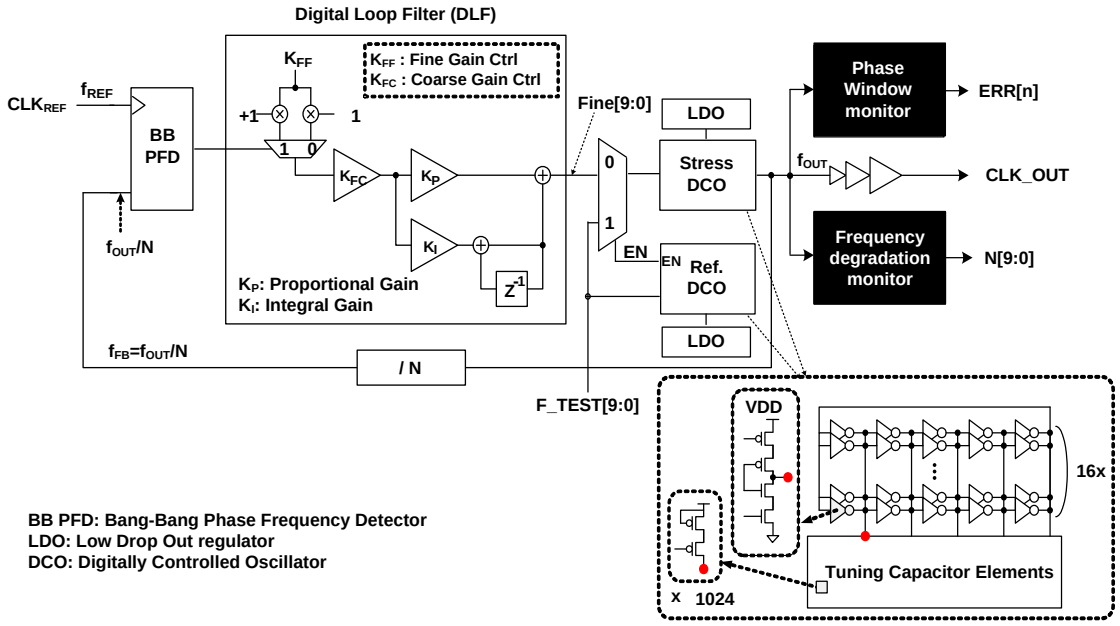
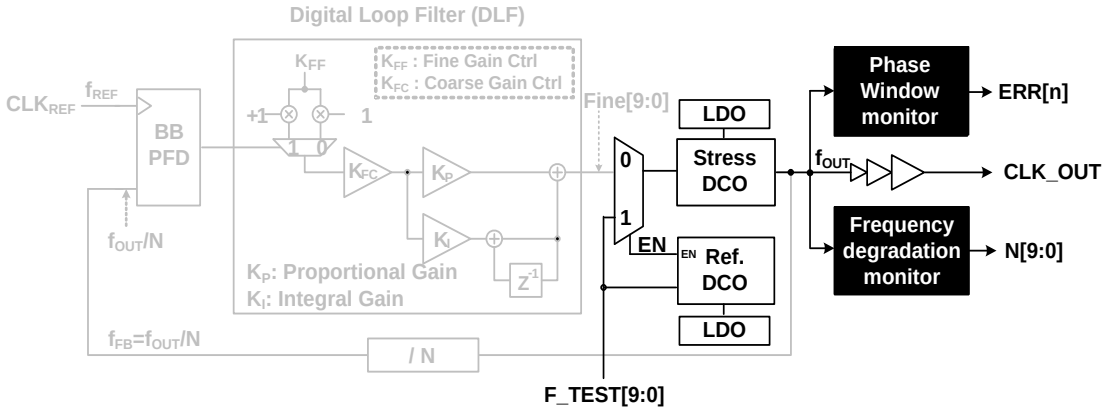
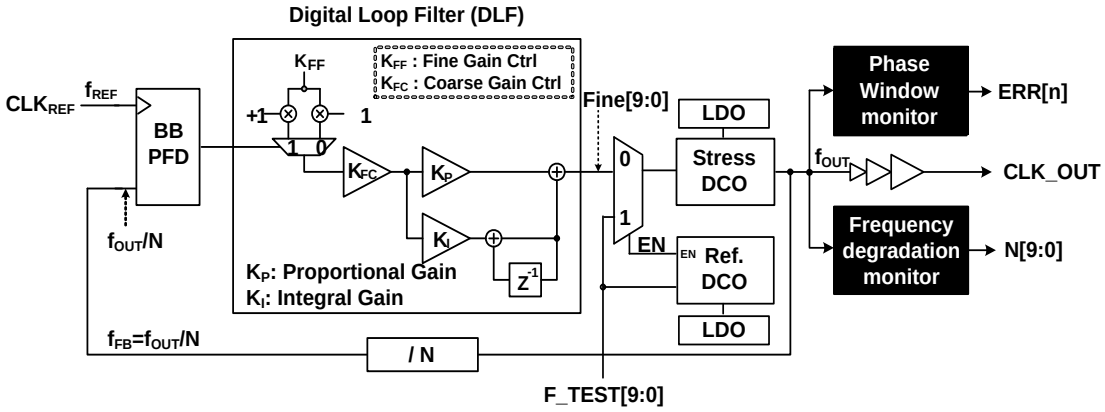


Fig. 2.3: All-digital PLL with on-chip frequency and phase noise measurement circuits.

By simply turning off the feedback loop of ADPLL as shown in Fig. 2.4(a), we can measure the open-loop characteristics. High voltage stress was applied to study frequency and phase noise. We also measured recovery effect under different annealing temperatures (~100°C, and ~240°C). Fig. 2.4 (b) shows the standard ADPLL configuration for testing closed-loop characteristics.



(a) Open-loop DCO Test Configuration



(b) Close-loop ADPLL Test Configuration

Fig. 2.4: (a) Open-loop test configuration. DCO's open loop frequency is measured. (b) Closed-loop test configuration. Locked ADPLL frequency is measured.

Fig. 2.5 shows the frequency measurement flow. Initially, frequency of the pre-stress DCO is measured in both open- and close-loop configurations. Then, we start applying the stress to the DCO and check the frequency shift in the open-loop configuration using the

on-chip frequency shift monitor. This process is repeated until the frequency shits to certain percentage (e.g. *A %*) of the initial frequency. If the frequency shift exceeds over *A %*, we stops applying stress and power down for the DCO at room temperature. In this condition, some portion of the aging induced frequency degradation can be naturally recovered. In the natural recovery phase, we measure the frequency recovery in both open- and close-loop DCOs. After natural recovery, we place the package on the hot plate for 100°C thermal annealing. The frequencies of both the open- and the close-loop DCO are measured to check the thermal annealing effect. After the 100°C annealing measurement, we cool down the chip and repeat the aforementioned steps for higher thermal annealing (i.e. ~240°C).

Fig. 2.6 shows the experimental flow for the phase noise measurement. As same as the frequency measurement, we measure the initial value of the pre-stressed DCO to record the result before applying stress. But, difference from the frequency shift measurement is that we measure both initial frequency and phase noise information. This is because the correlation between frequency and phase noise will be defined after this experiment flow. Unlike the frequency measurement, the phase noise measurement takes a long time (~minutes) as we use a bit error rate testing to define phase noise shift. For the testing, the DCO must perform for long time as much as a thousands of cycles. It indicates that the phase noise shift due to the aging can be recovered during the long test time. Thus, to avoid natural recovery of the phase noise during the measurement, we take phase noise measurements after sufficient time (~45mins) to ensure natural recovery is finished. In order to obtain a correlation between phase noise and frequency, the flow is repeated. Once

several data points are collected, the chip is placed on the hot plate with 240°C to check the effect of high temperature annealing in terms of phase noise recovery.

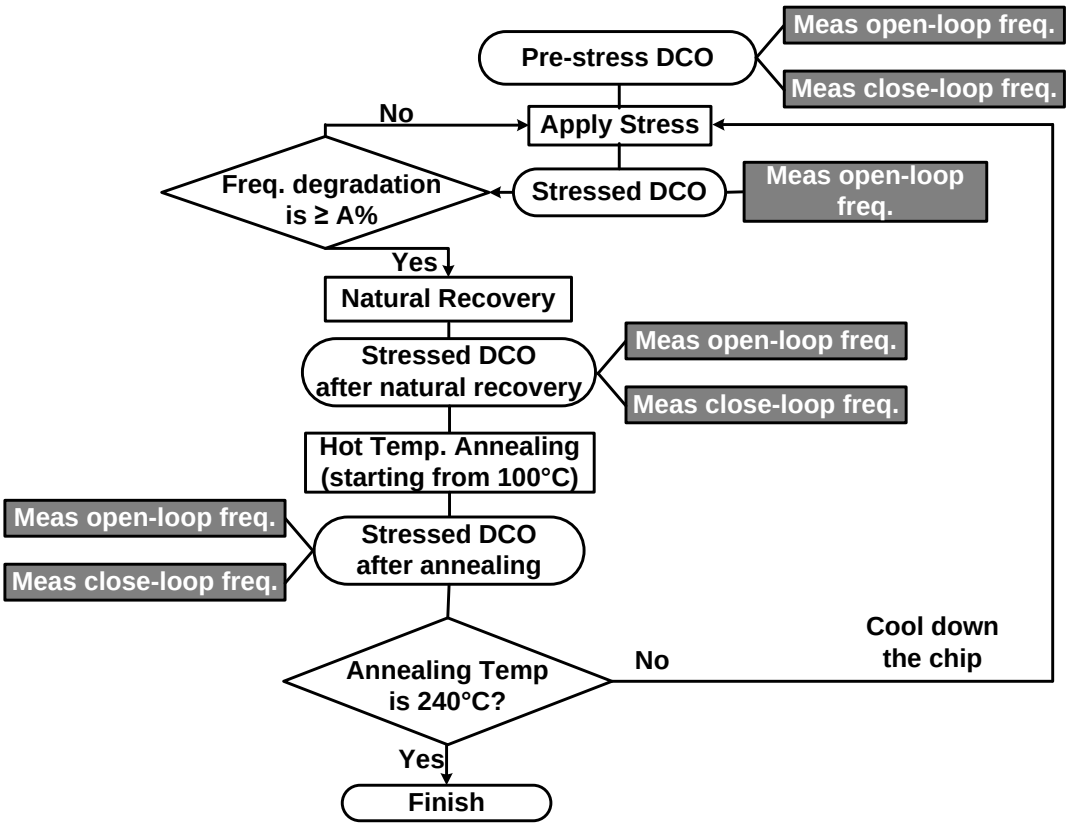


Fig. 2.5: Experimental flow for frequency shift measurement.

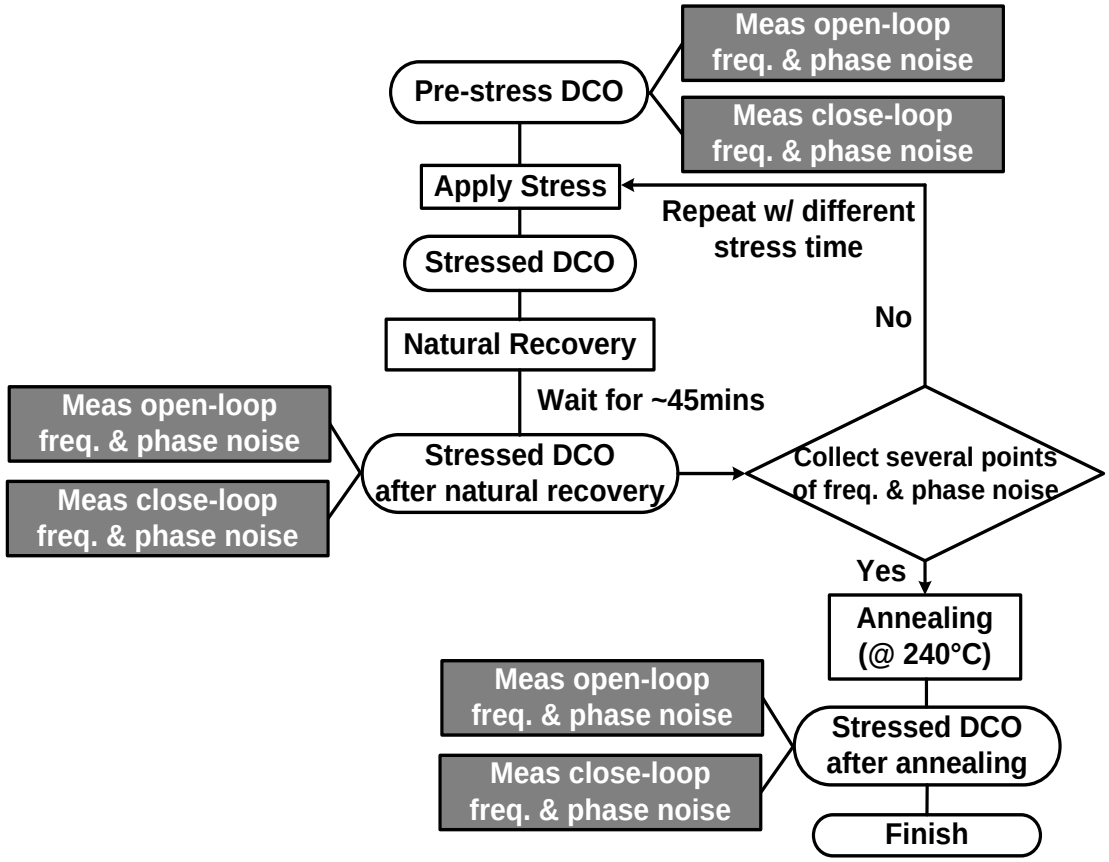


Fig. 2.6: Experimental flow for phase noise measurement.

2.2.3. Frequency and Phase Noise Window Monitors

Fig. 2.7(a) shows one of the on-chip monitors, which is the proven-and-tested beat frequency (BF) detection circuit for measuring the frequency shift of the stressed DCO [10]-[16]. The output signal of the D-flip-flop exhibits the beat frequency, fbeat = fref - fstress. The beat frequency is measured by counting the number of reference DCO periods that can fit within one period of the phase comparator output signal. Using the digital output code N[9:0], we can compute the frequency shift in the stressed DCO with picosecond accuracy. For example, when the initial frequency difference is calibrated to be 1%, an

additional 1% frequency change due to the stress leads to an output count change from 100 to 50 (Fig. 2.8). Therefore, the minimum frequency measurement resolution, corresponding to a count change from 100 to 99, is 0.01%. The BF monitor can measure frequency shifts as small as 0.01% within a few microseconds. The short interrupt time prevents unwanted BTI recovery from corrupting the aging data.

Phase noise is typically characterized by measuring the PLL output clock signal using a high-speed sampling oscilloscope or spectrum analyzer. In this work, we implemented an on-chip phase window (PW) monitor circuit which can indirectly measure the phase noise amplitude. The circuit shown in Fig. 2.7(b) consists of a tunable delay line, an XOR gate, sampling flops, and a 10-bit counter. Basically, the ADPLL clock period is compared with the tunable delay by measuring the error rate. Let us assume that initially the tunable delay is much shorter than the ADPLL clock period. Then, there will be no error and thus the counter value will be zero.

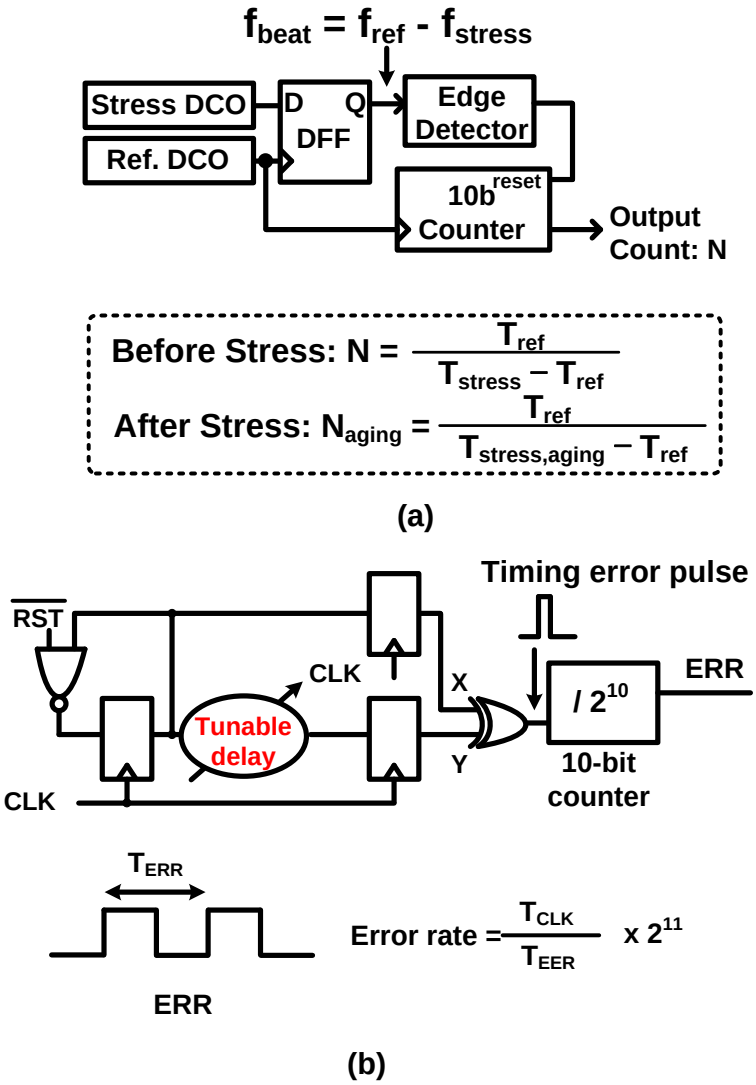


Fig. 2.7: (a) Frequency degradation monitor based on "silicon odometer" beat frequency detection scheme. (b) Phase window monitor based on a tunable delay.

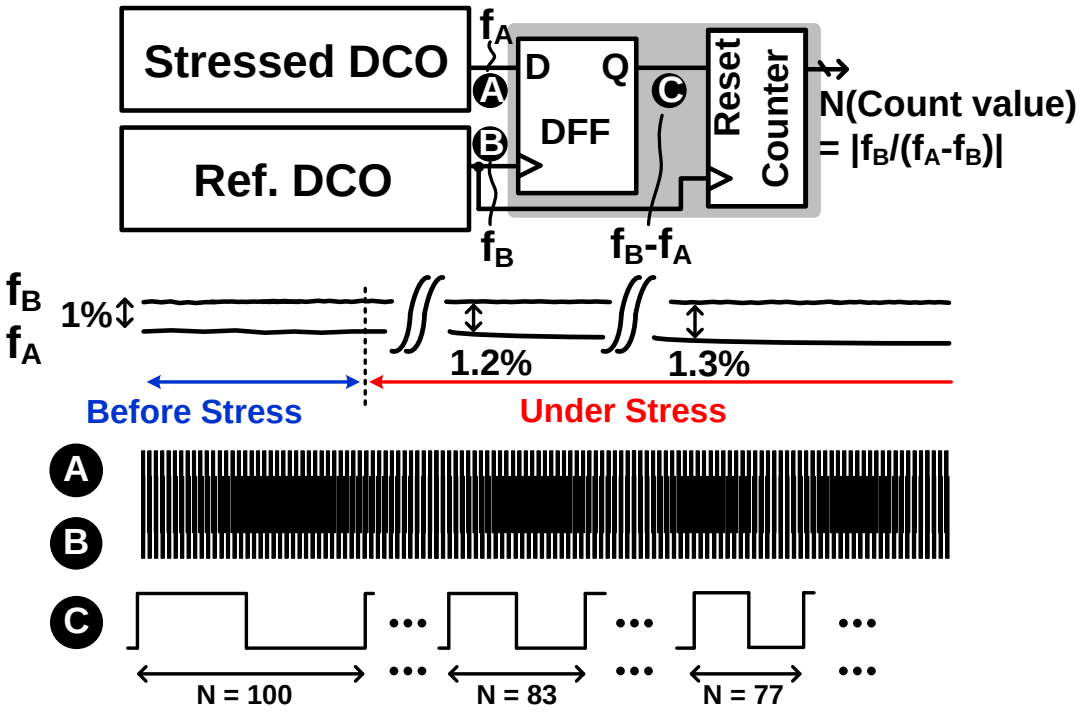


Fig. 2.8: Beat frequency monitor under stress. The output count *N* represents the number of f_B clock cycles that can fit within a single beat frequency (i.e., $f_A - f_B$) clock period.

As the tunable delay is gradually increased, errors will start to occur which can be detected by the XOR gate and tallied by the 10-bit counter. That is, any time there's an error in signal Y due to timing failure, the XOR gate generates an error pulse which increments the 10 bit counter. By measuring the average period of the counter output signal ERR and the period of the stressed DCO, error rate (or 1-error rate) can be calculated as shown in [17] -[19].

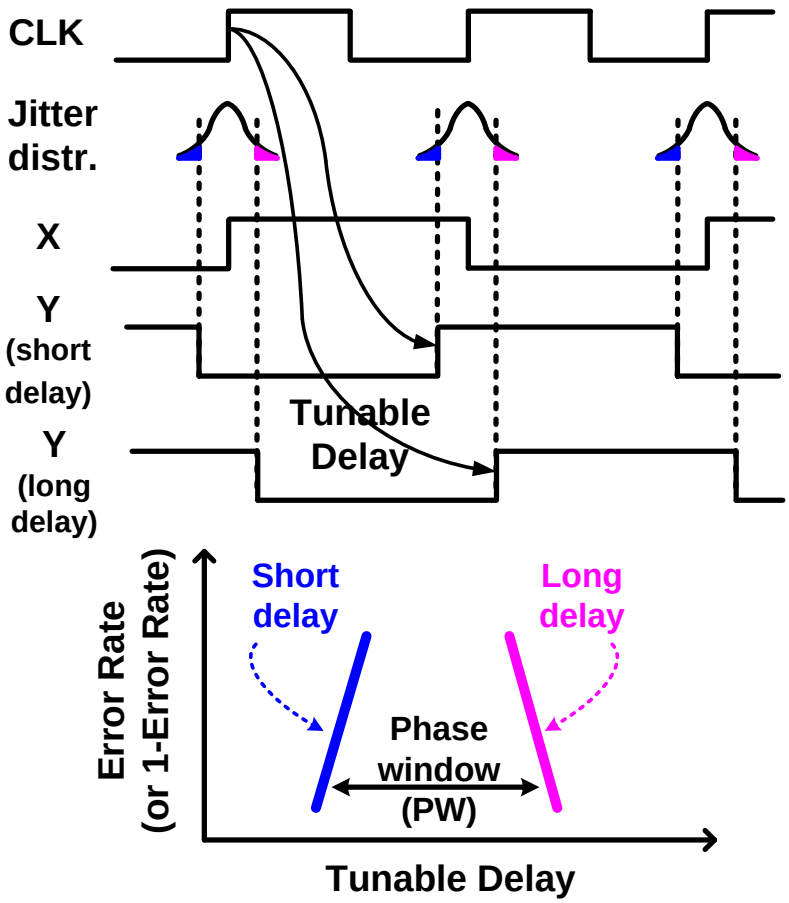


Fig. 2.9: Phase noise degradation can be indirectly measured by sweeping the tunable delay.

This is how the left boundary of the phase window denoted as “short delay” in Fig. 2.9 is measured. As we continue to increase the tunable delay, the error will continue to rise, eventually reaching 100%. The actual error rate can be deduced based on the error count and the total number of cycles. The right side boundary in Fig. 2.9 is measured in this way. Phase noise in the ADPLL output will affect the error rate which can be indirectly monitoring using the proposal circuit. The phase window for a specific error rate can be obtained by measuring the tunable delay as shown in Fig. 2.9.

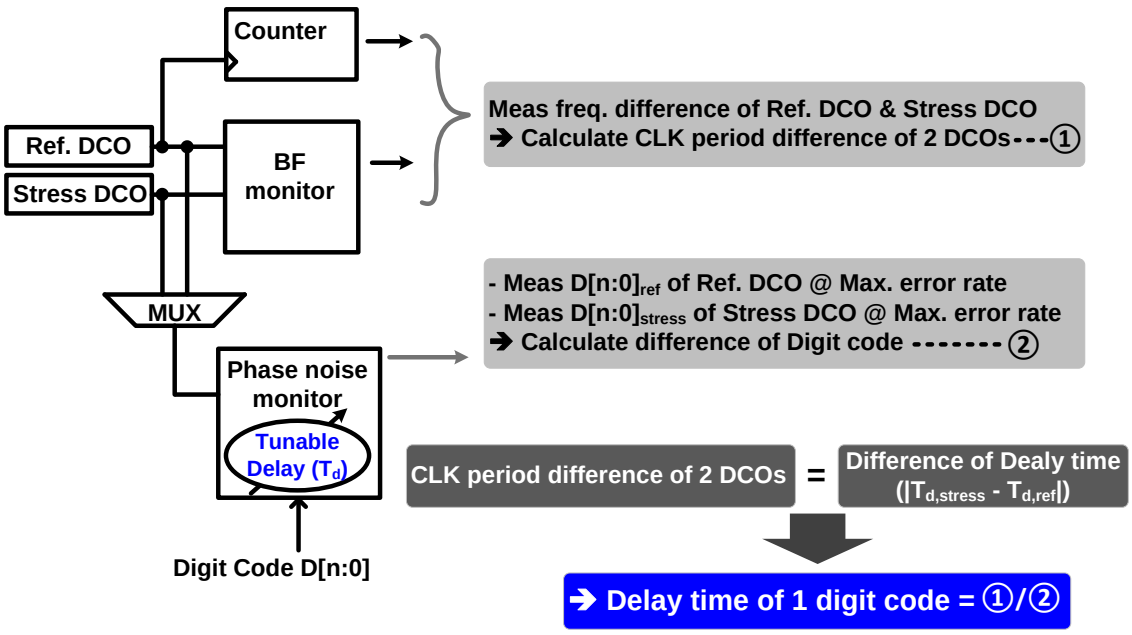


Fig. 2.10: Phase noise degradation can be indirectly measured by sweeping the tunable delay.

Fig. 2.10 shows the test method to measure the absolute tunable delay time of the tunable delay line of the phase noise monitor. First, we measured the frequency difference of the reference and the stressed DCO using the on-chip BF monitor circuit. From the frequency difference, CLK period difference of 2 DCOs can be calculated. Next, the digitally controlled tunable delay is increased by increasing digital code until the error rate became maximum. Since the error is occurred as the tunable delay gets close to CLK period, the tunable delay time at the max. error rate can indicate CLK period. Based on this, the difference of the delay time of 2 DCOs can be same as the CLK period difference of 2 DCOs which was measured in the first step. Finally, we can obtain the unit tunable delay time by dividing the difference of delay time by difference of digital code.

2.3 Experiment Results

2.3.1. Experiment Setup

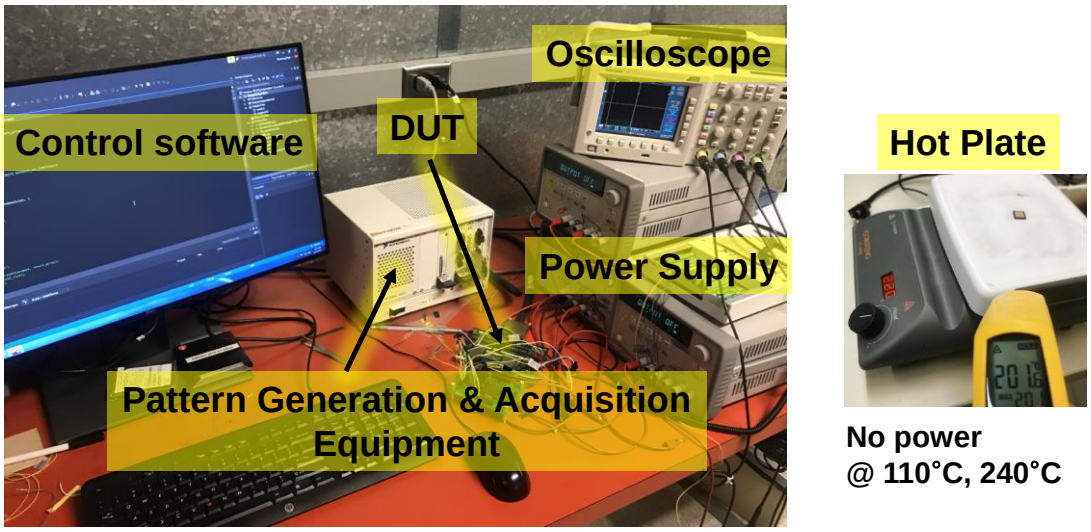


Fig. 2.11: Measured frequency degradation of open-loop DCO using beat frequency detection circuit.

National Instrument (NI) PXIe-1073 is used for data/clock pattern generation and acquisition. C/C++ code based software controls the NI PXIe-1073, and DAQ board is used for bias voltage generation. For hot temperature annealing (110°C, and 240°C), we use an off-chip hot plate equipment which can manually control temperature of hot plate as shown in Fig. 2.11.

2.3.2. Open-loop Stress and Recovery Experiments

We measured the open-loop DCO frequency using the BF monitor circuit in Fig. 2.12, while applying a 1.2V nominal voltage and a 2.4V stress voltage at 27°C. The stress

frequency was the natural oscillation frequency of the DCO at 2.4V, which is 1.56 GHz. The beat frequency was measured at a nominal supply of 1.2V at 27°C, while the measurement interrupt time was 2µs. A combination of BTI and HCI caused a frequency shift of 8.49% after 2.22 hours of stress.

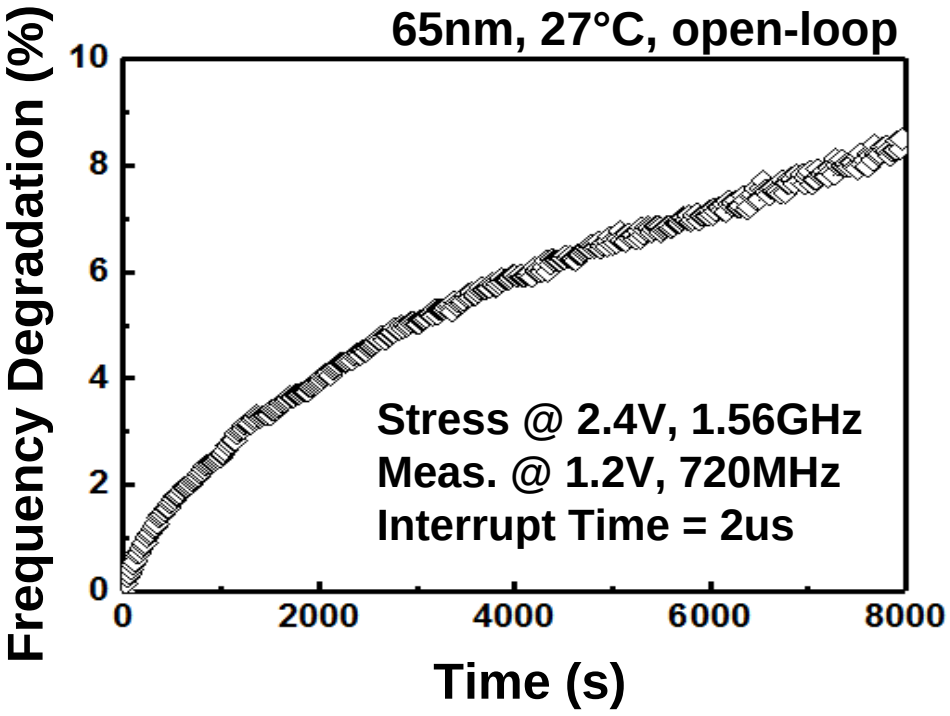


Fig. 2.12: Measured frequency degradation of open-loop DCO using beat frequency detection circuit.

Fig. 2.13 shows the DCO phase window measured using the on-chip PW monitor. Since phase window measurements take a long time (minutes), for consistency, the frequency was measured after sufficient recovery. The phase window is defined as the range of tunable delay where error rate is higher than 1E-8. Fig. 2.13 (right) shows the

open-loop phase window versus DCO frequency degradation. The phase window becomes larger with more degradation in the DCO frequency.

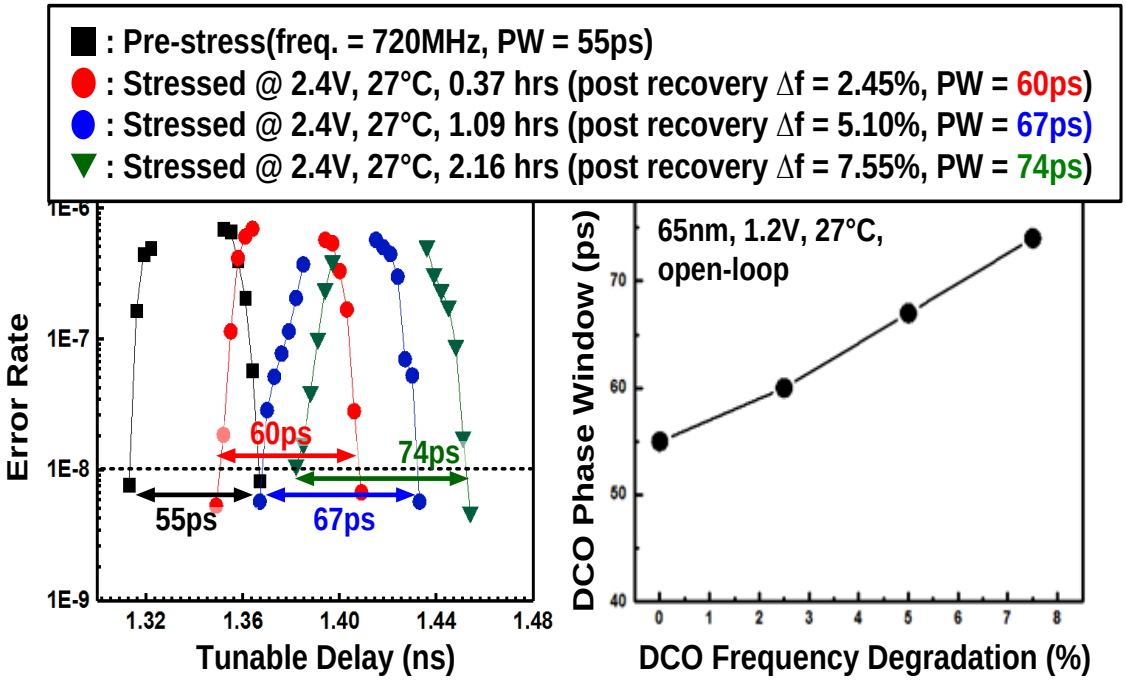


Fig. 2.13: (Left) Measured open-loop DCO phase window before and after stress. (Right) Measured open-loop phase window versus open-loop DCO frequency degradation.

Frequency recovery under different temperatures is shown in Fig. 2.14. Upon removing the 2.4V stress voltage, natural recovery at 27˚C induced a 0.76 % frequency recovery (Fig. 2.14, left, (b)). Then we place the package on a hot plate for annealing experiments. After a 20 second annealing period where the package temperature is raised to 110˚C, we let the package cool down to room temperature before taking frequency measurements. Fig. 2.14 (right) shows the measured temperature profile for a single annealing cycle. We repeat this cycle while measuring the frequency between each

annealing period. Annealing the chip repeatedly at 110°C resulted in a 1.9% frequency recovery. We reapplied the 2.4V stress voltage to bring the chip back to the state after the natural recovery, and repeated the annealing test at 110°C and 244°C.

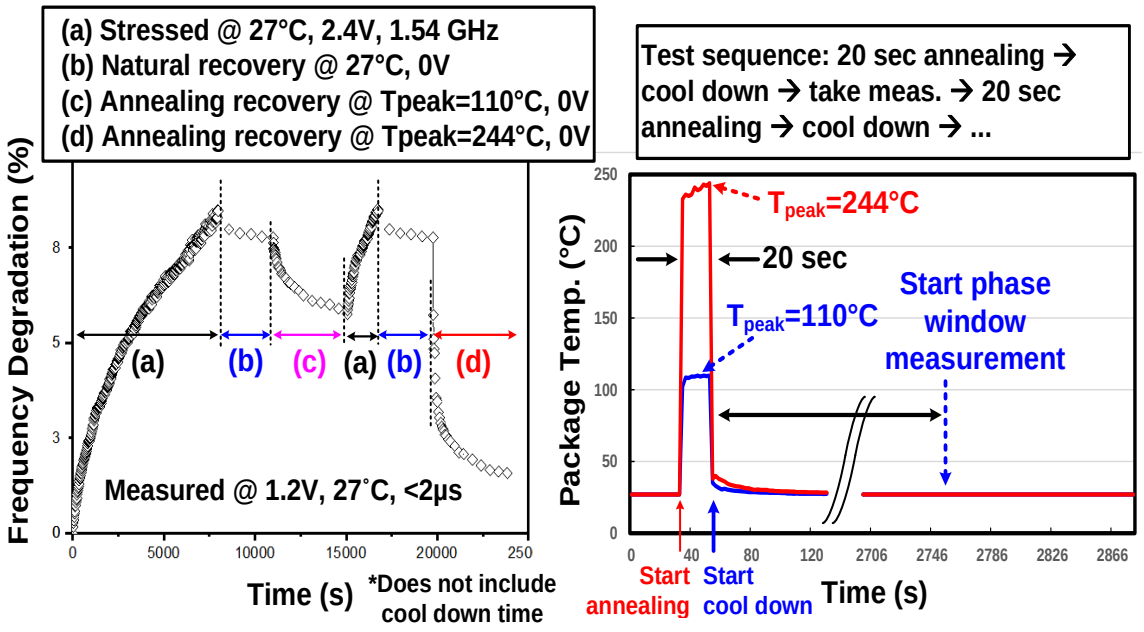


Fig. 2.14: (Left) Measured frequency shift under different stress and recovery conditions. (Right) Annealing test sequence. The package is cooled down after each 20 second annealing period to ensure accurate frequency measurements.

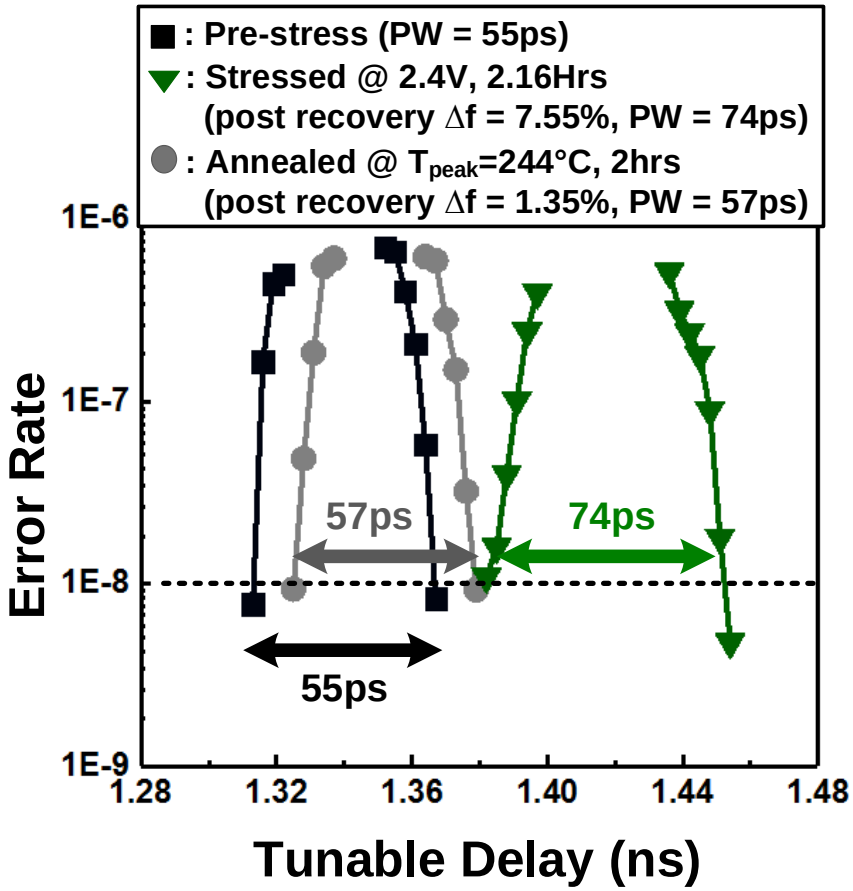


Fig. 2.15: Measured open-loop phase window curves for pre-stress, stressed, and annealed DCOs.

Annealing at higher temperature results in stronger recovery. We suspect annealing cures HCI degradation while BTI is mostly recovered by natural recovery. Fig. 2.15 shows the phase window recovery after annealing at 244°C for 2 hours.

2.3.3. Closed-loop Stress and Recovery Experiments

Fig. 2.16 shows the closed-loop ADPLL frequency versus open-loop frequency degradation of DCO. The open-loop DCO is degraded under same stress condition as that described in previous section, stress voltage 2.4V and 27˚C. And, after the stress, the frequency of closed-loop PLL was measured in nominal condition, 1.2V and 27˚C. Even though the DCO frequency is degraded, the feedback loop of the ADPLL ensures that the output frequency is constant. Fig. 2.17 shows the phase window of the ADPLL versus the DCO frequency degradation.

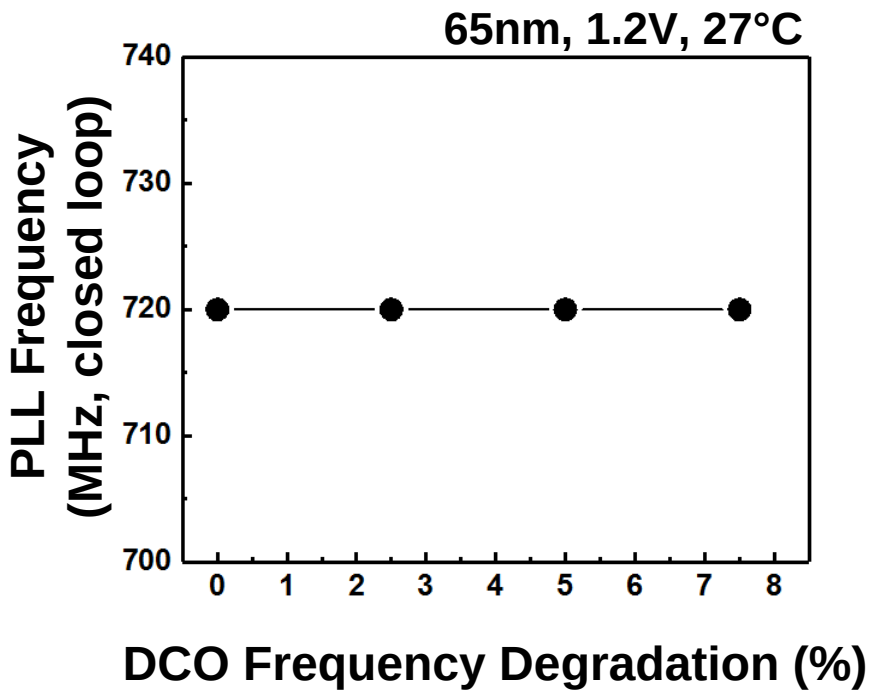


Fig. 2.16: Closed-loop PLL frequency remains constant despite DCO frequency degradation.

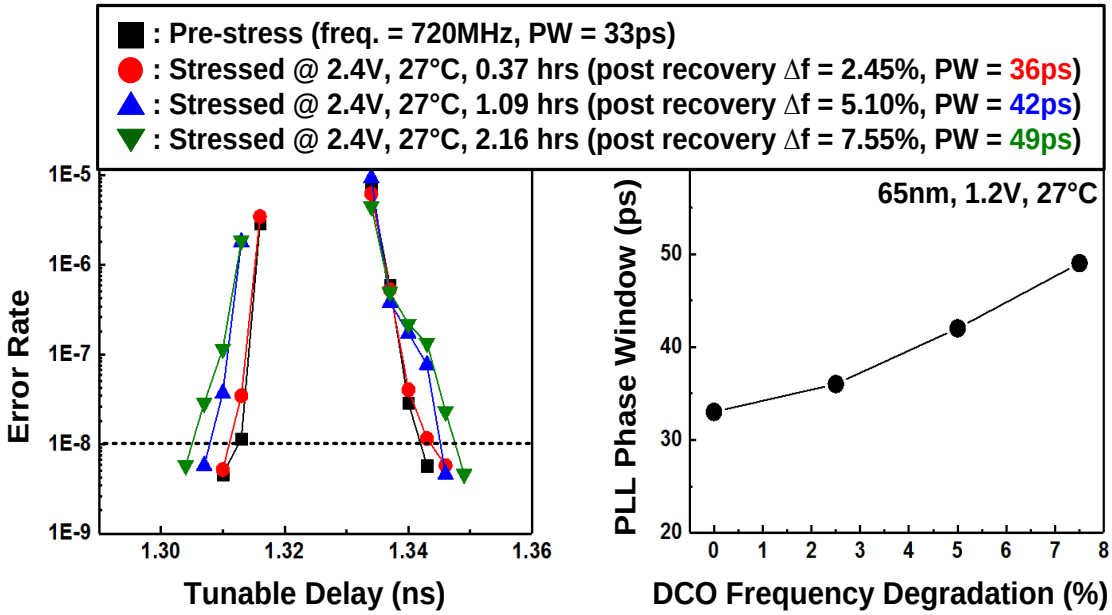


Fig. 2.17: Measured PLL phase window before and after stress.

Unlike the open-loop results, the error rate curves are all centered around the same output frequency, however, the phase noise window degrades with longer stress times. For instance, a 7.55% degradation in DCO frequency caused the phase window to increase by 16ps. Fig. 2.18 shows the phase window recovery of the closed-loop configuration after natural recovery and annealing at 244°C for 2 hours. The phase noise window is reduced from 49ps (before annealing) to 34ps (after annealing). The ADPLL test chip was fabricated in a 65nm CMOS process, and the die microphotograph is shown in Fig. 2.19.

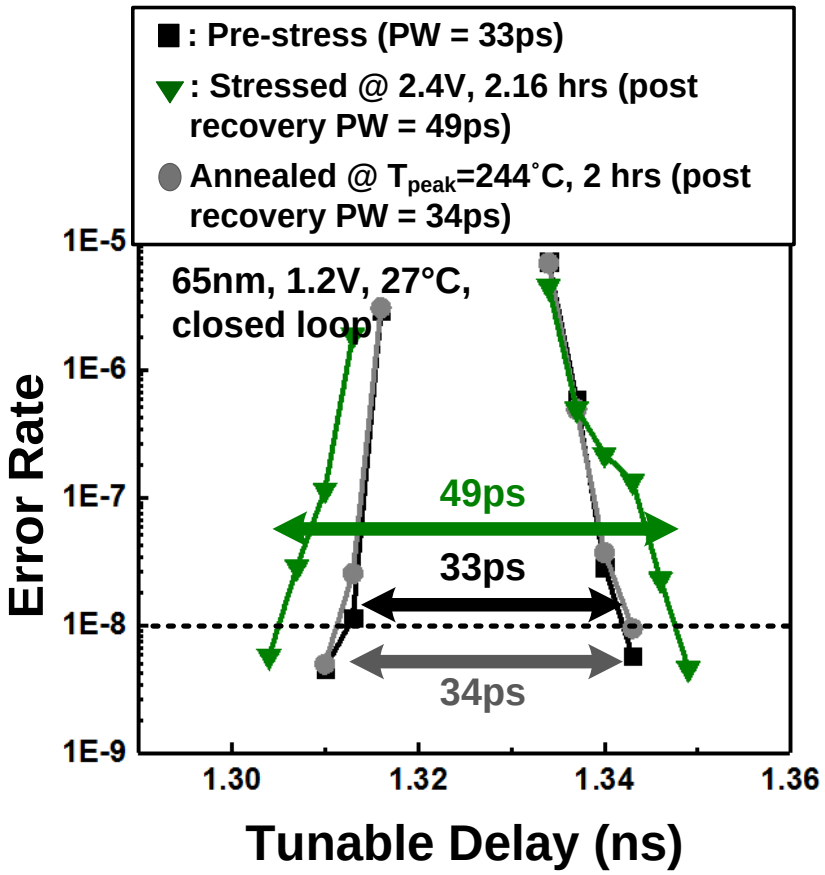
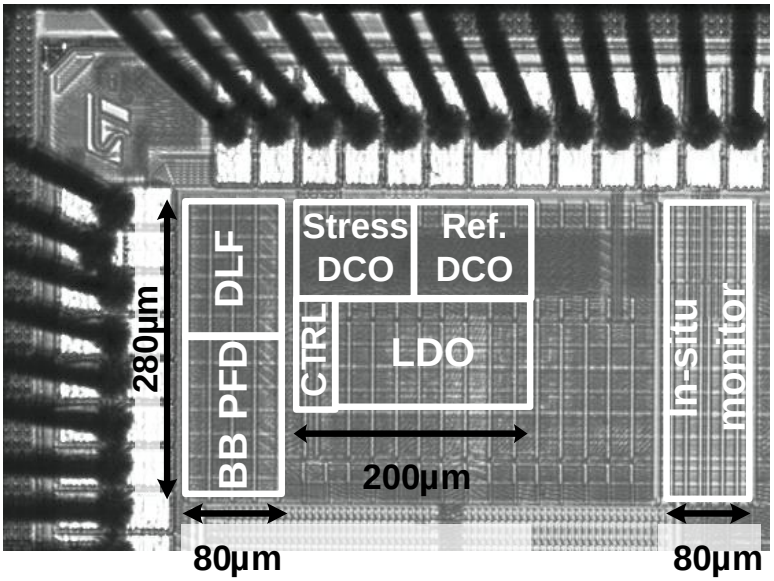


Fig. 2.18: Measured closed-loop phase window curves for pre-stress, stressed, and annealed DCOs.



Process	**65nm CMOS**
System	**All-Digital PLL**
Nominal supply	**1.2V**
Stress supply	**2.4V**
Annealing temp.	**110°C, 240°C**
DCO frequency (free running)	**720MHz @1.2V 1.54GHz @2.4V**
Circuit area	**0.08mm^2**

Fig. 2.19: 65nm all-digital PLL test chip die photo

2.4 Conclusion

Using simple on-chip monitoring circuits, we have experimentally shown that PLL phase noise degrades with aging even though the output frequency is maintained constant due to the PLL feedback operation. This has implications on ADPLL qualifications. Natural recovery alone was not enough to fully recover the phase noise due to permanent HCI and BTI damage. The proposed test structure was implemented in a 65nm CMOS process and tested under different annealing temperatures. In certain high-reliability applications where parts cannot be easily replaced and a long lifetime must be ensured (e.g. space electronics) [20] [21], annealing using an on-chip heat source may be a viable option.

Acknowledgement

This work was supported by in part by the Semiconductor Research Corporation (SRC) and the Texas Analog Center of Excellence (TxACE).

Chapter 3. ADC Reliability Study Using In-situ DNL/INL Measurement Circuits

3.1 Introduction

Characterizing analog-to-digital converters (ADCs) is a challenging task as their performance is sensitive to the noise in the measurement setup. There is a plethora of performance metrics that matter to ADC designers; differential non-linearity (DNL), integral non-linearity (INL), signal to noise and distortion ratio (SNDR), effective number of bits (ENOB), spurious free dynamic range (SFDR), and dynamic range (DR). Among these metrics, DNL and INL are the standard linearity parameters. For an ideal ADC, the output is divided into 2^N (N: ADC resolution) uniform steps each with the width Δ. Any deviation from the ideal step width is DNL. DNL errors accumulate to produce a total INL errors. The INL is defined as the maximum deviation from the ideal line. Also, it is measured from the center of the step (Fig. 3.1).

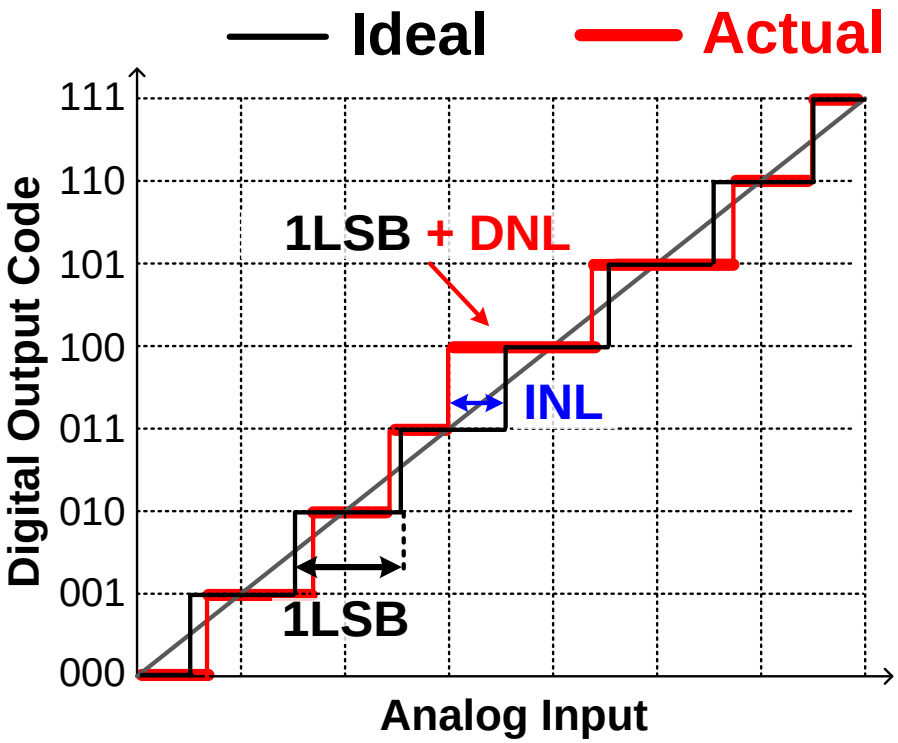


Fig. 3.1: Analog-to-Digital Converter (ADC) Non-linearity: DNL and INL.

For ADC non-linearity testing, the histogram method is widely used [22] – [24]. In this method, slow triangular/sinusoidal input voltage is applied to the ADC and ADC output codes can be obtained while the ADC performing. The frequency of the triangular signal should be low enough to avoid any settling time issues. In the ideal case, all ADC codes appear the same number of times.

In reality, however, some codes may have a higher (or lower) count than the ideal count due to non-linearity in the circuit and noise effects. Plotting the deviation of the actual count from the ideal count for each ADC code gives the DNL distribution (Fig. 3.2).

$$\mathrm{DNL}(n) = \frac{h(n)_{actual}}{h(n)_{ideal}} - 1 \tag{3.1}$$

M_T total samples for codes 1 to 2^N-2 (N: ADC resolution) are collected, and the count number of occurrences (hits) of each code is $h(n)_{Actual}$ where n is the number of the code. For the full-scale (FS) triangular input, the ideal (theoretical) number of hit is $h(n)_{Ideal} = M_T/(2^N\text{-}2)$. DNL of each code for n=1 to n=2^N-2 as written as (3.1). Integrating the DNL up to a certain code gives the INL distribution.

$$\mathrm{INL}(n) = \sum_{X=0}^{n} DNL_X \tag{3.2}$$

While measuring DNL or INL is not enough to fully characterize an ADC for high speed applications, they are highly relevant metrics for a wide range of ADCs.

Fig. 3.3 shows two conventional test setups for characterizing DNL and INL [25] – [28]. The setup in Fig. 3.3(a) simply retrieves the raw digital code from the ADC chip while applying a slow ramp voltage as the input. This setup does not require any special circuits; however, the high-speed digital interface can generate significant noise in the measurement setup. This is because the input-output (IO) signals are switching at a high frequency while the ADC is performing the sensitive analog to digital conversion. Consequently, this setup is not suitable for characterizing high resolution ADCs or studying subtle shifts in ADC performance. The test setup in Fig. 3.3 (b) addresses these concerns. Here, the raw ADC data is stored in an on-chip memory array and later transferred to the host computer. This setup separates the ADC operation from the data transfer operation, making the ADC characterization immune to measurement noise.

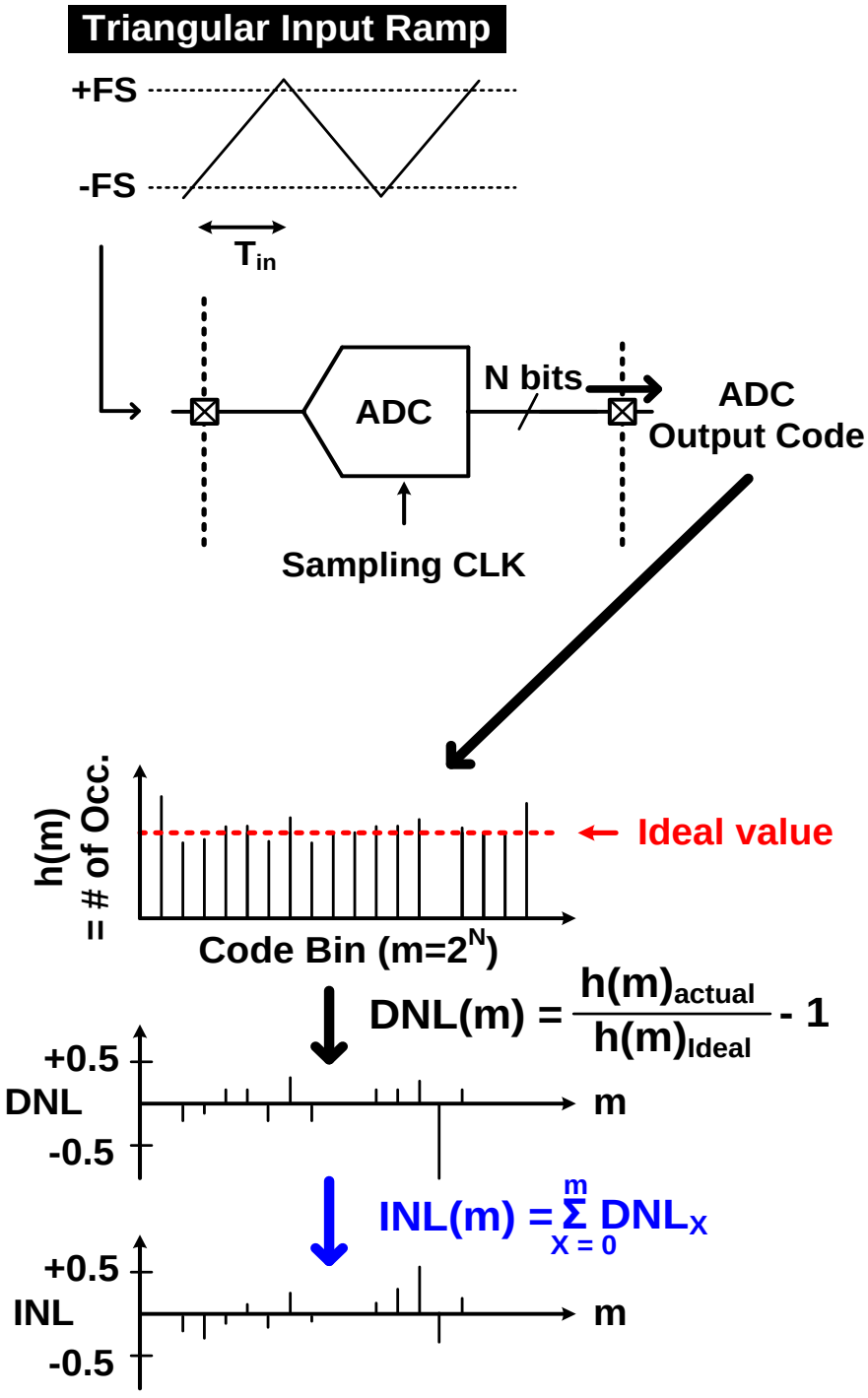


Fig. 3.2: Conventional ADC non-linearity testing: histogram method.

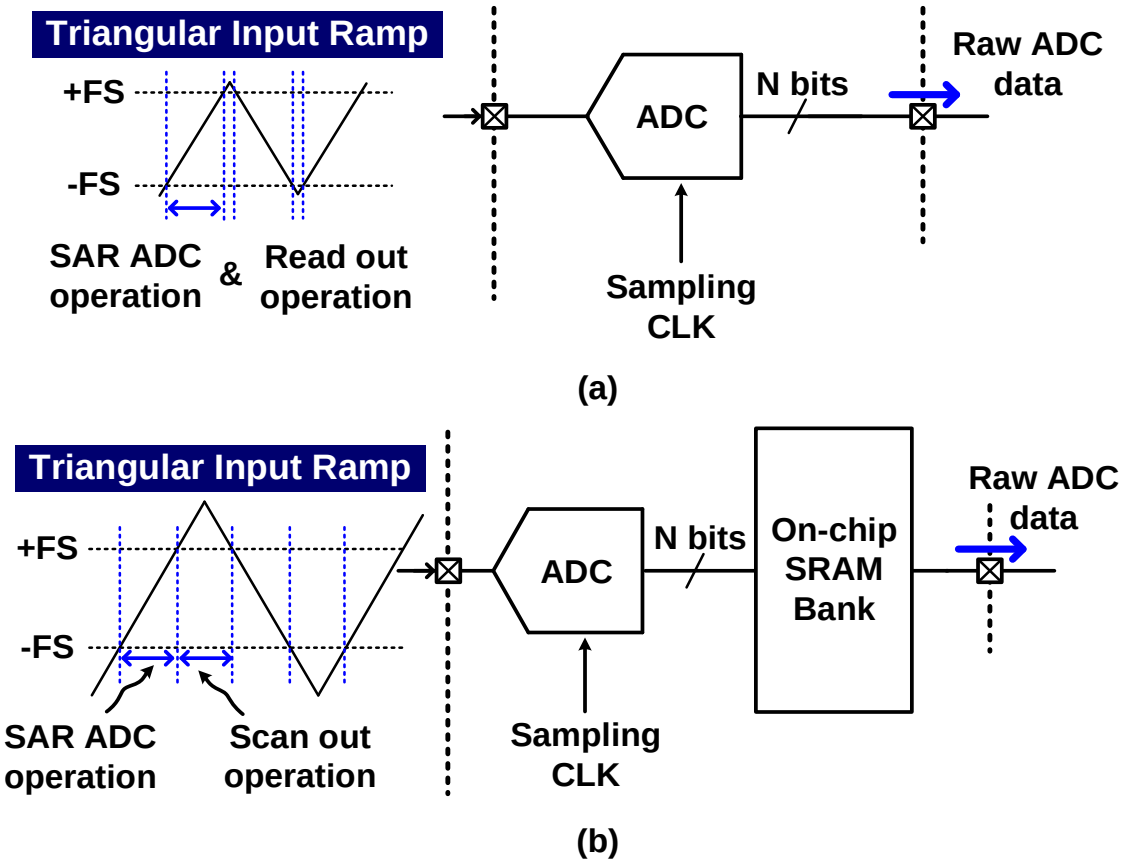


Fig. 3.3: Conventional DNL/INL characterization methods. (a) ADC samples are continuously retrieved by a test computer. Noise caused by the high speed IO signals can corrupt the conversion results. (b) ADC output is stored in an on-chip memory and transferred to the test computer later. ADC operation is not corrupted by IO switching noise.

The main drawback of this setup however is that it requires a significant amount of on-chip memory, as large as 1 megabits [25], to fully characterize an ADC. Furthermore, the amount of data that needs to be transferred to the host computer is very large. In this paper, we demonstrate a novel light-weight measurement circuit employing a bank of counters for precise DNL and INL characterization. The proposed method is immune to measurement noise as the ADC operation and data transfer operation are separated in time. Compared to the setup in Fig. 3.3(b), our design is simpler and more compact as only the

count values are stored on-chip. The test time overhead is negligible compared to prior art. Using the proposed approach, we successfully measured short-term reliability effects in a 10-bit successive approximation register (SAR) ADC, which would otherwise have been difficult using conventional test setups.

3.2 Proposed In-situ DNL/INL Measurement Circuit

Fig. 3.4(a) shows the proposed in-situ DNL/INL measurement circuit which consists of a decoder block and an array of counters. Each ADC output code is decoded, which enables the corresponding counter and increments its value. A 5-bit counter was chosen in our design considering the area overhead, ADC ramp time, and the target number of samples. For example, a larger counter would require a larger area, but allows a slower ramp signal and can collect more samples before having to transfer the counter values to the host computer. To prevent the counter from overflowing, the ramp signal should have a period shorter than 2^N * *max count* * *sampling period*. Here, N is the ADC resolution. Storing counts rather than raw ADC codes, reduces the amount of data that needs to be transferred off-chip. This allows the data transfer to occur briefly between the signal ramp up and ramp down. Since the ADC operation and the data transfer operation are separated in time, the ADC can be tested in an extremely low noise environment.

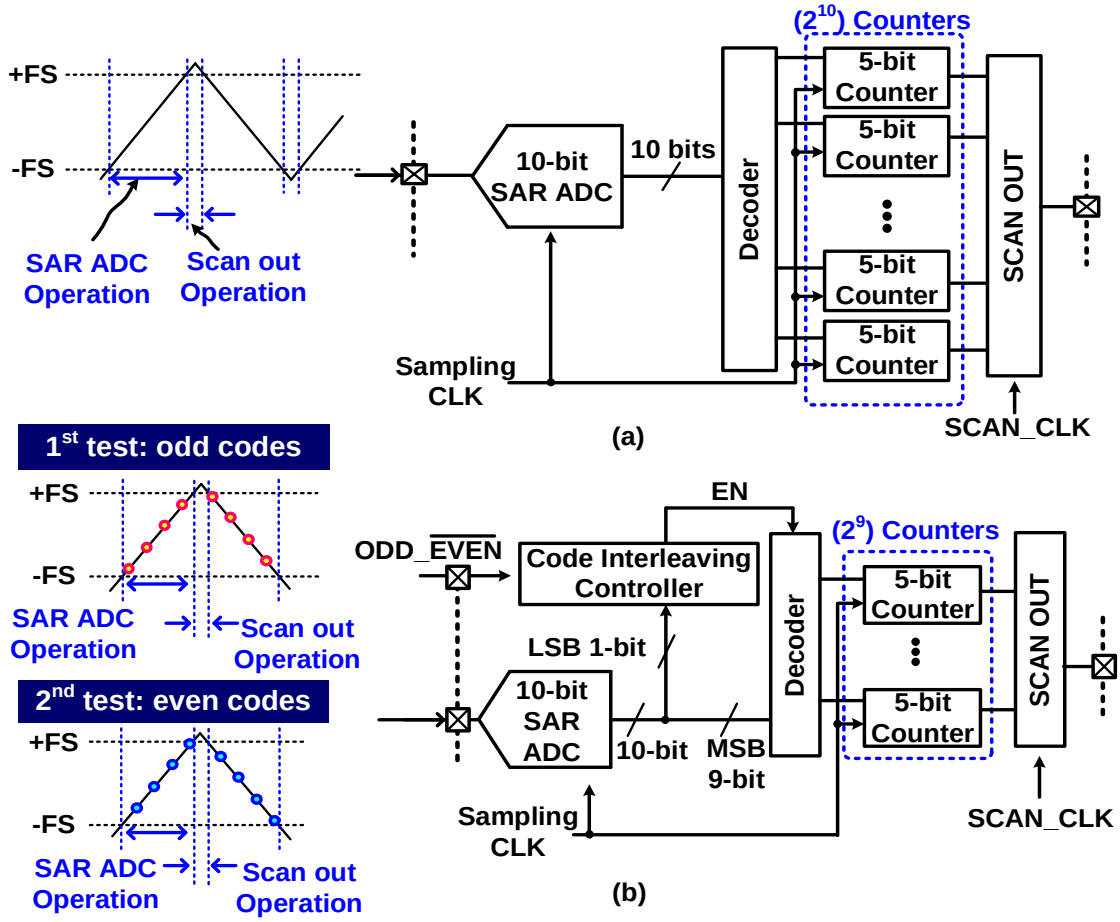


Fig. 3.4: Block diagram of the proposed DNL/INL measurement circuit; (a) standard design; (b) interleaved design with reduced number of counters. Here, odd and even codes measured from two separate tests must be combined together.

One drawback of the implementation in Fig. 3.4(a) is the large number of counters needed to measure the full histogram. That is, for an N-bit ADC, we need 2^N counters. This results in a significant area overhead for the test circuit. To make the circuit area more tractable, we opted for the 2-way interleaved design in Fig. 3.4(b) where only half the number of counters are implemented. To measure the full DNL and INL histograms with half the number of counters, we have to measure the odd and even codes in two separate tests and combine the results later. As shown in Fig. 3.4(b), the decoder is enabled only

when the LSB of the ADC code matches the ODD_EVEN control bit. Using the 2-way interleaved design, we can reduce the circuit area by 50% at the expense of two ramp tests. 4-way or 8-way interleaved designs can be considered for testing ADCs with higher number of bits.

3.3 Test Chip Structure and Circuit Design

The test chip is composed of a10-bit successive-approximate-register (SAR) ADC, the code interleaving logic, a decoder, an internal clock generator circuit, and the in-situ INL/DNL measurement block. The SAR ADC block consists of comparators, capacitor digital-to-analog converters (CDAC), a SAR logic, and MUX/DeMUX. We employ two comparators to measure BTI effect in two types of an input pair (i.e. NMOS, and PMOS pairs).

3.3.1 Split SAR-ADC using Bridge Capacitor

In this work, different noise tendencies should be avoided depending on the ADC clock frequency, because the characterization of ADC reliability under different frequency conditions is one of the purpose of this work. In other words, there should be no setting time issue in the input capacitor even at high frequency. Therefore, small input capacitor is required. Area of binary-weighted capacitor digital-to-analog converter (CDAC) increase exponentially with the increase of the bit resolution. Split capacitor arrays have been proposed as solutions to reduce input capacitance (i.e. CDAC capacitance) and area.

The capacitor array is split by two (i.e. MSB- and LSB-side) and a bridge capacitor is implemented to connect the two split capacitor arrays. There are several types of split capacitor DAC based on bridge capacitor size: (i) unit (1C) bridge capacitor [29] [30], (ii) fractional bridge capacitor [31] [32], and (iii) two times of unit (2C) bridge capacitor [33] [34]. The unit bridge capacitor based CDAC generate 1LSB gain error, and the fractional bridge capacitor causes poor matching with the other capacitors. Both problems degrade DAC linearity and thus the overall ADC linearity performance. So, we choose 2C bridge capacitor based CDAC to achieve both capacitor area reduction and good linearity as shown in Fig. 3.5.

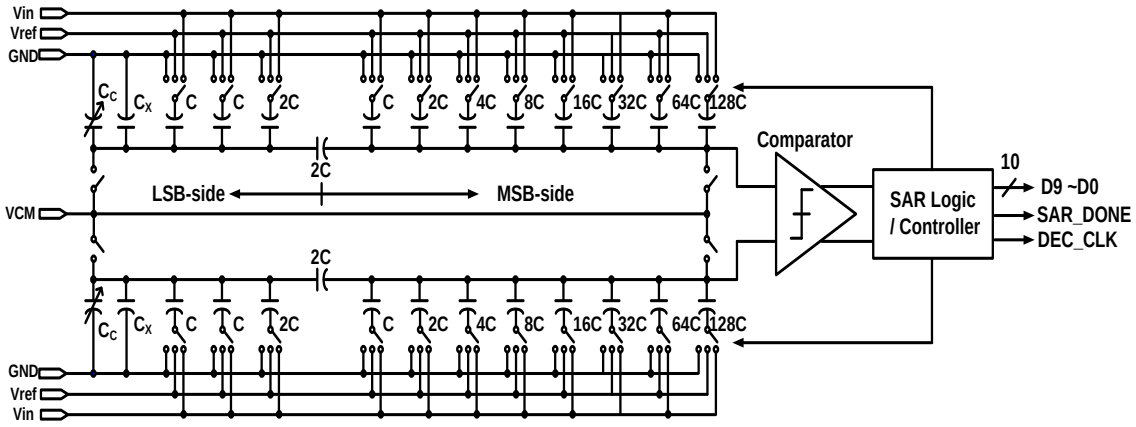


Fig. 3.5: 10-bit split SAR ADC using 2C bridge capacitor.

3.3.2 Comparator Design

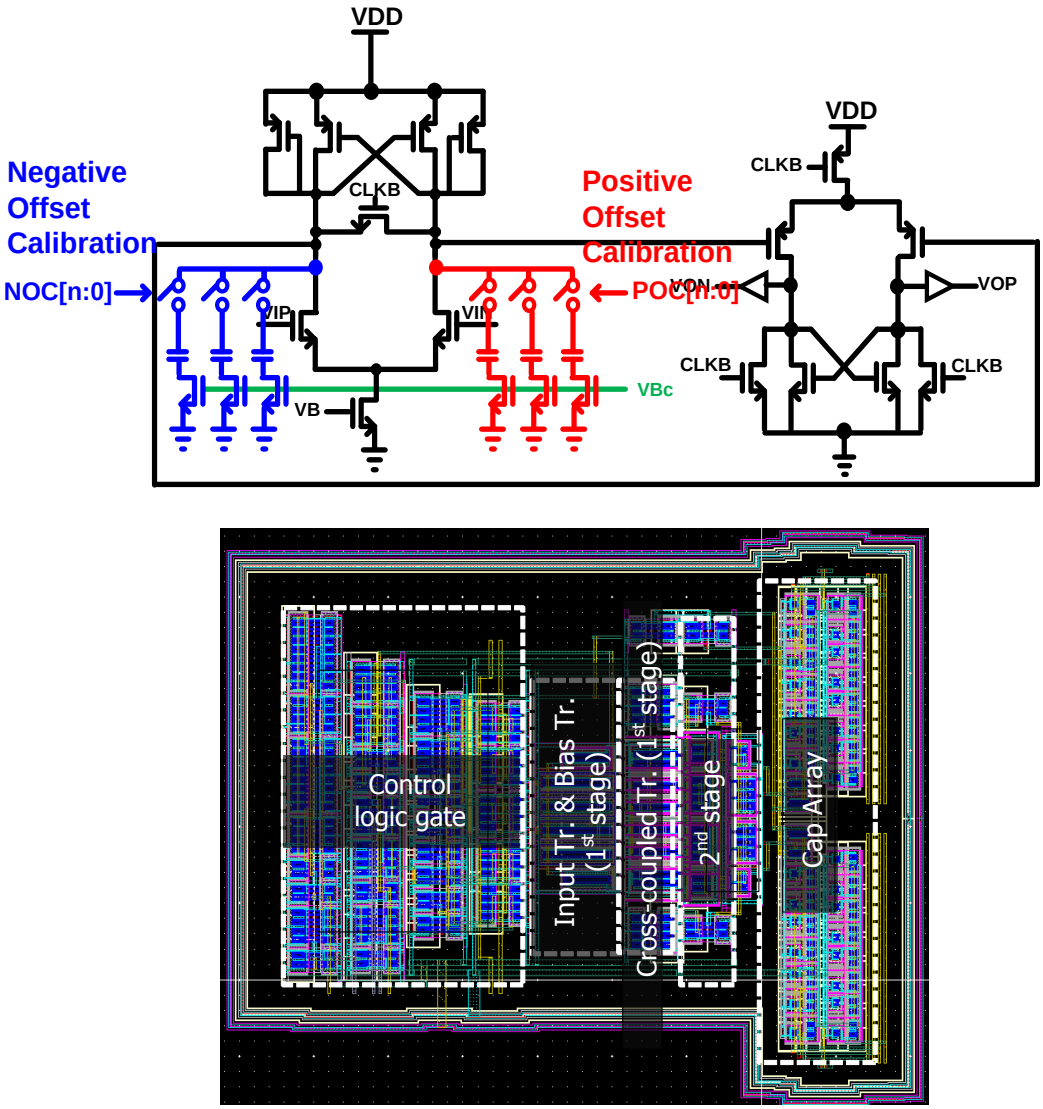


Fig. 3.6: Schematic and layout of a comparator

Fig. 3.6 shows the schematic and layout of a comparator with a NMOS input pair. Interdigitated layout and a guard ring are done for transistors in 1st stage to reduce mismatch. Also, bias lines is shielded with power and GND lines to make stable analog bias voltage against internal noise. Also, we employ trimming load capacitors for both

negative and positive offset compensation. By changing load capacitors of capacitor banks, a comparator transition point can be adjusted, which compensates a wrong transition point caused by comparator offset voltage. To make a symmetric layout, we connect an identical capacitor bank in the differential output nodes of 1st stage. Capacitors are digitally controlled for a coarse calibration, and trimming bias voltages (i.e. Vcn, and Vcp) are applied for a fine calibration.

3.3.3 Counter Based In-situ DNL/INL measurement Circuit

A total of 512 5-bit counters were laid out as shown in Fig. 3.7. The 10-bit code from the ADC, less the 1 LSB for even/odd code selection, is decoded by the column and row decoders. That is, a 4-bit column decoder and a 5-bit row decoder selects and increments the 5-bit counter corresponding to ADC code D<9:1>. The 5-bit counters can store count values up to 32, which are read out between signal ramps.

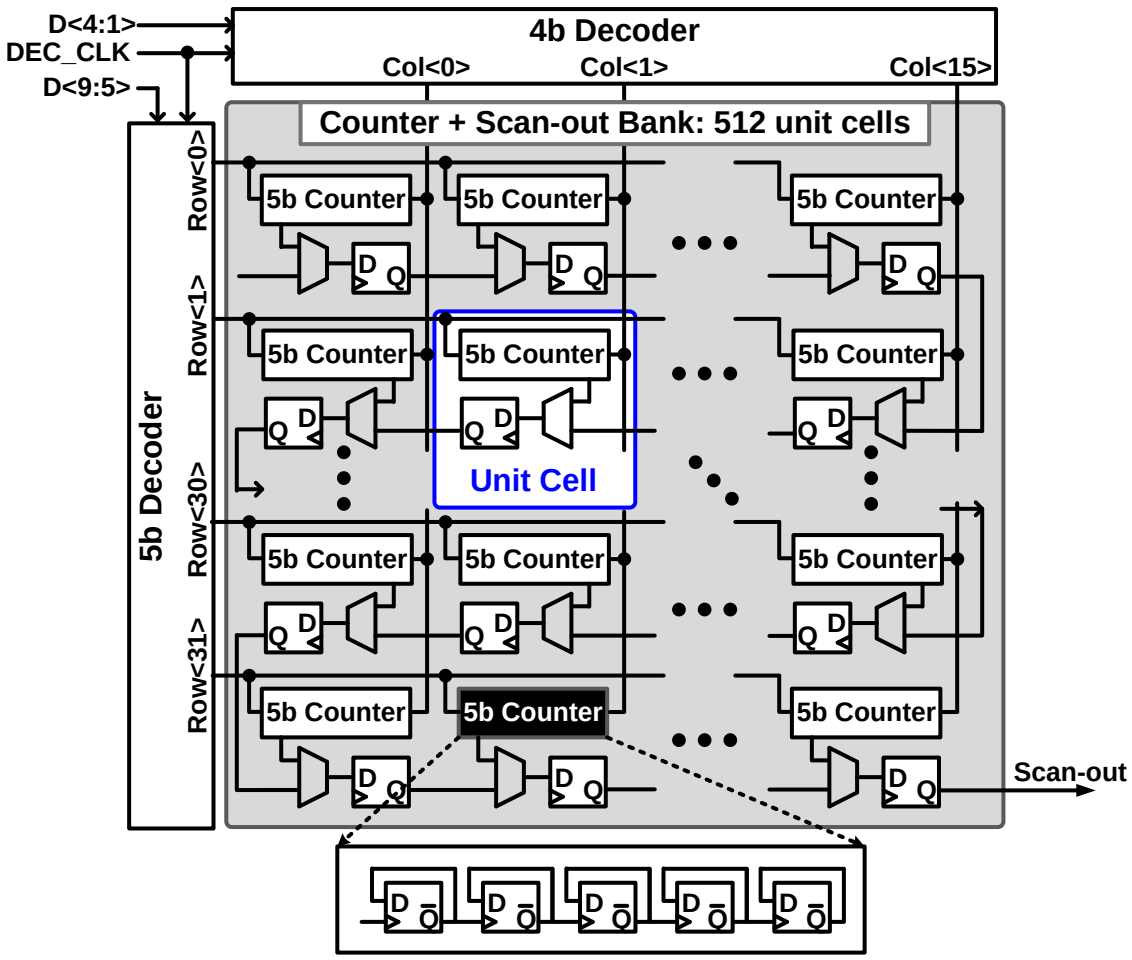


Fig. 3.7: Block diagram of the proposed DNL/INL measurement circuit; (a) standard design; (b) interleaved design with reduced number of counters. Here, odd and even codes measured from two separate tests must be combined together.

3.3.4 Counter Based Offset Cancellation

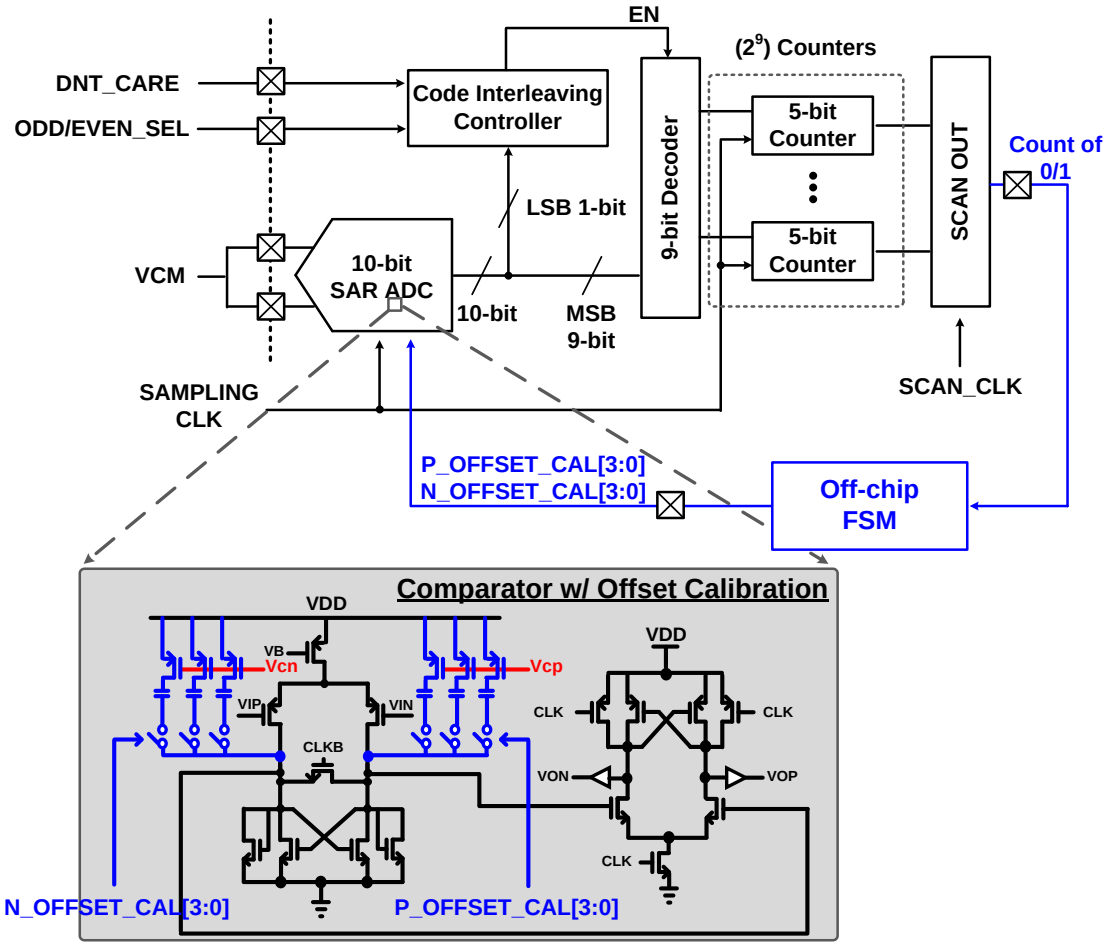
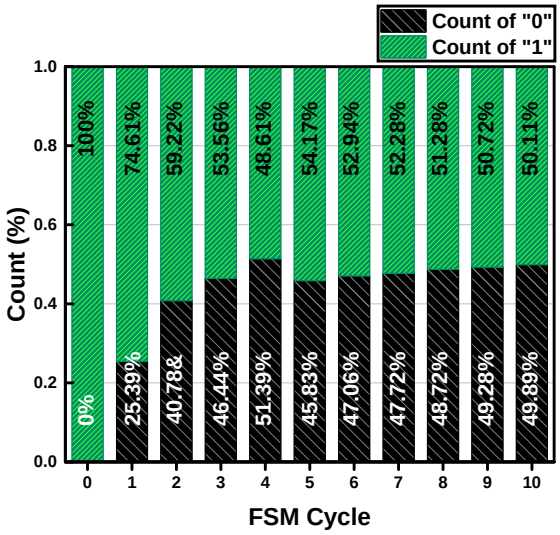


Fig. 3.8: Block diagram of counter based offset calibration using off-chip FSM.

Fig. 3.8 shows the block diagram of counter based offset calibration using off-chip FSM. In offset calibration phase, DNT_CARE=1 is applied and then EN signal of the code interleaving logic is always 1. So, all of 9b ADC outputs are decoded by the 9b decoder regardless of LSB of ADC outputs.



FSM Cycle	N_OFFSET _CAL[3:0]	P_OFFSET _CAL[3:0]	Vcn [V]	Vcp [V]
0	0000	0000	0.6	0.6
1	0000	1000	0.6	0.6
2	0000	1100	0.6	0.6
3	0000	1110	0.6	0.6
4	0000	1111	0.6	0.6
5	0001	1111	0.6	0.6
6	0001	1111	0.601	0.6
7	0001	1111	0.602	0.6
8	0001	1111	0.603	0.6
9	0001	1111	0.604	0.6
10	0001	1111	0.605	0.6

Fig. 3.9: Measurement results of counter based offset calibration.

Also, the differential input is tied to a same voltage (e.g. VCM=VDD/2), and the ADC is performing normally. In this condition, the number of 0 and 1 of the ADC output is a function of input offset of the comparator. For example, if an input offset is 0V, the probability (P_B) that output 0 and 1 can be generated is 50% due to randomness of input noise. Otherwise, P_B of output 0 and 1 would be different: (i) input offset > 0V → P_B (output=1) > P_B (output=0); and (ii) input offset < 0V → P_B (output=1) < P_B (output=0). Using the counter block, a histogram of output 0 and 1 can be obtain and thus P_B can be calculated. Once P_B reaches to 50%, the offset calibration is completed. Digital codes (i.e. N_OFFSET_CAL[3:0], and P_OFFSET_CAL[3:0]) are used for a coarse calibration, and trimming biases (i.e. Vcn, and Vcp) are for fine calibration. Automation test using off-chip finite state machine (FSM) is adopt to find optimal trimming condition. Fig. 3.9 shows the measurement results of the offset calibration.

3.4 Test Setup and Measured DNL/INL Data

3.4.1 Test Board Design and Test Setup

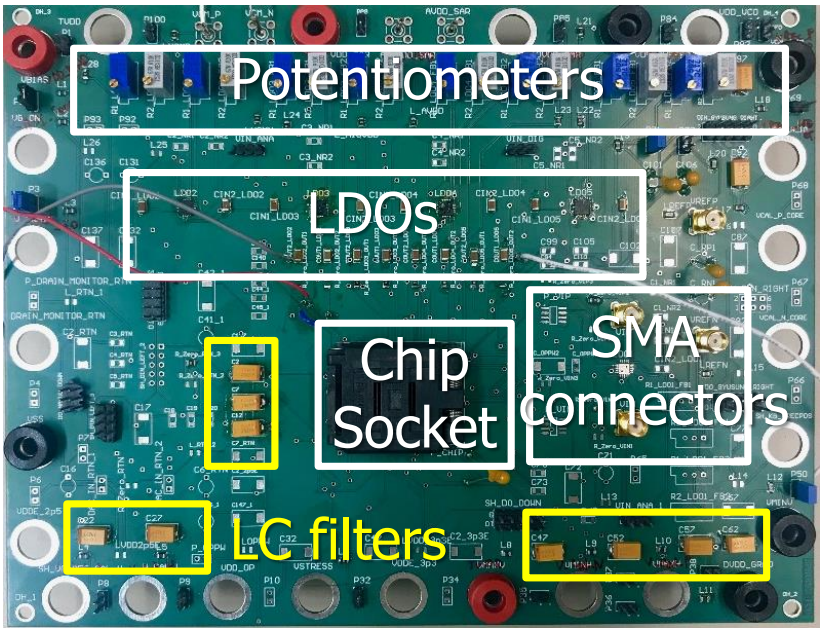


Fig. 3.10: Test PCB design.

The mixed-signal nature of our SAR ADC design contains both analog and digital circuit components. Combining both analog and digital components onto a system can cause noise issues. To reduce noise, the digital and analog power supplies are separated for the isolation between the noisy digital power fluctuation and the relatively quiet analog power. Additionally, digital power pins and digital circuits are placed as far from the analog power pins and circuit block inside the chip package. Fig. 3.10 shows our dedicated PCB. On the PCB, off-chip LC filters are placed between the power and ground nodes. To further reduce the power supply noise, several LDOs are used for analog power and reference

voltages (i.e. V_{REF+}, V_{REF-}, and VCM). Also, since purity of ADC input voltage is insignificant for accurate ADC measurement, SMA connecters are used to reduce noise issues at input signals.

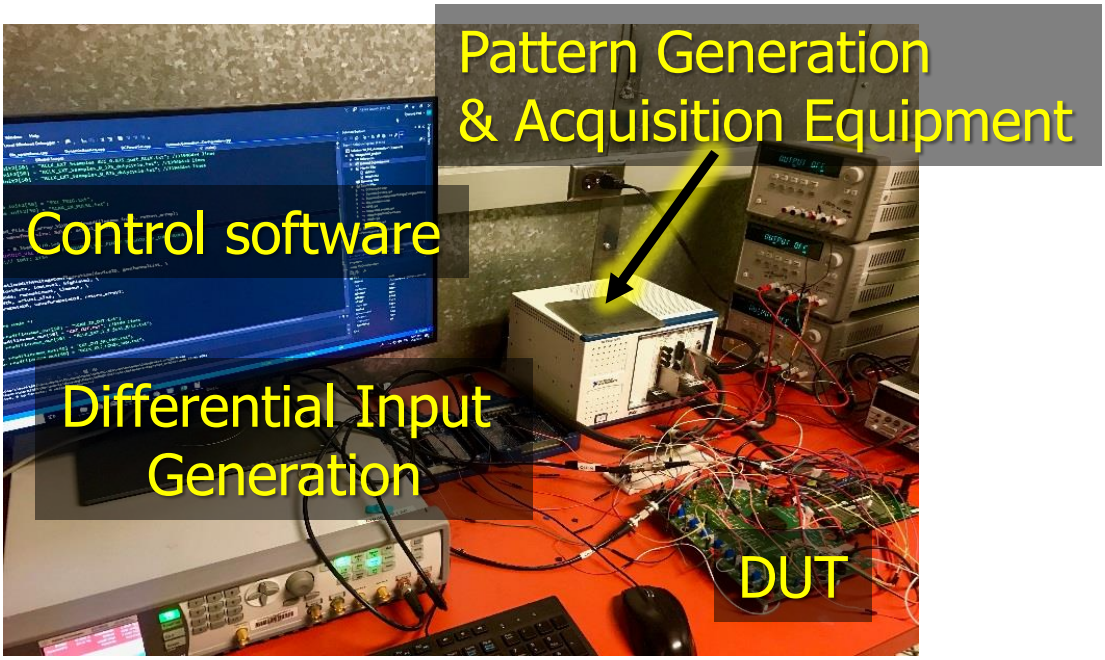


Fig. 3.11: ADC Test setup.

National Instrument (NI) PXIe-1073 is used for data/clock pattern generation and acquisition. C/C++ code based software controls the NI PXIe-1073, and DAQ board is used for bias voltage generation.as shown in Fig. 3.11. Also, the ADC input signals are generated by the function generator with 2 output channels (Agilent Technologies 81160A).

3.4.2 Measurement Data from 65nm Test Chip

A 10-bit SAR-ADC employing the proposed counter based measurement circuit was fabricated in a 65nm CMOS technology. Fig. 3.12 shows measured 10-bit DNL/INL at VDD=1.2V, IOVDD= 2.0V, input range=0.8V, and 1MHz ADC clock. DNL_{MAX} is -0.34/-0.88LSB and INL_{MAX} is +1.67/-1.41LSB. Fig. 3.13 shows the measured DNL histogram for the proposed in-situ method and the conventional method in Fig. 3.3(a). Results are shown for three different clock frequencies; i.e. 0.1MHz, 1.0MHz, and 10MHz. For the experiment, we used a core VDD of 1.2V, an IO VDD of 2.0V (which is slightly lower than the nominal level to further reduce IO switching noise), and an input ramp range of 0.8V. As the frequency increases, DNL measured using the traditional method gets progressively worse while the DNL measured using the in-situ method is not affected. The DNL for the in-situ method ranges from -0.88LSB to +0.34LSB while for the conventional method, it ranges from -1.00LSB to +2.11LSB. The higher immunity to noise means that ADC performance can be measured precisely without an elaborate board design or test setup.

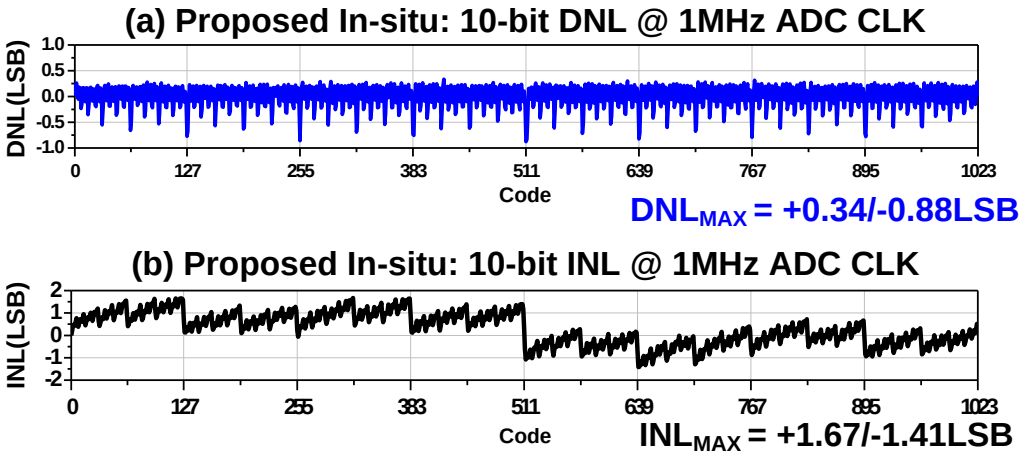


Fig. 3.12: Measured 10-bit DNL/INL using the in-situ measurement circuits.

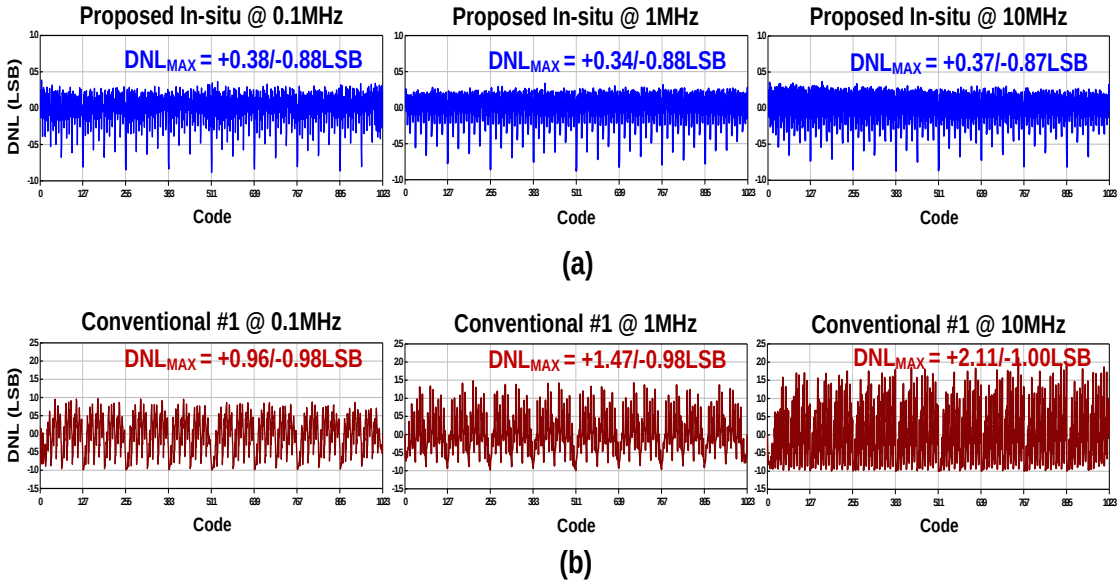


Fig. 3.13: DNL comparison between the proposed method and the conventional method in Fig. 3.1(a) for 0.1MHz, 1.0MHz, and 10MHz clock frequencies.

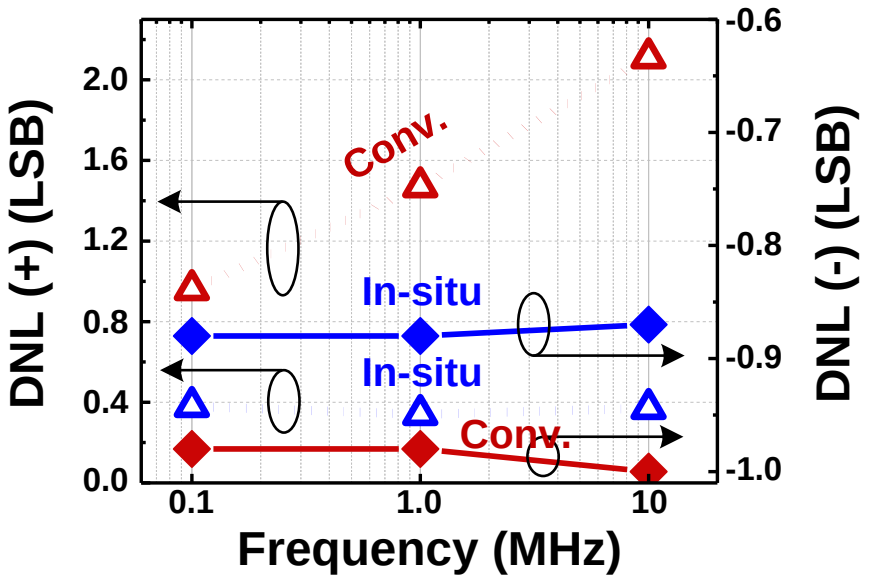


Fig. 3.14: DNL vs. clock frequencies.

Fig. 3.15 (left) compares the read out data volume of our in-situ method and the conventional method. For an N-bit ADC, the data volume of the two methods can be expressed as $2^N \cdot log_2$ *(# of samples/code)* and $2^N \cdot N \cdot$ *(# of samples/code)*, respectively. Our design employing a 5-bit counter reduces the data volume by 64 times. Fig. 3.15 (right) shows the transistor count comparison (array part only) between the proposed method and conventional SRAM array. An asynchronous counter based on a chain of D-flip-flop (DFF) circuits was used in our chip. Each DFF has a transistor count of 32. A single SRAM cell has a transistor count of 6. Based on these assumptions, we achieved a 12x reduction in transistor count.

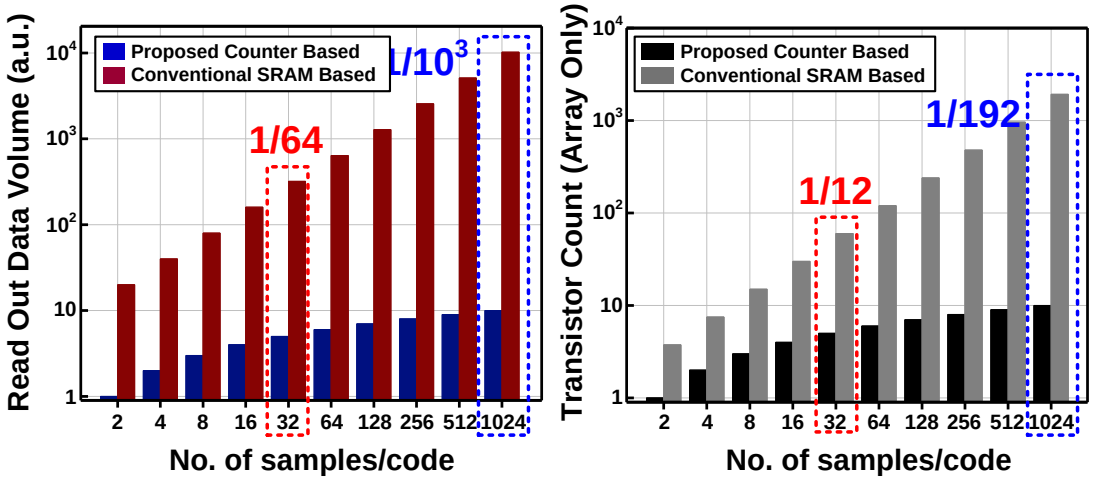


Fig. 3.15: Comparison between the proposed method and conventional SRAM based test method. (a) Read out data volume; (b) Transistor count (array part only).

3.5 Application to ADC Reliability Studies

3.5.1 Codes Vulnerable to Short-term BTI Effects

Bias temperature instability (BTI) has become a critical reliability concern in advanced technologies [35] [36]. BTI degradation occurs when carriers get trapped in the interface or the gate dielectric while the device is in a strong inversion mode. This causes the threshold voltage (Vth) to increase. The magnitude of the Vth shift is a function of temperature, voltage, and stress time. When the stress voltage is removed, the device immediately enters a "recovery" phase. BTI degradation and recovery can occur even at microsecond time scales affecting noise-sensitive circuits such as comparators [37] [38]. For instance, when two input transistors of a comparator circuit are exposed to two very different input voltages, asymmetric short-term BTI aging can lead to a time-dependent offset voltage as illustrated in Fig. 3.16. More specifically, a large asymmetric voltage

stress in the input transistors in early conversion steps can induce an error in the later steps where a small voltage difference must be resolved by the comparator. For example (Fig, 3.17), an incorrect conversion in the second SAR conversion step (i.e. D8 step) can be occurred when the input voltage difference in D8 step is smaller than Vth shift difference in D9 step which caused by the large input voltage difference applied during the preceding D9 step. An incorrect decision can be occurred during any SAR conversion steps, from D8 to D0. However, the probability of an error is higher for the earlier steps since the input subject to a large voltage difference at the steps and Vth shift is recovered in the latter steps. This issue can be detrimental to the performance of SAR-ADCs even for a fresh chip [39].

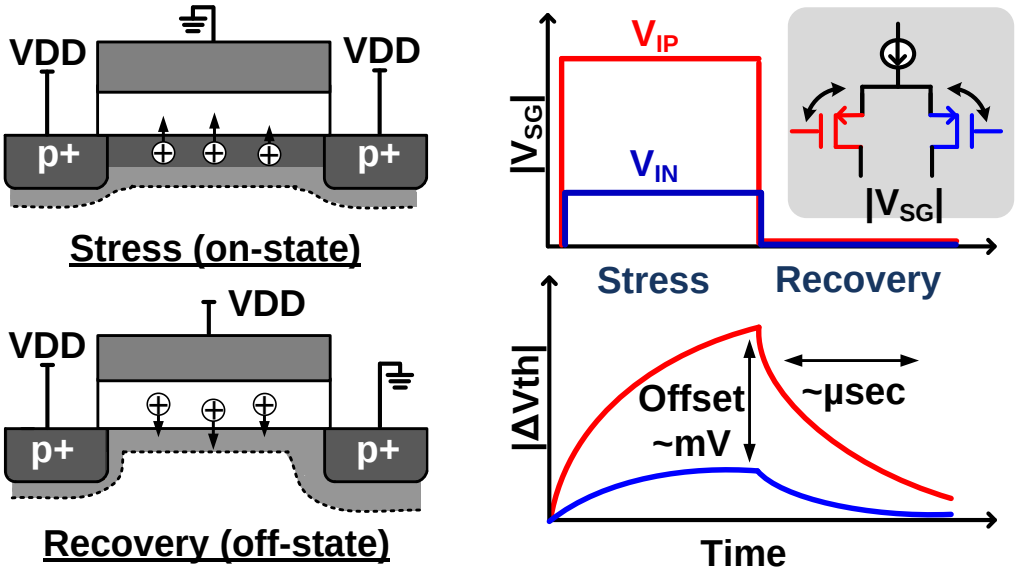


Fig. 3.16: (Left) Vth degradation and recovery due to short-term BTI effects. (Right) Input offset voltage of comparator circuit can vary dynamically when the difference between the two input voltages VIP and VIN is large.

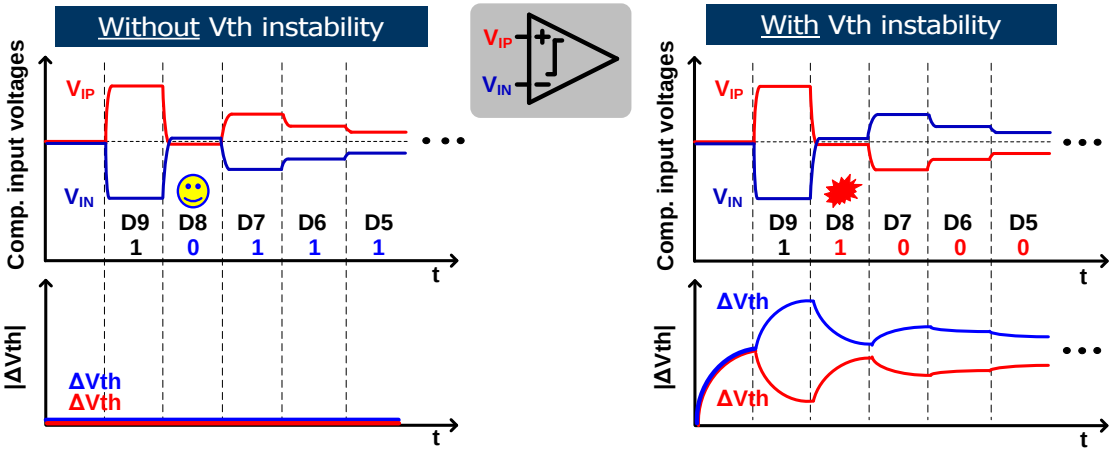


Fig. 3.17: Impact on SAR-ADC operation

Prior work has shown that certain codes are more vulnerable to short-term instability effects (Fig. 3.18). One of the vulnerable codes is D = 76710 which ends with a binary pattern of 0111… In the absence of short-term instability, the correct output code is produced. However, when short-term instability is present, an incorrect code of D = 76810 can be generated. Notice the pattern of the incorrect code which ends with 1000… The error in this example is caused in the third conversion step. Other vulnerable codes listed in Fig. 3.18 have similar patterns; i.e. 0 followed by 1's or 1 followed by 0's.

In this work, we characterized short-term BTI effects in a 10-bit SAR-ADC by measuring the DNL of vulnerable codes using the proposed in-situ measurement circuit. It's important to note that the typical value of voltage offset caused by short-term BTI can be less than a millivolt which is difficult to measure using conventional methods.

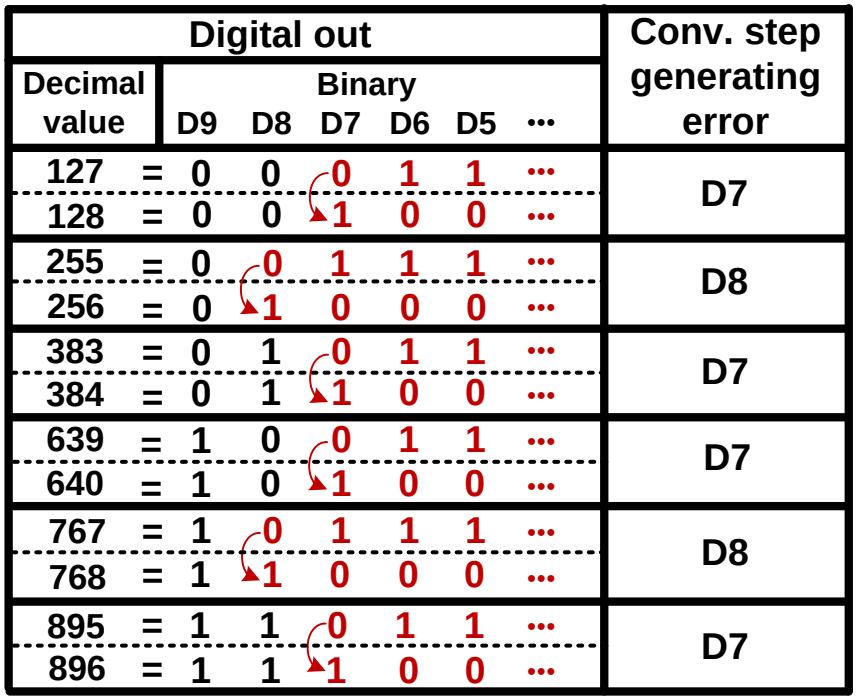


Fig. 3.18: Illustration of codes that are most vulnerable to short term BTI effects in a 10 bit SAR-ADC. Codes ending with a pattern of 0111… can get misinterpreted as the neighboring code which ends with a pattern of 1000….

3.5.2 Test Methodology

To study the detailed behavior of short-term instability, we varied the ratio between the stress and recovery times by switching on and off the header PMOS device of the comparator as shown in Fig. 3.19. The comparator includes a pre-amp stage to reduce kickback noise and input-referred noise. IO devices were used to implement the comparator circuit to suppress gate leakage and sub-threshold leakage. Both PMOS input and NMOS input comparators have been implemented and tested. A multi-phase voltage controlled oscillator (VCO) and a phase selection MUX were used to generate the variable duty cycle clock. For the PMOS input comparator shown in Fig. 3.19, switching off the header causes

the common source node of the input PMOS transistors to collapse, forcing the two input devices into a recovery state. |Vsg| of the two input transistors equalize and consequently, the asymmetric Vth degradation is recovered prior to the next conversion step. A shorter duty cycle clock can reduce the BTI induced Vth shift further by virtue of a short stress time and a long recovery time. We also characterize the impact of clock frequency on short-term BTI effect in a SAR-ADC.

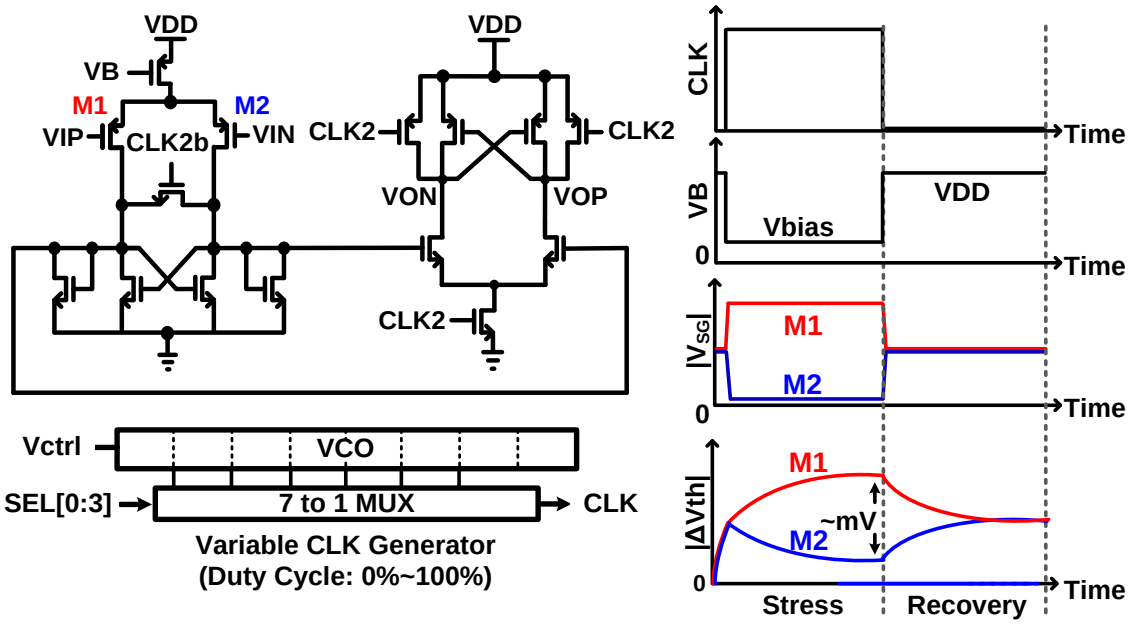


Fig. 3.19: Variable duty cycle clock generator and clocked bias current for studying fast BTI degradation and recovery effects in comparator circuits. PMOS input comparator is shown in this figure.

3.5.3 Measured Results and Analysis

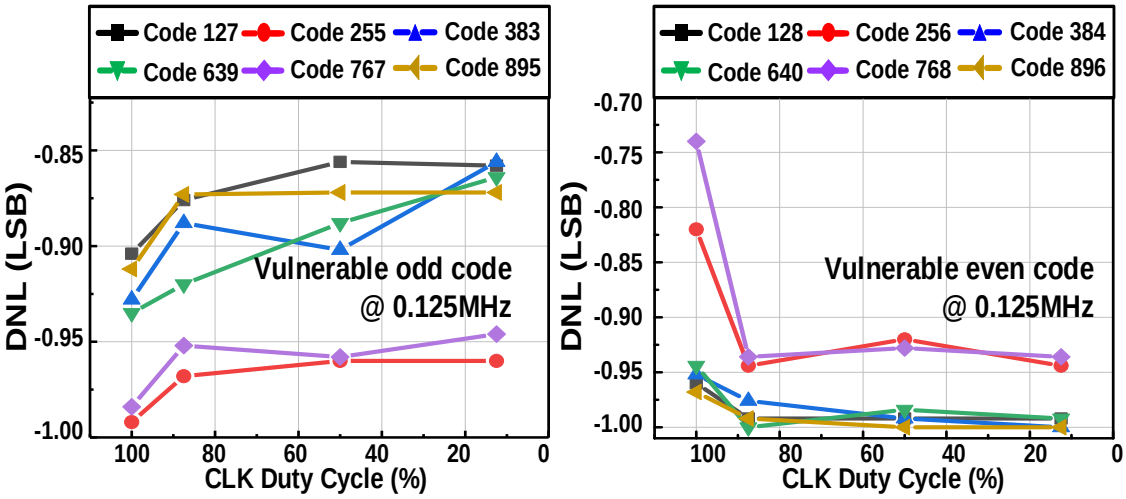


Fig. 3.20: DNL measured under different duty cycles for the most vulnerable codes; (left) codes ending with 0111…; (right) codes ending with 1000…. Results shown are for comparators with IO PMOS input transistors.

Fig. 3.20 shows the DNL of the vulnerable odd codes (i.e. D = 127, 255, 383, 639, 767, 895) and vulnerable even codes (i.e. D = 128, 256, 384, 640, 768, 896) for different duty cycles. A relatively slow clock frequency of 0.125MHz was used in this test to cause more BTI degradation. Results show that for shorter duty cycles, DNL tends to increase for the odd codes and decrease for the even codes. In other words, the number of occurrences of vulnerable odd codes increases while that of vulnerable even codes decreases. This trend suggests that some of the incorrect codes are rectified by the longer recovery time. We also measured the DNL versus duty cycle for different clock frequencies; 0.125MHz, 0.5MHz, and 2MHz. As shown in Fig. 3.21, the DNL trend lines are generally flat. That is, short-term instability is less obvious at higher frequencies due to the shorter stress time. Fig. 3.22 shows DNL results for an NMOS input comparator. We

found no apparent shift in the DNL value indicating that short-term instability is less pronounced for NMOS devices in this technology. So one remedy to short-term instability issues in this technology is to use comparators with NMOS input devices. Fig. 3.23 shows the 65nm test chip die photo and the chip feature summary.

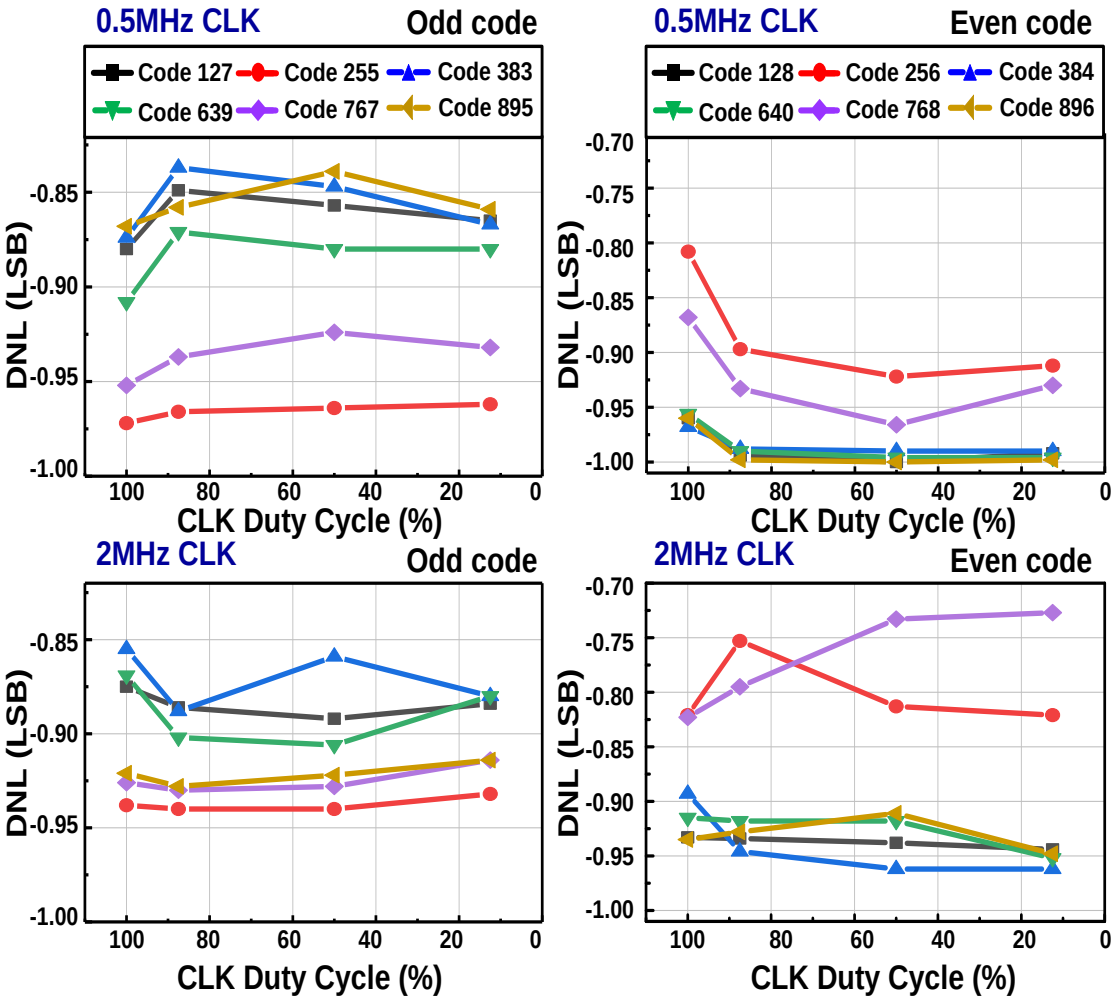


Fig. 3.21: DNL measured at 0.5MHz and 2MHz clock frequencies for the most vulnerable odd and even codes.

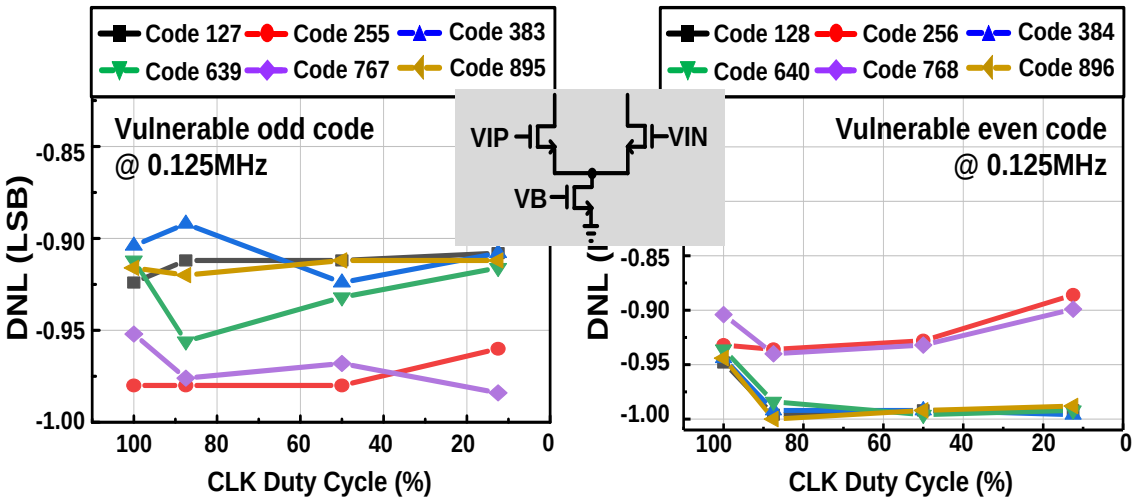
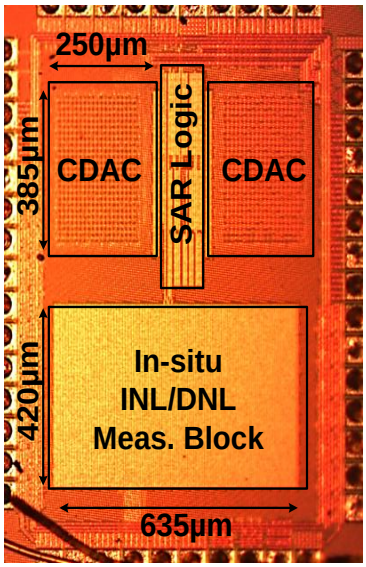


Fig. 3.22: Measured DNL for SAR-ADC with IO NMOS input comparators suggesting negligible short term instability effects.



Process		65nm GP CMOS
Core / IO supply		1.2V / 2.5V
ADC resolution		10-bit
DNL (max)	vs Con. (w/o SRAM)	0.88 LSB (1.23 LSB improv.)
Read Out Data Volume	vs Con.	1/64 (for 32 samples/code)
Tr. count of on-chip measurement block		94,208 (Counters only)
DNL		+0.34 / -0.88 LSB @ 1MHz
INL		+1.67 / -1.41 LSB @ 1MHz
Total chip area		0.57mm^2

Fig. 3.23: 65nm die photo and chip feature summary.

3.6 Conclusion

In this paper, we present a counter based measurement circuit for in-situ characterization of ADC DNL and INL. An array of counters collects the histogram of the ADC output code for a triangular input voltage. Since the ADC operation and data transfer operation are separated in time, the DNL and INL results are immune to noise in the measurement setup. Using the proposed characterization method, we studied short-term BTI effects in a 10-bit SAR ADC under different operating conditions. Precise characterization of ADC DNL and INL was demonstrated. Results confirm that subtle DNL shifts can be accurately measured using the proposed method.

Acknowledgement

The authors would like to thank Dr. Vijay Reddy and Dr. Srikanth Krishnan at Texas Instruments, and Dr. Wonho Choi for their technical feedback. This work was supported in part by the Semiconductor Research Corporation and the Texas Analog Center of Excellence (TxACE).

Chapter 4. All BTI Odometer based on a Dual Power Rail Ring Oscillator Array

4.1 Introduction

Parametric shifts caused by negative and positive bias temperature instabilities (NBTI and PBTI) have become a growing concern in advanced CMOS technologies. Without the necessary timing or voltage guardbands, these reliability mechanisms can cause premature circuit failures. Fig. 4.1 shows the bias condition of the four different BTI modes. When a device is biased in strong inversion mode, PMOS and NMOS devices undergo NBTI and PBTI stresses, respectively, whereas in accumulation mode, the devices experience PBTI and NBTI, respectively (Fig. 4.2). Previous works have shown that the device current decreases for all four BTI modes [40] - [44]. PMOS NBTI and NMOS PBTI have been extensively studied as they affect the performance of digital logic or memory circuits during normal operation [45]-[48]. In contrast, very few papers have shown the impact of PMOS PBTI and NMOS NBTI on circuit operation since these mechanisms mainly occur under specific operating scenarios in mixed-signal circuits [49] [50]. Fig. 4.3 shows one such scenario where the power supply of a differential amplifier circuit is shut down while the circuits generating the two inputs signals are active. This situation creates a bias condition where the PMOS gate voltage is driven to VDD while the source and drain voltages are discharged to ground [51]. This corresponds to the PMOS PBTI stress

condition illustrated in Fig. 4.1 which results in an increased threshold voltage (absolute value) thereby degrading the performance of the differential amplifier circuit. Despite the importance of this stress mode for mixed-signal applications, no circuit level measurements have been reported on PMOS PBTI or NMOS NBTI. Most of the previous works focus on device level measurements and modeling aspects of these two BTI modes.

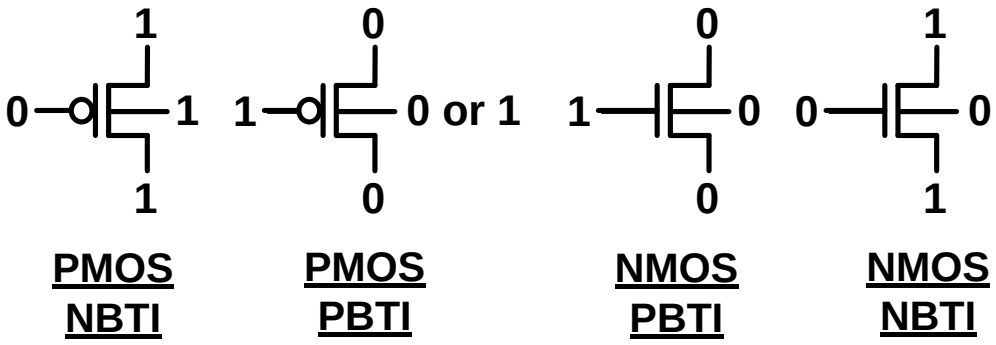


Fig. 4.1: Bias condition for all four BTI modes.

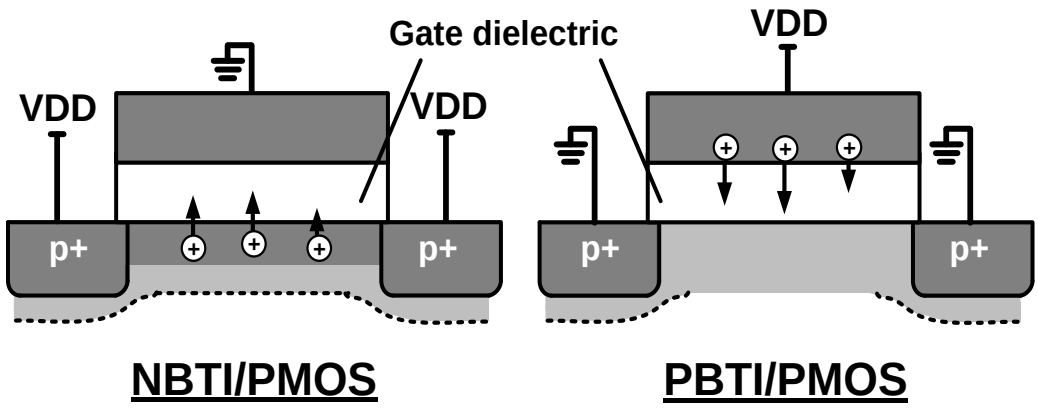


Fig. 4.2: Transistor cross sections describing (a) NBTI/PMOS, and (b) PBTI/PMOS [44]

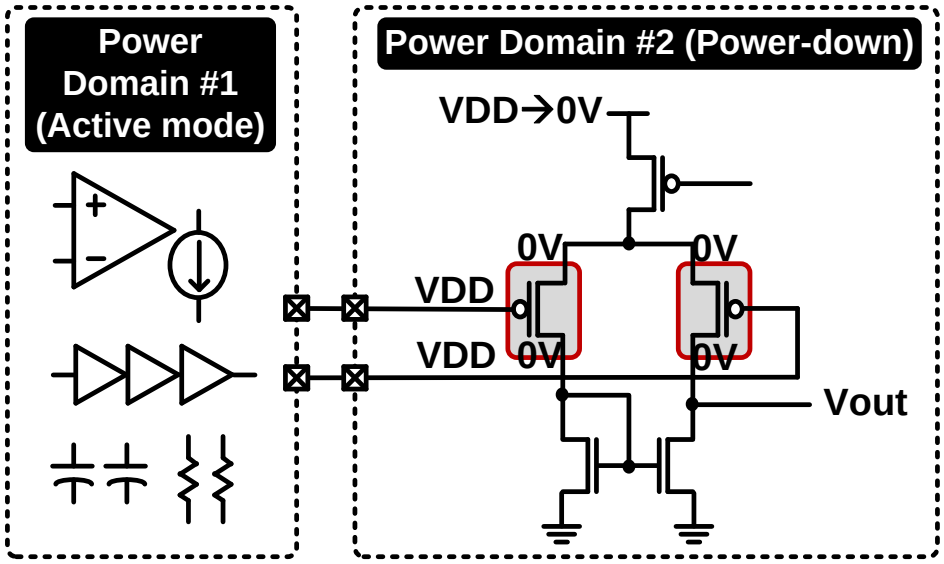


Fig. 4.3: Power down scenario where PMOS devices in a differential amplifier circuit are exposed to PBTI stress [8]. In this scenario, power domain #1 is active while power domain #2 is shut down.

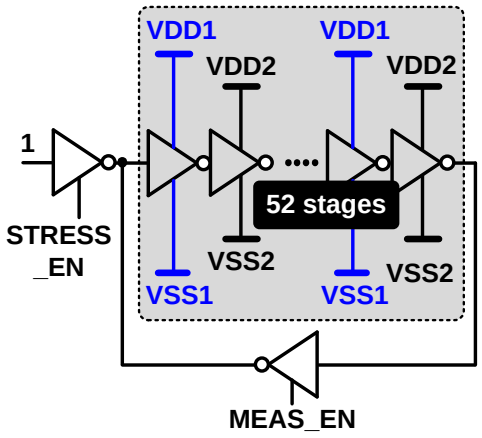
In this work, we demonstrate for the first time, an on-chip beat frequency based monitor circuit capable of characterizing frequency shifts caused by all four BTI modes. The main innovation is a ring oscillator (ROSC) circuit with dual power rails enabling different BTI stress modes. The beat frequency detection scheme offers a high frequency measurement precision (>0.01%) with minimal unwanted device recovery during measurements owing to the short stress interrupt time (>1µs) [52]-[56].

4.2 Dual Power ROSC Structure and Beat Frequency Circuit

4.2.1 Test ROSC with 4 BTI Stress Modes

The proposed ROSC circuit shown in Fig. 4.4 consists of two power rails, a 52 stage inverter chain, and two tri-state inverters. During stress mode, the ROSC is configured as

an open loop inverter chain whose input is set to 0V. To apply different BTI stress modes to the inverter chain, two sets of power supplies are used; VDD1 and VSS1 for odd inverter stages and VDD2 and VSS2 for even inverter stages. In measurement mode, the inverter chain is configured into a ROSC and the power rail voltages are switched to the nominal VDD and VSS voltages. Fig. 4.5 shows the transistor-level schematic of two ROSC stages for the 4 distinct stress modes. Stress mode #1 represents the typical stress condition of an inverter circuit with VDD1=VDD2=Vstress and VSS1=VSS2=0V. This induces PMOS NBTI in the first stage and NMOS PBTI in the second stage. In stress mode #2, VDD2 is switched to 0V which induces PMOS NBTI in the first stage and PMOS PBTI in the second state. VSS1 is switched to Vstress in stress mode #3 which results in PMOS NBTI and NMOS NBTI in the first stage, and NMOS PBTI in the second stage. Finally, in stress mode #4, all four devices undergo BTI stress using the specific stress voltage configuration in Fig. 4.5 (lower right). The individual BTI components can be obtained by taking the difference between the measured frequency shifts of the respective stress modes. In our implementation, the PMOS body was tied to the source terminal so Vstress is applied between the gate terminal and the other three terminals (i.e. source, drain, body) of the PMOS device. On the other hand, NMOS body is connected to 0V so Vstress is applied between the gate terminal and the source/drain terminals (not body terminal) during NMOS NBTI stress mode.



Mode 1	PMOS NBTI + NMOS PBTI
Mode 2	Mode1 + PMOS PBTI
Mode 3	Mode1 + NMOS NBTI
Mode 4	Mode1 + PMOS PBTI + NMOS NBTI

Power Supply Conditions				
Stress Mode	**VDD1**	**VSS1**	**VDD2**	**VSS2**
Mode 1	Vstress	0	Vstress	0
Mode 2	Vstress	0	0	0
Mode 3	Vstress	Vstress	Vstress	0
Mode 4	Vstress	Vstress	0	0
Meas. Mode	Vnom	0	Vnom	0

Fig. 4.4: (left) Proposed dual power rail ROSC. (upper right) BTI stress modes. (lower right) Power supply configuration.

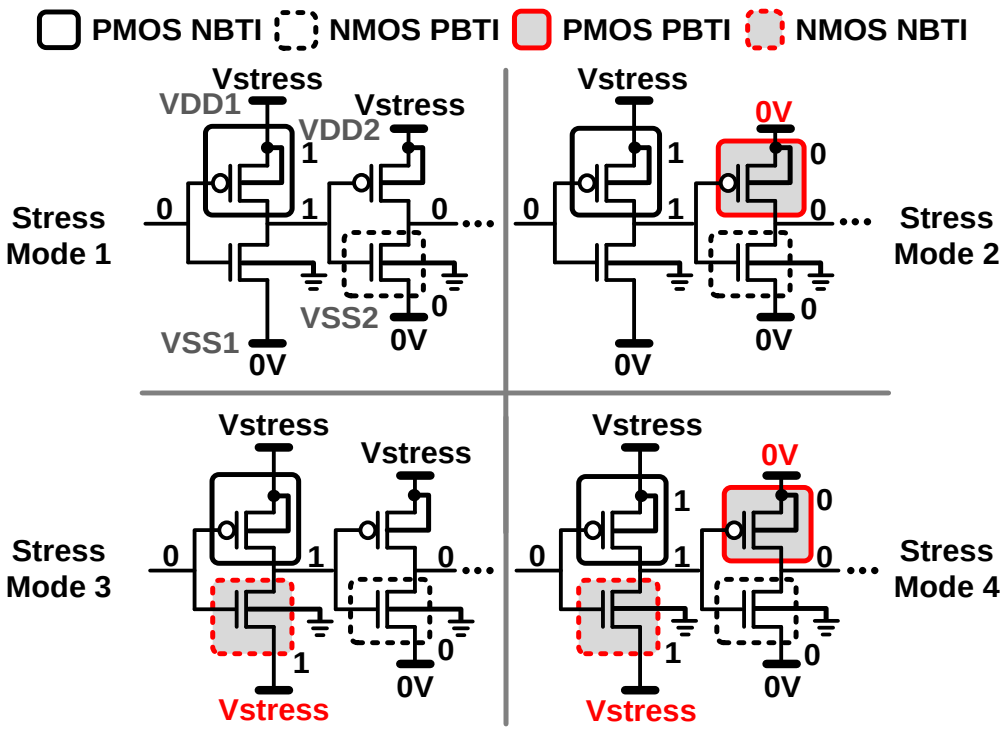


Fig. 4.5: (a) Stress mode 1: PMOS NBTI+NMOS PBTI, (b) stress mode 2: stress mode 1 + PMOS PBTI, (c) stress mode 3: stress mode 1 + NMOS NBTI, (d) stress mode 4: stress mode 1 + PMOS PBTI + NMOS NBTI. PMOS body is tied to its own source terminal while NMOS body is tied to the global ground voltage.

4.2.2 Array based Beat Frequency Measurement Circuit

Fig. 4.6 shows the beat frequency detection (BFD) circuit for measuring the frequency shift of the stressed ROSC. The output signal of the D-flip-flop exhibits the beat frequency, fbeat = fref - fstress. The beat frequency between the stressed and reference ROSC is measured by counting the number of reference ROSC periods that can fit within one period of the phase comparator output signal. Using the digital output code N[9:0], we can compute the frequency shift in the stressed ROSC with picosecond accuracy.

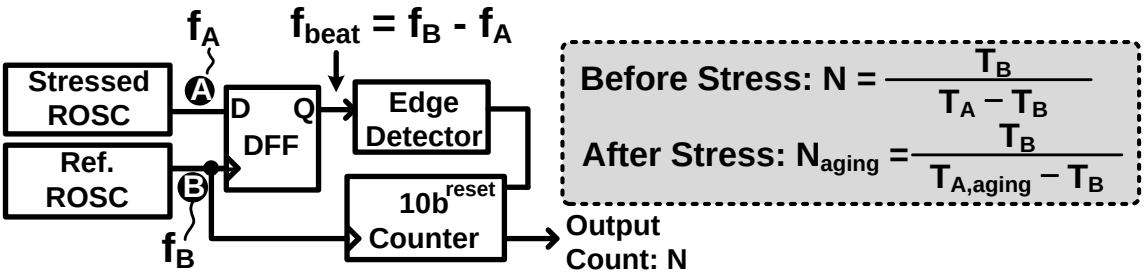


Fig. 4.6: Frequency degradation monitor based on "silicon odometer" beat frequency detection (BFD) scheme.

The top level diagram of the 65nm test vehicle is shown in Fig. 4.7. It consists of a 48 ROSC array grouped into four 12 ROSC sub-arrays, 3 reference ROSCs, and 3 parallel BFD circuits. Each sub-array is assigned to one of the four different stress modes, and power switches control the two VDD and VSS pairs depending on the stress mode. Before applying stress, we measured the frequency distribution of fresh DUTs. The frequencies of the three reference ROSCs were separated using on-chip trimming capacitors to cover the frequency range (~3%) of the ROSC array. During stress mode, one ROSC is selected at a time for frequency measurements using column and row decoders while the other ROSCs are kept in stress mode. The output of the selected DUT is multiplexed out and compared

with the three reference ROSC frequencies using the BFD circuits. Of the three beat frequency counts, we chose the one providing a high accuracy for data analysis. The frequency difference between the stressed ROSC and reference ROSC was kept within ~2% to maintain a high measurement precision throughout the entire stress period (Fig. 4.8).

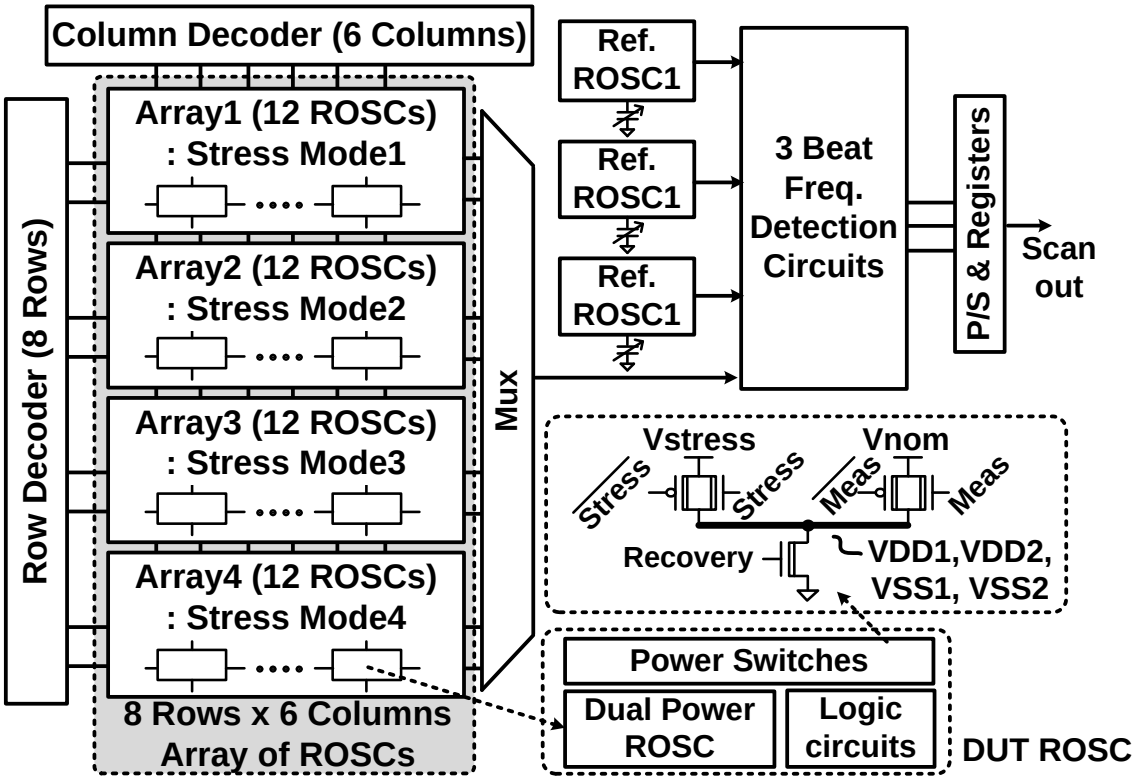


Fig. 4.7: Test chip organization: 12x4 ROSC array, three reference ROSCs, power switches, and BFD circuits.

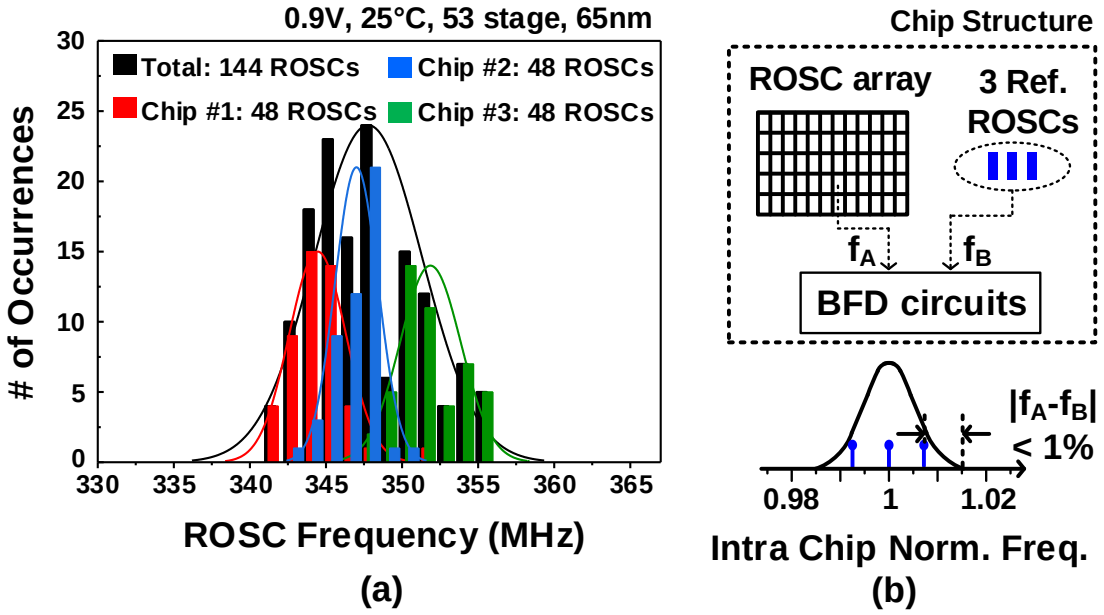


Fig. 4.8: (a) Fresh frequency distributions of three chips. (b) 3 reference ROSCs with frequency trimming capability were used to cover the entire frequency range.

4.3 BTI Stress Model

The BTI stress mechanism can be described using either the trapping/detrapping model or the reaction-diffusion (R-D) model [57] – [60]. In this work, the traditional R-D t^n model is used. ΔVth(t) is expressed as:

$$\Delta \mathrm{Vth}(t) = \mathrm{A} \cdot \exp(\gamma \mathrm{VDD} - \frac{E_a}{kT}) \cdot t^n \tag{4.1}$$

Here, Vth is threshold voltage, VDD is the power supply, *n* is the BTI stress time exponent, γ is the voltage acceleration factor, *Ea* is the temperature activation energy, *k* is the Boltzmann constant, *T* is the absolute temperature, and *t* is the BTI stress time . Also, Δfrequency (Δf) of ROSCs is expressed as:

$$\Delta \mathrm{f} = \Delta \mathrm{Vth} \,/\, (\mathrm{VDD} - \mathrm{Vth}) \tag{4.2}$$

From (4.1) and (4.2), the following formulas can be obtained:

$$\ln\left(\Delta f \cdot \frac{VDD-Vth}{t^n}\right) = \gamma VDD + C1 \text{ (@ fixed Temp.)} \quad (4.3)$$

$$\ln\left(\Delta f \cdot \frac{VDD-Vth}{t^n}\right) = -E_a \cdot \left(\frac{1}{kT}\right) + C2 \text{ (@ fixed VDD)} \quad (4.4)$$

Here, C1 and C2 are constants. Based on (4.1), the BTI stress time exponent (n) is obtained from the experimental data of the test chip. Also, the parameters of γ and *Ea*, are extracted from the silicon results based on (4.3) and (4.4), respectively. Both parameters of γ and *Ea* are reaction characteristics related coefficients under different stress voltage and temperature conditions. ΔVth is also obtained from the measured Δfrequency of the ROSCs.

4.4 Test Chip Stress Results

4.4.1 Test Setup

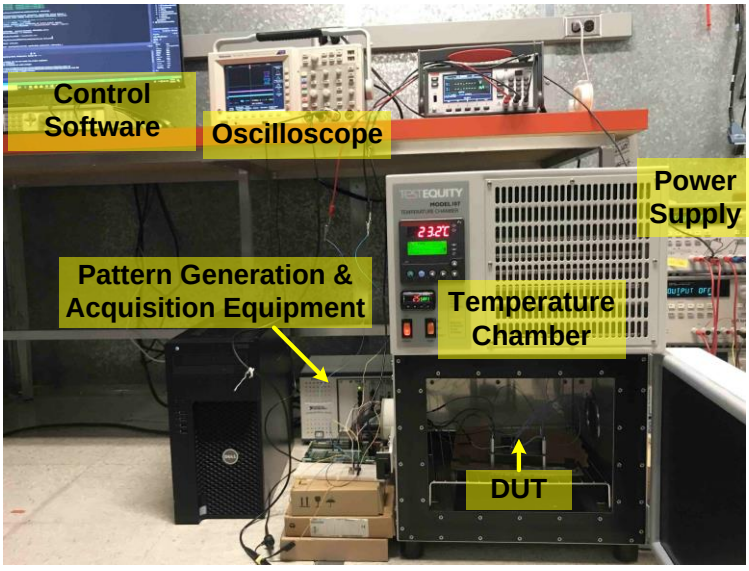


Fig. 4.9: Test setup

National Instrument (NI) PXIe-1073 is used for data/clock pattern generation and acquisition. C/C++ code based software controls the NI PXIe-1073, and multiple power supplies (Agilent Technologies E3631A) are used for different power of the ROSC array. To apply BTI stress under different temperature, we use the temperature chamber (TESTEQUITY Model 107) which adjust with the temperature range from -42°C to +130°C. The DUT chip and the PCB board are placed inside the temperature chamber as shown in Fig. 4.9.

4.4.2 Measurement Results

The 65nm ROSC array chip was tested under different stress conditions. Fig. 4.10 shows the frequency distribution before and after 3 hours of 2.2V DC stress at 25°C. The DUT frequencies were characterized at 0.9V. Each distribution was obtained from 36 ROSCs measured from 3 test chips. To extract the individual BTI components, we took the difference between the frequency shifts measured under different stress modes. For instance, PMOS PBTI induced frequency shift was obtained by subtracting the frequency shift of stress mode 1 from that of stress mode 2. The average frequency shifts at the end of the stress period were higher for stress mode 2 ($\Delta f = 2.88\%$) and stress mode 4 ($\Delta f=2.87\%$) as compared to that of stress mode 1 ($\Delta f=2.01\%$), due to the additional PMOS PBTI effect. On the other hand, the frequency shift for stress mode 3 ($\Delta f=1.72\%$) was less than that for stress mode 1 ($\Delta f=2.01\%$) by a small margin, indicating that NMOS NBTI is negligible compared to PMOS PBTI. The additional frequency shifts compared to the baseline 'PMOS NBTI + NMOS PBTI' induced shift at the end of the stress period are: (i)

0.87% for PMOS PBTI; (ii) -0.29% for NMOS NBTI; and (iii) 0.86% for 'PMOS PBTI + NMOS NBTI'.

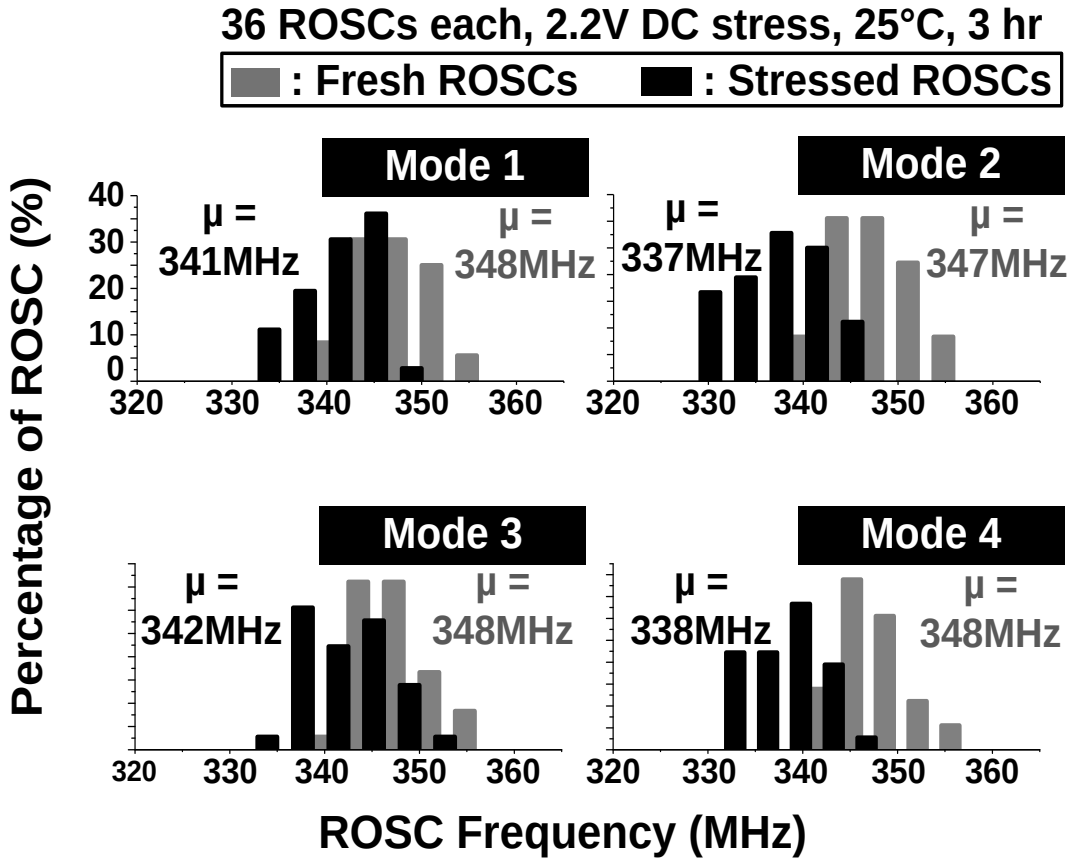


Fig. 4.10: Frequency distributions after 3 hours of stress (black bars), along with the fresh distributions (gray bars). Each histogram was obtained by measuring the beat frequency of 36 ROSCs.

Fig. 4.11 shows frequency shift data for a 2.2V DC stress measured at 25°C. Both 'PMOS NBTI+NMOS PBTI' and 'PMOS PBTI' show a similar increase in average frequency shift, indicating an increase in Vth, while NMOS NBTI exhibits the opposite trend, albeit with a much smaller magnitude. As shown in Fig. 4.11(b), PMOS PBTI shows

a higher time slope than PMOS NBTI. Also, PMOS N/PBTI induced shifts show a power law time dependence. However, the shift caused by NMOS NBTI does not follow the power law and instead shows two different trends. Short-term stress results in an increased frequency shift (i.e. degradation), as in PMOS NBTI/PBTI stress modes, while long-term stress results in a decrease in the frequency shift (i.e. recovery). These observations are consistent with the results reported in [49] [50]. Furthermore, Fig. 4.11(b) shows the relative magnitude of frequency shifts for the different BTI modes. NMOS PBTI is assumed to be negligible compared to PMOS NBTI since the 65nm technology used in this work does not employ high-k dielectrics [53][54]. In the early stage of stress, PMOS NBTI effect is most pronounced (~7x higher compared to NMOS NBTI effect), followed by PMOS PBTI effect (~3x higher), and then NMOS NBTI effect. Note that the degradation caused by PMOS PBTI effect is known to increase when a positive bias is applied between the gate and body node [49]. Fig. 4.11(c) shows the threshold voltage shift estimated based on the measured frequency data and the simulation results in Fig. 4.12. That is, the linear relationship between frequency shift and threshold voltage shift is used to map the measured frequency data to the corresponding Vth shift. At the last data point of the threshold voltage in NMOS NBTI, ΔVth has a negative sign, indicating Vth after long-term stress becomes smaller than the fresh Vth.

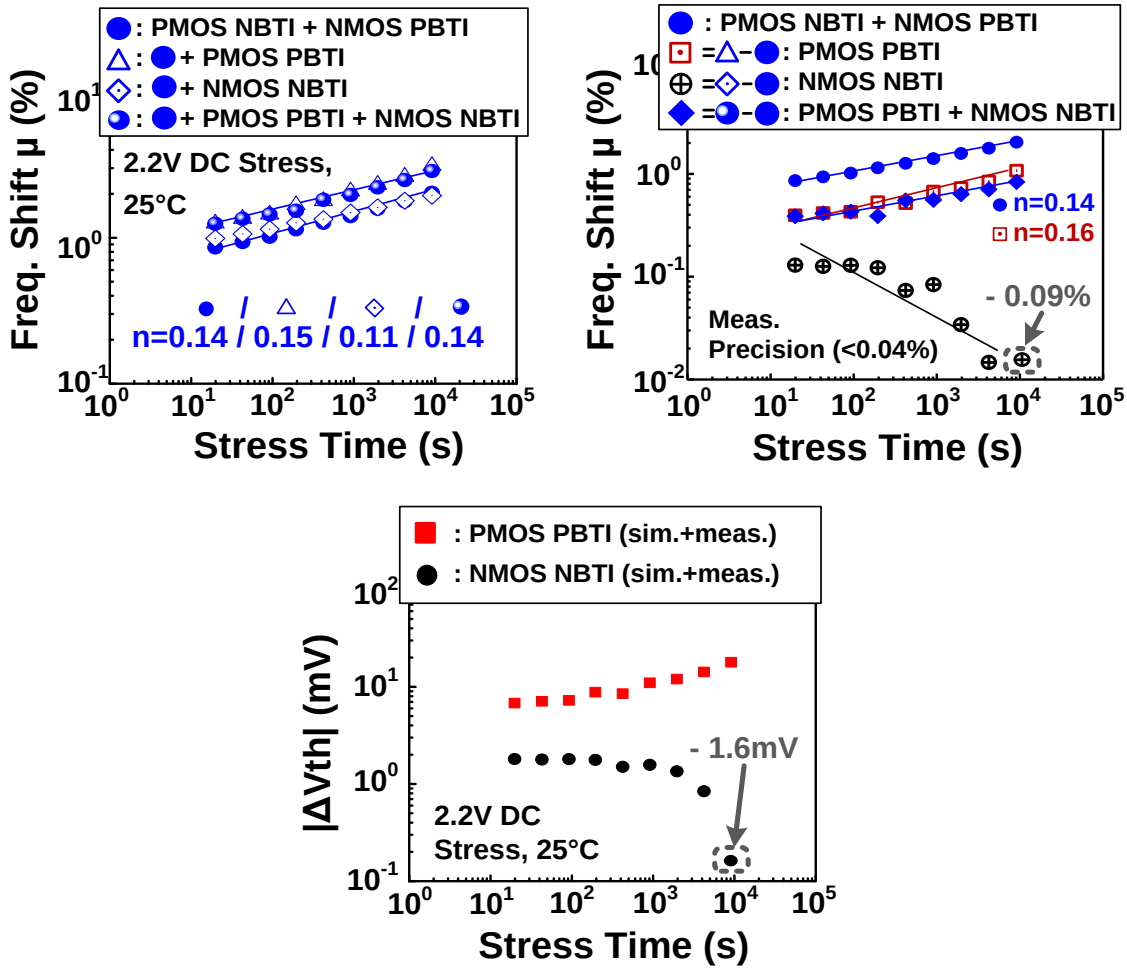


Fig. 4.11: Frequency shift data for 2.2V, 25°C DC stress. (left) Measured frequency shift under 4 stress modes. (right) BTI components extracted by taking the difference between the frequency shift results. (bottom) Threshold voltage degradation estimated based on the simulation results in Fig. 10. Vth degradation due to NMOS NBTI recovers and eventually shifts in the opposite direction after a long stress period.

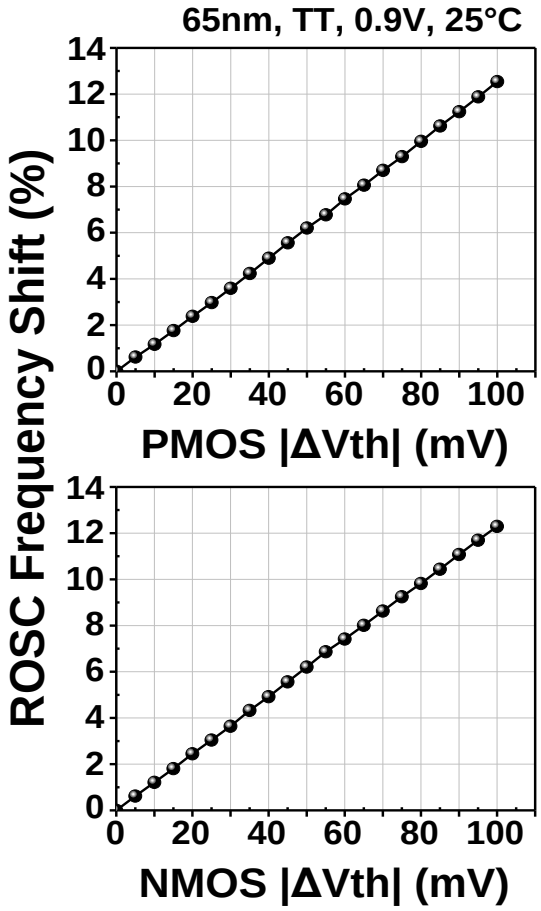


Fig. 4.12: SPICE results showing ring oscillator frequency shift versus threshold voltage shift for the 65nm technology used in this work. Vth shift in Fig. 4.11 (right) was obtained using these simulation results.

Frequency shift measurements for different stress voltages (2.6V, 2.2V, and 1.8V) at 25°C are shown in Fig. 4.13, indicating a larger frequency shift at a higher stress voltage for all 4 stress modes. As shown in Fig. 4.13(b), the time slope of the PMOS PBTI is higher than that of the PMOS NBTI at 1.8V and 2.2V. However, the trend does not hold at 2.6V. The voltage acceleration factors (γ) are 1.69V-1 and 3.94V-1 for PMOS NBTI and PMOS PBTI, respectively. The PMOS PBTI shows a larger acceleration factor, which is consistent with previously reported data in [49]. Frequency shifts measured at 25°C and 100°C under

a 2.2V stress are shown in Fig. 4.14. All 4 BTI components have a positive correlation with temperature while the power law exponent increases at higher temperatures. The time slope trend (i.e. PMOS PBTI's > PMOS NBTI's) is also observed under 100°C (Fig. 4.14 (b)). Finally, Fig. 4.14 (c) compares the PMOS PBTI + NMOS NBTI effect obtained using two different methods. The first method is subtracting the frequency shift data of stress mode 1 from those of stress modes 2 and 3, and summing them up. The second method is subtracting stress mode 1 result from stress mode 4 result. The error between the results obtained from the two methods was 6.6% for the 100°C case which indirectly confirms that the frequency subtraction method is reasonably accurate for extracting the individual BTI contributions. At 25°C, the error (23.0%) is somewhat larger than at 100°C, which can be attributed to the smaller frequency shift at 25°C. Fig. 4.15 shows the die photo and chip summary of the 65nm test chip.

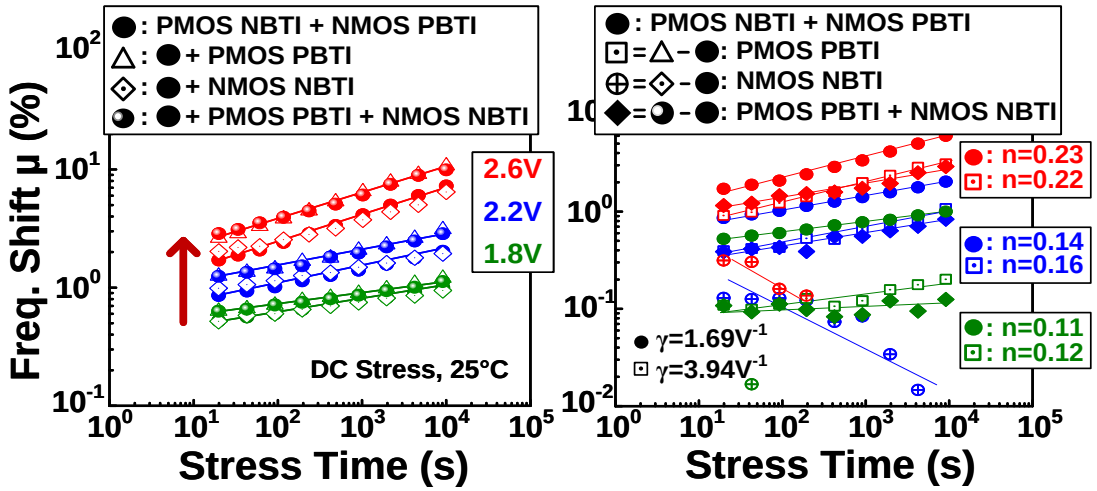


Fig. 4.13: Frequency shift for all 4 BTI modes under different stress voltages. (left) Combined frequency shifts. (right) Individual frequency shifts extracted from combined shifts.

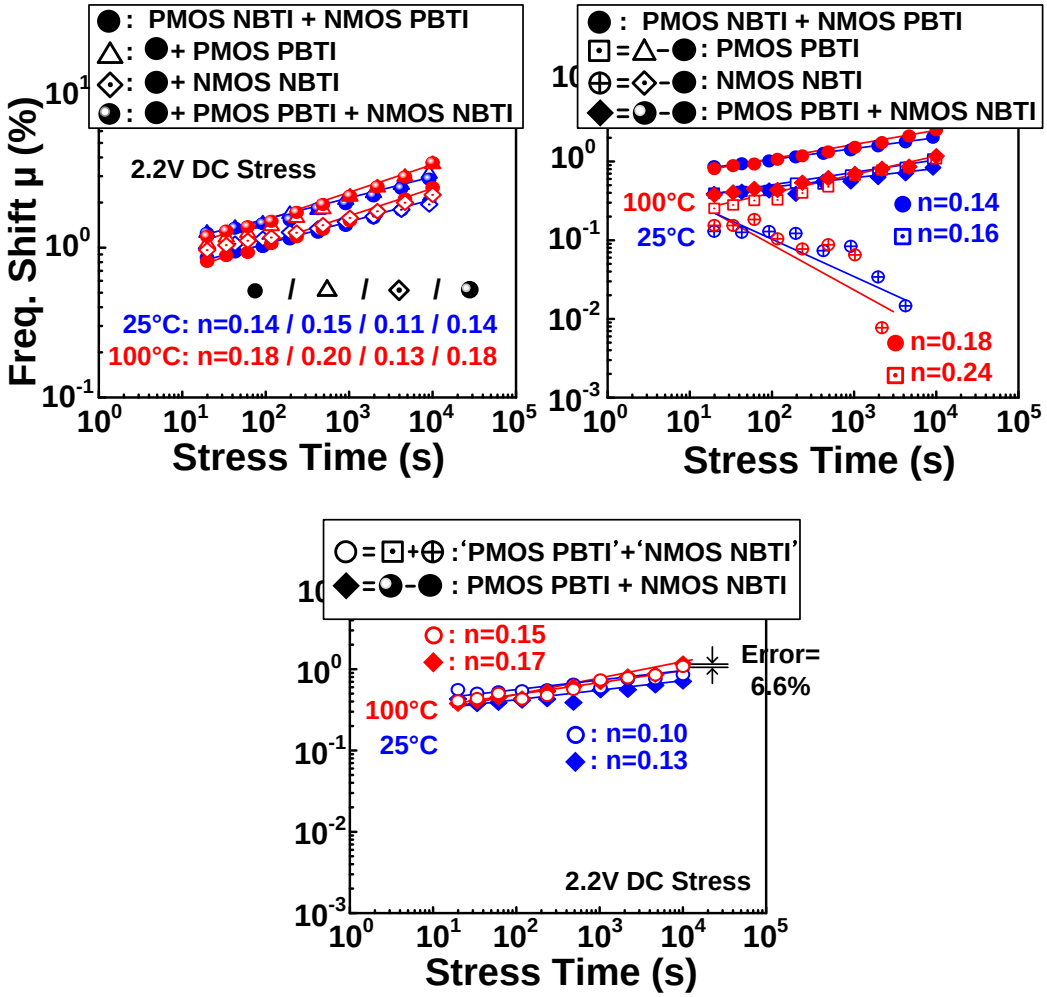
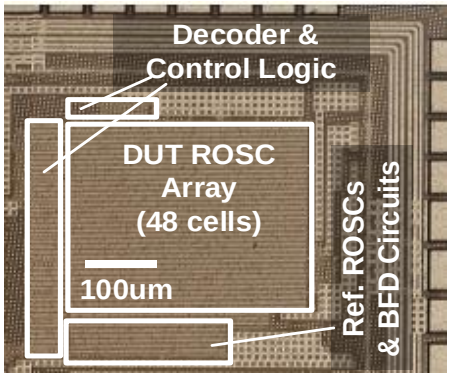


Fig. 4.14: Frequency shift for the 4 BTI modes at 25°C and 100°C. (left) Combined frequency shift measured from test chip; (middle) Individual BTI results obtained by subtracting the combined frequency shifts; (right) Comparison between the sum of individual PMOS PBTI and NMOS NBTI shifts and the combined PMOS PBTI + NMOS NBTI measured from test chip. The difference between the two methods is 6.6% at 100°C which suggests that the subtraction method is acceptable for estimating the individual BTI components.



Process	65nm GP
BTI Stress Modes	PMOS NBTI, NMOS PBTI, PMOS PBTI, NMOS NBTI
Core/IO Supply	1.0V / 2.5V
Stress Voltage	1.8V, 2.2V, 2.6V
Meas. Voltage	0.9V
DUT Device	Core Deivce
Area	425 x 360 μm^2

Fig. 4.15: Die photo and chip specification summary.

4.5 Conclusion

In this work, an on-chip reliability monitor capable of characterizing all four types of bias temperature instability (BTI) modes is proposed. Stressed ring oscillators with independent dual power rails are implemented in which odd and even stages of an inverter chain are subject to different stress voltage configurations. A beat frequency detection technique with 3 reference ring oscillators achieves a frequency measurement resolution as low as 0.01% with a short measurement interruption time of 1µs. Extensive BTI data collected from a 65nm ROSC array is presented for different stress conditions.

Acknowledgement

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Chapter 5. Op-AMP Reliability Odometer

5.1 Introduction

With the scaling down of CMOS technology, the reliability issues of devices have become more severe. While the impact of device aging on digital logic or memory circuits for different stress mechanisms have been widely explored, circuit researchers have yet to fully understand their impact on analog and mixed-signal circuit performance. Unlike in digital gates where transistors are subject to the full supply voltage, devices used in analog circuits such as operational amplifiers (Op-AMPs) under a lower Vgs and Vds voltage bias. Consequently, the absolute parametric shift due to device aging has known to be relatively small in analog circuits as compared to their digital counterpart. In a highly sensitive analog circuits, even if aging induced shifts are relatively small, it can cause a negative impact on circuit performance. Particularly, measuring the subtle performance shift and fast transient response of Op-AMP is extremely challenging. We can use the conventional off-chip measurement method, but the off-chip measurement components can introduce inaccuracy in the measurement. Practically, it would be impossible to accurately detect the subtle shift in fast transient response of Op-AMP without data loss using the conventional off-chip testing. Therefore, in this thesis, we propose an on-chip monitoring circuit for precise characterization of Op-AMP reliability issues for the first time. Based on our research, there have been no prior arts on this topic. Our proposed monitor characterizes the transient response of the Op-AMP output with two methods: (i) measuring the output transient

response for square wave input, and (ii) measuring the output transient response for load/power supply transition. Based on the two methods, we can obtain overshoot, settling time, slew rate, DC gain, and phase margin. In this work, we manipulate temperature using an implemented on-chip heater as an aging acceleration factor. Since an Op-AMP consists of a number of transistors with different bias condition (e.g. different Vgs and Vds), simply increasing the supply voltage (as Chapter 2 and 4) does not apply the same acceleration effect to all devices in the Op-AMP. Therefore, by applying the same temperature to all the devices in the Op-AMP at the same time, the same amount of acceleration effect can be reflected.

5.2 Transient Response Monitoring Methods

5.2.1 Monitoring Method 1: Transient Response for Square Wave Input

Fig. 5.1 shows the conceptual circuit diagram and the monitoring method 1. During the stress mode, hot temperature is applied to accelerate aging mechanism by turning on the on-chip heater. Since the stress needs to be just applied to the Op-AMP in the stress mode, the on-chip monitor (a comparator and a m-bit counter) turns off while the Op-AMP performs normally. Also, various types of signal (e.g. sine, square wave, ramp, DC, and etc.) are applied to the Op-AMP as an input to address a typical Op-AMP performing with various input signals. After applying the stress, the circuits are switched to the measurement mode. In the measurement mode, the on-chip heater is OFF to recover to room temperature and consequently aging acceleration is removed. All the circuits are ON

and a square wave is applied to the Op-AMP using an on-chip signal generation circuits. The comparator in the monitor captures the Op-AMP output by sweeping Vsweep across several cycles of the square wave signal. Then, the corresponding *N* count is collected from the m-bit counter and we can construct a distribution of the Op-AMP output. To change the sampling point in X-direction, the CLK edge can be adjusted by the programmable delay line.

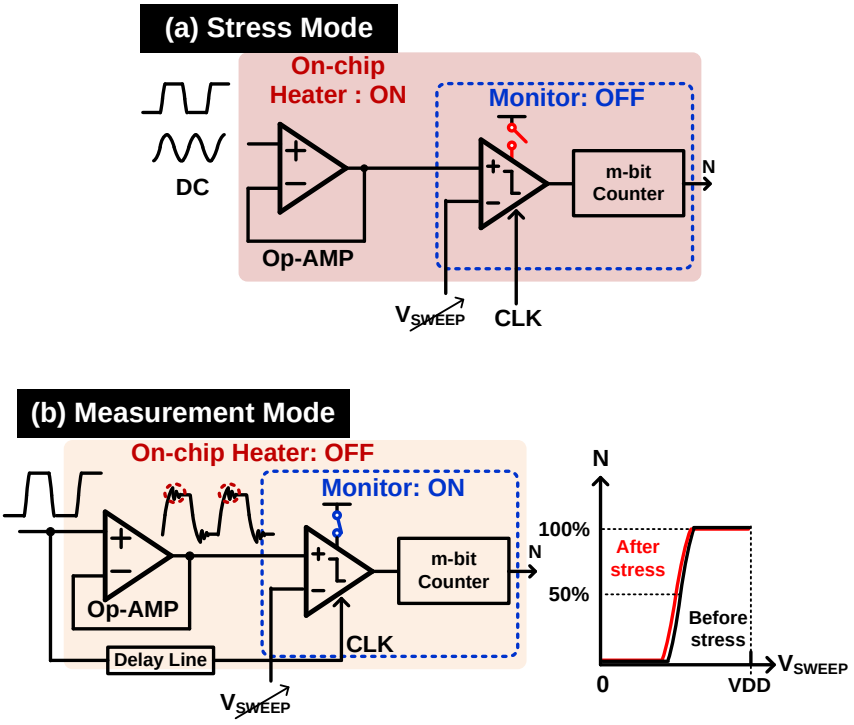

Fig. 5.1: Conceptual diagram for the monitoring method 1: (a) stress mode and (b) measurement mode.

5.2.2 Monitoring Method 2: Transient Response for Load/Power Supply Transition

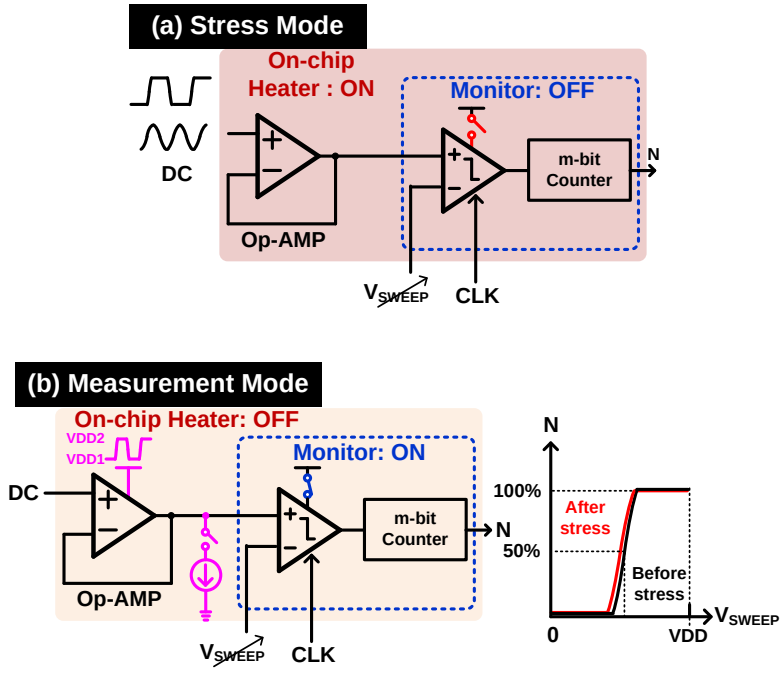

Fig. 5.2: Conceptual diagram for the monitoring method 2: (a) stress mode and (b) measurement mode.

In the monitoring method 2, the stress condition is same as the monitoring method 1. But, unlike the method 1, in the measurement mode of the method 2, DC signal is applied to the input of the Op-AMP while either power supply or load current step responses are measured at the Op-AMP output. Thus, the power supply is switched between two voltage levels (e.g. VDD1 and VDD2) and load current is changed between ON and OFF. Unwanted oscillation can be observed when the power supply or load is changed quickly. If the Op-AMP cannot correct the output promptly, overshoot or undershoot can happen until it is damped out. Thus, we can analyze stability of the Op-AMP using this method.

As same as the method 1, the comparator samples the Op-AMP output and we can construct a distribution from the counter (Fig. 5.2).

5.3 Overall Circuit Implementation

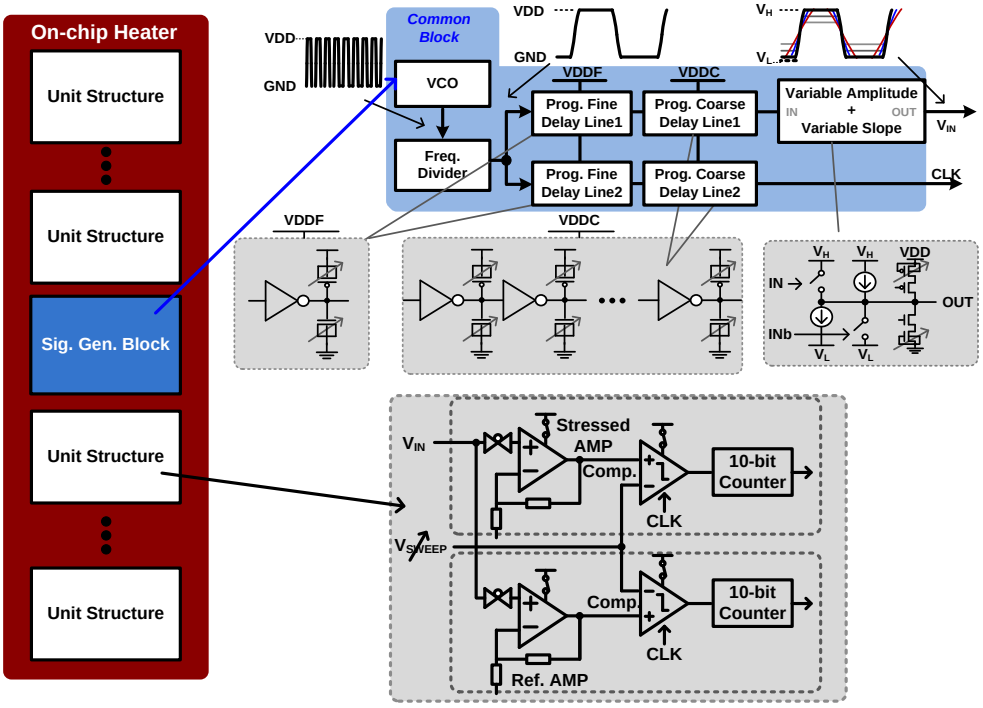

Fig. 5.3: Overall circuit diagram and individual block.

Fig. 5.3 shows the overall circuit implementation diagram and individual block. The on-chip heater covers the entire circuits. The on-chip signal generation block is a common block which consists of a voltage controlled oscillator (VCO), a frequency divider, two identical fine + coarse delay lines, a variable amplitude and slope generation circuit. The two fine and coarse delay lines share the dedicated power supplies of VDDF and VDDC, respectively. Also, multiple unit structures which consist of two identical blocks (i.e. two

sets of Op-AMP + comparator + 10b counter) are implemented. One set is for the stressed AMP and another set is for the reference AMP (i.e. fresh AMP). During the stress mode, only the stressed AMP performs while all other circuits in the signal generation block and the unit structure power down by turning off the power gating switches. In the measurement mode, all the circuits turn on and perform normally. By using two identical structures (i.e. two delay lines, and two sets of Op-AMP + comparator + counter), common-mode noise can be reduced. Also, several testability are employed such as programmable delay, gain, amplitude, slope of the Op-AMP input.

5.4 Conclusion

In this work, an Op-AMP reliability odometer using an on-chip monitor, on-chip signal generator, and an on-chip heater is proposed for the first time in 65nm CMOS process. A comparator and a counter are implemented to monitor the Op-AMP output before and after the stress. Two monitoring methods are employed: (i) monitoring output transient response for a square wave input, and (ii) monitoring output transient for power/load transition. The differential delay lines in the on-chip signal generator achieve high precision of timing control for both the Op-AMP input signal and the comparator clock by reducing common noise reduction.

Chapter 6. Summary

In this thesis, several simple on-chip monitoring circuits are proposed to characterize circuit reliability aspects in the mixed-signal systems such as ADPLL and SAR ADC. Also, we propose the new BTI odometer for sensing all four different BTI stress effects at a single system. Their performance are verified with the measurement results obtained from working test chips implemented in 65nm LP and GP CMOS technologies. Moreover, in-situ measurement schemes employed in these circuits enable accurate measurement without requiring sophisticated measurement setup in the noise sensitive mixed-signal systems.

Chapter 2 introduces two on-chip monitors for ADPLL reliability measurements: (i) the silicon odometer based on BF detector; and (ii) the phase window monitor. The silicon odometer utilizes beat frequency detection mechanism to achieve high resolution measurement for aging induced frequency shift detection. Moreover, the phase window monitor enables us to indirectly detect phase noise shift caused by aging effects at ADPLL system. Additionally, using the off-chip hot plate, we explore the annealing effects (i.e. recovery effects) from the stress state to the near fresh state under hot temperature conditions. In the 65nm test chip of the proposed two on-chip monitors, 1.2V of nominal supply and 2.4V of stress supply are used, and free running DCO frequencies are 720MHz and 1.54GHz at the nominal supply and the stress supply condition, respectively. 110°C and 240°C are utilized for the hot temperature annealing.

Characterizing ADC non-linearity is a challenging task as their performance is sensitive to the noise in the measurement setup. Also, it requires an extensive readout data volume from ADCs to analyze their non-linearity. To overcome these limitations, the in-situ counter based ADC non-linearity measurement circuit is proposed for SAR-ADC in chapter 3. It simply utilizes a decoder, a 5-bit counter array, and scan-out circuits. For further arear reduction of the counter array, a 2-way interleaved design is proposed. In this method, two separate test are required for odd and even ADC output codes. After the two separate tests, the two test results are stitched together for full DNL and INL histograms. The proposed 2-way interleaved design only requires a half of the counters meaning that 50% of area reduction is achieved. Furthermore, this method can be extended to N-way interleaved design. That is, we can reduce the area to 1/N by suffering N-time separate tests. The DNL and INL measurement results from the test chip confirms that the in-situ measurement circuits do not affect to DNL and INL results even if ADC clock frequency increases. Thus, it shows that the proposed design eliminates package and board noise issues. Due to the noise reduction, the measurement results from a 65nm test chip shows 1.23 LSB of DNL improvement compared to conventional methods. Moreover, it drastically reduces the read out data volume (i.e. 1/64 of the conventional method). Using the in-situ design, short-term BTI is studied in a 10-bit SAR-ADC in 65nm CMOS technology. The short-term Vth degradation and recovery can occur at the comparator of SAR-ADC due to BTI effects. It leads time-variant offset at the comparator and manifests as a 1LSB error in the ADC output code. The subtle DNL shifts can be accurately measured

in different comparator types, and different ADC clock frequency and duty cycle conditions due to the precise in-situ non-linearity measurement circuits.

In chapter 4, the odometer based on a dual power rail ring oscillator array is presented for the all four BTI (i.e. PMOS NBTI, PMOS PBTI, NMOS NBTI, and NMOS PBTI) effects detection. The proposed on-chip odometer enables accurate aging dynamics characterization for four different BTI stress simultaneously at a single system. In this test chip, 1.0V and 2.5V are used for core and IO devices, respectively. 3 stress supply voltages (i.e. 1.8V, 2.2V, and 2.6V) are used for the stress phase, and 0.9V is used for the measurement phase. The odd and even stages of an inverter chain in ROSCs are subject to different stress voltage configurations (i.e. 4 configurations for 4 BTI stress). Aging induced Vth shift is detected by a beat frequency detection technique with 3 reference ring oscillators. It enables high resolution measurement as low as 0.01% of frequency. Extensive BTI data is collected from a 65nm test chip for different stress conditions.

In chapter 5, the odometer based on the on-chip monitor, signal generator, and heater is presented. The proposed on-chip heater enables the precise on-chip temperature control. Also, the on-chip monitor and signal generator achieve accurate aging dynamics characterization for the Op-AMP transient response.

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