Modular Multilevel Converter based Power Electronic Transformers for Grid Integration of Renewables and Motor Drives

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Dedication

To my family for always believing in me

Abstract

At high voltage and power levels in utility-scale applications, transformers are needed for integrating renewables and motors. At present, 60-Hz transformers are used that are bulky and have significant weight. A novel interface using modular multilevel converter (MMC) based power electronic transformer (PET) is proposed which operates at much higher frequencies than 60-Hz transformers and thus can be significantly more compact and energy-efficient. Due to its modular structure, the high voltage side can be easily scaled resulting in higher reliability and easy maintenance. Such PETs also offer a smart solution for improving reliability in future power systems and interfacing of auxiliaries, such as storage batteries and STATCOMs.

The first part of the thesis describes the modular multilevel converter operation. By using an array of series connected submodules, this converter can generate high number of voltage levels resulting in a near sinusoidal output voltage waveform. This eliminates the need for lossy snubbers required otherwise for connecting devices in series to meet the high voltage stress. A new submodule of the MMC is proposed which requires lesser number of these submodules to result in smaller system footprint and lower losses. A hybrid modulation scheme with voltage balancing algorithm is proposed to balance the floating capacitors in the new MMC. An intelligent commutation technique results in $2/3^{\text{rd}}$ of the switching transitions to be soft switched in the proposed submodule.

The proposed power electronic transformers using MMCs generate sinusoidal voltages and currents through the high frequency transformer (HFT) resulting in significant reduction in transformer magnetic losses. Also natural commutation of leakage energy is obtained. Two variants of the low voltage side renewable or motor connected power converter are presented using either a back-to-back connected voltage source converter or single-stage matrix converter. Control of the output voltage requirement by the rotating machine is met by controlling the output voltage of the MMC on the high voltage side of the HFT, to result in reduced voltage stress and losses in the transformer, machine interfaced converter and the machine. A multi-winding transformer architecture to integrate multiple renewable energy sources is also presented.

The thesis presents the analysis and operating principle of such PETs for use in future power distribution systems and addresses the challenges for commercialization of such PETs. Simulations with experimental results on a scaled down laboratory prototype verify proof of concept.

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Chapter 1

Introduction

Climate change is a grave threat facing humankind and the need for reducing greenhouse gas emissions by using renewables is urgent. Hence it is highly desirable to utilize more renewable energy sources such as wind and solar in the power grid. Renewable sources of electricity are increasing their penetration of the electric utility grid in spite of low oil and gas prices. In certain markets, these have already achieved grid parity [1, 2]. However, further reducing their cost and increasing their efficiency and reliability will accelerate their penetration. There is ample room for cost reduction in wind plants by reducing the nacelle weight by 20 percent and in PV plants by reducing the balance-of-system cost which now accounts for two-third whereas solar cells only one-third of the overall cost [3].

Renewable energy from wind and solar is generated at voltages below 2 kV through power electronic converters. Same is true about voltage levels of motors used in pumps and compressors. The conventional method of interfacing the converter output to high voltage grid like 34.5 kV [4], that has become the de-facto collection grid voltage in utility-scale application, is by means of 60-Hz transformers [5, 6]. Such transformers are large and heavy (e.g., a typical transformer in a 2-MW class wind turbine weighs 7 tons) due to their operation at a low-frequency of 60-Hz. In spite of its weight, many wind-turbine manufactures are placing these transformers in the nacelle in order to reduce the amount of I^2R loss in the cables. This weight can be reduced by as much as a factor of 150 by means of transformers operating at higher frequencies, for example 10 kHz. These high frequency transformers require extra power converters and are called

power electronic transformers (PETs) or solid state transformers (SSTs). Therefore, PETs are a very attractive alternative to conventional low-frequency transformers to be directly mounted in the nacelle of the wind turbine. If PETs can surpass conventional transformers in cost, efficiency and reliability, they will have applications in all other utility-scale renewables such as solar, small hydro, and so on. In addition, they will be attractive in connecting auxiliaries such as storage batteries and STATCOMs. Another application area where PETs can be very advantageous is to supply electric motor loads and drive systems. Supplying these motors (e.g., in pumps and compressors in oil/gas industry, traction motors in electric locomotives, etc.), from a high voltage grid using PETs can prove useful by making the overall system compact and improving the system stability, efficiency and reliability. PETs have other additional features over conventional transformers such as control over voltage, frequency and real/reactive power flow through them [7, 8].

However, PETs must be able to interface to high voltage utility grid voltages, otherwise they are not applicable in utility applications mentioned above. The topologies for PETs described in literature [9, 10, 11, 12] fail to address this critical requirement. These topologies are not scalable to high voltages and hence semiconductors and passive capacitors need to be connected in series which is not easy. PETs based on complete modular design having many small high-frequency transformers in each module can be scaled for utility scale applications [13, 14, 15]. Such PETs however have large semiconductor count making the overall system large and expensive. A novel PET topology under research [16, 17, 18] and described in this thesis is modular in nature to reach voltages even higher than 34.5 kV, retaining all the attractive features of PETs mentioned earlier. The interface can provide ancillary services and control flexibility to offer a smart solution to maintain grid stability even when the penetration of renewables begins to approach conventional sources.

This thesis outlines the principle of operation of this interface so that it serves as the basis for commercializing it in wind/PV and motor drive applications. This will also lead to further research in application-specific topologies. This chapter first describes the application areas where bulky 60-Hz transformers are currently employed and the proposed PET can be used. The basis of proposed interface is described in Section 1.2. A review of current state of the art PET topologies is presented in Section 1.3 with

their limitations in extending them to utility scale applications. The proposed PET with its benefits is described in Section 1.4. The organization of the thesis is presented in Section 1.5 with concluding remarks in Section 1.6.

1.1 Present Interfaces using 60-Hz Transformers

The present methods of interfacing renewables, based on 60-Hz transformers and power electronic converters are discussed below in wind, PVs and battery-storage applications. These are the application areas where the proposed power electronic transformer based interface can be used.

1.1.1 Wind Turbine Interface

A typical arrangement of components in a MW scale wind turbine has a low-voltage 690 V generator in the nacelle that produces variable-frequency voltages and currents depending on wind speeds. Over two-thousand amperes of current flows through nearly a 100 meter long droop cable, thick enough to handle this current. These variable-frequency voltages/currents are converted by the power electronics converter, shown in Fig. 1.1 by its block-diagram, at the base of the tower to constant amplitude (700 V) and 60-Hz sinusoidal voltages that are boosted to 34.5 kV by a 60-Hz transformer weighing nearly 7 tons at these power levels.

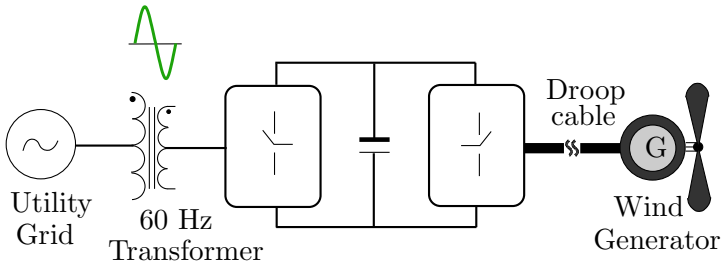


Figure 1.1: Block diagram of conventional wind generator interface using 60-Hz transformers

In a wind plant, now as large as 800 MW, hundreds such wind turbines are connected to an underground collection grid at a voltage of 34.5 kV [4, 5, 6]. Subsequently, another transformer boosts this voltage to 161 kV, for example, for transmission purposes.

Some companies are now opting to put the power electronic converter and the 60-Hz transformer in the nacelle so that only a small amount of current needs to be carried by nearly 100 meter cable. But it requires a heavy 7 ton transformer to be located in the nacelle, putting additional burden on the tower structure and the foundation, thus increasing their cost.

1.1.2 Offshore Wind Plants

Another important application is in offshore wind plants. In such systems, large cost savings are possible by using a dc collection system, as this will dramatically reduce the part count in the substation [19, 20]. The proposed topology will enable ac and dc collection grids to be combined, making the topology very flexible. In offshore systems, the platform real estate is of a high premium.

1.1.3 Photovoltaic Applications

There is substantially larger potential in harnessing electricity using photovoltaics. In a typical MW scale PV plant, power from a large array of PV modules, each operating at their maximum power point (MPP), is collected at 1,000 V (DC). This is interfaced through a power electronic converter and a 60-Hz transformer to the grid voltage of 34.5 kV.

1.1.4 Battery Storage Application

An interface, similar for wind and PVs, but with bi-directional power-flow capability, is used for large-scale battery storage facilities. These batteries are connected to the grid using 60-Hz transformers.

1.1.5 Motor Drives

The distribution systems in oil/gas industry is mostly 24.94/14.4 kV grounded wye systems. Most of the larger motors 700 hp+ are served from 4.16 kV bus work. Hence a 60-Hz transformer is used to provide this voltage step down.

1.2 Basis of Proposed Interface

The proposed topology and its derivatives are based on high-frequency transformers (HFT) replacing 60-Hz transformers to reduce weight, and a highly modular topology on the high voltage side to improve reliability.

1.2.1 High-Frequency (HF) Transformers versus 60-Hz Transformers

Compared to 60-Hz transformers, high-frequency (HF) transformers operating at 10 kHz, for example, can be significantly smaller and lighter by a factor of 150. This size reduction also implies a significant reduction in the amount of copper and the core material needed. The core of HF transformers is made up of a nano-crystalline material such as FINEMET that is ideal because of its high permeability, high saturation flux-density, and very low core-loss at frequencies of 10 kHz or so, at which these transformers are likely to operate at high power-levels. The cost of such material will reduce in large-volume production since no exotic material is required. It is important to note that the losses in the HFT are only one-tenth of those in a comparable 60-Hz transformer. Therefore, it is expected that the overall losses, including those in power electronic converters needed on both sides of the high frequency transformer, will be lower than in a 60-Hz transformer.

1.2.2 Modular Topology

The proposed interface is based on the Modular Multilevel Converter (MMC) concept commercialized in 2011 in an HVDC Transmission system at +/- 200 kV and 400 MW [21]. Such systems at much higher voltages and power-levels are being designed, confirming that the applicability of the MMC approach extends to very high voltages and power levels.

1.3 State of the art in Power Electronic Transformers (PETs)

The reduction in the weight by HFTs and commercial availability of greatly improved semiconductor devices, have led to research in power electronic transformers (PETs)

that are also referred in research literature as smart transformers and solid state transformers [7, 8]. Fig. 1.2 shows a PET topology using only 2 switches and 12 diodes on the high voltage side [9, 10], termed here as Reduced switch-count PET. However, due to leakage inductances present in the transformer, any switching of these devices results in high dI/dt (rate of change of current) across the primary leakage inductances resulting in large over-voltage, up to 4 times the grid voltage. Passive snubbers are required to protect the devices from this over-voltage which result in extra losses. Also, for utility scale applications at 34.5 kV, no devices exist with this high voltage blocking capability and hence devices have to be connected in series which is not easy. Hence, this topology is suitable for grid voltage applications below 2 kV.

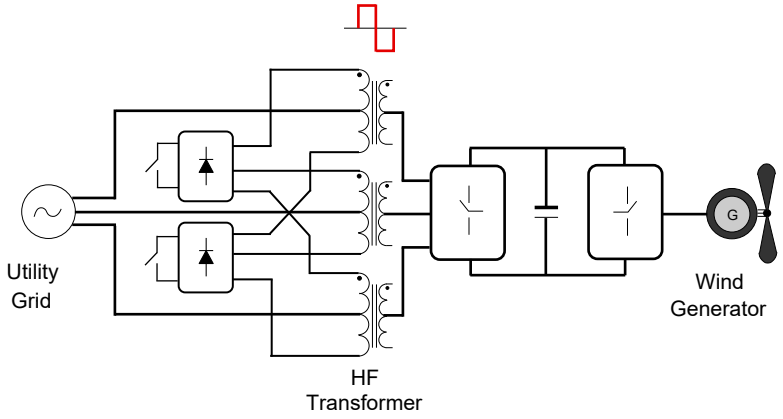


Figure 1.2: Block diagram of Reduced switch-count PET

Fig. 1.3 shows the block diagram of the PET, termed here as the Conventional PET being investigated at one of NSFs Engineering Research Centers [11, 12]. These are made using back-to-back connected voltage source converters (VSC) shown in Fig. 1.3, which are well documented in literature. In this scheme, the VSC generates high-frequency square waveform voltages that are applied to an HFT. The secondary side has a low voltage converter to synthesize adjustable magnitude and low frequency voltages. The high voltage utility side is made up of 2-level or 3-level power electronic converters using latest high voltage wide-band gap devices. This topology is very attractive to interface both medium voltage AC (or DC) grid with low voltage renewables and does not pose any problems with commutation of leakage energy in the high frequency transformers.

Limitations of Conventional PETs: A back-to-back connected 2-level converter (with

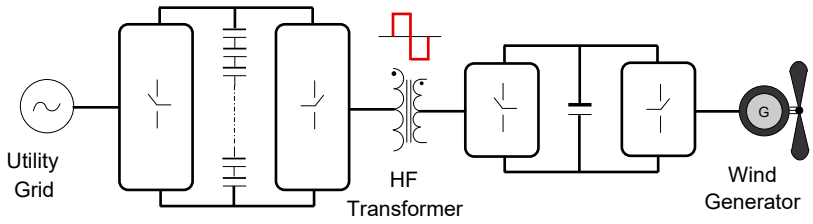


Figure 1.3: Block diagram of Conventional PET

just one leg) is shown interfacing the high-frequency transformer on one side and the grid on the other in Fig. 1.4. It has limitations described as follows for extending its application beyond 11 kV and even more so to 34.5 kV:

(a) Because of high voltages, semiconductor devices and capacitors need to be connected in series as shown in Fig. 1.4, causing additional losses in the circuitry needed to make them share blocking-voltages equally [22, 23, 24, 25].

(b) The high-frequency transformer is subjected to high dV/dt (rate of change of voltage) square waveform voltages as shown in Fig. 1.4, severely stressing the transformer insulation and causing Electro-Magnetic Interference (EMI), which can lead to spurious signals and failures in the control circuitry.

(c) The harmonics in voltages/currents at the multiples of the switching-frequency result in additional power losses in the transformer core and the windings,

(d) The 2-level or 3-level VSC generates voltages that are not perfectly sinusoidal and the unwanted voltage components require large grid-side filters which occupy a significant amount of space and have a lower lifetime,

(e) It is not modular and hence reliability is a concern.

To extend application to higher voltages like 34.5 kV, a modular structure as shown in Fig. 1.5 has to be used to improve system reliability and easy scalability [13, 14, 15]. Such topologies use the Conventional PET structure as a building block and connect them in series on the high voltage side (utility grid) and in parallel on the low voltage side (renewables, motor drives). Hence depending on the voltage and power level, such systems can be easily scaled. Each module has a high frequency transformer and its

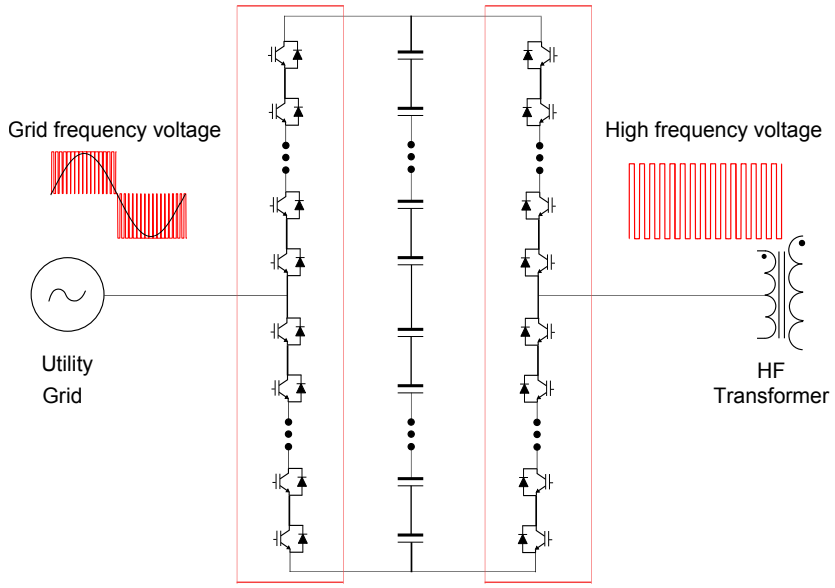


Figure 1.4: One leg of the 2-level converter interfacing the grid on one side and high frequency transformer on the other

own power electronic converter. The same topology as shown in Fig. 1.5 is identical for the three phases. However, such systems generally require large semiconductor count and magnetic material which increases the overall systems volume and cost. The high frequency transformers are still subjected to square waveform voltages and currents which have significant magnetic losses. Some of these topologies [15] are only for uni-directional power flow applications like PV to grid.

1.4 Proposed MMC based PET

To meet the requirements of utility scale voltages greater than 34.5 kV, MMCs for power electronic transformers are an attractive solution [16, 17, 18]. MMCs, which have already been developed for high voltage direct-current (HVDC) transmission applications (Trans Bay Cable project, USA [21]) have many promising features for use in a PET. These features include its scalable and compact structure by use of several submodules which can be easily replaced in case of failures, resulting in very low maintenance time [26, 27, 28]. Near-perfect sinusoidal voltage waveforms synthesized by the MMCs reduce

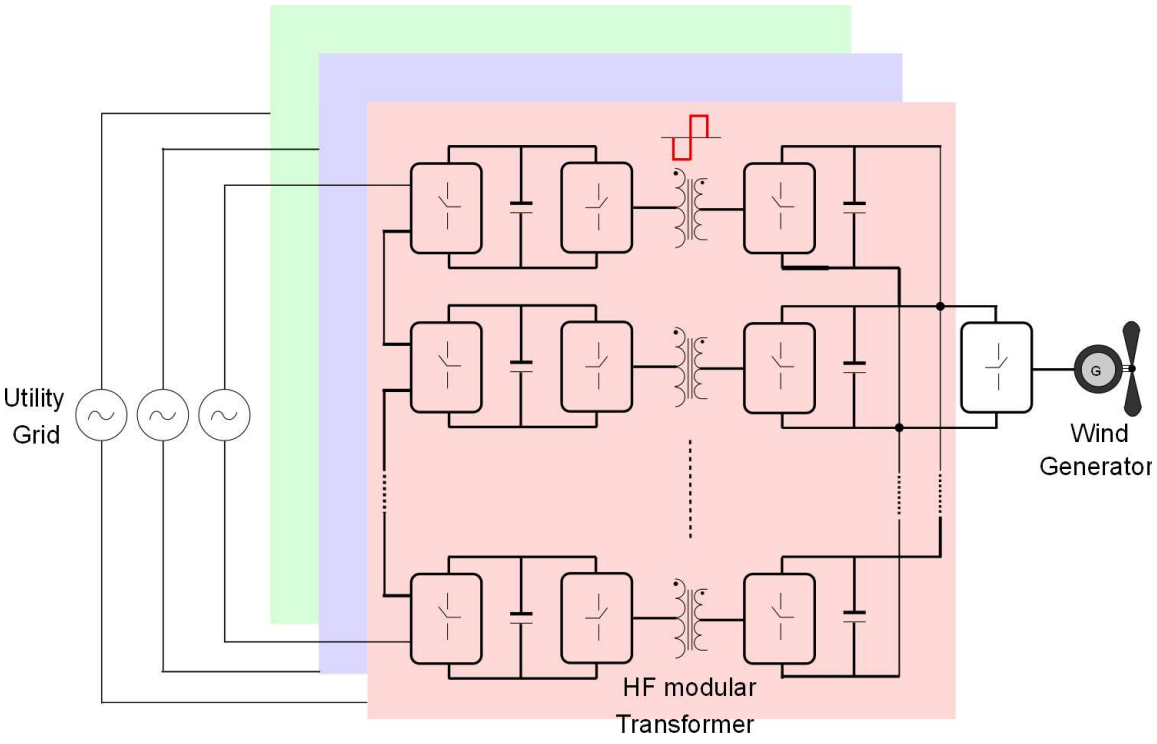


Figure 1.5: Block diagram of modular PET

the magnetic losses in the transformer and significantly reduce the grid-side filters and space they occupy.

Using MMC based-PET, the block diagram of a wind-electric system is shown in Fig. 1.6(a) and for interfacing PV plants in Fig. 1.6(b). It is formed of back-to-back connected MMCs on the high voltage utility side with a high voltage DC-link. The presence of a high voltage DC terminal can enable interfacing a DC transmission/distribution line, which is useful for offshore wind farms. This interface can be used to feed motor drives in compressors and pumps. The overall single-line block diagram for all applications is as shown in Fig. 1.7. The low voltage side power electronic converter can be an AC/DC rectifier for PV/solar integration, two-stage AC/DC/AC converter for machine drives (wind, motrs) or a direct AC/AC matrix converter. MMCs in Fig. 1.6(a) and Fig. 1.6(b) consist of a series of submodules, where each submodule itself consists of a charged-capacitor, which can be inserted or bypassed by the semiconductor switches,

thus resulting in two voltage levels. By appropriately inserting or bypassing the MMC submodules, a sinusoidal voltage can be synthesized at the ac output, reducing the need for large AC side filters.

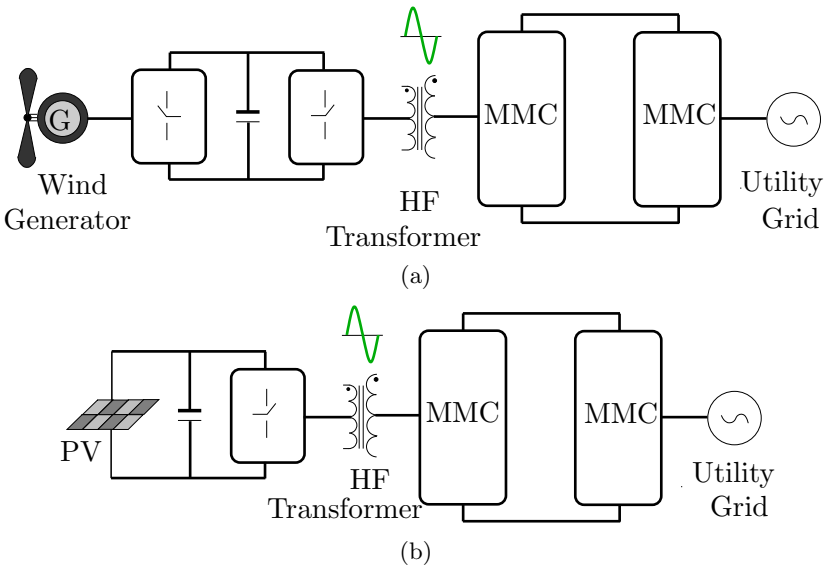


Figure 1.6: Proposed PET for (a) wind-generation; (b) PV

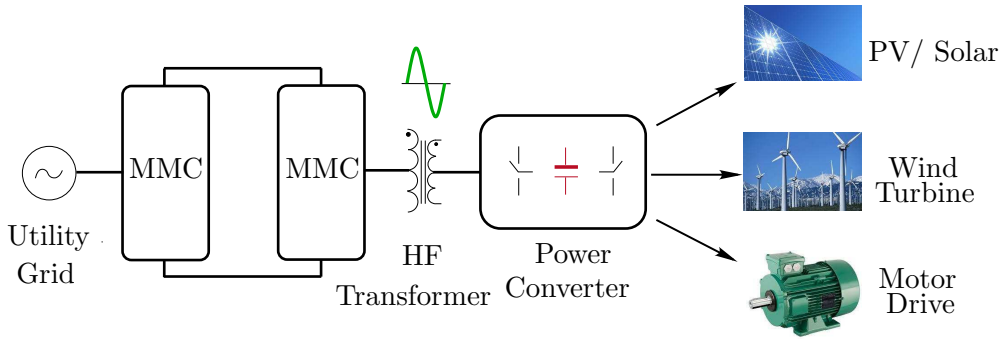


Figure 1.7: Block diagram of MMC-based PET

A simple modification is proposed to provide three voltage-levels by using split capacitances, and connecting the mid-point of the two capacitors through another switch, as shown in Fig. 1.9(b). To obtain the same number of steps in the ac-side voltage

being synthesized (ideally sinusoidal), the three-level submodule in comparison will result in the following benefits: half the number of submodules resulting in lower overall system footprint and higher efficiency with reduced conduction and switching losses. Other submodule structures have also been investigated in literature for fault handling capability, lower losses and reduced footprint [29].

The low voltage side interfacing the renewables is formed using any conventional power converter like 2-level voltage source inverter [16] or a direct AC/AC matrix converter [17] for single stage conversion. A back-to-back connected MMC (with just one leg) is shown interfacing the high-frequency transformer on one side and the grid on the other in Fig. 1.8. Compared to the conventional approach, the proposed MMC based-PET has the following advantages:

(a) Series-connection of semiconductor devices and capacitors is not required,

(b) The high-frequency transformer voltages are nearly sinusoidal as shown in Fig. 1.8, thus very low dV/dt in comparison, reducing the stress on transformer insulation and resulting in much reduced EMI,

(c) The transformer voltages and currents, being nearly sinusoidal, result in much lower power losses in the transformer core and transformer windings, respectively,

(d) Its modular structure allows a lineup of spare submodules, resulting in much higher reliability,

(e) The multilevel voltages generated at the grid side are nearly sinusoidal with very low harmonic content which significantly reduce the large grid-side filters and space they occupy,

(f) Intelligent commutation (using 3-level submodules) results in majority of switching transitions to be soft-switched, thus eliminating switching-losses associated with hard-switching, and

(g) This technology has been verified for HVDC applications at much higher voltages (200 kV) and hence can easily apply at 34.5 kV and at even higher voltages for interfacing green micro-grids to the main grid.

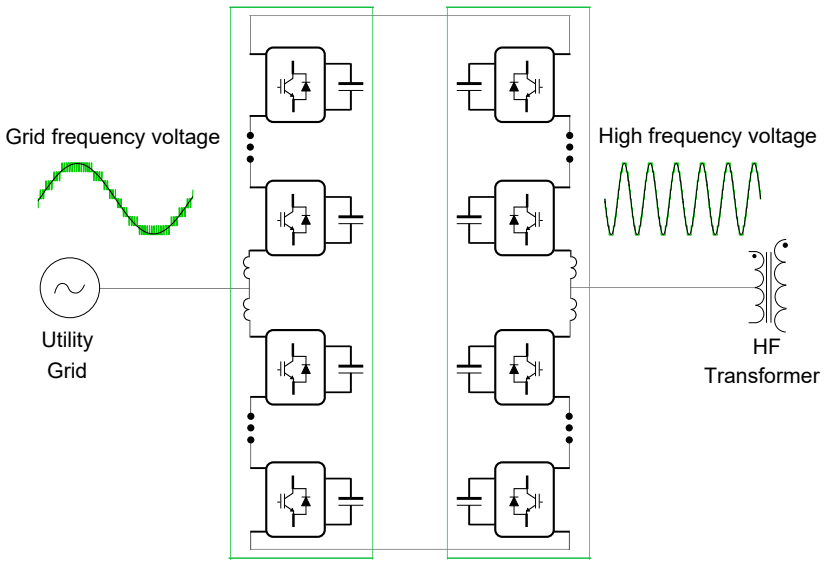


Figure 1.8: One leg of the MMC interfacing the grid on one side and high frequency transformer on the other

1.5 Outline and contributions of the thesis

The goal of this research is to make PETs practically feasible at utility scale voltages (like 34.5 kV), overcoming the challenges mentioned earlier (e.g., series-connection of semiconductor devices at high voltages), by using an MMC-based topology and achieving higher efficiency, smaller size and better reliability than the previously-proposed topologies in literature. This dissertation proposes a MMC-based PET topology that has the following advantages:

1. A new modular converter made up of multilevel submodules which have lower losses and a smaller size compared to the conventional state-of the art MMC using two-level half-bridge sub-module. This proposed MMC topology can reach double the number of voltage levels (or require half the sub-modules to yield a smaller size), has reduced voltage stress, considerable lower semiconductor losses resulting in higher efficiency, and lower protection and gate drive circuit requirements.

2. A new family of PET topologies, featuring an integrated MMC with high frequency transformer in kHz range, which would replace the bulky low frequency transformer and eliminate the disadvantages of conventional PET topologies in

literature.

3. The new PET structure has sinusoidal voltages and currents through the high-frequency transformer, thus reducing the magnetic losses of the transformer significantly and relaxing the requirement of cooling mechanisms. Also natural commutation of leakage energy is obtained which eliminates need of additional passive circuits like clamps.

4. For adjusting the motor speed in variable-speed applications, the MMC on the high-voltage side of the HFT can be controlled instead of controlling the low-voltage side converter. This results in lower output voltage distortion which translates to lower magnetic losses in the HFT, lower switching losses in low voltage converter and lower core losses in the machine.

The operation of the proposed MMC based-PET involves control of grid side MMC and control of the MMC connected to the high frequency transformer. Also control of the low voltage side converter interfacing the renewable energy source is required to meet changes in wind speeds and PV irradiation. The different chapters of this thesis address each part of the system.

1.5.1 Modular multilevel converter with 3-level submodules

A new submodule of the MMC is proposed in this thesis which can reach three voltage levels (Fig. 1.9(b)) as opposed to the conventional half-bridge submodule (Fig. 1.9(a)) which can only reach two voltage levels. This is achieved by splitting the capacitors into two and connecting the midpoint to the output terminal of the submodule through a bidirectional switch. Two variants of this submodule are presented depending on the bidirectional switch employed in the structure. Using the proposed topology, the MMC can generate the same number of voltage levels using half the number of submodules as compared to the conventional half-bridge submodule. Added advantages come in the form of reduced protection circuitry requirements, reduced semiconductor losses, lower gate drive requirements and lower bus-bar complexity.

The details of the operation of the new MMC for utility grid integration at 60-Hz is presented in Chapter 2. A hybrid modulation scheme is used for operation of the

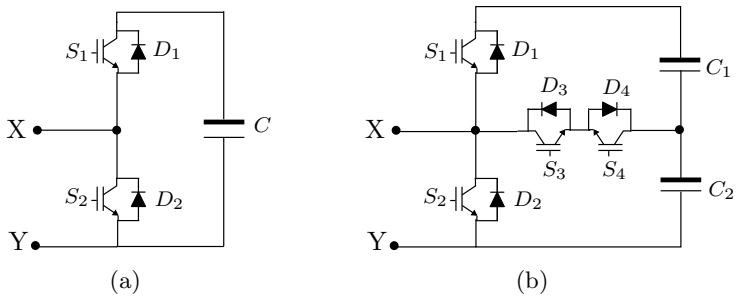


Figure 1.9: (a) 2-level submodule (b) 3-level submodule

proposed submodule based MMC. To balance the split capacitors in each submodule and the floating capacitors in all the submodules, a voltage balancing algorithm is developed. Because of ripple in the capacitor voltages, a circulating current flows between the arms of the MMC and the DC bus. This can result in additional losses and increase the ripple in the capacitor voltages. Hence a PI based circulating current control scheme is implemented based on the mathematical model of the new MMC. For practical implementation of such MMCs, challenges of commutation and precharge are addressed. Because of presence of a bidirectional switch, a 3-step commutation strategy is proposed which does not require any sense signals and results in 2/3rd of the switching transitions to be soft-switched. This reduces the effective switching losses in the proposed MMC. Effectiveness of the new submodules are validated using simulation and experimental results on a laboratory prototype.

1.5.2 Analysis of MMC for PET application

A back-to-back connected MMC interfaces the utility grid to the high frequency transformer. The MMC interfacing the high frequency transformer generates near sinusoidal voltages at relatively higher frequencies (greater than 1 kHz) compared to grid frequency (60-Hz). Analysis of modulation schemes is presented to find the best method for high frequency voltage generation. Using the same modulation strategy as described in Chapter 1, a sinusoidal voltage of 1 kHz generation will require the effective switching frequency of the semiconductor devices to be much higher (10 times and higher). This effectively would increase the switching losses of the system. Fundamental switching frequency modulation techniques like nearest level modulation are investigated for this

application. A comparison of output voltage THD using different modulation schemes at different switching frequencies is presented. Two nearest level modulation strategies are discussed and their effects on voltage balancing and circulating currents are discussed for high frequency voltage generation. It is observed that the passive components requirement (capacitors and arm inductors) is relaxed at higher frequencies and hence can be significantly smaller in size. The trade-offs of all approaches are presented with simulation and experimental results.

1.5.3 Single stage HVDC/AC power electronic transformer

Renewable energy sources like wind are generally at low voltages of 690 V. A single stage matrix converter is proposed to be used as the wind generator interfaced power converter. This is connected to the high frequency transformer which is fed from the MMC. This system builds a single stage high voltage DC to low voltage AC converter with high frequency transformer isolation. A 2-stage back-to-back voltage source inverter could also be used in place of the matrix converter. The matrix converter generates adjustable frequency voltages across the wind generator or motor drive from the high frequency voltages of the transformer. To do so, the matrix converter switches at relatively higher frequencies ($\geq$50 kHz). Being the low voltage side, this is easily possible using fast switching devices made from SiC or GaN.

At varying machine speeds, the voltage requirement is varied to keep V/f constant. A lower voltage demand on the machine is generally met by lowering the voltage transfer ratio of the machine connected converter (here the matrix converter). An advanced control approach is proposed which shifts the control of generating adjustable magnitude voltages at the machine terminals to the MMC on the high voltage side of the transformer. The machine connected matrix converter always generates the maximum voltage possible and only controls the machine frequency. This results in reduced voltage stress across the transformer, matrix converter and the machine during low speed operation as the voltage magnitude is easily reduced by bypassing many submodules of the MMC to generate a lower voltage. This would result in further reduction in losses to boost system efficiency at light load conditions. Simulation and experimental results validate the improvement to the machine in terms of voltage THD and common mode voltage switching.

1.5.4 Two-stage HVDC/AC multi-winding power electronic transformer

To interface multiple renewable energy sources, a multi-winding power electronic transformer is proposed. This makes use of a single transformer with multiple secondary windings feeding multiple renewable energy sources. The topology description with operation is discussed in detail and is validated with simulation results.

1.6 Summary

In order to enhance and accelerate the penetration of renewables for electric generation, a novel interface is investigated that can be scaled to accommodate various voltage and power levels in utility-scale renewable/storage plants and motor drives. The new interface is made of modular multilevel converter based power electronic transformers which are significantly smaller in size and weight compared to conventional 60-Hz transformers used today. It will result in substantial increase in the overall system efficiency and reliability, and lower cost. An overview of operating principle, applications with benefits of such interfaces is described and key challenges for future research are addressed in this thesis.

Chapter 2

Modular Multilevel Converters for HVDC

Modular multilevel converters have emerged as a viable solution over conventional 2-level voltage source converters (VSC) for applications in high voltage direct current (HVDC) applications. It is made up of an array of submodules comprising of semiconductor switches and floating capacitors. Due to modular structure, the converter can reach high number of voltage levels resulting in low switching frequency and near sinusoidal voltage waveforms. This chapter proposes new submodule topologies which can result in even higher voltage levels with reduced voltage stress across some switches and lower semiconductor losses. A modified modulation scheme and voltage balancing algorithm is proposed for the new topology. To suppress the circulating currents within the arms, a PI-based controller is presented based on mathematical modeling of the new MMC. For practical implementation, real world challenges of commutation and precharge are addressed. An intelligent commutation technique is proposed which results in $2/3^{\text{rd}}$ of the switching transitions to be soft switched. The working principle is validated by MATLAB/Simulink simulations and experimental results on a scaled down laboratory prototype. A comprehensive comparative analysis with other available submodule topologies is presented to show the added benefits.

2.1 Introduction

Forced commutated converters have now become an attractive choice in high voltage, high power transmission and distribution applications due to the rapid development in power semiconductor technologies and other additional advantages like full real-reactive power control, dynamic voltage regulation, black start capability, etc. This technology initially started with the voltage source converters (VSC) has now led to many new multilevel topologies with advanced features. The Modular multilevel converter proposed in 2003 has become so far the most competitive and widely sought solution for future HVDC transmission projects [28] [30]. Due to modular structure, the topology is compact and scalable to reach any number of voltage levels by simple series connection of submodules resulting in higher reliability and easy maintenance.

Over the years, researchers have studied different topologies of the MMC to improve its features. The authors in [31], [32] discuss a new MMC family based on cascaded connection of multiple bidirectional chopper cells and double star chopper cells. The different configurations of MMC chopper cell connections could be double star configuration, star configuration, delta configuration or double configuration [33]. A hybrid MMC topology was proposed in [34] which achieves soft switching of its H-bridge cells by addition of a chain-link converter in parallel, which performs wave shaping. A complete modular solution with integrated energy storage building blocks was proposed in [35]. A novel topology which connects the upper and lower bridge through a middle cell to provide voltage fluctuation suppression of the floating capacitors was discussed in [36]. IGCT based MMC using current source based H-bridge cells with an inductor instead of the capacitor as the storage element was proposed, which could improve the input and output power quality [37]. Also MMC's have been investigated with use of latest semiconductor devices like SiC JFET's [38]. However, most of the converter topologies still focused on the conventional half bridge (HB) submodule or the full bridge (FB) submodules. The clamp double (CD) submodule was proposed in [26] which is basically a series connection of two half bridge submodules with better fault handling capability. But it uses an additional switch and two diodes in normal operation which increases the semiconductor losses [39]. Three level submodule topologies like neutral point clamped (NPC) and flying capacitor (FC) were proposed in [40], [41] which showed the added

benefits of using multilevel submodule topologies for MMC.

For integrating the power electronic transformer topology as shown in Fig. 2.1, a back-to-back MMC system is used which integrates the utility grid on one side and the high frequency transformer on the other. This chapter describes the utility grid interfaced MMC generating 60-Hz voltage waveforms using novel submodule structures. Two new submodule topologies are proposed for the modular multilevel converter formed by addition of an extra bidirectional switch and center tapping the module capacitor [29]. The new topologies can reach three voltage levels like the NPC and FC topologies by addition of an extra bidirectional switch to the standard half bridge configuration. Thus, this could reduce the overall converter size making it more compact. Compared to conventional half bridge submodules that results in two output voltage levels, some of the advantages of the new proposed submodules are as follows:

- Generates double the number of voltage levels, or requires half the number of submodules as compared to standard half bridge submodules to attain the same number of voltage levels.
- The additional bidirectional switch has half the voltage stress in blocking state.
- The semiconductor losses are considerably reduced.
- Reduces complexity in gate drive circuitry.
- Requires lower protection thyristors and bypass switches and has lower bus bar complexity.

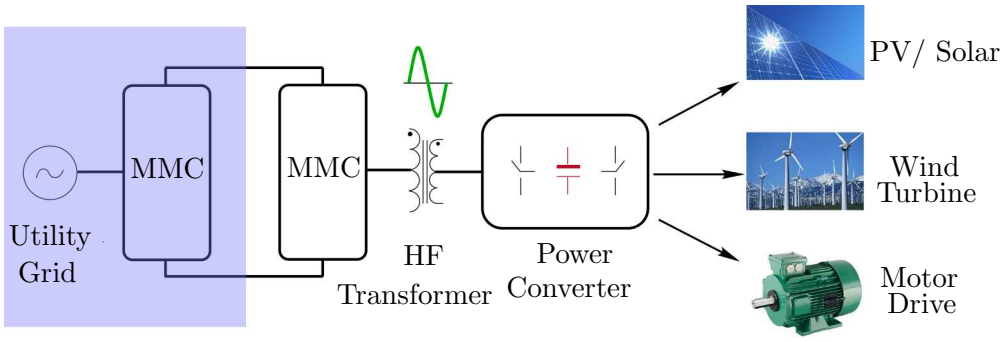


Figure 2.1: Block diagram of MMC-based PET integrating utility grid

Section 2.2 describes the overall MMC topology. The new submodule topologies with their operation is discussed in Section 2.3 in detail. The modified modulation strategy and voltage balancing algorithm using unequal capacitor sharing is proposed in Section 2.4 and 2.5, followed by mathematical model and circulating current control in Section 2.6 and 2.7 respectively. Modified 3-step commutation and precharge is described in Section 2.8 and 2.9, followed by simulation and experimental results in 2.10 and 2.11. The chapter concludes by presenting a comprehensive comparison between different existing and proposed submodule topologies in Section 2.12 and Summary in Section 2.13 respectively.

2.2 MMC Topology

The circuit topology of a modular multilevel converter is shown in Fig. 2.2(a). In this topology, three legs which generate the three-phases are made up of an array of submodules (SM) connected in series. Each leg representing a phase consists of two arms. The DC bus is connected between the upper point P and lower point N of the phases and the AC side is connected to the middle point of each phase (a, b, c). The arm connected to positive end P of the DC bus is called upper arm and the arm connected to the negative end N of DC bus is called lower arm. The sending end grid is represented by an ideal voltage source v_g which is interfaced with the MMC by converter reactance L_g for power transfer and resistance R_g to account for non-idealities. The converter reactance L_g is the combination of all line reactances, transformer leakage inductances and converter boost inductance required for power transfer between the grid and converter. The high voltage DC side is modeled by two ideal DC voltage sources ($V_{PO} = V_{ON} = V_{dc}/2$).

Each converter leg is made up of two arms consisting of n series connected submodules. A protection choke L_a is also present in each arm. It limits over-currents during any internal or external faults and also suppresses the harmonics in the arm currents due to instantaneous voltage difference between the arms and DC bus. Depending on the switching states, a submodule capacitor is either inserted or bypassed in an arm. The sum of all capacitor voltages that are inserted results in the total arm voltage v_u (upper arm) and v_l (lower arm) respectively in a leg. The difference of these arm voltages is

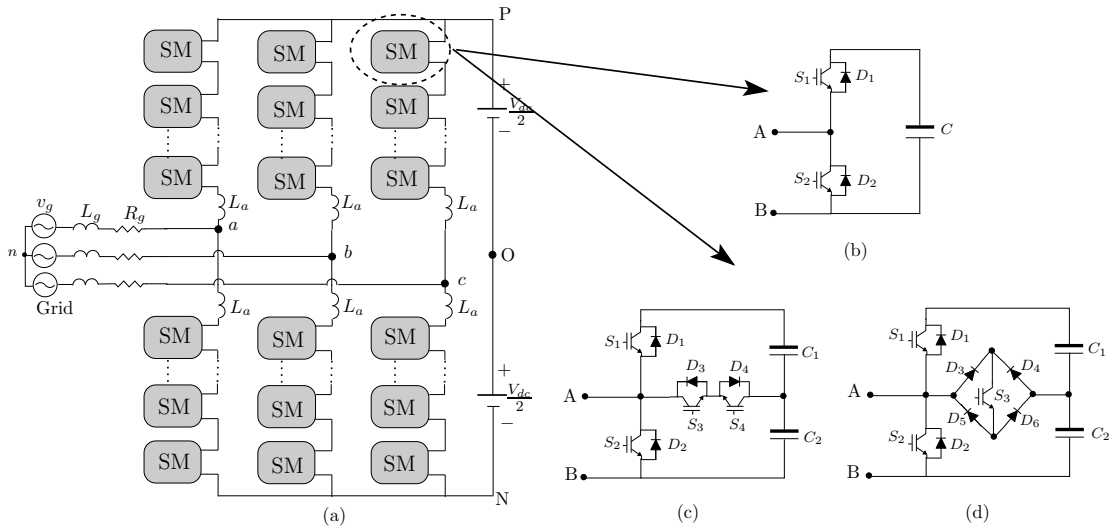


Figure 2.2: (a) Topology of the modular multilevel converter, (b) 2-level submodule, (c) 3-level submodule 1, (d) 3-level submodule 2

the synthesized output voltage of the MMC for that leg.

2.3 Submodule structure

The MMC topology as shown in Fig. 2.2(a) is made up of n series connection of submodules in each phase. By appropriate switching of the semiconductor devices in these submodules, a near sinusoidal voltage output is synthesized. The quality of the output voltage and associated losses in the system is dependent on the internal structure of these submodules. The conventional submodule is the 2-level half-bridge submodule as shown in Fig. 2.2(b). It is made up of two unidirectional switches and a floating capacitor. It results in either the capacitor voltage to be inserted or bypassed, thus resulting in two voltage levels. Two new submodule structures proposed in this dissertation are shown in Fig. 2.2(c) and Fig. 2.2(d). These result in three different voltage levels as opposed to only two voltage levels of the conventional half-bridge submodule. This section describes the operation and switching states of these submodules.

2.3.1 2-level half-bridge submodule

The half-bridge submodules are composed of a capacitor and two switching devices that have complementary signals. This module allows for two possible levels; the capacitor voltage is applied ($+V_c$) or the capacitor voltage is bypassed (zero voltage). The various states of operation for the half-bridge topology shown in Fig. 2.3 are Energization, Capacitor ON, Bypass. The Energization state occurs when no signal is applied to either gate, and depending on the current direction anti-parallel diode D_2 or D_1 will conduct. The Energization state never occurs under normal operation. The Capacitor ON state occurs when capacitor voltage needs to appear, to get this state a high signal is applied to S_1. The capacitor OFF or Bypass state is to bypass the capacitor and have zero voltage across the terminals, to get this state a high signal is applied to S_2. Depending on current direction, the IGBT or anti-parallel diode conducts as shown in Fig. 2.3.

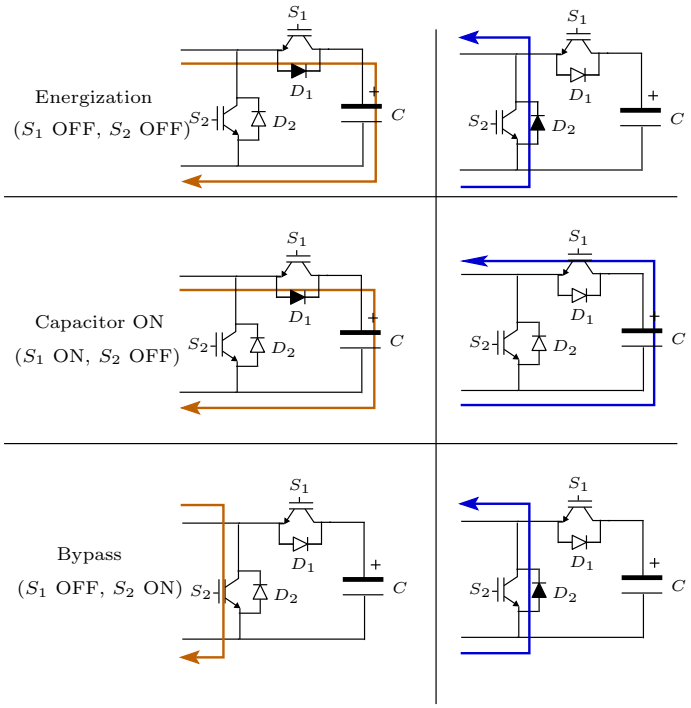
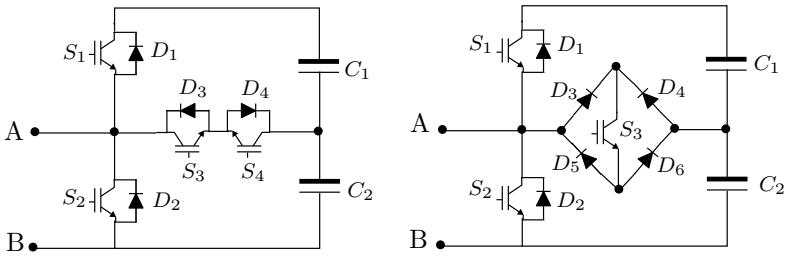


Figure 2.3: Different states of operation of the half-bridge submodule

2.3.2 3-level submodules

Two new submodule topologies proposed in this dissertation are shown in Fig. 2.4(a) and Fig. 2.4(b). It is achieved by splitting the capacitor and connecting its midpoint to the output terminal of the half-bridge submodule by an additional bidirectional switch. The structure of the bidirectional switch can take two configurations resulting in two submodule topologies. Also, the bidirectional switch in the new topology has to block a lower voltage V_{C_2} and hence can be of lower rating. The capacitor is divided into two capacitors C_1 and C_2 whose voltages are controlled to be equal. Submodule 1 is made up of two unidirectional IGBT's with anti-parallel diodes, one 4-quadrant bidirectional switch in common emitter configuration, and two capacitors. Submodule 2 uses 4 diodes and an unidirectional IGBT to form the bidirectional switch.



(a) (b)

S_1	S_2	S_3, S_4	V_{AB}
1	0	0	$V_{C_1} + V_{C_2}$
0	0	1	V_{C_2}
0	1	0	0

(c)

S_1	S_2	S_3	V_{AB}
1	0	0	$V_{C_1} + V_{C_2}$
0	0	1	V_{C_2}
0	1	0	0

(d)

Figure 2.4: (a) 3-level submodule 1, (b) 3-level submodule 2, (a) Switching states of submodule 1, (b) Switching states of submodule 2

Unlike the conventional half bridge submodules which can achieve only two voltage levels, the new topologies can switch to three voltage levels depending on the switching states as shown in Fig. 2.4(c) and Fig. 2.4(d) respectively. By properly controlling $V_{C_1} = V_{C_2} = V_C/2$, the submodule can reach 3 voltage levels, V_C, $V_C/2$ and 0. The

resulting states are called FULL-ON, HALF-ON and BYPASS state respectively. The switching states with current direction are shown in Fig. 2.5. FULL-ON state exists when switch S_1 is on. Depending on the current direction, IGBT S_1 or anti-parallel diode D_1 conducts and voltage across the submodule is equal to $V_{C_1} + V_{C_2} = V_C$. The bidirectional switch of the two topologies is represented by an ideal switch S in Fig. 2.5. HALF-ON state exists when the bidirectional switch conducts and we get half the voltage $V_C/2$ across the submodule. When switch S_2 is on, the submodule is bypassed and its the BYPASS state. Submodule 2 works in a similar manner. In HALF-ON state, the conduction takes place through two anti-parallel diodes and an IGBT. So the losses are more as compared to Submodule 1 but it eliminates the need of an additional IGBT. SiC diodes have already started commercializing and hence the losses across these two diodes can be highly minimized. There is also a state called OFF state or Energization state when all switches are off. This does not occur in normal operation of the converter and can exist only before pre-energization. The capacitors in the submodules are all precharged to $V_C/2$ before regular operation using some precharge technique. All the above states are shown in Fig. 2.5 where the current path with direction is highlighted.

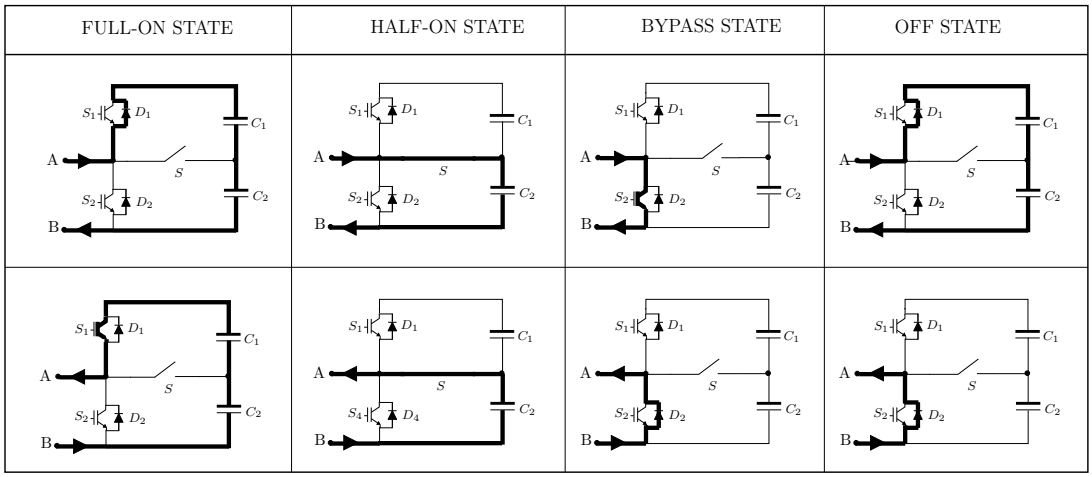


Figure 2.5: Different states of operation of the 3-level submodules

2.4 Analysis: Modulation of MMC

The most commonly used technique for generating the control signals for the switches in the submodules is by carrier based pulse-width modulation (PWM). A set of triangular waveforms called carriers are generated at switching frequency. A normalized reference sinusoidal waveform is superimposed with the carriers to generate the pulses. When the reference is higher than the carrier, a high signal is sent to the switch, otherwise a low signal is sent. Different types of carriers like phase shifted (PS), level shifted or phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD) are discussed in [42] for 2-level half bridge submodules. The most common are the phase shifted (PS) and level shifted carriers based PWM as discussed here:

Phase Shifted PWM: A phase shifted PWM scheme has all the carriers on the same level, but shifted such that they are equally spaced in one cycle (Fig. 2.6(top left)). Every other waveform is assigned to the upper submodules while the remaining are assigned to the lower submodules. For example, for 8 submdoules in a leg (submodules 1-4 in upper arm and submodules 5-8 in lower arm), 8 carriers are generated which are phase-shifted by $T_s/8$ (T_s is the switching time period). Then carrier 1 is assigned to submodule 1 in upper arm whereas carrier 2 is assigned to submodule 5 in lower arm. A sinusoidal reference is compared to these carriers to generate the switching pulses for the respective submodules. This modulation has the advantage that all submodules are used equally and it produces low harmonics even when the number of submodules is not high. The disadvantage comes in the form of switching losses, because the frequency at which submodules are turned on and off is relatively high.

Level Shifted PWM: In level shifted PWM scheme, the carrier waveforms are stacked one on top of the other as shown in Fig. 2.6(top right). Typically, each carrier is assigned to a specific submodule and when compared to the sinusoidal reference signal the submodule is either applied or bypassed. If the number of submodules is large enough then this scheme can produce a low harmonic output with a relatively low switching frequency. On the other hand when a carrier is assigned to a specific submodule then there will be submodules that will be used more than others, creating unbalance voltages in capacitors. The advantage comes in the form of relatively lower

switching losses as compared to phase-shifted PWM.

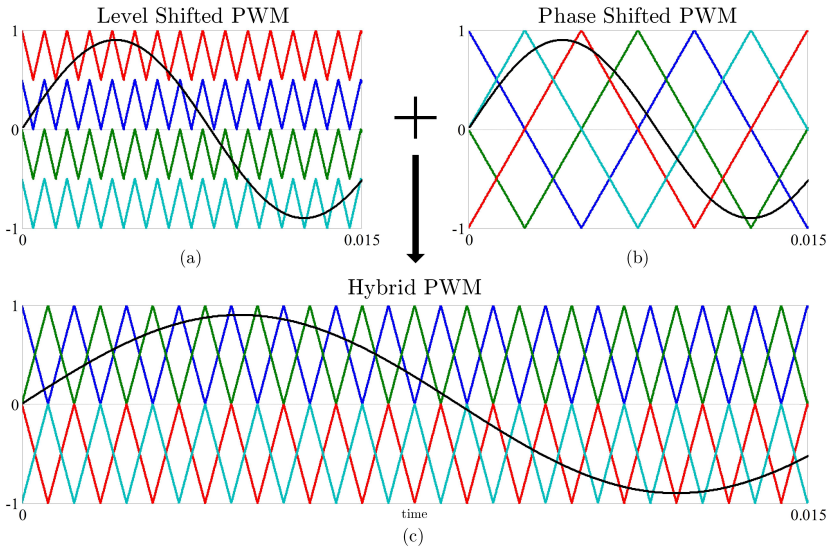


Figure 2.6: Hybrid PWM scheme

For the proposed 3-level submodules described in this dissertation, a hybrid carrier based PWM scheme is used using a combination of phase shifted and level shifted carriers called the hybrid modulation scheme, Fig. 2.6(bottom). It is composed of two sets of carrier waveforms that are level shifted between groups and phase shifted within its own group. Just like the phase shifted modulation, every other waveform from each group is assigned to the upper arm and the remaining to the lower arm. The carriers are phase shifted for the submodules and level shifted for the IGBT states inside each submodule. The three switches inside each submodule must have complementary gate signals and hence level shifted carriers do the job. By using this scheme it is possible to have two sets of capacitors where one set is used more often than the other, but within each set, the capacitors are used equally. In the proposed topology, the upper capacitor C_1 from each module can only be applied when the lower capacitor C_2 has already been applied. Each of the upper submodule capacitor will be on the level that is used less, and the lower capacitors will be on the level that is used most. The MMC synthesizes three-phase balanced output voltages given by (2.1). For each phase p ($p \in a, b, c$), two reference signals v^*_{up} and v^*_{lp} are used to synthesize the output voltage

reference v_p as given by (2.2). This is assuming a triangular carrier going from -1 to +1. A compensation term v_{zp} is present which will be discussed later in this chapter. Whenever the reference is more than the respective carrier, an active gate signal S_i is generated. The generation of output voltage with the individual voltages of submodules and arms is shown in Fig. 2.7 for a MMC with 4 submodules per leg.

$$\begin{aligned} v_a &= V_{in}\cos(\omega t) \\ v_b &= V_{in}\cos\left(\omega t - \frac{2\pi}{3}\right) \\ v_c &= V_{in}\cos\left(\omega t + \frac{2\pi}{3}\right) \end{aligned} \tag{2.1}$$

$$\begin{aligned} v_{up}^* &= \frac{-v_p}{V_{dc}} - \frac{v_{zp}}{V_{dc}} \\ v_{lp}^* &= \frac{v_p}{V_{dc}} - \frac{v_{zp}}{V_{dc}} \\ v_p^* &= \frac{v_{lp}^* - v_{up}^*}{2} \end{aligned} \tag{2.2}$$

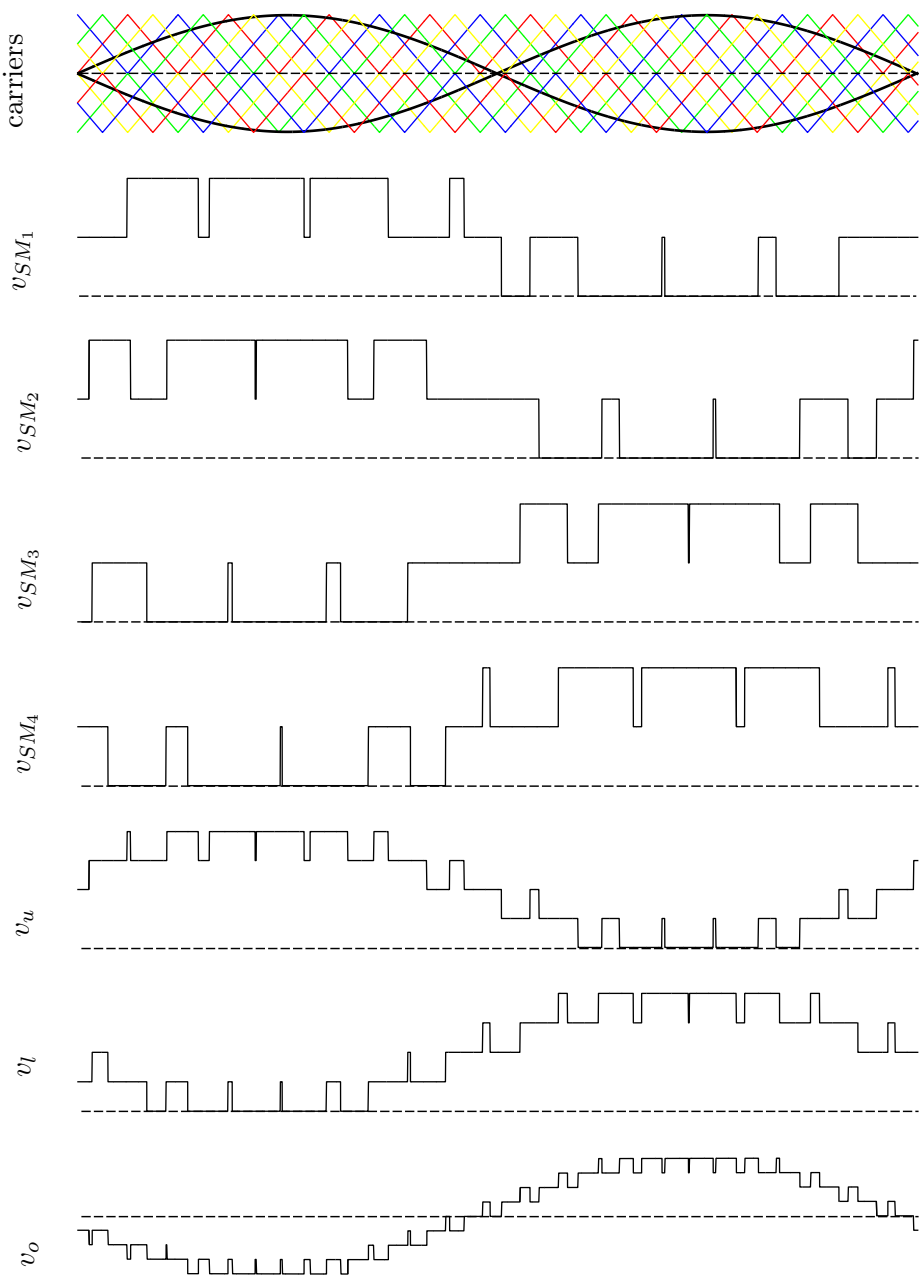


Figure 2.7: Hybrid PWM: Generation of pulses and AC voltage

The hybrid modulation results in 3 states of the MMC submodule: FULL-ON state ($S_1 = 1$), HALF-ON state (S_3, $S_4 = 1$) and BYPASS state ($S_2 = 1$). Whenever the reference signal is greater than both the upper and lower level shifted carriers, the entire submodule capacitor is inserted ($S_1 = 1$) and it is a FULL-ON state. When the reference is greater than the lower carrier but lesser than the upper carrier, it is a HALF-ON state (S_3, $S_4 = 1$). If the reference is lesser than both the upper and lower carriers, it is a BYPASS state ($S_2 = 1$) and the entire submodule is bypassed. Based on this modulation scheme, unequal capacitance division of the two capacitors $C_1 = C/3$ and $C_2 = 2C/3$ is used which can balance the capacitor voltages naturally in ideal conditions. This is chosen such that the voltage across the two capacitors is maintained constant ($V_C = Q/C = i.t/C$). Here Q is the charge across the capacitor, i is the current and t is the charging/discharging time. As seen from Fig. 2.8(a), both capacitors C_1 and C_2 are charged/discharged in FULL-ON state. In HALF-ON state, again capacitor C_2 is charged/discharged as shown in Fig. 2.8(b). Since C_2 would be charged or discharged in both the FULL-ON and HALF-ON states for double the time t, its capacitance value is chosen to be double of C_1. Since each set is used equally and the lower capacitors are larger, the voltage of all capacitors gets somewhat balanced. In real life situations, when capacitors degrade or their voltages fluctuate due to disturbances, a voltage balancing technique is proposed that maintains them at nominal values.

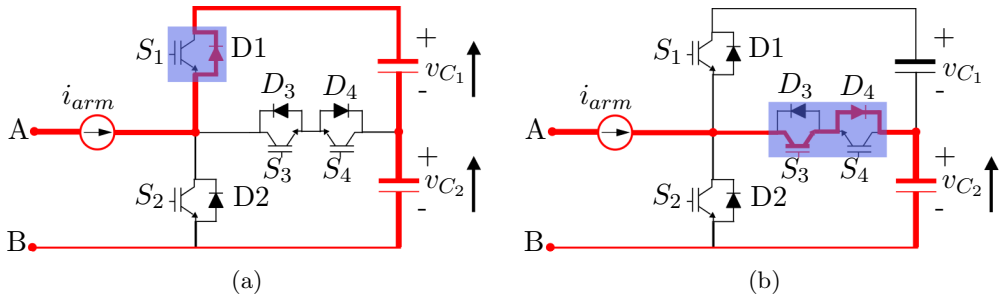


Figure 2.8: Charging/Discharging of submodule capacitors in (a) FULL-ON state (b) HALF-ON state

2.5 Capacitor Voltage Balancing

A modular multilevel converter has floating capacitors in each of its submodules. An important challenge in every MMC is voltage balancing of these floating capacitors. The voltages of individual capacitors in a submodule must be equally balanced for proper operation of the converter. Many voltage balancing techniques have been proposed in literature for the conventional existing half-bridge submodule based MMC topology. Voltage balancing based on phase shift carrier based modulation [43] and improved phase disposition PWM with selective loop bias mapping [44] have been presented. Capacitor voltage balancing using phase voltage redundant states is presented in [45]. References [33] [46] add a balancing modulation term in each cell of the MMC. In [47], voltage balancing control uses a 2-stage process to first control DC voltages inside each arm and then balance them between the arms. Other balancing techniques using more complex predictive control strategies based on cost function minimization is discussed in [48]. Reduced switching frequency voltage balancing uses the sorting algorithm [49]. Mathematical modeling has been used to derive multi-loops for control structure [50] and to analyze the limits to capacitor voltage balancing [51]. Improved voltage balancing techniques have also been proposed for other types of MMC like in a hybrid MMC using chain-link cells for soft switching [52] and a new MMC which connects the upper and lower cell through a middle cell [36]. Voltage balancing for half-bridge cells is extended for neutral point clamped and flying capacitor submodules in [40] [41].

This section presents the capacitor voltage balancing technique based on a hybrid PWM strategy for this new modular multilevel converter with 3-level submodules [53]. In the new MMC topology, the submodule has the main capacitor split into two capacitors that also need to be balanced at equal voltages. The modulation block generates ideal gate signals S_i for the IGBTs telling how many submodules and corresponding capacitors need to be inserted in the upper arm and lower arm respectively. Regardless which submodule capacitor is inserted, as long as the appropriate number is maintained, the output voltage synthesis happens correctly. This is made use of in a hysteresis kind of control to obtain capacitor voltage balancing. The entire control system block diagram is shown in Fig. 2.9. The voltage balancing control block assigns the ideal pulses generated from modulation block to the appropriate submodule of the MMC so as to

maintain nominal capacitor voltages across all submodule capacitors.

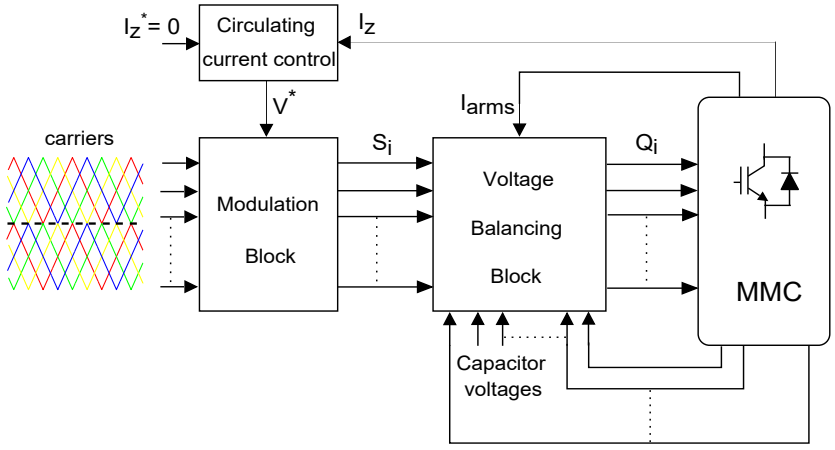


Figure 2.9: MMC control blocks

The idea is to use the capacitors with the highest voltage when the MMC is on a discharging state, and use the capacitors with the lowest voltage when it is on a charging state. Unequal capacitor values of $C_1 = C/3$ and $C_2 = 2C/3$ are used to balance the charge. Depending on the ideal pulses S_i generated from the hybrid modulation, the number of submodules operating in FULL-ON state, HALF-ON state and BYPASS state is known. The voltage balancing control block now assigns the actual gate pulses Q_i to those submodules and capacitors such that the voltages are all nominally maintained constant. To do this, all the lower capacitor voltages V_{C_2} and total submodule voltage $V_{C_1+C_2}$ is monitored and is a feedback to the controller. Since in FULL-ON state, both upper and lower capacitors are charged/discharged, the total submodule voltage $V_T = V_{C_1+C_2}$ is monitored. For the transitions between HALF-ON and BYPASS state, only $V_L = V_{C_2}$ is required. To determine when a capacitor is added or removed, the interceptions between the triangular carrier waveforms and the reference voltage are noted. If the reference voltage becomes lesser than a carrier then remove a capacitor and vice-versa. The direction of arm current $\overrightarrow{I}_{arm}$ is measured to know if the MMC is on a charging state or discharging state. If the current is going into the capacitor then the MMC is in a charging state, whereas if the current is coming out of the capacitor the MMC is on a discharging state.

The balancing algorithm is shown by a state flow diagram in Fig. 2.10. In the 3-level

submodule there are two ways to add a voltage level- either in the FULL-ON state or the HALF-ON state. Thus there are two branches to adding the module capacitors and it is decided depending on the capacitor voltages. For a transition to HALF-ON state, the module with lowest $V_L = V_{C_2}$ is inserted. If the modulation requires a FULL-ON state, two possibilities arise: it is the module with lowest $V_T = V_{C_1+C_2}$ or two of the modules with lowest V_{C_2}. Hence, during addition of a FULL-ON state, the controller can add two modules with HALF-ON states if need arises, this gives it another degree of freedom to balance the neutral point within the submodules. Mathematically it is shown in (2.3) for one case when a capacitor needs to be inserted and a charging current is sensed, then the capacitor with the minimum voltage is inserted but turning the corresponding switch ON.

$$S_i = 1, \ \overrightarrow{I}_{arm} \geq 0 \tag{2.3}$$
$$\Rightarrow \quad \text{Calculate } x = \{k : Q_k = 0, V_{ck} = \min(V_{cj}), \ k = 1, 2, ..., n, j = 1, 2, ..., n\}$$
$$\Rightarrow \quad Q_x = 1$$

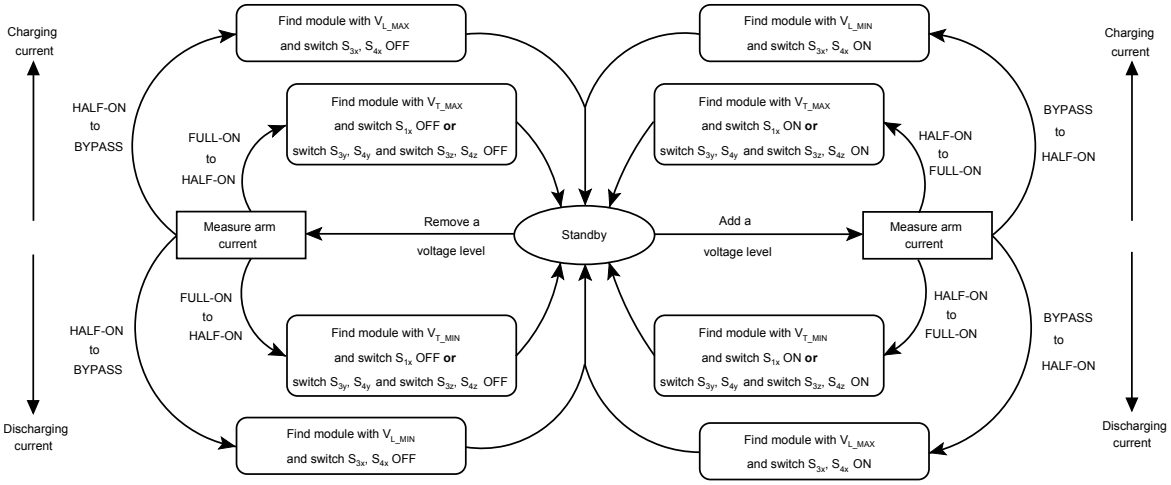


Figure 2.10: State flow representation of voltage balancing algorithm

2.6 Mathematical model

The mathematical modeling of the MMC with n submodules based on differential equations is presented in this section. This is based on the work done for conventional half-bridge submodule based MMC [54, 55, 56]. This can be useful in developing closed loop control of the system and also in simulating a system with very high number of submodules. Also the model can estimate the capacitor voltages from the switching signals which can be used by the voltage balancing algorithm. This could save placing sensors across each capacitor to monitor its voltage at all times. The MMC single phase diagram is shown in Fig. 2.11.

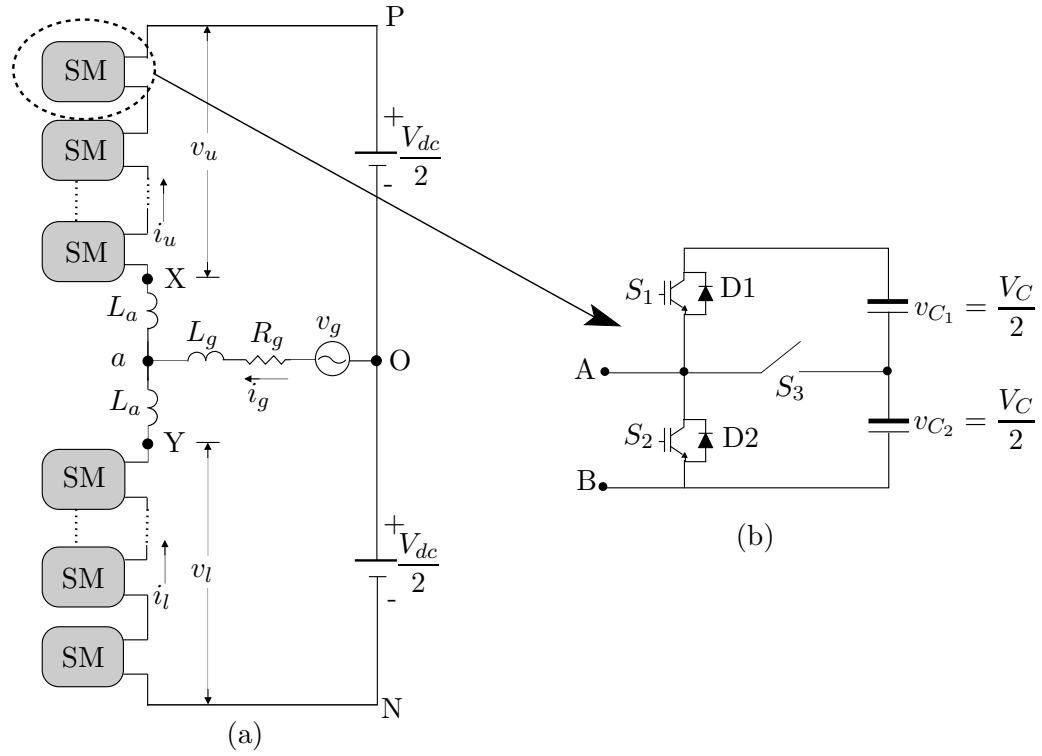


Figure 2.11: Per-phase circuit of MMC for mathematical modeling

The voltage between different points of the circuit of Fig. 2.11 which depends on the submodule states is calculated, where n refers to the total number of submodules

per phase.

$$v_{XO} = \frac{V_{dc}}{2} - v_u \tag{2.4}$$

$$v_{YO} = -\frac{V_{dc}}{2} + v_l \tag{2.5}$$

$$v_u = \sum_{i=1}^{\frac{n}{2}} (v_{C_2} S_{2i} + (v_{C1} + v_{C2}) S_{1i}) \tag{2.6}$$

$$v_l = \sum_{i=\frac{n}{2}+1}^{n} (v_{C_2} S_{2i} + (v_{C1} + v_{C2}) S_{1i}) \tag{2.7}$$

$$\begin{aligned} v_{XY} &= v_{XO} - v_{YO} \\ &= V_{dc} - v_u - v_l \end{aligned} \tag{2.8}$$

From Fig. 2.11, the arm currents fulfill the equation (2.9) and the average current along the phase i_z is defined as the half of the two arm currents (2.10). The individual arm currents depends on the circulating current i_z and the grid current i_g. From (2.9) and (2.10), equations (2.11) is obtained and using these, the voltage of the arm inductances (2.12) and (2.13) are calculated.

$$i_u - i_l = i_g \tag{2.9}$$

$$i_z = \frac{i_u + i_l}{2} \tag{2.10}$$

$$\begin{aligned} i_u &= i_z + \frac{i_g}{2} \\ i_l &= i_z - \frac{i_g}{2} \end{aligned} \tag{2.11}$$

$$v_{Xa} = -L_a \frac{di_u}{dt} = -L_a \frac{di_z}{dt} - \frac{L_a}{2} \frac{di_L}{dt} \tag{2.12}$$

$$v_{Ya} = -L_a \frac{di_l}{dt} = L_a \frac{di_z}{dt} - \frac{L_a}{2} \frac{di_L}{dt} \tag{2.13}$$

The equivalent Thevenin circuit of the converter from the point of view of the load is shown in Fig. 2.12. Thevenin inductance L_{th} is the parallel combination between the two arm inductances and Thevenin voltage (V_{th}) is the voltage between a and O terminals without connecting the load, i.e., when i_g current is zero. From (2.12) and (2.13), it could be noticed that under this condition ($i_g = 0$) and taking into account that the two arm inductors have the same value ($L_u = L_l = L_a$), the voltage drop is equal in both components. Including this equality, the Thevenin voltage (2.15) is obtained.

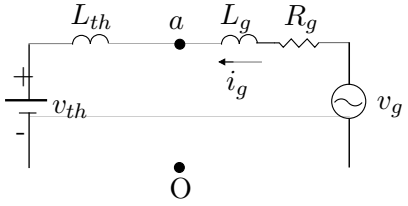


Figure 2.12: Thevenin equivalent circuit of MMC

$$L_{th} = L_a // L_a = \frac{L_a}{2} \tag{2.14}$$

$$\begin{aligned} v_{th} &= v_{aO} = v_{aX} + v_{XO} = v_{aY} + v_{YO} \\ &= -\frac{v_{XY}}{2} + v_{XO} = \frac{v_{XY}}{2} + v_{YO} \\ &= -\frac{V_{dc}}{2} + \frac{v_u + v_l}{2} + \frac{V_{dc}}{2} - v_u \\ &= \frac{v_l - v_u}{2} \end{aligned} \tag{2.15}$$

(2.16) is deduced from Kirchhoffs laws applied to the circuit in order to get the equations of the currents i_u, i_l and i_g. Putting in order the expression, the differential equation of the grid current results:

$$
\begin{aligned}
0 &= v_{th} + L_{th}\frac{di_g}{dt} + L_g\frac{di_g}{dt} + i_g R_g \qquad (2.16)\\
\Rightarrow \frac{di_L}{dt} &= -\frac{1}{L_L + \frac{L_a}{2}}(v_{th} + i_L R_L)\\
&= -\frac{2}{L_a + 2L_L}(v_{th} + i_L R_L)\\
&= -\frac{2}{L_a + 2L_L}\left(\frac{v_l - v_u}{2} + i_L R_L\right)\\
&= -\frac{1}{L_a + 2L_L}\left(\frac{v_l - v_u}{2} + i_L R_L\right)
\end{aligned}
$$

The expression which models the current circulating along the upper arm i_u depends on the voltage at the inductor terminals. It is achieved as shown in (2.17). The same way, the current along the lower arm i_l is obtained, this time as shown in (2.18).

$$
\begin{aligned}
\frac{di_u}{dt} &= -\frac{v_{Xa}}{L_a} \qquad (2.17)\\
&= -\frac{v_{aO} - v_{XO}}{L_a}\\
&= \frac{1}{L_a}\left(v_{th} + L_{th}\frac{di_L}{dt} - \frac{V_{dc}}{2} + v_u\right)\\
&= \frac{1}{L_a}\left(\frac{v_l - v_u}{2} + \frac{L_a}{2}\frac{di_L}{dt} - \frac{V_{dc}}{2} + v_u\right)\\
&= \frac{1}{L_a}\left(\frac{v_l + v_u}{2} + \frac{L_a}{2}\frac{di_L}{dt} - \frac{V_{dc}}{2}\right)
\end{aligned}
$$

$$
\begin{aligned}
\frac{di_l}{dt} &= -\frac{v_{Ya}}{L_a} \qquad (2.18)\\
&= -\frac{v_{YO} - v_{aO}}{L_a}\\
&= \frac{1}{L_a}\left(-v_{th} - L_{th}\frac{di_L}{dt} - \frac{V_{dc}}{2} + v_l\right)\\
&= \frac{1}{L_a}\left(-\frac{v_l - v_u}{2} - \frac{L_a}{2}\frac{di_L}{dt} - \frac{V_{dc}}{2} + v_l\right)\\
&= \frac{1}{L_a}\left(\frac{v_l + v_u}{2} - \frac{L_a}{2}\frac{di_L}{dt} - \frac{V_{dc}}{2}\right)
\end{aligned}
$$

The conducting pulses for upper and lower submodules are opposite, so that, the equations which define the voltage in the capacitors is also different, (2.19)(2.20) for the upper ones and (2.21)(2.22) for the lower ones.

Upper arm ($i = 1$ to $i = \frac{n}{2}$)

$$\begin{aligned} C_{2i}\frac{dv_{C_{2i}}}{dt} &= -i_u S_{2i} \\ \Rightarrow \frac{dv_{C_{2i}}}{dt} &= -\frac{1}{C_{2i}} i_u S_{2i} \end{aligned} \tag{2.19}$$

$$\begin{aligned} (C_{1i}+C_{2i})\frac{dv_{C_{1i}+C_{2i}}}{dt} &= -i_u S_{1i} \\ \Rightarrow \frac{dv_{C_{1i}+C_{2i}}}{dt} &= -\frac{1}{C_{1i}+C_{2i}} i_u S_{2i} \end{aligned} \tag{2.20}$$

Lower arm ($i = \frac{n}{2} + 1$ to $i = n$)

$$\begin{aligned} C_{2i}\frac{dv_{C_{2i}}}{dt} &= -i_l S_{2i} \\ \Rightarrow \frac{dv_{C_{2i}}}{dt} &= -\frac{1}{C_{2i}} i_l S_{2i} \end{aligned} \tag{2.21}$$

$$\begin{aligned} (C_{1i}+C_{2i})\frac{dv_{C_{1i}+C_{2i}}}{dt} &= -i_l S_{1i} \\ \Rightarrow \frac{dv_{C_{1i}+C_{2i}}}{dt} &= -\frac{1}{C_{1i}+C_{2i}} i_l S_{2i} \end{aligned} \tag{2.22}$$

2.7 Circulating Current Control

Each phase of the MMC is made up of series connection of submodules which are connected in parallel across the high-voltage DC side as shown in Fig. 2.13. Since the floating capacitors have a ripple voltage which do not sum up to be exactly equal to the DC bus, circulating currents flow in the arms between the individual phase units and the DC bus [57]. The converter arm inductors can damp these currents to a very low level and make them controllable by means of appropriate methods. These circulating currents do not reflect in the converter output currents given by the difference of the arm currents (2.23). On the other hand, the sum of these arm currents given

by (2.24) has a dominant 2nd harmonic component. The individual arm currents i_{up} and i_{lp} have this circulating current flowing between the arms and the DC bus (2.25). Because of these additional components in arm currents, the resultant RMS of the current flowing through the floating capacitors in the submodules is higher resulting in a higher capacitor voltage ripple. With a higher capacitor voltage, the THD in generated output voltage is higher which results in poor waveform quality and could affect system stability. Also, the extra currents results in additional losses in the converter arm inductors and semiconductor devices. Hence a need for circulating current suppression control is of need in MMCs. Various techniques have been proposed in literature for the conventional half-bridge submodule based MMC [33, 48, 49, 58]. Based on the abc to dq transformation at 2nd harmonic frequency, the three phase circulating currents are converted to DC quantities and then suppressed using PI controllers [49]. This section presents a control strategy based on [49] to suppress the circulating currents in 3-level submodule based MMC to improve efficiency and stability.

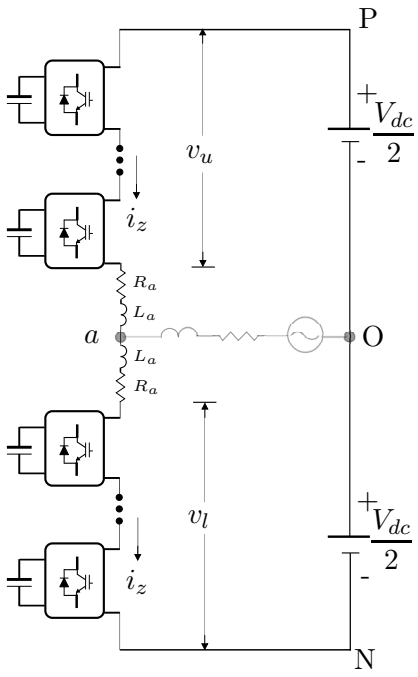


Figure 2.13: Per-phase circuit of MMC for circulating currents

$$i_{up} - i_{lp} = i_p \tag{2.23}$$

$$i_{zp} = \frac{i_{up} + i_{lp}}{2} \tag{2.24}$$

$$\begin{aligned} i_{up} &= i_{zp} + \frac{i_p}{2} \\ i_{lp} &= i_{zp} - \frac{i_p}{2} \end{aligned} \tag{2.25}$$

A simple control system design with the plant model looks like Fig. 2.14. The plant to be controlled consists of the arm inductance L_a and resistance R_a. The upper arm, lower arm and converter output voltages are given by (2.26). Using Kirchoffs voltage law (KVL), taking a loop from the positive DC bus through the upper and lower arm and negative DC bus, the equation (2.27) can be obtained. Thus a voltage v_{zp} can be applied across the arm inductor L_a and resistor R_a to control the difference in voltage between DC bus and sum of upper and lower arm voltages which results in circulating currents (2.27).

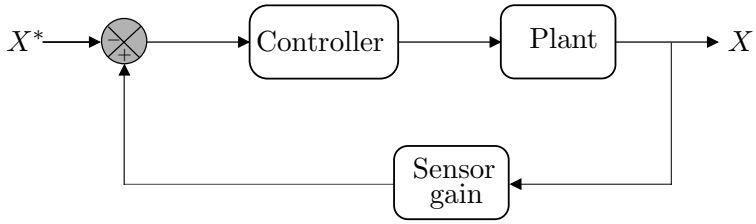


Figure 2.14: Controller design

$$\begin{aligned} v_{up} &= -v_p - v_{zp} \\ v_{lp} &= v_p - v_{zp} \\ v_p &= \frac{v_{lp} - v_{up}}{2} \end{aligned} \tag{2.26}$$

$$\begin{aligned} V_{dc} - v_{up} - v_{lp} &= 2L_a \frac{di_{zp}}{dt} + 2R_a i_{zp} \\ \Rightarrow v_{zp} = L_a \frac{di_{zp}}{dt} + R_a i_{zp} &= \frac{1}{2}\left(V_{dc} - v_{up} - v_{lp}\right) \end{aligned} \tag{2.27}$$

The circulating current have a dominant 2nd harmonic component and one-third the DC bus current (2.28). The goal of the control is to suppress these 2nd harmonic currents.

$$\begin{aligned} i_{za} &= \frac{I_{dc}}{3} + I_z \cos(2\omega t + \phi) \\ i_{zb} &= \frac{I_{dc}}{3} + I_z \cos\left(2\omega t + \frac{2\pi}{3} + \phi\right) \\ i_{zc} &= \frac{I_{dc}}{3} + I_z \cos\left(2\omega t - \frac{2\pi}{3} + \phi\right) \end{aligned} \tag{2.28}$$

From (2.27), for a three-phase system, the circulating current equations can be written as shown in (2.29).

$$\begin{aligned} L_a \frac{di_{za}}{dt} &= v_{za} - R_a i_{za} \\ L_a \frac{di_{zb}}{dt} &= v_{zb} - R_a i_{zb} \\ L_a \frac{di_{zc}}{dt} &= v_{zc} - R_a i_{zc} \end{aligned} \tag{2.29}$$

Using space vector transformation, the above equations can be converted to rotating frame which results in DC quantities as shown below in (2.30).

$$\begin{aligned} L_a \frac{di_{zd}}{dt} &= v_{zd} - R_a i_{zd} + 2\omega L_a i_{zq} \\ L_a \frac{di_{zq}}{dt} &= v_{zq} - R_a i_{zq} - 2\omega L_a i_{zd} \end{aligned} \tag{2.30}$$

Here 2ω is double the system angular frequency. To suppress the circulating currents completely, both the d-axis and q-axis components are forced to zero in the control as showin in (2.31).

$$i_{zd}^* = 0 \qquad i_{zq}^* = 0 \tag{2.31}$$

PI control is used to control the d and q axis currents and force them to follow their respective reference values. The current control regulates i_{zd} and i_{zq} at their reference values, denoted by i_{zd}^* and i_{zq}^*, by adjusting the output voltage references of

the converter as shown in (2.32). The resulting voltage reference commands v^*_{zd} and v^*_{zq} are converted back to three-phase quantities by using inverse vector transformation to result in v^*_{za}, v^*_{zb} and v^*_{zc} respectively. The total reference voltage needed to generate the output voltages of the MMC then incorporates this value (2.33) to result in circulating current suppression.

$$\begin{aligned} v^*_{zd} &= 2\omega L_a i_{zq} - \left[k_{pd} \left(i_{zd} - i^*_{zd} \right) + k_{id} \int \left(i_{zd} - i^*_{zd} \right) dt \right] \\ v^*_{zq} &= -2\omega L_a i_{zd} - \left[k_{pq} \left(i_{zq} - i^*_{zq} \right) + k_{iq} \int \left(i_{zq} - i^*_{zq} \right) dt \right] \end{aligned} \tag{2.32}$$

$$\begin{aligned} v^*_{up} &= \frac{-v^*_p}{V_{dc}} - \frac{v^*_{zp}}{V_{dc}} \\ v^*_{lp} &= \frac{v^*_p}{V_{dc}} - \frac{v^*_{zp}}{V_{dc}} \end{aligned} \tag{2.33}$$

The overall block diagram of the controller looks like as shown in Fig. 2.15.

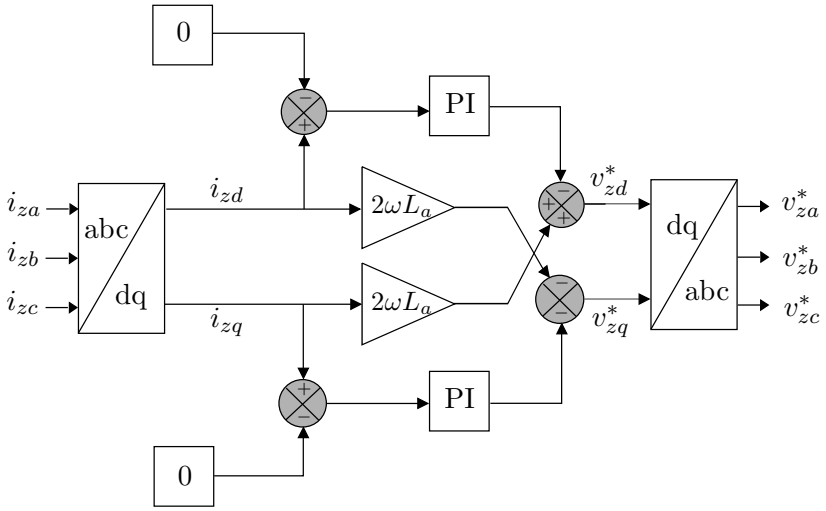


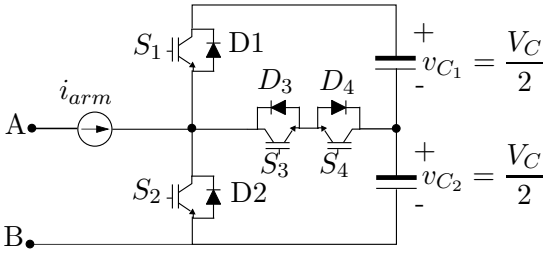
Figure 2.15: Block diagram for circulating current control

2.8 Commutation

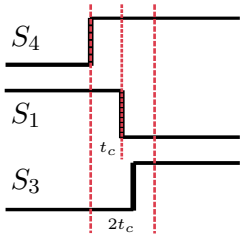
Under non-ideal conditions in hardware implementation, the transitions between switching has to have a finite time interval. For the transitions between HALF-ON and FULL-ON/BYPASS states, there is a change of switching using a bidirectional switch. An intelligent commutation strategy must be employed to permit smooth transition between switchings and also result in minimum switching losses. A reduced 4-step (as done in matrix converters) [59] can be implemented resulting in zero current switching (ZCS) in $2/3^{\text{rd}}$ of the transitions. This needs only 3 transitions as it involves 3 switches. The direction of arm current $\overrightarrow{I}_{arm}$ is a feedback for this commutation. The commutation stages are as follows:

1. Turn the passive outgoing IGBT OFF if present.
2. Turn the active incoming IGBT ON if present.
3. Turn the active outgoing IGBT OFF if present.
4. Turn the passive incoming IGBT ON if present.

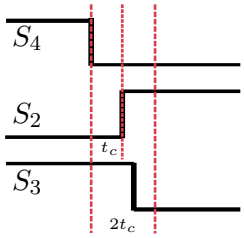
The active IGBTs imply the IGBTs that are conducting before and after the commutation and the passive IGBTs imply those that do not conduct. The outgoing IGBTs are those that are currently conducting and the incoming ones are those that are going to conduct. This type of commutation suffers from inaccuracies near the zero crossing of sensed current. Hence this section describes a reduced 3-step commutation which does not require any current sensing. Following the above steps, the truth tables for all possible transitions are shown in Fig. 2.16. In every combination, it can be observed that the 3-step commutation consists of two passive (P) states and one active (A) state. The active state is always the second step and is critical as it determines the forced commutations. The passive states only affect the natural commutations through anti-parallel diodes. If properly analyzed, it is found that one set of passive transitions do not affect the actual switch commutations and hence can be moved independently and do not affect the overall commutation process. Doing so, only one set of commutation steps is derived independent of current direction and shown by the steps marked in green in Fig. 2.16. Thus, need for sensing of arm currents is eliminated.



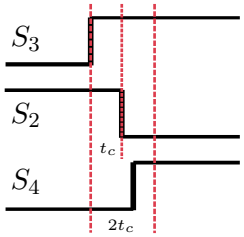
$S_1 \rightarrow S_3, S_4$	
$i_{arm} \geq 0$	$i_{arm} < 0$
(P) S_1 OFF	(P) S_4 ON
(A) S_3 ON	(A) S_1 OFF
(P) S_4 ON	(P) S_3 ON



$S_3, S_4 \rightarrow S_2$	
$i_{arm} \geq 0$	$i_{arm} < 0$
(P) S_4 OFF	(P) S_3 OFF
(A) S_2 ON	(A) S_4 OFF
(P) S_3 OFF	(P) S_2 ON



$S_2 \rightarrow S_3, S_4$	
$i_{arm} \geq 0$	$i_{arm} < 0$
(P) S_3 ON	(P) S_2 OFF
(A) S_2 OFF	(A) S_4 ON
(P) S_4 ON	(P) S_3 ON



$S_3, S_4 \rightarrow S_1$	
$i_{arm} \geq 0$	$i_{arm} < 0$
(P) S_4 OFF	(P) S_3 OFF
(A) S_3 OFF	(A) S_1 ON
(P) S_1 ON	(P) S_4 OFF

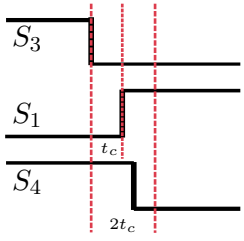


Figure 2.16: 3-step commutation truth tables with real gate signals

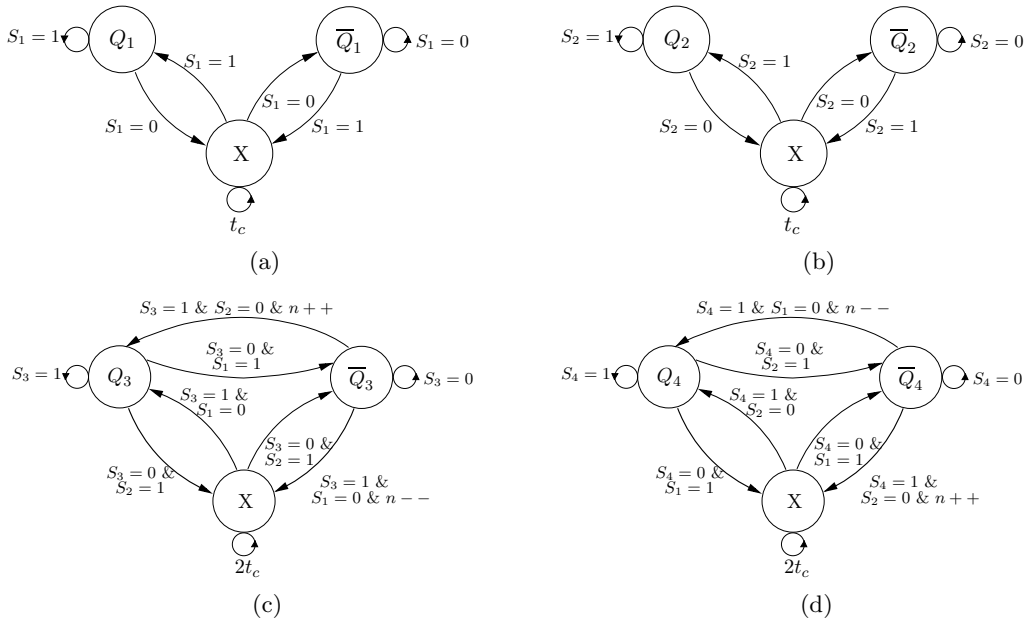


Figure 2.17: 3-step commutation state machines for (a) Switch Q1 (b) Switch Q2 (c) Switch Q3 (d) Switch Q4

The modified 3-step commutation without sensors is as follows:

1. Turn ON/OFF unidirectional switches after a time delay of t_c always.
2. While switching to a higher voltage level $(n++)$, turn S_3 immediately ON/OFF and S_4 after a time delay of $2t_c$ always.
3. While switching to a lower voltage level $(n--)$, turn S_4 immediately ON/OFF and S_3 after a time delay of $2t_c$ always.

The state machine implementation is done for individual switches of a submodule as shown in Fig. 2.17. An example of the 3-step commutation is shown for a transition from FULL-ON to HALF-ON state. Fig. 2.18 shows the steps during positive current direction and Fig. 2.19 during negative current direction respectively. The current path is shown in RED and the devices which are turned ON in BLUE. Following the modified commutation strategy, safe transitions happen in both cases regardless of the current direction. The only difference is that current commutation happens in different

commutation steps depending on if its a natural commutation of forced commutation. Each transition has a finite time interval t_c which is the commutation time interval. With the proposed commutation technique, $2/3^{\text{rd}}$ of the transitions are soft switched at zero current. This results in significant reduction in switching losses.

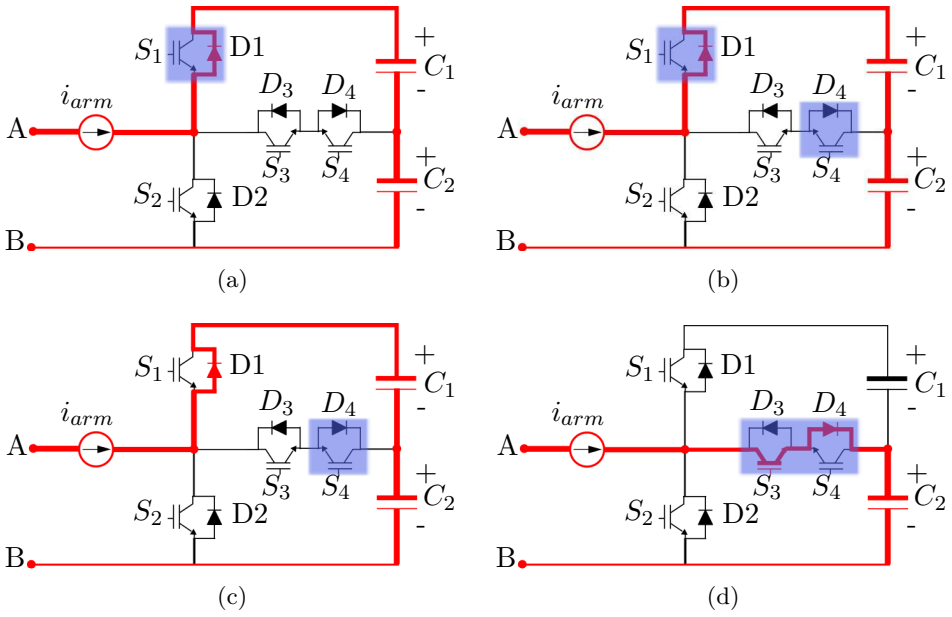


Figure 2.18: 3-step commutation transition steps from FULL-ON to HALF-ON state during positive current direction

2.9 Precharge and Startup

The MMC consists of storage elements integrated into the converter topology that are utilized during operation. These storage capacitors need to be precharged to a nominal voltage before operation starts. A simple and cost effective precharge method with a low-voltage dc source is presented in [60] and this method is afforded flexibility due to the characteristics of the boost circuit. Avoiding most of the auxiliary circuits, a PWM based charging method is demonstrated in [61] where the submodules inherent switches are used in a PWM pre-charge process along with the voltage balancing algorithm. Two closed-loop methods to pre-charge the SMs with constant charging current and less startup time is described in [62]. A self-start control strategy for the clamp

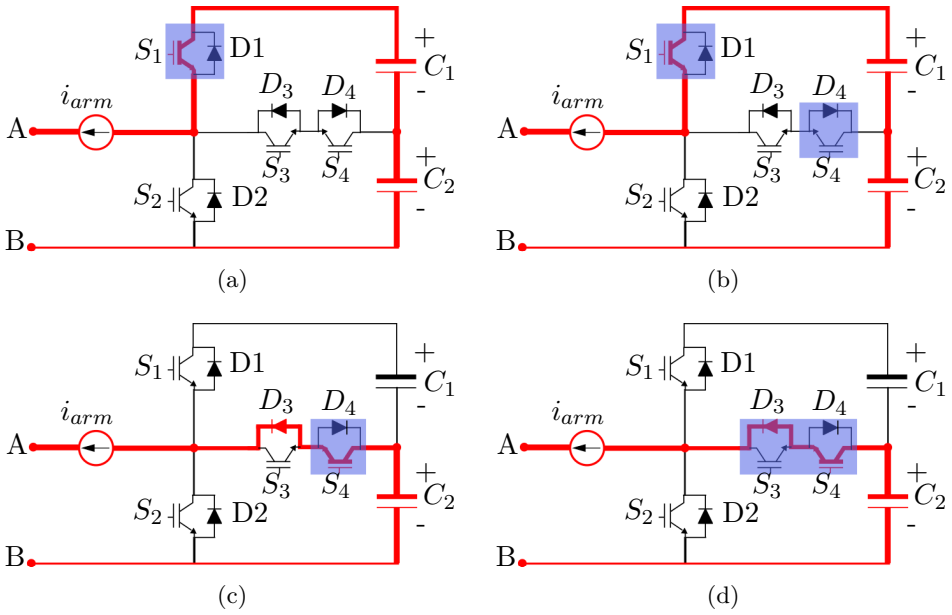


Figure 2.19: 3-step commutation transition steps from FULL-ON to HALF-ON state during negative current direction

double submodule based MMC-HVDC link is put forward in [63], in which a simple grouping sequentially controlled charge method is proposed to fully charge the capacitors in submodules and make each capacitor share sufficient stored energy. This thesis modified the PWM charging method described in [61] for the new submodules with unequal capacitance values.

2.10 Simulation Results

The MMC as shown in Fig. 2.2 is simulated with ideal switches in MATLAB/Simulink for a sending end HVDC station with parameters as shown in Table 2.1. Each leg of the 3-phase system consists of 4 submodules of the proposed 3-level structure with 2 each in the upper and lower arm respectively. The output voltage of the converter is generated by the hybrid modulation strategy as explained before. The arm currents, capacitor voltages and ideal switching signals from hybrid modulation are given as feedback to the state machine implementing voltage balancing. The reference voltage is set to generate an output voltage with modulation index $m = 1$ and power factor

$\cos\phi = 0.8$ which results in an active power of 2.75 MW. Circulating current control using PI controllers is also implemented for suppression of arm current harmonics. This section presents the simulation results in detail.

Table 2.1: Simulation for HVDC application : MMC parameters

Parameters	**Value**
Grid voltage $V_{g(LL,RMS)}$	4.16 kV
Grid inductance L_g	5 mH
DC bus voltage V_{dc}	10 kV
Submodule upper capacitor C_1	2.22 mF
Submodule lower capacitor C_2	4.44 mF
Arm inductor L_a	2.5 mH
Line frequency	60 Hz
Switching frequency	2.5 kHz

The steady state results of the MMC system with 3-level submodules is shown in Fig. 2.20, Fig. 2.21, Fig. 2.22 and Fig. 2.23. Fig. 2.20 shows the 3-phase voltage generated from the converter using 4 submodules per leg. It is clearly seen that the converter voltage reaches 9 distinct voltage levels (including zero level) using the new 3-level submodules. The levels are all of nearly equal magnitude of $V_{dc}/4 = 2500$ V each. The new topology generates double the number of voltage levels when compared to the conventional half bridge submodules, for the same number of submodules used. The generated voltage thus results in very low THD content and hence reduced filter requirements at the grid. The output current of the MMC is near sinusoidal with very low harmonic content, Fig. 2.20(middle). The line currents are sinusoidal and 120° phase shifted. The power factor angle is clearly seen between the grid voltage and current in Fig. 2.20(bottom) justifying that the converter can handle both real and reactive power flow. These waveforms are similar for both the topologies proposed earlier in Section I.

The voltage of upper and lower arms in a leg are shown in Fig. 2.21(top) and

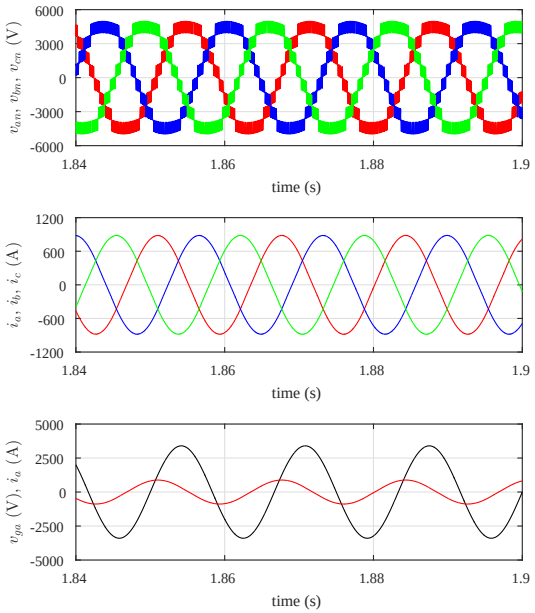


Figure 2.20: (top to bottom) Synthesized 3-phase output converter phase voltages, 3-phase line currents, grid voltage and current for phase a

2.21(second from top) respectively. As can be seen, the arm voltage reaches 5 voltage levels (including zero level) by use of 2 submodules. The output voltage generated is one-half of the difference of the arm voltages ($v_{an} = 0.5(v_{la} - v_{ua})$) as described in the Modulation Section.

The next set of results shows the steady state results of voltage balancing algorithm and circulating current control. The capacitor voltages are balanced by the use of unequal capacitances and voltage balancing algorithm. The capacitor voltages of the 4 submodules for capacitor C_1 is shown in Fig. 2.22(top). We see two distinct balanced waveforms which are the voltages for the capacitors C_1 in the upper arm and the lower arm respectively. Similarly the capacitor voltages for upper and lower arm also follow together for all capacitors C_2 in the leg as shown in Fig. 2.22(middle). The net total capacitor voltage for each submodule in a leg is also balanced which charges and discharges around the nominal voltage of 5000 V as shown in Fig. 2.22(bottom). The circulating current control using PI controllers is implemented to suppress the 2nd harmonic component present in the arms. The steady state results are shown in Fig. 2.23. It is seen that the arm currents are near sinusoidal at 60-Hz and the circulating current

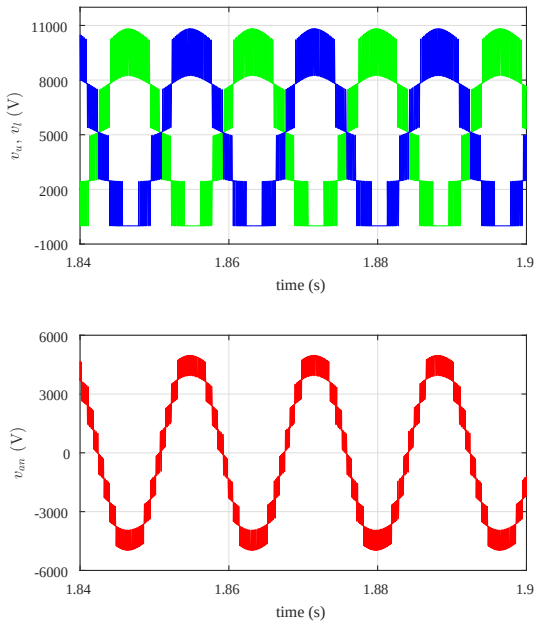


Figure 2.21: (top to bottom) Upper arm and lower arm voltages for phase a, converter output voltage for phase a

i_{az} $(= 0.5(i_{ua} + i_{la}))$ is very small in Fig. 2.23 (middle). The output line current is the difference between these arm currents $(= i_{la} - i_{ua})$ as shown in Fig. 2.23 (bottom).

A detailed analysis of voltage balancing algorithm is presented next with more results. These results are taken by adding a tolerance of $\pm 5\%$ in the capacitance values which is true in real capacitors. The initial capacitor voltages during startup are within $\pm 10\%$ of their nominal precharged voltage of 2500 V. This can happen in the absence of a well controlled precharge circuit which can result in the initial capacitor voltages to be slightly different from their nominal values. In the absence of voltage balancing algorithm, the capacitor voltages do not follow together and are unbalanced, Fig. 2.24(a). The capacitor voltages keep diverging until the system becomes unstable. The capacitor voltages are balanced by the use voltage balancing algorithm as proposed in this chapter. The steady state results are shown in Fig. 2.24(b). A transient state condition during startup is shown in Fig. 2.24(c) and Fig. 2.24(d) where the initial capacitor voltages of all capacitors were not equal. As can be seen, because of voltage balancing the unequal capacitor voltages converge to the nominal voltage level.

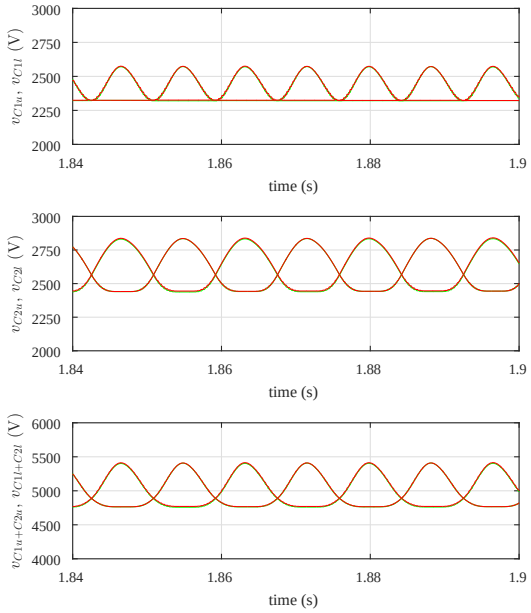


Figure 2.22: (top to bottom) Capacitor voltages in upper arm and lower arm for v_{C1}, v_{C2} and v_{C1+C2}

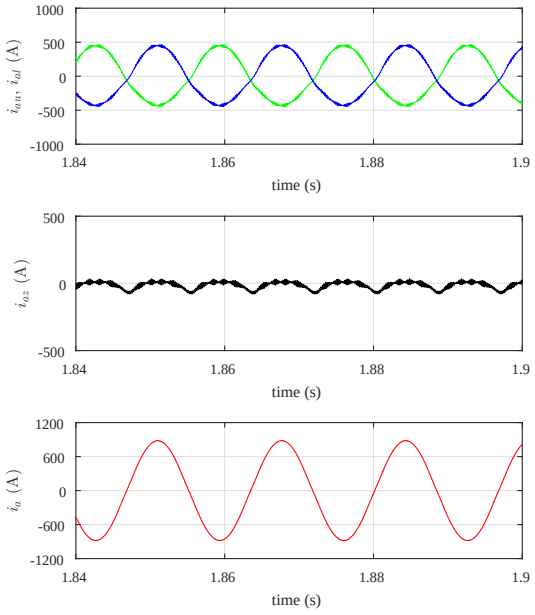


Figure 2.23: (top to bottom) Upper arm and lower arm currents for phase a, circulating current in phase a leg, phase a output line current

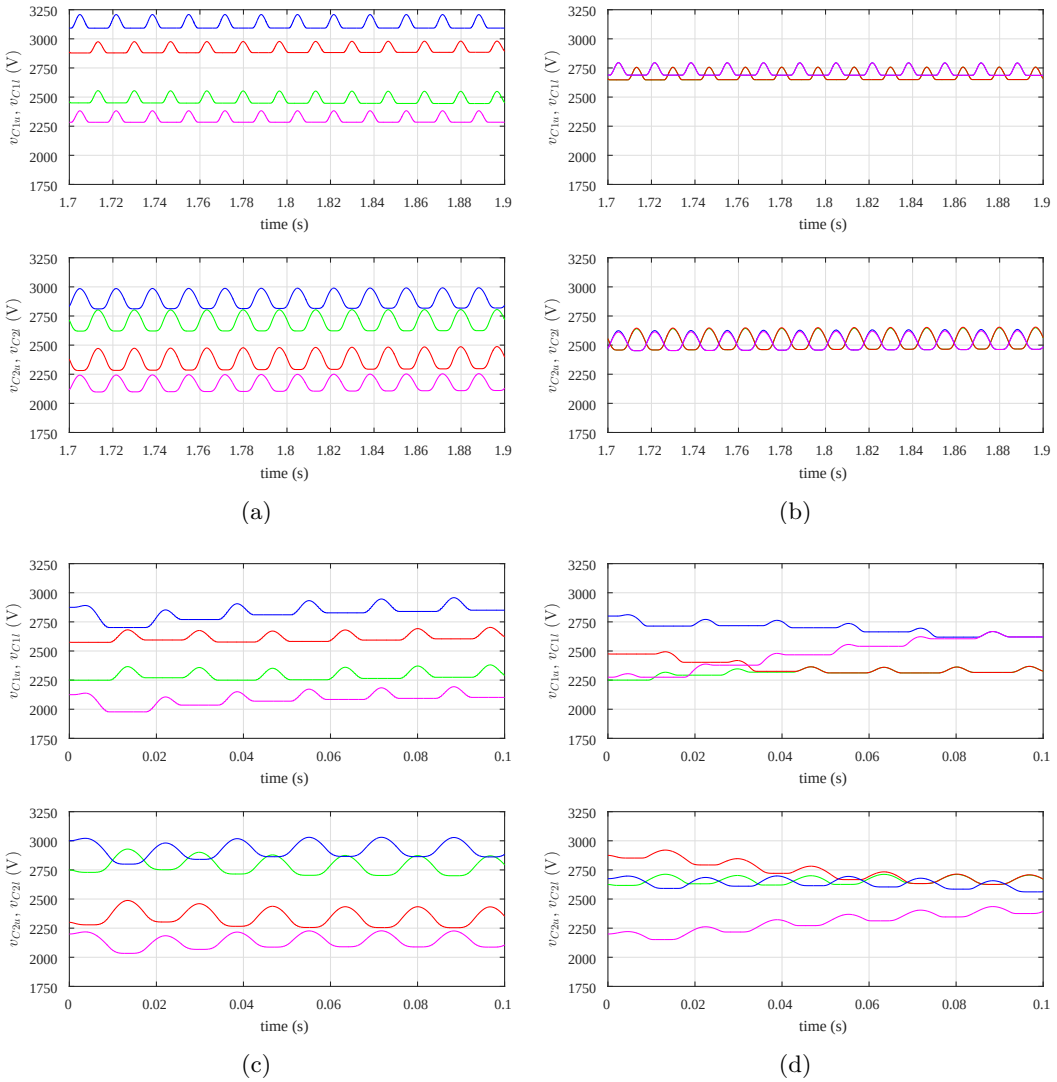


Figure 2.24: Capacitor voltages in upper arm and lower arm (upper) v_{C1} and (lower) v_{C2}: (a) during steady state without balancing algorithm (b) during steady state with balancing algorithm (c) during startup transient state without balancing algorithm (d) during startup transient state with balancing algorithm

Fig. 2.25(a) and Fig. 2.25(b) shows the results in the absence and presence of circulating current control. As can be seen there is dominating lower order harmonics in the arm currents in Fig. 2.25(a) (top). The circulating current due to these harmonics has a predominant 2nd harmonic (120 Hz) component with a peak value of nearly 275 A as shown in Fig. 2.25(a) (middle). This additional current circulates in the arms and results in additional losses and increased capacitor ripple voltage. The peak-peak ripple in the capacitor voltages is nearly 1000 V as shown in Fig. 2.25(a) (bottom). This results in a poor output voltage waveform quality with higher THD content. Hence need to suppress these harmonics is necessary. In the presence of circulating current control, the arm currents become near sinusoidal and the circulating current component becomes near-zero as shown in Fig. 2.25(b) (top and middle). The ripple in capacitor voltages reduces to almost half at 500 V. A FFT of the arm currents shows a reduction of nearly 230 A in the 2nd harmonic component, Fig. 2.26.

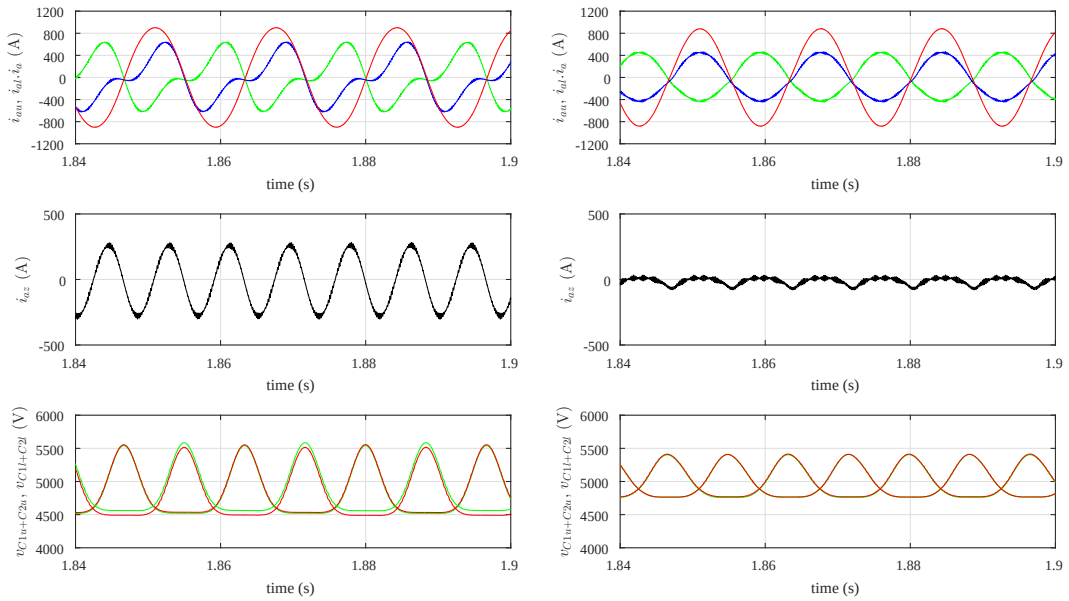


Figure 2.25: (top to bottom) Currents in upper arm and lower arm with output phase current, circulating current, capacitor voltages: (a) without circulating current control (b) with circulating current control

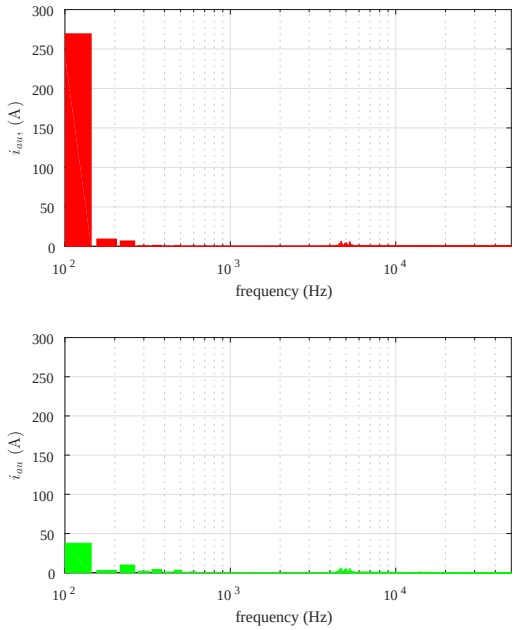


Figure 2.26: FFT of arm currents: (top) without circulating current control (bottom) with circulating current control

2.11 Experimental Results

This section presents experimental results obtained on a scaled down laboratory prototype of a 3-phase MMC setup as shown in Fig. 2.27. The results validate the theory described in previous sections. Closed loop circulating current control and hysteresis based voltage balancing is implemented to result in stable operation of the system. 3-step commutation is done in an FPGA for safe commutations between switching transitions. Detailed discussion of experimental prototype with results is presented in this section.

2.11.1 Hardware prototype

A scaled down laboratory prototype is built using IGBT modules and gate drivers laid out on PCBs. Each leg of the MMC is made up with four submodules per phase: two in each of the upper and lower arms. Integrated power IGBT modules from Vincotech are used which make the 3-level T-type submodules. Custom gate drivers ACPL-332J

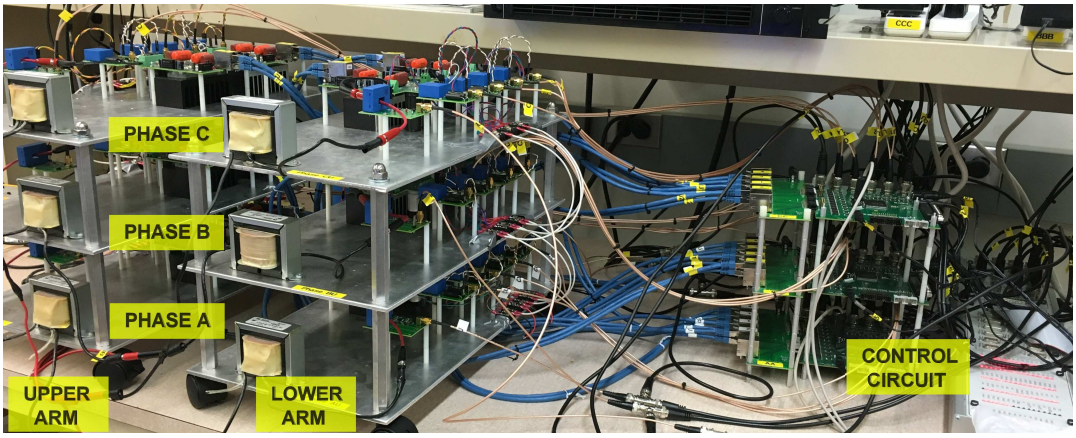


Figure 2.27: Hardware prototype of the 3-phase MMC

from Avago are laid out on a single 4-layer PCB. Distinct power and ground planes are used with the routing of components to reduce loop inductance and minimize noise due to EMI. The Avago drivers have desat protection and built in miller clamp functionality which eliminates the requirement of bipolar gate drive power supply. However, to achieve faster switching speeds and safe turn-off of IGBTs, a negative gate drive power supply is also incorporated. Isolated DC-DC converters from Cui with +15 V input and dual +17/-8 V output are used to power the gate drive circuit. Snubber capacitors are placed directly at the IGBT pins for protection. The submodule uses two capacitors at 1.1 mF and 2.2 mF. Digital gate signals are sent to each submodule using shielded ethernet cables through a RJ45 port. The driver chip also sends out a fault signal which is carried back through this port to the controller. One such submodule is shown in Fig. 2.28.

Each submodule receives 4 digital signals for the IGBTs and sends out 1 fault signal. Also each submodule is accompanied by 2 voltage sensors. Hall effect sensors LV25P from LEM are used. The input resistors of these sensors is designed at 5 kΩ to sense upto 100 V and result in an output of 10 V for the ADC. A sallen key filter follows it for signal conditioning. Every leg of the MMC also has two current sensors LA55P from LEM to sense the arm currents. The voltage and current sensor outputs are sent to the controller using shielded coaxial cables. These sensed voltages and currents are necessary for design of control algorithms of the MMC.

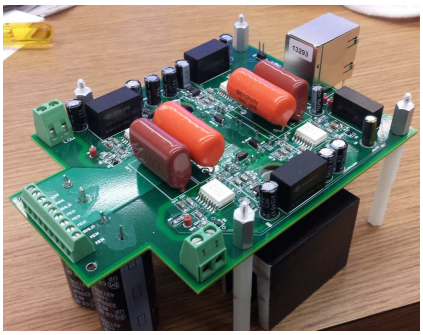


Figure 2.28: Hardware prototype of a 3-level submodule of the MMC

The 3-phase prototype has total of 12 submodules as shown in Fig. 2.27. Each phase is stacked on top of another using aluminum plates. Each phase has two 2.5 mH inductors to suppress the high frequency harmonics in arm currents. One arm of the converter is shown in Fig. 2.29.

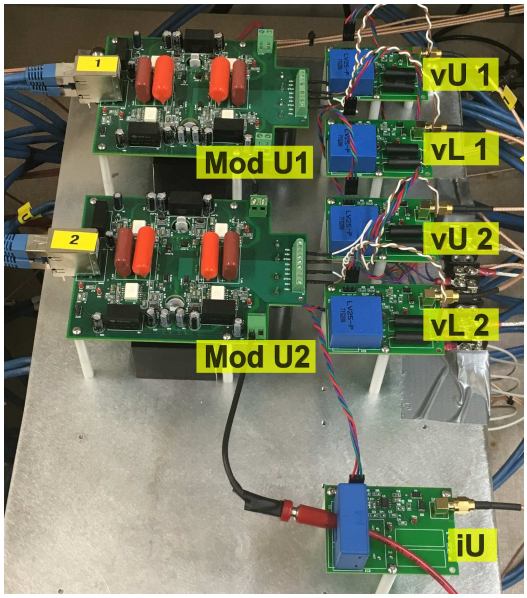


Figure 2.29: Hardware prototype of one arm of the MMC

2.11.2 Control platform

The control platform used is a combination of dSPACE DS1103 and three Spartan-3 FPGAs (Xilinx XC3S500E) as shown in Fig. 2.30. The sensed arm currents are sent to dSPACE where circulating current controllers are designed in MATLAB. The references for upper and lower arm voltages including the circulating current control is generated for every phase and is sent out from the DAC ports of the dSPACE unit to the ADC inputs of each FPGA. dSPACE acts as the master controller and sends out the 3-phase voltage reference signals to three FPGAs, one for each phase. Each FPGA has a 50 MHz clock which is used to sample and generate the gate signals for the IGBTs. Hybrid modulation using a combination of phase-shifted and level-shifted carriers is generated in the FPGA. Each FPGA also receives the sensed voltages from each submodule along with the arm current of that phase. This is used in the voltage balancing algorithm. A state machine is implemented in verilog which sorts the capacitor voltages in order and assigns the ideal gate signals generated from hybrid modulation to the appropriate switch in a submodule. 3-step commutation with a commutation interval of 0.5 μs is implemented in another state machine. All of the above is coded in verilog in Xilinx 14.4. The signals are sent out from the digital ports of the FPGA to the power boards using ethernet cables.

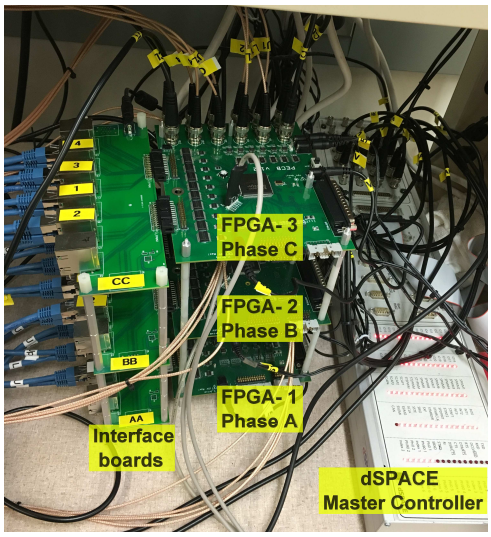


Figure 2.30: Hardware prototype of the MMC control platform

2.11.3 Results using 3-level submodules

This section presents the results obtained using 3-level submodules. Each submodule was first tested individually putting 40 V DC-sources across its capacitors before inserting them into the MMC system. Following the hybrid modulation, the upper set of capacitors can only be used when the lower set is already used. This is shown by the gate signals for FULL-ON and HALF-ON states in Fig. 2.31 (top, second from top). The output current and voltage of one submodule is also shown (second from bottom, bottom) which clearly shows 3 distinct voltage levels.

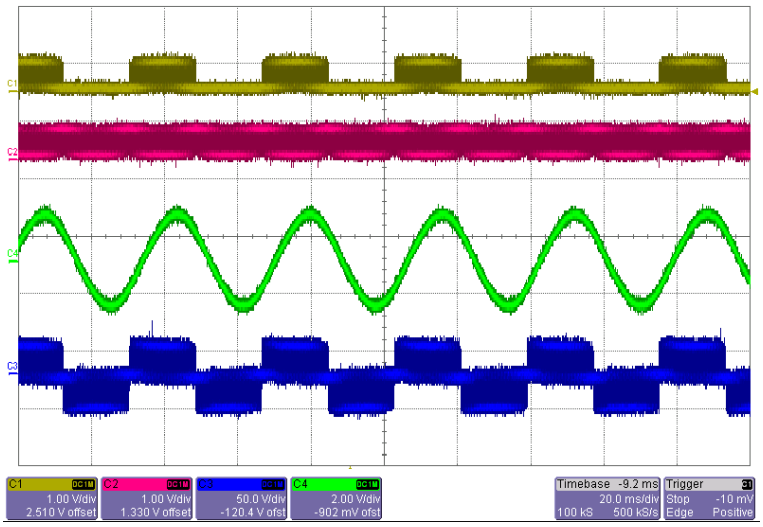
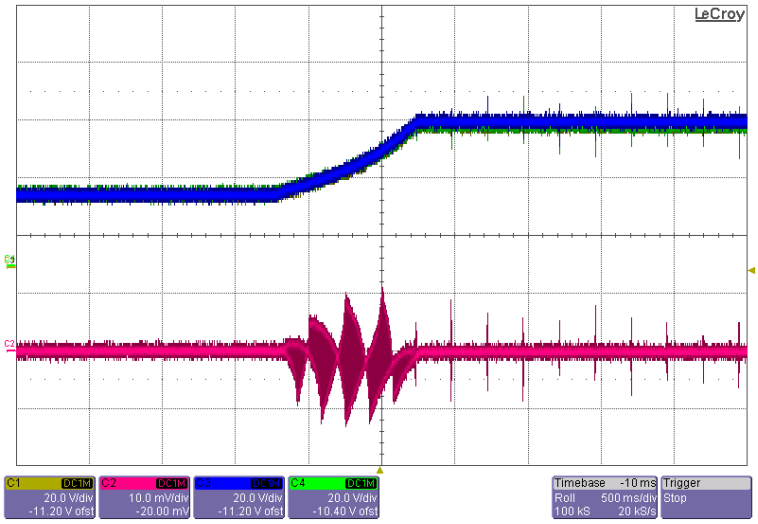
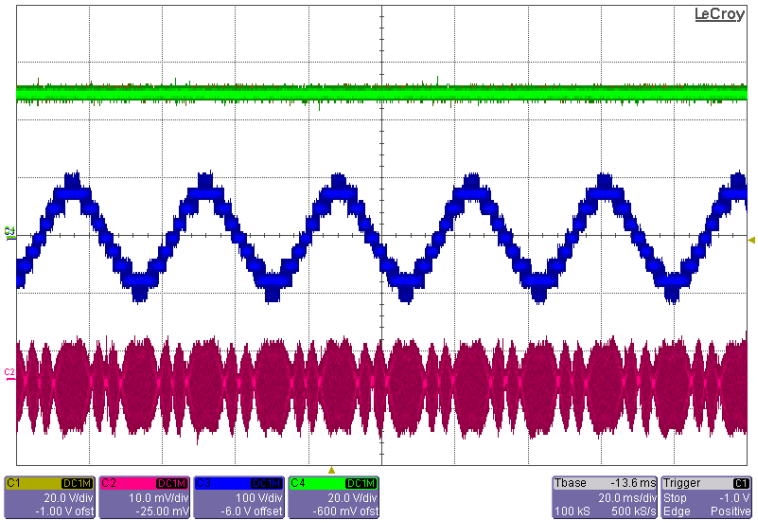


Figure 2.31: Submodule results: (top to bottom) Gate signal for S_1 for FULL-ON state, gate signal for S_3, S_4 for HALF-ON state, output current, output voltage

The experiments are run with a DC bus voltage of 200 V with a switching frequency of 2.5 kHz. Before the system can start in steady state, all the capacitors have to be precharged to the nominal capacitor voltage of 50 V. Following the precharge scheme as described before, the capacitors are all nominally precharged to 50 V as shown in Fig. 2.32(a). The charging currents is very small at 0.1 A. The modulation starts after the capacitors have been precharged to result in a 9-level voltage waveform as shown in Fig. 2.32(b). This result is under no-load, hence output current is zero and capacitors have almost zero ripple.



(a)



(b)

Figure 2.32: Precharge results:(a) capacitor voltages and arm current (b) no-load capacitor voltage, output voltage and arm current

Next, the RL load is connected and the 3-phase system is operated with voltage balancing and circulating current control. Results are obtained across an R-L load with R = 16 Ω and L = 30 mH. Hybrid modulation with a modulation index m = 0.86 is implemented in each FPGA. The steady state results are shown in Fig. 2.33 and Fig. 2.34. Using hybrid modulation for 4 submodules in each phase, 4 carrier signals are phase shifted by 360°/4 and level shifted one on top of the other. This results in 9 voltage levels as shown in Fig. 2.33 (top). The voltage levels are now fluctuating unlike those under no-load because of sinusoidal load currents flowing. Phase a load current is shown in Fig. 2.33 (bottom) which is near sinusoidal with very low harmonic content and a peak magnitude of 1.2 A. This is slightly lower as compared to the analytical value of 1.5 A, which can be accounted to voltage drop across devices. The upper and lower arm voltages are shown in Fig. 2.34 (top) which have 5 distinct voltage levels. The alternating output voltage in Fig. 2.34 (bottom) is one-half the difference of the arm voltages.

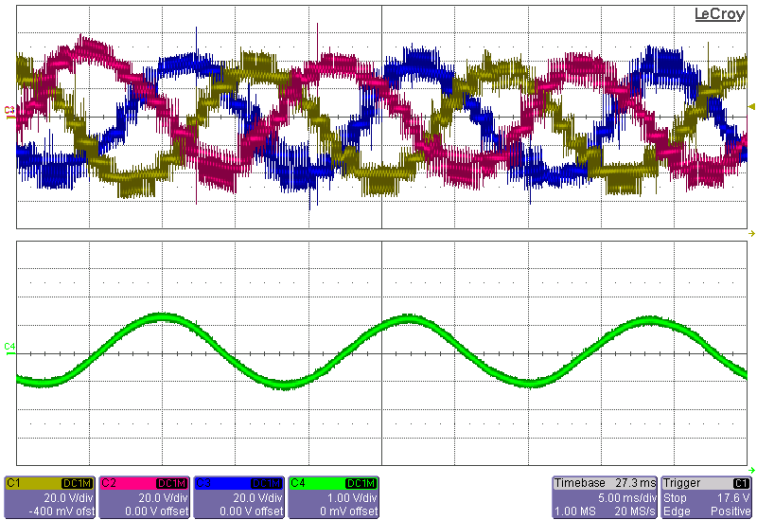


Figure 2.33: (top) Three line-neutral voltages (bottom) phase-a line current

Voltage balancing algorithm is implemented in each FPGA, hence the capacitors across submodules are held in place about their nominal values, as shown in Fig. 2.35(a) and Fig. 2.35(b). Fig. 2.35(a) shows the capacitor voltages of v_{C1} whereas those across v_{C2} are shown in Fig. 2.35(b). The capacitors chosen have a tolerance value of 5% as

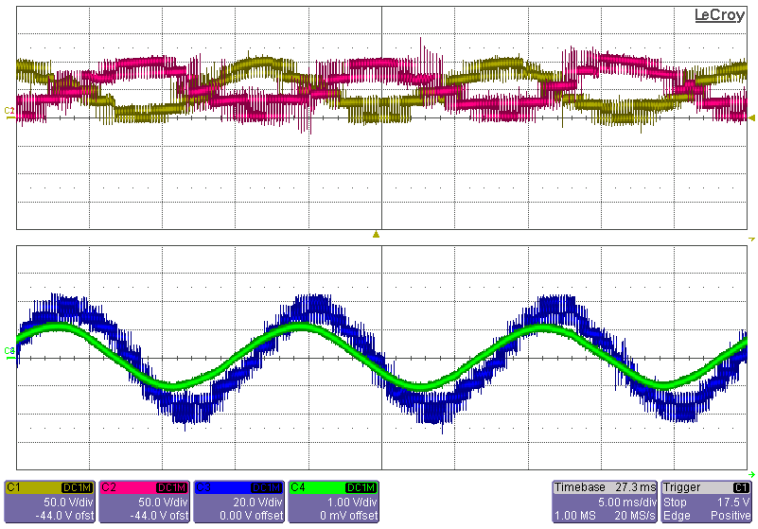
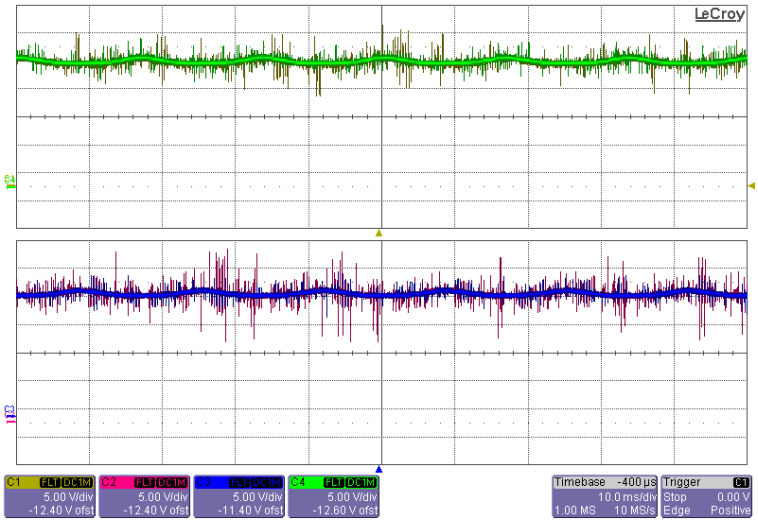


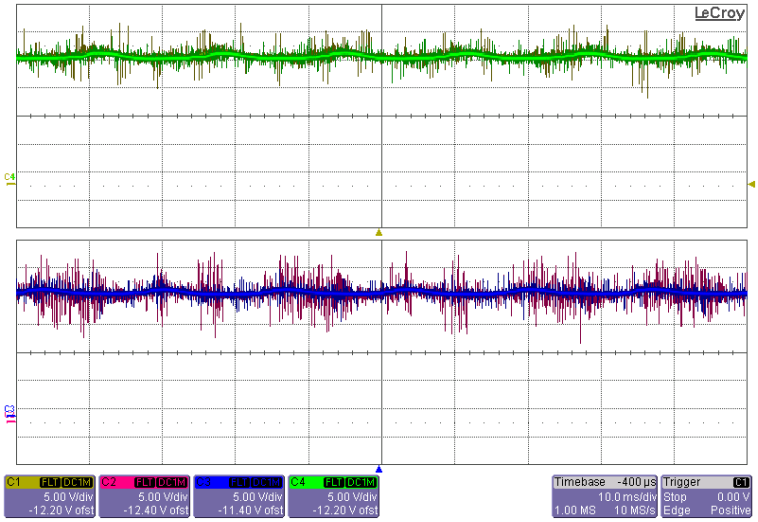
Figure 2.34: (top) Upper and lower arm voltages (bottom) converter output voltage

stated by the manufacturer. As seen in simulation results, without a balancing algorithm the capacitor voltages diverge. The system would become unstable and collapse eventually and hence such results were not implemented.

The next set of results are with respect to circulating current control. The currents along the upper and lower arms with corresponding arm voltage, output voltage and current are shown without closed loop control in Fig. 2.36(a) and with closed loop circulating current control in Fig. 2.36(b) respectively. It can be very well seen that the arm currents have dominant low order harmonics as described before. With the PI controllers implemented in dSPACE, the predominant 2nd order circulating current component is sufficiently suppressed to result in near sinusoidal arm currents as seen in Fig. 2.36(b) (top). This results in lower capacitor voltage ripple which reflects in lower THD in output voltages.

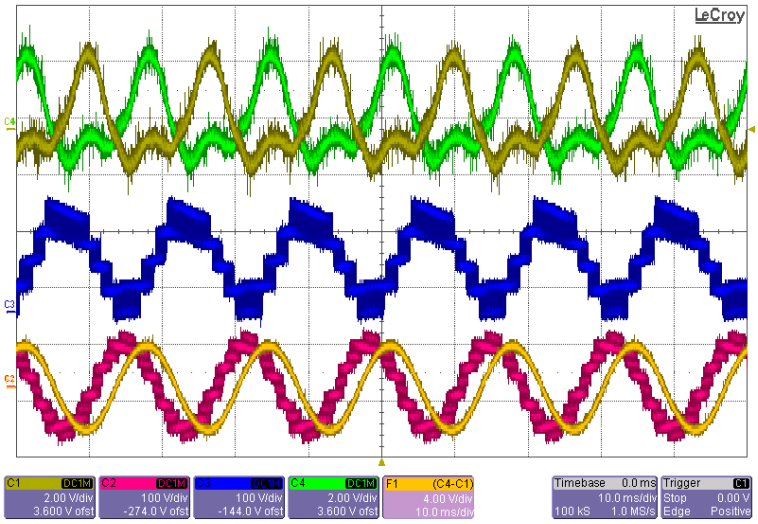


(a)

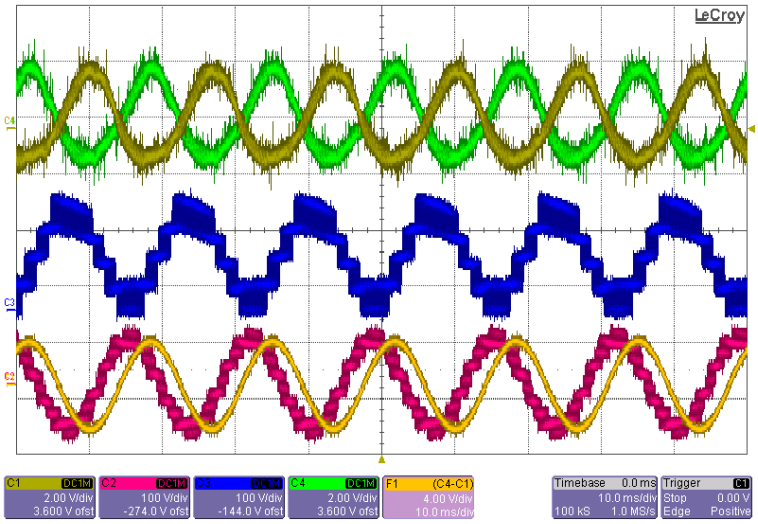


(b)

Figure 2.35: Voltage balancing results: (top to bottom) Capacitor voltages in upper arm and lower arm for (a) C_1 capacitors (b) C_2 capacitors



(a)



(b)

Figure 2.36: Circulating current control results: (top to bottom) Upper and lower arm currents, arm voltage, converter output phase voltage and current: (a) without circulating current control (b) with circulating current control

2.11.4 Results using 2-level submodules

The 3-phase MMC was also run with conventional 2-level half-bridge submodules to compare the performance with proposed 3-level submodules. If the bidirectional switch in the proposed 3-level submodule is always kept OFF, it turns into a 2-level half-bridge submodule which was used to get the results for this subsection. 4 submodules per leg were used similar to the proposed system described in previous subsection. This results in 5 distinct voltage levels in the converter output voltage as shown in Fig. 2.37 (top). The output current is near sinusoidal as shown in Fig. 2.37 (bottom). The result showing generation of output voltage from the difference of arm voltages is shown in Fig. 2.38(a) and the corresponding balanced capacitor voltages in upper and lower arms is shown in Fig. 2.38(b) respectively.

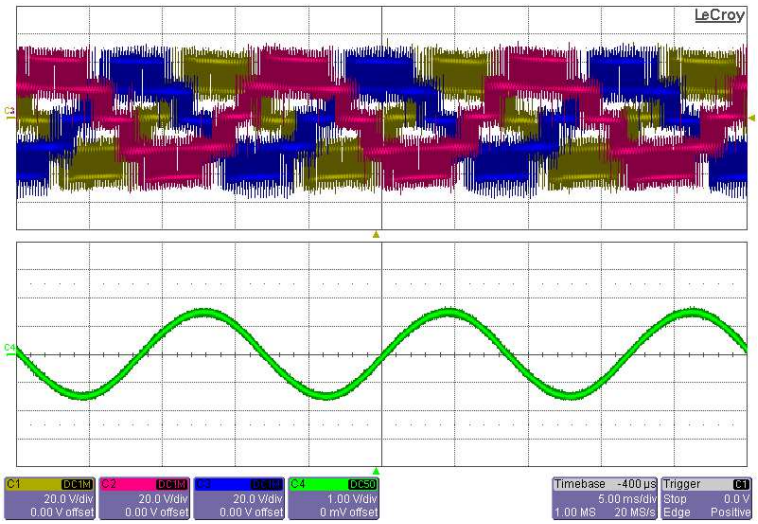
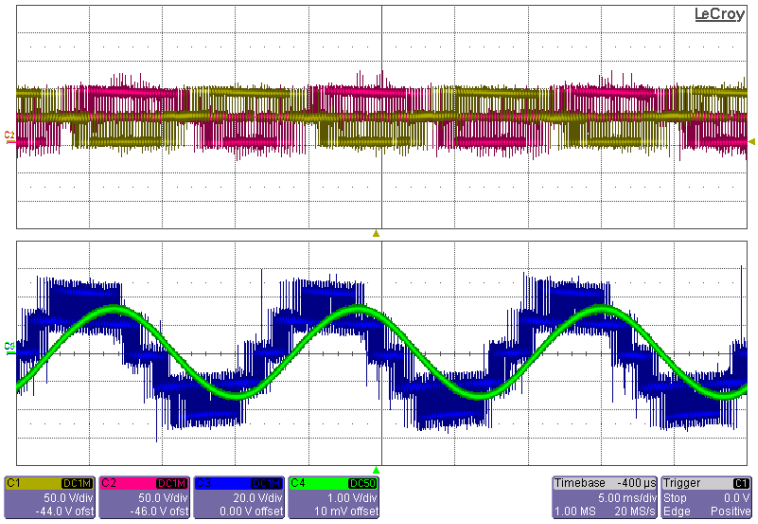
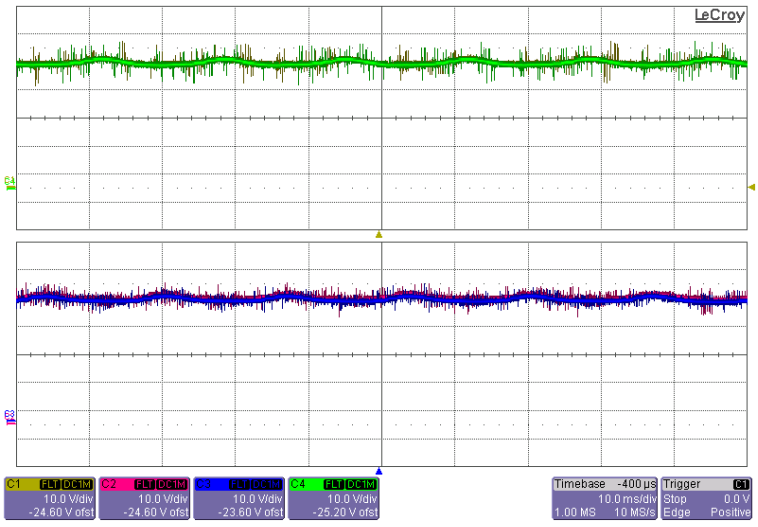


Figure 2.37: (top) Three line-neutral voltages (bottom) phase-a line current



(a)



(b)

Figure 2.38: (a) (top) Upper and lower arm voltages (bottom) converter output voltage (b) Voltage balancing results: (top to bottom) Capacitor voltages in upper arm and lower arm

For the sake of comparison, the MMC system using 2-level submodules was reconfigured with 8 submodules to match the same number of output voltage levels using four 3-level submodules per leg. The results are shown in Fig. 2.39. Using 8 submodules per leg of the half-bridge submodules results in 9 distinct voltage levels. However this increases the necessary connectors between modules and bus bar structure for interconnecting submodules. The THD in output voltage and current is almost similar in the 2 configurations.

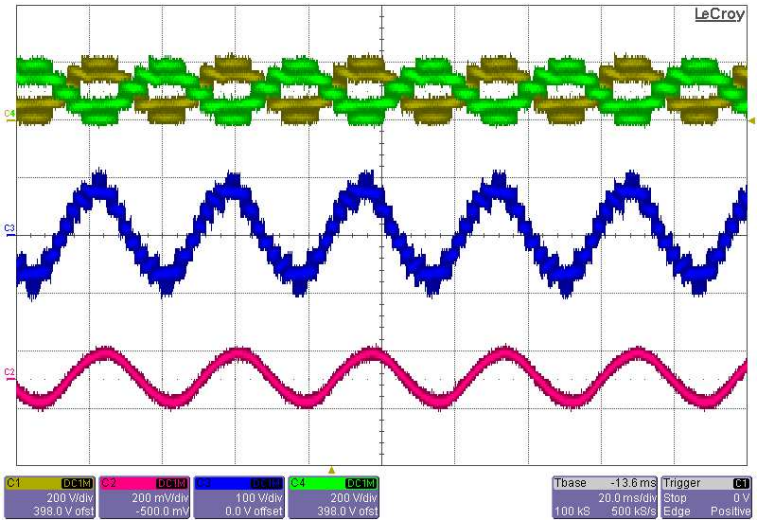


Figure 2.39: (top to bottom) Upper and lower arm voltages, converter output voltage, converter line current

2.12 Comparison with other submodules

A comprehensive comparison between different existing submodule topologies like the conventional half bridge (HB) submodule, full bridge (FB) submodule, clamp double (CD) submodule, neutral point clamped (NPC) submodule, flying capacitor (FC) submodule and the two new proposed topologies (SM1 and SM2) in this chapter is presented in Table 2.2. The comparison is done considering all the submodules generate same output voltage with equal number of voltage levels.

As can be seen the HB and FB submodules require double the number of submodules to achieve the same number of output voltage levels, as they can switch between only two voltage levels, V_C and 0. The FB and CD submodules use additional switches and diodes to limit short circuit over-currents during faults. The FB submodule can clamp the voltage to $-V_{dc}$ during faults and hence is the most favorable topology for protection. The CD, NPC, FC and proposed submodules can switch to 3 voltage levels, hence require half the number of submodules compared to conventional half-bridge submodules. The NPC structure has additonal clamp diodes.

In a practical submodule implementation, there are additional components like protection thyristors and high-speed bypass switches for safety and bypassing a module during maintenance as shown in Fig. 2.40. Connecting different submodules with each other requires high current carrying bus-bars. Using 3-level submodules reduces these additional components by one-half as compared to the 2-level submodule topologies. In FB and CD submodules, the additional semiconductor devices are of no use in regular operation but account for increased semiconductor losses. The NPC and FC submodules can reach three voltage levels and have voltage stress of $V_C/2$ across all the switches which make them a good choice for future modular multilevel operation. These topologies have two switches turning on or off during the FULL-ON and BYPASS states, they have high conduction and switching losses. The newer topologies undergo the least semiconductor losses due to just one switch conducting during FULL-ON and BYPASS states but have two of the switches with V_C rating. The bidirectional switch has $V_C/2$ rating. Since we are making use of a bidirectional switch, a gate driver with one isolated power supply will suffice and it reduces the gate drive circuit complexity. The only challenge with the 3-level topologies is voltage balancing control, which has been

addressed in this chapter. Overall the newer topologies prove a good choice for modular configuration to be used in future HVDC applications.

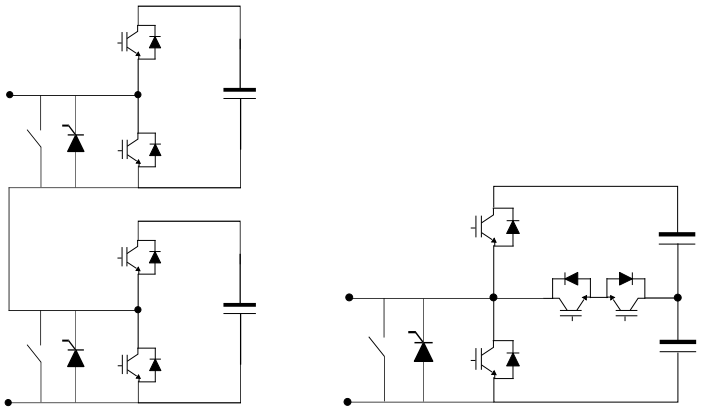


Figure 2.40: MMC submodules with protection circuitry to generate three voltage levels using (a) two 2-level submodules connected in series (b) one 3-level submodule

Table 2.2: Comparative analysis between different submodule parameters

Parameter	**Half bridge**	**Full bridge**	**Clamp double**	**NPC**	**Flying capacitor**	**New SM1**	**New SM2**
No. of submodules	$2n$	$2n$	n	n	n	n	n
No. of IGBT's	$4n$	$8n$	$5n$	$4n$	$4n$	$4n$	$3n$
No. of diodes	$4n$	$8n$	$7n$	$6n$	$4n$	$4n$	$6n$
No. of thyristors	$2n$	0	0	n	n	n	n
Bypass switches	$2n$	$2n$	n	n	n	n	n
No. of busbars	$2n$	$2n$	n	n	n	n	n
Voltage stress	$V_C/2$	$V_C/2$	V_C	$V_C/2$	$V_C/2$	V_C, $V_C/2$	V_C, $V_C/2$
Conduction losses	=	highest	high	high	=	lowest	low
Switching losses	=	highest	high	high	=	lowest	low
Gate drivers	$4n$	$8n$	$5n$	$4n$	$4n$	$3n/4n$	$3n$
Control complexity	low	low	low	high	medium	high	high

2.13 Summary

New topologies for modular multilevel converter based HVDC system are proposed in this chapter with advanced features. The newer submodule topologies can reach three voltage levels resulting in half the number of submodules required, as compared to conventional half-bridge submodules. Added benefits of reduced auxiliary circuit components and considerable lower semiconductor losses make the new topology an attractive solution for use in future HVDC applications. A hybrid modulation technique combining both phase shifted and level shifted carriers is proposed. Also a simple voltage balancing algorithm based on unequal capacitor sharing is proposed resulting in proper balanced capacitor voltages over entire modulation range and output power factor. To suppress circulating currents within the arms, a three-phase abc to dq transformation based PI controller is designed. For hardware implementation, an intelligent commutation technique is proposed that results in $2/3^{\text{rd}}$ of the transitions soft switched under zero current. The results are shown by MATLAB/Simulink simulations and experimental results on a scaled down laboratory prototype. A qualitative and quantitative comparison with other existing MMC submodule topologies is presented.

Note: Part of this chapter is reproduced from my previous publications [18, 29, 53, 64]

Chapter 3

Modular Multilevel Converters for Power Electronic Transformers

At high voltage and power levels in utility-scale applications, transformers are needed to step-down grid voltages for integrating renewables and motors. The conventional 60-Hz transformers are large and bulky which occupy a significant amount of space and volume. Recently power electronic transformers (PET) have become subject of interest in literature for such applications. PETs combine very compact high-frequency transformer (HFT) and electronic circuitry for frequency conversion (60-Hz to kHz and vice-versa) making the overall system much compact and efficient. A modular multilevel converter is proposed as the power converter on the high voltage side to meet the voltage stress in kV range. It retains all the advantages of MMCs as discussed in Chapter 2 for high voltage power conversion. It also offers other advantages of reduced dV/dt across the high frequency transformer windings by generating near sinusoidal voltages in the kHz range. This chapter describes the modulation and control of MMCs for interfacing high frequency transformers and the effects on voltage balancing and circulating currents. The analysis is validated by simulation and experimental results.

3.1 Introduction

The proposed system using MMC based PET is as shown in Fig. 3.1(a). Unlike the grid side MMC, the operation of the transformer interfaced MMC is very different. As shown by the highlighted part in Fig. 3.1(a), the MMC connected to the HFT needs to generate high frequency sinusoidal voltages in the kHz range. The pulse-width modulation approach described in Chapter 2 can not directly be applied here as it would result in very high switching losses. To generate a high frequency sinusoidal voltage at say 10 kHz, a carrier frequency at least 20 times higher will be required with pulse-width modulation. Fundamental switching frequency modulation techniques are of interest here for such application. Nearest level modulation [65, 66] and harmonic elimination method [67] have been proposed in literature for 60-Hz voltage generation with low switching frequencies. These techniques can be applied to MMC to synthesize near sinusoidal voltages in the kHz range by switching at relatively similar frequencies. Trapezoidal modulation [68] has been used for isolated DC-DC operation of MMC as it results in a switching frequency operation close to reference signal in kHz range, thus reducing switching losses. Research has been done on DC/DC isolated PET using MMCs for interconnecting two different HVDC transmission lines [69, 70]. These techniques have been applied to a MMC based HVDC system and can be extended to the proposed PET application described in this thesis. For operation of the MMC to generate high frequency voltages, problem of circulating currents is relaxed as the arm inductors and transformer leakage inductances act as filters for the high frequency currrents. Also capacitor voltage ripple is greatly reduced.

The renewable energy source or machine drive is interfaced with the high frequency transformer using back-to-back DC/AC or direct AC/AC converters. This low voltage converter converts the high frequency sinusoidal voltages from the transformer to low frequency AC or DC as required by the renewable energy sources. In this chapter, the low voltage side converter and load is modeled as an effective resistance R_e for the purpose of simplicity, as shown in Fig. 3.1(b). The HFT is modeled with the effective total leakage inductance L_{lkg} and resistance R_{lkg} of the windings.

Section 3.2 describes the different modulation techniques for high frequency operation of MMC. Voltage balancing and circulating current control is discussed in Section

3.3 with the effects of high frequency operation on the arm inductors and floating capacitors. The modulation and control is substantiated by simulation results in MATLAB/Simulink and experimental results on a scaled down laboratory prototype.

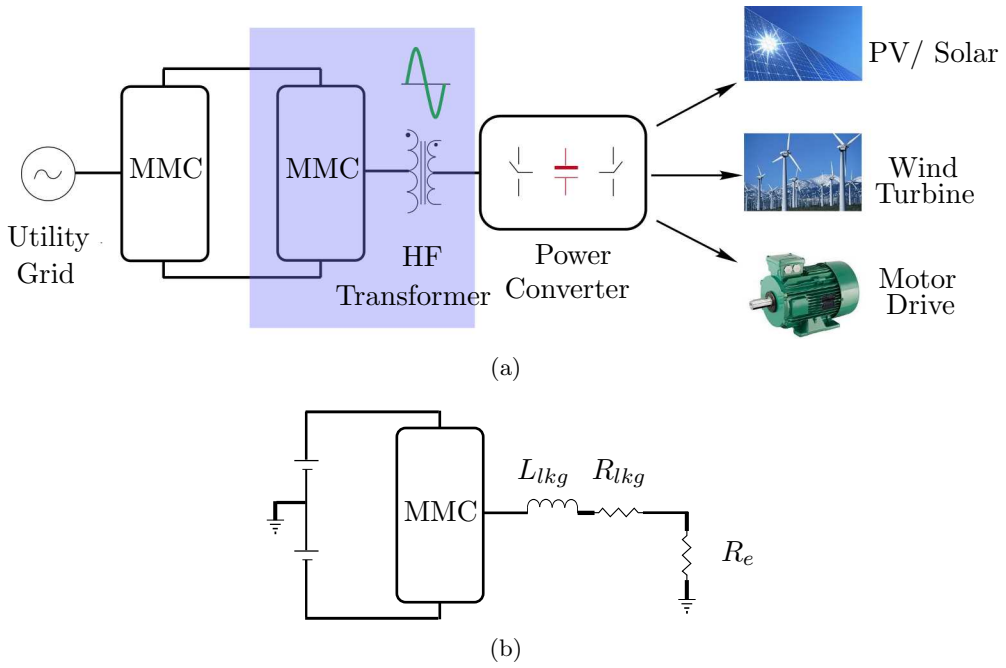


Figure 3.1: (a) Block diagram of MMC-based PET integrating HFT (a) Simplified block diagram

3.2 Analysis: Modulation

To interface a high frequency transformer, the MMC needs to generate high frequency near sinusoidal voltages, without compromising on overall system efficiency. This section discusses conventional pulse-width modulation approach for high frequency voltage generation and fundamental switching frequency methods like nearest level modulation.

3.2.1 Pulse-width modulation

One common technique for generating the control signals for the switches in the submodules is by carrier based pulse-width modulation (PWM) as described in the previous

chapter. A set of triangular waveforms at a switching frequency are compared with normalized reference sinusoidal waveforms to generate the switching pulses for the IGBTs. Phase-shift PWM and level-shift PWM are the two most common strategies for the half-bridge submodule, whereas hybrid PWM scheme was described for the new 3-level submodules modulation.

In the previous chapter, the reference voltages were generated at 60-Hz (grid frequency) whereas the carriers superimposed on top were at much higher frequencies of 2 kHz. Doing so, the reference signals behaved almost DC to the carriers which were at much higher frequencies. Thus a near perfect output voltage could be synthesized which had harmonics at much higher frequencies as compared to the grid frequency, hence the grid inductances were sufficient to filter them out. For applications as described in this chapter to interface a high frequency transformer, the generated output voltage is at higher frequencies compared to 60-Hz generation. The generated voltages are at frequencies greater than 1 kHz such that the magnetic cores can be significantly smaller resulting in a much compact and power dense transformer. To generate a sinusoidal output voltage at 1 kHz, following the same procedure as described in previous chapter, the carriers switching frequency needs to be significantly higher, say 20 kHz. But this would result in significant switching losses, resulting in poor overall efficiency of the system.

This section presents analysis of different PWM carrier frequencies for PET applications. For generation of voltage with a fundamental frequency much higher (say 1 kHz) compared to 60-Hz, the carrier frequency must be brought down to reduce switching losses. This does not diminish the voltage quality significantly since the harmonics in the voltage now are at frequencies greater than 1 kHz already, hence no need for large filters. A comparison of PWM at different switching frequencies is shown in Fig. 3.2(a) 3.2(b) 3.2(c) for $f_s = f_o$, $f_s = 5f_o$ and $f_s = 10f_o$, where f_s is the carrier switching frequency and f_o is the fundamental frequency of the output voltage to be synthesized.

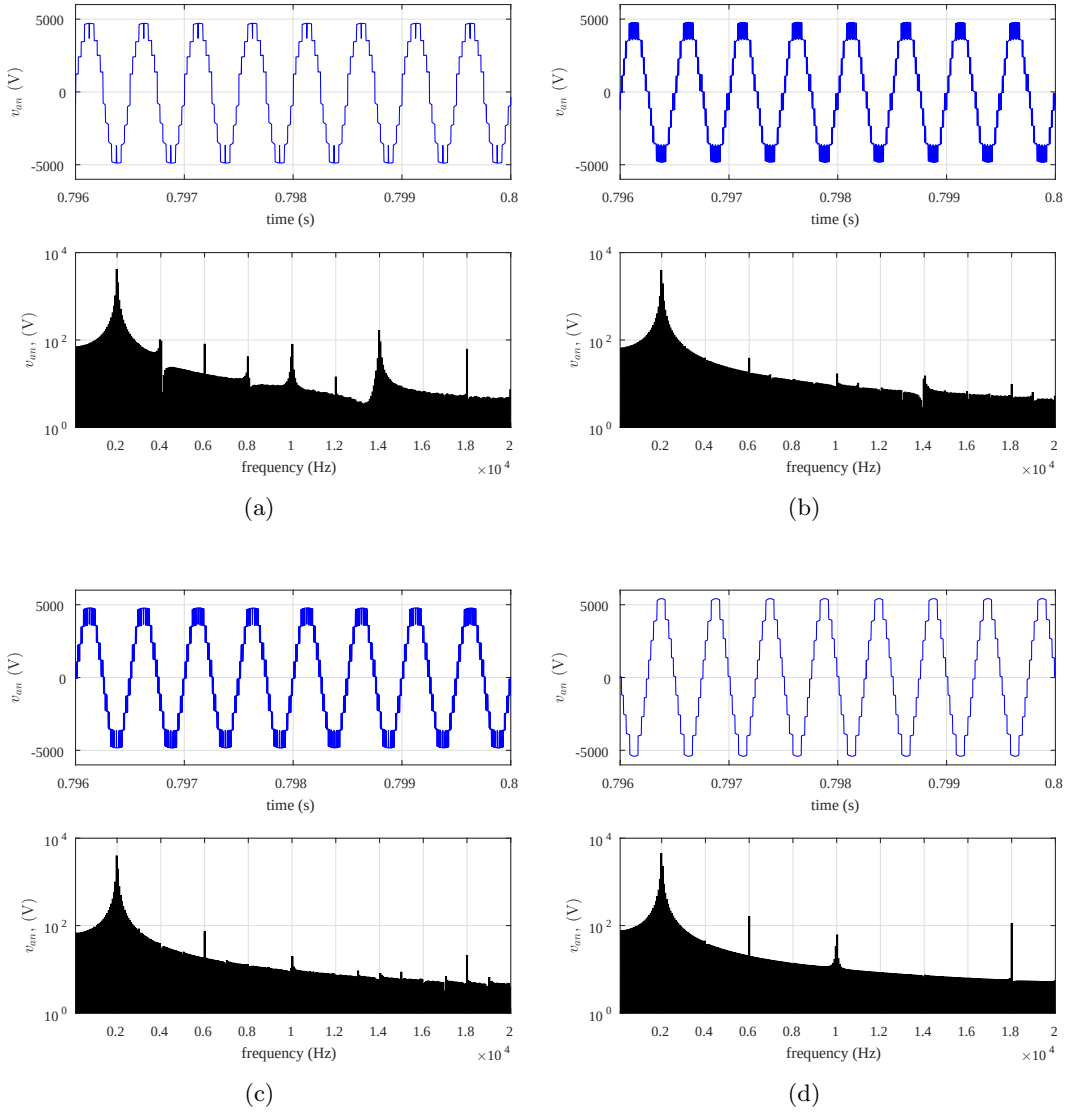


Figure 3.2: (upper) Converter output voltage, (lower) FFT of voltage generated for: (a) PWM with $f_s = f_o$ (b) PWM with $f_s = 5f_o$ (c) PWM with $f_s = 10f_o$ (d) Nearest level modulation

Fig. 3.2(a) shows that switching at $f_s = f_o$ is like switching at fundamental switching frequency. However, the reference signal and carriers need to be well synchronized to minimize low order harmonics. Switching at higher frequencies of $5f_o$ or $10f_o$ results in lower output voltage distortion as can be seen from the FFT plots, but results in higher switching losses. Since the synthesized voltage is multilevel in nature which resembles a near sinusoid when the number of submodules is large, output voltage distortion is of less importance compared to reduction in switching losses in such systems. Thus fundamental switching frequency operation is more preferred for such applications.

The first carrier is aligned along the reference voltage waveforms. The next carriers are phase-shifted by $360^\circ/4$ (assuming 4 submodules per leg) for every alternate upper arm and lower arm submodule. There are 2 sets of carriers level shifted on top of another to result in 3-voltage levels for each submodule. This analysis also applies to the 2-level submodule using just phase-shifted carriers. It can be seen that output voltage generated has all voltage levels except zero level, hence a total of 8 voltage levels using 4 submodules per leg. This results in the most optimal PWM operation for high frequency voltage generation with least losses. A more optimal solution than this is nearest level modulation as shown in Fig. 3.2(d), which will be described in the next subsection.

3.2.2 Nearest level modulation

A simpler way to generate high frequency output voltages without switching at much higher frequencies is using a fundamental switching frequency modulation approach like nearest level modulation (NLM). Unlike pulse-width modulation, the NLM method does not need a complex carrier generation, making NLM method the simplest and most practical modulation method for the MMC. However, in spite of the low switching frequency and simple implementation, the NLM method generates poorer quality waveforms than pulse-width modulation. But for the current application which needs voltage generation at higher frequencies, the harmonics generated are at multiples of fundamental frequency which is greater than 1 kHz (say), hence the harmonics can be easily suppressed. This section describes two NLM methods applied to MMCs for generation of $n+1$ and $2n+1$ output voltage levels.

The voltages to be synthesized at high frequency are given in (3.1) where V_o is the

amplitude of converter output voltage and f_o is the output frequency to feed the high frequency trandformer. This is generally at relatively higher frequencies ($\geq$ 1 kHz) as compared to the grid frequency (60-Hz). The arm voltage references are as shown in (3.2) and one-half the difference between the lower and upper arm voltage gives the total output voltage.

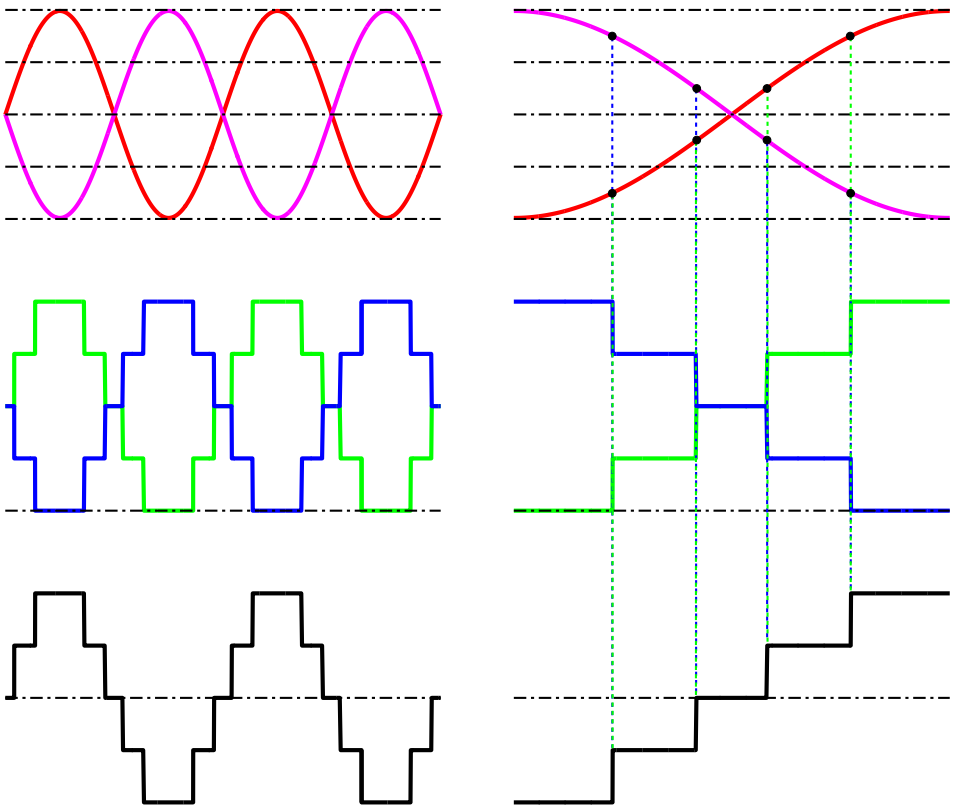
$$\begin{aligned} v_a &= V_o \cos(\omega_o t) \\ v_b &= V_o \cos\left(\omega_o t - \frac{2\pi}{3}\right) \\ v_c &= V_o \cos\left(\omega_o t + \frac{2\pi}{3}\right) \end{aligned} \tag{3.1}$$

$$\begin{aligned} v_{up}^* &= -\frac{v_p}{V_{dc}} \\ v_{lp}^* &= \frac{v_p}{V_{dc}} \\ v_p^* &= \frac{v_{lp} - v_{up}}{2} \end{aligned} \tag{3.2}$$

The inserted submodules in the upper and lower arms respectively are dependent on the step voltage level. This depends on the capacitor voltage in the submodule i.e capacitor voltage of one submodule if using 2-level submodules or capacitor voltage of each capacitor in a submodule if using 3-level submodules. Assuming step voltage level of V_c, the total number of inserted levels is given by (3.3). The round function (round $(x.y)$) means that the real number x is rounded to the nearest whole number according to the decimal fraction y. If the decimal fraction y is greater than 0.5, x is rounded up to the next whole number, otherwise rounded down to the previous whole number as given in (3.4). The detailed waveforms are shown in Fig. 3.3(a) with zoomed in version of a quarter cycle in Fig. 3.3(b) assuming 8 number of 2-level or 4 number of 3-level submodules respectively.

$$\begin{aligned} n_{ua} &= \text{round}\left[-\frac{2V_o}{V_c}\cos(\omega_o t)\right] \\ n_{la} &= \text{round}\left[\frac{2V_o}{V_c}\cos(\omega_o t)\right] \end{aligned} \tag{3.3}$$

$$n = \text{round } [x.y] = \begin{cases} x+1, & \text{if } y \geq 0.5 \\ x, & \text{if } y < 0.5 \end{cases} \tag{3.4}$$



(a) (b)

Figure 3.3: (upper) Reference signals, (middle) upper and lower arm voltages, (lower) converter output voltage: (a) without offset in reference voltages to generate $n+1$ voltage levels (a) zoomed version without offset in reference voltages to generate $n+1$ voltage levels

Assuming the number of levels possible in each arm to be 5 (including zero level), the waveforms with the above described method generates an output voltage with also 5 voltage levels as shown in Fig. 3.3. This happens with 8 submodules per leg of the 2-level submodules or 4 submodules per leg of the 3-level submodules. This is described in detail here with respect to the individual submodules and its switches operation. For a half bridge submodule, the submodules inserted are dependent on the expression (3.5) for upper arm and (3.6) for lower arm respectively.

$$\begin{aligned} \mathrm{SM}_{1234} = \mathrm{OFF}, &\quad \text{if } n_{up} = 0 \\ \mathrm{SM}_{1} = \mathrm{ON}, \quad \mathrm{SM}_{234} = \mathrm{OFF} &\quad \text{if } n_{up} \geq 1 \\ \mathrm{SM}_{12} = \mathrm{ON}, \quad \mathrm{SM}_{34} = \mathrm{OFF} &\quad \text{if } n_{up} \geq 2 \\ \mathrm{SM}_{123} = \mathrm{ON}, \quad \mathrm{SM}_{4} = \mathrm{OFF} &\quad \text{if } n_{up} \geq 3 \\ \mathrm{SM}_{1234} = \mathrm{ON}, &\quad \text{if } n_{up} = 4 \end{aligned} \tag{3.5}$$

$$\begin{aligned} \mathrm{SM}_{5678} = \mathrm{OFF}, &\quad \text{if } n_{lp} = 0 \\ \mathrm{SM}_{5} = \mathrm{ON}, \quad \mathrm{SM}_{678} = \mathrm{OFF} &\quad \text{if } n_{lp} \geq 1 \\ \mathrm{SM}_{56} = \mathrm{ON}, \quad \mathrm{SM}_{78} = \mathrm{OFF} &\quad \text{if } n_{lp} \geq 2 \\ \mathrm{SM}_{567} = \mathrm{ON}, \quad \mathrm{SM}_{8} = \mathrm{OFF} &\quad \text{if } n_{lp} \geq 3 \\ \mathrm{SM}_{5678} = \mathrm{ON}, &\quad \text{if } n_{lp} = 4 \end{aligned} \tag{3.6}$$

Similarly for a 3-level submodule based MMC, the states of individual submodules are as given by (3.7) for upper arm and (3.8) for lower arm respectively. The FULL-ON state can only occur after the HALF-ON state has occurred. As shown in Fig. 3.3(b), the upper arm and lower arm voltages are exactly 180° out of phase. Hence the difference in these voltages which dictates the output voltage also has 5 voltage levels. Thus this method of implementation results in $n+1$ voltage levels by use of $2n$ number of 2-levels submodules or n number of 3-level submodules per leg.

$$\begin{aligned}
\text{SM}_{12} = \text{OFF}, &\quad \text{if } n_{up} = 0 \\
\text{SM}_1 = \text{HALF-ON}, \quad \text{SM}_2 = \text{OFF} &\quad \text{if } n_{up} = 1 \\
\text{SM}_1 = \text{FULL-ON}, \quad \text{SM}_2 = \text{OFF} &\quad \text{if } n_{up} \geq 2 \\
\text{SM}_1 = \text{FULL-ON}, \quad \text{SM}_2 = \text{HALF-ON}, &\quad \text{if } n_{up} = 3 \\
\text{SM}_{12} = \text{FULL-ON}, &\quad \text{if } n_{up} = 4
\end{aligned} \tag{3.7}$$

$$\begin{aligned}
\text{SM}_{34} = \text{OFF}, &\quad \text{if } n_{lp} = 0 \\
\text{SM}_3 = \text{HALF-ON}, \quad \text{SM}_4 = \text{OFF} &\quad \text{if } n_{lp} = 1 \\
\text{SM}_3 = \text{FULL-ON}, \quad \text{SM}_4 = \text{OFF} &\quad \text{if } n_{lp} \geq 2 \\
\text{SM}_3 = \text{FULL-ON}, \quad \text{SM}_4 = \text{HALF-ON}, &\quad \text{if } n_{lp} = 3 \\
\text{SM}_{34} = \text{FULL-ON}, &\quad \text{if } n_{lp} = 4
\end{aligned} \tag{3.8}$$

To increase the number of voltage levels to double of what can be obtained by the method described above, a phase-shift needs to be developed between the upper and lower arm voltages. This is achieved by adding an offset of $-\frac{V_c}{4}$ in the reference voltages as given by (3.9). Doing so shifts the sinusoidal reference signals lower such that the resulting arm voltages have a wider zero level and narrower V_{dc} level as shown in Fig. 3.4. As can be seen in the zoomed version of Fig. 3.4(b), the arm voltages have a finite phase-shift between them which results in 9 voltage levels in the output voltage. By this simple modification, the resultant output voltage can have $2n + 1$ voltage levels, thus improving its voltage quality and reducing THD.

$$\begin{aligned}
n_{ua} &= \text{round}\left[-\frac{2V_o}{V_c}\cos(\omega_o t) - \frac{V_c}{4}\right] \\
n_{la} &= \text{round}\left[\frac{2V_o}{V_c}\cos(\omega_o t) - \frac{V_c}{4}\right]
\end{aligned} \tag{3.9}$$

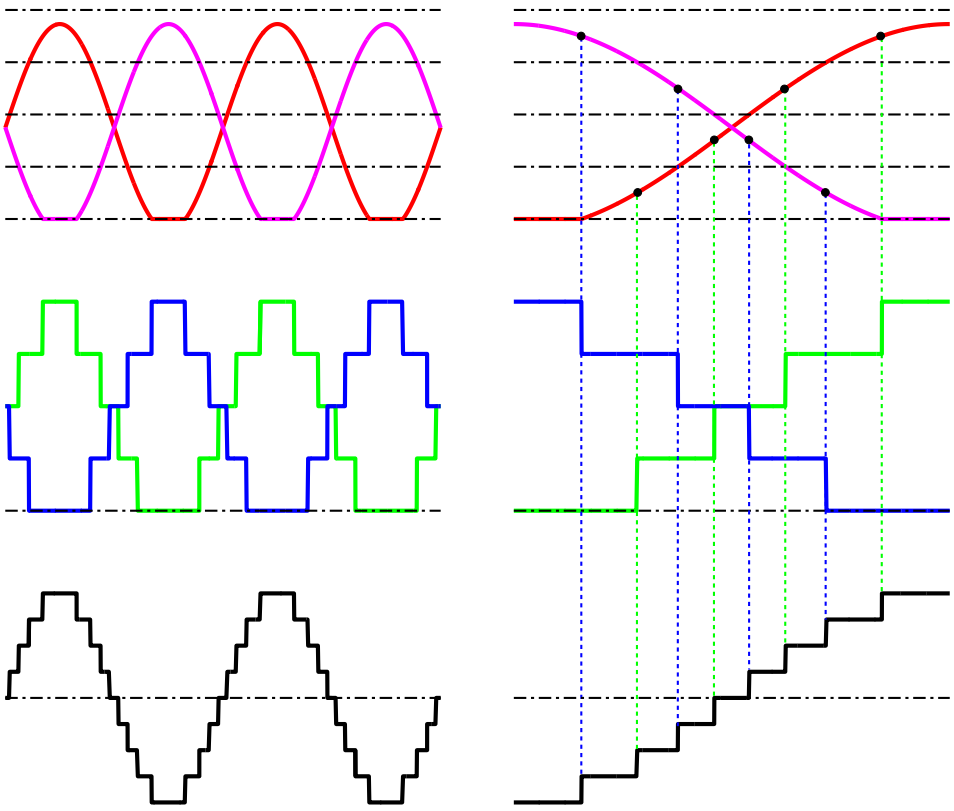


Figure 3.4: Zoomed version of (upper) reference signals, (middle) upper and lower arm voltages, (lower) converter output voltage: (a) with offset in reference voltages to generate $2n + 1$ voltage levels (b) zoomed version with offset in reference voltages to generate $2n + 1$ voltage levels

3.3 Analysis: Voltage balancing and circulating currents

To balance the floating capacitors in the MMC, the same voltage balancing can be employed as described in the previous chapter. The general state flow diagram is shown in Fig. 3.5.

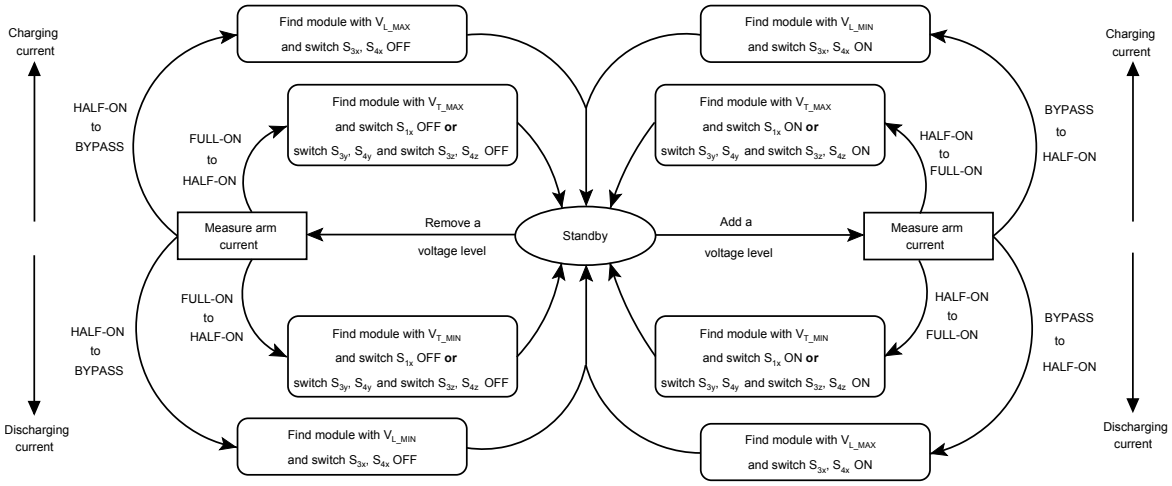


Figure 3.5: MMC voltage balancing

The voltage balancing control block assigns the ideal pulses generated from NLM block to the appropriate submodule of the MMC so as to maintain nominal capacitor voltages across all submodule capacitors. Arm current with capacitor voltages are given as feedback to the controller to make its decision. A comparison of voltage ripple in the capacitors at different output frequencies is shown in Fig. 3.6. The output load is varied with different frequency to maintain the same output current and hence same power. A few observations can be made:

1. The capacitor voltage ripple is inversely proportional to the frequency of generated voltage. It varies with double the fundamental frequency and hence with increase in frequencies, the ripple goes down.

2. The reduction in capacitor ripple voltage means there is less difference between the arm voltages and the DC bus which results in lower circulating currents.

The above two observations suggest that MMCs being used for power electronic transformers are even better than being used for HVDC grid applications since they require much smaller submodule capacitors and arm inductors. This is assuming the same ripple in capacitor voltages.

Using $n + 1$ voltage level generation method, the sum of arm voltages is always equal to the DC bus voltage and hence there are ideally no circulating currents, as shown in Fig. 3.7. This can result in very small arm inductors which are needed only during faults. In generating $2n + 1$ output voltage levels, the sum of arm voltages keeps jumping between the two highest voltage levels which results in choppy currents in the arms, as shown in Fig. 3.8. With this finite difference in voltages, the arm currents have sudden rise and fall in current waveform which happens at every voltage step level change. It is to be noted that with increase in number of voltage levels when the number of submodules is large, this ripple is significantly reduced. Otherwise, to suppress these currents, either a circulating current control strategy can be employed or the arm inductors can be made a little larger as compared to when needed for $n + 1$ voltage level generation. Overall, the capacitance and inductance requirement for MMC in PET applications would be smaller as compared to 60-Hz grid interface applications.

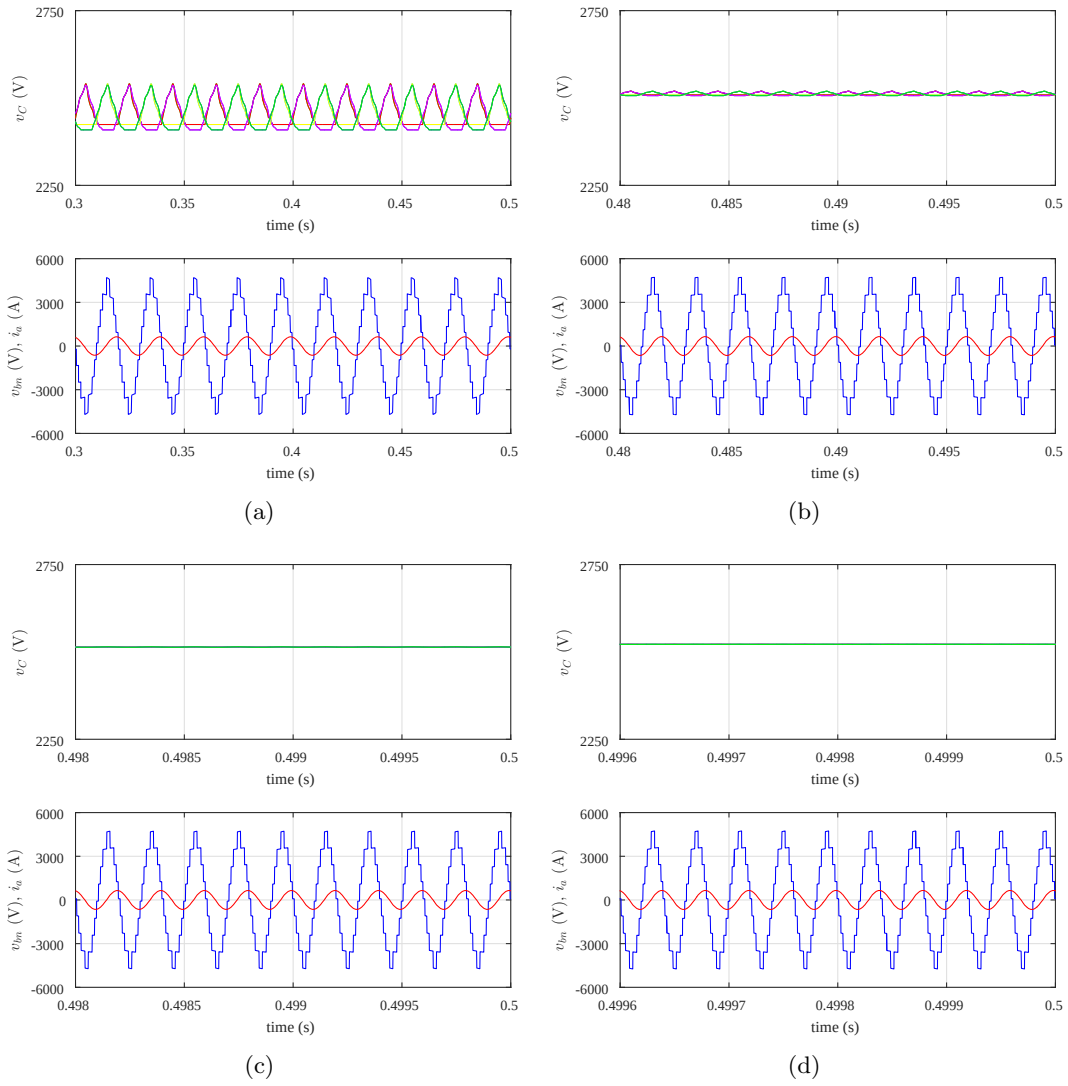


Figure 3.6: (upper) Capacitor voltages in upper arm and lower arm, (lower) converter output voltage and current for: (a) $f_o = 50$Hz (b) $f_o = 500$Hz (c) $f_o = 5$kHz (d) $f_o = 25$kHz

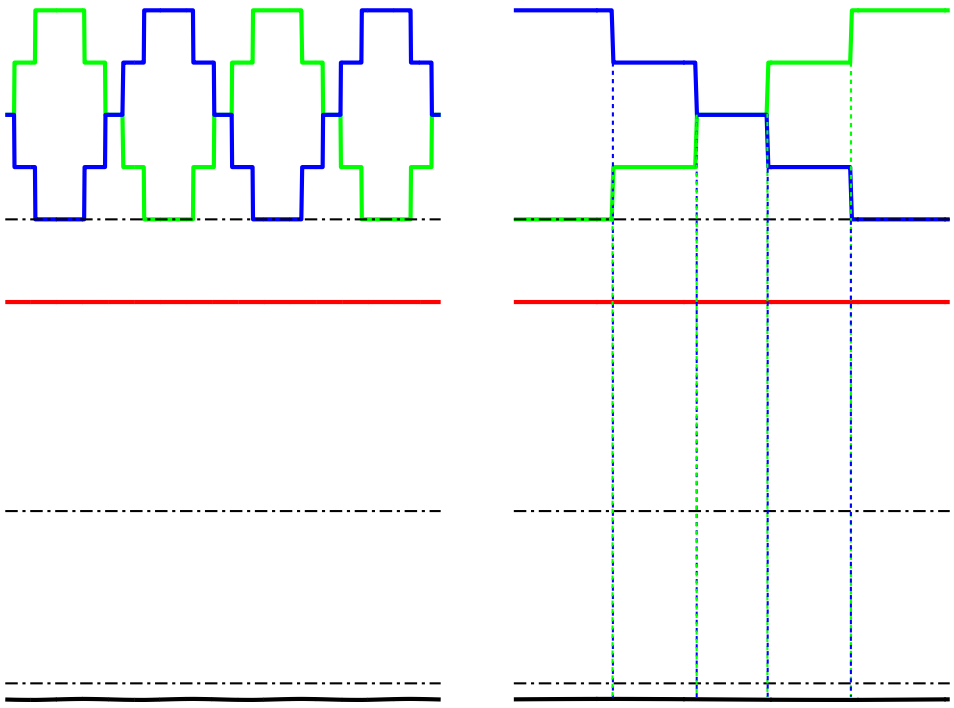


Figure 3.7: (upper) Upper and lower arm voltages, (middle) sum of upper and lower arm voltages, (lower) circulating current: (a) without offset in reference voltages to generate $n+1$ voltage levels (b) zoomed version without offset in reference voltages to generate $n+1$ voltage levels

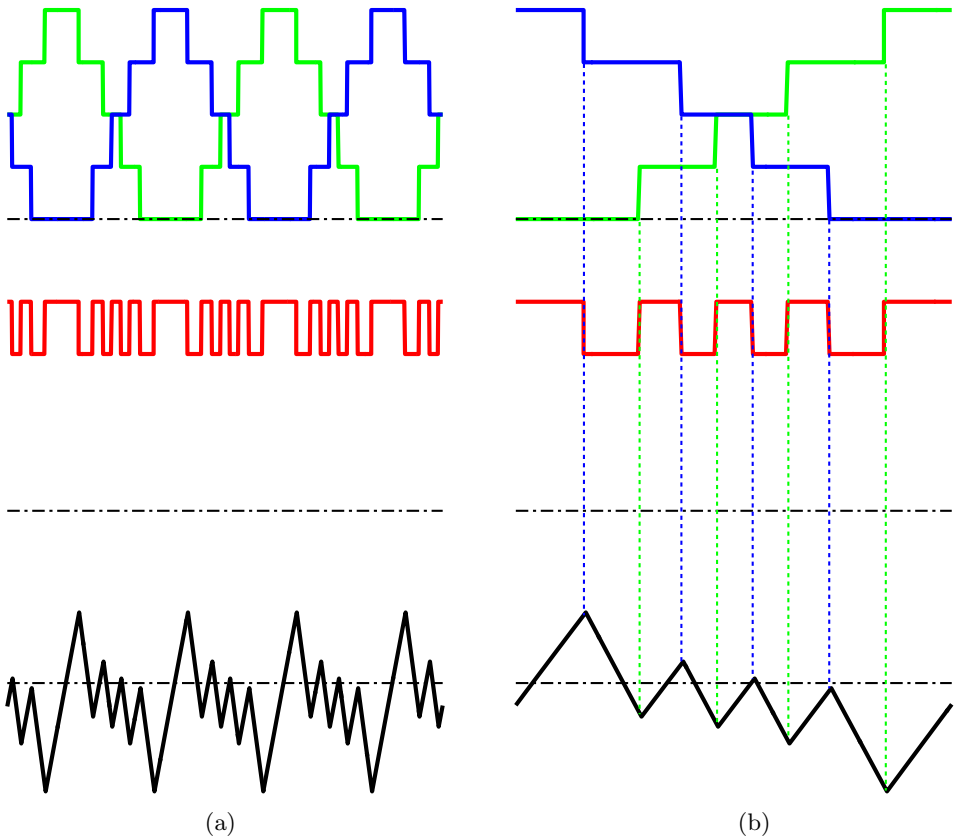


Figure 3.8: (upper) Upper and lower arm voltages, (middle) sum of upper and lower arm voltages, (lower) circulating current: (a) with offset in reference voltages to generate $2n + 1$ voltage levels (b) zoomed version with offset in reference voltages to generate $2n + 1$ voltage levels

3.4 Simulation Results

The MMC as shown in Fig. 3.1(b) is simulated with ideal switches in MATLAB/Simulink for a sending end HVDC station with parameters as shown in Table 3.1. The leg of the MMC is built using either 4 number of the 3-level submodules or 8 number of the 2-level submodules with half the number each in the upper and lower arm respectively. The output voltage of the converter is generated by nearest level modulation explained before. Both the $n+1$ and $2n+1$ output voltage generation NLM methods are implemented and the results are provided in this section. Voltage balancing similar to as described in the previous chapter is implemented using state machines. The reference voltage is set to generate an output voltage with modulation index $m = 1$ across an RL load. The generated output voltage is at $f_o = 2$ kHz. Circulating current control is not necessary at this high frequency and hence is not implemented. This section presents the simulation results in detail.

Table 3.1: Simulation for PET application: MMC parameters

Parameters	**Value**
Output load	$L_o = 75\mu$H, $R_o = 2\Omega$
DC bus voltage V_{dc}	10 kV
Submodule upper capacitor C_1	0.125 mF
Submodule lower capacitor C_2	0.250 mF
Arm inductor L_a	75μH
Output frequency	2 kHz

The first set of results are with $n+1$ output voltage generation method. Here two sinusoidal waveforms are used for output voltage generation which correspond to the upper arm and lower arm voltage references. As described in previous sections, since the capacitor voltage ripple becomes smaller at higher frequencies, the capacitance values have been reduced accordingly. The capacitors were designed for a ripple of 5% of rated voltage at 50 Hz. Hence for $f_o = 2$ kHz, the capacitors used are 1/40 times as used previously. Thus the capacitance requirement has been reduced a lot for PET applications.

The vaious waveforms of capacitor voltages, arm voltages and currents with converter output voltages and currents are shown in Fig. 3.9(a) using 2-level submodules and in Fig .3.9(b) using 3-level submodules respectively.

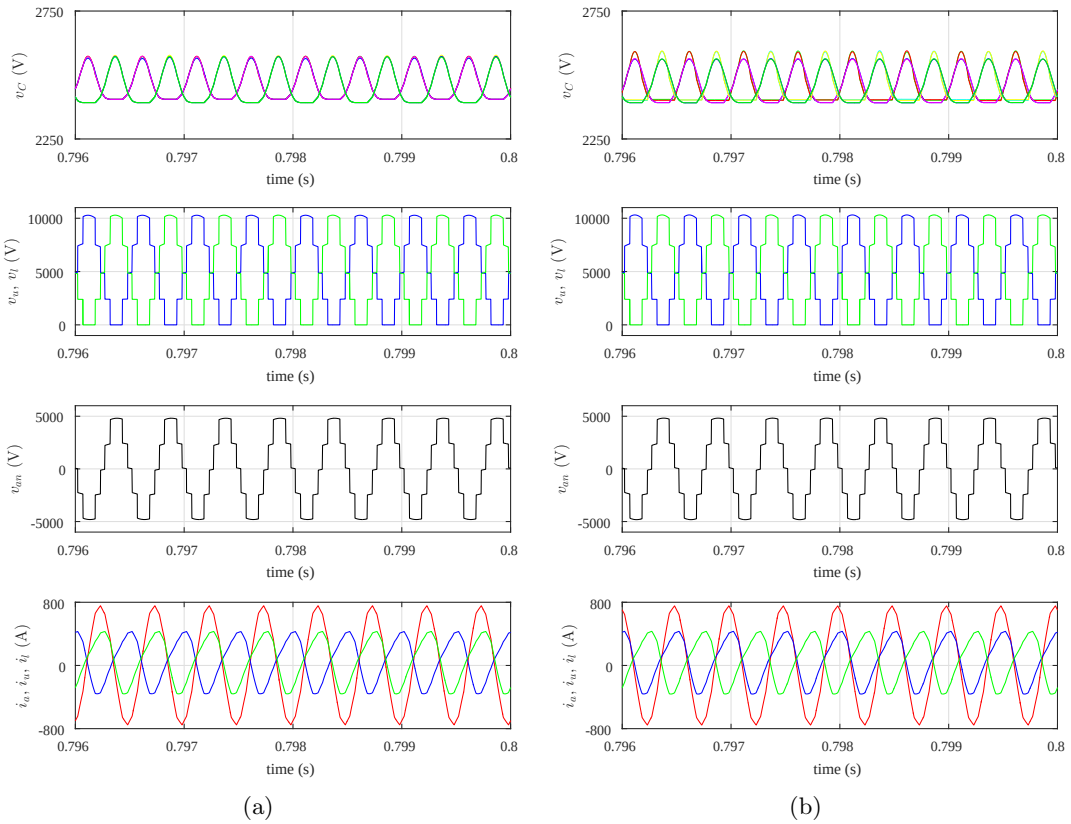


Figure 3.9: (top to bottom)Capacitor voltages in upper arm and lower arm, upper arm and lower arm voltages, converter output voltage, arm currents with output line current for (a) $n+1$ modulation using 2-level submodules (b) $n+1$ modulation using 3-level submodules

The capacitor voltage ripple is approximately 125 V which is 5% of the rated capacitor voltage of 2.5 kV. The 3-level submodules have four distinct waveforms showing the waveforms for upper arm and lower arm capacitor voltages in C_1 and C_2 capacitor pairs respectively. The arm voltages have 5 distinct voltage levels. Due to no offset in the reference signals, the arm voltages are exactly 180° out of phase and hence the difference between them results in an output voltage with 5 voltage levels. This is in sync with the description in the previous sections. Since the fundamental frequency is itself very high, the need for arm current suppression is not necessary. The arm inductors here have been also reduced to prevent voltage drop across them. The arm currents are shown in Fig. 3.9(a) using 2-level submodules and in Fig .3.9(b) using 3-level submodules respectively which have very low higher order harmonics. The harmonics do not get reflected in the output current of the MMC which is near sinusoidal with very low harmonic content.

By introducing a negative bias of $V_{dc}/16$ in the reference signals of the upper and lower arms, the $2n + 1$ output voltage NLM method is implemented. The results are shown in Fig. 3.10(a) using 2-level submodules and in Fig .3.10(b) using 3-level submodules respectively. Similar to the $n + 1$ NLM method, this also results in 5 distinct voltage levels in the upper and lower arms as shown in Fig. 3.10(a) and Fig. 3.10(b) (second from top). However now they have a small phase-shift introduced between them because of the modified reference signals. Hence the difference between lower and upper arm voltage resulting the converter output voltage has 9 voltage levels as shown in 3.10(a) and Fig. 3.10(b) (third from top). With double the number of voltage levels compared to previous method, the voltage is more close to a near sinusoid now which could result in lower core losses in the transformer. This comes at the penalty of higher circulating currents in the arms as shown in 3.10(a) and Fig. 3.10(b) (bottom). The non-zero voltage difference between the sum of arm voltages and DC-bus results in the sharp rise and fall in arm currents. This has been described in the modulation section in detail. To reduce these sharp rise and fall in arm currents, the arm inductors needed in $2n + 1$ NLM method is higher than the previous method of generating $n + 1$ voltage levels. However, the output current is sinusoidal without any of these harmonics in arm currents. The additonal harmonics in the arm currents also increases the ripple in the capacitor voltages as seen in the top plots.

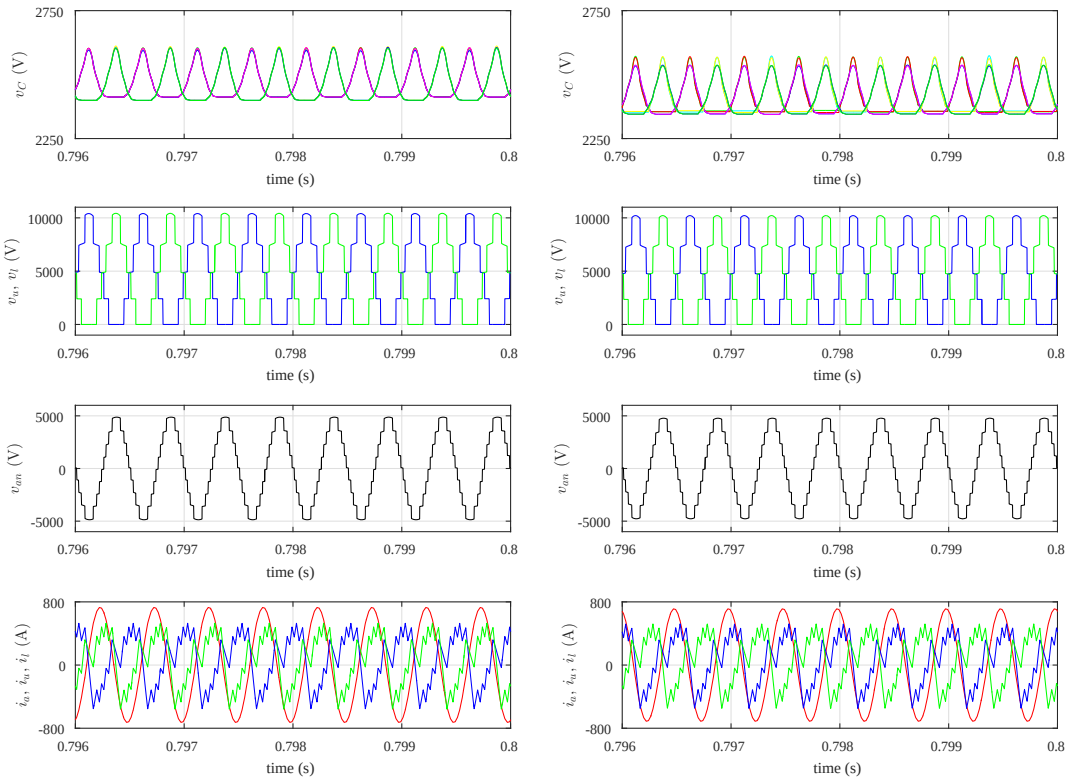


Figure 3.10: (top to bottom)Capacitor voltages in upper arm and lower arm, upper arm and lower arm voltages, converter output voltage, arm currents with output line current for (a) $2n+1$ modulation using 2-level submodules (b) $2n+1$ modulation using 3-level submodules

3.5 Experimental results

Experimental results were obtained on the scaled down laboratory prototype using single-phase MMC operation. The results validate the theory described in previous sections. Closed loop circulating current control was not implemented as high frequency voltage generation does not necessitate its need. Hysteresis based voltage balancing is implemented to result in stable operation of the capacitor voltages. 3-step commutation with 0.5 μs commutation interval is implemented for safe commutations between switching transitions. The experimental parameters are given in Table. 3.2. The capacitor used are the same as before and hence the ripple in capacitor voltages is minimized. The arm inductors have been reduced for high frequency generation. Output voltage at 1 kHz with a modulation index of 0.85 is generated using nearest level modulation techniques described in this chapter using both 2-level and 3-level submodule based MMC. Voltage is generated across an RL load where inductance L_o is chosen close to what is to be expected from leakage inductance of a high frequency transformer. The output resistance is the equivalent resistance representing the secondary side power converter of the PET.

Table 3.2: Experimental for PET application: MMC parameters

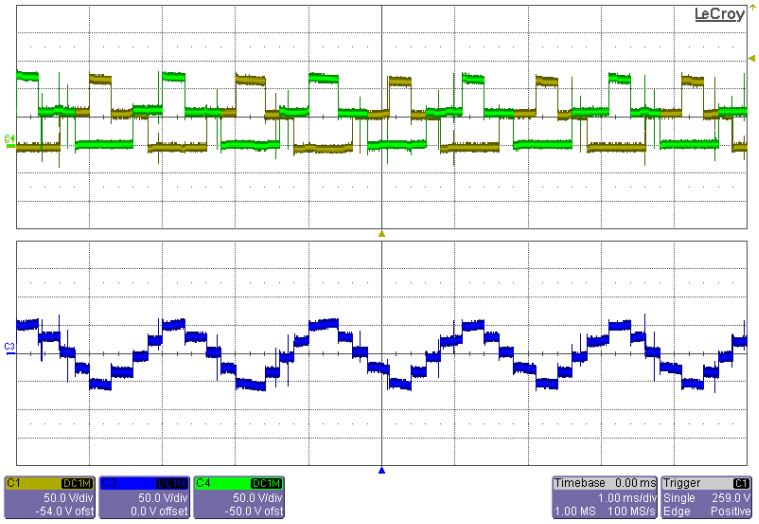
Parameters	**Value**
Output inductance L_o	2 mH
Output resistance R_o	20 Ω
DC bus voltage V_{dc}	100 V
Submodule upper capacitor C_1	1.1 mF
Submodule lower capacitor C_2	2.2 mF
Arm inductor L_a	0.3 mH
Output frequency	1 kHz

The first set of results is using 2-level submodules. The 3-level submodules built can be made to operate as 2-level submodules by sending zero gate signals to the bidirectional switches in each submodule. Thus 4 submodules are present in the leg of the

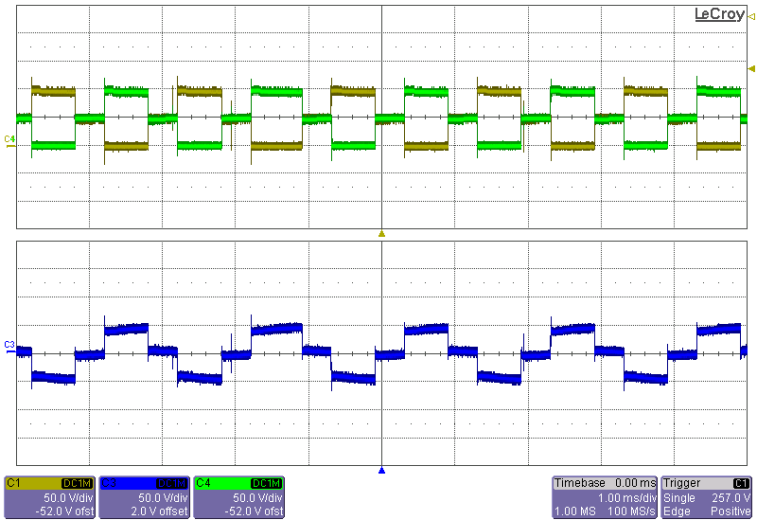
MMC. The upper and lower arm voltages are shown in Fig. 3.11(a) (top) and Fig. 3.11(b) (top). The difference in the two plots in terms of output voltage synthesis exists in the method implemeneted for number of output voltage levels. Fig. 3.11(a) (bottom) shows the output voltage using $2n + 1$ output voltage levels method, hence 5 distinct voltage steps can be seen using 4 submodules. It is seen that the upper and lower arm voltages have a small phase-shift between them which results in these additional voltage levels. On the other hand, Fig. 3.11(b) (bottom) has just 3 voltage levels same as the arm voltages because of no offset added to the reference signals for NLM.

As described in previous sections, using $2n + 1$ voltage level generation method results in an unbalance in arm voltages and DC bus voltage which results in sharp edges in arm currents as seen in Fig. 3.12(a) (top). This does not show up using $n + 1$ voltage level generation method as shown in Fig. 3.12(b) (top). The output currents however do not have any sharp edges and are near sinusoidal. Hence. the arm inductor requirement in the $2n + 1$ voltage generation method is higher, but it results in double the number of voltage levels, thus improving its quality.

Similar results are obtained using the 3-level submodules. Fig. 3.13(a) (top) and Fig. 3.13(b) (top) show the arm voltages which have 5 voltage levels. Depending on whether the reference signals had an offset in them, these are either in phase or phase shifted to result in higher number of output voltage levels. The output voltage generated has either 9 or 5 voltage levels as shown in Fig. 3.13(a) (bottom) and Fig. 3.13(b) (bottom). Similar to the 2-level submodules, the arm currents follow a similar trend. Using $2n+1$ voltage level generation method, sharp edges in arm currents exist with smaller steps as seen in Fig. 3.14(a) (top). These are continuous using $n + 1$ voltage level generation method as shown in Fig. 3.14(b) (top). The additional jumps in current occur at the output voltage levels.

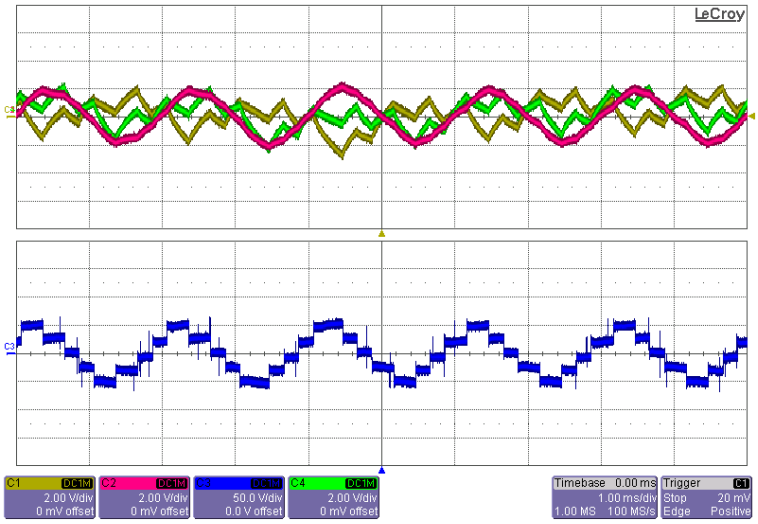


(a)

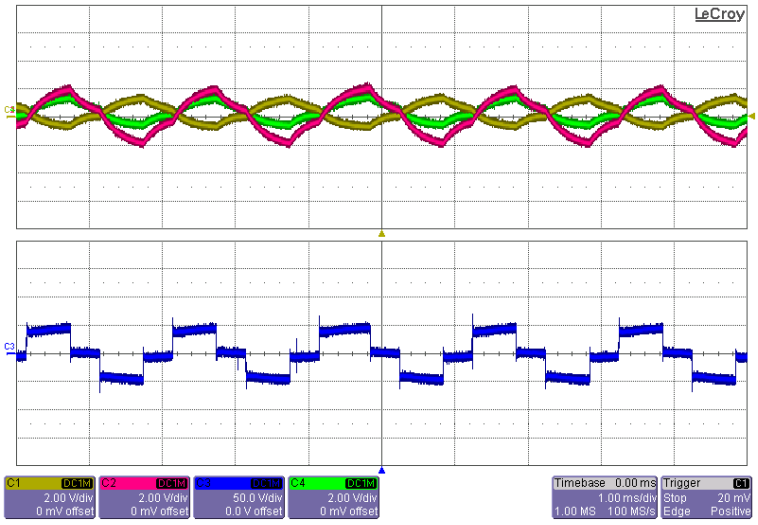


(b)

Figure 3.11: Nearest level modulation results using 2-level submodules: (top to bottom) Upper and lower arm voltages, converter output phase voltage for: (a) modulation method with $2n + 1$ output voltage levels (b) modulation method with $n + 1$ output voltage

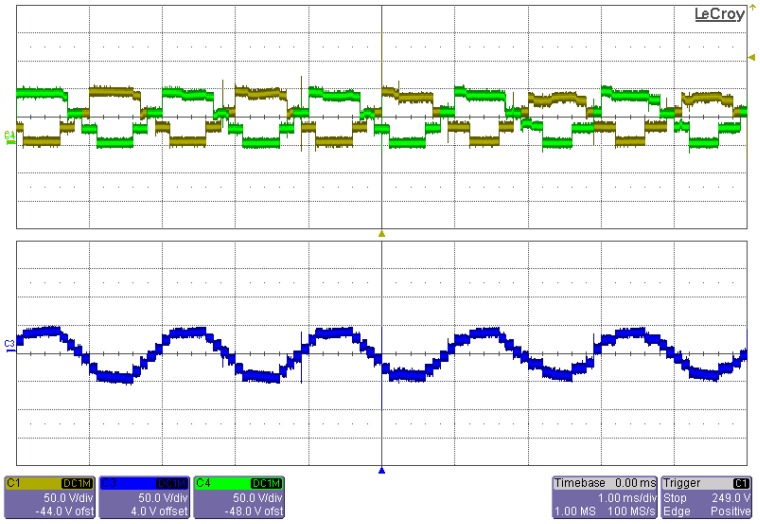


(a)

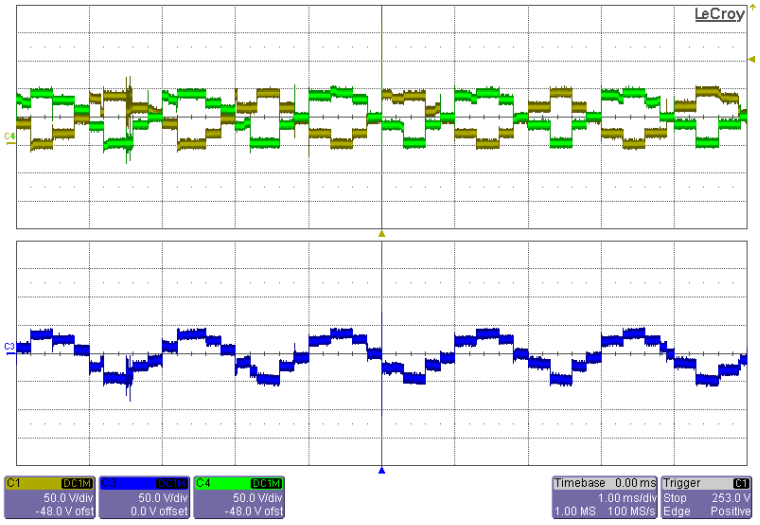


(b)

Figure 3.12: Nearest level modulation results using 2-level submodules: (top to bottom) Upper and lower arm currents with output current, converter output phase voltage for: (a) modulation method with $2n + 1$ output voltage levels (b) modulation method with $n + 1$ output voltage

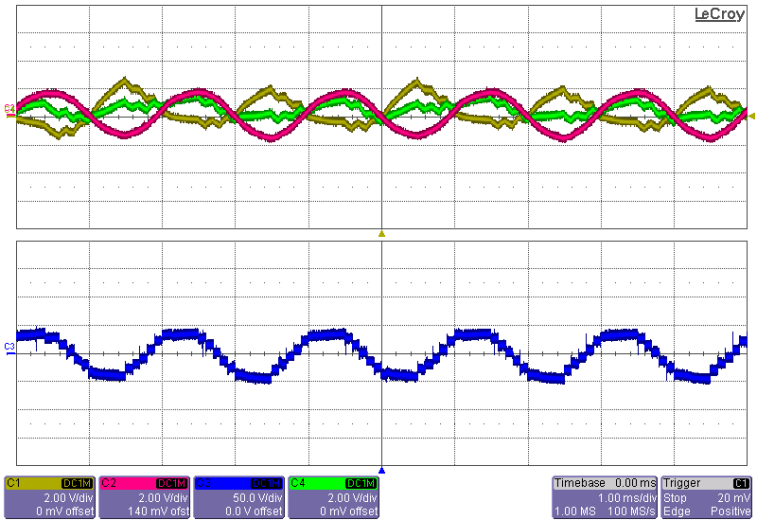


(a)

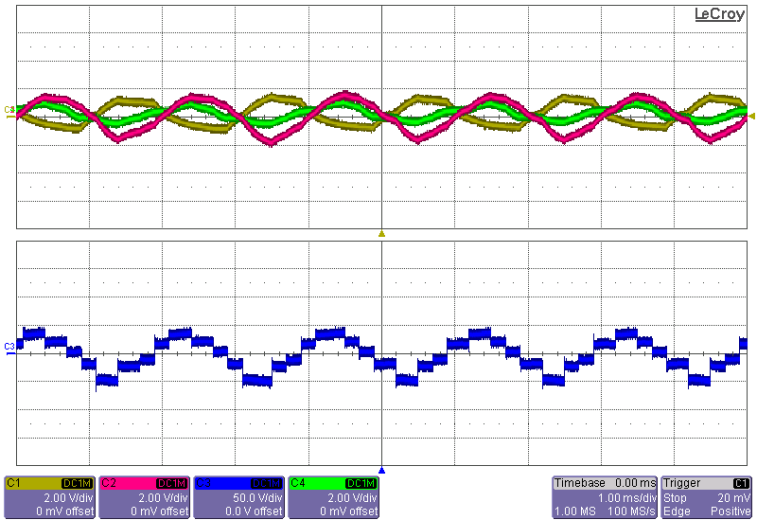


(b)

Figure 3.13: Nearest level modulation results using 3-level submodules: (top to bottom) Upper and lower arm voltages, converter output phase voltage for: (a) modulation method with $2n + 1$ output voltage levels (b) modulation method with $n + 1$ output voltage



(a)



(b)

Figure 3.14: Nearest level modulation results using 3-level submodules: (top to bottom) Upper and lower arm currents with output current, converter output phase voltage for: (a) modulation method with $2n + 1$ output voltage levels (b) modulation method with $n + 1$ output voltage

Table 3.3: Comparison of different MMC modulation methods for PET application

Methods	**PWM** $f_s = 2f_o$	**PWM** $f_s = 10f_o$	**NLM** $n+1$ **levels**	**NLM** $2n+1$ **levels**
Switching frequency	$2f_o$	$10f_o$	$\approx f_o$	$\approx f_o$
Output voltage THD	=	lowest	high	low
Circulating currents	=	low	lowest	=
Capacitor voltage ripple	=	low	lowest	=
Losses	=	high	lowest	low

3.6 Summary

Analysis of modulation, voltage balancing and circulating currents is presented for operation of MMC to generate near sinusoidal voltages in kHz range. Nearest level modulation with $n+1$ and $2n+1$ output voltage levels is investigated and effects on voltage balancing and circulating currents is analysed. It is observed that in the MMC interfacing the HFT, the arm inductors and floating capacitors can be substantially small compared to the MMC for grid integration. A comparison of different modulation techniques is shown in Table 3.3 and validated with simulation and experimental results.

Chapter 4

Single-stage HVDC/AC Power Electronic Transformer

Power electronic transformer consisting of power converters and a high frequency transformer (HFT) can be used to interface a low voltage machine to a high voltage grid. A modular multilevel converter (MMC) is proposed as the power converter on the high voltage side to generate high frequency, adjustable magnitude sinusoidal voltages. A matrix converter (MC) is used on the low voltage side to synthesize three-phase adjustable frequency PWM AC at the machine terminals. With the leakage inductance of the transformer, a capacitor bank forms an LC filter to result in sinusoidal currents through the HFT. With sinusoidal voltages and currents through the transformer, there is significant reduction in transformer losses and also natural commutation of leakage energy is obtained. The magnitude of the output voltage requirement by the machine is met by controlling the output voltage of the MMC on the primary of the HFT, to result in reduced voltage stress and losses in the transformer, secondary side converter and the machine. The operating principle, modulation and control of the proposed PET is validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.

4.1 Introduction

In the modern distribution system, power transformers play an important role in voltage boosting and providing galvanic isolation for protection. Replacement of line frequency transformers with power electronic transformers (PET) results in significant reduction in volume and weight along with added advantages like high power density, voltage regulation, power factor control, on demand reactive power support, etc [7]. This kind of transformer topologies find wide applications in interfacing renewables (solar, wind), traction, medium voltage ASDs, energy storage systems, UPS, mobile substations, etc.

Various PET topologies exist in literature [71]. Most PET configurations involve three stage power conversion [72] [73]. Two stage PET has the secondary side to be a direct AC/AC converter like a cycloconverter [74]. For high voltage and high power applications, PET topologies have to be connected in series/parallel due to limitation of power semiconductor device ratings. In [75], basic building blocks of isolated DC/DC converter made from DC/AC inverter and current source AC/DC converter with a medium frequency transformer are connected in input series-output parallel configuration. A HVDC transmission line is formed in [76] by series connection of PET modules involving a diode bridge rectifier on the secondary side of the high frequency transformer (HFT) in each module. Use of multilevel topologies like neutral point clamped converter [77] is difficult to scale. Cascaded H-bridge multilevel converter based PET have been widely discussed [78] [79]. Recently the modular multilevel converter (MMC) has emerged as a viable solution for high voltage applications because of its easy scalability to reach high number of voltage levels by simple series connection of submodules, resulting in higher reliability and easy maintenance [28]. Modular converters involving 3-stage power conversion with a dual active bridge and HFT in each module is given in [14]. Use of large number of conversion stages involves intermediate bulky energy storage elements and results in reduced power density and efficiency. Matrix converter based single stage PETs are discussed in [80] [81]. However these topologies cannot be used for high voltage applications and require additional techniques for commutation of leakage energy.

All of the previous modular PETs discussed above for high voltage applications involve a HFT in each module and multiple conversion stages. Also the HFT is subjected

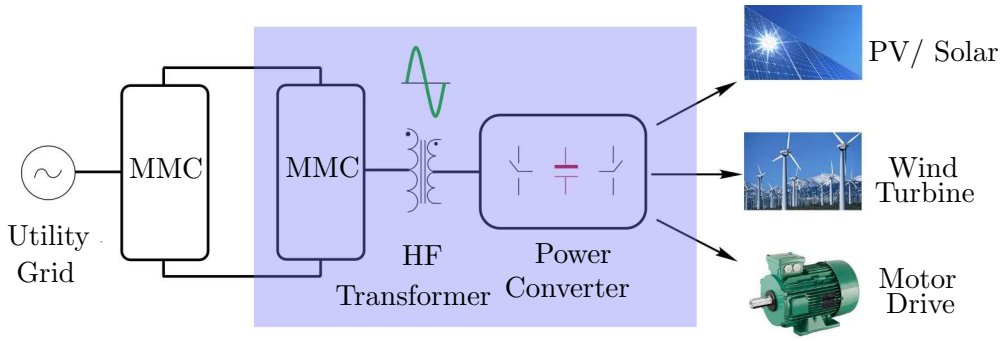


Figure 4.1: Block diagram of HVDC/AC MMC-based PET

to switched voltages/currents which is more lossy. The proposed PET topology involving MMC is shown in Fig. 4.1 [17]. It includes a two stage bidirectional AC/DC and DC/AC stage where the primary is at high or medium voltage and the machine is operated at low voltage. The DC bus could be very short as in the case of onshore wind farms or medium voltage drives. It could also be 100 miles HVDC line for offshore wind farms. The proposed topology results in sinusoidal voltages and currents through the HFT resulting in significant reduction of transformer losses and size. Also due to sinusoidal currents, natural commutation of leakage energy is obtained. This chapter focuses on single-stage HVDC to AC operation, which is a subset of Fig. 4.1 as highlighted.

The proposed topology with its working principle is presented in Section 4.2. Section 4.3 presents the individual modulation of the primary and secondary side converters, followed by modulation of the combined PET topology. The design of high frequency link filter capacitor is presented in Section 4.4. The proposed control of primary side MMC to meet the output voltage variation is given in Section 4.5. Key results are presented in Section 4.6 and 4.7 and performance evaluation of the modifed control is presented in Section 4.8. The chapter concludes in Section 4.9.

4.2 Topology

A partial circuit of Fig. 4.1 is a single stage HVDC to AC power electronic transformer topology to interface the high voltage DC bus with the low voltage machine. To meet

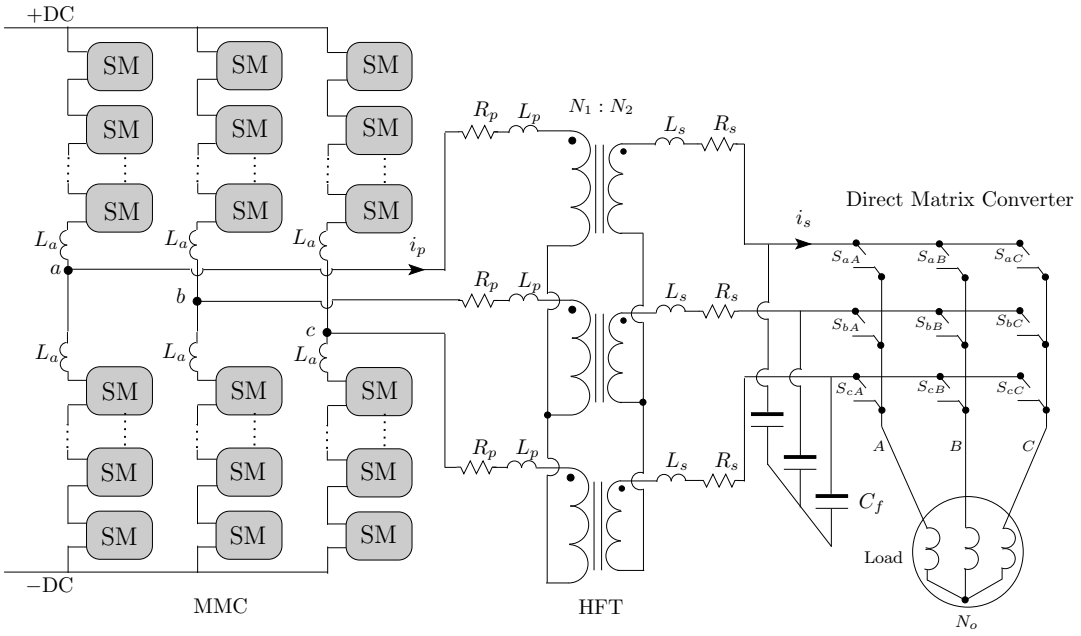


Figure 4.2: Proposed power electronic transformer topology variant 1

the device stress on the high voltage side, a multilevel structure using a modular multilevel converter is proposed. The MMC is modulated to synthesize high-frequency near sinusoidal voltages at the primary of the high frequency transformer. A single-stage matrix converter is used to convert these high-frequency sinusoidal voltages to synthesize 3-phase sinusoidal voltages of desired low frequency across the machine. Two variants of the matrix converter can be used which leads to the two topologies as shown in Fig. 4.2 and Fig. 4.3. This section describes the topology in detail.

On the high voltage side, a 3-phase MMC topology is used. Each leg of the MMC is made up of two arms consisting of n series connected submodules (SM). The internal structure of the submodule can be the conventionally used 2-level half bridge submodule (Fig. 4.4(a)) or the proposed 3-level submodule (Fig. 4.4(b)). The 3-level submodule has added advantages over the half bridge submodule as it results in nearly half the submodule requirements resulting in a more compact structure and significantly reduced semiconductor losses [29].

The 3-phase medium/high frequency transformer is made up of three 2-winding

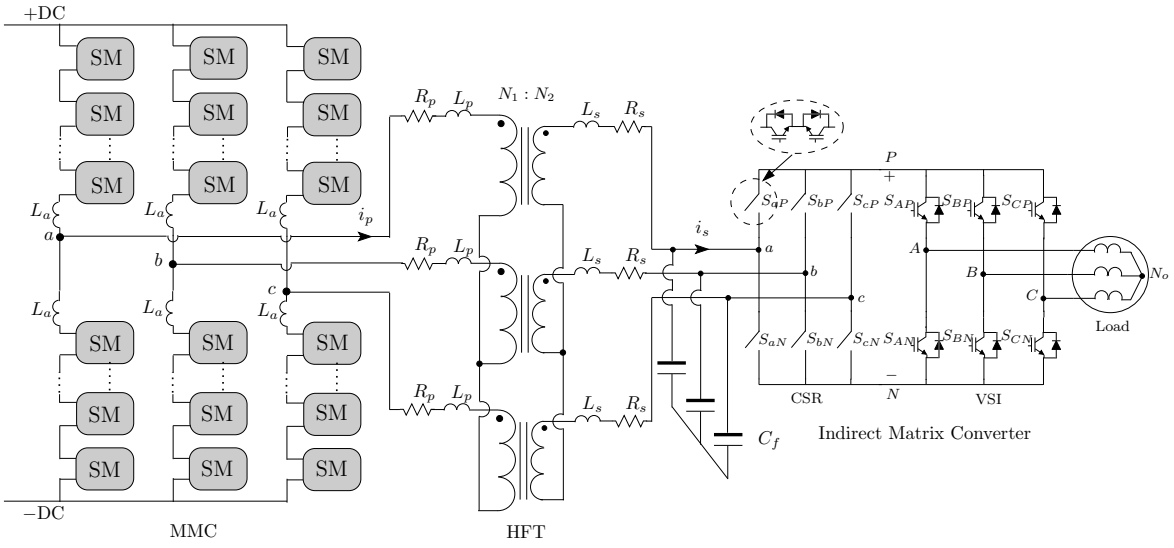


Figure 4.3: Proposed power electronic transformer topology variant 2

transformers with $N_1 : N_2$ turns ratio . Every transformer has leakage inductance in its winding. L_p, R_p are the primary winding leakage inductance and parasitic resistance. Similarly L_s, R_s are the secondary side leakage inductance and parasitic resistance. Instead of using three 2-winding transformers, a 3-phase high frequency transformer could also be used.

The secondary low voltage side of the HFT is connected to a 3×3 direct matrix converter (DMC) or a indirect matrix converter (IMC). A DMC is a one-stage matrix converter consisting of nine bi-directional switches which allows the three output phases to be connected to any of the three input phases directly as shown in Fig. 4.2. An IMC on the other hand is a quasi two-stage matrix converter which is configured as a combination of transformer linked current source rectifier (CSR) and machine interfaced voltage source inverter (VSI) connected by a virtual DC-link, as shown in Fig. 4.3. The performance of the IMC is similar to the DMC in terms of output and input waveforms but has lesser commutation problems compared to the DMC. From the sinusoidal voltages produced by the MMC, the matrix converter generates 3-phase PWM AC of desired frequency. It uses an array of controlled bidirectional switches to couple a 3-phase high frequency link with the 3-phase low frequency machine without the need

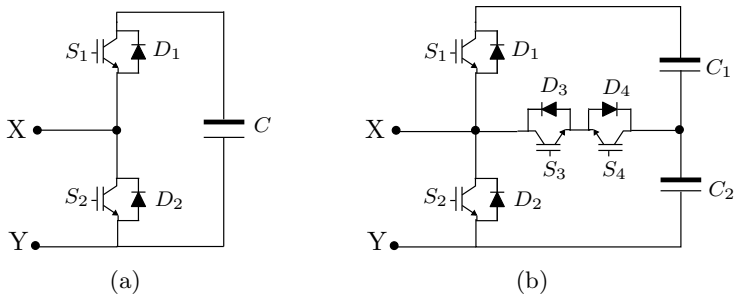


Figure 4.4: (a) 2-level submodule (a) 3-level submodule

of any intermediate energy storage elements, thus resulting in a single-stage conversion with high power density. Because of pulse-width modulation (PWM), the MC injects high frequency switching components into its input current. Hence an LC filter is required. Here the leakage inductance of the transformer is used along with an externally added very small capacitance C_f for filtering action. This results in sinusoidal currents through the HFT. Thus the proposed topology results in sinusoidal voltages and sinusoidal currents through the HFT, thus significantly reducing the transformer losses.

4.3 Modulation

The modulation of the proposed PET consists of the modulation of the MMC on the high voltage side and the matrix converter interfaced to the machine. The modulation of MMC for this application is described in detail in Chapter 3. An indirect space vector modulation approach for the matrix converter is employed which is described in detail in this section.

4.3.1 Modulation of primary side MMC

The MMC can be modulated using carrier based PWM scheme or fundamental frequency based nearest level modulation, as described in Chapter 3. Two reference signals are used in each leg for comparison with the carriers to generate gate signals for the upper arm and lower arm respectively. Nearest level modulation is preferred for such application to result in lower switching losses.

This modulation results in 3 states of the MMC submodule: FULL-ON state (S_1=1),

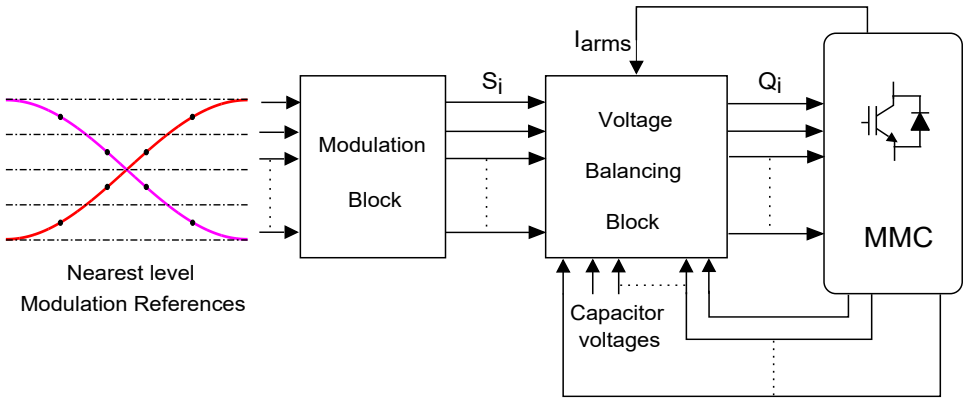


Figure 4.5: MMC control blocks for PET

HALF-ON state (S_3, S_4=1) and BYPASS state (S_2=1). Based on this modulation, unequal capacitance division of $C_1 = C/3$ and $C_2 = 2C/3$ is used which can balance the capacitor voltages naturally in ideal conditions. A voltage balancing algorithm based on a sorting algorithm monitors and sorts the capacitor voltages and then allocates the appropriate gate signal to the corresponding submodule IGBT. The modulation block generates ideal gate pulses S_i which is allocated in the voltage balancing block to the appropriate IGBT. The voltage balancing block then generates the actual gate signals Q_i for each IGBT inside every submodule. Because of high frequency operation, the arm inductors provide sufficient impedance to suppress the circulating currents, hence its control is not necessary. The control blocks for the entire MMC modulation is shown in Fig. 4.5.

4.3.2 Modulation of machine connected Matrix Converter

Space vector pulse-width modulation (SVPWM) is used to control the switching states of the matrix converter to result in sinusoidal output voltages and draw sinusoidal currents at the high frequency transformer terminals. In SVPWM of matrix converter, there are twenty seven switching states: eighteen stationary active vectors, six synchronously rotating vectors and three zero vectors. SVPWM of matrix converter can be direct modulation using synchronously rotating vectors or indirect modulation where the IMC topology is taken as reference and switching vectors leading to switching states are derived using active vectors. Every vector of the rectifying stage formed by a CSR and

the inverting stage formed by a VSI corresponds to a particular switching state which leads to a particular state of operation of the matrix converter. Direct modulation using synchronous vectors can result in zero common mode voltages at the machine terminal but result in lower voltage transfer ratio of 0.5. This can be offset by designing the turns ratio of the transformer to accommodate it. Indirect modulation achieves highest possible voltage transfer ratio of 0.866 in the matrix converter [82]. This section describes the indirect modulation scheme of operation of the MC.

In indirect modulation, the matrix converter is modulated using two fictitious converters, a current source rectifier (CSR) and a voltage source inverter (VSI) connected through a virtual DC-link. The switching states are shown in Fig. 4.6(a) and Fig. 4.6(b) respectively. Both of these converters together produce 18 active switching states. For example, state [a b b] in the MC in which a is connected to output phase A and, b is connected to output phase B and C respectively can be implemented by simultaneously applying [a b] and [1 0 0] by the indirect modulation. In this analysis, space vector corresponding to a set of 3-phase quantities x_a, x_b, x_c is a complex vector X as given in (4.1). The MC converts the high frequency link voltages to low frequency voltages at the machine terminals. Hence the switching frequency of the matrix converter f_s is set higher than the transformers link frequency f_{link} i.e $f_s >> f_{link}$.

$$X = x_a + x_b e^{j2\pi/3} + x_c e^{-j2\pi/3} \tag{4.1}$$

The space vector diagram of the CSR comprises of six active current vectors ($I_1 - I_6$) as shown in Fig. 4.6(a) and three zero current vectors. For every input phase $x \in a, b, c$, switches S_{xP} and S_{xN} can take values of 0 or 1. "$S_{xP} = 1$" or "$S_{xN} = 1$" implies that the input phase x is connected to the positive pole "P" or negative pole "N" of the DC-link respectively. In one sampling cycle $T_s = 1/f_s$, the reference current space vector $\overline{\mathbf{I}}_\mathbf{s}$ is generated from two adjacent active vectors and one zero vector, whose duty ratios are given by (4.2). Here m_I is the ratio of the peak of the fundamental component of the transformer link current to the average virtual DC-link current and β is the corresponding angle between the first vector and reference vector.

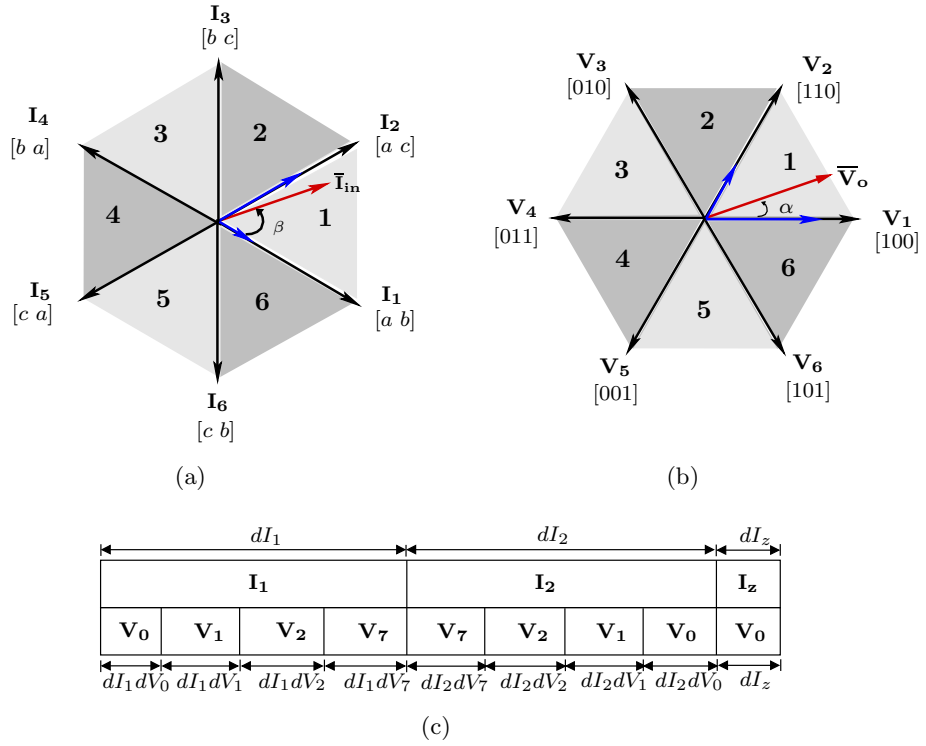


Figure 4.6: (a) Current space vectors produced by CSI (b) Voltage space vectors produced by VSI (c) Switching sequence of Matrix converter

$$
\begin{aligned}
dI_1 &= m_I \sin\left(\frac{\pi}{3} - \beta\right) \\
dI_2 &= m_I \sin\beta \\
dI_z &= 1 - dI_1 - dI_2
\end{aligned} \tag{4.2}
$$

The modulation of the CSR generates a pulsating DC-link voltage made up of the line-line transformer link voltages which has different voltage levels. The VSI modulates the output from this variable DC-link voltage. The space vector diagram of the inverting stage comprises of six active vectors (V_1-V_6) and two zero vectors (V_0,V_7) as shown in Fig. 4.6(b). The switching function of this stage is defined as $S_y = 1(y = A, B, C)$ when the switch is ON or $S_y = 0$ when that switch is OFF. The bottom switches have complementary switching signals. To generate three-phase output voltages, the

reference output voltage space vector $\overline{\mathbf{V}}_{\mathbf{o}}$ is generated by the use of two adjacent active vectors and one zero vector whose duty ratios are given by (4.3) where m_V is the ratio of the peak of the fundamental component of the output voltage to the average virtual DC-link voltage and α is the angle between the first vector and reference vector.

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha \\ dV_z &= 1 - dV_1 - dV_2 \end{aligned} \tag{4.3}$$

The switching sequence applied over a sampling cycle is given in Fig. 4.6(c). The peak of the average output voltage V_o can be written in terms of the peak of the transformer side link voltage V_s as in (4.4). Similarly the peak of the link current I_s on the secondary of the transformer can be written in terms of the peak of the load current I_o as given in (4.5) where ϕ_o is the load power factor angle.

$$V_o = \frac{3}{2} m_I m_V V_s \tag{4.4}$$

$$I_s = \frac{3}{2} m_I m_V I_o \cos\phi_o \tag{4.5}$$

4.3.3 Combined modulation of PET

For the proper operation of the PET, both the primary and secondary converters should operate synchronously. The net output voltage generated depends upon the modulation indices of both the converters along with the transformation ratio of the HFT. The peak output voltage synthesized can be represented in terms of the input high voltage DC bus as shown in (4.6). Here m_p is the modulation index of the primary side MMC and $m_s = m_I m_V$ is the modulation index of the secondary side matrix converter connected to the machine. The high voltage DC-bus current can be represented in terms of the peak output load current as shown in (4.7).

$$V_o = \frac{3}{2}\frac{N_2}{N_1} m_p m_s V_{dc} \tag{4.6}$$

$$I_{dc} = \frac{3}{2}\frac{N_2}{N_1} m_p m_s I_o \cos\phi_o \tag{4.7}$$

4.4 High frequency link filter design

Due to pulse-width modulation, the matrix converter injects high frequency switching harmonics over the fundamental link frequency in the secondary current of the HFT. As mentioned in the previous section, the modulation of the matrix converter is done at a switching frequency which is higher than the link frequency. To result in sinusoidal currents flowing through the HFT, a low pass LC filter is designed. The leakage inductance of the transformer forms this filter with an externally added small capacitance. The leakage inductance L_{lkg} is the combination of the secondary side leakage inductance L_s and the primary leakage inductance L_p referred to the secondary side as given by (4.8). The leakage resistance is obtained similarly in (4.9).

$$L_{lkg} = L_p \left(\frac{N_2}{N_1}\right)^2 + L_s \tag{4.8}$$

$$R_{lkg} = R_p \left(\frac{N_2}{N_1}\right)^2 + R_s \tag{4.9}$$

The RMS of the input current $\langle i_s \rangle$ of the matrix converter from space vector modulation is derived in [83, 84] and given by (4.10). The RMS of the switching components $\langle \widetilde{i_s} \rangle$ occurring at multiples of the MC switching frequency f_s are given by (4.11). The per phase equivalent circuit of the MC at its switching frequency is shown in Fig. 4.7. Here the harmonics injected by the matrix converter switching is represented by $\langle \widetilde{i_s} \rangle$. Since the MMC generates near sinusoidal voltages, it is represented by a short at the matrix converters switching frequency. Assuming all of the ripple components to be at the switching frequency of the matrix converter, a low pass filter can be designed with a corner frequency between the link frequency and switching frequency. $\langle i'_p \rangle$ is the reflected current from the primary side of the transformer ($\langle i'_p \rangle = \frac{N_1}{N_2} i_p$).

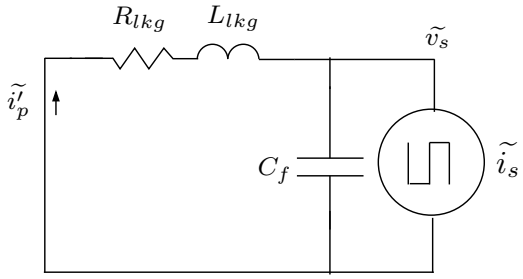


Figure 4.7: Per-phase equivalent circuit of the matrix converter with input filter at the matrix converters switching frequency

$$\langle i_s \rangle^2_{RMS} = \frac{3\sqrt{3} m_I m_V I_o^2}{\pi^2} \left(\frac{\pi\sqrt{3}}{12} + \frac{3}{8} \right) (1 + \cos 2\phi_o) + \frac{3\sqrt{3} m_I m_V I_o^2}{\pi^2} \left(\frac{\pi}{12} - \frac{\sqrt{3}}{16} \right) \sin 2\phi_o \tag{4.10}$$

$$\langle \widetilde{i_s} \rangle^2_{RMS} = \langle i_s \rangle^2_{RMS} - \left(\frac{3}{2\sqrt{2}} m_I m_V I_o \cos \phi_o \right)^2 \tag{4.11}$$

The filter capacitor is to be designed such that it takes in most of this higher harmonics ripple current. For an allowable ripple percentage λ_1 in the secondary side link current given by (4.12) and allowable distortion λ_2 in the input voltage of the matrix converter given by (4.13), the filter capacitor value can be calculated using (4.14). To ensure smoothly varying sinusoidal currents in the transformer link and have a stable voltage at the matrix converter input, λ_1 and λ_2 should be chosen within 10% of rated values. From the calculated value of C_f and given value of L_{lkg}, the corner frequency of the LC filter is calculated using (4.15). The leakage resistance R_{lkg} provides the necessary damping at the resonant or corner frequency f_c. The corner frequency should be more than the transformer link frequency f_t but less than the switching frequency of the matrix converter. For a good design, $3f_t < f_c < f_s/3$. If the calculated value of f_c is not in the above range, the specifications of λ_1 and λ_2 is varied and the value of C_f is recalculated.

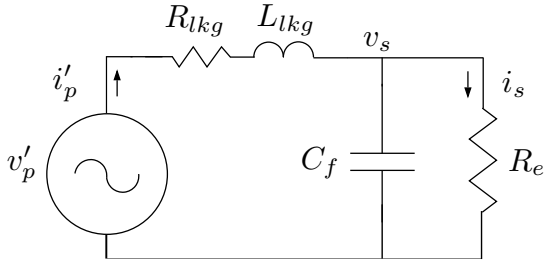


Figure 4.8: Per-phase equivalent circuit of the matrix converter with input filter at the transformer link frequency

$$\langle \widetilde{i}'_p \rangle = \lambda_1 \left(\frac{I_s}{\sqrt{2}} \right) \tag{4.12}$$

$$\langle \widetilde{v}_s \rangle = \lambda_2 \left(\frac{V_s}{\sqrt{2}} \right) \tag{4.13}$$

$$C_f = \frac{\langle \widetilde{i}_s \rangle_{RMS} - \langle \widetilde{i}'_p \rangle_{RMS}}{\omega_s \langle \widetilde{v}_s \rangle_{RMS}} \tag{4.14}$$

$$f_c = \frac{1}{2\pi \sqrt{L_{lkg} C_f}} \tag{4.15}$$

Since the frequency of operation across the HFT is relatively high, there is voltage drop across the filter designed. The per-phase equivalent circuit of the system at transformer link frequency is shown in Fig. 4.8. v'_p is the reflected MMC voltage on the secondary of the transformer ($\langle v'_p \rangle = \frac{N_2}{N_1} v_p$).

The average input current vector of the matrix converter is aligned along the input voltage vector to obtain unity power factor. So for the transformer link frequency, the matrix converter can be modeled as a resistive load R_e as defined by (4.16), where Z_L is the impedance of the machine load.

$$R_e = \frac{v_{s1_{RMS}}}{i_{s1_{RMS}}} = \frac{|Z_L|}{\frac{9}{4}(m_I m_V)^2 \cos \phi_o} \tag{4.16}$$

From Fig. 4.8, the current equation at the node is given by (4.17). The voltage seen by the matrix converter at its input v_s is the difference between the output voltage of the MMC reflected on the secondary side of the transformer and drop across the

filter components. This is shown in the Laplace domain in (4.18). The absolute ratio between voltage after and before filter hence depends on the filter components, effective resistance of the matrix converter and the transformer link frequency $\omega_t = 2\pi f_t$ and is given by (4.19).

$$\begin{aligned} i'_p &= i_{C_f} + i_s \\ &= \frac{v_s}{1/sC_f} + \frac{v_s}{R_e} \end{aligned} \tag{4.17}$$

$$\begin{aligned} v_s &= v'_p - i'_p(R_{lkg} + sL_{lkg}) \\ &= v'_p - v_s\left(\frac{1}{R_e} + sC_f\right)(R_{lkg} + sL_{lkg}) \\ \Rightarrow v_s &= \frac{v'_p}{1 + \left(\frac{1}{R_e} + sC_f\right)(R_{lkg} + sL_{lkg})} \\ &= v'_p \frac{R_e}{R_e + R_{lkg} + s\left(L_{lkg} + R_e R_{lkg} C_f\right) + s^2 R_e C_f L_{lkg}} \end{aligned} \tag{4.18}$$

$$\begin{aligned} \frac{|v_s|}{|v'_p|} &= \left| \frac{R_e}{R_e + R_{lkg} + s\left(L_{lkg} + R_e R_{lkg} C_f\right) + s^2 R_e C_f L_{lkg}} \right| \\ &= \frac{R_e}{\sqrt{\left(R_e + R_{lkg} - R_e C_f L_{lkg}\right)^2 + \omega_t^2 \left(L_{lkg} + R_e R_{lkg} C_f\right)^2}} \end{aligned} \tag{4.19}$$

4.5 Machine control at variable speed

A rotating machine is a generator in wind applications or an adjustable speed motor drive. In a generator in wind applications, due to variation in rotor speed, the magnitude and frequency of voltage at the machine terminal varies. In conventional wind energy conversion systems, the power converter interfaced with the rotating machine is controlled to adjust this variable magnitude and frequency AC generation. The controller regulates the voltage transfer ratio (or modulation index) and angular frequency of the modulating reference signal for the power electronic converter. The controller G_C generates the reference voltage for the power converter to meet the variation in

load voltage demand as shown in Fig. 4.9. Thus at low wind speeds when the voltage demand is lower, the average voltage generated by the power converter is reduced, such that ratio of voltage to speed remains constant ($V/f \approx$ constant). However the instantaneous PWM voltage still is a function of the input voltage and hence dV/dt subjected to the machine remains constant as shown in Fig. 4.9. In the proposed interface using power electronic transformer, another solution exists to control the modulation index of the MMC interfaced to the transformer on the high voltage side, as shown in Fig. 4.10 [18].

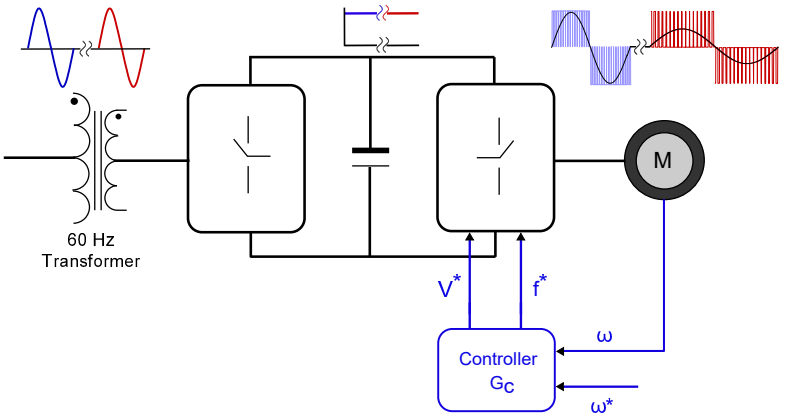


Figure 4.9: Control of conventional interface to meet variation in machine speed

In the proposed interface, the power converter interfacing the machine is always operated with full voltage transfer ratio between output and input. It only acts as an interface to generate adjustable frequency PWM voltages at the machine terminals. For a reduction in speed to one-half, the voltage requirement by the machine is also reduced to nearly one-half ($V/f \approx$ constant). The MMC interfaced to the high-frequency transformer is modulated to generate one-half the voltage magnitude. This in turn means bypassing many of the submodules so as to generate a lower peak voltage across the transformer primary, as shown in Fig. 4.10. This in turn also reduces the dV/dt to one-half for the machine interfaced power converter and the machine itself, as shown in Fig. 4.10. The purpose of pushing the control to the MMC is to reduce the voltage stress related losses in the transformer, machine interfaced power converter and the machine.

As can be seen from Fig. 4.10, the voltage output of the MMC has reduced to

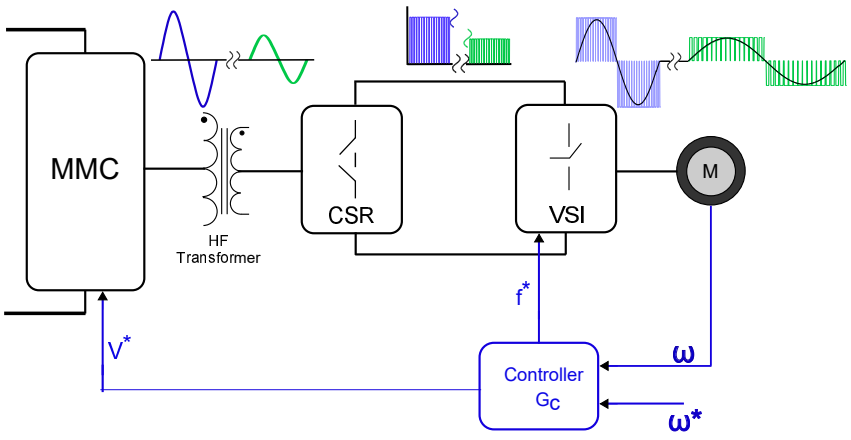


Figure 4.10: Control of proposed interface to meet variation in machine speed

one-half which reduces the voltage stress across the transformer, machine connected indirect matrix converter and the machine itself. This results in lower core losses in the transformer, lower switching losses in the matrix converter which is critical as the low voltage side matrix converter operates at high switching speeds, and lower core losses in the machine. Also reduction of dV/dt and common mode voltage switching reduces machines insulation stress which could result in longer lifetime. The matrix converter has input filter capacitors which always draw a particular amount of reactive current which they are designed for. Generally this is kept below 10%. When the voltage is reduced to one-half during low speed operation, the reactive current drawn is reduced to one-half ($i_{C_f} = v_s.\omega_t.C_f \Rightarrow i_{C_f} \propto v_s$). However, reduction of voltage results in increase in the transformer link current which flows through the MMC. This results in higher copper losses in the transformer, higher conduction losses in the MMC and higher voltage drop across the leakage inductance of the transformer. The modulation index of the MMC can be slightly increased to compensate for this voltage drop. Hence, a trade-off exists and detailed analysis and comparison is part of future work.

4.6 Simulation Results

The HVDC to 3-phase AC power electronic transformer topology as shown in Fig. 4.3 is simulated with ideal switches in MATLAB/Simulink with parameters as shown in Table

4.1. It makes use of a 3-phase MMC to interface with the high frequency transformer. Each leg of the MMC is made up of 16 number of 2-level submodules or 8 number of 3-level submodules. The HFT has turns ratio 100 : 6 and an effective leakage inductance of 300 μH, referred to the secondary side. The leakage resistance is 0.1 Ω. The PET feeds a three-phase $R-L$ load with a load power factor of 0.8 at 60-Hz. Following the design in Section 4.4, for an allowable ripple of 10% in the link current, the designed link filter capacitor comes out to be 6.6 μF. The detailed simulation results are presented in this section.

Table 4.1: Single-stage HVDC/AC PET: Simulation Parameters

Parameters	**Value**
DC bus voltage V_{dc}	20 kV
Submodule capacitor (MMC)	C_1=5 mF, C_2=10 mF
Arm inductor L_a	2.5 mH
Link filter capacitor C_f	6.6 μF
Transformer	100 : 6, 1 kHz, L_{lkg}=300 μH
Matrix converter switching frequency	20 kHz
Load	500 kW, 0.8 pf, 60-Hz

The steady state results at rated speed are shown in Fig. 4.11 and Fig. 4.12 respectively. The high frequency link waveforms are shown in Fig. 4.11 along with a zoomed view on the right. As can be seen, the primary voltage of the high frequency transformer as shown in Fig. 4.11 (top) reaches 17 distinct levels by use of 8 modules of the new 3-level submodule topology, using modulation index $m_p = 1$. The switching frequency is set at 2 kHz to result in a single voltage level in every switching cycle of the MMC using pulse-width modulation. It must be noted that similar results are obtained using nearest level modulation as well. The matrix converter injects switched currents at its input which is filtered and only sinusoidal currents pass through the high frequency transformer. This is shown by the sinusoidal currents on the primary side of

the HFT, Fig. 4.11 (second from top). The leakage inductance of the transformer acts as a smoothing reactor to minimize the harmonics in the primary voltage of the HFT. Hence near sinusoidal voltages can be seen on the secondary side of the high frequency transformer. Use of a 100:6 transformer steps down the voltage as can be seen in Fig. 4.11 (third from top). The high frequency switched currents injected by the matrix converter due to pulse-width modulation are shown in Fig. 4.11 (bottom). From the 1 kHz sinusoidal voltages, the matrix converter synthesizes output voltages at 60-Hz. It switches at a higher frequency of 20 kHz. The output line to neutral voltage is shown in Fig. 4.12 (top) and the 3-phase line currents in Fig. 4.12 (middle). As can be seen, the line currents are near sinusoidal and balanced. The common mode voltage generated due to PWM switching is shown in Fig. 4.12 (bottom).

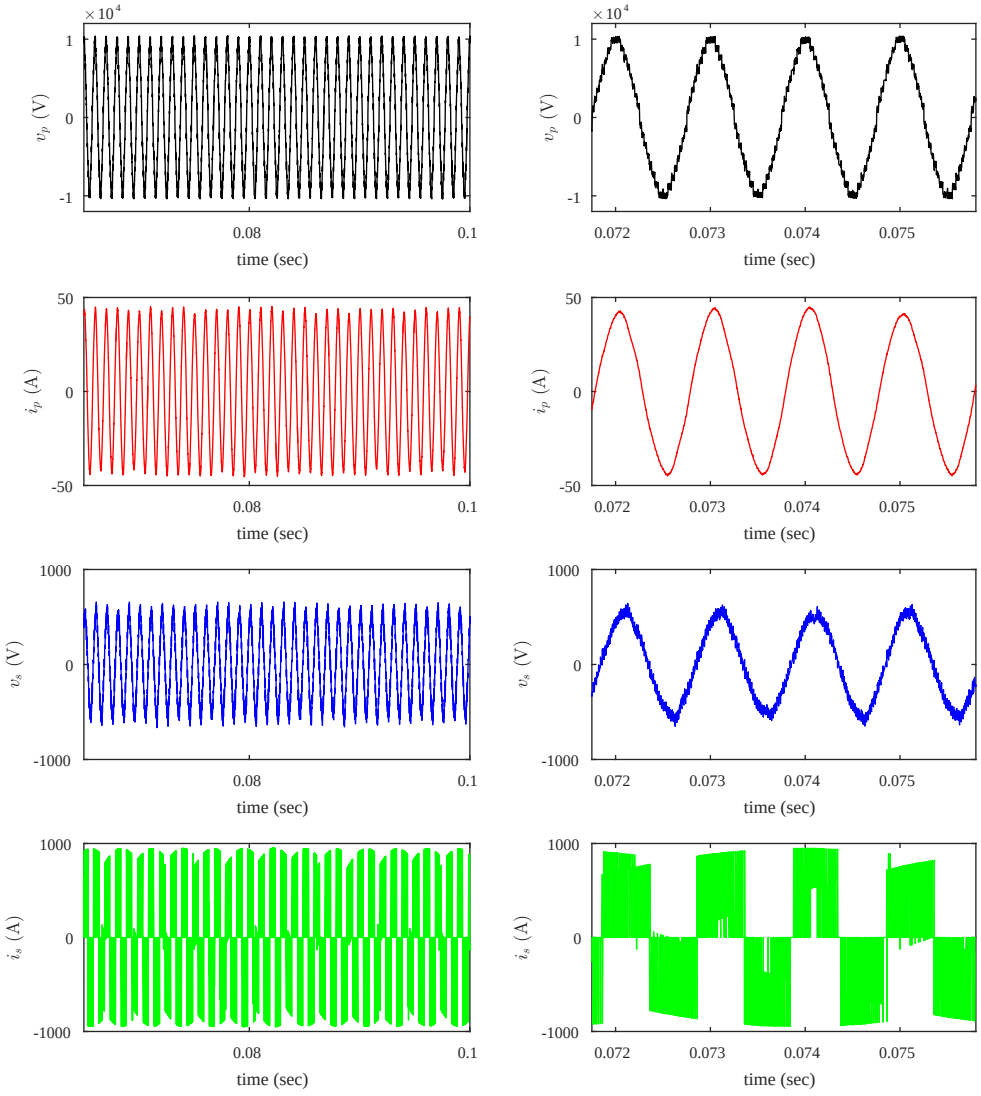


Figure 4.11: (top to bottom) MMC output voltage, high voltage side current, matrix converter input voltage, matrix converter input current with zoomed versions on the right

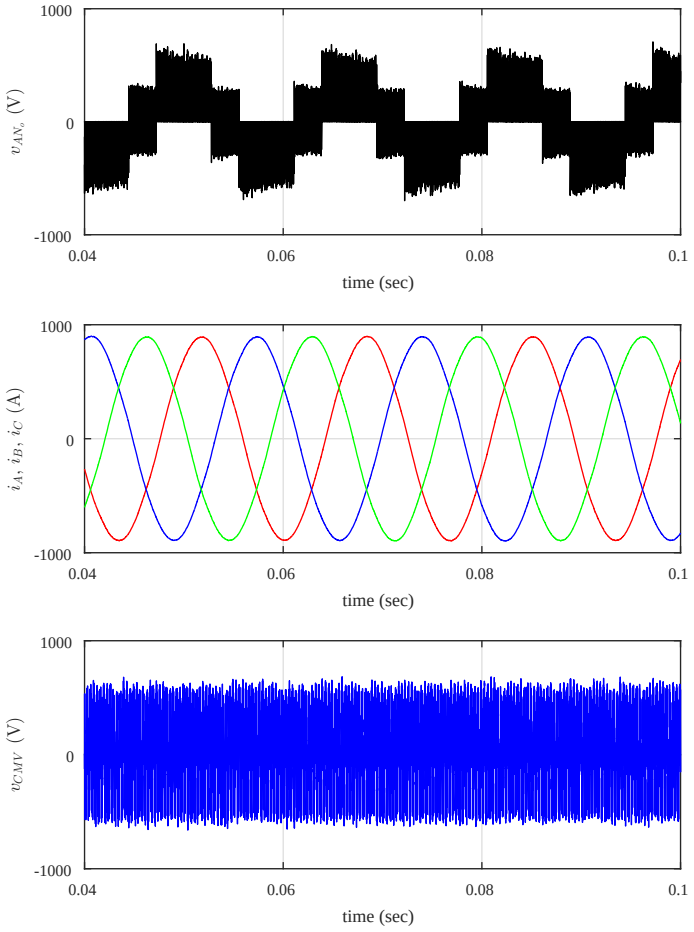


Figure 4.12: (top to bottom) Matrix converter output line to neutral voltage, 3-phase output line currents, common mode voltage

The next set of results pertain to the machine control at variable speeds. At lower machine speed, a reduction in output voltage requirement is met by controlling the modulation index of the MMC at the primary of the HFT. Because of the proposed control in Section 4.5, the matrix converter is modulated at a full modulation index of 0.866. For half machine speed, the output is synthesized at a frequency of 30 Hz. The load parameters are shown in Table 4.1. The transformer voltages and currents are shown in Fig. 4.13(a) and Fig. 4.13(b) for the conventional and proposed control methods respectively. It can be clearly seen that the voltage output of the MMC has been brought down in the proposed control method to meet the lower speed demand. This results in a lower input voltage applied across the matrix converter which is operating at full modulation index. As described in previous section, reduction of MMC output voltage results in an increase in the transformer link current as shown in Fig. 4.13(b)(second from top). The corresponding load line to neutral voltage of one phase and line currents are shown in Fig. 4.14(a) and Fig. 4.14(b) respectively. The change in modulation index of the MMC to one-half is reflected by a change in output voltage level of the matrix converter. The dV/dt across machine insulation is greatly reduced using the proposed control method which increases the machines lifetime. The FFT of output voltage clearly shows the reduction in total THD. The control of output voltage magnitude using matrix converter results in the same voltage levels but use of more number of zero vectors as shown in Fig. 4.14(a). Pushing the control to the primary side of the HFT has resulted in reduced voltage stress related losses in the transformer, matrix converter and the machine. Also the peak common mode voltage has reduced by approximately one-half by using the proposed control method. The THD has also considerably reduced as seen in the FFT plots.

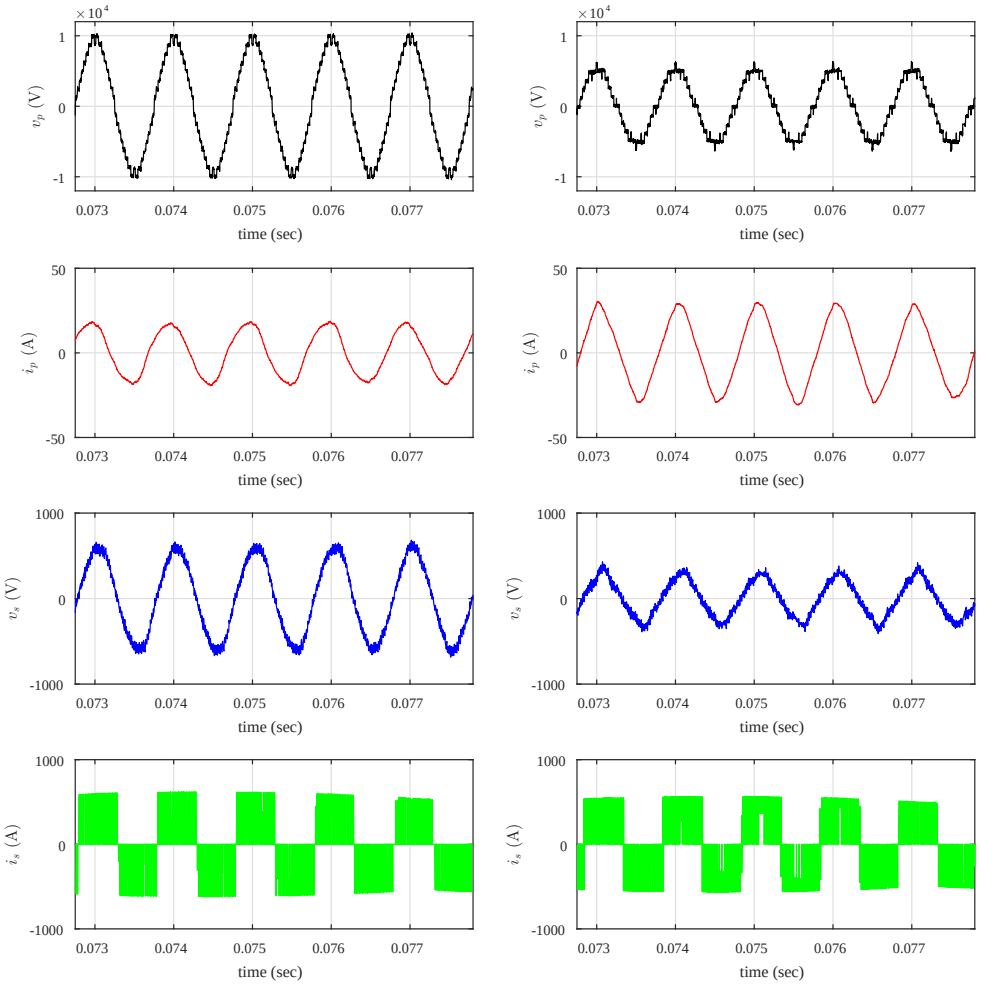


Figure 4.13: (top to bottom) MMC output voltage, high voltage side current, matrix converter input voltage, matrix converter input current with zoomed versions on the right for (a) conventional control approach (b) proposed control approach

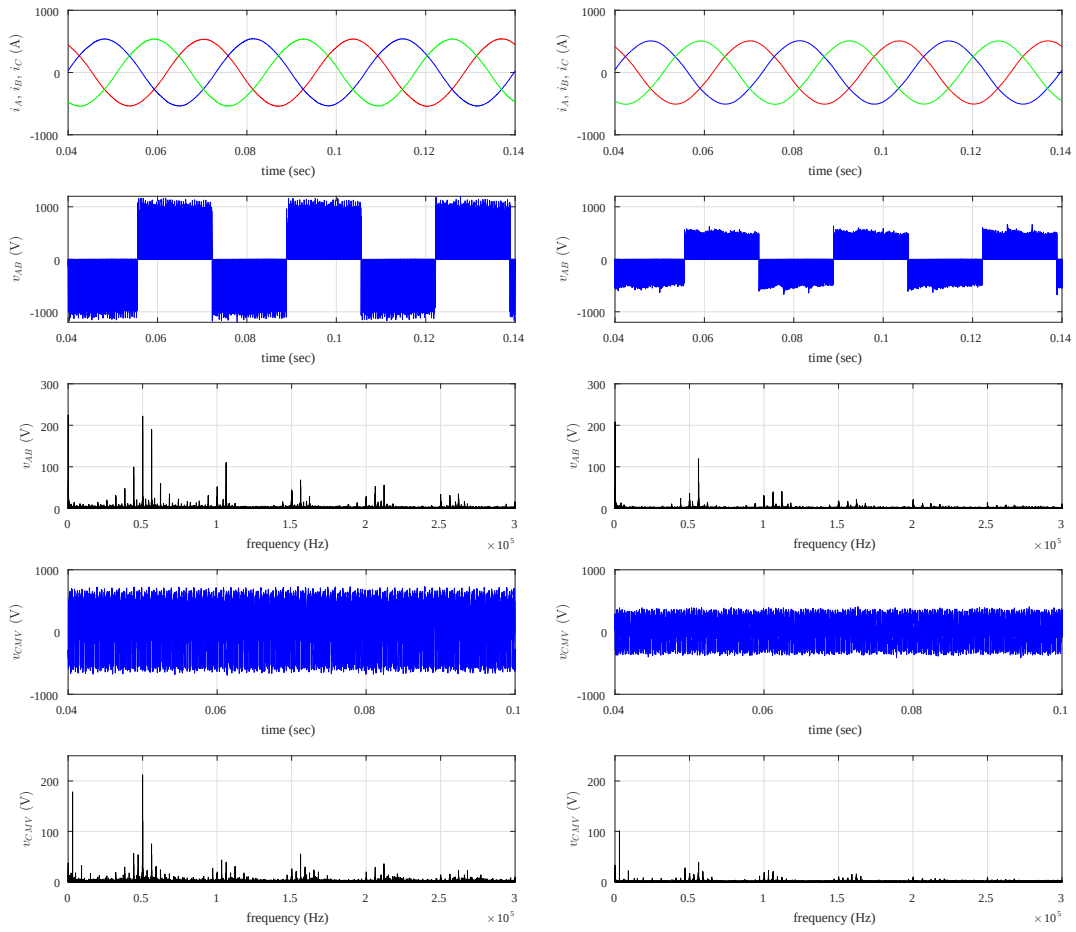


Figure 4.14: (top to bottom) Matrix converter 3-phase output line currents, output line to neutral voltage with FFT, common mode voltage with FFT for (a) conventional control approach (b) proposed control approach

4.7 Experimental Results

The single-stage HVDC/AC power electronic transformer was run with a DC-bus voltage of 100 V feeding a 3-phase RL load. The 3-phase MMC described in Chapter 2 with four number of 3-level submodules is used to generate high frequency 1 kHz sinusoidal voltages across the primary of the high frequency transformers. Nearest level modulation with $2n+1$ output voltage levels is used as described in Chapter 3. An indirect matrix converter topology is employed as the machine interfaced power converter. This section describes the overall hardware setup and experimental results.

The matrix converter is implemented using integrated power IGBT modules from Microsemi and gate driver 6SD106EI from CONCEPT as shown in Fig. 4.15. Control signals for SVPWM are generated from an FPGA (Xilinx XC3S500E). The experiments are run with a switching frequency of 15 kHz at a modulation index of $m = 0.78$ for rated conditions. Output at 60-Hz is generated across a balanced three phase load with $R_L = 16.66\ \Omega$ and $L_L = 30$ mH per phase. An appropriate C filter, with capacitor sized at 6.6μF respectively is used. Unlike simulation which had ideal pulses, a 4-step commutation strategy using verilog state machine was implemented for safe commutations of the CSR switches. Conventional dead time commutation was implemented for the VSI. The commutation interval was 600 ns. The transformers have 1 : 1 turns ratio in the experimental setup and designed using area product method. Due to small leakage inductance in the transformer, an extra inductor of 0.5 mH was added for filtering.

The output line to line voltage with 3-phase line currents is shown in Fig. 4.16. As can be seen, the line currents are near sinusoidal with a peak magnitude of 1.6 A which is slightly lower than the analytical value of 1.8 A, which can be accounted to the voltage drop across non-ideal devices.

To verify the proposed control method at lower voltage requirements, the system was run at half the maximum modulation index. Fig. 4.17(a) shows the various voltage levels using conventional method. Here the matrix converter is regulated to reduce the fundamental output voltage. Hence the voltage stress across all components remains the same as MMC output voltage. In the proposed method of control, the control is pushed to the MMC which generates half the rated voltage now. This brings down the input voltage of the matrix converter which is always operating at maximum modulation

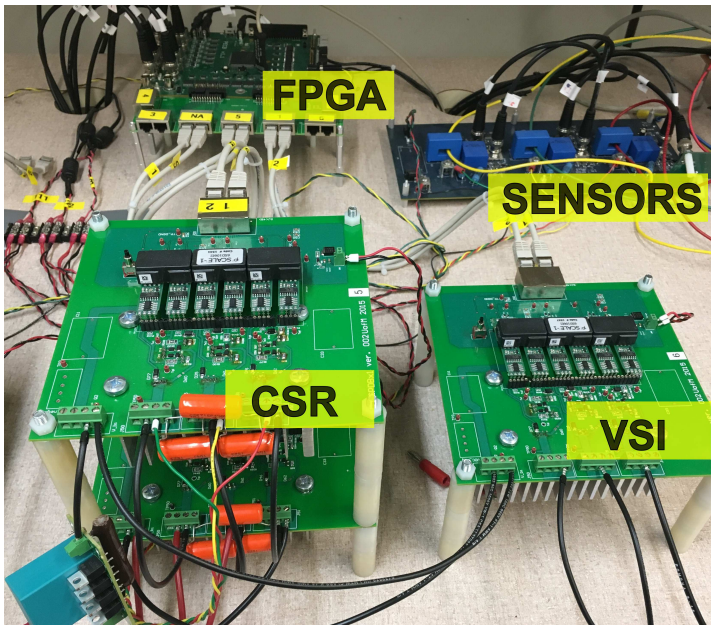


Figure 4.15: Hardware prototype of the indirect matrix converter

index. As shown in Fig. 4.17(b), the virtual DC-link voltage of the indirect matrix converter along with output line-line voltage has been reduced by half. This greatly reduces the dV/dt across all devices and also across the machines insulation. Another benefit of such control is reduction in common mode voltages generated due to SVPWM of matrix converter. They have also been reduced to half the peak value compared to conventional control method. The output voltage and 3-phase line currents are shown in Fig. 4.18(a) and Fig. 4.18(b) for the conventional and proposed methods respectively. Output is generated at 30 Hz under half the voltage demand to keep $V/f \approx$ constant.

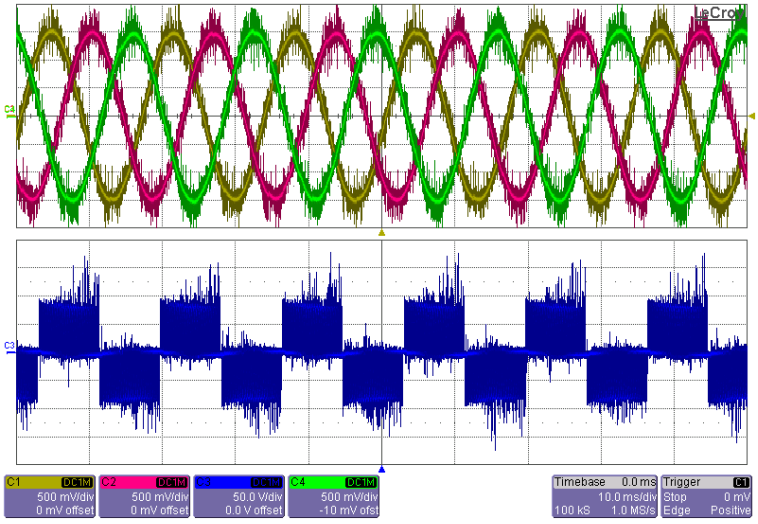
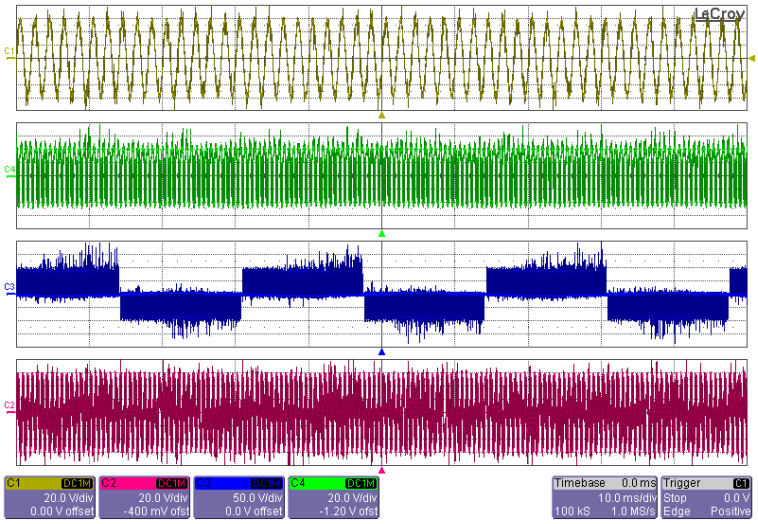
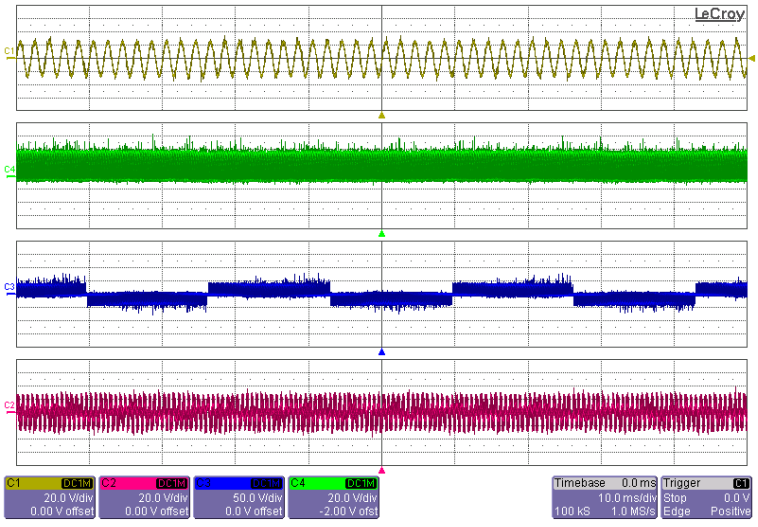


Figure 4.16: (top to bottom) Matrix converter 3-phase output line currents, output line to neutral voltage

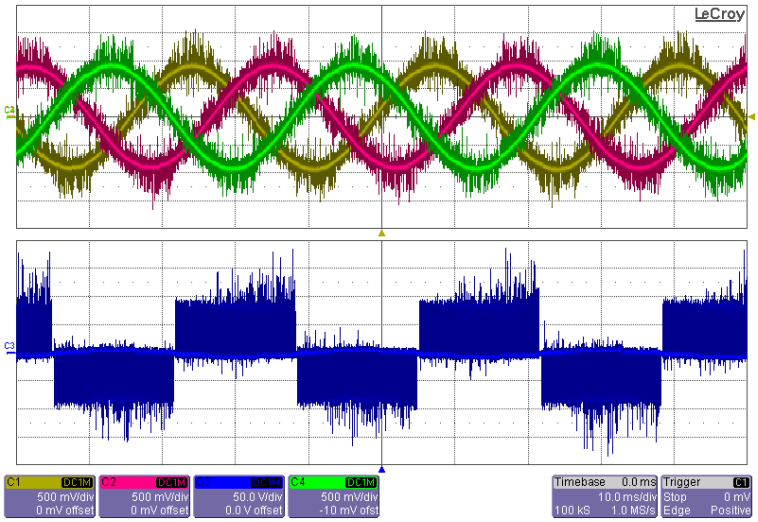


(a)

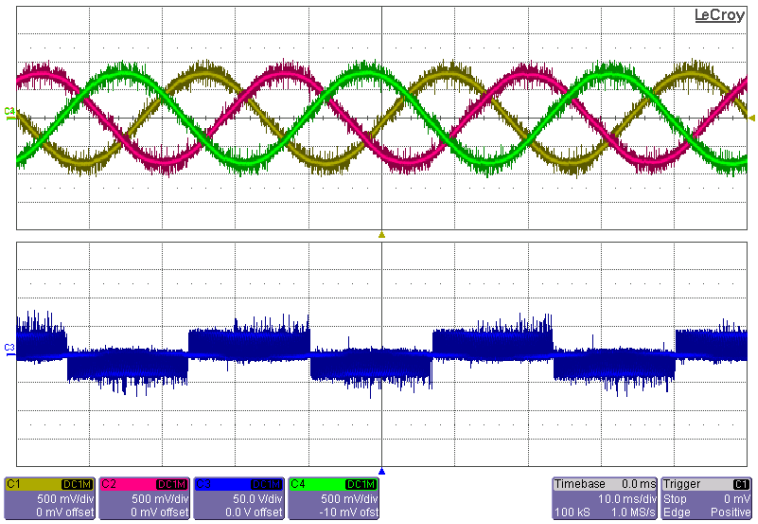


(b)

Figure 4.17: (top to bottom) Matrix converter input voltage, virtual DC-link voltage, output line to line voltage, common mode voltage for (a) conventional control approach (b) proposed control approach



(a)



(b)

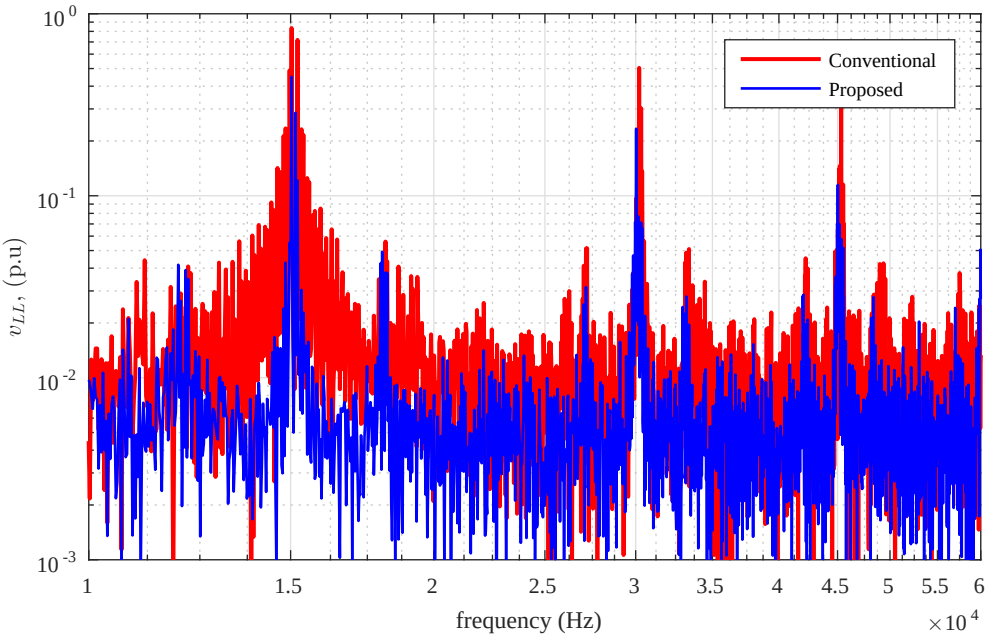
Figure 4.18: (top to bottom) Matrix converter 3-phase output line currents, output line to neutral voltage for (a) conventional control approach (b) proposed control approach

4.8 Performance evaluation

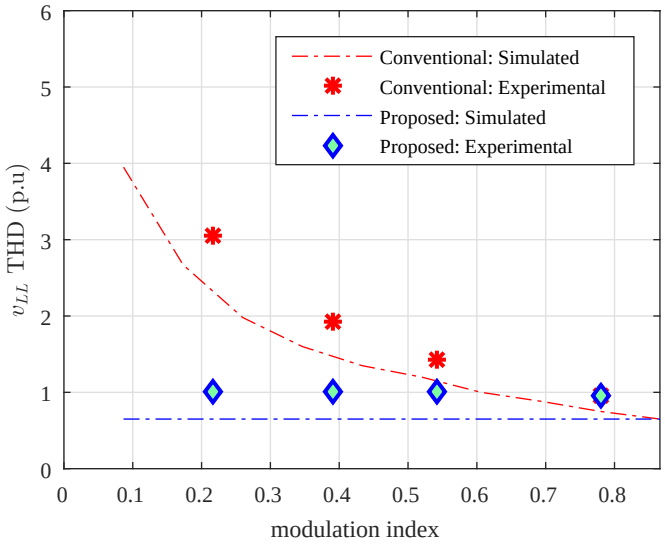
This section compares the machines performance in terms of output voltage distortion and common mode voltage generation using the proposed control method compared to the conventional approach.

4.8.1 Output voltage distortion

The IMC produces switched voltage at its output with a fundamental sinusoidal component. The distortion in this voltage is due to the presence of switching and higher order harmonics. The machine terminals are subjected to this voltage. A higher degree of distortion in output voltage would compromise its quality and increase the core losses in the machine. Fig. 4.19(a) shows the FFT of output line-neutral voltage running at half modulation index where an improvement in higher order harmonics can be seen. Fig. 4.19(b) compares the per-unit THD of output voltage for the proposed control method with the conventional method for different values of modulation indices. The improvement is higher at lower voltage requirement which becomes almost equal at full modulation index. At lower voltage requirement in conventional control method, usage of greater proportion of zero vectors results in high distortion as shown in Fig. 4.19(b).



(a)



(b)

Figure 4.19: (a) FFT of output line-line voltage using conventional and proposed control methods at half modulation index (b) Comparison of per-unit THD in output voltage using conventional and proposed control methods

4.8.2 Common mode voltage

A major problem in any electric drive is the generation of switching common mode voltages (CMV) at the machine terminals. Coupled with parasitic capacitance, this results in electromagnetic interference (EMI), shaft voltage buildup and high frequency bearing and ground currents which reduces the machine lifetime [85][86]. Common mode voltage (CMV) in a matrix converter is defined as the voltage difference between the load neutral N_o and the input neutral of the high frequency transformer N_i which can also be expressed as the average of instantaneous values of the three output phase voltages referred to input neutral, as given by (4.20). Output voltage v_{AN_i} referred to transformer neutral N_i is dependent on both the switching states of the CSR and VSI, as given by (4.21). The final expression for net CMV in terms of the switching states of the IMC and instantaneous value of transformer phase voltages is given in (4.22). Thus, instantaneous value of CMV is reduced by controlling the MMC to produce a lower peak voltage which is applied to the matrix converter.

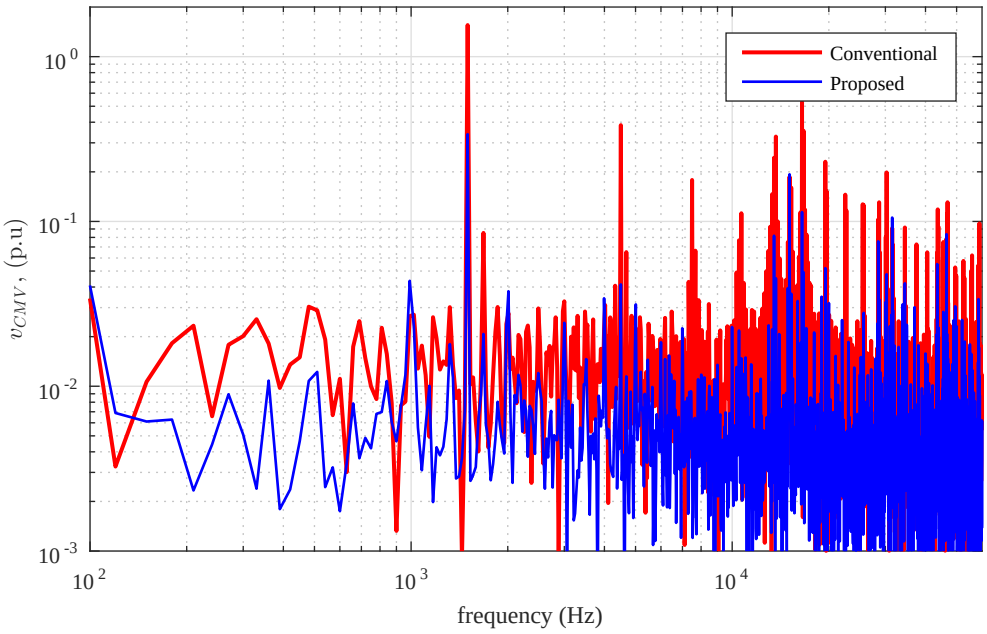
$$v_{CMV} = v_{N_oN_i} = \frac{v_{AN_i} + v_{BN_i} + v_{CN_i}}{3} \tag{4.20}$$

$$\begin{aligned} v_{AN_i} &= S_A.v_{PN_i} + \overline{S}_A.v_{NN_i} \\ &= S_A\left(S_{aP}.v_{aN_i} + S_{bP}.v_{bN_i} + S_{cP}.v_{cN_i}\right) \\ &\quad + \overline{S}_A\left(S_{aN}.v_{aN_i} + S_{bN}.v_{bN_i} + S_{cN}.v_{cN_i}\right) \end{aligned} \tag{4.21}$$

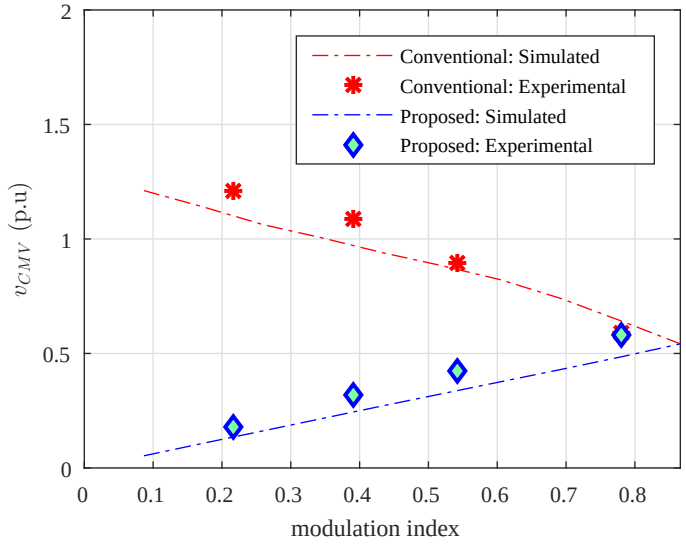
$$\begin{aligned} v_{CMV} &= \frac{1}{3}(S_A + S_B + S_C)(S_{aP}.v_{aN_i} + S_{bP}.v_{bN_i} + S_{cP}.v_{cN_i}) \\ &+ \frac{1}{3}(\overline{S}_A + \overline{S}_B + \overline{S}_C)(S_{aN}.v_{aN_i} + S_{bN}.v_{bN_i} + S_{cN}.v_{cN_i}) \end{aligned} \tag{4.22}$$

The results in previous section shows a reduction in peak value of the net CMV waveform in the proposed method of control as compared to the conventional method. Fig. 4.20(a) shows the FFT plots of common mode voltage for the conventional and proposed methods at half the maximum modulation index. A reduction in both lower and higher order harmonics is observed in the common mode voltage using the proposed

control method. Fig. 4.20(b) provides a comparison of the per unit RMS values of CMV for different modulation techniques over a range of modulation indices. Based on the experimental data, the RMS value of CMV has been improved which is more pronounced at low machine speeds when the voltage requirement is low. The decreasing trend in the RMS values of CMV with the increase in modulation index in the conventional control method can be attributed to the decrease in the usage of zero vectors for generation of output voltage. At full modulation index, the two methods almost produce the same common mode voltage RMS, as seen from Fig. 4.20(b). Further reduction in common mode voltage can be obtained by using specialized space vector modulation as described in [87] or by using an open-ended drive configuration [88, 89].



(a)



(b)

Figure 4.20: (a) FFT of common mode voltage using conventional and proposed control methods at half modulation index (b) Comparison of per-unit common mode voltage RMS using conventional and proposed control methods

4.9 Summary

A single-stage power electronic transformer based on modular multilevel converter is presented in this chapter which results in sinusoidal voltages and currents through the high frequency transformer. This results in significant reduction in the transformer losses and also natural commutation of leakage energy is obtained. The matrix converter supplying the machine is always operated at its full modulation index. The synthesis of adjustable magnitude voltages at the machine terminals is controlled in the primary side MMC to result in lower voltage stress related losses in the transformer, matrix converter and the machine. The operating principle, modulation and control of the proposed PET along with results have been presented.

Note: Part of this chapter is reproduced from my previous publications [17, 83, 84].

Chapter 5

Two-stage Multi-winding Power Electronic Transformer

Grid integration of multiple renewable energy sources using a power electronic transformer (PET) topology is presented in this chapter. A modular multilevel converter (MMC) on the high voltage grid side generates high frequency sinusoidal voltages. A multi-winding high frequency transformer (HFT) interfaces different wind generators/photovoltaic arrays using many full-bridge converters and PWM inverters. The leakage inductance of the transformer acts as the smoothening filter for the current through the HFT. With sinusoidal voltages and smooth currents through the transformer, there is significant reduction in transformer losses and also natural commutation of leakage energy is obtained. The operating principle, modulation and control of the proposed PET is validated by simulations in MATLAB/Simulink.

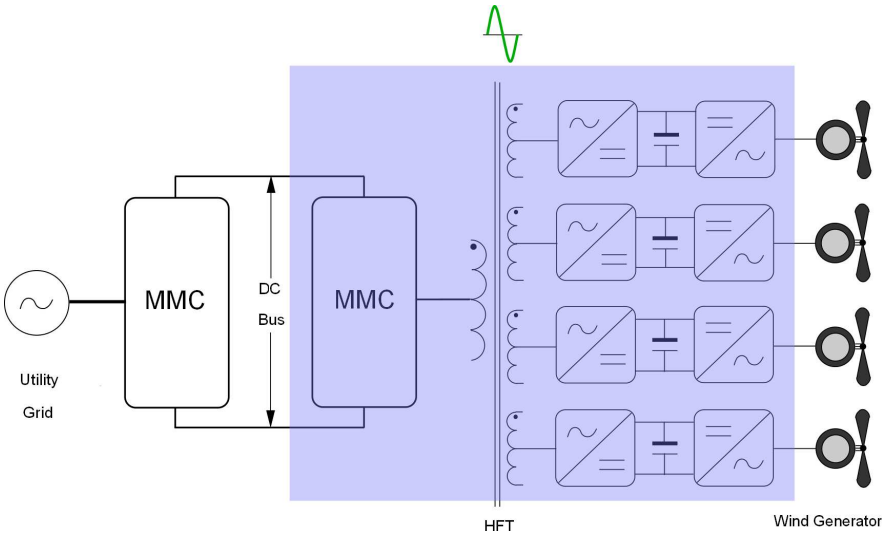
5.1 Introduction

Power transformers play an important role in the modern distribution system for voltage conversion and providing galvanic isolation for protection. Integration of multiple renewable energy sources like wind and solar with the medium voltage utility grid (13.8 kV/34.5 kV) uses a line frequency transformer. As discussed in previous chapters, replacement of line frequency transformers with power electronic transformers results in significant reduction in volume and weight along with added advantages like high power

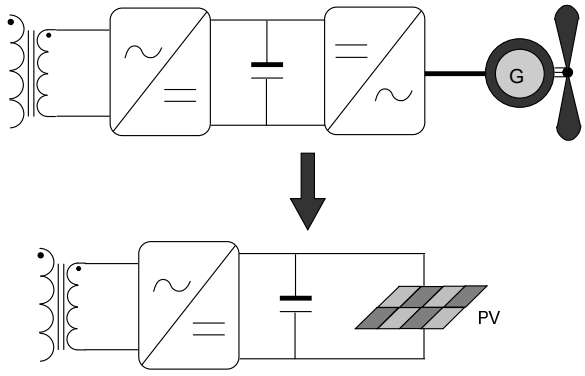
density, voltage regulation, power factor control, on demand reactive power support, etc [7]. This kind of transformer topologies can also find wide applications in UPS [72], medium voltage ASDs [77], energy storage systems [78], traction drives [90], mobile substations, etc.

Different configurations of available PET are presented in [8] [71]. The PET are widely classified into single stage, two stage and three stage. Single stage PETs use direct AC-AC matrix converters [9] or cycloconverters [91]. However, such PET do not have the flexibility to interface different types of renewable sources and also need series connection of devices on the high voltage side to meet the voltage stress. For high voltage and high power applications, PET topologies are connected in series/parallel due to limitation of power semiconductor device ratings. A two stage PET with series connected cycloconverters on the high voltage utility side is proposed to interface with a wind generator and battery energy storage [92]. These single stage and two stage PETs face the challenge of commutation of leakage energy in the transformer. A single-stage PET which does not face the problem of leakage energy commutation was discussed in Chapter 4.

Comparison of different three stage PET is given in [73]. A multi-winding transformer is used to generate multiple isolated DC-supplies from the renewable energy source for each H-bridge cell in the multilevel converter [13]. A single-phase PET connected in input series-output parallel consists of a modular multilevel ac-dc rectifier, a modular dual active bridge (DAB) dc-dc converter with high-frequency transformer, and a dc-ac inverter stage [14]. Use of neutral point clamped multilevel converters is difficult to scale [93]. Also using just 3-level structures on the high voltage side requires large input filters and series connected DC-link capacitors. HVDC grid connection of large scale photovoltaic power system based on series connected half-bridge choppers and interleaved flyback MPPT stage is given in [94].



(a)



(b)

Figure 5.1: (a) Proposed power electronic transformer topology, (b) Transformer secondary side converter for interfacing wind generator (top) or solar photovoltaics (bottom)

For offshore wind farms having an increased and constant wind speed with a higher output power, a DC grid is more suitable. A HVDC transmission line is formed in [76] by series connection of PET modules involving a diode bridge rectifier on the secondary side of the HFT in each module. A single isolated medium frequency DC-DC converter is used in [95] for DC transmission. A three stage PET configuration employing a MMC with an AC grid and DC terminal is given in [96].

The proposed PET topology involving MMC is shown in Fig. 5.1(a). It uses a multi-winding transformer to integrate numerous renewable energy sources to a high voltage AC or DC grid [16]. The DC bus could be very short as in the case of onshore wind farms or could be 100 miles HVDC line for offshore wind farms. Some of the advantages of the proposed topology are:

- The high voltage grid side converter employs a MMC which presents a modular structure resulting in easy scalability and higher reliability. Because of modular structure, lower voltage rated semiconductor devices operating at lower switching frequency and smaller capacitors can be used.

- The MMC uses 3-level submodules which results in half the submodule requirements compared to conventional half bridge submodules. This results in a much compact infrastructure. Also the 3-level submodules have considerable lower semiconductor losses [29].

- The MMC generates near sinusoidal voltage waveform at the primary of the HFT. Thus the transformer sees sinusoidal voltages as opposed to chopped square voltages in most of the available papers in literature. This results in lower core losses in the HFT.

- The PET uses a single transformer with multiple secondary windings to interface numerous renewables. This results in a much reduced transformer volume and weight. Also the HFT provides galvanic isolation.

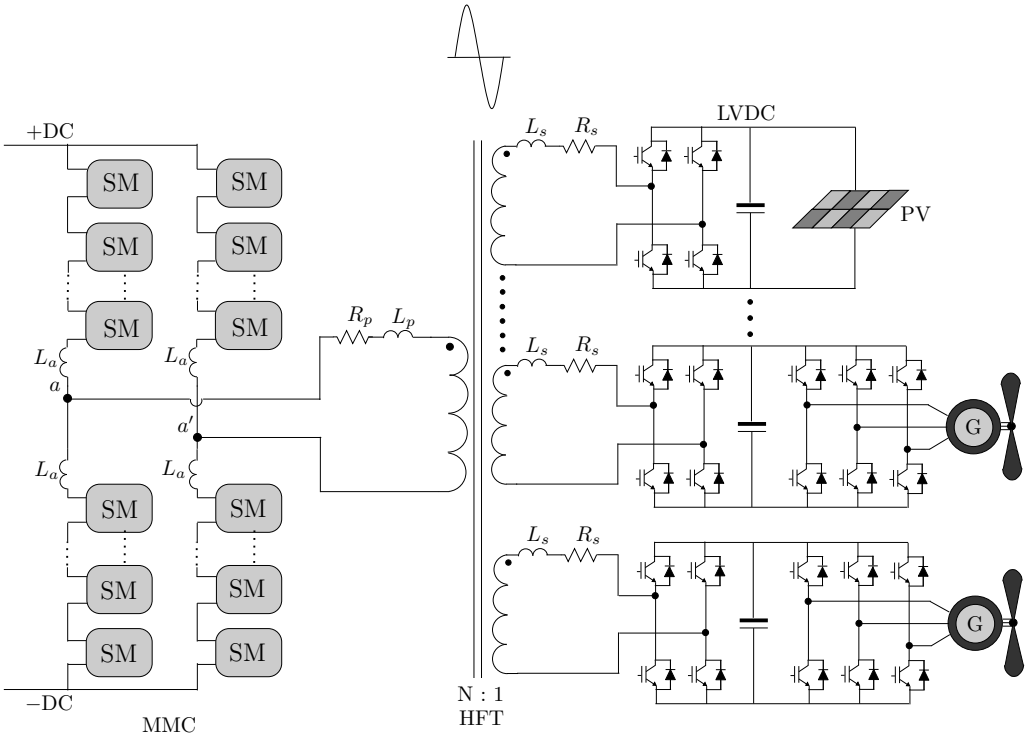
- The leakage inductance of the transformer is used as a smoothening filter for the link current. Thus we get smoothly varying currents which prevents the problem of leakage energy commutation. Natural commutation of leakage energy is obtained.

- Because of multi-winding structure, multiple renewable energy sources can be interfaced like wind, PV, etc. Also the MMC has a medium/high voltage DC terminal which can be used for DC transmission/distribution. Thus the proposed MMC presents a very flexible solution for renewable energy integration to an AC/DC grid.

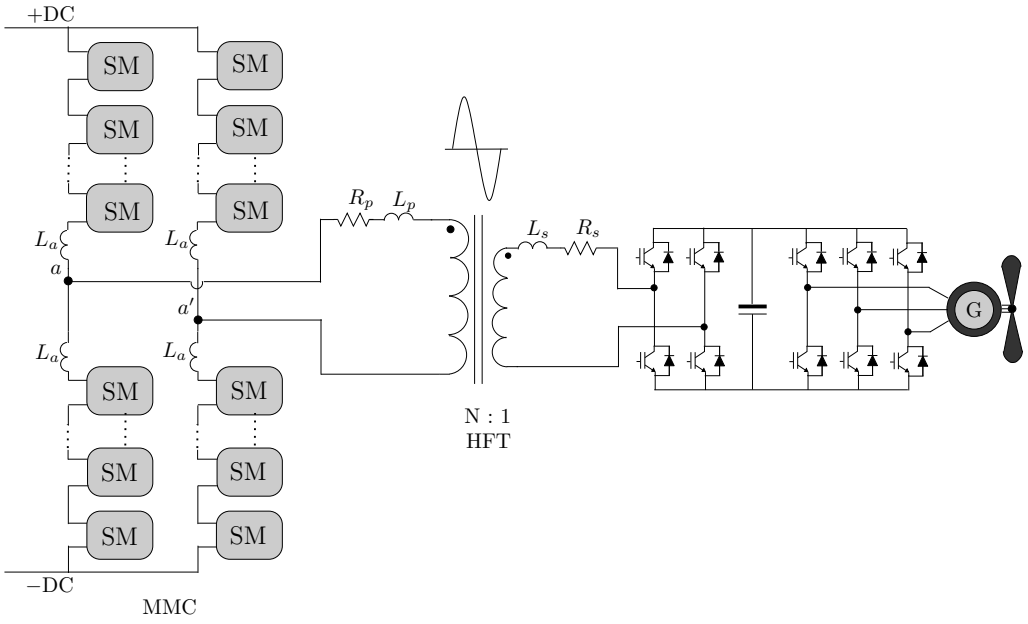
The proposed topology with its working principle is presented in Section 5.2. Section 5.3 and 5.4 presents the analysis of the MMC, HFT and secondary converters. Key results are presented in Section 5.5 and the paper concludes in Section 5.6.

5.2 Topology

The proposed power electronic transformer topology is shown in Fig. 5.1(a). It uses a back to back connected MMC on the primary side interfacing the medium voltage utility grid. Because of modular multilevel structure, the utility side synthesized voltages are near sinusoidal which eliminates the need for large size AC filters. The MMC structure also provides a medium voltage DC bus, which can be used to interface a DC distribution/transmission network. The high frequency transformer is a multi-winding transformer with one primary winding and multiple secondary windings. It can interface multiple wind generators at once. To interface a wind generator, the PET has a full-bridge and then a PWM inverter. Also it can interface photovoltaics using just a H-bridge converter, as shown in Fig. 5.1(b).



(a)



(b)

Figure 5.2: (a) Detailed circuit description of the two-stage multi-winding PET for integrating multiple renewable sources, (b) Detailed circuit description of the two-stage PET for integrating one renewable source

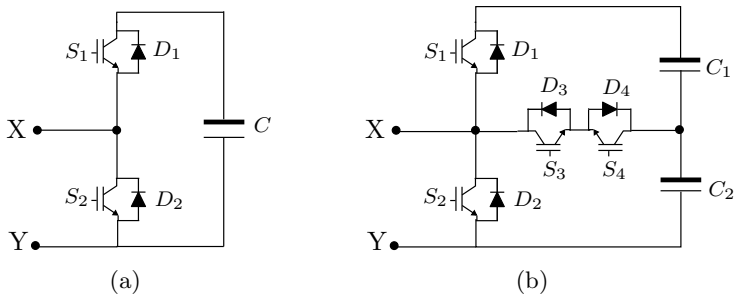


Figure 5.3: (a) 2-level submodule (a) 3-level submodule

A more detailed circuit of Fig. 5.1(a) is a two-stage HVDC/AC power electronic transformer topology to interface the high voltage DC bus with low voltage renewables as shown in Fig. 5.2(a). It can also be used to integrate one renewable energy source as shown in Fig. 5.2(b). A single phase modular multilevel converter is used to synthesize high frequency sinusoidal voltages at the primary of the HFT. This MMC is made up of two legs. Each leg of the MMC is made up of two arms consisting of n series connected submodules. Each arm also has a protection choke L_a to limit over-currents during any internal or external faults. The internal structure of the submodule can be a 2-level (Fig. 5.3(a)) or 3-level (Fig. 5.3(b)) submodule.

The high frequency transformer is a multi-winding transformer with N:1 turns ratio. It has leakage inductances L_p and L_s on its primary and secondary. Also there exist some leakage resistances R_p and R_s to account for non-idealities. The secondary low voltage side windings of the HFT are connected to multiple PWM full-bridge converters. This PET has sinusoidal voltages and smooth currents through the HFT, resulting in lower core losses. For integration of PV, an additional DC-DC converter is also generally present which is controlled for obtaining maximum power point tracking (MPPT). For integration of wind generators, a 2-level inverter generates 3-phase PWM AC of desired magnitude and frequency. Multiple such converters are synchronized using a closed loop controller when interfacing multiple renewables.

5.3 Analysis: High voltage side MMC

The high voltage side interfaces the HFT using a single-phase MMC. Modulation of the MMC follows the concepts discussed in Chapter 3. This section briefly reviews those concepts applied to the presented multi-winding PET topology.

5.3.1 Modulation

A hybrid carrier based pulse width modulation (PWM) scheme or fundamental switching frequency based nearest level modulation (NLM) scheme is used to modulate the MMC. The carriers are phase shifted for the submodules and level shifted for the IGBT's inside each submodule in PWM. In NLM, the sinusoidal reference is rounded of to the nearest integer to result in a single voltage level every switching interval. For each phase j ($j = a, b, c$) of the MMC, two reference signals v^*_{up} (upper arm) and v^*_{lp} (lower arm) are needed to synthesize the output voltage reference v^*_p as given by (5.1). A compensation term v^*_{zp} is present to account for circulating current control which can be relaxed in PET application. Using this modulation the upper capacitor C_1 from each submodule can only be applied when the lower capacitor C_2 has already been applied. Whenever the reference is more than the respective carrier, an active gate signal S_i is generated. Here v^*_p is the desired voltage per phase to be synthesized, where m is the modulation index of the converter, V_t is the peak of the transformer voltage to be generated and ω_t is the transformer link frequency.

$$\begin{aligned} v^*_{up} &= -\frac{v^*_p}{V_{dc}} - \frac{v^*_{zp}}{V_{dc}} \\ v^*_{lp} &= +\frac{v^*_p}{V_{dc}} - \frac{v^*_{zp}}{V_{dc}} \end{aligned} \tag{5.1}$$

Using PWM, the carrier/switching frequency of this 1ϕ MMC is tuned such that every switching cycle results in one voltage level of the synthesized high frequency voltage. This avoids the need for high switching frequency to generate the near sinusoidal voltage. This tuning requires the effective carrier frequency to be equal to the transformer link frequency ($f_s = f_t$). Thus at every switching cycle, the IGBTs switch such as to insert one capacitor voltage resulting in one voltage step. Nearest level modulation as described in Chapter 3 is another way to modulate the MMC with low switching losses.

The two legs of the MMC generate voltages v_x and v_y at the primary of the HFT. Thus the primary voltage becomes $v_x - v_y$. By using n 3-level submodules in a leg of the MMC, the number of voltage levels obtained using the full modulation index is $2n+1$ (including the zero level). The two legs of the 1ϕ MMC are modulated such as to result in nearly double the number of levels possible $4n+1$. This is done by phase shifting the reference signals v_x^* and v_y^* as shown in (5.2). The effective modulation index obtained is $2m\cos\left(\frac{\pi T_s}{2n}\right)$ as shown in (5.3). Here $\omega_t = 2\pi f_t$ is the transformer link frequency. Since $T_s = \frac{1}{f_s} = \frac{1}{f_t}$ is very small, we can approximate $\frac{\pi T_s}{2n} \approx 0 \implies \cos\left(\frac{\pi T_s}{2n}\right) \approx 1$ and hence the voltage synthesized by the 1ϕ MMC at the primary of the HFT can be approximated as shown in (5.3).

$$\begin{aligned} v_x^* &= mV_t\cos\left(\omega_t t\right) \\ v_y^* &= -mV_t\cos\left(\omega_t t - \frac{\pi T_s}{n}\right) \end{aligned} \tag{5.2}$$

$$\begin{aligned} v_t^* = v_x^* - v_y^* &= \left\{2m\cos\left(\frac{\pi T_s}{2n}\right)\right\} V_t\cos\left(\omega_t t - \frac{\pi T_s}{2n}\right) \\ &\approx 2mV_t\cos\left(\omega_t t\right) \end{aligned} \tag{5.3}$$

5.3.2 Capacitor Voltage Balancing

The entire control system block diagram for the MMC is shown in Fig. 5.4. The modulation block generates ideal gate signals S_i for the IGBTs telling how many submodules and corresponding capacitors need to be inserted in the upper arm and lower arm respectively. Regardless which submodule capacitor is inserted, as long as the appropriate number is maintained, the output voltage synthesis happens correctly. The voltage balancing control assigns these ideal switching signals to the appropriate submodule to obtain capacitor voltage balancing. The capacitors with the highest voltage are used when the MMC is on a discharging state, and capacitors with the lowest voltage are used when it is on a charging state. The direction of arm current $\overrightarrow{I}_{arm}$ is measured to know if the MMC is on a charging state or discharging state. The entire balancing algorithm is described in more detail in [53]. Since the transformer voltage is at much higher frequencies, the need for circulating current control is minimal and is neglected.

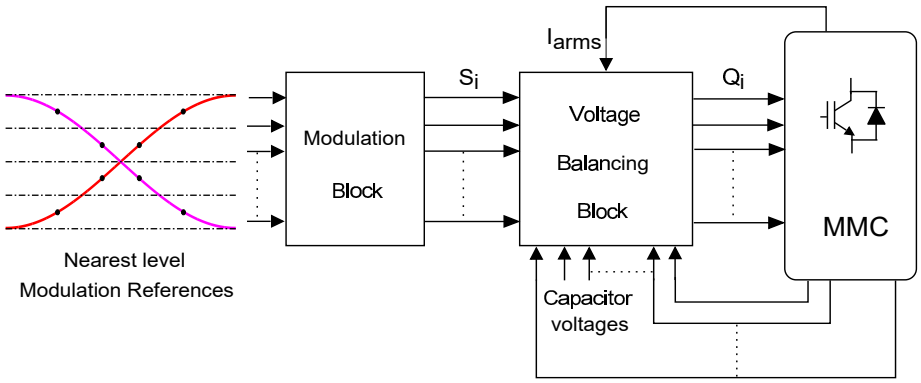


Figure 5.4: MMC control blocks for PET application

5.4 Analysis: HFT and machine interfaced converter

A single multi-winding transformer is used in the proposed PET to interface multiple wind generators. One of the major challenges in PETs being commercialized is design of high power and high frequency transformers, which can spawn future research. The HFT is a step down transformer with N:1 turns ratio. Because of switching at relatively medium frequency (1-20 kHz), nanocrystalline or amorphous cores can be used because of high saturation fluxes and low specific losses [97, 98, 99, 99]. All the windings can be wound on a single core which can result in lower volume and weight. Conventionally, foil windings on the high current side and litz wire on the low current side are utilized. Recent research shows that foil conductors could be used to improve the power density of the HFT while resulting in the same winding loss [100]. Thin foil conductors are used to reduce the eddy currents in case of high power transformers, especially in low voltage winding and also to have maximum filling factor. When interfacing multiple wind generators which are spread out across the wind farm, the transmission line between the distributed wind turbines and the multi-winding transformer sees high frequency sinusoidal voltages. Thus the proposed PET is more suitable when the wind turbines are close together. Using a single primary MMC with multi-winding transformer makes it more compact than having individual PETs for each wind turbine.

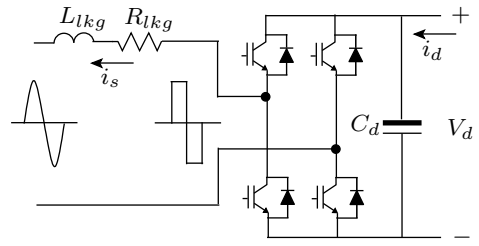
The sinusoidal voltage generated at the secondary of the HFT is interfaced to low voltage DC using a full bridge converter as shown in Fig. 5.5(a). The transformer has leakage inductances and resistances in its windings. This leakage inductance is used

for current smoothening in the link. The leakage inductance L_{lkg} is the combination of the secondary side leakage inductance L_s and the primary leakage inductance L_p referred to the secondary side ($L_{lkg} = L_p \left(\frac{1}{N}\right)^2 + L_s$). The leakage resistance obtained similarly provides damping. Similar to conventional diode bridge rectifier, the LVDC bus has an average DC value given by (5.4). With increase in value of L_{lkg}, the current tends to become more sinusoidal, but it results in a lower value of rectified voltage V_d and hence lower i_s as shown in Fig. 5.5(b). However, this can be adjusted by taking a proper turns ratio of the transformer to generate a suitable transformer secondary voltage V_s. Medium frequency transformer design with high leakage inductances in the mH range has been proposed in [101] for offshore wind farms. The currents at the high frequency link are smooth having the harmonics at odd multiple of the link frequency. These odd multiple harmonics in the current are not harmful to the MMC as they are further filtered out by the arm inductors. Because of smoothly varying currents, natural commutation of leakage energy of the transformer is possible. Also because of switching of the full bridge rectifier at the zero crossings of the link voltage, natural ZVS is obtained in secondary side converter of the HFT.

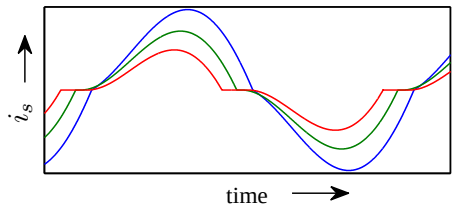
$$V_d = \frac{2V_s}{\pi} - \frac{2\omega_t L_{lkg} I_d}{\pi} \tag{5.4}$$

A PWM inverter is used to synthesize adjustable magnitude and frequency AC at the wind generator terminals. The PWM inverter is modulated using space vector modulation technique to obtain higher voltage gain. The net output voltage generated from this PET depends upon the modulation indices of both the converters (primary side and secondary side) along with the transformation ratio of the HFT. The peak amplitude of the voltage V_M generated at the wind generator terminals can be expressed in terms of the utility grid voltage V_g as given by (5.5). Here the MMC is modulated to operate at unity modulation index between the low frequency utility grid and high frequency transformer link. $\cos\phi_g$ is the power factor at the utility grid which is generally controlled to be at unity and m_v is the modulation index of the PWM inverter.

$$V_M = \frac{4}{\pi}\frac{1}{N} m_v V_g \cos\phi_g \tag{5.5}$$



(a)



(b)

Figure 5.5: (a) Full-bridge converter, (b) Variation of current i_s with different values of L_{lkg}

5.5 Results

The HVDC/AC power electronic transformer topology as shown in Fig. 5.2(a) is simulated with ideal switches in MATLAB/Simulink with parameters as shown in Table 5.1. The parameters are chosen considering interface of a 13.8 kV ac utility grid. The medium voltage DC bus is hence chosen at 22.5 kV and a single phase MMC interfaces with the high frequency transformer. Each leg of the MMC consists of eight 3-level submodules switching at 2 kHz. The HFT has two secondary windings feeding two machines with different operating parameters.

For generating the transformer link frequency of 2 kHz, a single phase MMC is used switching at 2 kHz. As shown in Fig. 5.6 (top), it reaches 33 distinct levels because of the proposed modulation in Section 5.3. A 2 kHz switching frequency is used which results in just one switching per voltage level every T_s period. The frequency spectrum shown in Fig. 5.6 (second from top) shows a THD content of 2.62%. On the secondary side of the HFT, the full-bridge converts the sinusoidal voltages to DC. The current waveform at the primary is smoothly varying and near sinusoidal as shown in Fig. 5.6 (third from

Table 5.1: Multi-winding PET: Simulation Parameters

Parameters	**Value**
DC bus voltage V_{dc}	22.5 kV
Submodule capacitor (MMC)	C_1=5 mF, C_2=10 mF
Arm inductor L_a	2.5 mH
Transformer	12 : 1, 2 kHz, L_{lkg}=0.5 mH
Machine 1	200 kW, 30 Hz
Machine 2	100 kW, 60 Hz

top). By using an appropriate leakage inductance the THD obtained is 7.63% in the primary current and has dominant odd harmonics as shown by the logarithmic scale in the frequency spectrum in Fig. 5.6 (bottom). The voltage balancing is done using the sorting algorithm described in Section 5.3. The balanced capacitor voltages show distinct balanced waveforms which are the voltages in the upper arm and the lower arm for all the capacitors C_1 and C_2 respectively, Fig. 5.7(a). It shows that all the capacitor voltages follow together and are fluctuating around the nominal voltage of 2812.5 V.

Two PWM inverters operating with space vector modulation at full modulation index are used to interface two machines with different operating parameters. The line to neutral voltage and three line currents are shown in Fig. 5.7(b). We see clearly different frequencies of 30 Hz and 60 Hz in these waveforms. Thus the proposed PET can interface multiple renewables running at different operating conditions.

5.6 Summary

A power electronic transformer based on modular multilevel converter is proposed in this chapter which results in sinusoidal voltages and smooth currents through the high frequency transformer. This results in significant reduction in the transformer losses and also natural commutation of leakage energy is obtained. A multi-winding transformer is

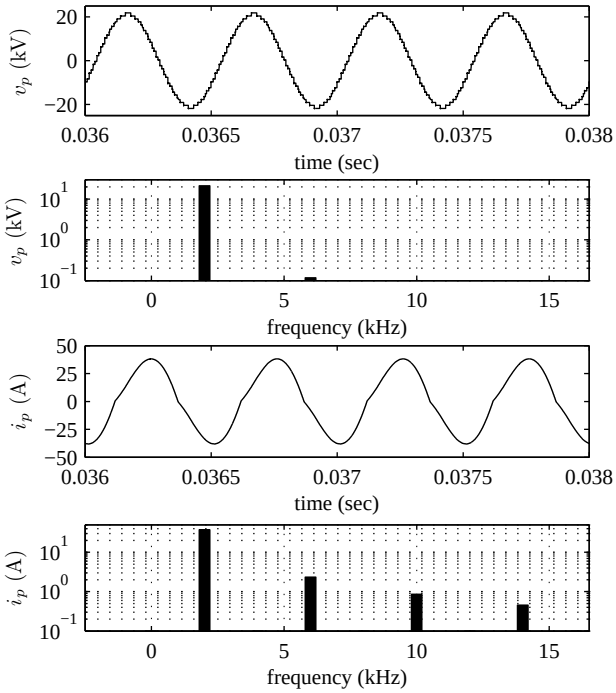
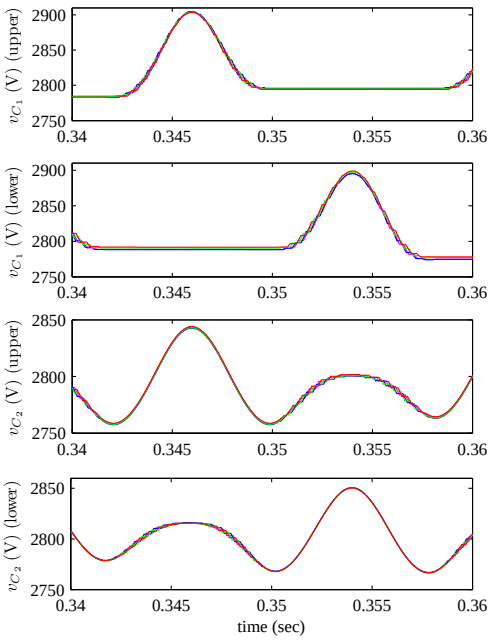


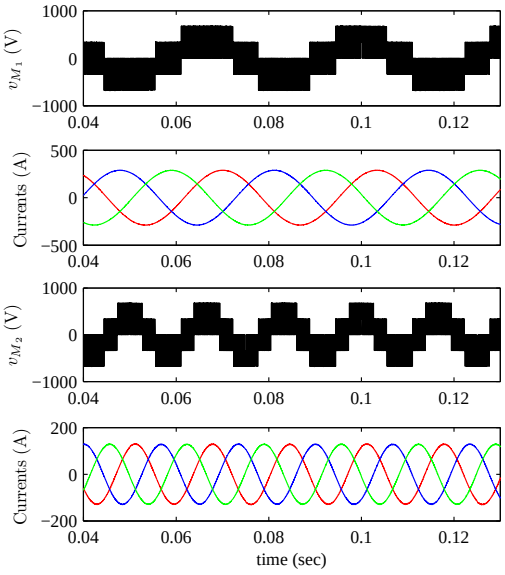
Figure 5.6: (top to bottom) Transformer primary voltage and its frequency spectrum, transformer primary line current and its frequency spectrum (frequency spectrum y-scale: logarithmic)

used to interface multiple renewable energy sources with a high/medium voltage AC/DC grid. The operating principle, modulation and control of the proposed PET along with results have been presented.

Note: Part of this chapter is reproduced from my previous publication [16].



(a)



(b)

Figure 5.7: (a) (top to bottom) Balanced voltages of C_1 in upper and lower arm, balanced voltages of C_2 in upper and lower arm (b) Line to neutral voltage and line currents for Machine 1 (top) and Machine 2 (bottom)

Chapter 6

Conclusion and Future Work

Integration of renewables (solar, wind) and motors into the power grid requires a bulky low-frequency transformer to interface the different voltage levels in a power system. A substitute to this bulky line frequency transformer is the power electronic transformer (PET) (also called solid state transformer/ smart transformer), which can be significantly smaller and offers numerous features which contribute towards a smarter electric grid. To quickly increase their penetration, this dissertation proposes a modular multilevel converter (MMC) based power electronic transformer (PET) which represents a breakthrough in interfacing renewables and micro-grids at much higher voltages than 4.16 kV. This novel interface can be scaled up to accommodate various voltage and power levels, e.g., 34.5 kV that has become de-facto collection grid voltage in utility- and community-scale renewable/storage plants. With substantial increase in the overall system efficiency, reliability, and lower cost, this interface promises a highly efficient, flexible and stable power grid capable of handling future challenges. The research focus is on the overall design, development and control of the proposed system.

The proposed interface uses a modular multilevel converter (MMC) arrangement which is by far the most competitive and widely sought solution for future HVDC projects. The use of several converter modules makes this technology scalable and compact and also results in improved reliability and low turnaround time in case of failures. This interconnection also results in near sinusoidal voltage waveforms, eliminating the need for bulky AC filters and allowing the individual semiconductor switches within the modules to operate at much lower switching frequencies. The proposed MMC-based

PET system has two back-to-back connected MMCs, one interfacing the utility grid and the other generating high frequency sinusoidal voltages across a high frequency transformer (in kHz range). This is interfaced by another power electronic converter doing frequency conversion (kHz to Hz) interfacing the renewable energy source or motor drive.

Chapter 2 presents new submodule structures for modular multilevel converter based HVDC system with advanced features. This MMC interfaces the high voltage utility AC grid on one side and the high voltage DC bus on the other. The newer submodule topologies can reach three voltage levels resulting in half the number of submodules required, as compared to conventional half-bridge submodules. This reduces the additional requirements in each submodule of protection thyristor, bypass switch and bus-bar connections. Added benefits include considerable lower semiconductor losses and reduced gate drive requirement. A hybrid modulation technique combining both phase shifted and level shifted carriers is presented. For proper operation of the new MMC, voltage balancing algorithm based on unequal capacitor sharing and circulating current control for suppressing 2nd harmonic component is proposed. Practical considerations of switch commutation and precharge are addressed for the new submodules. The results are shown by MATLAB/Simulink simulations and experimental results on a scaled down laboratory prototype. A qualitative and quantitative comparison with other existing MMC submodule topologies is presented.

Operation of the MMC to generate high frequency (kHz range) sinusoidal voltages is discussed in Chapter 3. With sinusoidal voltages through the high power transformer, magnetic losses are greatly reduced making the proposed interface more efficient than topologies in existing literature. Fundamental switching frequency modulation techniques like nearest level modulation with $n + 1$ and $2n + 1$ output voltage levels is investigated to reduce switching losses in transformer interfaced MMC operation. Effects on circulating currents and voltage balancing is analyzed. It is observed that in the MMC interfacing the HFT, the arm inductors and floating capacitors can be substantially small compared to the MMC for grid integration. A comparison of different modulation techniques is shown and validated with simulation and experimental results.

A single-stage HVDC/AC power electronic transformer based on modular multilevel converter is presented in Chapter 4 which results in sinusoidal voltages and currents through the high frequency transformer. This results in significant reduction in the transformer losses and also natural commutation of leakage energy is obtained. A matrix converter is proposed as the machine interfaced power converter which always operates at its full modulation index and does frequency conversion only (kHz to Hz). An advanced control at varying machine speeds is proposed by controlling the modulation index of the MMC to result in lower voltage stress related losses in the transformer, matrix converter and the machine. The operating principle, space vector modulation of matrix converter and high frequency link filter design is presented. Improvement in voltage THD and common mode voltage at the machine terminals is validated by simulation and experimental results.

Chapter 5 presents a different variant of the PET topology discussed in Chapter 4. This is based on a two-stage HVDC/AC PET system with a multi-winding transformer to interface multiple renewable energy sources. It results in sinusoidal voltages and smooth currents through the high frequency transformer, retaining the same advantages as discussed in Chapter 4. The operating principle, modulation and control of the proposed PET along with results have been presented.

In a nutshell, this thesis presents a new interface based on a modular multilevel converter based power electronic transformer for integrating low voltage renewables and motor drives to high voltage utility grid. The thesis discussed the operation and control of such an interface while addressing key challenges. Based on the contributions of this thesis, several future research possibilities are as listed below:

- This dissertation presented a MMC-based PET topology for integration of low voltage renewables and motor drives to medium/high voltage utility grid. However, analysis of various parts of the system were shown separately. A future work would be combining the whole system in hardware and validating it experimentally.

- Modulation and control of proposed PET with other machine interfaced power converters like open end drives, etc can be investigated. This would be with a focus on gaining higher voltage transfer ratio of the machine interfaced power

converter and common mode voltage elimination.

- Design of high-frequency transformers at high voltages using finite element analysis tools for loss and leakage inductance optimization.
- Analysis of various ancillary services like operation under unbalance voltages, reactive power and voltage support, frequency regulation and low-voltage ride-through and test them on the fabricated hardware prototype.
- Investigation of the proposed PET topology to interconnect different micro-grids and microgrid to the main grid. These would be operating at different voltages and frequencies and the MMC-based PET would act as the interface between them.
- Comparison with other PET topologies in literature experimentally in terms of losses, volume and cost.

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