High-k Gate Dielectric Materials for CMOS

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Dedication

To my husband, Ralph McCarthy, who encouraged me to pursue this work.

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Chapter 1 - Introduction

1.1 Device Scaling Impact on Gate Oxide Thickness

Continuous improvement in integrated circuit performance relies on scaling of semiconductor devices to smaller dimensions. The scaling of MOSFETs (metal-oxide semiconductor field effect transistor), a key component of integrated circuits, has allowed for exponential increase in the number of transistors integrated on a chip in accordance with Moore's Law (Figure 1).

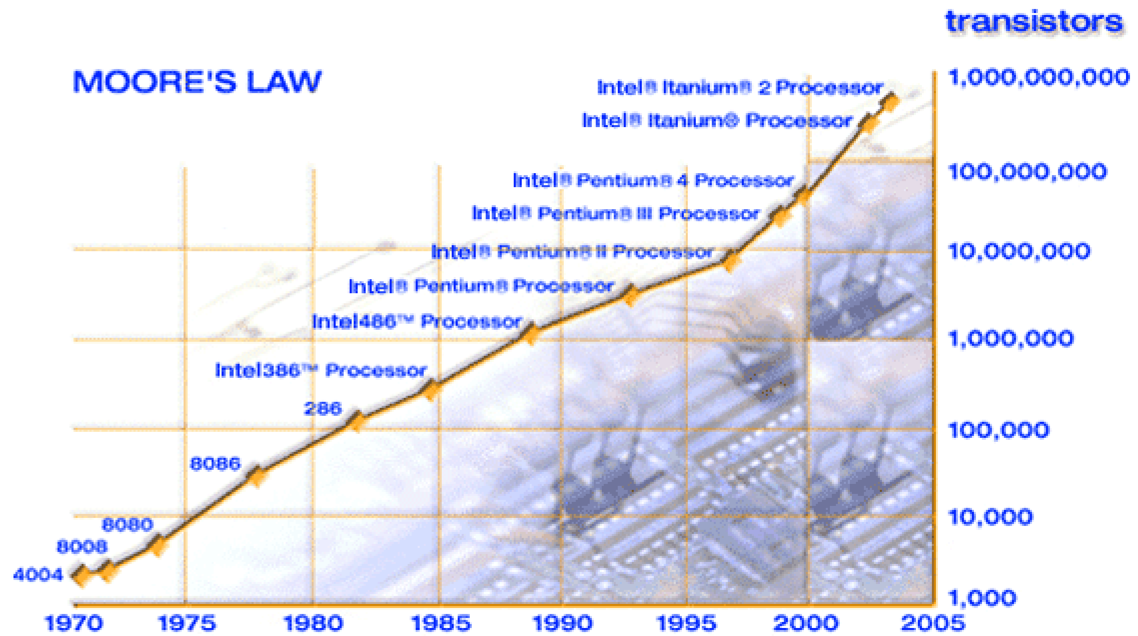

Figure 1. Moore's Law [6].

The key reason for device scaling is improved device performance. Device performance is typically characterized by switching speed, which largely depends on the drive current. However, shortening the transistor gate length to achieve higher drive currents can also result in the short channel effect if the gate oxide is not scaled appropriately to suppress this undesired effect. The gate oxide thickness is limited by the leakage current due to quantum mechanical tunneling of the charge carriers through the gate dielectric and by the reliability issues that arise with ultrathin SiO_2 gate layers (<2nm thick) due to defect generation in SiO_2 which leads to dielectric breakdown resulting from charge carrier flow through the device. The tunneling probability through SiO_2 increases with decreasing layer thickness. One estimate of the SiO_2 thickness limit from a reliability standpoint is ~2.2nm at room temperature and 2.8nm at 150 °C, however thinner oxynitrides have been used in production devices [33, 34].

1.2 Maximizing Switching Frequency and Drive Current Limitations

Switching time (or the switching frequency) used to characterize device performance can be determined using the CMOS inverter as shown in Figure 2.

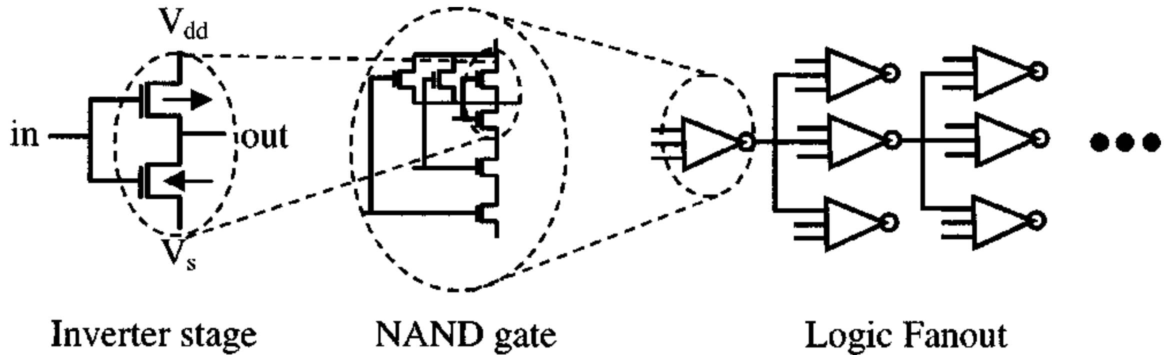

Figure 2. Components used to test a CMOS FET technology. V_{DD} and V_S serve as the source and drain voltages, respectively, and are common to the NAND gates shown. Each NAND gate is connected to three others resulting in a fanout of 3. Ref [5]

The input signal of the CMOS inverter is attached to the gates and the output signal is connected to both the n-MOS and p-MOS transistors associated with the CMOS stage. The switching time is limited by both the fall time required to discharge the load capacitance by the *n*-MOS drive current and the rise time required to charge the load capacitance by the *p*-MOS drive current. Therefore, the switching response time,τ, is given by:

$$\tau = \frac{C_{LOAD} V_{DD}}{I_D} \qquad 1.2.1$$

where $C_{LOAD} = FC_{GATE} + C_j + C_i$, and C_j and C_i are parasitic junction and local interconnection capacitances, respectively. F is the "fan out" for interconnected devices. The delay in gate electrode response can be ignored, since $\tau_{GATE} << \tau_{n,p}$, so the average switching time can be expressed by:

$$\bar{\tau} = \frac{\tau_p + \tau_n}{2} = C_{LOAD} V_{DD} \frac{1}{I_D^n + I_D^p} \qquad 1.2.2$$

The load capacitance of a single CMOS inverter can be approximated by the gate capacitance if parasitic contributions such as junction and interconnect capacitance are ignored (assumed

negligible). According to equations 1.2.1 and 1.2.2, an increase in *ID* results in reduced switching speeds.

For more realistic estimates of microprocessor performance, the load capacitance is connected to other inverter elements in a predetermined fashion. When coupled with other NMOS/PMOS transistor pairs in the configuration shown in Figure 2, one can create a logic ‘‘NAND’’ gate which can be used to investigate the dynamic response of the transistors and thus examine their performance under such configurations. For example, in microprocessor estimates, a fan out of *F*=3 is often employed, as shown in Figure 2. One can then characterize the performance of a circuit (based on a particular transistor structure) through this switching time. To do this, various ‘‘figures of merit’’ (FOM) have been proposed which incorporate parasitic capacitance as well as the influence of gate sheet resistance on the switching time. For example, a common FOM employed is related to equation 1.2.2 by [5]:

.

$$FOM \cong \frac{1}{\bar{\tau}} = \frac{2}{\tau_p + \tau_n} \qquad 1.2.3$$

As mentioned earlier, switching time can be reduced by increasing drive current. The drive current can be written (using the gradual channel approximation) as [5]:

$$I_D = \frac{W}{L}\mu C_{inv}\left(V_G - V_T - \frac{V_D}{2}\right)V_D \qquad 1.2.4$$

where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility (assumed constant), C_{inv} is the capacitance density associated with the gate dielectric when the underlying channel is in the inverted state, V_G and V_D are the voltages applied to the transistor gate and drain, respectively, and the threshold voltage is given by V_T.

The inversion capacitance density can be calculated as follows:

$$C_{inv} = \frac{C_{ox}}{1 + \frac{k_{ox}W_T}{k_s t_{ox}}} \qquad 1.2.5$$

where C_{ox} is the gate oxide capacitance density, k_{ox} is gate oxide dielectric constant, W_T is the depletion width, k_s is the dielectric constant of the semiconductor and t_{ox} is gate oxide thickness.

The drain current is proportional to the average charge across the channel (with a potential $V_D/2$) and the average electric field (V_D/L) along the channel direction. Initially, I_D increases linearly with V_D and then eventually saturates to a maximum when $V_{D,sat} = V_G - V_T$ to yield

$$I_{D,sat} = \frac{W}{L} \mu C_{inv} \frac{(V_G - V_T)^2}{2} \qquad 1.2.6$$

The term ($V_G - V_T$) is limited in range due to reliability and room temperature operation constraints, since too large a V_G would create an undesirable, high electric field across the oxide. Furthermore, V_T cannot easily be reduced below about 200 mV, because kT=25mV at room temperature. Typical specification temperatures (<100 °C) could therefore cause statistical fluctuations in thermal energy, which would adversely affect the desired V_T value. Thus, even in this simplified approximation, a reduction in the channel length and/or an increase in the gate dielectric capacitance will result in an increased $I_{D,sat}$.

Reduction in channel length leads to short channel effects (Figure 3), which result in different I_D vs. V_D characteristic (non-zero slope in I_D vs. V_D as shown in Figure 4) after pinch-off and reduced V_T as a result of drain induced barrier lowering (DIBL) – shown in Figure 5.

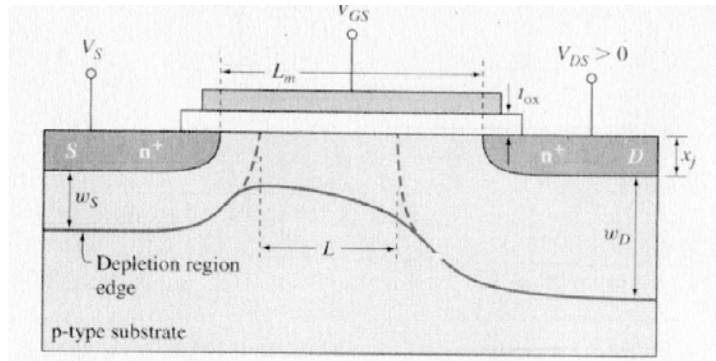

Figure 3. Short channel device [14].

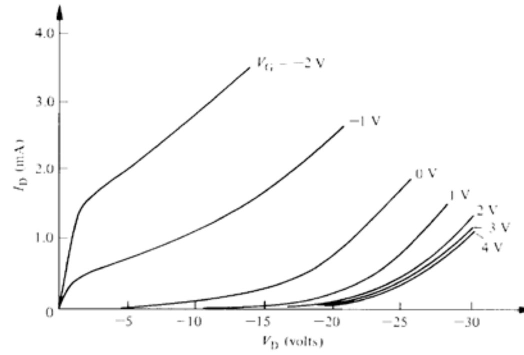

Figure 4. I_D -V_D characteristics of a MOSFET exhibiting severe short-channel effects [13].

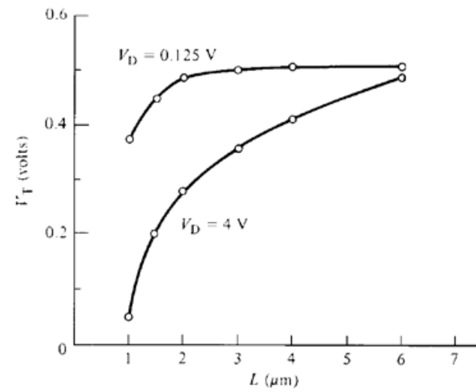

Figure 5. Observed threshold-voltage variation with channel length and applied drain bias in short-channel MOSFETs [13]

The difference between long- and short channel behavior depends on the oxide thickness t_{ox}, the source and drain junction depth x_j, and the depletion region thickness at the source, W_s, and drain, W_D.

The minimum channel length below which significant short channel effects are expected to occur must be greater than the sum of the source and drain depletion widths, which can be estimated using the empirical relationship known as Brew's rule [13]:

$$L_{\min} = 0.4[x_j t_{ox}(W_S - W_D)^2]^{1/3} \qquad 1.2.7$$

where x_j is source/drain junction depth, t_{ox} is the oxide thickness, and W_S and W_D are source and drain depletion widths, respectively. In order to ensure long channel operation in MOSFET, L_{min}

must be reduced by making shallower source/drain islands, increasing substrate doping to decrease source and drain depletion widths, and/or reducing gate oxide thickness [13].

1.3 Gate Dielectrics and Leakage Current Density Requirements

Physical gate oxide thickness is limited by the leakage current density requirements. Quantum mechanical tunneling of electrons through the thin gate oxide results in significantly large leakage current densities. Therefore, the physical gate oxide thickness limit for SiO_2 gate oxide is thought to be ~2nm. SiO_2 does not form a full band gap below 0.7nm thickness, which would result in high leakage current in this gate dielectric thickness range (Figure 6).

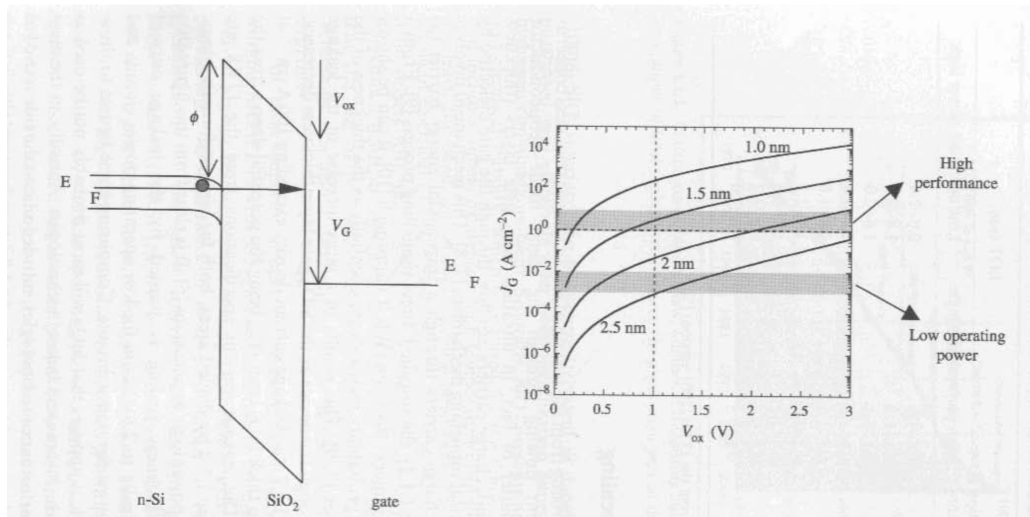

Figure 6. Quantum mechanical tunneling through the oxide layer in MOS structure (left). Leakage current density [4].

In addition to leakage current, there is also a reliability concern with ultrathin SiO_2 gate layers (<3nm thick) due to defect generation in SiO_2 which leads to dielectric breakdown resulting from charge carrier flow through the device, although the exact thickness reliability limits are somewhat controversial.

The metal oxide semiconductor structure (MOS) behaves as a parallel plate capacitor. Its capacitance can be increased either by decreasing the oxide thickness or by increasing the relative dielectric constant. MOS capacitance can be expressed as:

$$C_{ox} = \frac{Ak\varepsilon_o}{t_{ox}} \qquad 1.3.1$$

where A is the area of the capacitor plates, k is the dielectric constant, ε_0 is permittivity of air and t_{ox} is oxide thickness.

Since the gate oxide thickness is limited by the leakage current due to tunneling, it is necessary to increase the relative dielectric constant (k), which requires the use of new materials for the gate dielectric. High-k materials can meet the leakage current requirement by achieving lower equivalent oxide thickness (EOT) as shown in Figure 7.

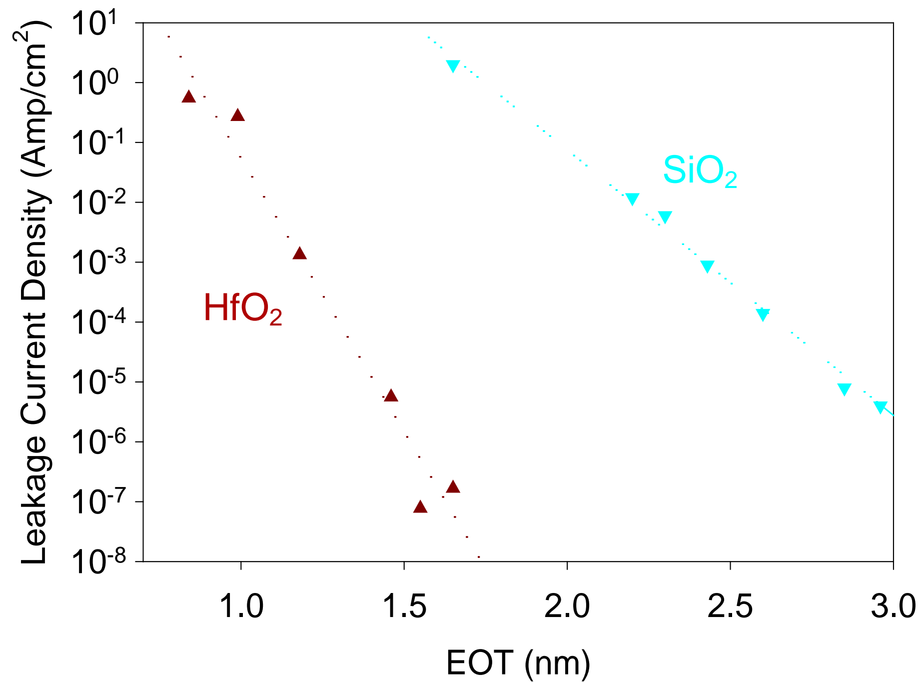

Figure 7. Leakage current vs. EOT.

Increasing k allows for thicker oxides to be used to achieve the same capacitance as the thin SiO_2. Therefore, the physical thickness of the high-k material can be much higher than the physical thickness of SiO_2 while maintaining the same capacitance density. The thickness of SiO_2 that is required to achieve the same capacitance density as the high-k material is referred to as the equivalent oxide thickness (EOT) and can be calculated as follows:

$$EOT = k_{SiO_2} \frac{t_{high-k}}{k_{high-k}} \quad 1.3.2$$

1.4 Impact of Oxide Fixed Charge on Device Performance

Fixed charge accumulation in the oxide can greatly impact device performance by shifting the flat band voltage. Many dielectrics exhibit a fixed charge (Q_F), which requires an applied voltage in order to achieve a flat band condition. The amount of fixed charge can be determined from V_{FB} using the following expression:

$$V_{FB} = \Phi_{MS} \pm \frac{Q_F}{C_{acc}} \qquad 1.4.1$$

where Φ_{MS} is the difference in the work functions between metal and semiconductor, Q_F is the fixed charge density, and C_{acc} is the measured capacitance in accumulation.

Thus, a value for fixed charge density Q_F can be determined from measured values of V_{FB}, Φ_{MS} and C_{acc} .

Negative V_{FB} (from ideal conditions) is required for positive Q_F for both *n*-type and *p*-type MIS structures. Similarly, a positive V_{FB} is required for negative Q_F.

A significant amount of fixed charge may result in performance issues for CMOS applications. Due to the scaling limitations on applied voltages and power consumption, shifts in the flat band voltage must be avoided. Furthermore, a reproducible V_{FB} (or V_T) value is required for stable and reliable transistor performance. Presence of positive charge in the oxide will shift the C-V curve to the left while the presence of negative charge in the oxide will shift the C-V curve to the right for both n-MOS and p-MOS devices as shown in Figure 8. Classically, the fixed charge is independent of oxide thickness and semiconductor doping conditions and it is a strong function of the annealing conditions. Fixed charge in oxides can be greatly reduced by annealing at high temperature in an inert atmosphere.

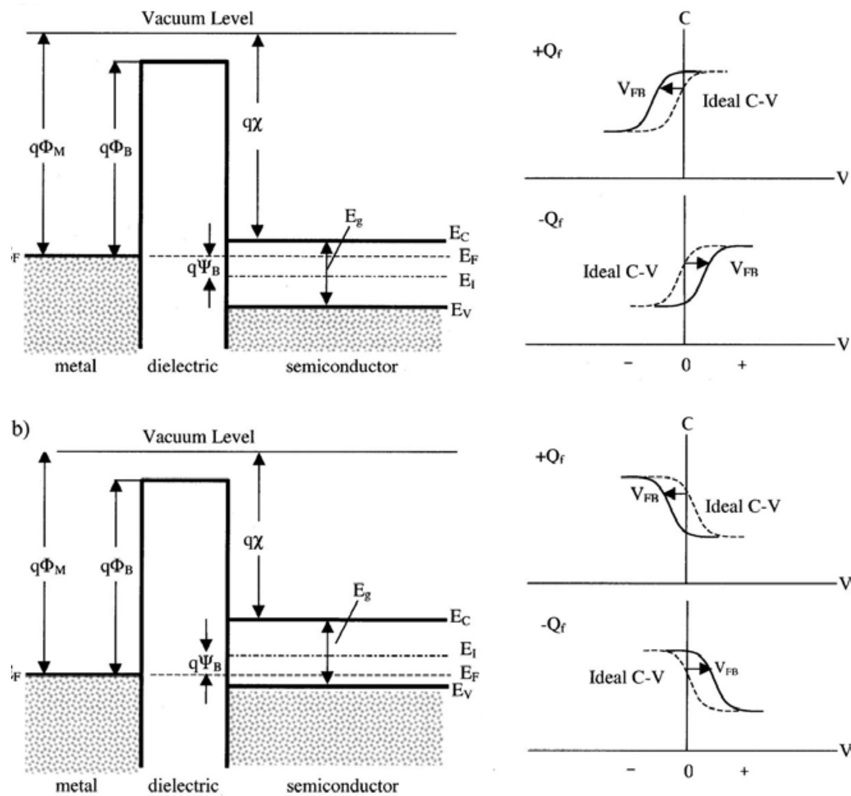

Figure 8. CV characteristic of non-ideal n-MOS and p-MOS (V_{FB} shift due to fixed charge in the oxide) [5].

1.5 High-k Gate Dielectric Materials

It can be argued that the key element enabling the scaling of the Si-based metal–oxide–semiconductor field effect transistor (MOSFET) is the materials and resultant electrical properties associated with the dielectric employed to isolate the transistor gate from the Si channel in CMOS devices for decades: silicon dioxide. The use of amorphous, thermally grown SiO_2 as a gate dielectric offers several key advantages in CMOS processing including a stable (thermodynamically and electrically), high-quality Si– SiO_2 interface as well as superior electrical isolation properties. In modern CMOS processing, defect charge densities are on the order of $10^{10}/cm^2$, midgap interface state densities are $10^{10}/cm^2$ eV, and hard breakdown fields of 15 MV/cm are routinely obtained and are therefore expected regardless of the device dimensions. These outstanding electrical properties clearly present a significant challenge for any alternative gate dielectric candidate [5].

Silicon oxynitride gate dielectric was introduced as a higher k material ($4 < k < 7$) which had the added benefit of decreasing boron penetration, which enabled the industry to continue to scale the oxide and meet the leakage current and power dissipation requirements for high performance logic and low operation power logic applications. Due to recent improvements in device performance through increased channel mobility by introduction of strained silicon and aggressive scaling of the junction depths, the need for high-k was postponed one generation. The use of silicon oxynitride as the gate dielectric was extended to the 65 nm node.

Oxynitride, however, no longer meets the strict leakage current requirement in low-power applications (10^{-3} A/cm^2) when scaled below the equivalent oxide thickness (EOT) of 1nm. Therefore, introduction of higher dielectric constant (high-κ) material in which tunneling current can be suppressed while maintaining the drain current was necessary for the 45 nm technology node. The gate electrode material and process needed to be optimized so that the depletion width in the gate electrode would be minimized and the boron-diffusion prevented. The former necessitates the introduction of metal gates having appropriate work function after the conventional poly Si ceases to work. These material changes posed a great challenge in MOSFET technology, where silicon dioxide/poly Si has long played a central role as the most reliable gate stack system.

High κ dielectric and metal gate electrode will be required beginning in ~2008. Timely implementation will involve dealing with numerous challenging issues, including appropriate tuning of metal gate work function, ensuring adequate channel mobility with high-κ, reducing the defects in high-κ to acceptable levels, ensuring reliability, and others [3].

For every 0.5nm decrease in thickness of SiO_2, gate leakage current density rises about 2 orders of magnitude [1], [2]. Although increasing permittivity is required to reduce gate leakage current density, in simple dielectrics, higher permittivity will result in smaller bandgap and higher leakage current as described by E_G vs. k in equation 1.5.1 and Figure 9. Therefore, simple dielectrics are not suitable for devices scaled below 1.3nm [5, 35].

$$E_G \approx 20\left[\frac{3}{2+k}\right]^2 \qquad 1.5.1$$

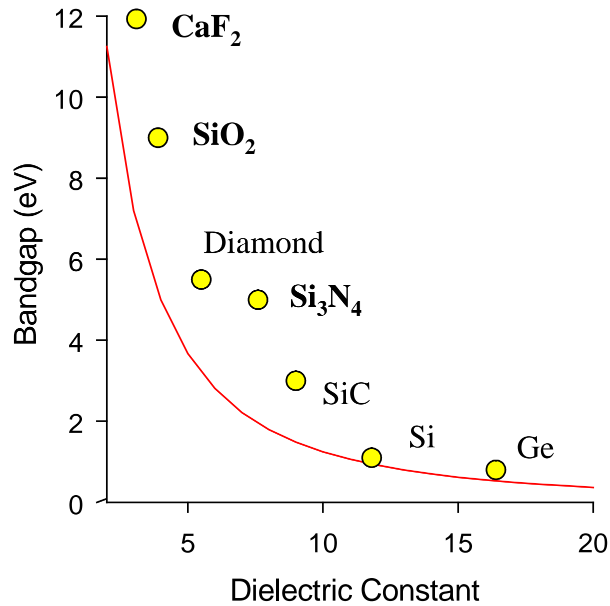

Figure 9. Bandgap vs. Dielectric Constant for simple dielectrics.

To overcome permittivity vs. bandgap relationship, one must use lattice polarizable materials. The polarization is due to a distortion of the valence shell electrons. In these films, one or more atoms will shift position in response to an externally applied electric field. The resultant bond stretch produces a sizable dipole that leads to large permittivities (candidates: TiO_2, ZrO_2, Ta_2O_5, Al_2O_3, HfO_2) as shown in Figure 10. Although a similar relationship exists between bandgap and dielectric constant, leakage current becomes less of a concern since higher oxide thickness is allowed to achieve the same gate stack capacitance with high-k materials.

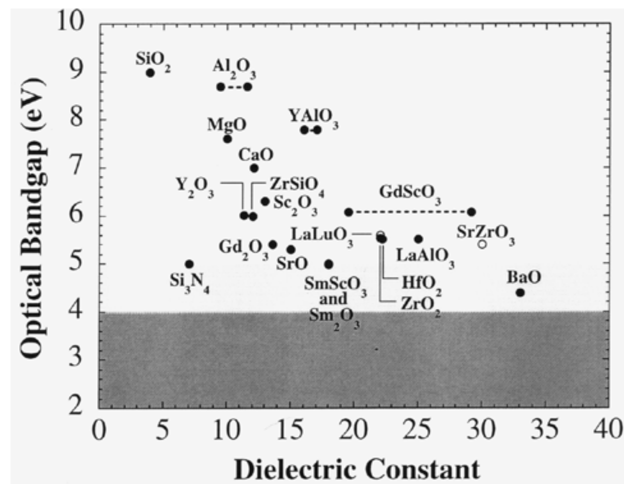

Figure 10. Bandgap vs. Dielectric Constant for Lattice Polarizable Materials.

There are two general concerns related to high-k gate dielectrics. The first involves the interface layer (low-k layer), which forms between the Si substrate and high-k dielectric. This layer usually forms during high-k deposition or during post-deposition annealing and it makes it difficult to achieve EOT of < 1nm. Another low-k layer may also form at the interface between the high-k gate dielectric and the metal gate.

The total capacitance of the gate stack then results from the series combination of the low-k and high-k dielectric layer capacitances:

$$\frac{1}{C_{tot}} = \frac{1}{C_{low-k}} + \frac{1}{C_{high-k}} \quad 1.5.2$$

The equivalent oxide thickness is then calculated as follows:

$$EOT = k_{SiO_2}\left(\frac{t_{low-k}}{k_{low-k}} + \frac{t_{high-k}}{k_{high-k}}\right) \quad 1.5.3$$

The equivalent oxide thickness increases by the factor of $k_{SiO2}*(t_{low-k}/k_{low-k})$ when the low-k interfacial layer is present. Typically, two interfacial layers are seen in MOS high-k capacitors, one at the upper interface between the gate electrode and the high-k film and the other at the lower interface between the Si substrate and the high-k film (Figure 11). Both of these layers, and particularly the lower layer, will reduce the overall dielectric constant of the high-k stack, thereby increasing EOT.

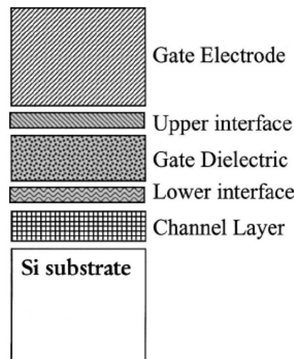

Figure 11. Typical high-k gate stack with interfacial layers. [5]

The second concern is mobility degradation. The silicon substrate and high-k interface degrade the electron and hole mobility. Mobility directly affects the drain current of the transistors and therefore switches the speed of the circuits. This problem can be remedied with high temperature gas annealing (~600C) or by the use of an extremely thin SiO_2 layer before the high-k dielectric [4]; however, the latter approach will degrade the total capacitance of the gate dielectric and increase equivalent oxide thickness.

Key materials considerations for high-k gate dielectric are: permittivity, band gap, barrier height, thermodynamic stability on Si, interface quality, film morphology, gate compatibility, process compatibility, and reliability. Fundamental limitations such as fixed charge, dopant depletion in the poly-Si gate electrode, and an increasing electric field in the channel region, which decreases device performance must be overcome. Furthermore, dopant diffusion characteristics, failure mechanisms, and reliability of any potential high-k dielectric need to be understood.

Various high-k dielectrics have been studied since the late 1990s. The leading candidates are HfO_2 and related compounds. TiO_2 studies showed that despite its high dielectric constant, this material is not suitable as a gate dielectric due to high leakage currents caused by oxygen vacancies which serve as carrier traps. Ti has several stable oxidation states of Ti^{3+} and Ti^{4+} which lead to reduced oxide in materials containing Ti–O bonds. In addition, TiO_2 crystallizes at temperatures much above 400°C [7] and it is not stable on Si during CVD deposition [8], resulting in interfacial layers at the channel interface and at the metal gate interface.

Material systems such as Ta_2O_5 and $SrTiO_3$, which have dielectric constants ranging from 10 to 80 have been studied as the potential candidates for high-k gate dielectric due to their wide use in the memory capacitor applications; however, the majority of these materials are not thermodynamically stable in contact with Si.
The bonding arrangement of Ti produces an unfavorable band alignment with silicon. Studies of $HfTiO_4$ suggest that the band gap of this material is approximately 4.4 eV with little evidence of Ti 3d orbital lower energy state [12]. Permittivities were found to be about 35 due to hybridization of the 3d state. However, the use of Ti in high permittivity materials remains a concern due to its low energy valence band and stability concerns.

Al_2O_3 is thermodynamically stable on Si, but susceptible to dopant diffusion (boron and phosphorus) [9], which results in fixed charge accumulation due to dangling bonds and flat band voltage shift and has only a moderate permittivity. La_2O_3 has desirable morphology (amorphous at high temperature), is thermodynamically stable, and has low leakage current [10], but this

material also exhibits flat band voltage shift due to fixed charge, which is also an issue with ZrO_2 [11].

Several perovskite materials containing Ti (such as $SrTiO_3$ and $BaSrTiO_3$) were studied [21], [23], and showed to have desirable permittivites, but low conduction band offsets to silicon due to the low energy valence band of Ti. Further studies were conducted to examine the generation of high-k materials based on perovskite structures which contain Hf instead of Ti to overcome the issues with band alignment. An increase in the band offsets is expected when changing from the 3*d*/2*s* valence of Ti to the 5*d*/6*s* of Hf although a reduction in the permittivity will be observed. While there is little data available on compounds of the form $A_XHf_YO_3$ (hafniates), a few reports exist for the corresponding zirconates. Hafniates are expected to behave very similarly, although with a slightly large conduction band offset to Si. The energy for the π-bonding between the O 2*p* and the Zr 4*d* in the $Ba_XSr_{1-X}ZrO_3$ series produces a paraelectric material with a permittivity of approximately 40.

Thus, this research was focused on the materials of the form $A_XB_YO_3$, where A is Sr, and B is Hf. The films were studied and characterized in terms of thickness, composition, and crystal structure. Due to the complexity of the materials, PVD was used rather than CVD to conduct the experiments. Capacitors were built from the high-k films and used to study the effect of the elements and film composition on the permittivity, flatband voltage, leakage current density, band gap and band offsets.

Chapter 2 - Experimental Procedure

Films were made with physical vapor (PVD) codeposition from Hf and SrO targets by depositing on lightly doped p-type 4" (100) silicon wafers. The wafers were cleaned with a conventional RCA process and loaded into the deposition chamber, an AJA 2400, through a load lock system. This system contains four confocal sputtering sources aimed at a 200 mm diameter sample platen, which holds two 100mm wafers. After sample loading, the system was pumped to a base vacuum of $5x10^{-8}$ Torr. Next, Ar was introduced into the chamber at a flow rate of 20sccm, with a pressure set point of 20 mTorr. After the pressure stabilized, RF power was applied to the RF target and the plasma was struck. After the strike step, the pressure was set to 5 mTorr and DC power was applied to the Hf target. Both targets were pre-sputtered while the shutters were closed to remove any surface oxidation. The Hf source was sputtered using a DC plasma, while the SrO target was sputtered using an RF supply (DC is used for metals since the target is conductive, while ceramics require the use RF due to charging).

The targets were 3" in diameter and 0.25" thick including the 0.125" thick copper backing plate. SrO target was manufactured using cup design with a 0.125" thick copper backing plate and a retaining ring around the edge to prevent it from chipping and edge damage during installation. The SrO target was manufactured from pressed powder and would degrade when exposed to air. Therefore, a storage chamber was assembled in order to prevent the target from oxidation and degradation when not in use. The chamber was connected to an Argon supply and was filled with Argon immediately after the target was placed inside and the air was displaced. BaO target was also supplied, but could not be used due to fast degradation when exposed to air even for a few minutes during installation. The substrate heater was not used during the deposition. The substrate was rotated at 5 rpm to improve film thickness uniformity. Gun angle for both targets was set to 10° to optimize sputter yield and uniformity.

The sputter rates of the two materials were studied individually as a function of power and/or as a function of pressure. Hf films were deposited using DC power ranging from 15 to 250 W with a fixed process pressure of 5mTorr. SrO films were deposited at pressures ranging from 3-15 mTorr at a fixed RF forward power of 250W. An attempt was also made to deposit SrO films at RF powers above and below 250W, but was unsuccessful due to matching network limitations that resulted in high reflected power. In addition, HfO_2 deposition was attempted by flowing oxygen during Hf sputtering but resulted in target oxidation and no DC current flow after several runs.

Post deposition annealing in O_2 at temperatures ranging from 450-1050 °C was done either using RTA or a diffusion tube in order to increase the oxygen content and investigate film stability. Thickness was measured both by Gaertner L116A ellipsometer and with Rutherford Backscattering Spectrometry (RBS) using a MAS 1700 pelletron tandem ion accelerator (5SDH) with He+ beam of 2.3 MeV, beam current around 20nA, and charge collection set to 10uC. Good agreement (+/- 5%) was seen between the two methods. The composition was also measured using RBS. XRD measurements were performed using a Bruker AXS Microdiffractometer with a 2.2 kW Sealed Cu X-ray source. Thick films (60 to 100 nm) were deposited to minimize interfacial layer effects and to improve the signal-to-noise ratio of the XRD measurements.

The physical structure was investigated by high resolution transmission electron microscopy (HRTEM) and by x-ray diffraction (XRD). TEM cross-section samples were prepared by standard sample preparation techniques with low-energy Ar+ ion milling as the final step. HRTEM images were taken using a field-emission TEM (Tecnai F30U, Cs = 0.52 mm), which was operated at 300 kV.

MOS capacitors and MOSFETs were fabricated for electrical characterization. After deposition, some of the high-k films were subjected to a post deposition anneal (PDA) with a rapid thermal annealing (RTA) system in an O_2 atmosphere at 600-1050°C for up to 30 seconds. MOS capacitors of 100 μm square were fabricated by depositing a 50nm layer of thermally evaporated Cr as the gate electrode, which was patterned using optical lithography and wet chemical etching. This was done to avoid any additional energetic processing which could introduce charge. For the last fabrication step, the devices were subjected to a H_2 forming gas anneal at 425 °C for 30 min to improve electrode/dielectric interface. This process was not followed for photoconductivity measurements. For this purpose the electrodes of 0.5 mm^2 area were fabricated on top of the oxide by evaporation of semitransparent (15-nm thick) Au layer through a shadow mask.

C–V and I–V characteristics were evaluated using an HP4294A impedance analyzer and an HP4156A precision semiconductor parameter analyzer, respectively. Capacitors were measured in a C_S-R_S mode. The phase angle of the measurements was found to be close to 90°. Measurements were done at 10 kHz, 100 kHz and 1 MHz on 100 um square capacitors. The EOT and flatband voltage values were extracted from the C-V curves using Hauser and Ahmed's technique [22].

Chapter 3 - Results and Discussion

The individual sputter rates of Hf and SrO were studied and characterized in order to predict codeposited film composition and thickness and examine MOS electrical properties and film characteristics for each of the codeposited films. The initial comparison of Hf and SrO sputter rates at DC (or RF) power of 250W and process pressure of 5 mTorr (20sccm Ar flow), showed that the sputter rate of Hf was 26 times faster than that of SrO. This is consistent with AJA PE2400 sputter rates of other metals and oxides; sputter rates of metals are typically in the 100A/min range while those of oxides are 10-20 A/min. The sputter rate of SrO at 250W RF and process pressure of 5 mTorr was only 8.4A/min. As an initial estimate, it was assumed that equal sputter rates would be required to achieve codeposited films with Sr:Hf mole ratio of 1:1. Increasing RF power during SrO deposition to achieve higher sputter rate resulted in RF matching network issues and failure due to high reflected power. Therefore, the Hf sputter rate at lower DC power was examined. Hf sputter rate appeared to be linear in 15-50W range. A minimum of ~ 12 W was required to achieve appreciable Hf film thickness. Hf sputter rate increased by 1.7 A/min for every Watt of DC power as shown in Figure 12. At the DC power of 12W (and process pressure of 5 mTorr), Hf sputter rate was approaching SrO sputter rate (at 250RF and 5 mTorr).

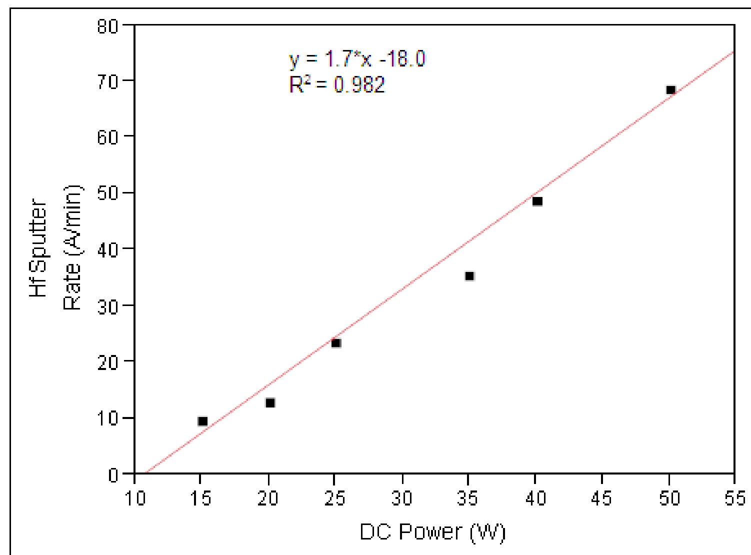

Figure 12. Hf Sputter Rate vs. DC Power.

Since the SrO sputter rate could not be increased by increasing RF power due to matching network limitations, the effect of pressure was studied to determine the optimum pressure for the maximum SrO sputter rate. The effect of pressure was ~30% change in sputter rate for the range of pressures from 3-7 mTorr with the local maximum of 8.4 A/min at 5 mTorr (Figure 13).

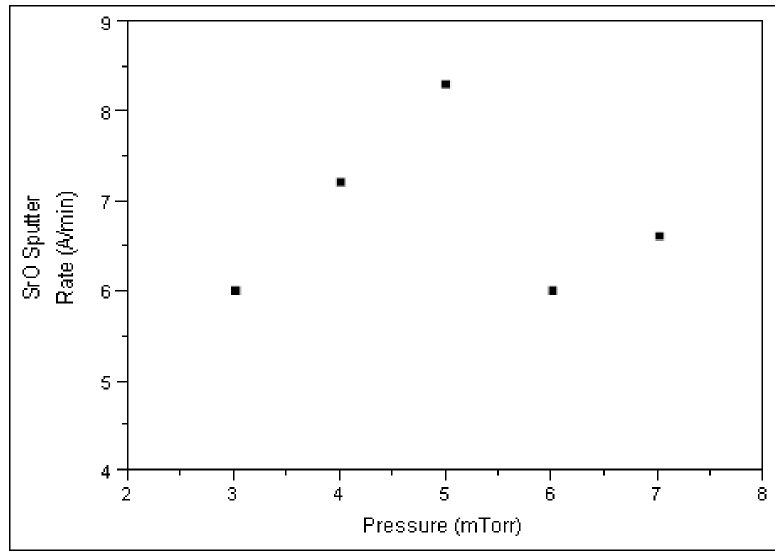

Figure 13. SrO Sputter Rate vs. Chamber Pressure.

Thus, Strontium hafnate films were codeposited at 5 mTorr and film composition and thickness were controlled by varying Hf DC power while maintaining SrO RF forward power at 250W. Film sputter rate (and therefore thickness) was shown to vary linearly with Hf DC power (Figure 14).

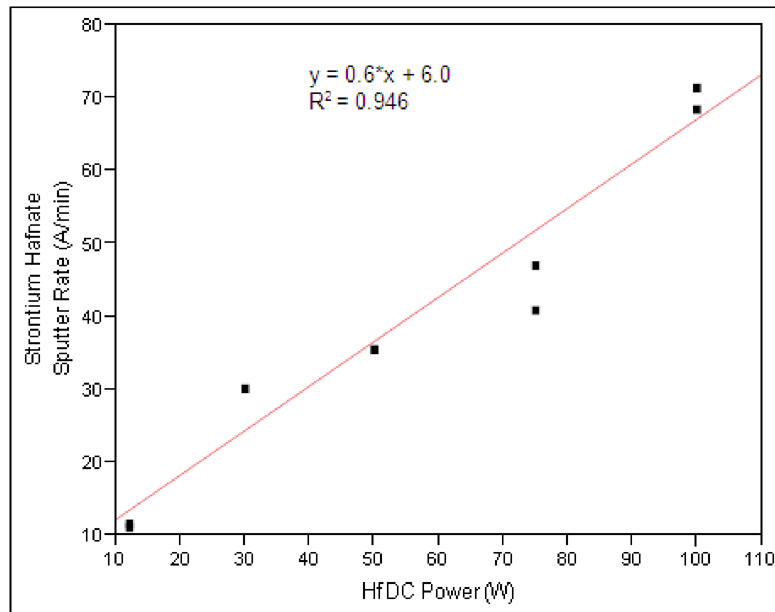

Figure 14. Strontium Hafnate Sputter Rate (A/min) vs. Hf DC Power (W).

However, film composition and power do not have a linear relationship (as shown in Figure 15), which does not agree with the initial prediction based on the individual sputter rates. This could be due to the difference in sticking coefficients or the surface binding energy of Hafnium and Strontium [26]. Surface binding energy is affected by ion bombardment and it varies with surface roughness and damage, but it can also change due to changes in the surface stoichiometry of the compounds. In the case of a diatomic molecule, such as SrO, the surface barrier can be viewed either as only acting on the center of mass or on each atom of the molecule individually. In the first model, only translational motion is altered while in the second model, rotation is strongly affected by the torques exerted by the surface barrier [15], [16]. The nonlinear relationship between film composition and target power could also be due to the difference in angular scattering distribution of each element in the gas phase.

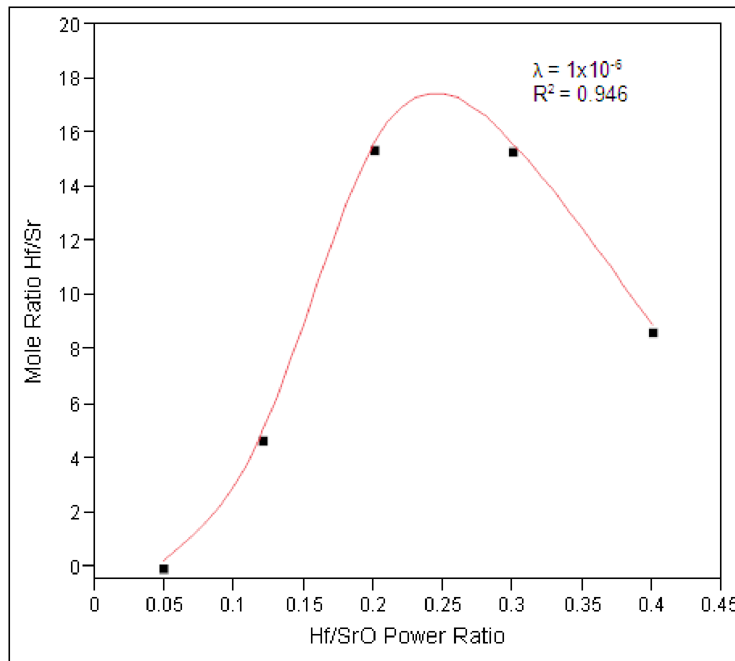

Figure 15. Mole Ratio Hf/Sr vs. Hf/SrO Power Ratio.

Film composition measurements done by RBS on as-deposited strontium hafnate films showed that the films were oxygen deficient and non-stoichiometric. It was previously reported that sputtering from a multicomponent stoichiometric oxide target produces a nonstochiometric oxide thin film [18]. In particular, SrO target, which was manufactured as a pressed powder, behaves very differently from the homogeneus metal targets such as Hafnium. Due to the presence of the different crystallites or powder particles with different compositions or crystal structures, the sputtering yield is often dominated by micro-topography. At low doses, each crystallite is sputtered with different rate determined by its own preferential sputtering and uninfluenced by

neighboring crystallites. When the thickness of the sputtered atom becomes of the order of the crystallite size, the grains with high sputtering yields will shrink and the surface becomes enriched with low-sputtering yield grains, which is referred to as selective sputtering [17]. This problem can be avoided by depositing at higher pressures [19], but, higher pressures could not be used here since the effect of higher pressures was to reduce the SrO sputter rate. Thus, an attempt was made to flow O_2 during Hf sputtering. However, this attempt resulted in Hf target oxidation and blocked DC current flow after a few runs. The effect of introducing O_2 flow during Hf sputtering was to increase the sputter rate such that for every Watt of DC power, the sputter rate increases by 5 A/min (Figure 16).

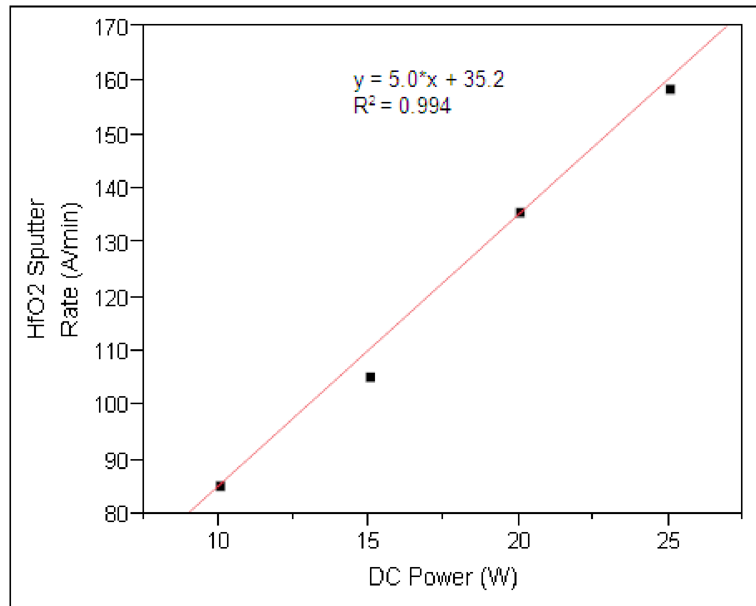

Figure 16. HfO2 Sputter Rate (A/min) vs. DC Power (W).

As-deposited films appeared to be amorphous as measured by XRD. Hf-rich films crystallized as expected when annealed at high temperature; they remained amorphous at the annealing temperatures of 450 °C, but crystallized at 1050 °C. Sr-rich films, however, appeared to remain amorphous (Figure 18) even when annealed at 1000 °C. This agrees well with HfO_2 results reported by D. Triyoso et. al [25], where hafnium oxide films were amorphous as deposited, but became polycrystalline when annealed at 800C.

Hf-rich films had k values of ~14, which agrees well with the k value of amorphous HfO_2. Film with Hf/(Hf+Sr) ratio of 0.9 annealed in oxygen at 1050 °C had a flat band voltage of 0.51V and EOT of 29.4nm (the physical thickness of the film was 104.4nm) and interface charge density of -

$5.29x10^{10}/cm^2$ obtained from -3 to +3 C-V sweep at 100kHz as calculated using CVC program which corrects for surface quantum mechanical effects. Threshold voltage, V_T', calculated based on the ideal n-channel device, was 1.75V.

$$V_T^{'} = 2\phi_F + \frac{k_s}{k_{ox}} t_{ox} \sqrt{\frac{2qN_A\phi_F}{k_s\varepsilon_0}} \qquad 3.1$$

where ϕ_F is the semiconductor potential in the bulk due to doping k_s is the semiconductor dielectric constant, k_{ox} is the dielectric constant of the oxide, t_{ox} is the oxide thickness, N_A is the doping level in the bulk and ε_o is the permittivity of air.

Assuming that the interfacial charge density remains constant when going from the onset of depletion to the onset of inversion, V_T, can be estimated as 2.26 V using the following relationship:

$$V_T = V_T^{'} + V_{FB} \qquad 3.2$$

C-V measurements were done at 10 kHz, 100 kHz and 1 MHz on 100 um square capacitors and a difference of ~8% was observed. The leakage current density at 1V below the flat band voltage is $4.10x10^{-5}$ mA/cm^2 (Figure 18). The film became crystalline after 30 sec RTA in oxygen at 1050°C as apparent from XRD spectrum in Figure 19.

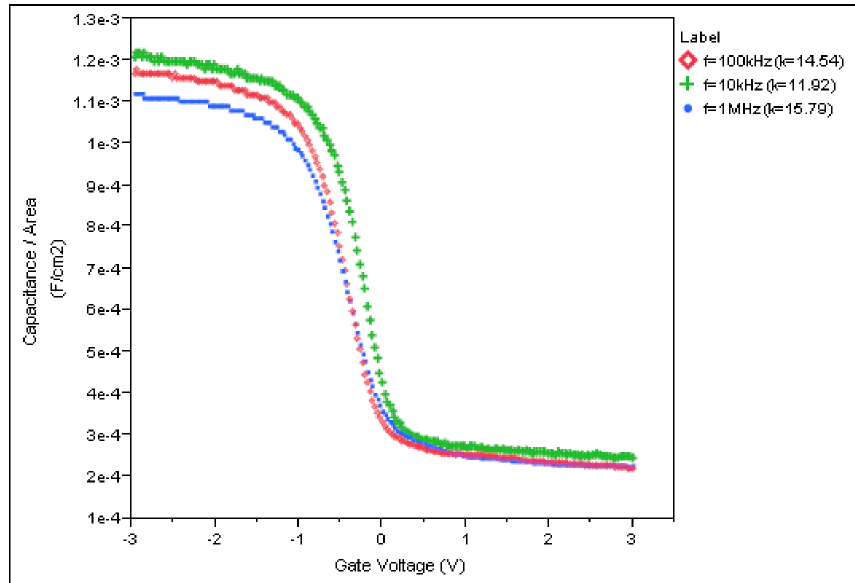

Figure 17. Capacitance per area vs. Gate Voltage for sample with composition $Sr_{0.10}Hf_{0.90}O_{2.7}$.

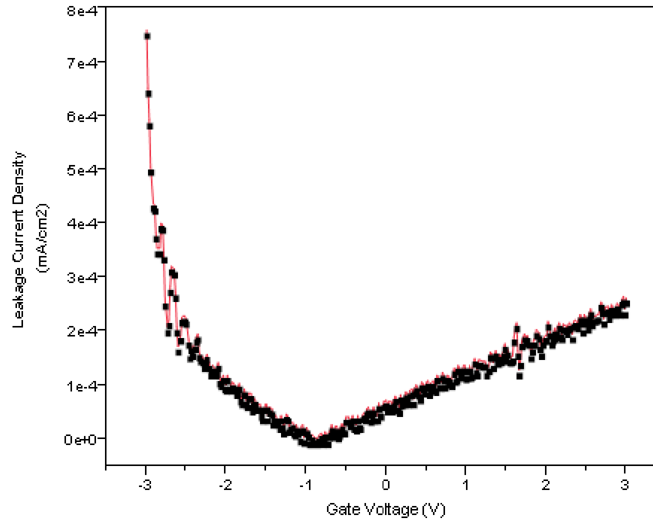

Figure 18. Leakage Current vs. Gate Voltage for sample with composition $Sr_{0.10}Hf_{0.90}O_{2.7}$.

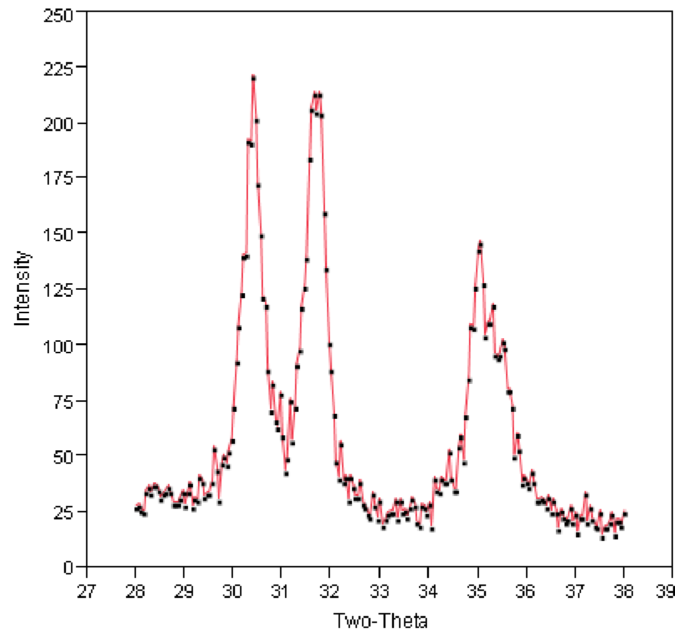

Figure 19. XRD spectrum of sample $Sr_{0.10}Hf_{0.90}O_{2.7}$.

Hf-rich film with Hf/(Hf+Sr) ratio of 0.83 annealed in oxygen at the temperature of only 450°C had a flat band voltage of 1.63V and EOT of 18.7nm (the physical thickness of the film was 62.4nm) and the interface charge density of - 1.40 x $10^{12}/cm^2$ obtained from -5 to +1 C-V sweep at 100kHz as calculated using CVC program (Figure 20). Threshold voltage, V_T', calculated based on the ideal n-channel device, Eqn14, was 0.93 V

Assuming constant interfacial charge density when going from the onset of depletion to the onset of inversion, V_T, was estimated to be 2.56 V. The film remained amorphous after 450°C oxygen anneal (Figure 22).

A difference of 5% was observed between C-V measurements done at 10 kHz,100 kHz and 1 MHz for strontium hafnate sample $Sr_{0.17}Hf_{0.83}O_{1.6}$ (Figure 20). The C-V curve was shifted further to the left compared to the samples with higher Hf/(Hf+Sr) ratio. This might be due to the higher concentration of positive fixed charge in the oxide. The leakage current density at 1V below the flat band voltage is $1.13x10^{-3}$ mA/cm^2, which is two orders of magnitude higher than that of the previously discussed Hf-rich sample. It has been reported that annealing has beneficial effects in reducing leakage current by as much as four orders of magnitude [25]. The inflection in the low frequency C-V curve (Figure 19) around 2V could also be due to the presence of the interface states (similar to $Hf_xTi_{1-x}O_2$ described in [27]). Furthermore, this sample also has a higher interface charge density and higher flat band voltage which is likely due to the fact that a lower annealing temperature was used. It has been reported that reducing oxidation temperature leads to an increase in fixed charge and interface state density.

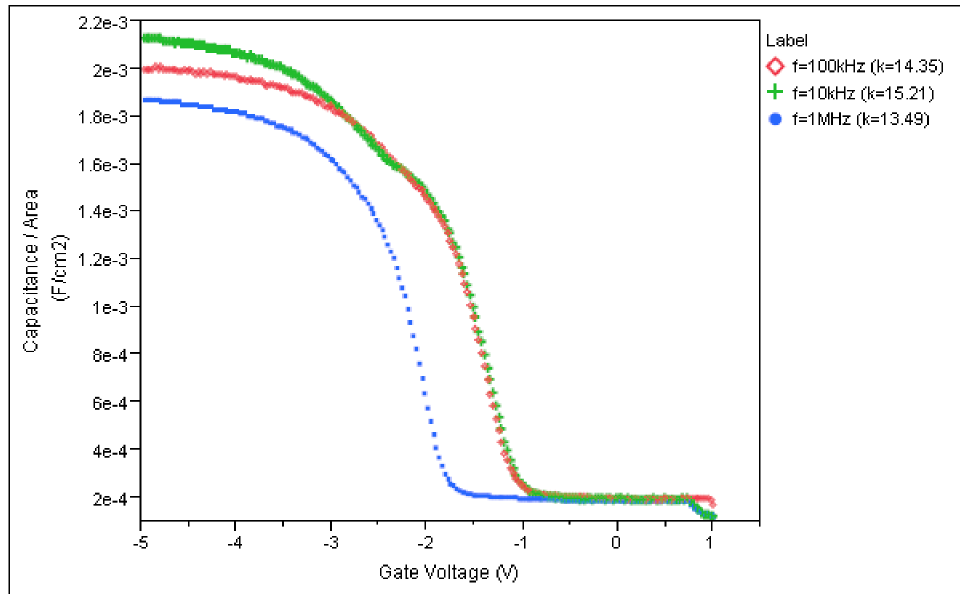

Figure 20. Capacitance per area vs. Gate Voltage for sample with composition $Sr_{0.17}Hf_{0.83}O_{1.8}$.

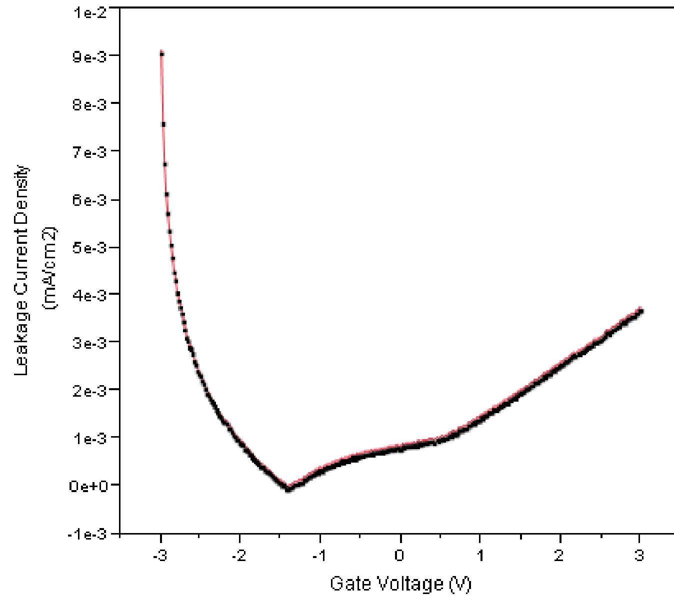

Figure 21. Leakage Current vs. Gate Voltage for sample with composition $Sr_{0.17}Hf_{0.83}O_{1.8}$.

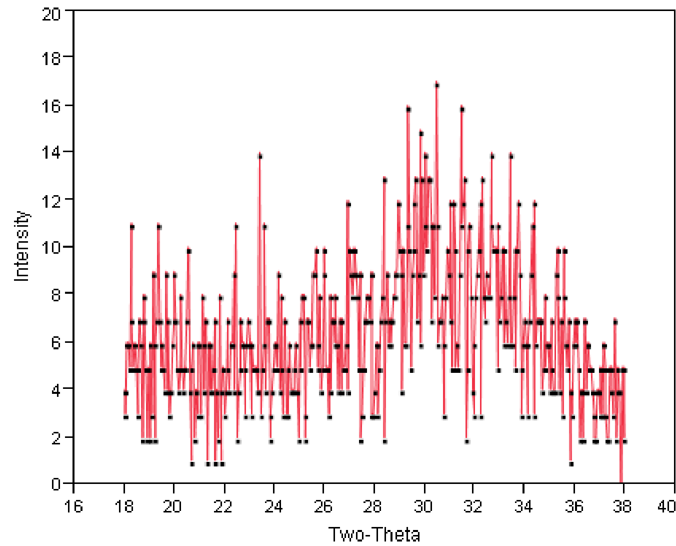

Figure 22. XRD spectrum of sample $Sr_{0.17}Hf_{0.83}O_{1.8}$.

Strontium hafnate films with low Hf composition had k of 35 and appeared amorphous even after annealing at temperatures of 1050 °C (Figure 22). Films with a Hf/(Hf+Sr) ratio of 0.15 annealed in oxygen at 30 sec at 600C and 30 sec at 700C had a flat band voltage of 1.26V and EOT of 7.88nm (the physical thickness of the film was 80nm) and interface charge density of $2.06\text{x}10^{12}/\text{cm}^2$ obtained from -2 to +2 C-V sweep at 1MHz as calculated using CVC program.

The threshold voltage, V_T', calculated based on the ideal n-channel device model was 1.59V and V_T was estimated to be 2.26 V. C-V measurements were done at 10 kHz, 100 kHz and 1 MHz and a difference of ~5% was observed. The leakage current density at 1V below the flat band voltage is 4.04 x 10^{-6} mA/cm^2 (Figure 24).

High interfacial charge density is likely related to the sputtering damage during oxide deposition. It was reported that the physical bombardment of energetic ions results in damage to the gate dielectric, generating interface and oxide trapped charges in the gate dielectrics during PVD [28].

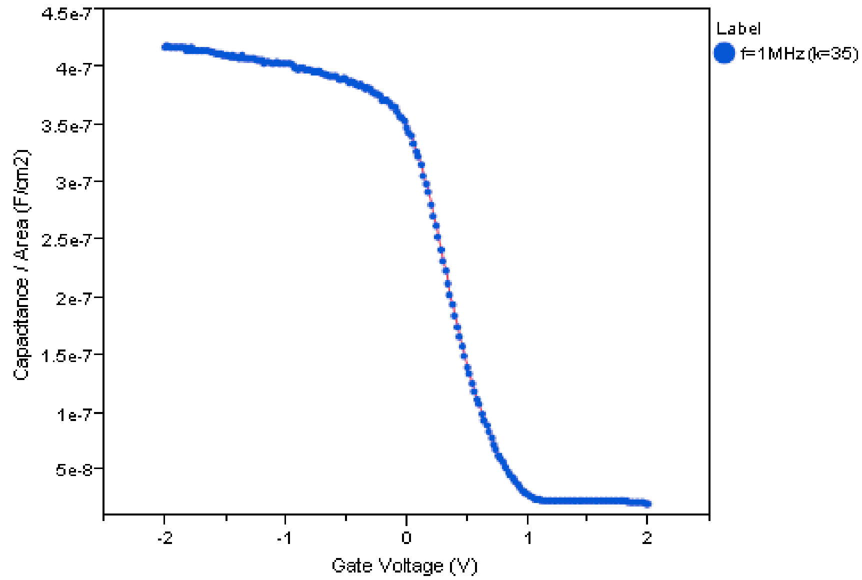

Figure 23. Capacitance per area vs. Gate Voltage for sample with composition $Sr_{0.85}Hf_{0.15}O_{1.9}$.

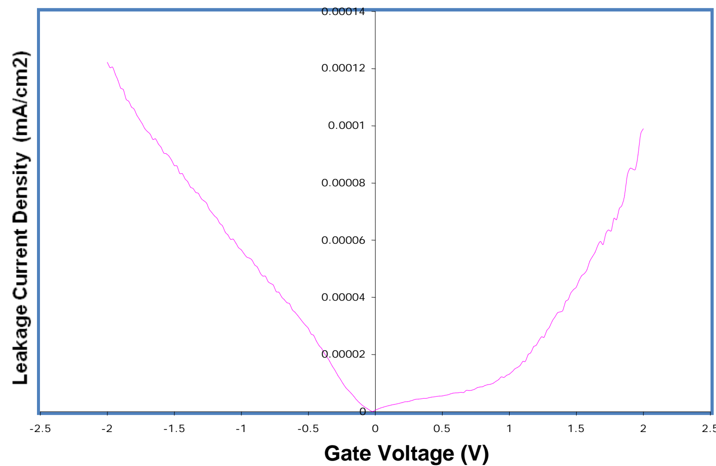

Figure 24. Leakage Current vs. Gate Voltage for sample with composition $Sr_{0.85}Hf_{0.15}O_{1.9}$.

High-k, low Hf composition, films were further annealed to examine changes in the crystalline structure at higher temperatures. XRD data indicated that the films remained amorphous even when annealed at 1000°C.

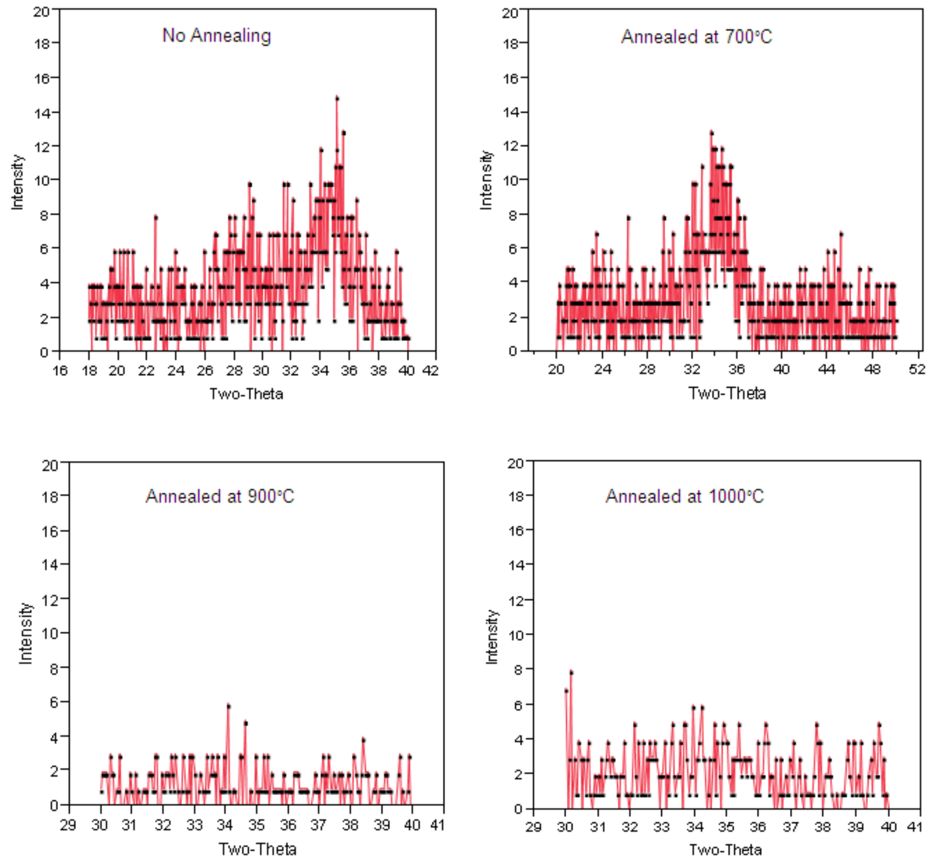

Figure 25. XRD spectra of sample $Sr_{0.85}Hf_{0.15}O_{1.9}$ as deposited, annealed at 700C, 900C and 1000°C.

However, a more detailed picture seen from the HRTEM (Figure 26) shows that two distinct layers are present in the film with Hf/(Hf+Sr) ratio of 0.15: a ~12 nm thick amorphous layer appears near the surface of the silicon and an upper layer containing nanocrystals with the size of only ~2nm is also evident.

HRTEM data for the annealed film is contradictory to the XRD results since it clearly shows nanocrystal growth in the upper portion of the film. It is likely that these nanocrystals were not detected by XRD because they did not produce large enough Bragg reflection due to their small

size. The interfacial layer is thicker than expected. High permittivity films deposited on silicon often form interfacial oxides which are typically a few nanometers thick. The surface of the silicon shows evidence of localized reactions, which might be due to the lack of oxygen in as-deposited films; as deposited films were oxygen deficient and post deposition annealing in O_2 was used to increase the oxygen concentration in the films [27].

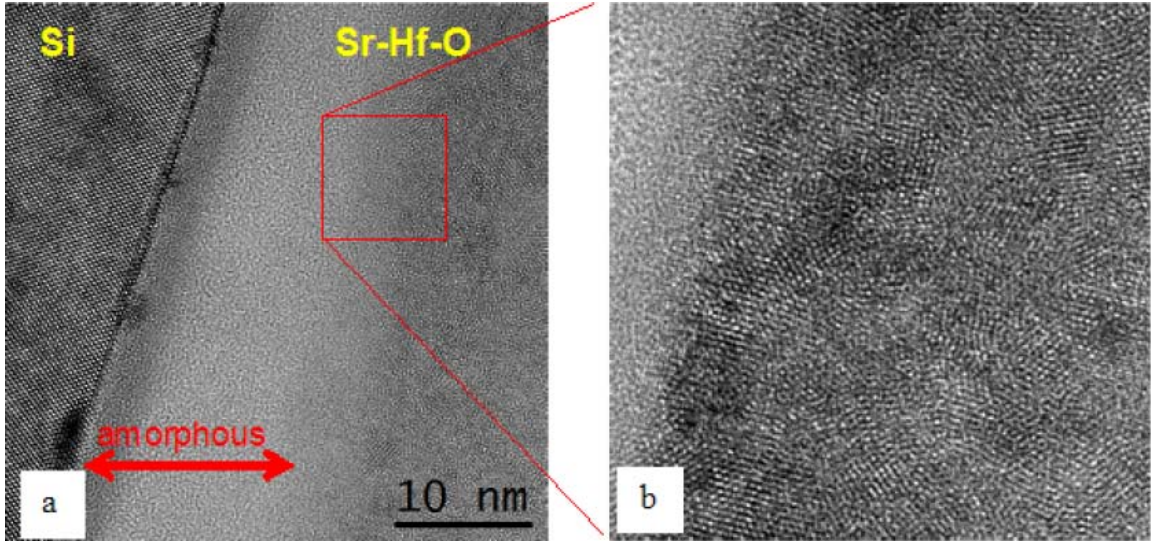

Figure 26. TEM images of sample with composition $Sr_{0.85}Hf_{0.15}O_{1.9}$.

Photoconductivity measurements were used to determine the bandgap width of Sr hafnate layers. 0.5mm^2 MOS capacitor samples were fabricated by depositing 80nm thick Strontium Hafnate film via PVD and then evaporating a 15 A thick, semitransparent layer of Au. The samples were exposed to a range of photon energies, $2<hv<6.8$ eV, and electrical conductivity was measured as the quantum yield, Y, which is defined as the photocurrent normalized by the incident photon flux while +1.5 V bias was applied to the metal electrode as shown in Figure 27. The band gap of the material was determined from the photoconductivity spectrum as described by Afanas'ev et al. [29], [30]. The curve exhibits several spectral thresholds: In the high-yield portion ($Y > 10^{-5}$), high efficiency of photocurrent excitation suggests transitions between high densities of filled and empty states which is typical for the intrinsic oxide PC. The spectral thresholds were evaluated by subtracting extrapolated contribution of the photocurrents with lower excitation thresholds from the measured signal, and then applying the $Y^{1/2}$-hv plot [29], [30]. The higher threshold was found to be at 5.7 ± 0.2 eV which is close to the bandgap of pure HfO_2. Therefore, this PC is likely due to excitation of electrons from derived states in the valence oxide band to the Hf-derived unoccupied states in the conduction band. The lower PC threshold observed at 4.4 ±0.1 eV may be explained by electron excitation to the conduction band states derived from Sr^{2+} cations. This

threshold is commonly not observed in pure HfO_2, which exhibits two thresholds, at 5.6 and 5.9 eV. Two lower thresholds were observed at 3.4± 0.1 and 2.6 ± 0.1 eV. As no detectable photocurrent in the spectral range hv<4 eV is observed in the capacitors with metal biased negatively, no electron excitations in the bulk of Sr hafnate could account for these transitions. At the same time, the absence of photocurrent modulation by increasing reflectivity of Si crystal at hv > 3.4 eV clearly seen in the case of Si/HfO_2 interfaces [29], suggests that internal photoemission of electrons from Si into the insulator is not the dominant mechanism of electron injection into Sr hafnate. It is possible, that the corresponding optical excitation is caused by imperfections in the relatively thick interlayer between Si and Sr hafnate revealed by TEM [27].

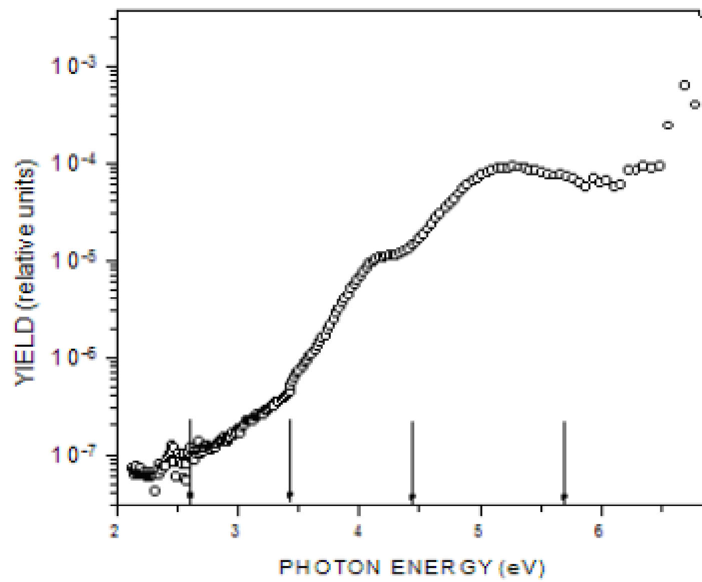

Figure 27. PC spectrum of sample with composition $Sr_{0.85}Hf_{0.15}O_{1.9}$.

Chapter 4 - Summary and Conclusions

Strontium hafnate films deposited by physical vapor deposition were characterized by RBS, XRD, TEM, and through electrical analysis. Strontium rich films appeared amorphous according to XRD even after a 1000°C anneal; however, high resolution TEM showed ~2nm size crystals in portions of the annealed films. The film permittivity for both as-deposited and annealed films was ~35.

Capacitance-voltage measurements were performed on MOS capacitors with Cr gates (the devices were biased under accumulation). No attempt was made to compensate for the presence of an interfacial layer. It was found that the permittivity derived from the C-V measurements was a function of film composition. Hf-rich films had a permittivity of about 15, which was in agreement with permittivity of HfO_2. Sr-rich films had a permittivity of 35 +2/-1, which is also in good agreement with theoretical predictions. It is possible that the permittivity of the film is not uniform (i.e. the bulk of the film might have different permittivity than the Si and Cr interfaces); however, both as-deposited and annealed films had comparable permittivity and XRD and TEM data showed that as-deposited films had no crystal structure. So, it is not clear how the overall high-k stack permittivity would remain the same if the permittivity through the annealed film was more non-uniform than that of the as-deposited film [27].

Thermodynamic stability of the high-k films can be further improved by introducing an interfacial layer of nitride or oxynitride. Nitrogen serves as an oxygen barrier and as such it can be used to control the thickness of the intermediate layer (between Si and high-k dielectric), which determines the overall capacitance and dielectric constant of the high-k material; however, given that this intermediate has a lower dielectric constant than the high-k material, this would result in reduced overall dielectric constant. The presence of nitrogen can also limit the mobility of Hf and Sr and their penetration into the Si. Therefore, nitridation of the intermediate layer has the potential of improving the electrical performance and stability of the high-k material during further thermal processing steps.

Further studies of Sr-rich films are recommended. Sr rich films with Sr mole fraction >0.85 may have dielectric constant >35 and might remain amorphous at higher annealing temperatures. The impact of oxygen annealing should be further characterized both in terms of crystallization temperature for varying film compositions as well as interfacial layer composition and oxygen diffusion through the high-k material. It was reported that HfO_2 samples pre-annealed in Ar at 1000°C prior to 800°C O_2 anneal exhibited higher resistance to O and Si migration [31]. Thus, inserting an Ar annealing step prior to O_2 anneal should also be explored.

Permittivity and crystallization temperature as a function of film thickness should also be examined. Depth profiles of Sr, Hf, O on as-deposited as well as on the annealed films might vary depending on the film thickness as seen on hafnium silicate films [37].

Finally, CVD precursors should be identified for strontium hafnate deposition in order to reduce oxide charge density and interfacial trap density induced by the ion beam during PVD. PVD was initially chosen for this research because the targets were manufacturable (unlike CVD for which the precursors have not been identified) and it was used to assess whether strontium hafnate films would be suitable as high-k dielectrics. The results obtained from PVD films indicate that these materials should be studied further and it would likely be advantageous to develop a CVD process in order to improve film quality.

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