FAST HOPPING FREQUENCY SYNTHESIS TECHNIQUES USING INJECTION LOCKING

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Abstract

The use of fast-hopping frequency synthesis is a critical component of frequency-hopped spread spectrum (FHSS) systems. FHSS offers many advantages including high resistance to narrow-band interference, low probability of intercept and capability to share spectrum with other narrow-band systems. Such qualities make FHSS a particularly attractive scheme for military applications. In commercial applications, the WiMedia specification for ultra-wideband (UWB)/Wireless-USB presents another standard that uses fast frequency-hopping. The most stringent constraint on the frequency synthesizer in these systems is the band-switching time.

This thesis presents novel techniques for fast-hopping frequency synthesis based on injection locking. First, extensive study of the transient behavior of oscillators under injection is presented. Analystical expressions are used as the basis for the study and interesting aspects of the locking process of an injection-locked oscillator (ILO) are identified. Two techniques, lock-range dependent fast-locking and predictive fast-locking, are then presented. In the first technique, fast locking times are achieved by using large lock-ranges for the ILO. Phase dependence of lock-time is exploited in the second technique and extremely fast settling is achieved. These theoretical findings are verified through simulation and measurements from a multiple of oscillator prototypes. Measurements from a low-speed Colpitts oscillator running at 57 MHz are used to verify tracking, out-of-lock behavior and frequency settling of ILOs. Measurements from an LC-oscillator implemented in 0.13-μm CMOS technology operating at a free-running frequency of 3.4 GHz are used to verify the dependence of locking time on the lock range and the initial phase of injection. Novel architectures for fast frequency-hopping synthesizers and high frequency direct-digital synthesizer are then presented.

Finally, a complete prototype for WiMedia-UWB/Wireless-USB-compliant fast-hopping frequency synthesizer architecture with quadrature outputs, based on sub-

harmonic injection-locking, is presented. The synthesizer features a cross-coupled quadrature digitally-controlled oscillator, that is injection-locked to a sub-harmonic frequency. An intuitive closed-form expression for the dynamics of the quadrature injection-locked oscillator is derived. The overall design is a CMOS-only implementation and has been fabricated in 0.13-μm SiGe BiCMOS process. Measurement results indicate lock-times of less than 2.5 ns, a locked phase noise of -114 dBc/Hz at 1 MHz offset and a quadrature accuracy of better than 0.5°. The frequency synthesizer (excluding output buffers) occupies an area of 0.27 mm^2 and consumes 14.5 mW of power. The best and worst-case spur suppression achieved are 47 and 31 dB, respectively. This is the lowest power fast-hopping quadrature frequency synthesizer reported to-date.

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Chapter 1

Introduction

The explosion of wireless technology in the past few decades has greatly impacted our society, changing the way we communicate with each other, access information and transfer data. There is an increasing demand for wireless connectivity in the present day. Almost every one has a mobile phone, more and more computers use Wireless Local Area Networks (WLAN) and wireless home networks are ubiquitous. Though the current wireless technology is mainly seen in the commercial applications, the radio has its origin in the military. The development of radio has been long and non-linear [3]. The first useful two-way wireless communication was developed by Marconi in the early 1900's.

The two World Wars in the first half of the twentieth century further spurred the development of wireless, particularly in the area of communication, detection & surveillance. Significant research into electromagnetic waves, antennas, microwave circuits and communication schemes were done by the military. RADARs, short for RAdio Detection And Ranging, were born in this period. Also, the possibility of the enemy intercepting wireless communication between allies, resulted in techniques like jamming and robust encoding schemes and triggered advancements in cryptography, some of which are used

even today. Cryptography was used to hide the intended message. A popular example of this is the Enigma machine that was used by German military during WWII.

Encoding schemes such as spread-spectrum techniques, hide the wireless signal under ambient noise. Only the designated user can detect the signal. Since an eavesdropper cannot decode the signal, it becomes exceedingly difficult to jam the communication link. Spread-spectrum techniques spread the energy of the narrow-band communication signal over a wide band, reducing the amplitude significantly, such that it is close to or below the noise floor. In the 1970's and 80's, the Federal Communications Commission (FCC) declassified a lot of information and research done on spread-spectrum communication by the military. Today, we find spread-spectrum techniques in almost all commercial wireless communication systems - Bluetooth, CDMA-based cellular phones, WiFi, etc.

Personal wireless communication devices have seen unprecedented growth in the last decade. In the early 1990s, cellular phone was considered a luxury for few. Today, cellular phones are used by farmers in third-world nations. Also, the newer models can perform many more functions, integrate more technologies (Bluetooth, GPS, WiFi) and perform more efficiently than their older counterparts. The credit for such growth in wireless devices goes to silicon technology. Driven by Moore's Law, silicon technology has been consistently evolving - resulting in smaller feature sizes, operating at higher frequencies, allowing larger integration and eventually driving down costs.

Traditional military radio/wireless systems consisted of discrete active/passive components and circuit block-level monolithic microwave integrated circuits (MMICs). Even the early commercial/civilian wireless systems adopted a similar design approach. However, the cost, design effort and reproducibility advantages of system-level integration in silicon were soon clear. This resulted in increasing levels of RF/analog system integration culminating in the concept of System-on-Chip (SoC). Another advantage of silicon (specifically CMOS) technology that drove this growth was the possibility of extensive digital signal processing (DSP), which is key to many wireless system architectures.

Traditionally, bipolar-junction transistors (BJTs) offered better RF/analog performance while CMOS was more power-efficient for digital operations. However, the rapid improvements in feature sizes and performance of CMOS technology, thanks to the microprocessor and memory industry, resulted in CMOS closing the gap in terms of analog/RF performance. Silicon-germanium (SiGe) based BiCMOS process offer both BJTs and CMOS transistor, but the small price overhead has resulted in BiCMOS holding only a minor share in the SoC market. One area where BiCMOS technology is still preferred over CMOS, when considering silicon-based technologies, is in power-amplifiers.

Present-day low to medium data rate communication standards like Bluetooth, GSM, CDMA, 802.11g/n, etc. have driven the personal wireless communication era. They rely on complex coding and digital signal processing techniques to attain high signal-to-noise ratio (SNR) over their limited bandwidths, also guaranteeing the required throughput by Shannon's theorem [4]. Lower costs, integration capability and pervasive DSP capabilities allowed CMOS to be the technology of choice for wireless SoC integration. Future wireless communication systems are aimed at attaining communication data rates in the Gigabit-per-second (Gbps) regime over a short range ($<$ 10m). Wireless applications requiring such high data-rates are 60-GHz Wireless Personal-Area-Network (WPAN)/Wireless HDMI [5] and Wireless-USB [6]. These applications operate over significantly large bands (ultra-wideband or UWB) and hence, by Shannon's capacity theorem [4] can support Gbps data rates.

There are numerous examples in recent literature of millimeter-wave and/or UWB circuits and systems integrated in sub-micron CMOS technologies. This thesis focuses on the frequency synthesizer section of the UWB systems. Specific emphasis is given to low-power design and fast-hopping capabilities of frequency synthesizers. In order to achieve both these goals, we propose new schemes based on a phenomenon called injection-locking.

1.1 Organization

The main objective of this dissertation is to study fast-hopping frequency synthesis techniques in CMOS technology and present architectures and techniques to improve their performance in terms of power consumption, hopping-time, etc. The performance of the techniques developed in this dissertation are tested against the stringent WiMedia-UWB/Wireless-USB standard. But the architecture and techniques developed here are general and can be easily extended to any application where extremely fast-hopping frequency synthesizers are required.

In Chapter 2, a background of frequency synthesizers is presented in the context of radio transceivers. A brief understanding of oscillators and phased-locked loops (PLLs) is provided. The settling behavior of PLLs based on a second-order loop transfer function is examined.

In Chapter 3, a clear understanding of injection-locked oscillators (ILOs) is presented. Several mathematical models governing the dynamics of an ILO are provided. These models describe both the within-lock and out-of-lock behavior of ILOs in the time-domain. Direct theoretical estimation of sidebands in unlocked oscillators is then presented. Finally a wide range of applications that currently use different characteristics of ILOs are presented.

Chapter 4 presents an extensive study of the transient behavior of oscillators under injection. Adler's equation is used as the basis of the study and some interesting and insightful aspects of the locking process of an ILO are derived. The trajectory of phase and frequency settling are theoretically established and their dependence on parameters like lock-range and initial phase of injection are identified. The behavior of the ILO when the injection is outside the lock range is then presented.

Fast-hopping frequency synthesis techniques are investigated in Chapter 5. Existing architectures for frequency synthesizers that meet the WiMedia-UWB specification are

reviewed. Two techniques based on injection locking, lock-range dependent fast-locking and predictive fast-locking, are then presented. ILOs behave as first-order PLLs and their bandwidth can be made very large without suffering from stability issues. This fact is used in the first technique and the required lock range for a specific lock-time constraint are estimated. However, achieving large lock ranges is not always possible. The second technique addresses this issue by exploiting the phase dependence of lock time in ILOs. Two architectures, one for frequency synthesis meeting Wimedia UWB specification and the second to extend the frequency of operation of a direct digital synthesizer, are presented.

Chapter 6 validates the theoretical understanding of ILOs developed in the thesis through measurement and simulation. A low-frequency discrete Colpitts oscillator is used to show time-domain lock acquisition, tracking and beat behavior. Transient measurement results from a high-frequency LC-oscillator show the fast-locking capabilities of the ILOs. Finally, simulation results based on fundamental and harmonic frequency-shift keying (FSK) of an LC-oscillator prove the predictive locking capability of the ILOs. This also validates the architecture for the frequency extension of direct-digital synthesis.

Chapters 7 and 8 present quadrature signal generation techniques and present a prototype design for fast-hopping quadrature frequency synthesizer. Chapter 7 discusses the theory of quadrature voltage-controlled oscillator (QVCO) from an injection-locking perspective is presented. Closed-form expressions governing the behavior of an injection-locked quadrature VCO are then derived based on the same procedure used to develop Adler's equation. Based on this understanding a complete architecture for a fast-hopping frequency synthesizer in presented in Chapter 8. The quadrature synthesizer hops across the first band-group frequencies of the WiMedia-UWB specification. Measurement results show that the system achieves excellent quadrature accuracy and spur suppression. It is the lowest power WiMedia-UWB/Wireless-USB-compliant quadrature synthesizer reported to-date. Finally, Chapter 9 provides some remarks on the comparison between

PLLs and ILOs and concludes with a summary of this work.

Chapter 2

Background

A transceiver is the combination of a transmitter and a receiver found in any communication equipment such as mobile phones, hand-held two-way radios, etc. A block diagram of a typical wireless transceiver is shown in Fig. 2.1. The signal picked up by the antenna is amplified by the low noise amplifier (LNA) while adding minimal noise to the signal. The amplified signal is down-converted using a mixer by multiplying it with a local oscillator (LO) signal. The LO signal is generated by a voltage-controlled oscillator (VCO) embedded in a phase-locked loop (PLL). A constant LO signal is maintained by the PLL by comparing the VCO output with a steady reference from a crystal whose output is at a lower, more available frequency. The PLL is one of the most power-hungry blocks due to the large power consumption in the frequency dividers used in the feedback path. This thesis looks at the problem of the reduction of power consumption of the VCO-PLL block by using non-conventional techniques of generating the LO signal.

2.1 Radio Architectures

For a complete on-chip implementation, usually a homodyne or low-IF based architecture is selected where the RF signal is down-converted to DC or a near-DC intermediate

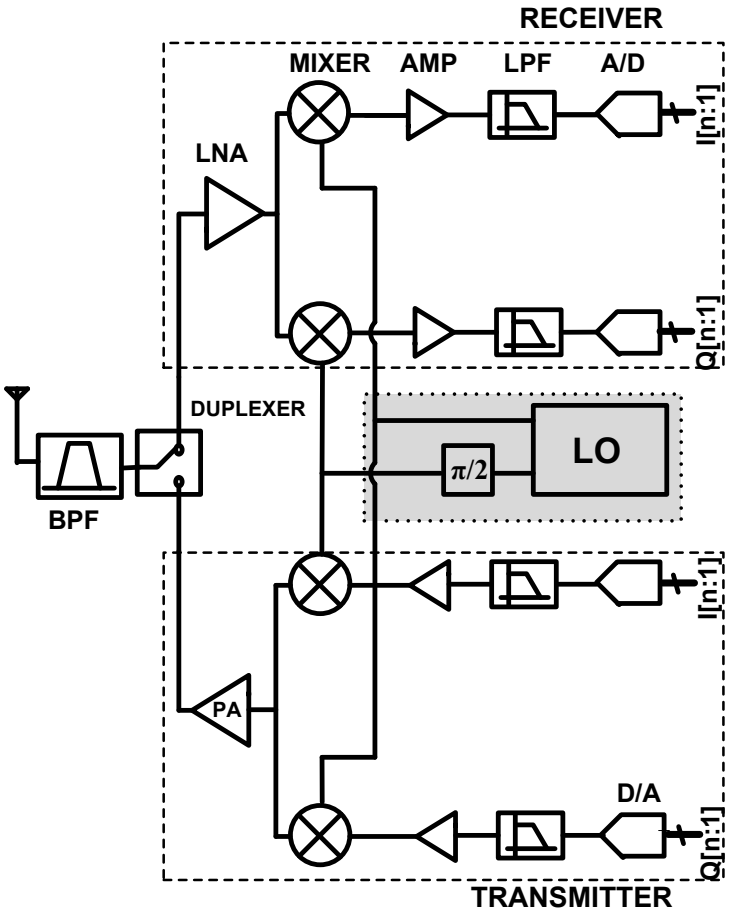


Figure 2.1: An example radio transceiver architecture

frequency (IF). In a direct conversion based architecture, the signal is its own image. This is good if both the side bands of the signal are up-converted and transmitted. But to conserve bandwidth, most of the current standards only transmit a single side band of the signal by employing a quadrature based up-conversion mixer. Hence quadrature mixing is needed to down-convert and recover the signal. The accuracy with which the LO signal and its quadrature are generated will determine the accuracy of image rejection. The unconventional LO generation technique, proposed in this work, has also been extended to generate the quadrature signals.

The transmitter performs a function inverse of that of the receiver where the base-

band signal is up-converted to a higher frequency and transmitted. The mixer in the transmitter performs the up-conversion and the power amplifier (PA) amplifies the signal and drives it into the antenna. The LO signal generator is the common block that is shared by both the receiver and transmitter and is on while transmitting or receiving. Therefore, any power saving will have a significant impact in the entire transceiver.

2.2 Frequency Synthesis

As discussed, frequency synthesizers form one of the most critical elements in the transceiver. Apart from its use in down-conversion of the incoming radio-frequency (RF) signal to an IF (intermediate frequency) using a mixer, frequency synthesizers also find use in clock generation for digital applications. Frequency synthesis, therefore, forms the backbone for the digital, front-end and back-end of any transceiver.

Frequency synthesis is most commonly realized by using a PLL. For most applications, any random fluctuation in the output phase of the frequency synthesizer is undesirable. Also, in order to cover a wide range of frequencies for down-conversion, the tuning range is critical. Within the PLL, which we will discuss in more detail later, the most important block is the VCO. As the name suggests, the output frequency of a VCO is dependent on an input voltage signal through an approximately linear transfer function with slope K_{VCO}, as shown in eqn. 2.1.

$$f = f_{fr} + K_{VCO}V_{ctrl} \tag{2.1}$$

where f_{fr} is the free-running VCO frequency and V_{ctrl} is the control voltage input to the VCO.

2.2.1 Oscillators

An oscillator functions on the principle of $2N\pi(N = 0, 1, 2...)$ overall phase around a feedback loop with a gain greater than unity at a particular frequency (Barkhausen's

criteria). As a result, any noise at that frequency (frequency of oscillation, say ω_0) is amplified through a positive feedback mechanism until the non-linearities in the system limit it to a particular amplitude (amplitude of oscillation, say A). In this thesis, we will discuss two main categories of VCOs used within PLLs: ring oscillators and LC oscillators. While in a ring oscillator, a net phase of 360 degrees is obtained around the loop through the use of inverters or inverting amplifiers connected in a ring, in an LC oscillator, the net phase is 0 degrees at the resonance frequency of an inductor-capacitor (LC) tank.

Ring oscillators

Ring oscillators are constructed by connecting a series of inverter/amplifier blocks in series with the output of the last block connected to the input of the first. The inverters/amplifiers thus form a ring as shown in Fig. 2.2, justifying the nomenclature.

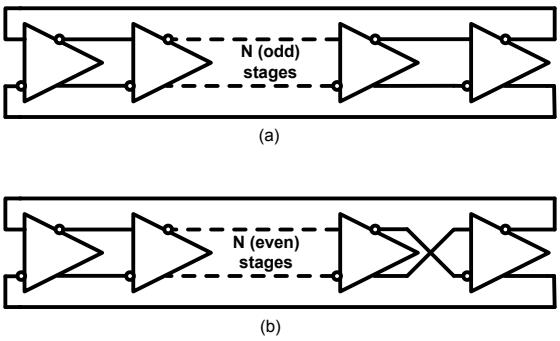


Figure 2.2: Construction of ring oscillators

The inverters/amplifiers are connected so as to provide a 180 degree phase shift at all frequencies as shown in Fig. 2.2. As shown in the Fig. 2.2(b), if an even number of stages are used, then one of them in a differential chain is flipped. Additionally, at some frequency ω_0, the additional frequency-dependent phase from each stage adds up to 180 degrees, thus providing a net 360 degrees phase shift around the entire loop. If the overall gain at this frequency, ω_0 is greater than unity, then the positive feedback

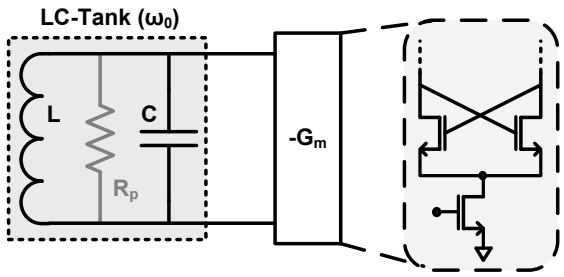


Figure 2.3: Conceptual construction of an LC oscillator

causes the circuit to oscillate at this frequency.

Ring oscillators have the advantage of being fully compatible with standard digital CMOS technology. The on-chip area consumption is small and relatively large tuning ranges can be achieved. However, the phase noise of these oscillators is traditionally poorer than that obtained in LC oscillators.

LC-oscillators

LC-oscillators function on the principle that an inductor (L) and a capacitor (C) connected in parallel offer an infinite impedance and zero phase shift at the frequency of resonance. However, a real LC-tank, due to its non-idealities, provides a finite real impedance at the resonance frequency. Therefore, in order for the oscillator to sustain oscillations at the resonance frequency, a parallel negative resistance needs to be connected to cancel out the loss in the tank, and provide a net loop gain for the oscillator to start up. The negative resistance is usually realized using appropriately connected active devices as shown in Fig. 2.3. Depending on the configuration in which transistors are connected, different kinds of oscillators can be constructed.

On-chip inductors and high performance capacitors often need special processes and are not readily available in vanilla digital CMOS technologies. Also, they consume a large area, especially for lower frequencies of operation. However, due to the higher quality factor (Q) of the LC-tank, LC-oscillators offer a relatively improved phase noise

performance.

Phase noise

Any random fluctuations in the output phase of a synthesized frequency is characterized using a metric known as phase noise. Phase noise is defined in the frequency domain as a function of the offset frequency from the frequency of the generated carrier. The magnitude of the power spectral density (PSD) of the generated frequency at the given frequency offset is compared to the carrier power to give what is known as the single side-band (SSB) phase noise. The mathematical definition is shown in eqn. 2.2.

$$L(\Delta\omega) = \frac{S(\omega_0 + \Delta\omega)}{\int_{-\infty}^{\infty} S(\omega) d\omega} \qquad (\Delta\omega > 0) \tag{2.2}$$

The spectrum of the oscillator as a function of the offset frequency is shown in Fig. 2.4. As shown in the figure, there are three distinct regions. The $\frac{1}{f^2}$ region is formed by the shaped thermal noise from different devices by the oscillator frequency domain response. The $\frac{1}{f^3}$ region is a manifestation of the up-converted flicker noise from the active devices and is seen close to the carrier frequency. At offset frequencies far from the center frequency, ω_0, white thermal noise of the devices dominate. Oscillator phase noise analysis has been traditionally challenging. In this thesis, we will discuss two main phase noise models popularly used for analysis.

Leeson's model: In 1966, D. B. Leeson presented a heuristic model of the oscillator spectrum in terms of the power, quality factor, absolute temperature, frequency, and frequency offset [7]. Although the model made intuitive sense, he did not provide any proof for the model.

One way to approximately derive Leeson's model would be to use the oscillator's frequency domain response to effectively shape the noise generated by the devices [8]. The result of such an analysis is given in eqn. 2.3.

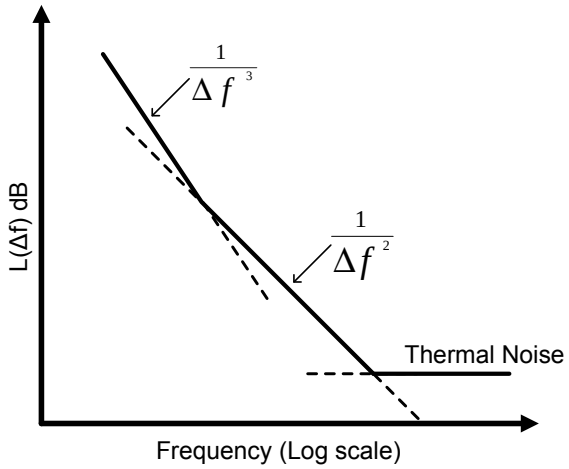


Figure 2.4: An example diagrammatic phase noise spectrum

$$L(\Delta\omega) = \frac{2FkT}{P_s}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{2.3}$$

Here, F is called the excess noise factor used by Leeson to model the excess noise from the active devices.

Despite the intuitive nature and simplicity of Leeson's model, it suffers from some limitations. The excess factor, F, cannot be calculated without using measurement data to fit the model. Additionally, the $\frac{1}{(\Delta f)^3}$ region should coincide with the flicker noise corner according to Leeson's model. However, in reality, this is not necessarily the case [9].

Hajimiri's model: In 1998, A. Hajimiri and T. Lee introduced the impulse sensitivity function (ISF), symbolized as Γ to capture the cyclostationary nature of the impact of device noise on phase noise [9]. An intuitive explanation for the cyclostationarity can be understood as follows: If a noise current impulse affects the circuit during the oscillator's zero crossing, all the noise is converted into a phase disturbance. On the contrary, if a noise current impulse affects the circuit at its peak output voltage, all the noise gets

converted into amplitude noise and the phase is not affected. Based on this the ISF is computed for each time instant, τ, within a time period. The ISF can then be expanded in a Fourier series given by:

$$\Gamma(\omega_0) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \tag{2.4}$$

where c_n represents the amount of noise contributed around the frequency $n\omega_0$ where $n = 0, 1, 2, \ldots$.

The phase noise expression in the single sideband case can then be derived as

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2} \tag{2.5}$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the circuit thermal noise and q_{max} is the maximum charge displacement across the capacitor on that node.

Razavi's model: As was discussed, on-chip inductors require a special process adding to the implementation cost. Also, inductors consume a large chip area, and provide limited tuning range. Therefore, ring oscillators have become very popular for frequency synthesis in monolithic CMOS designs. However, since Leeson's model is based on the Q of the resonator tank, ring oscillators could not be analyzed in a similar fashion. In 1996, B. Razavi proposed a definition of inductorless VCOs that could be used in Leeson's equation to predict their phase noise [10]. The theory can thus be used to mathematically describe the phase noise of ring oscillators as given in eqn. 2.6

$$Q = \frac{\omega_0}{2} \sqrt{(\frac{dA}{d\omega})^2 + (\frac{d\phi}{d\omega})^2} \tag{2.6}$$

where A and ϕ are the gain and the phase of the open-loop transfer function shown in Fig. 2.5.

The definition captures the sensitivity of the open-loop transfer function to circuit parameter variations. A larger Q, therefore, ensures a larger phase deviation with slight

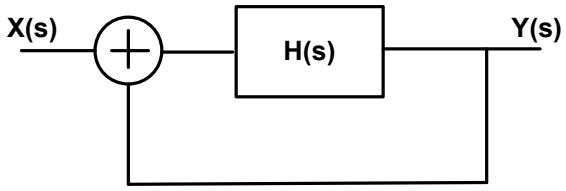


Figure 2.5: Linear model of an oscillator

perturbations, and consequently, a larger feedback bringing the oscillation frequency back to ω_0. This definition also holds for LC-oscillators, and therefore, can be used as a general definition of Q. However, please note that for ring oscillators the Q factor does not describe the ratio of active energy to energy loss per cycle.

2.2.2 Phase-Locked Loops

Phase-locked loops or PLLs are popularly used for frequency synthesis and use a reference frequency to generate a locked output frequency. A VCO as a stand-alone frequency synthesizer suffers from problems of frequency drift and degraded phase noise. In a PLL, negative feedback is used to eliminate these problems and synthesize a pure frequency tone. Fig. 2.6 shows the basic block diagram of a PLL. A PLL comprises three critical

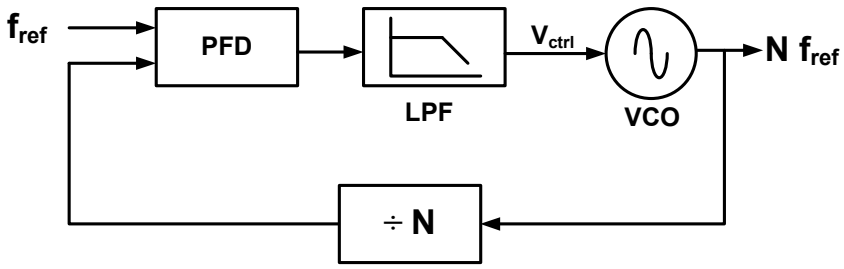


Figure 2.6: PLL block diagram

blocks: a phase detector, a low-pass filter and a VCO. The phase detector compares the phases of the reference signal and the VCO output and generates a voltage proportional to their difference. This voltage is low-pass filtered to eliminate any ripple and is provided

as a control voltage (V_{ctrl}) to the VCO. The VCO then produces an output frequency proportional to the control voltage. In the case there is a phase mismatch at the input, the frequency of the VCO is altered in a direction that reduces this phase error. When a steady-state is reached, the average frequencies of the input reference and VCO are exactly equal, and depending on the DC gain, a finite phase error may remain to maintain the VCO at the altered frequency. In case of frequency multiplication, a (programmable) divider is included in the loop. This imposes that $f_{ref} = \frac{f_{out}}{N}$ where N is the divide ratio. In low frequency PLLs, the dividers are usually implemented as digital counters but as the frequency of operation increases, current mode logic (CML) implementation becomes necessary.

In integer-N PLLs the output frequency can be changed in the steps of f_{ref}. If small frequency steps are required, the reference frequency should be made really small. This heavily constrains the loop bandwidth as it is chosen to be a fraction of f_{ref} because of stability and reference spur suppression considerations. Narrow loop bandwidths result in long acquisition and settling times. In applications where very small frequency steps are required, a fractional-N divider is often used.

Linear model for PLL

PLL systems are inherently nonlinear. However, in steady state, when the loop is locked and the phase error between the input and the output is small, the PLL can be modeled linearly as shown in Fig. 2.7. In this model, the input and output variables are phases instead of voltages or currents.

The input to the linearized system is the phase of the reference frequency. The PD generates a voltage directly proportional to this difference phase, given by

$$V_{PD} = K_{PD}\Delta\phi \tag{2.7}$$

where K_{PD} is the PFD gain and $\Delta\phi$ is the input phase difference. The loop-filter is

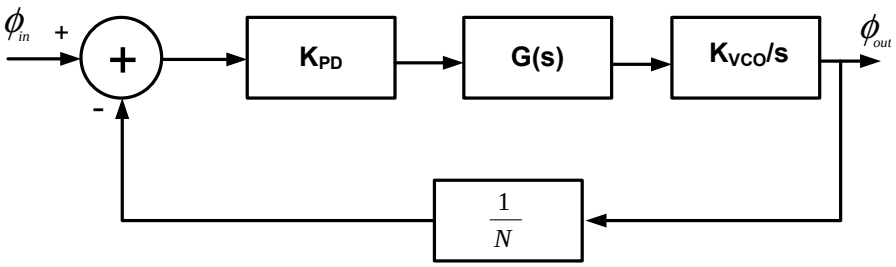


Figure 2.7: A linearized model for the PLL

represented by the transfer function $G(s)$. Since phase is the integral of frequency, the transfer function from the input of VCO (V_{ctrl}) to output (ϕ_{out}) is that of an integrator as shown by the transfer function in eqn. 2.8.

$$\phi_{out} = \frac{K_{VCO}}{s} V_{ctrl} \tag{2.8}$$

The closed-loop transfer function of the PLL is then given by equation

$$H(s) = \frac{K_{PD} K_{VCO} G(s)}{s + \frac{K_{PD} K_{VCO} G(s)}{N}} \tag{2.9}$$

Type and order of a PLL: The order of the polynomial in the denominator of the closed-loop transfer function (eqn. 2.9) is called the order of the PLL. In the case of eqn. 2.9, the loop-filter order determines the overall order. On the other hand, the number of integrators in the loop is called the type of the PLL. Since the VCO acts as an integrator, a PLL is at least of Type-I. If the loop-filter contributes additional integrators, the type of the PLL increases. The most common PLLs are Type-II. A popular example is charge-pump-based PLL (CPPLL). The order of a PLL is always greater then the type of the PLL i.e, a Type-II PLL is at least second order.

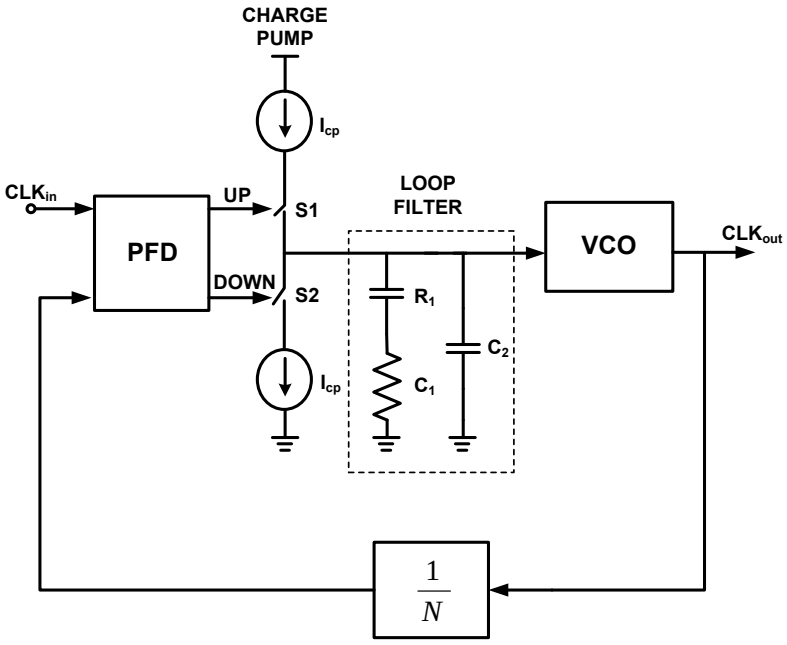


Figure 2.8: Charge pump PLL

Charge-pump PLL

The most popular implementation of a modern day PLL uses a charge pump as shown in Fig. 2.8. It consists of a charge pump that is designed to deliver or remove charge from the loop filter under the control of the phase frequency detector (PFD) discussed below. The PFD outputs turn the switches $S1$ and $S2$ on and off, controlling the up and down currents that accumulate charge onto the capacitor.

Phase/frequency detector: Traditional PDs suffer from a small linear (and even monotonic) range and more seriously, harmonic locking. Alternatively, a phase/frequency detector (PFD) can be used. A PFD is a sequential circuit that can discriminate between both frequency and phase between its two inputs. A particular implementation of PFD is shown in Fig. 2.9. If the frequency at input A (ω_A) if greater than that at B (ω_B), then Q_A produces positive pulses while Q_B remains zero. If $\omega_A = \omega_B$ then depending on the phase difference between A and B either Q_A or Q_B produces

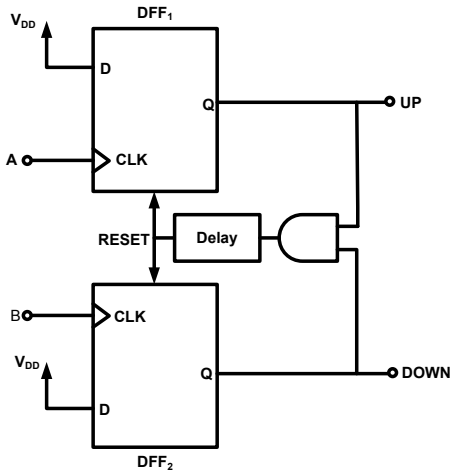


Figure 2.9: An example phase frequency detector circuit

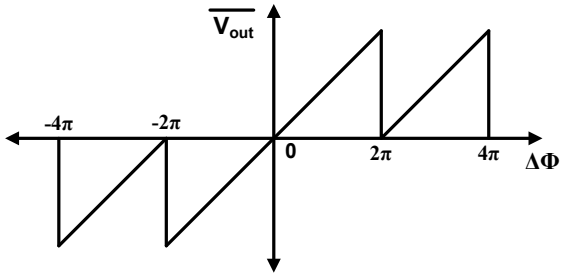


Figure 2.10: PFD transfer characteristics

positive pulses. Ideally the two outputs are not high simultaneously. This is the distinction between the PFD and XOR or latch-based phase detectors which always produce complementary outputs. The delay elements shown in Fig. 2.9 are used to mitigate the effects of dead-zone which reduces the loop gain when the phase error is very small. The transfer characteristics of the PFD discussed are shown in Fig. 2.10.

For the CPPLL shown in Fig. 2.8, the individual transfer functions can be expressed as follows:

$$K_{PD} = \frac{I_{CP}}{2\pi} \tag{2.10}$$

$$G(s) = \frac{1 + sRC_1}{s(C_1 + C_2 + sRC_1C_2} \tag{2.11}$$

$$\approx \frac{1 + sRC_1}{sC_1} \tag{2.12}$$

The capacitor C_2 is added to the loop to provide ripple suppression on the control voltage. In the equation above for $G(s)$, C_2 is small and without incurring a lot of error it is ignored to simplify the understanding. Using these expressions, the closed-loop transfer function is given by eqn. 2.13.

$$H(s) = \frac{\frac{K_{PD}}{N} K_{VCO} R(s + \frac{1}{RC_1})}{s^2 + \frac{sK_{PD}K_{VCO}R}{N} + \frac{K_{PD}K_{VCO}}{NC_1}} \tag{2.13}$$

Comparing with a general second-order system, the natural frequency and damping factor are given as follows:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC_1}} \tag{2.14}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_{PD}K_{VCO}C_1}{N}} \tag{2.15}$$

Since there are two integrators in the loop (one from the VCO and the second from the filter), the CPPLL shown here is a Type-II PLL. The order of the loop as seen from eqn. 2.13 is also two (Note: if C_2 is not ignored, its a third-order loop). If the loop filter resistor (R) is not used, the loop transfer function contains two poles at DC and no zeros which makes it unstable. Therefore a stable Type-II PLL must have at least one zero.

Loop Bandwidth: The closed-loop transfer function of the PLL has a low-pass characteristic. The 3-dB frequency of the closed loop is the same as gain cross-over frequency of the open loop transfer function. The loop bandwidth can be calculated as

$$\omega_{3dB} = \frac{K_{PD}K_{VCO}}{N}R = 2\zeta\omega_n \tag{2.16}$$

Note that this is also the loop gain of the PLL. The loop gain is a more useful indicator of the loop bandwidth than ω_n in wide bandwidth PLLs, while in narrow bandwidth PLLs noise bandwidth (B_L) is a better indicator [11]. The noise bandwidth for second order Type-II PLL is given by

$$B_L = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \tag{2.17}$$

All the analysis so far assumes continuous-time analysis which is true if the loop bandwidth is a small fraction of the input reference frequency. If large bandwidths are used, this approximation breaks down due to the discrete nature of CPPLLs. A z-domain analysis is requires for accurate analysis in such situations. One such analysis is presented in [12].

2.3 Transient Behavior of a PLL

In the steady-state, when the PLL is locked, the phase error is small and the PLL is said to *track* the input. In this mode, when there is a step change in the frequency or phase of the input (or a divide ratio change), the PLL tracks this change with an error. The settling behavior of the error is of interest in applications where fast frequency switching is needed.

A first-order PLL uses a proportional loop filter and eqn. 2.9 reduces to

$$H(s) = \frac{K}{s+K} \tag{2.18}$$

and the error function is given by

$$H_e(s) = 1 - H(s) = \frac{s}{s+K} \tag{2.19}$$

For a step change in phase ($\Delta\theta u(t)$) the error response is given by

$$\Phi_e(t) = \Delta\theta e^{-Kt} \tag{2.20}$$

Similarly, for a frequency step change, the transient of the error is given by

$$\frac{\Delta\omega}{K}\left(1 - e^{-Kt}\right) \tag{2.21}$$

Similarly for a second order Type-II PLL (eqn. 2.13), the phase error settling in case of a frequency step is given by [11]

$$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta^2}\omega_n t\right)e^{-\zeta\omega_n t} \qquad \text{for } \zeta < 1 \tag{2.22}$$

$$\frac{\Delta\omega}{\omega_n}\left(\omega_n t\right)e^{-\zeta\omega_n t} \qquad \text{for } \zeta = 1 \tag{2.23}$$

$$\frac{\Delta\omega}{\omega_n}\left(\frac{1}{\sqrt{\zeta^2-1}}\sin\sqrt{\zeta^2-1}\omega_n t\right)e^{-\zeta\omega_n t} \qquad \text{for } \zeta > 1 \tag{2.24}$$

From the settling expressions for both first-order and second-order PLLs, the settling for small phase and frequency jump at steady-state is exponential and the time-constant is inversely proportional to the loop bandwidth. In case the bigger steps in frequency or phase are applied, the PLL can loose lock and enter a nonlinear region. The limits of linear tracking are set by the limits of the linear regions of operation of the PFD and the tuning range of the VCO. There are several regions of operation of a PLL

- *Hold-in range* (ω_H) is the frequency range in which the PLL can stay in lock. For a CPPLL with passive loop filter, ω_H is ∞ and is only limited by the VCO tuning range.

- *Lock-in range* (ω_L) is the frequency range in which the PLL can acquire lock without cycle slipping.

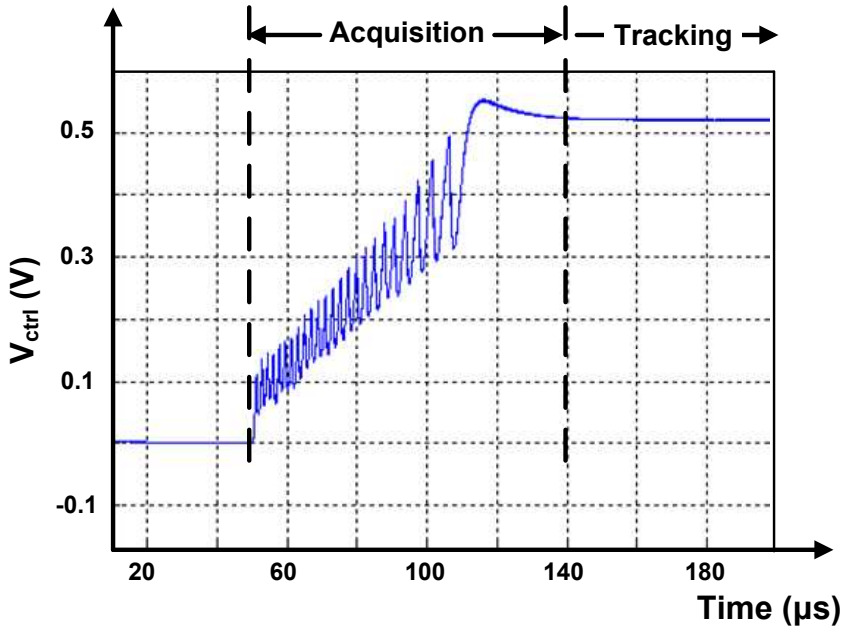


Figure 2.11: PLL loop dynamics

- *Pull-in range* is the frequency range in which the PLL can acquire lock after cycle slips.

If the applied input pushes the PLL beyond the linear region, cycle-slipping occurs and if the PLL regains lock it is called *acquisition*. Fig. 2.11 shows behavioral simulation of a CPPLL (simulated using CPPsim [13]) with a large frequency step. The PLL cycle slips during the acquisition phase and once the PLL is *pulled-in* close to the linear region the PLL settles within the next cycle and starts tracking the new frequency. Since the pull in process is a non-linear process, the accurate estimation of pull-in time is very difficult. Approximate expressions are available in literature [11, 14]. Assuming a sinusoidal phase detector the pull-in time is given by

$$T_p \approx \frac{4\zeta^2(\Delta\omega)^2}{K^3} \tag{2.25}$$

where K is the loop gain. This is the time taken from the start of the frequency acquisition to the edge of linear operation. This is a very slow process and cycle slipping should be

avoided if fast settling times are required.

2.4 Direct Digital Synthesis

Direct digital synthesis (DDS) is a digital technique to generate accurate and versatile waveforms. The basic architecture of a DDS (Fig. 2.12) comprises a phase accumulator, a phase-to-sine/cosine converter and a D/A converter (DAC). The basic operation is best explained in the case of sine-wave generation. The phase accumulator generates the phase information and since there is a definite relation between the phase and amplitude of a sine wave, the phase-to-amplitude conversion is done using a ROM look-up table. The DAC converts the sampled sine wave into an analog waveform. The M-bit control word determines the DDS output frequency given in (2.26).

$$f_{out} = M \times \Delta f \qquad \Delta f = \frac{f_{ref}}{2^N} \tag{2.26}$$

where N is the length in bits of the phase accumulator and Δf is the frequency resolution

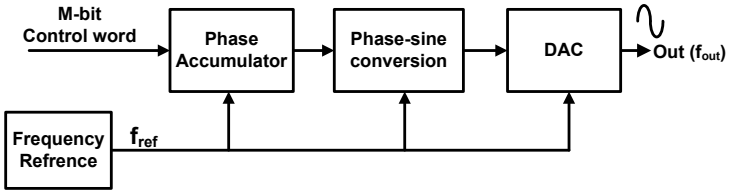


Figure 2.12: Basic architecture for a direct digital synthesizer

of the DDS. Direct digital synthesis systems have a number of distinct advantages over PLL-based synthesizers:

- Complete digital control
- Very high frequency resolution and sub-degree phase resolution
- Extremely fast hopping capability. The frequency hop can be made *phase continuous*; therefore there is no settling time associated with it.

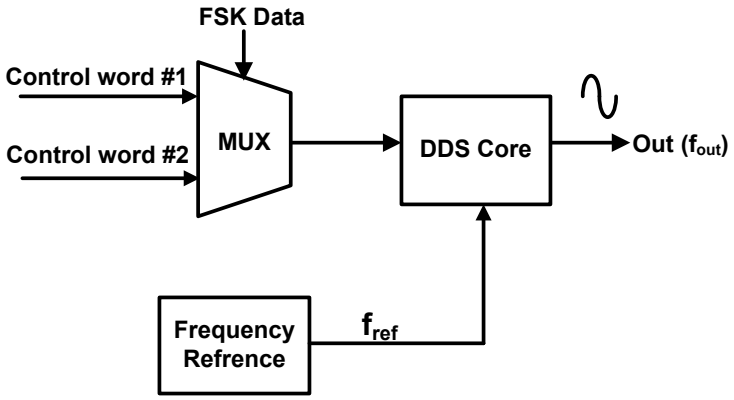


Figure 2.13: Generating a binary FSK signal using a DDS

- Excellent matching in polyphase synthesis (e.g., I and Q matching in quadrature generation).

The advantages of the DDS are more apparent if a modulated source is required. By choosing between different control words, the required modulation (i.e., frequency-shift-keying (FSK) or phase-shift-keying (PSK)) can be achieved. Fig. 2.13 shows a potential scheme to generate a binary FSK (BFSK) signal. Since both control words are available, switching between frequencies can be very fast.

The primary disadvantage of the DDS comes from the fact that it essentially performs a division on the input reference frequency and the maximum operating frequency is limited to $\leq \frac{f_{ref}}{2}$ (Nyquist theorem). The implementation of on-chip DACs [15] have allowed the use of higher reference frequencies and extended the operating frequency of the DDS but it is still limited to several hundreds of MHz or the lower GHz. This limits the applicability of DDS signal generators in wireless systems. We will show that our techniques for fast frequency hopping in ILOs can be used to extend the operating frequency range of DDS's

2.5 Chapter Summary

In this chapter a brief background of frequency synthesis techniques is presented. PLLs are most common frequency synthesis techniques used in radio transceivers. Linear models for a PLL are presented and the closed-loop transfer functions are derived. An overview of charge-pump-based PLLs is then presented. Settling behavior and lock times of first-order PLL and second-order Type-II PLLs were then discussed. It is found that the settling times in PLL in the tracking region depends on the loop bandwidth of the PLL. In applications where fast settling is required, wide bandwidths become necessary. However the PLL bandwidths are restricted usually to $\frac{1}{10^{th}}$ of the input reference frequency due to stability, noise and spur suppression constraints. Finally, direct digital synthesis is presented as another technique for frequency synthesis where extremely fast settling is possible. However, the main drawback of traditional DDS is that it is based on frequency division of input signal and so the frequency range is limited to half of the input frequency.

Chapter 3

Injection Locking in Oscillators

Oscillator systems appear in a variety of fields - electronics, optics, mechanical and chemical systems, to name a few. Oscillators are autonomous systems, i.e, no external input apart from the power supply is required to generate an output. But when a periodic signal is impressed on the oscillator, interesting non-linear behavior can be observed. If the applied signal is very close to the natural frequency of the oscillator, contrary to intuition, the output does not beat at the difference frequency. Rather, the oscillator locks to this external signal and at steady-state, the output frequency of the system is the same as that of the external signal. This synchronization of the oscillator to an external signal can be desirable or otherwise, depending on the application. If the external signal does not have enough power, for example substrate coupling between transmit and receive VCOs [1], locking does not occur. This phenomenon is referred to as injection-pulling. Observations of injection-locking have been reported since the beginning of the 17th century for a number of oscillatory systems (mechanical oscillators like pendulum clocks, for example) [1]. The first theoretical investigation of injection-locking of electrical oscillators was conducted by Balthasar Van der Pol in 1927 [16] and a simplified mathematical analysis of injection-locking was contributed by Robert Adler

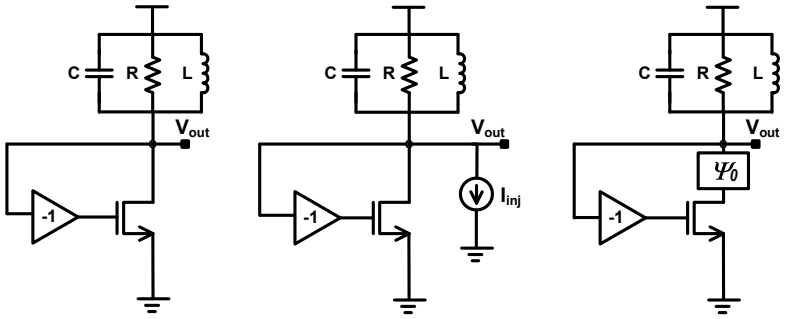


Figure 3.1: Conceptual model for an ILO

in 1946 [17]. Over the years, further analysis of injection-locked oscillators operating under various conditions, have been presented [18–21].

3.1 Fundamental Concept

Oscillators are inherently positive feedback systems. Injection-locking is best understood by analyzing the total phase around the loop of an injection-locked LC-oscillator [1]. The ILO consists of an oscillator with the provision to input an external signal in the form of current or voltage. Shown in Fig. 3.1 is a conceptual LC-oscillator represented as a feedback self-sustaining loop. The transistor introduces a phase shift of π from the gate to the drain terminal and the ideal inverting block introduces an additional phase shift of π making the overall phase-shift equal to 2π. The oscillator output frequency is the natural frequency of the LC-tank, ω_0 $(= 1/\sqrt{LC})$, at which the LC-tank introduces zero phase-shift.

When an injection-signal, here represented in the form of current I_{inj} at a frequency of ω_{inj}, is introduced into the loop, it creates an additional phase-shift in the oscillator feedback loop and the total current flowing into the tank is the vector sum of the oscillator current and injection current. Due to the phase-shift introduced, the oscillator no longer satisfies the Barkhausen criteria at its natural frequency ω_0. Its frequency will have to

be shifted so that the LC-tank contributes a phase-shift opposite to the phase introduced due to injection to satisfy the loop phase-shift criterion. If the injection frequency ω_{inj} is within the range $(\omega_0 - \omega_L,\ \omega_0 + \omega_L)$, the oscillator locks to the signal and the ILO output frequency is ω_{inj} [1, 17]. The quantity ω_L is defined as the single-sided lock-range of the oscillator. The estimation of lock-range needs mathematical modeling of the injection-locking process.

3.2 Mathematical Models for Injection Locking

The first known model for forced synchronization of oscillators was proposed by Van der Pol. It is based on the Van der Pol oscillator with non-linear damping which is governed by a second-order non-linear differential equation

$$\ddot{x} - \varepsilon(1 - x^2)\dot{x} + x = 0 \tag{3.1}$$

When $\varepsilon = 0$, then the equation reduces to a simple harmonic oscillator:

$$\ddot{x} + x = 0 \tag{3.2}$$

Van der Pol's equation can be extended to include the effect of injection (Eq. 3.1):

$$\ddot{x} - \varepsilon(1 - x^2)\dot{x} + x = A\sin(\omega_{inj}t) \tag{3.3}$$

where A is the amplitude of injection.

Van der Pol's equation for forced oscillations is commonly solved using numerical techniques, which makes it complicated for analysis. Estimation of locking behavior and parameters like lock-range depends very heavily on the description of the device I-V characteristic as a second-order equation. Circuits with multiple devices may be too complicated to be expressed as a second-order equation. Furthermore, simplifications for approximate conditions is not possible which makes developing an intuitive understanding of the locking process difficult.

3.2.1 Adler's Model

The phase/frequency dynamics of an ILO after the injection signal is applied, can be approximated by Adler's equation [17]. The mathematical interpretation, described by Adler, is in the form of a non-linear differential equation in terms of $\phi(t)$, where $\phi(t)$ is the phase difference between the injected signal and the instantaneous oscillator output signal. The Adler's equation assumes certain conditions:

- the injection-signal strength is relatively low ($E_{inj}/E_{osc} << 1$).

- the oscillator current amplitude is constant throughout the transient.

- the injection signal frequency is very close to the center frequency of the tank.

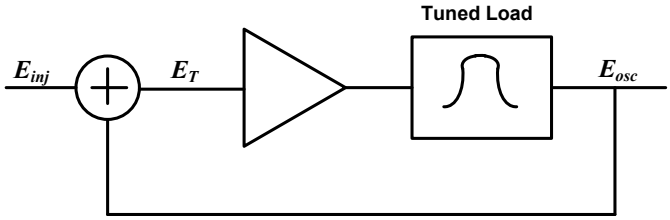


Figure 3.2: Adler's equation: block diagram

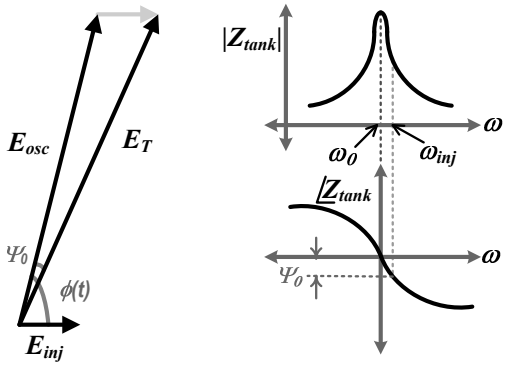


Figure 3.3: Phasor interpretation

In order to derive this equation, consider the oscillator modeled as a feedback amplifier with a tuned load shown in Fig. 3.2. The injection signal, E_{inj}, is added in the feedback path to the oscillator output signal, E_{osc} and the resultant signal is E_T. This is represented as a phasor shown in Fig. 3.3. The contribution of the tank (lead or lag) depends on the sign that is assumed for $\phi(t)$. Since the injection signal is known and constant, all the other vectors are drawn with respect to E_{inj}. The relative frequency (instantaneous beat frequency) can now be expressed as

$$\Delta\omega = \frac{d\phi(t)}{dt} \tag{3.4}$$

In the absence of the injection signal, the vectors E_{osc} and E_T are aligned. And since the output voltage is generated by E_T passing through the tank impedance (contributing zero phase at resonance), it is also aligned to E_{osc}. In the presence of the external signal, E_T is phase-shifted from E_{osc}. On the other hand, the output voltage aligns with E_{osc} only after experiencing the phase-shift provided by the tank. This is when injection-locking occurs. Applying the sine-law for triangles to the phasor diagram:

$$\frac{\sin\{\psi_0\}}{E_{inj}} = \frac{\sin\{\phi(t)\}}{E_{osc}} \tag{3.5}$$

$$\sin\{\psi_0\} \approx \psi_0 = \frac{E_{inj}}{E_{osc}}\sin\{\phi(t)\} \tag{3.6}$$

Eqn. 3.6 is valid for low-level injection. The phase-frequency relation for a tuned load (Fig. 3.3) in the vicinity of the free-running frequency is given by

$$\psi_0 = \arctan\left(\frac{2Q}{\omega_0}(\omega_0 - \omega)\right) \tag{3.7}$$

The instantaneous beat frequency (eqn. 3.4) can now be written as

$$\frac{d\phi(t)}{dt} = \omega - \omega_{inj} = (\omega - \omega_0) + (\omega_0 - \omega_{inj}) \tag{3.8}$$

From eqns. 3.6, 3.7 and 3.8 it follows:

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \frac{\omega_0}{2Q}\left(\frac{E_{inj}}{E_{osc}}\right)\sin\{\phi(t)\} \tag{3.9}$$

This non-linear differential equation is called Adler's equation. It describes the rate of variation of instantaneous phase difference between the oscillator and injection signal in terms of circuit parameters: oscillator signal strength (E_{osc}), injection signal strength (E_{inj}) and tank quality factor (Q).

The steady state, when injection locking occurs, is described by $\frac{d\phi(t)}{dt} = 0$. The steady-state phase difference between the injection signal and the oscillator signal is given by

$$\phi_{ss} = \sin^{-1}\left(\frac{2Q}{\omega_0}\left(\frac{E_{osc}}{E_{inj}}\right)(\omega_0 - \omega_{inj})\right) \tag{3.10}$$

From (3.10), the lock-range ω_L can be estimated since $|\sin\phi_{ss}|$ is always less than one. The lock range is given by

$$\omega_L = \frac{\omega_0}{2Q}\left(\frac{E_{inj}}{E_{osc}}\right) \tag{3.11}$$

The same equation is obtained using a different procedure in [1]. Though there are some simplifying assumptions in the derivation of Adler's equation, it very accurately describes the transient settling and out-of-lock-range behavior of ILOs (as long as eqn. 3.7 holds in this region). Several extensions to this equation have been presented to remove the simplifying assumptions [18, 21].

3.2.2 Adler's Equation for High-Injection Levels

A more accurate expression that does not assume the small-signal injection condition was developed in [18]. Considering Fig. 3.3 once again, we can write

$$\tan\psi_0 = \frac{E_{inj}\sin\{\phi(t)\}}{E_0 + E_{inj}\cos\{\phi(t)\}} \tag{3.12}$$

Substituting 3.12 in 3.7 and using 3.8 we arrive at extended Adler's equation given by

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \frac{\omega_0}{2Q}\frac{E_{inj}}{E_{osc}}\frac{\sin\{\phi(t)\}}{1 + (E_{inj}/E_{osc})\cos\{\phi(t)\}} \tag{3.13}$$

The lock range expression, following the same procedure as in Section. 3.2.1, now becomes:

$$\omega_L = \frac{\omega_0}{2Q}\frac{E_{inj}}{E_{osc}}\frac{1}{\sqrt{1-\left(\frac{E_{inj}}{E_{osc}}\right)^2}} \tag{3.14}$$

and the final steady state phase is given by

$$\phi_{ss} = \sin^{-1}\left(\frac{2Q}{\omega_0}\frac{E_{osc}}{E_{inj}}\frac{(\omega_0-\omega_{inj})}{\sqrt{1+K^2}}\right) + \sin^{-1}\left(\frac{2Q}{\omega_0}\frac{(\omega_0-\omega_{inj})}{\sqrt{1+K^2}}\right) \tag{3.15}$$

where

$$K = \frac{(\omega_0-\omega_{inj})}{\frac{\omega_0}{2Q}}$$

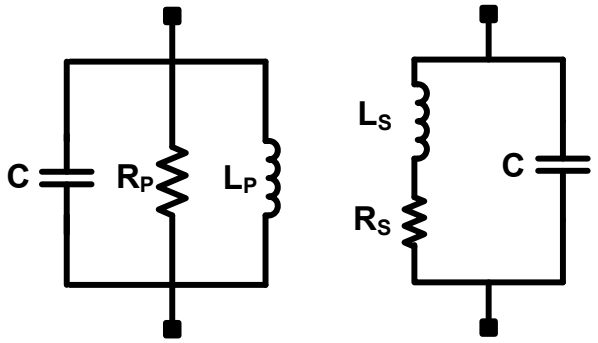
3.2.3 Other Models

The above models assume relatively high-Q and symmetric tuned loads. Some designs in CMOS may not meet the criteria described. For example, quality factors for inductors in pure digital CMOS are usually well below 10. In many designs where wide bandwidth is required the Q's are intentionally made low. Then there is the case of ring oscillators in which the individual stages in most cases have RC loads rather than tuned loads. Some models have been proposed to address these cases.

Low-Q oscillators

The issue of low-Q LC oscillators with high injection signals is addressed in [20, 22]. The primary difference is that the models discussed earlier consider the tuned load to be a symmetric parallel RLC circuit. This is an approximation of the series resistance that appears because of the Q of the inductor (assuming operating frequencies are low and capacitor Q is very high). The transformation used for series RL + parallel C (Fig. 3.4a) to parallel RLC (Fig. 3.4b) is given by

$$R_P = R_S(Q^2+1) \quad L_P = L_S\left(\frac{Q^2+1}{Q^2}\right) \tag{3.16}$$



(a) Parallel RLC

(b) Series RL with Parallel C

Figure 3.4: RLC tank high-Q vs low-Q

where L_S and R_S are the series inductance and series resistance and L_P and R_P are the transformed parallel values. The Q of the inductor is given by $Q = \frac{\omega_0 L_S}{R_S}$. Fig. 3.5 shows the comparison of impendence and phase between series and equivalent parallel transformation of an RLC tank (Fig. 3.4). The approximation holds well for inductor with high Q (Fig. 3.5(b)) and breaks down as the Q is reduced (Fig. 3.5(a)). In such cases, tuned loads with series RL and parallel C should be considered. The difference in derivation lies in estimating the phase shift contributed by such a circuit.

$$\tan\psi_0 = \frac{2Q(\omega_0-\omega)}{\omega_0}\left[\frac{1}{2}\left(1-\frac{1}{Q^2}\right)^{1.5}\left(\frac{\omega+\omega_0}{\omega_0^2}\omega\right)\right] \tag{3.17}$$

which yields the following very complicated equation for the ILO with series RL and parallel C load

$$\frac{\left(\frac{d\phi(t)}{dt}+\omega_{inj}\right)^3}{\omega_0^2} - \frac{d\phi(t)}{dt} = \omega_{inj} - \left(\frac{\omega_0}{Q\left(1-\frac{1}{Q^2}\right)^{1.5}}\right)\frac{K\sin\phi(t)}{1+\cos\phi(t)} \tag{3.18}$$

Some interesting outcomes of such analysis are as follows:

- The lock range of the ILO is not symmetric about the free running frequency of the oscillator which is the case in the parallel RLC analysis (Adler's equation).

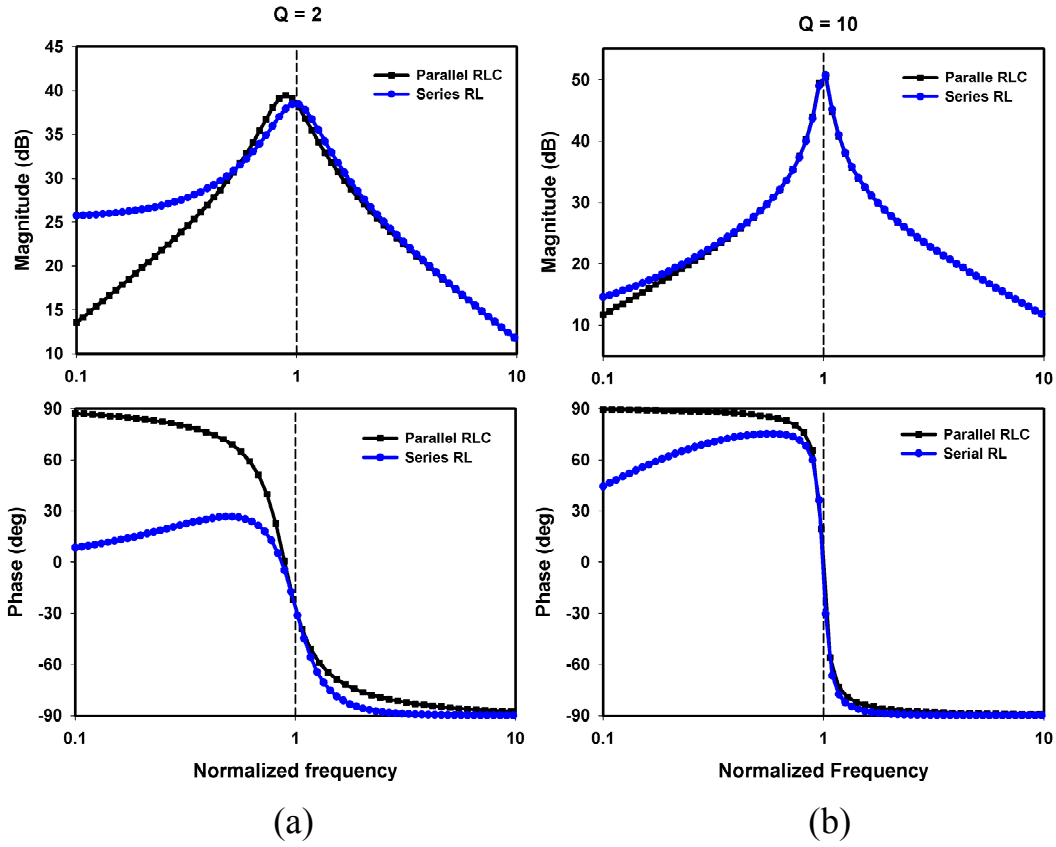


Figure 3.5: Amplitude and phase in series and parallel tank

- For low Q and high injection strength case, the maximum phase shift (ϕ_{ss}) achieved is not limited to $\pm 90^\circ$ but is larger ($\pm 120^\circ$ in some cases).

Ring Oscillator

The analysis of injection locking presented so far is based on harmonic oscillators with a narrow band tuned load. This allows for phasor representation of the locking signals as there is only one dominant frequency tone in the system. This cannot be directly applied to the ring oscillators based on RC loads. The non-harmonic nature of such oscillators means that the phasor representation of the signals in the loop is not valid for all general cases. But assuming a quasi-linear operation and a near sinusoidal output,

phasor analysis can be applied directly. Such an analysis is presented in [23].

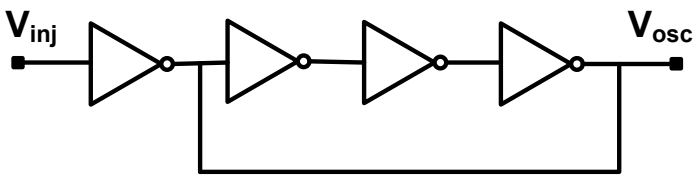


Figure 3.6: Injection locked ring oscillator with single point injection

Shown in Fig. 3.6 is a single-point injection scheme for ring oscillators. The corresponding model used is shown in Fig. 3.7. Here injection is modeled as an additional current source. The total phase contribution of the delay cells is lumped and a phasor diagram is drawn similar to the one shown in Fig. 3.3. Defining Q of the ring oscillator as [10, 23],

$$Q = \frac{\omega_0}{2}\frac{d\theta}{d\omega} \tag{3.19}$$

where θ is the phase of the open-loop transfer function of the oscillatory system and assuming a small signal injection level, an equation for injection locking in ring oscillators is derived as

$$\frac{d\phi}{dt} = (\omega_0 - \omega_{inj}) - \frac{\omega_0}{2Q}S\sin(\phi) \tag{3.20}$$

where $S = \frac{|I_{inj}|_{av}}{I_{osc}|_{av}}$ which, for the scheme shown in Fig. 3.6, is the ratio of the driving inverter size to the oscillator delay inverter size.

In order to remove the quasi-linear assumption, analysis is done in the time domain in [24]. Shown in Fig. 3.8 is the model used for a four-stage differential ring oscillator for the time domain analysis. The delay cell comprises a switching transconductor (V-I converter) and linear RC load. Here, as in the first case, single-point injection is considered.

Like the beat frequency estimated in the case of frequency-domain analysis, the delay introduced due to the injected signal is estimated in the time domain analysis to estimate the locking behavior. In free running condition, the period of oscillation $T = 2Nt_d$ where

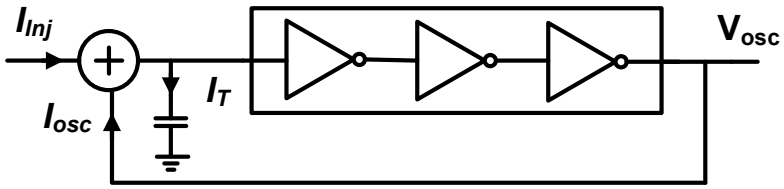


Figure 3.7: Model for injection locked ring oscillator

t_d is the delay contributed by each stage. Upon injection of an external signal, the delay of the first stage (the stage to which injection is applied) is increased or decreased by d depending on the injection signal frequency being lower or higher than the free running frequency respectively. The oscillation period now becomes $T + 2d$. The lock range is estimated by calculating the minimum and maximum delay that is possible by a particular injection strength. It can be shown [24] that the oscillator remains locked if

$$T + 2d_{min} \ < \ T_{inj} \ < T + 2d_{max}$$

where

$$d_{max} = \tau \ln \frac{V_{a,max}}{V_{a,max} - V_{ainj}} \qquad d_{min} = \tau \ln \frac{V_{a,max}}{V_{a,max} + V_{ainj}} \tag{3.21}$$

In the above expressions, $\tau = R_L C_L$, $V_{a,max}$ is the maximum amplitude of oscillation given by $V_{a,max} = I_{Bias} R_L$ and V_{ainj} in the injection signal amplitude. One observation from the above expressions is that the lock range can be increased by increasing the $\frac{V_{ainj}}{V_{a,max}}$ ratio which is intuitive. Further, by considering discrete operation and estimating delay at zero crossings, it has been proved [24] that the ring ILO follows a first order system behavior. Therefore, by increasing the lock range (locking bandwidth), the settling time for a frequency step input can be reduced.

In the case of a single point input the entire loop-delay is changed by modulating the delay of just one delay cell. This leads to a low lock-range. This can be increased by applying a progressively phase-shifted injection signal at multiple points [25, 26] within the loop (at each delay cell). One has to take care that the proper progressive phases are

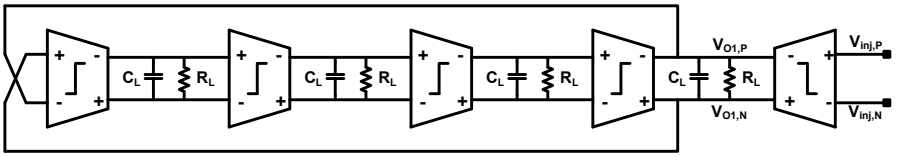


Figure 3.8: Ring ILO for delay based model

applied to achieve the maximum lock range. If non-optimal phase shift (non-progressive or anti-phase) is applied, the lock range will be greatly reduced and may be less than that achieved by single-point injection. One disadvantage of this technique is that the proper phases have to be generated before injection which is not always easy.

3.3 Output Spectra of Unlocked ILOs

An oscillator under injection shows a unique behavior when the conditions for locking are not satisfied. The output spectrum frequency is not just the beat-frequency but varies widely depending on the location of the injection frequency (ω_{inj}) with respect to the free-running oscillator frequency (ω_0). Measurements of oscillators have proved this behavior [27] and was most recently explained in [1] without mathematical expressions for the amplitude of the spurs. This was explained first in [28]. The approach to estimate the unlocked spectrum is based on Adler's equation. The output of an oscillator under injection can be expressed as

$$v(t) = \sin(\omega_{inj} - \phi(t)) \tag{3.22}$$

where $\phi(t)$ is obtained from Adler's equation.

$$\dot{\phi} = \frac{d\phi(t)}{dt} = \Delta\omega_0 - \omega_L \sin\phi \tag{3.23}$$

where $\Delta\omega_0 = \omega_0 - \omega_{inj}$ and ω_L is the lock-range. If the input signal frequency is far from locking condition, $|\omega_{inj} - \omega_0| >> \omega_L$, then $\dot{\phi} = \omega_{inj} - \omega_0$. That is FM sidebands

Table 3.1: Spectral components of unlocked ILO

Frequency	**Absolute amplitude**
ω'	$A_0\left(1-\frac{a^2}{4}\right)$
$\omega'+\Omega$	$\frac{A_0 a}{2}\left(1-\frac{a^2}{4}\right)$
$\omega'-\Omega$	$\frac{A_0 a}{2}$
$\omega'-2\Omega$	$\frac{A_0 a^2}{2}$
$\omega'-3\Omega$	$\frac{A_0 a^3}{8}$

of equal amplitudes at frequencies $\omega_0 \pm (\omega_{inj} - \omega_0)$ are seen. If the injection frequency is moved closer to the lock edge then $\dot{\phi(t)}$ can now be written as

$$\dot{\phi(t)} = \Delta\omega_0 - \dot{\theta(t)} \tag{3.24}$$

and eqn. 3.23 can now be expressed as

$$\dot{\phi(t)} = \omega_L \sin(\Delta\omega_0 t - \theta(t)) \tag{3.25}$$

Now defining a nearness factor $a = \frac{\omega_L}{\Delta\omega_0}$ and expressing $\theta(t)$ as power series $\theta(t) = a\theta_1 + a^2\theta_2 + a^3\theta_3 + ...$, a solution can be obtained for $\theta_1, \theta_2, ...$ Substituting $\theta(t)$ that is obtained in 3.22, the spectrum of the unlocked ILO is obtained and the spectral components are shown in the Table 3.1 where $\omega' = \omega_0 + \frac{a^2}{2}\Delta\omega_0$, $\Omega = \Delta\omega_0 - \dot{\alpha(t)}$ and $\dot{\alpha(t)} = \frac{a^2}{2\Delta\omega_0}$

Many interesting properties of the unlocked spectrum are explained with the above analysis:

- All the spurs in the spectrum appear on the opposite side of the injected frequency.

- The output of the oscillator is pulled from the free running frequency to a new frequency given by ω'.

- The amplitude of the sidebands opposite to the carrier frequency decreases exponentially away from the carrier frequency

The same results were obtained using a different method in [29].

3.4 Applications

One of the widespread initial applications of injection-locking has been in the field of optics [30]. The similarity between laser and oscillator theory has resulted in the use of injection-locking in high-power low-noise lasers. In electronics, some of the initial applications of injection-locking were in high-frequency FM signal generation and amplification [31, 32]. Injection-locking was also used for synchronization of high-frequency oscillators [33, 34]. More recently, it has been employed in electronic integrated circuits.

Frequency Division

The most popular present day application of ILOs is in frequency division. Injection-locked frequency divider (ILFD) is a low-power analog division technique useful in PLLs as pre-scalars. In PLLs, most of the power is consumed by the frequency dividers which operate at a much higher frequency compared with other components within the loop. Current-mode logic (CML) and static frequency dividers are widely used as pre-scalars. However, they consume significant power at such high frequencies. A lower power alternative are regenerative Miller dividers [35, 36]. They are the closest designs to ILFD but the primary difference is that Miller dividers are not self-oscillating and require an input signal to start-up. An ILFD based on a negative-G_m LC-oscillator is presented in [37]. The principle is easily understood by noting that the common source node of the cross-coupled transistor pair oscillates at twice the oscillator free-running frequency and by applying an input signal to this node at a close frequency, the oscillator is injection-locked. The output is half the input frequency and thus operating as a divide-by-2 circuit.

In [38], a ring oscillator is presented as a pre-scalar. Here the mixing action of the input frequency with higher harmonics from diff-pair switching and filtering (low-pass filter) characteristic is used to perform division. Here, as in the case with the LC-oscillator version described above, the input signal is applied to the tail current transistor. One issue with it is the low lock-range achieved. A technique to improve lock range by shunt peaking is proposed in [39] and a current-mode injection scheme is proposed in [40]. The primary advantage of ILFDs is the low power consumption. Also, since ILFDs are based on oscillators they can be designed to operate at very high frequencies [41].

Frequency Multiplication

Frequency multiplication is another application where ILOs are a low power alternative to the existing techniques. Very high frequency synthesis results in a high power consumption in the divider chain in a conventional PLL. Using a frequency multiplier allows the VCO to run at a lower frequency and reduces the power consumption. A common implementation of frequency multiplier is to generate harmonics of an input signal using a nonlinear device, and then choose the desired harmonic component by a filter network. The nonlinear device can be a diode or a transistor biased at a small conduction angle and the filter network is usually built by passive LC circuits. Such a harmonic generation and filtering approach requires the filter network to have a very large quality factor to achieve acceptable signal amplitudes and spur filtration. The same concept can be extended to the ILOs, that is, generate higher harmonics and use the ILO to lock onto the required harmonic. In a sense, the ILO is being used as a very high-Q filter and the output amplitude of the system is the same as that of the oscillator which can be made high. Such a scheme is presented in [42] where an ILO is used as dual modulus (by-2 and by-3) multiplier. The non-linear device used is a transistor and the signal is fed into the ILO using an on-chip balun into the source nodes of the diff pair. By tuning the oscillator closer to the required harmonic, locking is achieved. A ring oscillator version

of multiply by-3 is presented in [43]. Again a transistor is used as a non-linear device and the signal is injected between two stages of a three-stage ring oscillator.

Precision Quadrature Generation

Traditionally quadrature signals are generated using polyphase RC-CR networks, frequency division or quadrature VCO. Further discussion of each technique is presented in Chapter 7. In [44], a precision quadrature generation scheme using injection-locking is presented. The architecture is built on a differential ring oscillator having an even number of stages. Differential summing junctions are provided at the inputs of some stages driven by injection signals. Two stages of ring oscillators are fed from an RC-CR stage. The cascade results in a quadrature improvement which is limited by device mismatch in the second ring.

Clocking

With increased clock speeds in microprocessors, on-chip clock distribution is a critical issue. Current schemes consume a lot of power (about 40% of the total power) which is bound to increase with increasing frequencies. A clock distribution scheme based on injection locking is presented in [45]. Here ILOs are used to generate local clocks which are synchronized to the global clock through injection locking. In [45], an ILFD is used to generate local clocks. An interesting alternative to consider is to use injection locked multiplier for local clock generation which allows for a low speed distribution network if one is needed. This greatly reduces the power consumption. The application of ILOs is extended to clock deskew in clock and data recovery (CDR) circuits in [46]. The I/O receiver reported in [46] is based on a forwarded clock. DLLs are commonly used for clock-data deskew, but their all-pass jitter transfer characteristic does not reduce high-frequency jitter. PLLs may be used to filter jitter on the forwarded clock above the PLL bandwidth. Here the ILO based on a LC-digitally controlled oscillator (LCDCO) is used

to lock on to the forwarded clock. Phase tuning is achieved by exploiting the relation in eqn. 3.10. The DCO frequency is tuned to achieve the required phase relationship. An embedded clock technique is utilized in an injection-locking based CDR in [47] which eliminates the need for dedicated clock lines, therefore saving area.

Variable Phase Generation

The final steady-state phase dependence on injected and oscillator frequencies is exploited in [48] to create variable phase-shift. A dual-mode phased array receiver based on this technique is proposed in [48]. In one mode, the phase shift between different channels of the phase array is controlled by individually controlling the ILOs with respect to the injected signal. In the second mode, progressive phase shift is created by cascading the ILOs and applying the injection signal to the first ILO. Care has to be taken in this case to ensure unilateral injection locking.

3.5 Chapter Summary

In this chapter, a brief review of injection locking process in oscillators is presented. First, the fundamental concept of injection locking was explained using a conceptual oscillator model. Mathematical models for ILOs are then presented to understand the locking dynamics. The first model for forced oscillations in non-linear oscillators was presented by Van der Pol but the model is too complicated to get any intuitive design insight. The lock range was first estimated by Adler's model. By using some simplifying assumptions, an intuitive but powerful non-linear differential equation was developed by this model. An extension to this model was then presented which removed the assumption of very small injection levels. Then a model applicable for low-Q harmonic oscillators was presented which correctly estimates the non-symmetric nature of lock range in such systems. Models for non-harmonic (ring) oscillators in both frequency and

time domain were then presented. Finally applications utilizing the various aspects of ILOs were discussed.

Chapter 4

Transient Behavior of Injection Locked Oscillators

Several important models and applications for injection locking have been presented in the previous chapter. Investigation of injection-locked oscillators (ILOs) for most recent applications [41, 44, 49] has focused on their steady-state behavior and properties, such as the lock-range and the output phase noise. In applications where settling behavior of ILOs is important, this understanding is insufficient and a comprehensive theory for transient behavior is required. Of the models presented in Chapter 3, Adler's equation is most suitable for the analysis. As shown in this chapter, in spite of its simplifying assumptions, this equation very accurately predicts the ILO transient behavior. Models extending the Adler's equation, however, are too complex for design synthesis, thereby losing their intuitive appeal. For the rest of this work, Adler's original equation is used.

4.1 Adler's Equation: Graphical Interpretation

Adler's equation, as discussed in Chapter 3, repeated here for convenience:

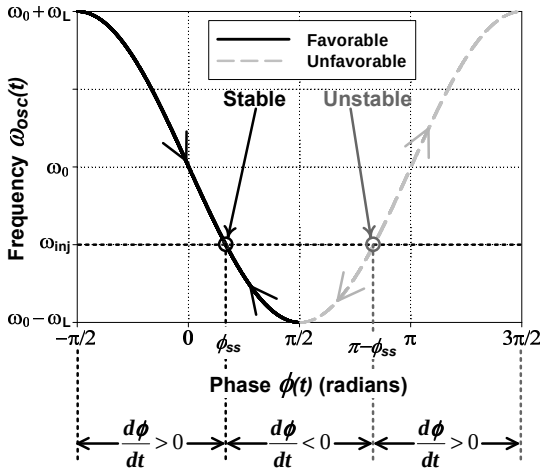


Figure 4.1: Plot of Adler's equation: we plot $\omega_{osc}(t)$ as a function of $\phi(t)$, the phase difference between the injection signal and the injection-locked oscillator output

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)\sin\{\phi(t)\} \tag{4.1}$$

Since frequency is the rate of change of phase, by writing $d\phi(t)/dt = \omega_{osc}(t) - \omega_{inj}$ in eqn. 4.1, Adler's equation can also be interpreted in terms of the instantaneous frequency of the oscillator:

$$\omega_{osc}(t) = \omega_0 - \omega_L \sin\left[\phi(t)\right] \tag{4.2}$$

This equation relates the instantaneous phase-difference to the instantaneous frequency of the oscillator output. A complete transient portrait can be obtained by solving the non-linear differential equation (eqn. 4.1). But before that, examining the graphical representation of Adler's equation gives some very valuable insights and allows us to intuitively predict some interesting aspects of an ILO and its transient behavior.

Fig. 4.1 shows a graphical representation of eqn. 4.1 for low-side injection (LSI) when $\omega_{inj} < \omega_0$. We see that the ILO reaches the injection-signal frequency (ω_{inj}) for two different phases, ϕ_{ss} and $(\pi - \phi_{ss})$. Since the steady-state frequency of an ILO is

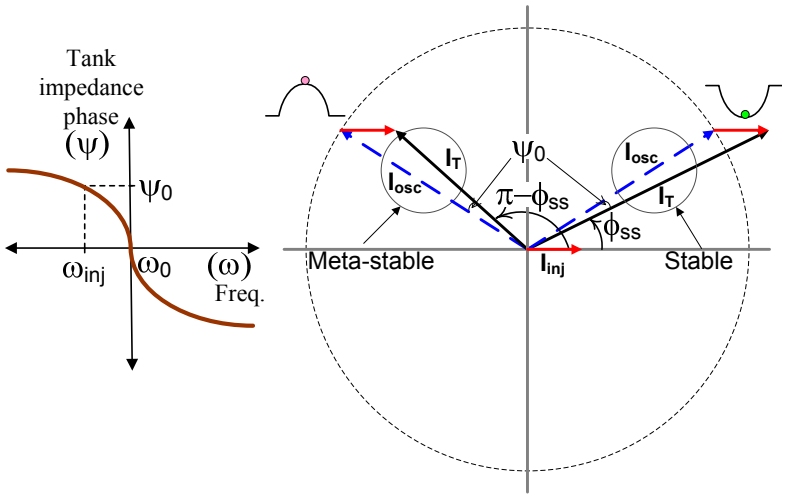


Figure 4.2: LC-tank impedance phase (ψ) plot (left) & Phasor diagrams for stable and meta-stable conditions (right)

ω_{inj}, both these two phases can be the final steady-state phases. If we assume that $\phi(t)$ is slightly less than ϕ_{ss}, the slope is positive ($d\phi(t)/dt > 0$) and $\phi(t)$ moves to the right towards ϕ_{ss}. If $\phi_{ss} < \phi(t) < \pi - \phi_{ss}$, $d\phi(t)/dt < 0$ and $\phi(t)$ moves to the left, again towards ϕ_{ss}. Therefore, ϕ_{ss} can be defined as a *stable equilibrium* point. On the other hand, if a similar perturbation analysis is performed around $(\pi - \phi_{ss})$, it reveals that it is an *unstable equilibrium* point. So ϕ_{ss} is the only *true* steady-state phase, whereas $(\pi - \phi_{ss})$ is an unstable equilibrium point.

The phasor diagram in Fig. 4.2 further proves the existence of two equilibrium points. The phasors represent the injection current (I_{inj}), current through the $-G_m$ cell (I_{osc}) and current through the LC-tank (I_T). The relation between the three phasors is $I_{inj} + I_{osc} = I_T$. When operating in the voltage-limited regime [50], the I_{osc} can be assumed to have a constant magnitude. Since I_{inj} is an external input, it has a constant frequency and also a constant magnitude. The phasor diagram is therefore referenced at I_{inj}. The phase characteristics of the tank impedance (shown left of the phasor diagram) requires that for a tank oscillation frequency of ω_{inj} (for LSI case), the voltage output

of the tank should lead the tank current (I_T) by ψ_0 and the tank voltage is always in phase with I_{osc}. Therefore, in the steady-state, I_{osc} must lead I_T by ψ_0. Geometry shows that there can only be two cases in the phasor diagram, when this can occur (shown in Fig. 4.2). These two cases are two the equilibrium points. One of them shows characteristics of stable equilibrium and the other one shows meta-stable equilibrium.

Looking at Fig. 4.1 again, we can draw some additional insights about the frequency settling characteristics. First, at the point of injection (assuming $t = 0$), the phase difference $\phi(0)$ controls the value of $\omega_{osc}(0+)$. Consequently, the oscillator frequency has to jump from ω_0 $(= 1/\sqrt{LC})$ at $t = 0-$ to $\omega_{osc}(0+)$. These two frequencies are only equal (no jump) when $\phi(0)$ is zero or π. Interestingly, for both $\phi(0) = \phi_{ss}$ and $\phi(0) = (\pi - \phi_{ss})$, the oscillator frequency jumps instantaneously to ω_{inj} at the point of injection. This is an interesting phenomenon where the frequency of an ILO can jump instantaneously and is discussed further later in this chapter.

Secondly, if $\phi(0)$ is in the interval $[-\pi/2, \pi/2]$, then the oscillator frequency $\omega_{osc}(t)$ settles monotonically to ω_{inj}. On the other hand, if $\phi(0)$ lies in the intervals $[\pi/2, 3\pi/2]$, then the frequency settling is non-monotonic. The frequency first moves away, reaches the edge of the lock-range and then falls back monotonically to ω_{inj}. Since this usually takes much longer than purely monotonic settling, therefore if we wish to design fast-settling systems, the region $[-\pi/2, \pi/2]$ is preferable.

4.2 Solution to Adler's Equation

An analytical solution to Adler's equation can be reached by substituting $\sin(\phi(t)) = 2u(t)/\{1 + u(t)^2\}$, where $u(t) = \tan\left(\frac{\phi(t)}{2}\right)$. After some simplification, the solution takes the following form, which has been described in literature [1, 17, 30].

$$\phi(t) = 2\tan^{-1}\left[\left(\frac{\omega_L}{\omega_0 - \omega_{inj}}\right) - \left(\frac{\omega_B}{\omega_0 - \omega_{inj}}\right) \times \tanh\left(\frac{\omega_B(t - t_0)}{2}\right)\right] \tag{4.3}$$

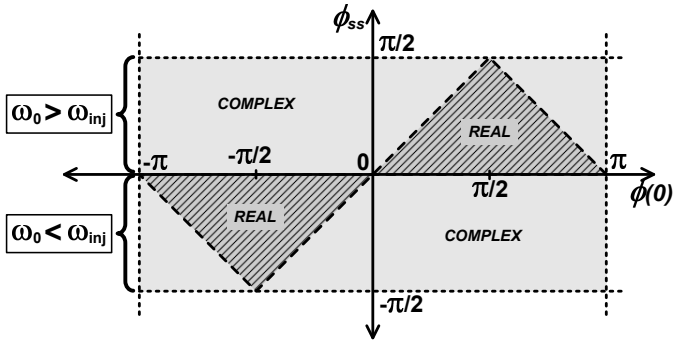


Figure 4.3: Variation of t_0 with initial phase $\phi(0)$ and steady-state phase ϕ_{ss} (shaded area represents the region where t_0 is real)

where

$$\omega_B = \sqrt{\omega_L^2 - (\omega_0 - \omega_{inj})^2} \tag{4.4}$$

Here, ω_B is a measure of the distance of the injected frequency from the oscillator's center frequency ω_0 with respect to both the edges of the lock-range. Also, it should be noted that t_0 is not a 'real' time constant.

$$t_0 = \frac{1}{\omega_B} \ln \left(\frac{\cot\left(\frac{\phi_{ss}}{2}\right) - \tan\left(\frac{\phi(0)}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)} \right) \tag{4.5}$$

In fact, it can acquire a complex value depending upon the initial phase of injection, $\phi(0)$ and whether $\omega_0 < \omega_{inj}$, or otherwise. Fig. 4.3 shows the behavior of t_0 for different cases of $\phi(0)$ and ϕ_{ss}. Clearly, for most cases, t_0 is in fact complex.

The solution to Adler's equation expressed in eqn. 4.3 is convenient in describing the phase of the output as a function of time (the frequency transient can be obtained by differentiating eqn. 4.3 with respect to time). In general, we are interested in the time it takes to lock to the injected frequency and the factors affecting it. By manipulating the solution for eqn. 4.1, the equivalent expression obtained is

$$t = \frac{1}{\omega_B} \ln \left| \left(\frac{\tan\left(\frac{\phi(t)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)} \right) \times \left(\frac{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(t)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)} \right) \right| \tag{4.6}$$

This solution for Adler's equation shows an exponential settling of phase. This settling behavior depends on ω_B. When the injection frequency is at either one of the edges of the lock range, $\omega_B = 0$. This means that the ILO would never settle and this behavior is further confirmed in [21]. Further analysis of ω_B and an optimal range for injection signal frequency for fast-locking are discussed in Section 4.4.

The solution in eqn. 4.3 represents the phase settling for all cases of low-level injection, differentiating which yields a complete frequency settling (presented in Section 4.4). But it is imperative at this point to present a simpler solution to give further intuition into the settling behavior before some theoretical and simulation results are presented.

Linearized solution: Eqn. 4.6 can be further simplified for the case when $|\phi_{ss} - \phi(0)| \ll \pi$. Assuming that $|\phi_{ss} - \phi(0)| \ll |\pi - \phi_{ss} - \phi(0)|$, eqn. 4.3 can be reduced to

$$\tan\left(\frac{\phi(t)}{2}\right) = \beta + \left(\tan\left(\frac{\phi(0)}{2}\right) - \beta\right) e^{-\omega_B t} \tag{4.7}$$

where $\beta = \tan(\phi_{ss}/2)$. Furthermore, if both $\phi(0)$ and ϕ_{ss} are extremely small, which occurs when the injected signal frequency is very close to the free-running oscillator frequency, then the equation can be further simplified to

$$\phi(t) = \phi_{ss} + \{\phi(0) - \phi_{ss}\} e^{-\omega_L t} \tag{4.8}$$

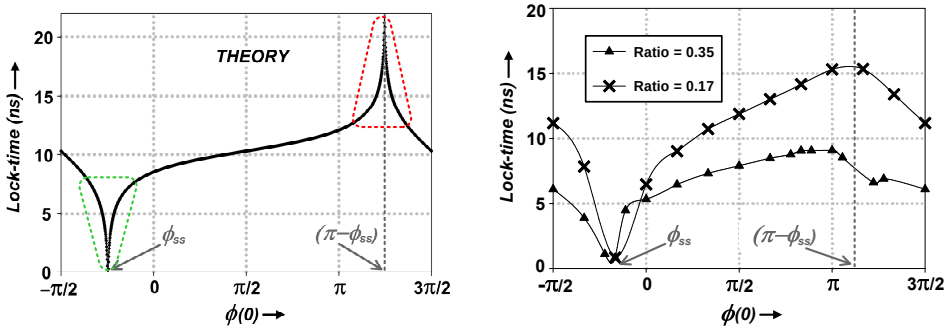
and the corresponding frequency settling behavior is given by

$$\omega_{osc}(t) = \omega_{inj} + \omega_L \{\phi_{ss} - \phi(0)\} e^{-\omega_L t} \tag{4.9}$$

From eqns. 4.7 and 4.8 it can be seen that the phase difference and the frequency difference indeed take on an exponential decay form. The ILO 'ideally' takes infinite time to lock to its final state. Naturally, some form of locking criterion (i.e., some percentage around steady-state value) can be defined to calculate the settling time. Eqn. 4.9 shows that if $\phi(0)$ is equal to ϕ_{ss}, the oscillator locks instantaneously. Further analysis reveals that the lock time is also a strong function of $\phi(0)$. Let us try to understand this behavior by plotting it graphically in the next section.

4.3 Phase and Frequency Settling

Considering a 1% phase settling condition around the steady-state phase, the lock-time (eqn. 4.6) versus initial phase difference, $\phi(0)$, has been plotted in Fig. 4.4a. There are two distinct points which are of interest for fast settling. The first point (surrounding area marked in green) is when $\phi(0) = \phi_{ss}$, where t_{lock} is zero. This is intuitive because for the given condition, ω_{osc} jumps to ω_{inj} at $t = 0+$ (explained by eqn. 4.2). So if the signal can be injected at close to this value of the initial phase, the locking is instantaneous. Another interesting point is when $\phi(0) = \pi - \phi_{ss}$, then t_{lock} is infinite (surrounding area marked in red). This is also expected, since it is an *unstable equilibrium* point. Under ideal conditions, the ILO stays at this point for infinite time. However, in real systems, noise and other perturbations unsettle the ILO from this point and this causes the frequency settling to follow a non-monotonic behavior that takes a long time to settle.



(a) For 1% Phase Settling (Theory)

(b) Simulated Frequency Settling

Figure 4.4: Effect of initial phase $\phi(0)$ and lock range ω_L on lock time: (a) Theoretical estimates of lock-time for 1% phase settling for different initial phase differences ($\phi(0)$) with following conditions: $\omega_0 = 3.54$ GHz, $\omega_{inj} = 3.62$ GHz, $\omega_L = 112$ MHz, (b) Lock-times obtained by simulating an ILO (under similar conditions) in Cadence Spectre^{TM}simulator for two different injection signal strength ratios ($I_{inj}/I_{osc} \Rightarrow$ two different lock-ranges), other conditions being relatively constant

The lock range of an ILO is also a critical factor in the lock time. The simulated frequency lock-times of an ILO for two different lock-ranges (by setting two different relative injection signal strengths) are plotted in Fig. 4.4b. The sharp peak for lock time observed in Fig. 4.4a is not seen here because of the limited accuracy in $\phi(0)$ that can be achieved in simulation. So, in addition to the injection point initial phase dependence, we can conclude to the first-order that the lock time is inversely proportional to the lock-range of an ILO. For systems that exploit the fast-settling behavior of ILOs such as UWB frequency synthesizers and high-frequency FSK synthesizers, a sufficiently large lock-range may be essential. Additionally, the proximity of ω_{inj} to ω_0 also reduces the lock-time.

The frequency settling characteristics for the ILO can be obtained by taking the time derivative of eqn. 4.3.

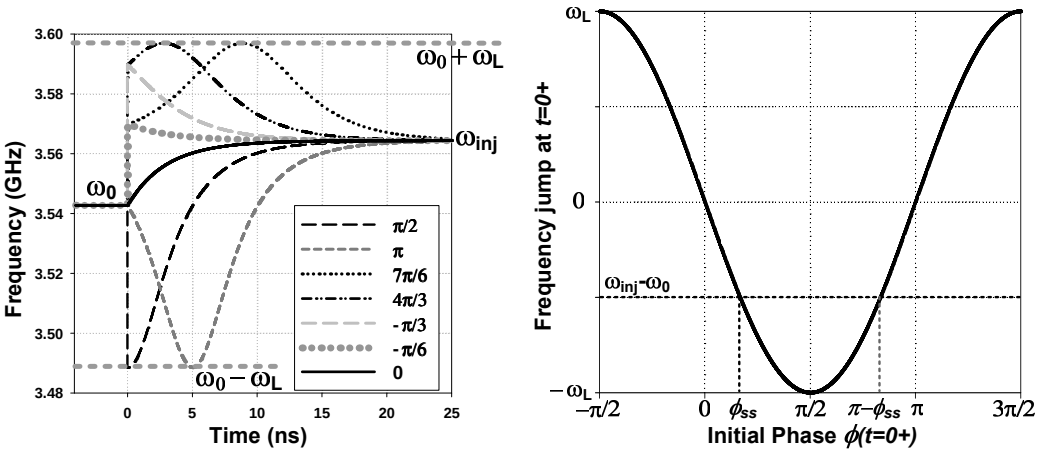
$$\omega_{osc}(t) = \omega_{inj} - \left(\frac{\omega_B^2}{\omega_0 - \omega_{inj}}\right)\left[\frac{\text{sech}^2\left(\frac{\omega_B(t-t_0)}{2}\right)}{1+\tan^2\left(\frac{\phi(t)}{2}\right)}\right] \tag{4.10}$$

Fig. 4.5a depicts the theoretical transient behavior of the frequency of an ILO in the process of locking for different values of $\phi(0)$. Fig. 4.5b plots the amount of frequency jump at the point of injection ($t = 0$) for different values of the initial phase of injection, $\phi(0)$. This graph has the same form as the plot in Fig. 4.1. The frequency jump when the signal is injected perfectly in-phase ($\phi(0) = 0$) or out-of-phase ($\phi(0) = \pi$), is zero. The condition for zero frequency jump at $\phi(0) = 0$ is shown in Fig. 4.5a using a solid black line and for $\phi(0) = \pi$ as a dashed ($--$) dark-grey line.

The conditions used in Fig. 4.5a are: $\omega_0 = 3.543$ GHz, $\omega_{inj} = 3.565$ GHz and $\omega_L = 54.2$ MHz. For these conditions, $\phi_{ss} = -24°$ (close to $(-\pi/6)$) and $\pi - \phi_{ss} = 204°$ (close to $(7\pi/6)$). When an ILO circuit, under similar conditions, is simulated in the Cadence Spectre^{TM}environment, the behavior of the frequency transient was very similar to the theory developed here, for the different values of $\phi(0)$ applied (Fig. 4.7a). However, the maximum (or minimum, depending upon the transient) instantaneous frequency

attained for a particular transient varies with $\phi(0)$. Among all the different traces in the two plots, we note that $\phi(0) = (-\pi/6)$ takes the shortest time to settle, whereas, $\phi(0) = 7\pi/6$ exhibits the longest settling time. The following theoretical predictions from eqn. 4.2 made earlier are validated in Fig. 4.7a.

- Lock-times are lower if $\phi(0)$ lies in the range $[-\pi/2, \pi/2]$.
- The oscillator frequency jumps from ω_0 to $\omega(0+)$ at $t = 0$.
- For $\phi(0) = \phi_{ss}$ and $(\pi - \phi_{ss})$, the oscillator frequency jumps instantaneously to ω_{inj} at $t = 0$. For $\phi(0) = \phi_{ss}$, the frequency settles instantaneously, but for $\phi(0) = (\pi - \phi_{ss})$, the frequency goes through a long transient (slowest locking).



(a) Frequency transient (Theory)

(b) Frequency jump at $t = 0+$

Figure 4.5: Transient behavior of the ILO instantaneous frequency for different values of initial phase $\phi(0)$ under the following conditions: $\omega_0 = 3.5428$ GHz, $\omega_{inj} = 3.5644$ GHz, $\omega_L = 54.2$ MHz. All the critical frequencies and frequency-limits have been marked in the plots.

Even though Figs. 4.5a and 4.7a are in excellent agreement in shape, there is a clear discrepancy in the maximum (or minimum) value attained by the oscillator frequency during settling. According to the theory, this maximum (or minimum) frequency is the

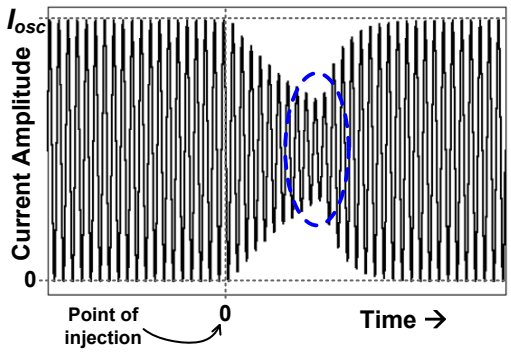
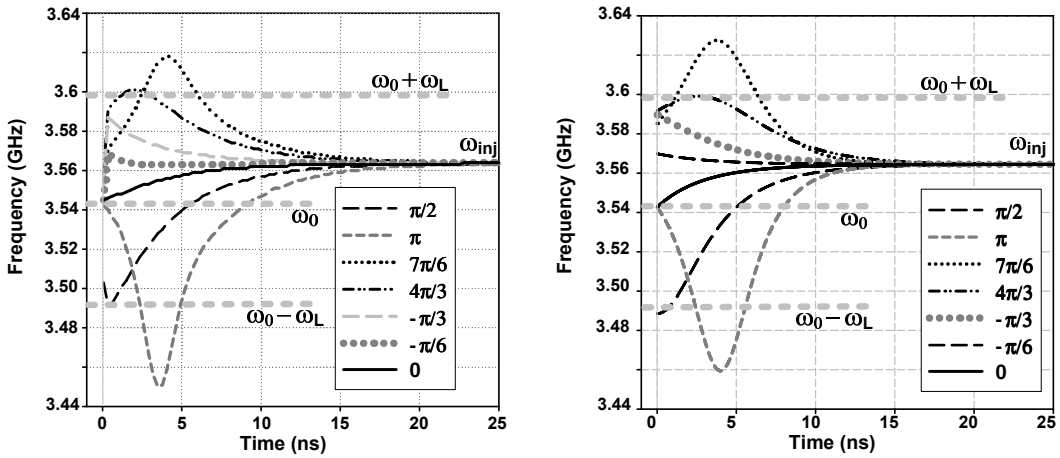


Figure 4.6: I_{osc} transient for $(\phi(0) = \pi - \phi_{ss})$



(a) Spectre^{TM} simulation

(b) Theory (corrected)

Figure 4.7: Simulated and theoretical (after first-order correction) frequency transient for an LC-oscillator-based ILO with following properties: $\omega_0 = 3.5428$ GHz, $\omega_{inj} = 3.5644$ GHz, $\omega_L = 54.2$ MHz

edge of the lock-range of the ILO. But this frequency shows a strong relationship to the initial phase, $\phi(0)$. The reason behind this behavior can be explained by looking at the current flowing through the oscillator during this transient. Adler's ILO analysis assumes a constant oscillator current [17]. But in a real oscillator (due to non-linear behavior), the oscillator current I_{osc} varies during the frequency transient. A representative plot

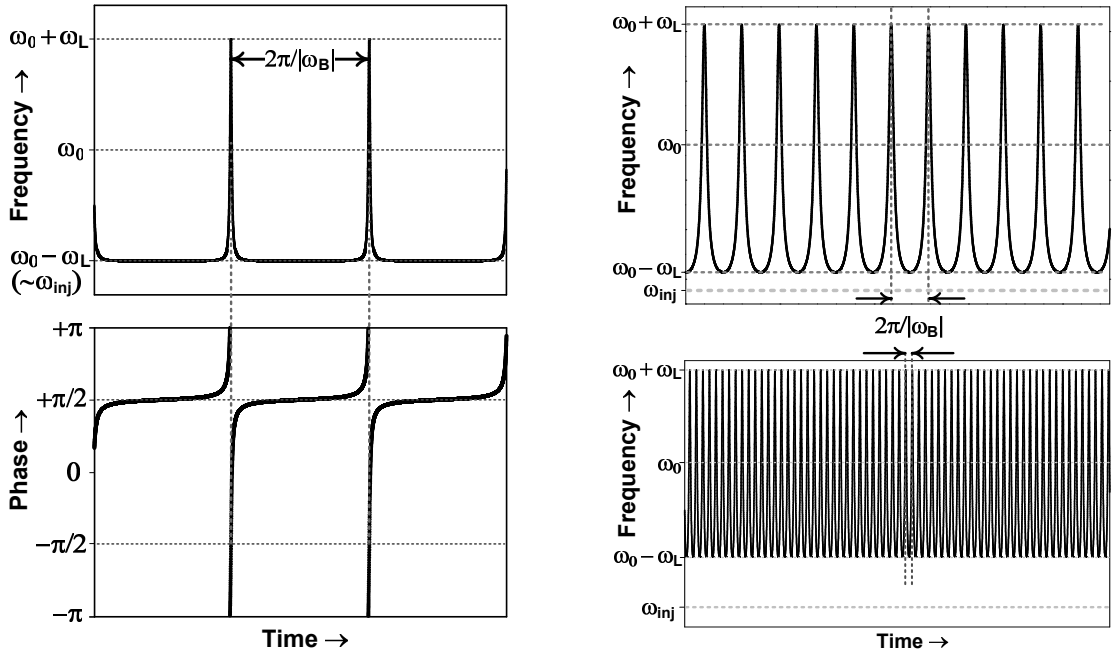
of the current through the oscillator for $\phi(0) = 7\pi/6$ (unstable equilibrium) is shown in Fig. 4.6. Since the oscillator current reduces significantly in the middle of the transient (demarcated in blue), the instantaneous lock-range of the ILO increases and hence, the maximum (or minimum) limit of the oscillator instantaneous frequency changes. On the other hand, for $\phi(0) = \pi/6$ (stable equilibrium), the change in oscillator current is negligible. By including a first-order correction for this $\phi(0)$-dependent behavior in the oscillator current in Adler's equation, the discrepancy can be minimized as can be seen from a comparison of Figs. 4.7a and 4.7b. However, alternately, higher-order models, which take the non-linear behavior of the oscillator into account, can be used [21].

The next section considers the acquisition and tracking behavior of injection-locked oscillator beyond the nominal lock range.

4.4 Lock Acquisition and Tracking

For most applications, an ILO is usually operated within its lock-range. However, there is some interesting behavior that can be observed when the ILO is at the edge or slightly beyond the edge of the lock-range. Such situations can occur in cases of significant LO-pulling [1]. In such cases, the injection signal could be some leakage from an adjacent channel and the local oscillator (LO) can get injection-locked. If the injection signal frequency is very close to the edge of lock-range of this 'parasitic' ILO, certain unwanted phenomena can occur. In this section, we illustrate the behavior of an ILO under such conditions.

Adler's equation (eqn. 4.1) does not assume that the injection-signal frequency is strictly within the lock-range of the ILO. Hence, the equation can be extended to frequencies slightly beyond the lock-range limits [1] (as long as it is ensured that the tank phase-frequency relationship is fairly linear). Depending upon how far the injection frequency is beyond the lock-range limits, the ILO can either be in quasi-lock or fast-



(a) Quasi-lock behavior for frequency and phase; quantified by $\omega_{inj} \rightarrow (\omega_0 - \omega_L)$

(b) Fast-beat frequency behavior as ω_{inj} moves away from $(\omega_0 - \omega_L)$ (two cases)

Figure 4.8: Frequency transient behavior of an *unlocked* ILO; $\omega_{inj} < (\omega_0 - \omega_L)$ [1]

beat state [1]. In the quasi-lock state, the injection frequency is very close to the edge of ILO lock-range. The oscillator, for the most part, oscillates at the frequency ω_{inj} (actually it oscillates at the frequency equal to the nearest edge of lock-range) and periodically (period $= 2\pi/|\omega_B|$, where ω_B is expressed in eqn. 4.4) exhibits phase-slip (Fig. 4.8a). In this representative graph, the injection signal frequency (ω_{inj}) is slightly below the lower edge of the lock range. The ILO remains at the lower edge of the lock range, i.e., $(\omega_0 - \omega_L)$. There is phase accumulation between the injection signal and the ILO output because of this frequency mismatch. The phase difference, $\phi(t)$, predominantly stays at $\pi/2$ (steady-state phase), but when the accumulated phase pushes it to $3\pi/2(= -\pi/2)$, the oscillator exhibits a phase slip, as illustrated in Fig. 4.8a. The rate of phase accumulation varies between $(\omega_0 - \omega_L - \omega_{inj})$ and $(\omega_0 + \omega_L - \omega_{inj})$ and the

average rate of phase accumulation is given by the geometric mean of these two extremes $\sqrt{(\omega_0 - \omega_{inj})^2 - \omega_L^2} = |\omega_B|$. Therefore, the beat frequency of this phase slip is given by $(|\omega_B|/2\pi)$. On the other hand, in the fast-beat state, the injection frequency is relatively farther away from the edge of ILO lock-range. In this state, the oscillator's frequency varies continuously and periodically (period=$2\pi/|\omega_B|$) as shown in Fig. 4.8b. When the injection frequency is significantly away from the lock-range, the oscillator spends almost equal time at $(\omega_0 - \omega_L)$ and $(\omega_0 + \omega_L)$, with the time-averaged frequency close to ω_0 (*quasi* free-running condition). For this case, the beat frequency can be well approximated by $(\omega_0 - \omega_{inj})$ - the difference between the injection frequency and oscillator's center frequency. In other words, ω_L loses significance.

4.5 Chapter Summary

This chapter has presented an extensive study of the transient behavior of oscillators under injection. Adler's equation was used as the basis of the study and some interesting and insightful aspects of the locking process of an ILO were derived. The trajectory of phase and frequency settling were theoretically established and their dependence on parameters like lock-range and initial phase of injection were identified. The behavior of the ILO when the injection is outside the lock-range is then presented. This study is relevant to cases where the frequency of a VCO (part of the frequency synthesizer in a system) is pulled by an *aggressor* signal of proximal frequency. Two regions - quasi-lock and fast-beat were analyzed by extending Adler's equation to this region. The beat frequency and the correct limits of ILO frequency jump during the beat were identified. On the basis of the in-depth understanding developed, it is shown that the locking time of an ILO is a strong function of lock range and the initial phase of injection.

Chapter 5

Fast-Hopping Frequency Synthesis

The use of fast-hopping frequency synthesis is well-known in the area of frequency hopped spread spectrum (FHSS) systems. FHSS offers advantages like high resistance to narrow-band interference (most of the conventional standards are narrow-band) and secure communication. Such qualities make this an attractive scheme for military applications. The WiMedia specification for ultra-wideband (UWB) presents another scheme that uses fast-frequency hopping. This scheme combines Orthogonal Frequency-Division Multiplexing (OFDM) with frequency-hopping for robustness against interference and multi-path fading. Also, this is used for multiple access. In all the schemes where frequency-hopping is required, one of the important specification is frequency-hop time of the carrier. In case of WiMedia-UWB the hop time is 9.5 ns. This is a very stringent constraint on the synthesizer in recent times. For the rest of the chapter, this specification will be taken as the test vehicle and several techniques will be compared and contrasted. Injection locking will be presented as a viable and attractive technique for fast hopping frequency synthesis.

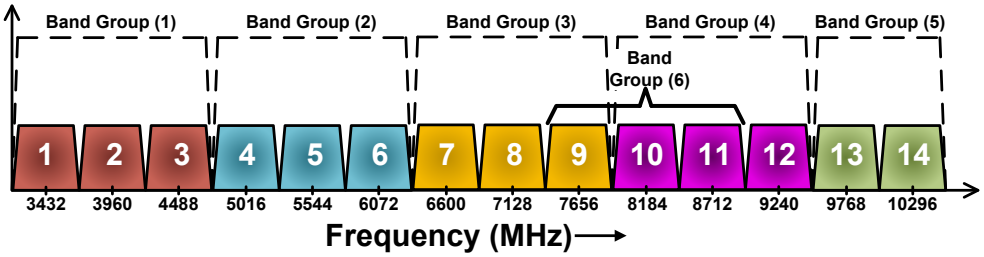


Figure 5.1: Wimedia UWB band structure

5.1 WiMedia-UWB System Overview

In 2002, the FCC opened up unlicensed spectrum between 3.1 to 10 GHz for UWB communication applications. The WiMedia standard for UWB divides the available spectrum into 14 sub-bands of 528 MHz each (Fig. 5.1), bracketing three sub-bands into a band-group, except for the last band-group which consists of two sub-bands. Each sub-band consists of 128 sub-channels which employ QPSK modulation. Band-group(1) constitutes Mode-1 and is mandatory for first generation devices. Other bands are envisioned for high-end products. It is worth noting that the center frequencies of the bands are odd multiples of 264 MHz. A pseudo-random hopping scheme, in order to achieve efficient and robust communication, is applied to hop across the carrier frequencies. In this scheme, the frequency is switched at the end of each OFDM symbol which has a duration of 312.5 ns. The band switching must occur within 9.5 ns. Conventional PLL designs fail to provide such fast-settling times. This is primarily because the bandwidth requirement for such settling times is large but in a typical charge-pump-based PLL (CPPLL), due to stability issues, the loop bandwidth is constrained by the input reference frequency (f_{ref}) to be approximate $f_{ref}/10$ [11]. Several alternative structures have been proposed to achieve the required band switching times and will be discussed in the next section.

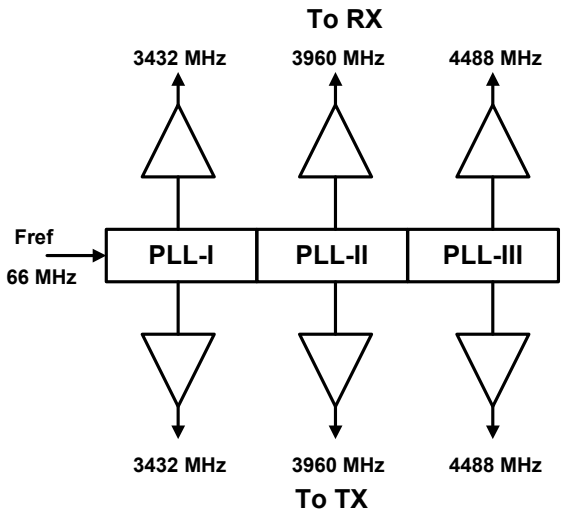


Figure 5.2: UWB Synthesizer: one PLL per band

5.2 Proposed Architectures for UWB

PLL-Based Architectures: Almost all the proposed architectures for WiMedia-UWB frequency synthesis use multiple PLLs or a combination of multiple PLLs and single sideband mixers (SSB mixers). The architecture shown in Fig. 5.2 uses three fixed-modulus PLLs to generate the required frequencies of band-group(1). Each PLL uses a ring oscillator and so occupies a low area per PLL. But using a PLL-per-band which run simultaneously is a power-hungry solution. Extending this scheme to higher bands becomes more expensive since implementing ring oscillators at higher frequencies is non-trivial. Moreover, since all the PLLs are always running, any feed-through form other PLLs appear as spurs and good isolation is needed for good spur suppression.

Fig. 5.3 shows an alternative scheme which uses a combination of PLLs and SSB mixers. This architecture generates center frequencies for 7 bands [51]. It uses a group-PLL and band-PLL, which is less number of PLLs compared to the first scheme. A tri-mode buffer generates the required mixing frequency or DC and an SSB mixer is used to generate the output. It is a simple scheme that uses minimum number of SSB

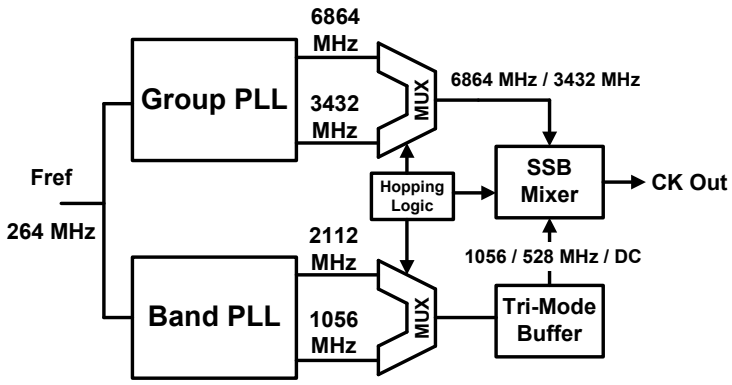


Figure 5.3: PLLs and SB mixers for UWB frequency synthesis

mixers. Also, it can be extended easily to other bands by extending the range of the band-PLL or using more of them. But the use of SSB mixers entails several drawbacks. One port of the mixer needs to be extremely linear to avoid generation of spurious tones. This can be achieved by degeneration but this increases power consumption. They also use band-pass loads which increase the occupied area. SSB mixer spurious performance also depends upon quadrature (I/Q) accuracy at its input. Any amplitude or phase mismatch leads to worse spurious performance. Also, care needs to be taken to avoid generation of harmonics of the band-PLL. These when mixed with group-PLL output generate spurs in the other bands of the UWB spectrum.

Shown in Fig. 5.4 is a variation of the above architecture [52]. It uses two PLLs and SSB mixers. Here the required quadrature inputs to the mixers are generated by a divide-by-2 ciruit after the VCO, which now needs to run at twice the required frequency. This leads to a higher power consumption. All the issues with the SSB mixers are also present in this architecture.

Single PLL based UWB frequency synthesizers are also proposed in [53, 54]. They are based on one PLL and SSB mixing. The suitable second frequency for the mixer is generated by proper division and signal conditioning of the VCO frequency. In [53] a divide-by-1.5 circuit is used. An additional signal conditioning is needed to generate the

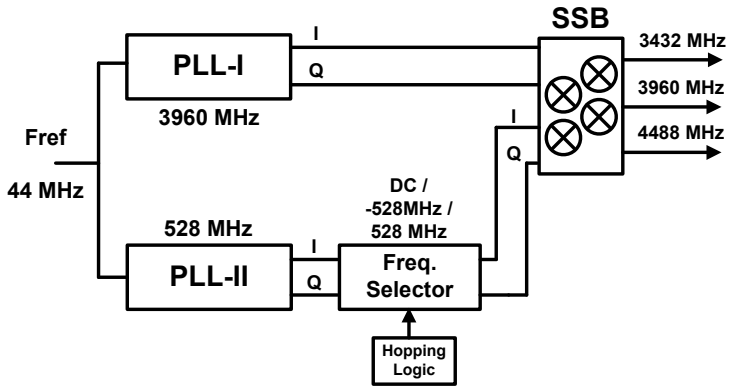


Figure 5.4: Alternative structure with PLLs and SSB mixers for UWB frequency synthesis

required quadrature imputs for the SSB mixer. As alluded to earlier, any mismatches in the I and Q signals will lead to spurious tones. Also this architecture is not easily extendable to higher bands. In [54] a multiply-by-1.5 circuit is required. This is generated by properly combining multiple phases of the VCO signal. Care has to be taken in this case also to ensure good quadrature accuracy and 50% duty cycle.

Non-PLL Based Architectures: Though PLL-based systems are very popular, there are other architectures that exploit other frequency generation techniques. In [55], a DLL-based frequency synthesizer is proposed for UWB applications. DLLs are first-order systems and so their bandwidth can be increased without sacrificing stability. By choosing a very wide bandwidth settling times can be made extremely small. The architecture is based on a static 528 MHz PLL and a multiplying DLL. Frequency switching is accomplished by choosing a different length voltage-controlled delay-line (VCDL) each time. The primary disadvantage in a conventional DLL structure is the behavior at the switching instance. Any glitches should be avoided to reduce lock time. The proposed architecture uses separate PFD-CP combination for each switching combination which increases power consumption. The edge-combiner is a critical part of the design. It uses

switched LC-tank load to convert combined current to voltage. Higher tank Q is required to increase the voltage swing at the output but that will increase settling time when the tank is switched. Further, extension of this architecture to higher bands increase power consumption.

Direct digital synthesis (DDS) is another frequency synthesis technique (discussed in Section 2.4) that is capable of extremely fast hopping. This can be used as the LO generation circuit in WiMedia-UWB-compliant transceiver [56]. The difficulty of generating very high frequencies with DDS have already been discussed in 2.4. This is obvious in the implementation in [56]. Since the highest frequency in a conventional DDS is limited by the input frequency, a very high frequency PLL (8.448 GHz) is used as the input. It should be noted that such high frequency is required to generate just the first 3-bands of the UWB spectrum. Extension to subsequent bands requires higher frequency PLL. Digital circuits (ROM, DAC) operating at such frequencies consume exorbitant amount of power. That is precisely the reason why the frequency synthesizer in [56] is the main culprit in terms of power consumption. Here the main problem is the implementation of high-frequency DDS.

As seen in this section several techniques have been proposed for fast-hopping frequency generation. Each is associated with its own set of issues but mainly issues with power consumption and extension to higher bands appear to be the common theme among all of the implementations. In the next two sections, the technique and architecture for WiMedia-UWB-compliant synthesizer and high-frequency DDS based on injection locking are presented.

5.3 Fast-Hopping Using Injection Locking

In Chapter 4, a complete understanding of the transient behavior of an injection-locked oscillator has been established. It was shown that ILOs behave as a first-order PLL and

the settling time shows a strong dependence on lock-range of the ILO and initial phase difference between the injected and oscillator signal. Based on this understanding, two conditions for fast settling of ILOs can now be proposed.

5.3.1 Lock-Range Dependent Fast-Hopping

It is clear from eqn. 4.6 that the lock-time strongly depends upon ω_B, expressed in eqn. 4.4. Adler's equation is further simplified by linearizing assumptions and eqns. 4.8 and 4.9 are obtained. These equations show that the behavior is similar to a first-order PLL. The settling behavior is strictly exponential with a time-constant $\tau = (1/\omega_L)$. Assuming 5τ ($\sim 99\%$) settling, the lock-time can now be approximated by

$$t_{lock} \approx \frac{5}{\omega_L} \tag{5.1}$$

for the given conditions. The first condition, requiring ω_0 to be in the proximity of ω_{inj}, can be attained through calibration. But the lock-time also depends upon the initial phase $\phi(0)$ and though possible, it is non-trivial to ensure that $\phi(0) \ll 1$(radian). In order to develop a more robust design constraint, we need to analyze eqn. 4.6 further. The equation can be expressed in terms of $\phi(t)$ as

$$\tan\left(\frac{\phi(t)}{2}\right) = \frac{\tan\left(\frac{\phi_{ss}}{2}\right) - K_0 \cot\left(\frac{\phi_{ss}}{2}\right) e^{-\omega_B t}}{1 - K_0 e^{-\omega_B t}} \tag{5.2}$$

where K_0 is given by:

$$K_0 = \frac{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}$$

So using eqn. 5.2 for the more general case (without the two conditions expressed earlier), the time-constant for exponential settling is now given by $\tau = (1/\omega_B)$. The mathematical quantity ω_B can be approximated by the real lock range ω_L (with a maximum margin of error $\sim 13\%$) as long as the injection frequency (ω_{inj}) lies in the range $[\omega_0 - 0.5\omega_L, \omega_0 + 0.5\omega_L]$, i.e., injection is done close to natural frequency of the oscillator, ω_0. The phase

noise of an ILO approaches that of the stand-alone oscillator if the injection frequency is in the vicinity of the edge of lock-range. So restricting the injection frequency range to the interval $[\omega_0 - 0.5\omega_L, \omega_0 + 0.5\omega_L]$ also ensures that the phase noise of the ILO output is close to that of the clean injection signal. Furthermore, as long as the initial phase is away from $\pi - \phi_{ss}$ (the unstable phase point), the quantity K_0 does not attain a large value. For these less restrictive conditions too, the lock-time can still be expressed by eqn. 5.1.

To get an idea of the typical lock range required, we consider the WiMedia-UWB standard [57], where the frequency synthesizer needs to hop to a new frequency and settle within 9.5ns. According to calculations using eqns. 5.1 and 5.2, the required lock-range is ~ 80 MHz and by taking into account, the error margin of about $\sim 13\%$, this required lock-range increases to ~ 90 MHz. In Section 6.2, we verify these predictions for lock-times through experimental measurements on a fabricated prototype. So we conclude that in order to design fast-locking ILO systems without restrictions on the initial phase at $t = 0$, the lock-range should be sufficiently large and that eqn. 5.1 can be used to obtain a close estimate of the lock-time.

5.3.2 Predictive Fast-Hopping

Obtaining large lock ranges might not be possible in applications where the injection signal is not very strong. For example, in case of sub-harmonic injection locking where the oscillator locks onto a harmonic of the injected signal, the injection power goes down as the harmonic number goes up. Also as shown [58] using a large lock-range to attain fast-lock times can reduce the spur suppression characteristics of an ILO in the case of sub-harmonic injection-locking. So there is a clear trade-off between lock-range and spur suppression of an ILO. The strong dependence of lock-time on the initial phase can also be exploited to obtain fast lock-times. As illustrated in Section 4.3, for $\phi(0) = \phi_{ss}$ the locking is instantaneous and this is independent of ω_L. This technique could be used to

attain fast-lock times without compromising the spur suppression properties.

It is non-trivial to precisely control the initial phase-difference between the injected and oscillator signals. But here we propose a novel technique to achieve the same. Most fast-hopping systems require the ILO to jump from one locked-state to another. Since, as discussed in Chapter 4, the phase of an ILO cannot change instantaneously at the point of frequency switch, the steady-state phase of the present frequency becomes the initial phase for the next frequency jump. Assuming $t = 0$ as the time of a particular frequency step, this condition can be formulated as

$$\phi(0+) = \phi_{ss}|_{t=0-}$$

If the steady-state phases of the frequencies on either side of the switch are matched ($\phi_{ss}|_{t=0+} = \phi_{ss}|_{t=0-}$), then the locking would be instantaneous. The condition required for this to occur can be expressed as

$$\frac{\omega_{0,present} - \omega_{inj,present}}{\omega_{L,present}} = \frac{\omega_{0,next} - \omega_{inj,next}}{\omega_{L,next}} \tag{5.3}$$

Though the first initial phase of injection can not be precisely controlled, each of the frequency quantities in eqn. 5.3 can be externally calibrated. In the next section, we verify these two techniques through simulation and prototype-chip measurements.

5.4 ILO-Based Fast-Hopping Synthesizer

5.4.1 UWB/Wireless-USB Architecture

We have discussed locking an LC-oscillator to a single tone input. However, when a multi-tone input is injected, the oscillator locks to the tone which is within the lock-range and has the highest strength. One example of this is when a square wave is applied to an LC-oscillator, it typically locks onto the nearest harmonic that is within its lock range. This is called sub-harmonic injection-locking. The oscillator locks to the

requisite harmonic and suppresses all the other harmonics/components. The amount of suppression depends on how far the tone is from the oscillator center frequency.

The block diagram of the proposed WiMedia/Wireless-USB-compliant UWB frequency synthesizer architecture based on sub-harmonic injection-locking is shown in Fig. 5.5. Its operating principle lies in the fact that the center frequencies of the UWB bands are all odd harmonics of 264 MHz. Hence, a square wave of 264 MHz would contain all these UWB center frequencies. We propose the architecture for the first band-group (3432, 3960 and 4488 MHz). These components of the 264 MHz square wave would have 1/13, 1/15 and 1/17 amplitude of the fundamental, respectively. If a digitally-controlled local oscillator (DCO) can be designed to switch frequencies close to the three appropriate harmonic frequencies, the oscillator can be locked to the exact frequency by injecting a precise 264 MHz square-wave generated through a PLL or a crystal oscillator, followed by a hard-limiter.

Clearly, the oscillator's slowest lock time should be less than 9.5ns to meet the MBOA specification. In Chapters 6 and 8, we discuss design techniques to achieve this fast lock-time. Additionally, to limit reciprocal mixing, the out-of-band spurs should be sufficiently suppressed. If the suppression is less than the required specification, a cascade of ILOs can be used to attain higher suppression. However, this comes at the cost of additional lock-time (all the ILOs in the cascade have to be locked fast). Alternately, a band-pass filter can be used before the ILO to suppress the unwanted tones.

5.4.2 DDS Architecture

To increase the applicability of DDS, the frequency range needs to be extended. Using the DDS as a reference to a PLL is a straight-forward solution, but it has all the issues associated with analog PLLs. Alternately, up-conversion of the output from a low-frequency DDS, as in [2], using doublers and mixers can be used to generate wireless frequencies. An illustration is shown in Fig. 5.6. The additional circuitry consumes a

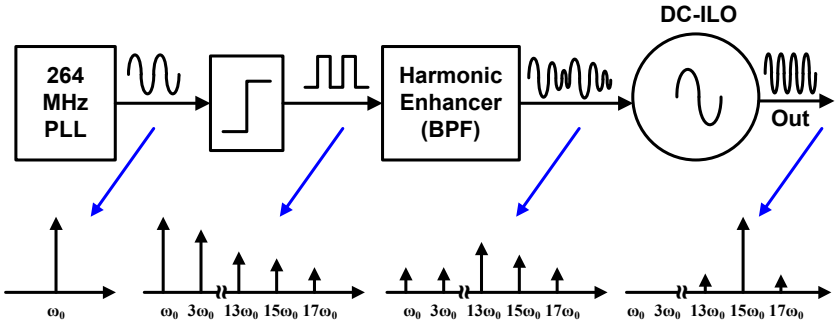


Figure 5.5: Simplified block diagram for proposed UWB frequency synthesizer

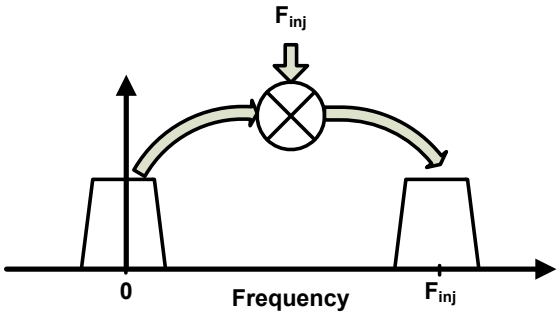


Figure 5.6: Mixer-based up-conversion technique for HF-DDS [2]

lot of power and the multiplication leads to increased phase noise. Moreover, this is also a very narrow band design and the distinct advantage of DDS agility is lost. Another solution is to generate higher harmonics of the fundamental signal and filter the required harmonic using some form of passive bandpass filtering to get the desired output. The power consumption associated with this technique can be made to be very low but requires very high quality factor (Q) filters to suppress the other undesired harmonics of the fundamental. Unfortunately, a filter output settles in approximately Q cycles of an input step change. Therefore, obtaining both fast settling and good spur suppression is difficult to achieve using high Q filters.

The proposed architecture is based on a low-frequency DDS and harmonic injection-locking of a digitally-controlled oscillator (DCO). The block diagram is shown in Fig. 5.7. An injection-locked oscillator behaves like a first-order PLL and generates the required

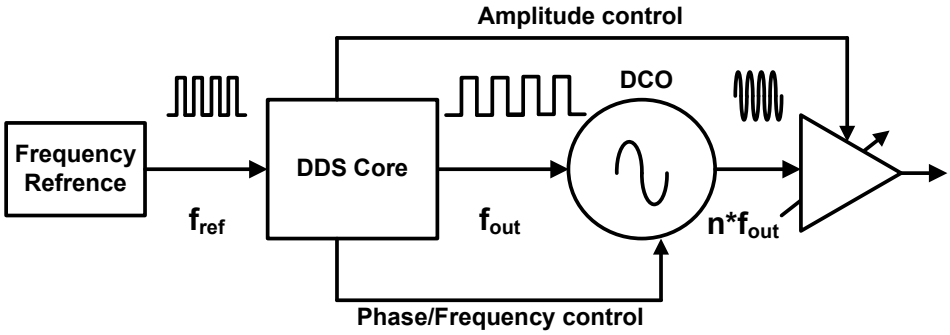


Figure 5.7: High-frequency direct digital synthesizer (HF-DDS)

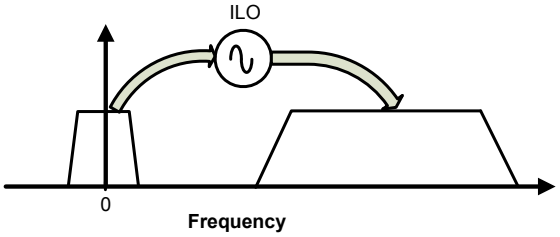


Figure 5.8: Up-conversion based on injection locking

high-frequency output by locking onto a harmonic of the injected (reference) signal. The DDS core can be programmed to generate multi-tone signals, the simplest of which is a square wave. The digitally-controlled oscillator (DCO) is digitally tuned close to the required harmonic of the multi-tone signal. If sufficient signal power exists at the harmonic, injection locking occurs. A proper choice of the digital word from the DDS core controls the intrinsic frequency of the DCO. A DCO with a wide tuning range [59,60] can be used to lock onto harmonics of a low-frequency DDS signal, thereby making the overall design fairly wide-band. This is illustrated in Fig. 5.8.

The critical constraint on this architecture is to retain the agility of the DDS. The lock time of the ILO is therefore the bottleneck that decides the agility of the entire circuit. In this architecture, the lock time is minimized by exploiting its phase dependence. Consider the case where a DCO with free running frequency ω_{01} is locked on to ω_{inj1} and is abruptly switched to ω_{02} to lock onto ω_{inj2}. The corresponding steady state phase

are given by eqn. 5.4, where ω_{L1} and ω_{L2} are the respective lock ranges. Since the DCO is locked onto the DDS signal, at the instance of the switch, ϕ_{ss1} becomes the initial phase of injection, $\phi(0)$, for the next frequency. If ϕ_{ss2} can be made close to ϕ_{ss1} almost instantaneous locking is achieved. Also, since there is little phase settling, the frequency switch is nearly *phase continuous*. This can be accomplished by a proper choice of ω_{02} such that $\frac{\omega_{02}-\omega_{inj2}}{\omega_{L2}} \approx \frac{\omega_{01}-\omega_{inj1}}{\omega_{L1}}$. The two ratios may not be exactly equal, but if one can remain in the fast lock regions (marked by triangles in Fig. 4.4a), the lock times are very small for all practical purposes. This is repeatable from one locked frequency to another except at the startup when the initial phase difference between the signals is not known.

One issue with ILO-based high-frequency direct-digital synthesis is the lack of variable amplitude. The amplitude control block, shown in Fig. 5.7 adds this feature to the architecture.

$$\phi_{ss1} = \sin^{-1}\left(\frac{\omega_{01}-\omega_{inj1}}{\omega_{L1}}\right) \quad \phi_{ss2} = \sin^{-1}\left(\frac{\omega_{02}-\omega_{inj2}}{\omega_{L2}}\right) \tag{5.4}$$

5.5 Spur Suppression

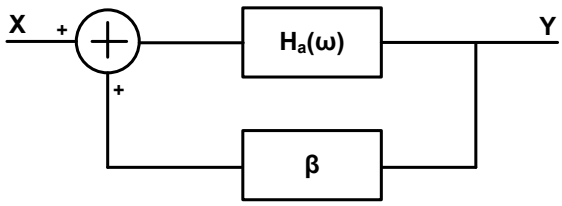


Figure 5.9: ILO modeled as regenerative amplifier

Both the architectures presented above use sub-harmonic injection locking in ILOs. This imposes another constraint on these synthesizers: out-of-band spur suppression. It is extremely difficult to precisely model out-of-band spur behavior in a non-linear system like an ILO. A method to estimate the sidebands in case of unlocked oscillators was presented in Chapter 3. This cannot be directly applied in this case since the

oscillator is already locked to another external signal. Here we present a simple linear analysis that estimates the worst-case spurs in the presence of a locked signal.

In this linearized analysis, the ILO is modeled as a regenerative amplifier. Regenerative amplifiers are positive feed-back systems on the verge of oscillation. Shown in Fig. 5.9 is the model for a positive feedback system. The transfer function of such a system is given by

$$H_R(\omega) = \frac{Y}{X} = \frac{H_a(\omega)}{1 - \beta H_a(\omega)} \tag{5.5}$$

In eqn. 5.5, if the loop gain $\beta H_a(\omega_0) = 1$, then the system oscillates at the free-running frequency of ω_0. In regenerative amplifiers, however, the loop gain is made very close but not equal to one at the required frequency to achieve a very high gain. Let us now approximate the oscillator as a regenerative amplifier to do a linearized spur suppression analysis. In this case,

$$H_a(\omega) = \frac{j\omega\left(\frac{\omega_0}{Q}\right)}{\omega_0^2 + \left(j\omega\frac{\omega_0}{Q}\right) + (j\omega)^2} \tag{5.6}$$

which represents the parallel RLC tank transfer function with center frequency of ω_0 and a quality factor Q. Using $\beta H_a(\omega_0) = 0.999$, we can now compare the simple tank transfer function to the regenerated transfer function as shown in Fig. 5.10. Note here that the gain of the regenerated tank depends on closeness of the open-loop gain to unity.

In order to calculate the spur suppression, the output amplitude is normalized and also hard-limited to emulate the oscillator output voltage saturation. This transfer function can now be plotted for various input levels as shown in Fig. 5.11. In Fig. 5.11, the output is plotted for two different input levels. As the input level is increased the amount of suppression achieved at frequencies away for the center frequency goes down. To test the accuracy of the model developed, it is compared against the simulation result for an ILO shown in Fig. 5.12. The ILO is designed for a center frequency of 3.4 GHz with a tank Q of 6. A two-tone current injection signal, with one tone close to the center frequency and the second tone at an offset of 528 MHz is applied to the ILO. The ILO

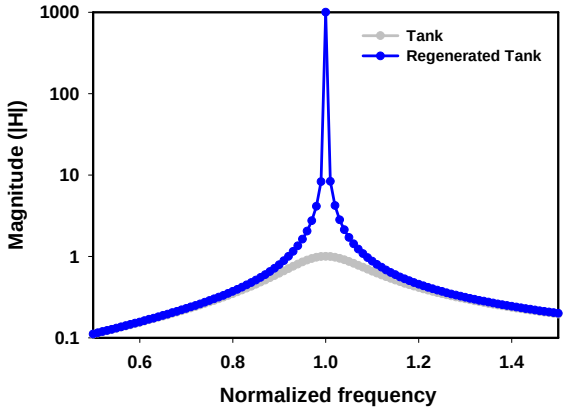


Figure 5.10: Regenerated tank characteristic

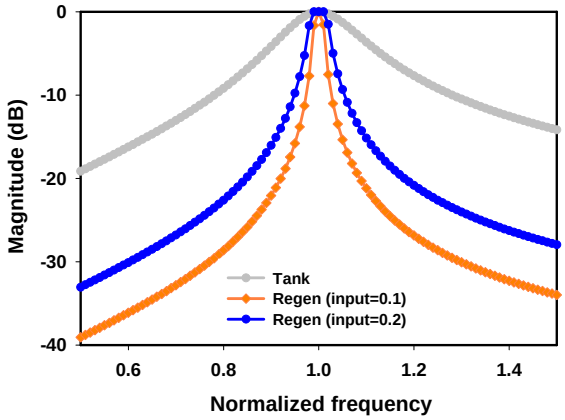


Figure 5.11: Theoretical estimation of spurs

locks onto one tone and the second tone appears as a spur. The suppression of this spur relative to the locked ILO amplitude is plotted in Fig. 5.13.

The result in Fig. 5.13 shows that the simplified model presented here is pessimistic in the spur calculation and the ILO achieves higher suppression. This model in a sense estimates the worst case spurs. There are two obvious reasons for this

- The model is a linear model in which the gain of the signal around the center frequency is hard limited whereas the spur undergoes a linear gain. In practice both the signals undergo a non-linear gain which is non-trivial to estimate particularly

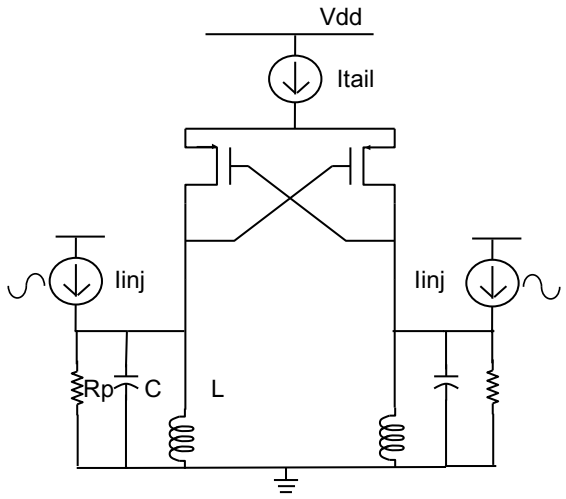


Figure 5.12: ILO schematic

using a linear analysis.

- The limiting of the output amplitude for various input levels to the same value is consistent with our assumptions in the derivation of Alder's equation for ILOs but in ILO simulation, the output amplitude increases sightly with increase in injection signal strength. This is evident in the plot as the $\frac{I_inj}{I_osc}$ is increased the discrepancy between the two curves increase.

However, this first order model gives a simple linearized analysis tool to estimate the spurs in an ILO in case of multi-tone injection.

5.6 Chapter Summary

Fast-hopping frequency synthesis techniques were investigated in this chapter. Existing architectures for frequency synthesizers that meet the WiMedia-UWB specifications were reviewed. Two techniques based on injection locking, lock range dependent fast locking and predictive fast locking, were then presented. ILOs behave as first-order PLLs and their bandwidth can be made very large without suffering from stability issues. This fact

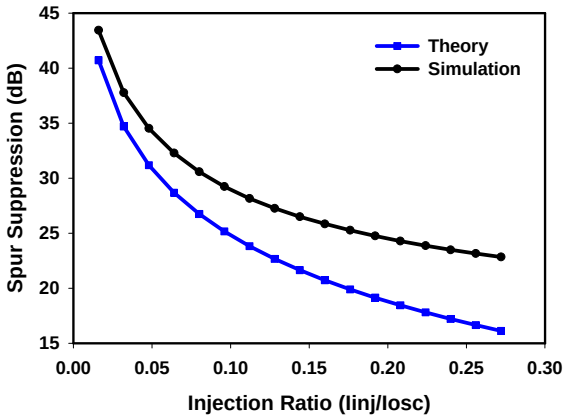


Figure 5.13: Spur suppression: model vs. simulation

is used in the first technique and the required lock-range for fast locking was estimated. Achieving large lock-ranges is not always possible. The second technique addresses this issue by exploiting the phase dependence of lock-time in ILOs. Two architectures, one for frequency synthesis meeting WiMedia-UWB specification and the second to extend the frequency of operation of a direct digital synthesizer, are presented. Finally, since both the architectures are based on sub-harmonic injection-locking, multiple tones are present in the system. Spur suppression becomes another constraint in these architectures. A simple linearized model is presented to estimate the spur suppression in ILOs.

Chapter 6

Experimental Verification of Theory

In order to experimentally verify behavior and performance of ILOs, two different circuits are discussed. The circuits chosen are two different oscillators, a discrete Colpitts oscillator and an on-chip PMOS-only LC-oscillator. This also shows that the theory does not depend on the topology of the oscillator used for injection locking. The only constraints: fast-reacting amplitude control mechanism and moderate tank Q [17]. Almost all the oscillator designs today meet these requirements. In this chapter, first a low-speed Colpitts oscillator is used to establish the out-of-lock time-domain behavior discussed in Section 4.4. Then spectrum measurements from a high-speed LC-oscillator are used to verify out-of-lock behavior in frequency domain and the spur suppression performance of an ILO in case of multi-tone injection (Section 5.4). Transient measurements of the same LC-oscillator prove the fast-locking capabilities discussed in Section 5.3.1. The architecture for high frequency DDS proposed in Section 5.4.2 is validated through simulation. This also proves the predictive fast-locking technique discussed in Section 5.3.2. A complete prototype that utilizes this technique will be shown in Chapter 8.

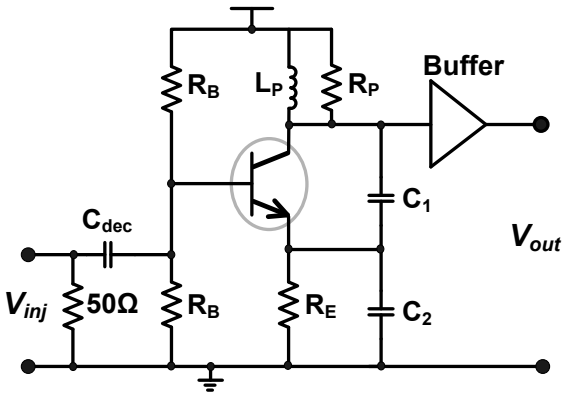


Figure 6.1: Colpitts ILO: simplified schematic

6.1 Low-Frequency Oscillator Measurement

A discrete Colpitts oscillator (Fig. 6.1) was assembled on a printed-circuit board. Table 6.1 details the specifications and the measured performance of the discrete oscillator. The transient output data was recorded on a digital storage oscilloscope (Agilent DSO8104), sampling at 4 GS/s. The choice of the center frequency was driven by the maximum DSO sampling rate available to us at that time. Band-pass filtering the extracted time-domain data in MATLAB removed the excessive out-of-band noise and then the cycle-to-cycle frequency was calculated from the zero crossings.

A sinusoid with a very slow frequency ramp (high to low) centered around the ω_0 was injected in to the oscillator to determine its lock range and out-of-lock behavior. The slow ramp (~ 0.08 MHz/μs - for theoretical worst-case settling time, frequency only changes by 128kHz) ensured that the oscillator frequency followed the frequency of the injection signal. Fig. 6.2 shows the DSO data with the ILO output (blue) and the ramp voltage controlling the input sweep (green). The region where the ILO acquires lock and tracks the frequency ramp is marked. Outside this region, the ILO is effectively unlocked. There is also a change in amplitude during the tracking phase. This is due to the change in the resonant impedance of the tank with output frequency. Fig. 6.3

Table 6.1: Colpitts oscillator measurements for -20dBm injected power

Center Frequency ($\omega_0/2\pi$)	57.312 MHz
Injection frequency ($\omega_{inj}/2\pi$)	57.495 MHz
Measured lock range ($\omega_L/2\pi$)	1.325 MHz
Theoretical worst case lock time (0.1% settling)	1.6 μs

shows the cycle-to-cycle frequency of the ILO as a function of input frequency. It clearly shows two distinct regions: tracking within the lock range and beat behavior outside the lock range. Far outside the lock range, the ILO exhibits fast beat (Fig.4.8b) gradually transiting in a continuum to quasi-lock (Fig. 4.8a) as the input approaches the lock range. Within the lock-range, the ILO output tracks the frequency ramp. Also, when $\omega_{inj} < \omega_0 - \omega_L$, the instantaneous output frequency is always greater than ω_{inj} and vice versa. These experimental results are in excellent agreement with the frequency transient theory and frequency-domain measurements demonstrated in [1].

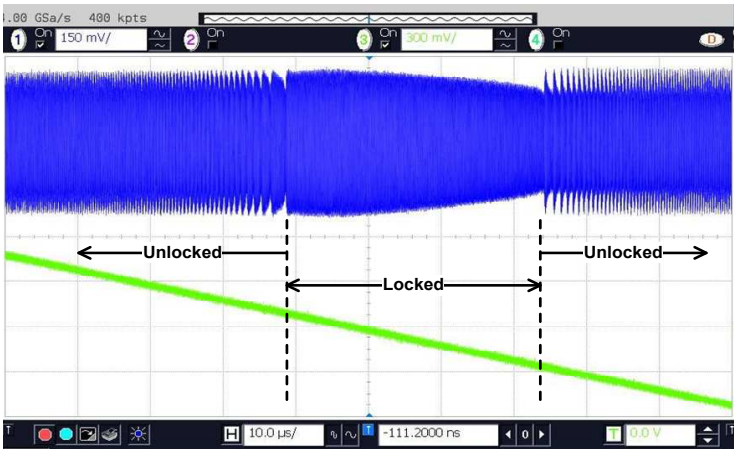


Figure 6.2: Measured ILO transient response sampled on a 4GS/s DSO for a slow frequency ramp input

To measure the frequency transient of the ILO, a frequency-shift keying (FSK) sig-

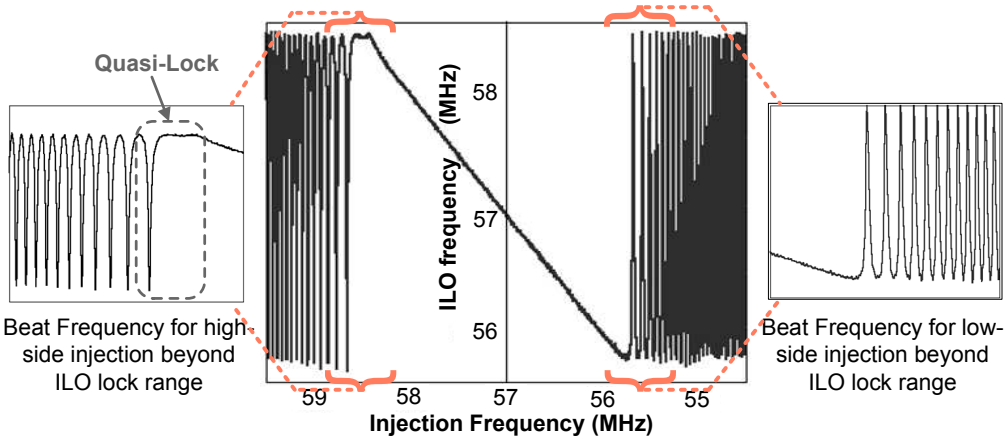


Figure 6.3: Measured ILO frequency behavior: frequency ramp

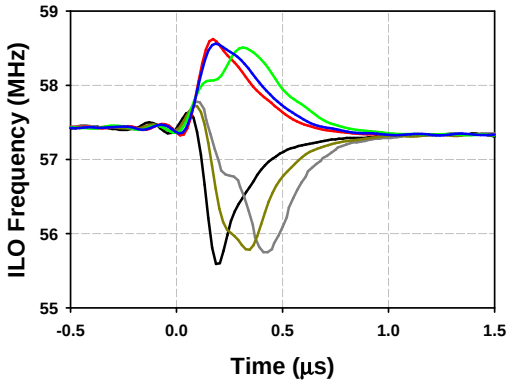
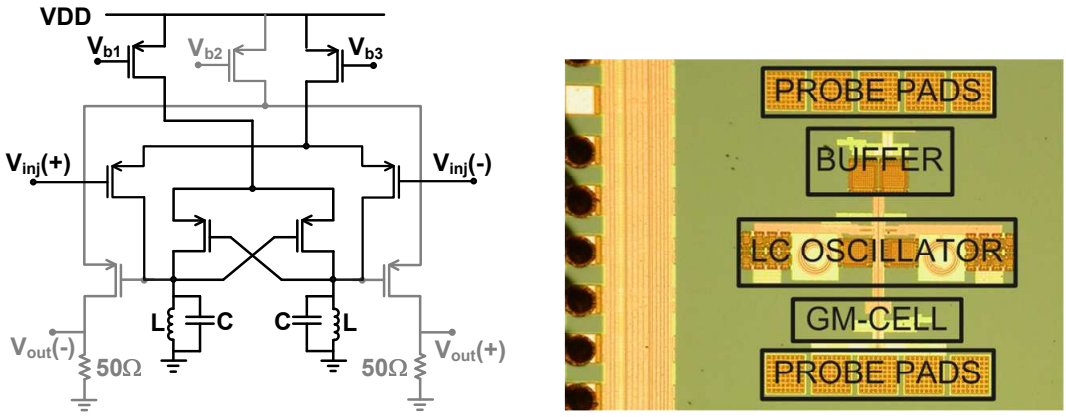


Figure 6.4: Measured frequency transients of the ILO for different FSK cycles

nal with a FM deviation of 10 MHz was applied. The FSK was setup so that one frequency occurred close to ω_0 (to ensure locking) and the other frequency occurred 10 MHz away (almost free-running), outside the lock range. The initial phase difference $\phi(0)$ is unknown in the measurement setup as the FSK signal was not synchronous with the modulated sinusoid, so the injection can occur at different $\phi(0)$ in each FSK cycle. Several cycles of FSK signal were used to obtain a range of different initial phases and the settling behavior is shown in Fig. 6.4. Quite clearly the settling behavior has the same shape and form as the other figures in Fig. 4.5, even if the time scales are different.

6.2 High-Frequency Prototype Measurement

To validate the rapid lock time capability of ILOs, a prototype design with PMOS-only negative-g_m oscillator, which uses an additional G_m-cell for signal injection and 50Ω output buffer, was designed and fabricated in a 0.13-μm RF-CMOS process. As mentioned earlier, the oscillator was designed to operate at a frequency of 3.3 GHz. The choice of frequency is based on the lowest frequency band of the WiMedia-UWB specification. Fig. 6.5 shows the complete circuit schematic and the die-micrograph.



(a) ILO Schematic

(b) Die Micrograph

Figure 6.5: ILO circuit schematic (LC-oscillator and G_m-cell shown in black and 50Ω output buffer shown in grey) and the fabricated prototype in $0.13-\mu$m CMOS process

The oscillator's natural frequency was measured to be 3.4 GHz. The total system (oscillator, g_m-cell and buffer) draws 18 mA of current from a 1.2 V supply. The area occupied by the entire circuit (including probe-pads, but excluding bias pads) is approximately 600×500 μm^2.

6.2.1 Measurement Setup

Spectrum Measurement Setup: To measure the spectrum of the ILO, a simple setup shown in Fig. 6.6 was used. The injection signal close to the fundamental frequency of

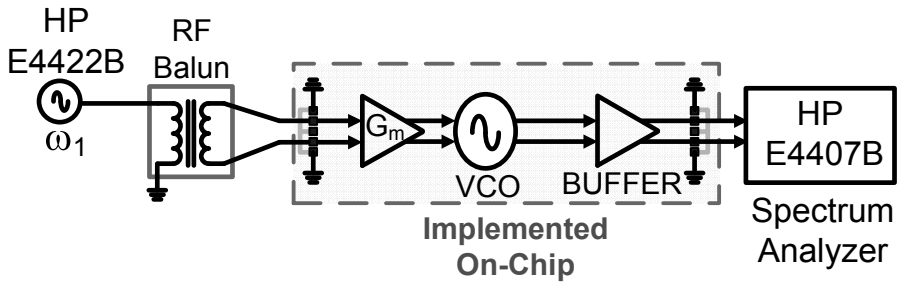
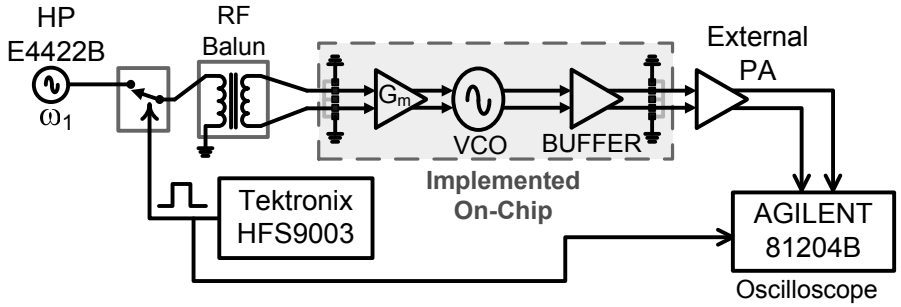


Figure 6.6: Test setup for spectrum measurement

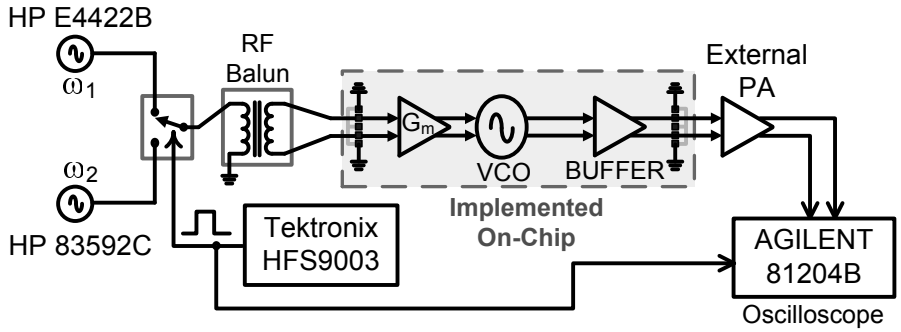
the free running oscillator was applied to the circuit through on-chip probes. The single ended input signal generated by a signal generator (HP E4422B) was converted to a differential signal using a wide band off-chip balun (Prodyne Tech. BIB-100G). The output was again probed out. The spectrum was observed using a HP E4407B spectrum analyzer.

Transient Measurement Setup: Two different scenarios were used to measure transient response and validate the necessary criterion described in Section 5.3.1 for lock-range dependent fast-locking. In the first case, Case I, the time required to move from unlocked (free running) state to locked state (lock acquisition) was tested. For Case II, the time required to hop between a one locked state to another locked state was tested. The latter was modeled by a frequency hop within the lock range of the ILO. The two separate test setups used to measure lock time for the two scenarios, described above, are shown in Fig. 6.7.

For Case I, the injection signal generated from an HP E4422B signal generator was switched OFF-ON (ASK) periodically (at a rate of a few MHz). This switched the ILO from unlocked to locked state and vice-versa. A wide-band SPDT RF switch (Mini-Circuits ZFSWA-2-46) generated the ASK signal. The high isolation between ON - OFF states of the switch ensured that the ILO was free running when the switch is OFF. The switch was controlled by a very fast rise/fall time ($<$ 200 ps) clock generated from a



(a) Case I



(b) Case II

Figure 6.7: Two test-setups used for measuring lock-range-dependent ILO lock-times

Tektronix HFS 9003 Stimulus System. Again a wide-band balun (Prodyne Tech. BIB-100G) converted the single-ended input to a differential (injection) signal for the ILO. The inputs and outputs were applied and measured, respectively, through GSGSG RF probes. Due to the 50Ω buffer and the additional signal losses in the path, the output signal strength was not sufficient for oscilloscope measurement. So, the output of the ILO was amplified using a power amplifier (Narda DBP-0206N533) and the transient data was recorded using a real-time digital storage oscilloscope (Agilent DSO81204B) operating at 40 GSa/s with a signal bandwidth of 12 GHz. For Case II, an additional signal source (HP 83592C) generated the second frequency and an FSK signal was generated by using two of the SPDT switches in complementary mode. Bandpass filtering the measured transient data removed any unwanted out-of-band noise, spurs and harmonics.

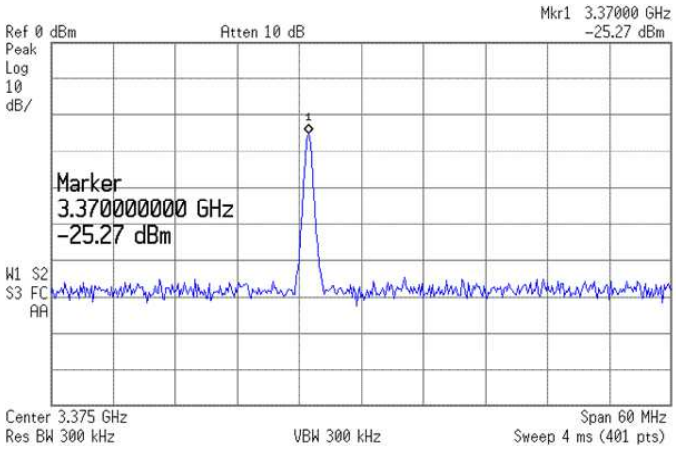
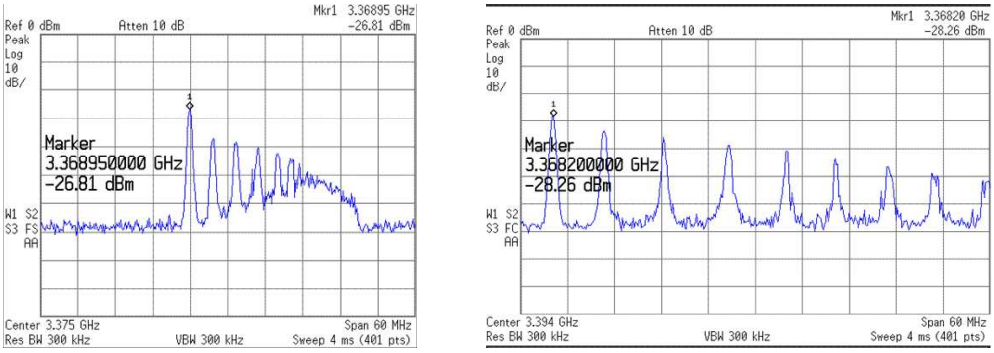


Figure 6.8: Locked ILO spectrum

Zero-crossings of the transient data were then used to calculate the period-to-period frequency. Since the output was sampled at a rate greater than five times the minimum Nyquist rate for the data, it allowed for both fine time resolution and accurate frequency estimation [61].

6.2.2 Spectrum Measurement Results

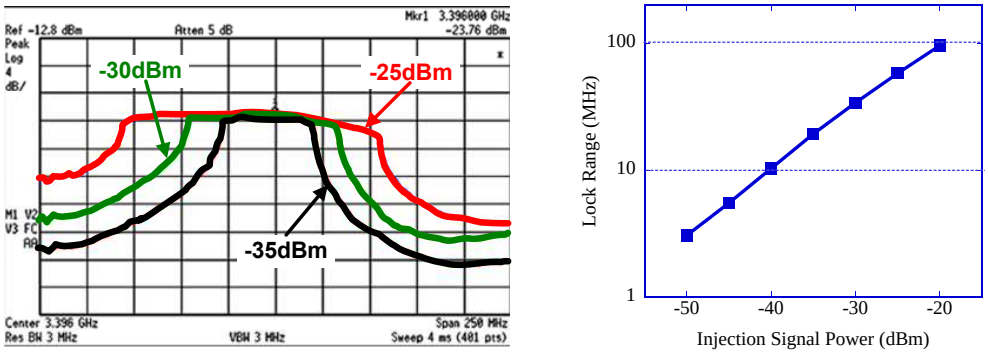
Fig. 6.8 shows the locked oscillator spectrum. The free running center oscillator frequency was first measured and the injection signal frequency was moved close to the measured frequency. To test the out-of-lock behavior of the ILO, the frequency of the input was reduced until it was less than the left lock edge of the ILO. Fig. 6.9a shows the ILO behavior when the input is just outside the lock range. The beat in this case frequency is small and the spurs are close to each other. It is worth noting that, as shown earlier, when the input frequency is to the left of the lock-edge, all the spurs appear to the right. If the input frequency is further reduced, the beat frequency increases and the spurs are spaced further apart (Fig. 6.9b). This verifies the behavior discussed in Chapter 3 and [1]. Also, this is the frequency domain version of the slow beat and fast beat discussed in Section 4.4.



(a) Close to the edge of lock range

(b) Far outside the lock-range

Figure 6.9: ILO behavior outside the lock-range

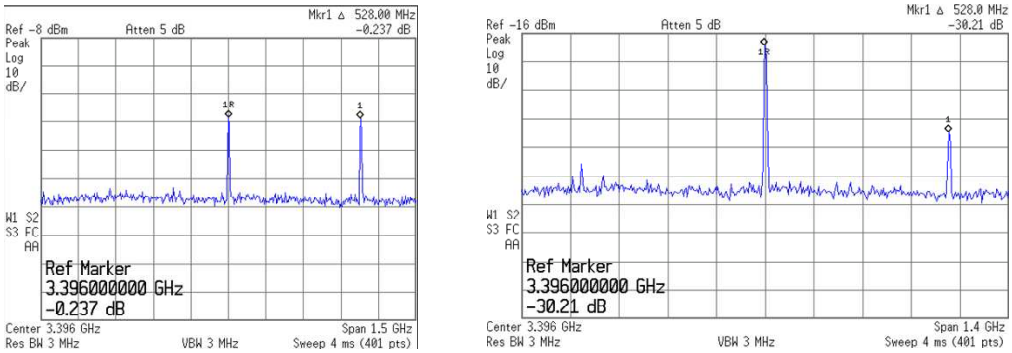


(a) Lock-range measurement for 3 different injection strengths

(b) Single-sided lock range vs. injected power

Figure 6.10: ILO lock-range measurement

In Section 5.3.1, the lock range required for WiMedia-UWB-compliant fast settling was calculated using linear settling expression. It is important to verify the achievable lock range experimentally. The lock-range for three different injection signal strengths are shown in Fig. 6.10a. The variation of lock-range with injection levels (expressed in dBm) is plotted in Fig. 6.10b. It shows that one-sided lock-range of the ILO can be increased well beyond the required value, thereby allowing the possibility of a sub-9.5 ns settling time.



(a) Two tone input 528 MHz apart

(b) Spurs at -35 dBm input

Figure 6.11: ILO spur performance

A frequency synthesizer for WiMedia-UWB needs to have good spur suppression of its side bands to avoid reciprocal mixing. A two-tone signal, as shown in Fig. 6.11a, was applied to the ILO. The two tones were equal in power and were placed 528 MHz, with one tone being the required injected frequency. When the oscillator locks onto one tone, it suppresses the other. The two tones at the injection input also produce a tone at the output of the ILO on the opposite side of the injected signal as shown in Fig. 6.11b due to mixing within the oscillator [1]. The dependence of the suppression magnitude on the injection level is depicted in Fig. 6.12. Naturally, from Fig. 6.10, it implies that the larger the lock-range, the more accommodating the ILO is in terms of spurs and hence, spur suppression is reduced at higher injection levels. This results in a clear trade-off between spur suppression and frequency lock time of the ILO in case of multi-tone injection.

Within the lock range, the phase noise of the ILO follows the phase noise of the input signal in case of fundamental injection locking [1]. This is validated in Fig. 6.13 which shows the phase noise of free-running and locked oscillator. Since the injection signal was generated using a clean source, the phase noise behavior shows a vast improvement. It should be noted that in case of sub-harmonic and super-harmonic injection locking, the phase noise of the particular locking harmonic should be considered for proper ILO

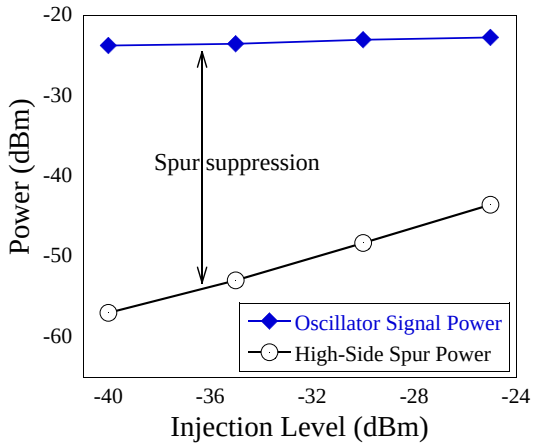


Figure 6.12: ILO measured spur suppression

phase noise estimation.

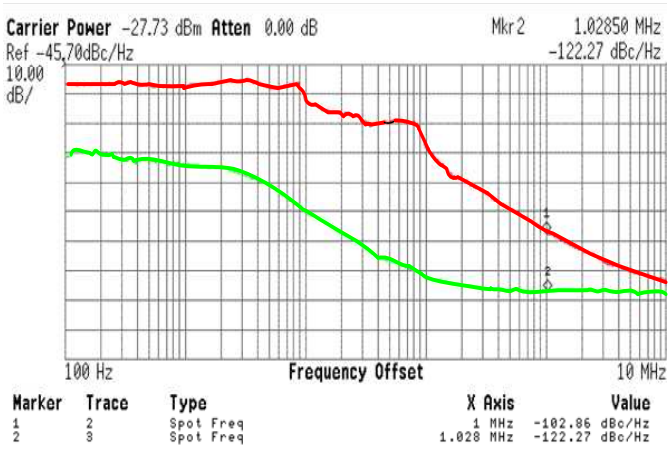


Figure 6.13: ILO phase noise: Locked vs unlocked

6.2.3 Transient Measurement Results

A typical ILO output and control signal transient from the DSO for one of the frequency steps are illustrated in Fig. 6.14. There is a delay of about 25 ns between the time of the control signal step and the time instant where the oscillator receives the switched injection signal. This can be attributed to delays arising from the external line drivers,

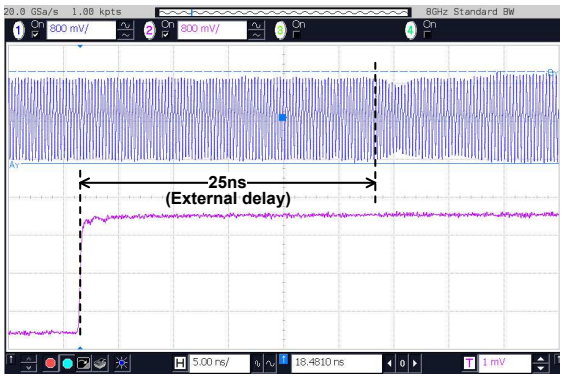
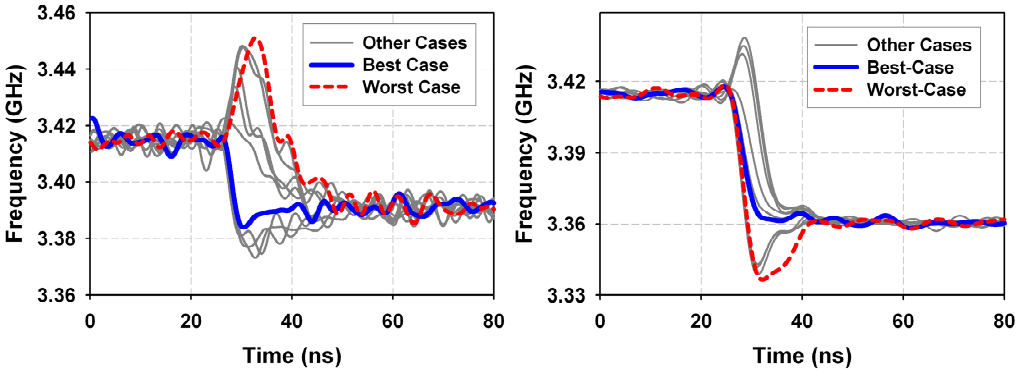


Figure 6.14: Typical ILO output and switching control signal shown on the DSO

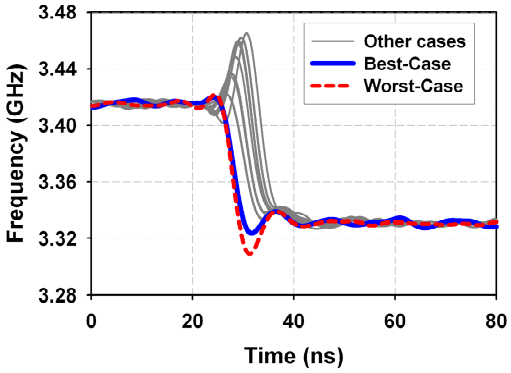
RF switches, balun and 50 Ω cables between the Digital Signal Generator (Tektronix HFS9003) and the injection input point on chip. In Section 5.3, approximate calculations showed that the necessary ω_L value for a lock-time of 10 ns was about 90 MHz. To verify this, we choose three different injection signal strengths for both the cases described in Fig. 6.7.

Case I Measurements (Unlocked to Locked): The measured frequency transients for each of the three different selected lock-ranges are shown in Fig. 6.15. The lock-ranges (ω_L) used for this case are 29, 61 and 100 MHz. The injection frequencies for each of these sub-cases were chosen to be 3.39, 3.36 and 3.33 GHz, respectively. Each of the three frequency transients plotted show the best-case (in solid blue) and worst-case (in dashed red) frequency settling characteristics. The other measured frequency transients for the respective case are plotted in grey. Controlling the initial phase of injection was not possible on chip. So an alternate technique was used to attain different $\phi(0)$ readings. The ON-OFF switching frequency was chosen such that it was not a sub-harmonic of the ILO frequencies. This ensured that different switching edges would result in different values for $\phi(0)$. Multiple measurements around the switching edge were stored in the DSO. After filtering in MATLAB to remove spurs and out-of-band



(a) $\omega_L = 29$ MHz

(b) $\omega_L = 61$ MHz

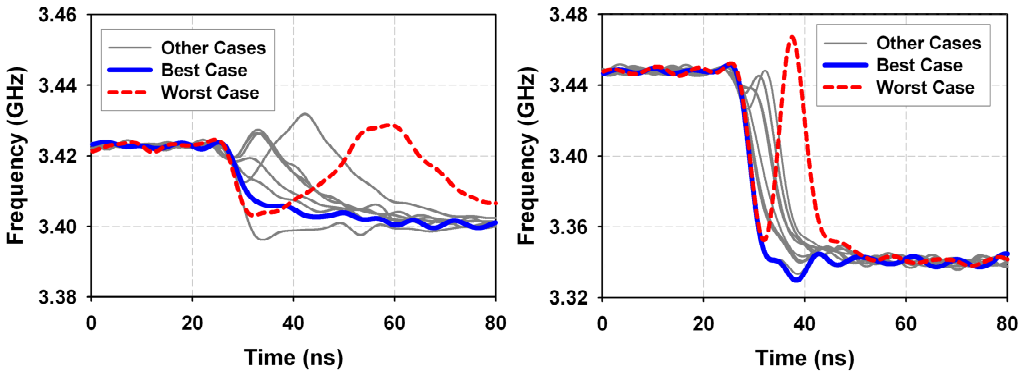


(c) $\omega_L = 100$ MHz

Figure 6.15: Case I Measurements

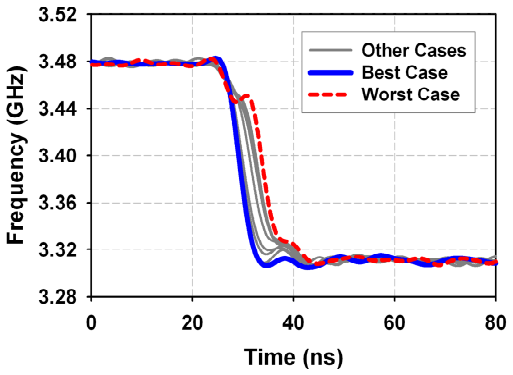
noise, the frequency transients for the different lock-ranges show behavior similar to that predicted by theory and the simulations shown in Fig. 4.5. The measured lock-times for the best and worst-case, and average lock-times are listed in Table 6.2.

Case II Measurements (Locked to Locked): The measured frequency transients for each of the three different chosen lock-ranges is shown in Fig. 6.16. The lock-ranges (ω_L) used for Case II are 18, 61 and 95 MHz. The injection frequency pairs chosen for the three different lock-ranges were (3.42, 3.4) GHz, (3.45, 3.34) GHz and (3.48, 3.31) GHz. Similar to Fig. 6.15, the best-case and worst-case frequency settling characteristics are



(a) $\omega_L = 18$ MHz

(b) $\omega_L = 61$ MHz



(c) $\omega_L = 95$ MHz

Figure 6.16: Case II Measurements

plotted in solid blue and dotted red, respectively, and the in-between cases are plotted in grey. Here again, multiple measurements were taken to obtain different values of $\phi(0)$. The frequency transients show very similar behavior to theoretical predictions. The measured lock-time statistics are quantified in Table 6.2.

The measured lock-times for both the cases clearly show the inverse relationship of lock-range and lock-time. Even though the best-case lock-times (these cases probably have $\phi(0)$ very close to ϕ_{ss}) are very close, there is a clear trend seen from the worst-case lock-times measured. The lock-range required for a 10 ns frequency settling time was estimated to be about 90 MHz in Section 5.3. It is clear from our measurements that a

Table 6.2: Summary of ILO transient measurements (Unlocked frequency = 3.41 GHz)

Experiment Set	Measured Lock Range	Estimated I_{inj}/I_{osc}	Injected Freq. I	Injected Freq II	Measured Lock Time (ns)		
					Best	Worst	Average
Case I	29 MHz	0.1	Unlocked	3.39 GHz	4.42	20.25	16.36
Case I	60 MHz	0.21	Unlocked	3.36 GHz	8.23	15.1	10.54
Case I	100 MHz	0.35	Unlocked	3.33 GHz	4.1	9.8	8.23
Case II	18 MHz	0.06	3.42 GHz	3.4 GHz	25.3	65.1	38.35
Case II	60 MHz	0.21	3.45 GHz	3.34 GHz	2.66	14.7	8.47
Case II	95 MHz	0.35	3.48 GHz	3.31 GHz	4.7	10.02	6.85

lock-range of 100 MHz is enough to attain this lock-time. The plots shown in Figs. 6.15 and 6.16 also confirm some of the following theoretical conjectures presented before.

(a) The locking transient shows a strong dependence on $\phi(0)$. This is verified by the different transients seen for similar cases.

(b) The ILO frequency can switch near-instantaneously when $\phi(0) = \phi_{ss}$. This is confirmed by the best-case plots in many of the cases shown in the two figures - Figs. 6.15 and 6.16.

(c) The ILO frequency initially jumps to ω_{inj} at the injection instant, when $\phi(0) = \pi - \phi_{ss}$, then drifts away and then settles back to ω_{inj}. This behavior is clearly noticed in the worst-case plots shown in Figs. 6.16a and 6.16b.

(d) The maximum or minimum value attained by ILO frequency depends upon $\phi(0)$. This behavior can be observed in the some of the lower lock-range plots, where settling is slower.

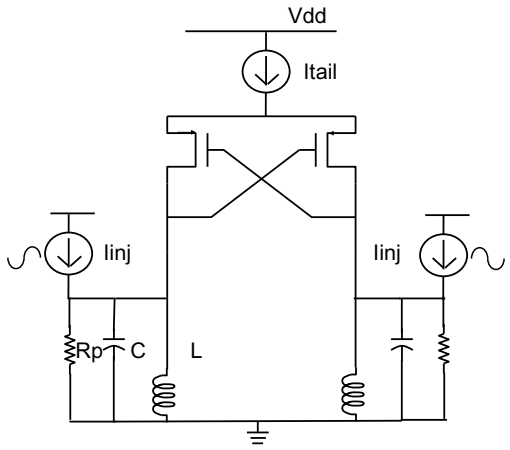


Figure 6.17: ILO schematic

6.3 Predictive Locking/High-frequency DDS: Simulation Results

In this section, simulation results are presented to demonstrate the capabilities of injection locking based high frequency DDS. Since this is based on the predictive fast-hopping capability discussed in Section 5.3.2, the simulation results also help prove this quality of the ILO. Shown in Fig. 6.17 is a PMOS-only oscillator with a parallel RLC tank. Switched capacitors were used to digitally control the frequency of the oscillator. I_{inj} sources represent current injection to the oscillator. They can be single or multi-tone signals. As noted earlier, the versatility of the DDS is clearly evident when used as a modulation source. Here we use frequency shift keying (FSK) as the modulation scheme.

6.3.1 Fundamental FSK

Table 6.3 shows the circuit parameters and simulation conditions used for fundamental FSK - when the frequency of the DCO is close to the injected FSK signal frequencies. The injected signal is a single tone signal switching between low frequency and high frequency. The center frequencies of the DCO were chosen such that the resulting ϕ_{ss} are

	Low frequency	High frequency
Center frequency (f_0)	7170 MHz	7165 MHz
Tank Q	6	6
Injected frequency (f_{inj})	**7000 MHz**	**7147 MHz**
Injection level (I_{inj}/I_{osc})	0.133	0.133
Lock range estimate (f_L)	78.6 MHz	80.3 MHz
Steady state phase (ϕ_{ss})	12.48°	13.0°

Table 6.3: Circuit / simulation parameters used for fundamental FSK

12.48° and 13.0°. The frequency-settling behavior is plotted in Fig. 6.18(a). Again long transient simulations were run and the period-to-period frequency was calculated from the zero crossings of the time-domain data. The plot shows three curves: instantaneous frequencies of the free-running DCO, the injected signal and the DCO under locking. At startup, the DCO oscillates at its free-running center frequency. Since the phase difference between the injected and the oscillator signal is arbitrary, there is an exponential settling to the locked frequency. The settling time is dictated by both the lock range and initial phase. In this case, settling occurs well before the first transition. Fig. 6.18(b) shows the transition from high to low frequency. The locked oscillator signal very closely follows the injected signal. Since each data point on the curve represents one period of the signal, the graph demonstrates that the locking occurs within two periods [1]

[1]Note, the two period settling is due to the finite rate of change of the injected signal frequency. Other results, not shown here, show one period settling. However, as we are only able to measure period-to-period frequency change we are unable to resolve the frequency settling behavior with any better resolution than one period.

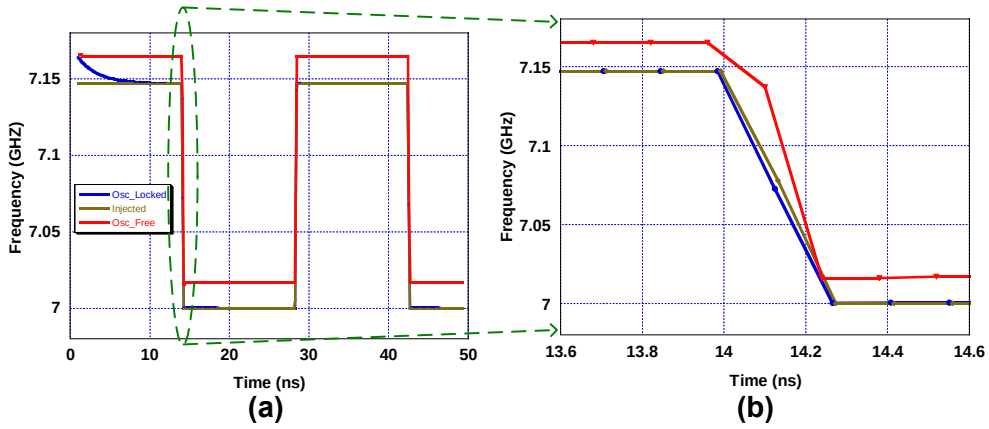
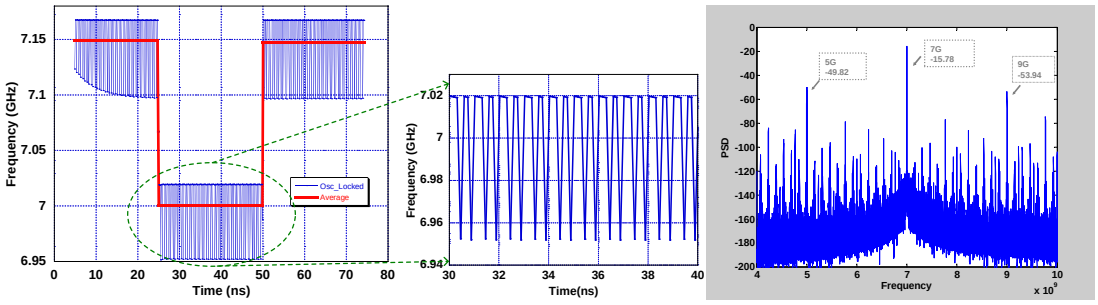


Figure 6.18: (a) Injection locked output of fundamental FSK (b) Zoomed in view of frequency transition point

6.3.2 Harmonic FSK

The multiplication capability of the DDS architecture is demonstrated using harmonic FSK. Here the DCO was tuned close to the seventh harmonic of a square wave injected signal. Any variation in the DCO frequency due to process or temperature can be calibrated out prior to final use. The circuit parameters and simulation conditions used for harmonic FSK are shown in Table 6.4. The square wave frequency was switched between 1 GHz and 1.021 GHz (corresponding to seventh-harmonic frequencies of 7 GHz and 7.147 GHz). The choice of center frequencies of the DCO resulted in ϕ_{ss} values of 25.8° and 26.8°, respectively. The simulation results are plotted in Fig. 6.19. The instantaneous frequency variation (blue) and the time-averaged frequency (red) is shown in Fig. 6.19a. The time-averaged frequencies are very close to 7 GHz and 7.147 GHz. The magnified version, however, shows the periodic variation of instantaneous frequency with time which indicates the presence of other harmonics of the injected square-wave. The power spectral density (PSD) plot of the output signal in Fig. 6.19b further validates this conjecture. The two most significant spurs are at least 34 dB below the principal harmonic. However, their presence affects our technique for measuring the near instan-

taneous frequency by using zero-crossing periods. The frequency-switching capability shows that the output signal is able to switch in frequency nearly instantaneously.



(a) Period-to-period frequency & zoomed in view of the lower frequency

(b) Spectrum of lower frequency

Figure 6.19: Generation of harmonic (7^{th} harmonic) FSK signal and the spectral content of the lower frequency in FSK

	Low frequency	High frequency
Center frequency (f_0)	7170 MHz	7165 MHz
Tank Q	6	6
Injected frequency (f_{inj})	**1000 MHz**	**1021 MHz**
Injection level (I_{inj}/I_{osc})	0.07	0.07
Lock range estimate (f_L)	39.0 MHz	39.9 MHz
Steady state phase (ϕ_{ss})	25.8°	26.82°

Table 6.4: Circuit / simulation parameters used for Harmonic FSK

6.4 Chapter Summary

This chapter presented measurement and simulation results validating the theoretical understanding of ILOs developed so far. A low frequency discrete Colpitts oscillator running at 57 MHz was used to show time-domain lock acquisition, tracking and beat behavior. Using an FSK input signal, locking transients were obtained. The shape of frequency settling was found to be in excellent agreement with theoretical plots developed earlier. A high frequency PMOS-only negative-g_m LC oscillator was designed and fabricated in 0.13-μm CMOS technology. The frequency was chosen to be 3.3 GHz which is the low end of WiMedia-UWB specification. Spectrum measurements were performed on the prototype to validate the locking and out-of-lock characteristics of the ILO. Achievable lock ranges were shown to be more that the required estimate to lock within 10 ns. A clear trade-off was identified when spur suppression measurement was performed using a two tone input signal. The spur suppression degraded as the input signal amplitude was increased which is necessary to achieve larger lock ranges. Two measurement setups were designed and transient measurement was performed on the LC-oscillator for three different lock ranges. As lock range increased, the average lock time decreased. Finally, high frequency DDS architecture and predictive locking were verified using fundamental and harmonic FSK simulation. Almost instantaneous lock times were achieved in both cases.

Chapter 7

Quadrature Injection Locked Oscillator

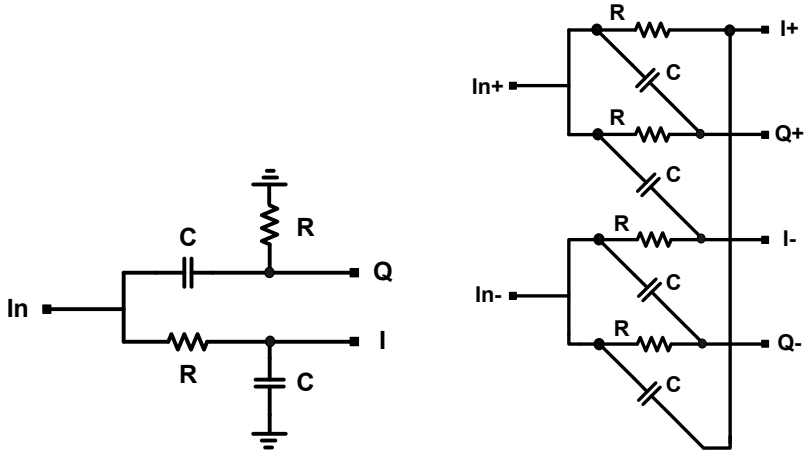
Frequency synthesizers, in addition to providing good phase noise, should some times provide quadrature signals. Many modern tranmitters and receivers use I (in-phase) and Q (quadrature) signals for modulations and demodulation (Chapter 2). Quadrature components of the signal are needed when phase modulation schemes are used. If not, phase information is lost due to overlap in both the sidebands. I and Q signals are required in direct conversion receivers and image reject architecture like the Weaver architecture. Many WiMedia-UWB-compliant receive chains are based in zero-IF architectures [62,63] which require the LO to generate quadrature outputs.

Quadrature voltage-controlled oscillator (QVCO) is a very attractive technique in cases where low-power consumption, wide-band amplitude and phase margin and very high frequency operation is required. In this chapter, traditional quadrature signal generation techniques are presented and QVCO is examined from an injection locking perspective. Injection locking of a QVCO is then presented. An intuitive closed-form expression for dynamics of a quadrature injection-locked oscillator (QILO) is developed using the

same methodology employed to develop Adler's equation

7.1 Quadrature Generation Techniques

One of the simplest ways to generate the quadrature phases is to phase-shift the signal by $\pm 45°$ by passing it through an RC-CR network shown in Fig. 7.1a. It can be easily shown that the phase difference between the output signals in Fig. 7.1a is 90° at all frequencies but their magnitude matches at only one frequency ($=1/(2\pi RC)$). A serious issue with this technique is that process and temperature variations shift this frequency. One way to address this problem is to use limiting stages in the LO path. However, this method consumes very high power at multi-giga hertz frequencies and one has to be careful about the AM-PM conversion [64]. Further more, wide-band matching is not possible and if wide-band matching is required, multiple stages are needed which involve more signal power loss and are very noisy.

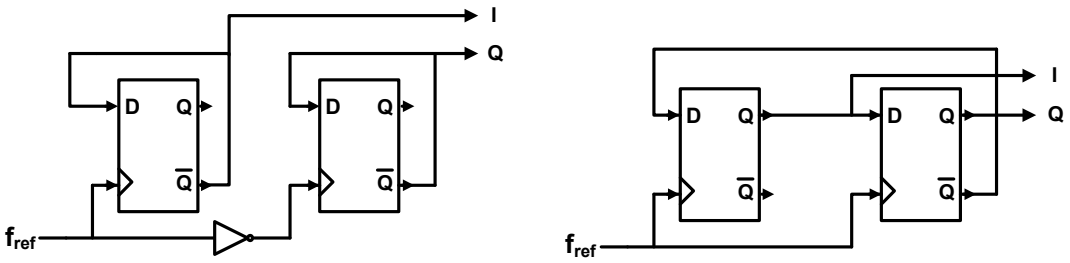


(a) RC-CR network (b) Polyphase filter

Figure 7.1: RC based quadrature generation

RC polyphase filters are symmetric networks with inputs and outputs in symmetric relative phases. If the network is driven by a differential signal as in Fig. 7.1b, the output

is differential quadrature outputs. Again, the useful bandwidth is about 10% around the RC pole frequency. This bandwidth can be extended by cascading multiple stages which results in higher signal power loss and noise.



(a) Divide-by-2 (b) Divide-by-4

Figure 7.2: Digital quadrature generation

A popular digital technique to generate quadrature outputs is frequency division. A divide-by-2 circuit shown in Fig. 7.2a produces quadrature outputs but at half the input frequency. So, the LO needs to be designed at twice the required frequency which is power consuming. Since the output depends on both rising and falling edges of the clock (input), the quality of the output depends both on the edge quality and the duty cycle. If the differential clock signal is generated by the crude technique shown in Fig. 7.2a, the delay of the inverter degrades the quadrature output. This dependence is absent in the divide-by-4 circuit shown in Fig. 7.2b but the input frequency must now run at even higher frequency than the first case which further increases power consumption.

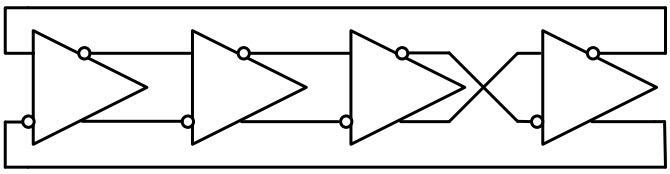


Figure 7.3: Ring oscillator

A direct method to generate a multi-phase signal is to use a ring oscillator (Fig. 7.3). This has very good phase and amplitude matching and runs at the required frequency.

However, ring oscillators have inferior phase noise performance compared to LC-based oscillators. Also their power consumption goes up as the frequency increases. A low power technique for quadrature signal generation is to use a pair of identical cross-coupled LC oscillators called the quadrature voltage controlled oscillator(QVCO).

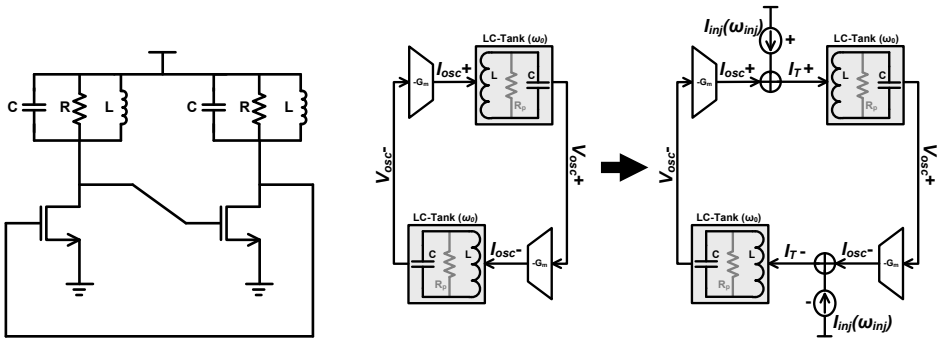
Quadrature VCO: The concept of a quadrature-coupled LC-oscillator on chip was first introduced in [65]. Two identical differential oscillators are connected in feedback and cross-connected to generate the two differential outputs which are in quadrature generating four phases - 0°, 90°, 180° and 270°. Popularly, known as the quadrature voltage-controlled oscillator (QVCO), shown in Fig. 7.6, the underlying concept here is to injection-lock the two identical oscillators to each other. Injection-locking ensures that the two oscillate at the same frequency and the cross-coupled topology forces the quadrature outputs. One particular implementation for a QVCO is shown in Fig. 7.6. Since the coupling is through transistors parallel to the switching transistors, this topology is popularly known as the parallel QVCO (PQVCO) [65]. Other topologies and tradeoffs will be discussed in Chapter 8.

7.2 Theory: ILO vs. QILO

As alluded to in Chapter 3, an injection locked oscillator (ILO) consists of an oscillator with provision to input an external signal in the form of a current or a voltage. Here, the example of an LC-oscillator with current injection as depicted in Fig. 7.4 is considered. Fig. 7.4a shows the classical $-G_m$ LC-oscillator as a cascade of two inverter stages in a feedback loop. A linearized model for this oscillator is shown in Fig. 7.4b. The voltage signal ($V_{osc}-$) from one-arm is converted to current ($I_{osc}+$) by the $-G_m$ cell, which in turn is converted to $V_{osc}+$ by the LC-tank. The overall phase-shift of 2π is introduced by the two G_m blocks, each introducing a phase-shift of π. The oscillator output frequency is the natural frequency of the LC-tank, ω_0 ($= 1/\sqrt{LC}$), at which frequency the LC-tanks

introduce zero phase-shift.

When an injection-signal, here represented in the form of current, as shown in Fig. 7.4b, is introduced into the loop, it creates an additional phase-shift in the oscillator feed-back loop and the total current flowing into the tank is the vector sum of the oscillator current I_{osc} (current through the cross-coupled pair) and injection current, I_{inj}. As illustrated in Fig. 7.5, $\phi(t)$ is the instantaneous phase difference between the total current I_T and the injection signal I_{inj}, and $\psi(t)$ is the phase-shift between the I_{osc} and I_T. Due to the phase-shift introduced, the oscillator no longer satisfies Barkhausen criteria at its natural frequency ω_0 and has to shift its operating frequency, so that the LC-tank introduces a phase-shift that is opposite to $\psi(t)$ to satisfy the loop phase-shift criterion. If the injection frequency ω_{inj} is within the range $(\omega_0 - \omega_L,\ \omega_0 + \omega_L)$, the oscillator locks to the injected signal and the ILO output frequency eventually becomes ω_{inj} [1,17]. The quantity ω_L is defined as the single-sided lock-range of the oscillator.



(a) LC-oscillator (b) Block-level oscillator to ILO transformation

Figure 7.4: Simplified oscillator and ILO

Adler's Equation for ILO

As presented earlier, the transient dynamics of an ILO, after the injection signal is applied, can be approximated by Adler's equation. A complete derivation is presented in Section. 3.2.1. The phase dynamics of the QILO are derived here based on similar

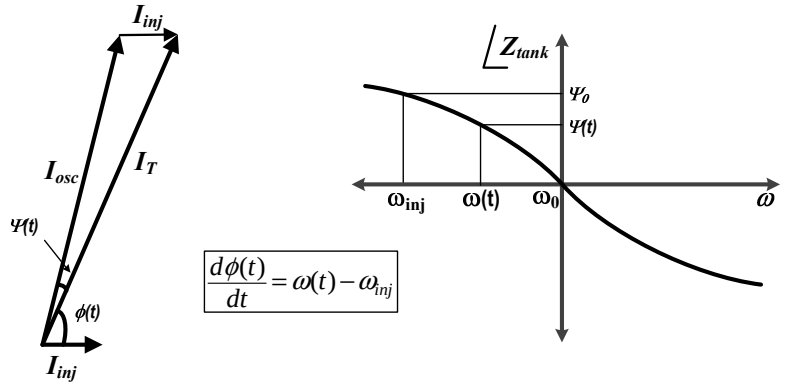


Figure 7.5: Phasor interpretation for an ILO

analysis. Therefore Adler's equation for an ILO is re-derived for the purposes of clarity and continuity. In order to re-derive Adler's original equation, the sine-law for triangles has to be applied to the phasor diagram and the linearity of the tank phase $\angle Z_{tank}(\omega)$ in the vicinity of ω_0 has to be exploited, leading to two equations

$$\frac{\sin\{\psi(t)\}}{I_{inj}} = \frac{\sin\{\phi(t)\}}{I_{osc}} \tag{7.1}$$

$$\sin\{\psi(t)\} \approx \psi(t) = \left(\frac{2Q}{\omega_0}\right)(\omega_0 - \omega(t)) \tag{7.2}$$

(Here note that for simplicity $\phi(t)$ is assumed to be between I_{inj} and I_T which is slightly different from Adler's original derivation (Sec. 3.2.1) where $\phi(t)$ is between I_{inj} and I_{osc}. It introduces no error in the derivation but does not render the phasor analysis for extension to higher injection levels.) Substituting eqn. 7.2 in eqn. 7.1, and applying the relationship between $\phi(t)$ and $\omega(t)$ (highlighted in Fig. 7.5), results in Adler's equation

$$\frac{d\phi(t)}{dt} = (\omega_0 - \omega_{inj}) - \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)\sin\{\phi(t)\} \tag{7.3}$$

7.2.1 Quadrature Oscillator

Consider the QVCO shown in Fig. 7.6. A simplified figure and the phasor diagram of the QVCO are shown in Fig. 7.7. The phasor diagram in Fig. 7.7b represents the orientation of the various signals in steady-state. The analysis here is done in steady state only

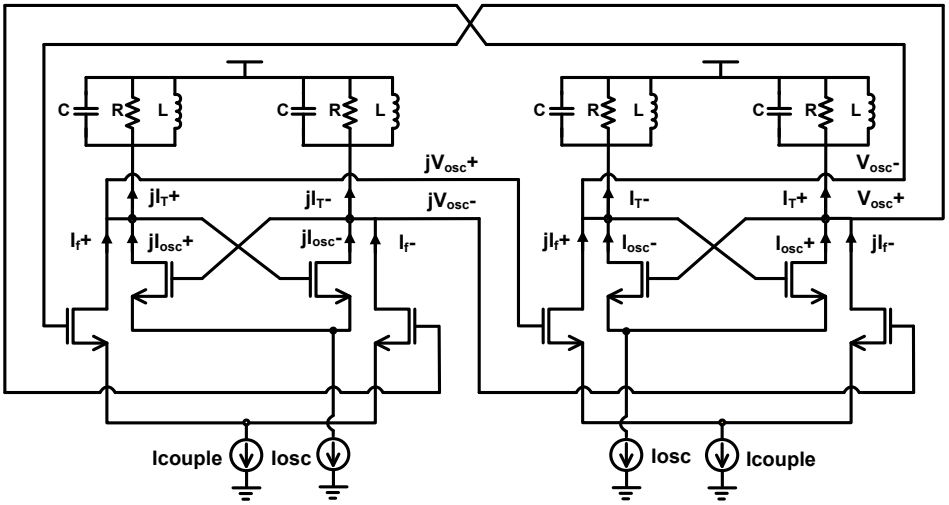
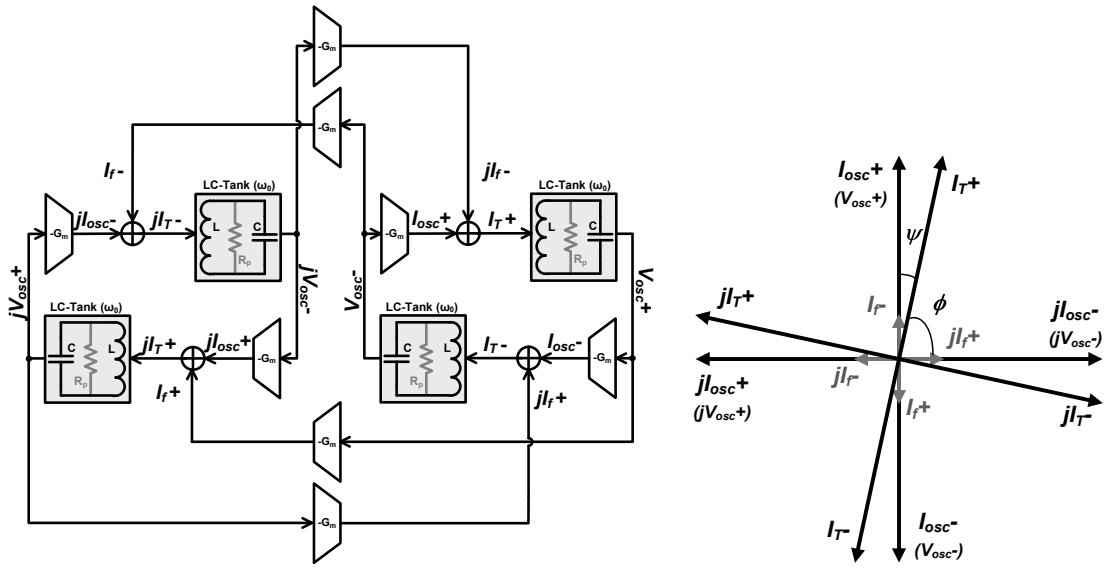


Figure 7.6: Quadrature VCO



(a) QVCO block diagram

(b) QVCO phasor interpretation

Figure 7.7: Simplified diagram and phasor representation of QVCO

because the lack of reference (I_{inj} in the case of an ILO) makes it difficult to obtain the evolution of phase dynamics. By applying similar techniques used to derive Adler's equation for a simple VCO, we arrive at the requirement for the two oscillators to lock

in quadrature in steady state:

$$\phi_{ss} + \psi_{ss} = \pm\frac{\pi}{2} \tag{7.4}$$

The '±' denotes that the one of the two oscillators could lead or lag the other by 90°. Under ideal conditions on a parallel RLC model for the tank and perfect matching between the two oscillators, either of the two states are possible. However, due to the asymmetry of an on-chip LC-tank around its center frequency due to finite inductor Q's and the mismatch between oscillators, the QVCO settles to one of the states [66]. For the case depicted in Fig. 7.7, $\phi_{ss} + \psi_{ss} = \pi/2$. This condition requires the QVCO to shift its operating frequency ω_{QVCO}, such that $\omega_{QVCO} < \omega_0$. Continuing from eqn. 7.4, ω_{QVCO} can be determined as follows:

$$\psi_{ss} = \pm\frac{\pi}{2} - \phi_{ss} \Rightarrow \tan(\psi_{ss}) = \frac{2Q}{\omega_0}(\omega_0 - \omega_{QVCO}) = \cot(\phi_{ss})$$

For small-signal injection, the expression for ω_{QVCO} can be simplified to

$$\omega_{QVCO} = \omega_0 \pm \frac{\omega_0}{2Q}\left(\frac{I_f}{I_{osc}}\right) \tag{7.5}$$

(Note that the relation in Eqn. 7.5 is exact because ϕ_{ss} is assumed to be between I_f and I_T.) This implies that both oscillators of the QVCO is pushed close to the edge (either higher or lower) of the lock-range. This is intuitive, since the injection signal and output of each block of the QVCO are phase-shifted by ±90°.

7.2.2 Adler's Equation Extended to QILOs

The QVCO output spectrum still behaves like an open-loop system, since both the oscillators in the QVCO are open-loop. In order to stabilize it, the QVCO has to be locked to a low-noise reference through either a phase-locked loop (PLL) [67] or by injection-locking [44]. A particular scheme for injection locking the QVCO is shown in Fig. 7.8 and its simplified block diagram is shown in Fig. 7.9a. The principal idea is to lock the two oscillators of the QVCO to a pair of quadrature injection signals. This adds

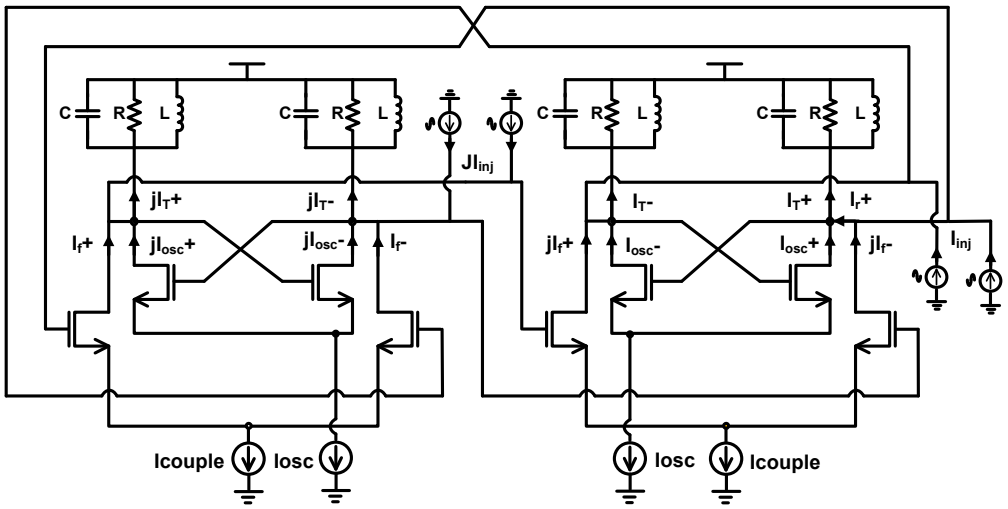
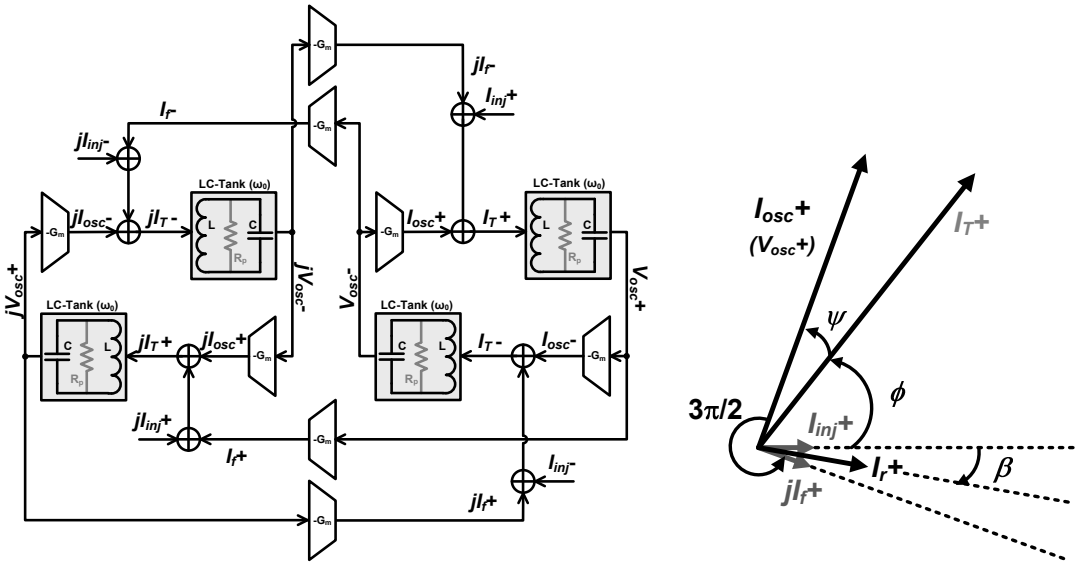


Figure 7.8: Injection locked quadrature VCO (QILO)



(a) QILO block diagram

(b) QILO phasor interpretation

Figure 7.9: QILO simplified diagram and phasor representation

a set of four additional current vectors to the phasor diagram in Fig. 7.7b. To simplify the understanding of the phasor mechanics, the phasors for only one of the quadrature signals is shown in Fig. 7.9b.

By taking into account the two assumptions stated while deriving Adler's equation for an ILO, we derive the Adler's equation for a QILO. In the following derivation, we also assume that $|I_{inj} \pm| = |jI_{inj} \pm| = I_{inj}$, $|I_{osc} \pm| = |jI_{osc} \pm| = I_T$, $|I_T \pm| = |jI_T \pm| = I_T$, $|I_f \pm| = |jI_f \pm| = I_f$ and $|I_r \pm| = |jI_r \pm| = I_r$. Applying the sine-law for triangles to this case, we arrive at

$$\frac{\sin\{\psi(t)\}}{I_r} = \frac{\sin\{\phi(t) - \beta(t)\}}{I_{osc}} \tag{7.6}$$

And the angle between I_{inj} and I_f vectors is $[2\pi - 3\pi/2 - \phi(t) - \psi(t)] = [\pi/2 - \phi(t) - \psi(t)]$. This adds two more relations:

$$I_r \cos\{-\beta(t)\} = I_{inj} + I_f \sin\{\phi(t) + \psi(t)\} \tag{7.7}$$

$$I_r \sin\{-\beta(t)\} = I_f \cos\{\phi(t) + \psi(t)\} \tag{7.8}$$

Substituting eqns. 7.7 and 7.8 into eqn. 7.6, gives

$$\begin{aligned} \sin\{\psi(t)\} &= \frac{\sin\{\phi(t)\}[I_{inj} + I_f \sin\{\phi(t) + \psi(t)\}] + \cos\{\phi(t)\}[I_f \cos\{\phi(t) + \psi(t)\}]}{I_{osc}} \\ &= \frac{I_{inj}}{I_{osc}} \sin\{\phi(t)\} + \frac{I_f}{I_{osc}} \cos\{\psi(t)\} \end{aligned} \tag{7.9}$$

Assuming low-level injection, approximate $\sin\{\psi(t)\} \approx \psi(t)$, $\cos\{\psi(t)\} \approx 1$ and substituting approximations, eqn. 7.2, eqn. 7.9 can be reduced to

$$\begin{aligned} \frac{d\phi(t)}{dt} &= \underbrace{\left(\omega_0 - \frac{\omega_0}{2Q}\frac{I_f}{I_{osc}}\right)}_{=\omega_{QVCO}} - \omega_{inj} - \underbrace{\frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)}_{=\omega_L} \sin\{\phi(t)\} \\ \Rightarrow \frac{d\phi(t)}{dt} &= (\omega_{QVCO} - \omega_{inj}) - \omega_L \sin\{\phi(t)\} \end{aligned} \tag{7.10}$$

The quantity, ω_L, can be defined as the single-sided lock-range of the QILO around the center frequency of the QVCO, ω_{QVCO}. Note that Eqn. 7.10 is the same form as

Adler's equation. Hence, the solutions (eqns. 4.3 and 4.6) to the non-linear differential equation can be extended to the QILO. Also, the theories/predictions for ILOs presented in Chapters 4 and 5 can be applied to the QILO.

The steady-state phase, ϕ_{ss}, for the QILO is given by

$$\phi_{ss} = \sin^{-1}\left(\frac{\omega_{QVCO} - \omega_{inj}}{\omega_L}\right) \tag{7.11}$$

7.2.3 Fast-locking Using QILOs

Similar to eqns. 4.3 and 4.6 derived in Section 4.2, solutions can also be derived for eqn. 7.10. By intuition, the solutions will be in the following form:

$$\phi(t) = 2\tan^{-1}\left[\left(\frac{\omega_L}{\omega_{QVCO} - \omega_{inj}}\right) - \left(\frac{\omega_B}{\omega_{QVCO} - \omega_{inj}}\right) \times \tanh\left(\frac{\omega_B(t - t_0)}{2}\right)\right] \tag{7.12}$$

$$t = \frac{1}{\omega_B}\ln\left|\left(\frac{\tan\left(\frac{\phi(t)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}\right) \times \left(\frac{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(t)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}\right)\right| \tag{7.13}$$

where

$$\omega_B = \sqrt{\omega_L^2 - (\omega_{QVCO} - \omega_{inj})^2} \tag{7.14}$$

This proves that many of the expected characteristics of an ILO in Section 4.3 can also be expected from a QILO. Most important to our requirements is the capability of ILOs to hop extremely fast across frequencies. As presented in Section 5.3, there are two ways of achieving fast lock-times: by ensuring a large lock-range for the ILO, or by appropriately matching conditions before and after the frequency hop. In the next chapter (Chapter 8), a prototype for fast-hopping frequency synthesis based on a QILO is presented. In this synthesizer, the latter of the two techniques mentioned above is utilized. The condition that would ensure fast-locking requires the steady-state phase for each of the different target (hopping) frequencies to closely match. So for any particular frequency hop at $t = 0$, this condition can be mathematically expressed as

$$\phi_{ss}|_{t=0-} = \phi_{ss}|_{t=0+} \Rightarrow \left.\frac{\omega_{QVCO} - \omega_{inj}}{\omega_L}\right|_{t=0-} = \left.\frac{\omega_{QVCO} - \omega_{inj}}{\omega_L}\right|_{t=0+} \tag{7.15}$$

This condition effectively translates matching the initial phase for the $t = 0+$ frequency with the respective steady-state phase. Ideally, instant locking is possible using this condition but limited frequency tuning accuracy and lock-range mismatch leads to small, yet finite lock-times.

7.3 Chapter Summary

In this chapter, the traditional quadrature generation techniques were discussed. It was identified that QVCO is a low power quadrature signal generation scheme with excellent amplitude and phase matching over a wide band of frequencies. Theory of QVCO from an injection locking perspective was presented. Theoretical expressions governing the behavior of an injection-locked quadrature VCO were developed. This was done using the procedure similar to that used for derivation of Adler's original equation. The closed-form expression for the QILO also closely resembles Adler's equation for stand-alone ILOs and the fast-hopping capability of an ILO are readily applicable to the QILO.

Chapter 8

Fast-Hopping Quadrature Frequency Synthesizer Prototype

In this chapter, a novel architecture for a fast-hopping frequency synthesizer based on sub-harmonic injection-locking that generates quadrature outputs and is compliant with the WiMedia-UWB/Wireless-USB standard is presented. The quadrature synthesizer hops across the first band-group frequencies of WiMedia-UWB specification (Section 5.1) [68] with lock-times of less than 2.5 ns.

Fast-hopping frequency synthesizers based on injection-locking have been proposed in recent years [58,69,70]. The architecture proposed in [69] generates quadrature output by frequency division. This method requires the design of LC-oscillators at twice the frequencies of interest and uses current-mode-logic (CML) for the divide-by-two operation to generate quadrature outputs (Section 7.1). A CML divider operating at such high frequencies draws significant amount of power. In addition, low-Q inductors are used to improve lock-ranges. Consequently, the LC-oscillator in [69] draws substantial power. The architecture presented here is based on a QILO and uses the understanding and fast-locking capabilities of QILO developed in Chapter 7. The prototype consumes

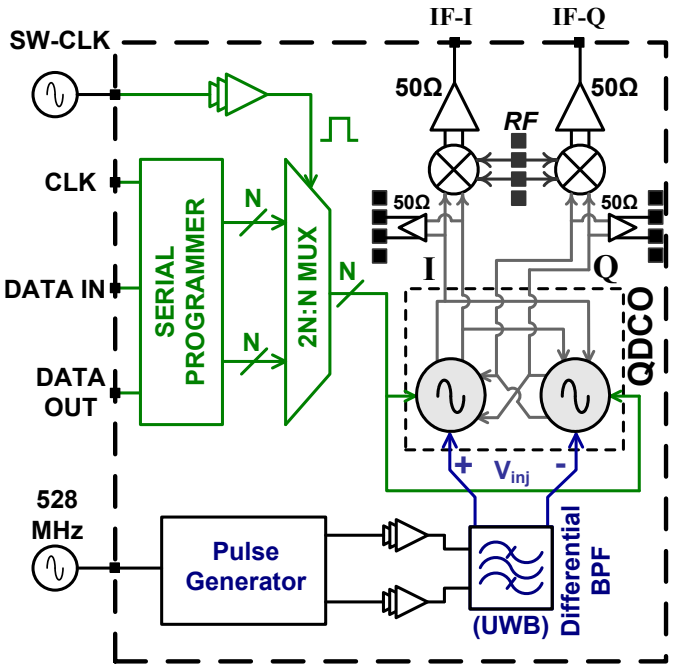


Figure 8.1: Fast-hopping Quadrature Frequency Synthesizer Architecture

14.5 mW of power and is the lowest power fast-hopping quadrature frequency synthesizer that has been reported to-date.

8.1 Architecture

The block-level architecture for the proposed frequency synthesizer is shown in Fig. 8.1. The architecture is based on sub-harmonic injection locking of a quadrature digitally-controlled oscillator (QDCO). The injection signal can be applied to the output node of the individual oscillators (Fig. 7.8) but that would require generation of multi-phase (quadrature) injection signal [44]. To avoid this, the signal is applied to the tail current source of each oscillator in the QDCO which makes it an injection-locked frequency-divider (ILFD) [49]. This scheme requires only a differential signal and since the injection signal is fully differential (Fig. 8.2) at the second harmonic frequency, the quadrature characteristic of the outputs from the QDCO is reinforced.

To test the performance, the architecture is designed to cover the first band (3432, 3960 and 4488 MHz) of the WiMedia-UWB specification [68]. The corresponding injection signal frequencies required are 6864, 7920, 8976 MHz, respectively which are the 13^{th}, 15^{th} and 17^{th} harmonics of a 528 MHz signal. A sine-wave at this frequency is applied to a single-ended-to-differential (S/D) converter, which generates a differential low-jitter square wave. This differential square wave output contains odd-harmonics of the fundamental frequency. In the case of a square wave, the magnitude of n^{th}-harmonic decreases as $1/n$. In order to improve the harmonic content, this square-wave is converted into a train of narrow-width pulses using the pulse-slimmer block. Narrow-width pulses are richer in higher frequency harmonic content, with the power of the harmonic component inversely proportional to the pulse-width. In order to suppress the fundamental and unwanted harmonics in the pulsed signal, a differential RLC band-pass filter (BPF) is introduced in the signal path. This BPF, in addition to suppressing the spurious tones, provides moderate gain at the frequencies of interest. The center frequency of this BPF is designed to be at 7920 MHz, with a 3-dB bandwidth of 3134 MHz, i.e., $Q \approx 2.53$.

By selectively tuning the QDCO frequency, it is injection-locked to the required harmonic frequency. The key design constraint here is that the QDCO's natural frequency should be as close as possible to half the harmonic frequency of the input pulse-slimmed signal. Ensuring this condition results in extremely fast locking. This proximity condition needs to be satisfied for all the frequencies of interest. The digital bits for frequency control are obtained from a serial register which is externally programmed. A multiplexer (MUX) is used to switch between two selected bit sequences of N-bits (N being the number of tuning bits for the QDCO). The control signal for the $2N : N$ MUX is designed to switch with fast rise/fall times so as not to affect the final locking process. The externally applied sine or slow-rising square wave signal (SW-CLK) is buffered on-chip to ensure this condition.

8.1.1 Quadrature DCO

The QDCO forms the core of the frequency synthesizer. As mentioned in Section 7.2.1, two identical differential oscillators are cross-connected in feedback through coupling transistors oscillate in quadrature. The placement of coupling transistors leads to several different topologies of quadrature oscillators. In a parallel quadrature VCO (P-QVCO) the coupling is accomplished by transistors parallel to the switching transistors [65]. This topology suffers from a tradeoff between phase accuracy and phase noise performance. Furthermore, the parallel transistors may need additional current which increases the power consumption. In order to improve the phase noise without sacrificing quadrature accuracy, a series QVCO (S-QVCO) is presented in [71]. Here the coupling transistors are in cascode to the cross-coupled negative-g_m cell , as shown in Fig. 8.2. While the degeneration from switching transistors reduces the phase noise contribution of the coupling devices, they need to be made large to achieve good I/Q accuracy which reduces the achievable tuning range. An alternative SQVCO scheme is to use coupling transistors at the source nodes of the switching transistors [72]. This eliminates the loading effect of the coupling transistors at the output node thereby increasing the tuning range but their degeneration effect reduces the effective g_m of the switching transistors. This increases the power consumption. More recently another topology for QVCO was proposed [73] where the coupling transistors are connected in the cross-coupling paths of the switching transistors. This is advantageous in low voltage designs where transistor stacking is not possible. A quick analysis and simulation will show that this topology has a startup issue and would require high oscillator current and very wide coupling transistors to ensure successful start-up. Since the coupling transistors are connected to the output node, larger devices lead to a reduced tuning range. The choice of topology depends on the system requirements and tradeoffs. In the architecture presented here, the QDCO should exhibit good phase noise and quadrature accuracy even in the unlocked state,. This is

because the output phase noise of an ILO increases as the locking signal approaches the edge of the lock range [23]. Also the tuning range needs to be large to cover all the three bands in the first band group.

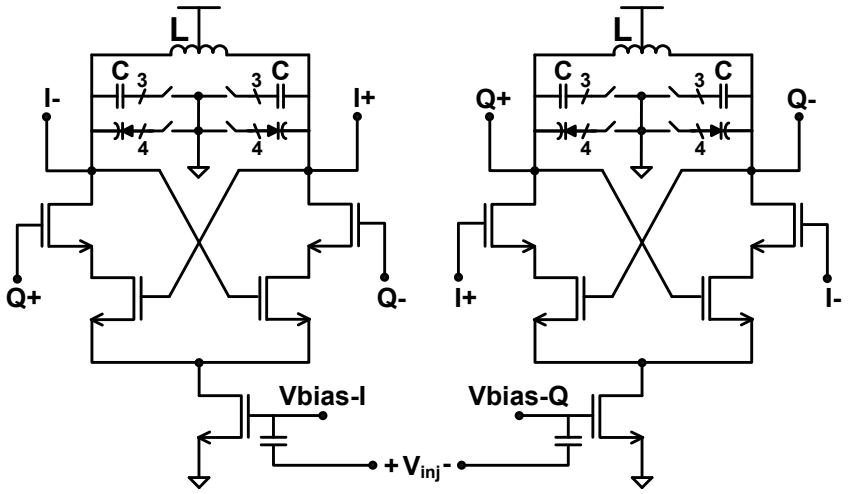


Figure 8.2: S-QDCO topology used in the prototype design

In this architecture a SQVCO is chosen since it can achieve both good phase noise performance and phase accuracy. Now the width ratio of the cascode coupling transistor to the negative-g_m cell transistor is a key parameter in the design. The value of this ratio for our S-QDCO design is optimized and chosen to be 7, in order to obtain the desired performance and tuning range. For accurate frequency tuning, each oscillator in the S-QDCO uses 3 bits for MIM-capacitor control for larger frequency jumps and 4 bits of switched varactor control for finer frequency tuning. As shown in Fig. 8.3, simulation of the extracted layout of the S-QDCO shows an overall tuning range from 3.34 to 4.7 GHz. The simulated phase noise is better than -120 dBc/Hz at 1 MHz offset when operating at 3.34 GHz. Introducing a 0.1% mismatch between the two LC-tanks in simulation, deteriorates the quadrature error by less than 1° showing the topology's resistance to phase error.

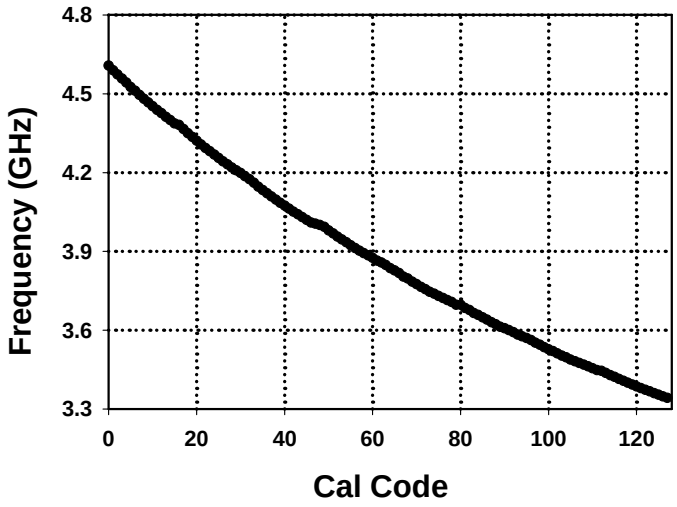


Figure 8.3: Simulated tuning range

8.1.2 Pulse Generator

The pulse generation circuit is shown in Fig 8.4. A single-ended sine-wave input is first converted into a fast-rising differential square-wave. This square wave is pulse-slimmed by using an AND gate the inputs of which are the signal and its delayed version. The key parameter in the design is the delay which controls the width of the output pulse. This has to be optimized to maximize the signal at the required harmonics.

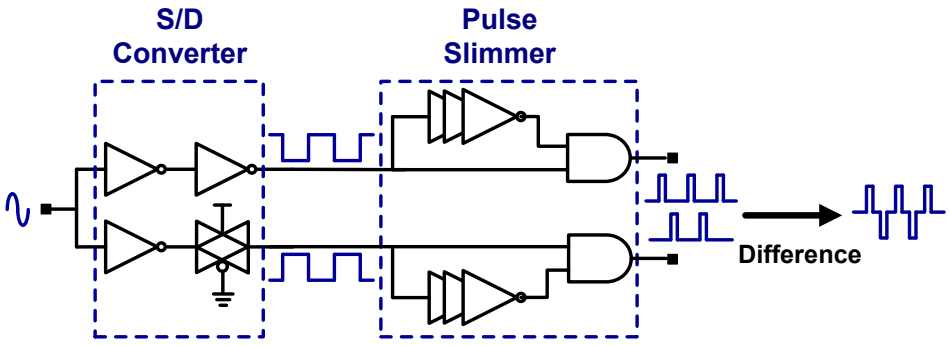
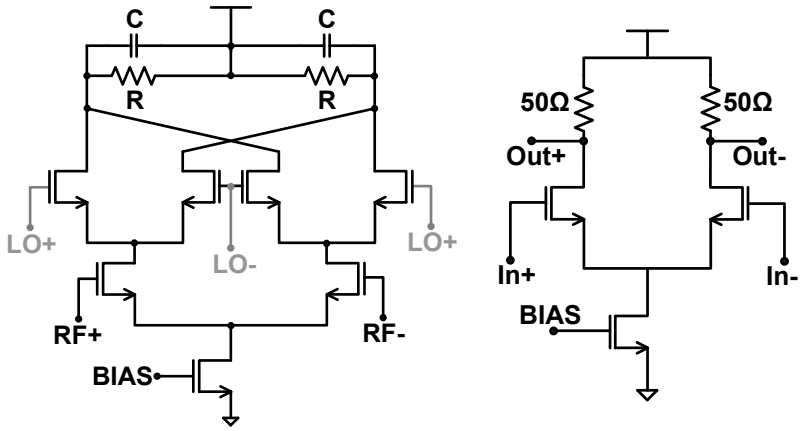


Figure 8.4: Pulse generator

8.1.3 Auxiliary Circuits

The rest of the circuits on the prototype design, shown in Fig. 8.1, are for test purposes only. The quadrature outputs of the frequency synthesizer are 50 Ω-buffered onto GSSG probe-pads for RF probing. Two separate double-balanced mixers with RC-loads, for in-phase (I) and quadrature-phase (Q), down-convert the quadrature output signals to a intermediate frequency (IF) signals, using an externally-applied RF signal. These IF-I and IF-Q signals are driven off-chip using 50 Ω-buffers for oscilloscope measurement. They are then sampled at high-frequencies to estimate quadrature accuracy. The double-balanced mixer and 50 Ω buffer topology are illustrated in Figs. 8.5a and 8.5b. In the next section, we discuss the measurement results obtained from the fabricated prototype.



(a) Double-balanced Gilbert mixer (b) 50 Ω output buffer

Figure 8.5: Auxiliary circuits

8.2 Measurement Results

The proposed architecture is fabricated in a 0.13-μm SiGe BiCMOS process, but all the circuits are CMOS-only. The die micrograph of the fabricated prototype is shown in Fig. 8.6. The active area occupied by this architecture is 0.27 mm^2. The complete frequency synthesizer, excluding auxiliary circuits, buffers and bias circuits, consumes

14.5 mW of power.

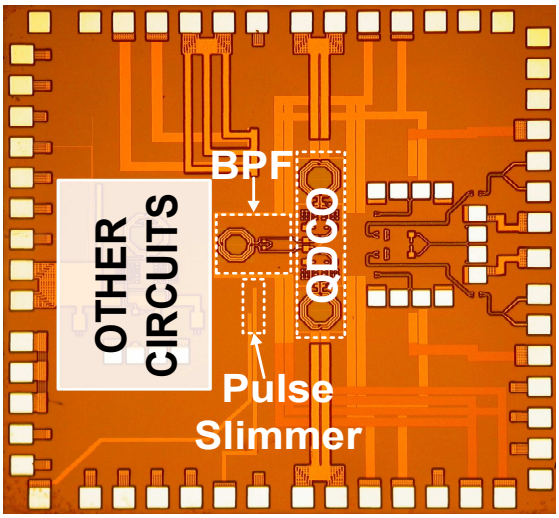


Figure 8.6: Die micophotograph of the CMOS transistor only prototype designed in a SiGe BiCMOS process

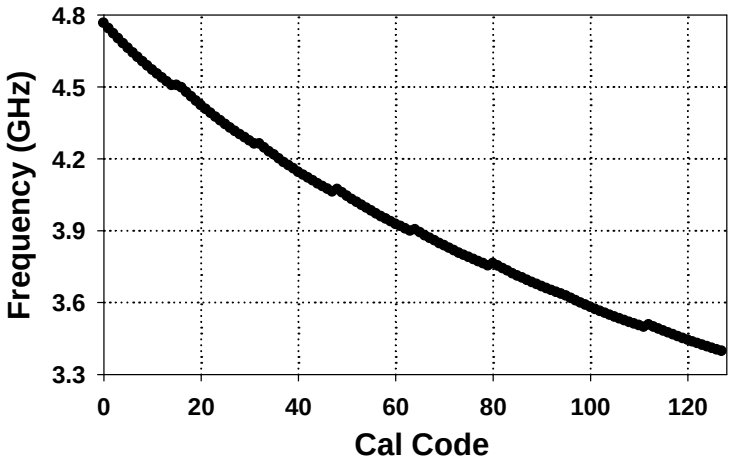


Figure 8.7: Measured frequency vs. calibration code for the QDCO

The measured frequency tuning range of the QDCO is shown in Fig. 8.7. At the lower-end of the tuning range, each frequency step is about 7 MHz, whereas at the higher end, this step size increases to about 20 MHz. The tuning range corresponds well with simulation results shown in Fig. 8.3 and the slight discrepancy is due to the

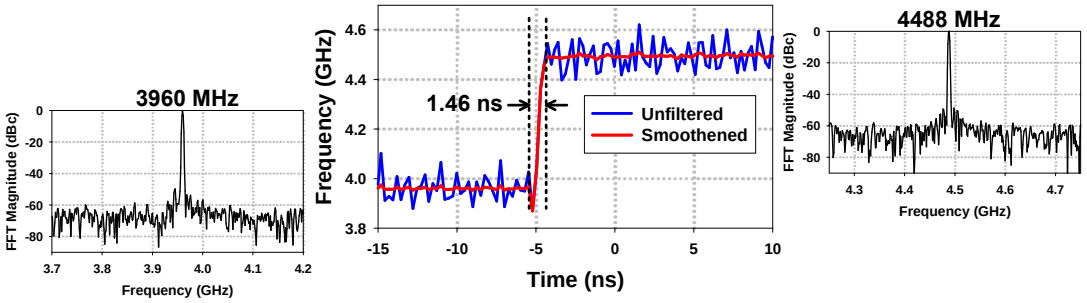


Figure 8.8: Frequency transient corresponding to 15th and 17th harmonic (3960 and 4488 MHz); FFT plots alongside show the accuracy of the frequency jump

overestimation of parasitics in RC extraction. With the injection frequency set to 528 MHz and the MUX switching frequency set to 100 kHz, the locked frequency synthesizer hops across the three different frequencies of the first band-group of the WiMedia-UWB specification - 3432, 3960 and 4488 MHz. The output is RF probed and sampled on a 40 GS/s Agilent DSO81204A real-time oscilloscope to obtain the transient data. The instantaneous frequency is then calculated from period-to-period zero crossings. The switching transient for the frequency jump from the 15th harmonic (3960 MHz) to the 17th harmonic (4488 MHz) is shown in Fig. 8.8. The normalized FFT of the transient data before and after the jump shows the locked frequencies. The frequency hop time for this particular transient is about 1.46 ns. Figs. 8.9 and 8.10 show the frequency switching times for two other sets of frequencies. Their corresponding lock times, as shown, are 1.64 ns and 2.44 ns, respectively. Each of these three plots show the frequency transient of the raw data (in blue), as well as the smoothed transient (in red) obtained by performing a moving-average operation on the raw data.

The phase noise for the unlocked and locked condition of the QDCO at 4488 MHz (unlocked frequency is 4492 MHz) are shown in Fig. 8.11. At 100 kHz and 1 MHz offsets the phase noise for unlocked oscillator are -80.51 and -106.87 dBc/Hz, respectively. For the locked condition, the measured values for phase noise are -110 and -113.86 dBc/Hz,

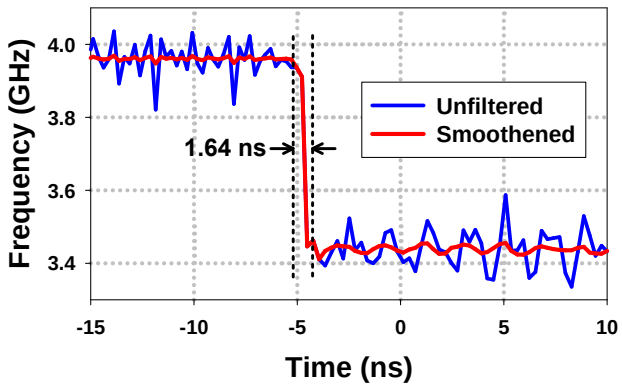


Figure 8.9: Transient frequency jump from 3960 to 3432 MHz

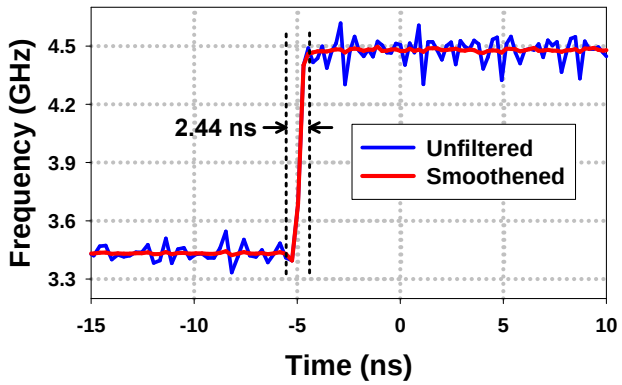


Figure 8.10: Transient frequency jump from 3432 to 4488 MHz

Table 8.1: Spur frequencies (MHz) and spur suppression (in dBc) at output

	Spur Frequencies (MHz)						
Carrier	**3432**	**3696**	**3960**	**4224**	**4488**	**4752**	**5016**
3432	–	31.1	34.5	32.1	35.94	BNF	BNF
3960	42.2	44.5	–	40.5	39.6	BNF	BNF
4488	42.88	46.88	37.41	43.88	–	40.88	32.23

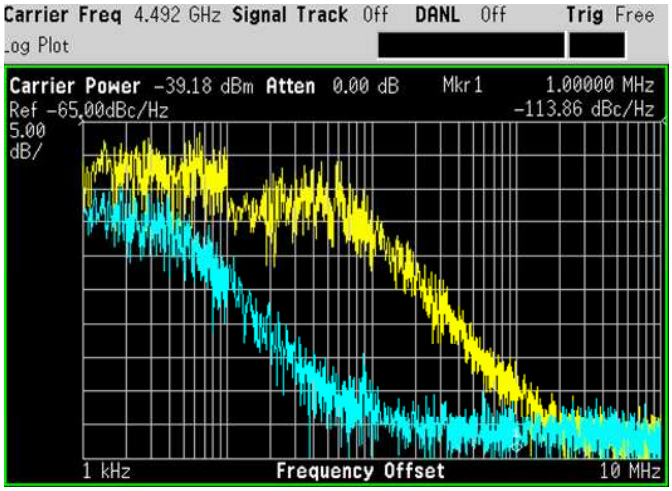


Figure 8.11: Unlocked (4492 MHz, yellow) and locked (4488 MHz, blue) phase noise of the frequency sythesizer

respectively. The injection signal is pulse slimmed, i.e., no longer a perfect square ware, and has both even and odd harmonics and the output was taken single-ended. However, effective suppression of these spurs is essential for the optimal performance of the transceiver. Fig. 8.12 shows measured spurs around the frequency of interest. Table 8.1 lists the spur frequencies and the corresponding suppression attained at the output. The best case suppression attained is about 47 dB, while the worst-case suppression attained is about 31 dB. (BNF: below the noise floor).

In order to measure the quadrature accuracy, the high-frequency synthesizer outputs are down-converted to a 10 MHz IF. Each of the IF signals is sampled at 20 GS/s, as shown in Fig. 8.13. The data is averaged 32 times to filter out the mixer high frequency component. The data is post-processed in MATLAB® to obtain the quadrature numbers. The measured quadrature accuracy for the unlocked QDCO varies between 0.65°-0.67°. In the locked condition, this phase accuracy improves to an average value of 0.45°.

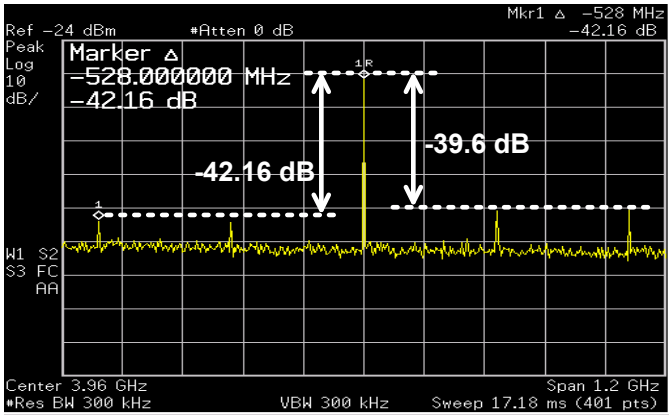


Figure 8.12: Spur suppression around center frequency of 3960 MHz

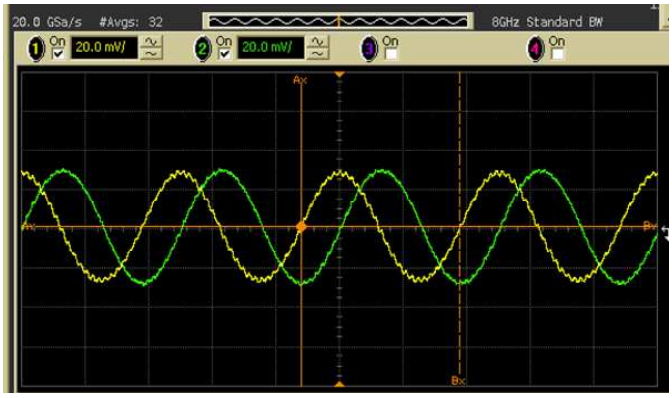


Figure 8.13: I/Q accuracy of the frequency synthesizer, estimated from the down-converted IF-I (yellow) and IF-Q (green) signals

8.3 Chapter Summary

This new architecture for a quadrature frequency synthesizer that is capable of fast-hopping has been presented in this chapter. The fabricated prototype (excluding bias, buffer and auxiliary circuits) dissipates a total power of 14.5 mW. This architecture consumes $1/3^{rd}$ the power of previous state-of-the-art designs [69]. It achieves this by using an injection-locked QDCO at the core. The measured best-case and worst-case spur suppression are about 47 dB and 31 dB, respectively. The measured phase noise of the

locked frequency synthesizer at 100 kHz and 1 MHz offsets are -110 and -113.86 dBc/Hz. The measured frequency hop times for the synthesizer are lower than 2.5 ns, which is compliant with the WiMedia-UWB standard, along with a quadrature error of less than 0.5°. The total active area occupied by the architecture is 0.27 mm^2. Table 8.2 compares the performance of the prototype design with prior work.

Table 8.2: Performance comparison to previously reported architectures

	[52]	**[74]**	**[69]**	**This Work**
Band-Group	#1	#1	#6	#1
Spur Suppression (dBc)	>30	∼35	19-38	31-47
Phase Noise (dBc/Hz, @ 1 MHz)	–	-106	-112	-114
Quadrature Error	–	–	<1°	0.45°
Lock Time (ns)	<2	–	4	1.46-2.44
Power (mW)	186	45	36	14
Area (mm^2)	∼1.1	–	0.074	0.27
Implementation	130-nm CMOS	130-nm CMOS	90-nm CMOS	130-nm CMOS

The low power consumption and the small area occupied by the frequency synthesizer presents the possibility of designing robust low-power UWB transceivers, utilizing multiband-OFDM technology, for next-generation Wireless-USB [6] standard. Since the presented architecture is primarily based on the QDCO, it can be extended to other band-groups by increasing the tuning range of the QDCO [75]. Furthermore, since oscillators can be designed close to the f_T of the transistors, this design can be extended to higher frequencies with limited penalty on power. Fast hopping is required only within band groups so the wide-band BPF center frequency can be made tunable to maintain good spur suppression, with negligible increase in frequency-hop times.

Chapter 9

Conclusions

Conventionally PLLs have been used for carrier frequency generation in wireless circuits and clock generation in wire-line circuits. In this thesis, the injection locked oscillators have been used for this purpose. At this point it would be interesting to examine the ILO against a PLL.

9.1 Remarks on ILOs vs. PLLs

In most transceivers, a large fraction of the receiver power consumption (30%-60%) is in LO generation [52, 76]. This also applies to the transmitter, if we exclude the power amplifier. Typically 40% of the PLL power is consumed by the divide chain and only 10% is used by the VCO [77]. The break down of power consumption of a PLL implemented in a 0.18-μm technology running at 5.6 GHz is shown in Fig. 9.1 and the corresponding pie chart is presented in Fig. 9.2. Here again the CML divider power is the dominant component (48%) of the total power consumption. This is not surprising since VCOs use tuned loads whereas broadband dividers use resistive loads. The case gets worse as the ratio of the frequency of operation to the f_T of the technology increases [49, 78]. Even regenerative dividers, which can operate at higher frequencies than static

dividers require significant power [49]. In fact, most mm-wave PLLs use injection-locked frequency dividers (ILFDs) as their first stage in the division process [79, 80]. However, even at these very high frequencies, the increase in the power overhead due to the VCO is negligible, i.e., VCO power remains roughly constant even as the frequency of operation varies [75]. Moreover oscillators can be designed very close to the f_T of the process. Extremely high frequency oscillators with transistors operating close to this limit have been demonstrated [81].

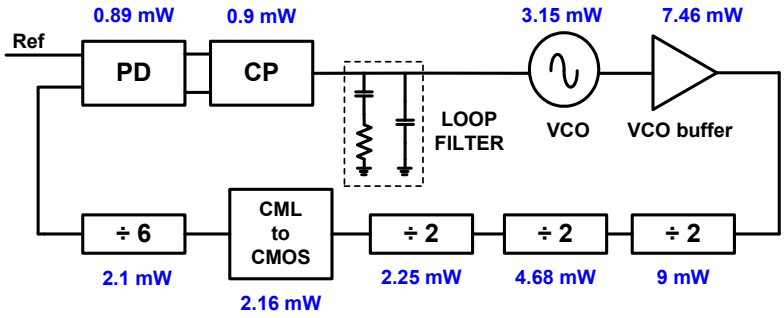


Figure 9.1: Power breakdown in a PLL

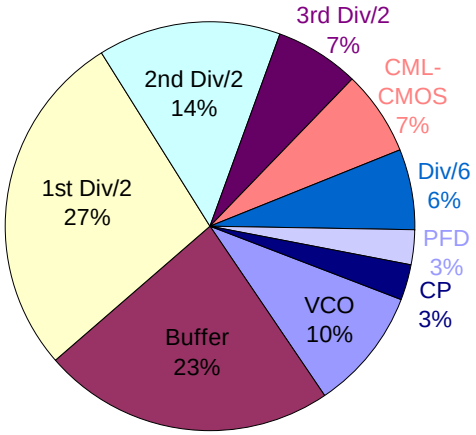


Figure 9.2: Power breakdown in a PLL: pie chart

Injection-locked oscillators behave as first-order PLLs. Interestingly, a first-order

mixer-based PLL operates exactly like an ILO and the system-level equations governing its operation are very similar [11]. Because of their high frequency of operation, ILOs were employed for a long time for the generation and amplification of FM and PM signals [31, 32]. The specifications for FM and PM radios have hardly changed over the years. With the maturity of CMOS technology, they are now met with standard PLL-based radio architectures. However, ILOs are still applicable as a low-power option for systems operating at frequencies where PLLs cannot operate or are too power hungry.

Using the techniques developed in this paper, we show that ILOs are capable of locking extremely fast and are very good candidates for frequency synthesis where fast hopping is required (like WiMedia-UWB). In this aspect, ILOs have distinct advantages over conventional charge-pump-based PLL designs (CPPLL). Since conventional PLLs are bandwidth-limited because of the available reference frequencies, fast hopping is difficult using single PLL designs. The vast advantage in lock-time can also be quantified by comparing the lock-range of an ILO to the loop-bandwidth of a similar-frequency PLL, which the stability rule-of-thumb recommends to be $1/10^{\text{th}}$ the reference frequency [11].

$$\frac{t_{lock\text{-}PLL}}{t_{lock\text{-}ILO}} = \frac{\omega_L}{\omega_{BW\text{-}PLL}} = \frac{5N}{Q}\frac{I_{inj}}{I_{osc}} \tag{9.1}$$

where N is the divider ratio of the PLL and Q is the quality factor of the oscillator tank. Assuming representative values of $Q = 5$ and $I_{inj}/I_{osc} = 1/3$, we can derive that as long as $N > 3$, the ILO will lock faster than a PLL. It should be noted that (9.1) is based only on lock-range-dependent fast-locking of an ILO. With predictive fast-locking, the ratio of lock-times ideally approaches an infinite value because $t_{lock\text{-}ILO} \to 0$.

Additionally, ILOs do not require high frequency dividers (pre-scalars) and so have a significant power advantage (often as large as 10X). Fig. 9.3 plots the frequency (relative to f_T) of various PLLs published in literature against their power dissipation. We observe that stand-alone PLLs which do not use ILFDs consume a lot of power but cannot operate close to the limits of transistor operation. We also see that PLLs using ILFDs

have a significant power advantage. In fact, the PLL design in [80] uses three stages of ILFDs in the divider block, which is the most power hungry component. We believe the most optimal design - high f_{OUT}/f_T and low power (left-most area in Fig. 9.3) - can be achieved by using a low-frequency PLL which sub-harmonically locks an ILO to generate a high-frequency output with similar phase-noise performance.

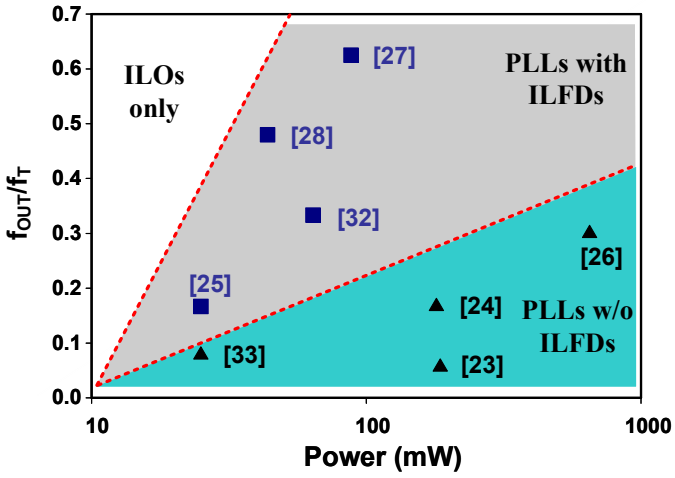


Figure 9.3: Comparison of PLLs and ILOs in terms of relative frequency of operation and power

On the other hand, lock range in ILOs (like the phase-acquisition range in the mixer-based PLLs) shows a strong dependence on the input signal amplitude. CPPLLs do not have this issue [11]. Also, unlike CPPLLs the loop gain of the ILO is finite and so there is a finite steady-state phase error between the reference and output signals (like mixer-based PLLs). This is a non-issue in wireless transceiver design but may not be suitable for wireline clock and data recovery applications. However, with the advent of small feature size CMOS devices, digital calibration techniques can be used to mitigate both of these drawbacks [82].

9.2 Contributions

The research presented in this dissertation shows that injection locking in oscillators is a viable and attractive technique to design fast hopping frequency synthesizers. Almost all the existing proposed architectures for frequency synthesis use multiple PLLs or a combination of multiple PLLs and single sideband mixers. This is expensive both in terms of power and area. Synthesizers based on injection locking that achieve fast frequency switching have also been proposed but no theoretical basis for the fast hopping capabilities have been presented.

In this dissertation a comprehensive theoretical understanding of the transient settling in injection locked oscillators is presented. By solving a simple but powerful nonlinear differential equation, Adler's equation, locking and outside lock behavior in time domain are examined. Lock range of the ILO and the initial phase difference between the injected and oscillator signal are identified as the parameters that determine the lock times.

ILOs are identified to behave like first-order PLLs, and unlike popular CPPLLs which are narrow band for stability issues, the ILO lock range can be made very large. Utilizing the dependence on the lock range, locking times are minimized by expanding the lock range. Low speed discrete oscillator and high frequency integrated LC oscillator measurements validate the findings. Interestingly, even for large lock ranges, the oscillator settling time continues to show a dependence on initial phase of injection. Furthermore achieving large lock ranges is not possible in scenarios with weak injection signal. This leads to the second technique we call predictive fast locking. This technique utilizes the most common application of a fast settling synthesizer where the hop is from one locked state to the other. A novel technique is developed in this thesis to control and match the final steady state phase between the frequency hops, using which almost instantaneous locking is achieved.

Apart from theory for lock time statistics in ILOs, this thesis also examines quadrature voltage controlled oscillators from an injection locking perspective. It is proved that that injection locked quadrature VCOs follow similar statistics as stand-alone VCOs. All the understanding developed so far is used in a novel architecture for a complete frequency synthesizer to meet the requirement of UWB frequency synthesizer specification. By implementing and measuring the architecture at a fraction of the power of existing state of the art, the efficiency of injection locked oscillators as frequency synthesizers is established.

The theory and the techniques developed in this thesis have wide applications where fast frequency switching or fast start-up times are required. In military applications which require frequency scrambling for stealth communication, high data rate wireless applications and clock distribution networks requiring fast startup, ILOs present an attractive and viable low power alternative to conventional (PLL-based) schemes.

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