Design, Simulation, and Optimization of Spintronic Logic Devices

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Dedication

To my wonderful parents.

Abstract

Over the past 50 years, complementary metal-oxide-semiconductor (CMOS) technology has developed aggressively and has undergone continuous scaling, as described by to Moore's Law. However, as transistor feature sizes approach the nanometer scale, there have been growing concerns with escalated power dissipation issues in very large scale integrated (VLSI) circuits, as well as device performance/reliability issues under process variations and aging. Meanwhile, emerging consumer electronic markets such as mobile and distributed computing, the internet of things, and autonomous driving platforms have posed various new challenges for the reliability and performance of electronic systems. While mainstream efforts have pushed forward scaling in CMOS technologies, there has been growing research interest in search for replacements for CMOS. Such efforts involve conceptualizing computational devices, based on new physics principles and new materials, that could serve as fundamental building blocks for new architectures, providing diversified computational functionality and offering better performance than the traditional CMOS-based paradigm.

Among these beyond-CMOS technologies, spintronics is one of the most promising candidates for building next-generation logic devices. Spintronics takes advantage of an intrinsic property of electrons, spin, and develops the concept of state based on magnetism, which is a physical manifestation of electron spin. However, this new technology requires new simulation frameworks and design methods to be developed and deployed in order to propose and evaluate the potential of new spin-based devices, accounting for the impact of novel material properties that dictate the performance of these devices. Such frameworks can further be employed in determining the dependence of circuit performance on material and device parameters, and in optimizing these new technologies.

The first part of the thesis provides a brief review of spintronics and explains a set of physical effects that are exploited to build spintronics-based devices descried in the later chapters. These include spin transfer torque (STT), which forms the basis for early spin-based logic devices, with its associated concepts of spin polarized current and non-local spin valve structure; the magnetoelectric (ME) coupling effect that provides low power and fast switching of magnetization in a ferromagnet (FM) with multiferroic material

stacks; domain wall (DW) structures in FMs that can be used for logic transfer; and inverse spin orbit coupling (ISOC) effects, which offer convenient conversion between spin and charge states.

The second part of the thesis develops performance optimization techniques for all-spin logic (ASL) devices. A framework for simulating ASL devices is first described, and a method for performance optimization through device sizing is developed. An algorithm for optimal device sizing, based on the geometrical dependence of the energy and delay for the ASL device, is then developed. The results of optimization on standard circuit benchmarks, implemented with ASL gates, are shown and the energy/delay trade-off relation is explored.

The third part of the thesis introduces a new device, composite oxide magnetoelectric logic technology (CoMET), and the role played by this thesis research in developing the device. CoMET employs DW as the logic transfer medium and uses the ME coupling effect as well as its inverse effect to realize fast DW creation and detection. A composite structure with magnetization coupling existing between in-plane FM and perpendicular FM is added to the input end of the device in order to further lower the energy of the nucleation process. A detailed study of how this device nucleates a DW at the input end is conducted, and it is demonstrated how input nucleation can be performed in a fast and power-efficient way, leading to a high-speed, low-power CoMET device implementation. The pinning effect with random artificial defects of various sizes is discussed to show how such defects mitigate DW oscillation after nucleation. Such oscillations are seen in idealized defect-free DW structures that are typically simulated by researchers using micromagnetic simulators.

The final part of the thesis studies the magnetoelectric spin orbit coupling (MESO) device that was recently proposed by researchers at Intel [1, 2]. The thesis presents a simulation framework and evaluates the performance of the device through detailed modeling, analysis and simulation. It is shown that when devices are cascaded, potential sneak path could corrupt the computation, and solutions to avoid this problem are proposed. To extend MESO to build general logic, two majority gate designs, based on a DW majority and a charge-based majority, are demonstrated and evaluated. It is shown under some scenarios, the charge-based majority gate may not provide correct output values and must be carefully designed to avoid these scenarios.

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Chapter 1

Introduction

Integrated circuits (ICs) constitute the core of almost all modern electronics machines that influence our day-to-day lives, from laptops, smartphones, medical devices, to emerging autonomous vehicle and virtual reality/augmented reality applications. The market of consumer and industrial electronics has increased tremendously with larger demands for systems of higher performance or lower energy cost [9, 10]. Such demands have kept driving the development of traditional CMOS technology according to Moore's law [11], which states that in approximately every two years, the number of transistors in a dense IC doubles. This doubling trend has been achieved through shrinking the feature size of transistors down to today's nanometer scale, where process technologies approach manufacturing limits and quantum-mechanical physics boundaries.

As researchers keep on pursuing ways to continue CMOS scaling in order to stretch Moore's Law ("More Moore"), efforts have been made to seek solutions in various technologies that could provide diversified functionalities to current ICs ("More than Moore") [12]. Spintronics, as one of the "More than Moore" technologies, stands out with its unique features as a promising candidate for next general logic device in the post CMOS era.

1.1 Challenges to CMOS circuits

As traditional CMOS technology has scaled down to nanoscale-dimension transistors, many problems have emerged along the path of scaling-as-usual. One of the major

challenges as we move to atomistic dimensions is the increase in leakage. Phenomena such as short channel effects and drain-voltage-induced barrier lowering increase the leakage current severely and decrease the on/off current ratio, leading to power density issues. In addition, at these greatly shrunk dimensions, it is impossible to control the manufacturing process precisely, and this leads to variations in device characteristics. These are expressed as stochasticity in the actual device geometries, which may incur a wide span of statistically distributed device characterisitics, such as large variations in the oxide thickness, threshold voltage, or critical dimension, affecting performance, as well as aging effects that degrade reliability. Research in the fields of material science, condensed matter physics, or even quantum physics is needed to mitigate or even to bypass these problems with intrinsically different physical mechanisms to achieve better device performance in successive generations of technology.

1.2 Spintronics

Spintronics provides one of the most promising avenues for building next-generation logic devices. Spintronics is based on exploiting an intrinsic property of electrons, their spin, and using it as another degree of freedom besides the charge state of electrons to design novel electronic devices.

1.2.1 What is spin?

In the study of condensed matter physics, spin is an intrinsic property of particles that represents the angular momentum of the particles. The existence of such angular momentum is inferred from experiments in 1920s [13]. There are two basic possible "directions" for the spin of an electron as up-spin or down-spin as shown in Fig. 1.1.

In our work, we focus on the interactions between the spin of electrons and its environment in materials, which involves a series of effects in the spin transport, spin dynamics and spin relaxation process. Very often, these effects are associated with ferromagnets (FMs), the materials that demonstrate ferromagnetism, the strongest type of magnetism. The reason behind is that the magnetism, or the magnetization of matter as its manifestation, originates from the spin of electrons. To be more specific, magnetism of a material is a collective expression of the magnetic dipole moments in it.

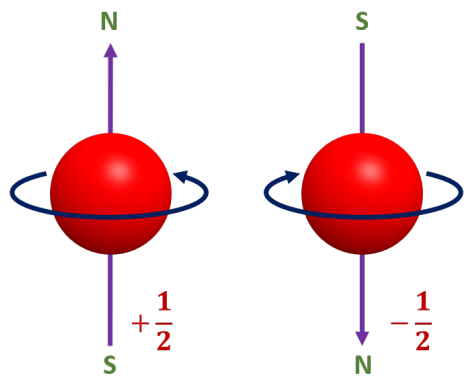


Figure 1.1: Two types of electron spin: spin up and spin down.

This magnetic dipole moment behaves like a tiny magnet producing a magnetic field. It partially comes from the more fundamental property of electron, which is the possession of quantum mechanical spin. Therefore, many of the spin-based effects take place in the FMs, which makes the study of ferromagnetic materials an indispensable part of spintronic research.

1.2.2 Advantages of spintronics

Spintronics-based circuits possess several advantages that can be beneficial in device level operations. These include:

- *Non-volatility.* The magnetization in the FMs can be preserved after modifications without the need of any form of power supply. This is naturally useful in building memory devices [14], and can also be exploited in the domain of logic operations [15].

- *Low power.* Changes of logic states stored in FMs can be realized with low power cost by ME coupling effect [16] with better energy scalability as device dimensions shrinking in the future [1, 2]. Logic transfer using DW as medium is an attractive option with proper material engineering to achieve automotion [17]. The spin orbit coupling (SOC) effects such as spin Hall effect (SHE) and Rashba-Edelstein effect (REE), together with their inverse effects, provide efficient conversions between spin and charge states with minimal energy cost.

- *Natural implementation of majority logic.* It is easier to construct a majority with many spin-based devices because of their underlying computation mechanisms. Structures with odd number of input branches could be constructed with proper materials to realize DW competing or STT current cancellation, leaving the majority logic represented by these spin states at the output end [18, 19].

Benefiting from the advantages listed above, the research of novel spintronic computing paradigm keeps drawing more attention. In 2010, the proposal of ASL device [20–24] is a major milestone in the development of spin-based logic device. With a close examination of the ASL device model, we discovered a trade-off relation between energy and delay due to their dependence on the device geometries and proposed a sizing algorithm for performance optimization suitable for standard circuit benchmark simulations.

Inspired by the work associated with DW automotion [17, 25] combing with ME coupling effect for low power nucleation, a joint work with faster DW propagation based on current driven DW motion mechanism is proposed [26]. It paves the way for the jointly proposed CoMET device [27] elaborated in this thesis. This device takes a further step in lowering energy by introducing a composite FM structure at the input end of the device channel and leveraging the coupling existing in the structure. In addition, a detailed study on the nucleation process with various up to date material parameter combinations further improves the nucleation speed. On the other hand, a series of simulations conducted with structural defects provide insights to the pinning effect that may give better control of DW states. My work on the above low power DW nucleation scheme, combined with the DW propagation scheme and logic cascading, developed by another member of my research group, makes the CoMET device one of the most efficient spin-based computing paradigms proposed so far.

With new advancements in the study of SOC effects [6, 7, 28–30], more research efforts have been seen on applying these effects in spin-based logic computing, among which the MESO device [1, 2] has drawn much attention. The research we have done in this thesis provides a simulation framework based on the device modeling. Analysis of the device performance is achieved using this framework. We identify a potential sneak path issue and show how this could jeopardize the computation when MESO gates are cascaded. Two majority gate schemes are proposed, which enriches the functionalities that the MESO device could achieve.

Our work in this thesis addresses multiple aspects of the spintronic-based computing research, including the device design for high efficiency in functionalities, the simulation framework for convenience with large scale benchmarks or various parameter choices, and the optimization algorithms for effective improvement of device performance. The research contribution in this thesis has undoubtfully advances the state of the art in spintronics.

1.3 Thesis organization

The thesis is organized as follows:

- Chapter 2 introduces a set of commonly seen spintronic effects that are used in spin-based devices discussed in this thesis.
- Chapter 3 first describes a framework for simulating ASL devices, followed by proposing a method for performance optimization through device sizing. Algorithms for optimal device sizing, based on the geometrical dependence of the energy and delay for the ASL device, are then developed. The results of optimization on standard circuit benchmarks, implemented with ASL gates, are shown and the energy/delay trade-off relation is explored.
- Chapter 4 explains our joint proposal of CoMET device, and the role played by this thesis research in the its development. CoMET employs the DW as the logic transfer medium, which inevitably involves both nucleation and propagation. However, this thesis focuses more on my research work for the optimization of the DW nucleation process. For the purpose of evaluating the whole device performance, a brief introduction to the propagation and device cascading schemes and results is given since it belongs to the work of another member from my research group. In order to further lower the energy of the nucleation process by the ME coupling effect, a composite structure with magnetization coupling existing between in-plane FM and perpendicular FM is added to the input end of the device. A detailed study demonstrating how input nucleation can be performed in a fast and power-efficient way through exploring the material parameter space is presented.

In addition, the DW pinning effect with random artificial defects of various sizes is discussed for mitigating DW oscillation after its nucleation.

- Chapter 5 presents a simulation framework the recently proposed MESO device and evaluates its performance through detailed modeling, analysis and simulation. It is shown that when devices are cascaded, potential sneak path could corrupt the computation, and solutions to avoid this problem are proposed. To extend MESO to build general logic, two majority gate designs, based on a DW majority and a charge-based majority, are demonstrated and evaluated. It is shown under some scenarios, the charge-based majority gate may not provide correct output values and must be carefully designed to avoid these scenarios.

- Chapter 6 concludes the thesis.

The bibliography is provided at the end of Chapter 6, followed by four appendices. The modeling of spin transfer process by modified nodal analysis method is elaborated in the first appendix. The second appendix provides the derivation of switching time t_{sw} for ASL device in Chapters 3. For FE capacitor, we demonstrate its hysteresis loop as well as the remnant polarization in the third appendix to support our work in Chapter 5. The last appendix shows the rise and fall transition for a single MESO inverter for better readability.

Chapter 2

Background on Spintronic Effects

As spintronics has made major inroads as a viable technology for building electronic systems, several spin-based physical effects have been discovered and/or evaluated for their potential in creating next-generations devices. In this chapter we will introduce several spin-based effects that are used in the logic device structures discussed in this thesis.

2.1 Nonlocal STT effect

Originally suggested by Berger [31] and Slonczewski [32], the spin-transfer torque (STT) effect is one of the most important spin-based effects used in new both memory and logic device concepts during the past two decades [33–37]. In simple terms, the STT refers to an effect in which the orientation of a magnetic layer in a spin valve can be modified using a spin-polarized current [35]. However, to understand the mechanism behind STT, we need to introduce two important concepts, spin-polarized current and the notion of nonlocal spin valve as well.

2.1.1 Spin-polarized current

Traditional charge current is in a spin neutral state, meaning that the composition of spin-up and spin-down electrons in the current is equal. However, the current becomes spin-polarized when there is an imbalance in the quantity of spin-polarized electrons. For example, when a spin-neutral current passes through a FM with fixed magnetization

(often called "fixed layer"), the electrons that pass through the FM are largely composed of only one type of spin carrying the same type of spin angular momentum due to the interactions between the FM and electrons, depending on the orientation of the fixed magnetization. Electrons with the opposite spin polarity, or in other words, different spin angular momentum, are reflected back by the magnet. Therefore, the current that pass through the magnet and the current that is reflected back are both spin-polarized, as illustrated in Fig. 2.1.

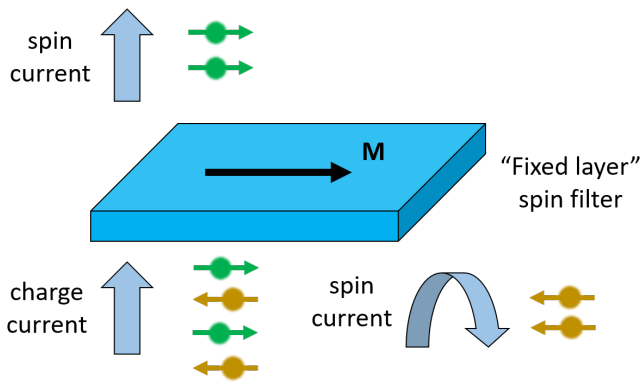


Figure 2.1: A charge current passing through a "fixed layer" results in two polarized spin currents: one that passes through the magnet and one that is reflected back.

When a spin-polarized current is through a FM with more flexible magnetization, the magnet will absorb a portion of the spin-angular momentum carried by the electron spins in the current. A torque rises from this absorption and is exerted on the FM to change its magnetization. This torque applied by non-equilibrium conducting electrons in a spin-polarized current is therefore called STT.

2.1.2 Nonlocal spin valve structure

The nonlocal spin valve structure typically consists of a nonmagnetic channel connecting two magnetic layers. The magnetization of one layer is pinned and therefore is considered as a "fixed layer", and the magnetization of the other layer can be changed freely and therefore is called "free layer". An example of such a structure is shown in Fig. 2.2, with an injector at the right and a detector at the left. When a positive or negative charge current is passing through the injector's fixed layer, it will be polarized by the magnetization in the fixed layer. The injected spin current will propagate through the

channel and switch the magnetization of the free layer at the detector due to the angular momentum carried by its electrons. This structure was first experimentally reported in [3, 38] and has been under actively research [39, 40].

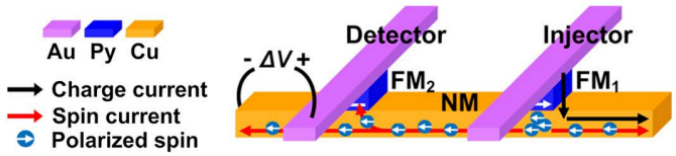
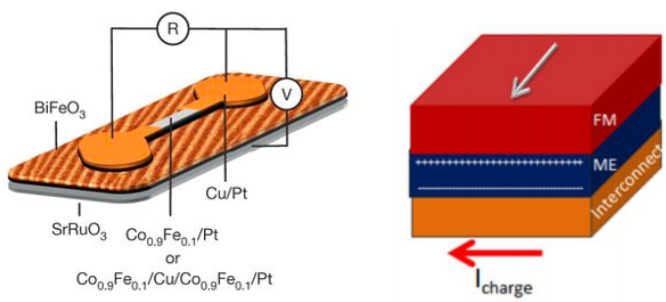


Figure 2.2: Non-local spin valve experiment [3].

The phenomenon whereby the orientation of a magnetic layer in a nonlocal spin valve structure can be changed by a spin-polarized current generated through another layer is referred to as nonlocal STT switching. As we will see in Chapter 3, it forms the foundation of ASL device.



(a) (b)

Figure 2.3: (a) A schematic for a ME device with $BiFeO_3$ beneath a spin valve [4]; (b) A proposed ME material stack for conversion from charge current to magnetization [1, 2].

2.2 The ME coupling effect

The magnetoelectric (ME) coupling effect in general refers to the coupling between magnetic and electric orderings in the materials. It has gained much attention and been under active research due to its potential in low-cost and fast magnetization switching under the application of an electric voltage [41, 42]. The inverse ME effect that reverses electric polarization reversal under a magnetization change has also been intensively studied. There are multiple identified sources for ME effects in a single material or a

heterostructure [43], including a product property of a magnetostrictive and a piezoelectritive compound, charge transfer, and exchange bias at the interface [16,44]. Typically, a heterostructure rather than a single material demonstrates a stronger ME effect. The material stack exhibiting such large ME effects usually consists of a layer of ferroelectric material (e.g., $BiFeO_3$ [4]), serving as a capacitor for creating an electric field, and an adjacent layer of ferromagnet material whose magnetization will be switched by the change in the induced magnetic field, as shown in Fig. 2.3. The Landau-Khalatnikov (LKh) equation is used to describe the response of the electric polarization to the excitation with time in the FE capacitor [45]. Such material stacks will be used in our devices proposed and analyzed in Chapter 4 and Chapter 5, with the coupling relation between electric polarization and effective magnetic field elaborated in Chapter 4.2.

2.3 DW nucleation and propagation in FMs

A domain wall (DW) is the interface region between two magnetic domains with different magnetization orientations, as shown in Fig. 2.5(a). The magnetization inside this region undergoes a transition as it is reoriented from one magnetization to its opposite direction. The orientation transition pattern and the DW width depend on the properties of the material, such as anisotropy and the exchange constant.

2.3.1 FM with different types of anisotropy

For a magnetic material, the magnetic anisotropy indicates the inclined direction of its magnetization. Often in thin film FMs, multiple types of anisotropy exist in the material, and their relative strengths determine the orientation of spontaneous magnetization. Under no external excitation, the magnetization will align with an easy axis in either one of its two directions, which is favored in the low energy state. A ferromagnetic material is defined as an in-plane magnetic anisotropy FM (IMA-FM) when the easy axis is in the plane of the thin film, as shown in Fig. 2.4(a). Similarly, for a perpendicular magnetic anisotropy FM (PMA-FM), the easy axis is perpendicular to the thin film plane, as in Fig. 2.4(b). In our work, we focus on PMA-FM rather than IMA-FM since it is more robust to DW pinning and surface roughness effects when used for logic propagation [46–48].

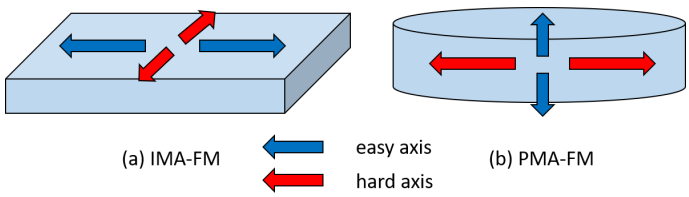


Figure 2.4: (a) FM with in-plane magnetic anisotropy; (b) FM with perpendicular magnetic anisotropy. The hard axis for IMA is also in the plane of the FM. It corresponds to the halfway point of switching: switching in an IMA-FM is predominantly within the plane.

2.3.2 Types of DWs in IMA-FM and PMA-FM

The magnetization transition patterns in a domain wall are characterized in terms of four different types of DWs in IMA-FMs and PMA-FMs: the transverse wall and the vortex wall for IMA-FM, illustrated in Fig. 2.5(a) and 2.5(b), and the Bloch wall and the Néel wall for PMA-FM, illustrated in Fig. 2.5(c) and 2.5(d), respectively. Magnetization for the two types of DWs for IMA-FM both stay inside the plane of the material and commonly exist in thick structures. The magnetization in the Bloch wall rotates out of the magnetization plane of the two domains on either side, and is also usually seen in thick structures. In thin films, Néel wall is more common, and its magnetization transition occurs within the magnetization plane of the two domains.

2.3.3 DW nucleation and propagation

A DW may be nucleated through various effects such as current-induced magnetic field switching or STT switching [49]. Our work in Chapter 4 propose the usage of the ME coupling effect for nucleation with a composite structure of IMA-FM and PMA-FM. The ME effect is essentially modeled as an effective magnetic field caused by voltage drop on the FE capacitor on top. This effective magnetic field then switches the magnetization in its adjacent composite FM material structure and creates a DW. The presence of an IMA-FM next to the PMA-FM allows further reduction in nucleation energy, as will be elaborated in Chapter 4.3.

The propagation of a DW is achievable through different methods [49] such as DW automotion [17] or current-driven motion [26, 50, 51]. DW propagation is useful in

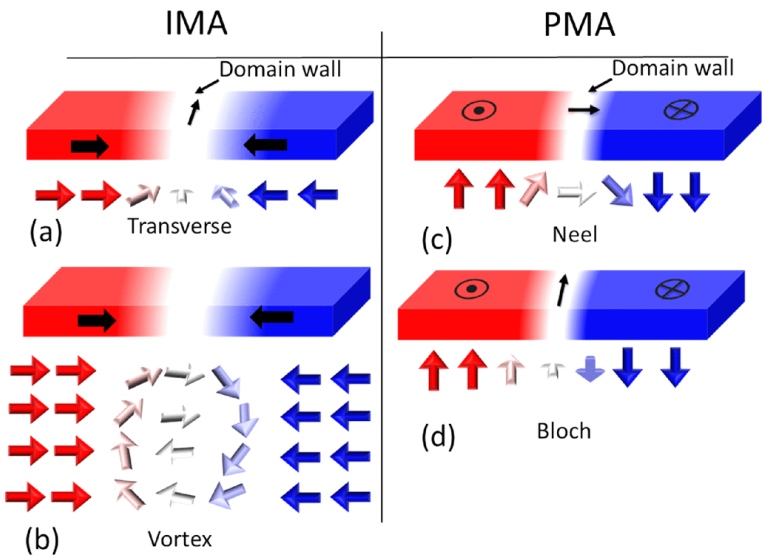


Figure 2.5: Typical DW structures [5]. (a) A head-to-head transverse DW in IMA-FM, where the magnetization rotates perpendicular to the wire's long axis. (b) A vortex DW in IMA-FM where magnetizations form a vortex around the DW. (c) A Néel wall, where the magnetization rotates along the wire's long axis. (d) A Bloch wall, where the magnetization rotates perpendicular to the wire's long axis.

transporting a magnetization spatially along a channel, making it a good candidate for efficient logic transfer within a gate, or between gates when combined with other mechanisms of creating and detecting the reorientation in the ferromagnetic material. With the proper design of a structure with multiple input branches for DW merging, DW propagation may even be used to realize a majority computation functionality by taking advantage of its analog nature [18].

2.4 The ISOC effect

The spin orbit coupling (SOC) effect is essentially the interaction between the spin of moving electrons and the potentials inside the material. In this thesis, we focus on two different types of spin-orbit coupling effect, SHE [52] and REE [7, 53].

The SHE is the phenomena that electrons of opposite spin accumulate on the two planes perpendicular to the direction of the injected charge current and is often observed in heavy metal, topological insulators, and 2D materials [1, 6]. An example of a SHE

device with measurement circuit is shown in Fig. 2.6(a). This allows a spin current to be formed between the planes with opposite spin accumulations and therefore suggests a charge to spin conversion process. If the injected charge current direction is reversed, the direction of spin current will also be reversed. This effect can also happen inversely: with a spin current injected into the material, a charge current could be generated along the perpendicular direction to the spin current. A similar coupling relation between the directions of spin current and charge current also exists in the inverse SHE (ISHE), which provides us a convenient method for spin to charge conversion. The REE and the Inverse REE (IREE) provides similar directional coupling relation between spin and charge current conversion but happens mostly at the interface of materials. Fig. 2.6(b) shows a schematic of an experiment device that uses the REE.

These two effects are together referred to as the inverse spin orbit coupling (ISOC) effect, and they facilitate the spin-to-charge conversion process as proposed in [1,2] and shown in Fig. 2.6(c). With proper material stack, fast detection of magnetization and conversion into charge voltage could be realized as we will see in Chapter 5.

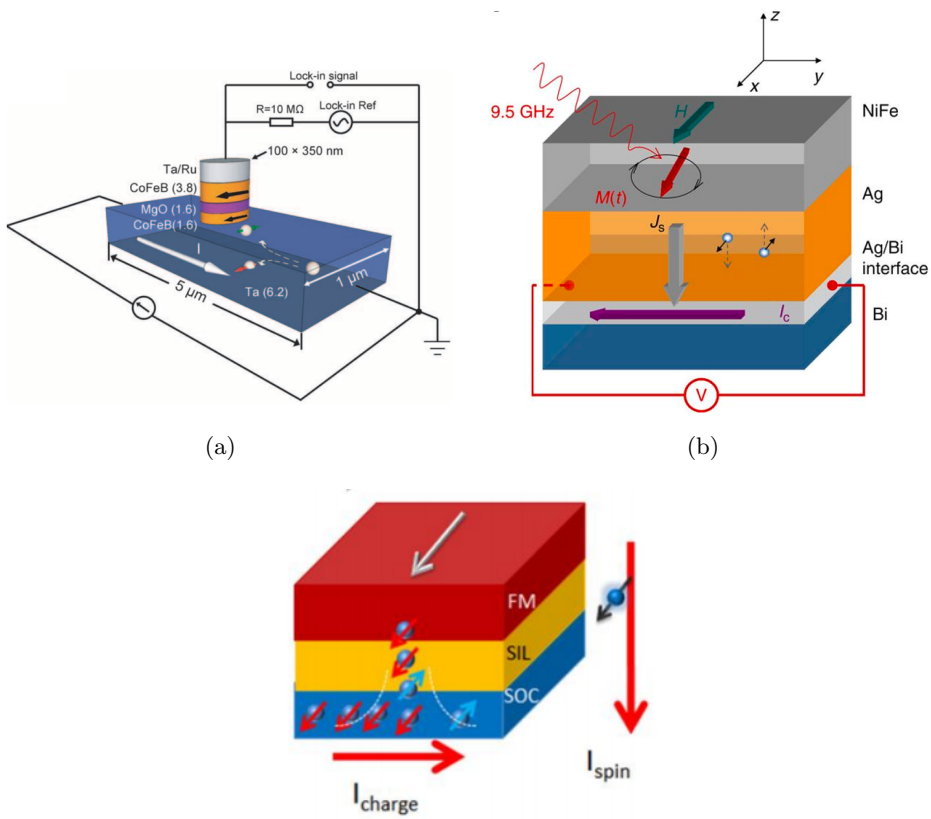
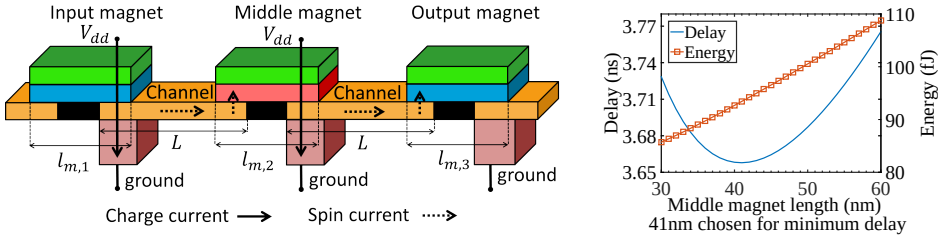


Figure 2.6: (a) A schematic of SHE enabled MTJ switching device and measurement circuit [6]; (b) A schematic of a device for detecting interface REE with Ag/Bi stack beneath a spin pumping NiFe unit [7]; (c) A proposed ISOC material stack for conversion from spin current to charge voltage [1, 2].

Chapter 3

Energy/Delay Trade-offs in ASL Circuits

As mentioned in Chapter 2.1, for spin-based logic, nonlocal STT devices are very promising, particularly All-Spin Logic (ASL) [8, 17, 20–22, 54, 55].



(a) (b)

Figure 3.1: (a) A three-magnet/two-channel ASL circuit. (b) Its energy and delay.

In this chapter, we study methods for improving the performance of ASL circuits through careful selection of the dimensions of circuit elements, resulting in energy-delay tradeoffs. To motivate the problem, consider an ASL structure with three magnets connected by two separated channels in Fig. 3.1(a). We fix the dimensions of the input/output magnets and channels and examine the energy and delay impact of changing the length, $l_{m,2}$, of the middle magnet, temporarily assuming that this value can be varied continuously. Increasing $l_{m,2}$ increases energy at both the input and output sides.

However, the delay impact is nonmonotonic: the time required to switch the middle magnet increases because a larger magnet requires more spin torque, but the switching time of the output magnet reduces since a larger middle magnet can deliver more spin torque. Thus, there is an overall energy/delay trade-off relation, as shown in Fig 3.1(b). Further, the choice of channel length also affects switching speed in such nonlocal spin valve structures [56–58], implying that buffer insertion in a long interconnect can help in reducing wire delays.

The major contribution of our work is in developing and assembling a modeling and optimization framework for performance optimization of general ASL circuits through magnet sizing and buffer insertion, and the demonstration of the energy/delay trade-off relation during the optimization. We introduce energy and delay models for ASL circuits (Chapter 3.1) and show the impact of geometric parameters on performance (Chapter 3.2). An optimization problem formulation is proposed (Chapter 3.3) to obtain energy-delay tradeoffs. We show results on a long interconnect line and large benchmarks under multiple technologies (Chapter 3.4) and conclude in Chapter 3.5.

3.1 ASL performance modeling

3.1.1 Structure of a basic ASL gate

A basic ASL gate [20] consists of three major components as shown in Fig. 3.2: an input magnet at left that polarizes the charge current and injects spin current into the channel, a channel that transfers the spin current from input magnet to output magnet, and an output magnet that sets its state based on the incoming spin torque. A metal contact, connected to the supply voltage, lies above each magnet, and a ground connection is placed beneath the input end of the channel. To allow a magnet to serve both as output to its previous magnet and input to its following magnet, an isolation feature is placed under it, separating the part of the channel beneath the magnet into two segments – an input and an output side – thus ensuring that the input and output spin currents interact minimally. Since this is a drawn feature, its size is constrained by lithography and corresponds to the minimum feature size.

For the ASL inverter in Fig. 3.2, at the input side, a charge current (solid arrow) flows from V_{dd} to ground. The polarizing action of the input magnet results in a spin

accumulation, opposite to the magnet spin, at the input end and this diffuses towards the output (dotted arrow), creating a spin torque at the output end that sets the output magnet state. A buffer is similar in structure, except that the role of V_{dd} and ground are interchanged: this ensures that the input magnet introduces a spin current of the same polarity into the channel.

3.1.2 An analytical model for switching delay in ASL circuits

For the gate in Fig. 3.2, annotated with its geometrical parameters, we consider each contributor to switching: spin current generation at the input, non-local spin transport through the channel, and spin-torque-based switching at the output.

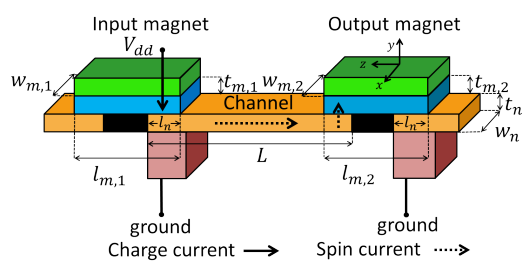


Figure 3.2: Structure of a basic ASL gate.

Charge current at the input magnet

The injected charge current is converted to spin current at the input end of the channel. For the structure in Fig. 3.2, the positioning of the ground terminal on the input side, along with the presence of the isolation feature, introduces an asymmetry that causes charge current, I_c, to be injected to the input side, given by:

$$I_c = \frac{V_{dd}}{R_s + R_m + R_n + R_g} \tag{3.1}$$

where R_s, R_m, R_n, and R_g indicate the resistance of the contact to supply voltage, magnet, channel, and ground connection, respectively, on the input side. The parasitics of both the supply and ground connections are included in the R_s and R_g, ensuring that the ohmic loss associated with power and ground distribution are incorporated in our

models. The other two quantities, R_m and R_n, can be calculated as:

$$R_m = \frac{\rho_F t_m}{A_{F,1}/2}, \quad R_n = \frac{\rho_N t_n}{w_n \cdot l_n} \tag{3.2}$$

where $A_{F,1} = w_{m,1} l_{m,1}$ is the interface area between the magnet and contact, with width $w_{m,1}$ and length $l_{m,1}$. The factor of 2 indicates that only half of the magnet is effectively available for injecting charge/spin current; the other half receives spin current from the gate that drives this magnet. The area $A_N = w_n \cdot l_n$ between the magnet and channel is used for calculating the channel resistance. The parameters ρ_F and ρ_N are the resistivity of magnet and channel, and t_m and t_n are the thickness of magnet and channel, respectively.

Spin transfer through the channel

The charge current at the input magnet is transformed into a spin current at the source end, which drifts down towards an output magnet through a lossy interconnect medium. We capture these factors and arrive at an expression for the input–output delay of an ASL gate. For a single fanout structure, i.e., a channel without branches, such as an ASL inverter or buffer, the spin current can be calculated by an analytical expression for the spin injection efficiency, while in more complicated structures with multiple fanouts, the spin current at each output can be evaluated using numerical computations [8].

The spin injection efficiency, η, is the ratio of the spin current, I_s, at the end of the channel to the injected charge current, I_c. In a single-fanout structure, η is given by [21, 59]:

$$\eta = \frac{I_s}{I_c} = \frac{e^{-L/\lambda_N} x_1 P_1}{(1+x_1)(1+x_2) - e^{-2L/\lambda_N}}, \tag{3.3}$$

where L is the length along the channel from the point of injection of spin current at the input magnet to the channel region below the output magnet, and λ_N is the spin diffusion length of the channel. The terms x_1 and x_2 are defined as:

$$x_1 = \frac{2R_1}{R_N(1-P_1^2)}, \quad x_2 = \frac{2R_2}{R_N(1-P_2^2)}, \tag{3.4}$$

where P_1 and P_2 are the polarization factors for the input and output magnets, respectively, R_1 and R_2 are the spin accumulation resistances for the input and output

magnet, respectively, and R_N is the spin accumulation resistance of the channel. These terms are given by:

$$R_{\{1,2\}} = \frac{\rho_F \lambda_F}{A_{F\{1,2\}}/2} = \frac{2\rho_F \lambda_F}{w_{m\{1,2\}} \cdot l_{m\{1,2\}}}, \tag{3.5}$$

$$R_N = \frac{\rho_N \lambda_N}{A_N} = \frac{\rho_N \lambda_N}{w_n \cdot t_n} \tag{3.6}$$

with λ_F and λ_N standing for the spin diffusion lengths and ρ_F and ρ_N being the resistivities, with subscripts F and N for the ferromagnet and channel, respectively.

3.1.3 Switching the output magnet

The Landau-Lifschitz-Gilbert (LLG) [60] equation describes the magnet switching dynamics due to a spin current:

$$\frac{d\vec{m}}{dt} = -|\gamma|\vec{m} \times \vec{H}_{eff} + \alpha\vec{m} \times \frac{d\vec{m}}{dt} - \frac{1}{qN_s}\vec{m} \times (\vec{m} \times \vec{I_s}) \tag{3.7}$$

Vector $\vec{m}$ indicates the normalized magnetization and changes from 1 to -1 or the opposite during switching over a time variable t, γ is the gyromagnetic ratio, α is the Gilbert damping coefficient, q is the electron charge, and N_s is the net number of Bohr magnetons of the magnet to be switched. The effective magnetization field, $\vec{H}_{eff}$, consists of the uniaxial anisotropy field $\vec{H}_k$ and demagnetizing field $\vec{H}_d$. For in-plane magnet structures, $\vec{H}_k$ is dominated by $\vec{H}_d$.

A complete analysis of the LLG equation is computationally intensive, especially within the inner loop of an optimizer. However, the equation can be used to infer information about the switching time t_{sw} under a spin torque switching current in a computationally inexpensive way. From Equation (3.3), writing the spin current at the end of the channel as $I_s = \eta I_c$, the switching time of the gate is given by [21].

$$t_{sw} = 2f_{sw}qN_s/(\eta I_c) \tag{3.8}$$

where I_c is given by Equation (3.1). The factor f_{sw} captures the fact that the spin current is partly responsible for switching, and the switching event also includes contributions from other related fields. In [21], f_{sw} was considered over a single magnet size, but our optimizer requires f_{sw} over a range of magnet sizes. In Chapter 3.2.3, we will show that f_{sw} is well approximated as a constant over a wide range of magnet sizes.

Delay in multifanin/multifanout structures

General ASL gates are based on majority logic and involve more complex structures than that in Fig. 3.2. For example, Fig. 3.3(a) represents an ASL NAND gate with two fanouts, and the channel has multifanin and multifanout substructures. For such structures, there is no known simple analytical form for the spin current, analogous to Equation (3.3), at the output magnet(s). However, the spin current at each output magnet can be calculated numerically by dividing the channel into wire segments [8].

Specifically, each component in the circuit – the input and output magnets as well as channel segments – can be described as a π–network of conductance matrices. By considering each logic stage separately, we divide this into two substructures and based on the π structures for each stage, illustrated in Fig. 3.3(b), we form a modified nodal analysis (MNA) matrix for the system and solve the resulting set of equations to obtain the charge and spin currents at any nodes. The currents injected into output magnets are then used to compute the spin injection efficiency, replacing the closed form in Equation (3.3), and the remainder of the process of computing t_{sw} is identical to the single-fanout case. A complete description of this interconnect model, along with a comparative evaluation against the analytical model, is provided in Appendix A.

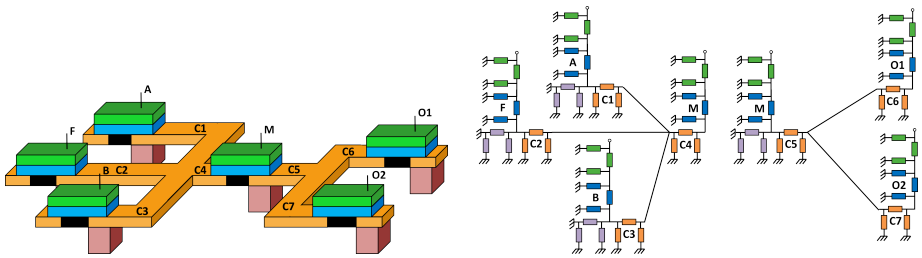


Figure 3.3: (a) A two-input ASL NAND gate with two fanouts [8]. (b) Its lumped circuit model.

From gate delays to circuit delays

Computing circuit delays from gate delays is a relatively straightforward process. As in static timing analysis for CMOS circuits, once the delays of each logic stage (i.e.,

a gate and its fanout interconnect) are computed using techniques described earlier in this chapter, a topological traversal from the primary inputs to the primary outputs can be used to find the delay of the circuit.

3.1.4 Modeling ASL switching energy

For any single-fanout or multifanout structure, the energy that is supplied comes from the V_{dd} source. Over a switching period, T, the total energy E for the gate is given by [21] as $E = V_{dd} I_c T$. Note that the energy dissipation can be attributed to the charge current, and the spin diffusion current and spin torque at the output are a consequence of the charge current. Therefore, for a logic circuit consisting of an interconnection of gates, the energy can be computed as:

$$E = \sum_{\text{all magnets } i} V_{dd} I_{c,i} T \tag{3.9}$$

where $I_{c,i}$ is the charge current injected into the magnet i.

3.2 Impact of ASL geometries

From the analysis of the energy and delay models in Chapter 3.1, it can be seen that the dimensions of the magnets enter into several expressions. We now analyze the impact of geometry choices on circuit performance, specifically focusing on *optimizable layout parameters*: the magnet length and the channel length. We assume that technology-specific parameters such as the magnet thickness or channel thickness are fixed. We consider each component of switching one by one. For illustration, we will primarily consider the ASL inverter in Fig. 3.2: the quantities associated with the input and output magnet are represented with the subscript 1 and 2, respectively.

3.2.1 Influence on charge current injection

The dependence of the injected charge current, $I_{c,1}$, and the geometry can be shown by combining Equations (3.1) and (3.2):

$$I_{c,1} = \frac{V_{dd}}{R_{s,1} + R_{n,1} + R_{m,1} + R_g} = \frac{V_{dd}}{r_1/l_{m,1} + r_2} \tag{3.10}$$

where r_1 and r_2 are constants that absorb terms other than the optimizable layout parameters listed above. The value of $I_{c,1}$ is directly related to the system energy, as indicated by Equation (3.9), and as we will see soon, also the delay.

3.2.2 Influence on nonlocal spin transfer

The charge current creates spin current that is transported across the channel to the output magnet. For the single-fanout ASL inverter, an analytical expression for the spin current at the output magnet can be derived based on spin injection efficiency η and charge current at the input magnet I_c as $I_s = \eta I_c$. From Equations (3.3), (3.4), and (3.10), the dependence of I_s on the magnet lengths and channel lengths is given by:

$$I_s = \frac{k_1 V_{dd} e^{-L/\lambda_N}}{\left[\left(1 + \frac{k_2}{l_{m,1}}\right)\left(1 + \frac{k_2'}{l_{m,2}}\right) - e^{-2L/\lambda_N}\right](r_1 + r_2 l_{m,1})} \tag{3.11}$$

where k_1, k_2, and k_2' are constants that absorb all fixed geometry parameters, which depend on technology-specific parameters, as well as material and physical constants.

This expression can be analyzed to understand how the spin current changes with the magnet and channel geometries in the ASL inverter. We focus on the optimizable layout parameters: the lengths of the input and output magnets, $l_{m,1}$ and $l_{m,2}$, and the length of the channel, L. It can be seen that

- Increases in $l_{m,1}$ and $l_{m,2}$ will result in a larger spin current at the output magnets. The increase with $l_{m,1}$ occurs because a larger input magnet has a smaller resistance and injects more charge current, resulting in larger spin current at the output magnet. A larger output magnet as the result of longer $l_{m,2}$ absorbs more spin current from the channel, improving η.

- A longer channel length, L, results in weakened spin current at the output magnet, i.e., spin diffusion becomes more inefficient with increasing channel length.

For the multifanin/multifanout case, these closed-form expressions cannot be used, but the impact of changing these parameters broadly follows the same trend as described above.

3.2.3 Influence on the switching of the output magnet

The spin current at the end of the channel switches the output magnet, as governed by the LLG equation, with an input-to-output switching delay as expressed in Equation (3.8), based on an integration of the LLG equation over time. We assume the magnet to be a single domain since macrospin simulation is a good approximation to reflect the switching time trends, as influenced by various factors [61].

This integration involves two geometry-dependent terms. The first is the net number of Bohr magnetons, N_s, of the output magnet is proportional to its volume through $N_s = M_s V/\mu_B$, with μ_B as the unit Bohr magneton. This factor appears and affects t_{sw} through Equation (3.8). The second is the demagnetizing field $\vec{H}_d$, an internal field related to the saturated magnetization, M_s, and demagnetizing factor, N_d, through the relation $\vec{H}_d = N_d M_s \vec{m}$. The demagnetizing factor N_d of a magnet is a function of its dimensions and shape. We follow the equation in [62] to calculate the demagnetizing field along all three axes for a rectangular prism in our LLG simulation. The effective anisotropy constant is calculated as $K = (N_{xx} - N_{yy})M_s^2/2$, with N_{xx} and N_{yy} being the demagnetizing factor along the minor and major axes. Based to our geometric and physical parameter settings, we find that the minimum thermal stability for the magnet sizes we consider is $29.5k_BT$, corresponding to a retention time of $6.7 \times 10^3 s$, which is adequate for the circuit switching frequencies considered in this work. The impact of $\vec{H}_d$ is incorporated in factor f_{sw} in Equation (3.8).

In order to precharacterize the factor f_{sw} and determine how it varies with ASL geometries, we design a series of simulations to examine the influence of magnet geometries to the relation between switching time t_{sw} and spin current I_s. We choose a discrete set of magnet lengths in the range from 30nm to 100nm. The parameters we used in the simulations are the same with those given later in Table 3.1 in Chapter 3.4.1 with the damping factor $\alpha = 0.007$ [21].

As shown in Figure 3.4, the switching time t_{sw} under a series spin currents I_s for various magnet lengths is obtained through LLG simulations and denoted by square markers. A data fitting procedure was then performed based on Equation (3.8), and the best fit, shown by the continuous curves in the figure, is seen to match the data points well at each magnet size. For the specific parameters used in this experiment, we obtained $f_{sw} = 4.7$, and the figure demonstrates that f_{sw} does not change significantly

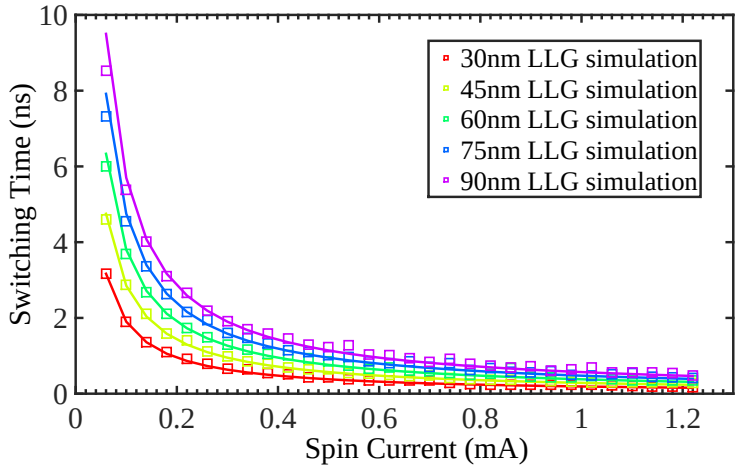


Figure 3.4: LLG simulation results and corresponding curves from analytical equations with $f_{sw} = 4.7$ for relation between t_{sw} and I_s under various magnet lengths (15nm, 30nm, 45nm, 60m, and 75nm).

with geometry, i.e., the geometric impact through $\vec{H}_d$ is minimal.

Therefore, from Equations (3.8) and (3.11),

$$t_{sw} = \frac{l_{m,2}\left[\left(1+\frac{k_2}{l_{m,1}}\right)\left(1+\frac{k_2'}{l_{m,2}}\right) - e^{-\frac{2L}{\lambda_N}}\right](r_1 + r_2 l_{m,1})}{k_1' V_{dd} e^{-\frac{L}{\lambda_N}}} \tag{3.12}$$

where k_1' modifies k_1 to capture the constants in $2 f_{sw} q N_s$.

3.3 Optimization

The net conclusion of our analysis in Equation (3.12) is that the switching time t_{sw} of an ASL inverter stage

- reduces sublinearly with $l_{m,1}$,
- increases linearly with $l_{m,2}$, and
- reduces by an exponential dependence with L.

Therefore, the switching delay can be improved by adjusting the sizes of the magnets and reducing the length of the channel. For a global interconnect of fixed length, the

insertion of buffers/inverters can reduce switching times by reducing channel lengths between buffers, with overheads due to the intrinsic delays of individual buffers. We now develop optimization formulations for an ASL buffer chain and a general circuit.

3.3.1 Optimization of an ASL buffer chain

Problem formulation

We now present an optimization formulation that optimizes the energy and delay of a long wire, driven by an ASL buffer and feeding an ASL load, through buffer insertion and sizing. We keep the width of each magnet constant, setting it to the width of the channel for better spin injection into the channel, and optimize the lengths of the magnets. The insertion of n buffers divides the wire of length L into $n+1$ stages of length $L_i, 1 \leq i \leq n+1$. In the ith stage, we denote the input magnet length by $l_{m,i}$ and the output magnet length by $l_{m,i+1}$; note that the output magnet for the ith channel also serves as the $(i+1)^{\text{th}}$ input magnet.

Denoting the delay from the ith to the $(i+1)^{\text{th}}$ buffer in the buffer chain as $T_i(l_{m,i}, l_{m,i+1}, L_i)$, the total delay is:

$$T_{tot} = \sum_{i=1}^{n+1} T_i(l_{m,i}, l_{m,i+1}, L_i) \tag{3.13}$$

and the total energy over a clock period of P_{clc} is:

$$E_{tot} = \left(\sum_{i=1}^{n+1} V_{dd} I_{c,i}\right) P_{clc} \tag{3.14}$$

The optimization problem can be formulated as minimizing the energy over a delay constraint related to P_{clc}, as:

$$\begin{array}{ll} \text{minimize}_{l_{m,i}, L_i} & \left(\sum_{j=1}^{n+1} V_{dd} I_{c,j}\right) \\ \text{subject to} & \sum_{i=1}^{n+1} T_i(l_{m,i}, l_{m,i+1}, L_i) \leq P_{clc} \end{array} \tag{3.15}$$

Buffer optimization as a posynomial programming problem

In this chapter, we consider a simpler and more practical version of the optimization problem in (3.15), using equal channel lengths, and then optimizing the magnet lengths. We show that for the buffer chain, the total delay and the energy consumption of the

ASL circuit are both posynomial functions, which implies that the optimization problem is a posynomial program [63] that can be solved to find the length of each magnet as well as the interconnect length in each stage. These problems can be efficiently solved with concrete guarantees of optimality since, unlike general nonlinear optimization problems, posynomail programs possess the property that any local minimum is a global minimum. In Chapter 3.4, we will use a posynomial program solver, `gpposy` from the geometrical programming optimizer GGPLAB [64] to optimize these ASL circuits. To the best of our knowledge, this is the first time this problem has been formulated as a posynomial program.

For a buffer chain with n magnets inserted between input and output magnets, we denote the length of the ith magnet by $l_{m,i}$ and assume that the channel length between two magnets is equal, i.e., $L_i = L/(n+1)$, and the magnet width is constant and set to the minimum value. The total delay for the buffer chain can be obtained from Equation (3.12) and (3.13) as:

$$T_{tot} = \frac{1}{k_1' V_{dd} e^{-L_i/\lambda_N}} \left(\sum_{i=1}^{n+1} l_{m,i+1} \left(r_1 + r_2 l_{m,i} \right) \cdot \left[\left(1 + \frac{k_2}{l_{m,i}} \right) \left(1 + \frac{k_2'}{l_{m,i+1}} \right) - e^{-2L_i/\lambda_N} \right] \right) \tag{3.16}$$

Assuming the buffer chain is run at its fastest speed, with $P_{clc} = T_{tot}$, then the total energy E_{tot} for the buffer chain is derived from Equations (3.10), (3.12), and (3.14) as:

$$E_{tot} = \frac{V_{dd}}{k_1' e^{-L_i/\lambda_N}} \left(\sum_{i=1}^{n+1} \frac{l_{m,i}}{r_1 + r_2 l_{m,i}} \right) \left(\sum_{i=1}^{n+1} l_{m,i+1} \cdot \left(r_1 + r_2 l_{m,i} \right) \left[\left(1 + \frac{k_2}{l_{m,i}} \right) \left(1 + \frac{k_2'}{l_{m,i+1}} \right) - e^{-2L_i/\lambda_N} \right] \right) \tag{3.17}$$

In Equation (3.16) and (3.17), if we take T_{tot} and E_{tot} as functions of $l_{m,i}$, the coefficients for all terms that include $l_{m,i}$ are always positive. Therefore, both functions are posynomial. It can be shown that even when the L_i values are not uniform, these are posynomial functions in $l_{m,i}$ and L_i.

For a more specific case where all magnets are assumed to have the same length, i.e., $l_{m,i}$ is the same for all i, it is possible to find a closed form minimum for the delay

of the buffer chain. Using Equation (3.16), the delay for the optimal l_m can be shown as:

$$T_{tot} = \frac{n+1}{k_1' V_{dd} e^{-\frac{L_i}{\lambda_N}}} \left(\frac{r_2 k_2 k_2'}{l_m} + \left[r_1 (1 - e^{-\frac{2L_i}{\lambda_N}}) + r_2 k_2 + r_2 k_2' \right] l_m + r_2 (1 - e^{-\frac{2L_i}{\lambda_N}}) l_m^2 + r_1 k_2 + r_1 k_2' + r_2 k_2 k_2' \right) \tag{3.18}$$

Note that in the above formulation all the coefficients of l_m are positive and therefore it is a polynomial of l_m, leading to a closed form solution of l_m for minimum delay.

3.3.2 Formulation for a general circuit

We now consider the sizing problem without buffer insertion for a user-specified clock period, P_{clc}. The energy consumed by an ASL circuit over the clock period is the summation of contributions over all gates in the circuit:

$$E_{tot} = \left(\sum_j V_j I_{c,j} \right) P_{clc} \tag{3.19}$$

The optimization problem of geometries for an ASL circuit to give minimum delay under certain delay requirement is:

$$\begin{array}{ll} \text{minimize}_{l_{m,i}, L_i} & \sum_j V_j I_{c,j} \\ \text{subject to} & T_{tot} \leq P_{clc} \end{array} \tag{3.20}$$

where T_{tot} is the delay of the critical path.

In order to explore the maximum amount of delay reduction that can be achieved through the optimization, we propose an optimization algorithm for general circuits and its pseudocode is shown in Algorithm 1. It solves the above formulation using a variant of the TILOS alogrithm [65].

Line 1 calculates the initial delay of the circuit based on the netlist and ASL gate and interconnect delays (Chapter 3.1.2) and finds out the critical path. Initial assignment for the minimum circuit delay is performed in lines 2–3. Next, lines 5–9 compute the sensitivity, $\partial Delay_j / \partial Power_j$, for each magnet in the gates on the critical path if its size will not exceed the upper-bound of magnet size $l_{upper\text{-}bound}$ after being sized up. This sensitivity is numerically achieved by upsizing one magnet by a geometric factor α at a time and calculating the delay reduction and power increase caused by changing

Algorithm 1 Geometric optimization for ASL circuit

Input: Circuit netlist and placement result;
Incremental length multiplier α.
Output: Delay, energy consumption and sizes of magnets.
1: Compute initial circuit delay T_0 and critical path.
2: $T_{min} \leftarrow T_0$.
3: $i \leftarrow 1$.
4: **repeat**
5: **for** each magnet j on critical path **do**
6: **if** $l_j \times \alpha < l_{upper\text{-}bound}$ **then**
7: Calculate the sensitivity $\partial Delay_j / \partial Power_j$ from sizing magnet j.
8: **end if**
9: **end for**
10: Identify the magnet k with the most negative sensitivity.
11: $l_k \leftarrow l_k \times \alpha$.
12: Compute corresponding circuit delay T_i and new critical path.
13: $T_{min} \leftarrow T_i$.
14: $i \leftarrow i + 1$.
15: **until** $T_i \geq T_{min}$.

this single magnet. By our algorithm, delay of the circuit is reduced with the minimal amount of power penalty. Line 10 then finds out the magnet with largest impact on circuit delay and sizes it up by a factor α to get the largest delay improvement for the smallest overhead (line 11). The circuit delay in iteration i is updated as T_i (lines 12–13), and the process continues until the stopping criterion is met when no more delay improvement can be made (lines 4, 14–15). This provides the tradeoff curve of interest.

3.4 Results

3.4.1 Simulation parameters

We present some material and geometric parameters used in our simulations in Table 3.1. These parameters, chosen in consultation with technologists, are intended to be representative and indicative of current and future technologies.

To realistically estimate the ohmic loss of the power delivery network in Equation (3.1), we evaluated a standard set of power grid benchmarks [66], and determined that the effective resistance from each pin to the supply node is on the order of 0.25Ω. Since these benchmarks evaluate the top few layers of a power grid (a typical number is five layers), we multiply this number by $2\times$ to model the impact of lower metal layers. Therefore, we use an effective resistance of 0.5Ω each for the supply and the ground line. This effective resistance is effectively translated into a dimension of

140nm×140nm×1400nm in width, thickness, and length, respectively, where the cross-sectional dimensions are based on [67]. We note that for an efficient ASL implementation, it is essential for the power grid resistance to be around this value, which is lower than the corresponding value for CMOS technologies. This is because $R_m + R_n \approx 7\Omega$, and if $R_s + R_g$ is much larger, then a large fraction of power will be wastefully dissipated in the power grid resistors.

Table 3.1: Material and geometric parameters for ASL devices.

Parameter	Value
M_s (saturation magnetization)	780×10^3A/m [21]
ρ_F (resistivity of magnet)	170Ω·nm [21] [38]
ρ_N (resistivity of channel)	7Ω·nm [21] [38]
w_m (width of magnet)	10nm
t_m (thickness of magnet)	5nm
w_n (width of channel)	20nm
t_n (thickness of channel)	30nm

For parameters that most closely affect performance metrics, recognizing that the technology is rapidly evolving today, we explore a range of values in our experiments that reflect various technology scenarios to reflect current-day and project future technologies. In our experiments, the value of λ_F is chosen in the range of 5nm to 50nm [54] [38], and the polarization factor P from 0.5 to 0.7 [59]. The channel spin diffusion length, λ_N, can take values in a large range since various materials could be considered [68]. Given this background and the strong materials research in this area, we choose two possible values of λ_N of 450nm and 1000nm, which could represent the spin diffusion lengths of bulk copper under room temperature and low temperature from various experimental measurements [68], [69]. However, as pointed out by [69] and [70], the spin diffusion length will degrade significantly due to size effects. Therefore, two more sets of simulations with λ_N of 180nm and 400nm are added, corresponding to a degradation to 40% of the bulk values, estimated under the channel dimensions in our work through the results shown in [69]. The supply voltage is chosen in 10mV–30mV range [21]. It is unrealistic to show results for all cross-products of these choices, and we focus on two parameter sets with bulk and degraded spin diffusion lengths in Table 3.2: from

parameter set 1, a nearer-term technology, to set 2 for projected technologies and with higher V_{dd}.

We calculate switching time and energy, static timing analysis, and optimizations using MATLAB and C++ on a 2.53 GHz Intel Core i3 with 4GB RAM.

Table 3.2: Three parameter choices for P, λ_N, and V_{dd}.

Values of technology nodes		
Parameter set	1	2
P (magnet polarization factor)	0.5	0.6
λ_N (spin diffusion length, bulk / degraded, nm)	450 / 180	1000 / 400
V_{dd} (supply voltage, mV)	10	30
w_c (channel width, nm)	10	20
t_c (channel thickness, nm)	20	30

3.4.2 Optimizing a buffered wire

We provide a simple example of a ASL buffer chain to illustrate the use of the posynomial formulation to individually optimize the size of each magnet. A total interconnect length of 1800nm is considered with nine equally-spaced buffers inserted between the input and output magnets. We consider the spin diffusion length of magnet $\lambda_F = 14.5$nm [68], channel width $w_n = 20$nm, and thickness $t_n = 30$nm. The length of the input magnet and output magnet are both set to 30nm. The posynomial formulation is fed to the GGPLAB solver [64], which optimizes the length of each magnets to minimizes the delay of the entire buffer chain. These optimized lengths (chosen to be multiples of the feature size, 10nm) are shown in Table 3.4 for the case when 9 buffers are inserted.

Next, we repeat these posynomial programming optimizations for a set of buffer chains with a varying number of buffers under the above technology parameters based on optimization (3.15). For a specified number of equally-spaced buffers (n), we provide the delay and corresponding energy under three cases in Fig. 3.5: (i) *Optimized delay*: the length of each magnet is sized individually for optimal delay; (ii) *Closed-form delay*: All the inserted magnets are assumed to have the same length, i.e., $l_{m,i} = l_{m,i+1} = l_m$, except for the first and last magnet in the buffer chain, whose lengths are fixed. In this case the delay is very similar to the situation described in Equation (3.18) and a closed

Table 3.3: Delay before optimization (unsized), delay after optimization (sized), improvement in percentage, and runtime of optimization program under two parameter sets with bulk / degraded λ_N of channel material for the ISCAS-85 benchmarks for (a) parameter set 1, and (b) parameter set 2.

Ckt.	Parameter Set 1			
	Unsized Delay (ns)	Sized Delay (ns)	Improvement (%)	Runtime (s)
C17	39.2 / 45.1	30.0 / 33.5	23.5 / 25.7	10.10 / 0.16
C432	422.0 / 495.1	352.8 / 402.8	16.4 / 18.6	5.03 / 14.7
C499	418.5 / 498.9	360.4 / 415.1	13.9 / 16.8	5.74 / 42.4
C880	374.6 / 441.0	316.5 / 363.9	15.5 / 17.5	3.20 / 11.1
C1355	352.8 / 418.9	297.9 / 345.0	15.6 / 17.6	20.7 / 68.6
C1908	481.2 / 567.2	407.6 / 465.1	15.3 / 18.0	14.8 / 54.8
C2670	427.7 / 509.0	367.3 / 427.5	14.1 / 16.0	4.07 / 18.8
C3540	647.1 / 763.8	549.7 / 630.1	15.1 / 17.5	17.2 / 53.5
C5315	551.7 / 646.9	468.0 / 536.0	15.2 / 17.1	11.5 / 45.1
C6288	1384.7 / 1610.3	1161.9 / 1305.2	16.1 / 18.9	158.8 / 412.3
C7552	662.7 / 793.3	573.6 / 668.5	13.4 / 15.7	20.0 / 82.1

(a)

Ckt.	Parameter Set 2			
	Unsized Delay (ns)	Sized Delay (ns)	Improvement (%)	Runtime (s)
C17	5.75 / 7.19	3.77 / 4.61	34.4 / 35.9	0.10 / 0.14
C432	58.0 / 72.9	41.0 / 50.8	29.3 / 30.3	8.1 / 11.1
C499	50.8 / 66.1	37.9 / 48.4	25.4 / 26.8	19.2 / 39.6
C880	49.8 / 63.2	35.7 / 44.6	28.3 / 29.4	4.1 / 7.8
C1355	45.2 / 57.7	32.8 / 41.4	27.4 / 28.2	31.3 / 57.2
C1908	63.7 / 79.2	46.0 / 56.7	27.8 / 28.4	25.4 / 44.1
C2670	49.5 / 64.9	37.1 / 48.0	25.1 / 26.0	7.3 / 15.6
C3540	83.3 / 106.2	60.7 / 75.9	27.1 / 28.5	32.9 / 52.1
C5315	70.9 / 89.6	51.1 / 64.2	28.9 / 28.3	21.4 / 38.3
C6288	198.4 / 242.0	141.8 / 169.5	28.5 / 30.0	369.6 / 499.4
C7552	77.6 / 101.0	58.0 / 74.8	25.3 / 25.9	25.6 / 64.6

(b)

Table 3.4: Optimized magnet lengths (nm) for minimal delay on a line with 9 buffers between fixed-size input and output magnets.

In	1	2	3	4	5	6	7	8	9	Out
30	80	90	90	100	100	100	100	100	90	30

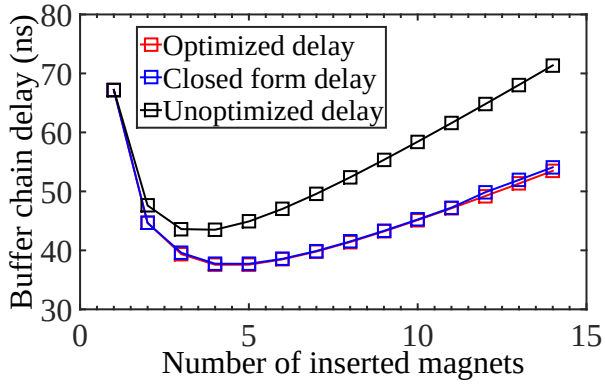
form solution of l_m can still be found for the minimum delay; (iii) *Unoptimized delay*: The lengths of all inserted magnets are of minimum length 30nm, i.e., no optimization is performed. The nature of these curves is similar for each value of the spin diffusion length in Table 3.2, and we choose a representative value of 400nm to illustrate the results. The zero buffer case is not considered as it cannot supply the critical spin current, I_s^{cr}, required for switching the output [21].

As shown in Figure 3.5(a), the minimum delay occurs when four magnets are inserted, corresponding to a delay of 37.6ns for the case where each inserted magnet is sized individually. As a comparison, the delay with the same number of unsized magnet insertion is 44.9ns, implying that the optimization provides a 16.3% improvement with only a small energy overhead, as shown in Fig. 3.5(b). It is also observed that when all magnets are identically sized, the delay curve virtually coincides with that for the individually-sized case. Therefore, the closed form is a fast predictor for the optimal delay.

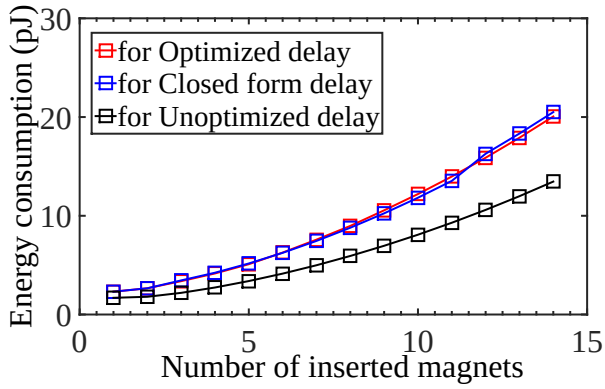
It is noteworthy that these optimizations employ the analytical method described in Chapter 3.1.2. An alternative to analytical modeling is the MNA-based modeling method described in Chapter 3.1.3. Although the results obtained by these two modeling methods are close to each other only under certain specific conditions, the analytical modeling method shows a good fidelity in finding minimum delay and is therefore very useful for delay optimization. Further details about the comparison of the two modeling methods and the notion of fidelity are provided in the Appendix A.

3.4.3 Optimization of benchmark circuits

In order to demonstrate the feasibility and the benefits of our optimization methods on general ASL circuits, we tested Algorithm 1 on ISCAS85 benchmark circuits. The benchmarks are placed using CAPO placement tool [71], using an estimation of the ASL



(a)



(b)

Figure 3.5: The (a) delay and (b) energy of the buffer chain under three different cases vs. number of inserted buffers.

cell area, with magnet lengths changed at a granularity of 10nm steps.

A buffer insertion step is performed for any interconnect longer than L_0 to strengthen the signal before the circuit is optimized through Algorithm 1. In the optimization for ISCAS benchmarks, we choose L_0 to be equal to λ_N, because in the π model for the channel mentioned in Chapter 3.1.3, the spin signal loss will be close to saturation when the ratio L/λ_N exceeds 1. The row utilization leaves sufficient space for inserting buffers and sizing these cells.

Two sets of parameters, representing two technologies as shown in Table 3.2 are used. The delay before optimization, after optimization, improvement in percentage, and the runtime for each benchmark under the two technology parameter sets with bulk

and degraded spin diffusion lengths are shown in Table 3.3. Although the degradation of spin diffusion length will inevitably induce higher delay, optimization through sizing could still bring a good amount of improvements for all circuit benchmarks, indicating the effectiveness and robustness of our algorithm across various technologies. Various techniques have been applied to enhance the efficiency of Algorithm 1, including the use of a precharacterized look-up table for intrinsic delay of ASL gates and incremental timing analysis after a change in the TILOS-like optimization algorithm. It can be seen from Table 3.3 that the more advanced technologies have shorter delays and larger delay improvements with reasonable runtime on the ISCAS85 benchmark circuits.

Detailed results are presented for the C6288 benchmark under the two technology parameters with bulk and degraded spin diffusion lengths of Table 3.2 to demonstrate the effectiveness of our optimization algorithm. The delay-power trade-off curve under parameter set 1 is shown in Fig. 3.6(a). The optimization begins at the highest delay, at the right of the curve. As the delay reduces through the optimization, the power increases as a penalty. The delay reduction and energy for C6288 benchmark is shown in Fig. 3.6(b) and clearly through each iteration, the delay of the circuit keeps decreasing. The energy, however, behaves differently. At the beginning of the optimization, it decreases together with delay since sizing the gates helps overcome gross inefficiencies in the interconnect bottleneck. The reduction of delay dominates the power increase in the power-delay product at this moment. As the benefit of delay reduction becomes smaller as the optimization proceeds, the increase in power finally dominates and the energy starts to increase. Similar trends are seen under three other sets of results. The trend of power-delay curves indicates that at the beginning of the optimization, power is relatively insensitive to upsizing of the magnets, yet as the magnets on the critical path become larger and are still sized up for smaller delay, power becomes more sensitive to sizing.

3.5 Conclusion

This chapter has explored the energy/delay trade-off relation and presented a systematic approach to optimizing ASL circuits. We have presented a posynomial programming approach for buffered lines and a numerical optimization scheme for general circuits.

Under realistic parameters that include factors such as degradation in the spin diffusion length due to scaling, our results demonstrate the utility of sizing ASL circuits to reduce delay by about 30%. This framework can enable technology-circuit codesign by allowing the evaluation of technology parameters on circuit performance.

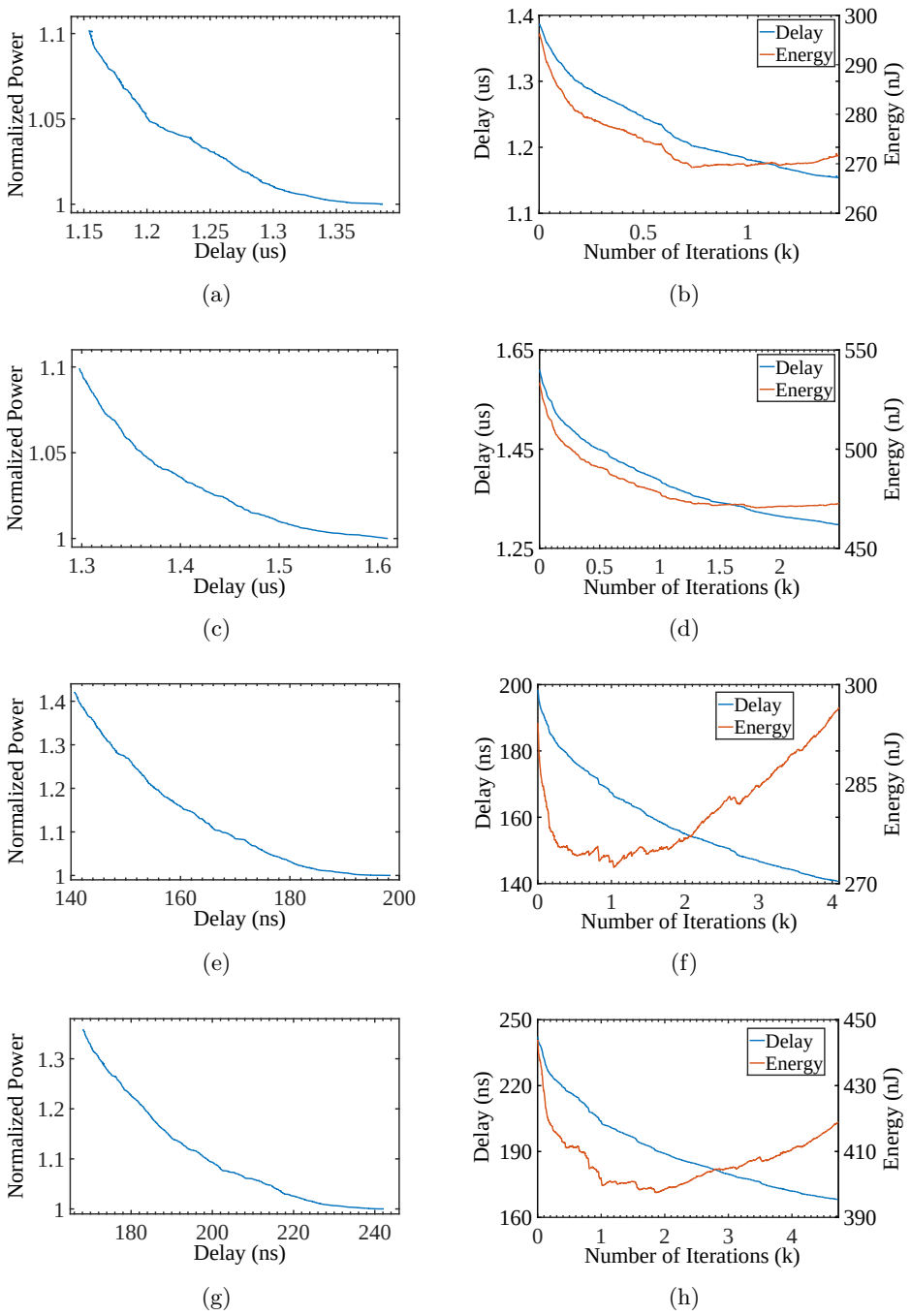


Figure 3.6: Relation between delay and power C6288 through optimization (left) and change in delay and energy through optimization iterations (right). (a), (b): parameter set 1 with bulk spin diffusion length of 450nm; (c), (d): parameter set 1 with degraded spin diffusion length of 180nm; (e), (f): parameter set 2 with bulk spin diffusion length of 1000nm; (g), (h): parameter set 2 with degraded spin diffusion length of 400nm.

Chapter 4

DW Nucleation in CoMET Device Design

Several spin-based devices have been proposed as alternatives to CMOS [72, 73], leveraging STT [18, 20, 74, 75], switching a FM by transferring electron angular momentum to the magnetic moment; SHE, generating spin current from a charge current through a high resistivity material [76]; ME effect [41], using an electric field to change FM magnetization [1, 2, 44]; DW motion through an FM using automotion [25, 44], an external field [77] or current [26, 74, 78]; dipole coupling between the magnets [79]; and propagating spin wave through an FM [80]. In order for the spin-based processor to be running at a CMOS–competitive clock speed of 1GHz, we need the device delay to be around 100ps. Theoretically, some of the proposed devices can achieve this target delay [73] at the cost of additional energy. However, in order to be competitive with CMOS, spin–based device not only has to be fast, but also energy efficient, i.e., its energy dissipation should be in the range of a few hundred aJ, in order to meet the requirements from high performance computation elctronic systems nowadays [81–90].

We jointly propose CoMET, a novel device that nucleates a DW in an FM channel with perpendicular magnetic anisotropy (PMA), and uses current-driven DW motion to propagate the signal to the output. A voltage applied on an input ferroelectric (FE) capacitor nucleates the DW through the ME effect. For fast, energy-efficient nucleation, we use a composite structure with an IMA–FM layer above the PMA–FM channel. The

DW is propagated to the output end of the PMA channel using a charge current applied to a layer of high resistivity material placed under the PMA channel. The IME effect induces a voltage at the output end, and we use a novel circuit structure to transmit the signal to the next stage of logic.

The contributions and novelties of our joint work are as follows:

- The composite structure of IMA–FM/PMA–FM allows DW nucleation under a low applied voltage of 110mV. Before the application of a voltage, the magnetization in the PMA–FM is moved away from its easy axis by the strong exchange coupling between IMA–FM/PMA–FM, thus enabling a fast low-power DW nucleation.

- We use charge current to realize fast DW propagation through the PMA–FM interconnect. The current-driven DW motion scheme has been experimentally shown to be fast [50, 51], with demonstrated velocities up to 750m/s. We choose a PMA channel for DW motion, as against one with in-plane magnetic anisotropy (IMA), since it is more robust to DW pinning and surface roughness effects [46,47].

- A novel circuit structure comprising a dual–rail inverter allows efficient cascading of devices. This scheme improves upon a previous scheme [44] of 6:1 device ratioing and the need for repeated amplifications.

- We explore the design space of the possible PMA–FM material parameters to optimize the performance of the device. Through this systematic design space exploration, we show that it is possible to achieve inverter delay/energy of 99ps/68aJ.

- The DW pinning effect is studies with artificial defects of different sizes on the PMA-FM and IMA-FM. It is observed that the presence of such defects breaks the smoothness in energy landscape of the structure and helps to stabilize DW at its position to some extent.

It is worth mentioning that the CoMET device is a co-developed work, the current-driven DW propagation scheme (bullet point 2 above) and device cascading structure (bullet point 3 above) belongs to the work of another member of my research group. For the convenience of evaluating the whole device performance, a brief introduction to the above contents is also given in this thesis.

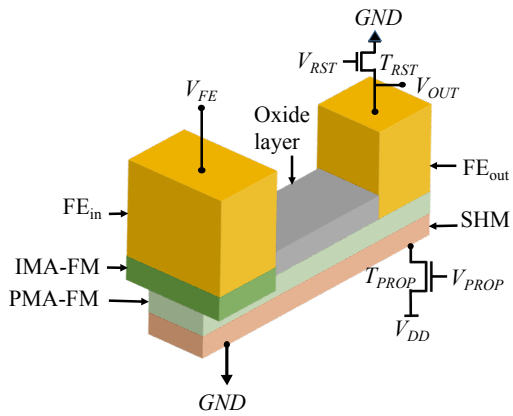


Figure 4.1: Proposed device concept of CoMET illustrating the composite structure of IMA–FM exchange–coupled with PMA–FM at the input end.

The rest of this chapter is organized as follows: In Chapter 4.1, we explain the operation of CoMET. We present the mathematical models and the simulation framework used in this work in Chapter 4.2. Next, we show the performance of the device as a function of the material parameters in Chapter 4.3. Chapter 4.4 concludes the chapter.

4.1 CoMET: Device Concept and Operation

The structure of the proposed device is shown in Fig. 4.1. At the input, a FE capacitor, FE_{in}, is placed atop an IMA–FM. The IMA–FM is exchange–coupled with the input end of a longer PMA–FM interconnect. At its output end, a second FE capacitor, FE_{out}, is placed on top of the PMA–FM interconnect. A layer of high-resistivity spin-Hall material (SHM), which is conducive to strong spin-orbit interaction, is placed beneath the PMA–FM. An oxide layer is present on top of PMA–FM between FE_{in} and FE_{out}.

4.1.1 CoMET–based inverter

We explain the device operation in four stages with the help of Fig. 4.2 and Fig. 4.3.

Stage 1 – DW nucleation: At time $t = 0$, an applied voltage, V_{FE}, charges FE_{in}. The resulting electric field across FE_{in}, E_{FE}, may be positive or negative, depending on the sign of V_{FE}, and generates an effective magnetic field, H_{ME}, through the ME effect

that couples the electric polarization in FE_{in} with the magnetization in the IMA–FM. This magnetic field acts on the composite structure. For $V_{FE} > 0$, this nucleates a DW in the PMA–FM as seen from Fig. 4.3(b), with a down–up configuration if the initial magnetization is along the $+z$ axis. For the opposite case, an up–down configuration is nucleated.

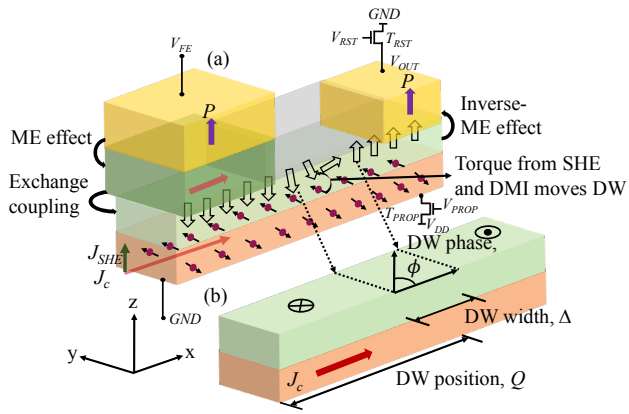


Figure 4.2: (a) Graphical representation of the different underlying physical mechanisms of the device. (b) The position of the DW (Q), width (Δ), and phase (ϕ).

If the initial orientation of the PMA–FM is at an angle to the z-axis, a smaller H_{ME} field can nucleate the DW. The composite structure creates this angle due to strong exchange coupling between the IMA–FM and the PMA–FM as can be seen from the magnetization of PMA–FM in Fig. 4.3(a), thus allowing nucleation under a low magnitude of V_{FE}. In the absence of IMA–FM, voltages up to 1V are necessary to nucleate a DW whereas we show that with the presence of IMA–FM, voltages as low as 110mV would suffice.

Stage 2 – DW propagation Once the DW is nucleated in PMA–FM, transistor T_{PROP} is turned on using the signal V_{PROP} to send a charge current (J_c) through the SHM. Due to SHE, electrons with opposite spin accumulate in the direction transverse to the charge current as shown in Fig. 4.2. As a result, a spin current (J_{SHE}) is generated in a direction normal to the plane of SHM. The resultant torque from the combination of SHE and Dzyaloshinskii–Moriya interaction (DMI) [50] at the interface of PMA–FM and the SHM propagates the DW to the output end.

Before the DW reaches the output, V_{RST} turns on transistor T_{RST} to connect FE_{out} to *GND* as seen from Fig. 4.3(c). This causes FE_{out} to charge due to the presence of an electric field across it as a result of the IME effect. This step resets the capacitor such that once the DW reaches the output, it can either reverse or maintain the electric polarization of FE_{out}, thus reflecting the result of the operation.

Stage 3 – Output FE switching: The DW reaches the output end in time $t_{propagate}$ as seen from Fig. 4.3(d) and switches the magnetization of PMA–FM. The magnetization in PMA–FM couples with the electric polarization of FE_{out} through the IME effect. As a result, a voltage, V_{OUT}, is induced at the output node.

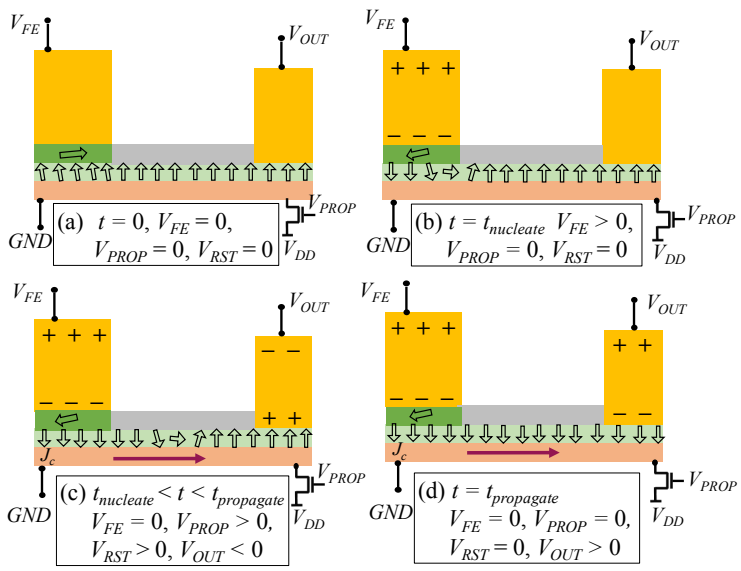


Figure 4.3: Operation of CoMET device showing (a) steady–state before V_{FE} is applied, (b) nucleation of the DW in PMA–FM after V_{FE} is turned on, (c) propagation of the DW by turning on V_{PROP}, and charging of the output FE capacitor when $V_{RST} > 0$ is applied, and (d) the induction of an output voltage V_{OUT} through the inverse–ME effect.

Stage 4 – Cascading multiple logic stages: Successive logic stages of CoMET can be cascaded as shown in Fig. 4.4, through a dual-rail inverter structure comprising transistors T_P and T_N. A timing diagram showing the application of the different input excitations and the output signal are shown in Fig. 4.5. The signal V_{RST} turns

on transistors T_{RST1} and T_{RST2} in the two logic stages to charge the respective FE capacitors. The output voltage induced through the IME effect, V_{OUT1}, turns on either T_N or T_P, depending on its polarity. These transistors form an inverter and set V_{FE} for the next stage to a polarity opposite that of V_{OUT1}. The result of the operation is retained in the PMA-FM when the supply voltage is removed. This allows the realization of nonvolatile logic with CoMET. As a result, the inverter can be power-gated after signal transfer, saving leakage. Unlike the charge transfer scheme in [44] with 6:1 ratioing between stages and repeated amplification, our scheme allows all stages to be unit-sized, resulting in area and energy efficiency. This scheme also allows efficient charge-based cascading of logic stages as opposed to spin–based cascading, which require a large number of buffers to overcome the spin losses in the interconnects [33].

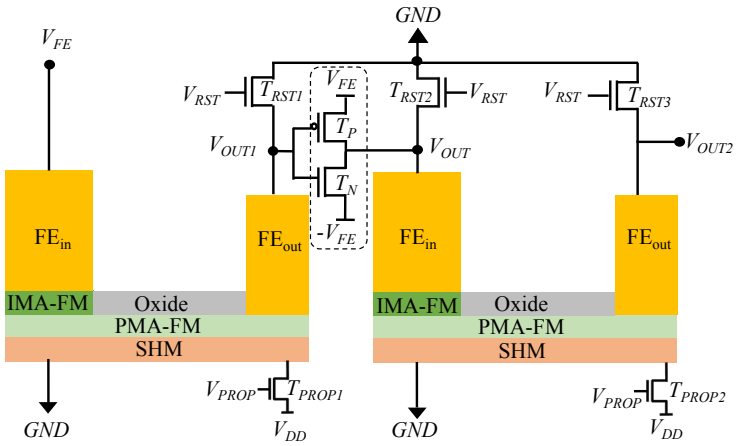


Figure 4.4: Logic cascading of two CoMET devices using transistors T_P and T_N.

4.1.2 CoMET–based Majority gate

The idea of the CoMET inverter can be extended to build a three-input CoMET majority gate (MAJ3), as shown in Fig. 4.6(a). The input voltage V_{FE} is applied to each input to nucleate a DW in the PMA–FM below each $\mathrm{FE_{in}}$. The DWs from each input is propagated to the output by turning on T_{PROP}. The DWs compete in the PMA–FM [18], and the majority prevails to switch $\mathrm{FE_{out}}$ using the IME effect. Subsequent gates are cascaded using the dual-rail inverter scheme described above.

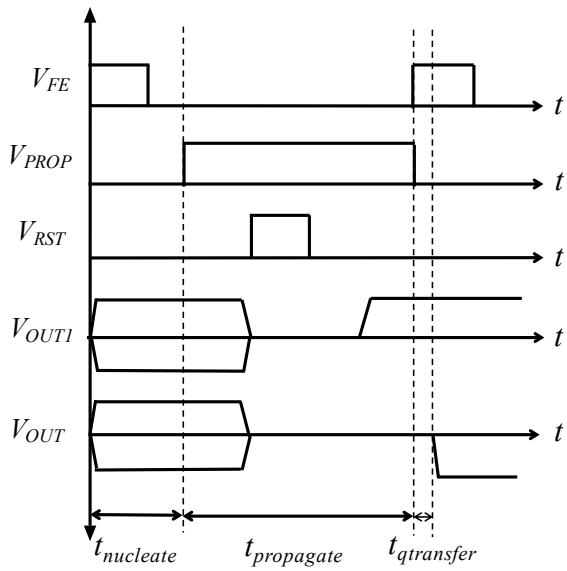


Figure 4.5: Timing diagram showing the application of the V_{FE}, V_{PROP}, and V_{RST} signals.

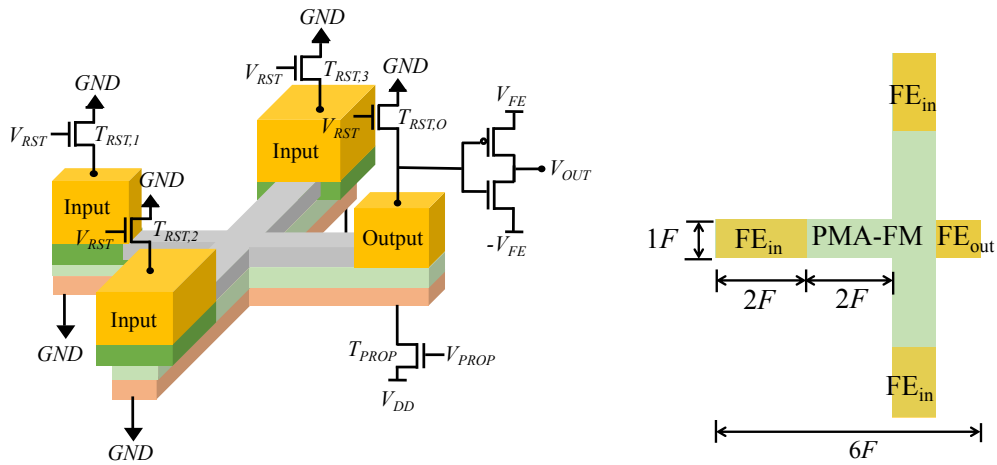
4.2 Modeling and simulation framework

We now show how the performance of a MAJ3 gate can be modeled. The worst–case delay of this gate occurs when one input differs from the others. At feature size, F, the DW for each input nucleates in PMA–FM below $\mathrm{FE_{in}}$ at a distance $2F$ once V_{FE} is applied. The DW from each input then travels a $4F$ distance to switch $\mathrm{FE_{out}}$ as shown in Fig. 4.6(b). The dimensions of the simulated structure are shown in Fig. 4.6(c). The IMA–FM aspect ratio (x:y) is set to 2:1 to align the magnetization of PMA–FM at an angle to the easy axis (due to shape anisotropy). The $\mathrm{FE_{in}}$ and $\mathrm{FE_{out}}$ thicknesses are set to 5nm to avoid leakage through the capacitors. The PMA–FM thickness is set to 1nm.

4.2.1 Modeling device operation

We analyze the device operation in each of the four stages as follows:

Stage 1 – DW nucleation: The dynamics of electric polarization, $\vec{P}$, of $\mathrm{FE_{in}}$ due to $E_{FE}(= V_{FE}/h_{\mathrm{FE_{in}}})$ as a result of the applied voltage V_{FE} across the thickness of the



(a) (b)

Structure	Dimensions (*l* x *w* x *h*)
FE_{in}	2*F* x 1*F* x 5nm
IMA-FM	2*F* x 1*F* x 1nm
PMA-FM, SHM	6*F* x 1*F* x 1nm
Oxide	3*F* x 1*F* x 1nm
FE_{out}	1*F* x1*F* x 5nm

(c)

Figure 4.6: (a) CoMET–based three-input majority (MAJ3) gate (b) top view of MAJ3 with the device dimensions marked for a feature size, F and (c) the length (l), width (w), and height (h) of the CoMET device in Fig. 4.1 considered in this simulation.

input FE capacitor, $h_{\mathrm{FE_{in}}}$ are described by the Landau-Khalatnikov (LKh) equation [91]:

$$\gamma_v \frac{\partial P_i}{\partial t} = -\frac{1}{a_{\mathrm{FE_{in}}}} \frac{\partial F_T}{\partial P_i} \tag{4.1}$$

where F_T is the total free energy of the input structure as a function of E_{FE}, γ_v is the viscosity coefficient, P_i is the component of $\vec{P}$ in the i direction, and $a_{\mathrm{FE_{in}}}$ is the volume of the input FE capacitor. The resultant $\vec{P}$ generates an effective magnetic field from ME, $\vec{H}_{ME}$ given by,

$$\vec{H}_{ME} = \frac{\kappa_{ME}}{\epsilon_0} \frac{h_{int}}{h_{\mathrm{FE_{in}}}} \vec{P} \tag{4.2}$$

Here, h_{int} is the ME interface thickness, $h_{\mathrm{FE_{in}}}$ denotes the thickness of $\mathrm{FE_{in}}$, and κ_{ME} refers to the ME coefficient. The magnetic field, H_{ME} is then applied as a Zeeman field

to the composite structure in the micromagnetics simulator, OOMMF [92], which solves the Landau-Lifshitz-Gilbert (LLG) equation [93,94] as shown below, to obtain $t_{nucleate}$:

$$\frac{(1+\alpha^2)}{\gamma}\frac{d\vec{M}}{dt} = -\vec{M}\times\vec{H}_{eff} - \alpha\vec{M}\times(\vec{M}\times\vec{H}_{eff}) \tag{4.3}$$

Here α refers to the damping constant and $\vec{M}$ denotes the magnetization in PMA–FM. The effective magnetic field, $\vec{H}_{eff}$ is given by:

$$\vec{H}_{eff} = \vec{H}_{ME} + \vec{H}_K + \vec{H}_{demag} + \vec{H}_{ex} \tag{4.4}$$

where $\vec{H}_K$, $\vec{H}_{demag}$, and $\vec{H}_{ex}$ refer to the contributions to $\vec{H}_{eff}$ from magnetic anisotropy, the demagnetization field, and the exchange field in PMA–FM, respectively.

Stage 2 – DW propagation: The propagation time is obtained through calculating the DW propagation speed based on the material parameters with the governing equations explained in details in [27].

Stage 3 – Output FE switching: The electric field developed across $\mathrm{FE_{out}}$ from IME effect, $\vec{E}_{IME}$, due to the magnetization, $\vec{M}$ in PMA–FM is used to calculate V_{OUT} as shown below:

$$\begin{aligned} \vec{E}_{IME} &= \kappa_{IME}\frac{h_{int}}{h_{\mathrm{FE_{out}}}}\vec{M}; \\ V_{OUT} &= \vec{E}_{IME}h_{\mathrm{FE_{out}}} \end{aligned} \tag{4.5}$$

where κ_{IME} is the inverse ME coefficient [16], h_{int} is the interface thickness, and $h_{\mathrm{FE_{out}}}$ refers to the thickness of the output FE capacitor.

Stage 4 – Cascading logic stages: The time, $t_{qtransfer}$, required to transfer V_{OUT1} to the input of the next stage includes the delay of the dual-rail inverter and the RC delay of the wire from the inverter output to $\mathrm{FE_{in}}$ of the next stage.

4.2.2 Modeling performance parameters

The delay and energy of a K-input CoMET majority gate are:

$$\begin{aligned} T_{\mathrm{CoMET}} =& 2(t_{nucleate} + t_{propagate} + t_{qtransfer}) \\ E_{\mathrm{CoMET}} =& 2(E_{FE} + E_{TX} + E_{Joule} + E_{leakage}) \end{aligned} \tag{4.6}$$

Parameter	**Value**
Viscosity coefficient, γ_v [Vm·s/K] [44]	5.47×10^{-5}
Vacuum permittivity, ϵ_0 [F/m]	8.85×10^{-12}
Vacuum permeability, μ_0 [T·m/A]	1.25×10^{-6}
Charge of the electron, e [C]	1.60×10^{-19}
Gyromagnetic ratio, γ [rad/s·T]	1.76×10^{11}
Speed of light, c [m/s]	3×10^{8}
ME coefficient for $\mathrm{FE_{in}}$, κ_{ME} [s/m] [16]	(0.2/c)
ME coefficient for $\mathrm{FE_{out}}$, κ_{IME} [s/m] [16]	(1.4/c)
Resistivity of SHM, ρ_{SHM} [Ω-m] [50]	1.06×10^{-7}
FE permittivity, ϵ_{FE} [44]	164
Adiabatic STT parameter, β [50]	0.4
DMI constant, $\lvert D\rvert$ [mJ/m^2] [50, 95]	0.8
ME interface thickness, h_{int} [nm] [44]	1.5
Transistor threshold voltage, V_{th} [V] [96]	0.2
Bohr magneton, μ_B [J/T]	9.274×10^{-24}
15nm Transistor on-resistance, R_{on} [Ω] [96]	3480
7nm Transistor on-resistance, R_{on} [Ω] [96]	4109
Spin Hall angle, θ_{SHE}	0.5
Spin polarization, $P_{\mathrm{PMA–FM}}$ [50]	0.5
Transistor gate capacitance, C_g [fF] [96]	0.1

Table 4.1: Simulation parameters used in this work.

where E_{FE}, E_{TX}, E_{Joule}, and $E_{leakage}$, respectively, refer to the energy for charging the $\mathrm{FE_{in}}$, turning the transistors on, SHM Joule heating, and due to transistor leakage currents. The factor of 2 is due to PMA–FM magnetization initialization of each input to a state that allows DW nucleation [44]. Finally,

$$E_{TX} = (C_g/2)\left((K+1)V_{RST}^2 + V_{PROP}^2 + 2V_{OUT}^2\right);$$
$$E_{Joule} = (J_c w_{\mathrm{SHM}} t_{\mathrm{SHM}})^2 \left[R_{on} + R_{\mathrm{SHM}}\right] t_{propagate};$$
$$E_{FE} = (K/2) C_{\mathrm{FE_{in}}} V_{FE}^2 \;\; ; \;\; R_{\mathrm{SHM}} = (\rho_{\mathrm{SHM}} l_{\mathrm{SHM}})/(w_{\mathrm{SHM}} t_{\mathrm{SHM}})$$

Here, C_g, $C_{\mathrm{FE_{in}}}$, R_{on}, and R_{SHM} refer to the transistor gate capacitance, capacitance of the input FE capacitor, transistor on–resistance, and resistance of the SHM, respectively. The length, width, and thickness of the SHM, are respectively, given by l, w, and h, each with subscript SHM.

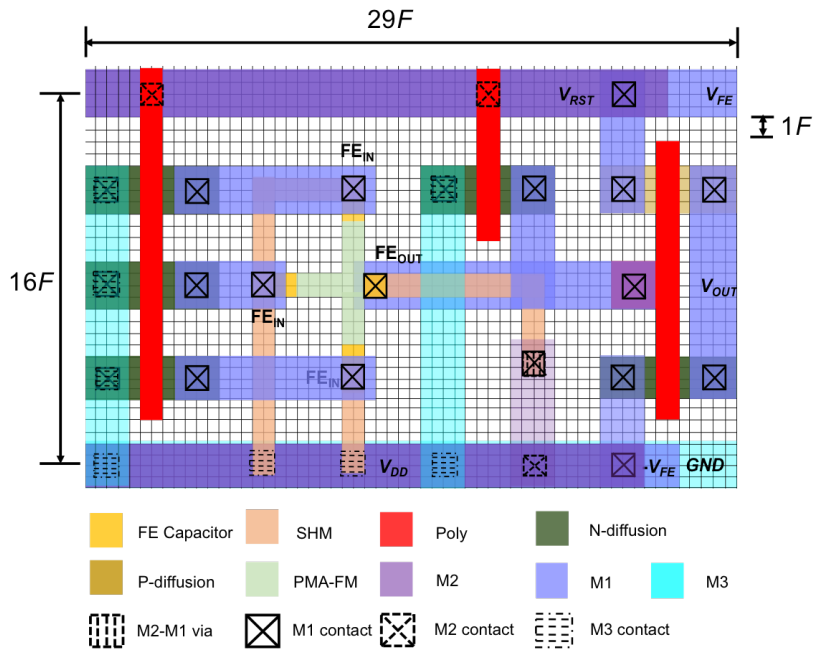


Figure 4.7: Layout of a CoMET–based three-input majority gate.

4.2.3 Layout of CoMET–based majority gate

The layout of MAJ3 corresponding to the schematic shown in Fig. 4.6 for a chosen value of F, is shown in Fig. 4.7. We draw the layout according to the design rules for F as described in detail in [72]. The reset transistor for each input FE capacitor i, $T_{RST,i}$, with $i \in 1, 2, 3$, and the reset transistor for the output FE capacitor, $T_{RST,o}$, are local to the majority gate as shown in the layout. The transistor required to send a charge current through the SHM, T_{PROP}, is shared globally by multiple gates. The dual-rail inverter is local to the majority gate and transfers the information to the next stage. The area of the MAJ3 gate is $29F \times 16F$ nm^2.

4.3 Results and Discussion

The delay of the device is a function of the dimensions of IMA–FM and PMA–FM material parameters, specifically $M_{\text{S,PMA–FM}}$, $K_{\text{U,PMA–FM}}$, A, and α. We explore the design space consisting of the combination of these parameters and analyze their impact

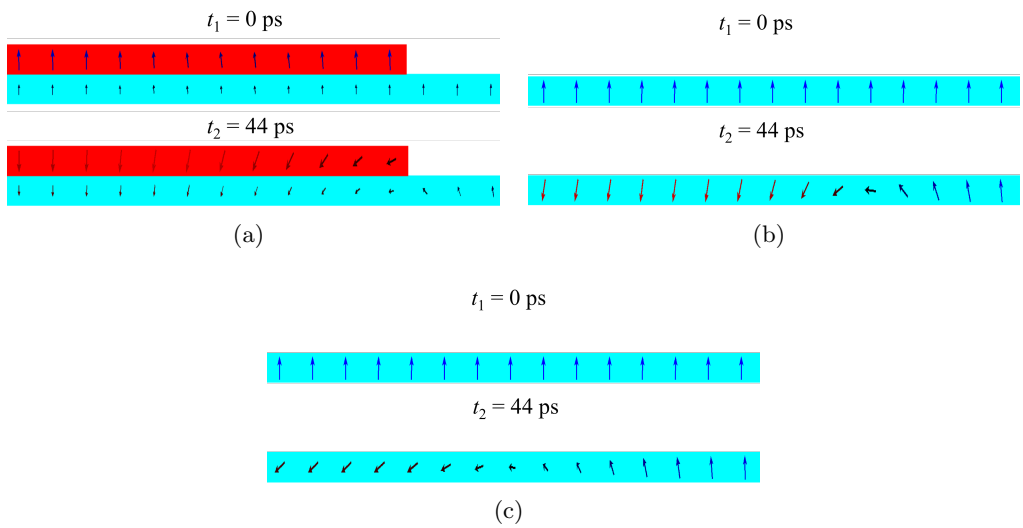


Figure 4.8: DW nucleation in PMA–FM (a) with the composite structure used in this work (b) without the composite structure, i.e., without the IMA–FM with the ME field applied for a region $2F \times 1F \times 1$nm from the left end of PMA–FM and (c) without the composite structure with the ME field applied for a region $1F \times 1F \times 1$nm from the left end of PMA–FM. In (a) the red region refers to the IMA–FM, and the blue region refers to PMA–FM in (a), (b), and (c). The material parameters used in the OOMMF simulation are: $M_{\text{S,PMA–FM}} = 0.5e6$A/m, $K_{\text{U,PMA–FM}} = 0.6e6$J/m^3, $A = 10$pJ/m, $\alpha = 0.01$. The voltages required to nucleate the DW at $t_{nucleate} = 44$ps corresponding to (a) $V_{FE} = 110$mV, (b) $V_{FE} = 350$mV and (c) $V_{FE} = 1.06$V.

on device performance. We demonstrate the results of the design space exploration for $F = 15$nm and show two sample design points for F set to 15nm and 7nm.

4.3.1 Choice of material parameters

The simulation parameters and their values used in this work are listed in Table 4.1. The parameter space is chosen to reflect realistic values: the choice of $A \in \{10pJ/m$, $20pJ/m$, $30pJ/m$, $40pJ/m\}$ is chosen to reflect the typical exchange constant of existing and exploratory ferromagnetic materials. Lowering A further would make the Curie temperature too low [97]. The choice of $M_{\text{S,PMA–FM}} \in \{0.3e6A/m$, $0.4e6A/m$, $0.5e6A/m\}$ and $K_{\text{U,PMA–FM}} \in \{0.5e6J/m^3$, $0.6e6J/m^3$, $1e6J/m^3\}$ allow the mapping of PMA–FM materials to existing materials. The choice of $\alpha \in \{0.01, 0.05, 0.08, 0.1\}$ is

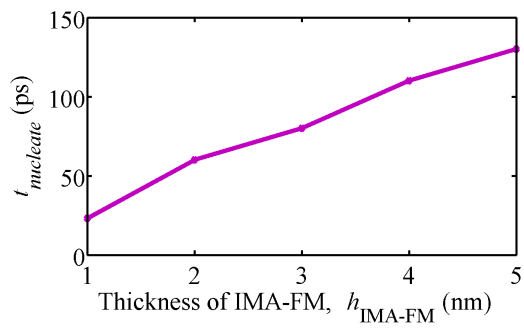


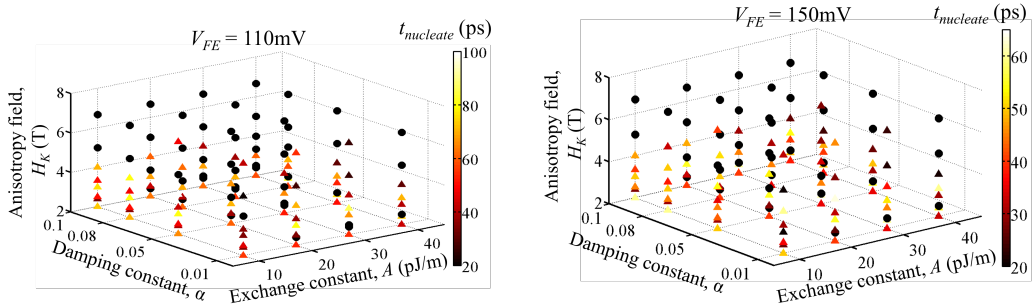
Figure 4.9: Nucleation delay, $t_{nucleate}$, of the CoMET device for $F = 15nm$, as a function of the IMA–FM thickness, $h_{\text{IMA–FM}}$. The PMA–FM material parameters used in the OOMMF simulation are:$M_{\text{S,PMA–FM}} = 0.3e6A/m$, $K_{\text{U,PMA–FM}} = 0.5e6J/m^3$, $A = 10pJ/m$ and $\alpha = 0.05$ (similar trends are seen for other parameter choices).

free of any constraint to material mapping as it can be modified by adequately doping the PMA–FM [98,99]. The saturation magnetization of the IMA–FM, $M_{\text{S,IMA–FM}}$ is set to $1e6$A/m. The value of A and α for the IMA–FM is set to the same value as that of PMA–FM.

4.3.2 DW nucleation

We estimate $t_{nucleate}$ in OOMMF when the DW nucleates beneath the IMA–FM as shown in the snapshots in Fig. 4.8(a). We first relax the composite structure in OOMMF for 200ps before applying the effective ME field as a Zeeman field. This time period allows the PMA–FM to reach an equilibrium state before the DW is nucleated. In a typical circuit, this state could be achieved by the PMA–FM in the time interval between successive switching activity. At the end of 200ps, denoted in the figure as $t_1 = 0$ps, the magnetization of the PMA–FM rests at an angle to the easy axis owing to the strong exchange coupling with the IMA–FM. After applying a Zeeman field, the DW nucleates in PMA–FM at $2F$ after a delay of 44ps.

We compare the voltages required to nucleate the DW in the PMA–FM at approximately the same $t_{nucleate}$, in the absence of the IMA–FM on top of the PMA–FM to provide the initial angle. The procedure to calculate $t_{nucleate}$ is identical to the experiment in Fig. 4.8(a). We perform this analysis for two cases: (i) when the applied Zeeman field acts on a region $2F \times 1F \times 1$nm corresponding to the scenario shown in



(a) (b)

Figure 4.10: Nucleation delay, $t_{nucleate}$, of the CoMET device for F = 15nm as a function of (a) material parameters for V_{FE} = 110mV and (c) material parameters for V_{FE} = 150mV. The triangles indicate successful nucleation and while the circles indicate unsuccessful nucleation.

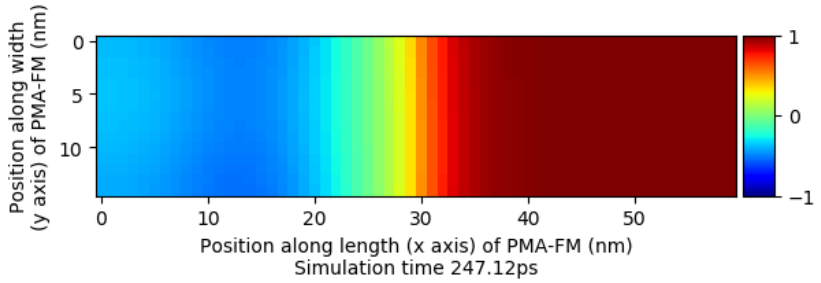
Fig. 4.8(b). The DW nucleates at $t_{nucleate}$ = 44ps at $2F$. However, V_{FE} required to generate the DW is now 350mV. After relaxing the magnetization for 200ps, an absence of IMA–FM translates to a very low initial angle at t_1 = 0ps which necessitates a stronger effective ME field, H_{ME}, and therefore a higher V_{FE} to nucleate the DW for a given $t_{nucleate}$. (ii) The absence of IMA–FM allows us to further compact the CoMET device such that the FE capacitor dimensions are the minimum possible at a chosen value of F. This corresponds to the dimensions, $1F \times 1F \times 5$nm (as opposed to those shown in Fig. 4.6(c)), the region from the left end of PMA–FM on which H_{ME} acts. We find that the voltage required to nucleate the DW at $1F$, as shown in Fig. 4.8(c), is close to 1V. From these two experiments, we conclude that the composite structure facilitates a fast and energy-efficient DW nucleation.

The nucleation of DW in the PMA–FM is not only a function of PMA–FM material parameters, but also depends on the material dimensions of the IMA–FM. As stated in Chapter 4.2, the aspect ratio of the IMA–FM is set to 2:1 to obtain the shape anisotropy necessary for the coupling with PMA–FM. We then explore the dependence of $t_{nucleate}$ on the thickness of IMA–FM, $h_{\text{IMA–FM}}$ and plot the results in Fig. 4.9. As $h_{\text{IMA–FM}}$ increases, it becomes harder to switch the PMA–FM due to strong exchange coupling between IMA–FM and PMA–FM, increasing $t_{nucleate}$. We therefore select $h_{\text{IMA–FM}}$ = 1nm.

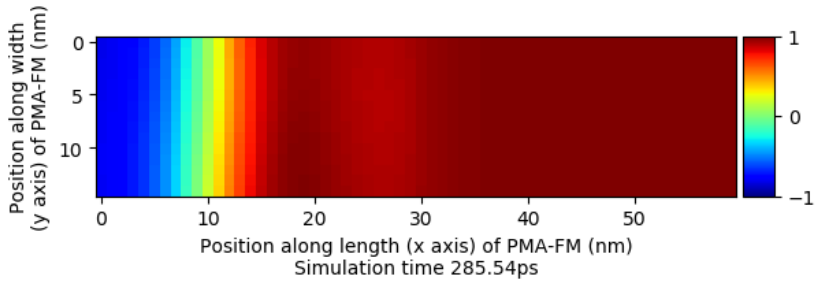
The impact of material parameters of PMA–FM on $t_{nucleate}$ is shown in Fig. 4.10(a) and Fig. 4.10(b) for V_{FE} = 110mV and V_{FE} = 150mV, respectively. It is seen that (a) a larger V_{FE} reduces $t_{nucleate}$, and this can be shown to be consistent with the DW nucleation Equations (4.1–4.3). A larger V_{FE} corresponds to a larger E_{FE} across $\mathrm{FE_{in}}$, which in turn creates a larger H_{ME} to nucleate the DW faster. (b) Lower values of H_K are more conducive to nucleation; a lower anisotropy field makes it easier for H_{ME} to switch the magnetization between the two easy axes and (c) low values of A reduce $t_{nucleate}$ owing to the weaker exchange coupling with the neighboring magnetic domains of the PMA–FM. We note that for $A > 10$pJ/m, the number of design points at which the nucleation does not occur increases. Therefore we pick the lowest value of $A = 10$pJ/m. This choice does not restrict the design search space for DW propagation as $t_{propagate}$ is primarily dictated by the choice of $M_{\mathrm{S,PMA–FM}}$.

4.3.3 DW pinning effects by defects

In the simulations of the DW nucleation, we observed that the DW will not hold its position where it formed. At the stage when the driving current has not been injected, oscillation of the DW occurs along its propagation direction. As an example shown in Fig. 4.11, the DW forms at around 247ps (Fig. 4.11(a)) after an effective magnetic field is applied at 200ps. However, it moves backward towards the left end of the FM (Fig. 4.11(b)) and forward (Fig. 4.11(c)) even without any change in the external conditions. In Fig. 4.12, the shift of the DW position can be seen more clearly with the magnetization of z axis averaged over the width of the PMA–FM along the propagation direction against simulation time. The oscillation of the DW position occurs multiple times during a simulation of over 1000ps.



(a)



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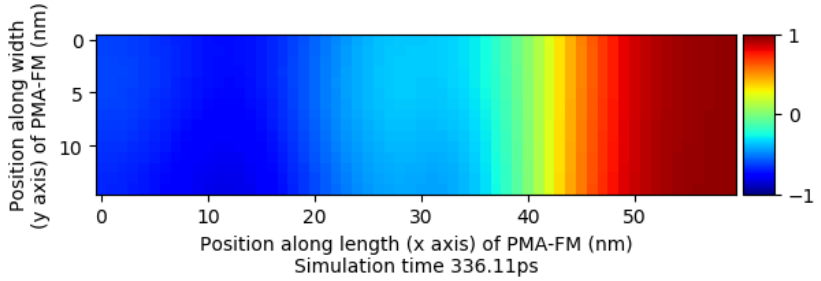


(c)

Figure 4.11: DW positions after nucleation at (a) 247ps, (b) 285ps, and (c) 336ps. The figures show the magnetization in z axis for a PMA-FM film of 60nm in length (x axis), 15nm in width (y axis), and 1nm in thickness (z axis). The range of magnetization is from -1 to 1, indicated with colors shifting from blue to red. The effective magnetic field corresponds to that generated with $V_{FE} = 110$mV from ME coupling effect, same as in Fig. 4.8(a), and is applied at 200ps on the 30nm by 15nm region on the left end.

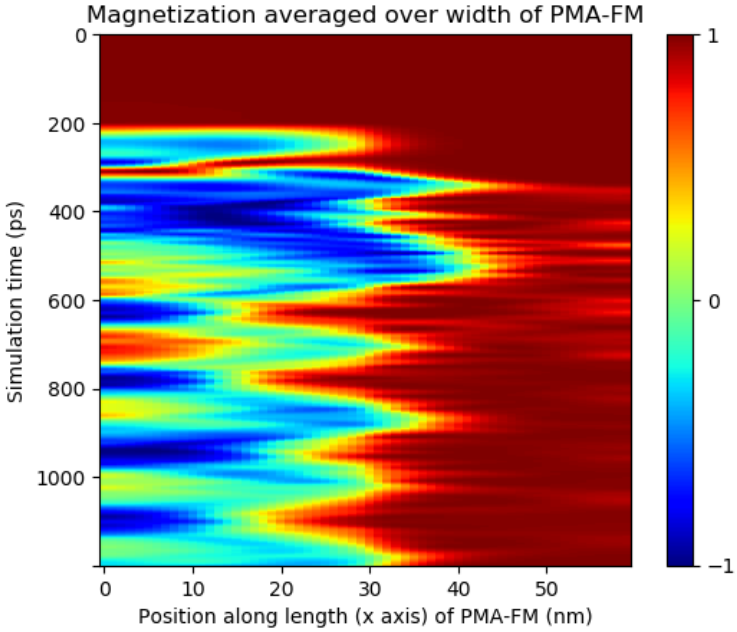
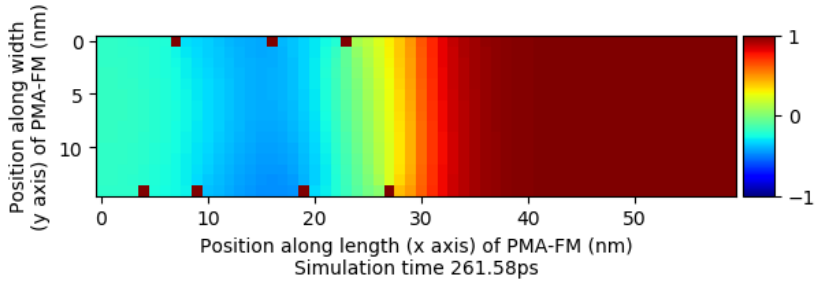


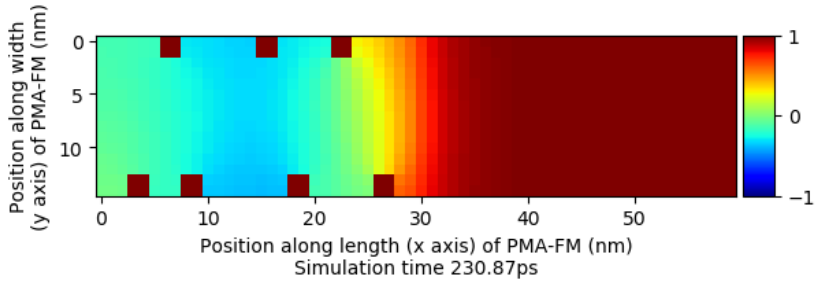
Figure 4.12: Magnetization of z axis averaged over the width along the propagation direction of the PMA-FM against time. The simulation configuration are the same as in Fig. 4.11.

It is suspected that the reason behind such oscillation comes from the smoothness of the energy landscape due to the lack of surface roughness in idea simulation conditions in OOMMF. Therefore, random artificial defects of different sizes are introduced at the edge of IMA–FM and PMA–FM structures as shown in Fig. 4.13 to simulate uneven landscape of the material.

The simulation setting in these experiments is the same as that for Fig. 4.8. The average magnetization of z axis over the width of the PMA–FM along the DW propagation direction is recorded and drawn along in Fig. 4.14 and Fig. 4.15. The result shown in Fig. 4.14 is for square defects of edge length 1nm as in Fig. 4.13(a) and it indicates that the defects indeed help the pinning of DW at the location where it forms to some extent. Similarly pinning effect is also seen in Fig. 4.15 for defects of edge length 2nm as located in Fig. 4.13(b). No significant difference in pinning effect is observed for defects of these two sizes. This suggests that artificial defects allow the states presented by DW to be held as long as it needs until its propagation by driving current, thus giving



(a)



(b)

Figure 4.13: Random square defects of edge length (a) 1nm, (b) 2nm. The simulation configuration are the same as in Fig. 4.11.

better control of the device logic states.

4.3.4 Performance evaluation

The DW propagation delay, $t_{propagate}$ is also studies with an exploration of the same parameters spaces as in the nucleation case [27]. The performance of the CoMET device is obtained by combining the results from both nucleation and propagation. For three different $M_{\mathrm{S,PMA}}$ values, we plot T_{CoMET} vs. E_{CoMET} for MAJ3 in Fig. 4.16 for the two values of V_{FE}. The dual–rail inverter delay, $t_{qtransfer}$, is calculated using the PTM technology models [96]. For a chosen $M_{\mathrm{S,PMA–FM}}$ and V_{FE}, the energy-delay data points are obtained by increasing J_c from $e10A/m^2$ to $e12A/m^2$ in discrete steps. The main observations from Fig. 4.16 are as follows:

- Increasing V_{FE} is seen to reduce T_{CoMET} by reducing $t_{nucleate}$, at the expense of a larger E_{CoMET}.

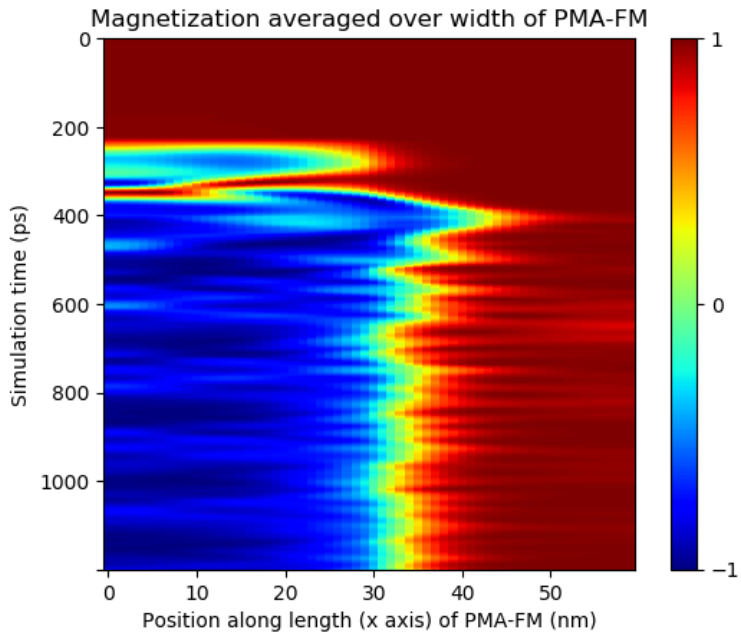


Figure 4.14: Magnetization of z axis averaged over the width along the propagation direction of the PMA-FM again time with square defects of edge length 1nm. The simulation configuration are the same as in Fig. 4.11.

- A higher J_c corresponds to lower T_{CoMET}, but E_{CoMET} is only marginally higher since it is primarily dominated by the transistor energy.

- Initially when J_c increases, T_{CoMET} reduces at the same rate as J_c, thus keeping the energy approximately constant. After a certain point, increasing J_c only gives marginal improvements in delay. This result is consistent with propagation delay simulations in [27]; as J_c increases from 10^{10} A/m^2 to 10^{12} A/m^2, DW velocity increases sharply initially but only increases gradually later.

- A robust design point can be chosen such that T_{CoMET} is less variable with material parameters. This corresponds to the right portion of each curve where the delay only improves marginally with increase in J_c.

The best (T_{CoMET}, E_{CoMET}) for each V_{FE} for MAJ3/INV for $F = 15nm$ and $F = 7nm$ are shown in Table 4.2(A) and (B), respectively. It can be seen that

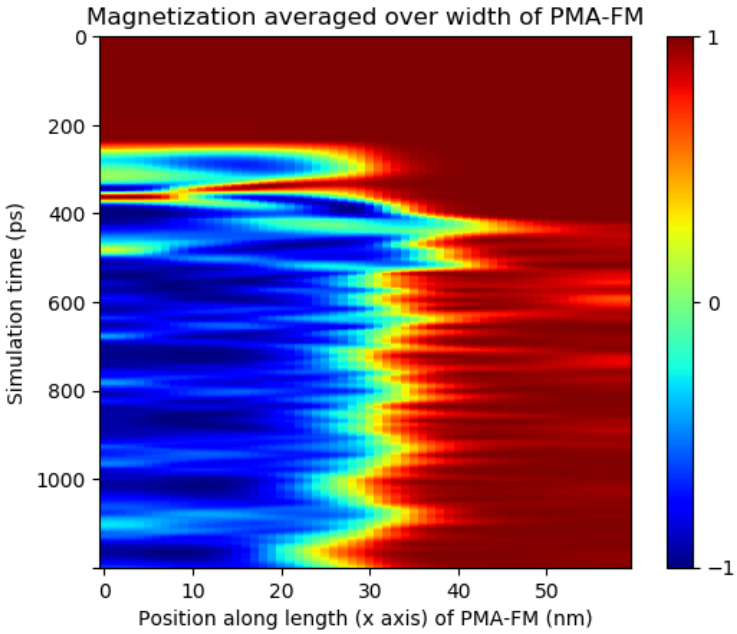
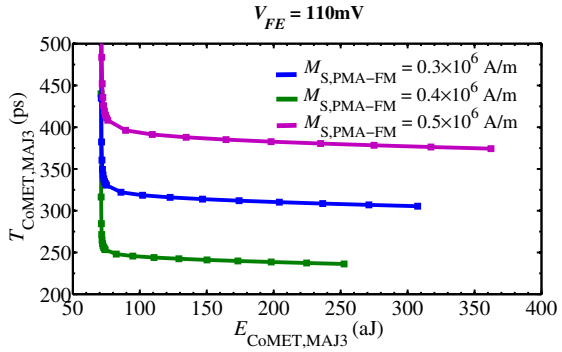


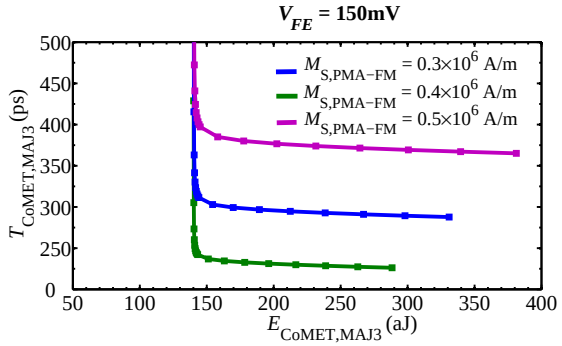
Figure 4.15: Magnetization of z axis averaged over the width along the propagation direction of the PMA-FM again time with square defects of edge length 2nm. The simulation configuration are the same as in Fig. 4.11.

$t_{propagate}$ dominates T_{CoMET} while E_{CoMET} is dominated by energy associated with turning the transistors on and the corresponding leakage. The delay and energy obtained using the CMOS technology given respectively by (T_{CMOS}, E_{CMOS}) for an inverter is $(1.8ps, 38.7aJ)$ at $F = 15nm$ and $(1.6ps, 19.8aJ)$ at $F = 7nm$. For CMOS-based MAJ3 gate, the performance numbers are (14.8ps, 704.2aJ) at $F = 15nm$ and $(11.4ps, 361.6aJ)$ at $F = 7nm$. The CMOS performance numbers were obtained using the PTM technology models [96] at nominal supply voltages of $0.85V$ for $F = 15nm$ and $0.7V$ for $F = 7nm$. Thus we see that a MAJ3 gate can be implemented more energy-efficiently with CoMET than with CMOS.

At these design points, $M_{\text{S,PMA–FM}}$, $K_{\text{U,PMA–FM}}$, and A can be mapped to MnGa–based Heusler alloy [41, 100]. The damping constant, $\alpha = 0.01$ can be engineered by choosing a new composition of PMA–FM. For the FE layer, $BiFeO_3$ (BFO) can be used [44], while the SHM could be β-W, Pt, β-Ta [101–103] or some new materials under investigation.



(a)



(b)

Figure 4.16: Energy vs. delay of the CoMET–based MAJ3 gate for three design points, corresponding to three different $M_{\mathrm{S,PMA-FM}}$ values. Other parameter values: $\alpha = 0.01$, $A = 10\mathrm{pJ/m}$, $K_{\mathrm{U,PMA-FM}} = 0.5e6\mathrm{J/m^3}$.

4.4 Conclusion

A novel spintronic logic device based on magnetoelectric effect and fast current–driven domain wall propagation has been proposed. We have shown that the composite input structure of a FM with IMA placed in contact with a PMA–FM allows circuit operation at low voltages of 110mV and 150mV. A novel circuit structure comprising a dual–rail inverter structure for efficient logic cascading has also been introduced. The impact of the different material parameters on the performance of the device is then systematically explored. An optimized INV has a delay of 98.6ps with energy dissipation of 68.4aJ at 7nm, while a MAJ3 gate runs at 134.8ps and 85.2aJ.

V_{FE} (mV)	$t_{nucleate}$ (ps)	$t_{propagate}$ (ps)	$t_{qtransfer}$ (ps)	T_{CoMET} (ps)
110	35/35	77.4/38.7	8.8/8.8	242.4/165.5
150	30/30	77.4/38.7	8.2/8.2	231.2/153.8

V_{FE} (mV)	E_{FE} (aJ)	E_{TX} (aJ)	E_{Joule} (aJ)	$E_{leakage}$ (aJ)	E_{CoMET} (aJ)
110	2.4/0.8	40.8/24.2	19.8/1.6	16.3/16.3	158.6/85.8
150	4.4/1.5	42.0/30.6	25.5/1.5	22.8/22.8	189.4/112.8

(A)

V_{FE} (mV)	$t_{nucleate}$ (ps)	$t_{propagate}$ (ps)	$t_{qtransfer}$ (ps)	T_{CoMET} (ps)
110	30/30	36.2/18.1	7.9/7.9	148.2/112.0
150	25/25	36.2/18.1	6.2/6.2	134.8/98.6

V_{FE} (mV)	E_{FE} (aJ)	E_{TX} (aJ)	E_{Joule} (aJ)	$E_{leakage}$ (aJ)	E_{CoMET} (aJ)
110	0.5/0.1	16.8/12.0	1.8/0.1	13.7/13.7	65.6/51.8
150	0.9/0.3	21.4/15.3	1.8/0.1	18.5/18.5	85.2/68.4

(B)

Table 4.2: Delay and energy of CoMET–based MAJ3/INV gate for (A) $F = 15nm$ and (B) $F = 7nm$ for the design point corresponding to parameters, $M_{\text{S,PMA–FM}} = 0.3e6A/m$, $K_{\text{U,PMA–FM}} = 0.5e6J/m^3$, $J_c = 5e11A/m^2$, $\alpha = 0.01$, and $A = 10pJ/m$.

Chapter 5

Majority Gate Design and Simulation Methodology based on MESO Device

As CMOS-based designs reach their limits, there is an increasing interest in developing novel device technologies. Spin-based computing shows promise as it embraces emerging physical mechanisms and new materials to enable better device performance and enriched design functionality. Through mechanisms that allow material and feature scaling, spintronics provides a pathway for designing future electronic systems [104], suitable for computational heavy applications required by big data technologies [105–113].

Magnetoelectric spin-orbit (MESO) logic [1,2] is a recently proposed spintronic logic device concept that achieves high energy efficiency by combining the magnetoelectric (ME) coupling effect [4, 114, 115] with the inverse spin orbit coupling (ISOC) effect [7, 30, 116]. Low energy magnetic state switching is enabled by the ME coupling effect and realized with the presence of multiferroic materials or heterostructures [117, 118]. The ISOC effect provides efficient spin-to-charge conversion and facilitates the use of charge-based signal propagation between stages of logic. Unlike technologies such as all-spin logic [20, 119] that use spin current to propagate signals, the use of charge current avoids the large overhead of repeater insertion [120]. Together, the ME and ISOC effects realize energy-efficient transduction between charge and magnetic state variables, and

either could implement majority logic.

In this work, we first develop a simulation framework to determine the energy and delay of a single MESO device as well as cascaded stages of MESO structures. We introduce our method for estimating the delay and energy of the MESO device based on our modified circuit model with conventional elements as well as the FE capacitor model based on Landau-Khalatnikov (LKh) equation. The simulation method and performance measurement are described in Chapter 5.1. Next, we examine issues related to cascading MESO logic stages in Chapter 5.2, with particular attention to the potential for sneak paths that may disrupt correct operation. In Chapter 5.3, we propose and evaluate two approaches for implementing MESO majority gates based on the two different physical mechanisms in the MESO device, and conclude with Chapter 5.4.

5.1 Modeling a MESO inverter

5.1.1 Structure of a basic MESO inverter

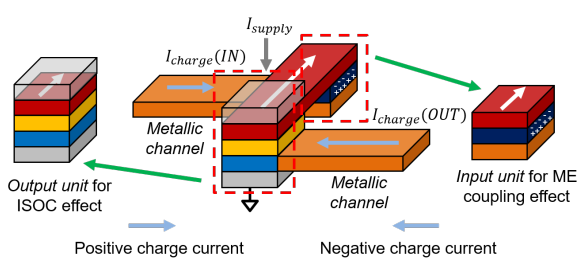


Figure 5.1: Structure of a basic MESO inverter [1, 2].

A basic MESO inverter [1, 2] consists of several major components, as shown in Fig. 5.1: an *input unit* that uses ME coupling to transduce incoming charge current to a magnetic state variable in the in-plane ferromagnet (FM); an *output unit* that generates positive or negative charge current using the ISOC effect, depending on the magnetization in the FM; and a *metallic channel* that conducts charge current from an output unit of the previous stage to an input unit of the current stage.

Fig. 5.2(a) shows a pair of cascaded MESO inverters, each associated with a different state, as indicated by the magnetization direction of the FM in each stage. The presence of two states is characterized by the sign of a parameter, η, defined as the conversion

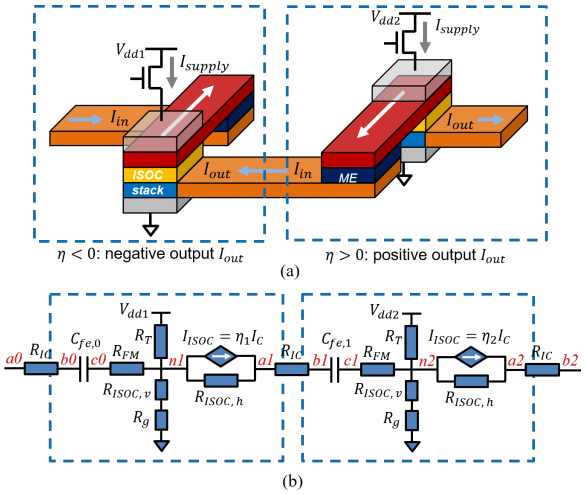


Figure 5.2: Cascaded MESO inverters and their circuit model [1, 2].

ratio between the supply current from transistor and the current generated by the ISOC unit. The sign of η indicates whether the ISOC charge current injected by the output unit goes into ($\eta < 0$) or out of ($\eta > 0$) the metallic channel: this sign is determined by the direction of magnetization in the FM layer in the output unit. More details about η will be elaborated in Chapter 5.1.2. The operation of a single MESO inverter proceeds as follows:

(1) The charge current from the output of the previous stage is injected into the FE material in the input unit of the current stage. The FE material is modeled as a capacitor whose behavior is governed by the LKh equation [121], and the input current generates a voltage that switches its polarization.

(2) The FE capacitor voltage induces a magnetic field on the FM due to the ME effect, flipping its magnetization.

(3) The output unit has a transistor above the ISOC material stack and a ground contact beneath it. A charge current, injected through the transistor, is polarized to positive or negative spin current, depending on the magnetization in the FM [122]. This spin current flows into the ISOC conversion stack beneath the FM, which performs spin-to-charge conversion based on the inverse spin-Hall effect (ISHE) and the inverse Rashba-Edelstein effect (IREE) [7, 30, 116, 123]. Depending on the spin current polarity, either positive or negative charge current flows into the metallic interconnect that drives

the next logic gate.

5.1.2 Circuit model for a MESO inverter

In this chapter, we will introduce a circuit model of a MESO inverter and elaborate upon the ISOC current conversion model as well as the response of the FE capacitor polarization. We will then show how a MESO stage can be analyzed using numerical circuit simulation to extract its delay and energy.

Circuit model

A circuit model for the MESO inverter was proposed in [1, 2]. We extend this model to show the model for cascaded pair of MESO inverters in Fig. 5.2(b), which shows the interations between successive stages. Our interest is in modeling the time required by this structure to charge the FE capacitor in the output unit, and accordingly we isolate the subcircuit that contributes to driving this capacitor and illustrate it in Fig. 5.3. This differs slightly from the model in [1, 2], where node c was connected directly to ground; in contrast, we show that this path goes through a few resistors.

The transistor is connected to a supply voltage, V_{dd}, and is modeled as an effective resistance R_T. This is valid given that gate capacitance is small enough compared to the effective capacitance of the FE capacitor, and thus a gate transition does not induce a coupled voltage spike at the source that moves the transistor out of the linear region. Under the assumption that the transistor driving each stage is clocked during the transition, only the R_T for the current stage must be considered. The FM and the ISOC material stack are modeled as a vertical resistance $R_{ISOC,v}$, and are connected to the ground lead resistance, R_g. The generation of charge current from spin current is modeled as a current controlled current source (CCCS), with a horizontal resistance $R_{ISOC,h}$ representing the internal ISOC source resistance. The interconnect resistance R_{IC} associated with the metallic channels leads to one plane of the FE capacitor. The other plane of the FE capacitor is connected to a resistance R_{FM} representing entire horizontal resistance of FM. The FM is then connected to the vertical ISOC unit and the ground lead of the next MESO inverter, represented by $R_{ISOC,v}$ and R_g from the next stage.

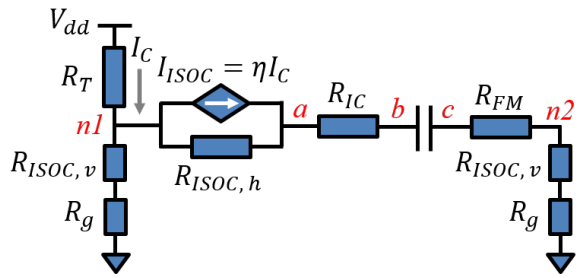


Figure 5.3: Circuit model for a single MESO inverter [1, 2].

Model for the ISOC unit

The spin-to-charge conversion occurs in the ISOC stack based on the ISHE and IREE effects. The conversion between the spin current I_s and the generated charge current I_{ISOC} can be written in the following form [1, 2]:

$$I_{ISOC} = \frac{1}{w}\left[\lambda_{IREE} + \Theta_{SHE}\lambda_{sf}\tanh\left(\frac{t}{2\lambda_{sf}}\right)\right] \cdot I_s \tag{5.1}$$

Here, w is the width of the ISOC conversion unit and λ_{IREE} represents the IREE length [124]. The bulk ISHE is indicated by the spin-Hall angle Θ_{SHE}, spin diffusion length λ_{sf}, and thickness t. The spin current, I_s, injected into this stack is polarized by the FM from the charge current I_c, i.e.,

$$I_s = \pm P \cdot I_c \tag{5.2}$$

where P is the spin polarization. Therefore the conversion ratio $\eta = I_{ISOC}/I_c$ for the CCCS can be written as

$$\eta = \pm\frac{P}{w}\left[\lambda_{IREE} + \Theta_{SHE}\lambda_{sf}\tanh\left(t/2\lambda_{sf}\right)\right] \tag{5.3}$$

Using simulation parameters that will be detailed in Table 5.1, the transient waveform for switching the voltage at node $n1$ and node b is shown in Fig. 5.4 when the sign of η changes from negative (before 0ps) to positive (after 200ps). It can be seen that the steady-state voltages for b are asymmetric about zero. To understand this, consider the steady state, where the FE capacitor can be treated as an open circuit, and no current flows through R_{IC}. Thus, the voltage drop on the FE capacitor equals the voltage drop at node b, i.e., the voltage across $R_{ISOC,h}$ plus the voltage of node

$n1$. The plot shows that the voltage at node $n1$ settles to 8.0mV in the steady state. Since no current flows into R_{IC}, the charge current I_{ISOC} must flow to ground through $R_{ISOC,h}$. From Eq. (5.3), the magnitude of η is identical for either FM polarization, but the sign depends on the polarization: as a result, in this case, the voltage drop from node b to node $n1$ is $\pm$40mV. This results in asymmetric steady-state voltage levels of 8mV$-$40mV $= -$32.0mV and 8mV+40mV $= +$48.0mV, as seen in Fig. 5.4.

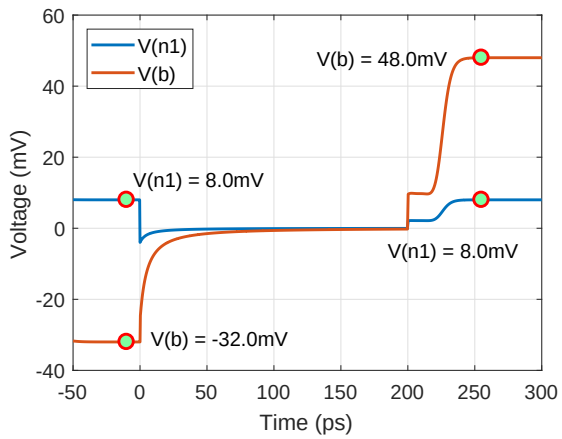


Figure 5.4: Voltage at nodes $n1$ and b for a single MESO inverter, with negative η before 0ps and positive η after 200ps.

Model for the FE capacitor

The LKh equation [121, 125, 126] governs the temporal response of the electric polarization P in the FE capacitor to the electric field E:

$$\gamma \frac{dP}{dt} = \frac{1}{2}\beta E - g_2 P - g_4 P^3 - g_6 P^5 \tag{5.4}$$

where γ is a parameter indicating the switching speed, and β, g_2, g_4, and g_6 are obtained as fitting parameters that match experimental data to this theoretic model [126]. In the Appendix C, we demonstrate a hysteresis loop obtained based on Eq. (5.4) and the related remnant polarization.

5.1.3 Circuit simulation

The components associated with the MESO circuits in Figs. 5.2(b) and 5.3 can be classified into elements defined by linear algebraic equations (resistors, supply voltage source, CCCS), and by nonlinear differential equations (FE capacitor). We analyze this structure by discretizing the differential equations in time, and at each time step, using Newton-Raphson linearizations to obtain affine representations of circuit elements that are solved by modified nodal analysis (MNA).

We focus on the FE capacitor that is represented by the LKh equation, which is a nonlinear differential equation. We show below how the FE capacitor can be represented using an $I - V$ relationship, eliminating the polarization variable P.

We begin with the equation $Q = A(\epsilon_0 E + P) = A(\epsilon_0 V/T + P)$ that describes the free charge Q as a function of voltage V and polarization P on a capacitor with area A and a distance T between plates: here T is the thickness of the FE capacitor. Based on the above equation, we obtain the following linear relation between P, I, and V in the $(i+1)^{th}$ time step:

$$P = \left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0 V_i}{T}\right] \tag{5.5}$$

where V_i and V_i are the values of V and P, respectively, in the ith time step, and h is the simulation time step. A derivation of Eq. (5.5) is provided in the Appendix C.

Next, we revisit Eq. (5.4) and replace electric field $E = V/T$:

$$\begin{aligned} \gamma \frac{dP}{dt} &= \frac{\beta V}{2T} - f(P) \\ \text{where } f(P) &= g_2 P + g_4 P^3 + g_6 P^5 \end{aligned} \tag{5.6}$$

To eliminate P and create an $I - V$ relationship for the FE capacitor, we combine Eqs. (C.4), (5.5) and (5.6) to obtain the nonlinear $I - V$ relation at the $(i+1)^{\text{th}}$ time step:

$$\begin{aligned} g(I,V) = \left[\frac{\gamma}{A}\right] I - \left[\frac{\gamma\epsilon_0}{Th} + \frac{\beta}{2T}\right] V + \frac{\gamma\epsilon_0}{Th} V_i + \\ f\left(\left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0}{T} V_i\right]\right) = 0 \end{aligned} \tag{5.7}$$

where g is a polynomial in I and V. Using standard circuit simulation approaches, we now create an affine approximation to this function about a guess, (I^k, V^k), where the

superscript k represents the Newton-Raphson iteration number:

$$g(I^k, V^k) + \frac{dg}{dI}\Big|_{I^k,V^k}(I - I^k) + \frac{dg}{dV}\Big|_{I^k,V^k}(V - V^k) = 0 \tag{5.8}$$

This provides a stamp [127] for the FE capacitor element, which when combined with the stamps for the resistors and CCCS, yields the MNA equations for each Newton-Raphson iteration.

The simulation method is summarized in Algorithm 2. After initialization (line 1), the entire simulation contains two nested loops: the outer loop (lines 2–12) performs time-stepping, setting up the computations for V, I, and P at each time step, while the inner loop (lines 5–10) performs Newton-Raphson iterations to solve the nonlinear equations at each time step. The Newton-Raphson iterations develop the affine form in Eq. (5.8) based on the partial derivatives of $g(I, V)$, (Eq. (5.7)), which is used to create and solve the MNA equations (line 8).

Algorithm 2 Simulation method for a MESO gate

Input: Circuit netlist, initial polarization P_0 and voltage V_0;
Output: Polarization P of the FE capacitor, voltage V and current I of every node in the circuit over the simulation period.

1: $t_i \leftarrow 0$, $i \leftarrow 0$, $P_i \leftarrow P_0$, $V_i \leftarrow V_0$. ▷ Initialization for time zero
2: **repeat**
3: $t_{i+1} \leftarrow t_i + h$, $i \leftarrow i + 1$. ▷ Time-stepping to the next simulation time
4: $k \leftarrow 1$, $V^0 \leftarrow V_i$ and $I^0 \leftarrow I_i$. ▷ Newton-Raphson initializations
5: **repeat** ▷ Newton-Raphson iterations at time step i
6: Calculate dg/dI and dg/dV at I^k, V^k, based on $g(I, V)$ in Eq. (5.7).
7: Construct the affine relation between V and I based on Eq. (5.8).
8: Construct the MNA equations and solve them for V and I.
9: $k \leftarrow k + 1$.
10: **until** V and I converge to the solution at time step i.
11: Use V and I to calculate P at time step i based on Eq. (5.5).
12: **until** End of simulation time.

5.1.4 Calculation of delay and energy for the MESO inverter

Calculation of the MESO inverter delay

The delay of a single MESO inverter includes two parts: the delay of switching the FE capacitor polarization, and the delay of switching the magnetization in the FM layer.

Delay of switching FE capacitor polarization: As mentioned in Chapter 5.1.2, the incoming charge current from previous MESO inverter is injected into the ME unit, creating a voltage drop across the FE capacitor and switching its polarization. The switching response of the FE capacitor polarization is governed by the LKh equation

and simulated numerically using the techniques from the previous chapter. As a baseline example, we perform the simulation to measure the inverter delay based on the parameters in Table 5.1. The resistances related to ISOC stack are estimated based on information from [128], with the rest of the parameters from [1,2]. For the FE capacitor, the parameters in Eq. (5.4) are set to $\beta = 500$, $\gamma = 3.5 \times 10^{-4}$, $g_2 = -2.0 \times 10^3$ Jm/C^2, $g_4 = -2.4 \times 10^9$ Jm^5/C^4, and $g_6 = 4.2 \times 10^{10}$ Jm^9/C^6 [126].

Table 5.1: Simulation parameters for the MESO circuit.

Parameter	Value
V_{dd} (source voltage)	100mV
η (conversion ratio)	1.0
A (ferroelectric capacitor area)	10×10nm^2
T (multiferroic layer thickness)	5.0nm
R_T (equivalent resistance of transistor)	23kΩ
R_g (ground lead resistance)	500Ω
$R_{ISOC,v}$ (vertical resistance of ISOC stack)	1.5kΩ
$R_{ISOC,h}$ (horizontal resistance of ISOC stack)	10kΩ
R_{IC} (resistance of interconnect)	1kΩ
R_{FM} (resistance of FM)	1kΩ
C_g (gate capacitance, per inverter)	0.2aF
V_g (gate voltage)	0.73V

As elaborated in Chapter S.4 of Appendix D, the rise time t_r, defined as the time required for the signal to transition from its 10% point to its 90% point, is 28.9ps. The fall time is analogously defined and obtained as 46.8ps. The average switching delay is $t = (t_r + t_f)/2 = 37.9$ps.

As mentioned in Chapter 5.1.2, the voltage drop across FE capacitor (between node b and c) has a higher absolute value when η is positive (48mV) compared to the case when η is negative (32mV), leading to the asymmetry in the rising and falling transition as $t_r < t_f$. This symmetry is inevitable due to the circuit structure, but could be alleviated if the resistance to ground from $n1$, $(R_{ISOC,v} + R_g)$, could be reduced and/or if the conversion rate, η, could be increased. Both correspond to materials-related advances. For example, reducing the $(R_{ISOC,v} + R_g)$ from $2k\Omega$ to 500Ω at the same η would change the steady-stage voltages to 44.7mV for $\eta > 0$ and -40.4mV for $\eta < 0$, with $t_r = 26.6$ps and $t_f = 30.2$ps, and a smaller average delay of $t = 28.4$ps.

Delay of switching FM magnetization: After the polarization of the FE capacitor is switched, the FM magnetization will be switched due to the ME effect. This delay is added directly to the switching delay of the FE capacitor to obtain the inverter delay. As in [1, 2], the switching delay of the FM is treated as a fixed time, which is determined by the in-plane FM material parameters and the FE material properties. When the sign of electric polarization P in the FE capacitor changes, this constant latency representing the switching of FM follows, after which the sign of η in the next MESO inverter becomes opposite to the sign of P in current MESO inverter.

Calculation of MESO inverter energy

The MESO device energy per transition consists of two parts: (i) the energy dissipated by the MESO inverter comes from the supply source through the transistor, i.e., the product of the source voltage V_{dd}, the current through the transistor resistance I_{supply}, and the delay of the MESO inverter t, and (ii) the energy for charging the gate capacitor, C_g. The total energy is given by

$$E = V_{dd} \cdot I_{supply} \cdot t + C_g \cdot V_g^2 \tag{5.9}$$

Note that the energy related to the ME coupling effect enabled FM switching is the charging energy of the FE capacitor. The charging process completes during the pulse t and is part of the first term in Eq. (5.9). For circuits with multiple MESO gates, if each gate i is pulsed for time t_i during its transition, the first term is altered to $V_{dd} \cdot I_{supply} \cdot \sum t_i$. Using the parameters in Table 5.1, the rise and fall switching energies are 13.4aJ and 19.2aJ, respectively, where $C_g V_g^2 = 1.1$aJ in each case.

5.2 Sneak paths in cascaded MESO inverters

As stated in Chapter 5.1.2, since the FE capacitor acts as an open circuit at steady state, the voltage drop across a FE capacitor (between node b and c as shown in Fig. 5.3) in a single MESO inverter model is determined by the voltage drop across $R_{ISOC,h}$ (between node $n1$ and a), plus the node voltage at $n1$. In this figure, the voltage for one plate of the FE capacitor, at node c, is zero since no current flows through the resistors between

c and ground in steady state; the same is true of the simpler model in [1, 2], where c is directly connected to ground.

However, the simplifications of considering a single stage must be reexamined for the case where inverters are cascaded. The circuit model for this case is shown in Fig. 5.2(b). Assuming that each stage is clocked while it is switching, the transistor for the first gate is turned off after $C_{fe,1}$ is charged, and the transistor for the second gate is turned on. In other words, R_T for the second gate was an open circuit while $C_{fe,1}$ was being switched, but enters the circuit after the FE capacitor is charged. This creates two sneak paths:
(i) A discharging path from b to ground through $R_{ISOC,h}$ and R_g (the CCCS goes to zero since $I_s = 0$ when the transistor is off), that sets the voltage of b to zero in the steady state.
(ii) An additional charging path to c through $n2$ that could corrupt the stored value on $C_{fe,1}$.

If only the former path were present, this would not be a cause for concern, since the polarization would move to its nonzero remnant polarization value when the voltage across the capacitor decays to zero. In this chapter, we show that the latter sneak path, when coupled with the former, may change the voltage drop across the FE capacitor and thus inadvertently switch its polarization under some clocking scenarios. This can be avoided, but imposes additional overheads and delay constraints in the design of MESO gates. We now consider the following two clocking scenarios:

- *Pulsed clocking:* Each MESO inverter in a cascade is turned on by a single pulse for a certain period of time.

- *Always-on:* Every MESO inverter in a cascade is turned on for the entire period of operation of the circuit.

5.2.1 Sneak paths under pulsed clocking

Fig. 5.5 shows the voltage waveform that clocks the transistors for two successive stages in a cascaded MESO inverter chain, and the circuit models during these two pulses. The operation of the circuit can be divided into several steps:
• As shown in Fig. 5.5(b), when the first pulse $t_{on,1}$ turns on the supply current, the

generated ISOC current will start to charge the FE capacitor in the first stage. For illustration, we consider the case where $\eta > 0$ (the $\eta < 0$ case is analogous): here, the voltage drop across $C_{fe,1}$ will be positive ($V(b) > V(c)$) and the polarization will switch to its positive saturation value.

• Next, in the off period t_{off}, the polarization in $C_{fe,1}$ drops towards its remnant value, and the magnetization in the adjacent ferromagnet is switched by the ME effect.

• The second pulse, $t_{on,2}$ in Fig. 5.5(a) corresponds to the circuit shown in Fig. 5.5(c), and serves to charge node b_2, setting $C_{fe,2}$ to a negative polarization. However, this pulse will also pull up the voltage at node c_1 through the path $V_{dd2} \rightarrow n2 \rightarrow c2$, while the sneak path $b1 \rightarrow a1 \rightarrow n1 \rightarrow$ ground will discharge the plate of $C_{fe,1}$ on the node $b1$ side. Thus, a negative voltage between node $b1$ and $c1$ may be created. This voltage sets up a transient that can change the polarization of $C_{fe,1}$ from positive to negative, which may cause an inadvertent error.

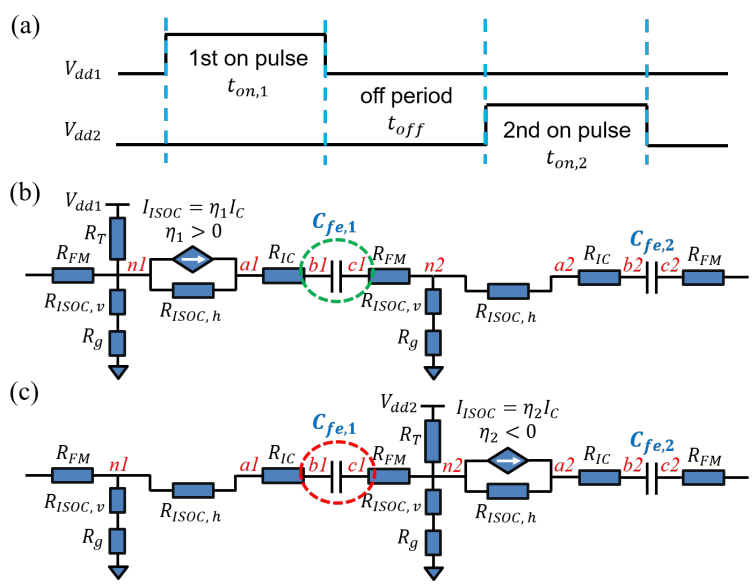


Figure 5.5: (a) A pulsed clocking waveform. (b) and (c) Equivalent circuit representations during successive clock pulses.

For the case when $t_{on,1} = t_{on,2} = 50ps$ and $t_{off} = 200ps$, as shown in Fig. 5.6(a), under the technology parameters in Table 5.1, we show the transient behavior of the polarization in the FE capacitor, $C_{fe,1}$, in Fig. 5.6(b). The choices for the on pulse

width are based on our simulation results for single inverter transition time as in Chapter 5.1.4. The polarization should have remained positive after 50ps, but it can be seen an inadvertent error is caused as $C_{fe,1}$ is switched to a negative polarization during $t_{on,2}$ due to the sneak path.

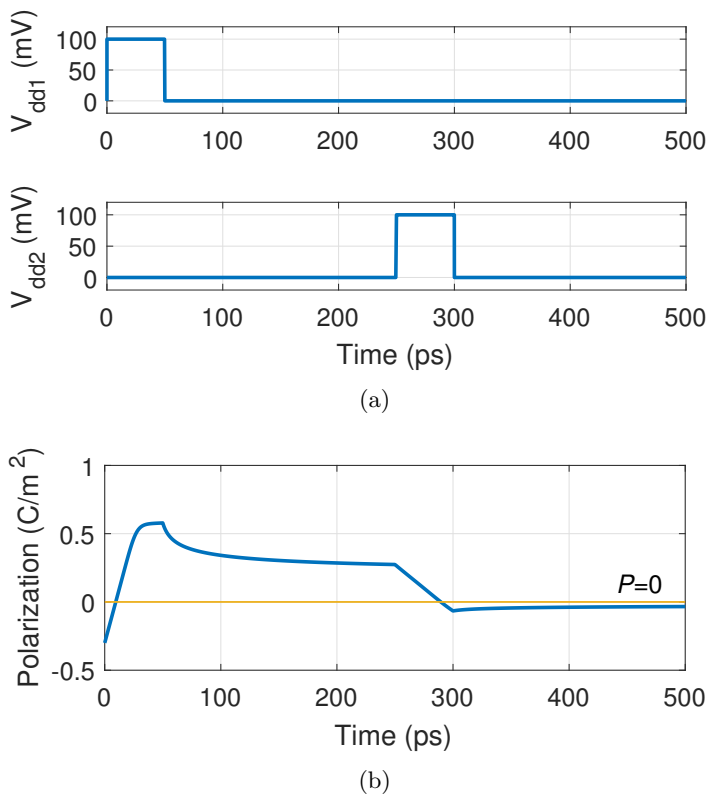
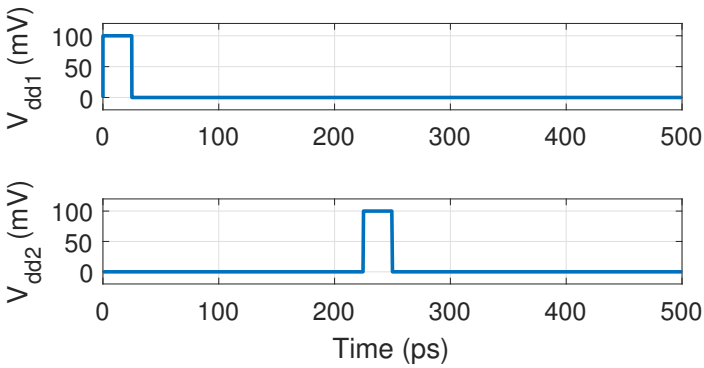


Figure 5.6: (a) Waveform for two successive on pulses (50ps pulse width, 200ps off time) for two cascaded MESO inverters, resulting in (b) an inadvertent polarization error in $C_{fe,1}$.

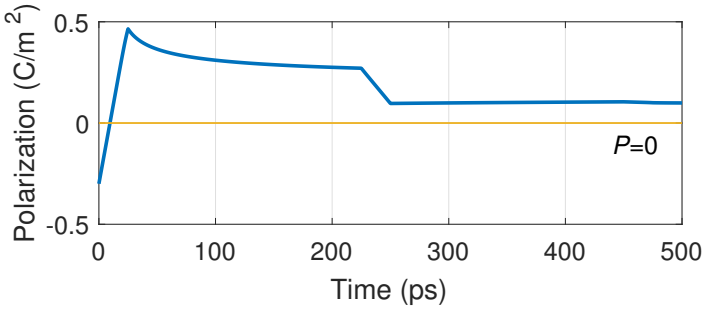
This inadvertent error may be avoided by optimizing the operation periods. For example, in Fig. 5.7, when we alter $t_{on,1} = t_{on,2} = 25$ps, the polarization remains positive even after the second pulse, even in the presence of a sneak path.

5.2.2 Sneak path effects under always-on clocking

The always-on clocking model negates the effect of sneak paths completely. Under this model, all transistors are on for the entire duration, and the circuit model is identical



(a)



(b)

Figure 5.7: (a) A modified waveform with 25ps pulse width, 200ps off time. (b) $C_{fe,1}$ functions correctly, retaining $P > 0$.

to that shown in Fig. 5.2(b). In this mode, the two nodes $b1$ and $c1$ on the two sides of the two plates for $C_{fe,1}$ are both connected to supply current paths, and there is no sneak path discharging the FE capacitor. However, the energy consumption here is high as the V_{dd} supply constantly provides current to the system.

In summary, the pulse time matters in several respects. As explained in Chapter 5.1.4, smaller pulse time is preferred for lower energy consumption. Nonetheless enough pulse width is still required to guarantee successful switching. Pulse time is also important in the occurrence of sneak path effects as discussed in Fig. 5.6 and Fig. 5.7. Choosing a proper pulse time (25ps in Fig. 5.7) could prevent the electric polarization from going to the undesired negative region (as seen in Fig. 5.6(b) at 300ps) due to the sneak path, while the FE capacitor still have enough time to complete a successful switching.

5.3 MESO-based majority gate design

We now discuss how to construct a majority gate based on two approaches for switching the FE capacitor polarization at the next stage. We use the gate inputs to either

- generate competing domain walls (DWs) that switch the magnetization at the FM output, or
- generate competing charge currents.

These gates calculate the minority amongst the three inputs. Instead of using the term "minority gate" or "majority complementary gate", we use the term "majority gate" as in [15].

5.3.1 Majority gate using competing DWs in the FM

A three-input majority gate could be formed by feeding each input to a structure similar to a MESO inverter, and connecting their FMs together into a single merged structure driving an output ISOC unit, as illustrated in the Fig. 5.8. Each input ME unit switches the magnetization of the partial FM region above it, and propagates a domain wall that transmits the magnetization from three input branches to the junction. The majority magnetization will propagate to the output branch O in a properly designed FM [18] with a switching time of 200ps. Next, as in the case of the MESO inverter: the magnetization at the output O determines the direction of the charge current generated out of the ISOC unit in the output stack, switching the polarization of the input FE capacitor of the next gate.

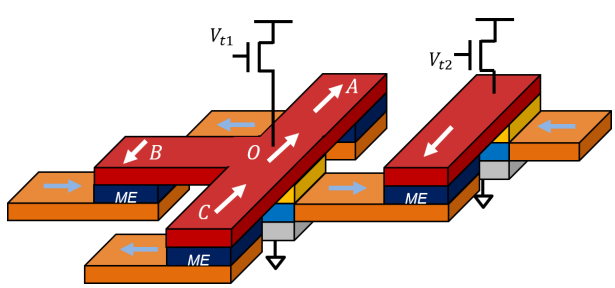


Figure 5.8: A majority gate with competing DWs.

In computing the energy for a gate, we count the energy required to switch O and to switch the input FE capacitor of the next gate. Therefore, the energy for switching the polarization in the FE capacitors in each input ME unit of the current gate is counted towards the energy consumption of the previous MESO gates. Based on this approach, the energy for this majority gate is identical to a single MESO inverter, as given by Eq. (5.9), and consists of the energy required to drive the load FE capacitance and the energy required to switch the transistor above O. Similarly, the delay corresponding to switching the polarization of the load FE capacitor is the same as that for a single MESO inverter delay, and as before, the delay of propagating the signal through the FM is treated as a constant. Therefore, the delay and energy consumption of this majority gate is the same as that in Chapter 5.1.4.

5.3.2 Majority gate using charge currents

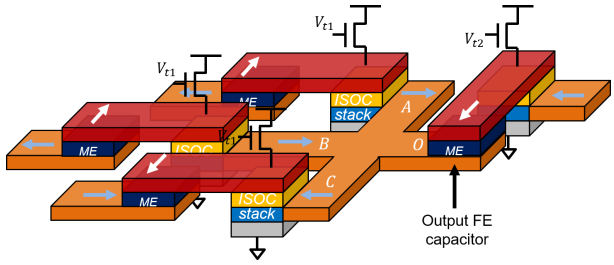


Figure 5.9: A majority gate based on competing charge currents.

Alternatively, majority gates can be implemented using the charge current, as shown in Fig. 5.9. Here, the three metallic channels A, B, and C going out of each ISOC unit merge together and connect to a common FE capacitor though the output branch O. The majority direction of the charge current in the three metallic channels determines whether the voltage drop on the output FE capacitor is positive or negative, which realizes the majority function. We show that the current to the load is not the algebraic sum of the I_{ISOC} values in each of the three branches, and other circuit elements also play a part.

The output voltage of the majority gate

The operation of the gate is captured by the circuit model in Fig. 5.10. The polarization each FE capacitor $C_{fe,k}$ $(k = 1, 2, 3)$ determines the magnetization in the adjacent magnets through the ME effect, and consequently the sign of η for each ISOC unit. The sign of each η indicates not only the direction of charge current in the three channels, but also the voltage level at nodes $n4$, $n5$, and $n6$: a positive η results in $V(ni) > 0$ $(i = 4, 5, 6)$ in the corresponding branch; otherwise $V(ni) < 0$.

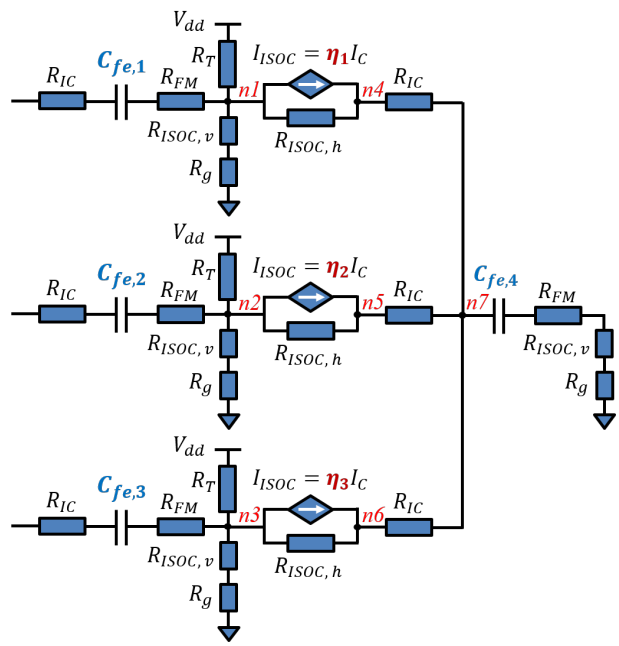


Figure 5.10: Circuit model for the charge-based majority gate.

Since an FE capacitor is an open circuit in the steady state, the voltage drop across $C_{fe,4}$ is determined by $V(n7)$ with the opposite plate at ground. The voltage at node $n7$ is a result of voltage division between $V(ni)$ $(i = 4, 5, 6)$ through the channels: a branch with $\eta > 0$ induces a higher voltage and will inject current into the branch with $\eta < 0$, so that

$$\min_{i \in \{4,5,6\}} V(ni) \leq V(n7) \leq \max_{i \in \{4,5,6\}} V(ni) \tag{5.10}$$

Therefore, if the inputs with positive η are in the majority [minority], $V(n7)$ will stabilize at a positive [negative] value.

Table 5.2: Steady-state voltages in a charge current based MESO majority gate for different input combinations.

Sign of η on the inputs	Node voltages			
	$V(n4)$	$V(n5)$	$V(n6)$	$V(n7)$
$+ + +$	48.0mV	48.0mV	48.0mV	48.0mV
$+ + -$	25.5mV	25.5mV	19.4mV	23.5mV
$+ - -$	1.2mV	−5.2mV	−5.2mV	−3.1mV
$- - -$	−32.0mV	−32.0mV	−32.0mV	−32.0mV

From Table 5.2, the cases with three or zero positive η values show no voltage difference between $V(ni)$ $(j = 4, 5, 6)$, and thus $V(n7)$ equals each $V(ni)$ since no current flows through the metallic channel. In the other two cases, the positive η branch(es) inject(s) current into the negative η branch(es), even in the steady state. This creates a voltage divider that determines the voltage at the intermediate node, $n7$.

The voltage values are not symmetric, e.g., the case where all inputs have $\eta > 0$ has a larger output voltage than the case where all inputs have $\eta < 0$. The root cause of this is similar to the asymmetry seen in the voltage drop on the FE capacitor in a MESO inverter under negative and positive η, as discussed in Chapter 5.1.2. For cases where all three η values do not have the same sign, the magnitude of $V(n7)$ is even lower, although for these parameter values, the majority gate operates correctly, i.e., the sign of the voltage at $n7$ matches the majority sign of the η values at the gate inputs.

However, this may not always be true, and $V(n7)$ depends on the voltage divider action. In fact, if the value of $(R_{ISOC,h} + R_g)$ is too high, the voltage for the $+ - -$ case may not go below zero, and the output FE capacitor may incorrectly carry a positive P. This effectively places an upper bound on $(R_{ISOC,h} + R_g)$. Keeping all other simulation parameters unchanged, if this total resistance is increased from 2KΩ to 3KΩ, then the polarization will not be switched to a negative value. In this case, the values of $V(n4)$, $V(n5)$, and $V(n6)$, are 4.2mV, −1.9mV, and −1.9mV, respectively. The voltage divider action then sets $V(n7) = 0.13mV$, which incorrectly results in $P > 0$ at the output FE capacitor.

Practically, switching at small voltages such as 3.1mV is challenging under current technologies and may even fail since it is smaller than the coercive field of typical candidate materials. Increasing the value of η or $R_{ISOC,h}$ and decreasing R_g or $R_{ISOC,v}$ in new technologies can help in raising the voltage to a higher value. For example,

reducing $R_g + R_{ISOC,v}$ from $2k\Omega$ to $1k\Omega$ and increasing η from 1.0 to 2.0 would raise the voltage from 3.1mV to 17.8mV.

Energy and delay of the majority gate

Table 5.3: Transition times for the output FE capacitor polarization in a charge current based MESO majority gate.

	Before transition		After transition		Delay	Energy
	Input η	$V(n7)$	Input η	$V(n7)$	(ps)	(aJ)
Rise	$- - -$	−32.0mV	$+ + +$	48.0mV	13.5	18.5
	$- - -$	−32.0mV	$+ + -$	23.5mV	26.0	34.1
	$- - +$	−3.1mV	$+ + +$	48.0mV	11.7	16.4
	$- - +$	−3.1mV	$+ + -$	23.5mV	22.4	30.6
Fall	$+ + +$	48.0mV	$- - -$	−32.0mV	21.3	26.5
	$+ + +$	48.0mV	$+ - -$	−3.1mV	155.4	188.4
	$+ + -$	23.5mV	$- - -$	−32.0mV	20.4	25.9
	$+ + -$	23.5mV	$+ - -$	−3.1mV	154.1	189.0

Table 5.3 provides a summary of the rise and fall transition time under various input combinations. The overall delay of the majority gate is the transition time listed, added to the 200ps delay of the ferromagnet. A rise transition goes from a case where the majority of η values is negative to one where the majority is positive. From Table 5.2, the negative and positive majorities each correspond to two cases, and therefore four cases must be considered. The same is true of the fall transition.

The table shows a large range of delay values for the 90% switching time of the output FE capacitor polarization, depending on the initial and final input states. This can be ascribed largely to the voltage drop on the FE capacitor after the transition: larger steady-state values of $V(n7)$ correspond to smaller delays. There are two cases in the fall transition time that are significantly larger than others, when inputs transition to $+ - -$ from different input states. Here, the final steady-state voltage at $n7$ has the smallest magnitude. This causes a small electric field across the FE capacitor, resulting in a slow transition. Considering the worst-case transition, for a three-input majority gate based on charge current, we have $t_r = 26.0$ps, $t_f = 155.4$ps, and the average delay $t = 90.7$ps.

The last column in Table 5.3 shows the energy dissipation of the charge current based majority gate implementation. Similar to the single MESO inverter case, the energy of the majority gate is the summation of energy from the V_{dd} source at each branch within

the transition time. Long transition times naturally involve large energy dissipation, e.g., the energy for the fall transition of $t_f = 155.4$ps is 188.4aJ, much higher compared to most of the other cases. Notice that there is another case with a delay of $t_f = 154.1$ps but a slightly higher energy of 189.0aJ. These two cases both share the same input states after transition, but the input state for the latter case before transition is composed of two positive η and one negative η, meaning that there are currents flowing between node $n4$, $n5$ and $n6$ at the beginning of the transition. Therefore the averaged current during the transition is slightly higher and incurs a larger energy in the latter case. These values are much higher than the DW based majority gate.

Improving the worst-case delay using STEM

For cases where the difference between the best- and worst-case delays is large, the work in [129] had proposed STEM, a two-phase majority gate scheme for faster operation. We now show how STEM can be applied here to reduce the energy and delay.

In the first phase, STEM uses an initialization pulse to preset the polarization at the output with only one input branch activated. Immediately after this initialization phase ends, a short evaluation pulse is applied to the other two branches. If η for these two branches have opposite signs, then the majority value corresponds to the initial value. In this case, under the short pulse, $V(n7)$ will be close to zero (even under asymmetric voltage levels), and the short pulse will not be applied for long enough to switch the polarization, and the majority function is correctly evaluated. On the other hand, if the two branches in the later phase have the same sign of ηs, they will induce a large voltage magnitude at $n7$, which will cause the polarization at the output to be switched very fast.

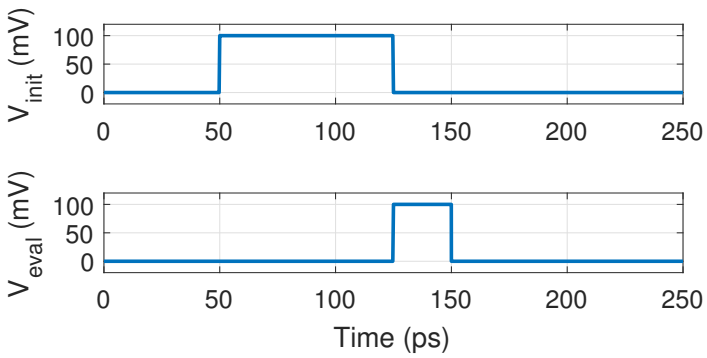
The two-phase STEM switching process is illustrated under an initialization pulse of 75ps and an evaluation pulse of 25ps, as in Fig. 5.11(a). We first consider the scenario where the input switches from η values of $+ + +$ to $- - -$ in Fig. 5.11(b). During the 75ps initialization phase, the output switching to one of the incoming inputs, corresponding to a negative polarization. In the second phase, this polarization is reinforced by two negative inputs, resulting in a net negative polarization at the end of the second pulse. The FE capacitor then returns to its remnant polarization, as seen in the figure.

Next, in Fig. 5.11(c), we show the fall transitions when the input switches from from $+ + +$ to $+ - -$. If the initialization activates a branch of negative η, the first pulse results in an identical waveform as the previous case. The second pulse causes a small increase in the polarization: this is caused by a positive $V(n7)$ due to asymmetry, when one branch with negative η and one branch with positive η are activated at the same time, and is a result of the voltage divider that determines $V(n7)$. As stated earlier, this is influenced by $(R_{ISOC,v} + R_g)$: in the same figure, we show another curve that considers a smaller value of $(R_{ISOC,v} + R_g)$: here, the polarization at the end of the second pulse is more negative. The smaller value demonstrates better switching and takes the polarization to saturation faster and suggests that the widths of the first pulse used in the two-phase scenario can be further reduced.

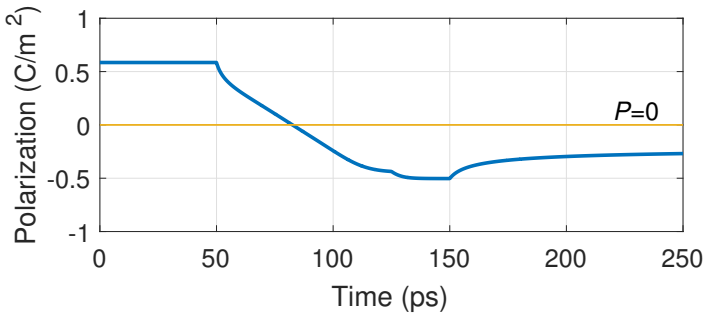
This STEM scheme reduces the worst-case delay from 155.4ps to 100ps, the sum of the two pulse widths, and results in an average energy of 42.5aJ, significantly better than the 188.4aJ associated with the worst case and the 66.2aJ average over all cases in Table 5.3. The energy of charging the gate capacitor per transistor under STEM is also 1.1aJ, the same as that for charging a single MESO inverter. The two-phase scenario may incur slightly more overhead for clock distribution, which is not included in our energy estimate.

5.4 Conclusion

This work has introduced a method to simulate the performance of the MESO device, incorporating the LKh equation for FE capacitor polarization switching into traditional MNA-based circuit simulation to compute the energy/delay under realistic parameters. The work has also presented the potential sneak path issue that may induce inadvertent logic errors in the cascaded MESO inverter chain. Two different majority gate implementations are proposed and analyzed based on the two computation mechanisms in the MESO device. For the charge based majority gate, some input scenarios may be unable to reach the coercive field of the material, which results in switching failure: this is avoided by the STEM-based scheme.



(a)



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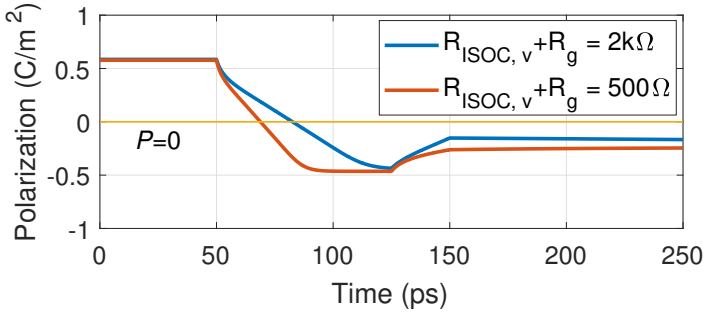

(c)

Figure 5.11: (a) The two-phase STEM pulse. (b) A fall transition with inputs going from 3 positive η to 3 negative η. (c) Two fall transitions with inputs going from 3 positive η to 2 negative η and 1 positive η, for different values of $R_{ISOC,v} + R_g$. The initialization phase activates one of input branches with $\eta < 0$.

Chapter 6

Conclusion

This thesis has developed novel techniques for the design, simulation, and optimization of spintronic logic devices. The emergence of beyond-CMOS technologies has brought up new demands for evaluating device concepts, and therefore new simulation framework and optimization techniques are required. This thesis has reviewed the underlying physics of three types of spintronic logic devices, and has built up the simulation frameworks based on the corresponding governing equations. Optimizations are made through adapting the traditional CMOS techniques as well as incorporating new spin-based effects and the up-to-date material properties.

For ASL circuits, this thesis invoked the notion of device sizing, analogous to the notion of sizing used by traditional CMOS circuits, and applied it to spintronic logic gates based on its performance dependence on the geometric parameters. The trade-off relation between energy and delay is explored under different external constraints. Optimization results on standard circuit benchmarks have proven the effectiveness of the proposed algorithm.

For the CoMET device, novel physics effects, with proper choice of material combinations, are employed to realize fast and energy efficient nucleation. Magnetization coupling between IMA-FM and PMA-FM allows lower nucleation field from ME coupling effect in a composite structure at the input end of the device. Parameters space for the state of the art material properties is explored in order to achieve the best nucleation performance.

For the MESO device, a simulation framework combining the LKh equation governing the dynamic polarization of the FE capacitor is proposed. The thesis discussed potential sneak path issues existing under always-on clocking scenario. Majority gate designs with two different computing mechanisms are proposed by the thesis with the device logic failure in charge current based scenario fixed by applying the STEM scheme.

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Appendix A

Spin transfer through the channel using modified nodal analysis

Detailed explanation of spin transfer through the channel using modified nodal analysis and the analysis for the differences between analytical method and MNA method is shown in this chapter.

1 A numerical model for modeling ASL circuit performance

An alternative to the analytical model mentioned in Chapter 3.1.2 is a numerical method, based on Modified Nodal Analysis (MNA), which enables fast simulations for spintronic circuits and can handle more complicated structures in the spintronic circuits [8, 21, 54, 55]. In this chapter we will briefly review this modeling method and show how to use it to calculate the spin injection efficiency in the non-local spin valve structure. The spin injection efficiency in the ASL inverter can be calculated in a similar way.

For each component in the non-local spin valve structure, a π–network of conductance matrices can be constructed. Every π–network is composed of two kinds of matrices: (a) a series conductance matrix that captures the relation between charge/spin voltage drop and charge/spin current and (b) a shunt conductance matrix that captures the dissipation of spin current. We focus on two types of components for (I) the ferromagnet and (II) the non-magnetic channel and only present the 2x2 matrix formulation

mentioned in [8].

1.1 π–network of conductance matrices for ferro-magnet

For the ferro-magnet, its series and shunt matrices are of the following form:

$$G_F^{se} = \frac{1}{\rho L}\begin{pmatrix} 1 & p \\ p & p^2 + \alpha \operatorname{csch}\left(\frac{L}{\lambda_F}\right) \end{pmatrix}, \tag{A.1}$$

$$G_F^{sh} = \frac{1}{\rho L}\begin{pmatrix} 0 & 0 \\ 0 & \alpha \tanh\left(\frac{L}{2\lambda_F}\right) \end{pmatrix} \tag{A.2}$$

where $\alpha = (1 - p^2)\left(\frac{L}{\lambda_F}\right)$ with p being the polarization factor of the magnet, L being the length along the current propagation direction of the magnet, and λ_F being the spin diffusion length of the magnet. Note that the off–diagonal components in the G_F^{se} indicate a coupling relation between charge and spin voltages/currents.

1.2 π–network of conductance matrices for non-magnetic channel

For the non-magnetic channel, its series and shunt matrices are of the following form:

$$G_N^{se} = \frac{1}{\rho L}\begin{pmatrix} 1 & 0 \\ 0 & \left(\frac{L}{\lambda_N}\right) \operatorname{csch}\left(\frac{L}{\lambda_N}\right) \end{pmatrix}, \tag{A.3}$$

$$G_N^{sh} = \frac{1}{\rho L}\begin{pmatrix} 0 & 0 \\ 0 & \left(\frac{L}{\lambda_N}\right) \tanh\left(\frac{L}{2\lambda_N}\right) \end{pmatrix} \tag{A.4}$$

where L being the length of the non-magnetic channel along the direction that current propagates, and λ_N is the spin diffusion length of the non-magnetic channel. The zeros in the off-diagonal positions of matrix G_N^{se} imply that there is no coupling between charge and spin quantities in the non-magnetic channel.

1.3 Non-local spin valve structure represented by π–network conductance matrices

With the above formulation for each component in the non-local spin valve structure, a representation for this structure can be constructed. The corresponding structure

for the basic ASL gate from Fig. 3.2 is shown in Fig. A.1. The element stamps for all components in the structure, described in the two chapters above, can be combined using a routine approach that creates the MNA equations [130] to solve for the unknowns, i.e., the charge/spin current and voltage in the structure.

Our analysis uses this method to calculate the spin injection efficiency, which is the ratio of the output spin current through magnet F2 versus the input charge current through magnet F1 as in Fig. A.1. This modeling method is also convenient for calculations of quantities in complicated ASL structures as we show in Chapter 3.1.3. This is used to determine the spin torque current that switches the output magnet, and is further used to determine the gate delay.

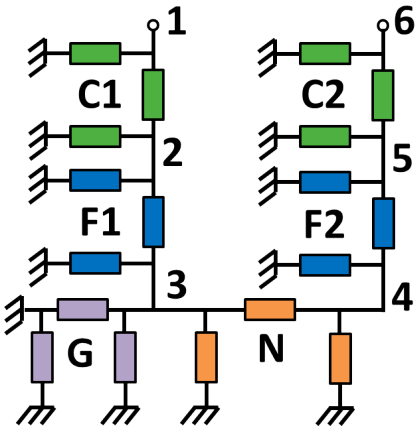


Figure A.1: Inverter structure represented by *pi*–network conductance matrices.

2 Differences between analytical method and MNA method

In the work, we have used two methods for modeling ASL circuits, one based on an analytical model, and another based on a numerical method derived from MNA. Due to its algebraic form, the analytical method is helpful in analyzing the trends and impacts of the material or geometrical parameters to the performance of ASL circuits. However, it is limited to single fanout circuits, and the MNA modeling method is more convenient and flexible in performing numerical analysis of complicated ASL structures with multiple fanouts.

These two methods are fundamentally the same, and both originate from the description of the diffusion behaviors for the two types of spins [21, 59]. However, as pointed out in [59], the analytical derivation makes the assumption that the thickness of the input and output magnets is much larger than the spin diffusion length of the magnet material. This assumption was valid in the experimental case considered in their paper and may not apply here since we are trying to explore a larger design space for the dimensions of the ASL structures where the magnets have very small geometries. Due to the influence of this assumption, a performance metric of interest under these two models may evaluate to inconsistent values under certain cases. In this chapter, we provide a numerical analysis of some discrepancies between these two methods for key performance metrics in an ASL structure.

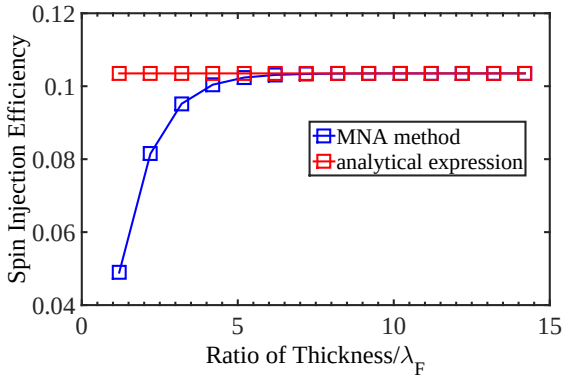


Figure A.2: Spin injection efficiency by two modeling methods under various ratio of magnet thickness versus spin diffusion length of magnet λ_F.

Fig. A.2 shows the difference between the spin injection efficiency by these two modeling methods under various ratio of magnet thickness versus its spin diffusion length λ_F. It is seen that if the magnet thickness is greater than $4\lambda_F$, the discrepancies from two models start to become negligible.

Going beyond the spin injection efficiency to system-level performance, we examine the impact of using the analytical or MNA models for optimizing buffered wires under our approach. Given a total interconnect of fixed length (L_{tot}) between the input and output magnets, we vary the number of buffers in the line, keeping the buffers equally spaced on the line. Under the simulation parameters in Table 3.1 and the same

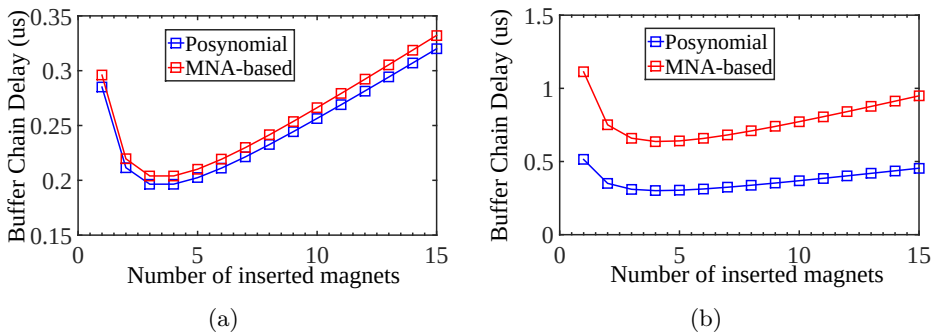


Figure A.3: The buffer chain delay optimization results generated by the analytical and MNA-based modeling methods under a magnet thickness of 20nm with a spin diffusion length of (b) $\lambda_F = 5$nm and (b) $\lambda_F = 15$nm.

experimental setting as in Chapter 3.4.2, we optimize the lengths of inserted magnets individually to achieve the optimal delay for the entire buffered wire under two separate delay models: the analytical modeling method and the MNA-based modeling method.

Fig. A.3 shows the optimal delays of a buffered wire, as the number of buffers is increased, under these two delay models. The magnet thickness is fixed at 20nm, but we perform the analyses under two different values for the spin diffusion length, λ_F. In Fig. A.3(a), $\lambda_F = 5$nm, i.e., the thickness of magnet is $4\lambda_F$, while in Fig. A.3(b), $\lambda_F = 15$nm, i.e., the magnet thickness is $4/3\lambda_F$. In Fig. A.3(a), the percentage improvements of optimal delay by MNA method and posynomial formulation are 63.1% and 64.4% respectively, while in Fig. A.3(b), the precentage improvements are 51.1% and 76.9% respectively. The differences between two methods are 1.3% and 25.8%, which indicates that the MNA method and posynomial formulation are more close to each other when the thickness of magnet is much larger than spin diffusion length of ferromagnet λ_F.

As predicted by Fig. A.2, the curves in Fig. A.3(a) closely track each other and the optimum point is roughly equal, both in terms of the number of magnets and the delay at each point. As expected, the analytical method has an advantage in terms of speed of evaluation. Similarly, as expected, in Figure A.3(b), where the λ_F is larger, the results from two modeling methods are quite different from each other. However, interestingly, their trends for this case remain roughly the same under both models: the minimum delay corresponds to the case where three buffers are chosen. In other words, although

the analytical method does not provide the same prediction on the optimal result as the more accurate MNA method, it has good *fidelity* with the final result. Therefore, it can still be used to analyze the minimal value. Due to its closed form, the analytical form is of great utility in assisting designers to explore the optimal performance of this circuit, and it can enable fast optimization (e.g., using geometric programming).

Appendix B

An expression for t_{sw} from the solution of the LLG equation

In this chapter, we discuss the approach in [21], with some minor modifications, for evaluating t_{sw} based on solving the LLG equation. We are particularly interested this evaluation since it provides a convenient way to evaluate the switching time inexpensively without a full LLG solution. Taking the time-integral of the LLG equation over the switching time,

$$\int_0^{t_{sw}} \frac{d\vec{m}}{dt} dt = -\int_0^{t_{sw}} |\gamma| \vec{m} \times \vec{H}_{eff}\, dt + \int_0^{t_{sw}} \alpha \vec{m} \times \frac{d\vec{m}}{dt} dt - \int_0^{t_{sw}} \frac{1}{qN_s} \vec{m} \times (\vec{m} \times \vec{I}_s) dt \tag{B.1}$$

During switching, we focus on the change along the z axis: in its stable states, corresponding to two logic states, the magnetization aligns along this positive or negative direction. This axis is also called the easy axis since the magnetization is in its lowest energy state along it. For the z component, $\vec{m}_z$, of the normalized magnetization vector,

$$\int_0^{t_{sw}} \frac{d\vec{m}_z}{dt} dt = \int_{\mp 1}^{\pm 1} d\vec{m}_z = \pm 2, \quad \int_0^{t_{sw}} \alpha \left[\vec{m} \times \frac{d\vec{m}}{dt} \right]_z dt = 0 \tag{B.2}$$

If $\vec{H}_{eff}$ only consists of the uniaxial anisotropy field $\vec{H}_k$, then the first term on the RHS of Equation (B.1) goes to zero. However, this is not the case when $\vec{H}_{eff}$ also contains the demagnetizing field $\vec{H}_d$. This perturbation is captured by using a multiplier f_1 on

the LHS of Equation (B.1) to obtain:

$$2f_1 q N_s = \int_0^{t_{sw}} [\vec{m} \times (\vec{m} \times \vec{I_s})]_z dt \tag{B.3}$$

Assuming a constant spin current I_s during switching, and approximating $\vec{m} \times (\vec{m} \times \vec{I_s}) = I_s/f_2$, where f_2 is a constant factor the right hand side evaluates to $I_s t_{sw}/f_2$. Therefore, Equation (B.3) becomes $2f_{sw} q N_s = I_s t_{sw}$, where $f_{sw} = f_1 f_2$ is precharacterized by LLG simulations.

From Equation (3.3), writing the spin current at the end of the channel as $I_s = \eta I_c$, the switching time of the gate is:

$$t_{sw} = 2f_{sw} q N_s/(\eta I_c) \tag{B.4}$$

where I_c is given by Equation (3.1).

Based on this expression, we have evaluated f_{sw} in the work and shown it to be independent of the magnet size over the optimization region.

Appendix C

Hysteresis loop and remnant polarization of the FE capacitor

Hyestersis loop under sinusoidal electric field

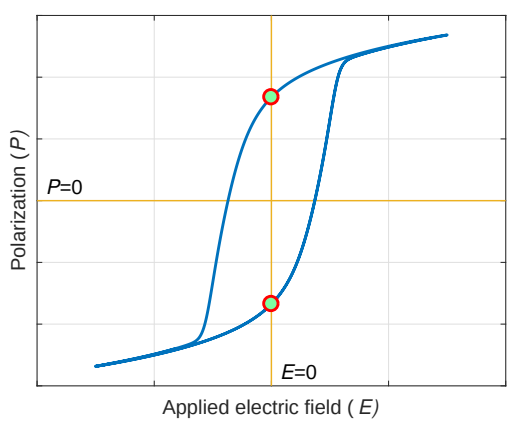


Figure C.1: A hysteresis loop in the $P - E$ plot of the FE capacitor.

Fig. C.1 shows a hysteresis loop for P under a sinusoidal electric field, E. When E is turned off, the polarization settles at one of two remnant values in the plot along the $E = 0$ axis.

Derivation of linear $I - V$ relationship for the FE capacitor based on LKh equation

To develop the $I - V$ relation for the FE capacitor, we begin with the equation $Q = A(\epsilon_0 E + P) = A(\epsilon_0 V/T + P)$. In the derivative form, this yields the following equation:

$$I = \frac{dQ}{dt} = A\left(\frac{\epsilon_0}{T} \cdot \frac{dV}{dt} + \frac{dP}{dt}\right) \tag{C.1}$$

We can see from the above equation that in the steady state, where all d/dt terms are zero, the FE capacitor can be treated as an open circuit; this fact was used in Chapter 5.1.2.

We discretize time using the backward Euler numerical integration formula with a time step size of h. If V_i and P_i are the values of V and P, respectively, in the ith time step, then in the $(i+1)^{\text{th}}$ time step,

$$V = V_i + h \cdot \frac{dV}{dt} \tag{C.2}$$

$$P = P_i + h \cdot \frac{dP}{dt} \tag{C.3}$$

Substituting Eq. (C.2) into Eq. (C.1),

$$\frac{dP}{dt} = \frac{I}{A} - \frac{\epsilon_0}{T}\left(\frac{V - V_i}{h}\right) \tag{C.4}$$

Further, Eq. (C.3) can be combined with Eq. (C.4) to obtain a linear relation between P, V, and I:

$$P = \left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0 V_i}{T}\right] \tag{C.5}$$

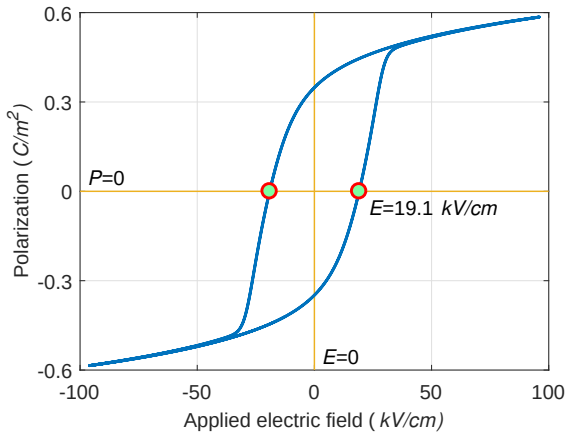
which is the Eq. (5.5) presented in Chapter 5.1.3

Hysteresis loops under various applied fields

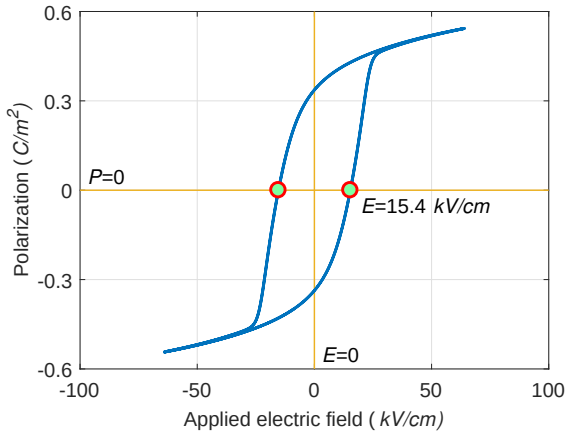
In this chapter, we show the hysteresis loops corresponding to a few switching voltages for the FE capacitor. The charge on the FE capacitor at the saturated voltage can be inferred, and the required coercive field is seen from these plots.

According to Eq. (5.4), we plot the hysteresis loops of P under sinusoidal electric fields E with the different maximum values E_m and mark the corresponding x-intercepts

with electric field axis in Fig. C.2. Formation of these hysteresis loops indicates that sucessful switching is achievable under these voltages. The concept that the shape of the hysteresis loop depends on E has been previously observed in [126]. The corresponding polarization charge under 48mV, and 32mV are 58.5aC, and 54.3aC with an area $A = 100\text{nm}^2$.



(a)



(b)

Figure C.2: Hysteresis loop under (a) maximum voltage of 48mV (E_m = 96kV/cm) with corresponding x-intercept E = 19.1kV/cm; (b) maximum voltage of 32mV (E_m = 64kV/cm) with corresponding x-intercept E = 15.4kV/cm. The thickness of the ferroelectric material in each case is 5nm.

Appendix D

Rise and fall transition for a single MESO inverter

To measure the rise transition time, we set the electric polarization to the negative saturation value before applied the clocking pulse to the transistor. Then we use a pulse of 100ps long enough to make sure the complete the switching of the electric polarization P. When the pulse is applied, the transition of electric polarization P occurs. We measure the rise time of 28.9ps from the point of its 10% saturation value to its 90% point as illustrated in Fig. D.1. Similarly, the fall transition time is 46.8ps as seen in Fig. D.3. The dynamic responses of voltage and current associated with rise and fall transitions are also shown in Fig. D.2 and Fig. D.4.

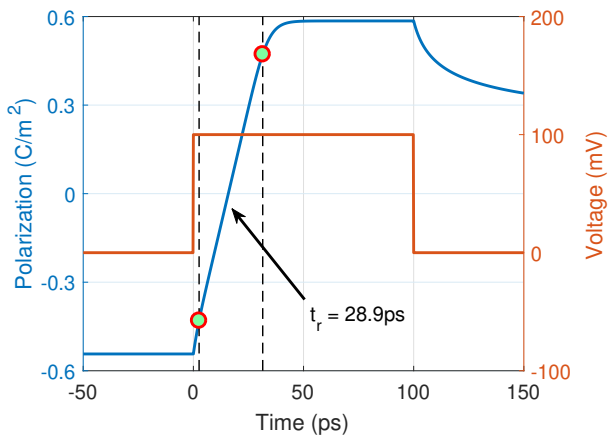


Figure D.1: Simulated rise transition in a MESO inverter: polarization and voltage pulse.

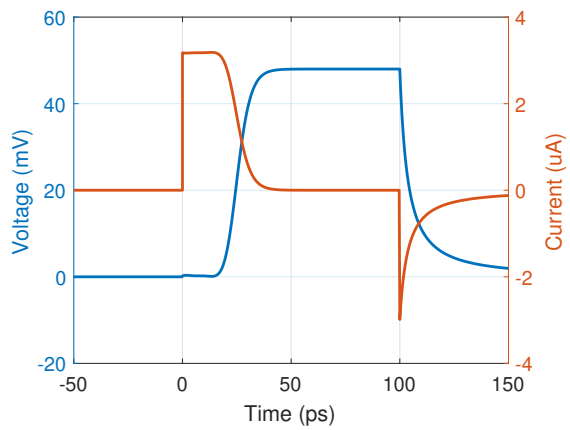


Figure D.2: Simulated rise transition in a MESO inverter: voltage and current versus time.

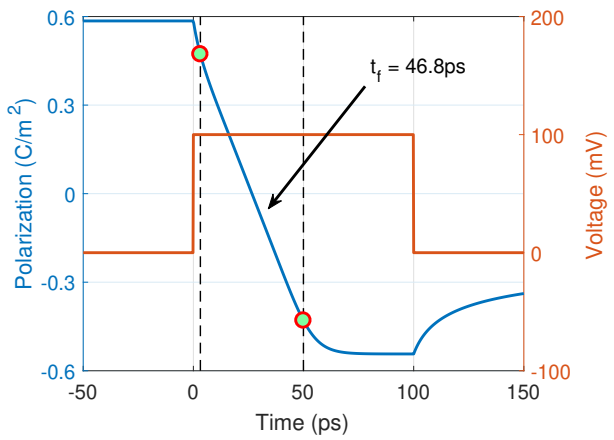


Figure D.3: Simulated fall transition in a MESO inverter: polarization and voltage pulse.

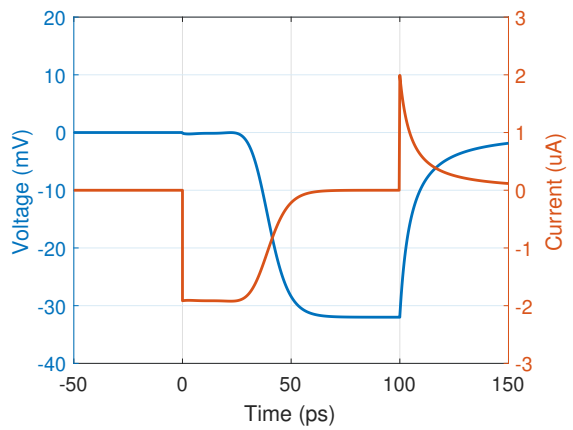


Figure D.4: Simulated fall transition in a MESO inverter: voltage and current versus time.