Design of an On-chip Thermal Sensor using Leakage Current of a Transistor

A THESIS
SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL
OF THE UNIVERSITY OF MINNESOTA
BY

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IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
MASTER OF SCIENCE

Chris H. Kim, Adviser

January 2010
Acknowledgements

I would like to thank Prof. Kim for his guidance in this work. The regular meetings, discussions and advice have proved valuable to the completion of this design. His patience and encouragement helped a lot as he advised me on how research is done. His stress on good presentation and documentation quality also made me realize that it is important to make others understand and appreciate the work I have done. This thesis proved a valuable learning experience for me.

I would also like to thank my colleagues in the VLSI research lab at the University of Minnesota, Hussain Dalal, Kichul Chun, Tae-Hyoung Kim, John Keane, Wei Zhang, Dong Jiao and Pulkit Jain who have helped to perform various experiments, simulations and provided insights which helped to improve the design.
Abstract

Our efforts are to design a self-contained, supply-insensitive, completely on-chip thermal sensor based on exponential temperature dependency of leakage current of a PMOS transistor in sub 90-nm technologies. Simulation results show an error of 3.9°C for a temperature range of 25°C to 110°C with +/-10% supply variation. The circuit was fabricated in 65 nm CMOS technology with a nominal supply voltage of 1.2V. Area of the sensor is 0.0026 mm² and power consumption 351.55 μW at 25°C. The circuit uses no temperature insensitive on-chip or external references.
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1. Introduction

Market trends today show devices becoming smaller, mobile, and more battery efficient. This was made possible by the shrinking die sizes and high frequencies achievable due to what we all know as scaling of the transistor. But scaling also means increased power densities that lead to unusual temperature gradients across the chip. Fig.1 below shows power density per unit area of Intel’s microprocessors in the past four decades. In certain areas of the chip high switching activity combined with fast speeds of processing can generate a localized high temperature area on the chip called a “hotspot”. Moreover, current power supply delivery networks, clock gating schemes and dynamic nature of circuits may cause these hotspots to change dynamically. This proves a significant threat to reliability and robustness of the product as well as increases the

Fig. 1. Power densities of Intel microprocessors (Source: Intel)
power consumption of the chip. Hence in addition to external cooling and heat sinks provided by the chip packaging, today there is a need for on-chip thermal monitoring and management of these localized hotspots through use of adaptive systems.

An example of a thermal management system is the one used by J. Clabes et al. in the implementation of POWER5 Microprocessor [1] as shown in fig. 2. The design includes

![Diagram of thermal control logic and sample thermal response of Power5 microcontroller](image)

**Fig. 2.** Thermal control logic and sample thermal response of Power5 microcontroller

24 temperature-monitoring sensors implemented at various different locations on a single chip. All sensors feed information to core control logic which provides a temperature-reducing feedback to overheated circuits. It manipulates the circuit operations performed by parts of the chip; for example it reduces the number of execution operations and
increases the number of stall, fetch or completion operations in the overheated part of the circuit and on the other hand increases the number of execution of computational operations in cooler part of the chip.

Another thermal management system is that of the SX-9 supercomputer designed by E. Saneyoshi et al. in [2]. An off-chip microcontroller collects temperature distribution through readings of multiple small thermal sensors placed on-chip and in turn controls the CPU throttling and the chip cooling fans. A block diagram is shown in fig. 3.

![Thermal management system of SX-9 supercomputer](image)

The first step towards designing any adaptive on-chip thermal management system is an accurate on-chip temperature sensor. A completely on-chip thermal sensor has many specific requirements which are discussed in the next section.
2. **Requirements of an on-chip temperature sensor**

For temperature measurements, a tolerance of 1-2°C is acceptable as an error margin, but accuracy should be maintained while sustaining variations in process and supply voltage parameters for a wide temperature range of at least 0 °C to 120°C. Process variations are static variations. Once the chip is fabricated, within die and die-to-die variations remain constant. These can be taken care of during calibration. But supply voltage variations being dynamic in nature are a major concern. The sensor must be immune to supply variations in a range of at least +/-10% of the nominal supply voltage.

Further, the sensor should occupy low area, as this will allow multiple sensors to be placed on-chip for localized measurements. To achieve this it is advisable to avoid any large blocks, complicated analog circuitry or precise references in the design.

Low power consumption (less than 1mW) is desirable as it reduces errors due to self-heating and conserves battery power in low-power portable devices.

A digital output which can be easily calibrated for direct measurements on-chip is preferable too. Digital circuits are also less susceptible to noise and easier to implement than analog circuits.

It is important that the sensor design is compatible with standard CMOS processes so that it can be implemented at no extra cost.

Most importantly, the sensor must be self-contained and must not make use of any external current or voltage references which makes it easy to use.

A sensor that fulfils all of these requirements will be reliable and easy to productize.
3. CMOS temperature effects

Two opposite temperature effects are seen in a CMOS transistor [3]. The two parameters responsible for this are mobility of electrons (μ) and threshold voltage of the transistor (V_T). The mobility of electrons decreases with temperature and a certain temperature it is expressed as \(\mu(T) = \mu(T_0) \cdot \left(\frac{T_0}{T}\right)^{K_1} = \mu_0 \cdot \left(\frac{T_0}{T}\right)^{K_1}\) where K1 is a constant in the range of 1.5 ~ 2. The mobility effect tries to reduce transistor current as temperature increases. The threshold voltage of a transistor decreases with temperature and is expressed at a certain temperature T as \(V_T(T) = V_T(T_0) - K_2(T - T_0)\) where K2 is a constant in the range of 0.5 mV/K ~ 4 mV/K. The decrease in V_T tends to increase the transistor current as temperature increases. Based on simulations of a ring oscillator in 130 nm and 65 nm CMOS technologies, mobility effect was found to dominate the V_T temperature effect as delay increases with temperature as shown in figs. 4 (a) and 4 (b).

Fig. 4. Ring oscillator time period vs. temperature in (a) 130 nm (b) 65 nm
4. Literature Survey

Since the early 1990’s different types of thermal sensors have been implemented completely or partially on-chip for the purpose of monitoring die temperature. Diode based sensors were the first to be implemented. Their basic principle of operation is stated in figs. 5 (a), (b) and (c). Two different currents are passed through an on-chip thermal diode and the $V_{BE}$ is measured in each case. $\Delta V_{BE} = \left(\frac{kT}{q}\right) \ln(N)$ where N is the ratio of the two currents. An ADC is required to convert the voltage into digital readout proportional to temperature. C. Poirier et al. have used conventional diode-based sensors for temperature control in 90nm Itanium family processor [4]. They use pFET current

![Diagram](image1)

![Diagram](image2)

![Diagram](image3)

Fig. 5. (a) Structure of substrate PNP bipolar transistor [12] (b) Circuit operation principle [12] (c) Bandgap reference voltage [5]
source to drive the thermal diode and a precision temperature insensitive bandgap reference for calibration. M. Pertijis et al. used Substrate PNP Bipolar Transistors for implementing thermal diodes on-chip instead of conventional diodes in [5]. They used a ΣΔ ADC to obtain a digital readout. To achieve high accuracy they incorporate techniques such as dynamic element matching for coping with errors due to mismatches in current sources, corrections for nonlinearity of $V_{BE}$ dependency on temperature, etc. Bandgap references which require 3V or higher supply voltages are inconvenient to use on-chip in sub-90nm technologies using supply voltages 1.2V or lower. Also, diode sensors require very stable current references to make them immune to supply variations which are either implemented on-chip at the expense of increased area or provided externally. In addition there still exist issues of non-linearity, parasitic resistances, etc. studied in [6] [7] which require complicated analog circuitry to resolve thus increasing the area of the sensor and reducing the ease of implementation and use.

P. Chen et al. proposed a time-to-digital-converter-based sensor for portable applications in [8] which did not use any voltage to current ADC or bandgap reference. Fig. 6 (a) shows the block schematic of the circuit and fig. 6 (b) shows the basic principle of operation. Output of a simple chain of inverters in delay line 1 is gated with a temperature insensitive pulse from delay line 2 to obtain an output pulse width proportional to temperature. Delay line 2 uses a delay cell to reduce thermal sensitivity of its inverters as shown in fig. 6 (c).

However, in this sensor there is an offset as shown in fig. 6 (b) which cannot be removed easily unless very long inverter chains are used in delay lines 1 and 2 which
tends to increase the area of the sensor. Also, the delay cell schematic in fig. 6 (c) shows 3 diode connected transistors in saturation connected between the supply rails. This is difficult to implement in sub-90nm technologies with supply voltages of ~1.2V because of the voltage headroom problem.

C.K. Kim et al. [9] had proposed a temperature sensor using two current-starved ring oscillators - one with a temperature sensitive bias while the other with a temperature
insensitive bias. Fig. 7 (a) shows the structure of the sensor. Figs. 7 (b) and 7 (c) show the schematics of the two bias current generator circuits used. The disadvantages of this sensor include use of resistor not preferred in CMOS circuits, requirement of precise biasing of transistors for a thermally insensitive bias current generator and susceptibility to process and supply voltage variations.
K. Kim et al. in [10] also proposed a ring oscillator based sensor with frequency-to-digital conversion and low power consumption of ~ 400μW. They use two current starved delay cell ring oscillators – a temperature sensitive oscillator (TSO) and the other insensitive oscillator (TIO). The TIO is biased with a temperature insensitive current bias which is as shown in fig. 8 (b). Problem with this scheme that a precise transistor biasing

![Conventional Design](image1.png) ![Proposed Design](image2.png)

\[ V_{ov,M7} + V_{ov,M8} + V_{ov,M9} \geq V_{DD} \]

Cutoff

\[ V_{DD} - V_{ov,M3} - V_{ov,M6} \geq V_{DS,M2} \]
\[ V_{DS,M2} \geq V_{gs,M2} - V_{th,M2} \]
\[ V_{gs,M2} \geq V_{th,M1,2} \]

Saturation

Fig. 8. Temperature insensitive bias circuit by K. Kim et al. [10]

is required to generate a truly temperature independent current which is very difficult to maintain given process and supply voltage variations.

E. Saneyoshi et al. in [2] designed an off-current based sensor for thermal management on the SX-9 supercomputer. Schematic is shown in fig. 9 (a). PMOS device leakage current is used to charge a capacitor. An inverter acts as time-to-digital converter. The advantage they claim is, leakage current has logarithmic temperature dependency which makes the circuit insensitive to supply voltage variations and is shown in fig. 9 (b).
Fig. 9. (a) PMOS off-current based sensor schematic (b) Influence of Vdd deviation [2]

This scheme does look attractive and easy to implement in sub-90 nm technologies where weak inversion operation is more feasible. Also, due to logarithmic dependency the design will have a high resolution. However, the circuit’s insensitivity to supply
voltage variations needs to be investigated closely considering effects like DIBL which are higher in these technology nodes.

Thus none of the above designs satisfy all the requirements for a small, easy to implement and use, and productizable on-chip thermal sensor. Most designs have no provision for tackling errors due to supply voltage variations. This problem cannot be ignored due to its dynamic nature and is likeliness to affect any on-chip thermal sensor. Therefore our plan is to work towards a new sensor design with emphasis on this particular issue.

In this work we investigate and improvise upon two different ideas to design thermal sensors on-chip – first using the beat frequency of two ring oscillators with different thermal sensitivities; and the second using off-current leakage of a transistor with logarithmic thermal dependence to measure temperature.

This thesis is further organized as follows: chapter 5 describes the first design approach, chapter 6 details the second design approach including the proposed thermal sensor design, chapter 7 gives the layout simulation results of the proposed circuit and chapter 8 concludes the thesis.
5. First approach: Beat frequency of two ring oscillators

In this design we used two ring oscillators of two different structures such that their frequencies show different sensitivities to temperature. The motivation for pursuing this design was that a temperature independent reference is not required. This is an important advantage since designing a temperature independent reference is non-trivial. The difference or beat frequency of the two ring oscillators gives us a metric proportional to the absolute temperature. It can be measured using the silicon odometer [11] designed by T. H. Kim et al.

5.1 Structure of reference ring oscillator

One of the two ring oscillators is a normal ring oscillator (RO) with simple inverter stages as shown in fig. 10 (a). We will call this RO the reference RO.

![Diagram of reference RO](image)

Fig. 10. (a) One stage of the reference RO (b) Structure of the reference RO

The delay of the reference RO is proportional to temperature as seen from the following:

\[
\text{Delay}_{\text{ref}} \propto C_L \cdot \frac{V_{dd}}{I_{\text{dsat}}}
\]

\[
\text{Delay}_{\text{ref}} = n_{\text{ref}} \cdot C_L \cdot \frac{V_{dd}}{\left(\mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - V_t) V_{\text{dsat}}\right)} \quad \text{ignoring} \quad \frac{V_{\text{dsat}}^2}{2}
\]
\[ \text{Delay}_{\text{ref}} = \frac{C_1}{(V_{dd} - V_t)} \cdot \left( \frac{T}{T_0} \right)^{K_1} \text{ where } C_1 \text{ is constant} \]

5.2 Structure of modified ring oscillator

The structure of the second RO was modified in order to change its sensitivity to temperature. We will call this the modified RO. In modified RO, stages used consisted of stacked inverters instead of a normal 2-transistor inverter. Figs. 11 (a) and (b) show the

\[ \begin{align*} &\text{VDD} \\
&\text{IN} \quad \text{OUT} \\
&\text{device 2} \\
&V_{d1} \quad \text{device 1} \\
\end{align*} \]

\[ \begin{align*} &\text{VDD} \\
&\text{IN} \quad \text{OUT} \\
\end{align*} \]

(a) (b)

Fig. 11. Modified ring oscillator stages (a) 2-stacked inverter (b) 4-stacked inverter

2-stacked and 4-stacked inverter stages respectively. Consider the 2-stacked RO stage for quantitative analysis. In the pull-down stack, device 1 is in linear region and device 2 in saturation region.
The delay of a 2-stacked stage is given by the equation:

\[ I_{d1} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - V_t) \cdot V_{d1} \]
\[ I_{d2} = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - V_t - V_{d1}) \cdot V_{dsat} \]

\[ \text{Delay}_{\text{mod}} = n_{\text{stk}} \cdot C_L \cdot \frac{V_{dd}}{\left( \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{dd} - V_t - V_{d1}) V_{dsat} \right)} \]

ignoring \( \frac{V_{dsat}^2}{2} \)

\[ \therefore \text{Delay}_{\text{stk}} = \frac{C_2}{(V_{dd} - V_t - V_{d1})} \left( \frac{T}{T_0} \right)^{K_1} \text{ where } C_2 \text{ is constant} \]

Here \( V_{d1} \) is the voltage at the drain of device 1 as shown in fig. 10(b). Next we show that \( V_{d1} \) actually increases with temperature. By equating the currents of the two transistors in the stack we can obtain the value of \( V_{d1} \). Further using Taylor series expansion we get:

\[ V_{d1} = \frac{V_{dsat}}{\left( 1 + \left( \frac{V_{dsat}}{V_{dd} - V_t} \right) \right)} = V_{dsat} \left( 1 - \left( \frac{V_{dsat}}{V_{dd} - V_t} \right) \right) \]

As \( V_t \) decreases with temperature, from the above expression we can conclude that \( V_{d1} \) increases with temperature. Thus it further opposes the \( V_t \) effect proving that 2-stacked RO stage has a different thermal sensitivity than a normal RO stage.

5.3 Assumptions and simulation results

Since the two RO structures have different sensitivities to temperature, difference in their frequencies is proportional to temperature. The beat frequency can be measured using a silicon odometer, which uses reference RO frequency for frequency division to give a digital output. If \( f_{\text{ref}} = V_{dd} \cdot \frac{C_L}{l_{\text{ref}}} \) and \( f_{\text{beat}} = V_{dd} \cdot \frac{C_L}{l_{\text{beat}}} \), then the ratio \( \frac{f_{\text{beat}}}{f_{\text{ref}}} = \)
\( \frac{I_{\text{ref}}}{I_{\text{beat}}} \) should be independent of supply voltage variations. Thus, assumption for this design is that supply voltage variations will be cancelled out. We carried out simulations in UMC 130 nm technology kit to verify our assumption. Fig. 12 shows a graph of this ratio versus temperature. Simulation results show that initial ratio varies a lot with supply voltage. If Vdd dependency of the ratio was negligible then all curves would have the same starting point coinciding completely. But the curves do not coincide. This discrepancy can only be explained as a result of second order effects such as DIBL. Error seen from the graph is more than 10ºC and hence not in acceptable range of 2ºC ~ 3ºC.

![Graph of \( \frac{f_{\text{beat}}}{f_{\text{ref}}} \) vs. temperature at nominal and +/-10% Vdd](image)

Fig. 12. Graph of \( \frac{f_{\text{beat}}}{f_{\text{ref}}} \) vs. temperature at nominal and +/-10% Vdd

To summarize, the sensor design based on two RO beat frequency approach has the following advantages. A temperature insensitive reference, difficult to implement on-chip, is not needed. The use of silicon odometer gives a very good resolution. But due to high resolution, supply voltage variation errors, caused by second order effects such as DIBL, are magnified beyond our acceptable range rendering the design impracticable.
Since process variation is a one-time effect, it can be calibrated out. However the supply voltage variation is a more important problem. We are trying to find some way of reducing the supply sensitivity of the circuit. So we shifted our focus to another sensor design based on leakage current of an off PMOS transistor which has logarithmic sensitivity to temperature but lesser sensitivity to supply variations.
6. Second approach: Using the off-leakage current of a transistor

The SX-9 supercomputer sensor design by E. Saneyoshi [2] et al. already described in section 2: literature survey claims insensitivity to supply voltage deviations because of logarithmic temperature dependency of leakage current. But a closer look at the sensor blocks reveals that the supply dependencies of the PMOS off-current, the inverter used as a comparator and the microprocessor clock used compensate each other to yield a final output obtained insensitive to supply variations. A detailed analysis follows.

6.1 Study of supply variation effects in sensor design of SX-9 supercomputer

From figure 9 (a) the main blocks of the sensor designed by E. Saneyoshi et al. that may exhibit supply voltage dependency are: i) PMOS off-devices charging the capacitor, ii) the inverter used as a comparator and iii) clock used by the counter which gives a final digital count proportional to temperature. Simulations were carried out in 65 nm CMOS technology. Fig. 13 (a) shows the schematic of PMOS devices charging a capacitor. While operating in the weak inversion the PMOS device widths had to be kept sufficiently large so that leakage current is enough to charge the capacitor. Reset signal is

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Fig. 13. (a) Schematic of temperature sensing circuitry with off PMOS devices charging a capacitor and reset switch (b) Graph of Vc against +/-10% supply variation at 25°C
used to drain off charge on the capacitor before temperature measurement. When reset is 
high, output of the inverter is high. When reset signal is low, PMOS devices are turned 
off and their leakage current starts charging the capacitor. The off-current of these PMOS 
devices is modeled by the equation $I_{\text{off}} = A \cdot e^{B \cdot T}$ where $T$ is the absolute temperature. As 
the capacitor voltage rises it trips the inverter when it reaches the threshold of the 
inverter. Since leakage current rises exponentially with temperature, the time to trip the 
inverter too decreases exponentially with temperature. The time taken by the inverter to 
trip is converted into digital output by a counter and reference clock. The count output 
can be written as $\text{count} = t_{\text{trip}} \cdot f_{\text{clk}}$ where $t_{\text{trip}}$ is the time to trip the inverter and $f_{\text{clk}}$ is 
the frequency of reference clock. The digital reading is calibrated to read the temperature.

Fig. 13 (b) shows the voltage up to which capacitor charges ($V_c$) in a fixed time 
period when the supply voltage is varied by +/-10% from nominal. The capacitor charges 
to a higher voltage in the same time duration at a higher supply voltage. This means that 
capacitor takes less time to charge to a particular voltage level at higher supply voltages. 
This is because leakage current of a transistor is proportional to supply voltage as shown 
in fig. 14 (a). This tends to decrease the time-to-trip the inverter ($t_{\text{trip}}$) with increase in 
supply voltage. The leakage current increases by 33.5% with +/-10% change from the 
nominal supply voltage.

Next consider the tripping threshold voltage i.e. trip-point ($V_{\text{trip}}$) of the inverter. Fig. 
14 (b) shows the trip-point the inverter simulated at different temperatures when the 
supply voltage is varied +/-10% from the nominal. Inverter trip-point is proportional to 
supply voltage, in fact the proportionality factor is the sizing ratio of the inverter. Hence
we have $V_{\text{trip}} \propto \beta \cdot V_{\text{dd}}$ where $\beta = \frac{W_p}{W_n}$. In this design the inverter is used as a comparator which compares the capacitor voltage $V_c$ to the switching threshold or trip-point of the inverter. The inverter output trips when $V_c$ exceeds the trip-point $V_{\text{trip}}$. Thus the inverter here forms a very simple comparator block. This tends to increase the time-to-trip the inverter ($t_{\text{trip}}$) with increase in supply voltage.
The graph 15 (a) shows the significant compensation obtained by having a supply dependent trip-point of the inverter.

Last we simulated the frequency of a ring oscillator clock for +/-10% change in nominal supply voltage and the results are shown in fig. 15(b). In the paper, E. Saneyoshi

![Graph 15 (a) Trip-time variation](image1)

![Graph 15 (b) Clock frequency variation](image2)

Fig. 15. (a) Trip-time variation (b) Clock frequency variation with +/-10% nominal supply voltage variation at 25°C
et al. used a microprocessor clock which is provided externally. But as our aim is to design a self-contained thermal sensor without any external references, we decided to simulate a ring oscillator based clock which can easily be generated on-chip. The graph shows that clock frequency tends to increase with increase in supply voltage.

To summarize, we see that outputs of all the three different blocks show variations with supply voltage deviation. The capacitor charges faster with increase in supply voltage, this tends to decrease the trip-time of the inverter, hence decreases the final count. On the other hand, inverter trip-point is higher at higher supply voltages, which tends to increase the trip-time of the inverter, hence increases the count. Thirdly, clock frequency also increases with temperature; hence increases the count with temperature. Thus supply variation effects of the off-current sensor are opposed by the supply variation effects of the inverter as well as a reference ring oscillator clock. As technology nodes are scaled further down, due to increase in DIBL, these clock and inverter supply variation effects may overcompensate for the sensor’s supply variation effects.

### 6.2 Modeling supply variation effects for design purposes

The effects of supply variation in previous design need to be modeled into a metric that can be used while improvising upon the previous sensor design. We know that the final count of the sensor is given by the equation:

\[ \text{count} = t_{\text{trip}} \times f_{\text{clk}} \]

where \( t_{\text{trip}} \) is the time-to-trip the inverter when the capacitor voltage \( V_c \) reaches the trip-point of the inverter and \( f_{\text{clk}} \) is the clock frequency given to the counter.

From the discussion in the previous section, we know that the tripping time of the
inverter decreases with increase in supply voltage. Suppose \( t_0 \) is the time-to-trip the inverter at nominal supply voltage. If the supply voltage rises and trip-time decreases by \( \Delta t_0 \) then the time-to-trip the inverter can be written as:

\[
\text{t}_{\text{trip}} = t_0 - \Delta t_0
\]

Also, we know that clock frequency increases with rise in supply voltage. Say \( f_0 \) is the clock frequency at nominal supply voltage. If the supply voltage rises and clock frequency increases by \( \Delta f_0 \), then the clock frequency of ring-oscillator based clock can be written as:

\[
f_{\text{cik}} = f_0 + \Delta f_0
\]

Substituting the first equation with the subsequent two equations, we have the following expressions for the final count:

\[
\text{count} = (t_0 - \Delta t_0). (f_0 + \Delta f_0)
\]

\[
\therefore \text{count} = t_0 \cdot f_0 + t_0 \cdot \Delta f_0 - \Delta t_0 \cdot f_0 - \Delta t_0 \cdot \Delta f_0
\]

Ignoring the second order term and rewriting the equation:

\[
\text{count} = t_0 \cdot f_0 \left( 1 - \frac{\Delta t_0}{t_0} + \frac{\Delta f_0}{f_0} \right)
\]

Our aim is that count should always remain equal to \( t_0 \cdot f_0 \) irrespective of the deviations in supply voltage. In order to achieve this, the sum of rest of the terms in the count equation should be zero. Since \( t_0, f_0 \) is constant the following sum should be zero.

\[
\text{sum} = \frac{\Delta t_0}{t_0} - \frac{\Delta f_0}{f_0} = 0
\]

We use this sum as our metric for design purposes and try to minimize it so to make the sensor insensitive to supply voltage variation.
6.3 Design decisions and proposed sensor design

We aim at designing a self-contained thermal sensor with a small form factor which is also easy to implement and use. A sensor based on the off-current of a transistor consists of the following components: i) temperature sensing circuitry using device leakage currents to charge a capacitor ii) comparator block that compares the capacitor voltage to a reference voltage iii) reference voltage generating circuitry for the comparator iv) a counter which is a time-to-digital converter v) reference clock generator which provides the counting clock to the counter. Fig. 16 below shows a basic block diagram of the sensor.

![Diagram of proposed off-current based sensor](image)

Fig. 16. Block diagram of proposed off-current based sensor

6.3.1 Temperature sensing circuitry

The actual temperature sensing circuitry consists of the PMOS devices operated in weak inversion region, the reset switch and capacitor. The schematic is shown in fig. 17. (a). Width of the PMOS devices must be large in order to increase the leakage current for
fast charging of the capacitor. For the same purpose of increasing the leakage current, multiple off PMOS transistors are connected in parallel.

Care has to be taken to ensure that the leakage current of the PMOS devices is not discharged though the leakage path of the reset switch. Long channel devices and stacking was therefore used in the reset switch for the purpose of leakage reduction.

For the capacitor design the options were either using a gatecap or using metal plate capacitors. Metal plate capacitors have the advantage of better characteristics. But they have a very large area, about 50X or 100X times the area of a gatecap as we found from our experiments. Since our application requires small area, we chose a gatecap.

6.3.2 Comparator design

The sensor design of SX-9 super computer [2] uses an inverter as a comparator. The supply sensitivity of the trip-point of the inverter opposes that of the leakage current. Thus there is an inherent compensation provided in the inverter comparator scheme. However, the total absence of any external knob hampers our ability to study and utilize
the compensation effect to its full potential. Hence in our proposed sensor design we use a simple differential amplifier as comparator. The schematic is shown in fig. 18. Output

![Comparator Schematic](image)

Fig. 18. Schematic of the comparator

of the diffamp is converted to single-ended output. Mismatches in the device pairs N1, N2 and P1, P2 are an important concern in diffamp implementation. To alleviate this concern longer channel lengths were used for the device pairs in the diffamp.

For quantitative analysis, we plotted the supply variations of time-to-trip the comparator when both an inverter and when a diffamp comparator is used. This information is showed in figs. 19 (a) and 19 (b) respectively. We can infer from the figures that the trip-time shows more variation with supply voltage when the new comparator is used. This means that there is more variation to compensate for the supply variation of the clock frequency when the new comparator is used. Further, we used the information from fig. 15 about the supply variation of clock frequency of a normal ring oscillator clock to plot the sum plots for each case.
From the sum plots as shown in fig. 20 we can see that the sum is closer to zero when using a diffamp comparator. The new comparator design gives us a more supply insensitive final count and is favorable. Moreover, we can vary the supply sensitivity of the reference through specific design as explained in the next section.
6.3.3 Reference generator design

The main advantage of our design is that it does not require a reference voltage that is insensitive supply variations. On the other hand it requires a reference with variable supply variation characteristics that can be controlled with an external knob.

The reference generator uses a simple diode connected NMOS device driven by a PMOS current source as shown in the fig. 21. Long channel lengths are used to minimize channel length modulation in both devices. Reference voltage $V_{\text{ref}}$ given by the equation:

$$V_{\text{ref}} = \left(\frac{\beta_p}{\beta_n}\right).V_{\text{dd}}$$

where $\beta_p$ and $\beta_n$ are the sizing ratios of the two transistors. From the above equation it is evident that the supply dependence of reference voltage can be varied easily by changing the ratio $\frac{\beta_p}{\beta_n}$. This can be done by simply changing the width of the diode connected NMOS. For implementing a variable width transistor, multiple diode-connected NMOS transistors were connected in parallel while providing switches to connect and disconnect them. When the width of the NMOS is increased $V_{\text{ref}}$ decreases and so does its sensitivity to supply and vice versa.
6.3.4 Clock generator

In order to make our design self-contained we designed a clock generator on-chip. This is a major advantage as it resolves any dependency on the system clock. Also, it makes it possible to vary clock frequency as desired which is very important. At different process corners, time-to-charge the capacitor to trip-point of the comparator varies from a less than a microsecond to tens of microseconds. Same clock cannot be used for counting in all cases using the same 12-bit counter; this will badly affect the resolution at fast corners. So we designed a variable frequency clock generator that allows us to vary the clock frequency as desired to obtain a good resolution across all corners.

The clock is generated by a simple ring oscillator circuit. Initially we designed the ring oscillator stages as inverters. But in case of slow process corners the capacitor may need even tens microseconds to charge and discharge hence requiring a very low frequency clock. Generating a low frequency clock makes the length of the ring oscillator too long creating a big area overhead.

Hence we designed each stage of the ring oscillator as a two stacked inverter as was shown earlier in fig. 11(a). The stacking effect of sub-90 nm technologies increases the delay of each stage making it possible to achieve a slow clocking frequencies and large time periods in as few as 20 ~ 25 stages. Switches are provided to reduce or increase the number of stages of the ring oscillator as required depending upon the process corner. Minimum number of stages will be used for fast process corners while maximum will be used for the slow corners to prevent the counter from overflowing. Thus, we can reach the desired resolution in spite of any process variations.
6.4 Calibration

Leakage current has an exponential dependency on temperature. As count versus temperature relationship log-linear, count can be expressed as $\text{count} = A \cdot e^{-B \cdot T}$, where $T$ is absolute temperature. In order to calibrate a sensor, two-point calibration is sufficient. But, it has many disadvantages - requires facility to heat the chip to a known temperature, increases calibration time, makes the sensor difficult to use. Most importantly, temperature characteristic of leakage is not truly log-linear, but has non-linearities which increase calibration error near the mid-point of the temperature range.

So we decided to use one-point calibration. For one-point calibration, parameter B is extracted from simulation results at 25ºC for different count values as shown in fig. 22. The count of sensor at room temperature is available. Value of B parameter for that count

![Fig. 22. B parameter values extracted from simulations at 25ºC for various different count values which represent different process corners](image)

can be obtained from above graph. Value of parameter A can then be easily calculated using B parameter value and the count at known room temperature.
7. Simulation results

The proposed sensor design was implemented in 65 nm CMOS technology and is currently being fabricated. Layout simulations were performed on the circuit for typical process corner and the plot of count for different temperature at nominal and +/-10% supply variation is shown in fig. 23. The calibration curve is shown in the graph too.

![Graph of count against temperature for nominal supply and +/-10% variation](image)

Fig. 23. Graph of count against temperature for nominal supply and +/-10% variation

Errors were calculated from the graph for a temperature range of 25 °C to 110 °C. The maximum error due to calibration was calculated as 3.9°C. The maximum error due to +/-10% variation in supply was calculated as 1.5°C.

The power consumption of the circuit was calculated from the total current sourced by the power supply for various blocks. Including sensor circuitry, clock generator and scan-in chain, the total power consumption of the circuit was calculated to be 351.55 µW.

The dimensions of the sensor including the three blocks - sensor circuitry, clock generator and scan-in chain are 105.85 µm × 25.06 µm i.e. a total area of 0.002653 mm².
8. Conclusion

In this thesis we have proposed a design for a leakage current based temperature sensor. Previous designs we studied did not consider the problem of supply voltage variation that affects on-chip thermal sensors. Our effort has been to consider the effect of process as well as supply voltage variations on our circuit and to make it as immune as possible to these variations.

The main advantages of our design are small area of 0.0027 mm$^2$, no need for a temperature insensitive reference, self-contained clock which can be operated at variable frequency, reference voltage with variable supply sensitivity, robustness due to provision of external knobs for testing, programmable resolution. The circuit is currently under fabrication. It will be tested after fabrication in order to obtain results data based on actual test-chips.

Another important candidate for future work with our design is the calibration. Although we used one-point calibration, we still have a calibration error of 3.9°C. Calibration of sensors which have exponential output characteristic is difficult because non-linearities are always present; if two-point calibration leads to mid-range errors then one-point calibration may lead to errors towards the ends of the range. This issue needs to be given more consideration.
9. References


