High Speed Analog-to-Digital Conversion Utilizing Time Quantization

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Abstract

As communication speeds have increased, high speed and resolution analog-to-digital converters (ADCs) have become necessary. ADCs have traditionally relied on comparing an input voltage to a reference voltage and digitizing the result. The increased speed of operation requires faster processes, which in turn limit the usable input voltage range due to breakdown voltage limitations. The work presented in this thesis studies two aspects of ADCs and possible alternate implementations to address existing limitations.

A sample-and-hold amplifier (SHA) is a common first stage for ADCs. At high frequencies, the SHA provides valuable timing relief to subsequent stages. Biasing of the high speed circuits consumes valuable headroom in low voltage circuits, limiting operation of existing architectures to supply voltages of at least 1.8V. An alternative architecture is presented that allows reduced supply voltages to be used.

An alternative core ADC architecture is also discussed. The implementation chosen utilizes a time measurement system that quantizes time instead of voltage. A phase delay proportional to the input voltage is first generated. This signal is then quantized using a time-to-digital converter. The use of active devices in the clock path is eliminated, allowing for increase operation speed while delay generation is accomplished with varactors, allowing for large voltage swings on the input signal.

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Chapter 1 Introduction

1.1 Introduction

As operating speeds for modern communications continue to increase, the need for high resolution conversion from the analog to the digital domain has created a critical bottleneck. Circuits operating at rates of 40Gbits/s are entering the marketplace, but current technologies have limited analog-to-digital conversion to fewer than three bits at these speeds [1]. In addition, breakdown voltages for high speed processes continue to drop, resulting in reduced input dynamic range, while cost per unit area is increasing expensive. These factors contribute to the need for alternative high speed analog-to-digital conversion (ADC) solutions.

Microwave theory has traditionally been used to model and predict the high frequency behavior of passive and active structures in systems such as radar and wireless communication. With the increasing bandwidth demands of wired and wireless communication, the knowledge and expertise from this specialty combined with that of integrated circuitry may be used to improve the operation of ADCs.

This work focuses on applying broadband microwave structures to integrated circuit design to improve the operation of ADCs limited to a small number of bits at high data rates.

Significant work has been done both in the field of microwave design and integrated circuit design. The structures of interest that were studied are broken into several sections: transmission lines and distributed amplifiers, time-to-digital

converters, sample-and-hold amplifiers and analog-to-digital converters. For each of these, the techniques and circuits employed are discussed in subsequent chapters.

The ideas represented in these areas of research suggest that the combination of microwave structures and integrated circuit technology to design ADCs may yield significant benefits.

1.2 Overview of Thesis

The thesis is organized as follows. Chapter 2 discusses transmission line and distributed amplifier analysis. Time-to-digital converter topologies are discussed in Chapter 3 with focus on flash and pipelined architectures. Chapter 4 covers the operation of analog-to-digital converters in general and proceeds to discuss the flash architecture as well as time based converter topologies. The operation of and simulation results for the proposed track-and-hold amplifier architecture are developed in Chapter 5. In Chapter 6, the theory and simulation of the proposed analog-to-digital converter is presented. Chapter 7 discusses the experimental results for the proposed ADC. Finally, Chapter 8 discusses the conclusions of this work and future areas of inquiry.

Chapter 2 Transmission Lines and Distributed Amplifiers

2.1 Introduction

The all pass transmission line offers significant benefits for broadband signal transmission. This chapter discusses the operation of transmission lines from a circuits' perspective and examines the active circuit design of a distributed amplifier that exploits the strengths of the transmission line to stretch the maximum gain-bandwidth product achievable.

Fundamental electromagnetic theory was developed over a hundred years ago and the governing equations developed by Maxwell have been applied to various structures since, including transmission lines. These applied equations give insight into the expected transmission characteristics of a transmission line, including the finite speed of the confined electromagnetic wave.

Circuit theory has also been used to describe transmission line behavior, resulting in a basic passive model for an infinitely small section of line. The circuit model suggests manipulations of circuit elements that may be used to maximize power delivery to the load over narrow and wide frequency bands. Section 2.2 further discusses the operation of a transmission line.

From basic circuit theory it is seen that maximum power transfer is obtained in a system when the source and load impedances are equal. Additionally, electromagnetic theory indicates that the impedance of the transmission medium must match the source

and load impedance. A matched connection between a source and load may be implemented with a transmission line.

Active circuits may be designed to take advantage of the all pass nature of a transmission line structure for broadband frequency designs. A capacitive input terminal on a transistor may be used to load a transmission line periodically to attain maximum power transfer over a broad range of frequencies. This performance may also be approximated using a periodic structure with lumped elements, emulating the finite circuit model of an ideal transmission line. Section 2.3 discusses the operation of the distributed amplifier, which exploits this structure.

2.2 Transmission Line Operation

A transmission line guides the wave propagation of an electrical signal. For distances that are on the order of an electrical wavelength, transmission line theory is important in accounting for timing and loss effects. From a circuit standpoint, an infinitesimal section of transmission line may be modeled as shown in Figure 2.1, where R_o is the resistance per unit length, L_o is the inductance per unit length, C_o is the capacitance per unit length, and G_o is the conductance per unit length.

From [2], the characteristic impedance per unit length, Z_o, of the transmission line is

$$Z_o = \sqrt{\frac{R_o + j\omega L_o}{G_o + j\omega C_o}} \tag{2.2.1}$$

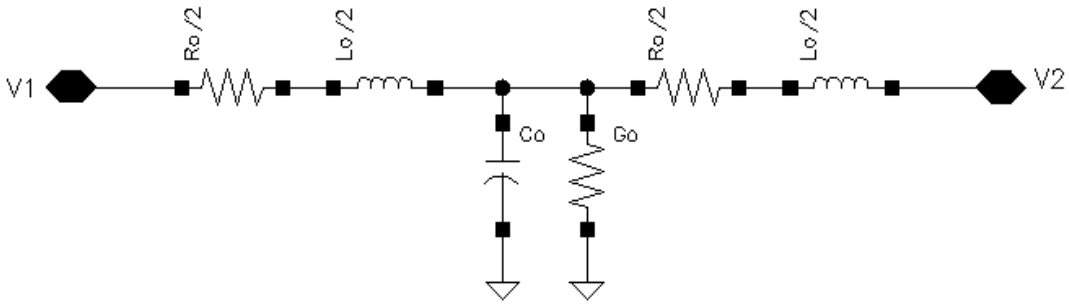


Figure 2.1 - Transmission Line Section Model

and the propagation constant, γ, of the signal is

$$\gamma = \alpha + j\beta = \sqrt{(R_o + j\omega L_o)(G_o + j\omega C_o)} \tag{2.2.2}$$

where α is the attenuation constant of the line in Nepers/meter and β is the phase constant of a wave in radians/meter. Voltage transmission along the line can be described as

$$V(x) = V_0 e^{-\alpha x} e^{-j\beta x}. \tag{2.2.3}$$

In an ideal, lossless transmission line, R_o, which is the series conductor resistance, and G_o, which is the conductance per unit length of the line to ground, are assumed to be zero. In this situation, (2.2.1) and (2.2.2) to reduce to

$$Z_o = \sqrt{L_o / C_o} \qquad \text{and} \qquad \gamma = j\beta = j\omega\sqrt{L_o C_o} \tag{2.2.4}$$

and (2.2.3) reduces to

$$V(x) = V_0 e^{-j\beta x}. \tag{2.2.5}$$

Assuming the line is low loss, the expressions in (2.2.4) may be used as an approximation of impedance and phase constant for design purposes.

The model shown in Figure 2.1 assumes an infinitely small section of transmission line, however it also suggests another possible transmission line

configuration. By employing inductors and capacitors arranged in this configuration, transmission line characteristics may be emulated to create an artificial transmission line. Unlike the all pass transmission line, an artificial transmission line composed of N LC sections creates a low pass structure with N LC poles.

Both the artificial transmission line configuration and a true transmission line may be loaded at fixed intervals with a capacitive element to create a periodically loaded transmission line (PLTL). These are employed in circuits ranging from phase modulators [4]-[6] to distributed amplifiers [7]-[15]. Analysis of a PLTL is similar to that of an artificial transmission line since N low pass structures are created with the lumped element capacitors introduced on the transmission line.

The impedance calculation of (2.2.4) may be used for a section of the structure instead of using an inductance and capacitance per unit length and the phase constant may be used to calculate transmission velocity. These calculations are an appropriate approximation if the transmission line is not near the -3dB frequency of operation at $1/\pi\sqrt{LC}$, where transmission of the signal becomes compromised and the circuit should not be used.

2.3 Distributed Amplifier Operation

The use of a periodic load on a transmission line for large bandwidth applications may be extended to use in active circuits. One example of this is found in distributed amplifiers. The basic operation of a distributed amplifier exploits the use of a periodic structure to extend the gain-bandwidth product of an amplifier beyond typical operation limits [7]-[8].

Distributed amplifiers have been used in various high speed circuit designs including low noise amplifiers [9]-[10] and phase-locked loop frequency dividers [11]. Due to the enhanced gain-bandwidth product, techniques to exploit various aspects of distributed amplifiers for communications [12] as well as general purpose amplifier [13]-[15] have been employed.

In a distributed amplifier (DA), the capacitive input node of several gain elements, commonly transistors, are spaced periodically along a true or artificial transmission line. Consequently, the input and output to the circuit now consists of a PLTL. This method has been employed in various technologies, including vacuum tubes, printed circuit boards, GaAs MESFETs, and more recently in bipolar and CMOS. The analysis below will focus on CMOS implementations, however it is applicable to other devices.

A circuit diagram of a DA in CMOS is shown in Figure 2.2. The first implementation shows the use of lumped elements to create an artificial PLTL while the second shows the use of transmission lines as the inductive circuit component.

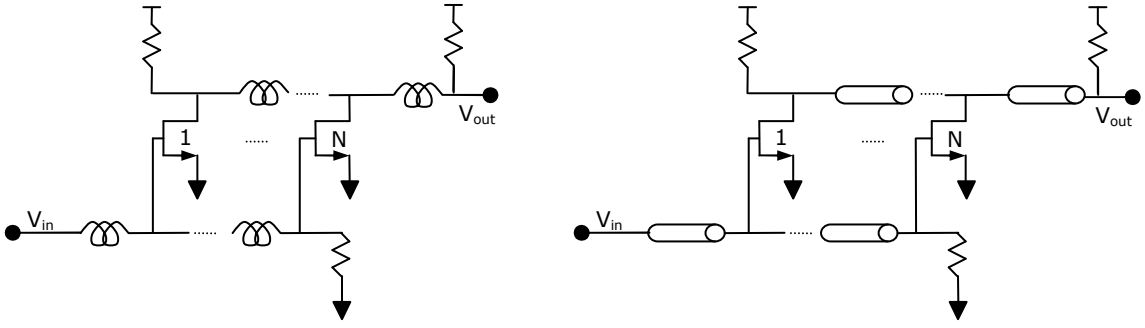


Figure 2.2 - (a) Lumped Element DA (b) Transmission Line DA

In both of these implementations, the gate capacitance, C_{gs}, and the drain capacitance, C_{ds} act as a periodic load. The load is typically much larger than the

capacitance per unit length of the transmission line or the capacitance of the lumped element component of the artificial transmission line. This produces a characteristic, real input impedance to the circuit of

$$Z_{in} \cong \sqrt{L_{xlineSec} / C_{xs}} \tag{2.3.1}$$

where Z_{in} is the input impedance, $L_{xlineSec}$ is the inductance of one section of the line on the gate or drain side of the amplifier, and C_{xs} is the gate capacitance of the amplifier on the input and the drain capacitance of the amplifier on the output. The input and output capacitances of the amplifier now appear real while the low frequency corner for amplifier operation is generated by the line itself and is on the order of

$$f_s \cong \frac{1}{2\pi\sqrt{L_{xlineSec} C_{xs}}} \quad . \tag{2.3.2}$$

As the frequency of operation approaches (2.3.2), the transmission line appears as a resonant LC circuit. The result of this is that the circuit effectively has a maximum frequency of operation.

The limitation on impedance imposed by (2.3.1) and on frequency of operation by (2.3.2) effectively bounds the allowable inductance and capacitance values for desired operation. Based on these constraints, one of two methods for producing inductance is chosen: a lumped element distribution employing a series of lumped element inductors driving the transistors, as in Figure 2.2 (a), or a length dependant inductance loaded with gate capacitances, as shown in Figure 2.2 (b).

Each of these methods has advantages: a lumped element distribution can generate a larger inductance in a given area with acceptable loss, which allows a higher capacitance value for a desired impedance. A transmission line will require more area

and has a higher loss for a given equivalent inductance, but it is able to operate at higher frequencies than a lumped element inductor which is frequency limited by coil coupling capacitance.

For the purposes of the highest speed broadband amplifiers, a periodically loaded transmission line approach is the most appropriate. Due to the physical limitations governing the gate capacitance of a MOS device and the inductance per unit length of the transmission line, this method is not well suited to CMOS processes with feature size larger than 0.18μm.

When implementing a DA, phase of the signal is important consider. This amplifier relies on the drain current of the devices adding in phase. The phase delay of a section of a DA is equal to

$$\tau = \sqrt{L_{xlineSec} C_{xs}} \,. \tag{2.3.3}$$

To ensure current is added in phase, τ of a section on the gate of the device should be equal to τ of a section on the drain of the device. This requires careful balancing of the gate and drain inductances due to a larger capacitance at the gate of a transistor than at the drain.

For some applications, particularly in the microwave domain, power gain of a DA is critical. For the purposes of this discussion, the focus will be on voltage gain. The voltage gain of the amplifier may be calculated by summing the current through each stage and calculating the voltage at the output load. This results in a gain of

$$A_v \cong -\sum_{i=0}^{n-1} \frac{g_m Z_{od}}{2} 1^i = -\frac{N g_m Z_{od}}{2} \tag{2.3.4}$$

where N is the number of stages, g_m is the transconductance of one of the amplifiers, and Z_{od} is the output impedance of the amplifier. This is a simplified, small signal equation that assumes lossless transmission of the signal through the transmission line, which is only valid for short distances.

Including the transmission line loss (with the conductance loss of the transistors), the voltage gain equation must be modified to include loss terms. Using equation (2.2.3) with (2.3.4), the equation for voltage gain becomes:

$$A_v = -\sum_{k=0}^{n-1} e^{-\alpha k l} \frac{g_m Z_{od}}{2} \tag{2.3.5}$$

From this equation, the maximum voltage gain is limited by the loss of the transmission line, α [7]. This result may be used to optimize voltage gain of a DA when transmission line loss is known.

The technique of periodically loading an active circuit on a transmission line has applications beyond DAs, as discussed briefly in Section 2.2. In situations where this configuration is employed, (2.3.1) through (2.3.3) may be used to determine various aspects of the input network.

Overall, the distributed amplifier takes advantage of the strengths of electrical conduction through transmission lines and the gain of active devices to create powerful broadband amplifiers.

Chapter 3 Time-to-Digital Converters

3.1 Introduction

For high speed structures, the transient behavior of a high speed signal in terms of a wave is critical to understanding the operation of structures. This suggests that exploiting the time interval information included in a traveling wave might be significant. One circuit category that focuses on time interval may be found in a time-to-digital converter (TDC).

As the name implies, TDCs convert time interval information directly to a digital value. For event based measurements, including arrival time information for particle accelerator detectors and valve timing in automobiles, they offer a straightforward implementation of a desired function.

Some TDC implementations are designed to measure large time differences with high accuracy, others to measure large differences with moderate accuracy, and still others to measure moderate differences with moderate accuracy. When measuring a time difference, the operational speed of the TDC is clearly determined by the length of the time difference. This indicates that data throughput is limited by the length of time being measured. A small time difference may allow high data throughput, while long time differences will necessarily entail low data throughput and high latency.

Architectures for TDCs may be broadly broken into two categories: flash and pipelined. Flash architectures may be used as a section of a pipeline system and also

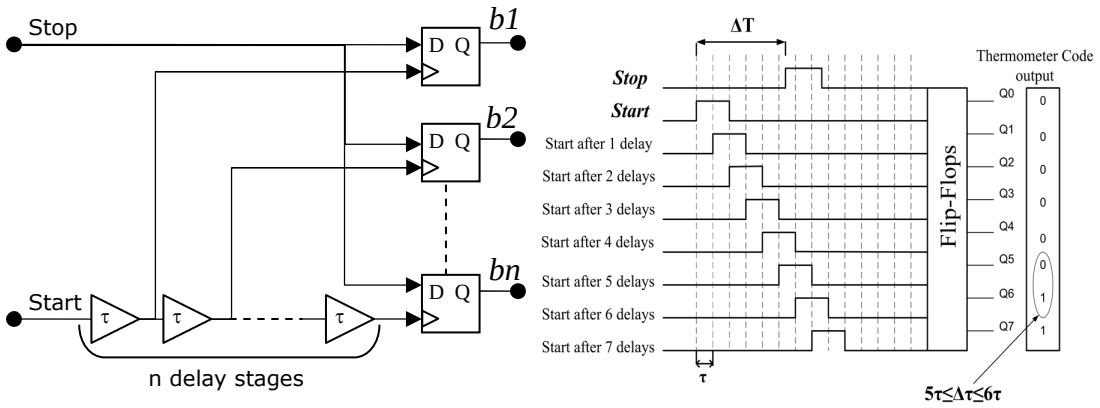
employ techniques such as interpolation [16]-[19]. This style of architecture is used to resolve small time steps and grows in size as a function of 2^N where N is the number of bits to be resolved. Some areas of application for this style of TDC may be found in all digital systems designed with only digital components that employ the TDC for phase measurements, such as in [20], as well as in time based measurements such as ultrasound [21].

TDCs are also employed in pipeline structures, where a smaller number of bits is resolved during one phase of processing and the difference between the ideal signal and the digital representation is resolved in a subsequent section. This style of conversion is attractive because it reduces the exponential growth in number of comparators necessary for N bits of resolution, however it results in higher system latency. In some cases, the pipelining is implemented with a time amplifier [22] to reduce the minimum resolution while in others the pipelining is implemented without amplification [23]-[24].

3.2 Flash Implementations

To resolve small time steps in the picosecond range, a flash implementation of a TDC is typically used. Various flash implementations attempt to reduce the minimum time spacing between sections. At the most basic, a flash TDC is designed as shown in Figure 3.1 (a). Delay, τ, in these stages is typically generated with an inverter or buffer stage, making the minimum time spacing equal to a gate delay. Each delayed signal is input to a flip-flop and the output of the flip-flops is the digital representation of the time delay. Figure 3.1 (b) from [16] is a timing diagram of this style of TDC. In the

timing diagram, it may be seen that a start pulse is generated and travels through seven delay stages. The arrival time of the signal at each flip-flop is compared to the arrival time of the stop pulse and an output logic level of "1" occurs if the start pulse is high when the stop pulse transitions high and "0" otherwise, resulting in a thermometer code.



(a) (b)

Figure 3.1 - Flash TDC Implementation

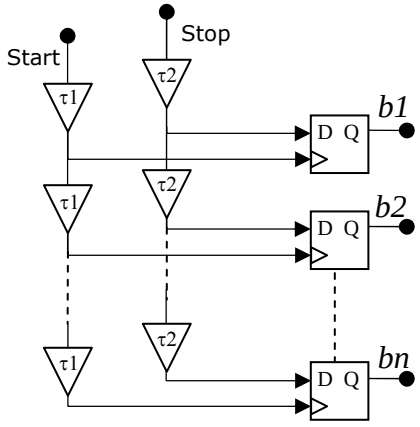


Figure 3.2 - Flash TDC with Vernier Delay Line

To reduce the minimum delay between stages, another style of flash implementation employs a Vernier delay line, as shown in Figure 3.2. The minimum time difference between the start and stop bit is reduced in this architecture to the time difference between the start and stop lines, which is equal to n*(τ1-τ2), where n is the

number of delay stages the signal has traveled through, $\tau 1$ is the delay per stage for the start line and $\tau 2$ is the delay per stage for the stop line . Implementations of this architecture have achieved time resolution as small as 1.25ps, a significant improvement over the standard delay implementation, however this comes at the expense of increased latency due to the delay required on the stop line.

Additional time resolution reduction may be achieved using time interpolation [17] in combination with a standard architecture or using a Vernier delay line. Figure 3.3 shows an example implementation of one delay stage with time interpolation. This delay section may be substituted for a standard buffer or inverter in a flash TDC to improve time resolution with reduced latency compared to a Vernier delay line implementation.

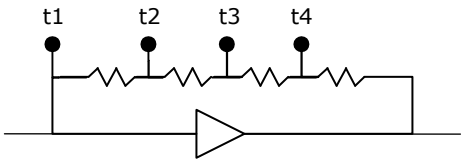


Figure 3.3 - Delay Stage with Four Interpolated Edges

3.3 Pipelined Implementations

A flash TDC implementation grows in size as 2^N where N is the number of bits of resolution. As a practical matter, this will limit the number of bits that may be implemented using this architecture. To alleviate the chip area and power consumption that are caused by this exponential growth, a pipelined TDC may be employed. The literature shows that pipelined architectures are implemented in various ways [22]-[24].

For a pipelined system, the minimum time for the conversion to be completed is the clock cycle multiplied by the number of pipelined stages. Many TDCs operate over multiple clock cycles, further increasing the latency of the system. The focus of this section are the pipelined architectures that operate with one clock cycle per pipeline stage.

A method employing time amplification is discussed in [22] and the architecture is shown in Figure 3.4. For this system, the first five bits are resolved with a coarse TDC while multiple time differences are simultaneously amplified, as shown in Figure 3.4. An offset time, kT_d, where kT_d is different for each residue block, is subtracted from time T_{IN} and the time residue is amplified in TA. The amplified time signal is chosen by the multiplexer (mux), controlled by the coarse TDC, and the final time difference is quantified using an additional four bit TDC. The pre-processing of the time difference using multiple time amplifiers and adder blocks is highly area inefficient in this implementation, but does allow relatively fast operation for a 9 bit TDC.

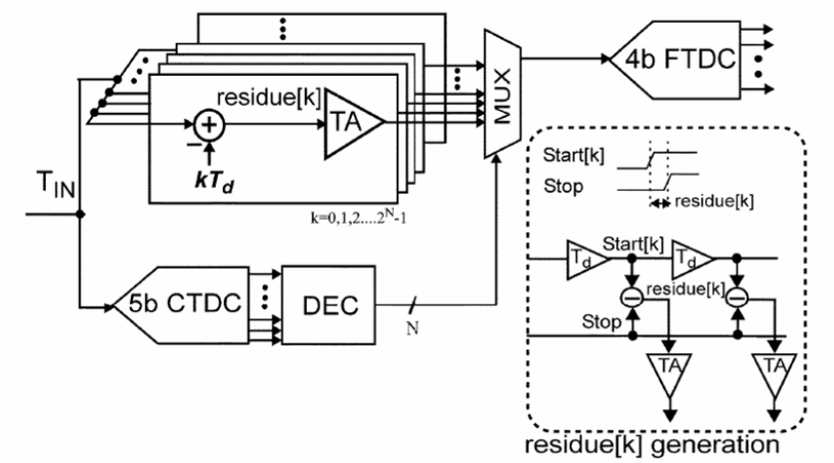


Figure 3.4 - Pipelined Two Step TDC

Another method of pipelining TDCs is proposed in [23] and the operational outline and timing diagram are shown in Figure 3.5. This implementation resolves the largest time step with the first comparator and subsequent time steps with additional time delays. As shown in the timing diagram of Figure 3.5, the START/STOP signal is compared to the Clock signal first after a delay of τ, then a delay of $\tau/2$, and finally after a delay of $\tau/4$. The START/STOP signal is found to be high for a time of $\tau+\tau/4$ over the Clock. More generally for this architecture, during the first stage τ is subtracted from the clock and the residue is used to determine if the time difference is more or less than τ. Each subsequent stage subtracts half of the time delay of the previous stage. This continues to the finest resolution attainable with given devices.

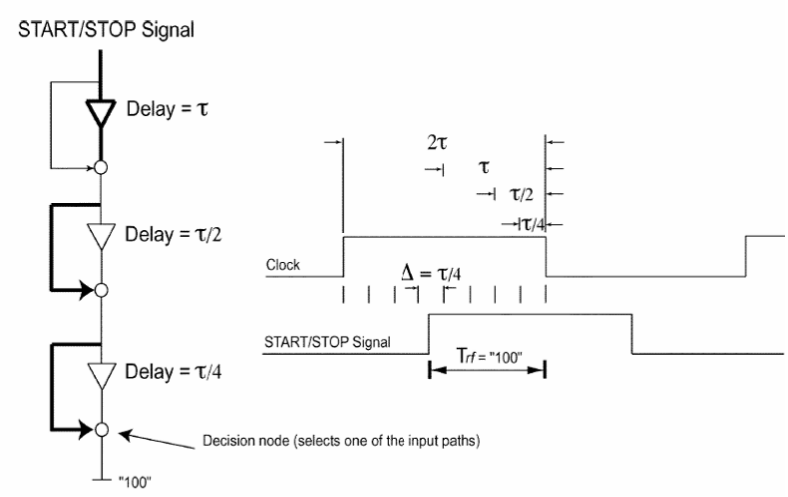


Figure 3.5 - Pipelined Multi-Step

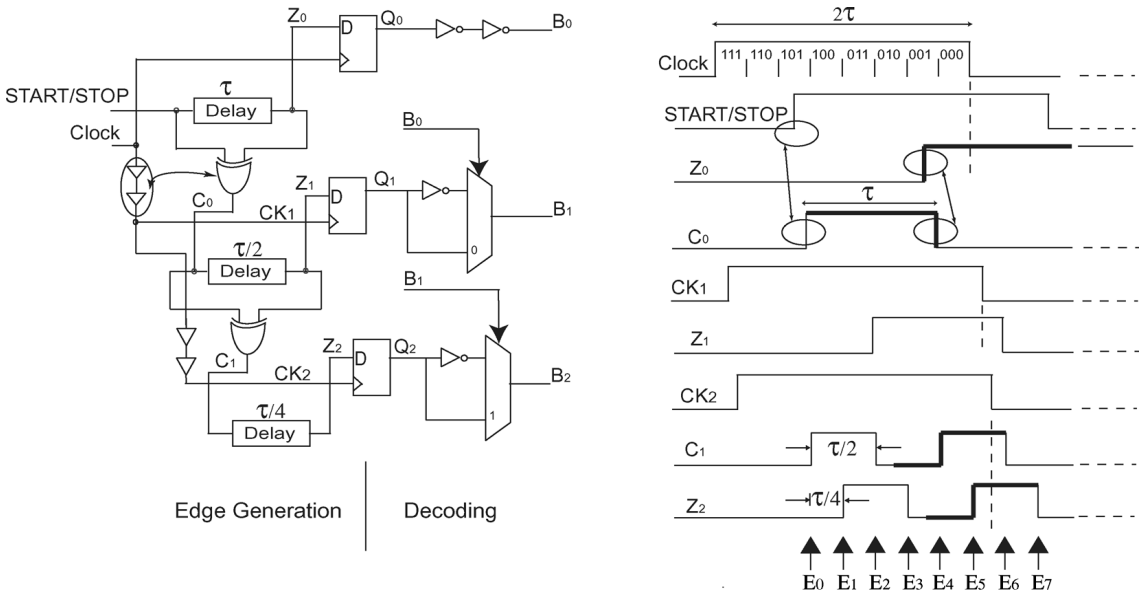


Figure 3.6 - Pipeline Implementation

The specific implementation and timing diagram discussed in [23] is shown in Figure. 3.6 and relies on cascaded decision making. Once a START/STOP signal is input to the system, the first flip-flop compares the delayed arrival time to the arrival time of the clock. The output decision of this circuit is fed to the output mux of the next stage. The output state Q1 of this stage is determined by comparing the delayed arrival time to the arrival time of the clock. From here, the value of B1 is determined based on the value of Q1 and B0. The delay addition to the start/stop signal becomes progressively smaller as the most significant bits are decided. This implementation has the benefit of very small area consumption and relatively simple implementation, however the latency of the output is strongly dependent on whether the propagation delay for the XOR gates are longer or shorter than the clock frequency. If they are longer than the clock frequency, the latency for this system will be larger than the expected three clock cycles due to pipelining.

A TDC allows the time information contained in a signal to be exploited. In Chapters 7 and 8, an alternative implementation of a TDC is presented. Additionally, the alternative TDC is used in conjunction with microwave structures to implement a high speed ADC. This style of ADC may also be implemented with one of the TDCs presented here to allow for reduced power and area consumption.

Chapter 4 Sample and Hold Amplifiers in High Speed Analog-to-Digital Converters

4.1 Introduction

The previous chapter discussed a TDC as a way to convert the analog signal of time to the digital domain. Analog conversion is more commonly implemented with an analog-to-digital converter (ADC), which converts an input analog voltage signal to a digital signal. An ADC operates by sampling an input signal at a given point in time and converting that sample to a digital word [25]. Physical implementations of this frequently employ a sample-and-hold (SHA) or track-and-hold (THA) amplifier to improve timing accuracy. At high frequencies, this is especially important due to the limitation on effective number of bits (ENOB) due to clock jitter [1]. With occasional exception [26], the most common high speed implementation of a THA is a structure that relies on switching the current in a source- or emitter-follower [27]-[34]. While this stage is crucial for accurate circuit timing in an ADC, gate switching times continue to limit the maximum rate of operation.

Two SHA architectures are further described in Section 4.2 along with a discussion on the importance of the SHA to the operation of the ADC.

4.2 Sample-and-Hold Architecture

An ADC commonly utilizes an SHA or THA as a first stage. The purpose of an SHA is to buffer the input analog signal and provide a steady output voltage over a portion of a clock cycle during digitization to reduce voltage error. The style of SHA

used varies based on the intended application and may be categorized by desired operation speed.

A common configuration for an ADC with an SHA is shown in Figure 4.1. The SHA receives an input analog signal and a sampling clock. Once per sampling clock cycle, the output of the SHA holds a constant analog voltage value proportional to the input analog signal. This voltage is "held" at a constant value for the remainder of the clock cycle and input to the ADC. The held value is then converted to a series of N ones and zeros, where N in the number of bits of resolution of the ADC core, to digitally represent the input analog signal. Timing considerations in the ADC are eased with the addition of the SHA block, making it a frequently used first stage for systems with large clock trees.

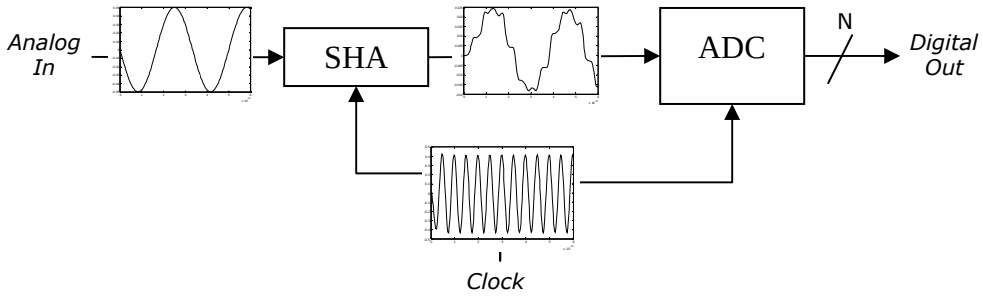


Figure 4.1 - ADC Utilizing SHA Block

For low speed, low power applications, a switched capacitor circuit is commonly used. As may be seen in Figure 4.2, a basic switched capacitor sample-and-hold circuit consists of a MOS device that is turned on and off at the gate to allow charge transfer through the channel of the device onto a hold capacitor, C_H. When the switch is on, the capacitor is charged, and when the switch is turned off, there is no current flow. The appeal of this approach is its simplicity and relatively low power

consumption. Power to the circuit is limited to the transient charge and discharge of the *Clk* line and the charge of V_{in} onto C_H.

The primary limitations of this circuit are due to the switch. An ideal switch control line, *Clk*, would be fully isolated from the signal path and the signal path would have zero resistance when the switch was closed and infinite resistance when the switch was open, making the fundamental speed limitation for the circuit the RC pole of the drive resistance and the load capacitance.

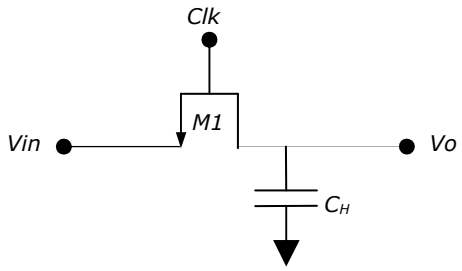


Figure 4.2 - Switched Capacitor Circuit

In reality, the switch contains parasitic capacitance from the switch control line to the signal path, which allows the clock signal to be injected onto the signal line. The switch also inserts a non-linear resistance into the signal path when it is turned on. Both of these factors limit the usable input frequencies of a switched capacitor circuit.

At frequencies from hundreds of megahertz and higher, different methods are used to reduce the impact of these limitations. One popular high speed implementation of the SHA is a switched emitter or source follower configuration, as shown in Figure 4.3.

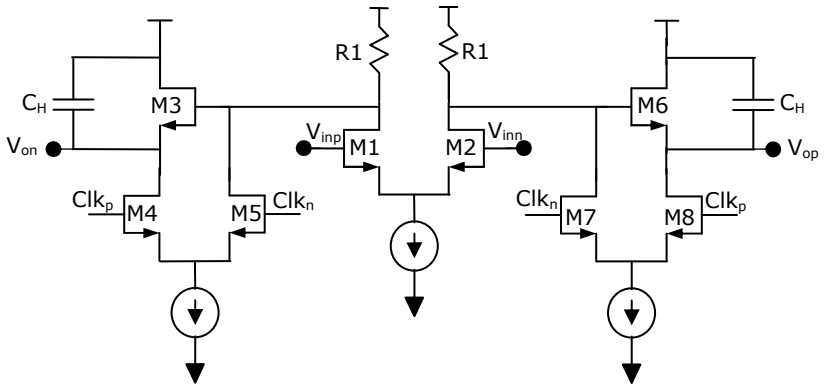


Figure 4.3 - Switched Source Follower SHA Architecture

This sample-and-hold amplifier typically contains an input unity gain amplifier consisting of M1, M2, and R1. From here, the signal is passed to the sample-and-hold amplifier core which operates by turning on and off the current in transistors M3 and M6. When M4 and M8 are on, current flows through the source follower, allowing the capacitor, C_H, to charge. When M5 and M7 are on, the source follower is turned off and the voltage on the capacitors is maintained. Due to the relatively small device stack up, this design may be used with relatively low supply voltages (on the order of 1.8V). This architecture has been used in designs up to 40GS/s in SiGe bipolar designs and at speeds up to 30GS/s in CMOS and InP designs [26]-[33]. Typically the input stage is a unity gain differential buffer with high bandwidth and the drive capability for the next stage. Implementations of this circuit claim between 4 and 8 effective number of bits resolution capability.

A model of the half circuit in Figure 4.3 containing M1 and M3 with M4 turned on and M5 turned off is shown below. This circuit shows the operation of capacitor charging in the tracking portion of the cycle.

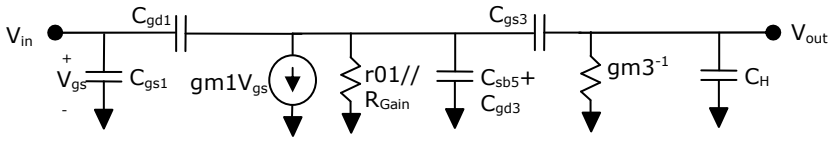


Figure 4.4 - Switched Source Follower Half Circuit

From Figure 4.4, it may be seen that there are two poles for this half circuit at approximately $1/[(r01//R_{Gain})*(C_{sb5}+C_{gd3})]$ and $1/[gm3^{-1}*C_H]$. Of these two poles, the dominant one is $1/[gm3^{-1}*C_H]$ given that the hold capacitance is expected to be significantly larger than the parasitic capacitance. The dominant pole will determine the maximum rate of operation for this circuit based on voltage settling and voltage stability considerations. This circuit is for the sample half of the clock cycle. For the hold half of the clock cycle, the resistance gm_3^{-1} is opened and the voltage at V_{out} is the value stored on C_H. The poles of the circuit in Figure 4.4 at this point no longer affect the speed of the subsequent circuitry.

The equivalent half circuit for a bipolar circuit may be derived in a similar manner, however due to the base resistance of the bipolar structure, the dominant pole becomes $(1+r_e+gm)/[C_H*(r_e+gm)]$. One significant problem with bipolar designs, is that leakage current through the base of device affects voltage stability of the held value. Compensation for this has been included in some designs, however it is preferable to avoid this problem altogether.

Another current switching design is shown in Figure 4.5 [23].

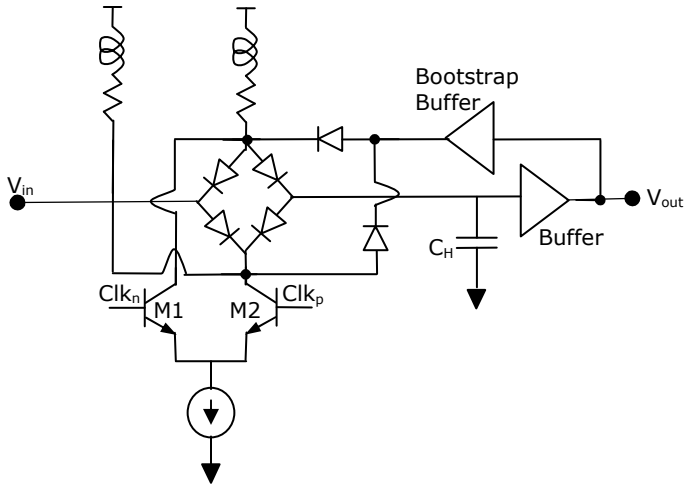


Figure 4.5 - Diode Bridge SHA

As can be seen from the schematic, this circuit also employs the current steering technique. When Clk_p is high, the diode bridge turns on, allowing the input signal to be sampled. When Clk_p is low, the diode bridge is non-conducting and the value is held on the capacitor C_H. This design is able to operate very quickly due to the fast response time of diodes, however, it is more complex and will clearly require a higher supply voltage than the design shown in Figure 4.3. Large supply voltages become a problem for state of the art high speed designs due to relatively low breakdown voltages of high speed devices, thus reducing the popularity of this architecture in current designs.

Chapter 5 Proposed Sample-and-Hold Architecture Analysis and Simulation

5.1 Introduction

As an interface to the outside world, analog-to-digital conversion is critical. Chapter 4 explored commonly used existing architectures of sample-and-hold amplifiers (SHAs). To address some of the limitations of these architectures at high speeds, an alternative sample-and-hold architecture is proposed. Section 5.2 discusses the proposed sample-and-hold architecture operation and Section 5.3 outlines the simulated operation of the architecture.

5.2 Proposed Sample-and-Hold Circuit Operation

Incorporating the strengths of the switched capacitor and the switched source follower circuits leads to an architecture, dubbed the switched cascode. The switched cascode, shown in Figure 5.1, relies on current steering to provide switching, similar to the switched source follower, but employs a switch along the signal path, similar to the switched capacitor. As with the switched source follower circuitry, the switched cascode is most appropriately implemented differentially to reduce non-linear effects, including charge injection.

In Figure 5.1, it is seen that this SHA works by steering current into *M3* and *M7* and out of *M4* and *M8* to turn the cascode on during the sample period of the clock.

Transistors *M2* and *M6* operate in a similar manner to the switch in a switched capacitor circuit. The difference in operation for this circuit relative to the switched capacitor circuit lies in the use of current steering as a switching mechanism. During the track stage of operation, *M3* and *M7* are turned on, pulling the source of *M2* and *M6* low while the gates of *M2* and *M6* is pulled high. The additional current provided to the circuit through the switch allows the capacitor, C_H, to charge more quickly than in the conventional switched capacitor architecture.

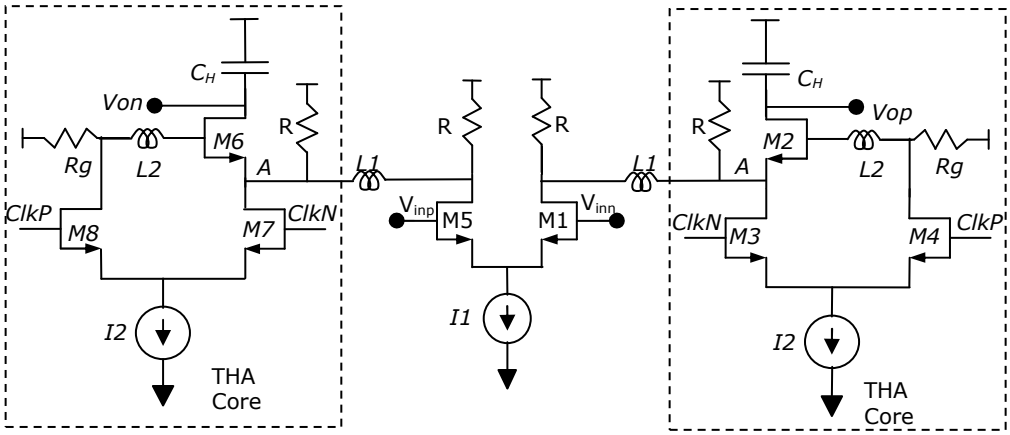


Figure 5.1 - Switched Cascode Circuit

During the hold period of the clock, *M4* and *M8* pull the gates of *M2* and *M6* low to shut the device off. The hold stage of operation occurs when *M4* and *M8* turn on and pull the gate of *M2* and *M6* low, turning the switch off. During hold mode, the charge leakage from the hold capacitor C_H is due to the intrinsic resistance across the capacitor and the finite shutoff time of *M2* and *M6*, making the held voltage highly stable.

The supply voltage required for operation of this circuit is dependent on V_{ds} of *M2*, *M3*, and the current source, allowing operation with lower supply voltages than the

switched source follower configuration. Additionally, by employing a current steering technique for switching, charge time for intrinsic device capacitance is minimized, permitting multi-gigahertz sampling rates.

When analyzing this structure, it is important to consider duty cycle distortion, attainable bandwidth, and output voltage stability. By controlling the source voltage of *M2* relative to the gate voltage, the sinusoidal clock for this circuit has reduced duty cycle distortion relative to the switched capacitor circuit. This occurs because *ClkN* and *ClkP* are greater than V_{gs}-V_{tsat} of *M3* and *M4* for a fixed period of time. These devices switch current at the gate and source of *M2* in a well controlled manner, although the source will continue to contribute to some data dependent duty cycle distortion. When only the gate of *M2* is switched with a control voltage, V_{gs}-V_{tsat} for *M2* switching is dependent on the voltage at the source, which varies with the input signal. Unlike the switched source follower, the switched cascode cannot be designed to maintain operation in only saturation and cutoff. Operation is dependent on V_{ds} of *M2* becoming small, forcing *M2* into triode

By incorporating a current steering switch at the base of a cascode type device, the initial V_{gs} and V_{ds} of *M2* in Figure 5.1, additional current is available for fast charging of C_H during track mode. Figure 5.2 shows simulation results of timing for V_{ds} and V_{gs}-V_{tsat} for *M2* through three clock cycles along with the output voltage signal of the circuit and the current into the hold capacitor, C_H. When V_{ds} is greater than V_{gs}-V_{tsat} which is greater than zero, the device is turned on in saturation mode. Once V_{ds} is smaller than V_{gs}-V_{tsat} and while V_{gs}-V_{tsat} is greater than zero, the device moves to triode operation. These modes of operation both occur when *M2* is conducting and on. In

Figure 5.2, a marker labeled "M2 On" indicates the start of a sample cycle and a marker labeled "M2 Off" indicates the end of the sample cycle and the beginning of the hold cycle. It is seen that charging of C_H begins with *M2* in the saturation region. As V_{gs}-V_{tsat} increases, *M2* begins to operate in triode region and charges at the expected 1/RC rate. The capacitor current is also indicative of circuit operation. During a sampling cycle, current is removed from or injected onto the capacitor until the capacitor voltage

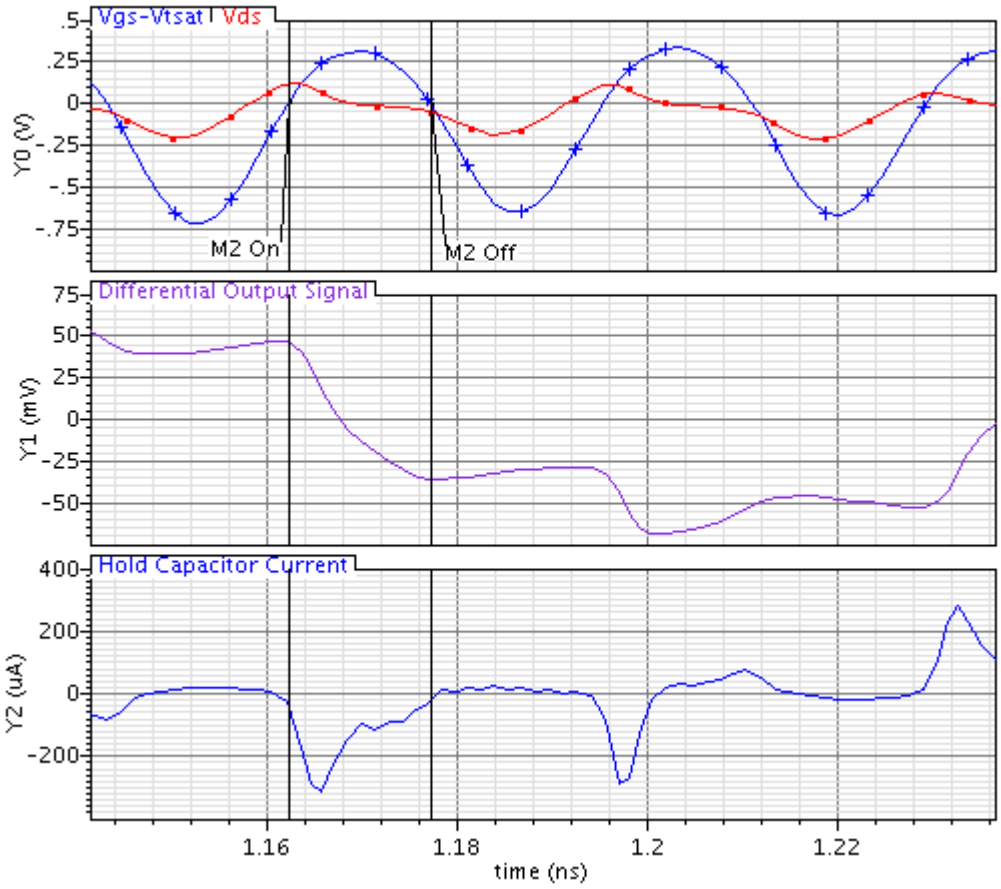


Figure 5.2 - Simulated Switched Cascode Circuit Operation

is equal to the voltage at the source of *M2*. Current remains constant at zero during the hold cycle, indicating that the voltage on the capacitor is held, as is seen from the differential output signal in the timing diagram.

To understand the output voltage limitations, the circuit in Figure 5.3 is analyzed. The output voltage, V_{op}, may be expressed as

$$V_{op} = V_{bias} + V_i + \frac{I_{M2}}{sC_H} \tag{5.2.1}$$

where V_{bias} is the bias voltage on the capacitor C_H, V_i is the initial held voltage on the capacitor, and I_{M2} is the current through *M2*. It is seen that the maximum rate change to V_{op} during the track portion of the cycle and the stability of a voltage during the hold portion of a cycle is due to the current through *M2*. The quality of these two states may be discerned by considering the operation of *M2* in each situation.

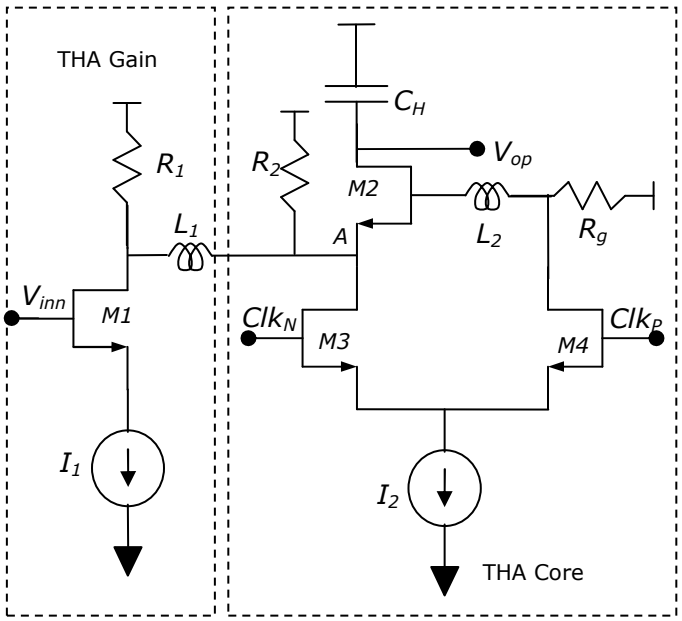


Figure 5.3 - Half Circuit Analysis Model of Switched Cascode Circuit

Switching between track-and-hold states is accomplished in this architecture by steering current from *M3* to *M4* in Figure 5.3. Steering current from *M3* to *M4* produces a change in gate voltage on *M2* that may be described as

$$\Delta V_g = \frac{I_2 \sin(\omega_{clk} t) R_g}{1 + R_g / Z_{Tot} + sL_2 / Z_{Tot}} \tag{5.2.2}$$

where I_2 is switched on and off by Clk_P, a sinusoidal signal, and Z_{Tot} is the combined impedance at the gate of *M2*. As seen in (5.2.2), the maximum switching frequency will be limited by the gate resistance, R_g, and the input impedance of *M2*.

At the source of *M2*, the current switching temporarily pulls the node lower, resulting in V_{ds} across *M2* greater than V_{gs}-V_t and allowing *M2* to operate in the saturation region. While in the saturation region, *M2* operates as a cascode. The primary charging limitation in this configuration is

$$I_{CH} = I_{M2} = C_H \frac{dV_{CH}}{dt} \tag{5.2.3}$$

where the change in voltage on C_H, denoted dV_{CH}/dt, is limited by the amount of current available for charging, I_{CH}, and the size of C_H.

When V_{ds} of *M2* falls below V_{gs}-V_t and V_{gs}-V_t is still greater than zero, the device operates in triode region. During operation in triode region, *M2* acts as a variable resistor with resistance from drain to source of

$$R_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)} \tag{5.2.3}$$

where V_{gs} is the gate to source voltage, V_t is the threshold voltage, W is the width, L is the length, and μ_n and C_{ox} are characteristics of *M2*. During operation, the voltage at the source will continue to change, resulting in a variation of the value of R_{ds}. The maximum speed limitation during this period of operation is due to the pole formed by R_{ds} and C_H. From (5.2.3), it is seen that as V_{gs}-V_t becomes smaller, R_{ds} grows and reduces the frequency of the pole.

When V_{gs} of *M2* is less than V_t, the device turns off and no current flows through *M2*. Since the only discharge path for C_H is through *M2*, I_{M2} goes to zero and the held value is seen from (5.2.1) to simply be V_{bias}+V_i.

5.3 Sample-and-Hold Circuit Simulations

Both the switched source follower and the switched cascode architectures were designed in a 0.13μm CMOS process and device sizing was preserved, where appropriate, for both circuits, with the hold capacitor for each architecture adjusted to attain matching bandwidths. Extracted simulations were run on the switched source follower and the switched cascode architectures and compared for gain and SFDR. Based on the design in [13], supply voltages were set to 1.8V. If degraded performance is acceptable, a lower supply voltage could be used. Figure 5.4 shows the extracted transient output for both architectures using a 30GHz clock and a 7GHz input signal.

The held value for the switched cascode has better definition than for the switched emitter follower and slightly lower voltage range. This indicates that an increased analog-to-digital resolution may be attained using the switched cascode architecture at high speeds due to reduced voltage error.

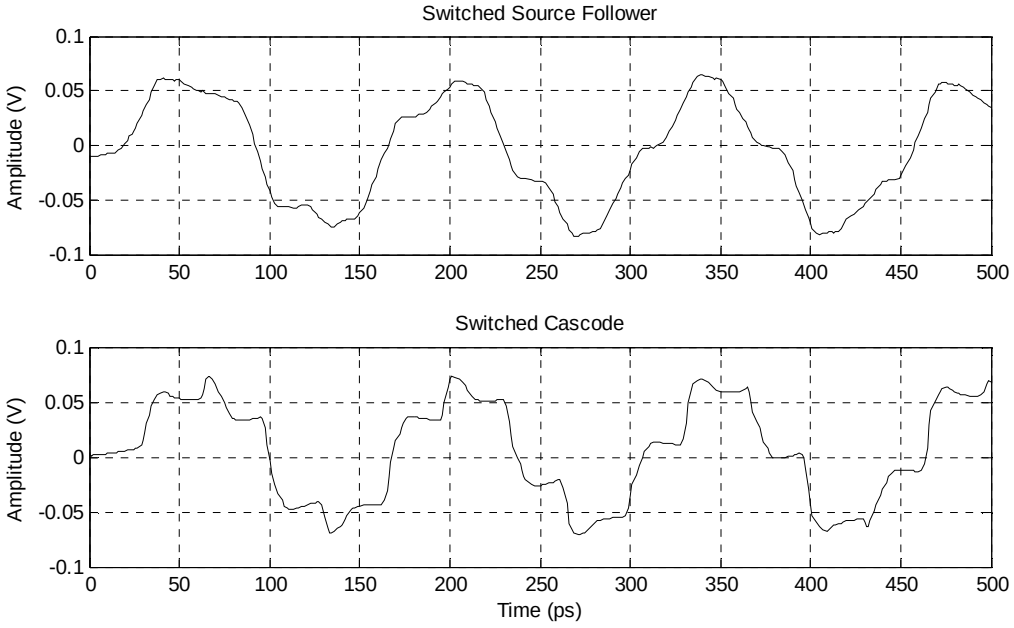


Figure 5.4 - 7GHz Transient Signal Sampled at 30GHz

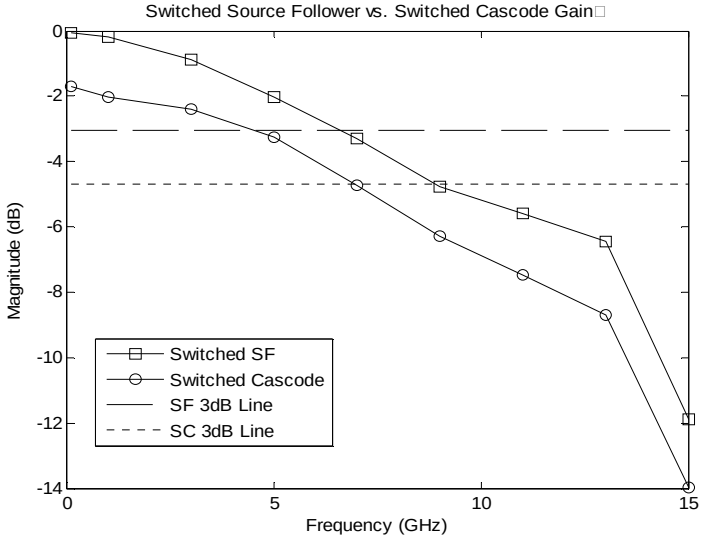


Figure 5.5 - Bandwidth Plot of Switched Source Follower vs. Switched Cascode

Output amplitude versus input frequency using a 30GHz clock is plotted in Figure 5.5. Each circuit has approximately 7GHz of bandwidth. The switched source

follower has about 2dB higher gain than the switched cascode architecture. Gain of the switched cascode may be increased by using a higher gain amplifier, however circuit biasing for the gain stage of the two circuits would not allow device sizing to be maintained. The 3dB frequency of the switched cascode is primarily affected by the voltage dependent resistance of *M2* and will ultimately limit the attainable bandwidth.

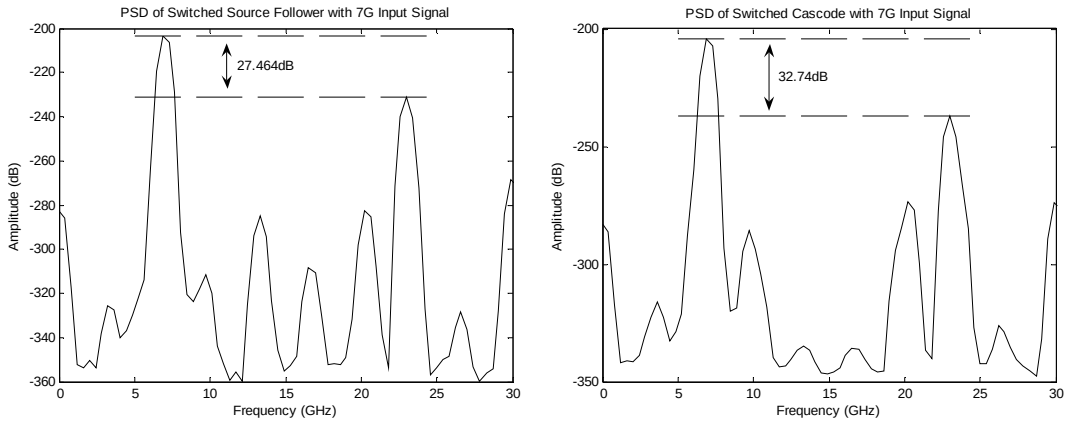


Figure 5.6 – Power Spectral Density (PSD) Plot of Switched Source Follower vs. Switched Cascode

The power spectral density (PSD) of the 7GHz transient signal seen in Figure 5.4 is plotted in Figure 5.6. It is observed that the switched source follower architecture attains 27.5dB SFDR while the switched cascode architecture attains 32.7dB. A 5.2dB increase in SFDR correlates to approximately 0.9 bits more resolution. Circuits operating at these speeds expect a resolution of 2-3 bits [14]. In Figure 5.7, it is seen that SFDR is improved for frequencies between 500MHz and 11GHz, with SFDR of the two circuits roughly equal for frequencies lower than 500MHz and higher than 11GHz.

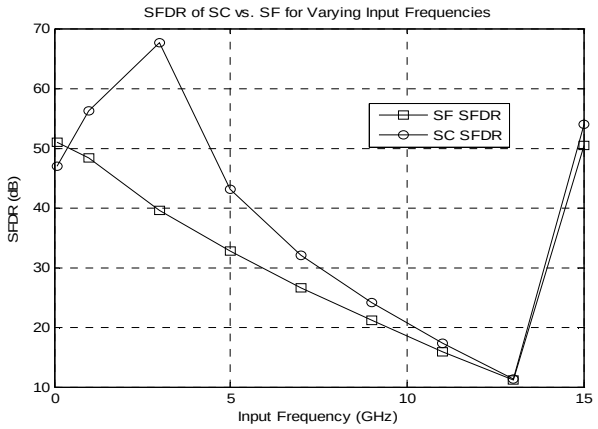


Figure 5.7 - SFDR Over Varying Input Frequencies

Chapter 6 Sample-and-Hold Experimental Results

6.1 Introduction

To verify the operation of the proposed SHA, an integrated circuit utilizing the architecture described in Chapter 5 was designed, laid-out, processed, and tested. The results are presented in the following sections.

6.2 Operation of Sample-and-Hold Amplifier

The SHA discussed in Chapter 5 was designed in 0.13μm CMOS and fabricated by UMC and testing was conducted to verify its performance. In addition to the circuits discussed in Chapter 5, a distributed amplifier was used as the input amplifier to the circuit and a 50Ω output driver was incorporated to allow external analysis of the circuit.

The distributed amplifier is shown in Figure 6.1. As shown in the figure, the circuitry was implemented differentially for increased common-mode rejection. Figure 6.2 is a schematic of the SHA core and the 50Ω output driver for the circuitry. Unlike the circuit used for analysis in Chapter 5 for comparison with the switched common-source amplifier, there is no inductor on the gate of the switches. This improves manufacturability, but reduces the attainable signal bandwidth. A simple 50Ω differential amplifier was used as an output driver and electrostatic discharge (ESD) devices were added to all external signal lines to prevent damage to core circuitry. Device sizing for the transistors is shown in both figures and assumes a minimum gate length.

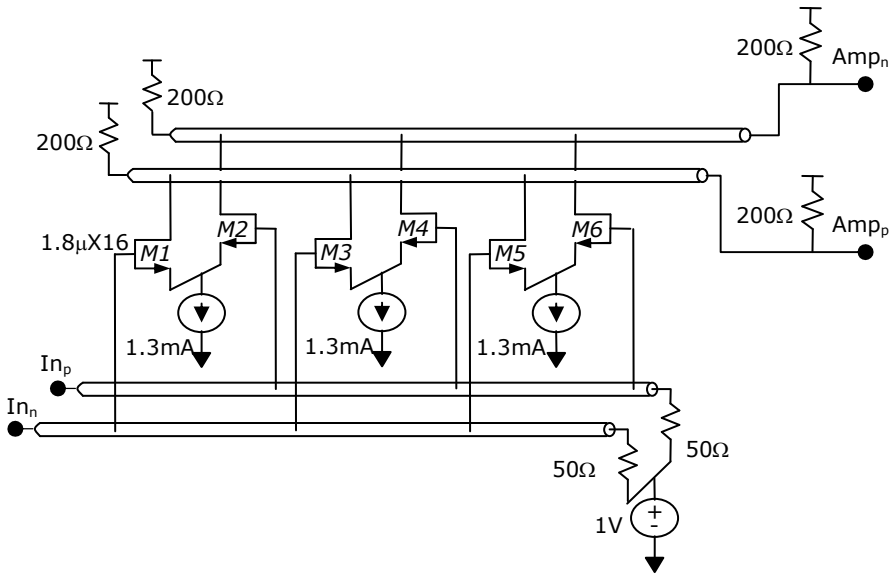


Figure 6.1 - Distributed Amplifier

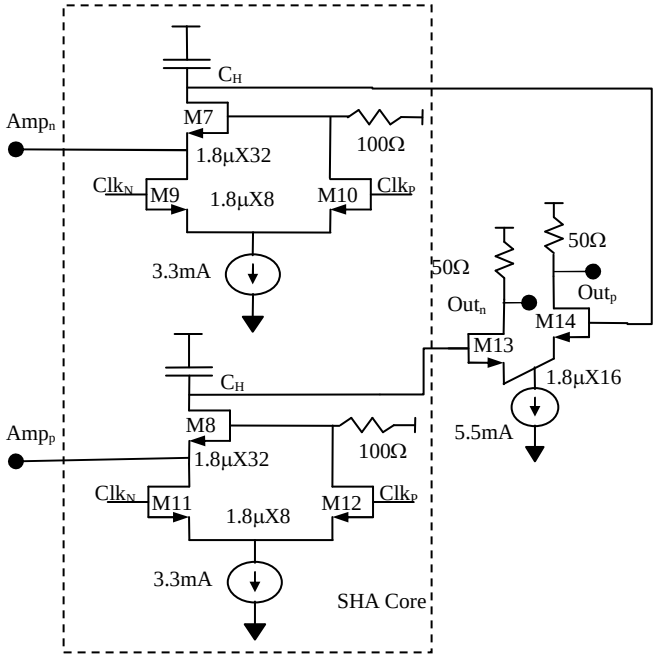


Figure 6.2 - SHA Core and Output Driver

Transistors *M1-M6* were sized and biased in conjunction with the transmission lines and output resistance to provide a voltage gain of 5dB, or roughly 2, and a bandwidth of 17.5GHz. Four of the transistors in the SHA core, *M7-M9* and *M11* are a capacitive load on the output of the distributed amplifier in addition to providing the

desired switching operation to the circuitry. This required a balance in design between loading of the amplifier and switching characteristics of the SHA core including on resistance, current carrying capacity, and turn on time. The output of this core was loaded with a 50Ω output driver whose size was a balance between current drive capability, capacitive load to the SHA core, and optimal current density for peak frequency operation. Current sources were designed for simplicity and tunability and consist of a current mirror connected to an external variable resistor.

A photograph of the test chip is shown in Figure 6.3. To improve performance of the circuit, the input and output signals were probed directly on pads. This significantly reduces the parasitic effects of packaging on high frequency operation.

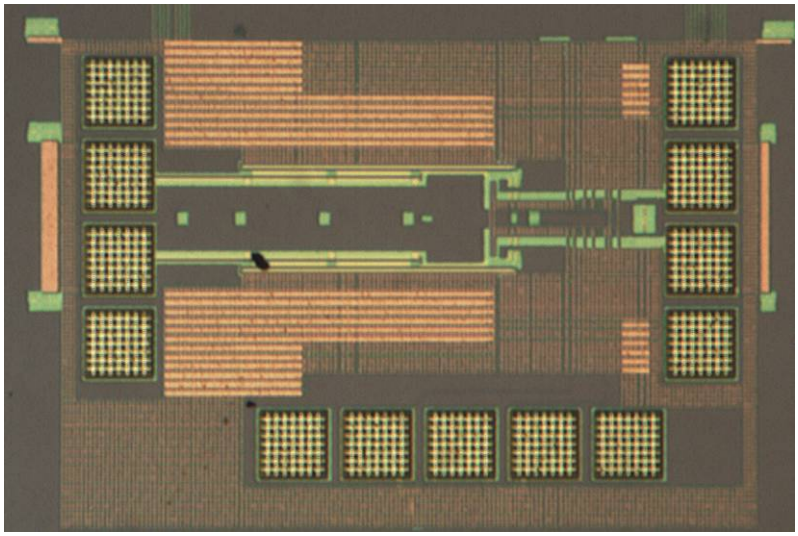


Figure 6.3 - Photograph of the Test Chip in 0.13μm CMOS

6.3 Test Setup

The test setup shown in Figure 6.4 was used to characterize the SHA described in previous sections. Microprobes were used to directly contact the clock, input, and

output signal lines to minimize contact inductance while biasing was provided through the test card to the chip.

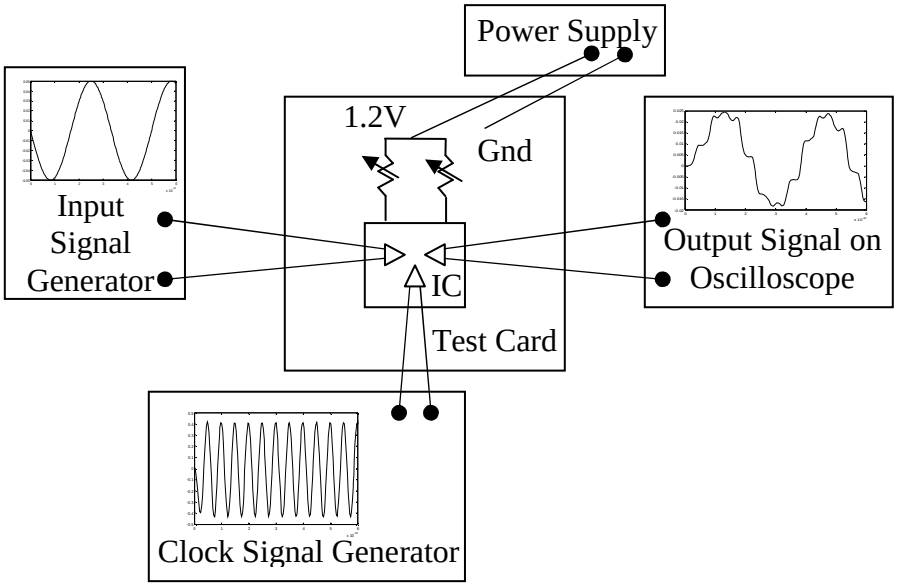


Figure 6.4 - Schematic of Test Setup

The circuit was fabricated in 0.13μm CMOS and packaged in an open cavity QFP package to allow probing of the high speed signal path. The high frequency signal path and the clock input path were terminated in differential probe pads with minimum metal to reduce parasitic capacitance. The chip was biased with a power supply of 1.2V drawing 59mA through a test board while three differential microwave probes provided connection for the high frequency input, output, and clock signals directly to the input pads of the chip, as shown. This configuration minimized the high frequency roll-off seen in traditionally packaged ICs due to the parasitic LC filter composed of the bond wire inductance and the pad capacitance.

Figure 6.5 shows the output frequency response of the fabricated circuit. The measurement was performed while the circuit was sampling the input signal by using an oscilloscope to determine the output amplitude of the signal over various input

frequencies. Proper evaluation requires the circuit be switching to maintain operation of transistors *M7* and *M8* in both saturation and triode region. If the circuit is evaluated while in track mode, the bandwidth will appear artificially low due to constant operation in the triode region. It is seen that the 3dB bandwidth of the circuit is 1.8GHz. This agrees with simulated data. The primary limitation to the bandwidth in simulation is the 50Ω output driver, which provides insufficient bandwidth to support operation beyond 1.8GHz.

The SFDR and the total harmonic distortion (THD) of the chip were taken differentially and the results are shown in Figure 6.6. A minimum value of 30dB SFDR was achieved, allowing up to 6 ENOB to be resolved from the output data.

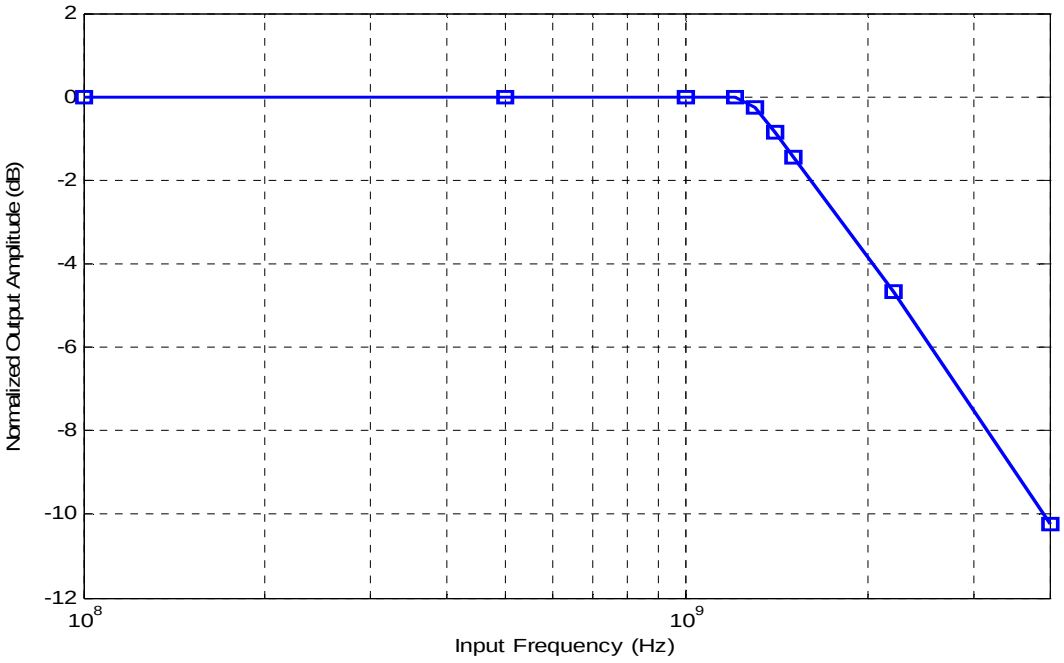


Figure 6.5 - Measured Output Frequency Response

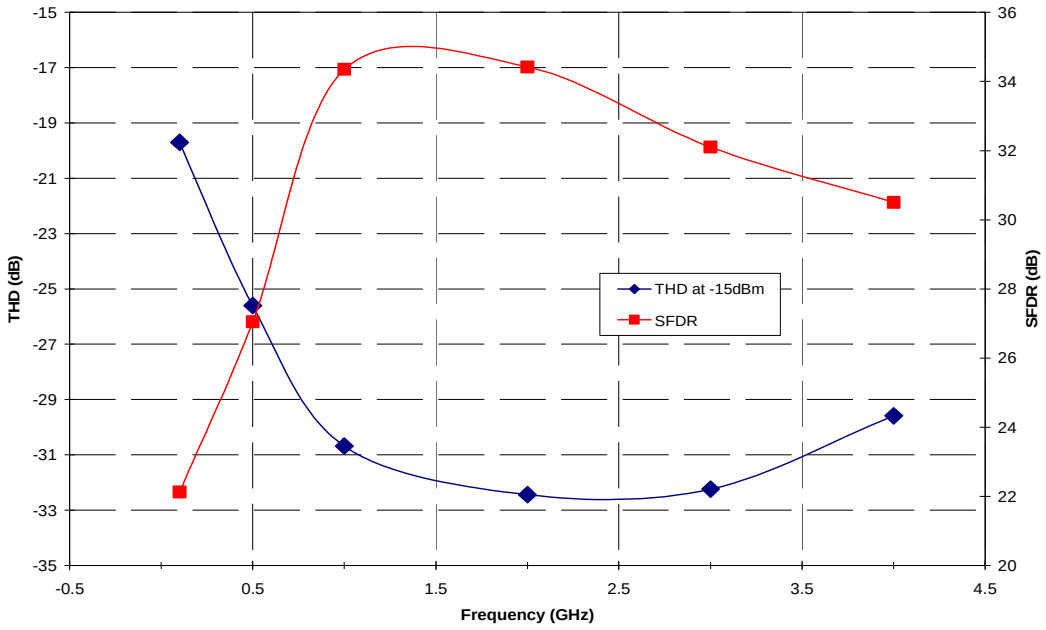


Figure 6.6 - Measured SFDR and THD of SHA Operating At 20GS/s

	[27]	[28]	[34]	This Work
Process	0.2µm AlGaAs/GaAs-HEMTs	0.18µm CMOS	0.13µm CMOS	0.13µm CMOS
Supply Voltage	-5V	1.8V and 3.3V	1.8V	1.2V
Sampling Rate	5GS/s	1.6GS/s	30GS/s	20GS/s
Bandwidth	3GHz	800MHz	7GHz	1.8GHz
Droop Rate at Sampling Speed	0.36mV		0.2mV	0.002mV
S11 from 100MHz to 13.5GHz			< -10dB	< -10dB
S22 from 0MHz to 13.5GHz			< -13dB	< -15dB
SFDR		> 62dB	> 32dB	> 30dB
THD	< -45dB	$\leq$ -60dB	< -29dB	< -29dB
Power Consumption	500mW	183mW	166mW	71mW
Area	0.63mm^2	0.12mm^2	1mm^2	0.09mm^2

Table 6.1 - Chip Dimensions and Power Usage

Table 6.1 lists the operation features of the circuit. The supply voltage is lower than previously reported multi-gigahertz SHA with low current draw. Total power consumption is 71mW from a 1.2V supply including reference currents and output buffer. The reference circuitry consumes 41mW, with the distributed amplifier, switched source follower and output buffer consuming 30mW. Input and output return loss were measured up to 13.5GHz. Due to the differential termination on the input, frequencies below 100MHz appear poorly matched to the two port 50Ω network analyzer. At frequencies between 100MHz and 13.5GHz, the input reflection coefficient is better than -10dB. On the output, a differential pair output driver terminated to the power terminal with 50Ω allows an output reflection coefficient of better than -15dB from DC to 13.5GHz. The transient output of the signal was measured at a low sampling frequency and hold value droop was found to be 7.7mV per 100ns, which translates to 0.002mV droop per held value at 20GS/s.

The active area of the chip occupies 0.09mm^2. The small area, high speed, and low voltage operation of this circuitry facilitates the design of multi-gigahertz THA, and by extension ADCs, using standard power supplies in existing CMOS processes.

Chapter 7 Analog-to-Digital Converter Architectures

7.1 Introduction

As previously discussed in Chapter 4, analog-to-digital converters (ADCs) frequently employ a sample-and-hold amplifier (SHA) or track-and-hold amplifier (THA) followed by a core ADC. Once the input signal has been sampled in an SHA, and occasionally without an SHA as seen in [35] and [36], the signal is fed to the core ADC.

The core ADC architectures are commonly categorized by speed and employ various methods to operate with lower power, higher speed, or a combination of both. High speed ADCs often incorporate aspects of multiple architectures to achieve desired operation speeds, effective number of bits (ENOB), area consumption, and power consumption. The fastest ADCs typically employ a flash architecture that may include an SHA similar to that shown in Figure 4.3. In addition to the flash architecture, an emerging area of interest in ADCs involves conversion of the input analog signal to the time domain with digitization performed on the time information using a TDC.

The flash architecture has been successfully implemented with up to eight bits of resolution at low speeds and five bits at sampling speeds up to 20GS/s [35]-[38]. Other high speed implementations have exploited a pipeline architecture where a smaller number of bits are resolved at each stage and the residual difference between the digital value and the analog value is amplified and converted in the next stage [39]. Folded architectures have also been examined [40], however this architecture suffers with

increased frequency of operation. The pipelined and folded architectures are outside the scope of this work and will not be discussed further. Section 7.2 discusses the operation and limitations of the basic flash architecture.

At lower speeds and/or lower data throughputs, time based analog-to-digital conversion has been explored [41]-[44]. Implementations have focused on low power, low resolution applications at relatively low speeds or with high pattern repetition rates. The fastest reported time based ADC is incorporated in a 70GHz sampling scope [41]. The input amplifier has a bandwidth of 70GHz and can resolve signals operating at this speed, however far fewer than 70 Giga-samples per second are taken, making the successful reconstruction of a signal dependent on a large number of repetitions of a given signal. This architecture is useful for measurement of signals with a repeating pattern, but is not generally usable for systems requiring data recovery. Other designs have focused on the implementation of a digitally compatible ADC [42] and the linearity of phase modulation [43]-[44]. The implications and operation of some of these architectures are further explored in section 7.3.

7.2 Flash Architecture

The flash ADC is a well known and commonly used architecture. Figure 7.1 shows an N bit flash ADC. The analog input may be driven by the output of an SHA or the output of a signal buffer. As may be seen in the figure, the number of comparators in a flash architecture grows as 2^N where N is the number of bits to be resolved. This results in a sharply increasing load at the analog input as N increases, which may cause significant speed limitations. It also results in a significant increase in required chip

area and power consumption. These factors effectively limit the maximum effective number of bits (ENOB) in a standard flash architecture to approximately eight.

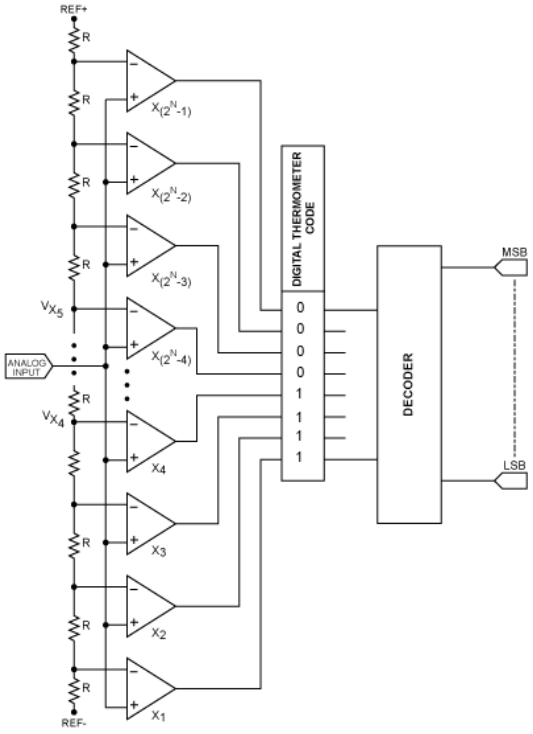


Figure 7.1 - N Bit ADC Design

A flash ADC operates by comparing the input signal to 2^N reference voltages simultaneously. The circuit in Figure 7.1 generates the reference voltages with a resistor string tied to REF+ at the top of the stack and REF- at the bottom to provide one side of a comparator with a signal while the other side is driven with the input signal. At the output of the comparators, a "1" or "0" digital value is output in thermometer code. This signal is typically converted to binary and fed to the digital system for further use. From a latency standpoint, a flash ADC is attractive because the conversion from analog-to-digital is complete in one clock cycle, however the exponential increase in comparators with number of bits may cause speed degradation due to the large load

imposed on the analog input signal and consequently limit the maximum input operating frequency.

From a theoretical standpoint, an ADC operating at the maximum input frequency of one half the sampling frequency, or the Nyquist frequency, is limited in three ways: thermal noise, aperture jitter, and ambiguity [1]. For systems resolving eight bits or less, the thermal noise limitation is irrelevant, leaving the aperture jitter and ambiguity limits. Aperture jitter limits performance of the ADC due to the imprecision of the sample time. In the worst case, the input signal is operating at half the speed of the sampling signal with an rms error voltage of

$$v_{rms} = \pi f_{clk} A \sigma_{clk} / 2 \tag{7.2.1}$$

where f_{clk} is the sampling frequency of the ADC, A is the full scale amplitude of the input signal, and σ_{clk} is the sampling jitter of the clock. Assuming an even distribution of voltage bins across the full input range, the quantization noise voltage is given by

$$\left\langle v_Q^2 \right\rangle = \frac{A^2}{12 * 2^{2Baperature}} \tag{7.2.2}$$

where $B_{aperature}$ is the ENOB that can be resolved. Taking the square root of (7.2.2), setting it equal to (7.2.1), and solving for $B_{aperature}$ results in the expression [1]

$$B_{aperature} = \log_2\left(\frac{1}{\sqrt{3}\pi f_{clk}\sigma_{clk}}\right). \tag{7.2.3}$$

Ambiguity in comparators due to the finite settling speed of comparators in a given process limits the ENOB when sampling speeds approach the unity gain

frequency of a process. From [1], the ENOB limit due to ambiguity has been found to be

$$B_{ambiguity} = \frac{\pi f_T}{6.93 f_{clk}} - 1.1. \tag{7.2.4}$$

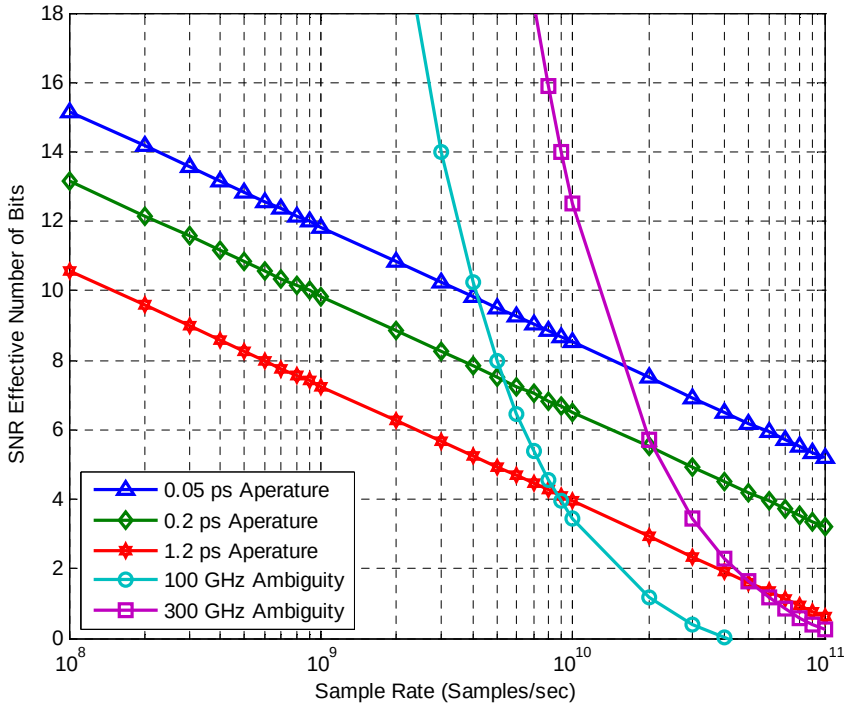


Figure 7.2 - ENOB Aperature and Ambiguity Limit

Equations (7.2.3) and (7.2.4) are plotted over frequency for different values of jitter and unity gain frequency, respectively, in Figure 7.2. It may be seen that high speed systems with sampling rates in excess of a few gigahertz are severely limited by these factors. For systems that require high resolution and high speed, this poses a significant challenge.

Experimentally, the ENOB of a system are calculated using the measured signal-to-noise ration (SNR) and spurious free dynamic range (SFDR) of the system. From [1], the calculated ENOB of a system using the SNR is

$$ENOB = \frac{SNR(dB) - 1.76}{6.02} \tag{7.2.5}$$

while the ENOB using the SFDR of the system is

$$ENOB = \frac{SFDR(dB)}{6.02}. \tag{7.2.6}$$

7.3 Time Based Architecture

Some papers [41]-[44] have investigated employing sampling in the time domain for low power and moderate frequency applications. These papers have used active devices to create a voltage to time conversion. The fastest operation is achieved by [41] at 70GHz, with the block diagram shown in Figure 7.3, however the throughput of this architecture limits the application to situations with a repeating input signal, such as in test and measurement.

The block diagram shows the input signal at "Nodes of the Analog CUT", where CUT is circuit under test, is sampled for a small portion of a clock cycle with a slowly varying reference time frame. At the blocks labeled DVCD, or differential voltage controlled delay, the input voltage is converted to a time term. From here the time difference is amplified with a time amplifier and then converted to a digital signal using a TDC as shown in Figure 7.4.

This work focuses on instrumentation and repeating signals. As a result, the throughput of this ADC is much lower than the full sampling signal would indicate. The stated application is a sampling oscilloscope, which will rely on a repeating input signal, thus limiting the applications this is appropriate for.

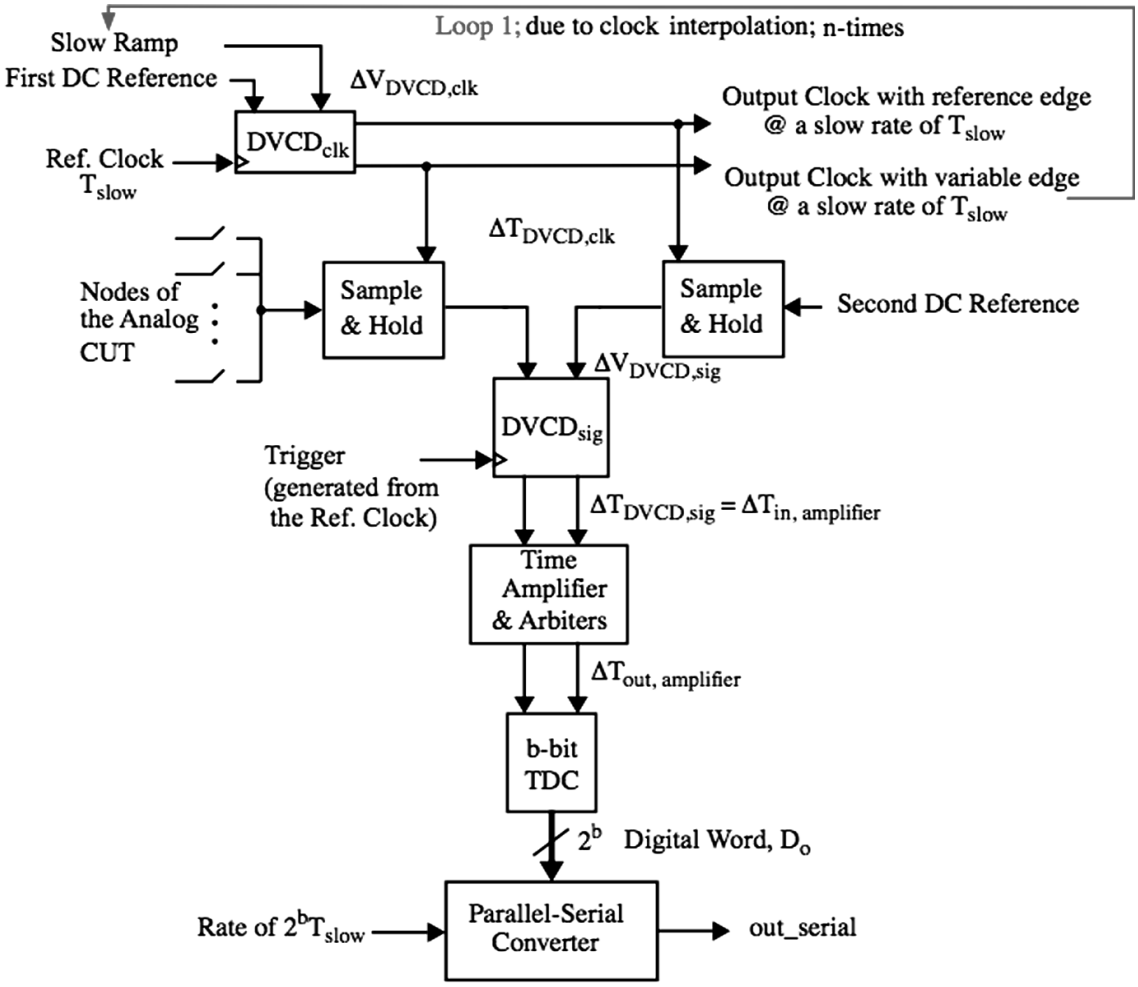


Figure 7.3 - Oscilloscope Time Based ADC Architecture [41]

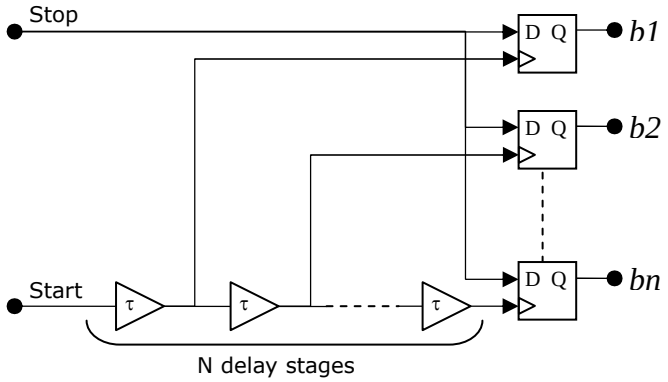


Figure 7.4 - N-bit Time-to-Digital Converter

Other papers have investigated time based ADCs for ease of implementation in a predominantly digital process [42]. By using the input voltage to modulate the supply voltage of an inverter chain, the delay of a signal through the chain varies. This circuit has the advantage of employing all digital subcomponents, however the linearity of the voltage to phase conversion is quite poor, making significant calibration necessary at high speeds. Operation was tested up to 1MHz with 7 bits of linearity, while at 10kHz the ADC operated with 14 bits of linearity.

Two additional papers have investigated the conversion of input voltage to a linear phase modulation on a pulse [43]-[44]. These papers show voltage to phase conversion linearity of up to 6 bits at speeds up to 1.8GHz [43] and 6 bits at speeds up to 300MHz [44]. The primary contribution of these designs is the linearity discussion of the voltage to phase conversions. This is important in determining the expected ENOB of a time based ADC.

The architecture described in [44] presents an interesting implementation of a time based architecture. A block diagram of the structure is shown in Figure 7.5 below. The input voltage signal, Vin, is first sampled in an SHA with the output sent to the differential block labeled voltage-controlled variable-delay transmission line. From here, the signals are sent to a Venier line TDC, as seen in Figure 3.2, where the delay is converted to a thermometer code representation of the input signal. One significant aspect of this design is that the Pulse signal is used to generate both the Start and Stop signal to the TDC. This dual use simplifies timing considerations for the circuit. A slightly misleading aspect of the diagram shown is the labeling of the blocks with the

term "transmission line." The delay is generated with active devices, as may be seen in Figure 7.6, and not using a periodically loaded transmission line.

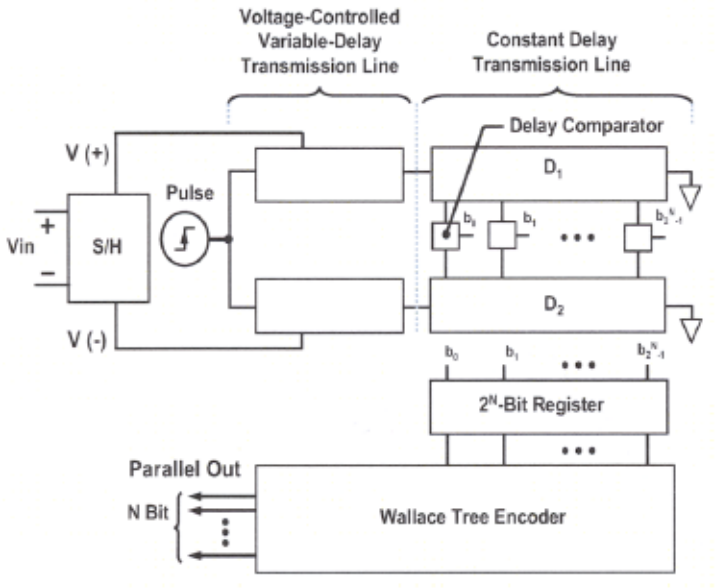


Figure 7.5 - Highly Linear 300MHz Time Based ADC Architecture [44]

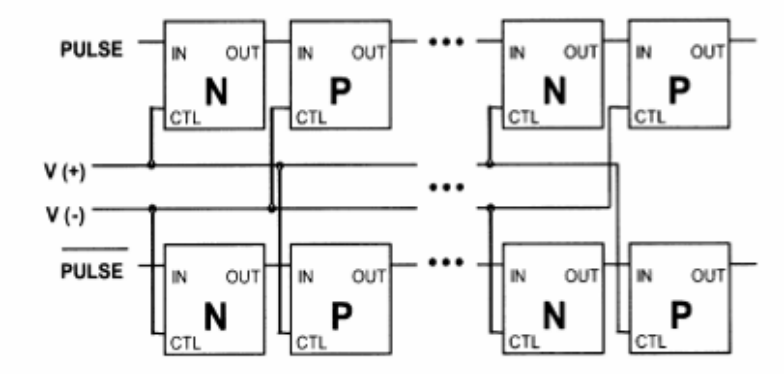


Figure 7.6 - Delay "Transmission Line" Block Diagram [44]

Chapter 8 Proposed Analog-to-Digital Converter Analysis and Simulation

8.1 Introduction

An alternative analog-to-digital converter architecture is proposed that exploits the strengths of microwave design techniques and integrated circuit design compactness. The following sections describe the analytical and modeled operation of the architecture. In Section 8.1, the operation of the proposed circuit is described and analyzed. Section 8.2 presents simulation results of the periodically loaded transmission line, followed by Section 8.3 with simulations of the time-to-digital converter and finally Section 8.4 discusses the system simulations.

8.2 Operation of Circuit

The proposed architecture is shown in Figure 8.1 in which a clock signal is split in-phase and fed to two phase variable delay stages. The phase of the clock line is modulated proportional to the input voltage V_{inn} on one path and V_{inp} on the other. These signals are fed to a TDC and the output digital word is a representation of the input voltage.

The signal at point *b* in Figure 8.1 is sampled at multiple delay intervals, as can be seen in the schematic of the TDC shown in Figure 8.2. A timing diagram for one comparator in the TDC is shown in Figure 8.3. From the timing diagram, it is seen that if the zero crossing of the falling edge of the modulated signal, *Clkb*, occurs before the falling edge of the signal *Clka*, the flip-flop outputs a logic 0. If the falling edge of *Clka*

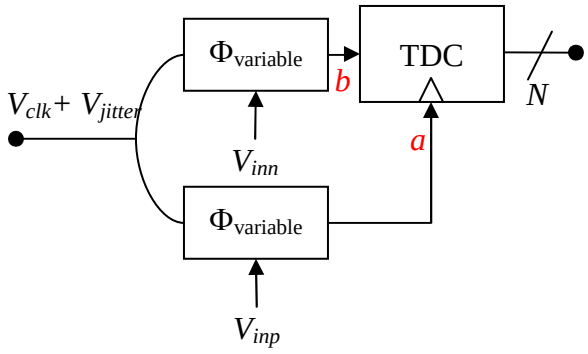


Figure 8.1 - Proposed ADC Architecture

crosses zero before the falling edge of *Clkb*, the flip-flop outputs a logic 1. Each section of transmission line in Figure 8.2 provides delay to the *Clkb* signal. This allows the magnitude of delay to be represented as a discrete value with the least significant bit (LSB) of the TDC equal to the minimum time spacing between making each flip-flop. The output of the TDC is a digital thermometer code of length 2^N where N in the number of bits.

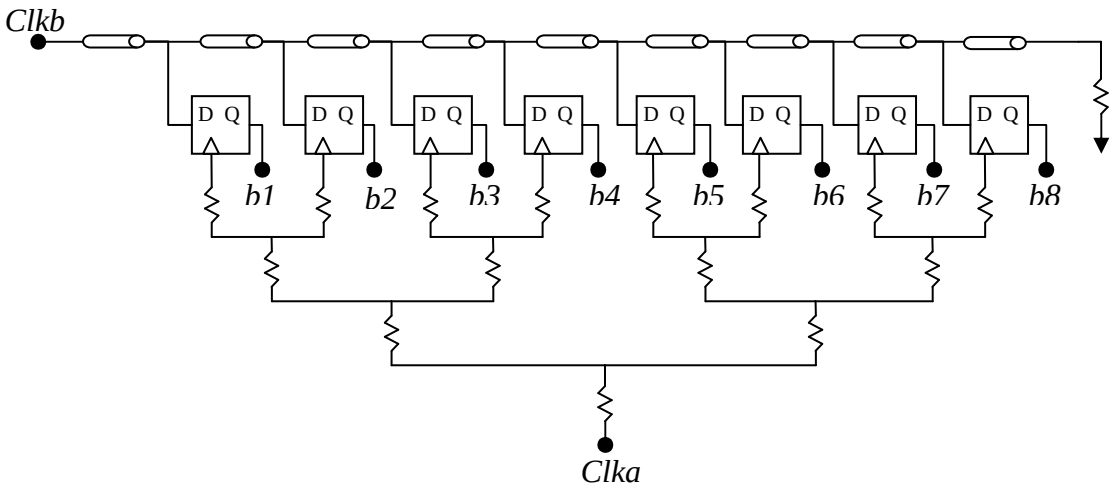


Figure 8.2 - Schematic of 3 Bit TDC Design

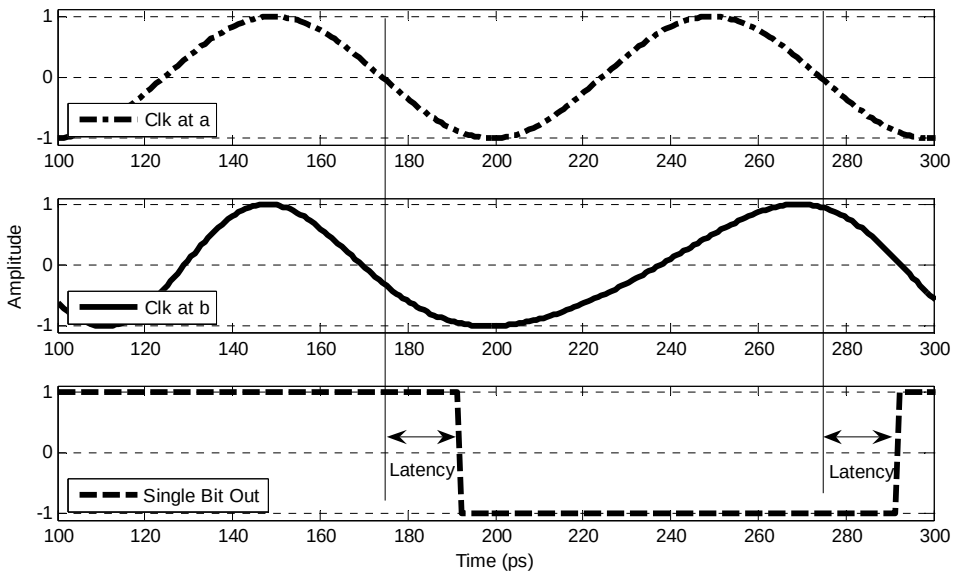


Figure 8.3 - Timing of TDC Signals

If the same clock is split and one branch is used for the time delay input of the TDC while the other is used for sampling, as in Figure 8.1, then the impact of clock jitter is reduced due to correlation of the signal, allowing for improved ADC performance. The conversion of input voltage to phase delay may be modelled as a phase modulation of a carrier signal. Assuming a modulation signal of depth β radians and signal frequency ω_s, a clock with amplitude A and frequency ω_{clk}, and phase noise Δt, the signal at point *b* of Figure 8.1 is

$$V_b(t) = A\cos[\omega_{clk}(t + \Delta t) + \beta\cos(\omega_s t)]. \tag{8.1.1}$$

For the purposes of analysis, the signal at point *a* is calculated as a non-modulated clock signal of the form

$$V_a(t) = A\cos[\omega_{clk}(t + \Delta t)]. \tag{8.1.2}$$

The clock samples V_b(t) when V_a(t) is equal to zero. This results in a sampling time of

$$t_{samp} = \frac{\pi(4n+1)}{2\omega_{clk}} - \Delta t \tag{8.1.3}$$

where *n* is an integer. Substituting this expression into (8.1.1) results in

$$V_{bSamp}(n) = \sin\left(\beta \sin\left(\frac{\omega_s \pi(4n+1)}{2\omega_{clk}} - \omega_s \Delta t\right)\right). \tag{8.1.4}$$

From Figure 8.2, it is seen that each comparator of the TDC receives a delayed signal from the stage previous. Each delay is equal to $2\beta/2^N$, where N is the number of bits to be resolved, and the comparator outputs a "1" if the delayed value of V_{bSamp} is greater than zero and a "0" if it is less than zero. The digital output of the TDC is in thermometer code which allows an analog statement of the digital value as the sum of the ones and zeroes output from the comparators. Mathematically, this is stated as

$$V_{out}(k) = \sum_{b=0}^{2^N-1} dig\left(A\sin\left[-\beta + \frac{2b\beta}{2^N} + \beta \sin\left(\frac{\pi\omega_s(1+4k)}{2\omega_{clk}} - \omega_s \Delta t\right)\right]\right) \tag{8.1.5}$$

where *dig* is used to indicate the conversion of the voltage value for each value of *b* to a "1" or "0".

The conversion of the time delay to a digital value relies on the difference in arrival times of the input signal and the sampling clock. To determine the limitation due to quantization on ENOB, the time signal information must be considered. At a given sampling instant, the time is

$$t_{sig} = \frac{\beta}{\omega_{clk}} \sin\left(\frac{\omega_s \pi(4n+1)}{2\omega_{clk}} - \omega_s \Delta t\right) \tag{8.1.6}$$

The worst case error due to noise may be found as the derivative with respect to time of (8.1.6) multiplied by the time error, resulting in

$$t_{rms} = \frac{\beta\omega_s \tau}{\omega_{clk}} = \frac{\beta\tau}{2} \tag{8.1.7}$$

where τ is the standard deviation of the phase noise and assuming ω_s is half the frequency of the clock signal.

Digital output error for this system is due to timing error as a result of jitter. The ADC equations in [1] assume the signal error is due to the sampled voltage error caused by jitter, but due to the different sampling method, the limitation on effective number of bits (ENOB) due to jitter requires to be restated. Assuming perfect conversion of the input signal to delay and an even distribution of timing bin sizes, the quantization error in time is [1]

$$\left\langle t_Q{}^2 \right\rangle = \frac{Q^2}{12} \tag{8.1.8}$$

where Q is defined as

$$Q = \frac{2\beta}{\omega_{clk} 2^B}. \tag{8.1.9}$$

with B the maximum achievable ENOB. Substituting (8.1.9) into (8.1.8), setting (8.1.7) equal to the square root of this expression, and solving for B results in

$$B_{aperature} = \log_2\left(\frac{T_{clk}}{\pi\sqrt{3}\tau}\right) = \log_2\left(\frac{1}{\pi\sqrt{3} f_{clk}\tau}\right). \tag{8.1.10}$$

This is equivalent to the achievable ENOB in a traditional voltage based ADC for a jitter limited system.

In addition to the performance of the circuit with respect to quantization, the phase modulation of the signal produces multiple harmonics of the combination of the signal and the clock. These harmonics will limit the attainable spur free dynamic range (SFDR) of the system and may be examined using a Bessel expansion of (8.1.5). This equates to

$$V_b(k) = \sum_{n=-\infty}^{\infty} \sum_{b=0}^{2^N-1} dig\left(J_n(\beta) A \cos\left[\frac{\pi}{2} - \beta + \frac{2b\beta}{2^N} - n\left(\frac{\pi f_s (1+4k)}{2 f_{clk}} \right) \right] \right). \quad (8.1.11)$$

Sampling this signal produces multiple copies of each frequency. By taking the sampled frequency transform of (8.1.11), the frequency representation may be stated as

$$V_b(f_d) = \sum_{n=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} J_n(\beta) \frac{A}{2} \left[\delta\left(f_d - (k+1) f_{clk} - n f_s \right) + \delta\left(f_d - (k-1) f_{clk} + n f_s \right) \right]. \quad (8.1.12)$$

This equation represents the frequency information in *Clkb*. By subtracting the frequency information from the unmodulated clock, an impulse function at f_{clk}, this may be used to determine the theoretical maximum SFDR of the signal as

$$SFDR(dB) = 20 \log_{10} \left(\frac{3 J_1(\beta)}{J_2(\beta)} \right). \quad (8.1.13)$$

This indicates that large modulation of the phase, or large values of β, will result in a reduced SFDR, limiting the ENOB of the output signal.

A differentially driven signal in the system where *Clka* in Figure 8.2 is 180 degrees apart from *Clkb* results in a signal that may be stated as

$$V_a(t) = A \cos[\omega_{clk}(t + \Delta t) - \beta \cos(\omega_s t)]. \quad (8.1.14)$$

where the variables have been previously described for (8.1.1). The frequency representation of this signal may be stated as

$$V_a(f_d) = \sum_{n=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} J_n(\beta) \frac{A}{2} \left[\delta\left(f_d - (k+1) f_{clk} + n f_s \right) + \delta\left(f_d - (k-1) f_{clk} - n f_s \right) \right]. \quad (8.1.15)$$

Subtracting (8.1.15) from (8.1.12) reveals the theoretical maximum SFDR for a differential signal to be

$$SFDR(dB) = 20 \log_{10} \left(\frac{J_1(\beta)}{J_3(\beta)} \right). \quad (8.1.16)$$

which is better than for the single ended case, but still provides a limit on the attainable SFDR for this system.

8.3 System Simulations

The analog-to-digital converter was simulated with multiple tools to accurately analyze significant aspects of the system. Design was simulated in Matlab's Simulink and Agilent's ADS to evaluate the limitations of the system.

Simulation was performed in Simulink for mathematical modeling of the ADC. Figure 8.4 shows the Simulink model for a three bit time based ADC and Figure 8.5 shows the model for an individual flip-flop in the system. For analysis purposes, the outputs of the flip-flops were summed to create an analog representation of the digital signal to aid in measurement of signal to noise ratio (SNR), spurious free dynamic range (SFDR), differential non-linearity (DNL), and integral non-linearity (INL).

The results of the modeling confirm the ENOB calculations in previous sections. Jitter was injected to the system and the SNR of the resultant output was calculated. These results were used to determine the ENOB of the system and compared to the expected ENOB based on (8.1.10). Modeling was performed with systems up to six bits. At this point, timing granularity limited further modeling due to necessary simulation time and time spacing of the fixed delays, which are defined as $2\beta/(\omega_{clk}2^N)$ and scales as a function of the number of bits to be resolved.

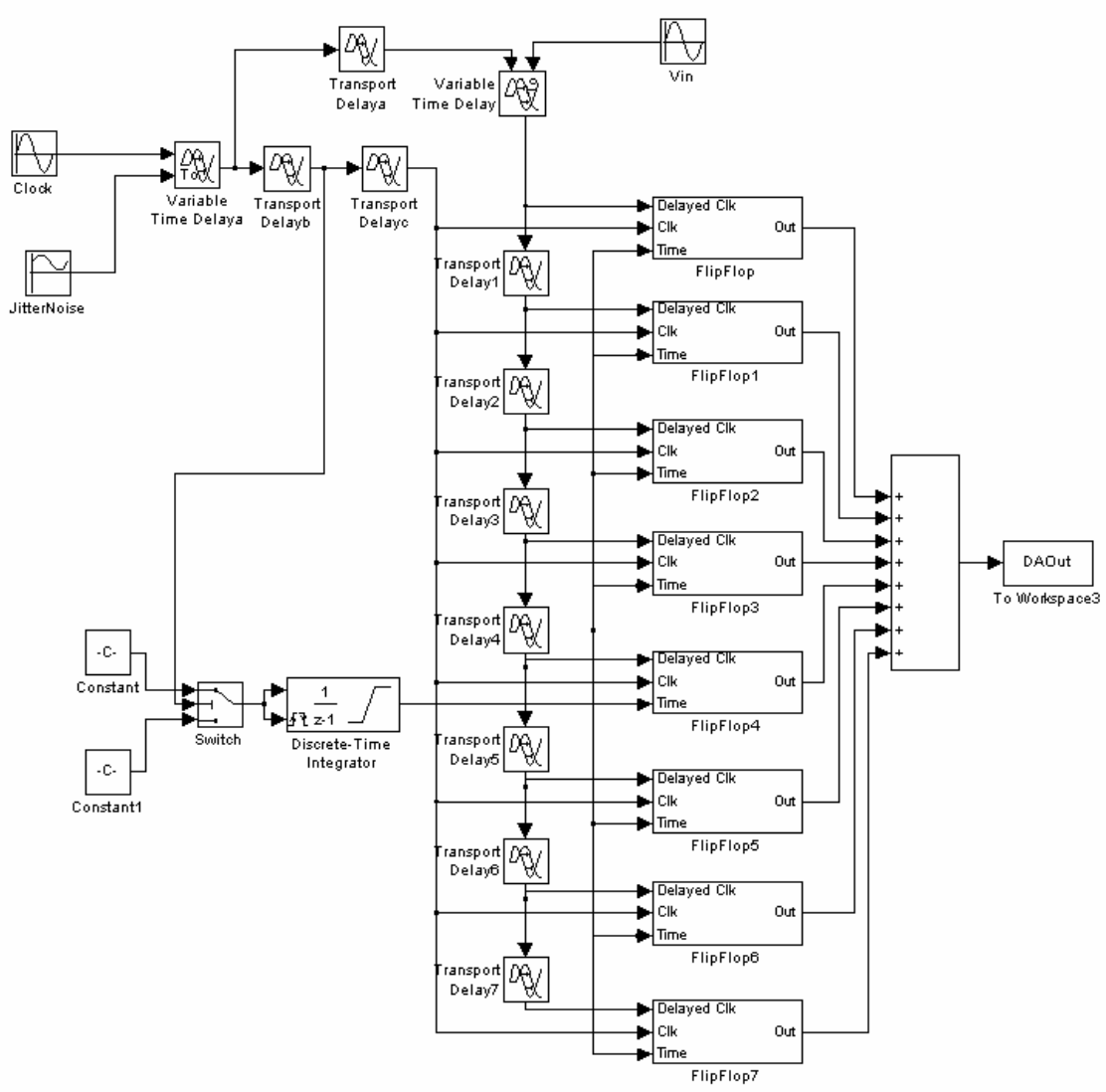


Figure 8.4 - Simulink Model of Time Based ADC

It was decided to design the system at the printed circuit board level using Agilent's ADS. The design of the periodically loaded variable delay transmission line required transmission line modeling and SPICE models of the components to be used. Specific device choices and geometries are discussed in Chapter 8. Simulations indicated up to 400ps of delay would be generated with the design structure. Comparisons of simulation to hardware may be seen in Section 8.3. The model

included package models of all devices and transmission line models of the proposed board design.

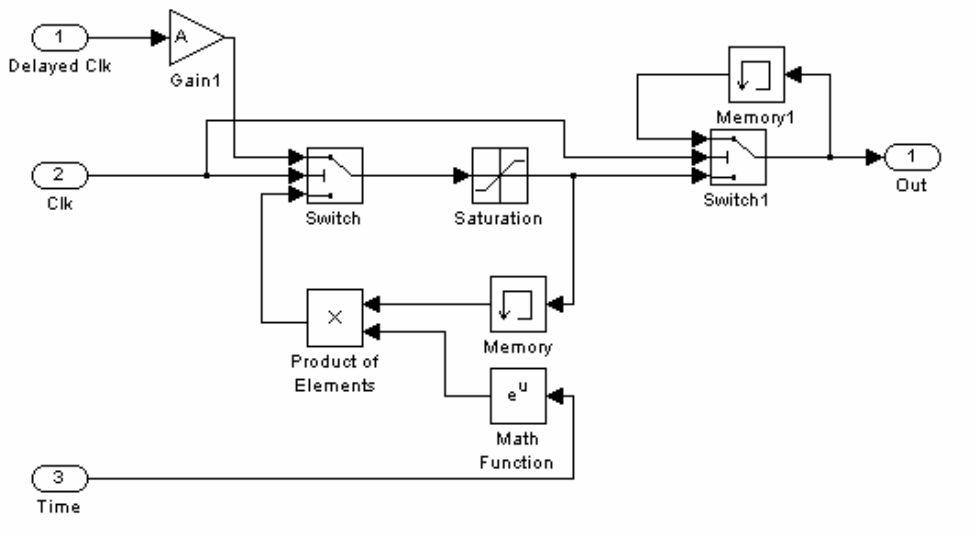


Figure 8.5 - Flip Flop Model for Use in Simulink Simulations

8.4 Transmission Line Simulations

The first section of the architecture described is a phase delay proportional to V_{in} and one way of generating this delay is shown in Figure 8.6. Varactors are used to provide variable capacitance periodically on a transmission line and adjust the delay, τ, where τ is

$$\tau = \sqrt{LC_{tot}} \tag{8.3.1}$$

L is the inductance of a section of the line, and C_{tot} is the total capacitance per section. Impedance of the line is

$$Z_{line} \cong \sqrt{L/C_{tot}} \ . \tag{8.3.2}$$

The cut-off frequency of the artificial line may be calculated as

$$\omega_c = 2/\sqrt{LC_{tot}} \tag{8.3.3}$$

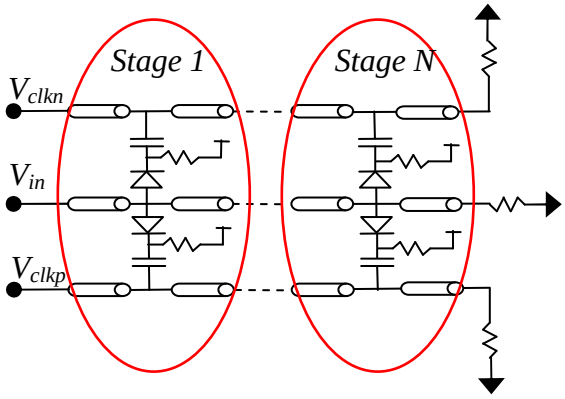


Figure 8.6 - Schematic of Phase Delay Transmission Line

Equations (8.3.1)-(8.3.3) imply a limit on the range of L and C_{tot}. For low return loss and high transmitted power through a transmission line, it is important to match the impedance of the line within plus and minus ten percent. This limits the amount of delay that can be generated per stage while (8.3.3) limits the maximum LC_{tot} product for operation at a given frequency.

To accommodate these constraints and generate sufficient phase delay, an artificial transmission line was constructed with multiple stages. This increased transmitted loss slightly, but allowed a good impedance match with large delay generation. For appropriate phase modulation and high V_{in} bandwidth, it was also necessary to modulate the clock lines with a well matched transmission line.

A delay line as shown in Figure 8.6 was designed and simulated for operation up to 900MHz. Instead of terminating in resistors, the V_{clkn} and V_{clkp} lines were split with resistive power dividers and the outputs of the power divider were simulated and measured. The results may be seen in Figure 8.7 for the nominal biasing condition of zero differential delay. Simulated values are approximately equal to measured values and indicate the loss and transmission are as expected. To ensure appropriate operation,

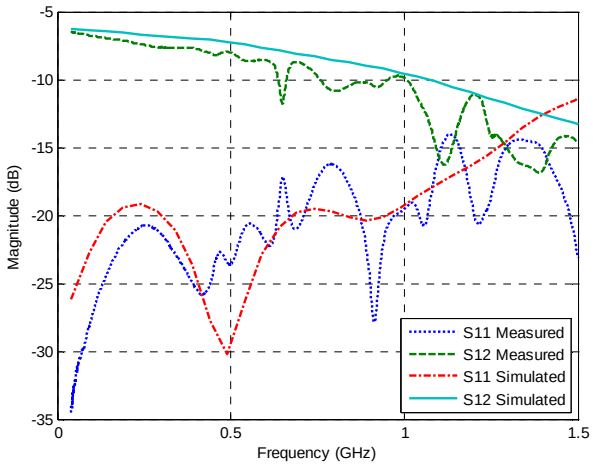


Figure 8.7 - S-Parameter Simulated and Measured Values from V_{clk} to *a*

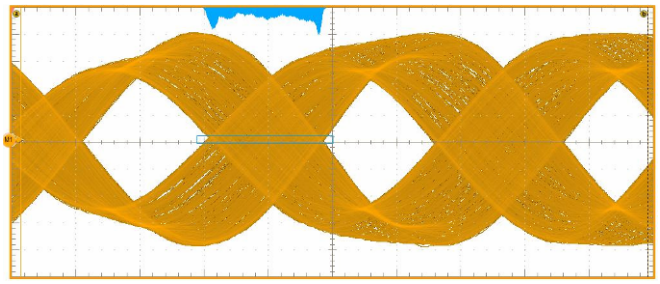


Figure 8.8 - Maximum Phase Modulation of 700MHz Clock Measured at *a-b*

the delay sections were designed to maintain less than -10dB return loss and no more than 3dB signal loss over the frequency band. Due to the power splitter, the signal was reduced by an additional 3dB.

Phase delay measurements were also made, the line was designed to deliver a maximum of 400 ps delay. To examine the phase delay, it is helpful to examine an eye diagram of the output signal, as in Figure 8.8. This plot shows a 700MHz clock signal modulated with β equal to $\pi/4$. The output of the signal contains 380ps of phase variation when V_{in} is modulated with a 2Vpp signal.

8.5 Time-to-Digital Converter Simulations

To design a fast TDC with minimal time spacing, the latch line requires a constant phase, zero differential phase distribution network and the delay line requires a linear phase delay with no active devices.

The architecture used was previously shown in Figure 8.2. Due to limitations in the comparators used for the circuit, it was necessary to split the clock to avoid impedance mismatch. A resistive power splitter was found to possess the best phase performance and was designed to split the clock eight ways with less than 1ps group delay difference between adjacent clock lines.

As with a distributed amplifier, active circuits may be evenly distributed along a transmission line. The arrival time of the wave at each input is calculated as

$$V(n) = V_0 e^{-\alpha n} e^{-j\beta n} \tag{8.4.1}$$

where n is the stage number, V_0 is the initial input voltage, α is the loss per section of line, and β is the propagation constant per section of line. Assuming the line is low loss and β is due primarily to the inductance of the transmission line segment and the capacitance of the circuit, the delay per section is approximately equal to $\tau=\text{sqrt}(LC_{tot})$, where C_{tot} is the input capacitance of the comparator.

Physical limitations at the board level require spacing between terminations of the comparators be 6mm or longer. The minimum spacing on the transmission line fixes the amount of inductance possible per section while the input capacitance is fixed by the devices available. These factors combine to limit the delay spacing to a minimum of 35ps.

The line width of the microstrip transmission line on the board is designed based on the minimum allowable length and on the input capacitance of the comparators. To optimize circuit performance, the line is designed for 50Ω impedance. Using this topology, a good match is maintained over all frequencies with small delay spacing.

Chapter 9 Analog-to-Digital Converter Experimental Results

9.1 Introduction

To verify the operation of the proposed time based ADC, a hardware implementation was designed and built. The results are presented in the following section.

9.2 Analog-to-Digital Converter

The time based ADC discussed in Chapter 7 was implemented on a printed circuit board (PCB). Testing was performed to verify predicted operation. To ensure appropriate phase modulation operation and to facilitate jitter generation, an additional phase modulation section was designed and incorporated as a first stage for the test

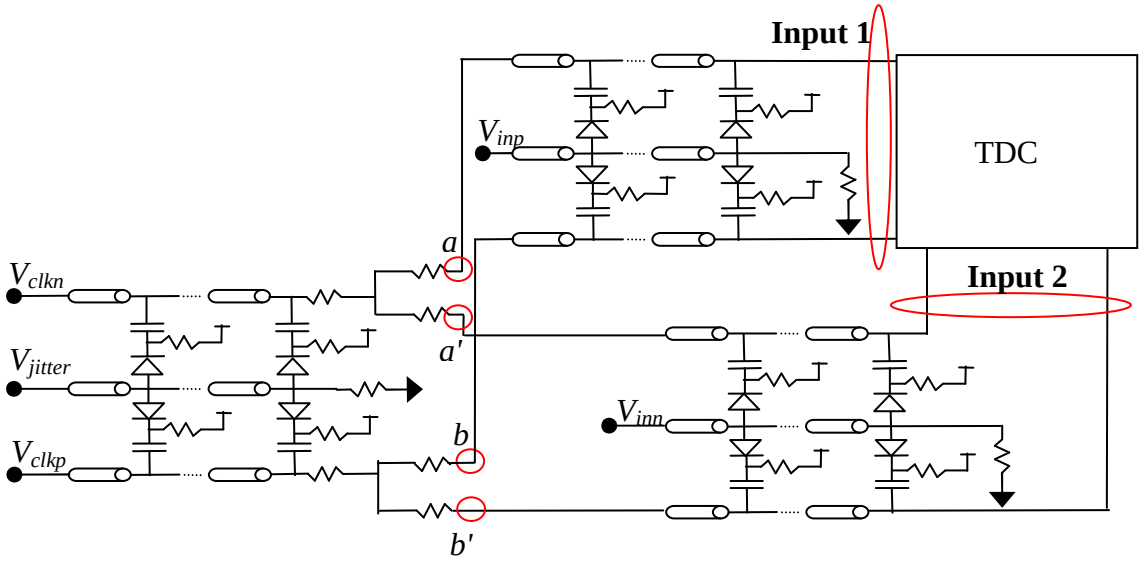


Figure 9.1 - Schematic of Board Design

board, as seen in Figure 9.1. Phase modulation testing was performed using this section of transmission line. This line was then used to drive the phase modulation sections of the time based ADC. The TDC was designed and implemented as outlined in Figure 8.2. Test results indicate good linearity and operation in high jitter environments.

9.2.1 Circuit Design

The architecture described in Figure 8.2 and 9.1 was implemented for a 50Ω, differential system with discrete components. The delay sections shown in Figure 9.1 are composed of multiple stages, as seen in Figure 8.6. Each stage was implemented with two 2pF blocking capacitors, two 5.1kΩ biasing resistors, and two Skyworks SMV1247-079LF varactors with capacitance range of 0.7pF to 6.5pF. Nineteen sections per delay stage were used with spacing of 5mm between stages on a 0.3mm wide microstrip transmission line 0.3mm above the ground plane. At the output of the first delay section, two resistive splitters are used to split V_{clkn} and V_{clkp}. The splitters were produced using three 16Ω resistors in a "T" configuration, as seen in Figure 9.1. From the splitters, each signal traveled through another nineteen section delay stage. The differential clock signal at Input 2 is fed to the input labeled V_{clk} in Figure 8.2 while the signal at Input 1 is fed to the $V_{clk+mod}$ input. At Input 1, the clock is distributed by a tree of 16Ω "T" configuration splitters, shown for a single line in Figure 8.2. Input 2 requires 50Ω impedance be maintained along the transmission line. This is accomplished using a transmission line with width of 0.25mm, a coupling capacitor of 0.5pF between the Analog Devices ADCMP572 comparator and the transmission line,

and spacing between comparators of 6mm. This creates delay between stages of the TDC equal to 35ps.

9.2.2 Test Setup

The design shown in Figure 9.1 was implemented and the PCB may be seen in Figure 9.2 below. All sections were implemented differentially for increased common mode rejection.

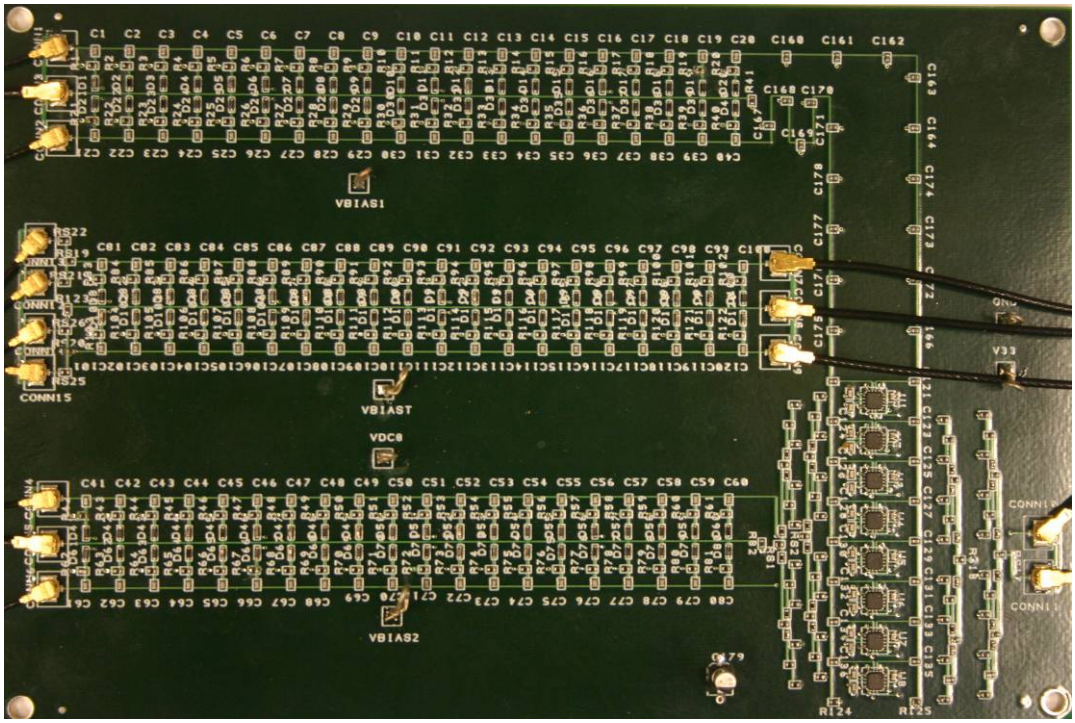


Figure 9.2 - Photograph of Board Implementation of Time Based ADC

To characterize the phase modulation path, the connections at point *a*, *a'*, *b*, and *b'* were made through contacts that could be connected to the subsequent sections or directly to test equipment. The clock is introduced to the circuit at V_{clkn} and V_{clkp}, and is phase modulated by applying a pseudo-jitter voltage at V_{jitter}. The clock signal is next split to points *a* and *a'* and *b* and *b'*. At these points the output clock signal was

examined and characterized to determine phase modulation characteristics. Additional testing involved feeding these signals to subsequent sections for quantization of the signal.

When a pseudo-jitter signal was introduced at V_{jitter}, the input clock was phase modulated, resulting in artificial jitter on the clock at points *a*, *a'*, *b*, and *b'*. From the split, the clock was modulated with true and complement signals V_{inp} and V_{inn} before reaching the TDC. After phase modulation, the clock at Input 1 was fed to the delayed side of the TDC. This signal was compared to the reference clock signal generated from Input 2, which was fed to the power splitter. The digital outputs were then converted back to the analog domain using a higher resolution digital to analog converter to facilitate testing and data analysis.

To test the ADC with jitter injected on the clock line, V_{jitter} signal created the jitter. Actual jitter is likely to be white in nature, but due to testing limitations, a 100MHz sinusoidal signal was used as a noise source. A diagram of the zero voltage crossings normalized to the mean clock frequency is shown in Figure 9.3. It is seen that the signal displays large levels of deviation from the expected crossing time, resulting in 98ps of average jitter. The power spectral density (PSD) of the clock with the pseudo 100 MHz jitter at *a-b* is shown in Figure 9.4. The sampling clock signal is at 900MHz with side lobes present every 100MHz. Due to the modulation depth, which is equal to a β of 0.25π, multiple side lobes are present in the frequency spectrum following the traditional Bessel function form.

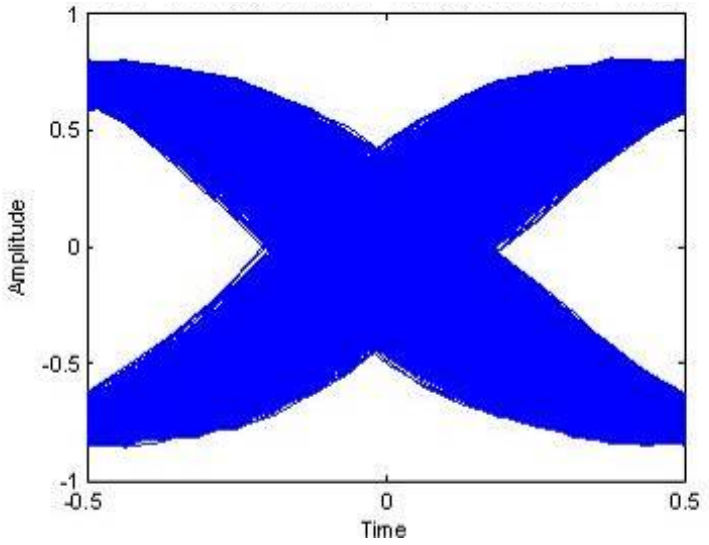


Figure 9.3 - 900MHz Clock Jitter

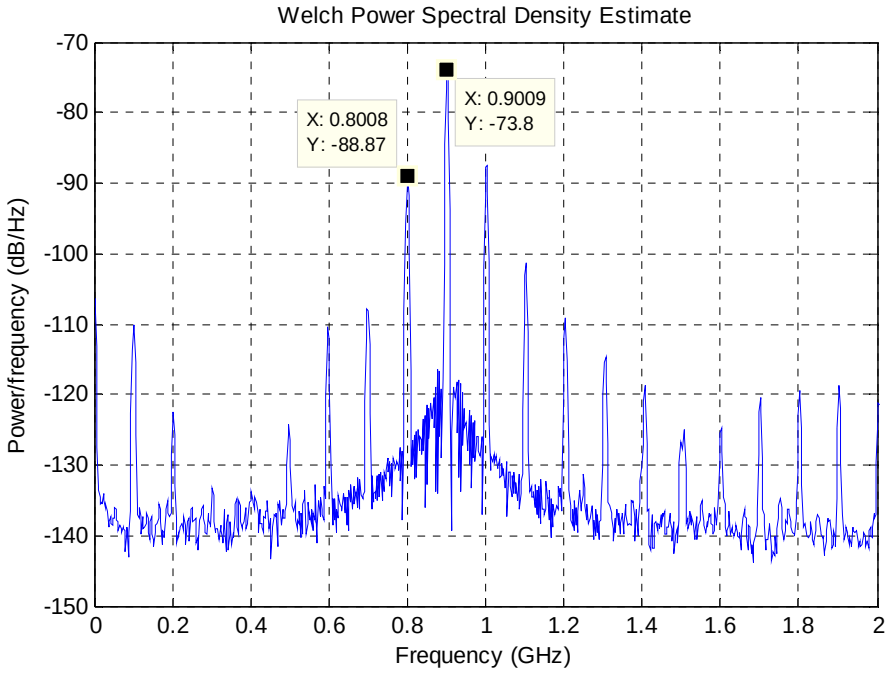


Figure 9.4 - 900 MHz Noisy Clock Spectral Density Analysis

9.2.3 Results

A clock with frequency of 900MHz was used to drive the ADC. The resultant output signal was analyzed for the effective number of bits (ENOB) resolved in the circuit. Results were obtained with and without the addition of clock jitter.

A 900MHz low noise clock was introduced to the ADC and then modulated with a sinusoidal input signal at 449MHz, 2Vpp. There was no jitter signal in these measurements. The digital output signal was analyzed in the frequency domain and the results are shown in Figure 9.5. As may be seen, the difference between the fundamental signal at 449MHz and the harmonic at 1MHz is 15.6dB, which corresponds to an SFDR ENOB of 2.6. The harmonic present at 1MHz is theoretically expected due to a depth of modulation equal to 0.25π. Smaller modulation depth of the phase modulation will reduce this effect, but for this implementation will reduce the number of output states due to reduced coverage of time delay signals.

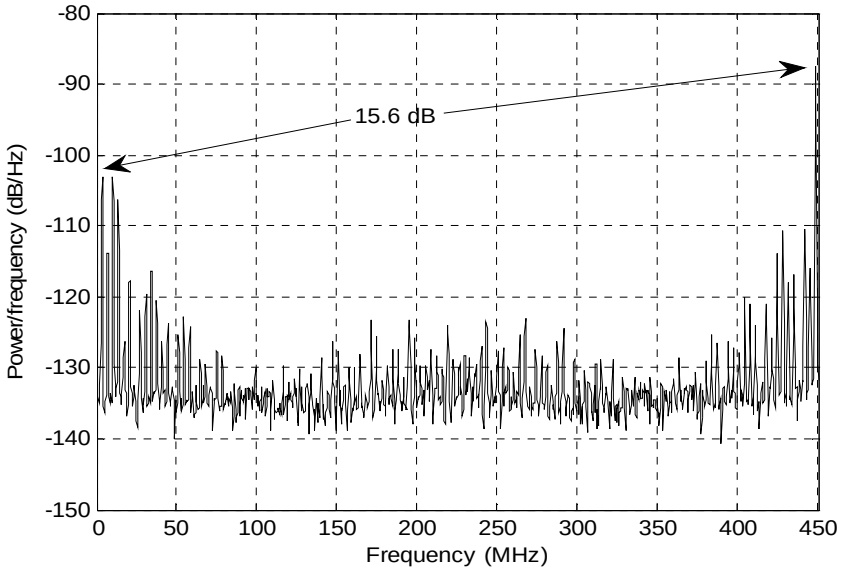


Figure 9.5 - 449MHz Sampled Signal SFDR Test Results No Noise

The three bit output SNR for the low jitter system is limited by SFDR to 2.6 ENOB. With reduced modulation of the varactors and improved SFDR, this will increase.

To understand the jitter tolerance of this architecture, a noise source was injected on V_{jitter}, as described in Section 9.2.2. From equation (4.3.3), it is predicted that a voltage based ADC with jitter of 98ps is limited to 1.2 SNR ENOB, while equation (8.1.10) predicts the similar results for this architecture.

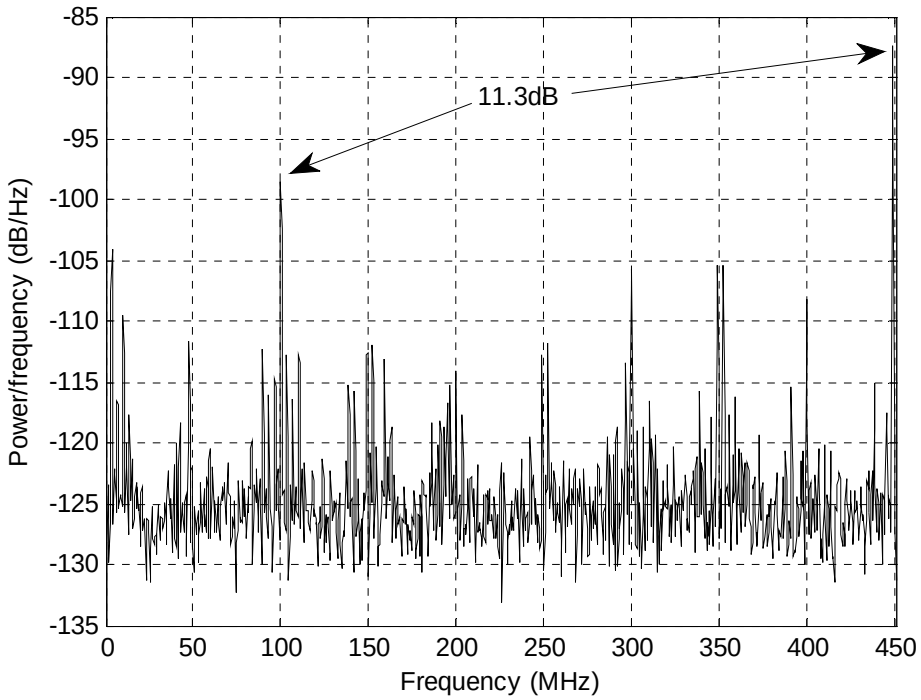


Figure 9.6 - 449MHz Sampled Signal SFDR Test Results With Noise

The clock with pseudo jitter described previously was used as the clock for the ADC which was then modulated with the 449MHz input signal. The digital output signal was analyzed in the frequency domain and the results are shown in Figure 9.6. As may be seen, the SFDR of the system with this noise is 11.3dB or 1.9 ENOB, a

slight reduction from the system with no jitter. The digital output signal was then used to calculate SNR ENOB, which was found to be 9dB or 1.2 ENOB. From [1], the expected ENOB, for a jitter dominant 900MS/s voltage based ADC with 98ps of jitter on the clock is 1.2. This indicates excellent performance of the ADC.

In Figure 9.7 the SFDR of the ADC with a 20MHz input signal is shown without the addition of noise while Figure 9.8 displays the SFDR of a 20MHz input signal with 98ps of jitter on the clock. Each of these figures allows for further examination of harmonics in the output signal. It may be noted that the addition of noise produces little difference in the SFDR of the output signal. The SFDR of the signal is dependent on the linearity of the phase modulation on the clock. This system modulates the clock signal with a β of 0.25π. From (8.1.13), it is seen that the maximum SFDR of the system is 23dB with the given value of β, which this system approaches.

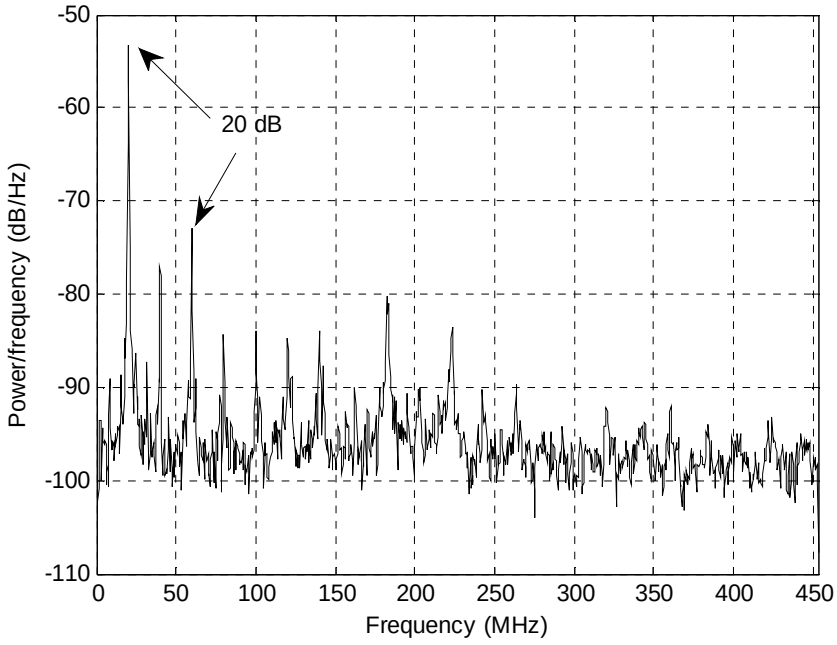


Figure 9.7 - 20MHz Sampled Signal SFDR Test Results with No Noise

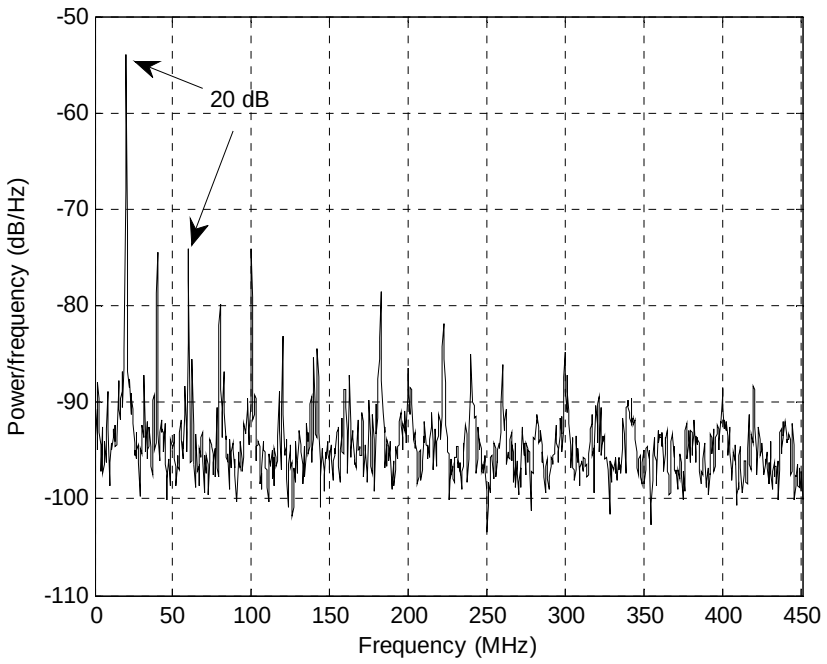


Figure 9.8 - 20MHz Sampled Signal SFDR Test Results with Noise

The circuit was also tested with DC inputs to evaluate the transfer characteristics. This revealed slightly unequal binning of voltage levels. Table 8.1 lists the results and shows some bits had larger windows while others had small ones. It is believed that the majority of this is due to the timing uncertainty in the discrete comparators used and the non-linear effect of capacitance tuning on the delay. Both these effects may be minimized in future designs by reducing the uncertainty in the comparators and calibrating the delay versus input voltage.

These values may be translated into non-linearity values to determine the operational limit due to non-linearities. This is commonly measured with two metrics: differential non-linearity and integral non-linearity. These measurements are calculated in terms of the least significant bit (LSB) of the system. If the differential non-linearity (DNL) or integral non-linearity (INL) exceeds 0.5 LSB, the linearity of the system is

insufficient to resolve the stated number of bits and the ENOB of the system is lower than stated.

Bit	High Voltage (V)	Low Voltage (V)	Bin Size (V)
0		1	
1	0.9	0.4	0.5
2	0.27	-0.17	0.44
3	-0.2	-0.68	0.48
4	-0.75	-1.39	0.64
5	-1.44	-1.87	0.43
6	-1.98	-2.45	0.47
7	-2.5		

Table 9.1 - DC Voltage Bins

DNL is the deviation in bin size from ideal, evenly sized bins. To calculate this, a basic equation is used

$$DNL = \frac{Actual\ Bin\ Size(V)}{Ideal\ LSB\ Bin\ Size(V)} - 1. \tag{9.2.1}$$

INL is the deviation of the input bin voltages from an ideal line and is calculated using another basic equation

$$INL = N + \frac{High\ Voltage(V) - DC\ Offset\ Voltage(V)}{Ideal\ LSB\ Bin\ Size(V)} \tag{9.2.1}$$

where *N* is the bit number.

Using the results in Table I, the DNL and INL of the ADC were calculated and are plotted below. These results indicate linearity is sufficient to resolve all three bits of data.

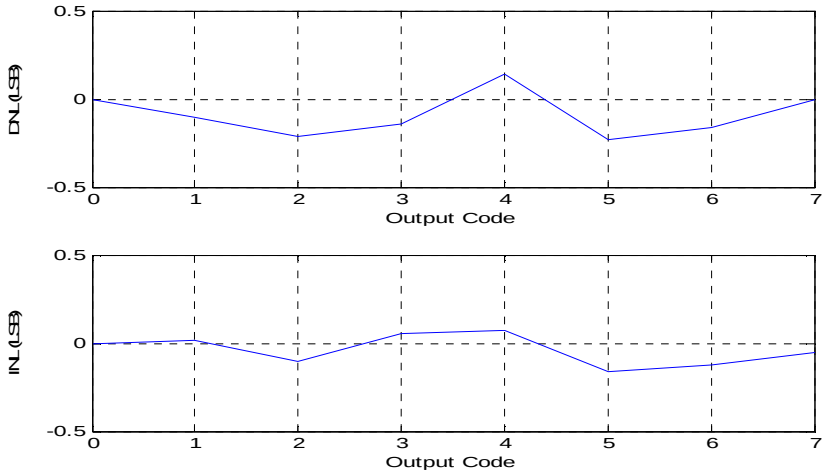


Figure 9.9 - DNL and INL of Time Based ADC

The ADC described in this section operates within the linearity requirement of a three bit system with jitter response as predicted by the analysis in Chapter 7. For a high speed system, this architecture holds promise in the ability to operate with high voltage input signals and low voltage processes with functionality equal to current voltage based ADC architectures.

Chapter 10 Conclusions

10.1 Summary and Conclusions

Microwave theory and techniques may be combined with circuit design in powerful ways. This thesis has explored the combination as applied to analog-to-digital converters. Two structures have been presented that combine the strengths of microwave and integrated circuit design.

Operation of an ideal transmission line was discussed and then applied to periodically loaded and lumped element systems. From this, the operation of a distributed amplifier was discussed.

Time-to-digital converters were briefly introduced and the basic structures commonly used were discussed. Various versions of the flash TDC were presented including the standard delay line, the Vernier delay line, and the interpolated delay line. Pipelined architectures were also presented. These structures employed time amplification in one case and time differentiation in the other.

Current high speed analog-to-digital converter building blocks, including sample-and-hold amplifiers, were discussed in conjunction with their limitations. The most common high speed sample-and-hold amplifier was presented in detail and analyzed at the circuit level. From here, discussion moved to voltage based analog-to-digital conversion systems. The flash based architecture was discussed in detail as a theoretical limit on the attainable ENOB resolution. Additionally, current implementations of time based analog-to-digital converters were discussed. Speed was a limiting factor in the operation of time based solutions.

The analysis and simulations of the proposed sample-and-hold amplifier architecture were presented. Extracted simulations were discussed validating the operation of the proposed architecture and comparing the results to the extracted simulated operation of the switched emitter follower circuit. These results indicate that the circuit is a valid alternative to the switched emitter follower sample-and-hold amplifier and improves the spur free dynamic range of the sampled signal at mid-range frequencies.

A version of the proposed sample-and-hold amplifier was constructed in 0.13μm CMOS. The designed circuit operated at voltages down to 1.2V at very low power and with small area footprint. Bandwidth of the circuit was consistent with simulated results, but much lower than half the rate of sampling.

The analysis and simulations of the time based analog-to-digital converter were discussed. The operation of the proposed implementation combines microwave structures and active circuitry to allow higher voltage operation in high speed, low voltage processes. Mathematical modeling of the system in Matlab and Simulink confirm theoretical expectations. Additional simulation was performed in ADS to verify design of the delay sections of the ADC architecture. Simulation results agree with test results and suggest good high frequency operation.

A PCB implementation of the proposed time based ADC was implemented and tested at rates up to 900MHz. Experimental results confirm operation in operation in a high jitter environment. Spurious free dynamic range measurements and signal to noise

ratio measurements were performed to measure ENOB performance. Linearity was also investigated and found to be sufficient for operation of a three bit system.

10.2 Future Work

To enable lower voltage operation of the proposed sample-and-hold amplifier, biasing networks must be designed to maintain appropriate current through devices at reduced supply. In addition, the operational frequency of the circuit may be increased by including an inductor on the gate of the switching transistor, as seen in the previous section comparing the switched cascode and switched emitter follower architectures. This will increase area consumption, but allow extension of allowable input frequencies.

An integrated circuit implementation of the analog-to-digital converter architecture would allow further optimization and improved operation. The reduced physical spacing achievable in a submicron integrated circuit would allow reduced time spacing, which is necessary for operation at higher clock speeds and for a higher ADC bit resolution.

Pipelining of the ADC system is also an area that would benefit from further investigation. Many different implementations of this are possible. The most promising from initial analysis is a voltage/time based system where voltage is used to store information between stages and time is used to quantize the signal. This may potentially allow operation of the architecture in the 12-bit and higher regime at reasonable power levels.

The primary limitation on the number of bits for the ADC will be the linearity of the voltage to phase conversion. Additional work in characterizing and designing voltage-to-phase converter blocks would allow the ADC to resolve a higher number of bits. A highly linear voltage-to-phase converter would also have additional applications in areas such as communications.

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