Scalable LO Distribution Schemes For Building Large-scale Phased Arrays

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Ruixing He

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Abstract

Facing the increasing demands of mmWave communication systems nowadays and the inherent adversity of higher signal attenuation in mm-wave wireless transmission, there is a continuous effort towards building larger scale phased arrays to achieve better effective isotropically radiated power (EIRP) and directivity. One of the critical challenges in array design is how to achieve frequency and phase synchronization in a scalable manner, which requires not only cell-level circuit optimizations but more importantly innovations at the architecture level.

In this thesis, we present three scalable schemes towards building large-scale active arrays with multiple local oscillators (LOs). First, a coupled oscillator array (COA) scheme based on unidirectional coupling is proposed. We derive the equilibrium states for the COA and demonstrate that our scaling scheme will preserve the steady state modes during scaling resulting in a predictable phase profile. We further evaluate the stability condition using the perturbation method. Based on the simulation results, we find that as long as the mismatches in the free-running frequencies are below a theoretical threshold, the scaled array could tolerate the presented element-to-element variations and could achieve frequency synchronization in a scalable manner.

Next, we present a two-dimensional coupled phase-locked loop array (CPLLA) scheme using type-II phase locked loop (PLL) as unit cell. Beside the concept of phase locking

between multiple oscillators, we implement a chip prototype of the PLL array at 28GHz. The chip performance is characterized by on-wafer probing. The measurement indicates that the out-of-band phase noise of the distributed array does not depend on the number of elements. However, we find several undesired issues including in-band phase noise degradation and stability issue with the taped out chip. In order to identify the reason behind the flawed performance, a theory of phase control conflicting between PLL loop and injection locking is proposed. We later verify our theory with the post-taped-out simulation which achieves consistent results with the measured data.

Finally, We adjust the method of mm-wave signal generation and distribution, and propose a new phase self-aligning array architecture. A prototype is made to demonstrate the phase self-aligning between a 1×2 array. The measured results verify our theoretical analysis, and show accurate phase control and a fast switching time with high spectral purity. As a result, we believe that the presented element-to-element self-alignment method is applicable for distributed tuning and control of scalable phased arrays without the need of extensive baseband calibration.

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Chapter 1

LO Distribution of Large-scale Phased Arrays

1.1   mmWave Phased Arrays and The Scaling Challenges

Millimeter waves band occupies the frequency spectrum from 30GHz to 300GHz. The mm-wave band integrated circuits are expected to have larger bandwidths, smaller components, better resolution and lower interference, than their radio counterparts that operate in the lower frequency band (K band and below) [1]. This has encouraged the development of new applications in wireless systems, including broadband new-generation wireless communication, and high-resolution sensing and imaging. However, there are several limitations presented with radios operating at mm-wave frequencies. First, the signals generally suffer from higher atmospheric and molecular absorption at

higher frequencies [2]. This means that there is a higher signal attenuation at mm-wave frequencies and shortening the transmission range in these bands, especially at the "attenuation peak" bands, like those at 60GHz and 120GHz. Secondly, as the mm-wave integrated circuits are moving closer to the trans-conductance cut-off frequency, performance of semiconductor components are limited in terms of power generation, which further limits the transmission range. In order to increase the radiating power, III-V compound devices could be used in integrated mmWave radios because of their superior power generation abilities, compared to silicon components [3, 4]. However, III-V compound devices are more expensive compared to silicon devices. Also, III-V devices have a relatively lower level of integration density, inferior yield and functionality compared to a silicon device with the same footprint [5]. Therefore, engineers continue to explore the potential of silicon-based mmWave system through circuit optimization and architecture innovation [6, 7, 8].

To improve the performance of mmWave communication systems, antenna array architectures, known as phased arrays, are used because they provide the ability to program the propagating beams in both power and direction through array scaling and beam steering, respectively [9]. During normal operation, phased arrays engage multiple antenna elements and maintain a tuned phase profile across the array. The antenna elements would radiate together and combine power coherently over the air at the beam angle. In other directions, the congregated power are at null due to phase interference from different elements. Besides higher output power, phased arrays also have a higher

radiating efficiency compared to single radiators because the effective isotropically radiated power(EIRP) of N-element phased array is $N^2 P_o$, when each element outputs power level of P_o. It is N times higher than a single-antenna radiator that consumes the same amount of dc power [7]. Since increasing N awards higher EIRP and radiation efficiency, it is not surprising that there has been an increasing focus on the design of phased arrays with more and more antennas [10, 11, 12, 13, 14]. Silicon-based phased arrays at scale comes with extra points in low cost advantage and high integration features [15, 16, 17].

However, scaling the size of phase arrays raises challenges. Since the local oscillator (LO) signal quality is crucial to the performance of wireless communication systems, maintaining the LO spectrum purity and phase consistency across array are quintessential for advanced array system. The conventional H-tree LO distribution network is not suitable for large-scale phased array because of the following reason. First, such global distribution network need to sustain identical phase delay and amplitude attenuation across routes from the center LO to each element, indicating a increasing layout difficulty as array scales up. It is reasonable to assume that such a distribution network is likely to be implemented on several substrates including chips, packages and boards with complex interface like flip-chip bonds or bonding wires which are difficulty to model accurately at mm-wave frequencies.

Compared to the use of a single LO source and a global distribution network, LO system with multiple sources could be more suitable to develop large-scale phased arrays

because it does not require a complicated global distribution network design. However, additional frequency and phase synchronization scheme are required to ensure a stable phase profile for coherent power combining over-the-air. For example, multiple phase-locked loops (PLLs) could coexist and form the top-level LO systems sharing the reference clock so that they are frequency locked to each other. However, the phase of each PLL would be in total random initially and would require additional calibration during the initialization process prior to the regular wireless communication sequences. However, since the phase profile are subject to any transient disturbance like the temperature drift in the active circuit blocks, such calibration would be a periodic requirement. The calibration process would require relatively long head-time periodically because frequency down-conversion are commonly involved in baseband calibration and each calibration practice would be time-consuming. Therefore, we identify the frequency and/or phase synchronization to be a critical challenge in the multi-LO system, placing a severe barrier ahead of scaling multi-LO array. The engineering solution to build large-scale mm-wave phased array demands innovations at fundamental level including array architectures and/or LO distribution schemes. Recently, people have proposed innovative multi-LO arrays based on coupled oscillator arrays (COA) [18, 7] and coupled PLL arrays (CPLLA) [19, 8]. However, more research works are still necessary in the topic of array scaling where new ideas are much welcomed because the reported prototypes so far haven't successfully demonstrated the scalability of the existing typologies(for example, arrays with >1000 elements).

In the following sections of this chapter, we will review several multi-LO array schemes including COA, CPLLA and an interferometry-based autonomous array.

1.2 Coupled Oscillator Array

Distributed LO network could compensate the signal loss along the mm-wave band signal paths [20]. To meet the requirement of power combing and beam steering during phased array operation, distributed LOs have to achieved frequency and phase synchronization. The injection locking feature of oscillators have been applied to build coupled oscillator array and achieve synchronization across elements [18, 21, 22, 23]. The phase dynamic analysis of the coupled oscillator arrays are necessary to predict the settled phase modes and the corresponded stability conditions, and it starts with understanding the basics of the injection locking.

The injection locking refers to the phenomenon that the oscillator frequency tend to be locked to an external signal source when the external source inject power to the oscillator. Several models are presented to analyze and predict the oscillator behavior under injection [22, 23, 24]. The well-accepted model proposed by Adler [24] describes the phase dynamics of the oscillator as:

$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{A_{inj}}{A}\sin(\theta_{inj} - \theta). \tag{1.1}$$

A is the amplitude of oscillator under injection, A_{inj} is the amplitude of the injected signal, θ is the instantaneous phase of oscillator, θ_{inj} is the phase of the injected signal,

ω_0 is the transient frequency of the free-running oscillator, Q is the quality factor of

the oscillator. If the oscillator is injection locked to the external source, we will have

$\frac{d\theta}{dt} = \omega_{inj}$, where ω_{inj} is frequency of the injecting signal. This means that the second

terms on the right hand side of the equation in (1.1) should equal to $\omega_{inj} - \omega_0$. Therefore,

the range limit on the circuit parameters and Sine function defines a finite range of the

injecting frequency that the injected oscillator could be locked to. The locking range is:

$$|\omega_{inj} - \omega_0| \leq \frac{\omega_0}{2Q} \frac{A_{inj}}{A}. \tag{1.2}$$

Using vector summation method, we can extend the equation (1.1) to represent the

multiple sources injection conditions in equation (1.3).

$$\frac{d\theta}{dt} = \omega_0 - \frac{\omega_0}{2Q} \sum_{j=1}^{N} \epsilon_j \frac{A_{inj,j}}{A} \sin(\Phi_j + \theta - \theta_{inj,j}). \tag{1.3}$$

In a coupled N-oscillator array, each oscillator could be injected by the rest N-1 oscil-

lators. The phase relationships could be represented in the form of Adler's equations:

$$\frac{d\theta_i}{dt} = \omega_i - \frac{\omega_i}{2Q} \sum_{j=1}^{N-1} \epsilon_{ij} \frac{A_j}{A_i} \sin(\Phi_{ij} + \theta_i - \theta_j)$$

$$i = 1, 2, ..., N. \tag{1.4}$$

ϵ_{ij} represents the coupling coefficient from j^{th} oscillator to i^{th} oscillator.

Equation (1.4) describes a general model and have been used to study COAs of

different structures which we assort into two categories: (1) bilateral coupled- and (2)

unidirectional coupled- oscillator arrays. The first coupling method, first proposed in

1990s [22], is the conventional method to build COA. Many works have studied the phase dynamics and stability conditions for LO generation in beamforming applications [20, 22, 23]. However, there is a known feature of bilateral COAs that the probability of locking for one- and two- dimensional arrays with randomly distributed frequencies will drop to zero as the number of oscillators increases [22]. To ensure that a COA of N element would be frequency locked, the coupling strength must increase at the rate of $\sqrt{N}$ [25]. As a result, the bilateral COA is not suitable for scalable phased arrays because the coupling strength is within a finite range. The second coupling method is a relative new scheme with a few reports with mmWave beamformer prototypes [7, 18]. More theoretical works on the unilateral COA are required to have a deeper understand about its potential in LO scheme for phased arrays at scale.

1.3   Coupled PLL Array

PLL uses a feedback loop to force a targeted oscillator to track the frequency of a reference signal. The loop operation results in a fixed phase difference between the oscillator and the reference signal. The settled phase difference could be further controlled by adding a DC offset voltage into the loop [26]. The phase tracking and tuning feature of this control method could be used to couple multiple PLLs together and form beam-steering active oscillator arrays. Fig. 1.1 shows a diagram of a CPLLA for a 1×2 array. Here a mixer is served as phase detector which determines the sinusoidal relationship between phase difference and control voltage [26]:
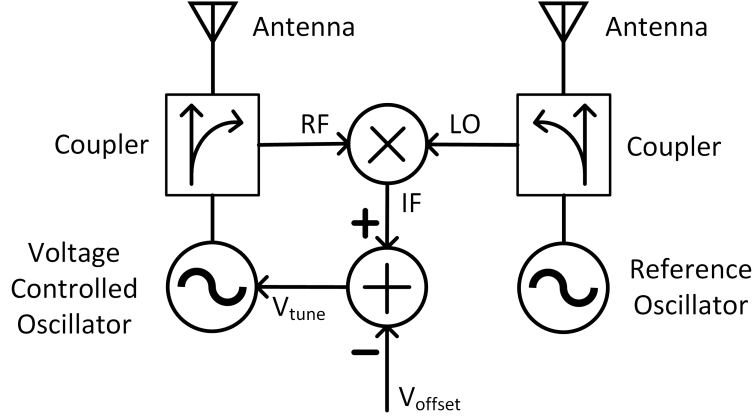
Figure 1.1: PLL applied to a 1×2 oscillator array.

$$\phi = \sin^{-1}\left(\frac{V_{tune} + V_{offset}}{K_\phi}\right) \tag{1.5}$$

where ϕ is the phase difference between two antennas and K_ϕ represents mixer's gain. Equation (1.5) also indicates that the PLL can generate a phase difference between antennas within range from $-90°$ to $+90°$. There are more works of the CPLLA including [27, 28, 29, 19]. There are two limitations in this type of CPLLA. First, to the best of the author's knowledge, the reported arrays could only be scaled in one dimension using daisy-chain topology. New coupling techniques are needed to scale CPLLA in two dimensions. Second, the array structure shown in the Fig. 1.1 uses unit PLL element with finite loop gain [30]. The finite loop gain comes with the advantage of tunable settled phase by controlling V_{offset}, however, it also translates mismatches of oscillator free-running frequencies to phase errors between array elements.

PLL with infinite loop gain such as type-II PLL could be used as LO elements in CPLLA as well. Type-II PLL consists of frequency/phase detectors, charge pump, loop

filter, voltage-controlled oscillator and frequency divider chain. The open-loop transfer function of type-II PLL has infinite loop gain at DC [30]. When the CPLLA uses type-II PLL as unit elements, the mismatches in oscillator free-running frequencies won't be transferred to phase errors. However, new coupling topology is required in order to build CPLLA in two dimensional because the reported prototypes are mainly limited to one-dimensional topology [19].

1.4   Drawbacks in Conventional mmWave Phase Control

In the conventional mmWave signal generation and phase control method, the mm-wave LO signal is generated and controlled through a PLL. In this scheme, a voltage-controlled oscillator (VCO) generates the mm-wave signal. At the same time, a phase detector compares the phase of the VCO with an input reference clock by indicating whether the source is leading or lagging behind the reference. Subsequently, the output of the phase detector connects to a loop filter which adjusts the control voltage of the VCO until the phase is locked. The phase detector is typically based on flip flops and digital gates so a frequency divider chain is necessary to down-convert the VCO frequency to the input reference [30].

The typical VCO is tunable using analog varactors and/or digitally controlled capacitor banks placed inside the LC resonator. Hence as shown in Fig. 1.2a, the PLL control loop consists of two main sections: (1) phase detection and comparison at the reference frequency, and (2) phase control that applies to the mm-wave source. While such

Phase Error ×M

Lower Q,
Degrade PN

×M

Phase
Detection

Phase
Control

÷M

→ f

Reference
Frequency

mm-Wave
Frequency

(a)

Tuning Range ×M

×M

Phase
Control

Phase
Detection

÷M

→ f

Reference
Frequency

mm-Wave
Frequency

(b)
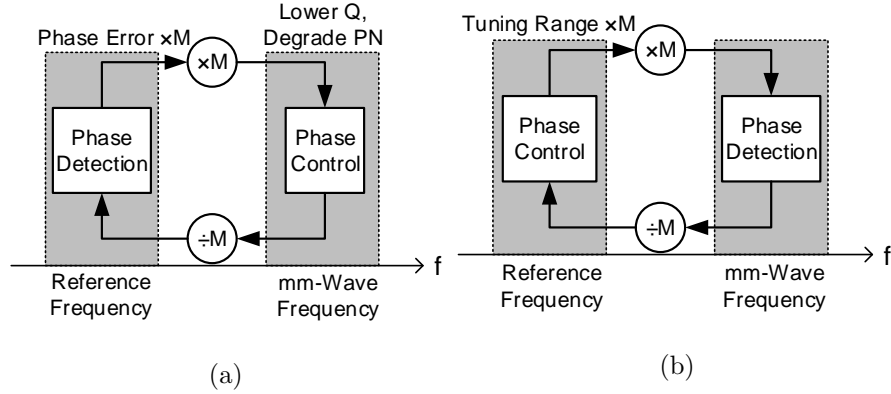
Figure 1.2: Two schemes for mm-wave signal generation: (a) The conventional scheme detects phase at the reference frequency and controls it at the mm-wave frequency. (b) The scheme proposed in chapter four detects phase at the mm-wave frequency and controls it at the reference frequency.

topology has been widely adopted in RF frequency generation, it is limited by underlying weaknesses when applied to mm-wave multi-source generation and synchronization. First, tuning the frequency and phase of a mm-wave oscillator involves tunable analog varactors or switch-based components in the resonator. At mm-wave frequencies, the varactor would dominate the quality factor of the LC tank and limit the phase noise and power efficiency [31]. The use of capacitor banks of metal-insulator capacitors alleviates this issue to some extent. However, even using this technique, the limited quality factor of the capacitor and switch eventually leads to the same degradation in the resonator and limits the frequency of operation [32]. As result, many recent high-frequency synthesizers have turned toward frequency multiplication to scale up the output frequency

[33]. However, such methods provide no control over the phase of the signal. The second issue with the traditional loop topology is that the phase detector operates at the low frequency of the reference signal. Therefore, any phase error inside the control loop is multiplied by the frequency division factor when examining the output of the VCO. As a result, the oscillator phasor would be locked to the reference signal but with a significant and unpredictable phase error. Sub-sampling PLLs can overcome this phase error multiplication issue within a single source [34]. However, in a multi-source array scenario, this architecture is still blind to random phase variation between adjacent elements.

Based on this discussion, we believe in Fig. 1.2b presents a scheme that is fundamentally more suitable for signal generation and synchronization at mm-wave and THz frequencies. In this scheme, we detect the phase at the target mm-wave frequency while phase control occurs at the lower frequency of the input reference. By effectively switching the location of detection and control we simultaneously avoid both above challenges: First, by controlling phase at the reference frequency, we avoid direct control of the resonator resulting in optimal frequency and spectral purity. Second, by directly measuring the phase at the mm-wave band, we prevent phase ambiguity and enable accurate phase alignment.

The rest of the thesis is organized as follows: In chapter two, we propose a scalable COA scheme based on unidirectional coupling method [35]. As a theoretical work, we analytically derive the stable modes for the scaled COA and demonstrate that the

coupling behaviour is stable and predictable regardless of the array dimension. In order to study the stability of the proposed array, we analyze the transient dynamics and the scalability of the structure in the presence of element-to-element variations. We believe the proposed scheme is a promising LO solution for large scale phased arrays.

In chapter three, we propose a two-dimensional CPLLA scheme using type-II PLLs as LO elements. We present the concept of phase locking between multiple oscillators and present a chip prototype of the PLL array at 28GHz. The measurements verify that out-of-band phase noise of the distributed array does not depend on the number of elements in the array. The measured results indicate that there are several limitations of the proposed scheme, including in-band phase noise degradation and stability issue. Through post-tape-out investigation, we find the underlying reason is due to the conflicting between the PLL phase control and magnetic injection coupling.

In chapter four, we use the method of mm-wave signal generation and distribution based on the topology shown in Fig. 1.2b [36]. We demonstrate the concept with a chip prototype showing accurate phase control and a fast switching time with high spectral purity. The presented element-to-element self-alignment method is applicable for distributed tuning and control of scalable phased arrays without the need of extensive baseband calibration.

Finally, we summarize the three projects in chapter five. In addition, we discuss about the future works in the author's perspective and mention two directions for the following up research.

Chapter 2

Scalable Oscillator Array Using Unilateral Coupling

2.1 Introduction

There is an increasing demand for high-speed wireless communication based on Silicon-based radio front-ends with mm-wave and sub-mm-wave carrier frequencies [10, 37, 38, 39]. At these frequency bands, however, a single-antenna front-end would inevitably suffer from limited output power and propagation loss. In order to achieve practical power levels, RF engineers commonly employ phased arrays to coherently combine power from many individual sources and radiators, and there is an effort to significantly increase the number of elements in such an array [40, 20].

There are several challenges that limit very large scale arrays particularly at mm-wave frequencies. One of the fundamental limits is to achieve even distribution of the RF or LO signal across many elements [41]. The increasing loss and inter-element coupling places a crucial limit on global distribution of such high frequency signals. Coupled oscillator arrays have been introduced as an alternative to this traditional distribution [23]. The idea behind this approach is that instead of only having a single source, each element has its own local oscillator (LO). As a result, the new array would have multiple LOs synchronized by the coupling network. This new scheme promises two main benefits: first, the synchronization network only relies of adjusting local coupling between neighboring element resulting in seamless scaling of the network. Second, the coherent combining of many independent oscillators, can increase the purity of the signal source far beyond what is achievable with a single source [28, 19].

Recent work has shown that such a coupled oscillator array can operate at small
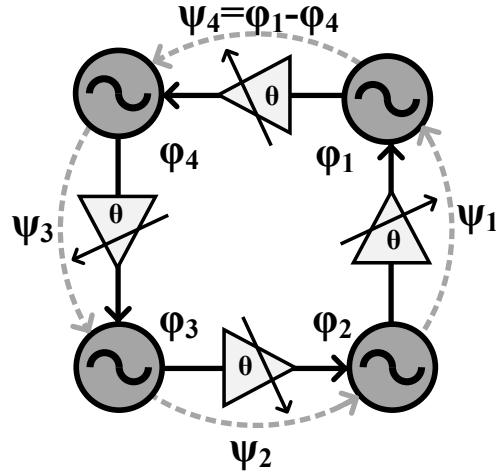
Figure 2.1: The diagram of ring made of four unilateral coupled oscillators.

number of elements [42]. Tousi presents the phase dynamics analysis of a 2×2 array using active unidirectional coupling between adjacent elements [6], as shown in Fig. 2.1. Later, he presents a 4×4 beamformer constructed upon the previous 2×2 unit blocks, and promotes a scalable scheme for phased arrays [7]. In order to have insight of this scaling scheme, more investigations on the scaled arrays are needed regarding phase dynamics and stability conditions. In this chapter, we analyze the scaling arrays using the 2×2 array as cell block, and propose a general theoretical framework as a method to scale the coupled-oscillator array.

The rest of this chapter is organized as follows: Section 2.2 starts with a case study, analyze the equilibrium modes of the example array. The stability analysis of the case study is continued and carried out in Section 2.3. Section 2.4 extents the conclusion drawn from the case study to the general condition. We will demonstrate that the array
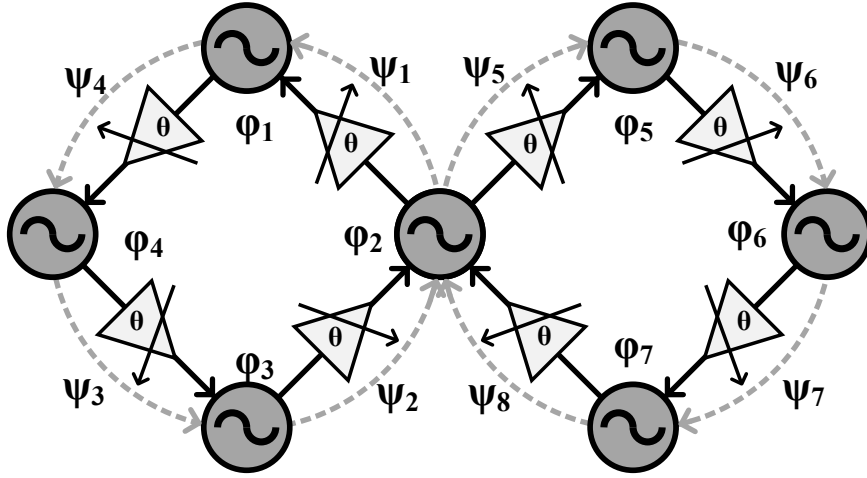
Figure 2.2: The diagram of the example array made of two ring array sharing one oscillator at the vertex.

could be scaled without compromising the stability. This chapter is concluded with a discussion of the settling dynamics and resilience to variation of the scaled arrays.

2.2 Steady-state Analysis: A Case Study

Based on the prior study [6], we know that a 2×2 array as shown in Fig.2.1 only has four fundamental modes $\psi = k\pi/2,\ k = 0, 1, 2, 3$ where ψ is the phase difference between adjacent oscillators. In order to expand the array we propose to use this four-oscillator ring as a unit block and construct larger arrays by connecting the rings through a common vertex which we call the "shared-vertex" technique. This is contrast to sharing a common edge between two unit blocks and we shall see how this technique is beneficial in scaling up the size of coupled oscillators.

Fig. 2.2 shows the smallest-expanded array by connecting two unit rings at a common oscillator. In this scheme, oscillator 2 is the common vertex and receives dual injection from both loops while all other oscillators only receive a single injection. As a result, in order to balance the coupling intensity across all elements, the intensity of injection to the shared oscillator is half compared to regular elements. To analyze the dynamics, we define the phase of the ith oscillator as ϕ_i, $i = 1, 2, ..., 7$ and the phase difference between adjacent oscillators as ψ_i. Based on Adler's equation [24], we derive the phase dynamics of the array elements as:

$$\dot{\psi}_1 = \frac{K}{2}\sin(\psi_2 + \theta) + \frac{K}{2}\sin(\psi_8 + \theta) - K\sin(\psi_1 + \theta)$$

$$\dot{\psi}_2 = K\sin(\psi_3 + \theta) - \frac{K}{2}\sin(\psi_2 + \theta) - \frac{K}{2}\sin(\psi_8 + \theta)$$

$$\dot{\psi}_3 = K\sin(\psi_4 + \theta) - K\sin(\psi_3 + \theta)$$

$$\dot{\psi}_4 = K\sin(\psi_1 + \theta) - K\sin(\psi_4 + \theta)$$

$$\dot{\psi}_5 = \frac{K}{2}\sin(\psi_2 + \theta) + \frac{K}{2}\sin(\psi_8 + \theta) - K\sin(\psi_5 + \theta)$$

$$\dot{\psi}_6 = K\sin(\psi_5 + \theta) - K\sin(\psi_6 + \theta)$$

$$\dot{\psi}_7 = K\sin(\psi_6 + \theta) - K\sin(\psi_7 + \theta)$$

$$\dot{\psi}_8 = K\sin(\psi_7 + \theta) - \frac{K}{2}\sin(\psi_8 + \theta) - \frac{K}{2}\sin(\psi_2 + \theta), \tag{2.1}$$

where θ is the extra phase delay from the phase shifter, and K is the intensity of the injection to the oscillator.

Furthermore, we apply the following boundary conditions based on the phase consistency:

$$\psi_1 + \psi_2 + \psi_3 + \psi_4 = 2m\pi, \qquad m = 1, 2, \ldots$$

$$\psi_5 + \psi_6 + \psi_7 + \psi_8 = 2n\pi, \qquad n = 1, 2, \ldots \tag{2.2}$$

The system arrives at the steady state when $\dot{\psi}_i = 0$, for $i = 1, 2, \ldots, 8$. This equilibrium solution, ψ_i^0, represents a constant phase difference between oscillators because every oscillators operates at the same frequency if the array settles successfully. By applying the steady state condition to (2.1), we arrive at the following relations:

$$\sin\left(\psi_1^0 + \theta\right) = \sin\left(\psi_j^0 + \theta\right), \quad j \in \{3, 4, 5, 6, 7\}, \tag{2.3a}$$

$$\sin\left(\psi_1^0 + \theta\right) = \frac{1}{2}\sin\left(\psi_2^0 + \theta\right) + \frac{1}{2}\sin\left(\psi_8^0 + \theta\right). \tag{2.3b}$$

The solution of (2.3a), ψ_j^0 can be either $\psi_j^0 = \psi_1^0$ or $\psi_j^0 = \pi - \psi_1^0 - 2\theta$. This ends up in $2^5 = 32$ possible results as the solution of (2.3). Considering all 32 conditions for both (2.2) and (2.3) and solve them one by one, we find out that ψ_1^0 could be one of the following values:

$$\psi_1^0 \in \{\frac{k\pi}{2}, \ \theta \pm \frac{\pi}{2}, \ -\theta \pm k\pi, \ -3\theta + \frac{\pi}{2} \pm k\pi\}, \ \ k = 0, 1, 2, 3. \tag{2.4}$$

This includes every possible equilibrium states of the phase difference ψ_1^0. Once ψ_1^0 is known, we can easily find out the phase differences of the rest oscillator pairs as $\psi_j^0, j = 2, 3, ..., 8$. As the next step, we look into the stability of these steady-state conditions.

2.3 Stability Analysis: A Case Study

In order to find out the physically realizable modes, we use the perturbation method [43] to analyze the stability of solutions listed in (2.4). Using this method, we can tell whether a steady state solution is stable by inspecting whether perturbations around it would decay over time. Equation (2.1) consists of multiple nonlinear differential equations, however, in order to manage the complexity of the following analysis, we use the first order linear approximation of the equation sets and introduce perturbations to the steady state solution, ψ_i^0.

We define $\boldsymbol{\psi} = [\psi_1^0 \dots \psi_8^0]^T$ and rewrite (2.1) as $\dot{\boldsymbol{\psi}} = J\boldsymbol{\psi}$, where J is the Jacobian matrix. To ensure the decay of any perturbation, the real part of all eigenvalues in J have to be non-positive [44]. Prior study has successfully employed Gershgorin theorem to study the eigenvalues of a four-oscillator ring structure using unidirectional coupling between neighbor elements and identify its four stable modes [6]. According to the Gershgorin theorem, eigenvalues should be inside a set of Gershgorin circles in the complex plane [43]. Here we first approach the stability inquiry of our case study with a similar method.

As shown in Fig. 2.3a, the four-element ring structure has all of its eigenvalues residing in a circle on the left hand side of the imaginary axis. This distribution of the eigenvalues indicates that the each corresponded steady state solution would be stable. However, as shown in Fig. 2.3b, when plotting the distribution of the eigenvalues of the two-ring system, these circles contain both positive and negative real values. As a result,
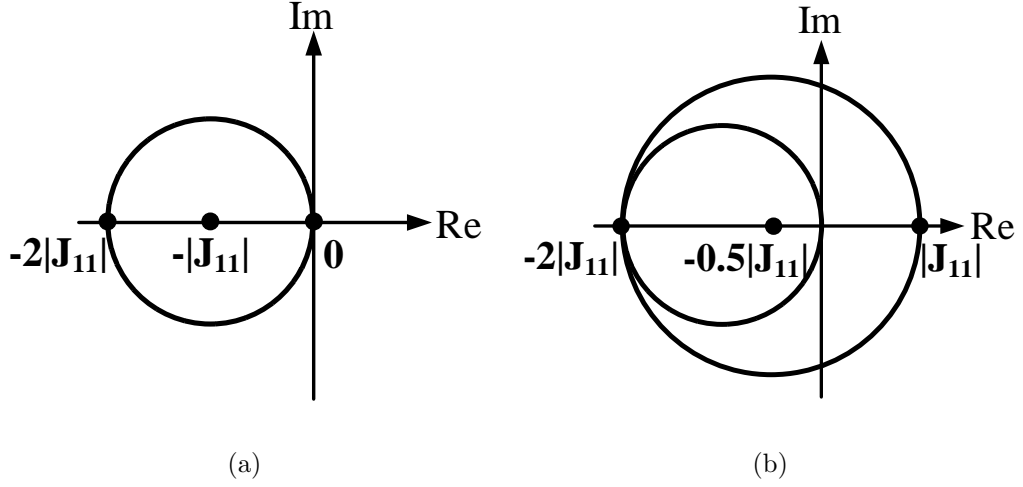
Figure 2.3: Gershgorin circles and the distribution of eigenvalues for (a) four-oscillator ring and (b) two-ring array.

the eigenvalue signs of a two-ring system are still uncertain following the same analytical process of the previous single-ring case. Therefore, we choose to directly compute the eigenvalues associated with each solution in (2.4) and examine the stability one by one.

The modes corresponding to $\psi_i^0 = k\pi/2$, lead to the following eigenvalues:

$$\lambda_1 = \lambda_2 = \lambda_3 = \frac{\lambda_4}{2} = -Ka_1$$

$$\lambda_5 = \lambda_6 = -Ka_1(1-i) \tag{2.5}$$

$$\lambda_7 = \lambda_8 = 0,$$

where $a_1 = cos(k\pi/2 + \theta)$. Since K is positive, in this mode, all λ_i's are non-positive for $a_1 > 0$. Hence the equilibrium solution $\psi_1^0 = k\pi/2$, is stable when:

$$-\frac{\pi}{2} - \frac{k}{2}\pi + 2n\pi < \theta < \frac{\pi}{2} - \frac{k}{2}\pi + 2n\pi. \tag{2.6}$$
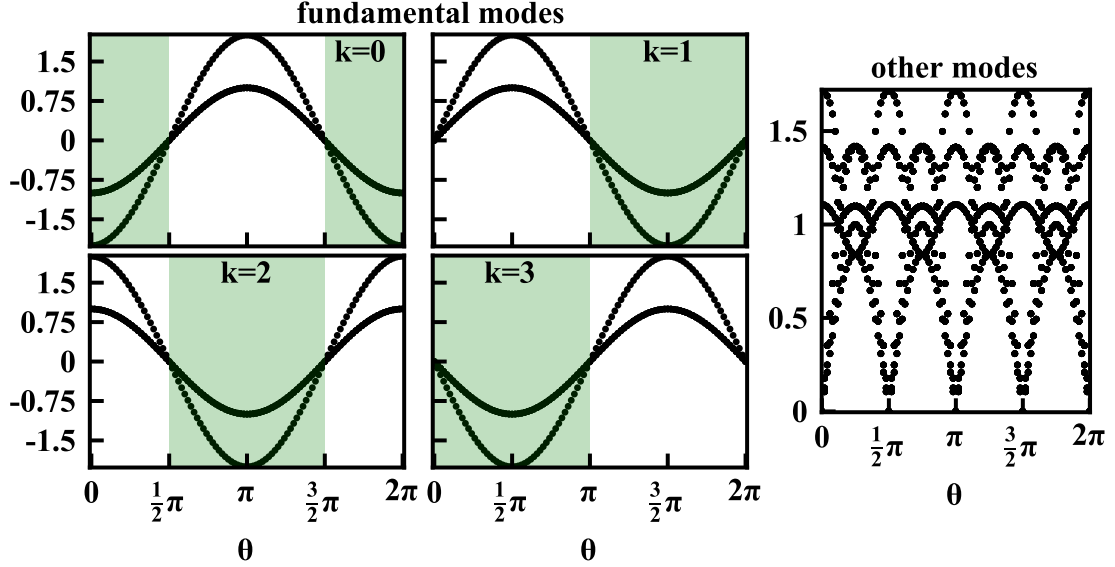
Figure 2.4: All non-zero $\text{Re}\{\lambda\}$ for the two-ring array across different modes of operation. The shaded areas represent stable regions.

Fig. 2.4 shows all of the non-zero $\text{Re}\{\lambda\}$ for each mode of $\psi_i^0 = k\pi/2$, $k = 0, 1, 2, 3$, and green rectangular areas denote stable regions with respect to θ.

Beside $\psi_i^0 = k\pi/2$, we also investigate the rest of the solutions corresponding to other values in (2.4). These solutions turn out to be unstable as they always contain a positive eigenvalue. The right figure in Fig. 2.4 shows $\max(\text{Re}(\lambda_i))$ for each of these equilibrium solutions. This demonstrates that there is always at least one positive eigenvalue, hence none of these modes are stable. This means that the fundamental modes are the only stable modes of the two-ring array. It is worth mentioning that the stability condition in (2.6) is identical to the stable solutions derived for the single ring structure in [18]. This demonstrates the benefit of shared-vertex expansion of the single loop which maintains

the fundamental stable coupling modes without adding extra modes.

2.4 Scalable Array Analysis: The General Model

In this section we analyze the stable modes of operation as we further scale the array using the shared-vertex technique. Fig. 2.5 shows the proposed scaling scheme with an example of a 4×4 array. For the general array we observe that there are three distinct types of connections. If we name the oscillator with two injected paths as the "center" and regular oscillators as "vertex" there are: (1) the center-to-center connection, (2) the vertex-to-center connection and (3) the vertex-to-vertex connection. Next, we derive the stable modes as a result of these three different connections.

2.4.1 Analysis of steady-state modes

In Fig. 2.5, we can use the connection between oscillators 2 and 5 as an example of a center-to-center connection with the following dynamical equation:

$$
\begin{aligned}
\dot{\psi}_5 = {} & \frac{K}{2} \sin(\psi_2 + \theta) + \frac{K}{2} \sin(\psi_8 + \theta) \\
& - \frac{K}{2} \sin(\psi_5 + \theta) - \frac{K}{2} \sin(\psi_9 + \theta).
\end{aligned}
\tag{2.7}
$$

Similarly, we use the connection between oscillator 3 and 2 as an example of the vertex-to-center connection:

$$
\dot{\psi}_2 = K \sin(\psi_3 + \theta) - \frac{K}{2} \sin(\psi_2 + \theta) - \frac{K}{2} \sin(\psi_8 + \theta).
\tag{2.8}
$$
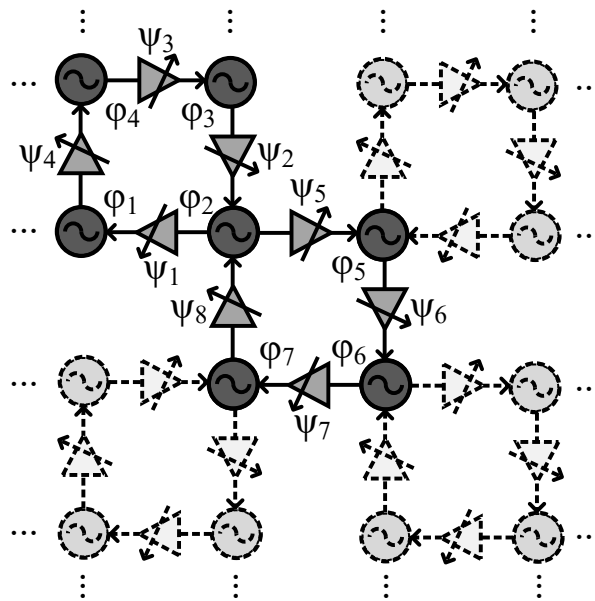
Figure 2.5: Proposed scheme for expanding the coupled array structure. The dimensions scale using the shared-vertex technique.

Finally, the connection between oscillator 4 and 3 is an example of the vertex-to-center connection:

$$\dot{\psi}_3 = K\sin(\psi_4 + \theta) - K\sin(\psi_3 + \theta). \tag{2.9}$$

When $\psi_i = k\pi/2$, the right hand side of the above three types of equations is zero. This is true regardless of the size of the array. Hence the fundamental modes derived in section II permeates throughout the expanded array. To ensure the stability of these fundamental modes in the expanded array, we test $\text{Re}\{\lambda\}$ across θ for different array sizes. Next, we exam the stability of equilibrium of the expanded array similarly as the previous section. For instance, Fig. 2.6 demonstrates the distribution of all non-zero $\text{Re}\{\lambda\}$ for an 4×4 array. We verify the stability of these modes up to a 16×16 array. Verifying this for larger arrays becomes computationally prohibitive, however we anticipate this conclusion to hold for any array size.

2.4.2 Transient Simulation

In this section we study the array dynamics, its transient behaviour, and synchronization in the presence of physical imperfections in a scaled array. Without losing generality[1] we use the following circuit parameters in simulations: Free running frequency $f_0 = 50GHz$, $Q = 20$, and injection intensity $(I_{inj}/I_{core}) = 2\%$ [2] .

---

[1] The choice of specific numerical values does not affect the conclusions in the work.
[2] The assumption for modeling injection-locked oscillators with Adler's equation is that the coupling strength is weak, i.e., $I_{inj} \ll I_{core}$.
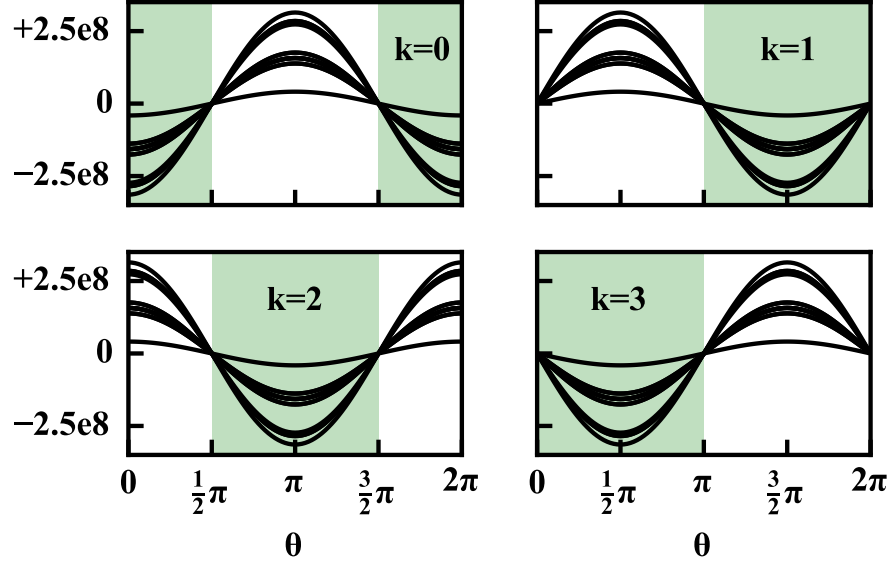
Figure 2.6: All non-zero $\mathrm{Re}\{\lambda\}$ for the 4×4 array across different modes of operation. The shaded areas in green color represent stable regions.

Stable modes and settling speed

To study the stable modes we start all oscillators from random initial phases. Fig. 2.7 shows the settling possibilities of the four fundamental modes across large volume repetitive tests. The density of each fundamental mode agrees with the stable regions predicted in (2.6).

According to nonlinear theory [45], the eigenvalues appear at the exponential part of the transient trajectories, so each real part of all non-zero eigenvalues is inversely proportional to the time constant of a transient mode. Therefore the minimum value of all non-zero real parts determines the dominant(largest) time constant which predicts the settling speed of the array. For this reason, we use $\min(\|\mathrm{Re}\{\lambda\}\|)$ as an indicator
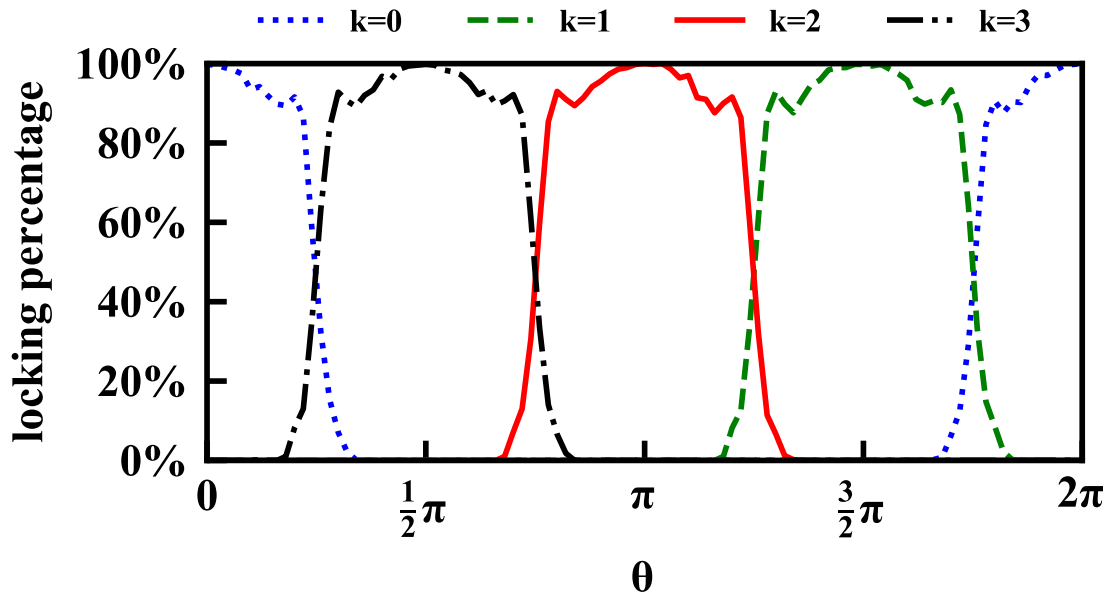
Figure 2.7: Probability density distribution associated with four fundamental stable modes ($\psi_i^0 = k\pi/2,\ k = 0, 1, 2, 3$) in the 4×4 array. For each θ, we run 500 iterations with random initial phases to get the statistical result.
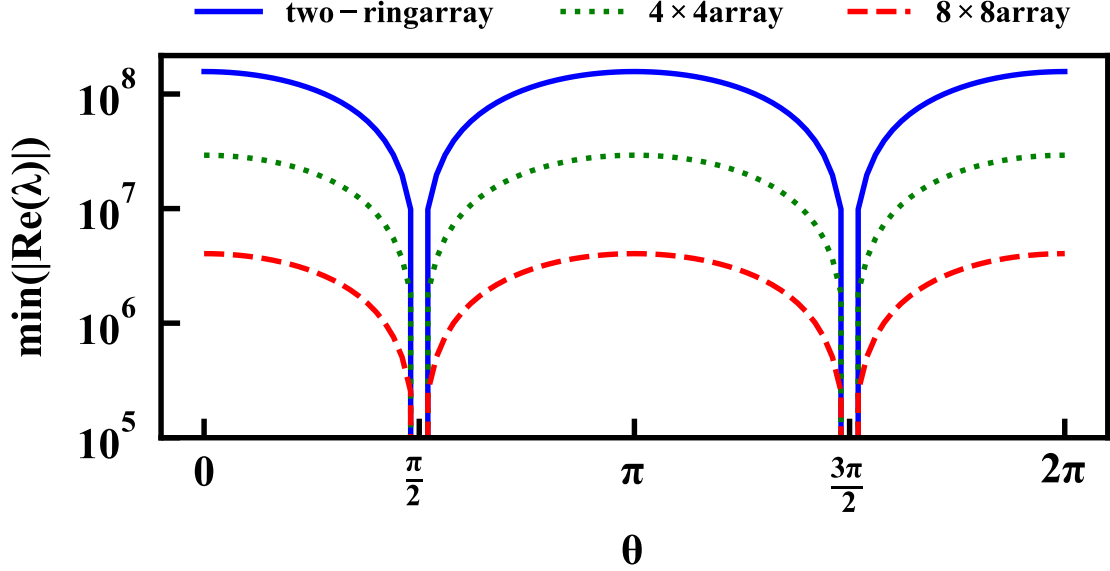
Figure 2.8: Array time constant derived from $\min(\|\operatorname{Re}\{\lambda\}\|)$. Each plot represents a particular array size.

of settling speed and compare it between different array sizes. As Fig. 2.8 shows, this $\min(\|\operatorname{Re}\{\lambda\}\|)$ decreases as the size of the array scales which indicates that a larger array needs a longer time to settle. We can observe this transient behaviour in Fig. 2.9.

Furthermore, in a given array size, (2.5) indicates that the settling speed is a function of the coupling coefficient K and the active phase delay θ. As a result, it is possible to reduce the settling time by temporarily reducing the Q of the oscillator or increasing the injection current [24].
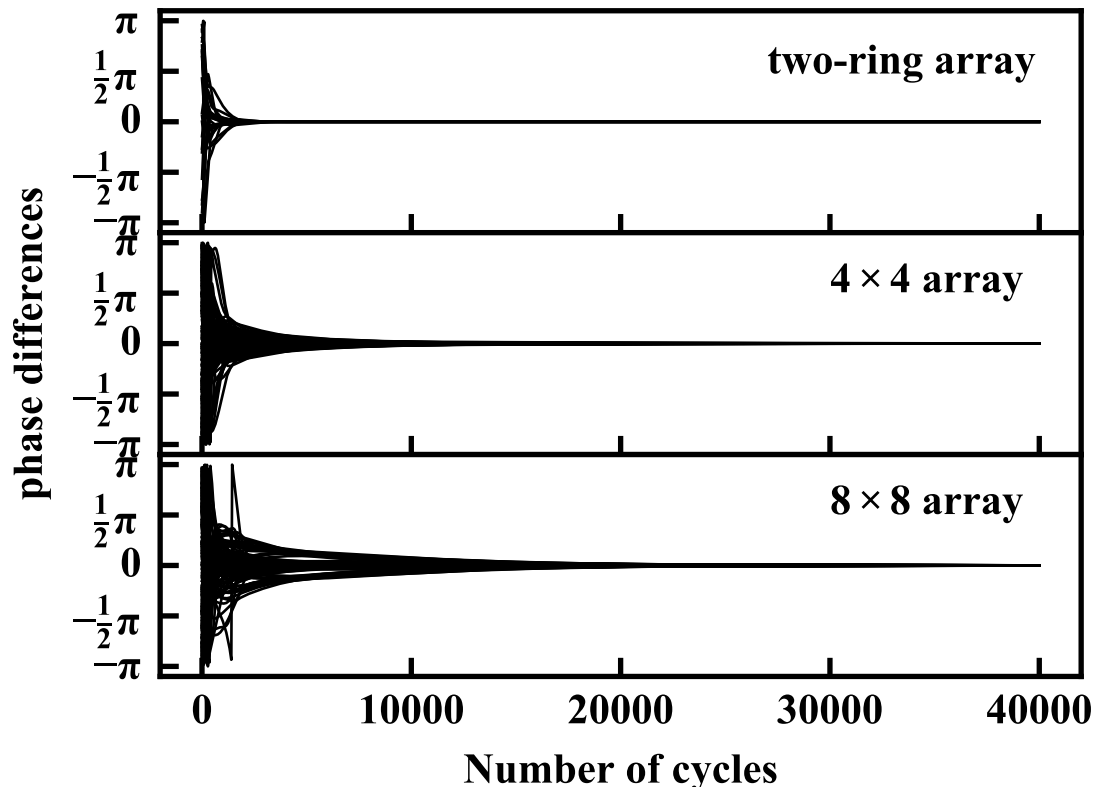
Figure 2.9: Transient response of individual elements when the coupled array is settling to $\psi = 0$.

Resilience to element-to-element variation

Physical variations including PVT introduce random and systematic drifts across arrays in two places: oscillator free-running frequency f_0 and injection intensity K. In this work, we focus on the f_0 mismatch since it would disrupt frequency synchronization in the coupled array when such mismatch exceeds the maximum locking range. The K mismatch is outside the scope of this thesis which requires future work to further study its effect.

For passive coupled oscillators, Strogatz shows that in order to maintain synchronization for an N-element structure, coupling strength should increase proportional to $\sqrt{N}$ [25]. This imposes a practical limit on such a coupled array [22].

However, in an actively coupled array, due to the modular structure of the network we anticipate a better resilience to random variation. This is because in the shared-vertex technique, as long as the sub-arrays are synchronized, we can expect the combined structure to operate in the same stable mode as the sub-arrays. According to Adler's equation the smallest block is guaranteed to synchronize as long as the frequency difference is within the maximum locking range, i.e. $\pm\frac{K}{2}$. As a result, even a much larger array should synchronize as long as all its elements are within this range.

To verify this we perform statistical transient simulation by randomly varying the center frequency of array elements. In this simulation, the frequency drift is a uniform random variable with bounds of $\pm\alpha K$. Fig. 2.10 shows the probability of synchronization as a function of α for different sizes of the array. This simulation verifies that 1)
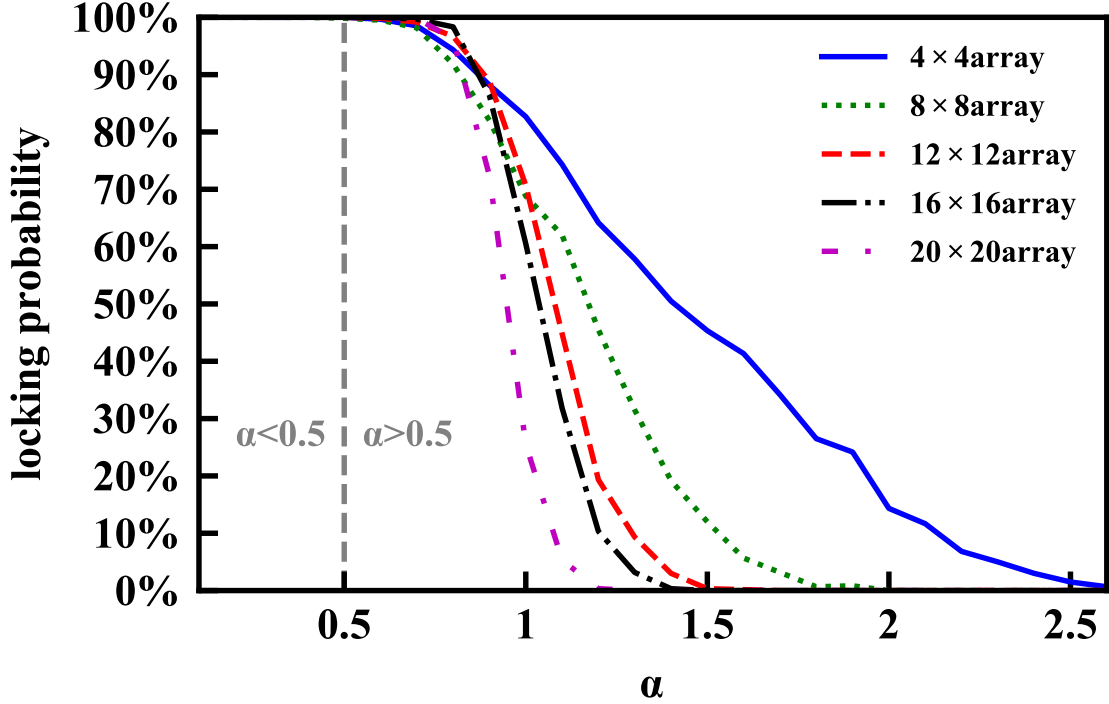
Figure 2.10: Probability of synchronization in the presence of element-to-element variation in the array. α represents random frequency variation relative to the locking bandwidth. For each array size, we run 500 iterations with random initial phases at a fixed θ ($\theta = 0$) to get the statistical result.

for $\alpha \geq 0.5$, the probability of synchronization in the combined array is smaller than the sub-arrays, as for the combined array to operate, all sub-arrays need to synchronize concurrently, and 2) for $\alpha < 0.5$, the array is synchronized regardless of the size. As a result, this proposed array guarantees synchronization for any array size as long as all variations are within $\pm \frac{K}{2}$.

Besides PVT variances in f_0 and K, other practical issues exist such as undesired

inter-coupling and across-chip interference. As a result, for future realistic hardware implementation, we need to co-design the chip-package solution, extract the high-frequency EM model, and incorporate the extra delays due to interconnects both on-chip and off-chip within the coupling model.

2.5 Summary

In this chapter, we present a novel technique for expanding the size of an array of actively coupled oscillators. We analytically derive the stable modes for an expanded network and demonstrate that the coupling behaviour is stable and predictable in a deliberately large array. Furthermore, we analyze transient dynamics and the scalability of the structure in the presence of element-to-element variations. We offer a promising solution for large scale signal distribution in phased arrays.

Chapter 3

Coupled PLL Array

3.1 Introduction

The growing interest in millimeter-wave phased arrays and massive MIMO, both part of the new wave of radios in 5G demand the deployment of large arrays for transmitters and receivers. Spatial diversity and multiplexing becomes effective when the number of elements in such arrays can scale to large numbers. While this is desirable, such benefits would only grow by size as long as the individual elements and their front end radios maintain their performance throughout this scaling. One of the most crucial components of both the transmitter and receiver with critical effect on overall system performance is the reference frequency, i.e. the LO. It is fundamentally difficult to share LO with a large number of elements without an inevitable degradation of the quality of the signal. This is a challenge that deepens as the number of elements and the physical

dimensions of the system increase [42]. The challenge of LO network design in mm-wave frequencies is two-fold: 1) creating low noise sources at higher frequencies and 2) distributing the source throughout the array with minimal degradation. Recently there is an increasing interest in developing mm-wave LO designs with focus on enhancing the phase noise of the source [46]. However, the challenge of LO distribution remains a major issue.

In the previous chapter, we approach this challenge by employing the injection locking of oscillators and propose a scalable COA scheme. We demonstrate that the COA could achieve frequency synchronization automatically despite of certain level of mismatches in oscillator free-running frequencies. However, the frequency calibration is still necessary in order to eliminate settled phase errors coming from frequency mismatches. Therefore, we would like to investigate alternative coupling methods for both frequency and phase synchronization. Besides injection-locked oscillators, prior studies have considered coupled PLL arrays (CPLLA) as an alternative solution to build scalable arrays as well [27, 28, 29, 19]. Those works commonly use type-I PLL as array element. Type-I PLL consists of phase detector, loop filter, voltage-control oscillator and frequency divider [30]. The open-loop transfer function of type-I PLL has finite gain at DC. Because of this finite loop gain, there is a monotonic relationship between the oscillator frequency and the phase difference between divided oscillator output and the reference. When multiple PLLs are connected in series and form a one-dimensional

CPLLA, tuning the oscillator free-running frequency changes the phase difference between adjacent oscillators in the chain. Although this type of CPLLA has desirable phase-tuning feature for beamformers, it has the following drawback. The frequency mismatch between oscillators from process, voltage and temperature (PVT) variance will be translated to phase error. In the presence of mismatch between different array elements, it can be shown that first order locking can compensate frequency mismatch but only at the expense of considerable phase mismatch between the elements.

In this chapter, we address this drawback from finite loop gain by employing type-II PLL as the array element due to its infinite dc loop gain. We propose a distributed phase locking mechanism where each PLL synchronizes with one of its nearest neighbors, alleviating the need to use a common reference. We introduce an architecture that 1) enables synchronization of frequency and phase locking at the presence of such non-idealities and 2) provides 2-dimensional scaling of the distributed PLL. The rest of the chapter is organized as follows: Section 3.2 presents the theoretical foundation of the proposed distributed PLL concept. Section 3.3 presents the circuit implementation of the architecture. Section 3.4 provides the prototype measurement result.

3.2   Array Architecture and Stability Analysis

The proposed system of distributed sources is based on a collection of independently operating local oscillators. In such a system, in the absence of proper synchronization, each of the sources will operate at their own free-running frequency and phase
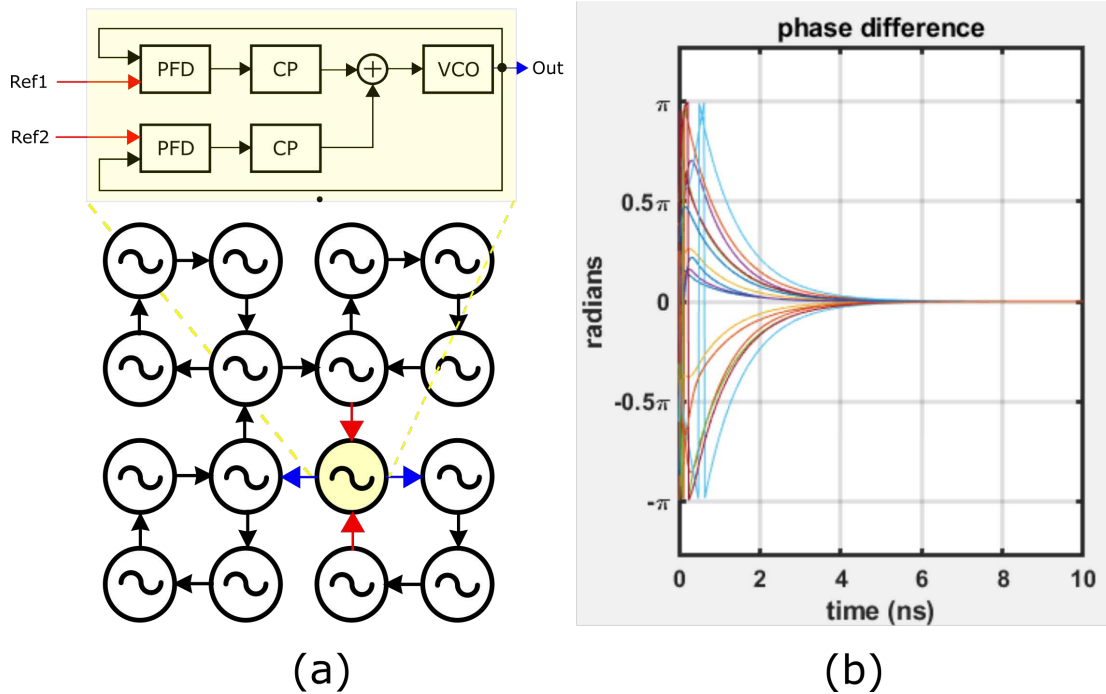
Figure 3.1: (a) Top: structure of the unit PLL, Bottom: a PLL array example. (b) Simulated phase locking of the distributed array.

undermining the coherent operation of the array. It is crucial to provide a mechanism to guarantee proper frequency synchronization between all the elements. One way to produce such synchronous behavior is by connecting all the units to a common external reference. However, such a method would also require distribution of such a reference across the entire array. Such a distribution would suffer from signal degradation effects similar to what we discussed earlier about normal LO distribution. Thus, we propose a frequency and phase locking method that would also scale with the structure in order to maintain scalability of the entire array.

The proposed distributed PLL as shown in Fig. 3.1.a is composed of a collection oscillators that connect to their nearest neighbor through local interconnects. Each oscillator unit is connected to its own local PLL. At the same time neighboring PLL's can connect to each other to provide phase and frequency synchronization between neighboring elements. Such method is merely based on local connections and would not require the reference signal to connect throughout the array. However, such a network of phase locking modules could result in an increasingly complex and unpredictable dynamic. We study how the locking mechanism is affected by the way PLL's connect to each other. Next we propose the interconnect structure that achieves desired locking dynamics in the network.

In order to understand the locking mechanism Fig. 3.1.a shows the linear model of a type II PLL that contains two separate inputs as the reference signal. We will demonstrate how two input references enable two-dimensional extension of the distributed array. At the presence of two inputs we can write the phase dynamics of the PLL as:

$$\ddot{\phi}_{out} = k_1 \dot{\phi}_{out} + k_2 \phi_{out} - \frac{k_1}{2}(\dot{\phi}_1 + \dot{\phi}_2) - \frac{k_2}{2}(\phi_1 + \phi_2),$$

where, ϕ_{out} is the output phase of the unit PLL and ϕ_1 and ϕ_2 are the input phases to the unit. k_1 and k_2 are coefficients that depend on the circuit parameters of the oscillator, charge pump and filter. Based on this equation we can derive the dynamical equations of the array. The dynamics of the array including the position of the poles depend on the way the individual elements of the array are connected to each other.

Based on this model, we can show that when the blocks are connected in particular

orientations, the entire system maintains stable regardless of the size of the array. Fig. 3.1.b demonstrates the time-domain simulations of the 2-D distributed structure in Fig. 3.1.a. As the results indicate when the phases start from random initial conditions the phase and frequency of all oscillators lock to a common value.

As the array size increases, the poles in the transfer function of the system proportionally increase. Due to the new poles, the settling dynamics of the array change with the number of elements. However, beside the transient response, at steady state all the LO's are phase locked and frequency locked to the desired reference. While the in-band noise performance does depend on the specifics of the PLL position in the array, out-of-band phase noise of the oscillators all follow the free-running frequency of the VCO regardless of the size of the array and the position of a particular oscillator inside the array. This ensure the array can scale while maintaining the same LO quality across all elements.

3.3   Circuit Design and Implementation

In order to demonstrate the proposed concept we consider a design that includes multiple independently controlled unit PLLs that connect together in various configurations. Fig. 3.2 demonstrates the proposed architecture. The outputs of the divider chain in all the unit blocks connect to a common multiplexer. The multiplexer has twice as many outputs as inputs. This ensures that each unit cell gets two different input references from this block. Digital control of the multiplexer enables the output from a unit cell

to connect to any input of any other unit cell.

An external reference also connects to the input of this mux to provide frequency control of the entire array. The digital interface enables the unit cells to configure in various forms. In the simplest form, both inputs of all PLLs can connect to the external reference. This reduces the array into a collection of standard phase locking units. Furthermore, it is possible to connect the output of this unit to the two inputs of the next unit. This becomes a basic 'daisy chain' configuration of the distributed PLL. It is also possible to connect the inputs of the PLL from two different outputs. For instance the inputs can be coming from two other PLLs or from one PLL and external reference. As we show in the next section this enables 2-dimensional array structures.

The VCO is designed to operate at 28GHz based on the standard cross-coupled pair. Continuous frequency tuning is achieved by adjusting the size of the varactor in the LC tank. A capacitor bank with 16 different configurations ensures that the oscillator frequency can tune by more that 10% around its center frequency. This tuning range ensures that all oscillators can lock together despite any undesired mismatch between them.

Fig. 3.3 shows the circuit details of the unit PLL. The output of the VCO connects to a buffer which is used for monitoring the output. A second buffer connects this output to the front-end of the divider chain. The high frequency dividers are designed based on common source master-slave D type flip flops. In order to ensure optimum power consumption, the lower frequency dividers are scaled in size and power.
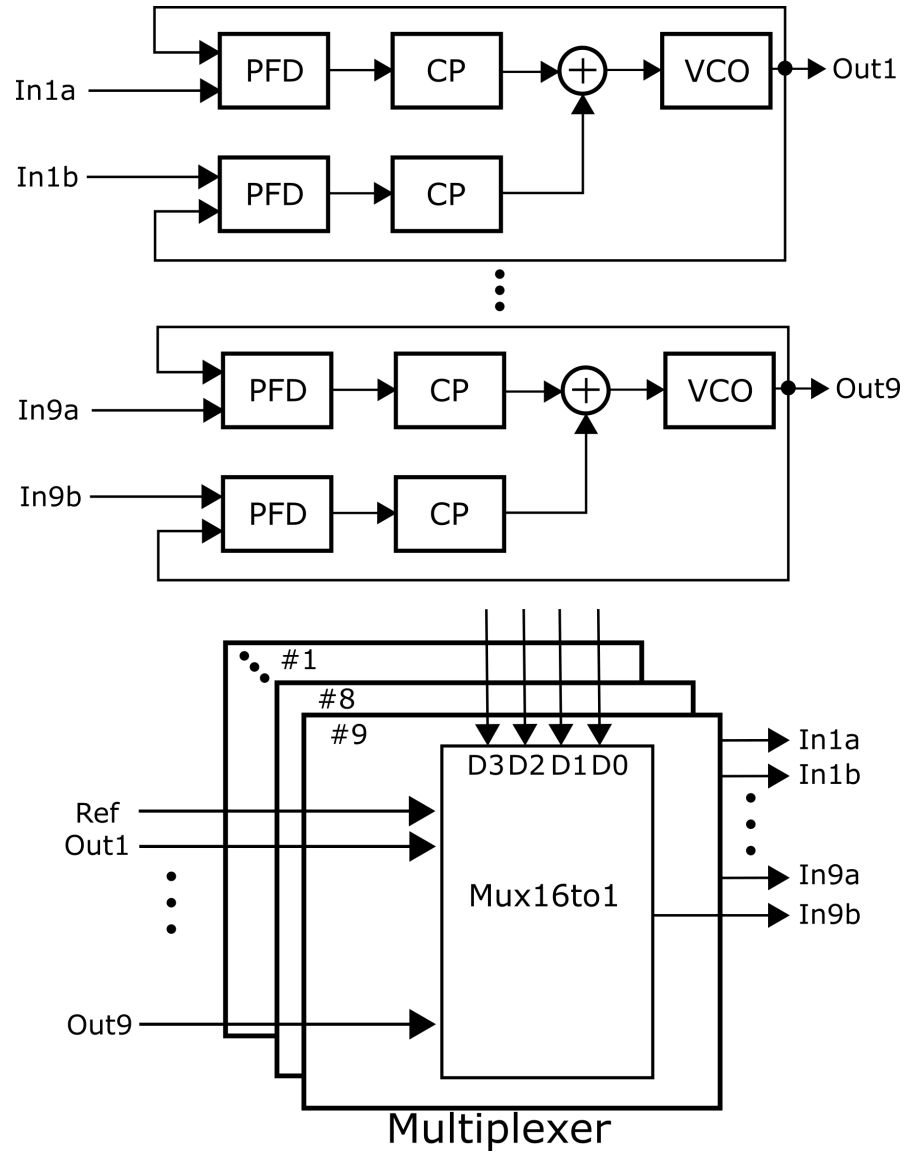
Figure 3.2: Top level block diagram of the distributed PLL with re-configurable interconnects.
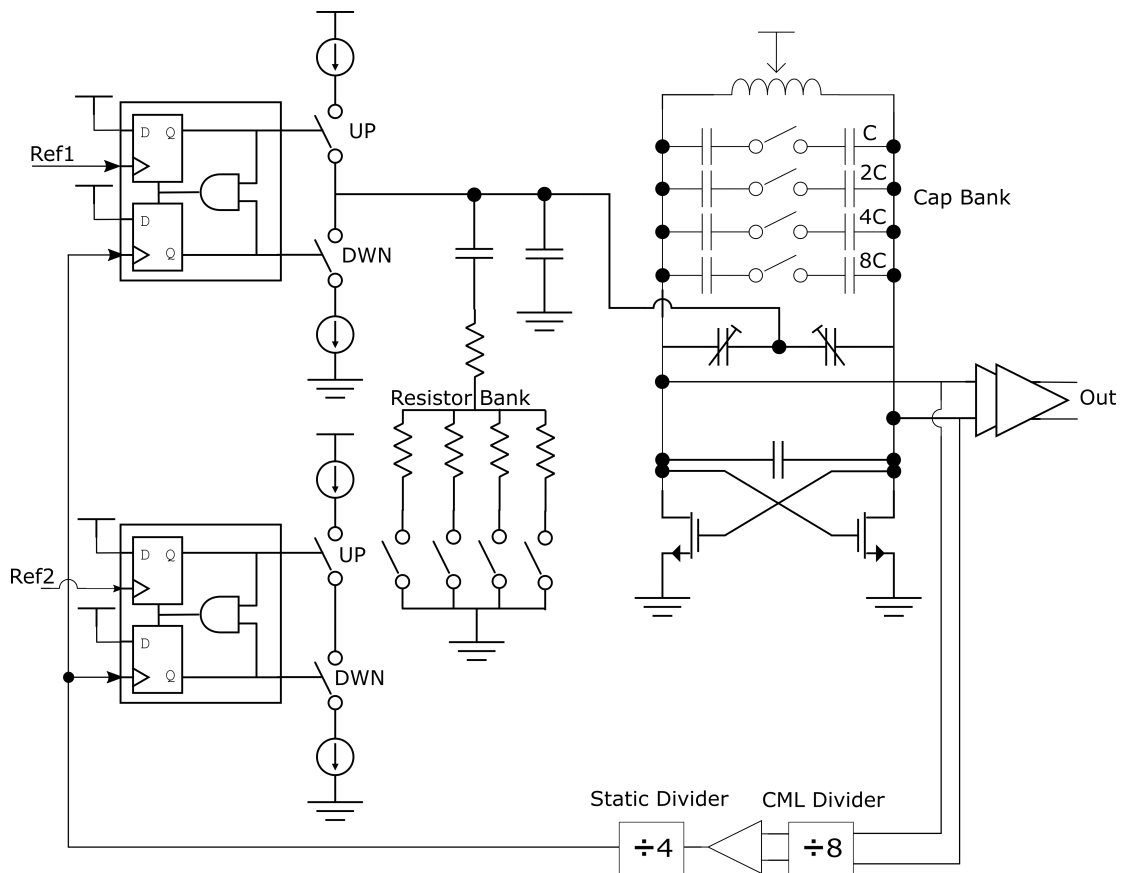
Figure 3.3: Unit PLL circuit.

Each PLL module contains two phase and frequency detectors (PFD's) followed by two charge pumps. The charge pump and PFD are designed to operate up to 1GHz. Proper sizing of the charge pump devices and adjusting the delay paths in the PFD ensure minimum phase error throughout the operation. Digitally controlled resistors in the loop filter enable digital control over the damping factor of the PLL. The outputs of the charge pumps add together in current mode and are then fed into the loop filter in accordance with the diagram in Fig. 3.1.a.

3.4   Prototype Measurement

The chip is fabricated in the TSMC 65nm CMOS process. The die photo of chip is shown in Fig. 3.4. To measure the chip, the digital interface and the supplies are wirebonded to a QFN package. The external reference for the array is centered around 875MHz and is fed through RF probes to the digital multiplexer. The chip contains 9 oscillators, however due to measurement limitations we simultaneously measure a maximum 4 oscillators in any configuration which we label as PLL_1 to PLL_4. The output of PLL_4 is connected through RF probes to an R&S FSW67 spectrum analyzer for measurement.

Each PLL consumes a total of 37mW where the VCO consumes 17mW and the divider chain including the input buffer consume 20mW. The power consume by the multiplexer and the rest of the blocks are negligible. Fig. 3.5 shows the measured spectrum of PLL_4 when all other PLL's are separated and are operating independently.
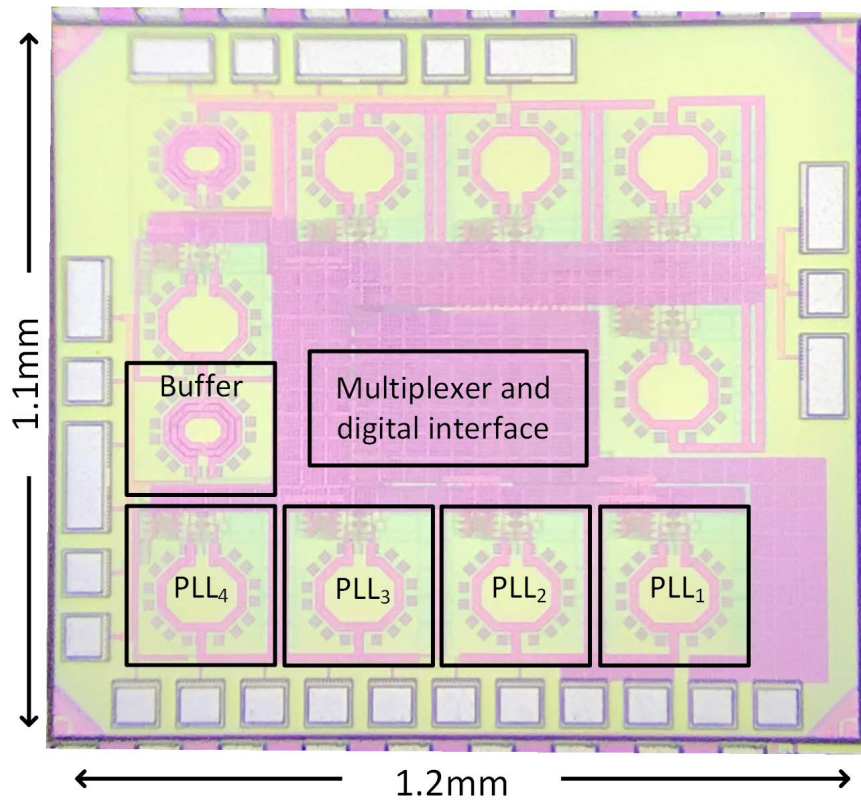
Figure 3.4: Chip microphoto.
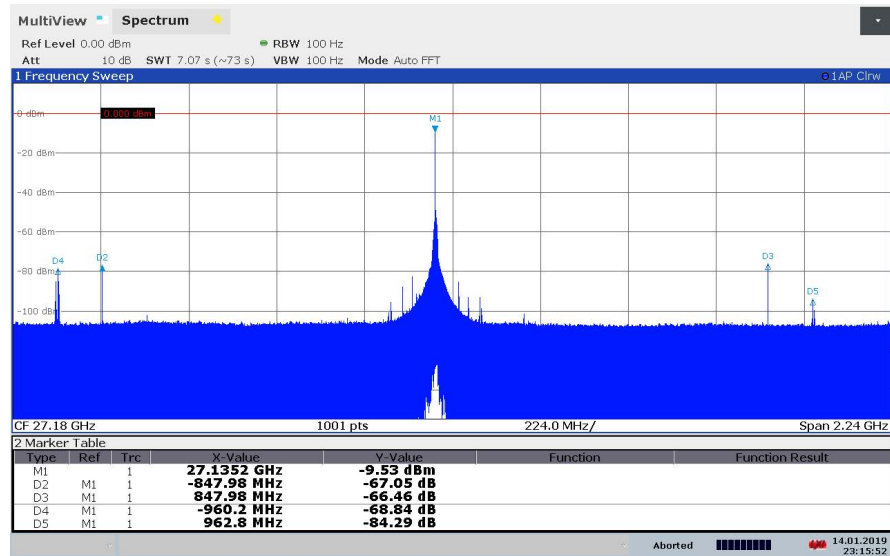
Figure 3.5: Measured spectrum and reference spurs in the stand-alone PLL.

The reference spur is -66.5dBc with respect to the carrier frequency.

The chip is configured in several different structures and the spectrum and phase noise are measured accordingly. The six structures that we report include 1) stand alone PLL's connected to the reference, 2) three different daisy chain configurations with different length, and 3) two 2-dimensional structures with 3 and 4 PLL's. Fig. 3.6 plots the measured phase noise of the six different configurations. The second category (daisy chain) and the third category (triangular and rectangular loops) are the basic building blocks that can further extend the array in one dimension and two dimensions, respectively.

When all the PLL's are connected to the external reference (first configuration), the phase noise at 1MHz and 10MHz offset are -100.3 dBc/Hz and -111.4 dBc/Hz
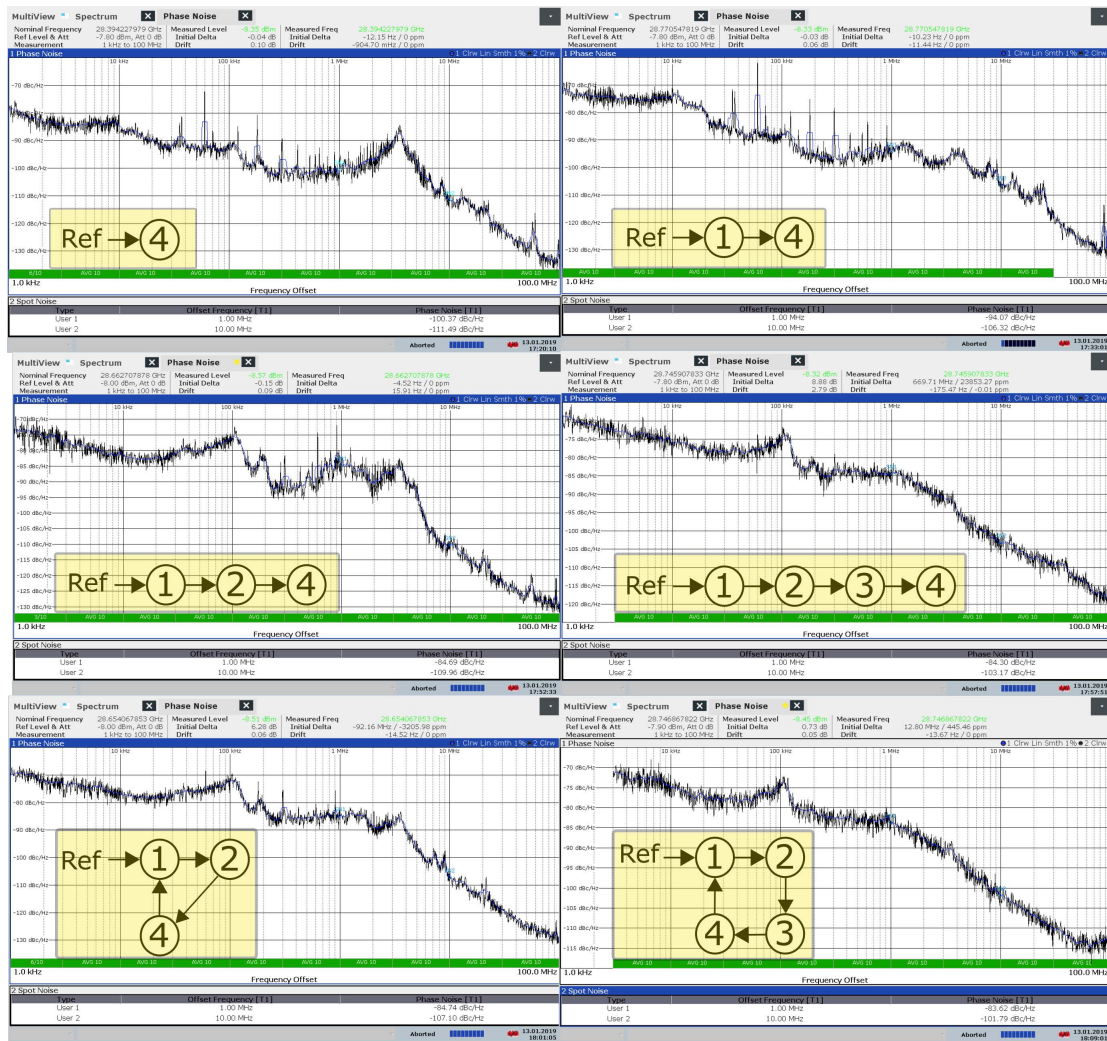
Figure 3.6: Measured phase noise plot for 6 different array configurations: direct connection, 3x daisy chains, triangular and rectangular loops.

Table 3.1: Measured phase noise for different array configurations at 28GHz.

Array configuration and no. of PLLs	PN@1MHz (dBc/Hz)	PN@10MHz (dBc/Hz)
Unit PLL	-100.3	-111.4
2 element daisy chain	-94.1	-106.3
3 element daisy chain	-84.7	-109.9
4 element daisy chain	-84.3	-103.2
Triangular loop	-84.7	-107.1

respectively. The the measured phase noise of all the configuration are summarized in Table. 3.1. Since the simulated bandwidth of the PLL is 2.6MHz, the 1MHz offset measurement corresponds to in-band phase noise while the 10MHz represents out-of-band phase noise.

We observe that the in-band phase noise is the lowest when the PLL's are directly connected to the reference and increase with more number of PLL's connected to each other in the different configurations. This is expected as the quality of the reference signal degrades as it passes through multiple units. However, as opposed to regular daisy chaining, the out-of-band phase noise doesn't show significant degradation among the different configurations. In other words, the out-of-band noise (beyond 2.6MHz offset

frequency) is not affected by the number of elements in the distributed array structure. The demonstrated daisy chaining and triangular structures are basic building blocks that can further extend to large 1D and 2D array structures.

While the in-band noise degradation does degrade the integrated noise across the entire frequency band, it is worth noting that for a mm-wave signal source at 28GHz, the signal bandwidth is at least two orders of magnitude larger than the designed PLL bandwidth of 2.6MHz. As a result, at high date rates with more that 100MHz bandwidth, the out-of-band phase noise is the dominant factor in determining the performance of the wireless system.

3.4.1   Stability Analysis Considering Magnetic Coupling

In measurement, we observe the degradation of phase noise when we integrate more PLL elements into the CPLLA. The array eventually lost frequency locking when the number of elements is larger than four. This chip measurement result contrasts with the expectation from the circuit simulations. The reason is that magnetic coupling between inductors is not included as part of the considerations during the design phase. The coupling between oscillators introduces the additional phase tuning mechanism besides the prior phase control by the PLL loop. The two mechanisms have conflicting effects on phase, and introduce unsettling of the voltage level on the oscillator control node. As a result the phase noise is degraded, and furthermore, the array might not able to be frequency locked at all.
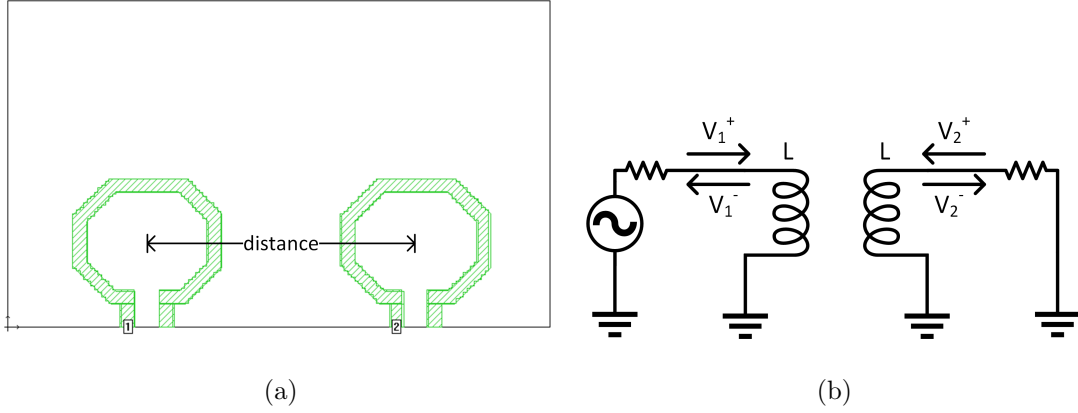
Figure 3.7: (a) EM modeling of two adjacent on-chip inductors in SONNET. (b) Equivalent circuit model.

To examine this explanation, we study the the magnetic coupling effect quantitatively. First, the coupling between inductors is estimated by modeling the mutual inductance, as shown in Fig. 3.7a. In this test bench, inductors have the same dimension, spacing and substrate stack up with the inductors used in the chip design. Assuming the inductance of each inductor is L, and the coupling coefficient is k. Based on the equivalent circuit model as shown in Fig. 3.7b, we can calculate k by:

$$k = \frac{kL\frac{\mathrm{d}I_1}{\mathrm{d}t}}{L\frac{\mathrm{d}I_1}{\mathrm{d}t}} = \frac{V_2}{V_1}. \tag{3.1}$$

Further, we can calculate the value of k based on S parameters:

$$k = \frac{V_2}{V_1} = \frac{V_2^-}{V_1^+ + V_1^-} = \frac{S_{21}V_1^+}{V_1^+ + S_{11}V_1^+} = \frac{S_{21}}{1 + S_{11}}. \tag{3.2}$$

Based the simulated S parameters and equation (3.1), we calculate the coupling coefficient as a function of the distance between the centers of adjacent inductors, as shown
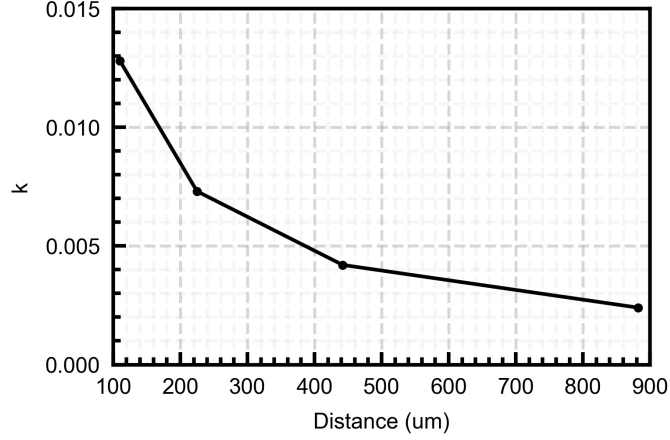
Figure 3.8: The coupling coefficient, k, is inversely depended on the distance between the adjacent inductors.

in Fig. 3.8. Consistent with intuition, the coupling coefficient is inversely dependant on the distance, and the drop of k roughly follows an exponential curve as the distance increases. As a result, the on-chip magnetic coupling is dominant between inductors of the neighboring oscillators. Since the distance between the on-chip neighboring inductors is 250μm, we estimate that k is around 0.007.

To study the system-level effect of the magnetic coupling, we perform the top-level circuit simulation of a 1×4 CPLLA. Since there are two phase control mechanism coexisting in the array: (1) magnetic coupling and (2) PLL control loop, we study their effect separately to learn their effect distinctively. Fig. 3.9a presents the settled transient phase of each PLL element fully controlled by the PLL loop, which means
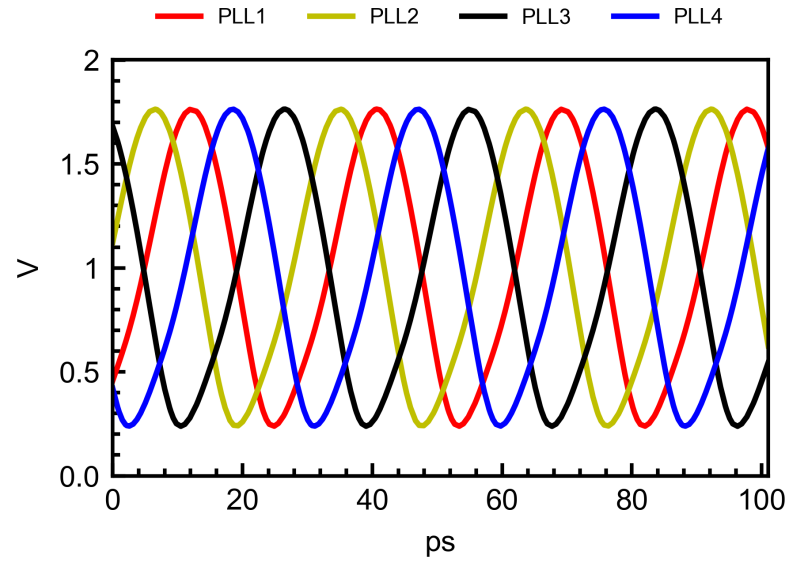
(a)
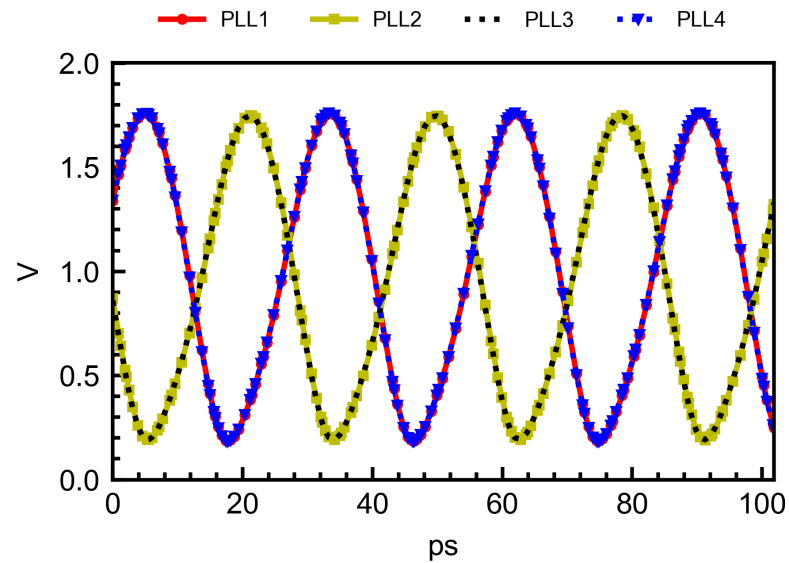
(b)

Figure 3.9: (a) Transient phase of element 1-4 inside a 1×4 CPLLA after the array settles into steady state. The magnetic coupling is not included in the simulation. (b) Transient phase of VCO element 1-4 inside a 1×4 array after the array settles into steady state. The magnetic coupling are modeled between each pair of adjacent inductors with k=0.007, but all PLL control loops are disabled.

the magnetic coupling is not enabled. Due to the charge pump mismatch and non-ideal effects from other circuit blocks, there is some phase delay at each stage, but the delay are fairly consistent between stages. In comparison, Fig. 3.9b presents the transient phase behavior fully controlled by the magnetic coupling, where the PLL loop of each element is disabled. Here the magnetic coupling are modeled between each pair of adjacent inductors, and $k=0.007$. It results in a different phase dynamics, where PLL1 have the same phase with PLL4, and PLL2 and PLL3 share a different phase. This is because the PLL2 and PLL3 are the center element inside the 1×4 array, subjecting to more injection coupling compared to boundary elements PLL1 and PLL4. The oscillators of PLL2 and PLL3 therefore have higher resonant frequency (due to smaller inductance), and the phase of PLL2 and PLL3 would lead PLL1 and PLL4, based on Adler's equation. As a result, we find that the two phase control mechanisms want to settle in different steady states, and would cause conflict in which phase to settle and impair the stability of the system when they coexist. This is confirmed in transient simulation as shown in Fig. 3.10. When the magnetic coupling coexists with the PLL operation, the control node voltage doesn't settle which means the array is not stable and doesn't lock in phase and frequency. Based on the conclusion, we find that there are two directions that can be investigated to avoid the stability challenge in the future endeavor: (1) within the same phase control scheme, reduce the magnetic coupling with circuit techniques such as using on-chip magnetic shielding or increase the distance between inductors. However, this doesn't solve the problem fundamentally

and comes at cost of extra on-chip space. (2) change the array scheme where there is only one phase control mechanism. In the next chapter, we follow direction (2) and proposes the updated version of the array with details.

3.5   Summary

This chapter demonstrates a distributed framework for phase and frequency locking of multiple mm-wave oscillators. We present the concept of phase locking between multiple oscillators and present a chip prototype of the PLL at 28GHz. The measurements verify that out-of-band phase noise of the distributed array does not depend on the number of elements in the array. However, we find that the array faces both in-band phase noise degradation and stability issue due to the conflicting between the PLL phase control and magnetic injection coupling. In order to solve the problem, we come up with direction of the next step and will provide our following up work with more details in the next chapter.
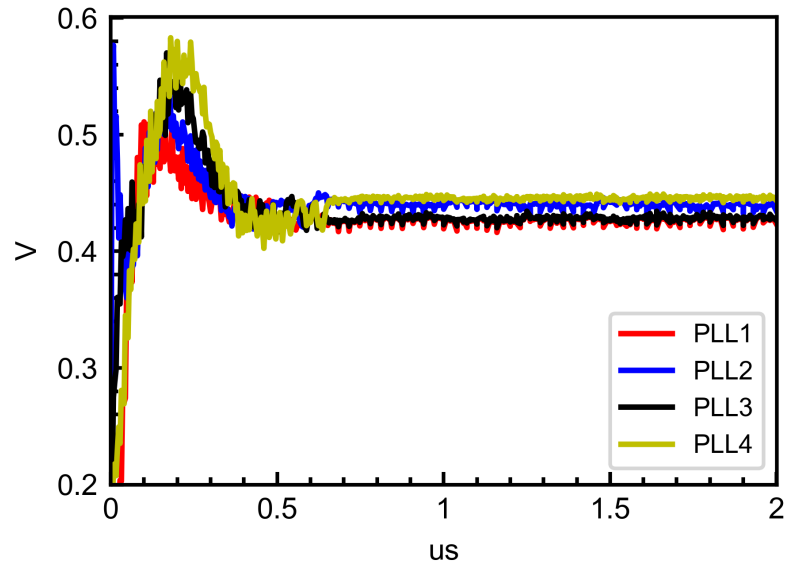
(a)
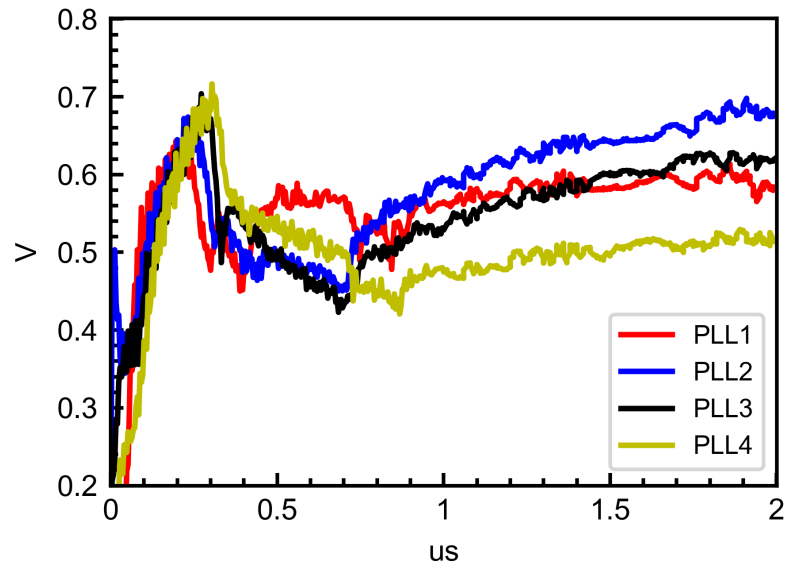
(b)

Figure 3.10: Transient waveform at the control node of each PLL inside a 1×4 CPLLA. (a) PLL operates without the magnetic coupling. (b) The magnetic coupling is included besides the PLL operation.

Chapter 4

Autonomous Array of Phase Self-alignment

4.1 Introduction

In chapter three, the multi-LO array uses PLL as unit element which has several limitations at mm-wave frequencies. First, any residual phase error from the loop operation is multiplied by the frequency division factor. This is because logic-based phase detectors work at the frequency of the reference signal. As a result, the mm-wave source would be locked to the reference signal but with a significant and unpredictable phase. Second, the unpredictable phase tracking imposed by the loop would be conflicted to a secondary coupling mechanism and threaten the phase/frequency synchronization. We show that with the presence of magnetic coupling between neighboring oscillators, the array has
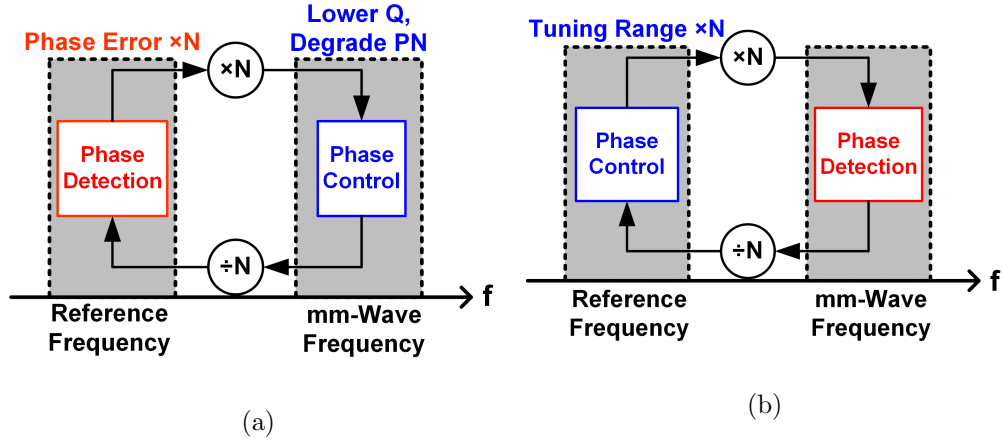
Figure 4.1: Two schemes for mm-wave signal generation: (a) The conventional scheme detects phase at the reference frequency and controls it at the mm-wave frequency. (b) The scheme proposed in chapter four detects phase at the mm-wave frequency and controls it at the reference frequency.

worse in-band phase noise as the number of PLL elements increases until eventually the frequency locking is lost. Third, tuning the frequency and phase of a mm-wave PLL involves the use of varactors or switched-based components, which degrades the resonator quality factor and the spectrum purity of the PLL.

In this chapter, we will explore the method of mm-wave signal generation and distribution based on the topology shown in Fig. 4.1b. In the new scheme, we detect the phase at the target mm-wave frequency while phase control occurs at the lower frequency of the input reference. By effectively switching the location of detection and control we simultaneously avoid both above challenges: First, by controlling phase at

the reference frequency, we avoid direct control of the resonator resulting in optimal frequency and spectral purity. Second, by directly measuring the phase at the mm-wave band, we prevent phase ambiguity and enable accurate phase alignment.

The rest of the chapter is organized as follows: Section 4.2 and Section 4.3 present the proposed interferometer for mm-wave phase sensing and phase detector design. Section 4.4 presents the architecture of the scalable phased arrays with phase self-alignment abilities. Section 4.5 presents the circuit implementation of the architecture. Section 4.6 shows the prototype measurement results and provide the discussion and comparison with other state-of-work prior works.

4.2   Interferometer-based Phase Sensing

First invented by Albert Michelson and used in the Michelson-Morley experiment [47], interferometers have been widely used ever since in science and engineering fields including in optical physics [48, 49] and electrical signal processing [50, 51, 52]. Interferometers work by merging multiple electromagnetic waves to create an interference pattern that contains information about the object being studied. In this work and based on the interferometric concept, we propose a method to directly measure the phase difference between two mm-wave signal sources. As shown in Fig. 4.2, a reference source and a target oscillator simultaneously drive a transmission line's left and right terminals. The two sources can have the same or opposite polarities in this scheme. These two scenarios are depicted in Fig. 4.2a and Fig. 4.2b, respectively.   To analyze the behavior of the
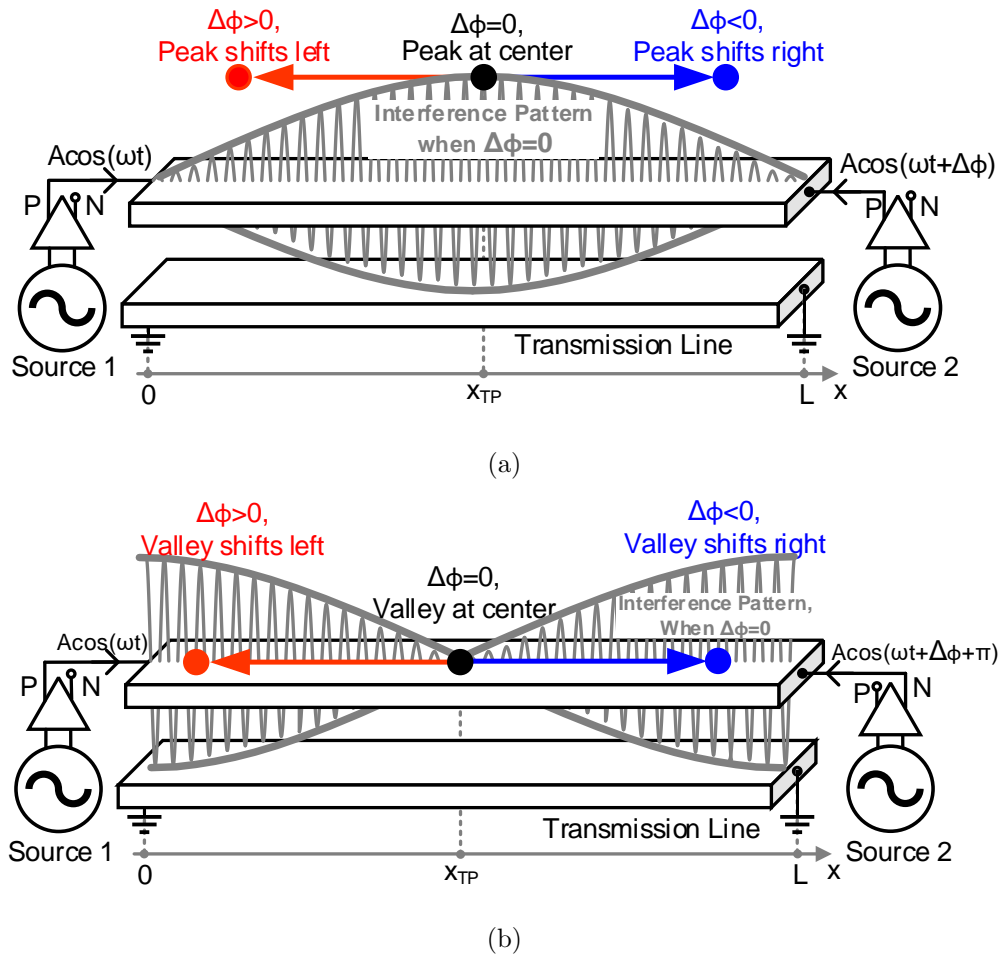
Figure 4.2: Proposed interferometer: (a) Connected with the same polarity, two mm-wave sources would generate an interference pattern with a peak on the transmission line. (b) Connected with the opposite polarity, the generated interference pattern has a valley. The position of the peak or valley shifts along the line as a function of $\Delta\phi$.
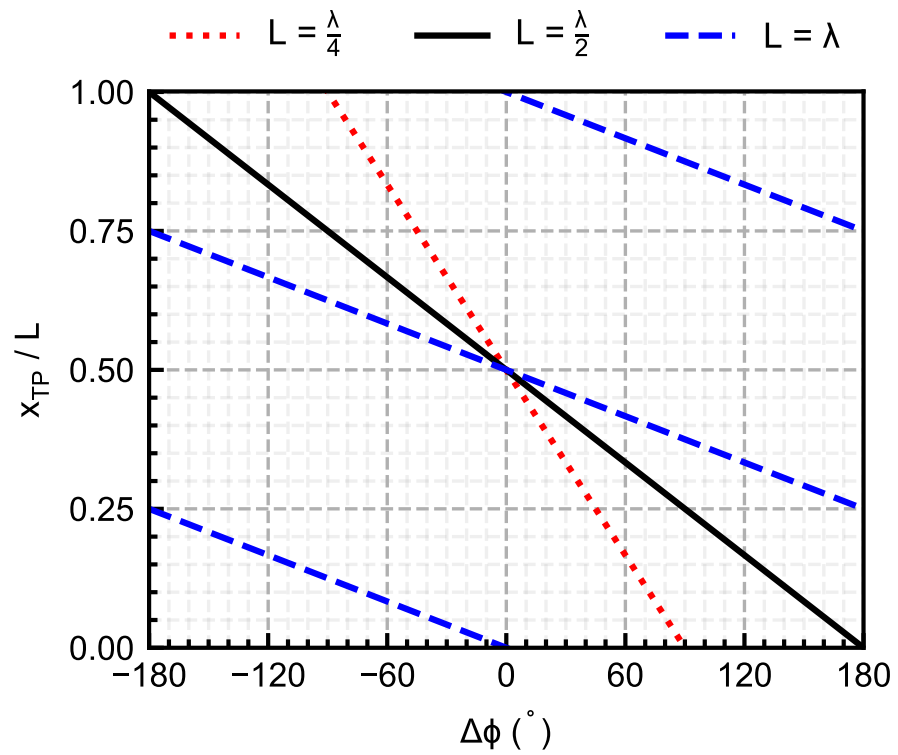
Figure 4.3: The normalized location of the turning point as a function of $\Delta\phi$ for three different lengths of the transmission line: $\lambda/4$, $\lambda/2$, and λ.

interference pattern, we assume the left and right sources are impedance matched to the transmission line and have the same amplitude and frequency. The reference source on the left would generate a traveling wave along the transmission line propagating from left to right:

$$S_L(x,t) = A\cos(\omega t - \beta x), \ \ 0 \le x \le L, \tag{4.1}$$

whereas the oscillator on the right generates a traveling wave propagating from right to left:

$$S_R(x,t) = A\cos(\omega t + \beta x - \beta L + \Delta\phi). \ \ 0 \le x \le L, \tag{4.2}$$

Here, A and ω are the amplitude and the angular frequency of the two signal sources, β is the phase constant of the traveling waves and L is the length of the transmission line. We define $\Delta\phi$ as the phase difference between the oscillator connected to the right end of the transmission line with respect to the reference source on the left side. The two traveling waves propagating in the opposite directions would interfere and generate a standing wave along the transmission line. A standing wave results from the summation of (4.1) and (4.2):

$$S(x,t) = S_R(x,t) + S_L(x,t). \tag{4.3}$$

We get two specific patterns depending on the relative polarity between the two sides. When the two sides have the same polarity, we get:

$$S(x,t) = 2A\cos(\beta x + \Delta\phi')\cos(\omega t + \Delta\phi'), \tag{4.4}$$

$$\Delta\phi' = \frac{1}{2}(\Delta\phi - \beta L), \qquad (4.5)$$

while for the opposite-polarity scenario, the wave equation becomes:

$$S(x,t) = 2A\cos[\beta(x + \frac{\lambda}{4}) + \Delta\phi']\cos\left(\omega t + \Delta\phi' + \frac{\pi}{2}\right). \qquad (4.6)$$

In the same-polarity scenario, the term $2A\cos(\beta x + \Delta\phi')$ in (4.4) represents the envelope of the interference pattern distributed across the transmission line as a function of $\Delta\phi$. When $\Delta\phi = 0$, the peak of the interference pattern appears at the center of the transmission line, as shown in Fig. 4.2a. As $\Delta\phi$ changes, this peak would move to the left for $\Delta\phi > 0$ or the right for $\Delta\phi < 0$. As shown in Fig. 4.2b, the same dynamic occurs in the opposite-polarity scenario, whereas (4.6) indicates the interference patterns generates a valley at the same place.

From (4.4-4.5), we calculate x_{TP}, the coordination of this *turning point*[1]   to be:

$$x_{\text{TP}} = \frac{L}{2} - \frac{\Delta\phi}{4\pi}\lambda + \frac{k}{2}\lambda, \qquad (4.7)$$

$$k = 0, \pm 1, \pm 2, \cdots, \quad 0 \le x_{\text{TP}} \le L.$$

From (4.7), due to their linear relationship, one can predict the phase $\Delta\phi$ by directly measuring x_{TP}. As shown in Fig. 4.3, when the two sources are in phase, the turning point appears at the center of the transmission line and shifts away when there is a non-zero phase difference between the two sources. Furthermore, we can make the following two observations from Fig. 4.3. First, the turning point appears periodically

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[1]   In the case of same-polarity, the turning point is defined as the location of the peak, while in the case of opposite-polarity, it is the valley's location.
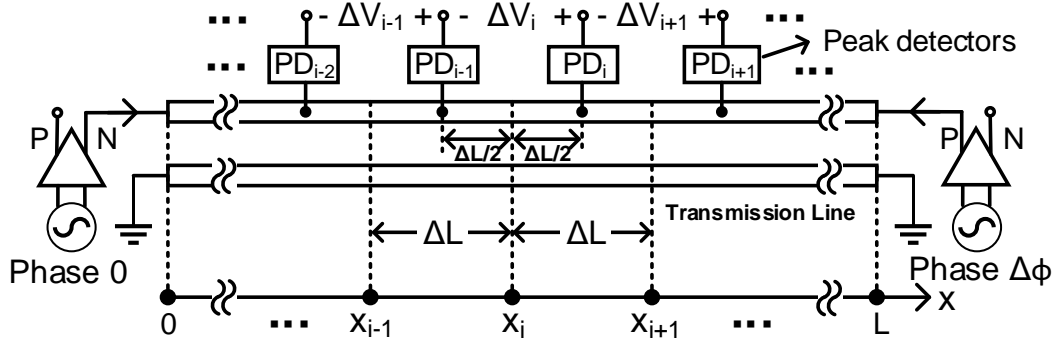
Figure 4.4: Diagram of the proposed phase detector based on multiple peak detectors distributed along a transmission line.

every half-wavelength. To ensure one-on-one mapping between x_{TP} and $\Delta\phi$, the length of the transmission line, L should not exceed half the wavelength. Second, since the measurable values of x_{TP} are restricted to $[0, L]$, L determines the detectable range of $\Delta\phi$. Based on (4.7), this is:

$$-\frac{2\pi L}{\lambda} \leq \Delta\phi \leq \frac{2\pi L}{\lambda}. \tag{4.8}$$

As a result, if one uses the maximum allowable length of $\lambda/2$, the interferometer detects the entire 2π range of $\Delta\phi$. Assuming there are P phase detectors evenly distributed across the line, the phase detector can adjust the phase difference between the two sources at increments of $\Delta\phi/(P-1)$.

4.3   mm-Wave Phase Detector

The proposed interferometer provides a direct mapping between phase and x_{TP}. Based on this mechanism and by measuring the position of x_{TP} in the transmission line we implement a mm-wave phase detector. As shown in Fig. 4.4, a series of peak detectors are evenly distributed across the transmission line. The distance between the ith and $(i-1)^{th}$ peak detectors is ΔL ($\Delta L \ll L$), and x_i refers to their mid-point location.

The peak detector converts the mm-wave input signal of an amplitude V_{in} into a DC output, V_{out}. Using linear expansion, this conversion can be estimated as:

$$G_{PD} = \frac{\mathrm{d}V_{out}}{\mathrm{d}V_{in}}, \tag{4.9}$$

where G_{PD} represents the RF-to-DC gain of the peak detector.

Next, we select the pair of peak detectors located at $x_i \pm \Delta L/2$ and measure ΔV_i, the voltage difference between their outputs. When the selected pair of peak detectors produces $\Delta V_i = 0$ we can conclude that $x_{TP} = x_i$. When the $\Delta\phi$ changes, it pushes x_{TP} away from x_i and changes ΔV_i accordingly.

First, we analyze the relationship between ΔV_i and $\Delta\phi$ under a special case, $x_i = L/2$. In the same-polarity scenario, we derive ΔV_i to be:

$$\Delta V_i = \begin{cases} K\cos\left(\frac{\phi_o}{2}\right)\cos\left(\frac{\Delta\phi}{2}\right), -\phi_o \leq \Delta\phi + \pi \leq \phi_o, \\ -K\sin\left(\frac{\phi_o}{2}\right)\sin\left(\frac{\Delta\phi}{2}\right), \phi_o < \Delta\phi + \pi \leq 2\pi - \phi_o, \end{cases} \tag{4.10}$$

where $K = 4G_{PD}A$, and $\phi_o = \beta\Delta L$.
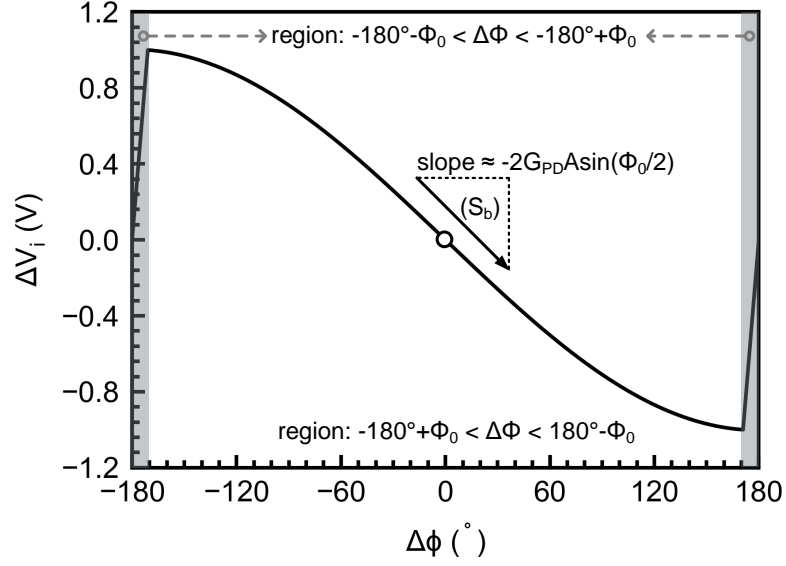
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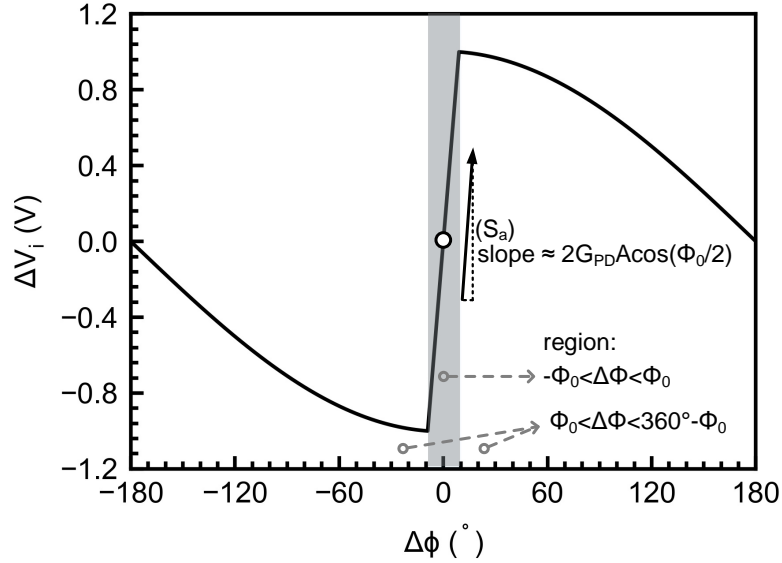
(b)

Figure 4.5: Characteristic of the proposed phase detector: (a) The theoretical relationship between $\Delta\phi$ and ΔV_i in the same-polarity scenario when $x_i = \frac{L}{2}$. (b) Theoretical relationship between $\Delta\phi$ and ΔV_i in the opposite-polarity scenario when $x_i = \frac{L}{2}$.
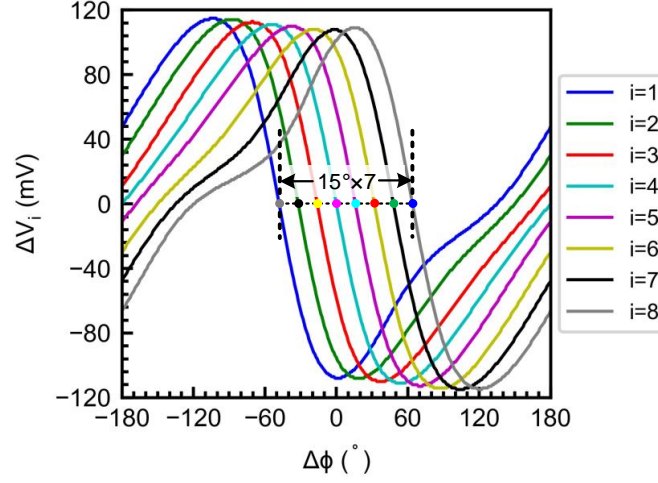
Figure 4.6: The simulated ΔV_i as a function of $\Delta\phi$ with opposite polarity connection, where i represents a specific pair of peak detectors.

Fig. 4.5a depicts this relationship between ΔV_i and $\Delta\phi$. Likewise, the opposite-polarity scenario results in:

$$\Delta V_i = \begin{cases} K \cos\left(\frac{\phi_o}{2}\right) \sin\left(\frac{\Delta\phi}{2}\right), & -\phi_o \leq \Delta\phi \leq \phi_o \\ K \sin\left(\frac{\phi_o}{2}\right) \cos\left(\frac{\Delta\phi}{2}\right). & \phi_o < \Delta\phi \leq 2\pi - \phi_o, \end{cases} \tag{4.11}$$

which is depicted in Fig. 4.5b. By comparing these two scenarios, we find that the $\Delta\phi$-to-ΔV_i characteristic of the two cases only differs by a phase shift of π. Furthermore, ΔV_i has two zero-crossings across $\Delta\phi$. From the above equations, we can approximate the slope at these two zero-crossings to be $S_a = K/2 \cos(\phi_o/2)$ and $S_b = -K/2 \sin(\phi_o/2)$, which for $\beta\Delta L \ll 1$ can be further simplified to $S_a = K/2$ and $S_b = -K\beta\Delta L/4$.

When comparing these two zero-crossings, a larger slope provides a higher small

signal conversion gain in the $\Delta\phi$-to-ΔV_i relationship. This in term results in a pro-portionally higher phase sensitivity and lower phase error. Since $S_a \gg S_b$, it is the desirable zero-crossing for phase detection. From Fig. 4.5, the location of S_a depends on the polarity of excitation. For the opposite-polarity case, S_a occurs at $\Delta\phi = 0$, while for the same-polarity case, S_a occurs at $\Delta\phi = \pi$. Since phase tuning normally occurs around $\Delta\phi = 0$, the opposite-polarity mode provides superior performance.

In the general case where the chosen x_i is any value within $[0, L]$, we can use equation (4.6) to derive a modified equation for the location of the zero-crossings. The zero-crossing corresponding to S_a appears at:

$$\Delta\phi = 2\beta(x_i - \frac{L}{2}), \tag{4.12}$$

where in the special case of $x_i = L/2$ we considered earlier, this results in the zero-crossing at $\Delta\phi = 0$. Based on this general relationship, we propose the topology in Fig. 4.4 to measure $\Delta\phi$ based on the measured ΔV_i from the chosen pair of detectors. In this scheme, by selecting a specific pair among the available sets of evenly distributed detectors along the line we can program the zero-crossing of the phase detector to our desired value.

Fig. 4.6 shows circuit simulation results of the proposed phase detector with pro-grammable phase characteristic. The S_a is negative at the zero-crossing in Fig. 4.6 because of the negative conversion gain of the implemented peak detectors. Further-more, eight different settings for zero-crossings are selected from nine peak detectors distributed on a transmission line. The proposed mm-wave phase detector has several

advantages over conventional logic-based phase detectors. First, by measuring the phase difference directly at the target frequency, the proposed phase detector avoids the phase error multiplication effect in Fig. 1.2a. Second, this new method is more power efficient for mm-wave detection because it replaces the power-hungry active modules such as frequency dividers and sub-sampling switches in conventional PLLs with a direct mm-wave to DC conversion module. Finally, employing a transmission line as the core sensing component connecting the adjacent sources absorbs any delay due to signal routing into the phase measurement.

4.4   Array Architecture

We propose a mm-wave scalable phase synthesizer based on the methodology shown in Fig. 4.1b. In this scheme, the phase is detected at the target mm-wave frequency and controlled at the frequency of the input reference signal. First, we employ the interferometer-based phase detector to directly measure the phase difference between the two mm-wave sources without any frequency division. Next, we use a phase shifter operating at the reference frequency to achieve phase alignment between the two mm-wave sources based on the measured phase difference.

In Fig. 4.7a, we present the architecture of a two-element array featuring the proposed phase self-alignment. The mm-wave source is implemented using a $\times M$ frequency multiplier from the reference signal. Alternatively, the oscillator could serve as the mm-wave source and fit in the phase self-align scheme as well. However, we choose the
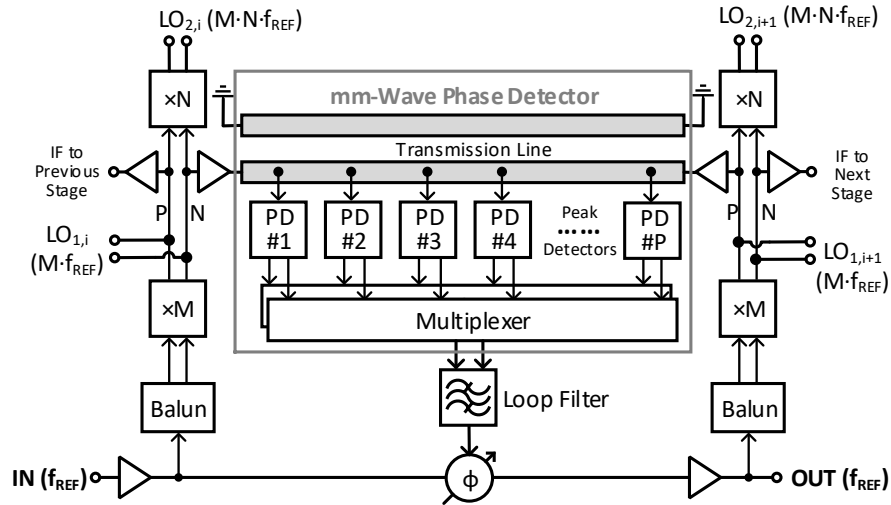
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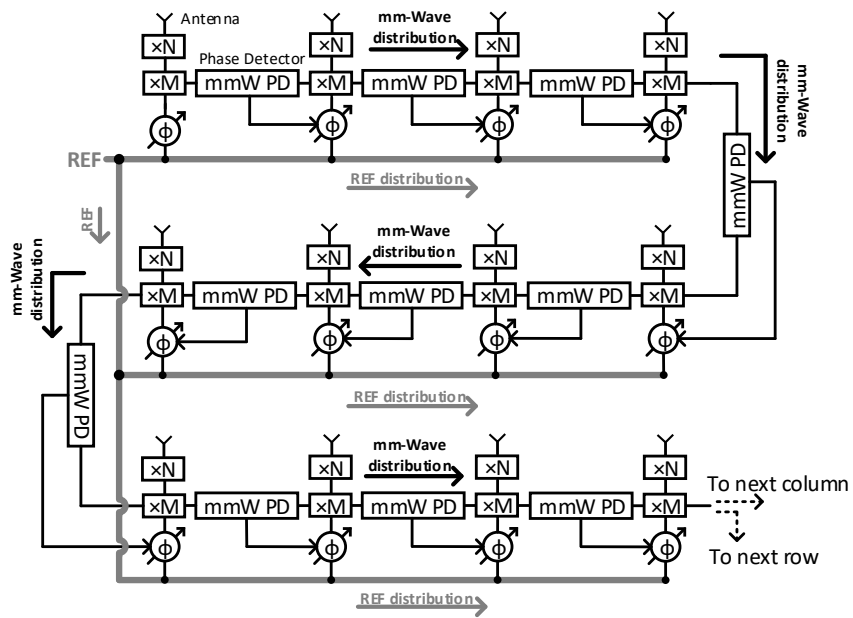
(b)

Figure 4.7: (a) The architecture of a 1×2 array with phase self-alignment. (b) A scalable phased array based on this concept.

frequency multiplier for practical consideration to avoid the potential conflict between injection locking and phase-align loop operation that we experience and explained in the previous sections. Here in this version of the circuit, the frequency at the input and output of the frequency multiplier is f_{ref} and $M \cdot f_{ref}$, respectively. The outputs of the two $\times M$ frequency multipliers in the array are synchronized in frequency. However, due to routings and error multiplication in the signal path the two mm-wave sources initially have an arbitrary phase difference. As the first step toward phase alignment, we detect the phase difference between the two mm-wave sources using the proposed interferometer-based phase detector. In this scheme, the differential output of each multiplier drives two 50Ω buffers. We form the interferometer by connecting a 50Ω transmission line between opposite-polarity buffers from the two multipliers. As a result, an interference pattern described in Fig. 4.2b is generated along the transmission line.

We measure the interference pattern using P peak detectors distributed along the transmission line. As discussed in Section 4.3 and Fig. 4.6, each pair of peak detectors corresponds to a specific zero-crossing, $\Delta\phi$, in the phase detector. Therefore, P peak detectors introduce $(P-1)$ phase settings. We use a P-to-2 analog multiplexer to select the two detectors associated with a specific phase setting. The two outputs from the multiplexer connect to a loop filter. This loop filter integrates the difference between two selected peak detectors while removing high frequency spurs. The loop filter output controls a phase shifter between the two sources. This phase shifter adjusts the phase

difference between the two references applied to the left and right multipliers. This results in a negative feedback loop between the phases of the two mm-wave sources. The loop settles to its equilibrium when $\Delta\phi$ becomes equal to the phase difference defined by (4.12). Although the system has two zero-crossings corresponding to S_a and S_b, only one would result in a stable equilibrium due to their opposite signs. In this design, we choose the feedback polarity to set the loop to our desired zero-crossing, corresponding to S_a.

To extend the frequency beyond the operating frequency of the interferometer operation, we can follow the $\times M$ output with a second frequency multiplier stage with a scaling factor of N. This can generate LO signals at $M \cdot N \cdot f_{ref}$, as shown in Fig. 4.7a while decoupling the LO frequency from the mm-wave phase detector. In this case, the two sources are still phase-aligned, and their phase difference would be $N \cdot \Delta\phi$.

This idea can be extended for 2D scalable self-aligning phased arrays. Fig. 4.7b presents an architecture for such an array by cascading multiple stages in a daisy chain topology. In this scheme a clean low frequency reference signal is distributed to all elements while phase alignment is performed at high frequency and between adjacent mm-wave sources. Since the dimensions of the interferometer scale down with frequency, such an architecture is suitable for large-scale mm-wave and THz phased arrays.
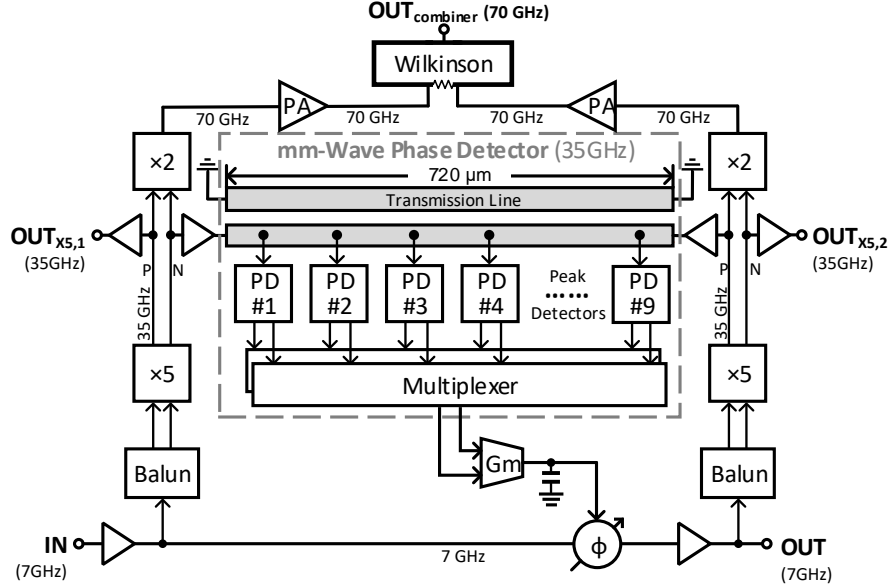
Figure 4.8: Block diagram of the prototyped two-element array.

4.5 Circuit Design and Implementation

We implement a two-element prototype of the proposed phase self-aligning array to verify this concept, as shown in Fig. 4.8. This prototype uses multiplication factors of $M = 5$ and $N = 2$ for the multiplier chain. The reference frequency is 7GHz resulting in 35GHz and 70GHz multiplier outputs.

4.5.1 Interferometer and Peak Detector

We implement the interferometer in Fig. 4.8 using a 50Ω coplanar waveguide (CPW) structure with signal line width and gap of 10μm and 17μm, respectively. The transmission line has a total length of 720μm. With the help of HFSS 3D electromagnetic simulator, we characterize the electrical field pattern with different values of $\Delta\phi$ between
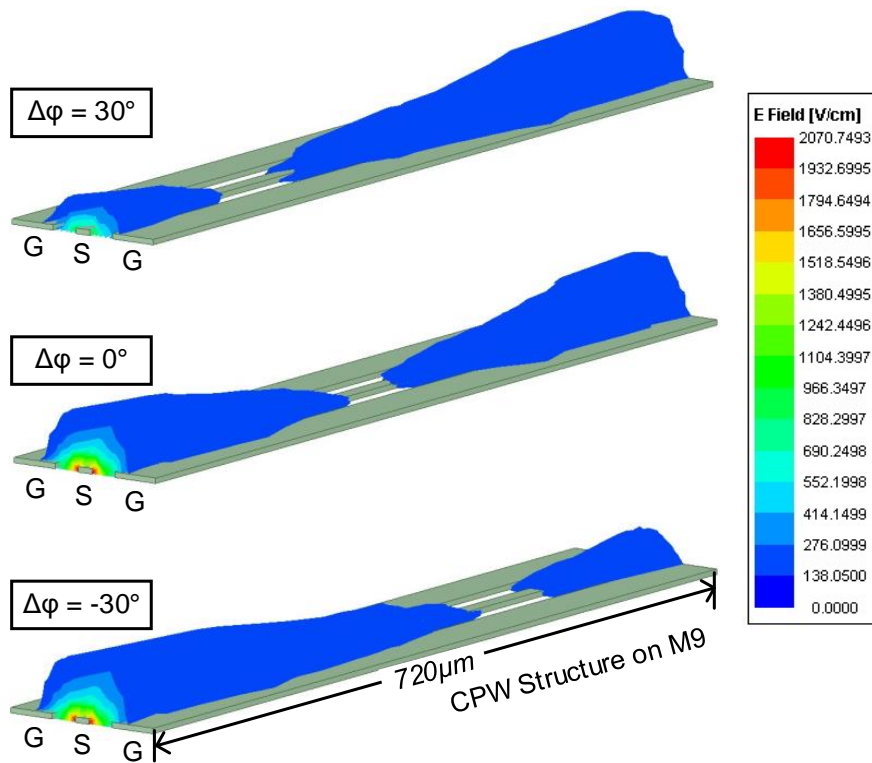
Figure 4.9: EM simulation of the electric field distribution on the CPW line as a function of $\Delta\phi$.
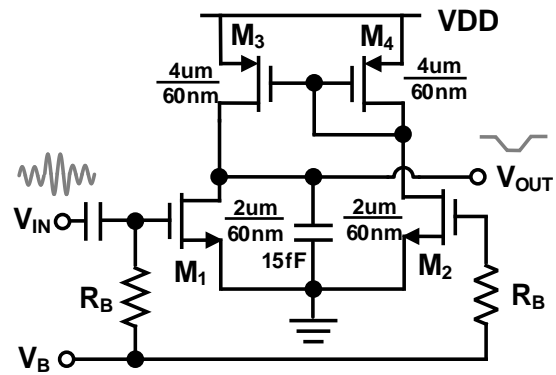
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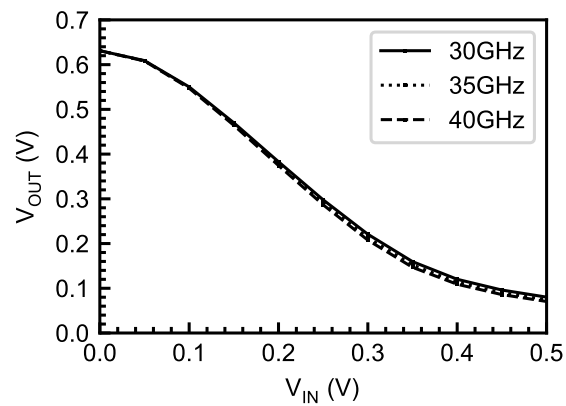
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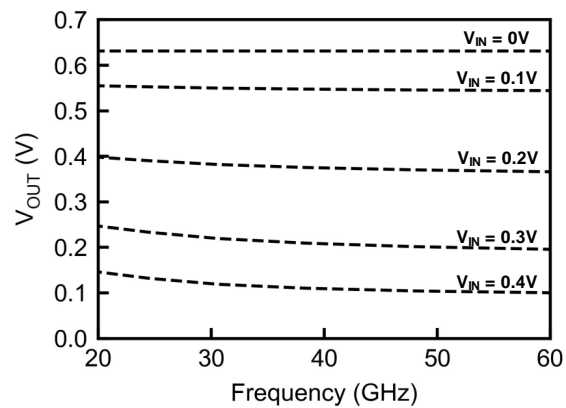
(c)

Figure 4.10: (a) Schematic of the peak detector. (b) Simulated output voltage of the peak detector as a function of the input signal amplitude. (c) Simulated RF-to-DC response vs. frequency.
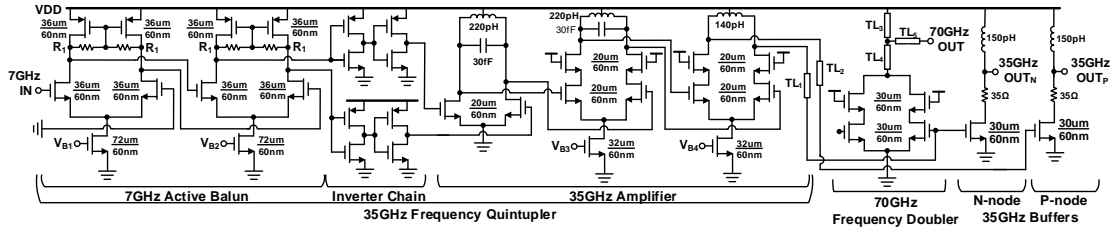
Figure 4.11: Schematic of the frequency multiplier chain consisting of the active balun, the inverter chain, the 35GHz frequency quintupler, the 70GHz frequency doubler, and two 35GHz buffers.

the interfering signals on the two sides. Fig. 4.9 shows the location of the valley as a function of $\Delta\phi$ in agreement with our earlier analysis. Based on (4.8), the line length corresponds to a phase tuning range close to 105 $^\circ$ at 35GHz. As (4.8) indicates, the smallest phase step depends on the proximity of adjacent peak detectors, ΔL. Thus, the number of peak detectors across the line is a design trade-off between the smallest phase step and the capacitive loading of the detectors on the transmission line. In this design, we place $P = 9$ evenly distributed peak detectors across the line resulting in an expected phase step of $15°$ from the $P - 1$ distinct phase settings. This phase step is verified by simulation results, as shown in Fig. 4.6. We choose the desired pair of detectors from a P-to-2 multiplexer based on complementary transmission gates to select the desired phase setting.

The peak detector circuit is shown in Fig. 4.10a. In this design, M1 is biased in

weak inversion to maximize its self-mixing property [53, 54]. This transforms the mm-wave signal amplitude into a proportional DC voltage at the output node. The width of M1 is 2μm which provides sufficient conversion gain while limiting the loading on the transmission line to a 4fF capacitance per detector. M3 is the active load, and C is a metal-oxide-metal (MOM) capacitor that provides low-pass filtering of the output signal. Fig. 4.10 shows the RF-to-DC conversion characteristic of the circuit.

4.5.2 Frequency Multiplier Chain

Based on our selected frequency scaling factors M and N, we achieve a frequency scaling from 7GHz to 70GHz. M should be larger than N, since any residual phase error at the output of the $\times M$ is going to further scale by N at the output of the $\times N$ multiplier. Thus, in this design, we choose $M = 5$ and $N = 2$. Another benefit of choosing a quintupler over a doubler or tripler is achieving a high-frequency conversion factor in a single stage.

Fig. 4.11 shows the schematic of the frequency multiplier chain. The chain consists of an active balun, followed by a chain of inverters and an amplifier at 35GHz. The active balun consists of two stages of differential amplifiers. The input reference feeds one input of the differential pair while the other is AC grounded. The combination of the tail current output impedance and the common-mode feedback resistor, R1, helps to suppress the input common-mode. Given the reference's relatively high frequency, we use two cascaded stages that provide sufficient common-mode rejection to generate a

balanced output signal. The following chain of inverters clips the waveform and enriches the fifth tone. Three frequency-tuned amplifiers further boost this harmonic.

Furthermore, the LC filters in the amplifiers suppress undesired harmonics at the output. The biasing of the amplifier is optimized to maximize the fifth harmonic, and the use of the cascode topology helps increase the drain-gate isolation for achieving unconditional stability. Compared to injection locking methods, the use of amplifiers to boost the harmonic provides a more robust and wide bandwidth solution without any need for frequency tuning and calibration [55]. The three-stage differential amplifier is followed by two single-ended buffers that drive the transmission line with the desired polarity. The output buffers are impedance matched to the transmission line in order to create the desired interference pattern across all phase settings. Furthermore, the buffers are biased as class A amplifies to minimize distortion on the interference pattern due to higher order harmonics. The simulated 3-dB bandwidth of the frequency quintupler is $33.5\mathrm{GHz}-38.5\mathrm{GHz}$.

A frequency doubler follows the quintupler to generate the 70GHz signal. The doubler uses a push-push topology that cancels the fundamental tone and combines the second harmonics at its output [56]. The biasing of the doubler is optimized for second-harmonic power. The doubler output is conjugate matched to the next stage for maximum power gain. The following three-stage common-source power amplifier enables the multiplier output to drive a 50Ω with sufficient amplitude.
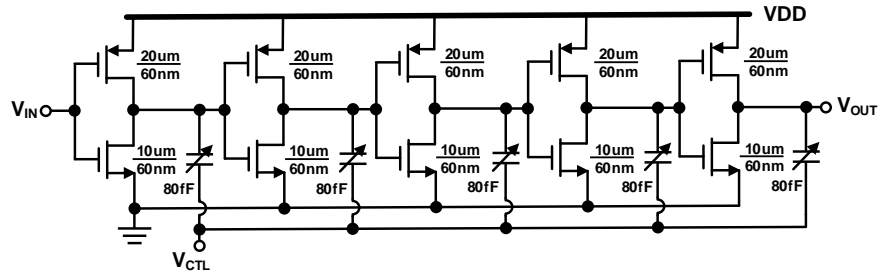
Figure 4.12: Schematic of the phase-shifter.

4.5.3 Phase Control

Following the phase difference detection and as part of the loop operation, the Gm-C cell integrates the difference between the outputs of the two selected peak detectors. As shown in Fig. 4.8, the output of the Gm-C cell controls a phase-shifter which adjusts the delay between the reference signals on the two sides. This provides a negative feedback loop between the two mm-wave sources. As a result, the loop settles to the designated phase difference, $\Delta\phi$ in equilibrium.

The Gm-C cell uses a folded-cascode OTA with a simulated DC gain of 47dB and a dominate pole at 125KHz, which is much smaller than the loop bandwidth. This ensures that the response of this Gm-C cell closely follows that of an ideal integrator. The phase shifter is based on a chain of varactor-loaded inverters, as shown in Fig. 4.12. By adjusting the time constant of each stage, the phase shifter achieves a simulated delay tuning range of 32ps which provides more than 2π phase tuning at our target 35GHz frequency.

To verify the performance of the control loop, we simulate the system for different
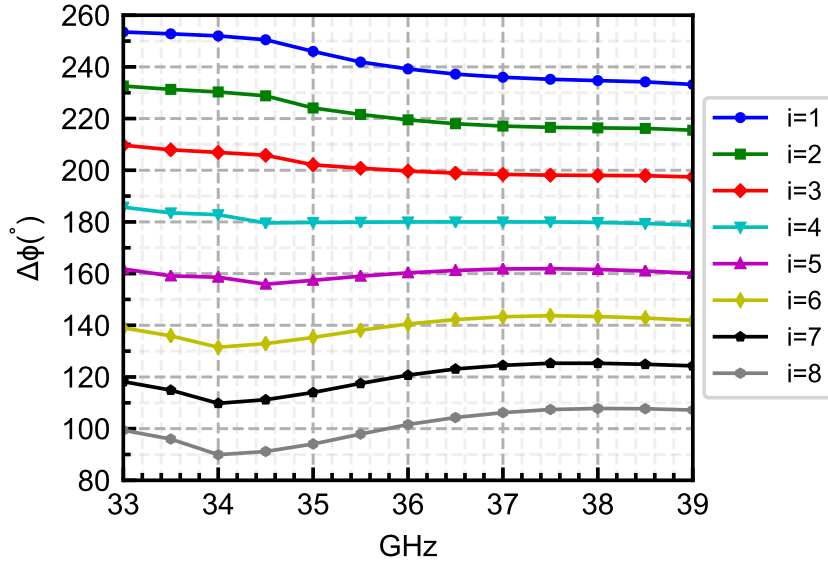
Figure 4.13: Simulated phase differences between the left and right sources across frequency for different phase settings.

target phase settings across the bandwidth. This compares the expected $\Delta\phi$ and the achieved result at the quintupler outputs. Fig. 4.13 shows 8 phase settings associated with the nine detectors on the transmission line. This covers a phase range of $140°$ with $20°$ steps within a 33GHz–39GHz bandwidth. The observed frequency dependence in the phase steps is due to the phase modulation of the driver inputs by the interference pattern and can be suppressed by increasing the reverse isolation of the buffers. We should mention that in the opposite polarity scenario, the in-phase setting of $i = 4$ corresponds to an expected $\Delta\phi = 180°$ between the quintupler outputs and $0°$ phase difference between the doubler outputs. The simulated RMS phase error is $<2°$ across the operating bandwidth.
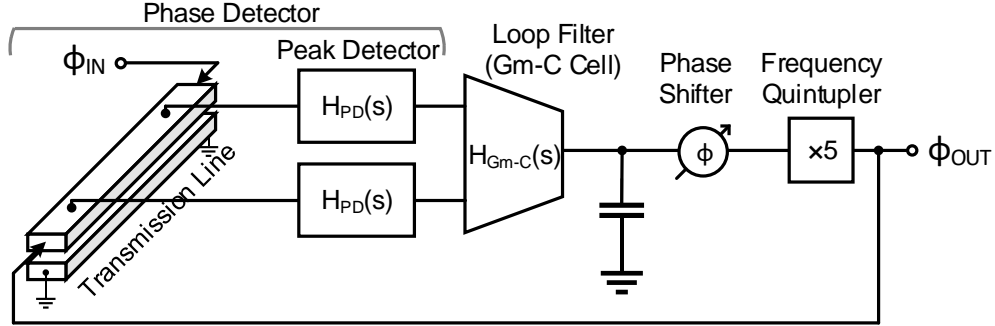
Figure 4.14: Linear model of the phase self-aligning feedback loop.

4.5.4 Stability Analysis

We analyze the stability and loop dynamics of the architecture in Fig. 4.8 by using the linear model shown in Fig. 4.14. The feedback loop starts with a transmission line-based interferometer that is sensed by the selected pair of peak detectors. Next, the output of the peak detectors is applied to the loop filter, which controls the phase shifter and the following frequency quintupler ($M = 5$). In this model, Φ_{in} is the input to the loop defined as the phase of the reference mm-wave source, and Φ_{out} is the output phase.

We derive the open-loop transfer function as:

$$H(s)|_{open} = \frac{K_{open}}{1 + \frac{s}{\omega_3}} \cdot \frac{1}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})}, \qquad (4.13)$$

where,

$$K_{open} = \frac{K}{2} \cos\left(\frac{\phi_o}{2}\right) \cdot K_{Gm-C} \cdot K_{PS} \cdot M \qquad (4.14)$$

is the gain of the open loop. The first term in (4.13) represents the transfer function of

the phase detector. We approximate the gain of the phase detector with S_a, the slope in the proximity of the zero-crossing. Based on parameters from circuit-level simulations, the peak detector contributes an open-loop pole at $\omega_3 = 2\pi \cdot 300\text{MHz}$. The second term is due to two poles introduced by the Gm-C loop filter. We compensate the transfer function by placing a 11pF load capacitance at the output node of the Gm-C filter, resulting in a dominant pole at $\omega_1 = 2\pi \cdot 125\text{KHz}$. The amplifier module also contains a secondary pole at $\omega_2 = 2\pi \cdot 250\text{MHz}$. The phase shifter and the $\times M$ frequency multiplier scale the open loop gain by K_{PS} and M without adding extra poles. As a result, the open loop transfer function provides a phase margin of $67°$, which satisfies the stability criteria. Fig. 4.15 presents the closed-loop step response of the system. The estimated settling time for this single-stage loop is 20ns.

Since the dominant pole in (4.13) is much closer to the origin compared to non-dominate poles, we can approximate the single-stage loop as a single-pole system and write the single-stage closed-loop transfer function as:

$$H(s)|_{closed} \approx \frac{1}{1 + \frac{s}{\omega_1 K_{open}}}. \tag{4.15}$$

As a result, when using this system in an n-stage daisy-chain topology, the transfer function of this n-stage system becomes:

$$H_n(s) \approx \left[\frac{1}{1 + \frac{s}{\omega_1 K_{open}}} \right]^n \approx \frac{1}{1 + n \cdot \frac{s}{\omega_1 K_{open}}}. \tag{4.16}$$

Based on (4.16), we expect that as n increases, the dominant pole would proportionally decrease. As a result, the overall settling time of the system linearly scales with
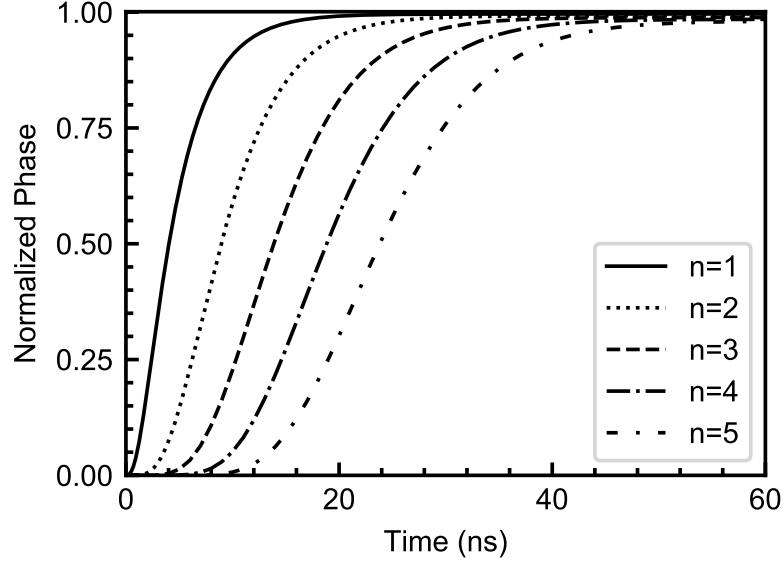
Figure 4.15: Closed-loop step response for different number of stages, n.

n. Fig. 4.15 verifies this expected trend as a function of n.

4.5.5 Noise Analysis

To analyze the output noise of the proposed signal generation and phase alignment scheme, Fig.4.16 identifies the main sources of noise contribution to the linear model. In this scheme, $\phi_{n,out}$ is the noise at the $OUT_{X5,2}$ port. This represents the output noise of the phase control loop. The noise sources from the first and second frequency multipliers, the phase detector, the Gm-C cell, the phase shifter and the input reference are identified as $\phi_{n,X5,1}$, $\phi_{n,X5,2}$, $\phi_{n,PD}$, $\phi_{n,Gm-C}$, $\phi_{n,PS}$ and $\phi_{n,ref}$, respectively.

To calculate the output noise transfer function of each individual noise source, we carry out the linear analysis of Section 4.5.4, as shown in Fig.4.17. Based on the derived
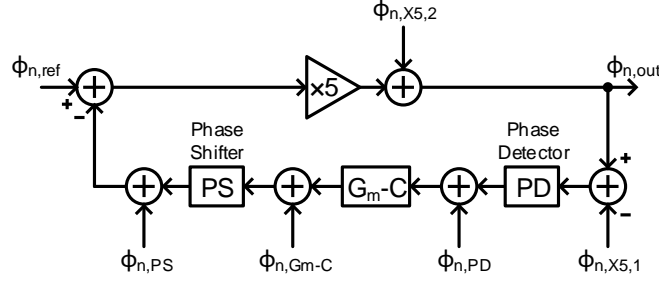
Figure 4.16: Noise analysis model and the individual noise sources.

transfer functions, the feedback loop results in a low-pass response from the first element, $\phi_{n,X5,1}$. On the other hand, the noise from the second frequency multiplier, $\phi_{n,X5,2}$, experiences a high-pass filtering by the loop. The loop has a similar high-pass effect on the noises from the Gm-C cell and the phase shifter, while having a low-pass effect on the noise from the phase detector. According to Fig.4.18, compared to other noise sources, the overall phase noise contribution is dominated by the first and second frequency multipliers.

As a result, the overall output phase noise spectrum can be divided into two subsections known as in-band and out-of-band phase noises as shown in Fig.4.19. Based on our analysis, the in-band section follows the phase noise response of the previous element, and the out-of-band phase noise follows the phase noise of the current frequency multiplier. In other words, in the two element prototype of the scalable array the in-band phase noise of the second element is similar to the phase noise of the first element with minimal degradation of in-band spectrum purity.
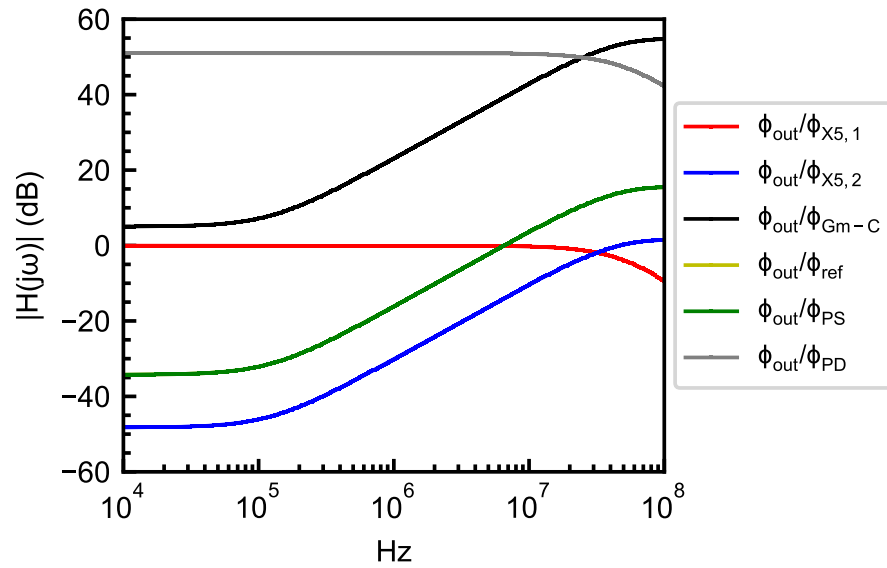
Figure 4.17: Magnitude of the output noise transfer function at $OUT_{X5,2}$, with respect to each sub cell.
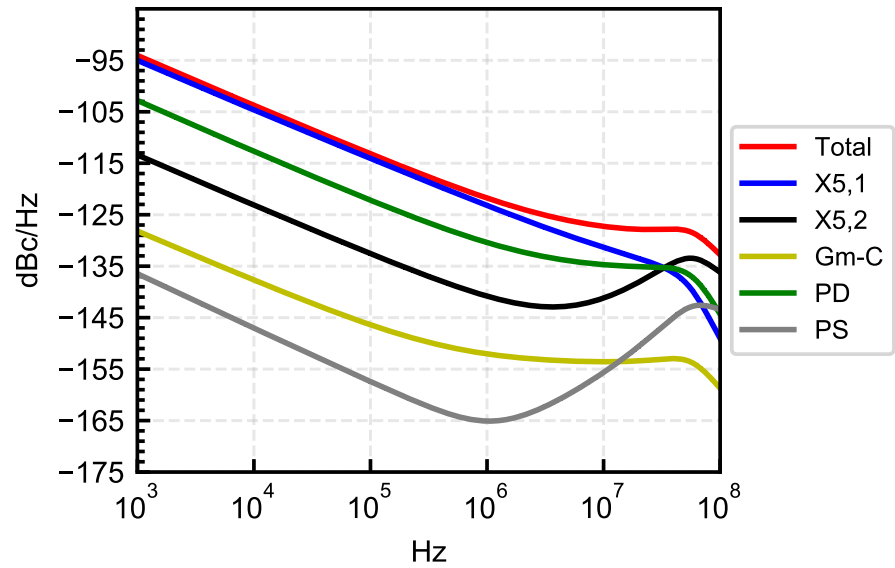
Figure 4.18: Simulated closed-loop phase noise at $OUT_{X5,2}$ with individual sub cell noise contribution.
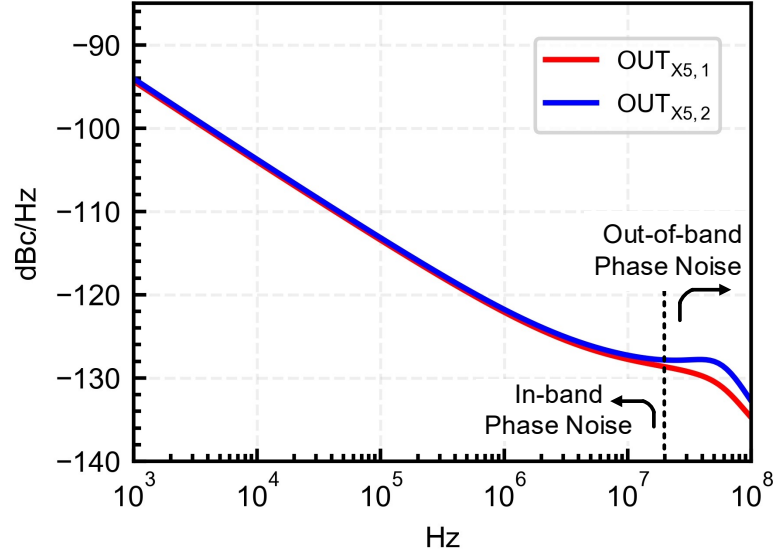
Figure 4.19: Simulated closed-loop phase noise at $OUT_{X5,1}$ and $OUT_{X5,2}$.

4.5.6 Phase Inaccuracy in The Presence of Mismatch

In this design, the differential output of a selected pair of the peak detectors is responsible for detecting the interference pattern. Due to its differential nature, this detection is relatively robust to PVT variations. However, any random mismatch between the characteristics of the peak detectors directly impacts the phase detection accuracy. The primary two sources of this mismatch are the input device and the load capacitor. These two sources of mismatch collectively introduce a random voltage error, E_v, in the output voltage of each peak detector. As Fig. 4.20 shows, once the loop settles, such a shift in the voltage translates into a proportional phase error, E_ϕ, in the $\Delta\phi$. We model E_v and E_ϕ as normal distributions with RMS values of σ_v and σ_ϕ, respectively. At steady-state
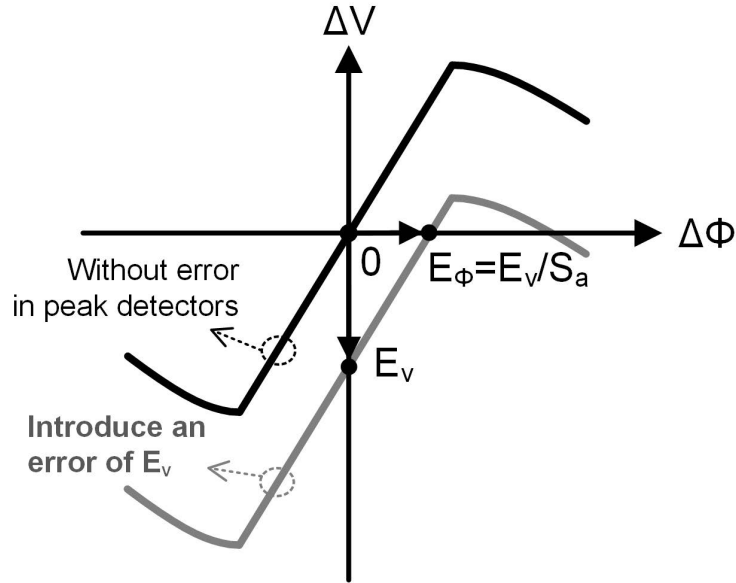
Figure 4.20: Translation of mismatch from E_v to E_ϕ.

and based on (4.11), we can estimate the relationship between σ_v and σ_ϕ as:

$$\sigma_\phi = \frac{\sigma_{v_d}}{S_a},\tag{4.17}$$

where $\sigma_{v_d} = \sqrt{2}\sigma_v$ is the RMS output difference between the two peak detectors.

Fig. 4.21a shows the Monte Carlo response of the peak detector showing a σ_v of 36mV. Based on Fig. 4.6, we calculate the slope, $S_a = 5$mV/deg. Thus, from (4.17), we expect a σ_ϕ of $10.2°$. This calculated phase error is consistent with the σ_ϕ from system-level Monte Carlo simulation of the loop shown in Fig. 4.21b. Since each pair of peak detectors follows similar Monte Carlo statistics, this estimated σ_ϕ also represents the overall RMS phase error of the phase detector across all settings. This phase error is due to a frequency-independent static offset which a one-time DC calibration can
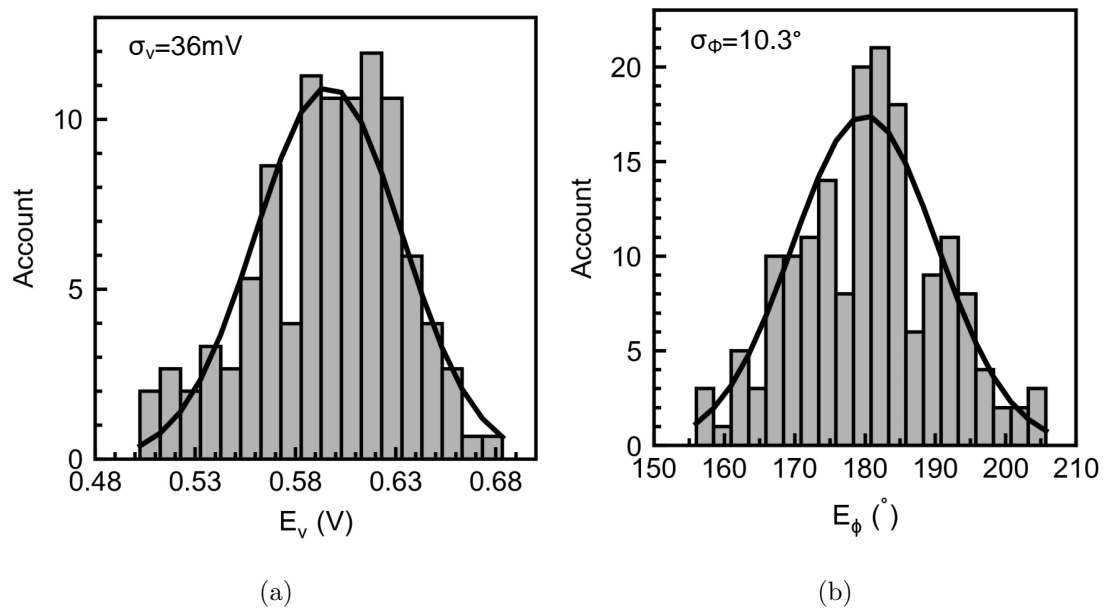
Figure 4.21: (a) Monte Carlo simulation of the peak detector output when the input amplitude is chosen to represent the valley of the interference pattern. (b) System-level Monte Carlo simulation of the settled phase difference between the two sources.
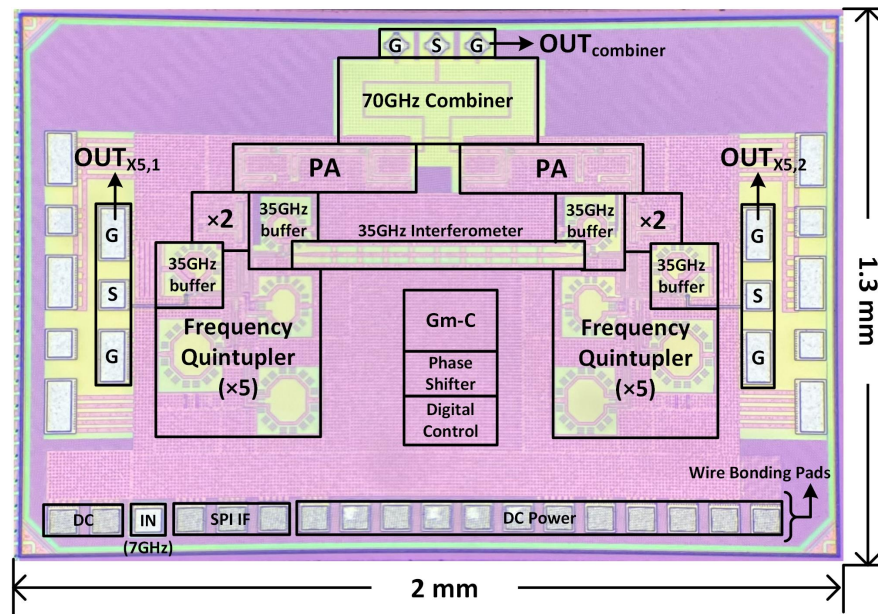
Figure 4.22: Chip microphoto.

correct.

4.6 Prototype Measurement

To validate the proposed phase self-alignment scheme, we fabricate a two-element proto-type of this array using the TSMC 65nm bulk CMOS process. The chip consists of two multiplier chains acting as two independent mm-wave sources and the proposed phase alignment control loop. Fig. 4.22 shows the chip microphoto with a size of 1.3mm × 2mm. The input reference is wire bonded to the chip and the digital interface and DC supplies. The outputs of the two quintuplers can be directly probed at 35GHz, while the doubler outputs are compared by probing a 70GHz power combiner. Fig. 4.23 shows the
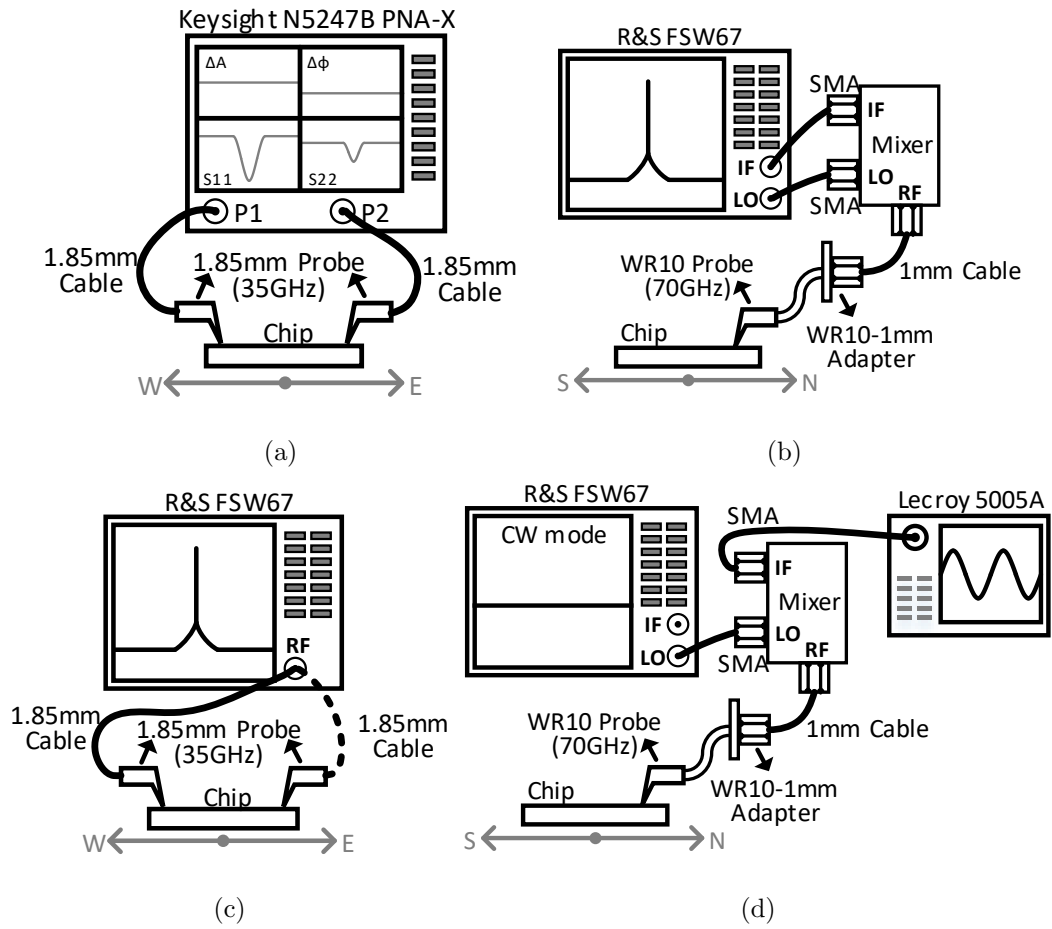
Figure 4.23: Measurement setups for (a) phase and amplitude of the 35GHz outputs, (b) the combiner output at 70GHz, (c) phase noise performance at 35GHz, and (d) transient response at the combiner output.
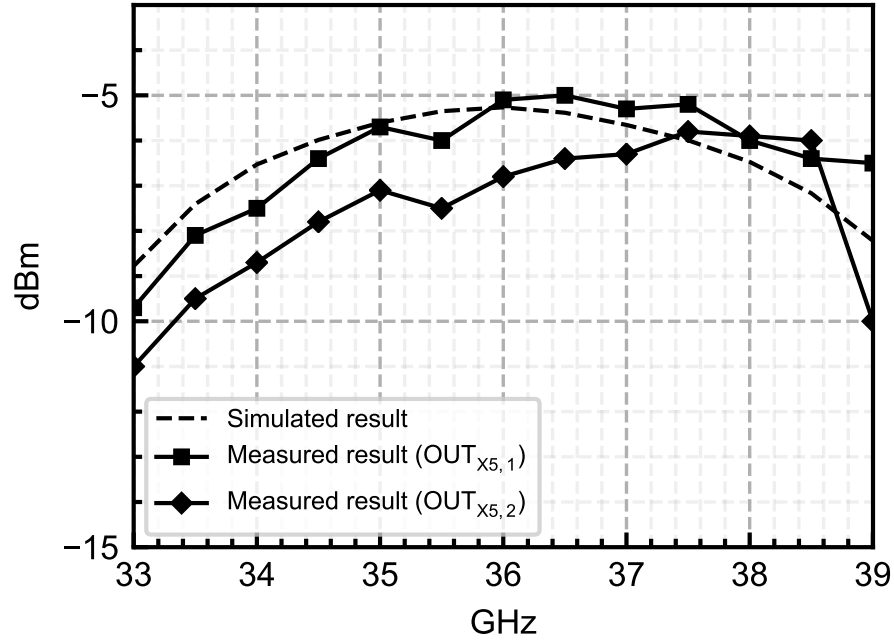
Figure 4.24: Simulated and measured quintupler output power.

measurement setups used to validate the chip's performance at both 35GHz and 70GHz

outputs. The first setup uses the Keysight N5247B PNA-X 67GHz network analyzer

to directly measure and compare the two 35GHz outputs. We first set the multiplexer

output to a particular pair of detectors to verify each phase setting. This programs the

system to achieve a target equilibrium phase, $\Delta\phi$. Next, we measure the phase and

amplitude of the two mm-wave outputs and compare with the expected outcome from

simulation.

Fig. 4.24 shows the the measured output amplitudes at 35GHz. The measured

bandwidth is 33.5–38.5GHz which is consistent with simulation. The amplitude mis-

match between the two 35GHz outputs is $<$ 2dB across frequency and phase settings,
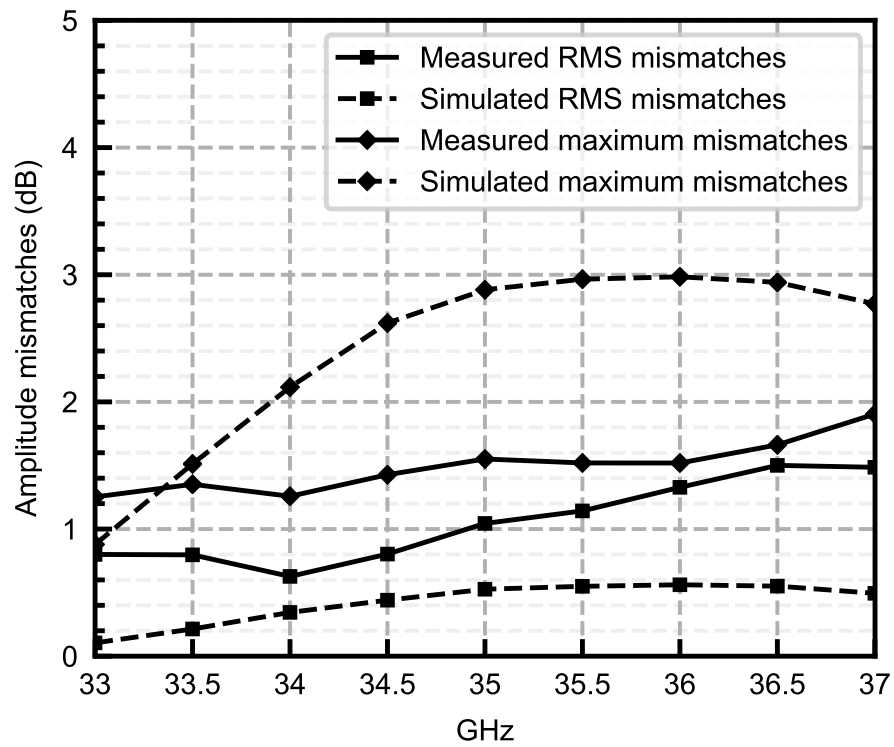
Figure 4.25: Simulated vs. measured amplitude mismatch between two frequency quintuplers across frequency and phase settings.

as shown in Fig. 4.25.

Fig. 4.26a shows the measured phase difference, $\Delta\phi$, between the two sides. This phase is measured after a two-step calibration of the measurement fixture: First, we use a calibration substrate for the initial compensation of the test setup. Next, we move the probes to the target chip and collect the raw data of the phase. Due to the sensitivity of the measured phase difference to any mechanical change in probing we estimate and compensate for any extra delay introduced by this probe relocation[2] . After this initial calibration, the measured tuning range of $\Delta\phi$ is consistent with simulation results.

Due to the mismatch effects discussed in Section 4.5.6 we observe a frequency-independent error in the measured $\Delta\phi$ compared to the perfectly matched case in Fig. 4.13. Since this is a static error, we can compensate for it by a one-time calibration at a single frequency. Fig. 4.26b shows the phase steps across frequency after mismatch calibration performed based on the measured data at 35GHz. Before this calibration, the measured RMS phase error is $< 10°$ across the bandwidth, consistent with Monte Carlo simulation results in Fig. 4.21. After calibrating for the detector mismatch, this error reduces to $< 3.5°$ across the operating bandwidth. Fig. 4.27 compares these RMS phase errors between simulation and measurement before and after this calibration. These results indicate that the detector mismatch is the primary source of phase error that a single-point calibration can correct. As (4.17) suggests, the RMS phase error is inversely proportional to the amplitudes of the two mm-wave sources driving the transmission

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[2] This initial calibration removes a length of 0.17λ at 35GHz which is equivalent to subtracting a fixed propagation delay of 5ps from the signal path.
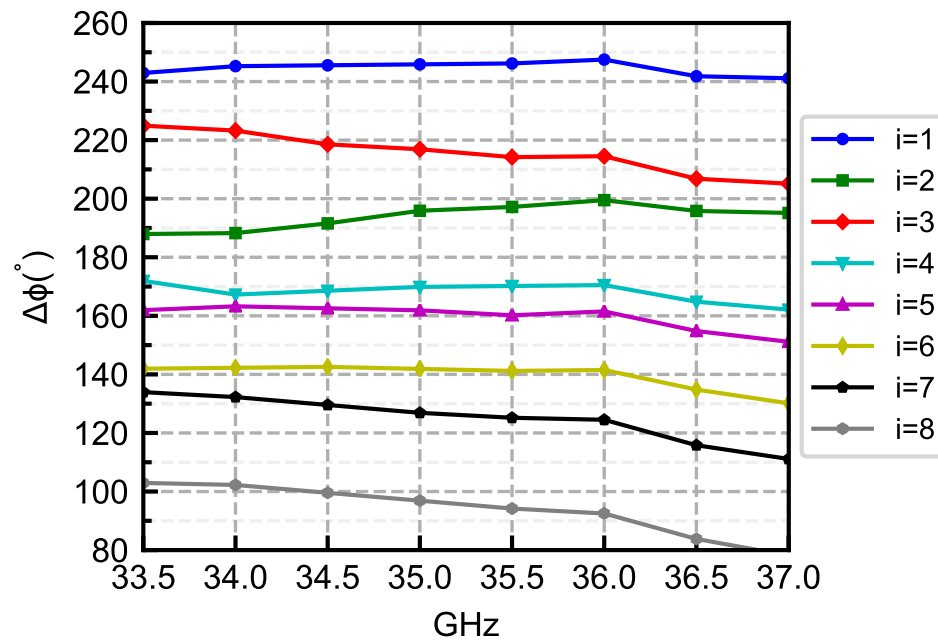
(a)
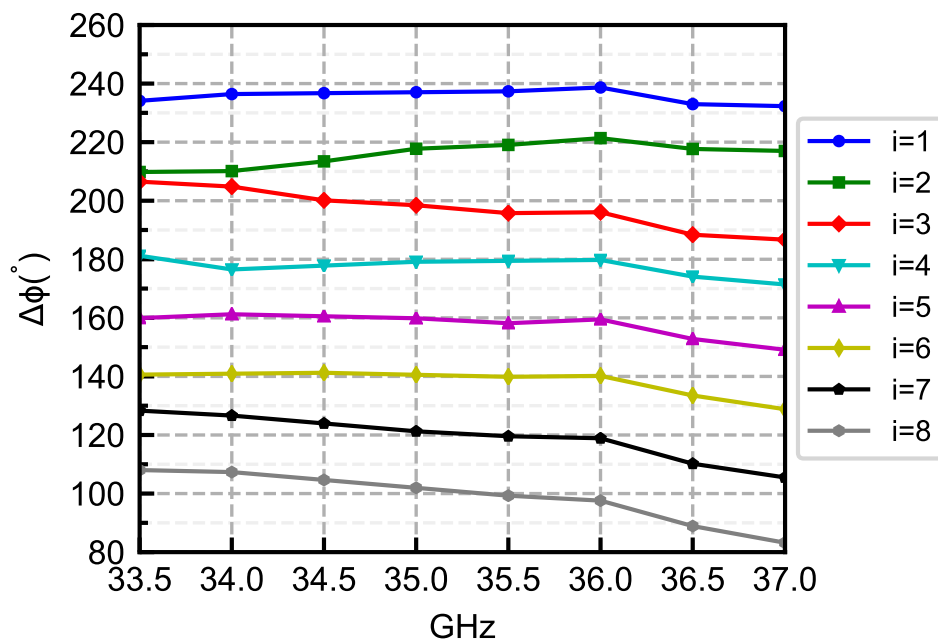
(b)

Figure 4.26: (a) Measured phase difference between frequency quintuplers before the mismatch calibration. (b) Phase difference after the mismatch calibration.
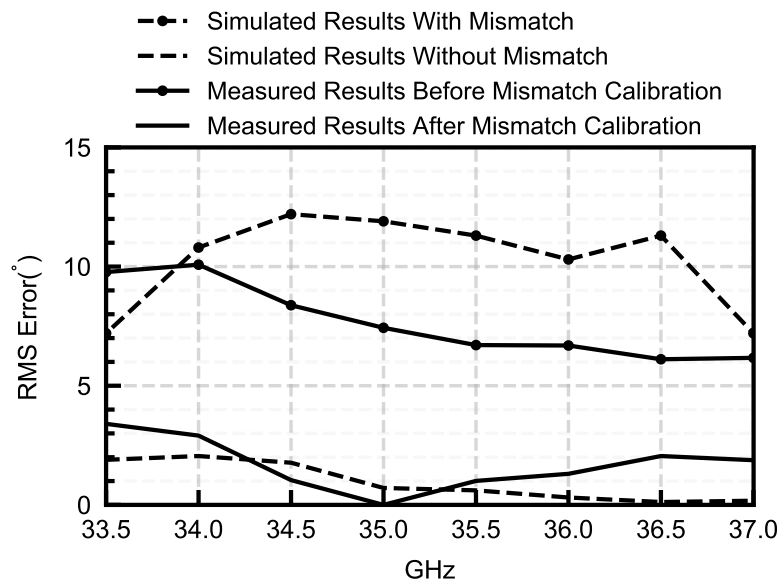
Figure 4.27: Comparison between measured RMS phase error and results from Monte Carlo simulations.

line. As a result, from Fig. 4.24, we expect that the phase error is proportionally lower at a frequency with a higher driver amplitude. We can confirm this behaviour by observing the frequency dependency of the measured RMS phase errors in Fig. 4.27.

For the subsequent measurement, the outputs of the two frequency doublers drive a quarter-wavelength Wilkinson power combiner shown in Fig. 4.8, and we measure the combined output power at 70GHz. Fig. 4.28 presents the 3D EM model of the power combiner. The test setup for this measurement is shown in Fig. 4.23b. This setup enables us to measure the phase difference between the two 70GHz sources indirectly. This measurement has two benefits: first, this is an independent method to measure the phase difference between the two sources and does not require the complicated
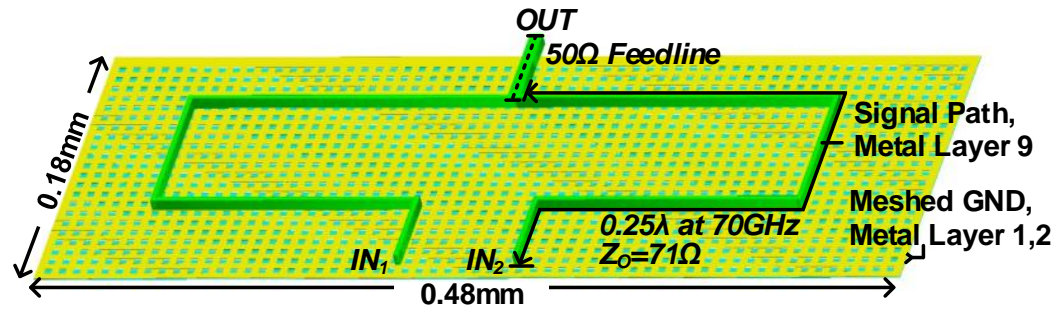
Figure 4.28: The 70GHz Wilkinson power combiner. A 100Ω resistor between port IN_1 and IN_2 is not shown in the figure.
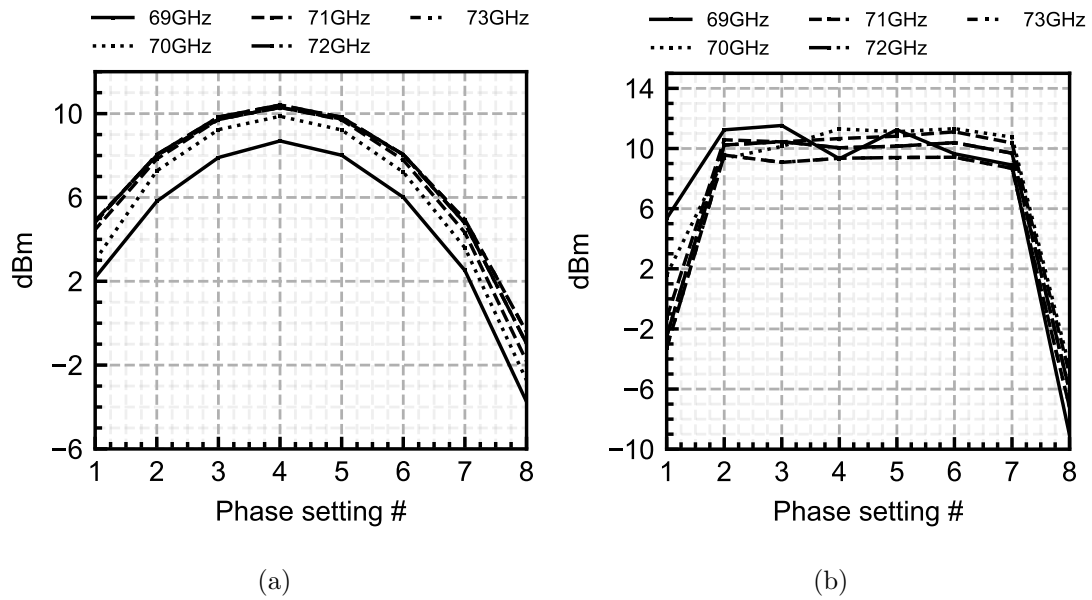
Figure 4.29: (a) Simulated and (b) measured power at the output of the Wilkinson combiner.
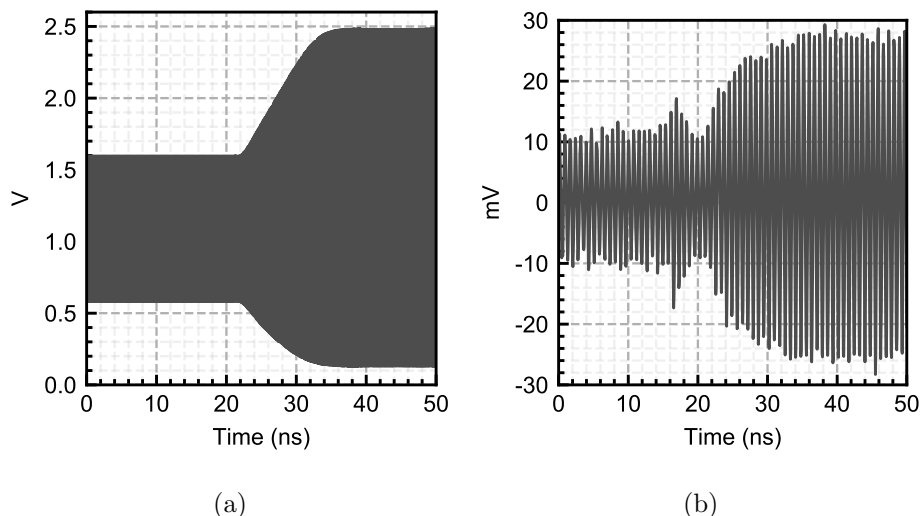
Figure 4.30: (a) Simulated and (b) measured transient switching response at the combiner output.

calibration needed for off-chip comparison between the two sides. Second, it enables us to measure the system at frequencies above the bandwidth of the 67GHz PNA-X, replicating the over-the-air combining of the two transmitters. Fig. 4.29 compares the combiner output simulation and measurement results. The output amplitude peaks at the center phase setting, followed by two minima at the two boundary phase settings. Given the phase difference at the doubler output, which is $2\Delta\phi$, and based on the measured $\Delta\phi$ at 35GHz, the expected output phase difference at 70GHz ranges from $+120°$ on the left to $-160°$ on the right side of the plot. Compared to simulation, the measured amplitude near the in-phase setting fluctuates due to its sensitivity to phase error. However, the locations of the measured nulls are consistent with their expected locations from simulation.
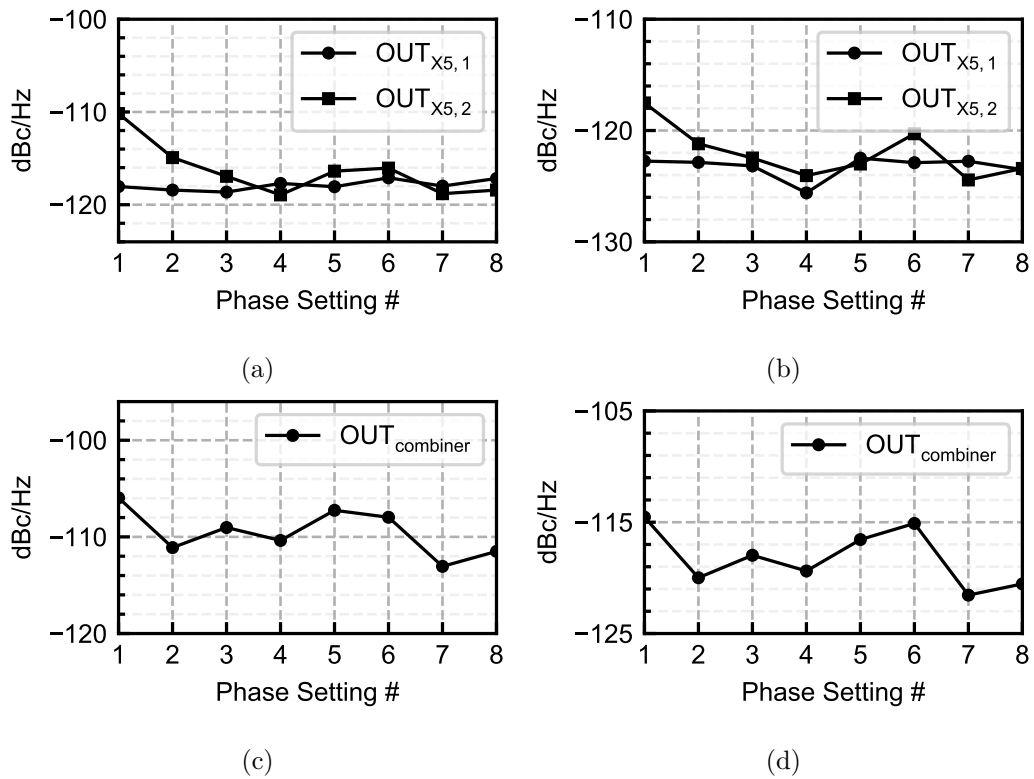
Figure 4.31: Measured phase noise of the two 35GHz quintupler buffered outputs at (a) 1MHz offset and (b) 10MHz offset. Measured phase noise of the 70GHz Wilkinson combiner output at (c) 1MHz offset and (d) 10MHz offset.

Figure 4.32: Measured phase noise spectrum of the input reference signal.
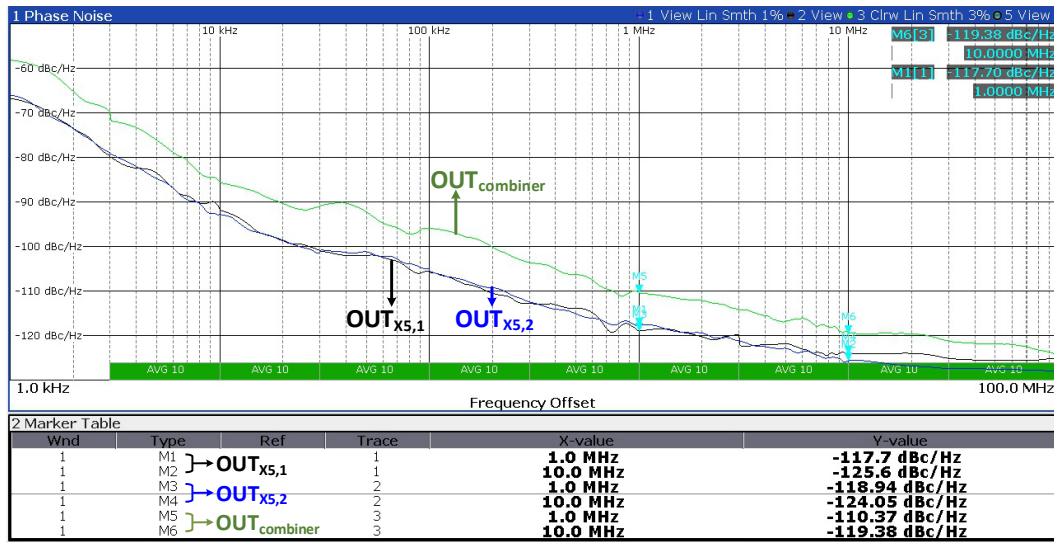
Figure 4.33: Measured phase noise spectrum of the two 35GHz outputs and the 70GHz

output for the $i = 4$ phase setting.

We capture the transient response of the loop using a 20GS/s Lecroy DDA-5005A scope as shown in Fig. 4.23d. We use a harmonic mixer to down-convert the 70GHz output to an IF signal below 8GHz that the scope can sample for this measurement. Fig. 4.30b shows the transition time when the phase setting switches from $i = 1$ to $i = 4$. The measured settling time is < 20ns, consistent with the expected response time from Section 4.5.4 and simulation results in Fig. 4.30a.

To measure the phase noise, we use the Rohde&Schwarz FSW67 Spectrum Analyzer, as shown in Fig. 4.23b and Fig. 4.23c. These setups measure the phase noise of the two 35GHz sources and their 70GHz combined output. Fig. 4.31 presents these phase noise measurements across all the different phase settings. The phase noise spectrums of the 7GHz input reference signal and the $35, 70$GHz output signals at $i = 4$ are shown in Fig.4.32 and Fig.4.33, respectively. At the 1MHz frequency offset, the measured phase noises of the first and second 35GHz outputs are -117.7dBc/Hz and -118.9dBc/Hz at the in-phase setting and across all settings, they remain below -117.1dBc/Hz and -110.2dBc/Hz, respectively. The measured phase noise of the 70GHz Wilkinson combiner is -110.4dBc/Hz in the nominal setting and remains below -106.0dBc/Hz across all phases. At the 10MHz frequency offset, the measured phase noises of the first and second 35GHz outputs are -125.6dBc/Hz and -124.1dBc/Hz at the in-phase setting and remain below -122.5dBc/Hz and -117.5dBc/Hz across all phase settings. The measured phase noise of the 70GHz Wilkinson combiner is -119.4dBc/Hz in the nominal setting and stays below -114.5dBc/Hz across all phases.

Figure 4.34: Phase noise of the proposed signal source compared to state-of-art mm-band signal generators.

Due to the benefits of this proposed phase-locking and tuning method, the measured phase noise is superior to conventional mm-wave PLLs and coupled arrays [8, 57, 58, 59, 60, 61, 62, 63, 64, 65], and is in fact comparable to stand-alone mm-wave multipliers [66, 67, 68, 69, 70, 71], as shown in Fig.4.34 and Fig.4.35.

The chip consumes a total DC power of 258mW, including the power consumed by the two mm-wave sources and the phase control loop. Each multiplier core consumes 128mW, and the power consumption of the phase control loop is 2mW. Table 4.1 summarizes the chip performance and compares with the state-of-art mm-wave multi-core frequency sources. The measured phase step is 20° which can be further increased by introducing more detectors. Before and after calibrating for the detectors mismatch,

Figure 4.35: FoM of the proposed signal source compared to state-of-art mm-band signal generators.

RMS phase error is $10°$ and $3.5°$, respectively. The reported phase noise is below -117dBc/Hz at 1MHz offset, superior to conventional phase-locking methods. To the best of our knowledge, this is the first array that enables direct phase monitoring and background control of the mm-wave signal source.

4.7 Summary

In this chapter, we present a novel background phase-locking and self-alignment technique for mm-wave phased arrays. The proposed phase locking method relies on direct monitoring of the phase at mm-wave while providing the control mechanism through a baseband loop. This method provides phase tuning without the need for extensive baseband calibration or degradation in the phase noise of the mm-wave source. We

demonstrate the concept with a chip prototype showing accurate phase control and a fast switching time with high spectral purity. The presented element-to-element self-alignment method is applicable for distributed tuning and controlling scalable phased arrays.

Table 4.1: Comparison with the state-of-art prior work.

Reference	This work	ISSCC16[19]	TMTT21[8]
Architecture	Frequency Multiplier Array	Coupled PLL Array	Coupled PLL Array
Array Size	1×2	1×3	1×2
Frequency Range (GHz)	$33.5 - 37$ [$\times 5$] $67 - 73$ [$\times 10$]	$25.3 - 30.3$	$112 - 121$
Fractional BW	9.9%	18%	7.7%
Phase Self-Alignment	Yes	No	No
Phase Tuning Range	$140°$ [$\times 5$]	N/A	$46.7°$
Phase Step / RMS Error	$20°$ / $3.5°$ [$\times 5$]	N/A	Analog / N/A
Phase Noise (dBc/Hz@1MHz)	-117.7 [$\times 5$] -110.4 [$\times 10$]	-95.3	-93.4
Phase Noise (dBc/Hz@10MHz)	-125.6 [$\times 5$] -119.4 [$\times 10$]	-117	-115.8
IPN / JitterRMS Integral Range	-37.6dBc / 85fs [$\times 5$] 1KHz–100MHz	N/A / 104fs N/A	N/A
On-chip VCO	No	Yes	Yes
Reference Frequency	$6.6 - 7.4$GHz	3.5GHz	88MHz
Switching Time	20ns	N/A	N/A
Power Per Element	130mW*	87mW	79mW
Total Power	258mW	261mW	147mW
Per Element /Total Area	0.21mm^2 / 2.1mm^2	2.4mm^2 / 2.4mm^2	0.27mm^2 / N/A
FoM$_P$[†]	-187dB [$\times 5$]	N/A	-176dB
FoM$_T$[§]	-187dB [$\times 5$]	N/A	-174dB
FoM$_J$[††]	-240dB [$\times 5$]	-233dB	N/A
Technology	65nm CMOS	65nm CMOS	65nm CMOS

* $P_{Element}$ = 128mW(X10)+2mW(loop).

[†] FoM$_P$=PN-$20log10$(f/f0)+$10log10$(Pdc[mW]). [§] FoM$_T$=FoM$_P - 20log10$(TR[%]/10).

[††] FoM$_J$=$20log10$(Jitter[s])+$10log10$(Pdc[mW]).

Chapter 5

Conclusion and Future Direction

In this thesis, we present several scalable schemes towards building large-scale active arrays with multiple LOs. In chapter two, a scalable COA scheme based on unidirectional coupling is proposed. We derive the stable modes for the COA and demonstrate that the scaling of the array will preserve four the steady state modes which are predictable and subject to control. Using the perturbation method, we find that as long as the mismatches are below a theoretical threshold, the scaled array would tolerate the presented element-to-element variations and could achieve frequency synchronization regardless of the array size. This is an advantage because the conventional bilateral coupled oscillator arrays cannot achieve frequency lock under the same condition.

In chapter three, to overcome mismatch limitations we propose a two-dimensional coupled PLL array scheme using type-II PLLs as the unit element of LO source. Beside the concept of phase locking between multiple oscillators, we implement a chip prototype

of the PLL array at 28GHz. The measurements indicate that the out-of-band phase noise of the distributed array does not depend on the number of elements. However, we also learn that there are several limitations as well, including in-band phase noise degradation and stability issue found in the prototyped array. We conduct an investigation post-tape-out and find there is an underlying phase control conflict between the PLL loop operation and magnetic injection coupling. We model both behavior in circuit simulation and verify that it is the reason for system instability and phase noise degradation.

Based on the lessons learned in chapter three, we adjust the method of mm-wave signal generation and distribution, and propose a new phase self-aligning array architecture in chapter four that overcomes element-to-element mismatch and provides phase alignment. A prototype is made to demonstrate the phase self-aligning between a 1×2 array. The measured results verify our theoretical analysis, and show accurate phase control and a fast switching time with high spectral purity. We believe the presented element-to-element self-alignment method is applicable for distributed tuning and control of scalable phased arrays without the need of extensive baseband calibration.

In order to further investigate the proposed schemes, as part of the future works, the author believe that it is beneficial to build next-generation prototype arrays integrated with more elements and at large scale. The author thinks that there are at least two directions as the next steps following up on the phase self-aligning array work in chapter four. The first direction is to increase the operational frequencies to the sub-mm-wave region. As discussed in chapter four, the area of the 1×2 array is dominated

by the interferometer, and the dimension of the interferometer is proportional to the quarter wavelength of the target frequency. Therefore, at sub-mm-wave frequency, more elements could fit within the same chip area. For example, a 4×4 array operating at $300GHz$ could fit into $1mm^2$ chip area approximately. In this direction, the focus of the work is the design of the sub-mm-wave frequency multiplier or PLL, whereas the inter-element interface could be the same. Second, expand the size of the phased array at the similar mm-wave frequencies. The mm-wave frequency multiplier block could be reused in the next-generation prototype. However, due to the area limitation per chip, multiple chips are necessary to scale up the size of the array. As a result, the mm-wave phase detection in the array contains both on-chip and between-chip interfaces. In order to maintain the correct phase aligning result, the key points are the design of reliable mm-wave packaging solution and accurate modeling of the on-chip and off-chip electromagnetic performance. Although both directions contain challenges that require design innovations, the author believes in the potential of the next-gen phased array at large scale, and is genuinely looking forward to the future updates and results.

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