ULTRA FAST FREQUENCY HOPPING TRANSCEIVER DESIGN AND IMPLEMENTATION FOR SECURE WIRELESS COMMUNICATION

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Abstract

Frequency hopping spread spectrum (FHSS) is used in a completely new way to provide processing gain for the first time.To improve the in-band blocker handling capability of the receiver the processing gain is realized in RF domain. The RF transceiver system is designed to provide 20dB of processing gain before any amplification occurs in receiver chain. This enables the receiver to reduce any in-band blocker by 20dB before the LNA and provide self-interference cancelation for the local transmitter that is located on the same chip. This enhances the dynamic range of the receiver above what has been possible before. Since this is the first attempt to build such a system, no system level analysis existed prior to this work. So on top of IC design, system level design and modeling of the system is presented as well.

Two major circuits were developed before this system was feasible. First, an ultra-fast front-end band-pass filter was designed to perform the correlation function. This circuit needs to switch frequency in extremely short periods of time, i.e. 20ns. Secondly, since the correlator circuit hopping speed depends on a fast-hopping LO signal, a signal generator sub-system was developed to generate the LO off a constant frequency RF signal. This sub-system consists of a digital oscilator, DAC, and an injection locked oscillator (ILO) that is used as a high-Q band-pass filter that can in theory switch frequency instantaneously. The digital nature of the LO generation circuits and the ILO's ability to move fast in frequency domain enables the sub-system to generate ultra-fast hopping LO signals.

The system is designed to accommodate 470Kbps in various wireless channel environments while providing 20dB of processing gain. This translates into 50 Mhop/s frequency hopping speed that is more than 300 times faster than the state of the art. The RF metrics of developed components and system level performance are proven in silicon and measurements are reported. The results are presented here and in top conferences and journal papers.

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Chapter 1

Introduction

Direct sequence spread spectrum (DSSS) techniques form the core of code division multiple access and is primarily used for multiple accesses in civilian applications. DSSS techniques are able to spread in-band jammers by the processing gain and have been exploited by military communication systems for in-band jammer immunity. Traditionally, direct sequence processing is done at baseband frequencies, such that the RF front end can still be overloaded by in-band jammers. More recently, direct sequence processing has been attempted at RF frequencies to improve in-band jammer resilience [14], [15].

Frequency-hopped spread spectrum (FHSS) techniques have traditionally been used for secure and resilient communications. Conventionally, FHSS systems avoid blocking signals by completely avoiding their frequency of operation. However, this requires blocker identification to continue communications. In addition, any in-band blocker would eventually end up jamming the active front-end circuits. Currently, the fastest FHSS systems operate at a maximum of one symbol per hop [16]. FHSS schemes, in theory, have the capability of suppressing in-band jammers if a single symbol is spread over multiple hops. Unfortunately, this has traditionally not been possible due to the limited transient response of phase locked loop (PLLs). In particular, the transient response of PLLs, while hopping from one frequency to another, is limited by the filter loop bandwidth. Given a loop bandwidth that is 1/10th of the input reference frequency and approximating the settling time as four time constants, the maximum hop rate for a 30 MHz input reference frequency PLL is limited to 75 kHop/s [17].

Conventional FHSS systems are classified as either slow hopping or fast hopping depending on the number of symbols transmitted per hop. Slow-hopping FHSS systems transmit multiple symbols per hop, while the traditional fast-hopping FHSS systems transmit the same symbol during one or more (but usually limited to two or three) hops. This handful of hops is usually done to provide frequency diversity and is not intended for blocker rejection. Hopping speeds for slow-hopping systems are usually limited to a few kHop/s, while that for fast-hopping systems is limited to about 200 kHop/s [16]. The ultra-fast FH design presented here (architecture shown in Fig. 1.1) is able to hop at 47 MHop/s and provides 20 dB of processing gain at RF that improves the in-band blocker suppression by the same amount. For 20 dB of processing gain, the system uses 100 hops per symbol.

The ultra-fast hopping transceiver front end discussed in this paper provides the 20 dB of processing gain at RF. Thus, the blocker is rejected before any amplification occurs in the receiver chain. Two issues have been addressed to make this system possible. First, a circuit architecture is introduced that enables the correlation to be performed at RF. This circuit is able to perform the correlations in extremely short periods of time that has not been possible prior to this work. Second, low-power local oscillator (LO) circuits are designed that can hop extremely fast. Simultaneously solving both these issues has been critical to making ultra-fast hopping with processing gain at RF possible.

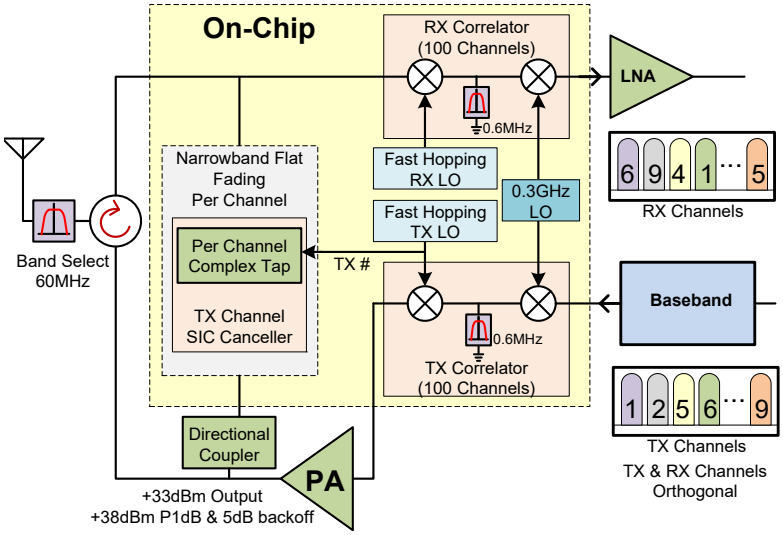


Figure 1.1: Ultra-fast frequency hopping transceiver front-end architecture

Series N -path band-stop filters have, sometimes, been used to suppress in-band blockers [18]. However, they suffer from poor linearity, limited jammer rejection and require a priori knowledge of the exact location of the blocker in the frequency domain thus, requiring power hungry spectrum sensing techniques. In addition, these circuits become power hungry and complex with multiple LOs, one for each jammer, when attempting to suppress multiple blockers at the same time. Furthermore, as these filters operate in-band, they need to be very narrow so as to not reduce the usable signal. Narrow-band N -path notch filters require extremely large on-chip area to minimize the bandwidth. In our design, however, utilizing low-power ultra-fast circuit architectures, multiple blockers can be suppressed without any a priori knowledge of their frequency content. Like other designs, any out of band blockers can be removed using well-known on/off chip techniques [19].

Chapter 2

Background

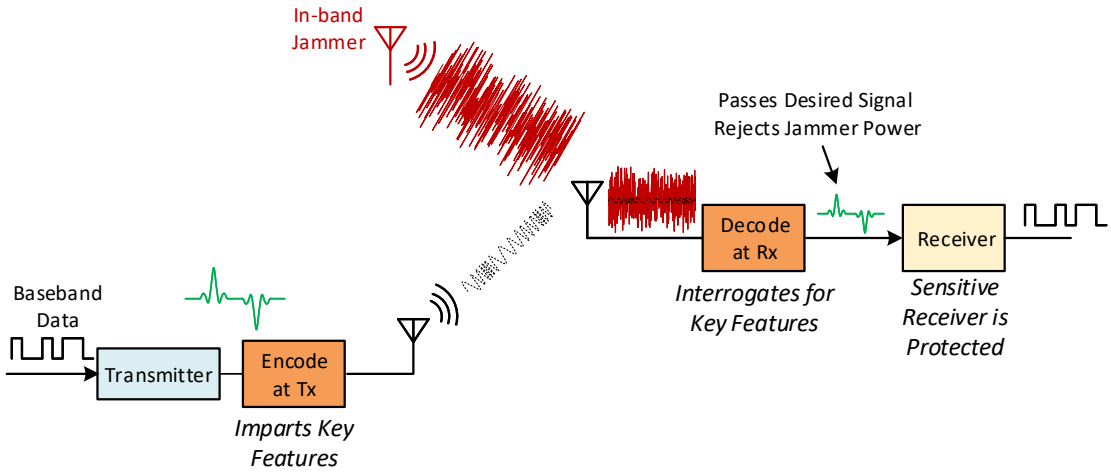


Figure 2.1: RF Signal Processing for In-band Blocker Rejection

2.1 In-Band Blocker Rejection at RF

The objective of this research is to develop transceiver systems that reduce in-band blocker prior to the receiver at RF. This enables RF operation in unpredictable, high interference environments. The transceiver operation is shown in Fig. 2.1 [20].

The transmitter incorporates a code into the signal so that the receiver can differentiate between the desired signal and the interfere and thus removing the unwanted signals. Done at RF this improves the blocker handling capability of the receiver. To do so coding and decoding schemes are implemented using transistor based circuits at RF for the first time. The encoder and decoder can be implemented using any of the spread spectrum techniques. We briefly introduce these communication systems in the next section and discuss their advantages and disadvantages for use in system of Fig. 2.1.

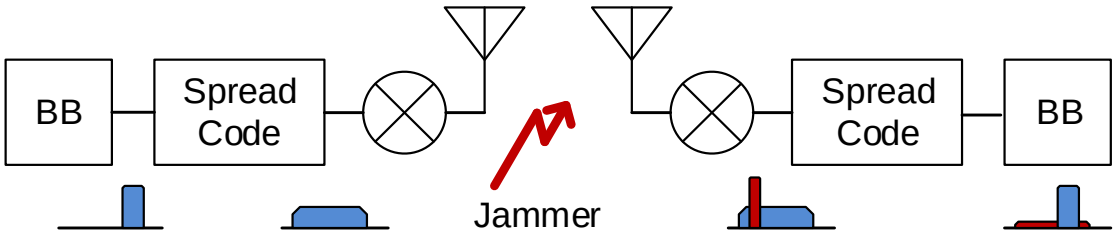


Figure 2.2: Architecture of DSSS system.

2.2 Spread Spectrum Communication Systems

Spread spectrum techniques are used in communication systems for enabling multiple access and avoid blockers. In this chapter two type of spread spectrum communication techniques namely Direct Sequence Spread Spectrum (DSSS) and Frequency Hopping Spread Spectrum (FHSS) are briefly introduced.

2.3 Direct Sequence Spread Spectrum

In this scheme the base-band data is multiplied by a chip signal that is much faster than the data speed as shown in Fig.2.2. The resulting signal is then up-converted and transmitted. In the receiver side, the signal is multiplied by the same chip and the original signal is recovered.

2.3.1 Blocker Performance

The blocker is multiplied by the chip signal and is spread at the receiver side. The data is de-spread and filtered at the same time thus providing blocker resistance or processing

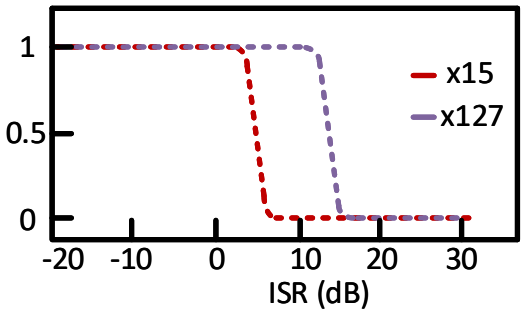


Figure 2.3: DSSS packet throughput throughput vs signal to interferer ratio [1].

gain which is defined in 2.1 where P_G is the processing gain of the system. The downside of this architecture is that DSSS can not avoid the in-band jammer and may completely fail in presence of a large blocker. This happens when the jammer power is higher than the jamming margin [1]. This is shown in the throughput plot of the DSSS system in Fig. 2.3.

$$P_G = \frac{SpreadBW}{DataBW} \tag{2.1}$$

2.3.2 Multipath Performance

The equalization needs to be performed prior to chip multiplication making the RAKE architecture necessary. Thus if implemented at RF, the implementation will be expensive.

2.4 Frequency Hopping Spread Spectrum

The frequency of the Local Oscillator (LO) is changed at the transmit side in accordance with a sequence that is known to the receiver as shown in Fig. 2.4. At the receiver, the

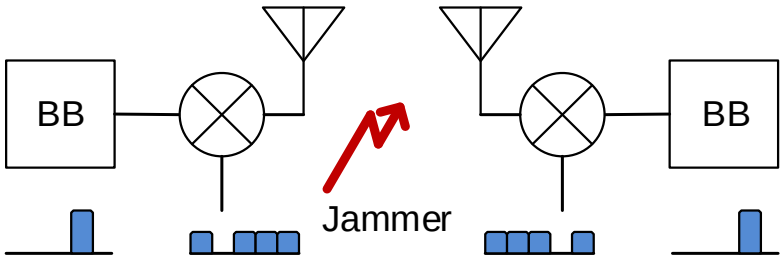


Figure 2.4: Architecture of FHSS system.

same frequency sequence is multiplied to the received signal and the data is recovered after low pass filtering. The advantage of this system compared to the DSSS system is the ability of this system to completely avoid the in-band blockers. Another advantage of FHSS to DSSS is that the TX mask can be improved using LO filtering techniques which is not possible in DSSS. These advantages are further explained later.

2.4.1 Blocker Performance

While it's relatively straight forward to handle out-of-band interferes using on or off chip filters, in-band interferers could easily jam the reception in traditional receivers. To improve the resilience against in-band jammers spread-spectrum techniques can be used. This work, for the first time, demonstrates in silicon the capability of frequency hopping as a means for suppressing in-band jammers. The system is capable of suppressing single or multiple jammers without any prior knowledge of their carrier frequency or bandwidth. The frequency hopping is implemented in the analog domain using passive N-path switches before the received signal goes through any active amplification. This limits the possibility of any of the active circuits from getting saturated due to potentially

large in-band interferes.This jammer rejection property in frequency hopped systems can be easily understood with the help of Fig. 2.5. Suppose that a narrow band jammer exists in-band and is located at one of the receiver channels. Assuming that the receiver visits all the N channels before returning to the channel with the interferer, it only sees the jammer $1/N$ of the times. However, the signal is seen at each of the N channels. Therefore, effectively, the jammer power after the correlation process is reduced by N times while the signal power is retained. In our design with $N = 100$, i.e., 100 channels, the jammer suppression is $10log(N) = 20dB$. This process is shown in Fig. 2.5 where a single narrow-band fixed-frequency jammer, shown in red, is spread by the receive correlator and filtered at baseband. At the same time the received signal which is shown in blue is de-spread. Since this is achieved in the current domain, it limits the voltage swing at the correlator input due to the blocker, enhancing the jammer handling capability of the receiver. This means the system can operate effectively with jammers that are 20dB larger than what would have saturated a normal receiver.

An important advantage of FHSS to DSSS is the ability to completely avoid the blocker channel and operate at a slightly lower speed as shown in throughput versus signal to interferer ratio plot of Fig. 2.6. This means that the communication is possible in presence of large narrow-band interference. However, the broadband blocker is similar for DSSS and FHSS. FHSS is not traditionaly utilized to provide processing gain due to hopping speed limitations. This research presents the first frequency hopping system that provides processing gain. The processing gain is realized in RF in this work.

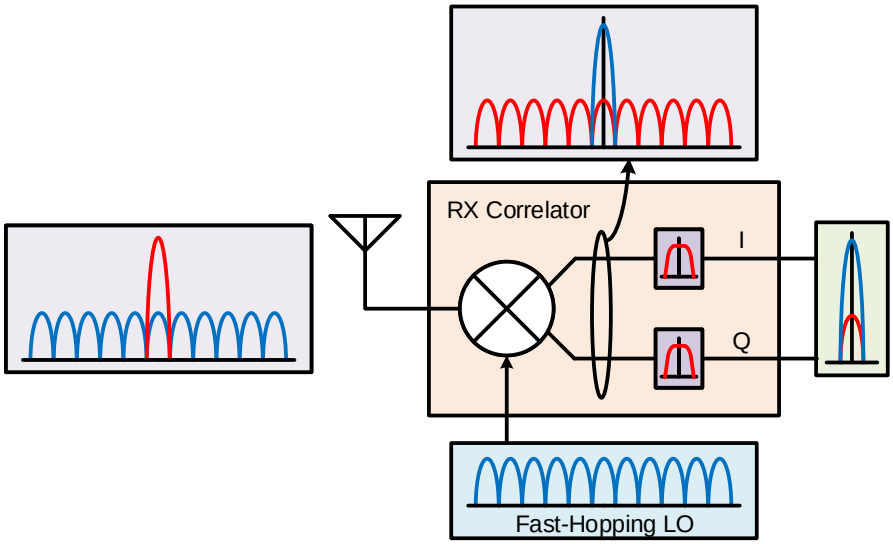


Figure 2.5: In-band jammer suppression using frequency hopped processing gain.

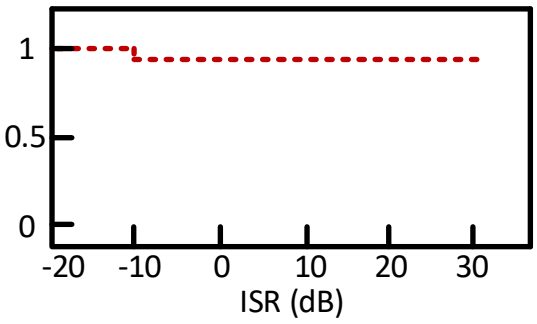


Figure 2.6: FHSS packet throughput vs signal to interferer ratio [1].

2.4.2 Multi-Path Resilience

In a wireless channel, the signal travels through different paths to get from the transmitter to the receiver. The signal that reaches the receiver therefore, consists of multiple copies of the original signal with different delays and amplitude as shown in Fig. 2.7. The amplitudes and delays differ since the length of each path can potentially be different. In the worst case these copies could result in complete cancellation (frequency selective fading) and inter symbol interference (ISI). Traditionally equalization is performed at the receiver baseband to align the received copies and recover the signal. However, in our design it can be shown that in many typical multipath environments there is no ISI thanks to fast hopping nature of the receiver. As shown in Fig. 2.8, receiver jumps to a new frequency before the signal from the second path at first frequency arrives at the receiver. Since the delay from the transmitter to the receiver at each channel is different these need to be aligned if the signal is to add up correctly.

However, there is no ISI. This means that each channel can now be "equalized" by a single complex coefficient in the frequency domain that corrects for the different delays at different frequencies. ISI can be avoided as long as the hop-rate (T-hop) is fast enough so that the receiver only captures the signal that arrives from the first path and not the other copies. All the other copies disappear after T-delay (delay spread). Fig. 2.9 shows Simulink/MATLAB system-level simulations of received baseband data for a typical LTE urban environment. The black line shows the baseband data at the TX side. The blue line shows the received data when TX and RX operate at a fixed

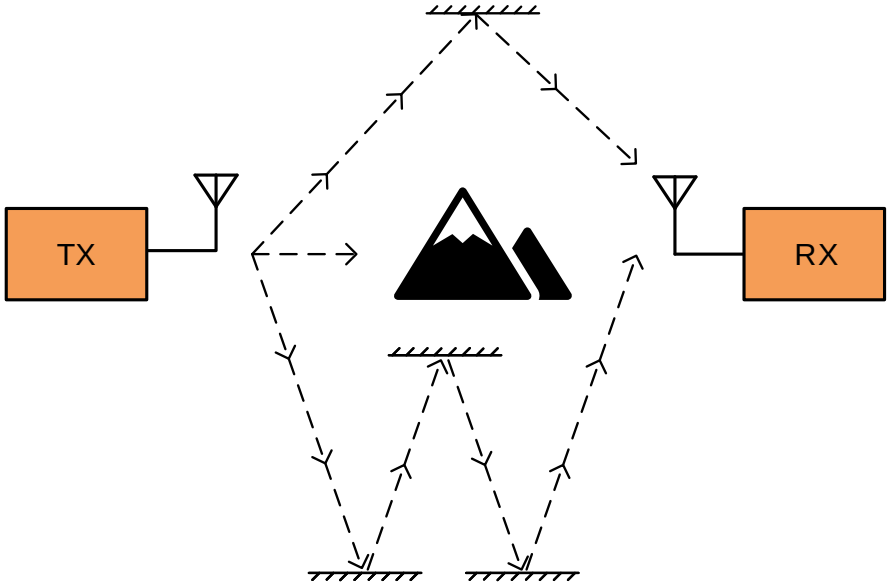


Figure 2.7: Wireless multipath channel.

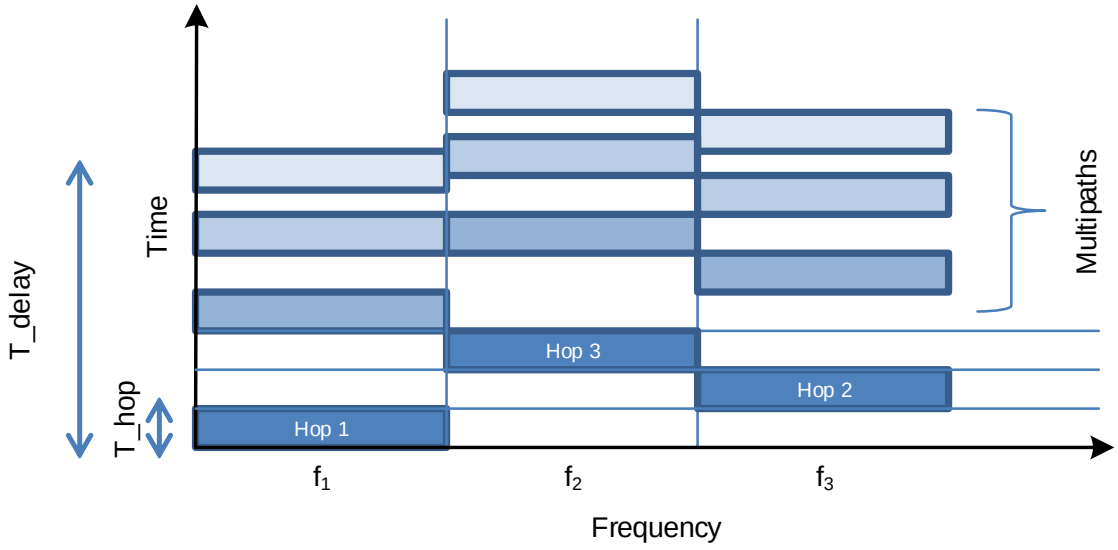


Figure 2.8: Impact of fast hopping on the accumulation of the multiple signal rays at each channel frequency.

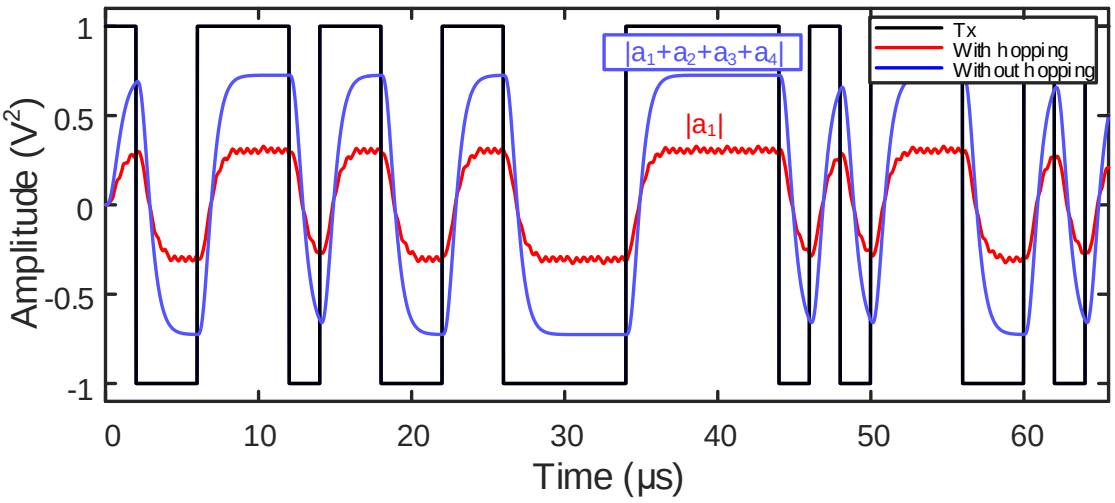


Figure 2.9: Single tap equalization for FH transmitter in an urban multipath channel. BK: Transmit signal, BL: sum of all signal rays (after equalization), RD: received signal with FH transceiver.

RF frequency of 1GHz (after equalization). In this instance, amplitude of the signal is same as amplitude of the summation of all the channel coefficients. The red line shows the received data when TX and RX hop with a hop-rate of 50MHop/s. The amplitude of the red signal is equal to the first coefficient only (a_1) as the system has hopped to a new frequency before the other signal rays (a_2, a_3, and a_4) arrive. This means that the other copies of the TX signal that arrive later do not contribute to the received data in this case. In other words, there is no ISI and each channel can now be modeled using a single complex valued coefficient.

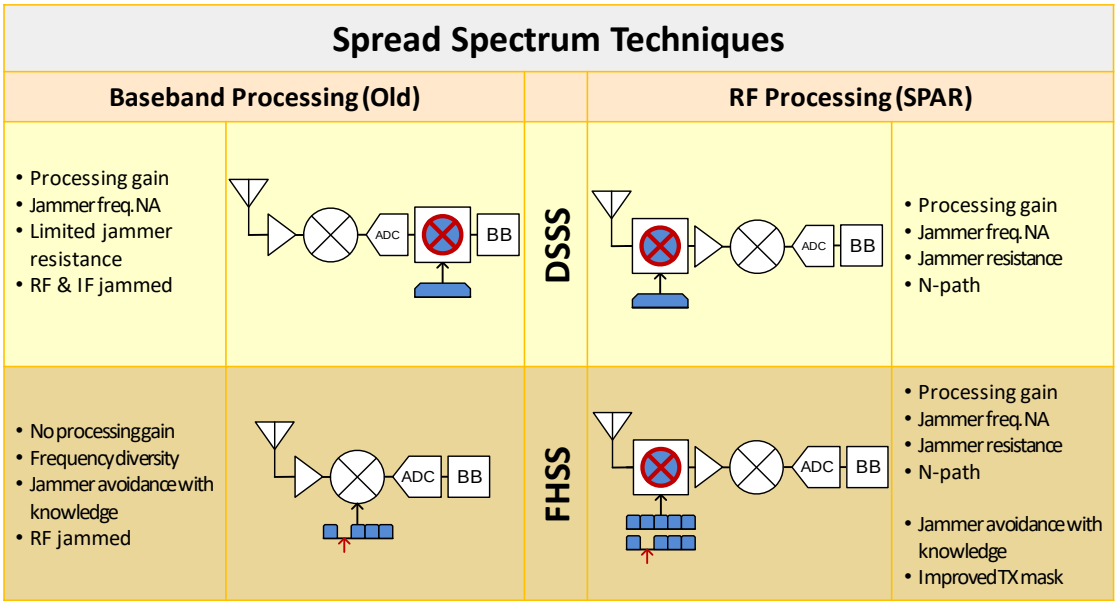


Table 2.1: Comparison of DSSS and FHSS.

2.4.3 DSSS vs FHSS

Table. 2.1 compares the two spread spectrum techniques in the Old designs and the new designs. The DSSS and FHSS share a lot of features but the FHSS has two advantages over the DSSS. First, FHSS system can completely reject the in-band jammer with avoiding the channel where the blocker exists. Second, in the RF domain, the FHSS can use smoother transitions to shape the spectrum and improve the transmit mask which is not possible in DSSS implementation. Another advantage of FHSS over DSSS is that simpler implementation is possible due to multipath avoidance property of FHSS system. This however needs experimental investigation.

Chapter 3

Ultra Fast Frequency Hopping Transceiver Design

3.1 System Level Design

The architecture for the ultra-fast FH system was shown in Fig. 1.1. Next, we clarify system operation and provide system specifications, followed by additional details of the receive and transmit correlators, the self-interference cancellation circuit, and the fast-hopping LO generators.

3.1.1 Transceiver Specifications

The design specifications for this transceiver are based on the requirements of the DARPA SPAR (Signal Processing at RF) program [20]. However, the design is flexible and easily programmed digitally for different processing gains or different hop rates within circuit limits. In addition, the RF center frequency is programmable via the clock input. The current system is designed to be bolted on to the front of the traditional fixed-frequency RF transceiver. Therefore, the receiver (RX) and transmitter (TX) correlators have both a down-converter and an up-converter. For the design shown in Fig. 1.1, the fixed-frequency RF transceiver is assumed to be at 300 MHz. However, this frequency is completely flexible. In addition, the system can be redesigned so that the FH RF is converted directly to the RX baseband and the TX baseband is directly up-converted to an FH TX signal. In which case, the second mixer at 300 MHz in Fig. 1.1 can be eliminated. For the rest of this paper, the architecture in Fig. 1.1 will be assumed.

The transceiver can operate with a center frequency that ranges between 0.4 and 1.0 GHz. The transceiver operates in a 60 MHz "band," which is divided into 100 "channels"

that are each 0.6 MHz wide. The spacing between the channels (channel spacing) is 0.6 MHz. The receiver and the transmitter hop between these channels with a hopping speed of 47 MHop/s, i.e., a hopping time of 21 ns, to enable a maximum symbol rate of 470 KSymbol/s for a processing gain of 20 dB. Both the transmitter and receiver paths operate in this 60 MHz band, but the transmit and receive systems never operate on the same channel to minimize self-interference. The transmitter completes 100 hops for each data symbol, spreading the signal power into the 60 MHz band. This means that the power in each channel is now 20 dB (10log(100)) smaller than the original non-hoped signal, i.e., the processing gain is 20 dB. On the receive side, the signal power from each channel is added back together to recreate the original 0.6 MHz unspread signal.

The overall system operation is best understood with the help of Fig. 3.1 that shows the signal flow through the system. It is easiest to follow the signal by starting at the transmitter. The modulated TX signal is FH by the fast-hopping TX correlator (blue). This signal is amplified by the 2-W off-chip power amplifier (PA) (33 dBm). The PA adds broadband noise (light blue). A portion of this signal (-25 dB down) couples through the duplexer to the RX (now at +8 dBm). The RX sees the FH RX signal (green) plus a narrow-band CW in-band jammer (red). The self-interference cancellation (SIC) block partially cancels (by 20 dB) the FH TX leakage at the receiver (now at -12 dBm). This signal then passes through the RX correlator where the FH RX sees 20 dB of processing gain while the jammer is spread by 20 dB. A filtered version of this signal is sent to the baseband where any residual out of channel signal is removed.

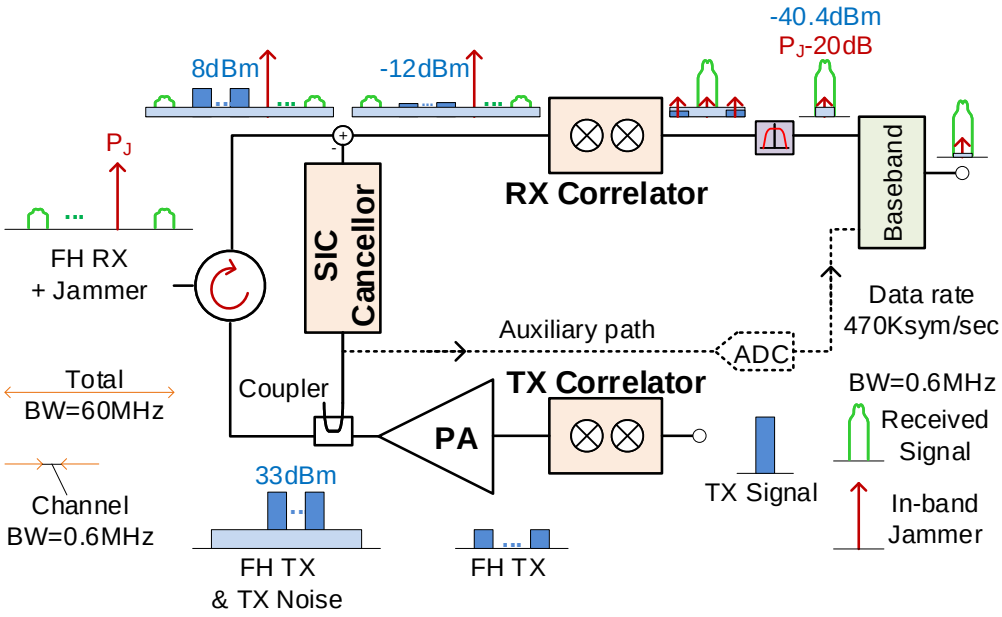


Figure 3.1: Receive, self-interference, and jammer signal flows through the system

As mentioned earlier, the TX and RX channels are orthogonal, and the amount of the TX channel power that shows up in-band in the receiver channel is a function of the TX and RX channel separation and the filtering capabilities of the N -path-based correlators. The residual TX signal after the SIC is orthogonal to the RX LO and, hence, gets reduced by the correlator. Due to the ultra-fast hopping speed of the transceiver, the rejection is limited, and a portion of this power shows up in the receiver channel. The sinc filter response caused by the fast hopping has its first null at the hop rate of 47 MHz. Therefore, there is still significant TX energy in the RX channel. The transmitted signal over one symbol can be written as shown in (1), where P[t] is the rectangular pulse, Th is the hop time, N is the total number of channels, fTi is the transmit frequency at the i th hop, and phiT(i) is the necessary phase at the i th hop at the transmitter to ensure

continuity between the frequency hops

$$x(t) = \sum_{i=1}^{N} P[t-(i-1)T_h]\sin[2\pi f_{T_i} t + \Phi_T(i)]. \tag{1}$$

The signal at the receiver then is given by (2), where fRi is the receive frequency and phiR(i) is the necessary phase at the i th hop at the receiver to ensure continuity between the frequency hops

$$y(t) = \sum_{i=1}^{N} P[t-(i-1)T_h]\sin[2\pi f_{T_i} t + \Phi_T(i)] e^{j2\pi f_{R_i} t + \Phi_R(i)}. \tag{2}$$

The spectrum at the receiver can be estimated by performing the Fourier transform of (2), which can be written as shown in the equation in the following. Here, we note that the transmitter and receiver channels are distinct and that the final spectrum has a sinc shape that is proportional to the hop-time Th . This means that even if RX and TX channels are different, there is still going to be spill over from TX to RX. The spacing between TX and RX frequencies alters the phase and the sinc magnitudes of each of the summation terms that fall in-band and changes the self-interference that shows up in the RX band. As the hopping speed increases, Th decreases, which widens the sinc function that causes more energy to show up in the RX baseband. This problem is normally not seen at lower hopping speeds, as the sinc main lobe is much narrower. We have verified this phenomenon via numerical simulations and also via measurements as

discussed later.

$$
\begin{aligned}
Y(f) = & \frac{T_h}{2j} \sum_{i=1}^{N} e^{-j(2i-1)\pi T_h (f - f_{R_i})} \\
& \times [\mathrm{Sinc}(T_h(f - f_{R_i} - f_{T_i}) \\
& \quad \times e^{j((2i-1)\pi T_h (f_{T_i} - f_{R_i}) + \Phi_T(i) + \Phi_R(i)} \\
& \quad - \mathrm{Sinc}(T_h(f - f_{R_i} + f_{T_i}) \\
& \quad \times e^{-j((2i-1)\pi T_h (f_{T_i} - f_{R_i}) + \Phi_T(i) + \Phi_R(i)}].
\end{aligned}
\tag{3}
$$

Our measurement results for the transmit signal seen at the RX channel for a ten-channel separation between the TX and RX show a 27 dB suppression of the TX signal. For the 8 dBm TX signal input at the antenna and 20 dB suppression by the SIC, this results in a -40.4 dBm self-interference in the RX channel, as shown in Fig. 3.1. The broadband TX noise signal can be suppressed in the digital baseband using an axillary path as in [21] and is not included in this prototype. In the case of the PA, the primary limitation is that since the TX correlators are before the PA, the PA needs to be able to pass the fast hopping signal, i.e., it has to be sufficiently broadband. Not surprisingly, broadband PAs are normally less power efficient than high-Q narrow-band PAs.

3.1.2 Fast-hopping N-path filter core

N-path filters are capable of switching between frequencies instantly. In our design, the receive correlator looks into frequencies that are close to that of its multiphase clock signal. In the transmitter case, the output of the N-path filter can switch instantly to the switching frequency. In case there is a settling behavior associated with the injection locked oscillator, it will show up at the output of the N-path filter. Here, we demonstrate this settling behavior for the system shown in Fig. 3.3. It consists of an injection locked oscillator followed by a divide by two circuit. The resulting four phase signals are then applied to a 4- path filter that up converts the baseband signal to its RF port. The inputs to the capacitors is baseband information. For sake of numerical simulation simplicity, here we only consider the DC component of the baseband signal which gets translated to the clock frequency at the output of the 4-path filter.

The injection signal (Vinj) is a phase continuous frequency hopped signal that is generated using a digital oscillator. Since the oscillator output moves in the frequency domain and additionally has

quantization noise, a high-Q fast hopping band-pass filter (BPF) with programmable center frequency is required. Given the low quality factor of integrated inductors on silicon, implementing such a high- Q filter using passive elements is challenging. Additionally, a passive high-Q filter will take Q cycles to settle. The injection locked oscillator, on the other hand, has a sharper fall off and is used to realize the BPF. We have previously shown that an injection locked oscillator can settle to a new frequency in less

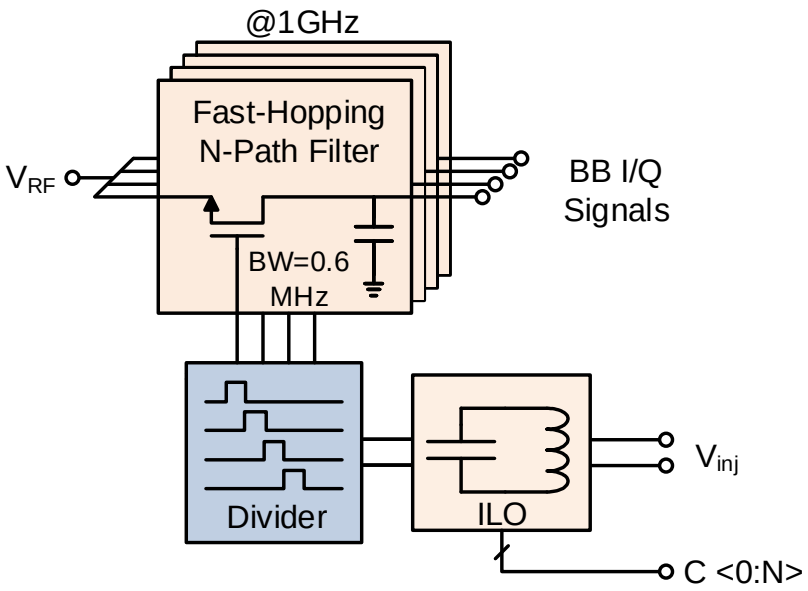


Figure 3.2: Fast hopping N-path and ILO

than 2.5ns in 130nm CMOS technology [17]. We expect the locking time to be shorter in further scaled modern technologies. The settling time of the ILO can be minimized and potentially made zero if the center frequency of the ILO tank is equal to the injection signal frequency and if these two frequencies can be switched at the same time instance. In practice however, settling time will not be zero due to the ILO cap bank finite resolution, switching speeds of the digital switches connected to the tank (tau delay) and process variations. During this period the ILO has an exponential phase settling that has a time constant that is inversely proportional to the locking bandwidth [17]. Any delay in the hopping process results in slight smearing of the output waveform which can be accommodated by adding a small delay to ensure settle behavior. This delay will result in a phase change in the received signal. However, if repeatable it will be removed

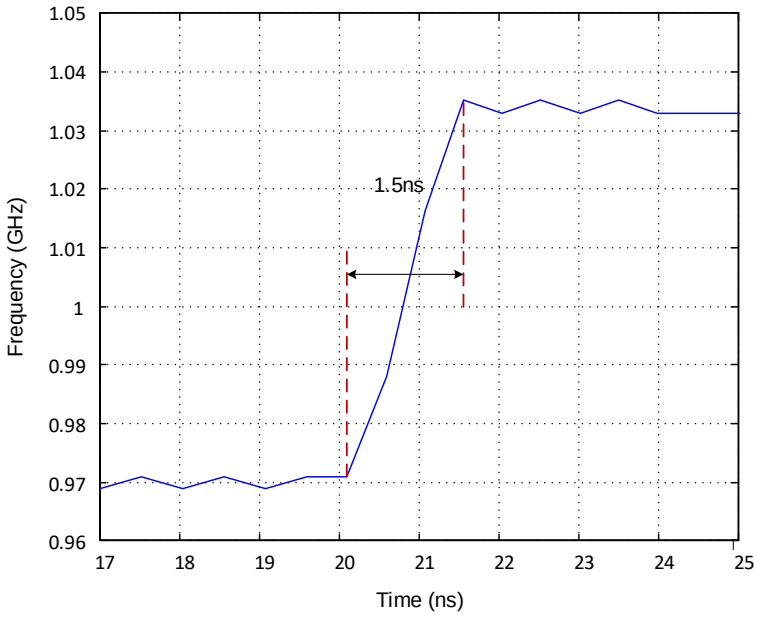


Figure 3.3: Simulation of FH-N-path + ILO

during the equalization and synchronization phase discussed in Section 2.2.

To evaluate this constraint, the system in Fig. 3.2 was designed in 65nm CMOS technology and simulated in Cadence Spectre RF. Fig. 3.3 shows the transient frequency center of the ILO + Divider + N-path filter. The frequency is approximated by evaluating the zero crossings at every half-period. The total settling time is 1.5ns with a frequency estimation granularity of approximately 0.5ns.

Any phase noise in the LO will detrimentally affect the performance of the transceiver both in terms of the direct impact on the EVM and also in terms of jammer resistance and reciprocal mixing. Our design should perform similarly to narrowband systems with fractional-N PLLs. As an example [22] had a-124dBc/Hz phase noise performance at 3MHz offset with a 2.4GHz center for the fractional-N PLL.

3.1.3 Receive Correlator

The receive correlator consists of two passive four-phase mixers. N -path mixers use passive switches and a 25% duty cycle clock generator (for four-phase). These are "digital-like," in which they do not have any memory and can switch frequencies instantly. The only element that maintains memory is the baseband filter capacitor. As long as the RF and LO frequencies are synchronized, the memory element effectively only sees signals close to dc. The mixer on the left that is synchronized to the received signal de-spreads and down-converts the desired signal to baseband. At the same time, the mixer also spreads out any narrow-band blockers that may exist in-band. The de-spread signal is then filtered out to remove any out of band interference. In our design, the de-spreading/processing gain is 20 dB. The blocker is also reduced by the same amount. The reason for the processing gain is that the receiver only sees the blocker once every 100 times, effectively reducing its power by a 100 times or 20 dB. The same thing happens when there are multiple blockers in-band, i.e., the receiver spreads the blockers such that the sum of the powers of the resulting spectrums that show up in the receive channel is 20 dB down. Note that the spreading and filtering/averaging of the blocker occur in the current domain, which means that large voltage swings due to the interferer are avoided.

The resulting baseband signal is then up-converted to a fixed-frequency RF. As discussed previously, the reason for this up-conversion is that the front end can be added to any commercial off-the-shelf (COTS) transceiver, which also allows us to exploit the

excellent noise figure of COTS low noise amplifier (LNA).

3.1.4 Transmit Correlator

The transmit correlator down-converts the fixed-frequency transmit signal with the mixer to the right and up-converts it back to RF using the fast-hopping LO signal. Similar to the receive correlator, the double mixer structure makes this correlator suitable for use with COTS transceivers. The fixed-frequency mixers in the receive and transmit correlators may be removed for an integrated solution.

The hopped transmit signal is then amplified using a broadband linear PA. An example broadband PA that meets our specifications is given in [23]. The PA is operated with 5 dB backoff to insure linear operation. The 33 dBm PA output power is fed to the antenna using an off-chip circulator. This output power enables the transceiver to support a range of 1.5 Km for the 3 GPP suburban channel model, assuming that 30 dBm power is radiated from the antenna. The transmit correlator is placed before the PA to relax its power handling requirements. However, this means that a high-Q narrow-band PA may not be used, as it will ring during channel hopping.

3.1.5 Self-Interference Cancellation Circuit

Part of the large transmit signal at the PA output leaks into the receiver side due to the finite isolation of the front-end circulator. Assuming 25 dB-isolation [20], the self-interference can be as large as 8 dBm at the input of the receive correlator and limits its linearity. The SIC circuit (SIC canceller) is therefore added to cancel a part of this

signal. The circuit is placed after the PA so that any signals due to the PA nonlinearity are also canceled. It does not consume dc power and does not degrade receiver noise performance. The design is based on the same principles as those described in [24] but differs in implementation.

The PA noise is also attenuated by the circulator and shows up in the receive band. The total in-band noise is given by the integration of the attenuated PA noise in a 0.6 MHz band, which is very small in our design and does not limit the performance. For designs where the PA noise is an issue, an extra auxiliary path can be added to cancel the PA noise in the baseband. Previous works have demonstrated 20 dB of cancellation [21].

3.1.6 LO Signal Generator

A potential approach to generate the ultra-fast hopping signals is to use a direct digital synthesis (DDS). DDS circuits are designed to generate any custom periodic signal and therein lie its disadvantage. Here, our goal is to generate the LO signal only. The LO signal can be either a sine wave or a square wave (i.e., odd harmonics are not critical). In comparison to our design, DDS circuits consume significantly more power, as shown in Fig. 3.4. This can be intuitively explained due to the limited function required of the digital oscillator (DO), which generates a sine wave only, while DDSs are able to generate any type of periodic signal. In addition, due to its operational mode, the digital-to-analog converter (DAC) resolution in our signal generator can be of a lower resolution. The power consumption of our prototype in mW/GHz is an order of magnitude smaller

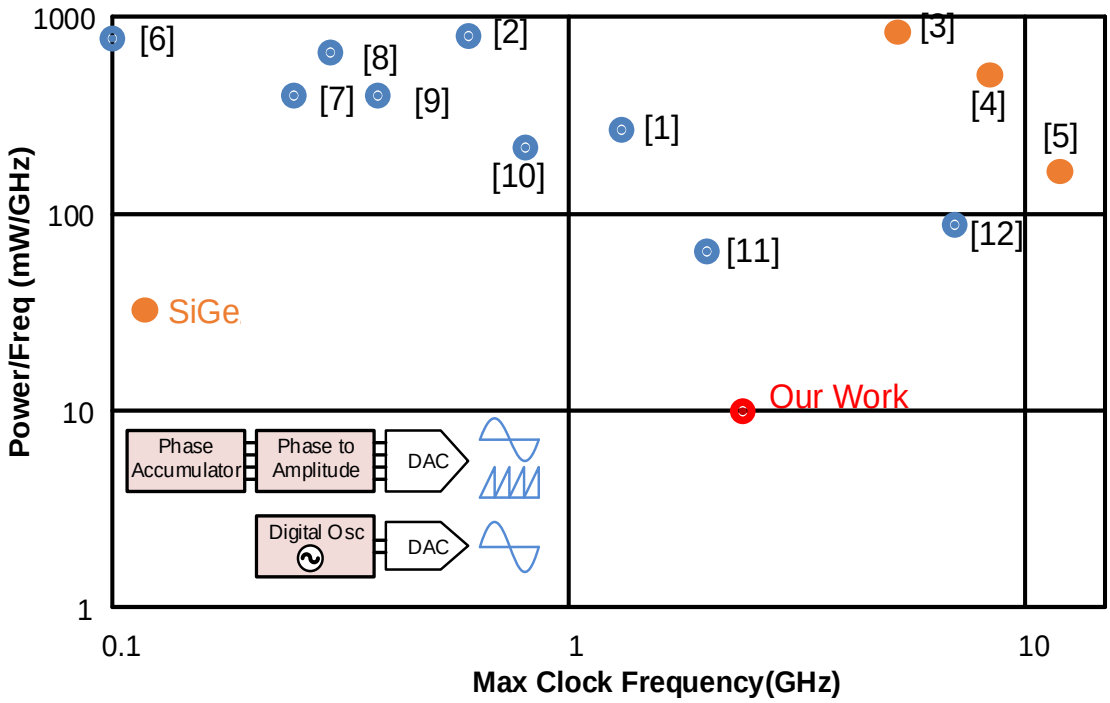


Figure 3.4: DDS versus DO power consumption and maximum clock frequency (see [2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13]).

than prior DDS designs.

In our design, the programmable LO signal is in the range of fclk /4, i.e., the oversampling ratio is only around two. We therefore require a reconstruction filter at the output of the DAC that removes the other unwanted harmonics. The digital oscillator is based on a design presented in [25]. The original design was made to drive a bandpass sigma-delta DAC and was designed for lower speeds. The improved version of the design is shown in ig. 3.5 (left). The new design halves the number of multipliers and integrators, allowing it to operate at higher speeds. The center frequency is set by setting the

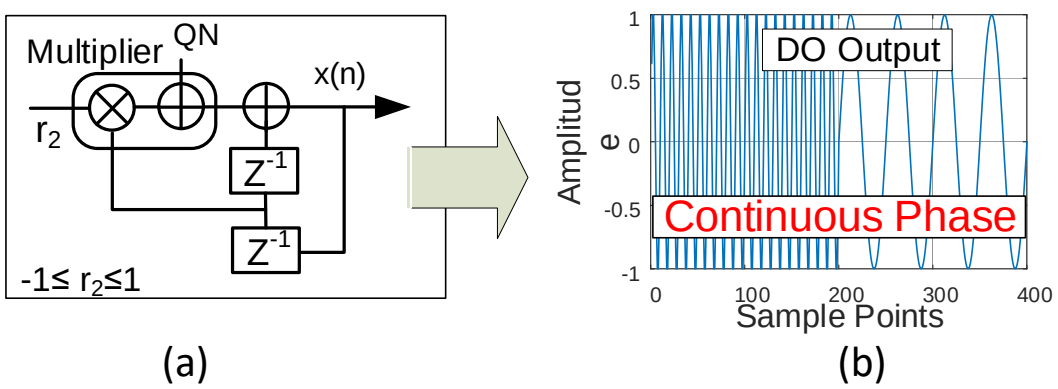


Figure 3.5: (a) Structure of the digital oscillator with an additive quantization noise model. (b) DO output with continuous phase between frequency jumps.

value of r2 in ig. 3.5 (left).

The transfer function from r2 to the output x(n) for the DO in Fig. 3.5 is given by (3). Fig. 3.5 also includes a model for the quantization error in the DO. The roots of the resulting characteristic equation give us the oscillating frequency. In particular, the input variable r2 is limited from -2 to 2 to provide real values, and therefore, the poles can be written, as shown in (4). As a result, the precise output frequency can be simplified to (5)

$$x(n-2) + r_2 x(n-1) + x(n) = 0 \tag{3.1}$$

$$z_{1,2} = \frac{-r_2}{2} \pm j\sqrt{1 - \frac{r_2^2}{4}} = e^{\pm j cos^{-1}(-\frac{r_2}{2})} \tag{3.2}$$

$$f_{out} = \frac{f_{clk} cos^{-1}(-\frac{r_2}{2})}{2\pi} \tag{3.3}$$

When $r_2 = 0$, $f_{out} = f_{clk} cos^{-1}(0)/2\pi = f_{clk}/4$. The output frequency range can be

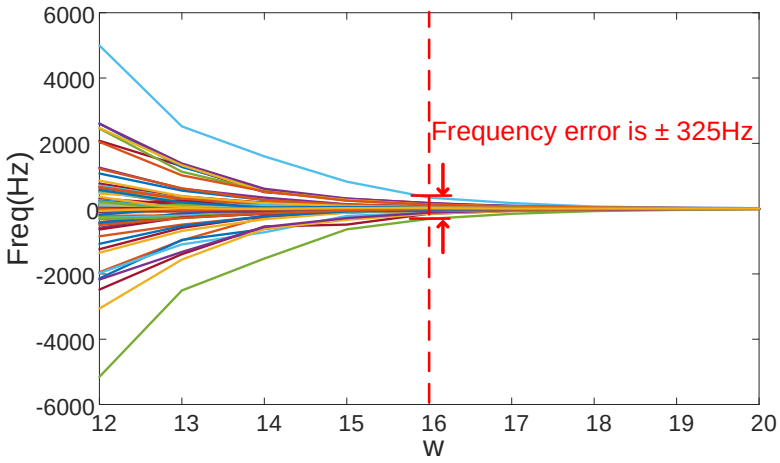


Figure 3.6: Frequency deviation from ideal (frequency error) for all 100 channels vs computational accuracy

varied from near 0 to $f_{clk}/2$.

3.1.6.0.1 Frequency error from computational accuracy The DO output frequency is determined by the value of r_2 and the input clock frequency. The frequency error is determined by the digital computation accuracy. The amplitude of the DO output is solely determined by the initial conditions of the two registers [25]. Next, we discuss the digital computational accuracy needed versus frequency error of the digital oscillator.

Fig. 3.5-right shows the ideal output when floating point computation is used. Note, that the phase is continuous between frequency hops. Fix point computation is more suitable for low power design, but finite computation resolution is likely to degrade the frequency accuracy. Our design uses 100 channels. Fig. 3.6 shows the frequency error

in Hz for all the 100 channels vs the computation accuracy for a tuning range from $f_{clk}/6$ to $f_{clk}/3$. The computational accuracy is varied between 12 to 20 bits. For 16bit computational accuracy, the maximum one-sided frequency error is 325Hz, which corresponds to 0.84 PPM. Most wireless systems allow the crystal oscillator to have a maximum deviation of 10 to 20ppm. We wanted to ensure that the DO did not contribute significantly to this. The computational accuracy is a compromise between frequency error and power. The relationship between the frequency output and the clock frequency given in Eqn. 3.3, is nonlinear, therefore, for simplifying the design of the reconstruction filter and for the modeling of the quantization noise we limit our r_2 input to lie between -1 to 1. All 100 channels lie within this input range. We maintain the same number of computation bits throughout the digital oscillator, i.e., the number of bits at the output of multiplier are the same as at the input. Therefore, choosing a r_2 value that is bounded by +1 and -1 allows us to simplify the design.

3.1.6.0.2 Phase noise from computational & DAC accuracy In a transceiver, the phase noise of the LO has significant impact on the EVM and on jammer performance due to reciprocal mixing. The total phase noise will include the contributions from the a) input clock b) digital oscillator, c) LO DAC and ILO and duty cycle generators for the correlators. In this work we primarily focus on the contributions of the digital oscillator and DAC as other contributors are will understood.

The DO model with quantization noise was shown in Fig. 3.5-left, where the input coefficient to the DO, r_2 sets the oscillation frequency. Therefore, it stands to reason

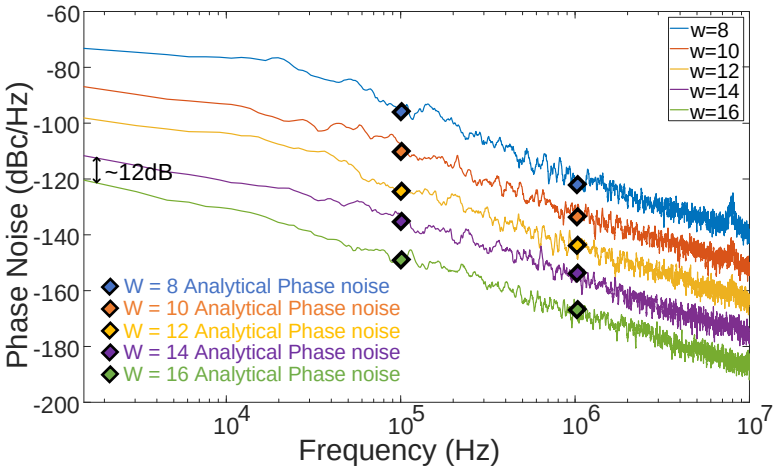


Figure 3.7: Analytical model and numerical simulation for the DO phase noise

that the quantization noise due to finite computation accuracy will cause perturbations in the oscillation frequency, i.e., phase noise. The only contributor to quantization noise is the digital multiplier. In general when two operations of w bits are multiplied then the resultant can have a maximum of $2w$ bits. However, in our system the output is also limited to w bits as r_2 is limited by ± 1 which bounds the quantization noise.

The quantization noise distribution for a multiplier where one of the inputs is a constant is the same as the quantization noise from a regular quantizer (i.e., ADC). So, we can simplify our analysis by assuming that the quantization noise can be modeled as an additive white noise [26]. Using phase noise analysis methods similar to continuous-time LC oscillators [27], we developed an analytical model for the phase noise contribution of the computational accuracy of digital oscillators. We used this analytical model to derive the phase noise at 100kHz and 1MHz offsets for 8 to 16 bits of accuracy. These are shown as diamonds in Fig. 3.7. In the same figure we plot the phase noise contribution

of the DO separately by building a bit-accurate model of the DO in Matlab (lines). For this simulation we operate the DO with w-bit resolution. The output is then down-converted to baseband using an ideal LO and then we perform an FFT on the low-pass filtered signal. We performed these simulations for multiple resolutions between 8 and 16bits. There is good matching between the analytical model and numerical simulations validating our white noise assumption. So, the 16bits accuracy required from a frequency accuracy perspective results in a DO-only phase noise assuming an ideal input source as -163dBc/Hz at 1 MHz offset. This is much lower than the phase noise at the DO output from the input source assuming infinite accuracy of -144dBc/Hz at 1 MHz offset. So, 16 bits of accuracy was considered to be sufficient from both a frequency accuracy and phase noise perspective. The 16 bit fixed point digital oscillator was implemented in Verilog and synthesized using a custom standard cell library in TSMC's 65nm technology.

The DO generates a binary sampled and held sinusoidal signal with W-bit resolution. The DO output is then converted to the analog domain by a DAC. Because our goal is to hop rapidly between frequencies we have to use a memoryless DAC, i.e, not a sigma-delta. The output from the M-bit DAC is then filtered by an ILO with very high Q to remove the unwanted harmonics. Prior work has shown that ILOs can act as high-Q bandpass filters that can jump frequencies almost instantly [17]. The fast hopping nature of the DO, the DAC and the ILO enables the LO frequency to change almost instantaneously. The settling time is primarily limited by the digital circuits that provide the control signals.

3.1.7 In-Band Jammer Resistance

Spread spectrum systems are designed for jammer resistance. The fast-hopping FHSS system designed here is no different. The frequency spectrum and filtering properties of the passive N-path based fast-hopping FHSS system at every frequency hop is shown below. The marron spectrum shows the raised-cosine filtered baseband signal sent by the transmitter. When the receive and transmit channels are synchronized the signal is down-converted to DC at the center of the RX correlator by the frequency hopped N-path filter as shown below. We will first consider the impact of a fixed narrowband jammer and then consider other scenarios.

3.1.7.1 Narrowband jammer performance

For the jammer performance analysis it is easier to assume that the transmit and receive frequencies are fixed and that the jammer is hopping. To first order, simply by virtue of frequency hopping of the 100 channels there is 20dB reduction of a single narrowband jammer. However, this is not the complete story for the simple 1st order N-path filter, shown in blue in Fig. 3.8. In this case when the jammer is in the adjacent channel it is only suppressed by 7dB and if no additional filtering is followed then this signal also shows up at the baseband. However, if care is taken not to alias it in-band then the jammer signal acquired in the adjacent channel can be filtered by post processing provided none of follow on circuits get saturated. As switch based passive circuits, such as N-path filters, are known to have higher linearity than active circuits so higher order

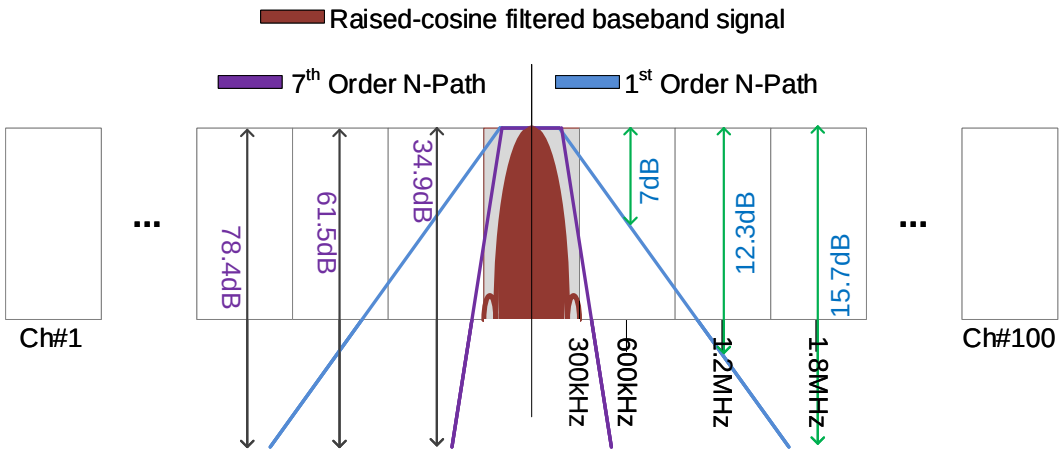


Figure 3.8: Filtering properties of 1st and 7th order N-path passive filters.

IIR passive filters and polyphase filters have been explored as alternatives [28, 29, 30]. In particular, the 7th order N-path filter in [28] approximates a 5th order Butterworth filter and its properties are shown in purple in Fig. 3.8. It behaves almost like an ideal brick wall filter such that we can take full advantage of the 20dB processing gain.

To validate these assertions we have built a simplified frequency hopped system in Mathlab/Simulink. For visual clarity and for ease of simulations we have made the following changes, we have reduced the number of channels to 5, the total hopping bandwidth is increased to 200MHz, the center jammer is 1GHz, the hop-rate is 1MH/s, the transmit signals are offset by 200kHz from DC and a with the same power as the signal is applied at 1.004GHz, i.e., 4MHz offset. The transmit frequency signal (in red) and the jammer (in blue) are shown in Fig. 3.9.

In Fig. 3.10 we plot the baseband signal from DC to 120MHz, i.e., all channels. A single channel only goes till 25MHz (200MHz/(5-1)/2). We note that as suspected the

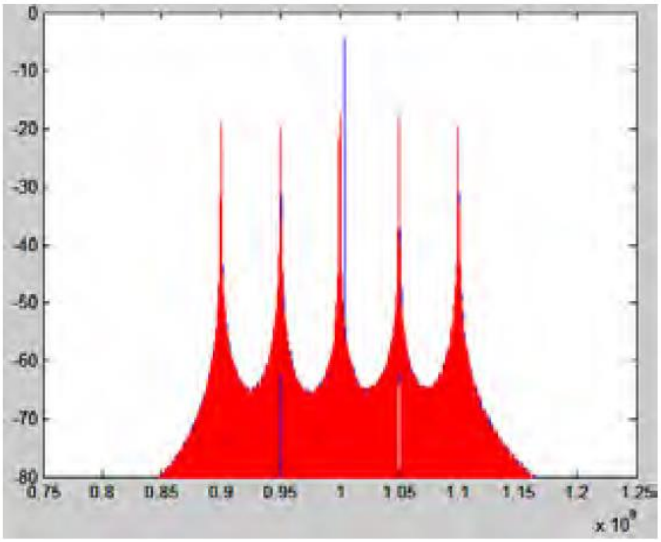


Figure 3.9: Frequency hopped transmit signal (red) + jammer(blue). X-axis frequency, Y-axis magnitude in dB.

in-band jammer is suppressed by the processing gain. However, the jammer signal still shows up in the adjacent channels. We also note that for the adjacent and alternate adjacent channels there are two jammers, one from the negative frequency and one from the positive frequency but now the separation between them is 2X, i.e., 8MHz. In the actual architecture with an I/Q mixer we would be able to distinguish between positive and negative frequencies.

Fig.3.11 a shows SpectreRF (Cadence) simulation for a frequency hopped input, a frequency hopped N-path (0.6MHz) with a NB jammer at 1.036GHz. After the N-path filter the desired signal is upconverted to 1GHz. The desired signal is "despread" and the NB jammer signal is "spread" and filtered. Jammer only spreading was verified in a separate simulation. In this simulation the total bandwidth was increased to 60MHz (for

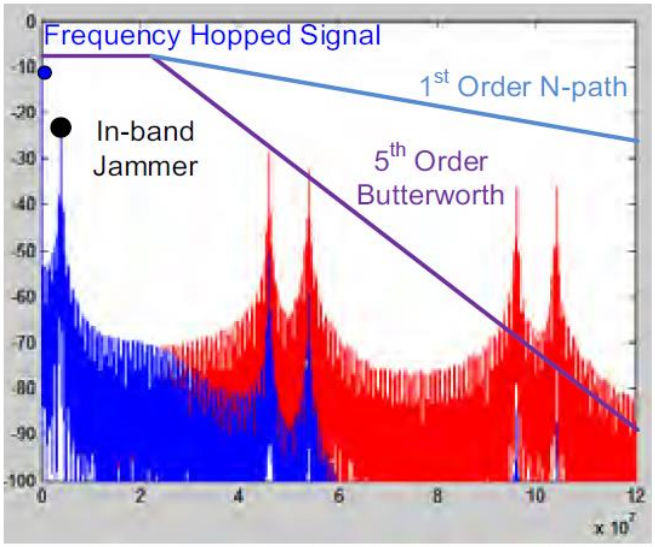


Figure 3.10: RX signal from 0 to 120MHz for 1st order N-path(blue) and 5th order Butterworth (red). Channel is 25MHz

10 channels) for visual clarity only. Out-of-band IIP3 is usually greater than in-band IIP3 by 4dB to 10dB [31, 32]. In our FH-N-path the in-band interference is out-of-channel 99/100 times, i.e., the effective average IIP3 is likely to be much better than for non-hopped systems, i.e., we should have better jammer resistance.

3.1.7.2 Multi-tone and barrage jammers

The performance to multi-tone jammers or to broadband noise jammers, i.e., barrage jammers, are likely to be no different than from DSSS techniques. Once the SNR per channel drops below the minimum required SNR that channel cannot be used for signal transmission. Performance will differ depending on the shape and power of the barrage jammer. For example, if the 3-sigma power PDF is normally distributed and covers

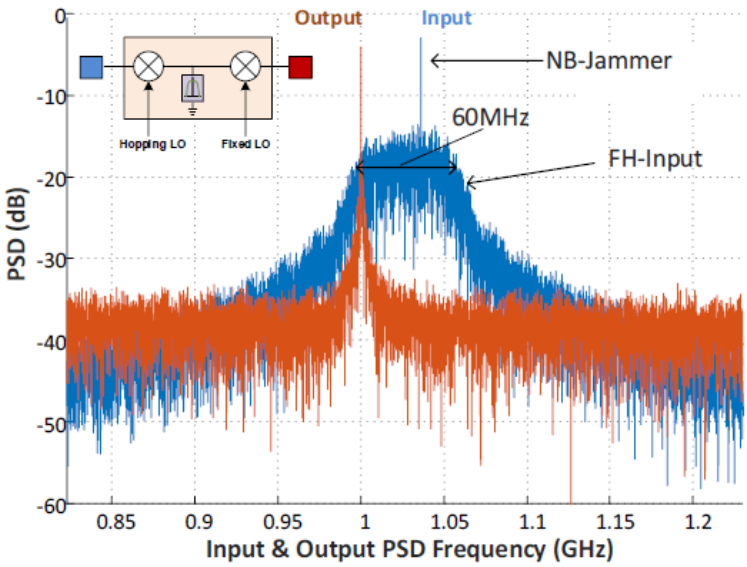


Figure 3.11: Circuit simulated response to NB jammer @1.036GHz (10 channels, 60MHz RF BW, simulation time 24us, step 100ps)

60MHz, then the channels at the jammer center are likely to fail first and the channels at the edge will fail last. If the channels at the end still have a positive SNR then the frequency hopped system will still be able to operate but at a lower throughput. This is one of advantages of a smart frequency hopped spread spectrum system that is able to avoid overloaded channels. Alternately, if the jammers are restricted to 60MHz centered at 1GHz then avoidance strategies like moving the center frequency can be attempted. However, this requires that the 60MHz band select filter up front also be moved. We still obtain 20dB broadband interference rejection.

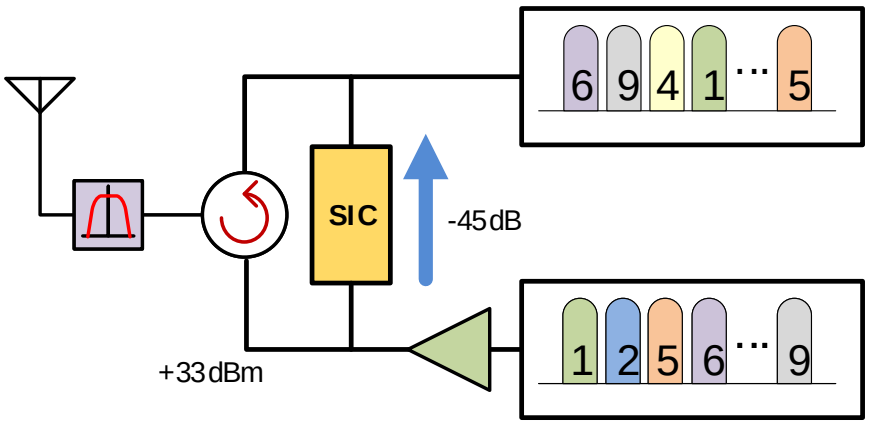


Figure 3.12: Orthogonal TX and RX channels

3.1.8 Handling Self-Interference

Self-interference jamming in this design is handled in two ways, one at the system level and one at the circuit level. At the system level self-interference jamming is virtually eliminated by ensuring that receive and transmit channels are never coincident. This is illustrated in Fig. 3.12. In this figure the transmit and receive channels are never coincident, i.e., when the transmitter is on channel 1 the receiver is on channel 6, when the transmitter is on channel 2 the receiver is on channel 9 and so forth.

3.1.9 Maximum hop rate

The maximum hop rate is primarily limited by the settling behavior of the very narrow N-path filter, i.e., the voltages on the baseband capacitors. The 25% duty cycle of a 4- path filter makes the resistance behave like a switched resistance of 4xRs leading to a time constant of 4RsCi. The one-sided bandwidth is 600kHz/2=300kHz leading

to τ=0.53us. The total time for the capacitors to settle is 4τ =2.12us. During this period the input data must not change and the system should have completed the 100 hops. This leads to a maximum hop rate of 47Mhops/s and a maximum data rate of 472ksymbols/s. If we assume an interchannel hop time of 2.5ns, limited by the ILO, the maximum dwell time becomes 18.71ns. The data rate is also consistent with the maximum data rate that can be supported in a 0.6MHz channel which for BPSK data is 428.6kbps [Raza11]. Fig. 3.13 shows the SpectreRF transient simulation response for the voltage at the 1st N-path capacitor with and without hopping. Recall, this is the baseband downconverted equivalent of the RF. The subfigures show the capacitor voltage for two signals, one exactly at the LO frequency and one that is offset by 300kHz. To reduce simulation time the number of channels was reduced to 10 with a hop rate of 20Mhops/s. The right sub-figure shows the same simulation but now with a hopping input and a hopping N-path. We note that as expected, synchronized frequency hopping does not affect signal detection but results in the 20dB processing gain desired.

3.1.10 Multipath Performance

For multipath channels, it is important to understand the effect of frequency selective fading on system performance. Fig. 3.14 shows a typical frequency response of a multipath wireless channel. If the BW of the signal is smaller than the coherence BW of multipath channel, the channel can be approximated by a flat frequency response. The BW of each channel in our system is 0.6MHz so that for multipath channels with coherence BW larger than 0.6MHz, a single tap equalizer is sufficient. For instance, 3GPP

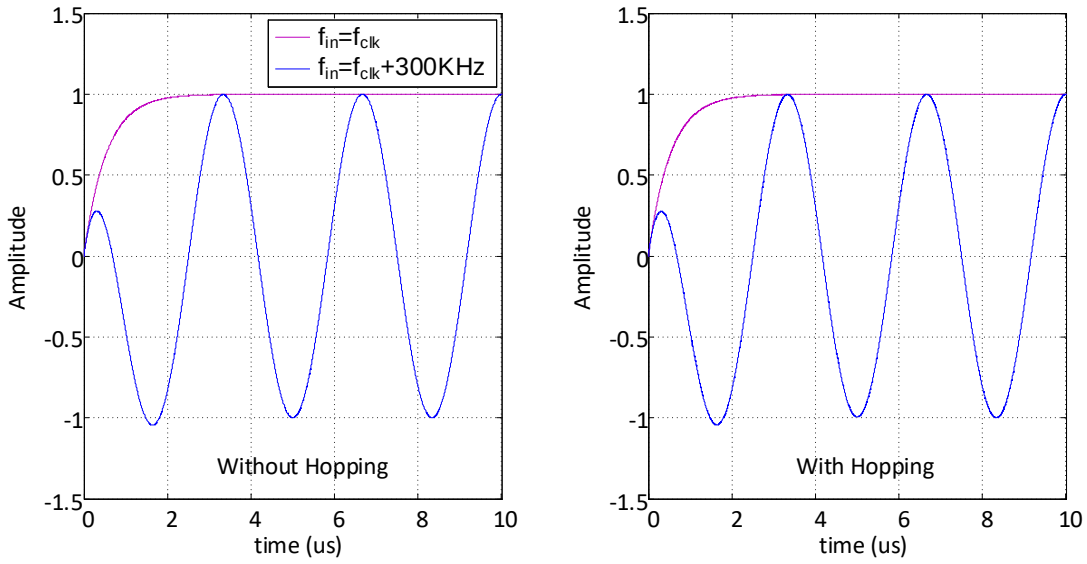


Figure 3.13: Transient Spectre RF response of the N-path filter capacitor with and without hopping (0.6MHz, 10 channels)

rural area channel has coherence BW of 1MHz. We focus on such channels for the purposes of this project.

The equalization can be done in the RF front-end itself. To do the equalization a phase-shifter is required. Fig. 3.15 shows that a 3-bit/2-bit phase shifter results in only %2.5/%10 power loss in a 3-GPP rural area channel model. The Fig. 3.15 also shows an 8-path filter structure and the relative phase of different channels that need to be compensated by the phase shifter. We can use different phase shifter architectures but we propose a scheme that takes advantage of already available phases of the N-Path filter. This architecture is shown in Fig. 3.16 where a logic circuit determines the order of clocking and hence can control the phase of the down-converted signal. The traditional

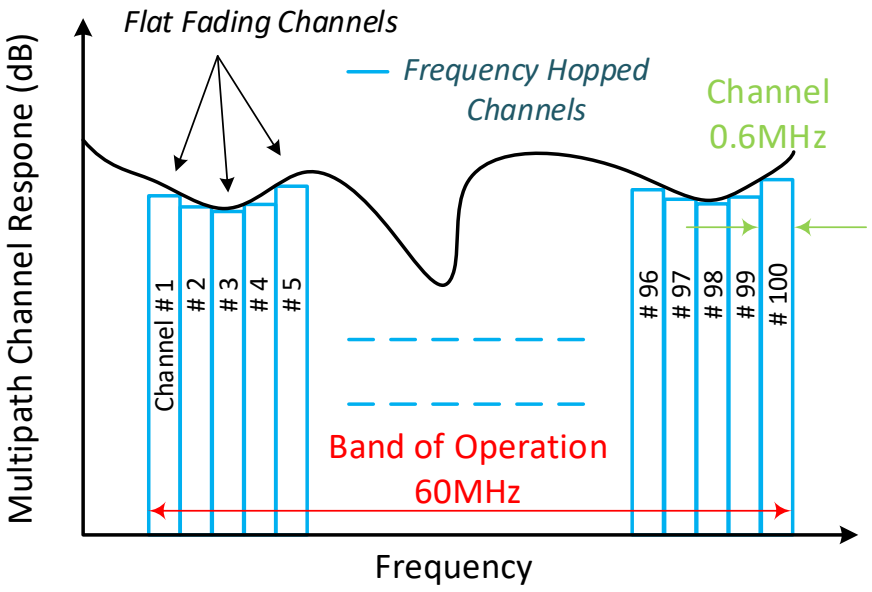


Figure 3.14: Wireless channel frequency selective fading.

LO path phase-shifting is also shown in this figure where a phase shifter is included in the LO path. In our design the proposed incorporation of the phase shifting function into the N-Path filter would be sufficient to equalize the band of interest. Table.3.1 compares the 8-path and 4-path filters for equalizations. Having 8 different phase steps an 8-path filter can be used to implement a 3-bit phase shifter. We however focus on the 4-path implementation in this work and leave the 8-path filter for future investigations.

An important property of this design is the ability to avoid Multipath by hopping very fast. This can be understood by the help of Fig. 3.17 which shows 3GPP rural area channel model tap weights. The second tap arrives 42ns after the first one. By that time the receiver has already moved to another frequency since the hopping rate is around 20ns. If the receiver avoids this channel for the next 0.6us, then the Multipath can be

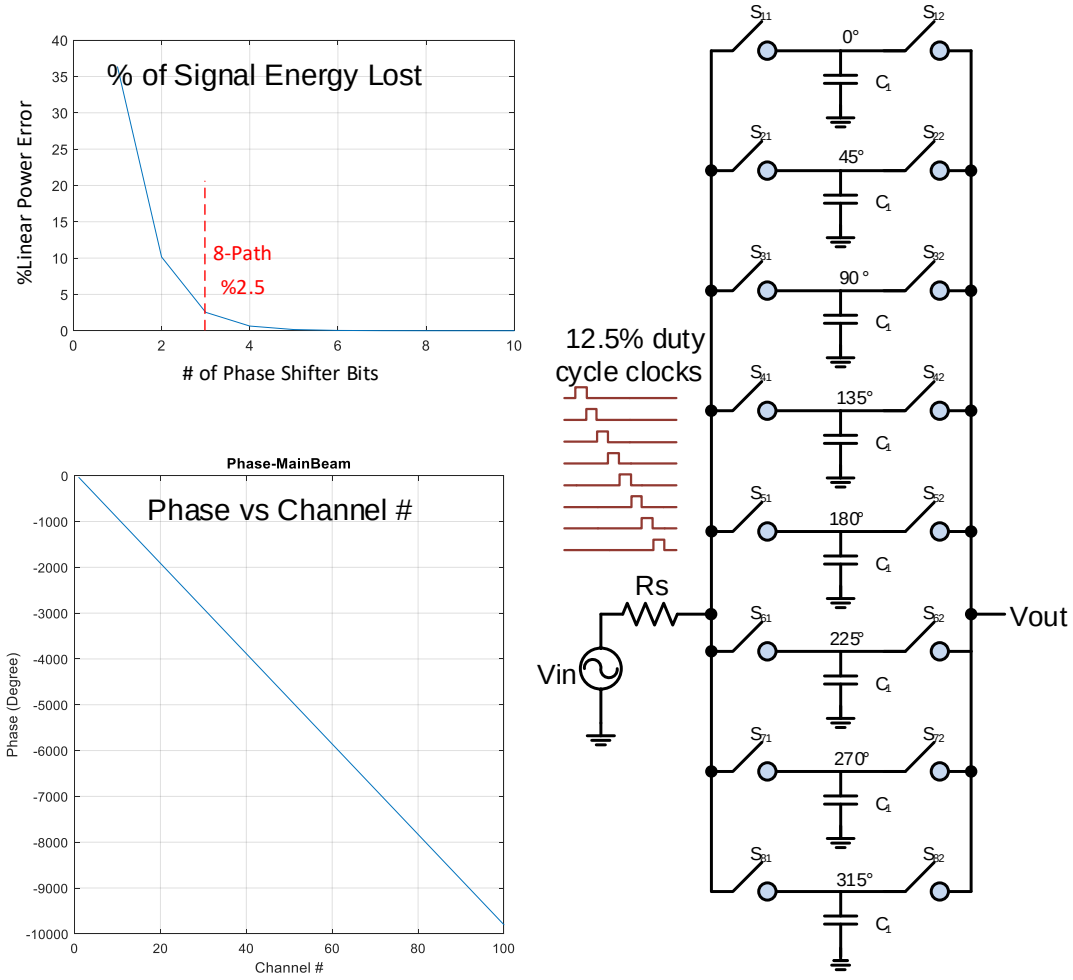


Figure 3.15: Power loss percentage vs phase shifter resolution.

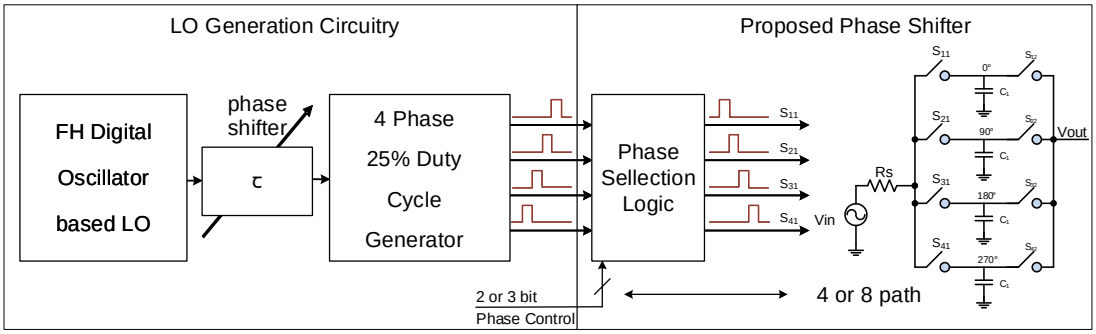


Figure 3.16: Proposed incorporation of the phase shiter into the N-Path filter.

Table 3.1: Comparison of the effectiveness of 8-path and 4-path filters in channel equalization

Topology	# of phase steps	# of phase shifter bits	Equalization power loss (%)
4-path	4	2	10
8-path	8	3	2.5

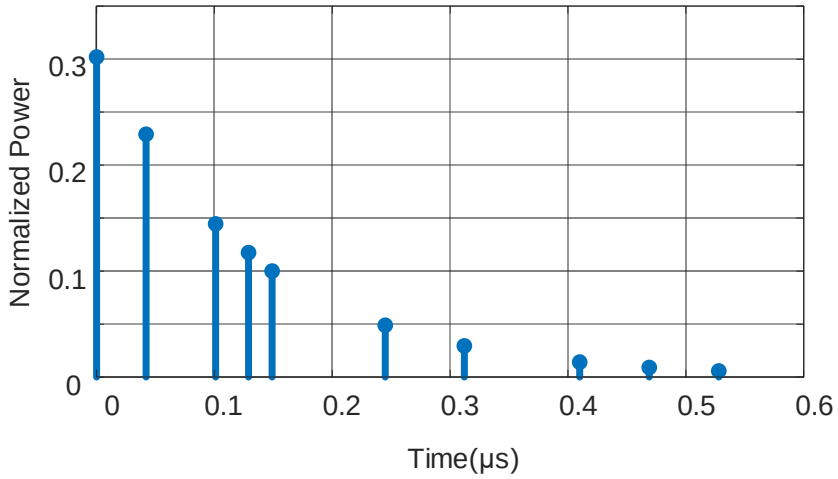


Figure 3.17: 3GPP rural area channel model tap weights.

completely avoided. This is the first time any receiver has the ability to avoid Multipath of the wireless channel.

Since no multipath exists, no RAKE receiver (Fig. 3.18) is required and a single single phase shifter is enough for the equalization as discussed above. This however needs to be verified by future measurements.

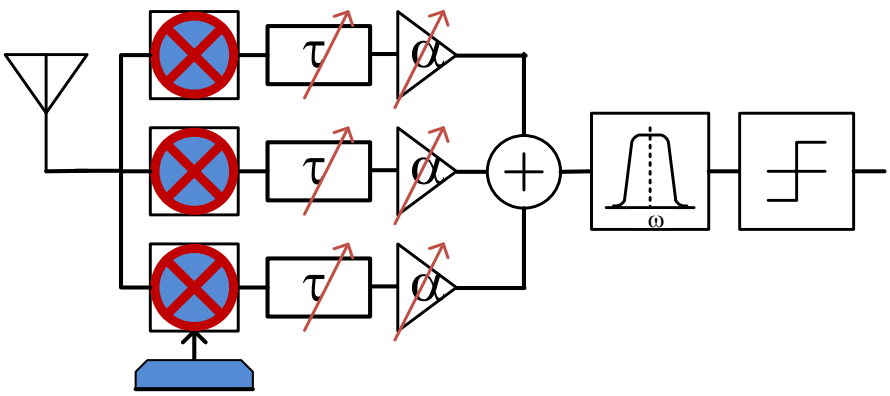


Figure 3.18: Structure of a RAKE receiver.

Table 3.2: Typical PA specifications

NF (dB)	Power Gain=A_P (dB)	System Bandwidth (MHz)
10	24	60

3.1.11 PA Noise

The PA is shown in the system diagram of Fig.3.19 and it does not contribute a significant noise to the system as calculated below. To prove this, we assume typical specifications for the PA that are shown in Table. 3.2. Using Fig. 3.19 the PA noise is calculated

$$P_{N_PA} = -174 + 10.log_{10}(BW) + NF + A_P - 25 - 20 = -107.2dBm \qquad (3.4)$$

where P_{N_PA} is PA noise in the RX band and equals -107.2dBm. This is below RX sensitivity spec of -103.8 dBm. Lower noise PA can always be used for better performance.

It is assumed that the circulator has 25dB of insertion loss and that the PA noise

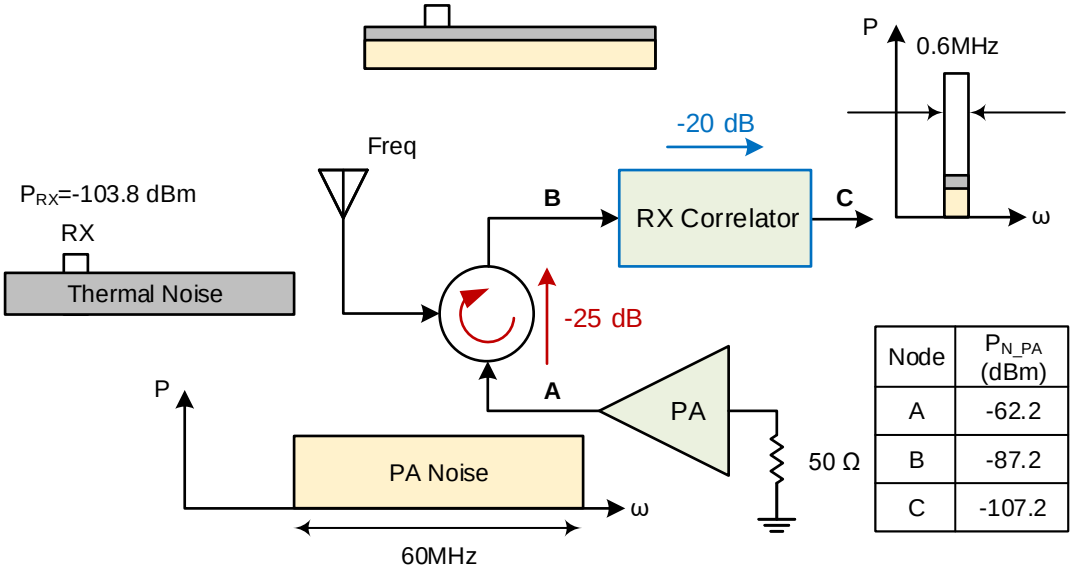


Figure 3.19: System diagram used to calculate PA noise in RX band.

is white and it's spectrum does not change by going through the first mixer in the correlator. Assuming 100 channels, the effective BW reduces by 100 times after the correlator. That is why the PA noise goes down by 20dB in Fig. 3.19 after passing the correlator. It is assumed that extra filtering can be performed in base-band if necessary. We do not expect the need to extend the SIC canceler to cancel the PA noise based on the calculations presented here. The auxiliary path that is used in [21] is an option which is not required in this work. It samples the spectrum at the large enough bandwidth to be able to cancel the noise in the base-band. This is not however attempted here due to the low noise floor from the PA.

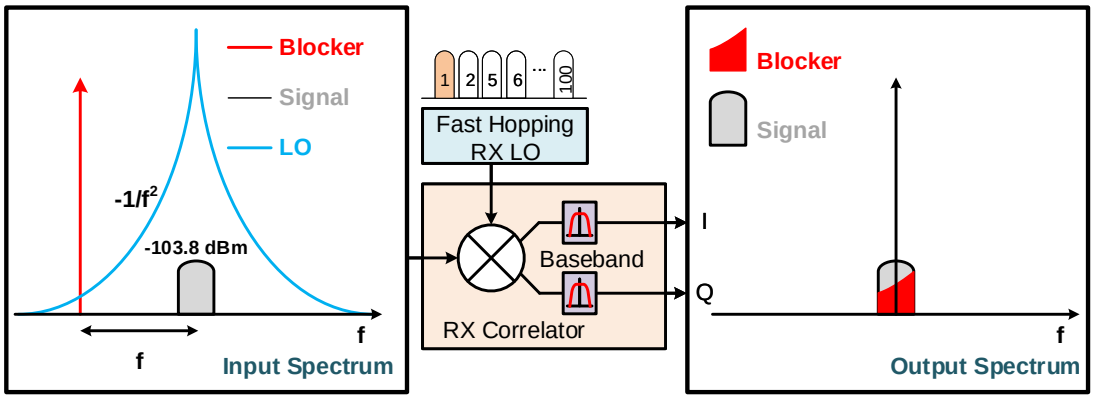


Figure 3.20: PN impact due to reciprocal mixing.

3.1.12 Impact of Phase Noise

Here we investigate the impact of phase-noise due to reciprocal mixing. In particular we show how much interferer can be tolerated at each offset frequency. For simplicity we assume that the blocker can be located at the center of each channel. It can be shown that the phase noise that is down-converted to base-band in Fig. 3.20 can be calculated as follows

$$A_{B-PN} = PN_{1MHz} + 10log10(10^6(\frac{1}{f-0.5} - \frac{1}{f+0.5})) \tag{3.5}$$

Where PN_{1MHz} is the phase noise of local oscillator at 1MHz offset and P_{B-PN} is the blocker conversion gain due to phase noise (PN). It represents the conversion gain with which the interferer gets down converted to base-band and on top of the desired signal. Assuming $PN_{1MHz} = -140dBc/Hz$, the A_{B-PN} is plotted versus frequency offset and is shown in Fig. 3.21.

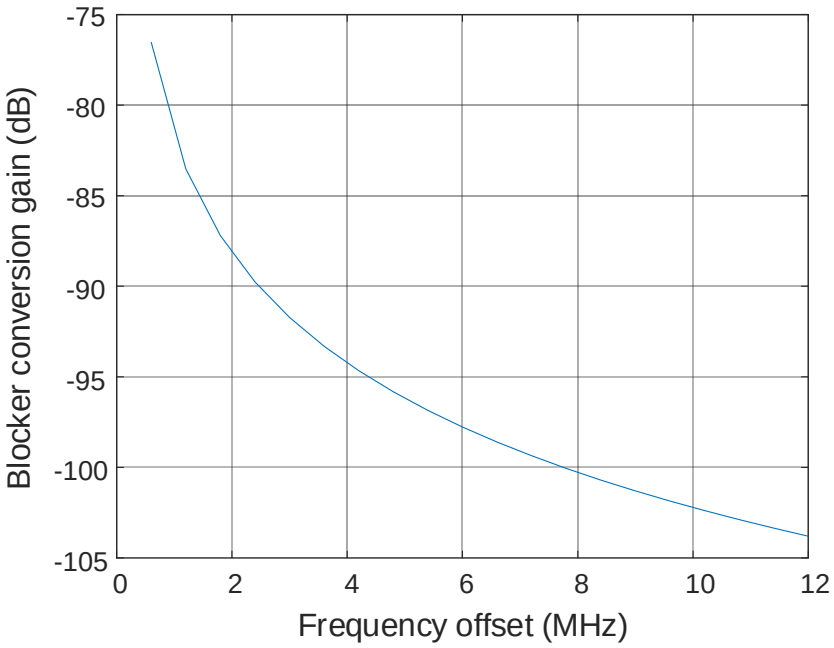


Figure 3.21: Blocker conversion gain due to PN.

Assuming -103.8dBm receiver sensitivity and $PN_{1MHz} = -140dBc/Hz$, the maximum tolerable blocker can be calculated using 3.5 as follows

$$MaxP_B = -103.8dBm - A_{B-PN} \tag{3.6}$$

Where the $MaxP_B$ is the maximum blocker power that the receiver can handle before it fails and is plotted in Fig. 3.22.

3.1.13 Passive Front-End Filter

A passive front-end filter is required after the antenna to remove any out of band blockers and select the band of interest. However due to fast hopping nature of the receiver some

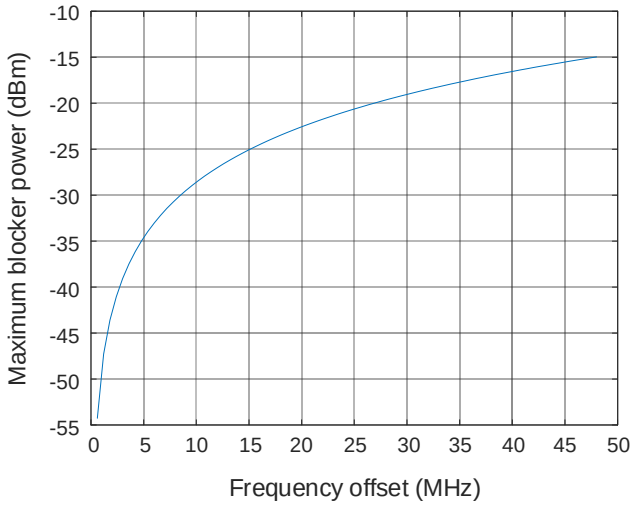


Figure 3.22: Maximum blocker power that receiver can handle due to PN for a received signal power of -103.8dBm.

of the signal will be lost due to falling outside the allocated hopping time as shown in Fig. 3.23. The loss due to the filter can then be calculated as follows

$$\frac{P_2}{P_1} = \frac{T_h - \frac{5}{12}t_r}{T_h - \frac{t_r}{3}}, t_r = \frac{1}{BW} \tag{3.7}$$

Where T_h is the hopping time, t_r is the filter rise time, and BW is the bandwidth of the filter.

Using 3.7 and given that the rise time of the filter is roughly one over the filter bandwidth [33], signal loss is plotted in Fig. 3.24. This shows that a trade off exists between filter bandwidth and insertion loss. Note that this loss is without any equalization in base-band. With proper equalization the insertion loss is negligible and is verified in MATLAB.

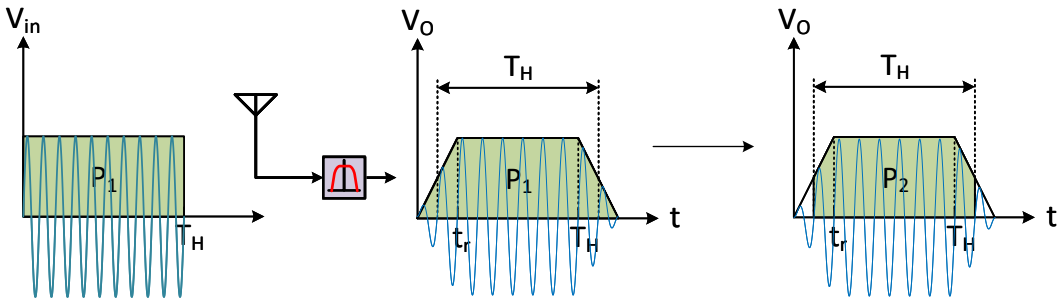


Figure 3.23: Signal loss due to the band-select passive front-end filter.

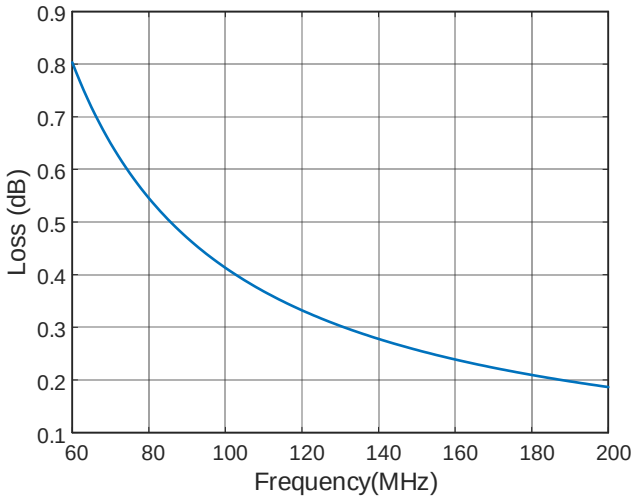


Figure 3.24: Signal loss versus bandwidth due to the band-select passive front-end filter.

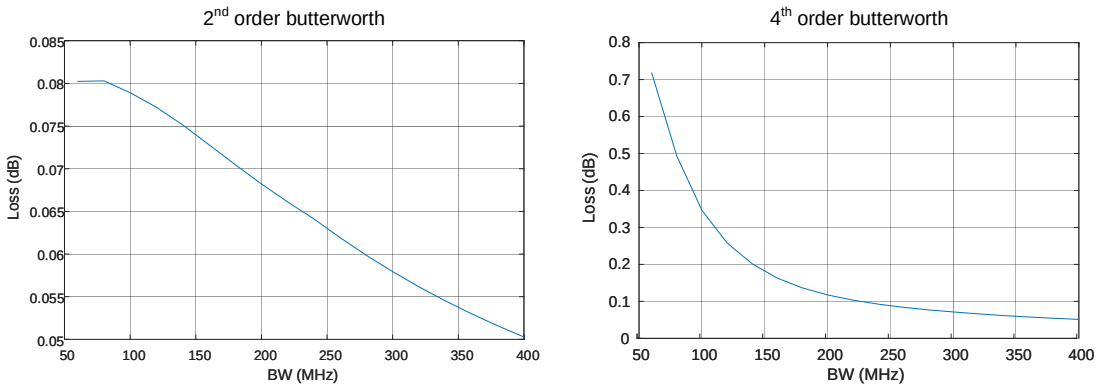


Figure 3.25: Front end filter insertion loss after base-band equalization.

Fig. 3.25 shows the insertion loss after base-band equalization of the front-end filter for second and forth order butterworth filters.

3.1.14 TX Spectrum Modeling

Given the random hopping nature of our ultra-fast FHSS system, modeling the TX spectrum mathematically can be a very mathematically involved task. Here we approximately derive a formula for the transmitter spectrum. To do this we note that the transmit signal consists of 100 different frequencies that are randomly distributed in time domain. Fig. 3.26 shows one of the frequency components in the time domain. In total there are 100 such time domain signals that makeup the TX signal. Thus the spectrum of the transmitter is summation of spectrum of all the 100 time domain signals.

$$S_{NRZ}(f) = 2(\tau_D A)^2 \frac{sin^2(\pi f \tau_D)}{(\pi f \tau_D)^2} \tag{3.8}$$

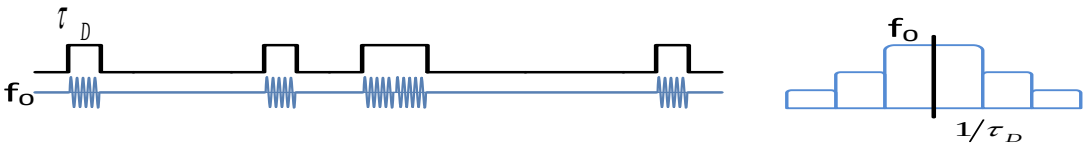


Figure 3.26: One of the frequency components in the time domain.

$$S_{TX}(f) = (\tau_D A)^2 \sum_{i=-N/2}^{N/2} \frac{sin^2[\pi(f+f_i)\tau_D]}{[\pi(f+f_i)\tau_D]^2} \tag{3.9}$$

Where τ_D is dwell time. Output spectrum is sum of all channels. The calculations that are presented here are to provide insight and do not take into account the phase of the sinc functions to simplify the problem. Fig. 3.27 shows the theoretical TX spectrum of the transmitter. The red plot is a single frequency hop as shown in Fig. 3.26 and in 3.8. The blue line shows the total sum as calculated in 3.9. The resulting spectrum is very close to the actual measurements that we have performed on the transmitter. This similarity suggests that equation 3.9 can be used to characterize the TX spectrum. In this plot hopping speed of 50MHops/s, 100 channels, and 0.6MHz channel spacing are used. The channels are centered around DC to speed up the plot..

3.1.15 TX Spectral Mask Shaping

The TX spectral mask can be improved in FHSS systems by applying a filter, for instance a raised cosine, to the local oscillator signal. This causes more gradual transition in frequency and thus reduces the occupied BW as shown in Fig. 3.28. This however is not possible in DSSS if attempted at RF. An example of such raised cosine filtering and

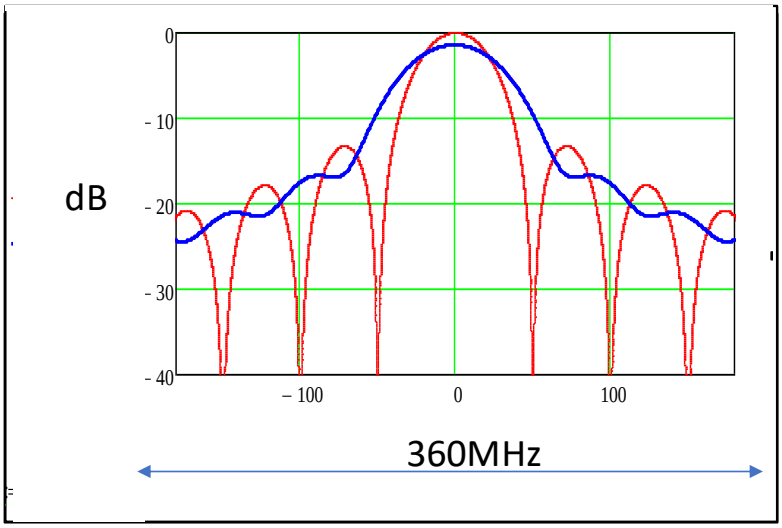


Figure 3.27: Theoretical TX spectrum of the transmitter.

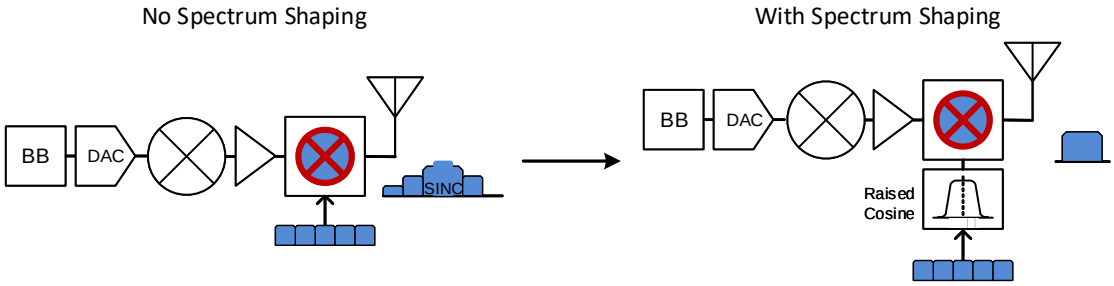


Figure 3.28: Raised cosine filtering to improve spectral efficiency of FHSS.

spectral shaping is shown in simulation of Fig. 3.29. As shown in this figure, the side lobes can improve as much as 50dB.

3.1.16 Estimation of Residual Self-Interference

We use MATLAB simulations to estimate the self-interference from the local transmitter that is located on the same die. To do this we only look at one of the channels at the

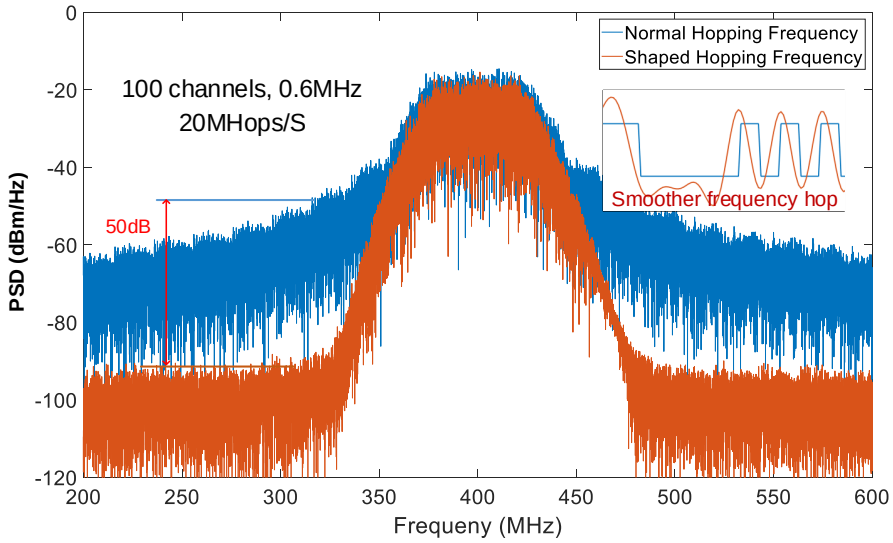


Figure 3.29: TX spectral mask improvement due to raised cosine filtering of the local oscillator signal.

receive side. To simplify things we assume TX is sending out data at a fixed frequency and RX is hopping around and we look at how much power ends up in the receiver. The test bench for when TX and RX are in the same channel is shown in Fig.3.30.

Fig. 3.31 shows the blue and red signals of Fig. 3.30. The blue line is the TX signal and the red line is received signal after the low pass filtering is performed. Fig. 3.31 shows the received signal for two cases where data's are represented by box signals with amplitudes of +1 or -1. In this simulation the LPF has a BW of 50MHz. Number of channels are 10 and each channel has the same probability of occurring i.e. 0.1. The hop rate is set to 50MHops/s which means that dwell time is 20ns.

Now assume setup of Fig. 3.32. In this figure the TX and RX are not the same but spaced by Δf. Fig. 3.33 shows the results for $\Delta f = 1, 2, 10$. We choose these numbers

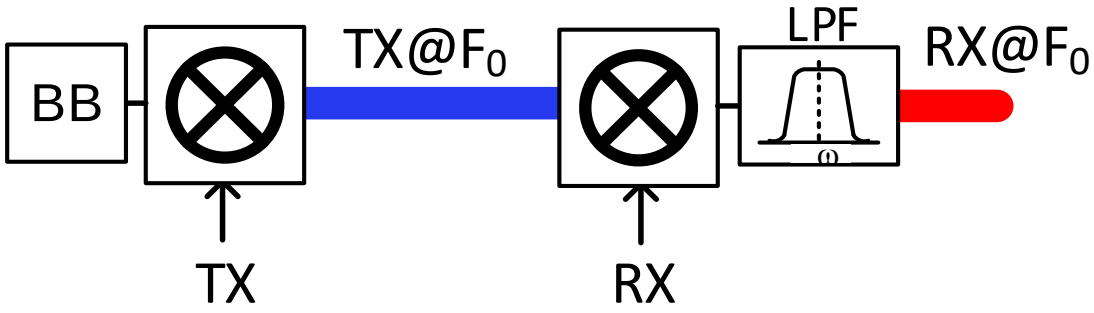


Figure 3.30: Test bench for residual self interference simulation. RX and TX occupy the same channel.

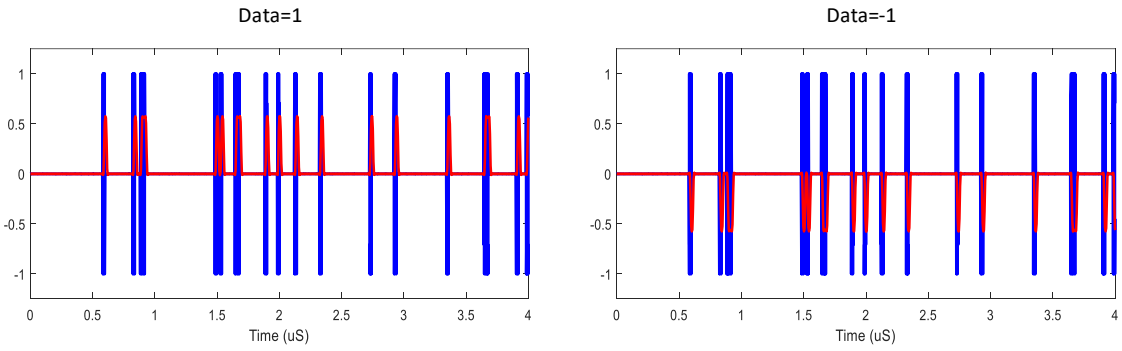


Figure 3.31: Blue: transmitter and Red: receiver output signals. Transmitter and receiver occupy the same channel.

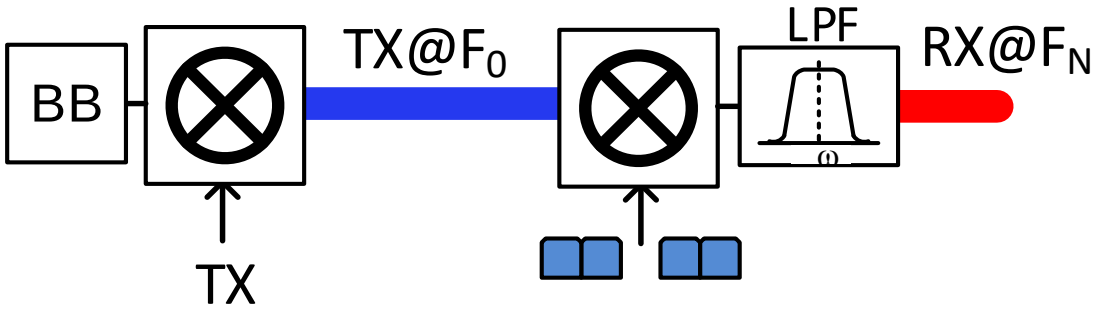


Figure 3.32: Test bench for residual self interference simulation. RX and TX occupy different channels.

for visual clarity. The green line shows the envelope of the received signal which has a frequency of $|f_{TX} - f_{RX}|$. All the channels are orthogonal other than the 0 because the TX transmits at this channel in our setup. The baseband integrated these red impulses for all 10 channels in this simulation. In our system number of channels are 100. We expanded this simulation to find out the residual self interference in our design.

Fig. 3.34 shows the sampled and held (SH) output of the receiver with 100 channels and it's associated histogram. The moving average of the sampled and held signal at the receiver output is shown in Fig. 3.35 . The averaging is done for 100 channels. Fig. 3.36 shows the averaging filter response and the histogram of the channels that RX has visited during this simulation. The averaging filter response is shown in 3.10.

$$H(z) = \frac{1}{N}\left(\frac{1 - z^{-N}}{1 - z^{-1}}\right) \tag{3.10}$$

The total power reduction, i.e. the SIC, for $\Delta f = 10 and 30$ equals 28dB and 34

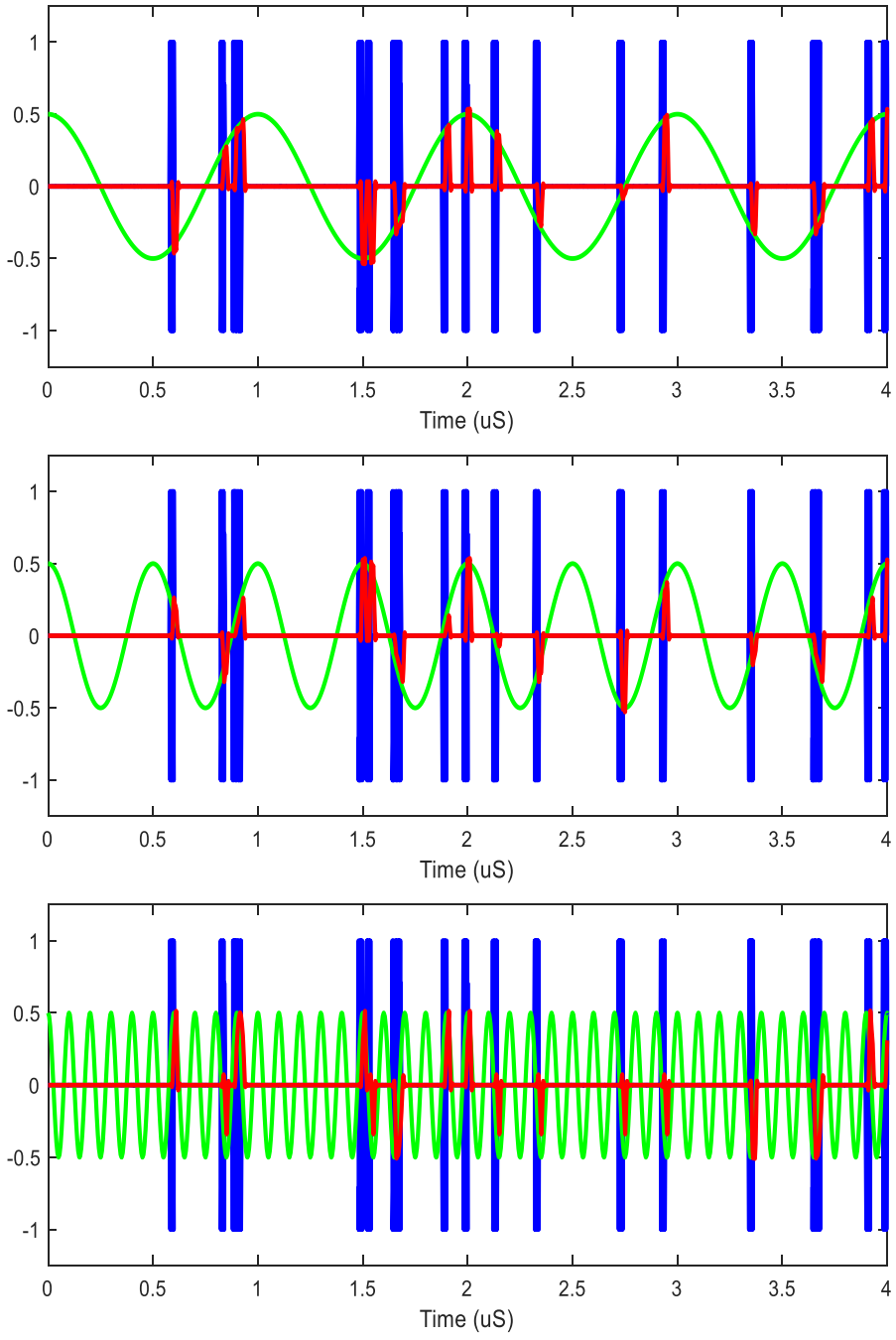


Figure 3.33: Blue: transmitter and Red: receiver output Green: envelope of the received signals. Transmitter and receiver occupy different channel. Spacing is at least Δf channels

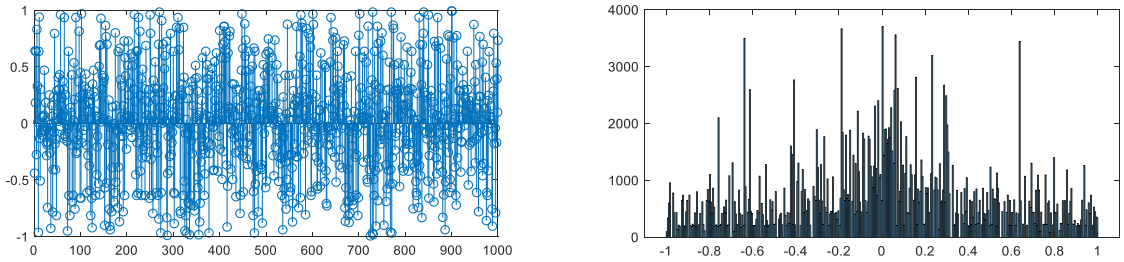


Figure 3.34: sampled and held (SH) output of the receiver with 100 channels and it's associated histogram.

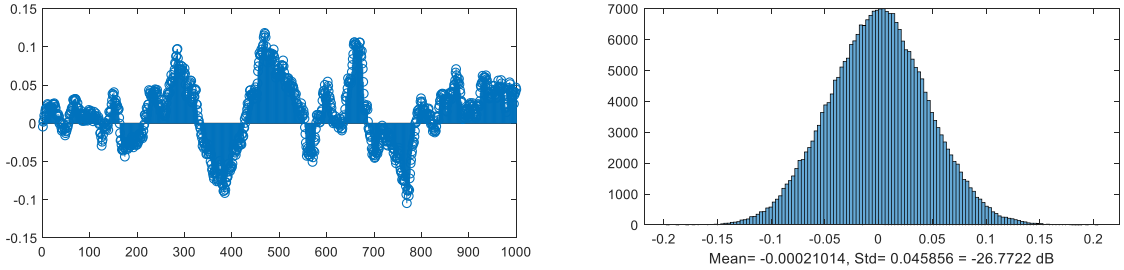


Figure 3.35: Sampled and held (SH) output of the receiver with 100 channels and it's associated histogram with averaging.

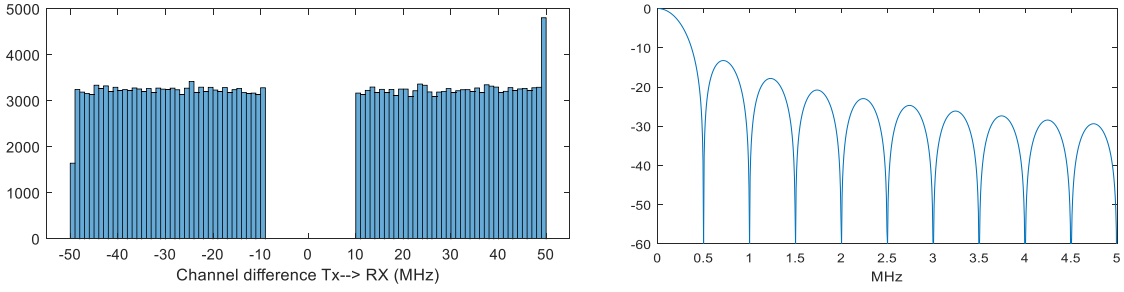


Figure 3.36: averaging filter response and the histogram of the channels that RX has visited during the simulation.

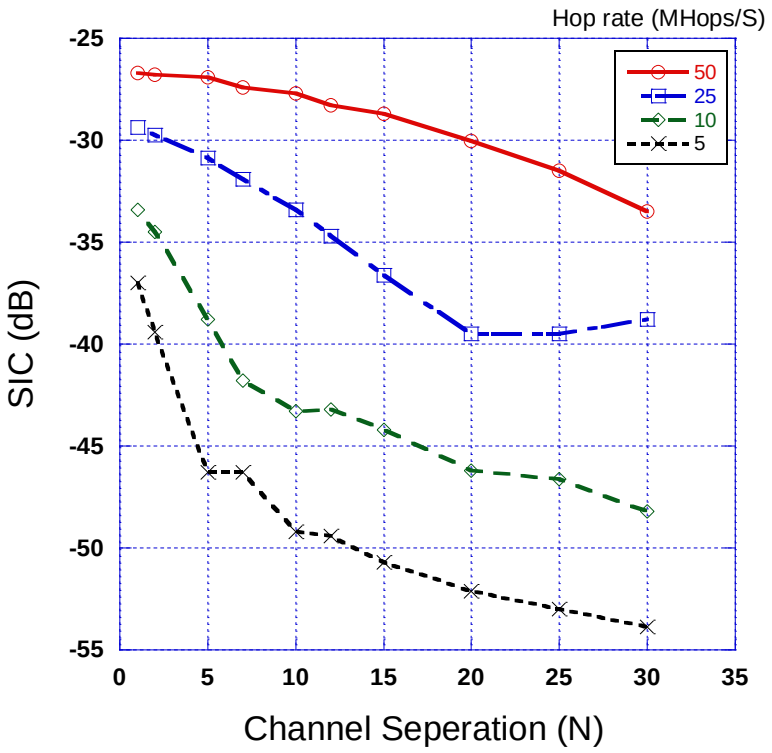


Figure 3.37: Self interference at the receiver output.

dB. These are very close to our measured results that are presented in measurement chapter. The self interference that shows up at receiver output is proportional to the channel spacing, Δf, and hopping speed as shown in Fig.3.37. The dependence of self interference to hopping speed can be understood using Fig.3.38. The higher hopping speed translates into larger main lobe and hence causes more self-interference.

3.1.17 CONOPS

The CONOPS for the overall transmit and receive system is system is shown in 3.39. The maximum power at the antenna is assumed to be +30dBm. Assume TX and RX

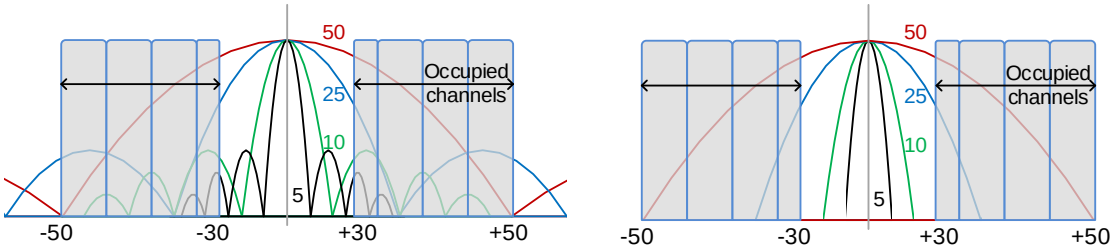


Figure 3.38: The since function due to hopping and main lobs for different hopping speeds.

antenna gains of 0dBm and a NLOS path loss exponent of 3 the maximum distance of operation is 0.68km. The LOS link margin for this distance is 42dB. The antenna is following by 60MHz band-select filter centered at 1GHz that severely limits all out-of-band signals. So, the proposal will only focus on in-band jammer. The performance of the system to single-tone, multi-tone and barrage jammers are discussed later. In addition to the external in-band jammer there is also self-interference from the transmitter that is attenuated by the circulator by 25dB such that a +8dBm in-band self-interference signal is seen receiver during full duplex operation.

3.2 Timing Synchronization

Symbol timing synchronization at the receiver is needed for proper alignment of hopping patterns. We propose a synchronization algorithm based on a specifically designed preamble consisting of chirp modulated symbols as depicted in Fig. 3.40. Let T_{sym} be the symbol duration of the BPSK symbol as well as the duration of the chirp symbols.

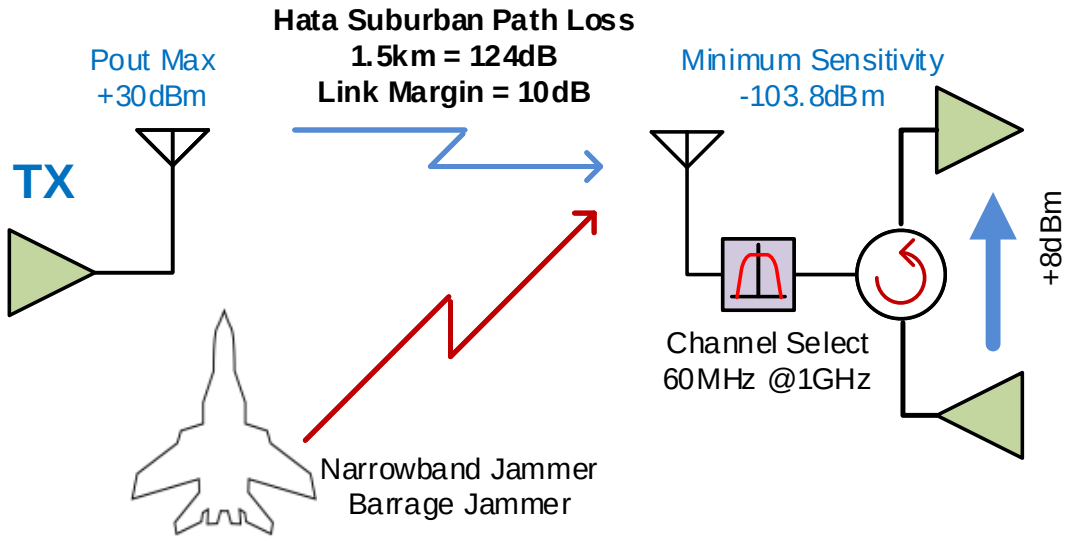


Figure 3.39: CONOPS with jamming scenario.

The instantaneous frequency of the linear chirp at the time t is given as

$$f(t) = f_0 + (t - t_0)R, t_0 < t < t_0 + T_{sym} \tag{3.11}$$

where, R is the chirp rate in Hz per sec and f_0 is the starting frequency of the chirp. The receiver will be measuring the power in the received signal through the bandpass filter centered at f_1 and comparing it with a given threshold. During the preamble phase, the output of the comparator will toggle from 0 to 1 and back to 0 at time instance $t = T_1$. The start time of the symbol T_0 can be estimated from the following relationship $T_0 + 2T_{sym} = T_1 - \frac{f_1 - f_0}{R} + 2T_{sym}$. In order to ensure that the output the comparator triggers for only one time instant the chirp rate $R = \frac{f_u - f_0}{T_{sym}}$ is selected such that $RT_s > B$, where T_S is the ADC sampling rate and B is the channel bandwidth. Now, this scheme will fail if a jammer is occupying channel f_1, in which case the output

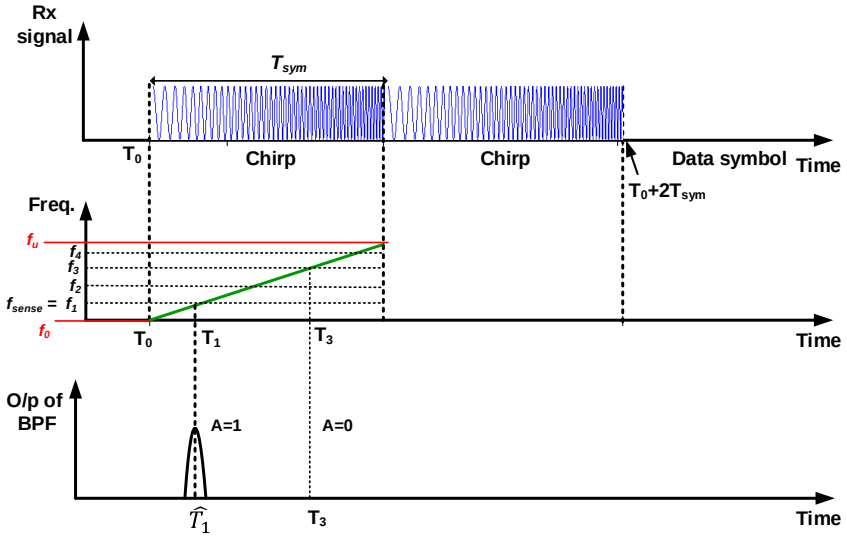


Figure 3.40: Chirp symbols for timing synchronization.

of the comparator will remain 1 over the entire T_{sym}. This will also indicate that a jammer is occupying channel f_1. To overcome this problem, the bandpass filter will be tuned to another f_k during the second symbol duration. Similarly, the start time of the data symbol can then be estimated using the time instant T_k at which the frequency f_k is detected, as follows $T_0 + 2T_{sym} = T_k - \frac{f_k - f_0}{R} + T_{sym}$.

3.3 Circuit Level Design

Next, we provide the circuit details for the above-discussed system blocks. In particular, we provide circuit details and simulations to validate our design selections for the correlators, the self-interference cancellation circuit, and the LO.

3.3.1 Transmit and Receive Correlators

The correlators are implemented as a set of four-phase passive mixers with 25% duty cycle clocks, which is shown in Fig. 3.41. The correlator design is essentially identical to an N -path structure except that the input and output mixers are operated at different frequencies. In an N -Path filter, both mixers are operated at the same frequency, and usually, one is removed from the design for improved noise performance. Here, we maintain the dual-mixer format for flexibly and for improved out-of-band performance [18]. For the transmitter, the input mixers are connected to a fixed-frequency LO, and the other one is driven by an ultra-fast FH LO. The input data are down-converted to baseband from a fixed RF center frequency and up-converted back to RF using the fast-hopping LO signal. The same circuit is used for the receiver with opposite directions. When synchronized, the receive correlator down-converts the received hopping signal on the baseband capacitors. The received signal is then up-converted to a fixed frequency and further processed by a COTS receiver. The switches are implemented using 1 V RF nMOS devices, and they have 3Ω series resistance when they are ON. The baseband capacitors are implemented using only MIM capacitors so that the linearity is only limited by the nMOS switches. The 25% duty cycle clocks are generated using a divide-by-two flip-flop loop and standard logic operations [18].

The correlator is an RF bandpass filter that changes the center frequency according to the LO signal. Hence, if two tones exist in-band, they will generate an third order intermodulation product (IM3) products that may fall in-channel. The low-frequency

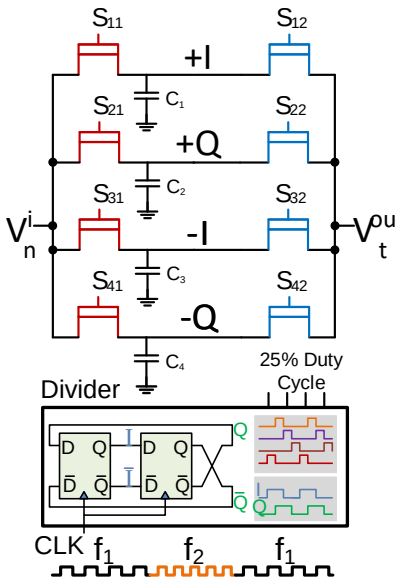


Figure 3.41: (a) Structure of the digital oscillator with an additive quantization noise model. (b) DO output with continuous phase between frequency jumps.

LTI model for N -path filters was presented and validated in [34]. We use this same model plus insight from [35] to develop an analytical model to evaluate the ratio between in-band third order intercept point (IIP3) and out-of-band IIP3 for our design. The simplified circuit model of a top-plate switch circuit is shown in Fig. 3.42 (top). The large jammer causes VGS of the switch to vary [35]. As the frequency moves away from the channel center, the capacitor becomes more of a short reducing the signal amplitude of the jammers.

In our system, our channel hops but the jammers are assumed to be stationary. However, for a simpler analysis, we assume that our channel is stationary and the jammers hop. In our case, we have a total of 100 channels but only certain combinations of two

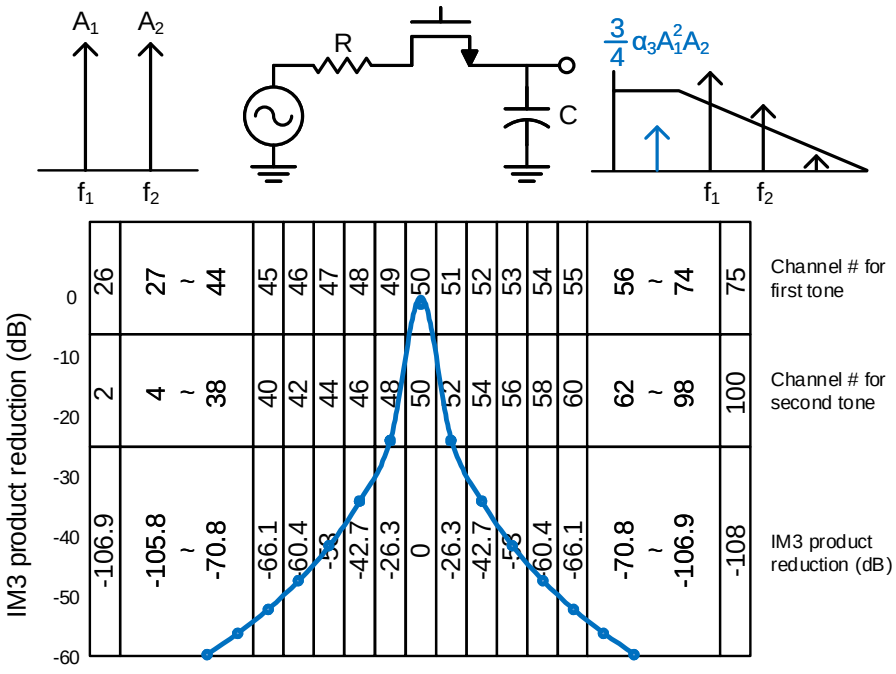


Figure 3.42: Out-of-band IM3 product reduction due to baseband filter response.

tones fall in-band. The cases for which the IM3 products falls in the channel are shown in Fig. 3.42. The first row shows the channel number in which the first tone exists. The second row shows the second tone channel that results in an IM3 product, which falls in-channel. The suppression of the IM3 product due to the baseband filtering is shown in the third row. The IIP3 improvement compared with the in-band IIP3 is the average value of all the suppression values for the other 99 channels. This results in a 20.1 dB IIP3 improvement for output-of-band IIP3 in comparison with in-band IIP3. The calculations provided here are in reasonable agreement with the previously published results [35].

3.3.2 N-Path Filter Capabilities and Limitations

Clock programmable high-Q RF BPF's have been demonstrated on silicon [Ghaf11, Andr10, Darv13] utilizing an N-path filter architecture that had previously been reported as early as 1960 [Fran60]. Npath filters realize the high-Q BPF by taking a low-pass impedance and transferring it to high frequencies. The BPF has twice as much BW as the low-pass counterpart due to negative and positive frequencies. The center frequency of this filter is decided by the clock frequency. This property makes these N-path based high-Q filters extremely flexible. They can be moved easily in the frequency domain by changing the switching frequency of their master clock. Since these N-path filters are made of passive switches and capacitors they can be extremely linear. The maximum linearity is primarily decided by the signal and clock amplitudes. The noise performance of this circuit is also fairly reasonable and passive mixer first receiver frontends with 2.5 dB NF have been demonstrated using the N-path filter as a downconverter [Andr10, Wu15, Nejd15, Lin15].

Fig. 3.43 shows the structure of a 4-path filter with triple well transistor and the associated voltage levels at the input and at the switch transistor gates. At any given time only one of the four paths are active as shown in the figure (only the bottom path is active). The maximum signal swing at the input of the filter is limited by the voltage at the gate of the switches, i.e., VDD+VB. For linear operation, the off switches must stay off and the on switches must stay on during the full period of the input signal. The maximum positive swing at the input can be determined by considering the

input voltage when the transistor just turns off: Vin,max=V+=VDD+VB-VTH, where VB is the DC offset voltage so as to accommodate the negative swing of the signal. Therefore, the maximum positive signal swing is given by ΔV+= V+-VB=VDD-VTH. Likewise when the input reaches its minimum it puts the off transistors at the edge of turning on: Vin,min=V-=-Vth. For the swing to be maximized symmetrically, positive and negative swings must be equal: ΔV- =ΔV+=VDD-VTH and VB=-VTH+VDD-VTH=VDD-2VTH. This means that the maximum input signal amplitude can be as large as VDD-VTH, where we define VDD here as the maximum drain-to-gate voltages tolerated by the transistors. From this simple approximation the maximum power that the circuit can handle without causing significant nonlinearity is given by Eqn 4.

$$P_{in,max} = 10.log_{10}[(V_{DD} - V_{TH})^2/(2Rs)] \tag{3.12}$$

Circuit simulations have been used to verify that this constraint is fairly accurate and only underestimates the linearity limit by about a dB. However, its simplicity allows us to evaluate the tradeoff between the supply voltage and signal linearity. If the input power increases beyond this point, the output power will not increase since the switch will turn off. This means that if the power increases 1dB beyond this maximum, the output power will not increase. In this manner we can estimate both the P-1dB and IIP3 as: P-1dB=Pin,max+1dB, IIP3=10+P-1dB. From this the maximum power handling of the N-Path filter utilizing different transistors is summarized in Table. 3.3. As Table. 3.3 suggests a 2.5V NMOS transistor will able to provide the required 25dBm of IIP3 provided

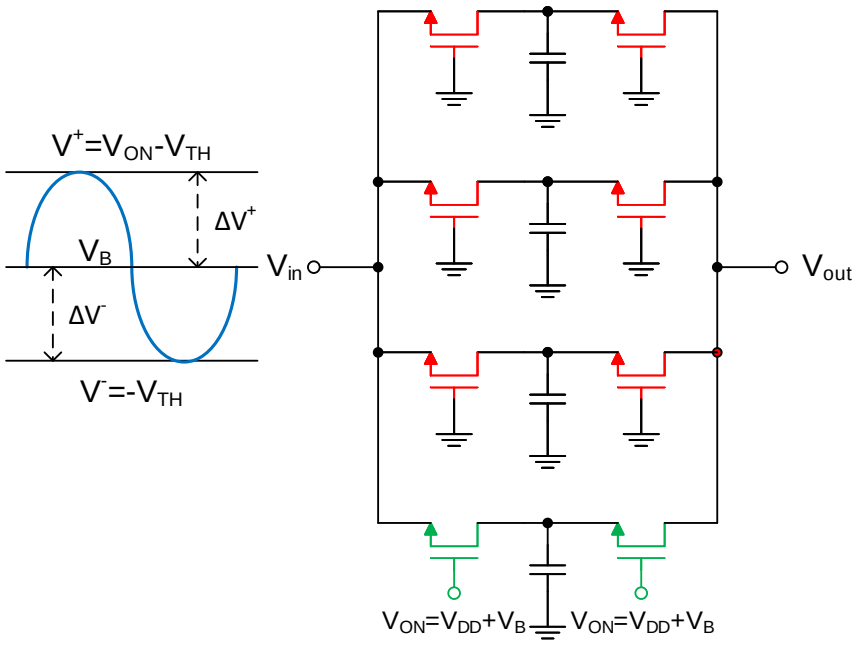


Figure 3.43: Evaluating the maximum signal amplitude for a 4-Path high-Q RF BPF.

that we are able to bias the gate voltage with a maximum clock voltage of 4.2V. In the case of 65nm CMOS technology the maximum gate to drain voltage to drive the switches can be as large as 3.5V which translates to an IIP3 of +24dBm (VGS=2.5,VB=3.5-VGS=1,ΔV-=VB+VTH=1.4V,ΔV+=VGS-VTH=2.1). Not surprisingly, as we will also see in Section 7, we are going to tradeoff between linearity, NF and power dissipation. We are currently evaluating other technologies including 40nm bulk, and 32nm SOI that are likely to provide better NF, power tradeoffs.

Measured in-band IIP3s exceeding +22dBm [Luo15] and measured out-of-band IIP3 of +29dBm has been demonstrated [Luo15, Liu16]. Out-of-band suppression of more than and 53dB has also been reported [Thom14, Darv13]. Higher order IIR filters provide

Table 3.3: N-Path power handling ability

Technology V_{DD}	P_{-1dB}	IIP3	V_{ON}
1	6.6	16.5	2
1.8	13.9	23.9	2.8
2.5	17.4	27.4	4.2
3.3	20.2	30.2	5.8

sharper transitions but result in degraded NFs [Tohi14]. Our simulations suggest that in-band IIP3 exceeding +30dBm should be possible.

Fig. 3.44 shows the simulated N-path filter behavior for a 4-path circuit. The orange graph shows the signal behavior when looking at one port only. This is how the design is normally used in many circuits. We see that the out of channel suppression levels off at about -15dB. The blue graph shows the two port behavior where the signal is applied on port 1 and the output is seen at port two. We note that the out-of-channel suppression continues to about 70dB and this is the mode that we are using the device. The noise figure is slightly higher in this mode due to the two series transistors. We have made the tradeoff of linearity over NF while still meeting the requirements for the project.

3.3.3 Self-Interference Canceller Circuit

Due to high PA power, the self-interference canceller circuit needs to be very linear suggesting a passive structure. The circuit should also have minimal impact on the noise

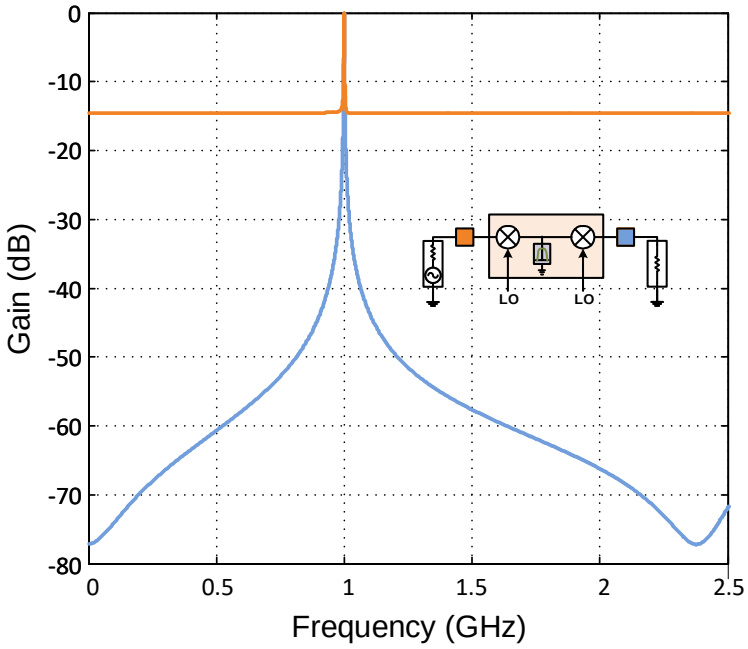


Figure 3.44: Simulated N-path behavior, 1-port performance vs 2-port performance.

figure (NF) of the receiver. As shown in Fig. 3.41(b), the circuit is implemented using resistors, capacitors, and switches and is similar to the design in [24]. The design in [24] uses an R-2R and C-2C ladder networks. We use binary resister and capacitor ratios. Both designs start with the NF consideration first. It can be shown that a 200 Ohm resistor only degrades the NF by 0.5 dB when the receiver NF is 1 dB. This means that the smallest combination of the resistors in the circuit needs to be larger than 200 Ohm . The capacitors are then sized accordingly. The switches are located on the receive side where cancellation occurs, as they do not see large voltage swings. The circuit does not consume any DC power. Dynamic power is small due to slow reconfiguration speed which, at maximum, only operates at the hop rate.

3.3.4 Ultra-Fast Hopping Signal Generator

The overall circuit design for LO generation is shown in Fig. 3.45, and the DO architecture has been discussed earlier. Next, we consider the impact of DAC resolution on the overall LO phase noise. The current-mode DAC puts out a finite resolution sample-and-hold analog value. Ideally, the finite quantization contributes broadband additive noise but does not directly cause phase noise. However, the broadband quantization at the DAC output can get converted to phase noise due to finite rise and fall times and due to the AM-to-PM conversion of the buffer or ILO that follows the DAC. To evaluate this contribution, we used the same test setup as the DO quantization but with varying DAC resolution. This simulation was done in Cadence using PNOISE where an equivalently shaped Gaussian noise model substitute was used for quantization noise to achieve convergence. The authors are aware that the probability density function of the two noise sources (quantization versus Gaussian) are different but the expected values and frequencies were appropriately adjusted and we expect that this should provide a good approximation. If we assume that the input clock is ideal and that the digital part of the DO generates no phase noise, then the phase noise contribution due to the AM-to-PM conversion of the 8 bit DAC alone at a 1 MHz offset is -136 dBc/Hz. Actual phase noise measurements will be a function of the phase noise from the source, the computational accuracy, and the contributions from the DAC AM-to-PM.

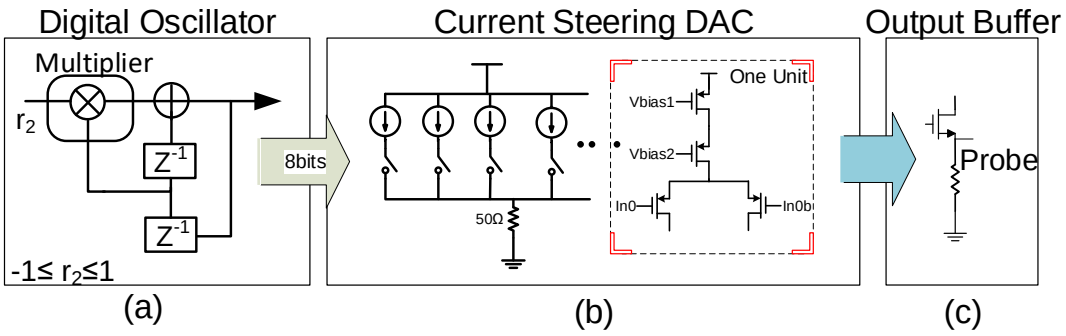
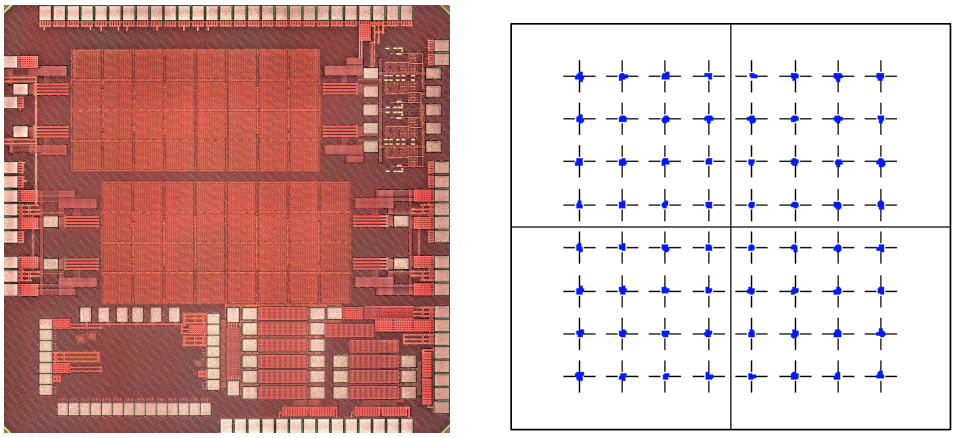


Figure 3.45: (a) DO structure. (b) Current-mode 8 bit DAC. (c) Buffer included for testing purposes only.

Chapter 4

Ultra Fast Frequency Hopping Transceiver Measurement Results



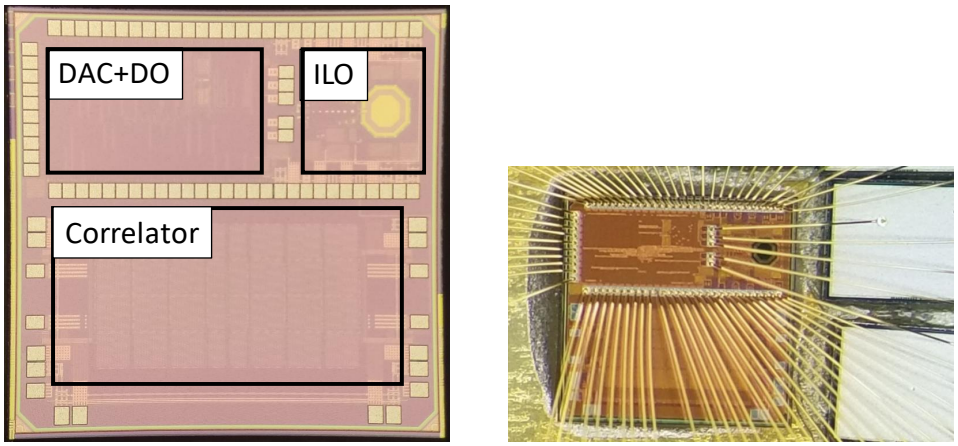
(a) (b)

Figure 4.1: (a) Chip microphotograph (b) Received 64QAM signal

The design was fabricated in the TSMC's 65 nm RF-GP CMOS technology. The active area is 3.1 mm2. The microphotograph of the fabricated chip is shown in Fig. 4.1a. There have been other versions of this Chip. The 3rd Generation Chip is also shown in Fig. 4.2a. The bonded version of the 3rd generation chip is shown in Fig. 4.2b. Next, we present measurement results for the various components of the system, i.e., the correlators, the DO, and the DAC. This set of measurements is followed by more system-level measurements, including TX to RX intended signal, TX to RX self-interference, and narrow-band jammer rejection.

4.1 Component-Level Measurements

First, we provide measurements for the fast-hopping critical components, including the correlator.



(a) (b)

Figure 4.2: (a) Latest version of the Chip (b) Bonded version of the latest version Chip

4.1.1 Correlator Measurements

Correlator gain is shown in Fig. 4.3 versus input frequency. The insertion loss of 4dB is achieved. The setup used in the measurement is also included in the plot. The measured IIP3 is shown in Fig. 4.4. Two wones at offsets of 2 and 3MHz are fed to the correlator and the output tone and IM3 products are measured and shown. The measured in-band IIP3 is +18dBm. This is in agreement with the calculation provided in Table. 3.3.

We attempted to improve the linearity by biasing the RF port using an RF Bias-T. Biasing the RF port should increase the linearity since it reverse biases the off transistors and S/D diodes. Reverse biasing the diodes reduces their parasitic capacitance by increasing the junction depletion region. The result is shown in Fig. 4.5 for in-band IIP3. The V_{DD} is also increased with the bias voltage to keep the V_{GS} of the on transistors constant. These figures show that IIP3 can is improved around 6dB by proper biasing

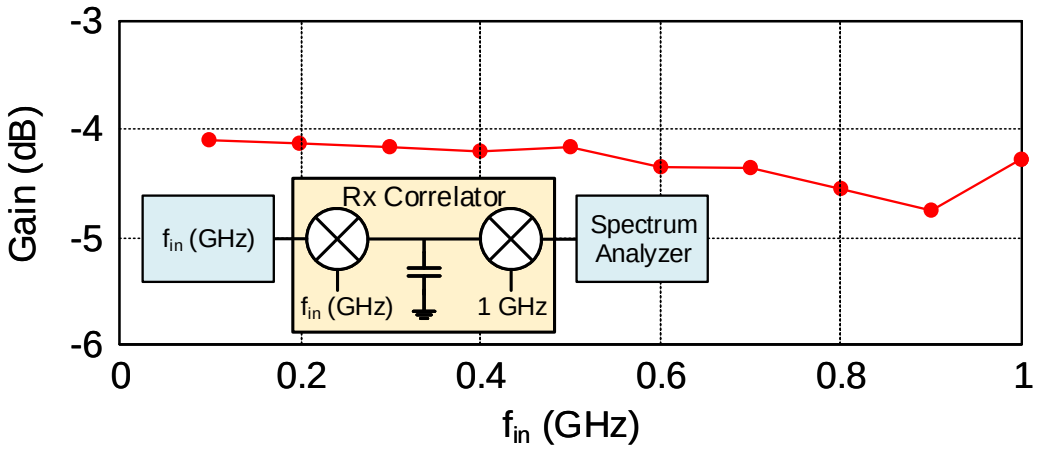


Figure 4.3: Measured correlator gain versus input frequency.

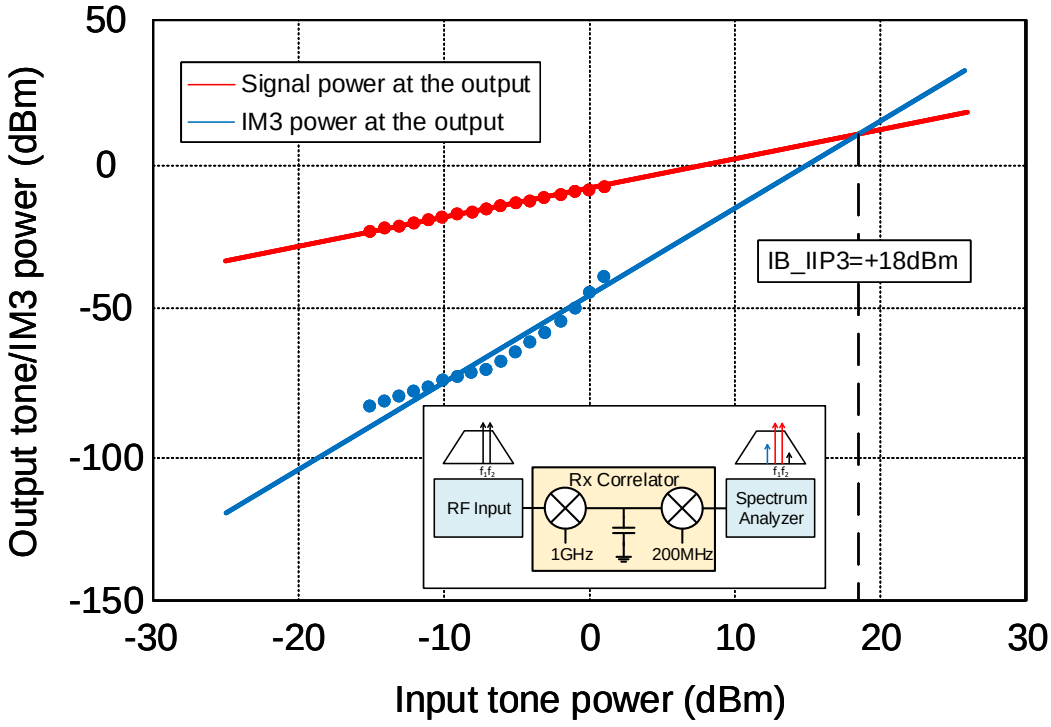


Figure 4.4: Measured correlator gain versus input frequency.

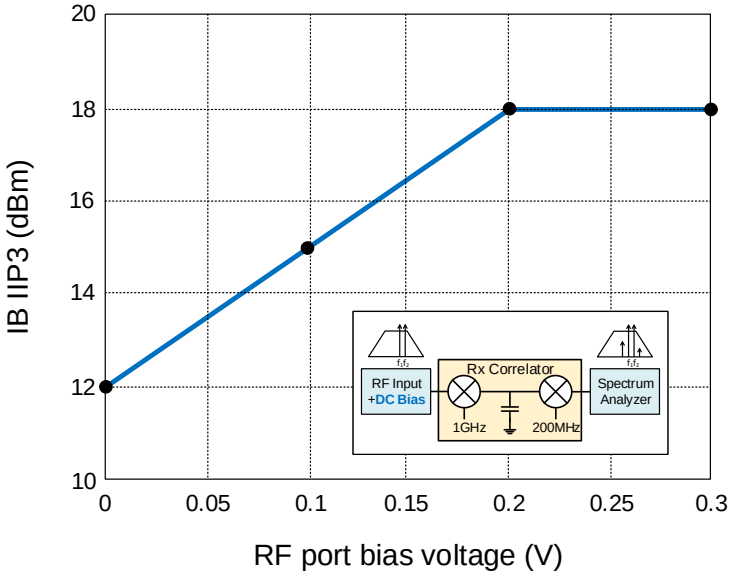


Figure 4.5: In-band IIP3 of the correlator versus the input RF bias voltage.

of the RF port. The setup shown to measure IIP3 is included inside of the plot. We however observed that increasing the V_{DD} did not increase the IIP3 and the only way to increase IIP3 was to increase the bias voltage in our measurements.

The out-of band IIP3 versus the frequency offset from the center is plotted in Fig. 4.6. The out of band IIP3 can be as high around 20dBm. Correlator power consumption is shown in Fig. 4.7. The power consumption is 22mW at 1GHz RF frequency.

Fig. 4.8a shows a spectrogram of the transmit correlator while hopping between two frequencies centered at 1 GHz. For this and the next measurement, the LO signal that drives the output mixers of the transmit correlator is hopped, and the output of the correlator is measured using a 20 GSa/s R&S oscilloscope. Due to IF bandwidth limitations of our spectrum analyzer, transient response measurements are performed by

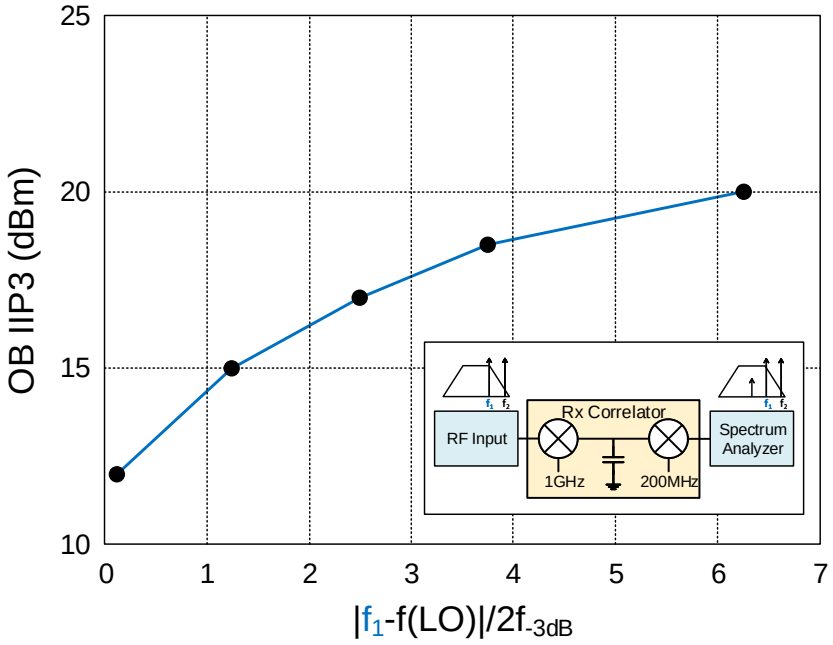


Figure 4.6: Out-of band IIP3 of the correlator versus the frequency offset.

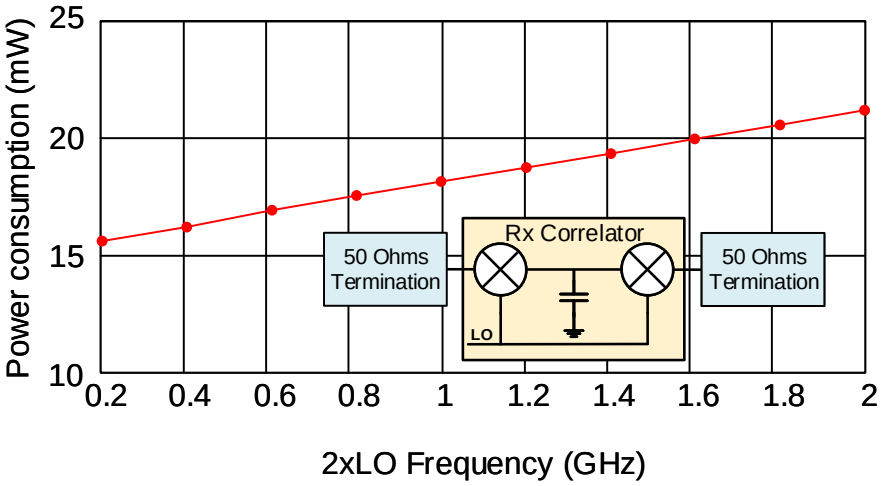
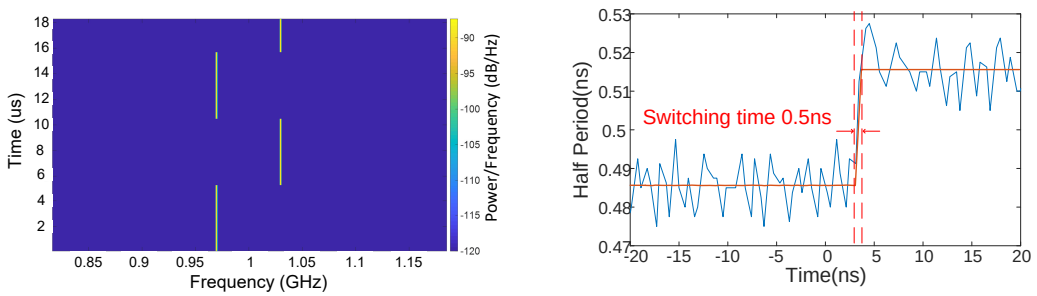


Figure 4.7: Correlator power consumption.



(a) (b)

Figure 4.8: (a) Frequency hopping spectrogram used to measure the transient response of correlator (b) Measured TX correlator transient response. Only two hopping frequencies are shown here to ease transient response behaviour.

using the time-domain sampled values of the output using a digital oscilloscope. The data are then taken to MATLAB, interpolated and filtered, and a spectrogram performed on the output. As can be seen, we clearly see the hopping pattern but it is difficult to measure the exact transient response time using the spectrogram.

To better evaluate the transient response, we estimate the instantaneous frequency by looking at the zero crossings of the time-domain signal. Fig. 4.8b shows the transient response of the transmit correlator to an abrupt frequency change in the LO signal. The time resolution using the zero-crossings method is limited to one half period, i.e., 0.5 ns when the output is centered at 1 GHz. The blue line shows the measured signal. The orange line shows the average of 200 data points. The perturbations in the measurement are due to the finite oversampling (≈ 2) and the practical limitations of the interpolation. The measured settling time is 0.5 ns, which means that the correlator output frequency

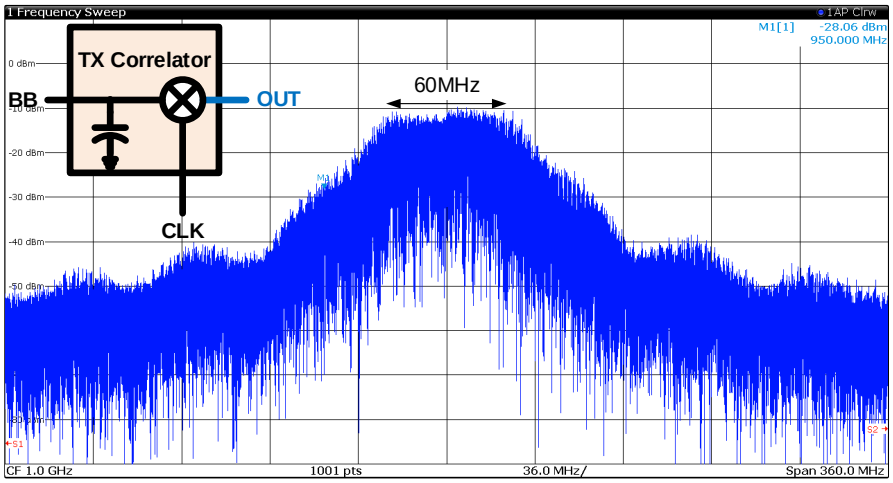


Figure 4.9: Transmit correlator output spectrum for random FH LO.

settles in less than 0.5 ns. This shows that the correlator is able to hop nearly instantly and the settling time is only limited to the fast-hopping LO that drives the correlator.

Fig. 4.9 shows the transmit output spectrum on a spectrum analyzer centered at 1 GHz. For this measurement, a dc input value was provided at the baseband for a fixed LO. The LO was then hopped randomly across all 100 channels to occupy a bandwidth of 60 MHz. Due to the divide-by-two circuit in the N -path LO generator, the external LO input was centered at 2 GHz and was hopped randomly to cover 120 MHz. In Fig. 4.9, we see the spreading of the single sinusoidal spread across the 100 channels providing 20 dB of processing gain.

4.1.2 SIC Measurement

The normalized measured constellation points for one arm of the SIC circuit is shown in Fig .4.10. The measurement is done using only 2 most significant bits for the R and C

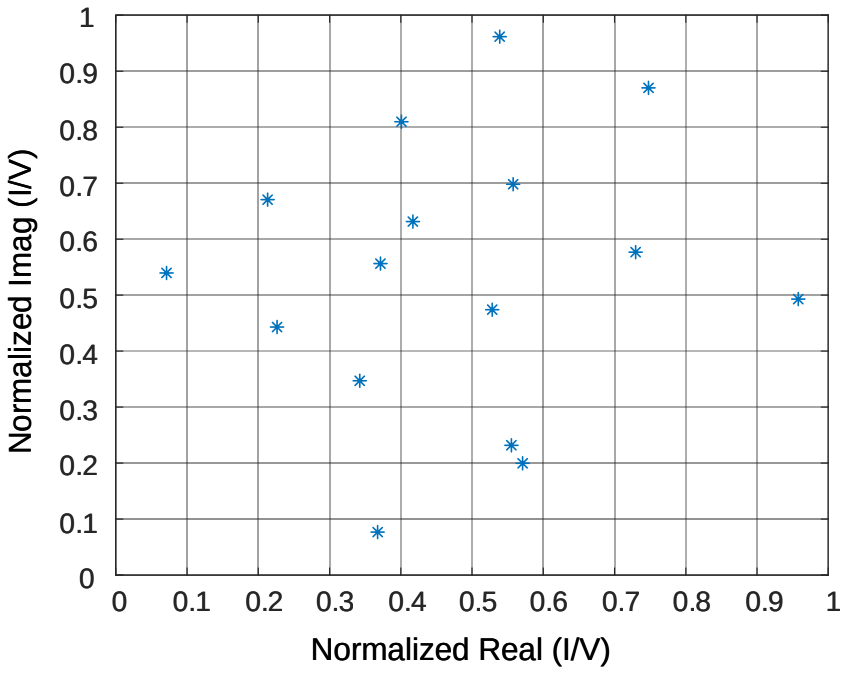


Figure 4.10: Measured SIC Transconductance for the 2 most significant bits of R and C.

banks that resulted in 16 points. The constellation shows the transconductance of the SIC circuit.

4.2 System-Level Measurements

Now, we provide system-level measurements. In particular, we provide TX to RX intended signal performance, TX to RX self-interference rejection, and in-band jammer rejection.

4.2.1 TX to RX Intended Signal Performance

We use the same measurement setup for normal operation (TX $\rightarrow$ RX) and for jammer rejection. This setup is shown in Fig. 4.11, except that for normal operation, there is no added jammer. We use a signal generator to generate BPSK, QPSK, 16 quadrature amplitude modulation (QAM), and 64 QAM signals centered at 0.5 GHz. This signal goes through the TX correlator, centered at 1 GHz, which spreads the signal by 20 dB. The output of the TX correlator is followed by a 26 dB LNA and a 16 dB attenuator to isolate the TX from the RX. The extra 10 dB of gain compensates for test setup losses so the signal seen at the RX correlator is at -19.5 dBm. The RX correlator is synchronized with the TX correlator. The output of the RX correlator, centered at 0.5 GHz, passes through a 500 MHz bandpass filter with a filter bandwidth of 7 MHz and then demodulates using an R&S FSW 43 spectrum analyzer. The choice of the 0.5 GHz frequency for the fixed TX and RX mixers is due to the availability of the band-pass filter.

The fast-hopping LO is provided by an arbitrary waveform generator (AWG) for two reasons. First, as a mechanism to reduce risk, all the blocks in this chip tapeout were designed to be tested separately. In particular, the signal generator and the correlator were not connected together. Second, due to an error in the source follower buffer after the DAC, the output voltage from the buffer was not sufficiently large to run the correlators. Synchronization between the transmitter and the receiver is also important in the system where the problem gets worse with a wireless channel and mobility. This

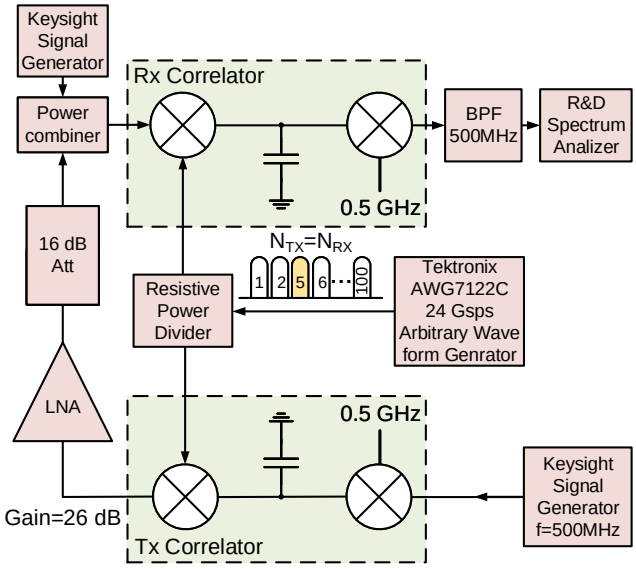


Figure 4.11: Measurement setup used for TX → RX intended signal performance and for in-band jammer performance.

problem is likely to be exasperated with the high hopping speed of this design. The details of synchronization for this architecture are still ongoing research. As mentioned earlier, we are driving the correlators with an external AWG. Since we are assuming perfect synchronization, a single AWG is used for both receive and transmit. In a practical system, however, this correlates the phase noise of the TX and RX, which is unlikely to be correlated in a real system. To make sure that the TX and the RX are synchronized, LO paths were designed symmetrically and were connected together on chip. Also the delay between the TX and the RX was minimized using short cables.

For this measurement, no in-band jammer is added. Due to space limitations, only the 64 QAM signal is shown, here, in Fig. 4.1b. The sensitivity measurements for the receive

correlator were performed without hopping. The output of the receive correlator was fed directly to an R&S FSW43 spectrum analyzer with a pre-amp option. External input and output baluns were used. There are two differential mixers in the receive correlator. RF data were provided at 401 MHz with a 1 MHz offset to avoid LO feedthrough. The input and output mixers were operated at 400 MHz. The measured sensitivity after de-embedding for the baluns for QPSK signals at a symbol rate of 470 Ksps (600 KHz occupied bandwidth) was -95 dBm. The measured EVM was 6 dB, and assuming a 9 dB NF for the spectrum analyzer (-165 dBm DANL), the effective noise figure for the receive correlator is about 6 dB.

4.2.2 TX Signal Rejection in RX Channel

The receive and transmit correlators are operated at different channel frequencies at all times to reduce self-interference. However, due to ultra-fast hopping speed of the correlators in this design, some of the transmit signal shows up in the receive band. Fig. 4.12 shows the setup that is used to measure the self-interference cancellation. Fig. 4.13 shows the self-interference cancellation when minimum channel spacing is 30. In this case, the hopping sequence for the receiver is determined randomly using a uniform distribution, and then, another uniformly distributed random function is used to determine the transmitter hopping sequence with the condition that the transmit channel at any given time is at least 30 channels away from the receive channel. In this case, the total measured self-interference cancellation is 28.4 dB. The measured self-interference cancellation is 27.3 dB for ten-channel, 28.4 dB for 30 channel, and 33 dB for 50 channel separations

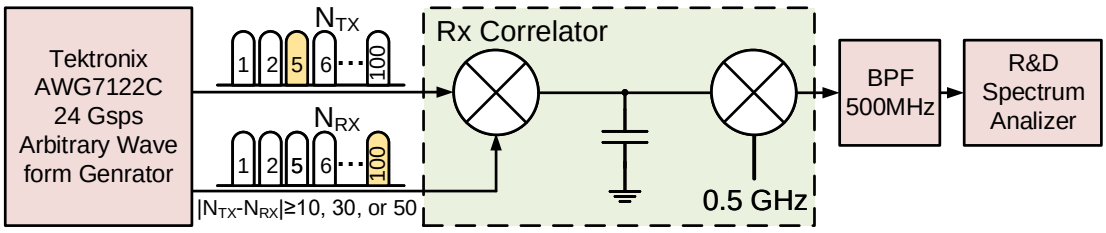


Figure 4.12: Self-interference cancellation measurement setup.

confirming that TX $\rightarrow$ RX isolation improves only slight, as the channel spacing increases due to the sinc function introduced as a result of ultra-fast hopping. We have numerically calculated the rejection in MATLAB for a 10 MHz bandwidth (consistent with our measurements), which shows -27.7, -33.9, and -37.7 dB rejection for 10, 30, and 50 channel separations, respectively. For this simulation, two 500 MHz signals were generated that are hopped with different TX and RX sequences at 50 MHops/s and are multiplied to get the baseband component of the signal. The filter used in this simulation is an ideal low-pass filter. We think that the discrepancy between the simulated and measured results is likely due to a substrate or supply coupling and/or LO feedthrough that causes a leveling-off in the measurement results.

4.3 Jammer Behavior

We use the measurement setup in Fig. 4.11 for this test as well but, except in this case, we add an in-band jammer to mimic the scenario shown in Fig. 4.14. The 20 dB processing gain of the receive correlator can also be seen when a narrow-band blocker exists in the receive band. The measured constellation at the receiver is shown in Figs. 4.15 and 4.16

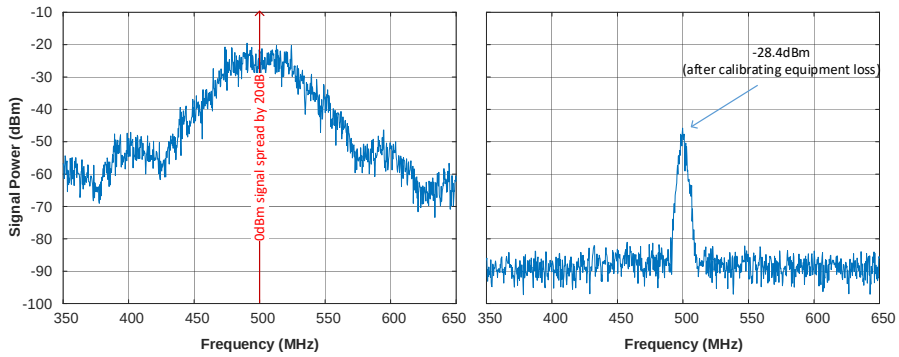


Figure 4.13: Self-interference cancellation due to transceiver orthogonal operation.

versus the in-band blocker power for two cases. The top row shows the constellation versus blocker power when there is no hopping. The bottom row shows the constellation for when the transmitter and the receiver hop with 50 MHop/s. The input signal is at -29 dBm. The EVM with no jammer is at -33.8 and -23 dB, which reduces to -7.8 dB for both cases. The blocker power difference is 19 dB, i.e., processing gain is 19 dB. In this setup, the TX/RX fixed LO is run at 300/500 MHz. This is to avoid influencing the measurements from the substrate and board coupling, which will happen if the TX and the RX have the same frequency. Also the data are fed to the TX at 301 MHz to avoid LO feedthrough and I/Q mismatch.

The EVM versus blocker power is shown in Fig. 4.17 for the two cases where the transmitter and the receiver are both hopping or both not hopping for the same jammer. The measurement setup is the same as in Fig. 15. The only difference is that the LO frequencies in the baseband side of the TX correlator was set to 0.4 GHz for this measurement. The data were fed to the TX correlator at 401 MHz to avoid LO feedthrough

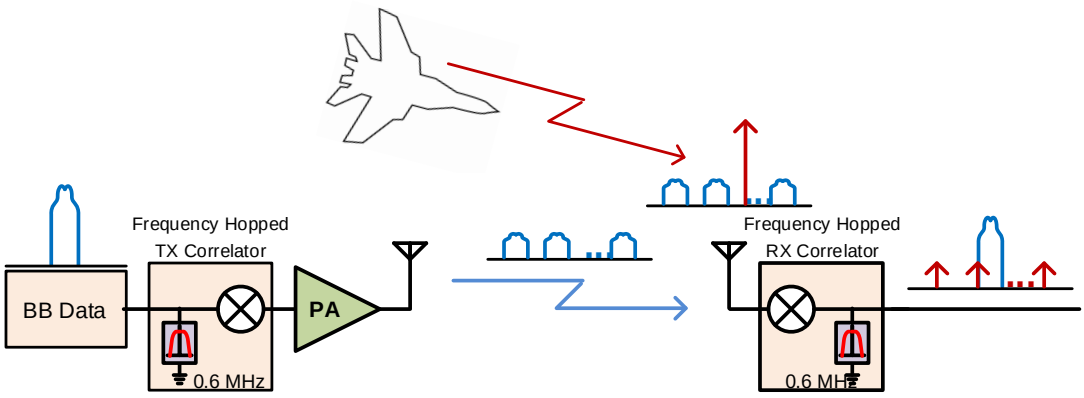


Figure 4.14: Jamming scenario of the FHSS system.

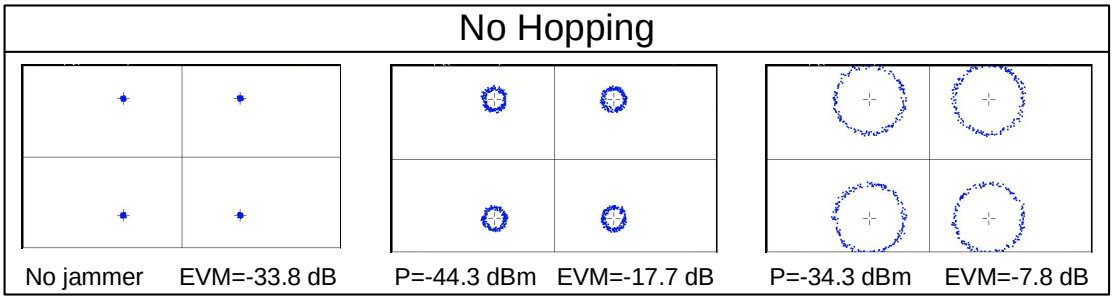


Figure 4.15: Received signal constellation versus in-band blocker power when the RX and the TX are not hopping.

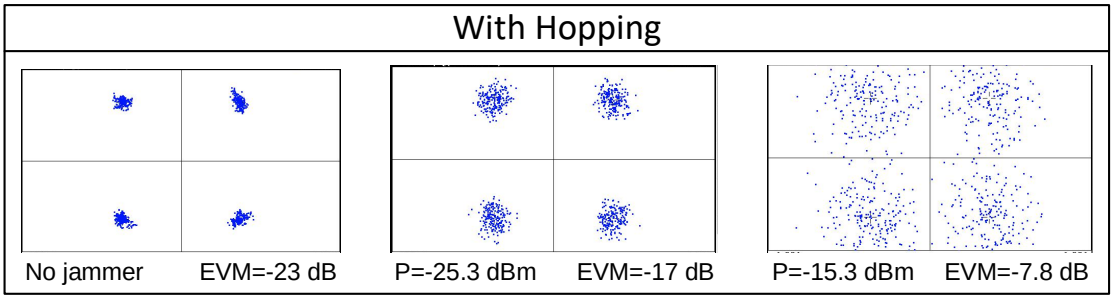


Figure 4.16: Received signal constellation versus in-band blocker power when the RX and the TX are hopping. Note that we have attempted to keep the EVMs between the hopping and not hopping cases. Thus, the difference can be seen in the jammer power levels between hopping and not hopping.

and I/Q mismatch. The red and blue lines show the EVM for hopping and non-hopping cases. As Fig. 20 shows, for the same EVM, blocker handling capability goes up by 19.4 dB. In other words, the blocker is rejected by 19.4 dB. The input power to the receive correlator is set to -29 dBm at each port. We have been also able to measure 20 dB processing gain when the signal is at a 5 MHz offset from the center frequency. The EVM rises linearly with the signal power and can be estimated as EVM=10log(PB/PM) , where PB and PM are the blocker power and the signal power, respectively. The level-off in the red circles in Fig. 20 is due to the limited EVM of the system when there is no blocker present. As was also seen in Figs. 19 and 18, there is an increase in the noise level with hopping. We are still investigating the reasons for this.

The spurs from the DO can also affect the blocker performance. The spurs that are out of band are not problematic since the front-end filter removes any out of band block-

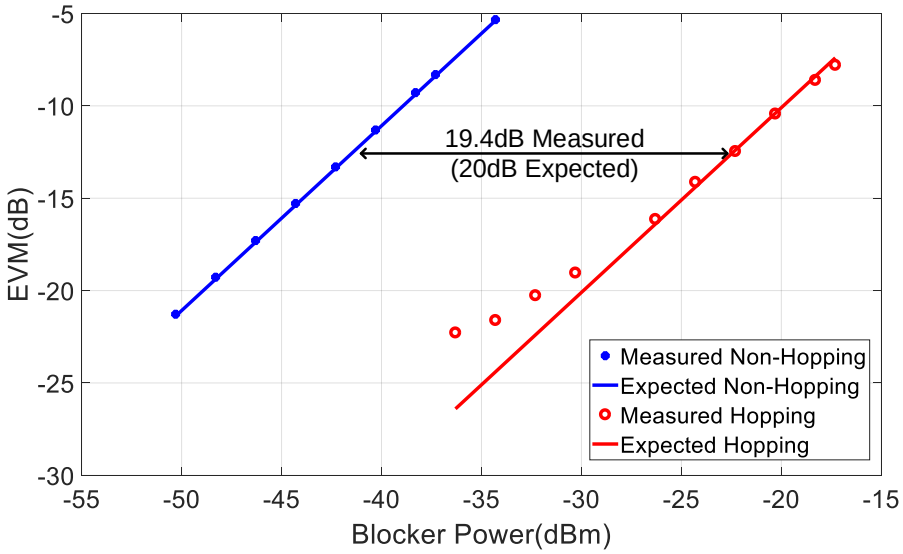


Figure 4.17: EVM versus blocker power with 100 channels for two cases, i.e., hopping and not hopping.

ers. There is, however, a spur that is 50 MHz away and is due to the hopping of the DO at 50 MHops/s. This spur shows up at 25 MHz away from the LO after down-conversion, which would be in-band and is around -65 dB lower than the LO. Since the spur is much smaller than the LO, it does not affect the blocker performance.

We have also measured EVM performance of the system under other blocker types. Fig. 4.18 shows the EVM at the receiver output for a two tone blocker. The RX input signal power is set to -20.8dBm and the nlocker power is varied between -20.8dBm and +0.2dBm. The blocker is 5MHz higher than the center frequency of the receiver which is 1GHz. The data rate was set to 10Kbps for visual clarity. The reported power is in PEP that is roughly 3dB larger than each individual tone. The figure shows that the

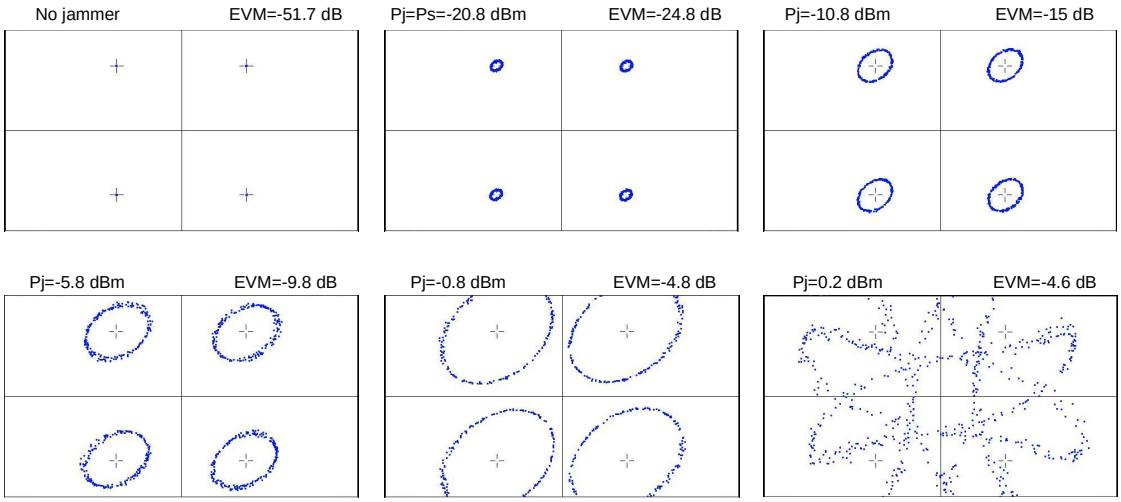


Figure 4.18: EVM vs jammer power at the receiver for a two-tone blocker.

receiver is able to decipher between the symbols even when the blocker is 20dB larger than the signal.

Fig. 4.19 shows the EVM at the receiver when the blocker is a pseudo-random modulated sequence. The RX input power is set to -20.8dBm and the blocker power (PEP) is varied between -20.8dBm to +0.2dBm. The rate of the data in the blocker is set to 470Kbps with a QPSK modulation. Again the receiver is able to receive data even when blocker is 20dB larger than the signal.

Fig. 4.20 shows the EVM jammer power at the receiver when the blocker is a broadband noise. The RX power is set to -20.8dBm and the blocker power is varied from -20.8dBm to -1.8dBm. The noise that is generated by the signal generator and used as the blocker in this measurement is shown in Fig. 4.21.

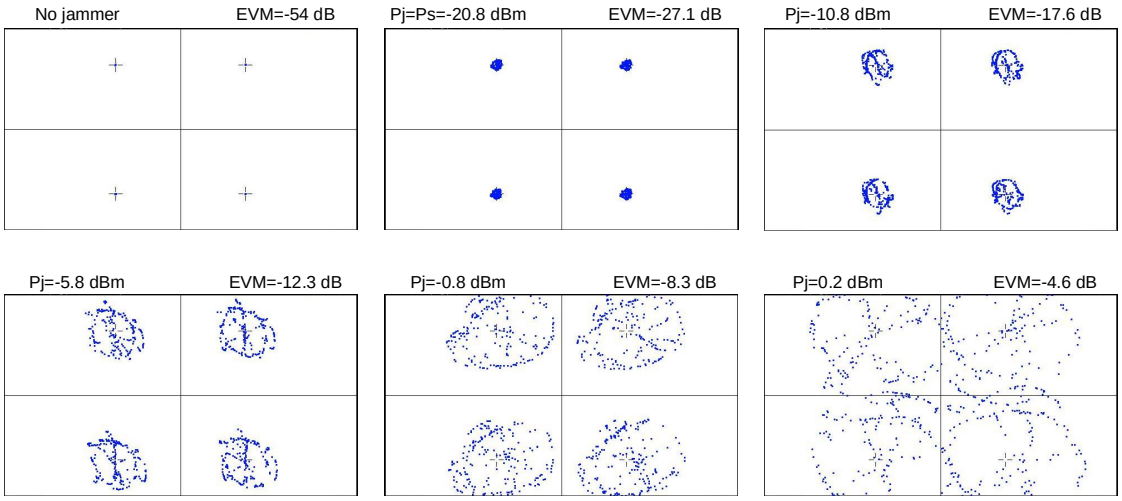


Figure 4.19: EVM vs jammer power at the receiver for a pseudo-random blocker.

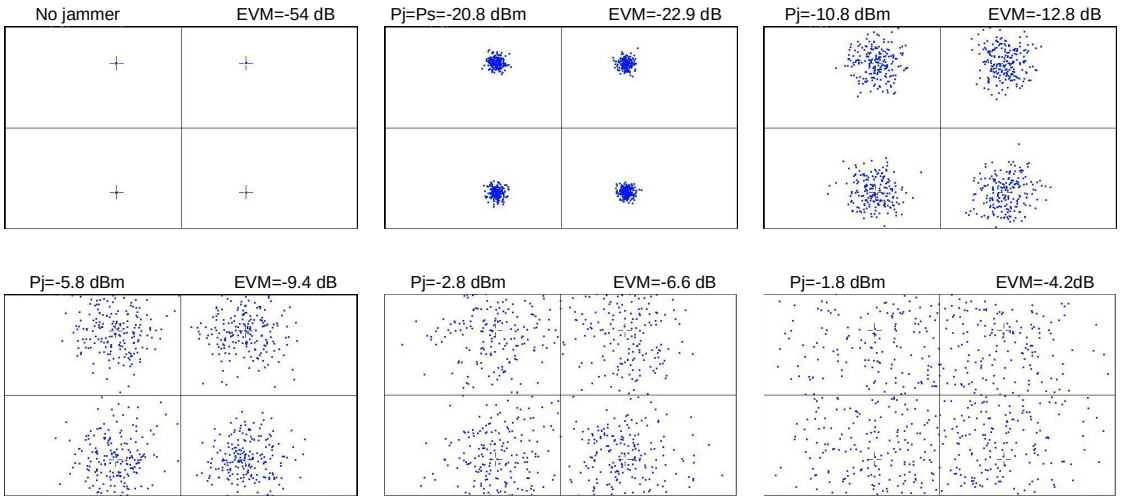


Figure 4.20: EVM vs jammer power at the receiver for a broad-band noise blocker.

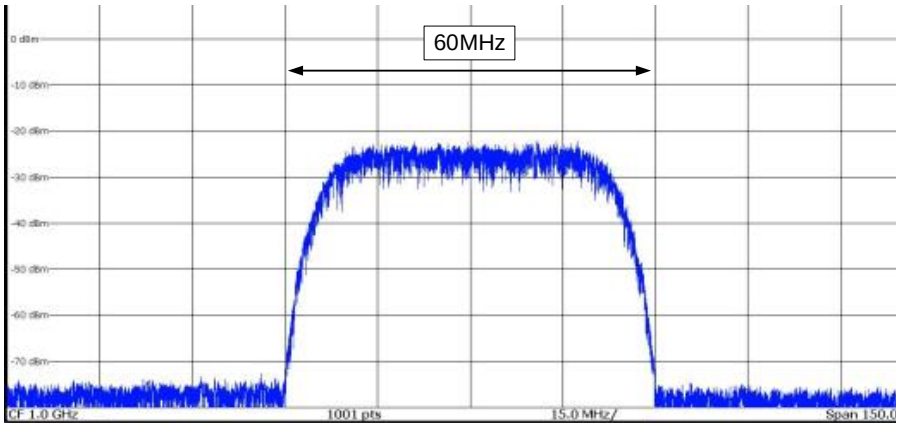


Figure 4.21: The broad-band noise blocker used in measurement of Fig. 4.20.

4.3.1 TX Spectral Mask

One of the important aspect of any communication system is the occupied bandwidth. Spectrum is a scarse and very expensive today due to high demand for over the air communications. Here we show the occupied bandwidth of our system. Fig. 4.22 shows the setup that is used to generate the transmitter spectrum. We have generated a 50Mhop/s signal using this setup and the result is shown in Fig. 4.23. The Tektronix signal generator is programed using a MATLAB and generates our disired fast hopping LO for this measurement. Two LNAs are used as linear PAs. The high-pass and low-pass filters are used as band select filter the combined measured frequency response of these filters is shown in Fig. 4.24. The total power in the band is around 20dBm. The data rate was set to 470Kbps which did not have much impact on the TX spectrum. The TX spectral mask is also shown for a lower hopping speed of 10MHop/s in Fig.4.25.

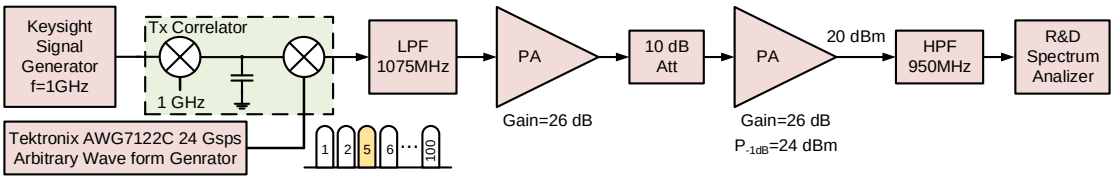


Figure 4.22: Transmitter setup used to measure spectral mask.

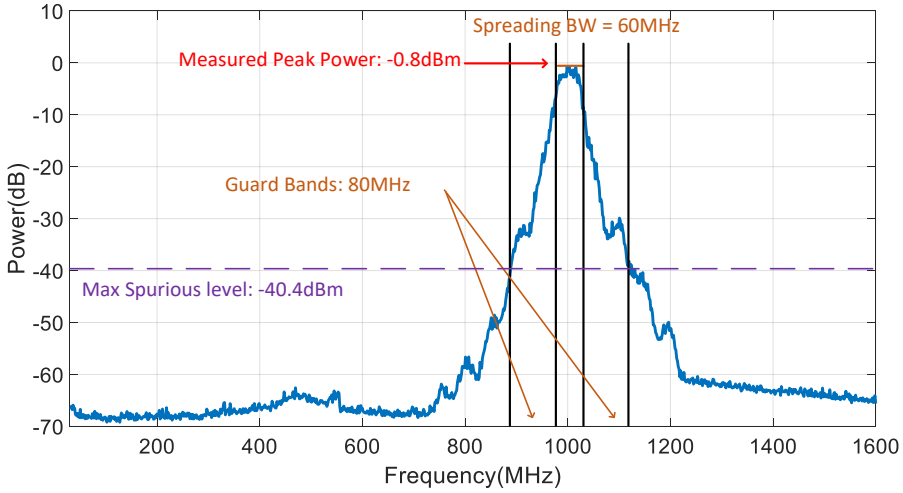


Figure 4.23: Transmitter spectral mask for hopping speed of 50MHop/s and data rate of 470Kbps.

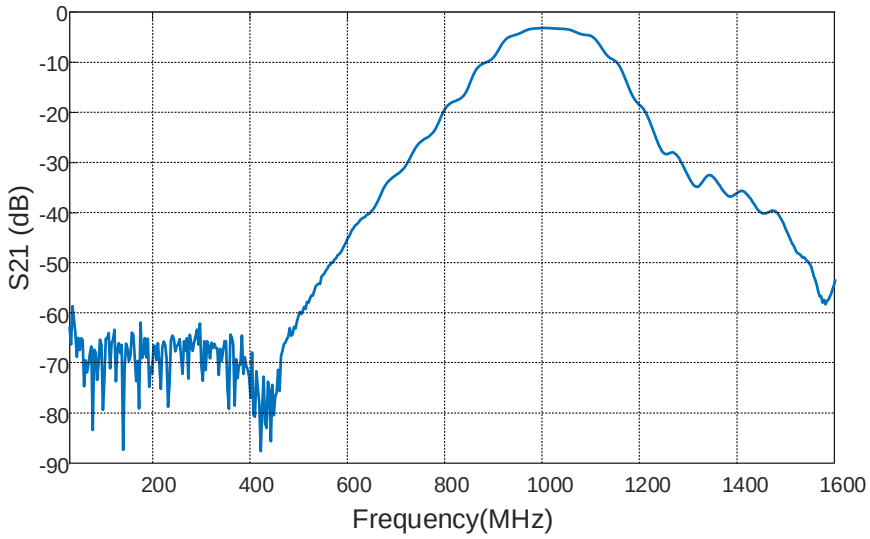


Figure 4.24: Combined response of LPF and HPF constructing a BPF response. The -3dB band is 950-1075MHz.

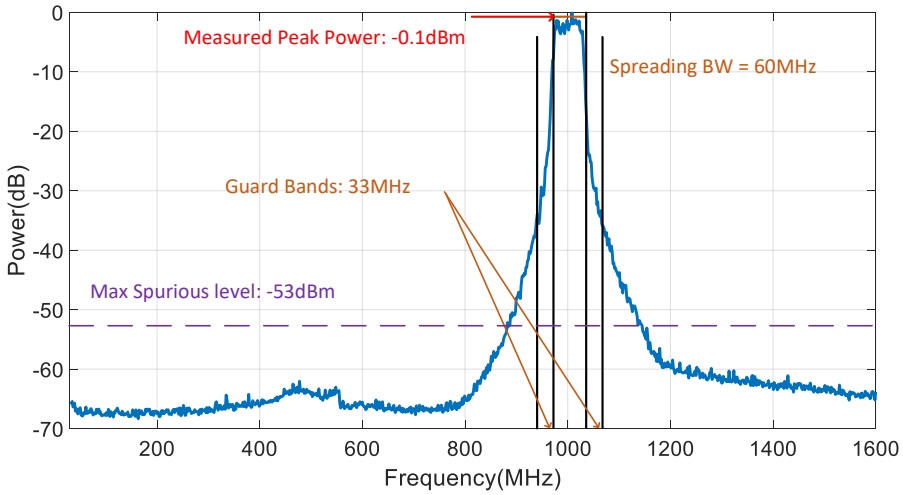


Figure 4.25: Transmitter spectral mask for hopping speed of 10MHop/s and data rate of 470Kbps

Table 4.1: Power break down for the system

f_{RF} (GHz)	f_{clk} (GHz)	f_{dac} Output (GHz)	Power (mW)		
			DO+DAC	Correlator	Total
0.4	2.4	0.8	24	1.2	25.2
1	1.6	0.4	16+6(ILO)	2.6	24.6

4.4 Power Consumption

4.1 provides details for the power consumption for two specific cases. In case 1, the RF signal is at 0.4 GHz, and the fundamental of the DAC output, at 0.8 GHz, drives the 25% signal generator without an ILO. The total power for TX and RX are 25.2 mW each. In case 2, the RF signal is at 1 GHz, and the first image of the DAC output, at 2 GHz=fclk+fdac , drives the 25% signal generator with an ILO. The total power for TX and RX are 24.6 mW each. The ILO (not included in this prototype) power is estimated at 6 mW from simulations. All other powers are measured.

4.5 Measurement Summary

4.2 compares our design transceiver with previously published spread spectrum transceiver designs with a focus on FH implementations. Table II shows that our design is the only one that provides processing gain and importantly does this at RF. The processing gain translates into in-band blocker rejection as demonstrated using EVM measurements and

as shown in Table II. The hopping speed is more than 312 times higher than the next fastest reported system [36]. Other systems hop at much lower speeds. For instance, [37] and [38] hop at 0.024 and 0.007 Mhops/s, respectively, assuming that the hopping speed is ten times the PLL settling time. This is the first FH system that spreads a single symbol over more than one hop and provides processing gain. In comparison to others, we have increased the number of hops/symbol by 100 times, i.e., 20 dB of processing gain [16], [36]. References [39] and [40] do not report the processing gain but report 18.6 and 38.5 dB of self-interference cancellation compared with 33 dB for this design. These designs use DSSS techniques, which use the entire frequency band regardless of the specific code used. Because the total bandwidth occupied is large at all instances, DSSS techniques normally use RAKE receiver architectures to mitigate multipath fading. RAKE receivers increase the complexity and power consumption of these architectures. On the other hand, for FHSS receivers, the occupied bandwidth is narrow at each instance simplifying multipath equalization. In addition, FHSS techniques inherit another advantage, i.e., once the jammer location is identified, the jammer frequency location can be avoided entirely [39, 40]. In our design, the random channel hopping behaves like a spectrum sensor where the jammer channel can be identified. The sensitivity of the correlator is -95 dBm, which translates into 6 dB NF for QPSK modulation at 470 KSps.

Table 4.2: Comparison with the state of the art

Reference	This work	[16]	[36]	[37]	[39]	[40]	[38]
Method	FHSS	FHSS	FHSS	FHSS	DSSS	DSSS	FHSS
Center frequency (GHz)	0.4-1.0	0.9	0.9	0.12	0.9-1.1	0.3-1.4	2.4
RF processing gain(N=10/100) (dB)[1]	10/19.4	0	0	NA	NA	NA	NA
IB blocker rejection (N=10/100) (dB)[1]	10/19.4	0	0	NA	NA	NA	NA
NF (dB)[2]	6	NA	NA	NA	4-5	2.5-4	NA
Hop speed (MHops/S)	50	0.08	0.16	0.024	NA	NA	< 0.07
Hops/symbol	100	1	1	< 1	NA	NA	< 1
Power (mW)	24	NA	525	4.6	9.37	35	NA
RF TX SIC (dB)	33	NA	NA	NA	18.6	38.5	NA

[1] The signal power was set to -29dBm and the blocker power was varied from -50dBm to -15.3dBm.

[2] The NF of the correlator was measured without hopping. This measurement does not include the circulator noise.

Chapter 5

Discussion and areas for future work

5.1 Conclusions

The first ultra-fast hopping transceiver front-end architecture that provides 20 dB processing gain at RF is presented. The front end is implemented in a 65 nm CMOS RF GP process and is made possible by two sub-circuits: first, an RF correlator that can change frequency in less than 0.5 ns in response to the LO and second, ultra-fast hopping all-digital signal generator that can hop in less than 1.5 ns. Even better performance is expected for scaled technologies due to the digital nature of the circuits. The 20 dB processing gain is realized by using 100 hopping channels. The processing gain can be increased with the number of channels used. The receiver is able to reject one or more blockers at the same time without any a priori knowledge of their frequency. With the jammer frequency information, the performance can be improved further by avoiding the jammer channel completely.

Chapter 6

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