Strontium Stannate – An Emerging Wide Gap Semiconductor for Field-Effect Transistor Applications

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Dedication

I humbly offer this dissertation as a homage to *Goddess Saraswati* who bestowed me with the abilities to produce this work. I dedicate this work to the *hindu guru parampara* whose guidance has empowered me to make the appropriate decisions at every step of my life. I also dedicate this work to every single life on this planet that has influenced me and contributed to molding me into the person that I am.

To my parents, my sisters, my family, and my love, …

Abstract

Perovskite oxides are a promising family of materials with the potential for enabling the development of advanced novel electronic device components. However, the lack of an appropriate channel material has hindered the development of game-changing perovskite-based electronic devices. Perovskite stannates are emerging tin-based perovskite oxide semiconductors that have all the requisite material properties for a channel material and are capable of high electron mobilities at unusually high carrier concentrations. Among the perovskite stannates, barium stannate (BSO) has been the most popularly researched material. Strontium stannate (SSO), another interesting perovskite stannate, has been relatively less explored, even though by virtue of its smaller lattice constant, it is more amenable for heterostructure growth than BSO and for eventual integration with other perovskite oxide materials of novel technological interest. SSO also has a wide band gap in the range of 4-5 eV, which makes it particularly well suited to high-power and radio frequency (RF) applications. These properties provided us enough motivation to explore SSO for field-effect transistor (FET) applications.

In this dissertation, the demonstration of first-ever SSO-based FETs with record performance for any stannate-based FET is presented. Further, the challenge of producing low resistance ohmic contacts to SSO is addressed through a systematic study, and optimized contacts for use in FETs are demonstrated. Improvement in performance over our previously reported SSO-based FETs is presented by utilizing a bi-layer film structure

and RF operation in SSO-based FETs is also reported. This study lays the foundation for the development of future high-performance and novel perovskite devices.

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Chapter 1

Introduction

Electronic circuits have vastly transformed our daily lifestyles through their use in an endless list of applications in several sectors, including medical, communication, defense, automotive, aerospace, consumer electronics, industries, and services. The ubiquitous presence of electronics in our lives has been arguably made possible by the groundbreaking invention of a field-effect transistor (FET), a fundamental electronic device, which operates on the principle that the conductivity in a semiconducting channel can be modulated by applying an electric field. A basic FET consists of a semiconducting channel with a well-defined carrier concentration, conducting metal lines to make low-loss contacts to the semiconductor, and another gate metal line to control the electric field in the channel directly, or through a dielectric in between the gate metal and a semiconductor. Today, a billion transistors, which have more complex designs and perform various individual functions, can be monolithically integrated to produce a circuit operating as a high-performance computer that can be as small as a United States one-cent coin.

Tremendous progress has been made in advancing the transistor technology since the invention of the FET. As researchers continue to innovate to devise the next major technological breakthroughs, there is an interest in exploring the integration of novel materials with interesting physical properties, within the standard FET structure, in order to create improved transistors that can allow significantly lower off-state leakage currents, provide higher on-state currents, can switch substantially faster, and may also perform unique additional functions. These novel materials that are broadly referred to as functional materials may exhibit one or more of interesting physical properties, including ferroelectricity, ferromagnetism, piezoelectricity, ultra-high dielectric permittivity, thermoelectric properties, superconductivity, metal-to-insulator transition, electro-optic, and optoelectronic properties.

A sizeable number of these functional materials, which have been identified so far, happen to be oxides, and may be integrated with semiconductors and/or other types of materials to produce novel electronic devices [1, 2]. An illustration in Figure 1.1 shows the broad device categories that one or more of these functional materials can enable. New device structures that do not exist currently may also emerge in the future by utilizing a combination of these

materials. In order to ensure stable operation of such complex devices, the functional as well as the semiconducting materials used are typically required to be of high-quality and free of any defects. Identifying a suitable combination of materials and achieving monolithic integration to fabricate reliable device components can be a significant challenge as many of the functional materials may not be compatible with the widely used conventional semiconductor materials, such as silicon (Si), gallium arsenide (GaAs), and gallium nitride (GaN). These novel materials and devices form topics of great interest for fundamental research, despite the difficulties involved, because of the remarkable properties exhibited by these functional materials.

In order to be able to employ these materials with intriguing physical phenomena in real life applications, identification of an apt material system is a necessary initial step and may depend on the specific application itself. This motivated me to delve into a materials system known as perovskite oxides, which led me to an exciting wide gap semiconductor known

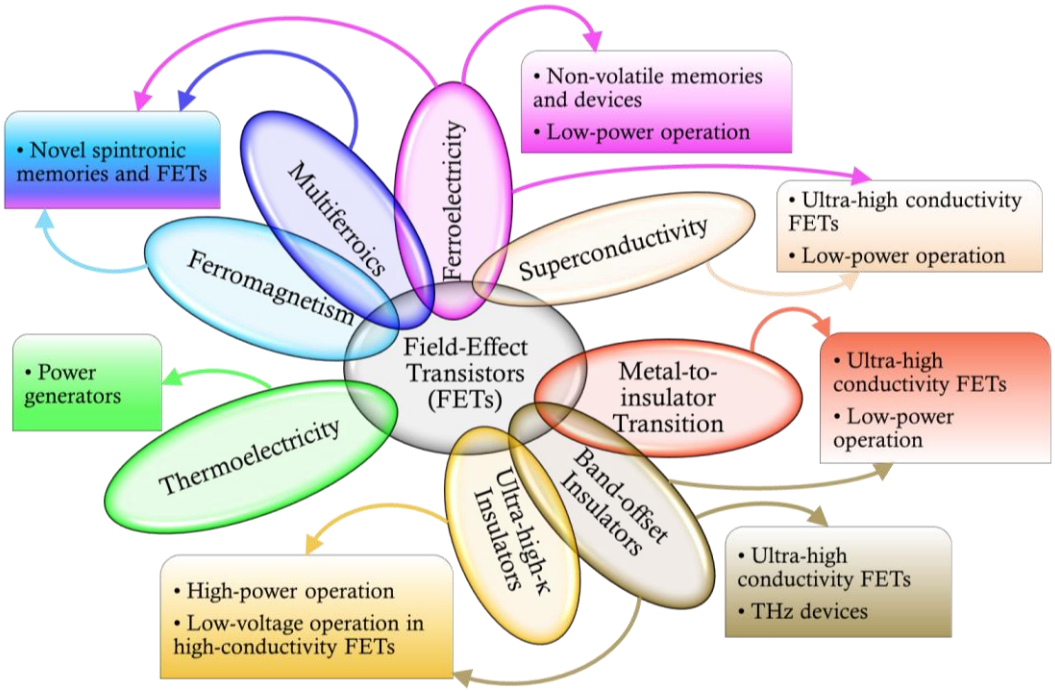

FIGURE 1.1. One, or a combination of functional materials may be integrated with field-effect transistors (FETs) to improve performance and/or effectuate a unique characterstic. Each oval shape represents an interesting physical property that may be combined as suggested by overlapping shapes.

as strontium stannate ($SrSnO_3$ or SSO). I chose to work on SSO for my dissertation because it has the potential to fill the void created by the lack of a perovskite oxide-semiconductor channel material with requisite properties and may eventually contribute to the development of game-changing electronics. I will first introduce the perovskite oxide materials, their rich functionality, and the known semiconductors within this material family, which should explain the rationale behind my decision to work on this emerging material.

1.1 Perovskite Oxide Materials for Transistor Applications

All materials whose crystal lattice structure can be derived from basic cubic perovskite crystal structure that is shown in Figure 1.2 can be broadly classified as a perovskite oxide material. Here, the oxygen anion atom, O, occupies the eight corner-sites, and a cation atom, '*B*', occupies the center of a 'BO_6' octahedron, which coincides with the center of the cube formed by another cation atom, '*A'*. The structure of any perovskite oxide can be derived from the basic skeletal structure formed by the three ionic sites. Different cation sizes can lead to a change in the number of symmetry elements possessed by the material's crystal structure and cause the 'BO_6' octahedron to rotate, resulting in different repeating unit cell structures for different materials. The difference in symmetries arising from the changing unit cell structures of the respective perovskite oxide materials gives rise to

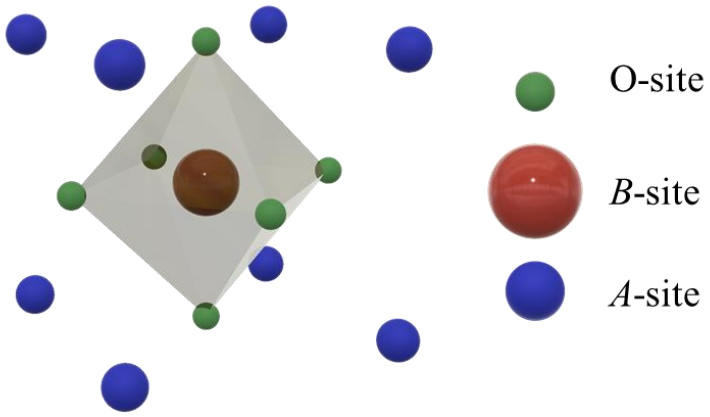

FIGURE 1.2. A perovskite unit cell showing the cations, *A* and *B*, and O-atom. This can be understood as the basic skeletal structure from which all perovskite materials' crystal structures can be derived through modifications dictated by changes in atomic sizes and bond-angles. The octahedron represents the BO_6 bonds.

different fundamental physical properties in the respective materials. A total of 17 elements in the periodic table, namely Na, K, Rb, Ag, I, Cs, Ba, Tl, Bi, La, Nd, Sm, Eu, Gd, Tb, Dy and Yb can fit in the perovskite structure as the cation atom, *A*, while 32 elements, namely Li, Mg, Al, Sc, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Zn, Ga, Ge, Zr, Nb, Mo, Tc, Ru, Rh, Pd, Sb, Hf, Ta, W, Ir, Hg, Th, Pa, U, and Np may occupy the *B* cation site. Another 15 elements, namely Ca, Sr, Y, Cd, In, Sn, Pb, Ce, Pr, Ho, Er, Tm, Lu, Pu, and Am can occupy both the *A*- and *B*- sites. A perovskite oxide can be represented by the generic chemical formula ABO_3. Partial substitutions in the *A*- and *B*- sites is also possible, leading to substituted compounds with formulas of the form $A_xA'_{(1-x)}B_yB'_{(1-y)}O_3$, where x and y represent the stoichiometric ratios of the number of *A* and *B* atoms for every three oxygen atoms, respectively. Owing to a wide choice of elements and elemental compositions, the perovskite oxide material system consists of a plethora of compounds, some of which have been explored and are being used for various kind of practical applications.

Several functional perovskite oxide materials that are suitable for transistor applications have also been identified. Some of these materials are listed in Table 1.1 along with their corresponding distinct physical properties. Novel electronic devices have also been proposed that utilize one or more of the functional perovskite oxide materials [3-15]. These devices are also included in Table 1.1, listed by naming the broad device category to which they belong to, and indicating the corresponding physical property that was used in order to achieve a performance improvement or a unique capability in the respective devices. Despite these being preliminary results, they demonstrate the promise of perovskite-oxide-based novel devices. A combinatorial approach has also been proposed [16, 17], where two or more of the perovskite oxide materials can be monolithically integrated to produce tailor-made atomic interfaces such that, a combination of desired physical properties may be observed near the interfaces.

Perovskite oxides offers the twin advantages of choosing from a wide variety of materials combined with the capability to produce engineered interfaces with desired physical properties, making the perovskite oxide material system a compelling choice for next-generation transistor development. However, except for a few, several of these functional

Reference	Material	Functionalilty	Application or Unique Device Property
[3]	$Pb(Zr,Ti)O_3$, $BaTiO_3$	Ferroelectricity	Ferroelectric FET, memories
[4]	$Nb:SrTiO_3$	Superconductivity	Extreme charge density FET with low leakage
[5]	$Pb(Zr,Ti)O_3$/ $Nb:SrTiO_3$	Ferroelectricity/ superconductivity	Extreme charge density FET, non-volatile operation, superconducting quantum interference devices
[6]	$Pb(Zr_{0.2}Ti_{0.8})O_3$/ $La_{0.85}Ba_{0.15}MnO_3$	Ferroelectricity/ ferromagnetism	Ferromagnetic FET, spintronics
[7]	Bi_2Se_3 CoFe/ $BiFeO_3$	Ferromagnetism	Spin-orbit-torque FET, spintronics
[8]	$Nb:SrTiO_3$	Mott transition	Extreme charge density FET with low leakage
[9]	$NdNiO_3/SrTiO_3$	Modulation doping/ Mott transition	Extreme charge density FET with low leakage
[10]	STO/$LaAlO_3$ STO/$GdTiO_3$	Mott transition/ Heterostructure interface engineering	Extreme charge density FET with low leakage
[11]	$SmTiO_3$/ $BaTiO_3$/ $SrTiO_3$	Electrostatic doping/ Ferroelectricity/ Metal-to-insulator transition	Extreme charge density FET with low leakage
[12]	$BaSnO_3$/ $LaInO_3$	Polarization doping	High-electron mobility transistor
[13, 14]	$SrTiO_3$/ $GdTiO_3$	Heterostrucure Interface Engineering	Extreme charge density FET with low leakage
[15]	$CaMnO_3$, $SrTiO_3$	Thermoelectricity	Power generators

TABLE 1.1. A non-exhaustive list of perovskite oxides and their proposed applications in FETs [3-15].

perovskite oxide materials are not suitable for direct integration with existing semiconductor technologies, including Si, GaAs, SiC, and GaN that are currently the leading semiconductor technologies. This is because their crystal structures and lattice constants can be very different from that of the functional perovskite oxide materials. A suitable perovskite-oxide-based semiconducting channel material is required in order to provide the ideal crystal surface template required for monolithic integration with these functional materials. The next section of this chapter discusses the perovskite oxide semiconductors that were identified and examined in the existing literature. The major drawbacks that prevented the use of these existing perovskite oxide semiconductors is also discussed.

1.1.1 Perovskite Oxides as Semiconductor Channel Materials

In order for a semiconductor to be suitable for practical transistor applications, a reasonably high carrier mobility, μ, and a capability to grow the material with a well-defined carrier concentration on a wafer are the bare-minimum essential requirements. The rich functionality offered by the perovskite oxide materials was well-known and attempts were made to explore suitable perovskite oxide semiconductors that can enable novel devices [18, 19, 20]. Using a sub-class of perovskite oxides, known as manganites, in which the *B*-site is occupied by a manganese cation, Mn, ferroelectric FETs, were demonstrated in [18], to explore their use in memory applications. Phase modulation was also explored in manganites in [19, 20], where strain-mediated metal-insulator transition was exploited in FET structures in [19], while electric-field effect on the separation of two competing phases namely, a metallic ferromagnet-based phase, and an insulating charge-based phase in manganite thin films was explored in [20]. Basic FET structures using tantalates, where the *B*-site is occupied by a tantalum cation, Ta, were also investigated motivated by a similar future outlook [21]. Titanates, which have a titanium cation, Ti, in the *B*-site were also studied, among which, Strontium titanate (STO), $SrTiO_3$, one of the most widely studied perovskite oxide semiconductors, deserves a particular mention. Electron mobilities above 1000 cm^2/Vs [22] were measured at a temperature of 7 K in FET structures fabricated on crystalline STO wafers. Novel heterostructure STO-based FETs were also demonstrated, where metal-to-insulator transition was demonstrated in [9, 10] and heterostructure interface engineering in order to achieve the highest modulated sheet-carrier density in a planar FET, for any semiconductor material system, was shown in [13, 14].

Despite these experimentally demonstrated novel device structures, the performance of transistors based on all the three perovskite oxide-subclasses mentioned above, viz. the manganites, tantalates, and titanates, remained significantly below par in comparison to that offered by conventional semiconductors, including Si, GaAs, and GaN. A discussion regarding performance of perovskite-based FETs will be presented at a later stage in this chapter, while the common pertinent reason for the unattractive FET performance, a

characteristic low electron μ in these materials, is discussed here. The main reason for the low mobilities in the titanate-, tantalate-, and manganite-semiconductors is that the conduction bands, derived predominantly from the *d*-orbitals of their respective *B*-site atoms, are relatively less dispersive resulting in heavy electron effective masses in these semiconductors [23, 24, 25]. Figure 1.3, adapted from [26], shows the band structure of STO, where a less-dispersive conduction band similar to that of other titanate-, tantalate-, and manganite-semiconductors, can be seen. A low maximum Hall mobility, μ_{Hall}, of 30 cm^2/Vs for electrons was observed in tantalates ($KTaO_3$) at room temperature [23], while those observed in titanates (STO) and manganites ($CaMnO_{3-\delta}$) were lower than 10 cm^2/Vs [24, 25]. The field-effect mobilities, μ_{FE}, in the channels based on the three materials [9, 10, 13, 14, 18, 19, 20] can be at least an order of magnitude lower than their μ_{Hall}. Obviously, these semiconductors are not promising as channel materials in practical transistor applications.

The search for an appropriate perovskite oxide channel material led to rediscovery of perovskite stannates [27, 28], which are tin- or Sn-based perovskite oxides, where Sn occupies the *B*-site. The potential of stannates as channel materials remained dormant until then due to poor material quality of previously measured stannate films [29, 30]. The next section focusses on their superior material properties which motivated me to study perovskite stannates as a part of my dissertation work.

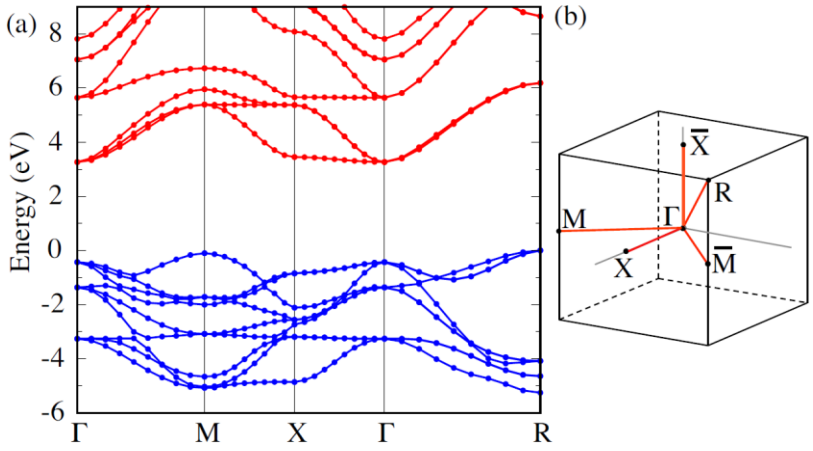

FIGURE 1.3. A calculated band structure for $SrTiO_3$ showing the relatively lesser dispersion near the conduction band minimum (Γ). Figure adapted from [26].

1.2 Perovskite Stannates

A key experimental result observed in bulk barium stannate ($BaSnO_3$ or BSO) crystals [27], where a maximum room-temperature μ_{Hall} = 320 cm^2/Vs was measured for electrons at a relatively-high electron concentration of 8×10^{19} cm^{-3}, triggered an interest in perovskite stannates, including BSO, strontium stannate ($SrSnO_3$ or SSO), and calcium stannate ($CaSnO_3$) as a semiconductors capable of high-conductivity. The corresponding μ = 70 cm^2/Vs observed in an unoptimized crystalline BSO thin film [28] had suggested that the μ can be improved with future structural improvements as well as optimized growth methods, and that stannates may potentially help translate the functional diversity observed in perovskite oxides into practical transistor structures.

The chief distinctive feature in stannates, which helps in achieving such mobilities, are their Sn 5*s*-derived conduction bands, which are generally more preferable as opposed to *d*-derived bands because of their high-dispersive nature that produces low-effective masses [28, 32] (*The band structures of BSO and SSO are shown in later sections*.). Moreover, relatively-high dielectric constants are also observed in these materials which helps screen the carriers from charged-dopant atoms that can otherwise act as scattering centers. This permits higher μ values at relatively-high carrier concentrations in the stannates. Stannates tend to have band gaps wider than ~3 eV, where the band gap increases as the cation size reduces from Ba → Sr → Ca [31]. This, when coupled with the high μ and high carrier concentrations, makes them an interesting material system for applications, including transparent conductive electrodes, transparent thin film transistors, extreme-temperature electronics, UV-blind electronics, high-power, and radio-frequency (RF) transistors. One important requirement is having the ideal Sn-O-Sn bonding-angle close to 180º, in order to preserve the dispersive nature of the conduction bands [28, 32]. Additionally, the Sn-atom may also occupy the *A*- site as mentioned in the previous section, which if not avoided or minimized, can significantly compromise the stoichiometric and crystalline quality of the material. Meeting these two requirements and ensuring overall structural as well as stoichiometric integrity can be non-trivial and highly dependent on the growth technique

and conditions. This leads to a discussion on the material growth techniques for stannates in the following section.

1.2.1 Material Growth

μ in BSO thin films grown using pulsed laser deposition methods were encouraging but was still limited by defects, including grain boundaries, point defects, and dislocations [28, 31] that may be formed during the growth process due to the presence of unavoidable high-energetic particles in the growth chambers. Molecular-beam epitaxy (MBE) can help overcome these defects because of its inherent advantages. MBE can help grow robust-quality films that are required for electronic device applications and is a particularly valuable technique to grow oxide thin films [33]. The growth of an MBE film involves a controlled reaction, where atomic or molecular species that travel in the form of beams to react at a crystalline surface (substrate or wafer) in ultra-high vacuum conditions. The relative concentrations of the individual reacting species can be adjusted by regulating the flux or beam equivalent pressures (BEPs) of the respective species, providing a way to control the stoichiometry of the films being grown. A direct benefit of the clean ultra-high vacuum environment is the absence of high-energetic species which enables a low-energy and controlled growth with minimized defect density [33], apart from ensuring that the growth chamber is free from contaminant species. Other notable advantages of MBE include epitaxial growth, *in situ* characterization during growth, and capability to engineer precise heterostructure interfaces at the atomic level.

Conventional oxide MBE growth techniques involve the supply of cation film constituents via effusion cells consisting of solid high-purity elemental sources, while the oxygen is normally supplied via an oxygen plasma source, molecular oxygen vapor source, or even ozone. However, such techniques can fall short of producing phase-pure stoichiometric films in certain oxides, where some metal atoms, including Sn, Co, and Ni, display significantly weaker tendency to oxidize [34]. This problem can be amplified in the case of ternary oxides of the form ABO_3, where the *A*-cation, such as Ba or Sr can have significantly different oxidation potentials as compared to say, Sn, Co, or Ni, which are to be restricted to the *B*-site only [34]. The precursors and environmental conditions in the

growth of such films have to be meticulously determined in order to ensure good-quality MBE-films. Two different research groups were the first to independently demonstrate two distinct modified-MBE methods to address this issue for the growth of stannate films. One approach, also referred to as the radical-based hybrid-MBE involves the use of a chemical precursor, hexamethylditin, $(CH_3)_6Sn_2$ (HMDT) as the source of reactive Sn-radical during the growth, in order to make the Sn-O reaction thermodynamically favorable [34]. The other approach addresses the issue by sourcing high-purity solid SnO_2 via an effusion cell that can act as additional oxygen source apart from an RF O_2 plasma source and together help maintain the stoichiometry in the as-grown films [35]. Both the approaches were successful in demonstration of conducting-BSO thin films with excellent control over dopant concentration [35, 36] and a brief contrast of the experimental results obtained by the two methods is discussed in the following paragraphs.

The radical-based hybrid-MBE technique was pioneered by Prof. Bharat Jalan's research group belonging to the Department of Chemical Engineering and Material Science at the University of Minnesota, Twin Cities. A schematic of the hybrid-MBE chamber used by the Jalan MBE lab is shown in Figure 1.4 which illustrates the Ba effusion cell, an O_2 RF

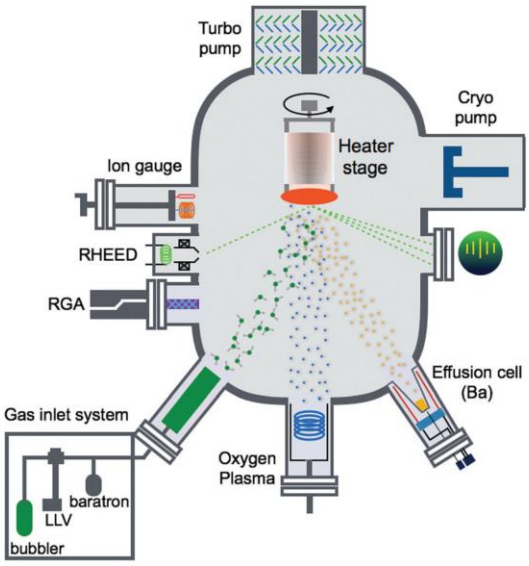

FIGURE 1.4. A schematic of a hybrid molecular beam epitaxy (MBE) chamber and its various components. Sn precursor is supplied via a gas bubbler system, O_2 precursor via an RF plasma, and other cation or dopant precursors can be supplied using an effusion cell. Figure adapted from [36].

plasma source, and the HMDT precursor source. Additional sources such as a La effusion cell may also be used in order to dope the stannate films. The atomic and molecular beams travelling from the individual sources to a heated substrate wafer is also depicted to help understand the MBE-growth concept. The MBE chamber used in the other approach with SnO_2 as a precursor can be imagined to be very similar with an additional effusion cell for the Sn-precursor.

Using both the distinct approaches [36, 37] an adsorption-controlled growth regime was achieved in which, the film composition is locally self-regulated because of the volatility of the surplus growth constituents. The stoichiometry of the films is regulated by controlling the relative BEPs of the various precursors as stated previously. Using the hybrid-MBE approach and a Sr effusion cell instead of Ba, successful growth of conductive doped-SSO thin films has also been shown with a maximum room-temperature μ = 70 cm^2/Vs [38, 39] and remains the only experimental demonstration of conductive MBE-grown SSO thin films to date. The only other MBE-grown SSO thin films which were obtained using SnO_2 as precursor [40] were insulating for unknown reasons. However, it is interesting to note that the same approach led to the display of a maximum μ = 180 cm^2/Vs in BSO thin films reported to date [35, 37], slightly larger than that of 120 cm^2/Vs reported using the hybrid-MBE approach [41]. Both the approaches seem viable to obtain stannate thin films for semiconducting device applications with room for improvement through further optimizations. The hybrid-MBE method is perhaps a more versatile technique that may be extended to grow other types of epitaxial films where a compound source equivalent of SnO_2 may not be easily available for use in the MBE effusion cells to produce reactive precursors. Regardless, the superior transport properties observed in films obtained using both the techniques show that stannates hold promise as perovskite oxide semiconductors suitable for electronic device applications.

1.2.2 Barium Stannate

Among the perovskite stannates, barium stannate ($BaSnO_3$ or BSO) in particular has invited well-deserved attention as an attractive channel material for perovskite-based electronic devices, ever since a record room-temperature electron μ = 320 cm^2/Vs for any

perovskite-based semiconductor was reported [27]. A wide band gap of ~3 eV [42] and a high-conductivity in BSO thin films attributable to mobilities above 100 cm^2/Vs at carrier concentrations exceeding 10^{20} cm^2/Vs [35, 37, 41] already places BSO at par with the benchmarks set by commonly used and best available transparent conducting oxides [41]. This also partly due to a relatively-high dielectric constant of 15-17 [43] in BSO. The above properties make it an interesting channel material candidate for applications, including transparent conductive electrodes and transparent electronics, high-power and RF electronics, high-density quantum-well structures apart from the potential multi-functional perovskite-based novel devices as stated before. BSO, even in its thin film form, was found to be extremely thermally stable up to temperatures in excess of 500 ºC [27] with only minimal degradation in transport properties suggesting possible use in extreme environment electronics and sensors. In less than a decade since its rediscovery [27, 28], a number of research avenues have opened up [31], based upon which one can argue that BSO has begun to displace STO as the archetypal perovskite semiconductor and is certainly the most-studied perovskite stannate. A discussion on any stannate materials without discussing BSO is simply unthinkable.

1.2.2.1 Crystal and Band Structures

BSO adapts to an ideal cubic perovskite crystal structure as shown in Figure 1.5(a), where the positions of *A*- (Ba), *B*- (Sn), and *C*- (O) sites are shown within a unit cell. Figure 1.5(b) also shows a BSO crystal with multiple unit cells highlighting the shared SnO_6 octahedron network and the Sn-O-Sn bond angle formed as a result. The lattice constant of the bulk cubic BSO crystal is a = 4.116 Å, slightly larger than those of commercially available perovskite substrates. As a result, the as-grown BSO films are generally not lattice matched to these substrates, with the mismatches ranging from the lowest of +2.3% that was demonstrated on $PrScO_3$ substrates to +5.1% on $SrTiO_3$ substrates [35, 37, 41]. This mismatch generally results in misfit dislocations and strain relaxation in the films that tend to be concentrated near the film-substrate interface in thin films, and additionally causes threading dislocations in thicker films that can propagate through the entire

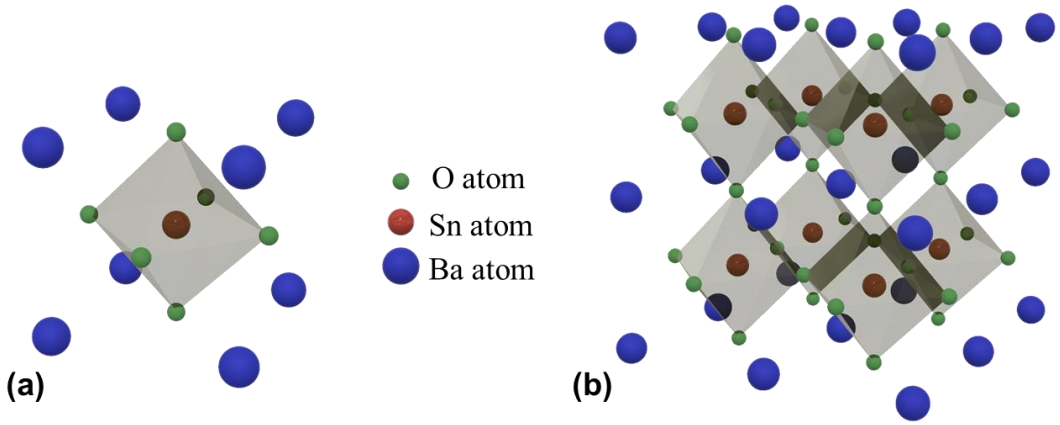

FIGURE 1.5(a) A simple unit cell of a $BaSnO_3$ (BSO) crystal. SnO_6 bonds are represented by the octahedron. (b) An alternate representation of the BSO crystal which shows the shared octahedral network and the perfect cubic lattice arrangement.

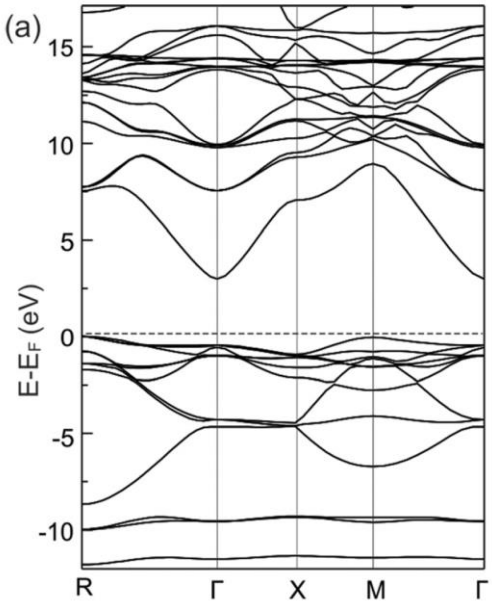

FIGURE 1.6. Calculated band structure of $BaSnO_3$ showing a dispersive conduction band minimum that results in a low effective mass. Indirect band gap of ~3 eV is also shown (Γ and R). Figure adapted from [44].

thickness of the films. The BSO films grown on these substrates also tend to be compressively strained single-phase films because of the larger lattice constant of BSO relative to the substrates.

The band structure of BSO obtained using *ab initio* calculations by the authors in [44] is shown in Figure 1.6. Figure 1.6 reveals a conduction band minimum at the Γ point and a valence band maximum at the R point in the reciprocal space that corresponds to an indirect band gap of ~3 eV, which was confirmed experimentally as well in [44]. The dispersion in the E-*k* curves of the conduction band near the minimum, derived predominantly from the Sn-5*s* bands as stated earlier, can also be seen in the Figure 1.6. While theoretically calculated values of effective masses vary in the literature, recent results supported by experiments seem to indicate a relatively-low electron effective mass of ~0.2m_e [32, 44, 45, 46], where m_e is the electron rest mass.

1.2.2.2 Mobility

The carrier μ is a fundamental material property that impacts the operation speed and currents in all electronic devices. Owing to its light electron effective mass and low phonon

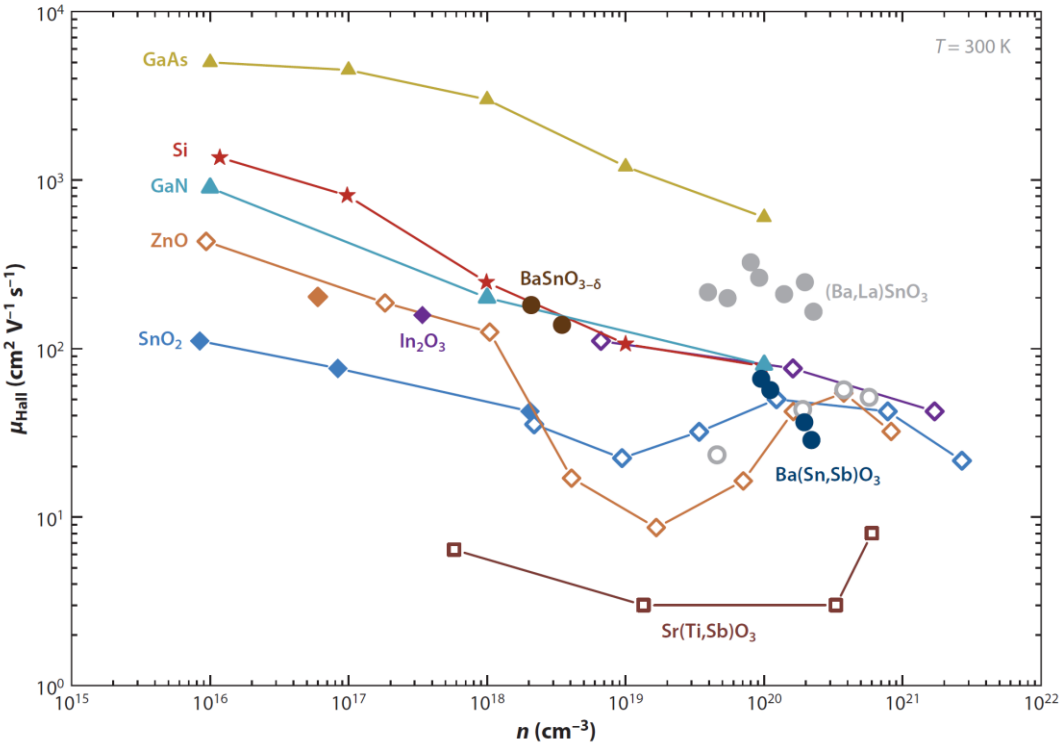

FIGURE 1.7. Log-log plot of the μ_{Hall} measured at 300 K vs carrier concentration that compares the μ_{Hall} of $BaSnO_3$ with that of other transparent conducting oxides and conventional semiconductors. Figure adapted from [31].

scattering compared to other polar oxides, BSO is a high mobility material. The distinctive feature of BSO, as highlighted in Figure 1.7, is that it is capable of such high mobilities even at carrier concentrations close to 10^{20} cm^{-3}, a property that is not commonly observed in other conventional semiconductors as well as transparent conductive oxides. This can be attributed to a combination of stronger dielectric screening [43] of the electrons from various charged-impurity scatterers and low electron-phonon scattering in comparison to other polar-materials [46]. Figure 1.7 shows that at comparable carrier concentrations, BSO has higher μ than all the commonly used transparent conducting oxides and most other semiconductors, except GaAs. A comparison of BSO with STO is also presented in Figure 1.7 showing a 30× higher μ.

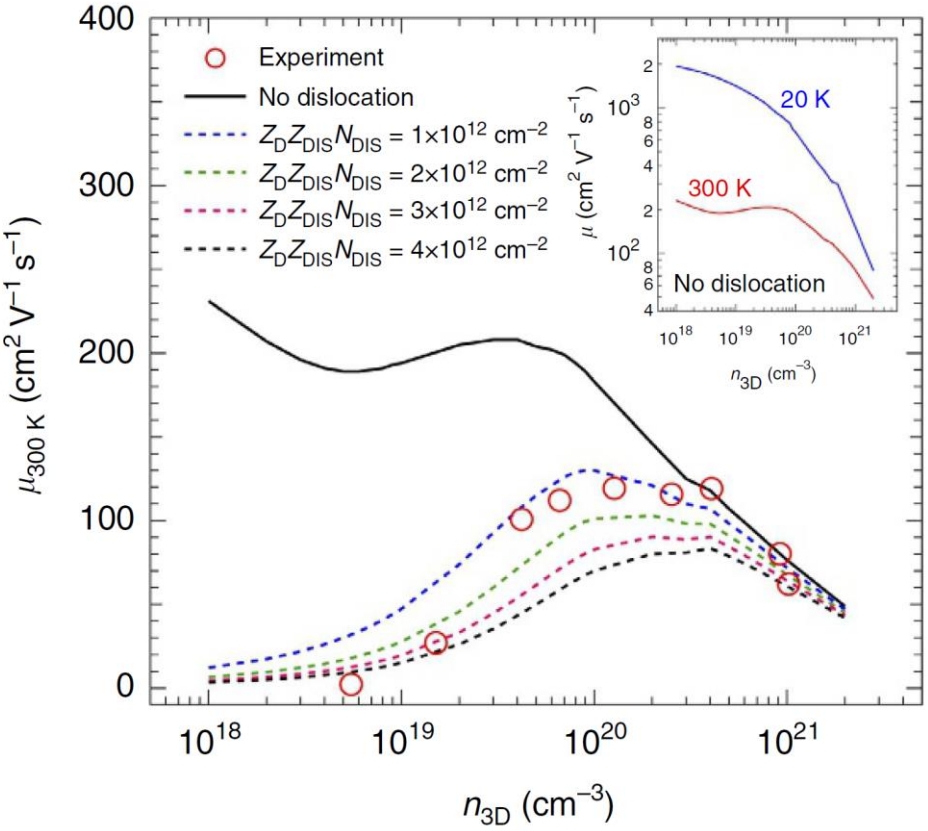

FIGURE 1.8. Semi-log plot of the measured mobility in $BaSnO_3$ vs n_{3D} cm^{-3}, plotted as a function of different dislocation densities. Figure adapted from [41].

Figure 1.8 displays the effect of changes in threading dislocation densities on the mobility in BSO films, shown as a function of three-dimensional carrier concentration, n_{3D}. To

obtain the data in this figure, the authors in [41] assumed that the dislocations which can arise due to lattice mismatch with the substrates are negative (acceptor-like) charged scatterers. *Ab initio* calculations were then used to fit the experimentally measured mobility vs n_{3D} curves with the dislocation density as a fitting parameter. Figure 1.8 suggests that a high dislocation density in BSO films can degrade the carrier μ and dislocation densities on the order of 10^{12} cm^{-2} were estimated in these BSO films. The expected μ as a function of n_{3D} is also shown for the case of no dislocations, demonstrating a path forward to improve the μ in these films. The inset in Figure 1.8 also shows that the electron-phonon scattering limits the maximum room-temperature μ achievable at lower n_{3D}.

Figure 1.9, obtained from [47], compares the μ data in BSO thin films and bulk crystals obtained by various research groups showing the consistent high mobilities measured for carrier concentrations ranging from ~2×10^{19} cm^{-3} to ~4×10^{20} cm^{-3}. For very high carrier concentrations above 5×10^{20} cm^{-3} the μ degrades steadily with increasing carrier concentration as the impurity scattering due to dopant atoms begins to manifest in a

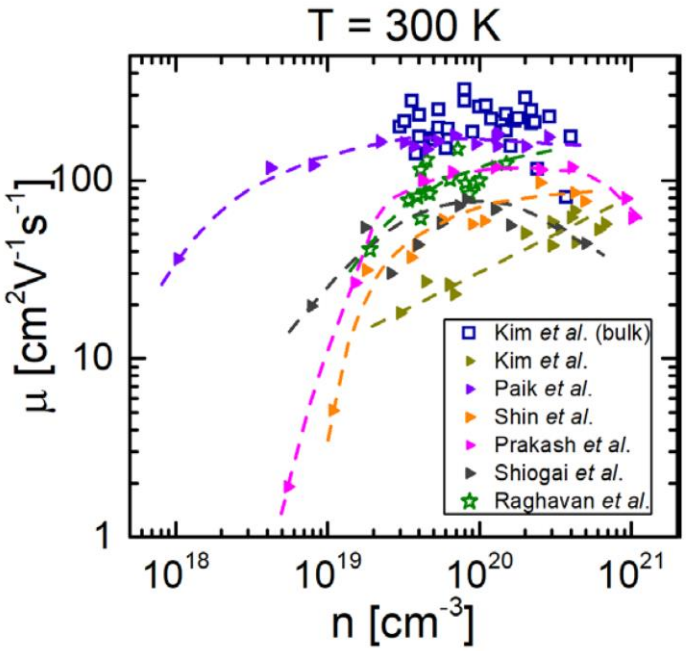

FIGURE 1.9. Log-log plot of the μ cm^2/Vs, in bulk and $BaSnO_3$ thin films vs carrier concentration. Figure adapted from [47].

significant way. Another noteworthy observation is that Paik *et al.* [37] were able to measure significantly higher mobilities at lower carrier concentrations in the range of 10^{19} cm^{-3} to 10^{18} cm^{-3}, which they attribute to superior stoichiometric control in their growth process, leading to a lower shear and point defects that can otherwise act as trap centers for the carriers. This not only allowed them to measure these relatively-low carrier concentrations but also likely improved the μ measured at all carrier concentrations. Discrepancies in the data in Figures 1.8 and 1.9, despite similar dislocation densities, suggest that the presence of point defects could be contributing to lower mobilities in the existing BSO films. The insights provided in [37, 41] clearly indicate that higher mobilities can be attained in BSO films by lowering the defect densities and further carefully designing the underlying buffer (or substrate) layers as well as adjusting the growth conditions.

1.2.3 Strontium Stannate

Strontium stannate ($SrSnO_3$ or SSO) is another exciting semiconductor material belonging to the perovskite stannate family. Bulk SSO stabilizes in the form of an orthorhombic (space group: *Pnma*) unit cell, at room temperature, with an in-plane lattice parameter, a_{pc} = 4.035 Å [48]. Two other crystal phases, namely orthorhombic (space group: *Imma*) and tetragonal (space group: *I4/mcm*) are also possible with a_{pc} = 4.068 Å, and 4.069 Å respectively, which normally exist at temperatures in excess of 905 K and 1062 K, respectively [49]. The smaller in-plane lattice parameter for SSO with respect to BSO (4.116 Å) not only allows better lattice matching to commercially available substrates but makes SSO more amenable to heterostructure integration with perovskite materials of functional and technological interest. Moreover, SSO has a wider band gap (4-5 eV) [50, 51, 52] than BSO (~ 3eV) and primarily has similar energy dispersion in the *k*-space, near the conduction band minimum indicating that similar mobilities are achievable in SSO thin films. Among the stannates, the above properties make SSO particularly well-suited to high-power and RF electronic applications. The better lattice matching can make low defect density growths possible, because of which SSO is perhaps well-suited even for novel heterostructure devices.

1.2.3.1 Crystal and Band Structure

Figure 1.10(a) represents a unit cell of SSO that shows the Sr (*A*-), Sn (*B*-), and O (*C*-) sites. As stated earlier, SSO can exist in multiple crystal phases which differ primarily in terms of the tilting of the octahedrons in the shared three-dimensional network. Figure 1.10(b) shows the tetragonal phase structure, from which the other phases can be derived with the help of the Glazer notation [53]. For the benefit of better visualization, the top and front views of the SSO tetragonal phase crystal in Figure 1.10(b) are shown in Figure 1.10(c) and (d), respectively. The Glazer notation can be used to describe the different SSO crystal phase structures with respect to the perfect cubic perovskite structure that has no

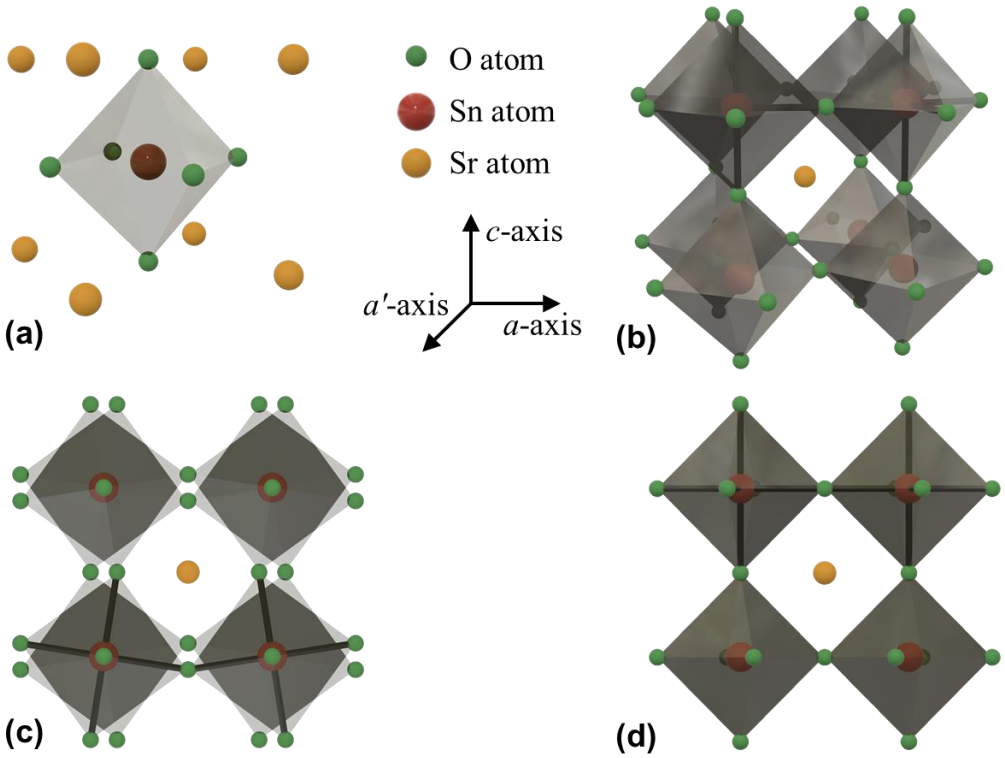

FIGURE 1.10. (a) Simple unit cell of $SrSnO_3$ (SSO) showing the SnO_6 bonds and relative positions of the Sr atom. (b) SSO in tetragonal *I4/mcm* phase and the corresponding axis directions are also shown. (c) Top view of crystal shown in (b). (d) Front view of crystal shown in (d).

octahedral tilts (same as the BSO crystal structure). The symbol notation, $a^{\#}a'^{\#}c^{\#}$, where the superscript # can take on the values 0, +, or –, can be used to indicate no tilt, adjacent

octahedrons tilting in the same, or opposite directions, respectively. The letters a, a', and c refer to tilt around the [100], [010], and [001] directions of the cubic perovskite coordinate system, respectively. Starting from $a^0a'^0c^0$, which is the perfect cubic perovskite structure, the *I4/mcm* tetragonal phase in Figure 1.10(b) can be obtained with $a^0a'^0c^-$ tilting [49]. The orthorhombic *Pnma* and *Imma* phases can be obtained using $a^-a'^-c^+$ and $a^-a'^-c^0$ tilts, respectively [53]. The smaller size of the Sr cation in comparison to the Ba cation allows these octahedral tilts and thus, multiple crystal structures to exist. Even though the *I4/mcm* tetragonal and *Imma* orthorhombic phases normally do not exist at room temperatures, it has been shown that all the three phases can be stabilized on different substrates using strain engineering and hybrid-MBE growth method [54].

While no significant change in the band gap is expected in the three phases [55, 56], it has been shown experimentally and supported via theoretical calculations that the *I4/mcm* tetragonal phase is capable of a higher μ than the orthorhombic *Pnma* phase [54]. In fact, the experiments showed a 3-fold μ increase in the *I4/mcm* tetragonal phase films even though the dopant concentration was kept the same as that of the orthorhombic *Pnma* phase films, suggesting that other factors such as defect- or phonon-scattering may be further reducing the μ in the orthorhombic *Pnma* phase films. Figure 1.11(a), obtained from [55],

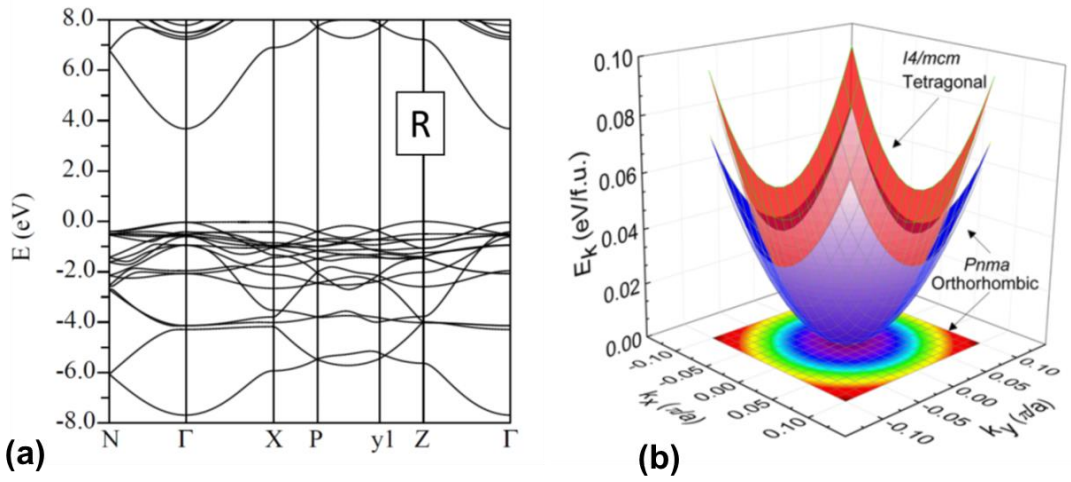

FIGURE 1.11. (a) Calculated band structure for tetragonal *I4/mcm* $SrSnO_3$ (SSO). (b) Dispersion around the conduction band minima for the tetragonal and orthorhombic phases are shown which shows a lower effective mass for electrons in the tetragonal phase of SSO. (a) and (b) adapted from [55] and [54], respectively.

shows the calculated band structure for the *I4/mcm* tetragonal phase, where the dispersive conduction band minimum can be seen. Figure 1.11(b), obtained from [54], compares the two-dimensional projection of E-*k* surface of the *I4/mcm* tetragonal and orthorhombic *Pnma* phases to show that the electron effective mass is smaller in the *I4/mcm* tetragonal phase. The effective mass of electrons in the *I4/mcm* tetragonal phase was found to be ~0.3m_e which is comparable to that of the BSO effective mass indicating that similar μ values can be obtained in SSO films as well. However, other factors such as phonon-scattering that can vary from phase to phase may also come into play which can affect the mobilities attainable in SSO. As a final note on the band structure, even though Figure 1.11(a) suggests a smaller band gap obtained from theoretical calculations, other experimental and band gap calculations that have accounted for strain in the SSO films strongly suggest a band gap in the range of 4-5 eV [50, 51, 52, 54, 55].

1.2.3.2 Mobility and Surface Effects

The tetragonal-phase stabilized SSO films grown on $GdScO_3$ (110) [39, 54] using the hybrid-MBE approach were shown to have good mobilities with a record reported value of 70 cm^2/Vs for any SSO film [38, 39, 50, 52, 54, 56]. These films [38, 39, 54] happen to be the only MBE-grown conductive-SSO films reported to date. Figure 1.12 shows the dependence of mobility and n_{3D} on the La-effusion cell temperature, T_{La}, (equivalent to La-doping concentration). The record μ value of 70 cm^2/Vs was observed, much like in BSO, at a high n_{3D} of 1.1 × 10^{20} cm^{-3}. At even higher dopant concentrations surpassing the La-

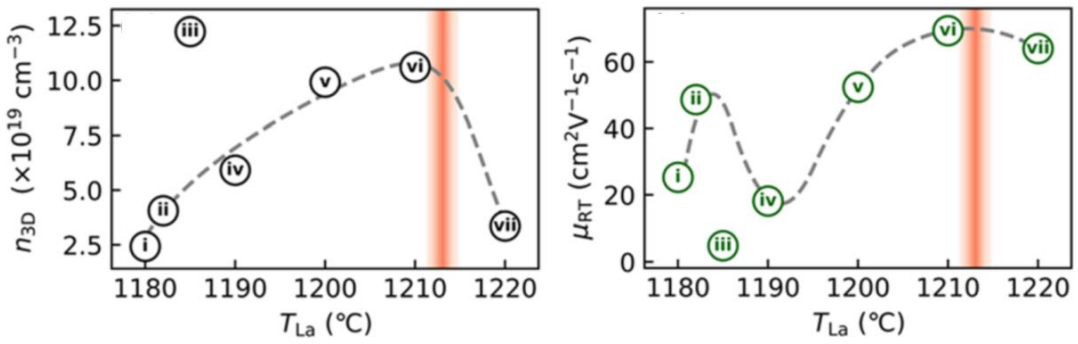

FIGURE 1.12. n_{3D} and Hall mobility in $SrSnO_3$ plotted vs T_{La} Figure adapted from [39].

solubility limit, charge compensation can occur [57], and the μ begins to drop due to increased scattering. A decrease in the μ value with decreasing n_{3D} as in BSO is observed here as well. In BSO thin films, this was attributed to dislocations induced by lattice mismatch between BSO and the substrate. However, in the SSO films which are better lattice matched threading dislocations should be significantly lower and other charged-impurity disorder sources are suspected to cause the observed reduction in μ [39, 54]. A detailed study on the defects and disorder in SSO thin films is lacking which is needed to understand the means to improve the μ in SSO thin films.

n_{3D} lower than 10^{19} cm^{-3} in SSO thin films could not be measured because of an undesirable surface depletion in the films [39]. This surface depletion may also exist in films with higher n_{3D} as well and can have adverse effects on devices fabricated on such films as explained in later chapters. Such surface effects have also been observed in other oxide semiconductors as well [58, 59, 60] but is more pronounced in SSO possibly due to its larger dielectric constant [43, 61]. Surface depletion widths greater than 3 nm have been estimated in SSO thin films. As a result, when determining three-dimensional (3D) carrier densities using the measured two-dimensional sheet carrier densities, one must note that the true 3D carrier densities may be different depending on the surface depletion in the films [39].

1.3 Early Perovskite Oxide Device Results

Early perovskite-based FETs were based on low room-temperature–mobility materials, including STO and $KTaO_3$ [13, 14, 21, 62-66]. The measured μ_{FE} in these devices were less than 5 cm^2/Vs and the mobilities were low even in high-charge density two-dimensional electron gas-based heterostructures, negating the advantage offered by the ability to modulate a large carrier density in the channels [13, 14]. Apart from a low-mobility, oxygen vacancies can also be a cause of concern in STO-based devices [13, 63, 66]. Since the emergence of BSO as a high-mobility material [27], much of the work has been focused on BSO-based FETs [31, 67-70]. In Table 1.2, key early perovskite oxide-based transistor results [13, 14, 21, 31, 62-70] are recorded, where the μ_{FE}, gate length, L_G,

Reference	Publication year	Channel	Mobility, μ_{FE} (cm^2/Vs)	Gate length, L_G (μm)	Trans-conductance, g_m (mS/mm)	Band gap (eV)	Device Type
[21]	2004	$KTaO_3$	0.4	100	0.001	3.8	MOSFET
[13]	2013	$SrTiO_3/GdTiO_3$	5	1	1.75	3.25	HFET
[14]	2014	$SrTiO_3/GdTiO_3$	0.5	1	2.9	3.25	HFET
[62]	2004	La:STO	0.5	50	0.2	3.25	MISFET
[63]	2012	LAO/STO	3.8	4	2	3.25	FET
[64]	2013	LAO/STO	-	400	0.0025	3.25	JFET
[65]	2015	LAO/STO	-	0.06	53	3.25	HFET
[66]	2014	STO	0.4	1.85	5	3.25	MESFET
[31]	2017	BSO-δ	49	50	1	3.1	HFET
[67]	2014	La:BSO	18	140	1.4	3.1	MOSFET
[68]	2015	La:BSO/LIO	90	118	1.4	3.1	HFET
[69]	2015	La:BSO	25	100	0.04	3.1	MOSFET
[70]	2016	La:BSO	97	140	0.2	3.1	MOSFET

TABLE 1.2. Comparison of early perovskite oxide-based FET results.

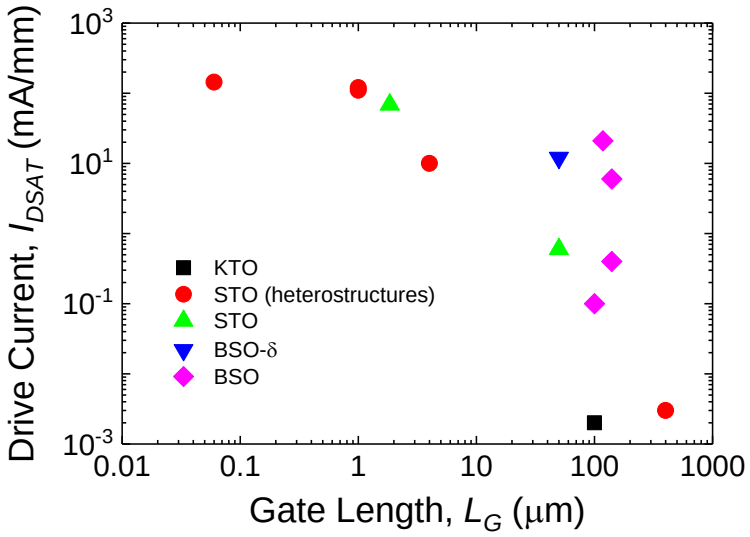

FIGURE 1.13. Drive current obtained from reports of early perovskite oxide FETs [13, 14, 21, 31, 62-70] plotted vs gate length.

transconductance, g_m, the band gap of the semiconducting channel are listed. The maximum μ_{FE} in a BSO-based FET was ~20× of those observed in any STO-based device. The μ_{FE} observed in all the BSO FETs with different configurations were in fact higher than in any

other perovskite oxide material. Consequently, the g_m values in BSO FETs at a comparable L_G are also higher, as can be inferred from Table 1.2.

Figure 1.13 plots the maximum drive currents, I_{DSAT}, in the devices with different channel materials [13, 14, 21, 31, 62-70] vs L_G. The high-charge densities in [13, 14] and the small L_G in [65] allow these devices achieve drive currents in excess of 100 mA/mm. While the drive currents in the BSO-based devices are lower in comparison mainly due to their large L_G, significantly large currents can be achieved in these devices by optimizing the device dimensions. The encouraging early BSO device results indicate huge potential for stannates as semiconducting channel materials. Early stannate-based FETS were based entirely on BSO and there were no SSO-based FET results reported to my knowledge before this work. Apart from one initial report [50], the potential for SSO as a channel material remained latent until the report of hybrid-MBE grown SSO thin films with conveniently controllable doping and moderately high mobilities [38, 54].

1.4 Dissertation Goal

Higher performance requirements have been projected for the electronics that are to drive the future high-speed communication ecosystems. This has compelled researchers to study a newer class of ultra-wide gap (UWG) materials with band gaps wider than that of GaN and SiC, which enable the existing RF-integrated circuits (RFICs) that form the basis of such communication systems.

The preceding sections elucidated the unparalleled edge offered by the multi-functional perovskite oxide system towards development of novel electronic devices. The evaluation of hetero-oxide interfaces for novel functional devices is still a nascent research field but one with vast potential. The unearthing of stannates as high-mobility wide gap semiconductors opens up avenues for researchers to tap the enormous multitude of interesting physical properties within the perovskite oxide family via heterostructure engineering. Among the stannates, BSO is certainly an exciting material with potential for use in several electronic and optoelectronic applications but SSO is perhaps more interesting for high-power and RFIC applications because of its wider band gap (> 4 eV). SSO can be an exciting addition to the emerging UWG-materials-class as it can potentially

have large intrinsic breakdown fields that are essential for such applications. Besides, the smaller lattice constant in SSO can be beneficial for heterostructure growth which can help produce high-current and high-speed transistors. Higher mobilities similar to those that have already been demonstrated in BSO thin films can be achieved in SSO as well.

One of the key insights that I have learned from my research so far is that while exploring novel materials for future electronic applications, one needs to look beyond just their suitability for current needs and instead envision what new applications could eventually be realized. While there are several emerging UWG materials, the distinct advantages enumerated in the earlier discussions make SSO stand out as a uniquely interesting material for next-generation RFICs, and this material is the focus of my dissertation research. As one of the first few device researchers working on SSO thin films, my goal is to overcome the challenges of working with new materials to develop processing methodologies, understand the material properties, experimentally demonstrate the suitability of SSO for FET applications, and lay the foundation for development of next-generation devices using the perovskite family.

Chapter 2

Single-Layer MESFET Results

This chapter reviews the results obtained from transistors fabricated on strontium stannate ($SrSnO_3$ or SSO) thin films grown using hybrid-MBE. All the films used during the course of my dissertation research were grown by the Jalan MBE lab, Department of Chemical Engineering and Materials Science, University of Minnesota, Twin Cities. Working with a new material can involve many challenges as many of the material properties are simply unknown. In the initial phase, I used Sentaurus technology computer-aided design (TCAD) simulations to determine the design specifications and then worked on developing fabrication recipes that led to the demonstration of a first-ever SSO-based FET. The details are presented below.

2.1 MESFET

A metal-semiconductor field-effect transistor (MESFET) is one of the simplest among all the FET structures and involves fewer fabrication complexities compared to metal-oxide-semiconductor FETs (MOSFETs). This prompted me to choose to fabricate SSO MESFETs as it does not require an additional dielectric layer, avoiding unknown complications near the SSO interface, but can still allow evaluation of the channel properties and the processing methodologies of these materials, paving the way for fabrication of more complex FET structures in the future. A MESFET consists of a semiconducting channel controlled by a Schottky gate. Via the application of an electric field in the channel through the Schottky gate, the current flowing through the source and drain (S/D) terminals can be modulated. A schematic of a simple MESFET is shown in

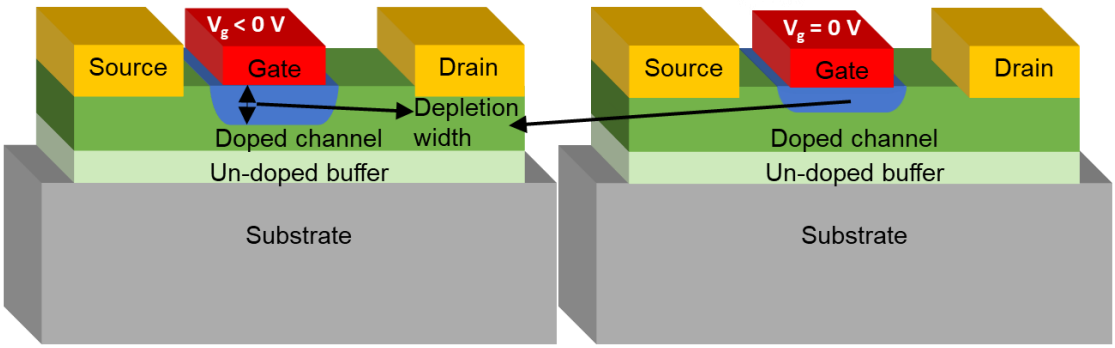

FIGURE 2.1. A schematic of a typical MESFET showing that the depletion width under the Schottky gate can be modulated to change the channel conductivity.

Figure 2.1 highlighting the Schottky gate contact and the S/D Ohmic contacts. Figure 2.1 also shows the change in the effective channel thickness as the depletion region varies with applied gate voltage. In a MESFET, the depletion region created by the semiconductor-Schottky gate interface separates the carrier away from the surface, which can reduce the scattering time of the carriers, resulting in higher field-effect mobility, μ_{FE}, in the MESFET as an added advantage.

2.2 Sentaurus TCAD Simulation

The key design parameters in a MESFET are the doping and the thickness of the channel. As shown in Figure 2.1 the depletion region can be modulated with an applied gate voltage and for a given applied gate voltage, known as the threshold voltage, the channel is completely pinched off. The channel doping and thickness are co-dependent parameters that can be tuned in order to produce an optimal combination that maximizes the drive current while still being able to pinchoff the channel. This was the primary goal of my simulation.

The parameters used in the simulations were determined based on discussions with Jalan MBE lab members, Abhinav Prakash, Tristan K. Truttmann, and Fengdeng Liu. In a Schottky junction, for a n_{3D} > ~10^{18} cm^{-3}, the tunneling leakage current increases exponentially with increasing current [71]. High gate leakage currents are generally unfavorable in a transistor and are detrimental to the device behavior. As a result, n_{3D} >> 10^{19} cm^{-3} are generally avoided in MESFET designs. In films with moderate thicknesses and n_{3D} << 10^{19} cm^{-3}, surface depletion effects which were described in the earlier chapter, tend to make the films very resistive. Very thick films (> 80 nm) were avoided for reasons beyond the scope of this discussion. Based on the discussions with Jalan MBE lab members and their experience from initial success in the growth of SSO films with good quality, films with an n_{3D} close to ~10^{19} cm^{-3} were targeted, and the thickness was kept fixed at ~28 nm. At this thickness, the SSO films grown on $GdScO_3$ (110) tend to be dominantly tetragonal in phase which is favorable for transistors because of the smaller electron effective mass in the films with this phase.

Material	Parameter name	Values
$SrSnO_3$	Electron effective mass	$0.3m_e$
	Hole effective mass	$0.6m_e$
	Dielectric constant	15-30
	Mobility	50 cm^2/Vs
	Band gap	4.3 eV
	Electron Affinity	4.0 eV
	Pt work-function	5.64 eV
	Channel doping concentration	5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}
$GdScO_3$ (Substrate)	Electron effective mass	$0.2m_e$
	Hole effective mass	$0.8m_e$
	Dielectric constant	35
	Mobility	10 cm^2/Vs
	Band gap	5.6 eV
	Electron Affinity	2 eV

TABLE 2.1. Summary of simulation parameters used in SSO MESFET simulations.

In the simulations, an effective mass of $0.3m_e$ and $0.6m_e$ was used for the electrons and holes, respectively. The effective masses for tunneling were assumed to be the same. The dielectric constant of SSO thin films is unknown and was varied in the range of 15-30. The band gap and electron affinity of SSO was assumed to be 4.3 eV and 4 eV [31, 72], respectively. The actual band gap of SSO is not precisely known and the device simulation results would not be impacted by changing the value within the entire known range of band gap for SSO of 4-5 eV. The electron affinity which determines the Schottky barrier height was estimated at a later stage as discussed in this chapter. The work function of Pt was assumed to be 5.64 eV [71] and the S/D contacts were assumed to be purely Ohmic. To calculate the Schottky gate leakage in the simulations, thermionic emission and a non-local barrier tunneling model was used [73]. The channel doping was varied in the range of 5×10^{18} cm^{-3} to 2×10^{19} cm^{-3} for a fixed channel thickness of 28 nm and the channel pinchoff behavior for different doping concentrations was observed. The simulation parameters are summarized in Table 2.1. The simulated device had L_G = 3 μm, source-to-drain spacing = 9 μm, and width of 1 μm.

Figure 2.2 displays the simulation results, where drain current, I_D, is plotted in log-scale as a function of gate-to-source voltage, V_{GS}, for four different doping concentrations, and a

drain-to-source voltage of 5 V.. As can be seen from Figure 2.2, the gate leakage current due to tunneling, dominates the off state I_D for doping greater than 2×10^{19} cm^{-3}. For a channel doping of 5×10^{18} cm^{-3}, the I_D in the off state is close to the thermionic emission limit with no appreciable tunneling current, but this is not an optimal doping for this thickness as the drive current in the on state is too low. Based on these results, an n_{3D} in the range of 1×10^{19} cm^{-3} to 1.5×10^{19} cm^{-3} was targeted during growth for this experiment.

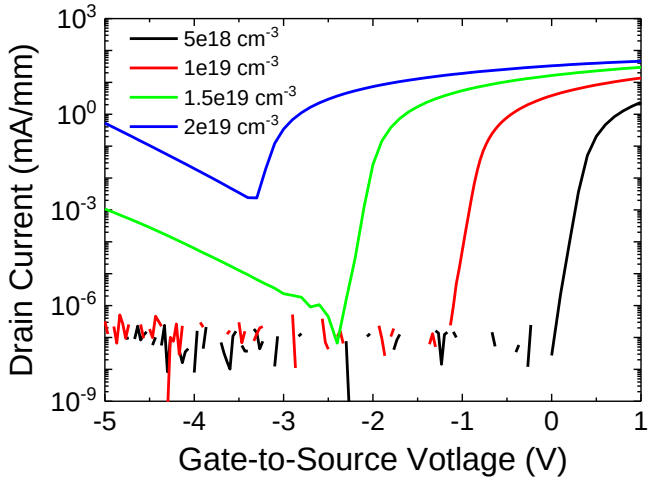

FIGURE 2.2. Simulated transfer characteristics of a MESFET with SSO channel thickness of 28 nm and four different values of channel doping. L_G = 3 μm, source-to-drain spacing = 9 μm. Drain-to-source voltage = 5 V.

2.3 Device Fabrication

The device fabrication sequence started with using radical-based hybrid-MBE to grow epitaxial SSO thin films on a 5 mm × 5 mm, semi-insulating $GdScO_3$ (110) substrate that was commercially purchased. The growth was performed by Abhinav Prakash and Jin Yue from the Jalan MBE lab. SSO is -1.6% lattice mismatched to the substrate $GdScO_3$, which provides a pseudocubic $(001)_{pc}$ perovskite template for the epitaxial growth of SSO. The substrate was heated to a thermocouple temperature 950 ℃ in an MBE chamber with a background of 10^{-10} Torr. The substrate was then cleaned using a 250 W RF O_2 plasma which is also used as the precursor source for O_2 later during the growth. The precursors, Sr and La were supplied via thermal evaporation from an effusion cell, Sn was supplied via the chemical precursor hexamethylditin (HMDT). The details of the growth technique

are explained elsewhere [34, 38, 54]. As explained in the previous chapter, using this hybrid-MBE approach an adsorption-controlled growth regime can be achieved with scalable growth rates and atomically smooth film surfaces [36]. Along these lines, using beam equivalent pressures of 3×10^{-8} Torr for Sr, 2.4×10^{-6} Torr for HMDT, and 5×10^{-6} Torr for O_2 (RF plasma) a stoichiometric condition was achieved for the growth. La was used as an n-type dopant and its concentration in the channel layer was fixed by keeping the effusion cell temperature, T_{La} = 1125 °C. Using these conditions, a thin 11 nm near-intrinsically-doped (NID) buffer layer was first grown on the substrate without providing any La precursor. Then, a 28 nm La:SSO film was grown as the active channel layer. Figure 2.3(a) shows a schematic representation of the as-grown SSO layers on the substrate. From van der Pauw measurements, the as-grown films were known to have an $n_{3D} = 2.3 \times 10^{19}$ cm^{-3}, sheet resistance, R_s = 1.9 kΩ/□, and μ_{Hall} = 50 cm^2/Vs. The carrier concentration was calculated assuming the effective thickness of the film to be the same as that of the doped-film thickness = 28 nm, and the actual carrier concentration could be higher as this value does not account for surface depletion which changes the effective thickness of the film.

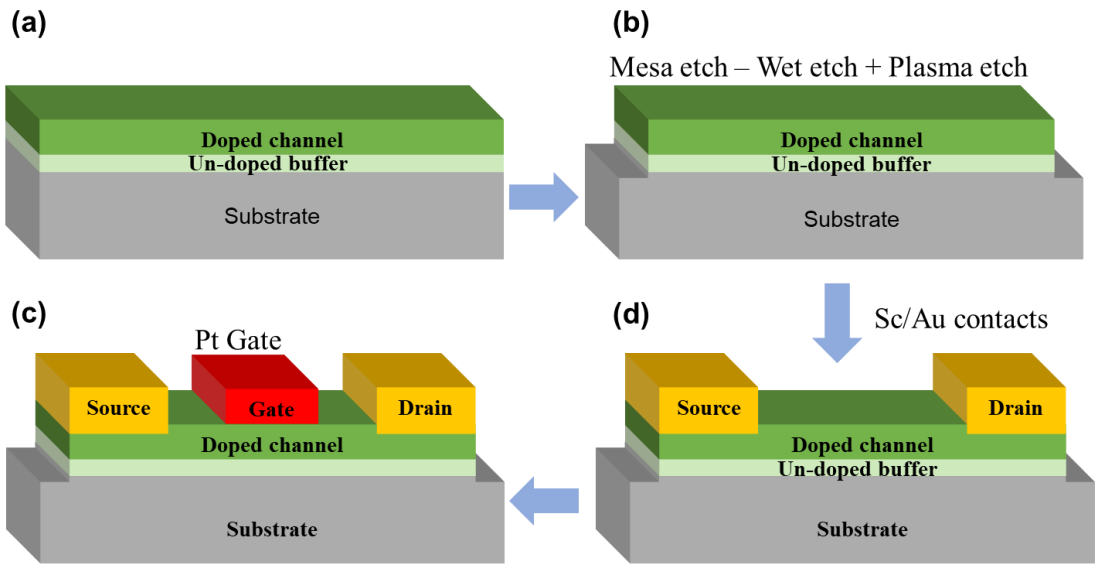

FIGURE 2.3. Fabrication sequence of a MESFET showing (a) as grown film, (b) mesa isolation step, (c) Ohmic contacts deposition, and (d) Schottky gate deposition.

The reminder of the fabrication sequence, which is shown in Figure 2.3, was performed in the Minnesota Nano Center. As shown in Figure 2.3(a)-(d), after the growth, regions outside of the mesa patterns are first etched away to isolate the devices, then source and drain ohmic contacts were deposited, and finally the gate metal was evaporated and lifted off to complete the device structure. The essential details of the process and each of the fabrication steps are discussed below.

2.3.1 Photolithography Process and Alignment Marks

Hard contact exposure was used to perform photolithography in all my fabrications to help achieve features with tight tolerance. A dynamic-dispense spin coating technique was used to form a near-uniform photoresist layer on the substrate. In the dynamic-dispense spin coating process, the substrate, which is attached to the spin chuck via vacuum, was set to spin at a speed of 5000 rpm prior to dispensing the resist. Then using a pipette, one drop of AZ® 1512 photoresist was dispensed close to the center of the substrate and the photoresist solvent was subsequently allowed to evaporate by continuing to spin the substrate for 45 s. The standard static-dispense spin coating process, where the photoresist is dispensed before starting the spinning, was avoided as it results in a prominent edge bead because of the small size and square shape of the substrates. The edge bead, if not avoided, interferes with the contact exposure process and results in poorly exposed features. For

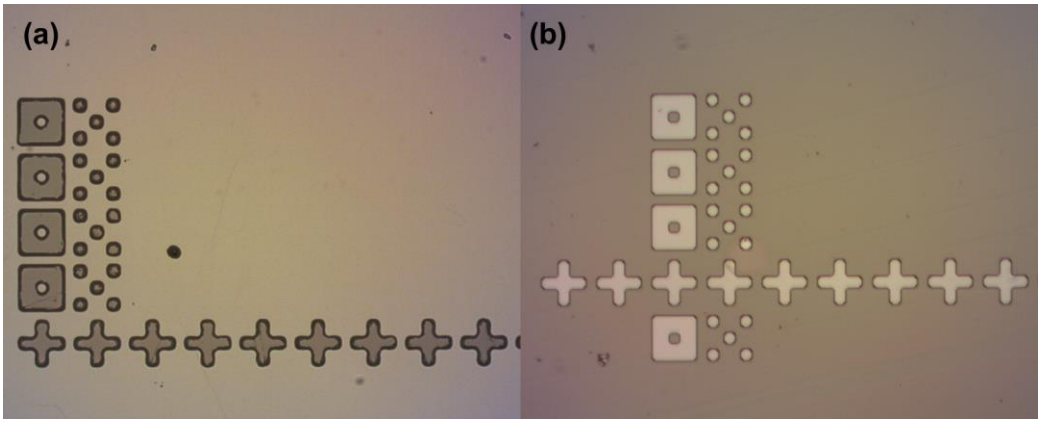

FIGURE 2.4. Optical micrographs of substrates obtained after develop and exposure on a resist film obtained using (a) static dispense spin coating (b) dynamic dispense spin coating techniques, respectively. Same develop time (3.5 min) was used in both cases. The small square features are ~10 × 10 μm^2.

comparison, features obtained after exposure with the same mask using the two different coating techniques are shown in Figure 2.4. Because of a significant edge bead resulting from the static-dispense coating, the features that were supposed to be sharp and rectilinear were blurred and rounded. Owing to the small size and square shape a small edge bead was still present even after dynamic spin coating, because of which the corner features, particularly in patterns away from the center of the sample, were not perfectly sharp even though the features were significantly less rounded in comparison with those obtained using the static coating technique. This edge bead can be removed, if needed, using bead-removal lithography step before pattering in future. For all the photolithography steps, the dynamic-dispense spin coating process described above was used along with a hard contact exposure of 5 s. In order to better clear the resist in the corners despite the slight edge bead, 5.5 s exposure was used in all the subsequent experiments apart from the current one being described. Post-exposure, the features were developed for 30 s in a MF® 351 developer. In photolithography steps where an image reversal of the exposed patterns was performed, the features were developed for 3.5 min using the same developer, after an additional exposure for 8 min under a UV light source.

Since the film and the substrate are transparent, reflective alignment marks were first formed on the substrate in order to be able to align the subsequent layers with each other. For this, after patterning the mark features using photolithography, a Ti (10 nm) / Al (50 nm) metal stack was evaporated and lifted off to form the alignment marks on the substrate.

2.3.2 Mesa Isolation

A wet-etch process was developed to perform the mesa isolation. After initial room temperature trials using hydrochloric acid (HCl) with concentrations ≤ 1M produced no measurable etch depths, etch experiments were performed using 1M HCl heated to 60 °C using a hot plate. The solution was allowed to rest on the hot plate for 30 min before starting any etching in order to stabilize the actual solution temperature. For the purpose of performing etch experiments a sample with similar doping concentrations (T_{La} = 1150 °C) was used. These trials produced an etch rate of ~16.8 nm/min which was calibrated using linear fitting of the data shown in Figure 2.5(a). Short etches produced a sharp edge profile

as can be seen from the AFM graphs in Fig. 2.5(b), which corresponds to an etch of 30 s. If the etching was performed for relatively longer durations, due to isotropic etch and possible resist wicking near the pattern edges, a tapered edge profile was observed in both profilometer and AFM scans which are shown in Fig. 2.5(c) and (d), respectively. The data in 2.5(c) and (d) correspond to an etch duration of 2.5 min. In the actual sample, the mesa

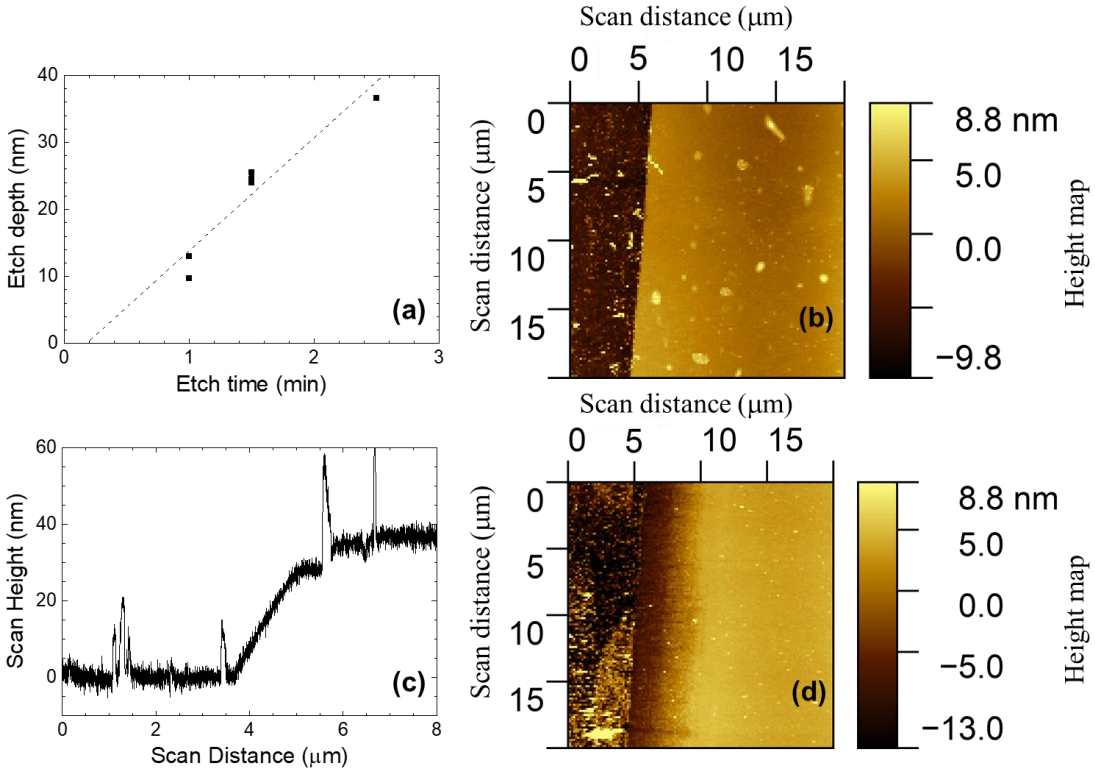

FIGURE 2.5. (a) Etch rate for SSO using 1M HCl at 60 ºC. (b) AFM height map after SSO 30 s etch in HCl. (c) Profilometer scan results after 2.5 min etch in HCl. (d) AFM height map after 2.5 min etch in HCl.

patterns were generated using photolithography and the isolation was performed using a combination of the above described wet etch and dry etch in an Ar plasma for 1.5 min and 10 min, respectively. The total etch depth after this process was measured to be ~47 nm.

2.3.3 Schottky and Ohmic Contacts

The source and drain (S/D) features were patterned and Sc (10 nm) / Au (80 nm) was deposited using electron-beam evaporation to form the S/D contacts. Then, gate features were patterned next using photolithography and Pt (10 nm) / Ti (10 nm) / Al (80 nm) / Ti

(10 nm) was evaporated to form the Pt Schottky gates. An O_2 RF plasma (50 W and 100 sccm O_2 flow) clean was performed for 30 s in both the gate and contact deposition steps just before the metals were evaporated in order to remove any organic residue remaining after the resist development. The evaporation was performed under vacuum conditions and it was ensured that the chamber pressure was always below 1.3×10^{-6} Torr for the entire duration of the deposition.

2.4 Device Measurement Results

All the measurements were obtained at room temperature using a Keysight B1500 semiconductor parameter analyzer.

2.4.1 Transfer-Length Method Results

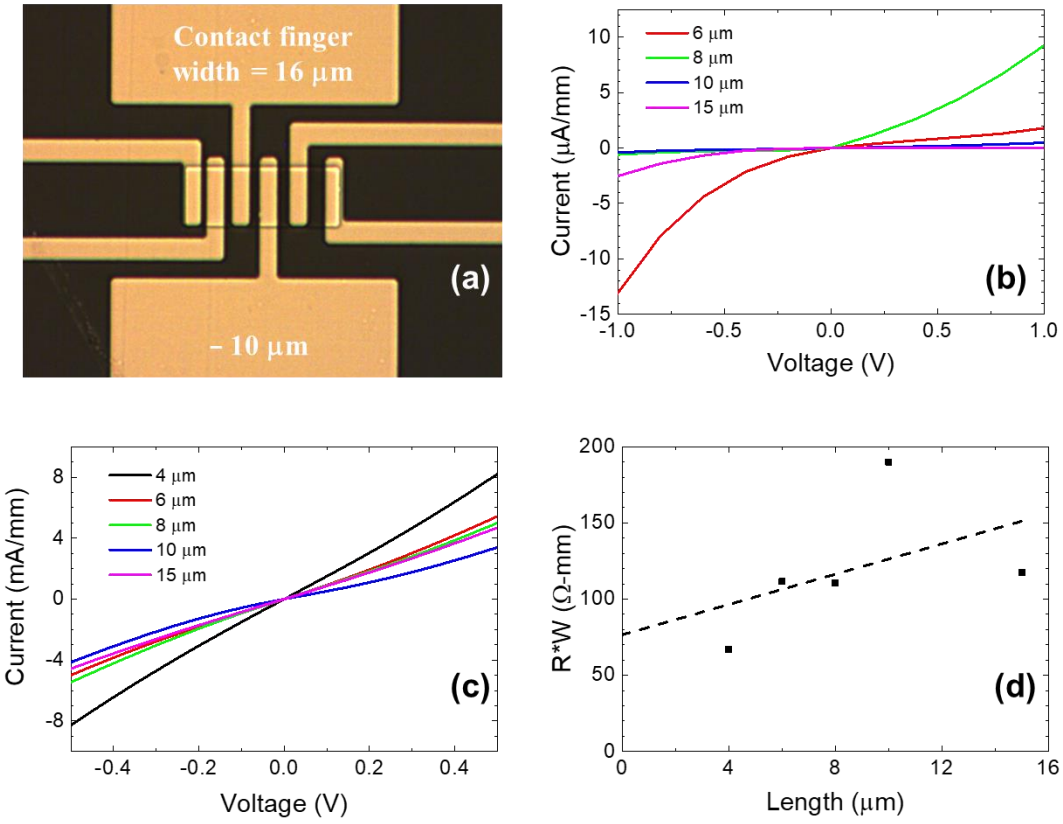

FIGURE 2.6. (a) Optical micrograph of a TLM structure with different contact spacings. (b) Current vs voltage curves of Sc contacts measured at room temperature before annealing. (c) Current vs voltage curves of Sc contacts after 300 ºC annealing. (d) Contact and sheet resistance extraction from the TLM data. Contact spacings of 4, 6, 8, 10, and 15 μm were used.

A picture of the fabricated transfer length structure is shown in Figure 2.6(a). Despite, the low-work function (~3.7 eV) of Sc metal, the contacts were found to be Schottky-type and highly resistive in nature when measured immediately after fabrication. Figure 2.6(b) plots the current as a function of voltage applied between the contact fingers, for different spacings between the fingers. It is suspected that the O_2 plasma clean may have created unintentional surface depletion, in addition to what may be already existing in the films, creating an insulating barrier between the contacts and the underlying La:SSO, and resulting in such resistive contacts.

In an attempt to improve the contacts, the substrate was then annealed in an inert Ar atmosphere for 5 min at a thermocouple temperature of 300 ℃ inside a rapid thermal annealing (RTA) system. The annealing improved the contact resistance by possibly diffusing the Sc contacts and removing the barrier in between. The current-voltage curves obtained from the same TLM structures are shown in Figure 2.6(c). As can be seen from Figure 2.6(c), the contacts show Ohmic behavior after annealing. The resistance data obtained as the inverse of the slope of the IV curves is plotted vs contact separation distance in Figure 2.6(d). The contact resistance, R_c, was extracted by extrapolating the linear fit of the resistance data plotted vs contact spacing that is shown in Figure 2.6(d). However, the extracted R_c = 38 ± 24 Ω-mm had a large error because of the high variability in the contacts. The large error bar caused the extracted sheet resistance, R_s = 4976 ± 5344 Ω/□, obtained as the slope of the linear fit in Figure 2.6(d), to significantly deviate from the values obtained using van der Pauw measurements on the as-grown films.

2.4.2 MESFET Characterization

Figure 2.7(a) and (b) show the schematic and micrograph of a MESFET. The MESFET in Figure 2.7(b) had a L_G = 3 μm, and a S/D spacing, L_{DS} = 9 μm. The output characteristics of this MESFET is shown in Figure 2.8, where the I_D is plotted vs drain-to-source voltage, V_{DS}, for different V_{GS} ranging from -3 V to 1 V, in steps of 0.5 V. The output characteristics of the devices are similar to that of a typical n-FET, showing good saturation and low output conductance. The drive currents of these devices were limited by the relatively-high S/D contact resistance. A maximum extrinsic drive current of 36 mA/mm was measured

for the MESFET at a V_{GS} = +1 V and a V_{DS} = +3.5 V. This was the first-ever demonstration of a SSO-based FET to my knowledge.

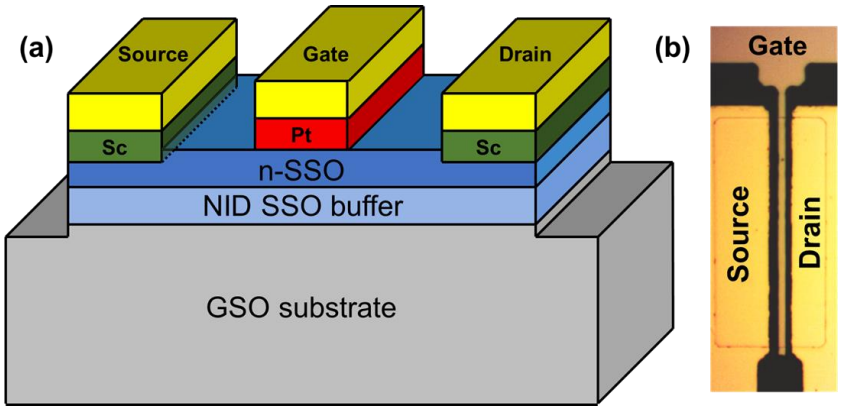

FIGURE 2.7. (a) Schematic of a completed MESFET. (b) Optical micrograph of a MESFET with L_{GS} = 3 μm and L_{DS} = 9 μm [75].

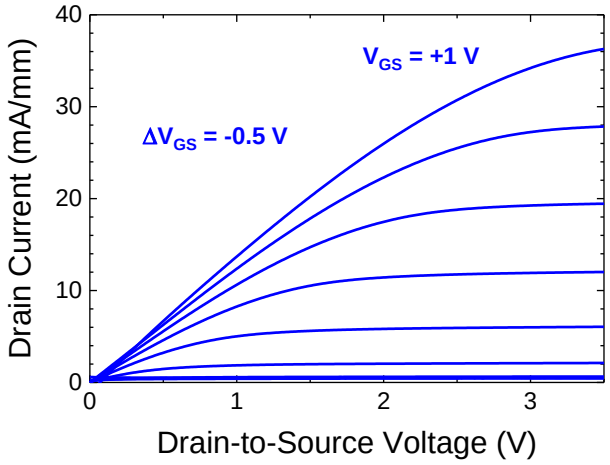

FIGURE 2.8. Output characteristics of a MESFET showing I_D plotted vs V_{DS} for different values of V_{GS} ranging from +1 V to 3 V, in steps of –0.5 V [75]. Devices had L_{GS} = 3 μm and L_{DS} = 9 μm.

Figure 2.9(a) shows the transfer characteristics of the same device, in which the I_D is plotted vs V_{GS}, for a V_{DS} = +3.5 V, a value that biases the MESFET in the saturation region of its operation. The extrinsic transconductance, g_m, of this device is also plotted in the same chart on the right-hand side axis. From this data, the peak g_m was determined to be 17 mS/mm, once again limited by the high-contact resistance, is lower than the actual or intrinsic transconductance, g_{mi}. The g_{mi} can be estimated if the source resistance, R_S, is known, using the equation 2.1:

$$g_{mi} = g_m/(1 - g_m R_S) \tag{2.1}$$

The contact resistance in the devices was estimated to be 30 Ω-mm, using the output characteristics in Figure 2.8 with the help of the known values of R_c and sheet resistance. This resulted in an estimate for g_{mi} = 35 mS/mm. Figure 2.9(b) shows a plot of the $\sqrt{I_D}$ vs V_{GS}, which can be used to extract the threshold voltage, V_T, and the μ_{FE}, based on the equations 2.2 and 2.3 shown below, if the dielectric constant, κ, of SSO is known.

$$I_D = k_n(V_{GS} - V_T)^2, \tag{2.2}$$

where, k_n is known as the conduction parameter of the MESFET and is given by the equation 2.3.

$$k_n = \mu_{FE}\kappa\epsilon_0/2aL_G \tag{2.3}$$

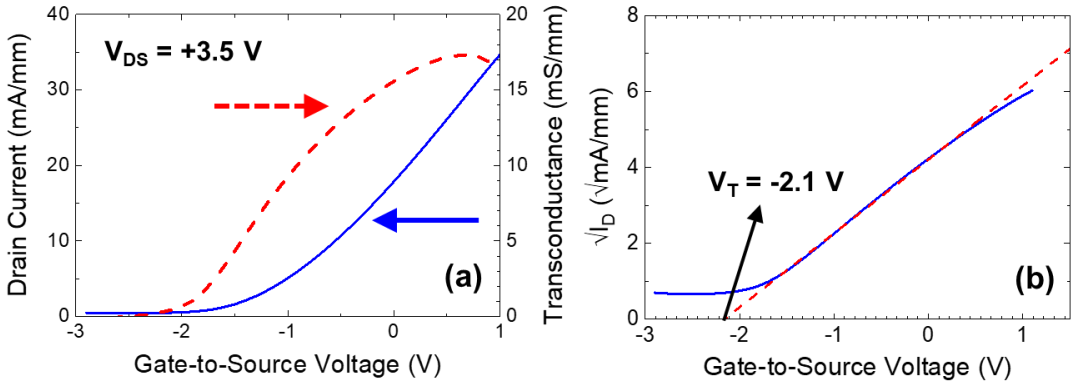

FIGURE 2.9. (a) Transfer characteristics of a MESFET showing I_D plotted vs V_{GS}, for V_{DS} = +3.5 V [75].

The k_n and I_D, used in the equations 2.2 and 2.3 are in units of $SV^{-1}m^{-1}$ and A/m, respectively. The parameter, a, is the thickness of the active layer, i.e. 28 nm. Using these relations, a linear fitting, as shown in Figure 2.9(b), was performed and a V_T = -2.1 Vwas obtained using extrapolation. This can be verified from Figure 2.9(a) where the depletion-mode behavior is also evident. A precise value for the κ of SSO has not been measured so far. Using a value [43, 61], in the range of 15 to 30 for the κ, the μ_{FE} was found to be ranging from 48 to 24 cm^2/Vs, which is a reasonable estimate in comparison with the values obtained from van der Pauw measurements on the as-grown film.

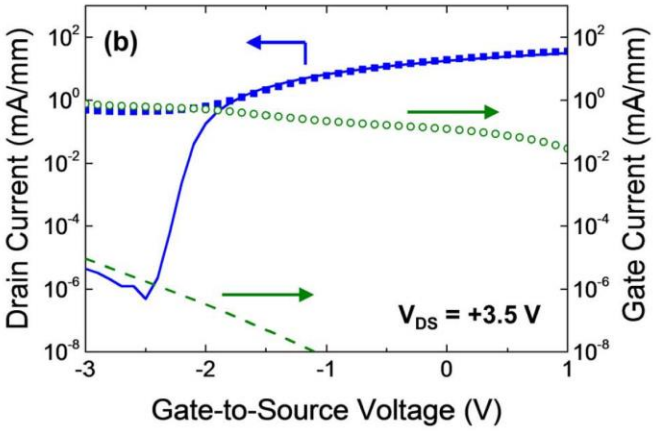

FIGURE 2.10. Experimental (points) and simulated (lines) I_D (blue) and I_G (green) plotted vs. V_{GS}. The results show that the on-to-off current ratio is mainly limited by gate leakage [75].

Figure 2.10 shows the transfer characteristics with I_D plotted on a log scale, from which the off current can be seen to be limited by the gate leakage current. Using the Sentaurus TCAD simulation setup described in the previous sections, the on-state characteristics of the device were fitted to the simulated I_D, using the parameter values of n_{3D}, μ, and κ of SSO as 1.6×10^{19} cm^{-3}, 50 cm^2/Vs, and 30, respectively. The comparison of the simulated and actual off currents in Figure 2.10 indicates that the expected off current is much lower than the actual measured current. The excess leakage current can be attributed to the annealing of the Schottky gates at a moderately high temperature of 300 °C. The non-ideal approach of annealing after the deposition of Schottky gates can be avoided in future to prevent the excessive gate leakage. It must be noted that the simulations assume that the channel is a uniformly doped layer and its entire thickness of 28 nm is modulated by the applied gate voltage. In reality, the existence of surface states could be additionally depleting the channel apart from the Schottky gate and the three-dimensional carrier concentration may be non-uniformly varying with the depth of the channel layer. The real material parameters would then be different from the fitted simulation parameters but should likely be in the vicinity of the values estimated above.

In order to determine the Schottky barrier height of the Pt-SSO junction, capacitance-voltage and current-voltage measurements were performed between the anode and cathode

electrodes of the Schottky junction. The current-voltage characteristics shown in the inset of Figure 2.11 were used to obtain an estimate for the series resistance, which in-turn was used to obtain corrected capacitance, C, and diode voltage, $V_{Schottky}$, values using the method described in [74]. Using a linear extrapolation of the $1/C^2$ vs. $V_{Schottky}$ plots, obtained at 100 kHz, a barrier height of 1.55 eV was extracted. This value is consistent with the measured rectifying forward current characteristics of the Schottky diode. The barrier height for Pt-SSO Schottky junction also confirms the conduction band edge position of SSO, which can be estimated to be at ~4.1 eV. If the κ is known, these plots offer another independent way to verify the doping concentration. Using the range of κ = 15-30 as above, a doping concentration value of 2×10^{19} cm^{-3} to 4×10^{19} cm^{-3} is estimated from the slope of these curves, which is roughly consistent with the value obtained from van der Pauw Hall measurements. The μ_{FE} value was also estimated using the g_{mi} and the C data, which resulted in 16 cm^2/Vs at V_{GS} = +0.8 V to 30 cm^2/Vs at V_{GS} = -0.8 V. The accuracy of this value is reliant on the effective area of the Schottky junction which cannot be precisely determined. As a result, the μ_{FE} extracted from equation 2.3 is likely a more accurate estimation.

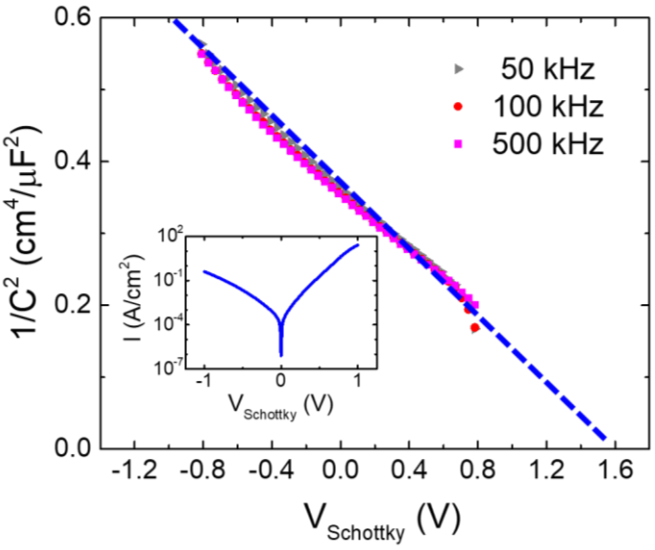

FIGURE 2.11. $1/C^2$ vs. $V_{Schottky}$ plots obtained from capacitance-voltage measurements performed at frequencies of 50 kHz, 100 kHz, and 500 kHz. Inset: Gate current density vs. voltage for the Schottky diode [75].

Finally, the performance of this FET was compared with that of the prior results on STO, BSO, and $KTaO_3$ FET data in Table 1.2. The performance of this FET measured in terms of peak g_m, is higher than any previously reported stannate-based FET owing to the shorter gate length and superior quality of the hybrid-MBE grown SSO films. The peak g_m of our MESFETs is also a roughly 5× improvement over the best STO-based FET at a comparable gate length. The peak g_m values reported in [75] based on my preliminary work was a record value for any perovskite-based FET during the time of the publication. This study also led to estimation of first-ever experimental μ_{FE} in SSO films. Despite the promising peak g_m values in the devices, the μ_{FE} estimated from both methods, seems to be lower than the Hall mobility obtained on the as-grown films. A detailed study is needed to understand the reasons behind the same. The performance improvements demonstrated in SSO FET over any prior perovskite-based FETs is a further evidence to the capability of stannates as channel materials.

2.4.3 Contact and Device Degradation

Although the Sc contacts demonstrated good Ohmic behavior after deposition and annealing, the contacts degraded in air gradually. Based on the learnings from prior measurements performed on SSO films good long-term atmospheric stability is expected for SSO which points to oxidation of the Sc metal as the likely reason for contact

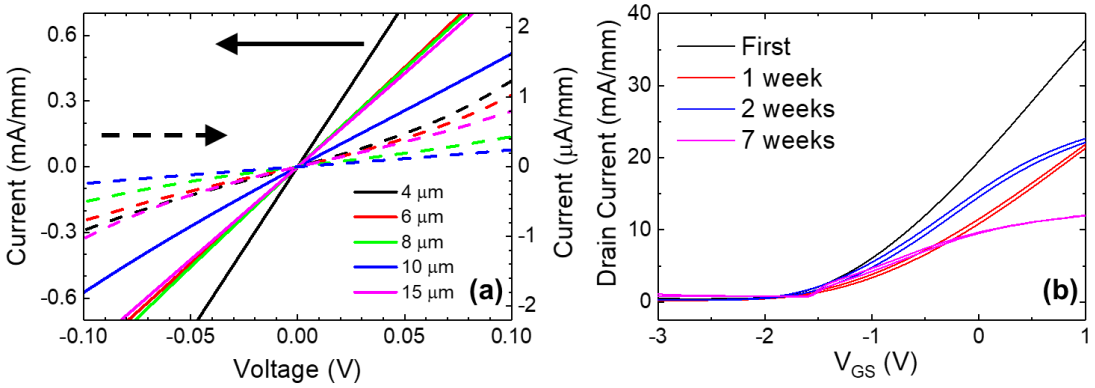

FIGURE 2.12. (a) TLM current vs voltage curves obtained initially (solid lines) compared to those obtained 4 weeks later (dashed). (b) Transfer characteristics measured of the same MESFET (L_{GS} = 3 μm and source-to-drain spacing, L_{DS} = 9 μm) measured over a period a time to device degradation.

degradation. Figure 2.12(a) shows the significantly lower currents measured on the same TLM structures four weeks (dashed lines) after the initial measurements (solid lines) were obtained. The transient behavior of the device discussed above is also compared with the initial measurement in Figure 2.12(b). Here, four different measurements obtained at different times over period seven weeks is shown. Clearly, these contacts are unstable and require significant optimization and the contact resistance obtained in the initial measurement was itself too high. The approach used to address these issues is discussed in the following chapter.

Chapter 3

Ohmic Contact Optimization

The ability to achieve low contact resistances, stable and reliable contacts are vital to any electronic device. A high contact resistance not only prevents the ability to measure and understand intrinsic device properties, as shown in the previous chapter, but can also lead to higher resistive losses and excessive heat dissipation which can in turn degrade the device performance further and can even lead to device failure. Contact resistance has, in some cases, been identified as radio frequency (RF) performance bottlenecks in both active and passive electronic circuit components [76, 77] limiting the achievable maximum operational frequency and quality factor in these devices. The importance of achieving low contact resistance cannot be understated. This chapter outlines the results of the Ohmic contact experiments performed on SSO.

3.1 Band-Edge Work Function Metals

Several approaches have been proposed to form low-resistive Ohmic contacts to semiconductors [71, 78-81]. The easiest approach, in theory, is the use of a contact metal whose work function is the same as or very close to the band edge of the semiconductor, with a band offset of under ~0.025 eV. This can result in very low contact resistances because the active electrons (holes) that are made available by the metal, can then move freely to and from the conduction (valence) band of the semiconductor without having to surpass an energy barrier [71]. However, practical metal-semiconductor interfaces can be non-ideal and due to Fermi-level pinning or simply, lack of a band-edge work function metal can produce finite barrier heights. One alternate approach is the use of a heavily-doped semiconductor beneath a contact metal that minimizes the effect of the energy barrier at the metal-semiconductor junction and causes tunneling to be the dominant conducting mechanism. In the absence of a metal that can produce a low enough barrier, alloyed contacts with engineered work functions may also be used. Both these approaches have been used in Si as well as in GaN, where metal-silicide alloyed contacts on heavily implanted Si [80] and Ta, Ti, Al, or Ni-based alloys have been used on regrown GaN layers [78, 79] to produce record low contact resistances for those materials systems. Another unique approach was used on InP semiconducting layers, where the metal deposition was carried out *in situ* immediately after the growth of the underlying film in an MBE chamber

avoiding exposure of the film to air. This process ensures a clean interface, free of contaminants, prevents surface oxidation and produced low-contact resistance that helped achieve THz operation in InP-based devices [81].

Alloyed Al-based contacts have been previously explored on perovskite oxide semiconductors, including $KTaO_3$ and $SrTiO_3$ [82]. However, because they are a relatively new material system no such contact studies exist on the stannates. This is the first study on Ohmic contacts to any perovskite stannates, to our knowledge. In this study, we attempt to exploit one of the key features of the stannates that was discussed in the first chapter, viz. the capability of achieving high mobilities at a relatively-high doping level of up to ~10^{20} cm^{-3}. The high doping levels and the high mobility can be exploited to produce low contact resistance by using a low-barrier metal that can lead to tunneling band-edge contacts. The low effective mass in the stannates can allow for high tunneling probabilities, and thus lower contact resistance than other materials with relatively higher effective masses.

From the study described in the previous chapter, the electron affinity or conduction band-edge of SSO was found to be at roughly ~4.1 eV. During initial experiments, Cr contacts were explored on an SSO thin film with thickness of 28 nm and carrier concentration of 2.3×10^{19} cm^{-3}. These contacts were highly resistive and also Schottky type in nature as shown in Figure 3.1. The barrier height for Cr contacts is expected to be ~0.4 eV assuming the above electron affinity for SSO and a work function of 4.5 eV for Cr. Even though the

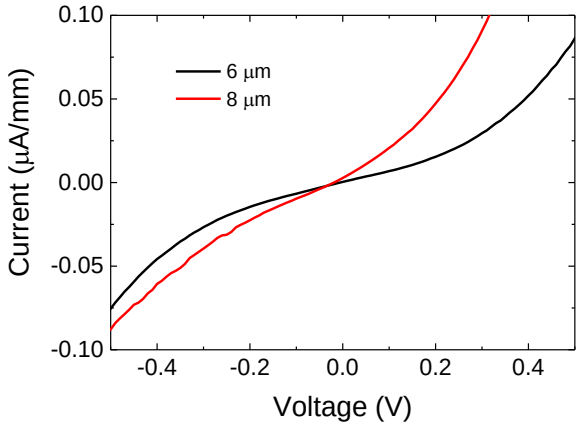

FIGURE 3.1. Current vs voltage curves obtained for Cr contacts to SSO showing high resistivity and Schottky type behavior when measured at room temperature.

barrier height was not too large, these contacts conducted much smaller currents when the as-fabricated structures were measured at room temperature, without any annealing. This is a surprising result and is a good example of the non-idealities associated with metal-semiconductor interfaces that can create contact-conductivity issues. The Sc contacts, whose performance was detailed in the previous chapter, displayed strong Ohmic behavior when measured immediately after annealing at 300 ℃. The low work function of Sc, which is expected to be ~3.7 eV, could be the reason the Ohmic behavior observed in these contacts. Based on the above insights, an experiment was designed where metals with low-work functions namely, Sc (3.7 eV), Mn (4.1 eV), and Ti (4.3 eV) were explored as contact metals on a heavily doped n^{+}-SSO film. In order to measure the true contact resistance attainable by each of these metals and protect the metal layers from oxidation, especially Sc and Mn which can be readily oxidized in air, the samples were passivated with an aluminum oxide layer immediately after liftoff as described in the later sections. This was an initial contact study that helped identify the best candidate metal for contacts to n:SSO.

These learnings were then translated to an ensuing contact study on a bi-layer film structure that is more suitable for FETs. The bi-layer structure consists of a heavily doped SSO capping layer on top of an SSO channel layer, which is doped according to FET design specifications. The capping layer allows for low contact resistance by virtue of its higher doping, while the channel layer can have a lower doping that is preferable in order to be able to achieve complete channel pinch off in the off state. Additionally, a single-layer film

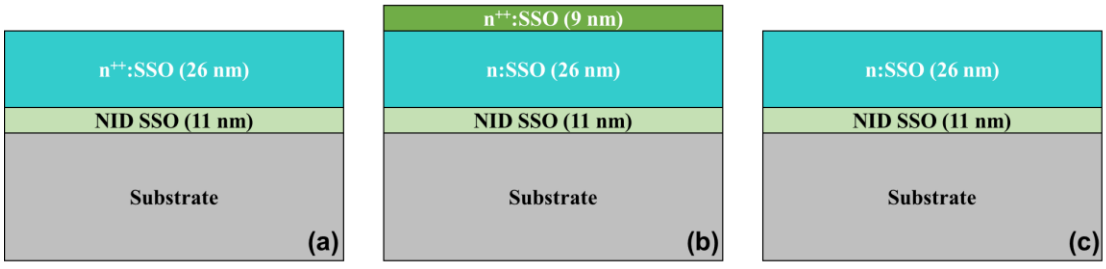

FIGURE 3.2. (a) Heavily doped SSO film used for initial contact study to identify metals suitable to form low-resistive Ohmic contacts to SSO. (b) A bi-layer film that consists of heavily doped capping layer and a channel layer. (c) A single-layer film used as a control sample along with the bi-layer film. The bi-layer film is more suitable for FET applications, to perform another experiment to study the effect of the capping layer.

with similar doping as in the active layer of the bi-layer structure was used as a control sample in this auxiliary contact experiment to demonstrate the benefit of using the capping layer. Figure 3.2 depicts film structures of all the three films used to perform the contact studies.

3.2 Transfer-length Method Structures Fabrication

Using a growth procedure similar to that described in the previous chapter, all the films used here were grown on a semi-insulating $GdScO_3$ substrate. The Nd was supplied as the dopant atom using an effusion cell kept at 940 °C during the active layer growth. These films were grown by Tristan K. Truttmann and Fengdeng Liu and consisted of a 10 nm near-intrinsically-doped (NID) SSO buffer layer, and a 26 nm Nd^{++}:SSO active layer on top. Van der Pauw measurements performed on the as-grown films yielded a high n_{3D} = 3.5×10^{19} cm^{-3}, μ_{Hall} = 37 cm^2/Vs, and a R_s = 1874 Ω/□. From here on, this film will be referred to as the "*SSO_heavy*" film for the sake of clarity and convenience.

The bi-layer sample used in the additional contact experiment (Figure 3.2), consisted of a 10 nm NID SSO buffer layer, a 26 nm Nd:SSO layer grown by setting the Nd effusion cell temperature at 915 °C, and a 9 nm Nd^{++}:SSO capping layer grown with the Nd effusion cell temperature at 950 °C. The single-layer sample, used as a control sample, was grown using the exact same conditions as in the bi-layer sample growth but without a capping layer. The bi- and single-layer films will be referred to by using the names, "*SSO_bilayer*" and "*SSO_control*," respectively. While the properties of as-grown *SSO_bilayer* film were not measured, the *SSO_control* film was found to have a n_{3D} = 2.3×10^{19} cm^{-3}, μ_{Hall} = 27 cm^2/Vs, and a R_s = 3845 Ω/□. The properties of all the three films used here are summarized in Table 3.1.

In order to fabricate the structures for the transfer-length method (TLM) measurements on the *SSO_heavy* films, a fabrication procedure similar to the one described in Chapter 2 was used. The fabrication sequence consisted of a series of steps, namely alignment mark deposition, mesa isolation, Ohmic contact deposition, contact passivation with Al_2O_3,

Sample	Film thickness	Carrier Conc. (cm^{-3})	Sheet resistance (W/□)	Mobility (cm^2/Vs)
SSO_heavy	11 nm NID SSO + 26 nm channel	3.5×10^{19}	1874	37
SSO_control	11 nm NID SSO + 26 nm channel	2.3×10^{19}	3845	27
SSO_bilayer	11 nm NID SSO + 26 nm channel + 9 nm capping	Channel – Expected to be similar to SSO_control Capping – Expected to be similar to or > SSO_heavy	Unknown	Unknown

TABLE 3.1. Summary of properties of the films used for contact studies.

Al_2O_3 etch to create pad openings, and annealing. The first three steps are only briefly described here because of close resemblance to methods described in Chapter 2. For the alignment marks, Ti (10 nm) / Au (100 nm) were used after patterning with electron beam lithography. The mesa isolation was performed using Ar plasma for 18 min and electron beam lithography patterning to achieve an etch depth of 58 nm. Electron beam lithography was used to pattern the Ohmic contact features to achieve tightly packed features. For the Ohmics, Sc (55 nm) / Ti (10 nm) / Au (50 nm) were used for Sc contacts, while Mn (55 nm) / Ti (10 nm) / Au (50 nm), and Ti (65 nm) / Au (50 nm) were used for Mn and Ti contacts respectively[1]. Shortly before depositing the Ohmic contacts, the patterned regions were cleared of any surface residue by using a dry etch for 30 s in O_2 plasma (RF power =

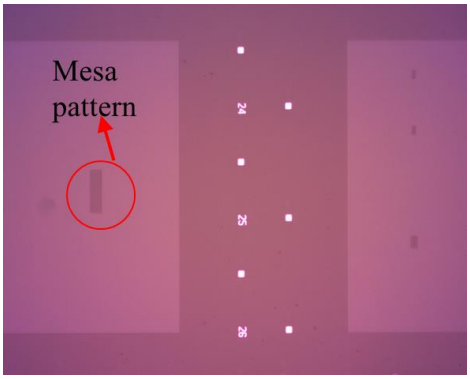

Figure 3.3. Optical micrograph showing patterns after mesa isolation etch and some alignment marks. The square alignment marks are of the size 20 × 20 μm^2.

[1]*In a separate initial trial, Al contacts consisting of Al (55 nm) / Ti (10 nm) / Au (50 nm), were also used but the lift-off yield was low. The reason for this low lift-off yield was unknown. The Al-contact experiment was not repeated because the structures resulted in highly resistive contacts when measured at room-temperature. Effect of annealing could not be tested.*

50 W) first and then in Ar plasma for 45 s. This O_2 plasma clean and Ar dry etch cleaning process ensures a clean interface between the contact metals and SSO. The remaining fabrication steps performed on the *SSO_heavy* films are described in slightly more detail in the following sub-sections. Figure 3.3 consists of optical micrographs obtained after mesa isolation showing some patterned mesa regions and alignment marks.

3.2.1 Contact Passivation and Annealing

In order to prevent the oxidation of contact metals, particularly in view of the degradation observed in prior Sc-based contacts, the contacts were immediately passivated after liftoff with a 500-cycle-thick Al_2O_3 layer that was deposited using the atomic layer deposition (ALD) technique. ALD technique can produce films with high-conformality and Al_2O_3 films and coatings are commonly used and known to act as a moisture barrier [83]. Water vapor and trimethylaluminum were used as precursors for the ALD deposition, with respective precursor pulse durations of 0.015 and 0.4 s. The chamber was stabilized to a temperature of 200 °C for the duration of the deposition. On a control SiO_2 substrate, the ALD thickness was verified using an ellipsometer to be ~53 nm, assuming a refractive index of 1.7 for Al_2O_3.

The Al_2O_3 film must be etched away in the pad areas so as to allow the probes to make electrical contact with the metal pads while performing measurements. For this step, openings in PMMA resist were patterned using electron beam lithography and reactive ion etch in the presence of 22 sccm BCl_3 and 5 sccm Ar, using an RF power of 50 W was used to etch the Al_2O_3. It is not recommended to not use 10:1 buffered oxide etchant (BOE) to etch Al_2O_3 while using PMMA as a resist, as in earlier attempts, BOE was found to liftoff the PMMA. Further, the BOE also proceeded to attack the Al_2O_3 and SSO aggressively even with short etch times.

Another pitfall that can occur while exposing pad areas with an electron beam is substrate charging. Figure 3.4 shows images obtained after the pad opening exposure step. The substrates commonly used for perovskite growth are ultra-wide gap substrates that are highly insulating. In the absence of a good conduction path for the electrons bombarding the PMMA, in some cases it was observed that the electrons can find a conduction path

through the contact metal lines or the doped SSO. As a result, when a large electrical current flows through narrow channels, the heat generated due to the current flow can bake the PMMA causing it to intermix with the sputtered Au layer on top of the PMMA. In some case this may even damage the channel as shown in Figure 3.4. The optical micrographs in Figure 3.4 indicate the PMMA may be outgassing and mixing with the Au. Some substrate damage near narrow channels can also be seen. From prior fabrication runs involving similar pad-area electron beam exposure, it was understood that when the contacts were highly resistive this problem was significantly less evident when observed under the micrograph and substrate damage did not occur at all. This clearly points to current conduction issues which can be resolved by use of conductive polymer films (aquaSAVE™) on top of the PMMA resist that can provide an alternate current path.

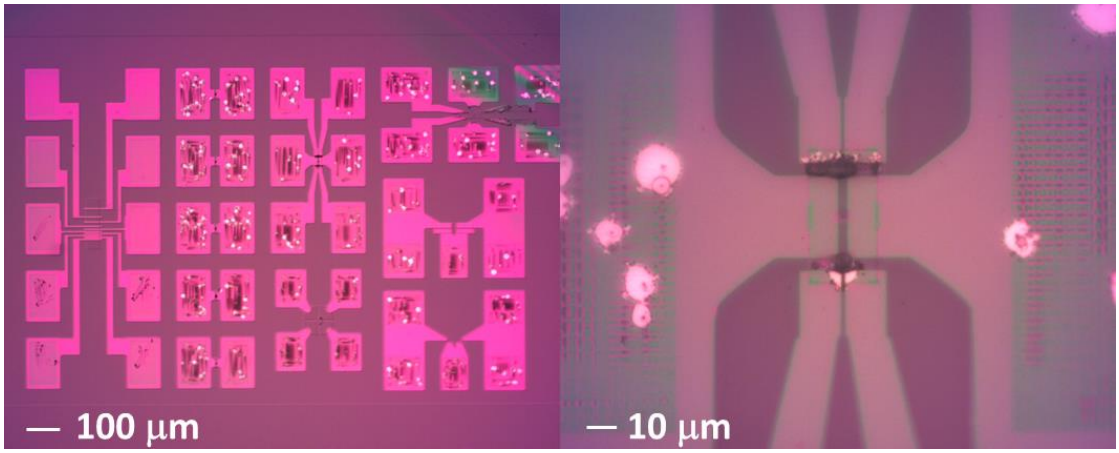

Figure 3.4. Optical micrographs showing atypical artifacts observed after electron beam lithography exposure (before develop step). (a)-(b) Au migration, PMMA outgassing, pad damage, and (b) damage to substrate and PMMA near very thin channels can be seen.

A 300 ℃ annealing in Ar atmosphere for 5 min was also performed on the *SSO_heavy* films. However, due to the stress in the Al_2O_3 layer, some of the large metal structures buckled and collapsed. Also, annealing at temperatures slightly higher than 300 ℃ led to outgassing which could be observed under the microscope. The outgassing was believed to be related to organic residue trapped underneath the Al_2O_3 layer and caused visible deformities that rendered the devices inoperable. An optical micrograph obtained before and after a 350 ℃ annealing on the *SSO_heavy* substrate with exactly same lighting

conditions is shown in Figure 3.5. The Au appears to have disappeared possibly due to stress-related buckling failure. For these reasons, thinner ALD passivation layers should be used in the future which can lower the stress and also allow holes in the passivation layers around the resist residue facilitating its escape. Measurements were only possible with annealing up to 300 ºC as a result of this pad failure.

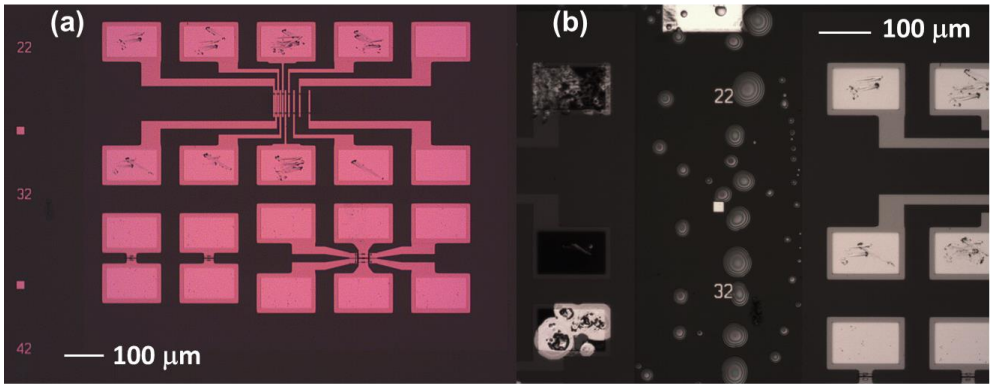

Figure 3.5. Optical micrographs showing substrate in the vicinity of the same patterns (a) before (b) after 350 ºC annealing. Contrast change is likely due to Au disappearing during 350 ºC anneal. Outgassing of resist can also be seen after 350 ºC annealing.

The fabrication sequences on the *SSO_bilayer* and *SSO_control* films, where only Ti-contacts were used, were mostly similar, and the few deviations are not relevant to the context of the current chapter. A discussion on the fabrication is thus deferred to the next chapter where it is more relevant and only the pertinent TLM results are discussed here in the following sections. Figure 3.6 illustrates all the different layers present post-fabrication on each of the three samples namely, *SSO_heavy*, *SSO_bilayer*, and *SSO_control*. The measurement results obtained on each of the films are discussed next.

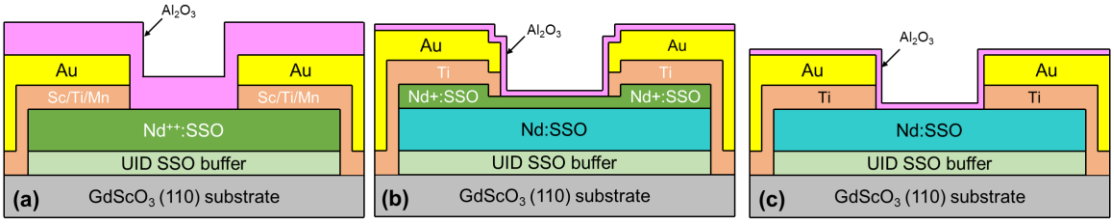

Figure 3.6. Schematic showing the layers post-fabrication on (a) *SSO_heavy*, (b) *SSO_bilayer*, and (c) *SSO_control* films. Sc, Mn, and Ti contacts were used on *SSO_heavy*, whereas only Ti contacts were used on the other two films.

3.3 Measurement Results

3.3.1 Comparison of Sc-, Mn-, and Ti-contacts

Figure 3.7(a) displays the TLM structures fabricated on *SSO_heavy* substrates. Features with spacings < 0.6 μm were not considered for measurements because of a suspected short. The current vs voltage curves obtained from the TLM structures based on Ti-, Mn-, and Sc-contacts are shown in Figure 3.7(b), (c), and (d), respectively. All three contact metals show strong Ohmic behavior. These measurements were obtained after the ALD Al_2O_3 deposition which was a ~1 hr long process while the substrate was continuously heated at 200 °C. Thus, the ALD deposition can be considered as a contact passivation as well as an annealing step. Based on the prior results shown in Chapter 2, the Sc contacts are not expected to show Ohmic behavior when measured at room temperature before any annealing. Other independent experiments also suggested that Ti and Mn contacts also tend

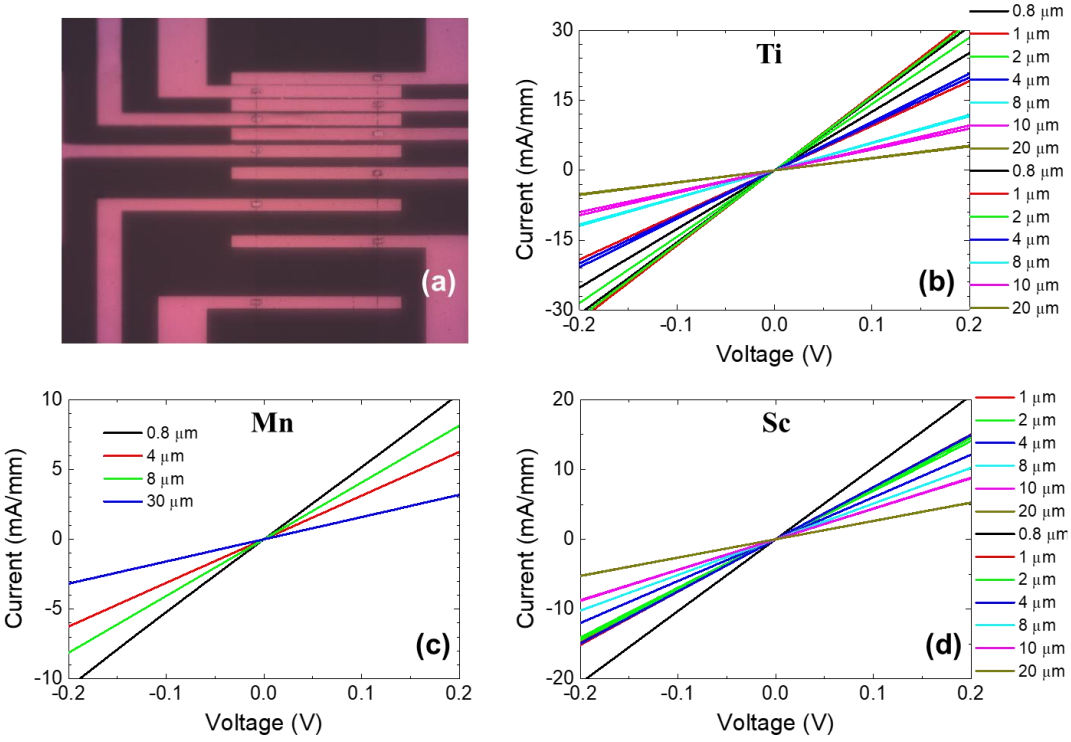

Figure 3.7. (a) Optical micrograph of TLM structures fabricated on *SSO_heavy* substrate with a contact finger width = 5 μm. Current vs voltage curves obtained from TLM structures corresponding to (b) Ti-contacts, (c) Mn-contacts, and (d) Sc-contacts, after ALD passivation.

to produce contacts with high and variable resistances, when measured before any annealing. This supports the theory that the ALD step not only passivates but also anneals the contacts. Another observation from Figure 3.7 is that the Ti contacts seem to be conducting the highest current at a given applied voltage for any given spacing between the contacts.

In order to extract the contact resistance and transfer lengths for each contact metallization, the resistances, normalized to width, extracted for different spacings between the contact fingers are plotted in Figure 3.8(a) vs the length of the spacing between the contacts. Clearly, while all three metals produce good contact performance, the Ti-contacts seem to provide the lowest contact resistance with the least variation. The contact resistances were extracted as 2.4 ± 0.3 Ω-mm, 9.8 ± 2.3 Ω-mm, and 5.2 ± 0.3 Ω-mm for Ti-, Mn-, and Sc-contacts, respectively. The corresponding sheet resistances were determined to be 1655 ±

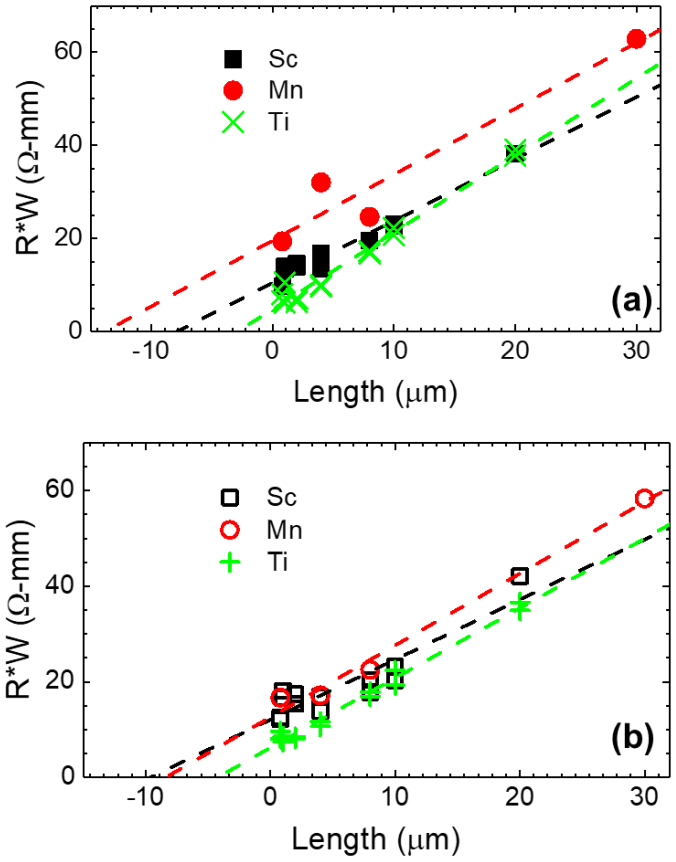

Figure 3.8. Contact resistance extraction for Sc-, Mn-, and Ti-contacts on *SSO_heavy* films after (a) ALD passivation and (b) 300 ºC forming gas anneal.

71 Ω/□, 1417 ± 290 Ω/□, and 1331 ± 69 Ω/□, which are lower than but close to those obtained from as-grown film values (Table 3.1). The small reduction in the sheet resistance could be due to passivation of surface states by the Al_2O_3 which could make more carriers available in the channel. The transfer-lengths obtained from Figure 3.8(a) were 1.4 μm, 6.9 μm, and 3.6 μm for Ti-, Mn-, and Sc-contacts, respectively. From this, the corresponding specific resistivity data calculated for the three metals were 34 ± 6 μΩ–cm^2, 490 ± 115 μΩ–cm^2, and 187 ± 23 μΩ–cm^2, respectively. The actual width of the contact figure was 5 μm, which was used to calculate the specific resistivity for Mn-contacts because the extracted transfer length was greater than the contact width itself for this case. The smallest transfer length obtained for Ti-contacts also point to these contacts being superior in comparison to the Sc- and Mn-contacts.

The transfer-length data obtained after 300 °C annealing is shown in Figure 3.8(b) and the corresponding contact resistance, sheet resistance, and specific resistivity obtained for all three metals at both these temperatures is summarized in Table 3.2. The contact resistance obtained for Ti-contacts is a ~15× improved over the previous value obtained using Sc contacts. The Sc-contacts itself registered a ~5× improvement which can be attributed to the protective passivation layer which prevented any further oxidation of Sc-contacts. The

Contact metal	**200 °C**			
	R_c (Ω-mm)	**R_s (Ω/□)**	**Transfer Length (μm)**	**R_{sp} (μΩ-cm^2)**
Sc	5.2 ± 0.3	1331 ± 69	3.6 ± 0.4	187 ± 23
Mn	9.8 ± 2.3	1417 ± 290	6.9 ± 2.8	490 ± 115
Ti	2.4 ± 0.3	1655 ± 71	1.4 ± 0.2	34 ± 6
	300 °C			
	R_c (Ω-mm)	**R_s (Ω/□)**	**Transfer Length (μm)**	**R_{sp} (μΩ-cm^2)**
Sc	6.0 ± 0.6	1257 ± 132	4.8 ± 0.9	288 ± 61
Mn	6.3 ± 0.9	1503 ± 121	4.2 ± 0.9	265 ± 69
Ti	3.1 ± 0.2	1460 ± 50	2.1 ± 0.2	65 ± 7

TABLE 3.2. Summary of transfer-length method data obtained for Sc-, Mn-, and Ti-contacts on *SSO_heavy* film.

Ti-contacts also produced the least variable contact resistance values along with the smallest transfer-length among the three metals. Based on the electron affinity value of 4.1 eV for SSO, the Sc (work function = 3.7 eV) and Mn (work function = 4.1 eV) likely formed band-edge contacts while the Ti-metallization formed tunneling contacts. The resistivities values of pure Sc, Mn, and Ti metals obtained from [84] are 0.55, 1.6, 0.4 μΩ-m, suggesting that Ti may be supplying a larger number of active carriers for tunneling through the contact. Theoretical calculations suggest that Mn metal should have higher number of active carriers than in Ti, but the actual carrier density in the contact metals can vary based on the purity of the deposited films. All three metals can get oxidized during deposition and the presence of small amounts of oxygen during the deposition could cause a reaction with these metals within the evaporation chamber. Also, the Sc, Ti, and Mn evaporation sources were not stored in vacuum continuously and could be partially contaminated with oxygen as well. A detailed study is required in order to understand the actual contact-conduction mechanism and the above explanation is offered as a preliminary hypothesis.

3.3.2 Comparison of Ti-contacts on Single- and Bi-layer Films

The Ti-contacts exhibit lowest contact resistance to SSO on heavily doped films, among the metalizations tested so far. In an auxiliary experiment, the Ti-contacts were compared to understand the dependence on the doping in the film. As explained earlier, the *SSO_control* film does not have any heavily doped capping layer and is the control sample. The *SSO_bilayer* film on the other hand has a heavily doped capping layer on top of an active layer with the same doping as in *SSO_control*. For the *SSO_control* and *SSO_bilayer* films, annealing up to 300 ℃ was performed first and then both the films were passivated with ALD Al_2O_3. The ALD passivation was performed after the 300 ℃ annealing step because the Ti-contacts are relatively less prone to oxidation than the Sc-contacts and allows the study of the effect of the passivation on the contacts.

A comparison of the transfer-length data obtained on the two films after a 300 ℃ and after the subsequent ALD passivation is shown in Figure 3.9. Clearly, the *SSO_bilayer* provides

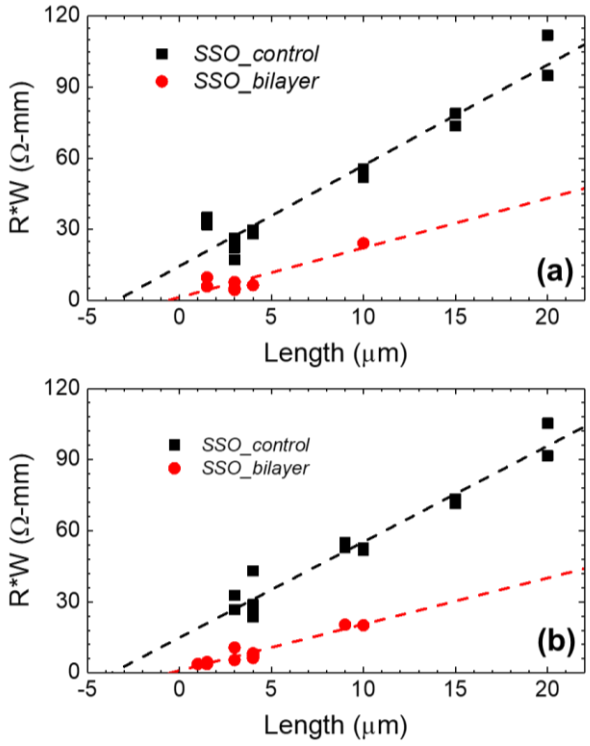

FIGURE 3.9. Contact resistance extraction for Ti-contacts on *SSO_bilayer* and *SSO_control* films obtained after (a) 300 ℃ and (b) ALD passivation.

much lower resistance at each spacing length. The extracted contact resistance, specific resistivity, and the transfer-lengths obtained on the two films are summarized in Table 3.3. The error bar for the data obtained on *SSO_bilayer* films is high, partly because the actual contact resistances are very small. Despite the error bar the advantage of using the bi-layer

Film	**300 °C**			
	R_c (Ω-mm)	**R_s (Ω/□)**	**Transfer Length (μm)**	**R_{sp} (μΩ-cm²)**
SSO_control	7.3 ± 1.6	4247 ± 307	1.7 ± 0.5	124 ± 46
SSO_bilayer	0.7 ± 1.1	2089 ± 486	0.3 ± 0.6	2 ± 8
	Al_2O_3 passivation			
	R_c (Ω-mm)	**R_s (Ω/□)**	**Transfer Length (μm)**	**R_{sp} (μΩ-cm²)**
SSO_control	7.4 ± 1.3	4045 ± 250	1.8 ± 0.4	133 ± 38
SSO_bilayer	0.5 ± 0.5	1953 ± 212	0.2 ± 0.3	1 ± 2

TABLE 3.3. Summary of transfer-length method data obtained for Ti-contacts on *SSO_control* and *SSO_bilayer* films.

structure is obvious from Figure 3.9 and data in Table 3.3. The low specific resistivities achievable using SSO is a promising aspect for future RF applications.

Prior to the 300 ℃ anneal, the dependence of temperature on Ti-contacts was studied on each of the two samples. After obtaining room-temperature TLM measurements, measurements were also obtained after liftoff, 150 ℃, and 225 ℃ anneals as well. The data for the 300 ℃ was already shown in Figure 3.9. Figure 3.10 shows the TLM data obtained for the room-temperature (no annealing) and the remaining two temperatures namely, 150 ℃ and 225 ℃. The contacts were found to be highly resistive irrespective of the substrate doping even after the 150 ℃ annealing, while the contacts on *SSO_bilayer* films seemed to improve only after a 300 ℃, suggesting a 225-300 ℃ annealing as a crossover point for

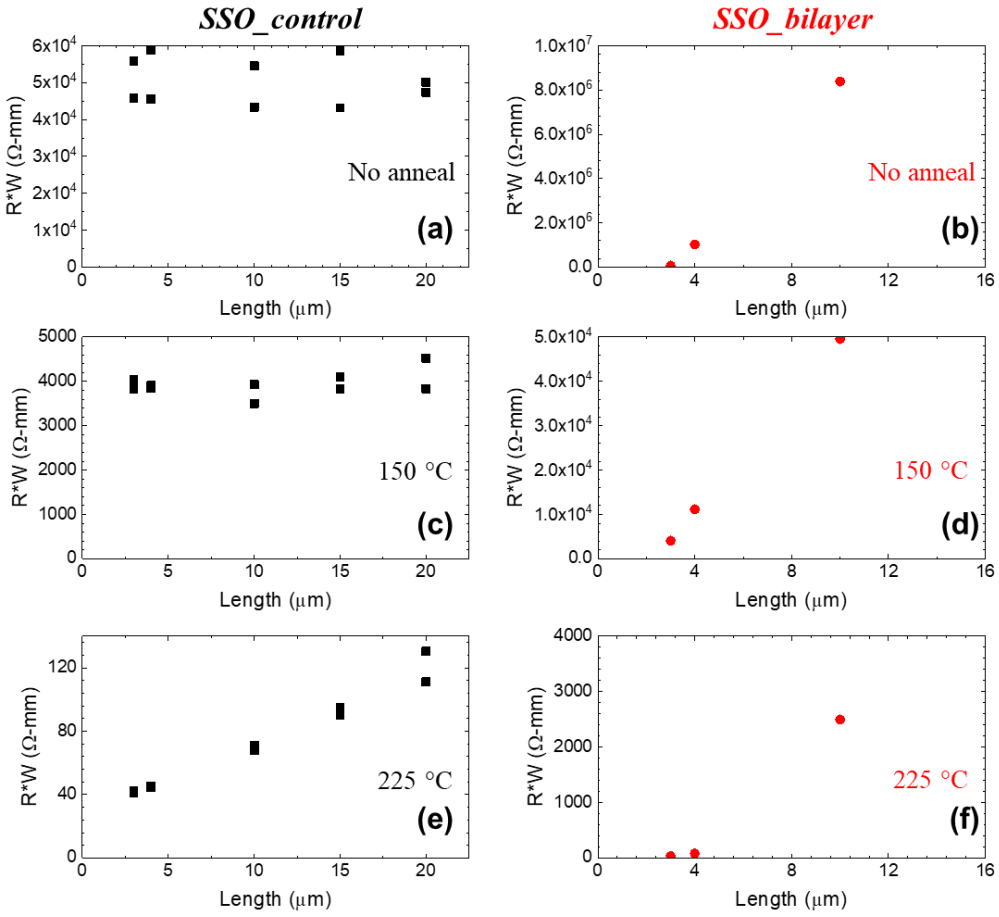

FIGURE 3.10. (a), (c), and (e) show TLM data for Ti-contacts on *SSO_control* films obtained before any anneal, after 150 ℃, and 225 ℃ anneals, respectively. (b), (d), and (f) show the corresponding data obtained on *SSO_bilayer* films.

the contact resistance with SSO. It is suspected that surface state-related thin-insulating barrier could be the reason for the much higher contact resistivity before the annealing.

In conclusion, Ti-contacts were proven to make reliable, low-resistance contacts to heavily-doped n-type SSO. The Sc- and Mn- contacts also provided reasonable contact resistances although their tendency to readily oxidize in air makes them less desirable as contact metals. This is the first-ever contact resistance study performed on any perovskite stannate and can have significant impact on the future applications of stannate-based FETs.

Chapter 4

Bi-Layer MESFET Results

The bi-layer film structure which can provide lower contact resistances was described in the preceding chapter. There can be other advantages to this bi-layer structure in FET applications. In Figure 4.1, a schematic of a recess MESFET structure is compared with that of a regular MESFET that utilizes only a single-layer film. Such a recess MESFET structure allows one to measure the intrinsic performance of the device. This is because the series resistance contribution from the contact resistance, and from the S/D access regions is greatly reduced by the capping layer, which is heavily doped in order to have high conductivity. A similar approach adopted in different FET geometries has been proven to provide improvements in various aspects of the device performance, in prior GaN (and other III-V) literature, namely improved DC performance by reducing the series resistance [85, 86], or by providing better control gate control in a heterostructure device [87], and also, high-power performance as well as efficiency in heterostructure FETs [88]. Two approaches are possible to implement recess-geometry devices namely, via a controlled recess etch [85, 87] or using selective-area growth (SAG) [86]. While SAG may be possible with perovskite stannates, such growth techniques have not been demonstrated, so far, owing to the stannates being a budding research topic. The alternate approach is to etch down the heavily doped capping layer in order to pinch off the channel layer below, but care must be taken to ensure minimal damage to the underlying material during the etching process [85, 87]. In this work, a fabrication process developed to demonstrate recess MESFETs based on SSO is presented and the improvements in device performance resulting from the recess structure are discussed. The recess etch process described below can generally be applied to all stannate materials and extended to other perovskite oxide

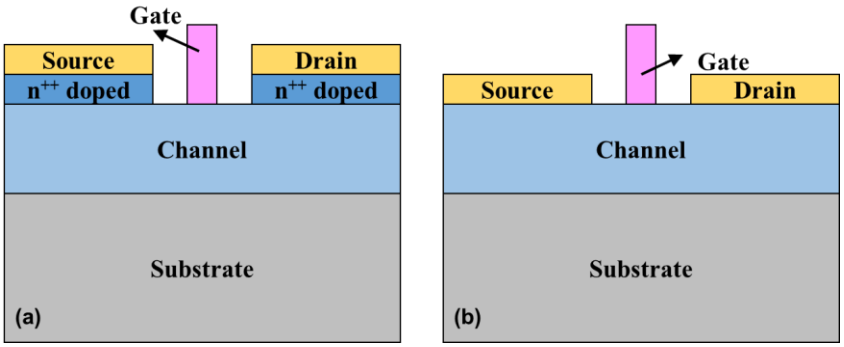

FIGURE 4.1. Comparison of (a) recess MESFET and (b) regular MESFET structures.

materials as well, facilitating development of high-performance heterostructures similar to that demonstrated in III-V-based devices [88].

4.1 Device Fabrication

The bi-layer films (*SSO_bilayer)* described in Chapter 3 were used here to fabricate recess MESFETs. *SSO_control* films were also used to fabricate control devices without any recess in order to establish a comparison point for demonstrating the performance improvement. The properties of the *SSO_bilayer* and *SSO_control* films are summarized in Table 4.1.

Sample	**Film thickness**	**Carrier Conc. (cm^{-3})**	**Sheet resistance (W/□)**	**Mobility (cm^2/Vs)**
SSO_control	11 nm NID SSO + 26 nm channel	2.3×10^{19}	3845	27
SSO_bilayer	11 nm NID SSO + 26 nm channel + 9 nm capping	Channel – Expected to be similar to SSO_control Capping – Expected to be similar to or > SSO_heavy	Unknown	Unknown

TABLE 4.1. Comparison of (a) recess MESFET and (b) regular MESFET structures.

The fabrication steps described in Chapter 3, namely alignment marks and mesa isolation were repeated here without any changes. The alignment marks were fabricated by depositing Ti (10 nm) / Au (90 nm) and lifting off the resist patterns. The mesa isolation was performed using a dry Ar plasma etch for 17.5 min to produce an etch depth of ~53 nm. The different fabrication steps are shown sequentially in Figure 4.2 while comparing the *SSO_bilayer* and *SSO_control* films in each step. The key fabrication steps introduced in this chapter are discussed in the following two sub-sections.

4.1.1 Recess Etch

It is highly essential to minimize any surface and material damage that could occur during the recess etch [85, 87]. A low-power (40 W) reactive-ion-etch (RIE) recipe with Ar (5 sccm), BCl_3 (47 sccm), a chamber pressure of 8 mTorr, and an inductive-coupled plasma power of 1000 W was first tested on a thick Nd:SSO film that had an active layer thickness

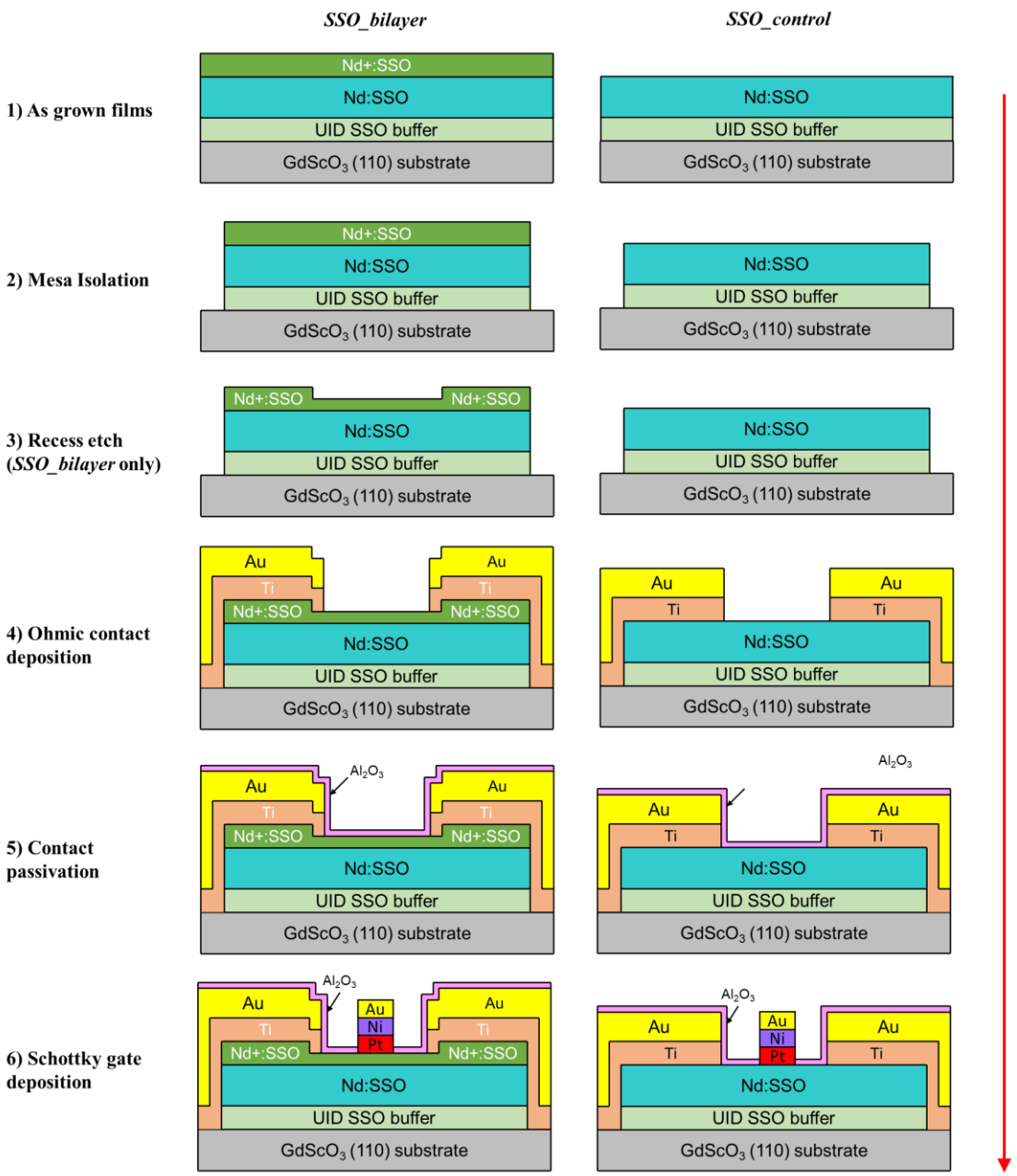

FIGURE 4.2. Fabrication sequence of recess MESFETs on *SSO_bilayer* and regular MESFETs on *SSO_control* films.

= ~221 nm, and ~10 nm was etched away. Atomic force microscopy (AFM) was performed before and after the etch on the SSO film to inspect the surface and corresponding AFM surface maps are shown in Figure 4.3(a) and (b). The surface roughness measured as standard deviation in height across the scan area was found to be 1.5 nm and 0.98 nm,

before and after the etch, respectively. This suggests the etch results in a uniform and smooth surface after etching. No significant change in Hall mobilities in the film were observed before (64 cm^2/Vs) and after (61 cm^2/Vs) the etch, while a slight decrease in sheet carrier concentration was observed which changed from 1.7×10^{14} cm^{-2} to 1.3×10^{14} cm^{-2}. The slight decrease could be due to compensating traps created during the etch which could be recovered potentially via annealing, although this was not confirmed experimentally. Overall, this initial study proves that the RIE recipe is a reliable and uniform process. An etch rate of 3.8 ± 0.7 nm/min was also calibrated on SSO films from the plot of etch depth vs etch time shown in Figure 4.3(c). The circular patterns in Figure 4.3(b), which could very well be AFM artefacts, were also present on films on which no etch was performed based on observations from other independent AFM scans.

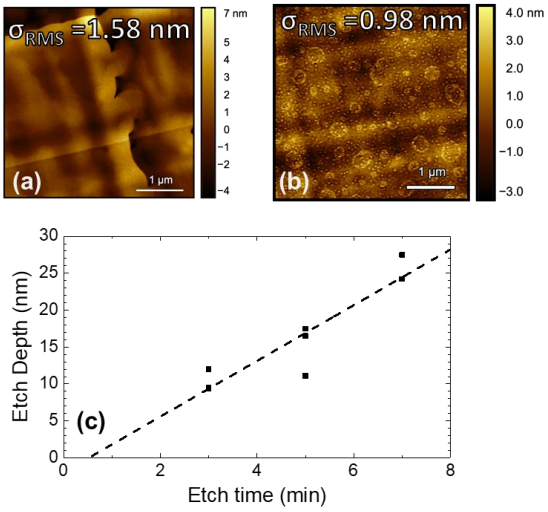

FIGURE 4.3. (a) AFM height maps of an SSO film obtained (a) before and (b) after RIE etching. (c) Etch rate is fitted for RIE recess etch using etch depth vs etch time plot.

Using the RIE recipe described above, the capping layer in between the S/D regions was partially etched after photoresist openings were patterned on the *SSO_bilayer* films such that the openings are wider than the S/D spacing. Approximately, 6 nm of the capping layer was etched away with the help of 1.75 min of etching. Subsequently, Ohmic contact patterning was performed and Ti (75 nm) / Au (100 nm) was deposited and lifted off to form the Ohmic contacts. The thick Ti layer ensures that Ti metal completely surrounds the active and capping layer, increasing the effective contact surface area. Then the contacts

were annealed up to 300 °C in forming gas atmosphere for 5 min and the sample was passivated with a 10 nm Al_2O_3 layer, deposited using the ALD technique described in the previous chapter. The passivation layer thickness was reduced due to reasons related to possible resist outgassing as described in the previous chapter.

4.1.2 Schottky Gate Deposition

Gate patterns were fabricated using electron beam lithography and the Al_2O_3 layer was etched using Microposit MF® 319 solution. Then the remaining capping layer in the *SSO_bilayer* films was etched by using the same RIE etch procedure described above with a etch time of 45 s. The recess etch was done in a two-step process so as to minimize the effective contact area for the Schottky gate with the capping layer, which can otherwise lead to higher gate leakage currents owing to the higher doping in the capping layer. No recess etch was performed on the *SSO_control* films as these films did not consist of any capping layers.

Next, Pt-Schottky gates were formed by depositing Pt (15 nm) / Ti (15 nm) / Ni (45 nm) / Ti (20 nm) / Au (80 nm) and liftoff. In comparison with the gate-metal stack used in the devices in Chapter 2, Al was not used in the gate stack since it can lead to unintentional leakage paths owing to its low-work function. However, in the first attempt, where a small number of devices were first patterned, the liftoff yield was low likely due to the Pt metal layer which is known for its low-adhesive properties and higher stress. Hence, some of these devices in which, the Pt gates were believed to have completely peeled off due to liftoff failure, were repatterned and Ni-Schottky gates comprising of Ni (65 nm) / Ti (10 nm) / Au (80 nm) were then deposited. Pt-gated devices were fabricated only in the recess geometry, while the Ni-gated devices were fabricated on both the *SSO_bilayer* and *SSO_control* films. Schematics of the completed MESFET structures with and without (control devices) a recess are shown in Figure 4.2.

4.2 Measurement Results

In the previous chapter, contact resistance improvement observed using Ti-contacts fabricated on the *SSO_bilayer* films over those on *SSO_control* films was discussed in

detail. Further to that, here the device DC performance improvements are presented. Ni-gated devices, which were fabricated on both *SSO_bilayer* and *SSO_control* films, were tested for comparison of recess and control devices. These results are discussed first, after which, the performance of Pt-gated devices is discussed in the subsequent section.

4.2.1 Comparison of Recess and Control Devices with Ni-Schottky Gates

The transfer characteristics in which I_D and g_m are plotted vs V_{GS} are shown Figure 4.4(a) and (b), respectively. These curves are plotted for a total of four devices, with two devices fabricated on *SSO_bilayer* and *SSO_control* films each. All devices show enhancement-mode behavior. From Figure 4.4, it can be observed clearly that for a given L_{DS} the recess devices drive higher current and also have higher peak g_m. A 2× improvement is observed in the maximum drive current as well as the peak g_m in the recess devices over the control devices. Saturation drive currents, I_{DSAT}, in devices with L_{DS} = 3 (4 μm), was 33 (27 mA/mm) for gate-recessed devices, while those observed in the control (non-recessed)

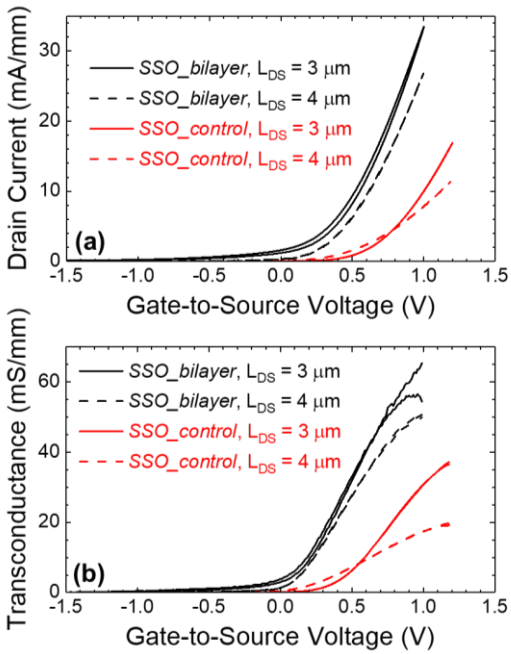

FIGURE 4.4. Plots showing (a) I_D vs V_{GS} and (b) g_m vs V_{GS} for SSO MESFETs with L_G = 0.5 μm and L_{DS} = 3 μm (solid) and 4 μm (dashed). Results for devices on recessed bi-layer (black) and non-recessed single-layer (red) films are shown for V_{DS} = +5 V.

devices were 17 mA/mm (12 mA/mm). A higher (42%) percentage increase in the current was observed for a 1 μm reduction in the L_{DS} in the gate-recessed devices, while the corresponding increase observed in the control devices was much lower (22%). This confirms that the heavily doped capping layer contributes to a significant performance improvement by reducing the contact resistance and also the access resistance in S/D region which is an additional source of series resistance in these devices. The measured gate leakage for these devices corresponding to the above transfer characteristics are shown in Figure 4.5, where gate current, I_G, is plotted vs V_{GS} in a semi-log scale. While there is some detrimental impact on the gate-leakage in the recess devices in comparison to the control devices, the increase in the gate-leakage was limited to an order of magnitude increase in the on (V_{GS} = +1 V) and off (V_{GS} = –2 V) states, respectively. This increase in leakage could be attributed to some minimal surface damage created by the recess etch and a small overlap between the Schottky gate and the partially recessed capping layer, which could lead to additional tunneling leakage paths. A detailed study is required to understand the gate-leakage mechanism.

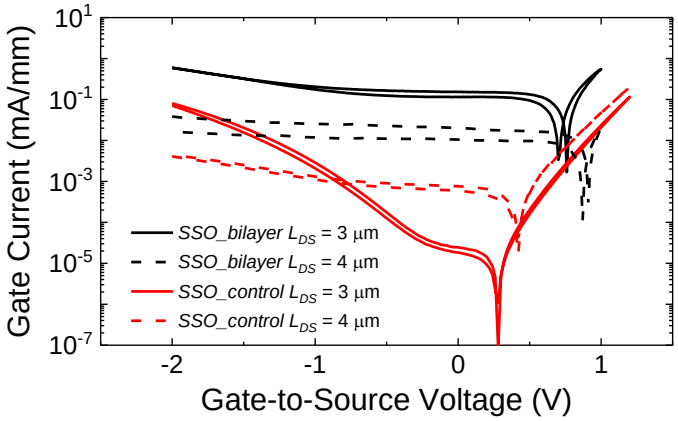

FIGURE 4.5. Gate current plotted vs V_{GS} to compare Schottky gate leakage on the *SSO_bilayer* and *SSO_control* films for V_{DS} = +5 V.

One surprising aspect of these results was that the devices on both the *SSO_bilayer* and *SSO_control* films showed enhancement-mode behavior, even though the carrier concentration and thickness of the channel were designed to be roughly the same as in the Pt-gated devices discussed in Chapter 2 [75]. The V_T of the Pt-gated devices discussed in

Chapter 2 was roughly -2 V. The V_T is extracted for the recessed and control devices, with L_G = 3 μm, fabricated here using the same method as in Chapter 2 (Equation 2.2) and found to be 0.25 V and 0.5 V, respectively. This drastic change in V_T may be attributed to surface states in the *SSO_bilayer* and *SSO_control* films that could be additionally depleting the channel apart from the Schottky gates. It is suspected that the O_2 plasma clean or the Al_2O_3 wet etch could be the source of these depleting surface states. It must be noted that the Pt-devices in Chapter 2 were annealed after the gate was deposited as a result of which a one-to-one comparison must be considered with caution. Irrespective of the change in V_T, the value of the peak g_m in the recessed device with Ni-gate on the *SSO_bilayer* film with L_{DS} = 3 μm was found to be 65 mS/mm which is a ~4× improvement over the Pt-devices discussed in Chapter 2, while the corresponding control device showed a ~2× improvement. The larger improvement observed in recess devices over our prior Pt-devices is due to the additional reduction in S/D access region, owing to the heavily doped capping layer. The control devices also register a significant improvement because of the large reduction in contact resistance by using Ti-contacts, as described in Chapter 3. These results validate the effectiveness of the recess device structure.

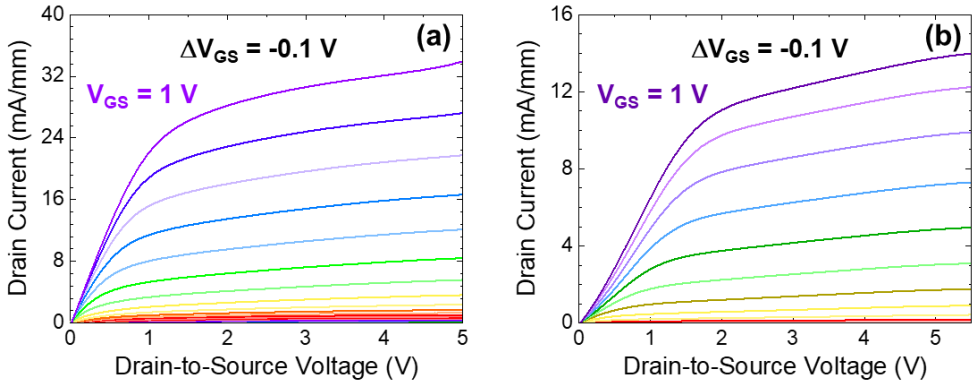

FIGURE 4.6. Output characteristics of MESFETs on (a) *SSO_bilayer* and (b) *SSO_control* films. L_G = 0.5 μm, L_{DS} = 3 μm. Values of V_{GS} were varied from +1.0 V to −0.5 V in steps of −0.1 V.

The output characteristics, where I_D is plotted vs V_{DS} are shown Figure 4.6(a) and (b) for recess and control devices with L_{DS} = 3 μm. I_D is plotted for several values of V_{GS} from −2 V to +1 V. Both devices demonstrate typical n-FET behavior but with an unexpectedly

large output conductance. The reason for the larger-than-expected output conductance is not clear, but could be related to surface defects.

4.2.2 Pt Schottky Devices

Pt-gated devices were fabricated only on *SSO_bilayer* films and are discussed in this sub-section. These devices exhibited a tendency to drift under certain conditions which caused its V_T to shift gradually. During the course of the entire measurements the devices transitioned from being enhancement-mode to depletion-mode devices. The devices were eventually stabilized after thermal annealing. The transient device behavior and post-annealing measurements are discussed in the following two sub-sections.

4.2.2.1 Transient Device Behavior

Initial transfer characteristics of the Pt-devices are shown in Figure 4.7(a), where I_D vs V_{GS} curves are shown for a device with L_G = 1 μm, and L_{DS} = 9 μm. Two successive measurements obtained on this device are shown in Figure 4.7(a), where a clear shift in the V_T of the device can be seen with the shift being in the decreasing or negative direction, leading to a significant increase in I_D. The corresponding two output characteristics (I_D vs V_{DS}) obtained for this device are shown in Figure 4.7(b). Upon application of a slightly higher V_{DS} voltage (10 V), the device V_T shifted to even more negative values. As the V_T shifted further to more negative values, the I_D also increased for a given $V_{GS} > V_T$. Noting

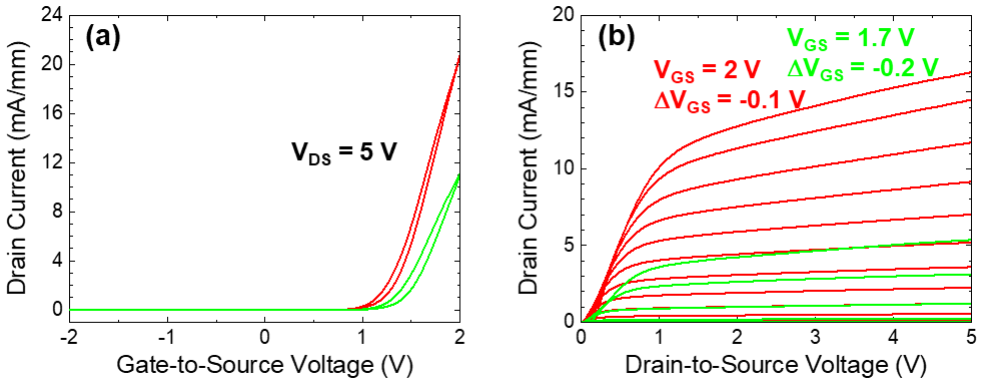

FIGURE 4.7. (a) Transfer and (b) output characteristics of a MESFET showing the change in threshold voltage of the device observed in two subsequent measurements. L_G = 1 μm, and L_{DS} = 9 μm.

this instability in the device, along with the larger-than-expected output conductance similar to that observed in Ni-gated devices, thermal annealing at a relatively-low temperature of 200 °C was attempted to help the stabilize the device. The device behavior post-thermal annealing is discussed in the next sub-section.

4.2.2.2 Anomalous Device Behavior after Thermal Annealing

The device characteristics dramatically changed after a 200 °C annealing to a depletion-mode behavior along with a large increase in the drive current in the device. However, the device initially showed some hysteresis while the transfer characteristics were being measured. As shown in Figure 4.8(a), the V_T of the device can be clearly observed to be negative. The hysteresis indicated that the device might still be unstable. In an attempt to remove the hysteresis and stabilize the device, successive measurements were performed on the device. While the device continued to drift initially, it eventually stabilized with a V_T = -5 V. The transfer characteristics obtained after stabilizing the device, along with the initial measurement obtained after annealing, and an intermediate measurement are shown in Figure 4.8(a). Further measurements attempted on this device did not show any appreciable change in V_T. The g_m is plotted in Figure 4.8(b) corresponding to the transfer characteristics obtained after the device was stabilized.

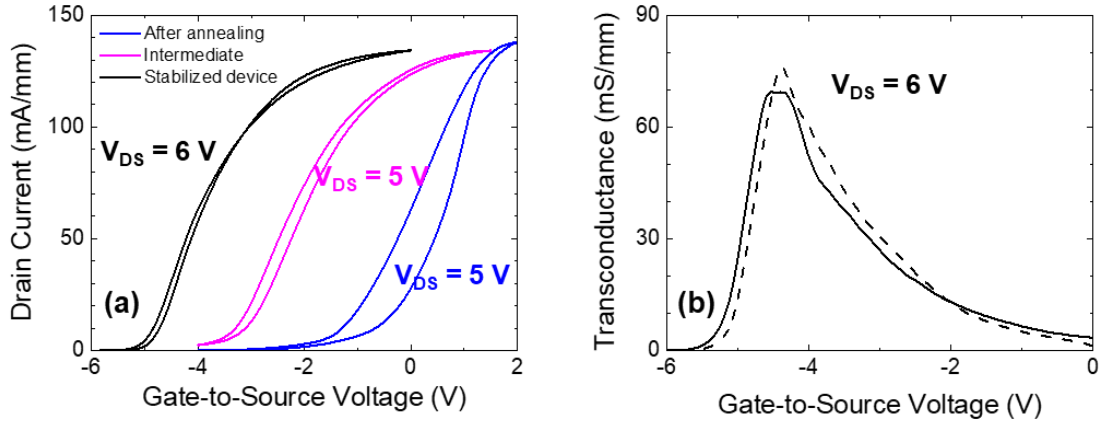

FIGURE 4.8. (a) Transfer characteristics of a recessed Pt-gated MESFET on the *SSO_bilayer* film measured after thermal annealing at 200 °C. The device was initially showed large hysteresis. After stabilization the hysteresis is reduced and V_T changed to −5 V. L_G = 1 μm, and L_{DS} = 9 μm. (b) Transconductance of the MESFET after V_T stabilization.

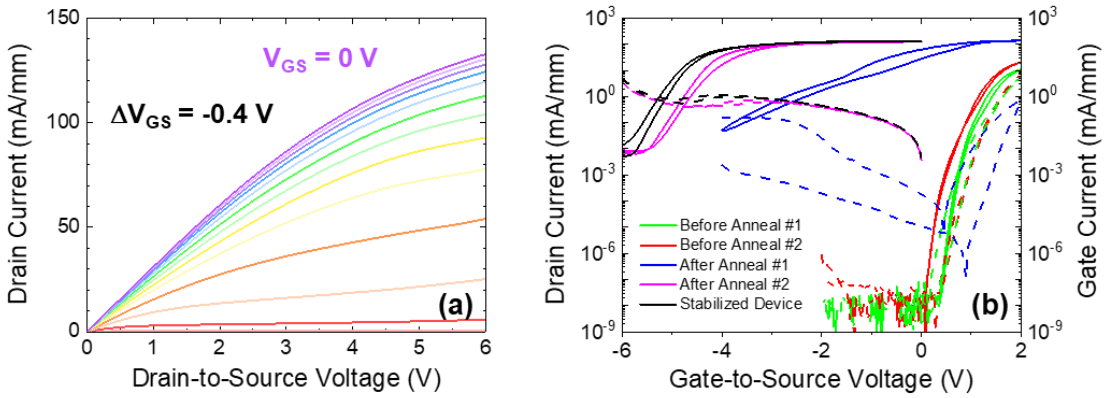

FIGURE 4.9. (a) Output characteristics of a Pt-gated MESFET after V_T was stabilized at −5 V. L_G = 1 μm, and L_{DS} = 9 μm. (b) Drain current and gate current vs V_{GS} corresponding to several measurements of the same device plotted on semi-log scale to show the effect of annealing on gate leakage.

The output characteristics obtained for this device after the V_T was stabilized are shown in Figure 4.9(a). The output characteristics clearly show that a finite output conductance is still present in the device. While the instabilities in the device and the changes after annealing are not clearly understood, the device is now closer to the expected depletion-mode behavior that was originally intended and confirmed by simulations presented in Chapter 2. This indicates that the surface depletion may have been reversed partially by the annealing. A thorough dedicated study is needed to understand the dependence of surface depletion on temperature. The gate current corresponding to all the measurements discussed above are plotted in Figure 4.9(b) to show the effect of V_T shift and thermal annealing on the leakage. Clearly, the V_T shift and the annealing do not have a desirable effect on the gate leakage. Methods to eliminate or reduce surface depletion without impacting the gate leakage negatively need to be devised. Moving to a heterostructure or metal-insulator-FET configuration can eliminate the additional surface depletion created during the fabrication by avoiding exposure of SSO surface to any plasma or etching.

In some devices on *SSO_control* films, Ni-gates were redeposited, where the Pt-gate fabrication failed due to a poor liftoff yield. The substrate was annealed at 200 °C before the Ni-gates were redeposited. Such devices also showed anomalous high-currents that was not observed in other Ni-gated devices. It is suspected that a small amount of Pt-residue

may have remained on the SSO surface after the liftoff failure, which when subjected to annealing changed the effective carrier concentration in the underlying SSO, thus causing this anomalous device behavior. Transfer characteristics and gate-leakage currents of two such Ni-gated devices are shown in Figure 4.10. A clear depletion-mode behavior and unusually high gate-leakage occur, which were not observed in other Ni-gated devices.

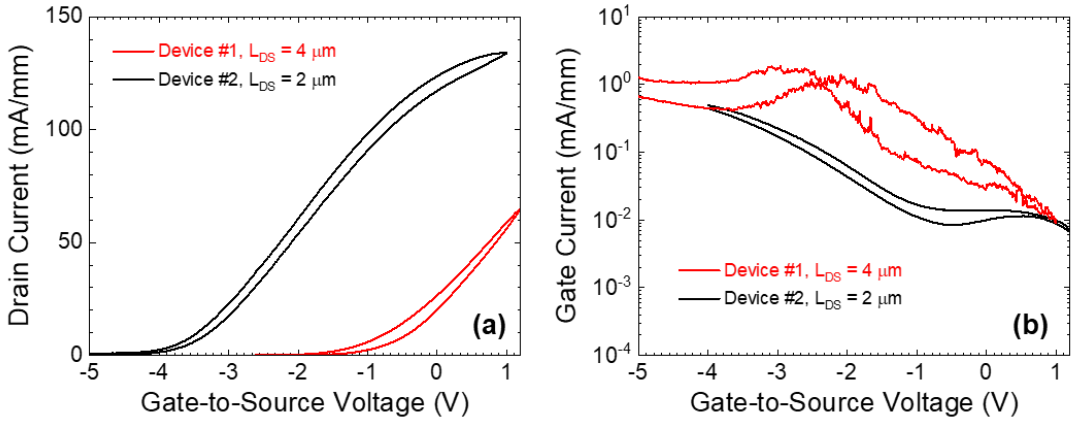

FIGURE 4.10. (a) Transfer characteristics of two Ni-gated devices on *SSO_control* films where Pt had delaminated after a failed lift-off. (b) Gate current vs V_{GS} for the same two devices.

In conclusion, recess-gated MESFETs were fabricated for the first-time on SSO and a 2× improvement in device performance is shown over control devices on single-layer epi structures. Devices without annealing showed enhancement-mode behavior which is not expected based on simulations. After annealing the devices, a large shift in the V_T of the devices is observed. This shift is not clearly understood but indicates that standard fabrication processes may be causing a surface depletion that changes the effective carrier concentration in the SSO films. This may be addressed by avoiding the exposure of SSO to plasma or other etches. The currents in excess of 100 mA/mm on SSO-FETs with L_{DS} spacing as large as 9 μm promises significant potential for SSO, and stannates in general to produce high-performance FETs in the future.

4.3 RF Measurement Results

Initial RF measurements were performed on the MESFET devices fabricated on *SSO_control* films. These measurements were performed using a Keysight E5063A RF

network analyzer in air at room temperature. Preliminary results indicate that SSO MESFETs can have high operating frequencies. Figure 4.11(a) and (b) show the plots of current gain, h_{21}, and Mason's unilateral gain, U, (in dB) vs. measurement frequency for a

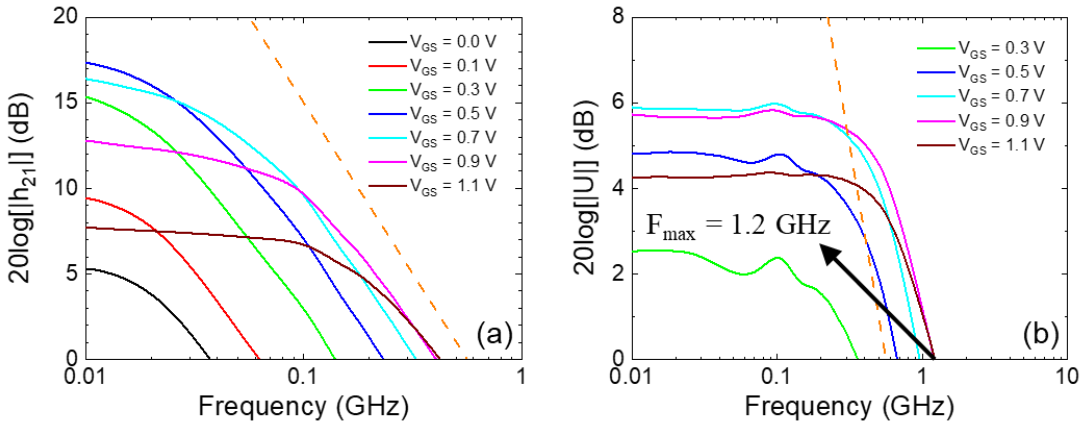

FIGURE 4.11. Extracted gains (a) h_{21}, (b) U are plotted vs measurement frequency. A dashed orange line with a slope of -20 dB/dec is also added for convenience to compare the roll-off characteristics of the device. f_{max} = 1.2 GHz and f_T = 0.4 GHz is observed for a device with L_G = 0.5 μm, and L_{DS} = 4 μm.

MESFET with L_G = 0.5 μm, and L_{DS} = 4 μm. The MESFETs fabricated on the *SSO_control* film, as can be seen from Figure 4.11, has an f_T = 400 MHz, and an f_{max} = 1.2 GHz. Here, the gain vs frequency curves are plotted for various values of V_{GS} from 0 V to 1.1 V, for a V_{DS} = 5 V. In order explain the cut-off frequency, values obtained from DC characteristics were also measured. The corresponding DC transfer characteristics and transconductance of this MESFET are plotted in Figure 4.12(a) and (b), respectively. In 4.12(a) and (b), two sets of curves are shown which were measured on this MESFET before (black) and after (red) performing the RF measurements. The transfer characteristic obtained after the RF measurement has a very high off current accompanied by substantial reduction in g_m, in comparison to the initial measurement characteristics. The increase in the Schottky gate leakage can be modeled as a shunt resistance in the small-signal equivalent circuit and explain the measured f_{max} being greater than the f_T. The high f_{max} despite the leaky gate and low g_m indicates that the device RF performance could have been much better if not for the aberrant shorting of the gate. Further improvements in RF performance should be possible if improved device stability can be achieved.

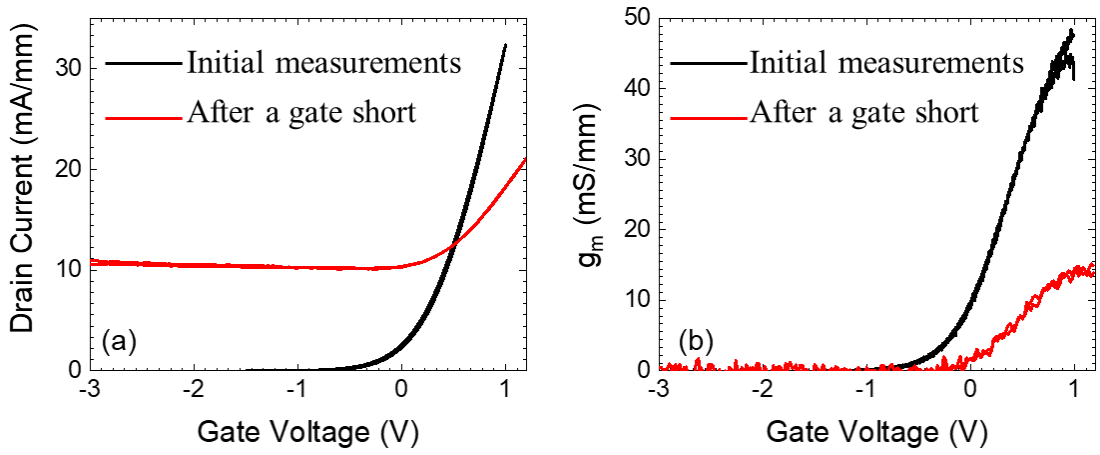

FIGURE 4.12. (a) Drain current, and (b) transconductance plotted vs. gate voltage. Two sets of curves measured are shown: before (black) and after (red) a gate degradation that likely occurred while the RF measurements were being obtained.

Chapter 5

Outlook and Conclusions

6.1 Conclusions

The vast potential offered by the perovskite oxide material system was reviewed in Chapter 1 and the realization of novel devices based on this material system may hinge on identification of an apt perovskite oxide semiconductor. Perovskite stannates possess several necessary material properties that are required of a semiconductor to be useful as a channel material. Among the stannates, SSO, due to its wider band gap and smaller lattice constant than that of BSO may be better suited to high-power and RF device applications and also in general to other novel heterostructure devices.

In Chapter 2, single-layer SSO MESFET results were presented, which despite being the first-ever SSO-based device results, were shown to have superior performance than any prior perovskite oxide-based FETs. The electron affinity of SSO was confirmed using the experimentally determined Pt-SSO Schottky barrier height. The key processing difficulties identified here paved the way for the following experimental studies. In Chapter 3, key issues revealed in the preliminary SSO MESFET devices, namely a high-contact resistance and contact degradation in air were addressed. A first systematic study of Ohmic contacts to any stannates was presented. Improved contact resistances with specific resistivity of Ti-SSO contacts as low as 34 $\mu\Omega$–cm^2 were produced. These results can significantly benefit future SSO-based RF devices. Additionally, the advantage of a bi-layer film structure in terms of contact resistance improvement was proven. These results could be improved further in future by utilizing a heavily doped BSO-capping layer which can potentially reduce the contact resistance as BSO is capable of higher doping concentrations than in SSO.

In Chapter 4, SSO bi-layer MESFETs in a recess-gate configuration were demonstrated and improvement in device performance due to the use of the recess structure was shown. A recess etch was demonstrated to aid in successful fabrication of such structures, which can be extended in future to other perovskite stannate materials and even heterostructures based on SSO. Peculiar device behavior was observed in Pt-gated devices before and after annealing which helped identify surface depletion as a major obstacle to fabrication of

SSO-based MESFETs with superior DC performance. Alternate device structures to mitigate this issue may be explored in future.

The work performed as a part of this dissertation is a first such study on SSO and is a stepping-stone towards the development of future novel perovskite-based devices. SSO has unique advantages over other emerging ultra-wide gap (UWG) semiconductors, including β-Ga_2O_3, diamond, and AlN by virtue of being a perovskite oxide semiconductor with the capability of heterostructure integration with multifunctional perovskite oxides. Moreover, initial studies indicate that SSO (and BSO) can have higher intrinsic theoretical mobility limits than β-Ga_2O_3 [46], which is presently the most extensively studied emerging UWG semiconductor. Despite its tremendous promise, many fundamental questions remain as to how to design and implement RF transistors using $SrSnO_3$ materials. This could be the focus of future work on SSO-based devices.

6.2 Proposed Future Work

6.2.1 Achieving High-Power Operation

Despite the promise of higher breakdown voltages in SSO owed to its wide band gap of 4-5 eV, the critical breakdown fields in SSO have not been experimentally determined so far. To this end, the SSO MESFETs fabricated on thin films described in Chapter 2 were used to understand breakdown properties of these devices. Low breakdown voltages of ~30 V were observed in these devices for a L_{GD} spacing of 8 μm. The breakdown was observed to occur in the on state of the device which is unusual because the on state is usually not associated with high-electric fields that can trigger impact ionization. The output characteristics of the device corresponding to this breakdown event is shown in Figure 5.1(a). Measurement of another device, whose breakdown was observed near the off state, is shown in Figure 5.1(b). This device also had similar breakdown voltages. Both the breakdown events were catastrophic and subsequent measurements on these devices were not possible.

One observation is that the MESFETs, which were designed to have a relatively high doping in the channel are not considered to be suitable for breakdown measurements

because of a relatively-large gate leakage under large negative biases, due to tunneling. Moreover, the devices were not field-plate passivated [71] which is commonly required, especially in MESFETs, to reduce the electric field-line crowding near the drain-side edge of the gate. In the absence of a field-plate in MESFETs with high channel doping even relatively smaller reverse bias voltages can cause large leakage currents eventually leading to breakdown or possibly device burnout. These reasons make the SSO MESFET designs fabricated, so far, as a part of this dissertation work to be unsuitable for breakdown measurements.

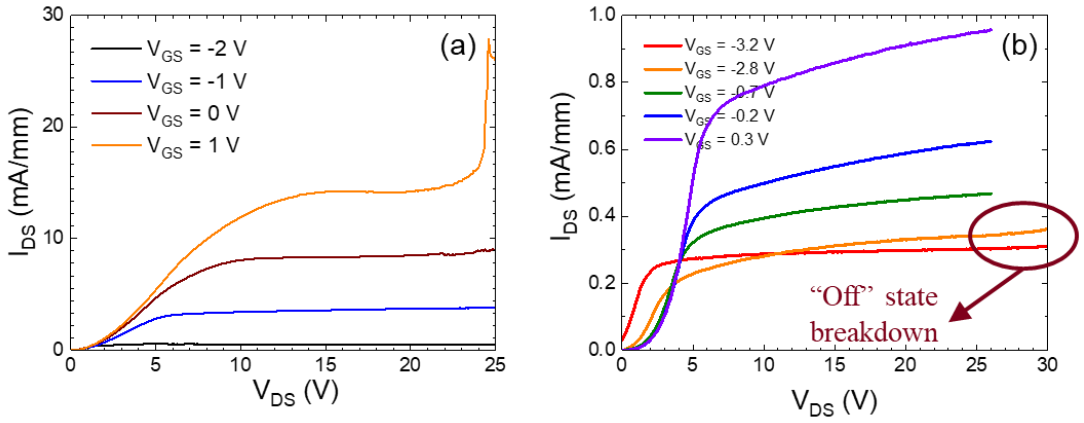

FIGURE 5.1. (a) On state breakdown in a single-layer Pt-gated MESFET with Sc-contacts. (b) Off state breakdown in another similar MESFET. L_{GD} = 8 μm in the both devices.

In the future, devices with a field-plate structure and preferably in a MOSFET geometry may be attempted to study the *ideal* breakdown in these devices. For MOSFETs, identifying a suitable dielectric as gate oxide is critical. While ALD dielectrics, such as HfO_2 and Al_2O_3, can be used, their dielectric constants can be lower than that of SSO, which can be detrimental to high-power applications as the breakdown voltage may then depend on the peak electric fields and critical breakdown fields of the ALD dielectrics. It could be beneficial to make use of the vast material choices available in the perovskite oxide family to identify a gate oxide material with a higher dielectric constant that can be deposited *in situ* and epitaxially. The epitaxially grown gate oxide can provide a good interface with SSO which is crucial for a MOSFET and for high-power operation as well. A higher dielectric constant in the gate oxide will also allow for modulation of higher

charge densities in the channel which can then be exploited to achieve higher drive currents as well as DC and RF performance improvements.

As stated above, films with low doping are preferred to measure the breakdown voltage of a Schottky-gated device. With this in mind, a thin SSO film with a 11 nm NID buffer layer was first grown, and a 11 nm moderately doped active layer was subsequently grown by setting the La effusion cell at a temperature of 1080 ℃. Surface depletion caused the film to be insulating and prevented any Hall mobility and sheet resistance extraction. Based on doping calibrations, the dopant concentration is expected to be in the range of 10^{18} cm^{-3} to 5×10^{18} cm^{-3}. To measure the breakdown voltage in these films, interdigitated capacitance structures (IDCs) were fabricated and an optical micrograph of one such structure is shown in Figure 5.2. These structures consist of an anode and a cathode which are both Schottky-type contacts, which ensures that the current flowing through the anode and cathode is very low. The fabrication procedure consisted of only one step, as a result of which alignment marks were not required. The separation between the two Schottky contacts determines the breakdown field in these structures. Electron-beam lithography was used to pattern the features and Pt (10 nm) and Au (40 nm) was deposited and lifted off.

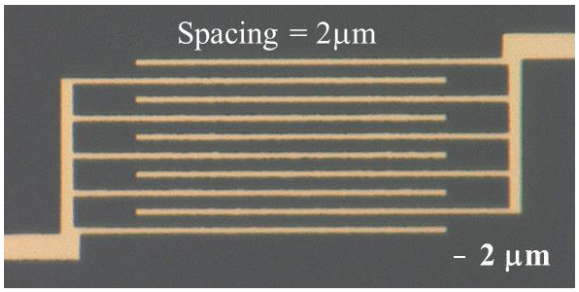

FIGURE 5.2. Optical micrograph of an IDC structure with 2 μm spacing between the Schottky contact fingers. Width of the device = 50 μm.

IDC devices with inter-electrode spacings of 2 μm were measured up to a voltage of 200 V and no breakdown was observed in these devices suggesting a breakdown field of at least 1 MV/cm in SSO, which is an encouraging preliminary result. The current-voltage characteristics obtained on these IDC structures are shown in Figure 5.3. The current-voltage curves that are shown were extracted from the measured data after correcting for

the displacement current. While a slight increase in current for higher applied voltage was observed, this current can be attributed to a slight leakage through the Schottky electrodes as well as a residual displacement current remaining due to the use of an imperfect method to de-embed the displacement current from measurement data. Due to lack of a high-voltage supply which can provide > 200 V bias, further measurements were not performed on these devices. These preliminary results are encouraging and suggest potential high-power applications for SSO. Similar structures can be studied on undoped SSO films to determine the intrinsic breakdown fields.

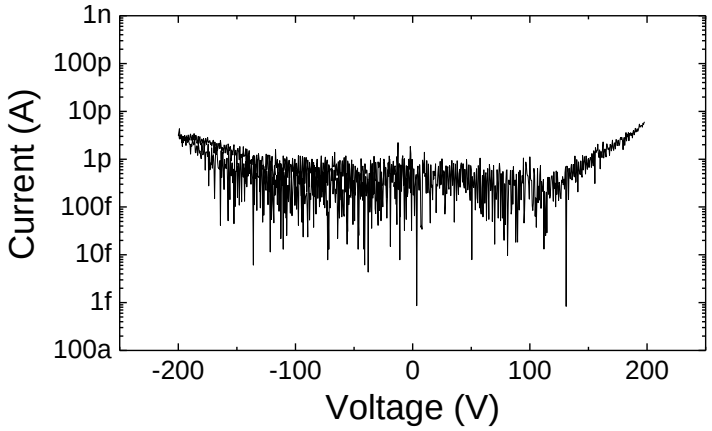

FIGURE 5.3. Current vs voltage curves for a 2 μm spacing IDC device showing no breakdown occurring when measured up to 200 V. Width of the device = 50 μm.

6.2.1.1 Inverse Capped Structure

In order to make best use of the key advantage of the stannates, viz. the ability to achieve high-mobilities at high doping levels and the wide gap of SSO, an inverse capped film structure whose schematic is shown in Figure 5.4 is proposed. In this structure, the active layer is capped with a near-intrinsically-doped SSO layer which can be then used to

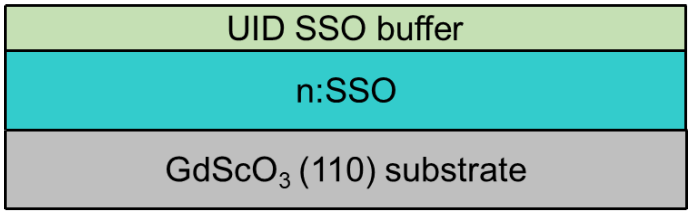

FIGURE 5.4. Schematic of an inverse capped structure, where the insulating capping layer can suppress gate leakage and may help in measuring higher breakdown voltages.

fabricate MESFETs whose gate leakage will be vastly minimized because of the low (or no) doping in the capping layer. This structure can be useful to study breakdown performance of SSO while retaining the higher doping in the channel which can help achieve high currents, transconductance, and good RF performance. The capping layer may possibly address some of the surface depletion effects observed in current SSO thin films, although this is yet to be verified experimentally.

6.2.2 Path Forward to Heterostructures

The proposed inverse capped structure can also act as a natural transition step to move towards heterostructures, which can be achieved by doping the capping layer with other atoms that can increase the band offset with respect to the active layer and potentially the dielectric constant in the capping layer. Heterostructures have helped achieve superior performance in the devices based on III-V material system owing to the superior mobilities that electrons can possess in a two-dimensionally confined state. Also, the advantage of multifunctionality in perovskite oxide material world simply cannot be utilized if heterostructures are not incorporated. The foundation laid down in this dissertation work, provides the necessary framework for heterostructure device experiments and the results of such experiments may well decide the fate of stannates as channel materials. It was revealed in Chapter 1 that SSO is an ultra-wide band (UWG) semiconductor with band gap in the range of 4-5 eV. Materials with a wide gap (WG) can have higher intrinsic breakdown fields than their counterparts with narrow band gap. Existing WG semiconductors, including GaN and SiC have been shown to have larger intrinsic breakdown fields than narrow gap semiconductors, including Si and GaAs [89]. Emerging UWG materials, including β-Ga_2O_3, diamond, and AlN are being studied for future high-power, extreme environment, and other novel applications, and can have breakdown fields larger than those of WG semiconductors [89]. SSO has the potential to be added to the emerging UWG materials list owing to its band gap > 4 eV. However, many of the fundamental material properties, including thermal conductivity and intrinsic breakdown field of SSO are as yet unknown and further work is required to uncover the potential for SSO in high-power applications.

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Appendix A: Optical Photolithography Process Flow

Soak the sample in acetone overnight before starting any processing. Gentle sonication can help partially clean up any solder residue present near the edges of the substrates.

I. Dynamic dispense photoresist spin and exposure

1. Clean the substrate with acetone and IPA and perform a 120 ºC dehydration bake.
2. Use the headway spinner and set the spin speed to 5000 rpm after placing the substrate on the vacuum chuck. Then use a pipette to dispense one drop of photoresist (AZ® 1512) close to the center of the substrate while it is spinning. Start the timer simultaneously and allow the substrate to spin at the set speed for 45 s.
3. Transfer the substrate to a 100 ºC hot plate and bake for 1 min.
4. After alignment, expose with hard contact for 5.5 s.
5. If necessary, perform image reversal. Image reversal bake has to be followed by an additional exposure under Oriel lamp for 8 min. It is good practice to perform a first exposure for 4 min and then expose the remaining 4 min after rotating the substrate by 90º.
6. The develop time using standard developer provided by MNC is 30 s without any image reversal. If image reversal is used, then the develop time is 3.5 min.

II. Alignment marks

1. It is important to have good and reliable alignment marks.
2. Ti (10 nm) / Al (50 nm) may be evaporated and lifted off.

III. Mesa

1. After mesa patterning, prepare a 1 M HCl solution and place it on a hot plate set to 60 ºC. Allow the solution to rest on the hot plate for 30 min.
2. Perform wet etch for 1.5 min in 1 M HCl. Etch times longer than ~1.5 min can result in significant lateral etching.

3. Then use Ar plasma dry etch for 10 min. The name of the recipe to be used here is "slow_200_70_24".
4. After this perform an O_2 plasma clean with 100 W power for 20 s.
5. Soak overnight in acetone for resist strip.

IV. Ohmic Contacts

1. After patterning, perform O_2 plasma clean with 50 W power for 20 s.
2. Load the substrates into the evaporation chamber and pump down for 1 hr.
3. Deposit Sc (10 nm) / Au (80 nm) and liftoff in acetone overnight.
4. Sonicate, if needed, using gentle powers for 5-10 s. Increase the sonication time only if needed.

V. Schottky Contacts

1. After patterning, perform O_2 plasma clean with 50 W power for 20 s.
2. Evaporate Pt (10 nm) / Ti (10 nm) / Al (80 nm) / Ti (10 nm) after pumping down for 1 hr.
3. Watch the Pt deposition carefully and pause the process if the chamber pressure exceeds 9×10^{-6} Torr during deposition. The process may be continued after pressure is stabilized. Better to pump down for longer time before starting Pt deposition in the beginning to avoid this. Slow ramp up process must be used for efficient Pt deposition.
4. After liftoff, anneal at 300 ºC in Ar/H_2 atmosphere for 5 min to activate the Ohmic contacts.

Appendix B: E-beam Lithography Process Flow

Soak the sample in acetone overnight before starting any processing. Gentle sonication can help partially clean up any solder residue present near the edges of the substrates.

I. General PMMA spin and sample preparation

1. Clean the substrate with acetone and IPA and perform a 120 ºC dehydration bake.
2. After spinning PMMA, bake for 15 min at 180 ºC. Longer bakes will not hurt.
3. Use the SEM sputterer to deposit a thin Au layer. The recommended sputter time is 30 s and must be increased only if a good reflection is not observed under the alignment stage.
4. Use regular rectangular clips to hold the sample. Use of Cu clips may help but has the downside of losing patternable sample area. It may also lead to unintentional scratches.

II. Alignment marks

1. Spin MMA EL9 at 3000 rpm for 45 s. Bake at 180 ºC for 8 min and allow the sample to cool down for 2 min.
2. Spin PMMA C2 at 3000 rpm for 45 s. Bake at 150 ºC for 15 min and allow the sample to cool down for 2 min.
3. Sputter Au for 30 s.
4. Use 15 nm beam step size, 15 nA current and a dose of 250 $\mu C/cm^2$.
5. Strip Au using wet etchant (KI-based) for 2 min or longer, if needed.
6. Develop for 50 s in 3:1 IPA:water and rinse with water.
7. Perform O_2 plasma clean using 100 W for 20 s.
8. Evaporate Ti (10 nm) / Au (90 nm) and lift-off.

III. Mesa

1. Use photolithography process described in Appendix A for patterning.
2. Use Ar plasma dry etch for 17.5 min. The name of the recipe to be used here is “slow_200_70_24”. Etch rate is ~3 nm/min.

3. Perform O_2 plasma clean using 100 W for 20 s.
4. Soak in acetone overnight to strip PMMA.

IV. First recess etch

1. Use photolithography process described in Appendix A for patterning.
2. Use "N-SrTiO3-8mt Low POWER" recipe in a dry run to clean the Oxford etcher chamber for 2 min.
3. Then use the same recipe to partially etch the capping layer for 1.75 min. Etch rate is 3.8 ± 0.7 nm/min as determined from profilometer measurements.
4. Soak in acetone for resist removal.

V. Ohmic contacts for $L_{DS} \geq 2$ μm

1. Use photolithography process described in Appendix A for patterning.
2. Perform O_2 plasma clean using 50 W for 30 s and then in Ar plasma for 45 s.
3. Evaporate Ti (75 nm) / Au (100 nm) and liftoff overnight in acetone. Sonicate gently for 5-10s and repeat, if necessary.

VI. Ohmic contacts for $L_{DS} \geq 2$ μm

1. Spin PMMA C6 at 2500 rpm for 60 s using ramp speed of 500 rpm/s. Bake at 180 ºC for 15 min.
2. Sputter Au for 30 s.
3. Use 50 nm beam step size, 100 nA current and a dose of 560 μC/cm^2.
4. Strip Au using wet etchant (KI-based) for 2 min or longer, if needed.
5. Develop for 40 s in 3:1 IPA:water and rinse with water.
6. Perform O_2 plasma clean using 50 W for 30 s and then in Ar plasma for 45 s.
7. Evaporate Ti (75 nm) / Au (100 nm) and lift-off.
8. Anneal at 300 ºC in Ar/H_2 atmosphere for 5 min.
9. Deposit 10 nm ALD Al_2O_3 at 200 ºC.

VII. Al_2O_3 etch for pads

1. Use photolithography process described in Appendix A for patterning.
2. Perform O_2 plasma clean using 50 W for 30 s.
3. Etch Al_2O_3 using "N-HfO2 Etch Lower pwr" recipe for 15 s.
4. Strip resist in acetone overnight.

VIII. Schottky Contacts

1. Spin PMMA C6 at 4000 rpm for 60 s. Bake at 180 ºC for 15 min.
2. Sputter Au for 30 s.
3. Use 20 nm beam step size, 8 nA current and a dose of 800 $\mu C/cm^2$.
4. Strip Au using wet etchant (KI-based) for 2 min or longer, if needed.
5. Develop for 1 min in 3:1 IPA:water and rinse with water.
6. Perform O_2 plasma clean using 50 W for 30s.
7. Etch Al_2O_3 using MF® 319 solution for 12 min.
8. Evaporate Ni (65 nm) / Ti (10 nm) / Au (80 nm) and lift-off.