Engineering Novel Transistors Based on Black Phosphorus

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DEDICATION

This work is dedicated to my lovely wife Becca, my parents, Paul and Debbie, and in science as in all things, glory to God.

ABSTRACT

Black phosphorus (BP), a layered 2D semiconductor that can be isolated to one monolayer thicknesses re-emerged in 2014 because of its promise for use in applications such as high performance MOSFETs, optoelectronic devices, novel devices like tunneling-field-effect-transistors (TFETs), and flexible electronics. The promise of BP comes from its unique material properties such as a high mobility, crystal anisotropy, a tunable direct band gap, an anisotropic effective mass, and the ability to scale to sub-1 nm thicknesses while retaining good electronic properties. These properties make BP particularly interesting as a possible post-silicon channel material in advanced logic transistors which could enable the continuation of transistor scaling beyond the foreseeable future. However, most experimental demonstrations of BP transistors have displayed poor OFF-state performance caused by gate-induced-drain-leakage (GIDL) which limits the device's overall usefulness. In this dissertation, novel BP transistors that utilize the unique properties of BP to improve OFF-state performance are demonstrated. These novel devices include a heterostructure BP MOSFET which utilizes the thickness-tunable band gap of BP to supress GIDL current, an electrostatically doped BP MOSFET which takes advantage the thin body of BP with a novel device structure used to effectively dope the source and drain regions of the BP, to again suppress GIDL current, and BP TFETs which utilize the anisotropic effective mass in order to open a path for realizing transistors with a subthreshold slope (SS) of less than 60 mV/dec in BP.

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CHAPTER 1 INTRODUCTION

Transistors are the building blocks for modern computers and since the invention of the first integrated circuit in the early 1970's the number of transistors on a chip has doubled every 18 to 24 months. This trend was named Moore's law and has driven the rapid advances in processing speed and price lowering in modern electronics [1]. The driving force behind Moore's law has been the scaling of transistor size in silicon CMOS (complementary-metal-oxide-semiconductor) circuits enabled by advances in patterning technologies [2], [3], device architectures, and materials engineering [4]. In addition to the scaling benefit of more transistors per area, Robert H. Dennard demonstrated that transistor performance also improves with scaling which meant that circuit performance could be increased at a new node while keeping the power density constant [5]. However, in recent years, geometric scaling has been approaching its physical limit and Dennard scaling broke down in 2005 due to increased current leakage as transistor dimensions grew smaller [6]. Overcoming these issues have been a driving force behind research into new materials systems and novel types of transistors that could reignite Dennard scaling and extend Moore's law far into the future.

1.1 Black Phosphorus

Black Phosphorus emerged in 2014 as a potential as a post-silicon CMOS channel material but its origins go much farther back. Black phosphorus (BP) was first discovered by Percy Williams Bridgman at Harvard University in 1914 when he was attempting to convert white phosphorus into red phosphorus by the application of a high hydrostatic pressure of 1.2 GPa at 200 °C [7]. He noted that it showed good electrical conductivity and that it was the more stable than the other allotropes of phosphorus. After this initial

discovery, a number of experimental and theoretical works throughout the 1900's determined some additional characteristics of BP including the crystal structure [8],[9], energy band structure [10],[11], effective mass [12], and carrier mobility [11]. In summary, these works showed that black phosphorus is a layered, two-dimensional semiconductor with an anisotropic puckered crystal structure which consists of sheets of covalently bonded phosphorus atoms in the x-y plane held together by the Van der Waals force in the z direction. It also is a semiconductor with a direct band gap of ~0.3 eV in the bulk, has an anisotropic effective mass, and has relatively high carrier mobility in the low-mass direction. These discoveries formed the foundation for the re-emergence of BP in 2014 which was spurned by the isolation of few-layer BP by a number of groups using mechanical exfoliation [13]–[17]. These early reports generated immense interest in the semiconductor device community because of demonstrations of high field-effect-mobility (μ_{FE}) and layer-dependent band gap (E_g) (up to 2 eV in a monolayer) which indicated the possibility of BP outperforming silicon as a channel material in transistors with ultra-short channel lengths (< 5 nm). The following sections will cover in detail the basic properties of black phosphorus.

1.1.1 Crystal Structure of Black Phosphorus

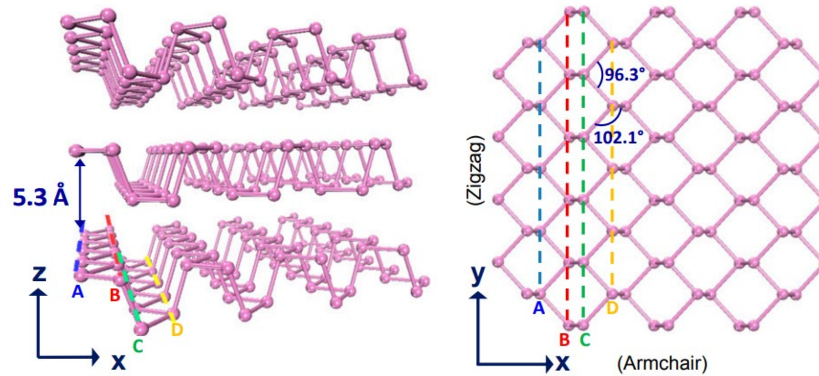


Figure 1.1 Ball and stick model for the crystal structure of black phosphorus in the x-z and x-y planes. Figure adapted from reference [18], Copyright (2015) National Academy of Sciences.

A single sheet of black phosphorus consists of two rows of P atoms, each bonded to three adjacent P atoms forming a puckered crystal structure [13]. This puckered honeycomb crystal structure yields asymmetry in the x-y plane leading to a strong in-plane anisotropy. The two in-plane directions are commonly referred to as the armchair (AC) and zigzag (ZZ) and can be seen in the ball and stick models in Figure 1.1 [18]. In the bulk, BP forms an orthorhombic crystal structure where sheets are held together with the Van der Waals force in the z direction. The in-plane lattice parameters have been measured to be x = 4.34 ± 0.05 Å and y = 3.31 ± 0.03 Å and the out-of-plane (z/2) lattice parameter is measured to be 5.4 ± 0.2 Å [19]. These values were measured using annular dark field-scanning transmission electron microscopy (ADF-STEM) but are consistent with other computational results [11], [20], [21]. The crystal anisotropy is a unique feature of BP that leads to effective mass anisotropy [11] as well as optical conductivity anisotropy [22]. The crystal anisotropy also leads to a polarization dependence of the Raman spectroscopy. This is particularly useful because it provides a convenient way to identify the crystal orientation

of black phosphorus on a sample. Figure 1.2 shows the Raman spectra of black phosphorus and how it changes with the polarization of incident light. The Raman spectrum of black phosphorus shows three peaks, the A_g^1 peak corresponds to phosphorus atoms vibrating in the out-of-plane mode, the B_{2g} peak corresponds to the the in-plane ZZ directional mode, and the A_g^2 peak corresponds to the in-plane AC directional mode [23]. From Figure 1.2 it is apparent that the A_g^2 peak height is strongly dependent on the polarization of the incedent beam with respect to the AC crystal axis of BP. The peak is maximized when linearly polarized light is aligned parallel to the AC crystal axis. This experimental details of this technique will be described further in future chapters of this work as it used for characterizing the crystal orientation of BP samples.

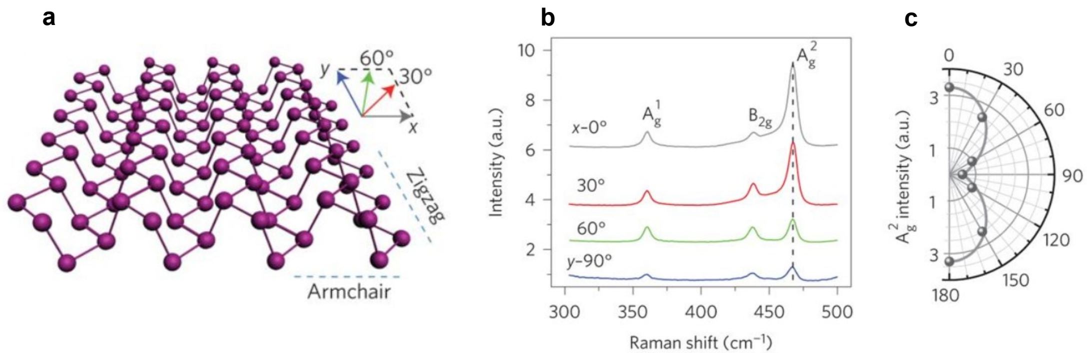


Figure 1.2 Raman spectra of BP for various polarization angles (reference crystal axis shown in (a) are shown in (b). (c) shows the polar plot indicating the A_g^2 peak is maximized when the light is polarized parallel to the AC axis of BP. Adapted by permission from Springer Nature Customer Service Centre GmbH: [Springer Nature] [Nature Nanotechnology] Ref. [23] *copyright 2015.*

1.1.2 Electronic Band Structure of Black Phosphorus

Black phosphorus has a direct band gap ranging from ~0.3 eV in the bulk to ~2.0 eV in a monolayer. This band gap range makes BP useful for a number of applications from transistors to thermal imagers [24]. Density functional theory calculations show how

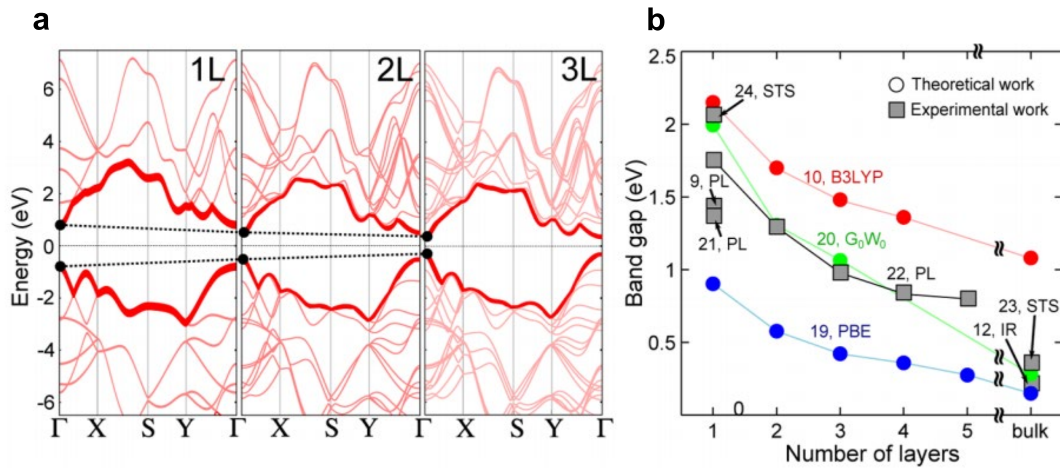


Figure 1.3 The E-k diagrams in (a) show the evolution of the band structure of BP as more layers are added. (b) Band gap vs. the number of BP layers. Adapted with permission from reference [24]. Copyright 2015 American Chemical Society.

the band structure changes with increasing layer numbers in Figure 1.3 [24]. The observed decrease in band gap with additional layers is due to band splitting which occurs over the entire brilloin zone [25], however the band gap remains direct at the Γ point for all BP thicknesses. This tunablility allows an engineer to select a particular thickness of BP in order to obtain a band gap optimized for a given application. The fact that the band gap is direct for all thicknesses makes this particularly useful for optoelectronic devices because it means BP can be an efficient absorber or emitter for a chosen wavelength of light. This feature has been used to fabricate waveguide integrated photodetectors in BP at telecommunications [26] and mid-IR wavelengths [27]. In the following sections it will also be described how the thickness tunable band gap can be used to create quasi-heterostructures in black phosphorus which enable optimized transistor performance as well as novel optoelectronic devices.

1.1.3 Effective Mass Anisotropy in Black Phosphorus

A large effective mass anisotropy arises from the lack of in-plane crystal symmetry in BP and is another unique property that makes BP interesting. Table 1.1 shows displays the electron and hole effective masses (m_{AC} and m_{ZZ}) in the armchair and zigzag direction obtained experimentally and from theoretical calculations [28], [29]. This large effective mass anisotropy has a number of implications related to the electronic properties of BP. One of these implications, as will be discussed in the next section, is mobility anisotropy [30]. The effective mass anisotropy also leads to a large band-to-band tunneling anisotropy [31], a topic that is a large subject of this work.

Direction	Hole		Electron	
	Expt. [28]	Calc. [29]	Expt.[28]	Calc.[29]
m_{AC}/m_0	0.076	0.09	0.076	0.076
m_{ZZ}/m_0	0.648	0.81	1.027	1.16

Table 1.1 Experimental and calculated in-plane effective masses of black phosphorus. Experimental values obtained from cyclotron resonance absorption spectra in reference [28] and calculated values obtained from tight binding model in reference [29].

1.1.4 Mobility of Black Phosphorus

One of the key reasons for the re-emergence of BP in 2014 was the high mobility values over 1,000 cm^2/V·s for both holes and electrons in bulk BP reported by previous experiments in the 1980's [11]. Due to the anisotropic effective mass, the highest mobility values are observed are observed in transport aligned with the low-mass, AC direction. Since the applicability of BP as a channel material in ultra-short channel metal-oxide-field-effect-transistors (MOSFETs) requires the use of few-layer BP it is important that high mobility values are maintained in ultra-thin BP films. This was simulated in reference [32]

and results indicate electron and hole mobilities of ~1,100 $cm^2/V{\cdot}s$ and ~1400 $cm^2/V{\cdot}s$ respectively for monolayer BP for transport in the AC direction and electron and hole mobility of ~80 $cm^2/V{\cdot}s$ and ~400 $cm^2/V{\cdot}s$ respectively for monolayer BP in the ZZ direction. This indicates that a reasonably high mobility is expected BP in the light mass AC direction even as it is scaled to a monolayer, although the mobility in the heavy mass ZZ direction is much lower. However, experimental verification of these results is important, especially in a field-effect-transistor (FET) geometry that would be employed in real devices. To the best of my knowledge, the highest room temperature field-effect mobility experimentally demonstrated is 5,200 $cm^2/V{\cdot}s$ for holes [33] and ~ 1,400 $cm^2/V{\cdot}s$ for electrons [34]. These values are similar to the predicted values for 5-layer BP, however the devices are not fabricated using high-k gate dielectrics which are the CMOS industry standard. To this point, BP transistors fabricated with more realistic high-k gate dielectrics have shown moblility < 200 $cm^2/V{\cdot}s$ [30] representing an area in need for improvement before transistors with performance comparable to silicon transistors can be fabricated.

1.2 Growth and Transfer of Black Phosphorus

Currently, the primary way to obtain few-layer black phosphorus samples is by mechanical exfoliation from a bulk crystal. Bulk BP grown using multiple methods, the Bridgman method was the first method used in 1914 to convert white phosphorus to black phosphorus under high pressures and temperatures. This general method remains the gold standard for producing BP crystals of the highest purity however it requires pressures as high 1.3 GPa [7] making it difficult and costly. Lower pressure chemical vapor transport growth methods have been demonstrated for an easier path to synthesizing BP [35]–[37]. In this work, bulk BP crystals grown via a chemical vapor transport method were purchased

from Smart Elements® and thin films were obtained via mechanical exfoliation using scotch tape. BP films were then transferred to a poly-dimethylsiloxane (PDMS) stamp on top of a glass slide which is attached to a micro-manipulator and used to align thin BP flakes with pre-patterned structures under an optical microscope. The PDMS is then lowered down until contact is made with the sample, the BP flake is held onto the sample with the Van der Waals force and is released from the PDMS as it is lifted back up. This method is similar to the method employed in reference [38] and is shown in Figure 1.4.

While these methods are effective for experimentation and making discrete devices, there are not suitable for large scale manufacturing of circuits using black phosphorus.

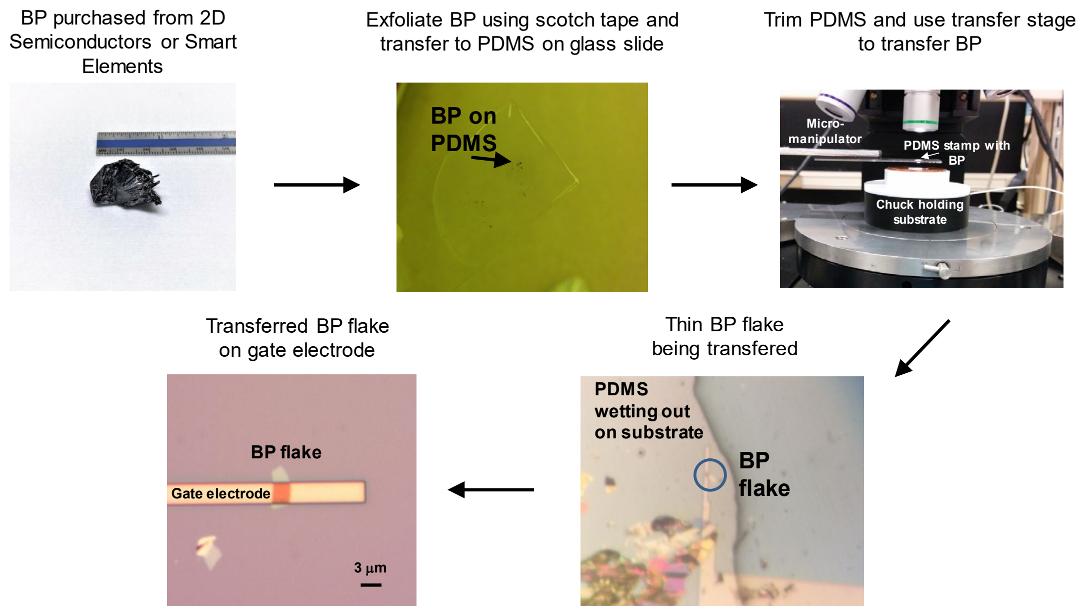


Figure 1.4 Process flow for transferring BP from bulk crystals onto pre-patterned substrates.

Therefore, it is important to find ways to grow large, uniform, thin BP films that can be transferred to and cover large substrates. There have been some initial reports of attempts large area growth of BP including a chemical vapor deposition (CVD) method which grew BP directly onto a substrate but only achieved sparse growth of small BP flakes (< 20 μm)

[39] and one method which was a modified version of the Bridgman method, converting red phosphorus to black phosphorus directly on a sample [40]. This method produced larger crystals up to 70 μm however it utilizes a high pressure method which may make it a costly solution. In any case, these early works represent a step in the right direction for large area growth of BP.

1.2.1 Air Stability of Black Phosphorus

While BP is stable relative to red and white phosphorus, it still suffers from degradation in air. BP has been discovered to react with H_2O and O_2 [15], [41]–[43] in a reaction that is accelerated by light [44]. Reference [41] suggests that BP primarily reacts with O_2 forming P_xO_y species on the surface of the BP. However, the formation of P_xO_y changes the surface from being hydrophobic to hydrophilic which then promotes the

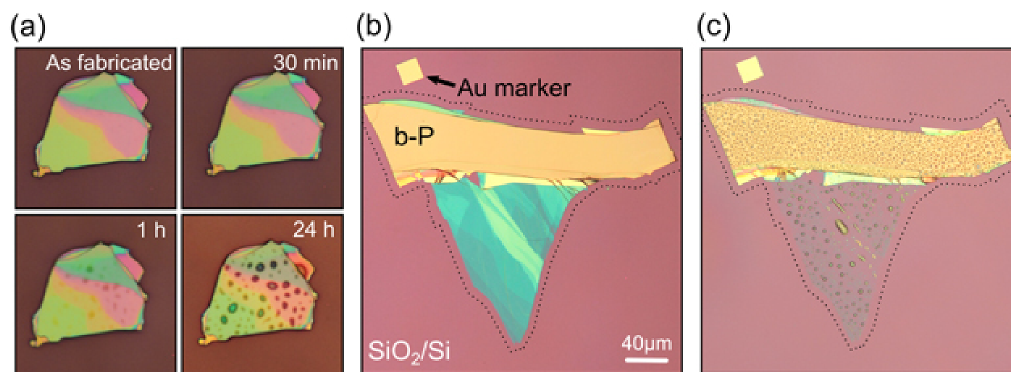


Figure 1.5 (a)-(c) Optical images of BP before and after degradation from prolonged air exposure. Thinning is observed along with bubbles that correspond to adsorbed moisture. © IOP Publishing. Reproduced with permission from reference 15. All rights reserved. doi:10.1088/2053-1583/1/2/025001

absorption of water which therefore accelerates the reaction and also results in the formation of $H_xP_yO_z$ (phosphoric acid). Experimental work like that shown in Figure 1.5 displays that thin BP films left in ambient conditions will degrade and form droplets on the surface indicative of water adsorption.

Additional experiments shown in Figure 1.6 have also shown that the degradation of BP has adverse effects on the electrical performance of BP in FETs. A decrease in ON/OFF ratio of the device and a decrease in mobility is observed with exposure to ambient air until the device eventually becomes open circuit after 50 hours [43]. This degradation means effective passivation of BP must be achieved in BP devices in order for them to be viable for most applications. Several passivation techniques have been effectively utilized including atomic layer deposition (ALD) deposited Al_2O_3 [43], [45], preventing water and oxygen from reaching the surface of the BP. Figure 1.6 demonstrates

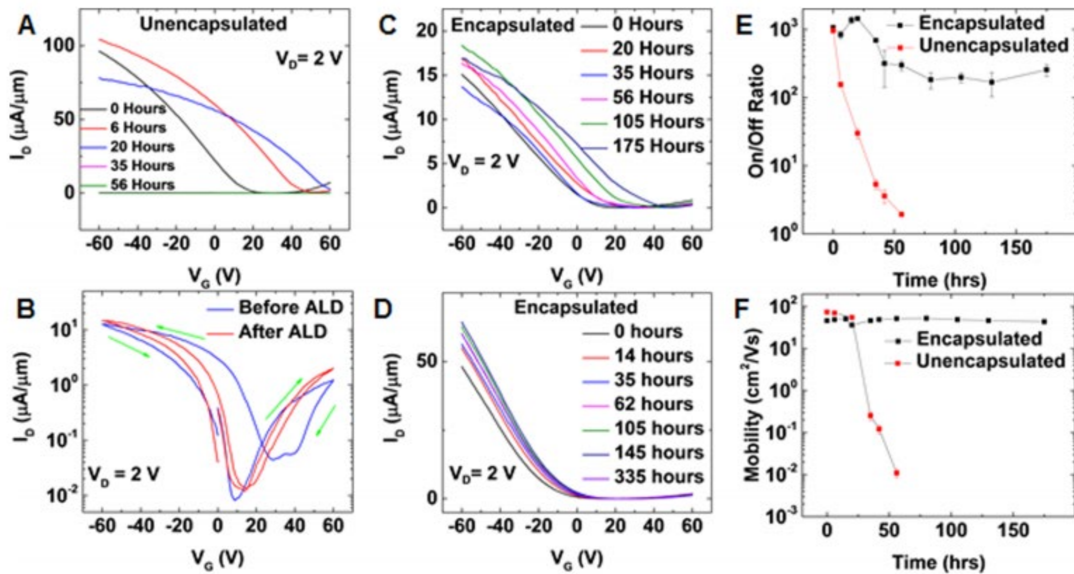


Figure 1.6 Transfer characteristics of passivated and unpassivated BP MOSFETs measured after different periods of air exposure. (d) Represents a device with Ni contacts while the rest of the plots are from devices with Ti contacts. Al_2O_3 proves to be an effective passivation layer. Reprinted with permission from reference [43] Copyright 2014 American Chemical Society.

BP FETs passivated with Al_2O_3 show no degradation after 8 months [45]. Two dimensional hexagonal boron nitride (h-BN) has also been demonstrated as an effective passivation layer [46]. In addition to these methods, chemical functionalization and polymer coatings

have also shown to improve the stability of BP in air [47]. Al_2O_3 passivation is the primary technique used in this work to protect BP devices.

These passivation techniques make reliable BP devices possible however the issue of BP degradation in ambient conditions during the device fabrication remains. Several methods including performing BP exfoliation in inert environments as well as vacuum have been employed however these techniques may not practical in a manufacturing setting and this remains an issue when considering the manufacturability of BP devices. However, there have been some of examples of using the degradation of BP enable unique uses or processes. One such thinning process will be the subject of chapter 2 of this work. One other interesting use of the instability of BP is its potential clinical use, specifically in novel cancer therapies where the optical and electronic properties of BP provide novel functions and its biodegradability means it does not stay in the body for long periods of time [48], [49].

1.3 Black Phosphorus MOSFETs

While the unique properties of BP are potentially attractive for many different applications such as opto-electronic devices, flexible thin-film transistors [50], radio-frequency (RF) transistors [51], and more. The application that has perhaps been the biggest driver for interest in BP is the use in advanced CMOS technologies which could extend the future of Moore's law and maybe even revive Dennard scaling. CMOS scaling which has followed Moore's law has been the key force behind the rapid increase in computing power and computing capabilities over the past few decades, and with fears of a slowdown or even a halt in this trend, any new material or device technology that shows promise for enabling its continuation naturally garners immense interest.

The limitations of current materials systems and device architectures that inhibit the long term future of CMOS scaling come primarily down to their inability to achieve good electrostatic gate control in order to suppress short channel effects as channel lengths become smaller. Short channel effects lead to unacceptably high source to drain leakage currents in the off-state of a transistor and therefore should be avoided. One parameter used to characterize the ability of a transistor to achieve good electrostatic gate control based on geometric and material properties is the natural scaling length (λ). The natural scaling length is derived from solving Poisson's equation in the channel region of a single gate, double gate, or gate-all-around transistor. It is understood that in order to prevent short channel effects and acceptable subthreshold performance the effective gate length of a transistor should 5 – 10 times the natural scaling length [52]. The equations for the natural scaling length in single gate, double gate, and gate-all-around transistors are shown below in equations 1.1-1.3 respectively.

$$\lambda_1 = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} t_{ox} t_{ch}} \tag{1.1}$$

$$\lambda_2 = \sqrt{\frac{\varepsilon_{ch}}{2\varepsilon_{ox}} t_{ox} t_{ch}} \tag{1.2}$$

$$\lambda_3 \approx \sqrt{\frac{\varepsilon_{ch}}{4\varepsilon_{ox}} t_{ox} t_{ch}} \tag{1.3}$$

From these equations, the channel thickness requirement for a gate-all-around silicon (best possible geometry) transistor with an effective gate length of 5 nm (λ = 1 nm) and a gate oxide thickness (SiO_2) of 1 nm is 1.3 nm. Unfortunately, as many bulk materials thicknesses scale below ~3 nm, the mobility can decrease [53] and the band gap can increase due to quantum confinement effects [54], therefore if sub-5 nm gate length transistors are to be realized other materials systems will likely be needed to replace silicon. IRDS recommends high mobility Ge or III/V materials like InGaAs to replace Si in order to improve drive current as silicon mobility degrades with scaled dimensions [55]. However, these other bulk materials are still subject to quantum confinement effects at around 5-6 nm which could prevent their use at these very short gate lengths (< 5 nm) where channel dimensions must be ~ 1 nm.

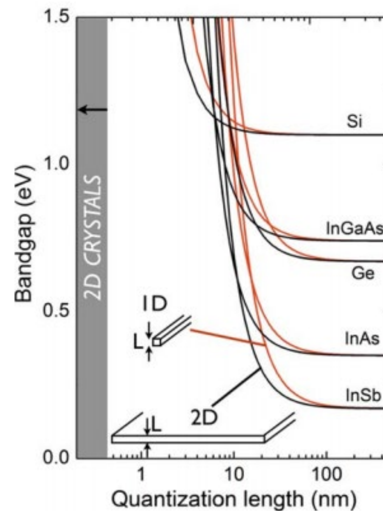


Figure 1.7 Qualitative plot showing the effects of quantum confinement on bulk materials. © 2013 IEEE Reprinted with permission from reference [54].

Because of these limitations of bulk materials, layered materials that can be scaled to sub-1 nm thicknesses with good electrical characteristics present a potential path forward to achieving sub-5 nm gate lengths. Initial interest in these layered materials, often called

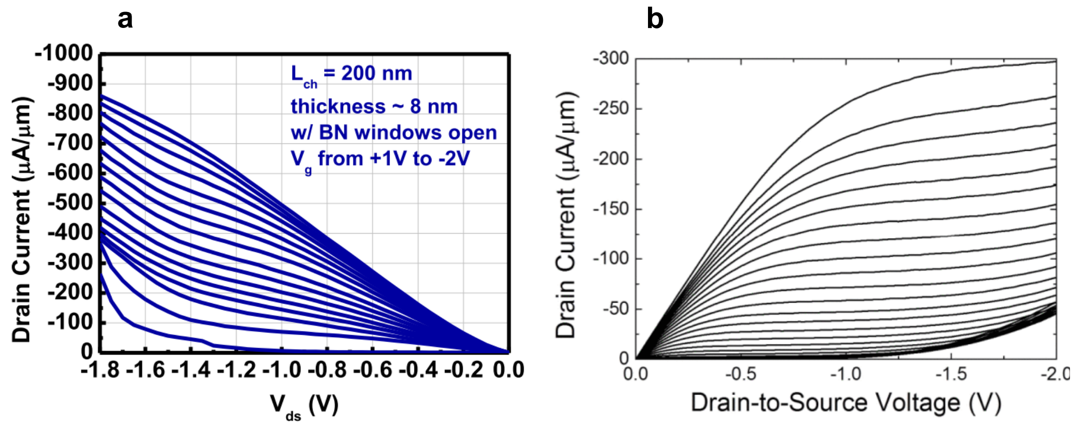


Figure 1.8Output characteristics of two high performance BP MOSFETs. (a) h-BN encapsulated BP MOSFET © 2016 IEEE. Reprinted, with permission, from reference [59]. (b) BP MOSFET using a high-k gate dielectric © 2015 IEEE. Reprinted, with permission, from reference [60].

two-dimensional materials (2D materials) focused on graphene and transition-metal-dichalchogenides (TMDs) however graphene is a semi-metal with no band gap rendering it not applicable as a channel material in transistors [56]. TMD materials do have moderate band gaps however, they suffer from relatively low mobility (~200 cm^2/V·s for MoS_2) and large effective masses (0.45 for MoS_2) which makes it difficult to realize transistors with large drive currents [57]. The limitations of these materials led to the exciting re-emergence of black phosphorus since it is a 2D semiconductor with a moderate band gap and mobility over 1,000 cm^2/V·s. There have been a number of demonstrations of p and n-type BP transistors which have displayed high ON-state performance (high I_{ON}) [58]–[61]. The best BP MOSFET ON-state performance reported to our knowledge is from reference [59] where they used h-BN to passivate the BP and create a defect free interface which enabled high BP mobility (144 cm^2/V·s). They reported I_{ON} = 850 μA/μm and transconductance (g_m) = 340 μS/μm. This appears to be the highest absolute performance achieved however, the use of h-BN may not be suitable in scaled CMOS device. A work by our group shows

the highest performing BP which uses a conventional high-K gate dielectric (HfO_2). We reported I_{ON} = 300 μA/μm and g_m = 250 μS/μm, these values were limited by a lower than expected mobility (~ 44 $cm^2/V{\cdot}s$) which was likely due to air exposure and phonon scattering associated with the HfO_2 gate dielectric [60]. The I_D vs. V_{DS} or output characteristics displaying the good ON-state performance of these devices is shown in Figure 1.8.

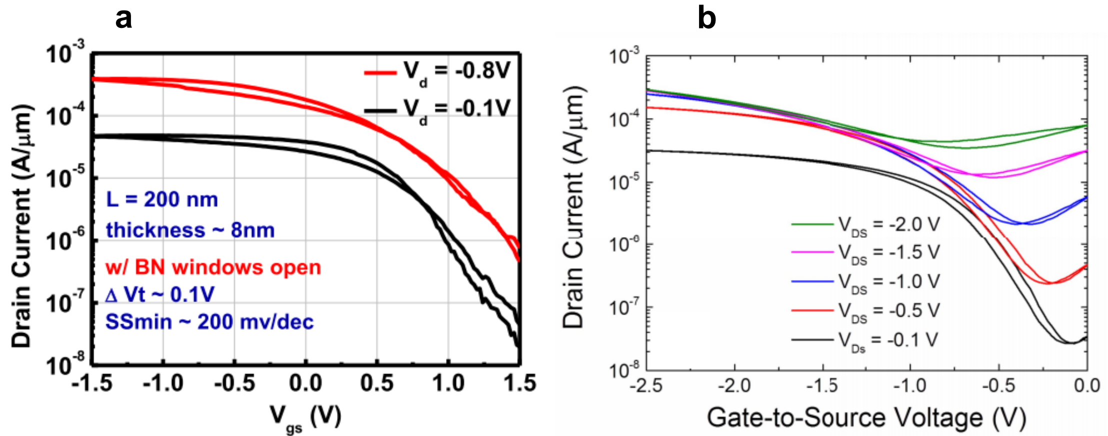


Figure 1.9 Transfer characteristics of the two high performance BP MOSFETs from Figure 1.8. (a) h-BN encapsulated BP MOSFET © 2016 IEEE. Reprinted, with permission, from reference [59]. (b) BP MOSFET using a high-k gate dielectric. © 2015 IEEE. Reprinted, with permission, from reference [60].

These early demonstrations displayed the potential of BP for achieving ON-state performance close to or better than Si in advanced MOSFETs however in order for BP to be truly viable as a Si replacement, the OFF-state or subthreshold performance must also be acceptable. A transistor with good OFF-state performance has low I_{OFF} and a steep subthreshold slope (*SS*), so the device can be turned on from a very low current state to a high current state with as little voltage as possible. In these early device demonstrations, OFF-state performance was a severe limitation. Figure 1.9 shows the I_D vs. V_{GS} or transfer characteristics of the same device in which the output characteristics were shown in Figure

1.8. From these characteristics, it is observed that at V_{DS} values close to CMOS supply voltages (~1 V) the max I_{ON}/I_{OFF} is less than 10^3. This is a major issue because the International Technology Roadmap for Semiconductors (ITRS) requires operational I_{ON}/I_{OFF} greater than 10^4. In conjunction with these poor on-to-off ratios, the subthreshold slope in these BP FETs are also quite poor at > 300 mV/dec in both devices whereas current CMOS devices operate with a SS ~ 70 mV/dec [62]. It is apparent especially in Figure 1.9 (b) that the subthreshold performance becomes worse as V_{DS} increases. This comes from the efficient ambipolar carrier injection at the drain as the transistor is being turned off and large electric field are generated at the drain contact. This phenomenon is commonly called gate-induced-drain-leakage (GIDL) and is especially high in BP due to its low effective mass, direct band gap, and small band gap at larger thicknesses which results in a small Schottky barrier at the drain. These characteristics, along with the use of gated, Schottky contacts in these initial demonstrations result in large ambipolar carrier injection due to a large component of thermionic emission over the drain Schottky barrier as well as efficient tunneling through the Schottky barrier. This issue was thoroughly characterized in reference [63] where a transport model combined with experimental results was used to demonstrate the effect of this ambipolar carrier injection in BP MOSFETs. Simulated I_D vs. V_{GS} curves and band diagrams shown in Figure 1.10 display how ambipolar carrier injection effects the subthreshold performance in BP MOSFETs with Schottky contacts and band-edge contacts.

From Figure 1.10 it is clear that Schottky contacted BP MOSFETs suffer from subthreshold performance degradation because of ambipolar carrier injection at the drain. This GIDL current puts a lower limit on I_{OFF} at the $V_{GS} - V_{MIN}$ point where source current

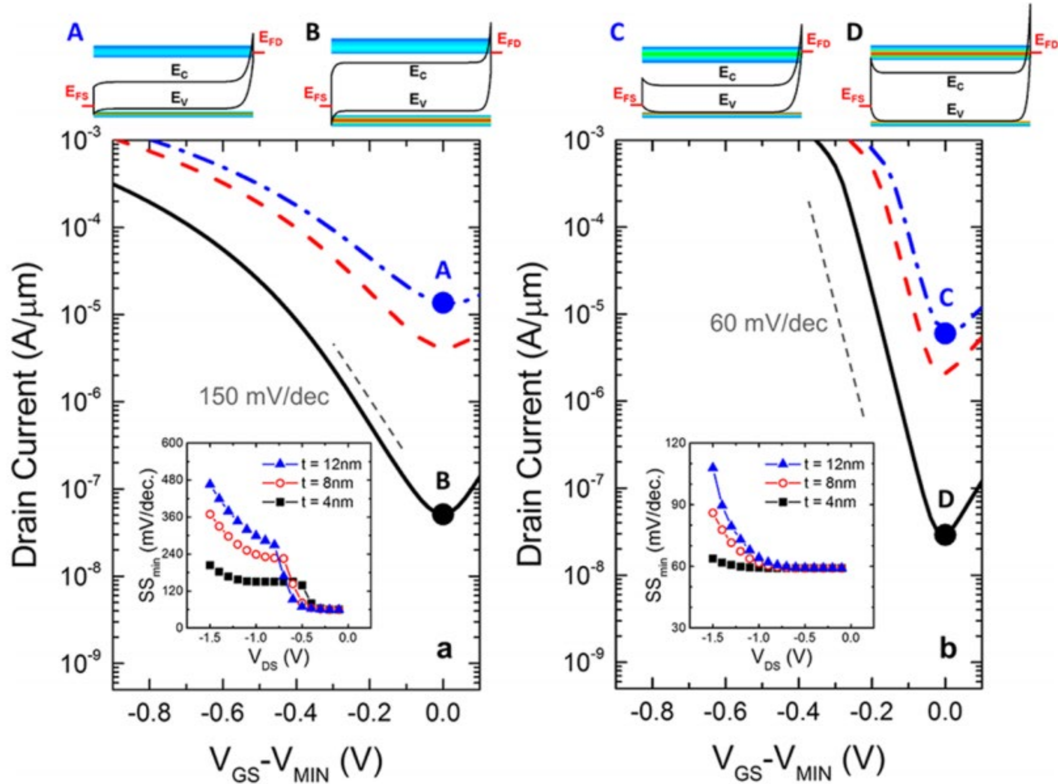


Figure 1.10 Simulated transfer characteristics and band diagrams for a Schottky contacted BP MOSFET and a band edge contacted BP MOSFET. (a) and (b) show the Schottky device with a small and large band gap respectively. (c) and (d) show the band edge device with a small and large band gap respectively. The transfers show how SS and I_{OFF} degrades due to ambipolar current. Adapted from reference [63]

and drain current are equal. The drain current being high is the primary reason that I_{ON}/I_{OFF} is poor in Schottky contacted BP MOSFETs. However it is also apparent that the ambipolar current degrades the subthreshold slope both because the ambipolar current at the drain becomes higher than the current injected at the source before device enters the true subthreshold regime (when current is limited primarily by thermionic emission over the energy barrier in the channel) and because even when the device is in the true subthreshold regime, the ambipolar current is increasing as the device is turning off which degrades the

subthreshold slope. Because of these subthreshold performance degradation mechanisms, it is important to engineer devices with suppressed ambipolar carrier injection.

Utilizing a band edge contact is one way to suppress ambipolar current and Figure 1.10 shows how this improves the *SS* in BP MOSFETs. However because of Fermi level pinning, band-edge contacts have not be achievable in BP. Because of this, other ways of suppressing ambipolar current in BP MOSFETs while retaining good I_{ON} mmust be utilized. Two ways of doing this are discussed in chapters 2 and 3 in this work. One method utilizing the thickness tunable band gap of BP in order to fabricate a heterostructure MOSFET with a large band gap and thus a larger Schottky barrier at the drain which suppresses ambipolar current while maintaining good I_{ON}. And another method utilizing a novel electrostatic doping technique to dope the source and drain contacts, making them behave more like band-edge contacts. Employing techniques like this will be essential in order to create BP MOSFETs with high ON-state performance as well as adequate subthreshold performance.

1.4 Black Phosphorus TFETs

The previous section discussed the potential of BP as a post-silicon channel material for MOSFETs in advanced CMOS circuits as channel lengths are scaled down to less than 5 nm. This would enable the continuation of Moore's law for years to come, however even in transistors with ideal subthreshold behavior, Dennard scaling, which enables the increase in CMOS speed at a constant power, would remain halted because of the inability to reduce the supply voltage (V_{DD}). The inability to scale the supply voltage is a result of the fundamental limitations for the minimum subthreshold slope (60 mV/dec at room temperature) in a conventional MOSFET. This fundamental limit arises from the Fermi-

Dirac distribution of carriers in a semiconductor and the mechanism which is used to turn off a conventional MOSFET. A conventional n-MOSFET is turned off by using a gate voltage to tune the potential of the conduction band in the channel so that the semiconductor band gap blocks electrons from the source from being transported to the drain. The efficiency of this mechanism is limited by the fact the carriers follow a Fermi-Dirac distribution which results in an exponentially decaying, high energy "Fermi tail" of carriers, ultimately limiting how many carriers can be "blocked" with any given decrease in channel potential. This limit for the minimum achievable *SS* is quantified in Equation 1.4.

$$SS_{Min} = \ln(10)\frac{kT}{q}(1+\frac{C_s}{C_{ox}}) \tag{1.4}$$

Where k is equal to Boltzmann's constant, T is the temperature in Kelvin, q is the charge of an electron, and C_s and C_{ox} correspond to the respective semiconductor depletion and gate oxide capacitances. The first term in this equation ($\ln(10)\frac{kT}{q}$) is a result of the Fermi-Dirac distribution of carriers while the second term ($1+\frac{C_s}{C_{ox}}$) is often referred to as the body factor and quantifies the efficiency of the gate. At room temperature (T = 300 K), in the ideal case where the all the potential from the gate drops across the semiconductor ($\frac{C_s}{C_{ox}} = 0$), this equation evaluates to ~ 60 mV/dec. This subthreshold slope limit of 60 mV/dec in conventional MOSFETs has prevented V_{DD} reduction in advanced CMOS devices and has resulted in the exploration of novel device concepts which could potentially beat this limit, and thereby reignite Dennard scaling.

A novel device called the tunneling-field-effect-transistor (TFET) was proposed as a possible way to overcome this limit in 2004 [64]. The minimum *SS* of a TFET is not

proportional to $\frac{kT}{q}$, therefore SS < 60 mV/dec can theoretically be achieved. The way that TFETs eliminate this $\frac{kT}{q}$ proportionality enabling sub 60 mV/dec SS, is by utilizing a band gap filtering effect in which the high energy tail of carriers is effectively cut-off by the semiconductor band gap in the source region. In order to achieve this filtering effect in an n-TFET, a transistor is designed with a heavily doped p-type source, a gate-tunable,

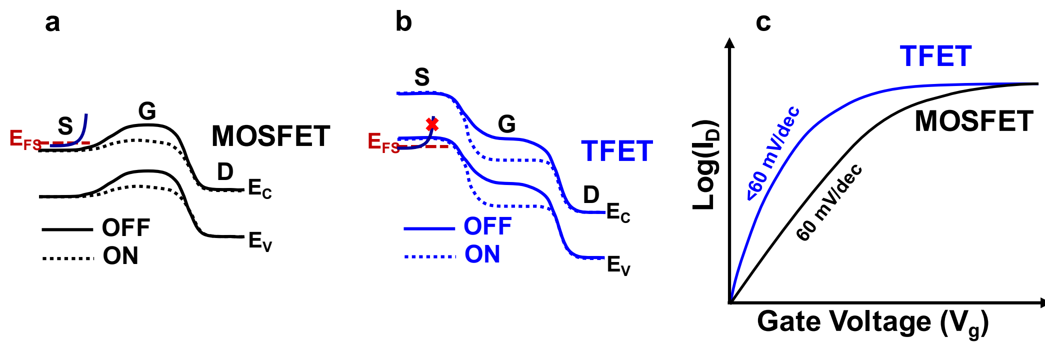


Figure 1.11 The band diagram of a MOSFET in the OFF and ON state is represented in (a) with the Fermi tail represented by the curved line at the source. (b) The band diagram of a TFET in the OFF and ON state with the Fermi tail shown being cut-off by the band gap in the source. (c) Cartoon demonstration of the improved characteristics of a TFET over an ideal MOSFET.

intrinsically doped, channel, and a heavily doped n-type drain. The transistor is turned on and off by using the gate to tune the channel potential in order to open and close a band-to-band-tunneling (BTBT) window between the source and the channel [65], [66]. This operation and how it contrasts with a conventional MOSFET is shown in the band diagrams and cartoon transfer characteristics in Figure 1.11.

Despite the initial promise of TFETs, it has proven very difficult to realize TFETs with both SS < 60 mV/dec at room temperature and high I_{ON}. Initial demonstrations utilized Si due to it's natural CMOS compatibility and achieved SS < 60 mV/dec, but low I_{ON} (<10 μA/μm) [67] due to the relatively large effective mass and the large, indirect band gap of

Si which causes poor tunneling efficiency. Because of these material limitations of Si, low-mass, direct gap III-V materials have also been explored for use in TFETs, and initially demostrated higher I_{ON} (50 μA/μm), however the smaller band gap combining with trap effects resulted in a *SS* > 60 mV/dec [68]. In order to optimize TFET performance heterojunction TFETs were proposed [69] and eventually a III/V heterostructure TFET was

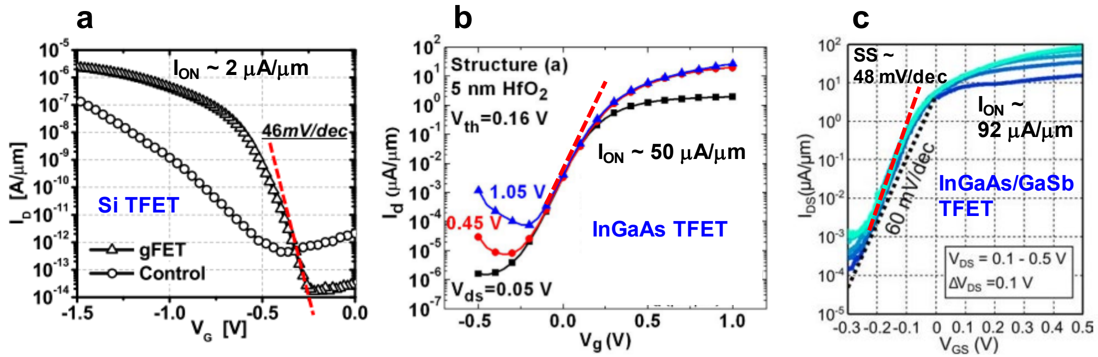


Figure 1.12 (a) transfer characteristics for a Si TFET reprinted with permission from reference [67] © 2010 IEEE. (b) transfer characteristics for an InGaAs TFET reprinted with permission from reference [68] © 2011 IEEE. (c) transfer characteristics for an InGaAs/GaSb heterostructure TFET reprinted with permission from reference [70] © 2016 IEEE.

utilized to demonstrate the highest performing TFET to date shown in Figure 1.12 with SS_{MIN} = 48 mV/dec and I_{ON} as high as 92 μA/μm [70]. This device utilized small band gap InGaAs at the source and large band gap GaSb at the drain in order to achieve high tunneling efficiency at the source while suppressing parasitic tunneling at the drain. It was a promising result, however this heterostructure device is complex to fabricate and is ultimately limited in it's scalability because of the use of bulk materials.

In a similar manner to MOSFETs, this lack of scalability has again led researchers to explore 2D materials, this time for their use in TFETs [71]. Among these, black phosphorus has perhaps shown the most promise due to it's unique properties such as it's anisotropic effect mass (low in the AC direction) and tunable direct band gap which enable

high tunneling efficiencies and present numerous engineering levers to play with in order to optimize ON and OFF state performance. A number of simulation based demonstrations of BP TFETs have been published [72]–[78] and show the promise of BP as TFET channel material to achieve even higher performance than the current state-of-the-art with much simpler designs. One such homojunction black phosphorus TFET simulation reported I_{ON} ~ 1 mA/μm with SS < 60 mV/dec. This type of performance would be unrivaled by other demonstrated TFETs, however what may be even more compelling about BP as a channel material in TFETs are it's unique properties like anisotropic effective mass and tunable band gap that give engineers ways to optimize performance by reducing ambipolar current while maintaing high I_{ON}. Off-state leakage due to ambipolar current is a significant issue in TFETs because source and drain tunneling is symmetric unless design tricks or novel device structures are used in order to supress it.

There have been two simulation based papers which have utilized the tunable band gap of BP in order to achieve high I_{ON} while reducing I_{OFF} and decreasing SS [72], [76]. One such example from reference [72] which is shown in Figure 1.13 simulates a device

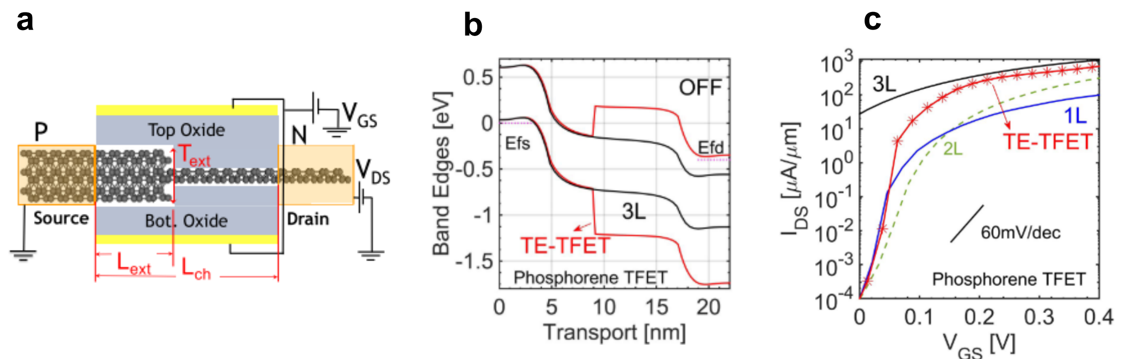


Figure 1.13 (a) Side view cartoon of a thickness-engineered BP TFET. (b) Energy band diagram of the same TFET. (c) TFET transfer characteristics which show the advantage of the thickness engineered BP TFET over homojunction devices. © 2016 IEEE. Figure reprinted with permission from reference [72].

using 3-layer BP at the source and monolayer BP at the drain in order to achieve high tunneling efficiency at the small band gap source and low tunneling efficiency at the large band gap drain. The transfer characteristics show the how the heterostructure BP TFET offers optimized performance over homojunction BP TFETs by achieving I_{ON} close to the level of the thicker BP TFET and I_{OFF} close to the monolayer BP TFET. By doing this they also report two orders of magnitude higher I_{60} than any homojunction BP TFET. I_{60} is an important metric in TFETs because it measures the current at which the *SS* = 60 mV/dec, meaning devices with a high I_{60} achieve steep *SS* at high current values where it is the most important.

Another simulation based paper utiltized the anisotropic effect mass of BP to supress I_{OFF} while maintaining high I_{ON} [75]. Because of the exponential depence of tunneling efficiency on effective mass, the simulated band-to-band-tunneling current was 3 orders of magnitude higher in the AC direction than it was in the ZZ direction. Simulations showed that designing a device with an L-shaped gate optimized I_{ON} and I_{OFF} and enabled viable

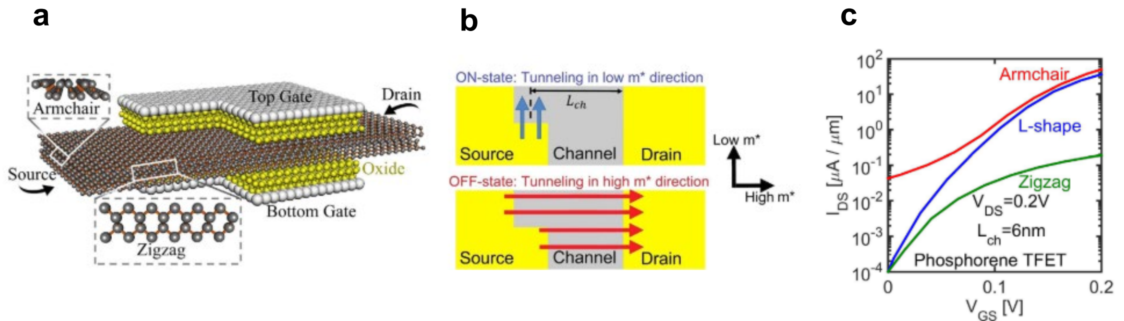


Figure 1.14 (a) and (b) show the side view and top view cartoon of an L-shaped BP TFET. (c) shows the TFET transfer characteristics which show how the L-shaped BP TFET optimizes ON and OFF-state performance isotropic AC and ZZ devices. Figures adapted with permission from reference [75]. According to the creative commons license. https://creativecommons.org/licenses/by/4.0/legalcode

transistor operation at V_{DD} = 0.2V at channel lengths close to 2 nm, only a few atoms long.

This device design and transfer characteristics are shown in Figure 1.14.

These simulation based works on BP TFETs show that BP may be an ideal TFET channel material and could represent a potential toward reigniting Dennard scaling by beating the thermal *SS* limit of 60 mV/dec and enabling lower V_{DD} down to 0.2V. However, TFETs simulations typically assume ideal interfaces and materials, and many are based on devices that are difficult to fabricate in a lab. In addition to this, because TFETs utilize band-to-band-tunneling, they are extremely sensitive to process variations as well as defect inducted traps which introduce parasitic leakage mechanisms. Because of these things, performance of experimentally demonstrated TFETs have lagged far behind simulated TFETs, therefore it is extremely important to be able to demonstrate the ability to fabricate TFETs in order to examine their true potential and what practical issues may need to be solved to in order to reach the ideal performance shown in simulations. The first experimental demonstration of a BP TFET was presented by me in 2017 and showed *SS* close to the thermionic limit at low temperature as well as BTBT current anisotropy in BP [31]. This work will be the subject of chapter 4 in this paper. Later, Complimentary BP TFETs were demonstrated experimentally in reference [79]. These works represent first experimental demonstrations of BP TFETs and performance did not come close to the simulated devices for reasons which will be detailed in further sections. Chapter 5 of this work will also present the first experimental demonstration of an L-shaped BP TFET which utilizes the anisotropic effective mass of BP in order to suppress I_{OFF} while maintaining high I_{ON}.

1.5 Dissertation Outline

In this dissertation I will present my own experimental work on engineering novel

transistors utilizing the unique properties of black phosphorus to improve OFF-state or subthreshold performance while maintain the good ON-state performance which BP offers. First, in chapter 2, heterostructure BP MOSFETs are presented which utilize the thickness-tunable band gap of BP to suppress ambipolar carrier injection at the drain, improving OFF-state performance while maintaining good ON-state performance. This device was enabled by the development of a patternable, layer-by-layer thinning process which allowed the BP thickness to be tuned in the MOSFET source and drain regions. Next, in chapter 3, BP MOSFETs with electrostatically doped source and drain contacts are presented. Electrostatically doped contacts enable band-edge like contacts which suppress ambipolar current injection at the drain and improved subthreshold performance is demonstrated. Electrostatic doping is enabled by the design and fabrication of a novel triple-gated device structure which allows independent gate control in BP source, drain, and channel regions. In chapter 4, this electrostatic doping scheme to experimentally demonstrate BP TFETs for the first time resulting in *SS* close to the thermal limit at low temperature as well as the first observation of BTBT current anisotropy in BP. Finally, in chapter 5, an L-shaped BP TFET is presented and experimentally demonstrates the use of the anisotropic effective mass in order to suppress ambipolar drain tunneling in a BP TFET and improve I_{ON}/I_{OFF} and subthreshold slope compared with isotropic BP TFETs.

CHAPTER 2 HETEROSTRUCTURE BP MOSFETS

The scalability of BP and its relatively high electron and hole mobilities in the AC crystal direction has driven research interest in BP as a post-silicon channel material in advanced CMOS technologies. As previously described, BP MOSFETs with high ON-state performance have been demonstrated however they have suffered from poor OFF-state performance with unacceptably high *SS* and I_{OFF} primarily due to ambipolar carrier injection from the drain. These limitations are the motivation for this section where the tunable band gap of BP is used in order to fabricate heterostructure MOSFETs with suppressed ambipolar current while maintaining good I_{ON}. The band gap of BP varies from 0.3 eV (bulk) to 1.5−2.0 eV (monolayer) and is direct at the Γ-point. In MOSFETs, the band gap impacts the I_{ON}/I_{OFF} as well as the Schottky barrier height at metal−semiconductor interfaces. In most materials, the band gap cannot be controlled in a practical manner, making any type of tunable performance difficult without using a different material. Before this study, the thickness dependence of the band gap in BP had primarily been studied simply by utilizing random variations in thickness resulting from mechanical exfoliation. These studies have yielded interesting results showing thickness-dependent ON/OFF current ratios in MOSFETs [80] and thickness-dependent photoluminescence spectra [15]. Other literature has reported controlled thinning of BP by use of plasma-based processes [81]–[83], ozone oxidation [84], laser oxidation [85], [86], and thermal sublimation [87]. However, these methods do not provide cyclical thinning, thereby requiring precise calibration of etch time. A layer-by-layer scanning probe nanopatterning method [88] has been demonstrated, but layer-by-layer precision is lost when the process is performed on insulating substrates that are necessary for device

fabrication. In this section, a robust, cyclical, top-down, BP thinning process that represents a novel method for precise BP thickness control is presented. This method also enables high spatial etch resolution, which gives it the potential to enable a plethora of novel devices including double-heterostructure light emitters and a variety of heterostructure FETs. This process is used to fabricate BP MOSFETs and compare the transport characteristics of the thick and thin regions, in addition to fabricating the first-ever lateral heterostructure BP MOSFET, which shows 3 orders of magnitude improvement in off-state leakage with minimal degradation to I_{ON}. Most of this work was published and is available in reference [89].

2.1 Layer-by-Layer Thinning of Black Phosphorus

The heterostructure BP MOSFET was fabricated using a novel layer-by-layer thinning process. The thinning process utilizes BP's inherent reactivity in air as the primary mechanism for controlled thinning. It has been shown by multiple groups [19], [41], [44], [90] that as BP is exposed to ambient atmosphere and light the top layer(s) react with the adsorbed H_2O and O_2 on the surface creating large bubbles and enlarged flake volumes consisting of P_xO_y and $H_xP_yO_z$ compounds after prolonged exposure (greater than one week). It has also been shown that some of these compounds volatize if the sample is annealed at a high temperature leaving behind a thinner version of the original BP along with some residues [41], [44]. Multiple works in the literature [41], [90]–[92] suggest that one of the reaction byproducts is P_2O_5 which is stable at high temperatures and could be a component of the residue which was observed in reference [41]. However, Edmonds *et al.*'s [92] photoelectron spectroscopy findings suggest that when ambient air exposure is limited (~ 5 minutes) the stable P_2O_5 does not form. Instead the findings provided evidence

for the formation of more volatile phosphoric acid or physisorbed oxygen and nitrogen. Experimental results presented in this chapter support the findings that if the ambient exposure time is limited, the BP surface reacts with the air and forms volatile compounds. These volatile compounds are then removed by the subsequent 300 °C anneal, with 300 °C being a temperature at which BP has been shown to remain crystalline [93]. Next, it will be shown that this property creates a platform for developing a cyclical thinning process for BP.

To investigate the use of this mechanism, a patterned thinning process was developed and used to fabricate samples containing BP flakes with spatially-controlled thickness variation. These patterned flakes were then characterized using optical microscopy, atomic force microscopy (AFM), Raman spectroscopy, and photoluminescence (PL) measurements. The procedure began by exfoliating BP (from Smart Elements™) using adhesive tape, then transferring the BP on the adhesive tape to a PDMS stamp. Next, the BP was transferred from the PDMS stamp to a 290 nm SiO_2 on p++ Si substrate using the process described in Section 1.2. Then the sample was immediately cleaned with solvents and spin coated with Poly(methyl methacrylate) (PMMA) to act as a temporary passivation to BP as well as an electron-beam lithography resist for the following pattering step. We then defined a pattern in the PMMA mask using electron-beam lithography (E-beam

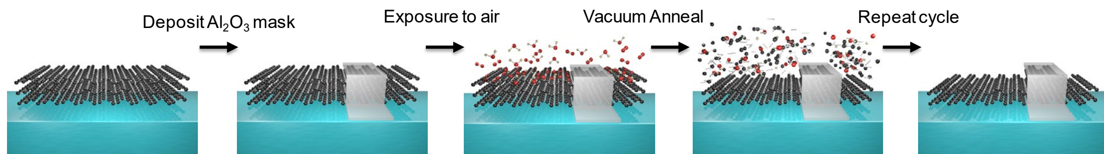


Figure 2.1 Cartoon representation detailing each important step in one cycle of the cyclic oxidation/annealing process.

lithography) and deposited 1.5 nm of Al via electron-beam evaporation, followed by removal of the PMMA mask in acetone. The thin layer of Al reacts with air and forms ~5 nm of Al_2O_3 which has been shown to protect BP from degradation as discussed in Section 1.2.1. Once the Al_2O_3 protection layer has been formed, the cyclic oxidation / annealing procedure is performed as shown in Figure 2.1. One cycle consists of a ~10 minute exposure to ambient atmosphere (where the environmental conditions are well-controlled at 20℃ and 45% relative humidity) followed by annealing in N_2 (20 sccm) at 300℃ at a pressure of approximately 1 Torr for ~10 minutes. These time scales were arrived at experimentally, however the process is not dependent on the anneal time and it will be shown later that the process is robust against variations in the air exposure time as well. The thinning cycles can be repeated until the desired thickness is reached. For all samples, an *in situ* deposition of 15 nm Al_2O_3 via atomic layer deposition (ALD) was performed after the last annealing step. This final Al_2O_3 layer acts as a protection layer for the entire sample so that characterization can be performed. Figure 2.2 shows optical micrographs after each cycle in the thinning process for a BP sample that underwent a total of 7 thinning cycles displaying a change in contrast after each cycle. A 3D topographic AFM image of this sample is shown in Figure 2.2(b).

AFM was used to characterize the thinning process by extracting the etch depth and measuring surface roughness. To determine the resulting thicknesses and accumulated roughness, statistical data was taken from rectangular regions of BP patterned flakes. Figures 2.3(a) and 2.3(b) show a typical patterned flake after 7 thinning cycles and how the thickness and roughness data were extracted. A two-dimensional height distribution mapping technique was used to extract the thicknesses of the thick and thin regions of the

patterned BP flakes (Figure 2.3(b)). The positions of the peaks indicate the thicknesses of

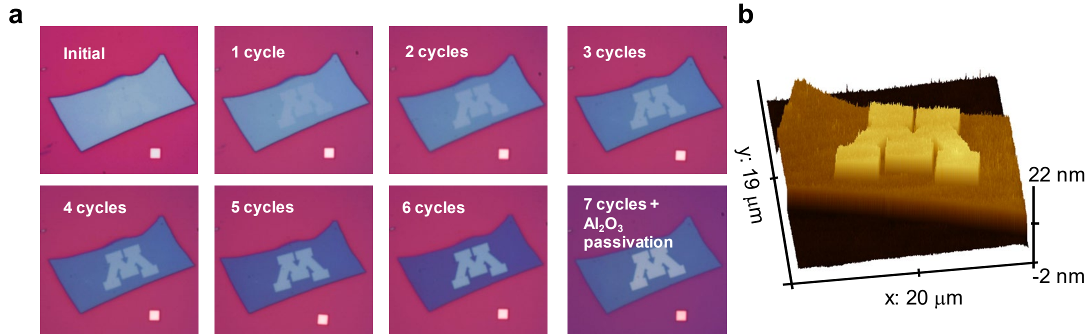


Figure 2.2 (a) Optical micrographs of sample after each thinning cycle. The M logo region is passivated with Al_2O_3 and the other flake regions are thinned in a cyclical manner, evident by the change in color/contrast. (b) 3D AFM representation of a patterned, thinned flake, where the vertical scale has been cropped at 23 nm to improve the image contrast.

the patterned BP flake (11.88 nm original, 8.74 nm after 7 thinning cycles) in addition to the Al_2O_3 mask (5 nm). Once the thickness of the Al_2O_3 mask is subtracted out, the thicknesses of the thick and thinned BP regions can be measured directly.

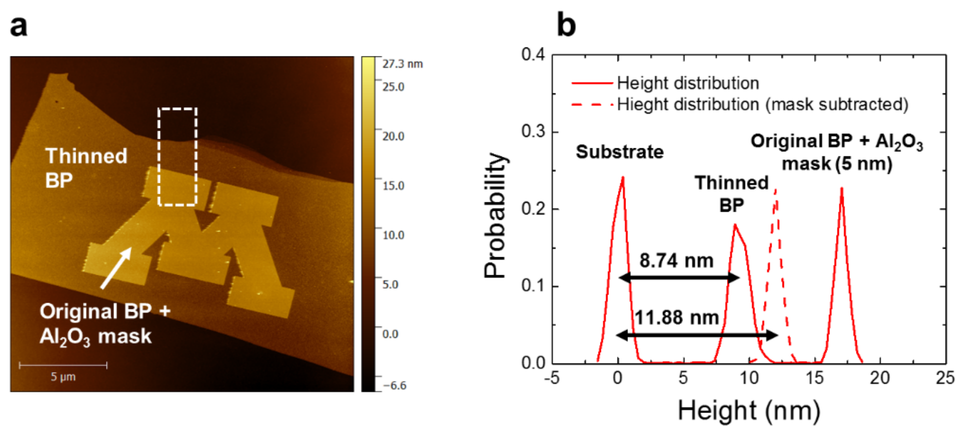


Figure 2.3 (a) AFM micrograph of the patterned BP flake. Dotted rectangle indicates region where height distribution was collected. (b) Height distribution chart of patterned BP flake with labels indicating the representation of each peak. The second solid red peak represents the thickness of thinned BP (8.74 nm), and the dotted red peak indicates the thickness of the thick BP region (11.88 nm).

Figure 2.4(a) shows the etch depth as a function of the number of thinning cycles collected across 11 patterned BP samples. The linear fit of the experimental data through the origin

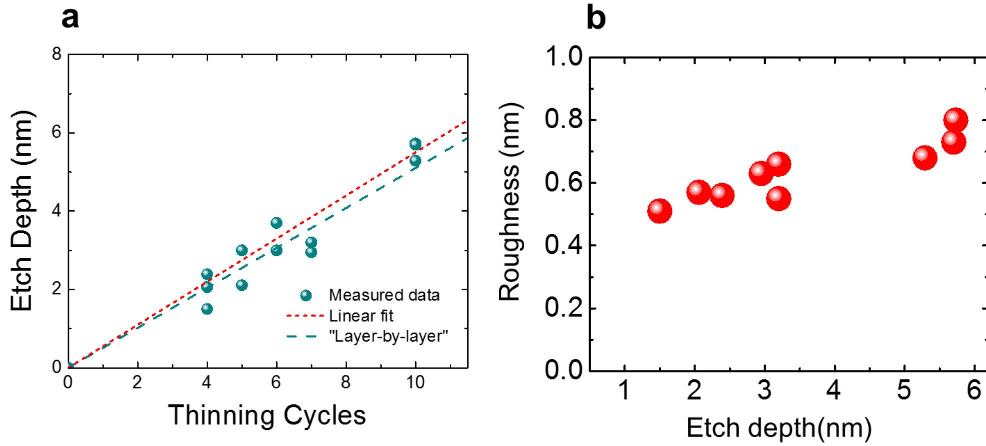


Figure 2.4 (a) BP etch depth versus number of thinning cycles for individual flakes, plotted alongside the expected layer-by-layer rate (dashed red line) and the linear fit through the origin (dashed green line). (b) Thinned flake roughness (rms) vs etch depth. Each point was collected from a separate BP flake.

gives a slope of 0.51 ± 0.08 nm/cycle. Given the experimental interlayer spacing of 0.55 nm, this result suggests that this is a layer-by-layer thinning process. The surface roughness of the thinned BP flakes was also extracted from the AFM data to provide an indication of flake quality and to determine the uniformity of the thinning process. In Figure 2.4(b), the flake root-mean-square (rms) roughness after thinning vs. the etch depth is plotted. The roughness extracted using the Gwyddion™ software package based upon the AFM scan from a roughly 2 × 2 μm^2 area. The data show a slight increase in the roughness with accumulated etch depth, going from 0.5 nm roughness after 1.5 nm of etching to 0.8 nm roughness after being etched 5.7 nm. The average roughness of the passivated unetched BP is 0.44 nm so, after the removal of 10 layers, the maximum additional roughness (0.36 nm) remains less than the thickness of single layer. This slight increase in surface roughness

could indicate some formation of non-volatile surface oxides during the air exposure step, however it will be shown later that crystalline BP still remains after thinning.

One primary advantage of this cyclical thinning process is its robustness to changes in the air exposure time and anneal time. The robustness of the process against changes in air exposure time is understood qualitatively from the observation that highly repeatable thinning results have been achieved (Figure 2.4(a)) while there is uncertainty in the exact exposure time throughout the fabrication process, particularly during the Al_2O_3 pattering process before the first N_2 anneal. Based upon this observation the sensitivity of the thinning process to the air exposure time was examined in a more quantitative manner by repeating the patterned thinning process with an increased air exposure time of 30 minutes. Figure 2.5 shows a side-by-side comparison of two patterned BP flakes that underwent 4 thinning cycles, one using ~10 minute air exposure steps and the other using ~30 minute air exposure steps. The etch depths were 1.99 nm and 2.07 nm respectively indicating that the etch rate is robust to small changes in the air exposure time. This result is significant because it indicates that precise control over BP thickness can be achieved in a process that does not require precise calibrations of etch times.

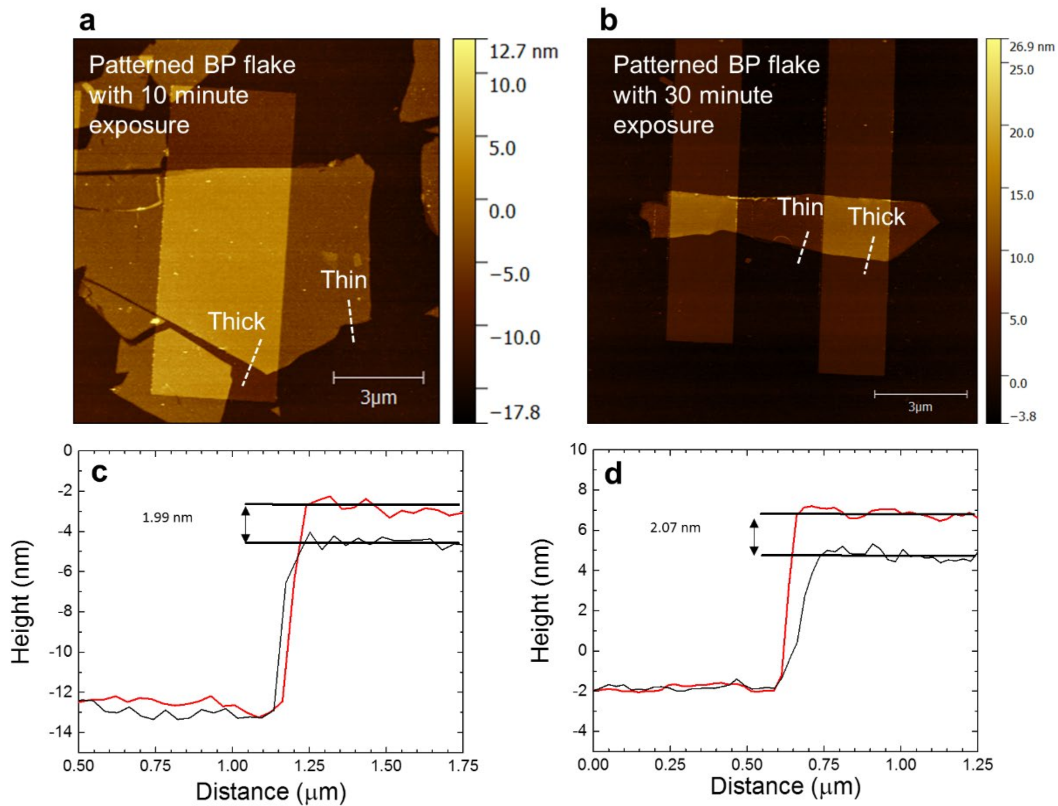


Figure 2.5 BP flakes fabricated using 4 thinning cycles with (a) 10 minute and (b) 30 minute air exposure steps. The step heights with 10 minute air exposures (c) and 30 minute air exposures (d) are shown and etch depths of 1.99 nm and 2.07 nm respectively are extracted showing little change in the etch rate as the air exposure time is increased to 30 minutes. This demonstrates that the cyclical oxidation and annealing thinning process is robust to small changes in air exposure time.

Overall, the combination of the linearity of the etch depth vs. cycle number, the low degree of accumulated roughness and the closeness of the etch depth per cycle to the known interlayer spacing provides evidence that the etching method proceeds in a layer-by-layer fashion. Of course, because each cycle takes 20 minutes, this is an inherently slow thinning process and is not practical if deep etching is required. However, the slowness and controllability of this method becomes advantageous when precise control over the number of layers is desired.

In addition to precise thickness control, another benefit offered by this thinning process is its ability to provide high spatial pattern resolution. Figure 2.6 shows an example of sub-150 nm lateral features consisting of 8 nm and 10 nm BP regions defined using electron-beam lithography. Further scaling is possible with optimization of the resist development and lift off processes, and therefore we believe this process could readily be scaled down

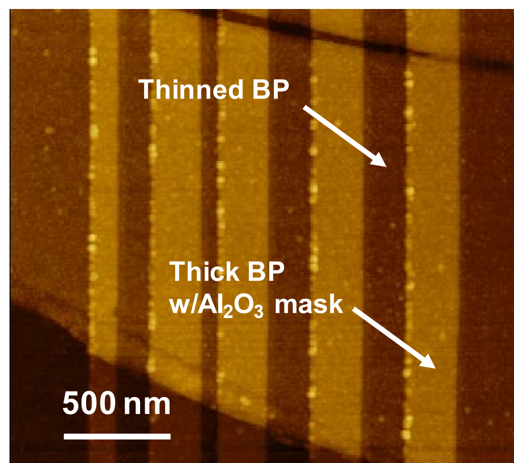


Figure 2.6 AFM micrograph of patterned BP flakes with sub-150 nm features.

to few-nanometer-scale dimensions. It also should be noted that this thinning process could be utilized to create self-aligned heterostructures, where the thinned region is aligned to the edge of a gate or contact in a device. This type of self-alignment allows the device to be contacted in a thick, small band gap region while creating a thin, large band gap channel via the cyclical thinning process. This type of patterning scalability is essential for fabricating high performance devices including scaled heterostructure MOSFETs or heterostructure TFETs and could also be interesting for exploring optical applications such as BP quantum well heterostructures and superlattices.

2.2 Optical Characterization of Thinned Black Phosphorus

The slow, cyclical nature of this thinning process also makes it an attractive method to consistently produce ultra-thin BP films. However, comprehensive optical characterization including a photoluminescence study revealing the optical band gaps of thinned BP flakes as well as the peak sharpness indicating the thickness uniformity and Raman characterization which confirms crystallinity is important for verifying the quality of thinned BP films as well as the increase in band gap of the thinned BP flakes. It is especially important to verify the quality of ultra-thin BP films after the thinning process because their characteristics are expected to be more sensitive to degradation. In addition to this, if one wants to optimize devices for NIR and visible applications, ultrathin flakes are required. For example, a 4-nm flake is predicted to have a band gap of ~0.8 eV which corresponds to an optical wavelength of about 1500 nm [94]. The presented cyclical annealing thinning process shows promise in being able to achieve these flake thicknesses, as well as provide the ability to pattern large flakes and make novel heterostructures.

2.2.1 Raman Characterization of Thinned Black Phosphorus

First, I will show an example of Raman characterization of ultra-thin BP produced by the layer-by-layer thinning process. Figure 2.7 shows the method by which ultra-thin BP flakes were fabricated and characterized. For these samples, a BP flake with some degree of thickness variation was exfoliated and transferred to a SiO_2 substrate (Figure 2.7(a)). 5 thinning cycles were used to thin the flake and then the BP was passivated by exfoliating and aligning a 17-nm-thick sheet of hexagonal boron nitride (h-BN) as shown in Figure 2.7(c). h-BN is an effective passivation layer for BP and produces a high-quality

interface with BP, enabling Raman and PL spectra and AFM measurements to be obtained on ultrathin flakes.

After passivation, the ultrathin BP flake was examined by AFM and Raman spectroscopy. Figure 2.7(d) shows the AFM topographic map of the h-BN passivated BP flake, indicating two lines in which the step heights were extracted. Figure 2.7(e) shows the thicknesses in these regions to be 1.6 nm and 7.3 nm in regions 1 and 2, respectively. To confirm that the thinned region contained crystalline BP (rather than an oxidized or amorphous layer), Raman spectra were collected from the two regions where the thicknesses of the BP were extracted. These results are plotted in Figure 2.7(f), where in

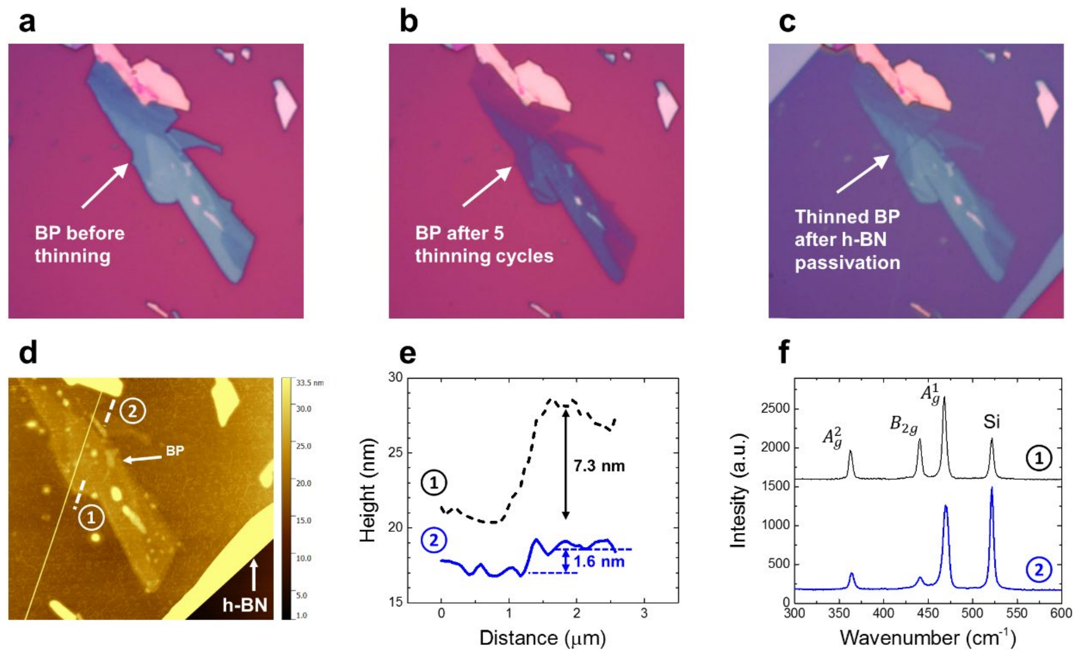


Figure 2.7 (a, b) Optical images of exfoliated BP, (a) before and (b) after five thinning cycles. (c) Thinned flake after passivation with 17-nm-thick exfoliated h-BN flake. (d) AFM topographical image of h-BN passivated BP flake. Dotted lines labeled ① and ② correspond to the two slices used to extract the height and collect Raman spectra. (e) Step heights of the two regions marked in panel d. (f) Raman spectra collected from BP regions corresponding to the thickness extracted in ① and ②. Three BP characteristic Raman peaks are observed in the 1.6 and 7.3 nm flake regions, proving that both regions contain crystalline BP.

both the 7.3 nm-thick and 1.6 nm-thick regions, the in-plane A^2_g and B_{2g} modes and out of plane A^1_g mode are clearly visible, along with the Si substrate peak. A decrease in the A^1_g to Si peak ratio peaks was observed for the thinner flake, as expected due to a decrease in optical absorption as the BP gets thinner. Results similar to theses have been reported by Favron et al. [44] The ratio of the A^2_g to the A^1_g peak was also used by Favron et al. as a measure of the BP oxidation; they indicated that A^2_g/A^1_g ratios > 0.2 are characteristic of low oxidation levels. Spectra from regions 1 and 2 show A^2_g/A^1_g ratios of 0.31 and 0.74 respectively indicating low oxidation levels. The observation of the characteristic BP Raman peaks and $A^2_g/A^1_g > 0.2$ in the thinned BP sample provide good evidence that the cyclical oxidation and annealing thinning process produces high purity BP layered crystals.

2.2.2 Photoluminescence of Thinned Black Phosphorus

Another indicator of high purity BP is the presence of photoluminescence peaks. In order to obtain PL in the near-IR or visible regime BP flakes must be thinned to ~3 layers or lower where the band gap is higher than ~1 eV. A similar method to the Raman characterization of ultra-thin BP films was employed where a thinned BP flake with various thicknesses was passivated with exfoliated h-BN in order to protect BP from oxidation and

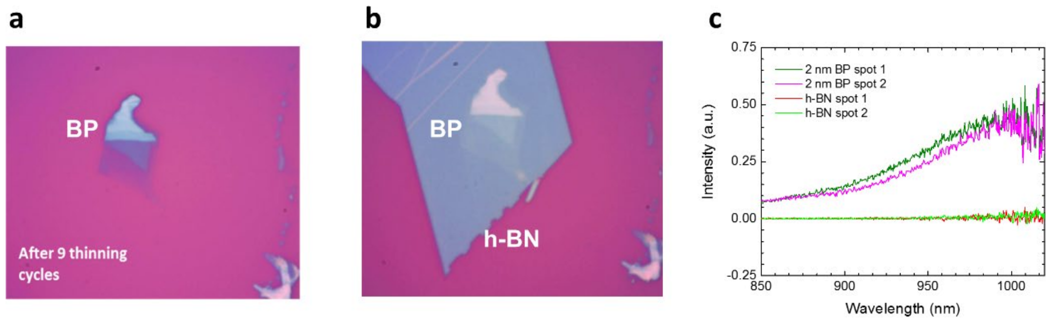


Figure 2.8 (a)-(b) Optical images of a BP sample before and after 10 thinning cycles followed by passivation with h-BN.(c) Photoluminescence (PL) spectra for 4 different regions after subtraction of the background h-BN/SiO2/Si signal.

form a clean interface for optical characterization. In collaboration with a colleague, Dr. Seon Namgung PL measurements were performed using a 532 nm laser with a ~ 2 μm focused spot size as an excitation source. PL spectra were collected from the thinned BP flake in the region which was measured by AFM to be 2 nm (initial thickness can be inferred to be between 7 and 8 nm by assuming a layer-by-layer rate) as well as a region with only the h-BN/SiO_2/Si stack. Two spectra taken from the 2 nm BP regions show a peak at ~ 990 nm, or 1.25 eV, while the spectra collected from the h-BN/SiO_2/Si region show no signal, confirming the signal only comes from the thin BP region. Previously reported experimental results show emission peaks for monolayer, bilayer, and trilayer BP at 1.65 eV, 1.28 eV, and 0.96 eV respectively [15]. This indicates that the peak at 1.25 eV is likely coming from bilayer BP. The emission peak is broader than what might be expected for bilayer BP so it is possible that there is some non-uniformity in the thinned sample or some trap states present. In addition, the 2-nm-thick BP region is thicker than expected from bilayer BP based on an interlayer spacing of 0.55 nm. We believe the likely source of this discrepancy is the thickness of the oxide layer on the surface of the bilayer-BP from prolonged exposure to atmosphere throughout the process. Despite this discrepancy, the Raman spectra and PL spectra of ultra-thin BP produced by the layer-by-layer thinning process show that it is possible to thin BP down to < 2 nm and maintain highly crystallinity.

2.3 Black Phosphorus Heterostructure MOSFETs

Next, it is shown how the thinning process was used to create lateral heterostructures in BP in order to observe the effects of the cyclic annealing thinning process on electrical

performance as well as demonstrate a novel heterostructure MOSFET which is used to improve the OFF-state performance in a BP MOSFET.

2.3.1 Black Phosphorus Heterostructure MOSFET Fabrication Process

The process flow for the heterostruture BP MOSFET is shown in Figure 2.9. First, BP was exfoliated and transferred onto a 290 nm SiO_2/Si using the same transfer methods described in the previous section. Once a suitable thick flake was identified via optical microscopy, PMMA was spin-coated and E-beam lithography was used to open patterns for two contacts. Ti/Au contacts (10 nm /45 nm) were then deposited using an electron-beam evaporation and liftoff process. Next, as shown in Figures 2.10(a) and 2.10(b), the patternable cyclic oxidation/annealing procedure described previously was used to passivate the contacted regions of the flake and then thin the exposed region down. After the region was thinned, the same E-beam lithography/evaporation process was used to

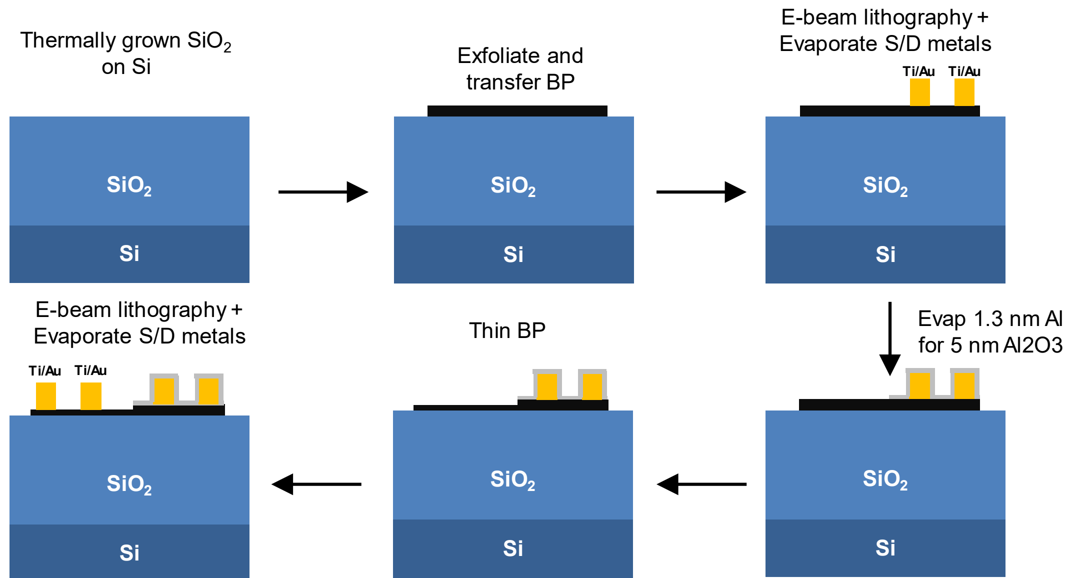


Figure 2.9 Diagram of the heterostructure BP MOSFET process flow.

deposit two new contacts on the thin region. The two pairs of contacts were designed and positioned so that, not only could transport across the heterojunction be measured, but transport in thick and thin regions could also be measured independently. Following deposition of the contacts onto the thin region the device was passivated with 20 nm of Al_2O_3 using ALD. Figure 2.10(c) shows an optical micrograph of one of the completed devices.

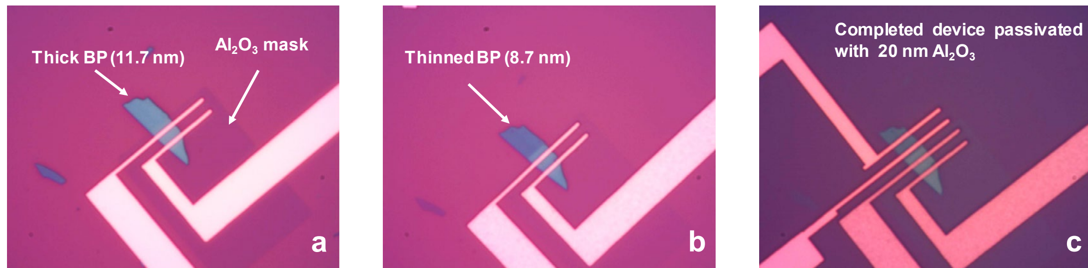


Figure 2.10 Optical micrographs of BP p-MOSFET, (a) after Al2O3 mask was deposited but before oxidation/annealing process and (b) after full thinning process was performed. (c) Optical micrograph of completed BP heterostructure p-MOSFET.

2.3.2 Black Phosphorus Heterostructure MOSFET Electrical Characterization

All device measurements were performed using an Agilent B1500A semiconductor parameter analyzer at vacuum levels less than 10^{-5} Torr. First, in order to examine the effect of thinning on homojunction BP MOSFETs, the transfer characteristics in the thick and thin BP regions were measured. It is important to note that since 290 nm of SiO_2 was used as the gate dielectric, the gate capacitance is very low in comparison with other high performance BP MOSFETs fabricated using thinner SiO_2 gate dielectrics or high-k gate dielectrics such as HfO_2. This low capacitance results in high turn-on voltages, high subthreshold slopes, and low g_m but still allows for analysis of the thick and thin BP channels through observing I_{ON} and I_{ON}/I_{OFF} in the transistors.

Figure 2.11(a) shows the drain current, I_D, vs. gate-to-source voltage, V_{GS}, for the device in Figure 2.10 (device #1) at a drain-to-source voltage, V_{DS}, of −0.1 V. A decrease in the OFF current and an increase in I_{ON}/I_{OFF} is observed after thinning. To calculate I_{ON}/I_{OFF}, the OFF current was taken as the minimum current value, within the range of V_{GS} values measured, while the ON current was taken as the I_D value at a value of V_{GS} that is 50 V more negative its value at the minimum current. After thinning, I_{ON}/I_{OFF} of device #1 increased from ~ 3.2 in the thick (11.7 nm) region to 2.8×10^3 in the thin (8.7 nm) region. The I_D vs. V_{GS} curves for the same device at V_{DS} = −2.0 V are shown in Figure 2.11(b) and

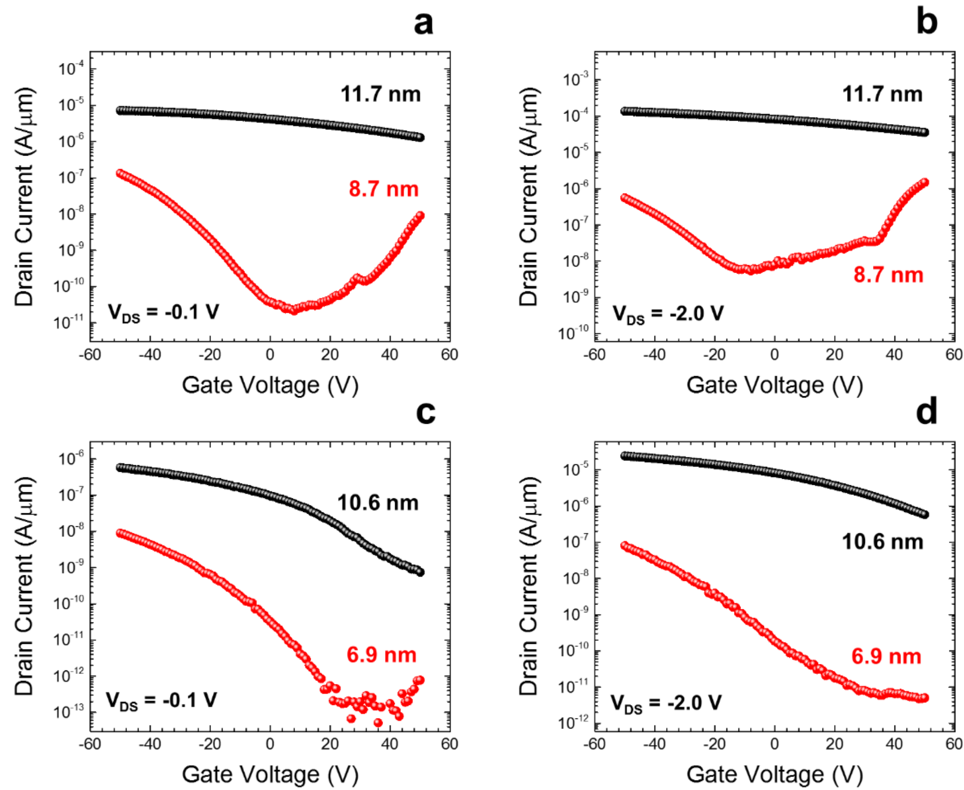


Figure 2.11 (a, b) Transfer curves for thick and thinned regions of BP p-MOSFET (device 1) with the indicated thicknesses, at V_{DS} = −0.1 and −2.0 V, respectively. (c, d) Transfer curves for thick and thinned regions of BP p-MOSFET (device 2) with the indicated thicknesses, at V_{DS} = −0.1 and −2.0 V, respectively.

the results show that I_{ON}/I_{OFF} is generally maintained, though the ambipolar behavior in the 2.11(d). For both device #1 and #2, incomplete turn-off was observed in the thick regions, which could be due to incomplete channel pinch off resulting from the thicker body and narrower band gap which prevents the channel from being fully depleted. It could also be due to some hole doping resulting from the Al_2O_3 mask. After thinning, I_{ON}/I_{OFF} improvement can be attributed to both the thinner BP, which ensures that the channel is fully depleted enabling complete channel pinch-off, as well as the wide band gap in the thinned regions. For example, A. Penumatcha et al. extracted the BP band gaps from a Schottky barrier MOSFET model and found a band gap of ~0.5 eV for a 9-nm BP device and a band gap of ~0.6 eV for a 7-nm BP device. The thinned devices also show an improved subthreshold slope, which has also been shown to be associated with an increasing band gap in BP as thickness is decreased. Unfortunately, while I_{ON}/I_{OFF} improves, the overall ON current decreases after thinning due in part to the increased Schottky barrier height between the Ti source contact and the valence band of the BP, which results in a more resistive path for carriers to be injected.

An energy band diagram depicting the metal-semiconductor interface at the source is shown in Figure 2.12 and displays this idea clearly. Higher work function metals could be used to improve this trade-off in p-MOSFETs, however, lack of band-edge metals for

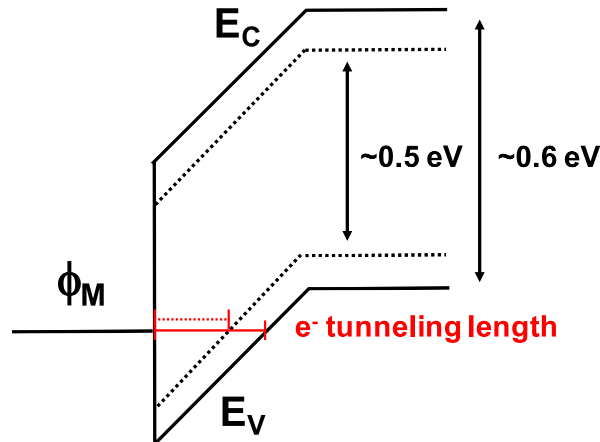


Figure 2.12 Band diagram of metal−semiconductor interface for BP channels with ~0.6 eV band gap (solid lines) and ~0.5 eV band gap (dotted lines). It is evident from the diagram that as the band gap increases, the Schottky barrier increases, decreasing the current from thermionic emission over the barrier. It is also clear that as the band gap increases, tunneling current through the Schottky barrier will decrease due to the larger electron tunneling length. These factors combine to give lower overall ON current in thinner BP MOSFETs, which have larger band gaps.

contacting BP puts limitations on this method. In addition to an increased Schottky barrier height, the ON-current also may decrease because of a lower BP channel mobility. The mobility of BP can decrease with a decrease in flake thickness, but a decrease in mobility could also be attributed to BP degradation during the thinning process. The field-effect-

Device	Thick Region Mobility (cm^2/V·s)	Thinned Region Mobility (cm^2/V·s)
#1 Thick 11.7 nm/Thinned 8.7 nm	91	16
#2 Thick 10.9 nm/Thinned 6.7 nm	14	0.6
#3 Thick 12 nm/Thinned 7.8 nm	99	3.8

Table 2.1 Field-effect mobilities for thick and thinned BP regions of three different BP MOSFETs are displayed.

mobility, (μ_{FE}) for the BP MOSFETs shown in Table 2.1 are in general agreement with that trend. The mobility was extracted from the g_m of the BP MOSFETs in the linear regime (V_{DS} = –0.1 V). The mobility is observed to drop after thinning, however additional studies would be needed to determine to what extent the mobility degradation is due to the thinning process vs. simply the changes in band structure and scattering due to the absolute thickness of the sample itself. From these results it is seen that thinning the entire BP region is not an adequate way of achieving increased I_{ON}/I_{OFF} without sacrificing ON current, however measuring the device in the heterostructure configuration enables this desireable result.

To investigate this possibility, a heterostructure device was fabricated (device #3) with a 12nm-thick BP region and a thinned BP region that was 7.8 nm thick and measured the I_D vs. V_{DS} device characteristics and the I_D vs. V_{GS} device characteristics. It should be noted that the sample was not passivated with a final ALD Al_2O_3 layer for these measurements in order to prevent any n-type doping in the thin channel from the ALD deposition process. Initially, the I_D vs. V_{DS} characteristics of the heterostructure device were measured, where the drain contact was the 12-nm-thick BP region and the source contact was the 7.8 nm-thick BP region and the V_{DS} is swept from –1 V to +1 V. The characteristics are shown for V_{GS} = –80 V and V_{GS} = 0. Figures 2.13(a) and 2.13(b) show that the I_D vs. V_{DS} curve exhibits strong asymmetry with rectification on the order of 10^2 at V_{GS} = –80 V and 10^3 at V_{GS} = 0. This rectification can likely be explained by band gap asymmetry in the thick and thin BP regions, although it is also possible that there is some doping asymmetry between the thick and thinned regions. The band diagrams in Figure 2.13(c) show the anticipated band diagrams and a potential origin of the asymmetry. For the forward bias condition, the current initially increases exponentially, which can be attributed to an increase in

thermionic emission of holes over the heterojunction barrier as the bias is increased. At higher values of V_{DS}, the bias is high enough that the holes are largely unaffected by the energy barrier in the middle of the channel, and so the current is limited only by the small Schottky barrier to the narrow-gap BP at the drain. At sufficiently high bias, the current increase becomes more linear with V_{DS} as the drain injection barrier becomes more transparent. In the reverse bias condition, it is suspected that the hole current injection from the source is suppressed due to the fact that the Schottky barrier for holes is now higher due to the presence of a larger band gap. Overall, these characteristics provide further confirmation of the enlargement of the BP band gap with thinning and shows how carrier transport is affected by the heterostructure.

Next, in order to see the improved subthreshold performance in the heterostructure BP MOSFET, I_D vs. V_{GS} characteristics of the device were measured using four different contact combinations: two homojunction configurations where the source and drain

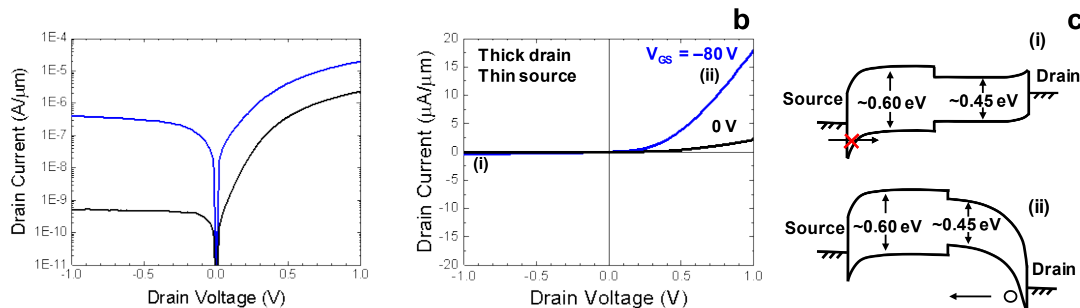
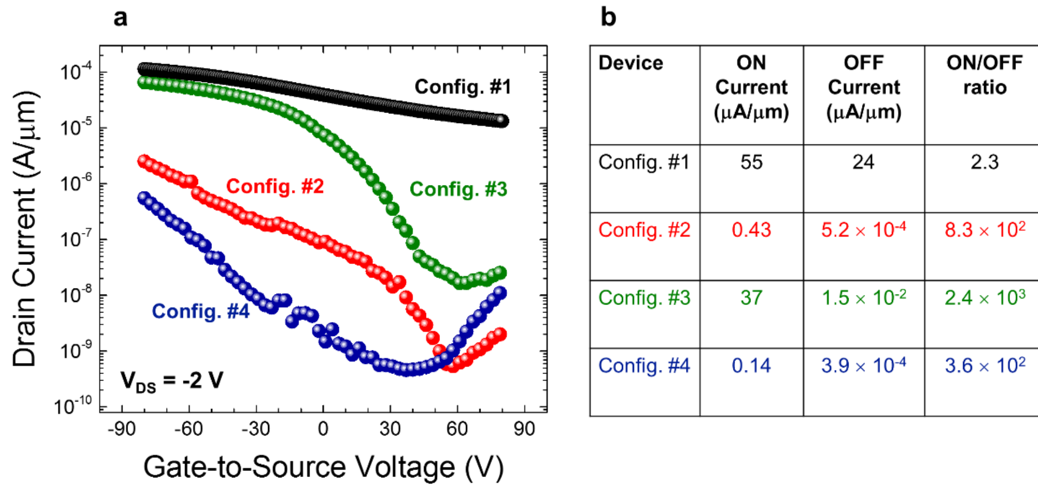


Figure 2.13 (a) I_D vs V_{DS} characteristics measured across the heterostructure interface in device 3 at $V_{GS} = -80$ V (blue) and $V_{GS} = 0$ V (black), plotted on a logarithmic scale, showing asymmetric current characteristics. Thick drain indicates the measurement setup in which the drain contact is made on the 12 nm BP region, whereas thin source indicates the source contact made on the 7.8 nm BP region. (b) I_D vs V_{DS} characteristics shown in panel a plotted on a linear scale, showing an exponential increase in I_D at small positive values of V_{DS} becoming linear as V_{DS} increases. (c) Energy band diagrams representing two points on the I_D vs V_{DS} plot: (i) band condition when $V_{GS} = -80$ V and $V_{DS} = -1$ V and (ii) band condition when $V_{GS} = -80$ V and $V_{DS} = +1$ V. Band gaps are estimated from the model by Penumatcha et al. [94].

contacts are both made to the (1) thick and (2) thin BP regions and two heterojunction configurations with (3) thin BP source / thick BP drain and (4) thick BP source / thin BP drain. Figure 2.14(a) shows the p-MOSFET I_D vs. V_{GS} characteristics at $V_{DS} = -2$ V for configurations (1)-(4). Here, V_{GS} was swept from −80 V to +80 V, while V_{DS} was kept at a constant −2V. For the thick homojunction device (config. #1), high drive current is obtained, but the gate is unable to completely turn off the channel. In contrast, the thin homojunction device (config. #2) shows good turn-off behavior, but I_{ON} is roughly two orders of magnitude lower than the thick BP device. However, the heterojunction device with thick BP source and thin BP drain (config. #3) demonstrates the benefit of the heterostructure BP MOSFET. In this device, I_{ON} is close to that of config. #1 is achieved, while excellent I_{ON}/I_{OFF} is obtained. Finally, config. #4 displays both low current drive and increased ambipolar current, as expected from a device with wide band gap source and narrow gap drain. The chart in Figure 2.14(b) shows a quantitative comparison of the device performance in the different contact configurations. Most importantly, the chart shows that the heterojunction configuration (config. #3) increases I_{ON}/I_{OFF} by over 10^3 in



Device	ON Current (µA/µm)	OFF Current (µA/µm)	ON/OFF ratio
Config. #1	55	24	2.3
Config. #2	0.43	5.2×10^{-4}	8.3×10^{2}
Config. #3	37	1.5×10^{-2}	2.4×10^{3}
Config. #4	0.14	3.9×10^{-4}	3.6×10^{2}

Figure 2.14 (a) I_D vs V_{GS} measurements of device 3 for all four device contact configurations: (1) thick BP homojunction, (2) thin BP homojunction, (3) heterojunction with thick BP source and thin BP drain, and (4) heterojunction with thin BP source and thick BP drain. (b) Table summarizing the key MOSFET characteristics in panel a. OFF current is taken as the minimum drain current value for each contact configuration. ON current is taken as the drain current value at $V_{GS} = V_{GS}$ (min drain current) − 100 V. The ON/OFF ratio (I_{ON}/I_{OFF}) is ON current divided by OFF current. Configuration 3 provides the best performance when both ON current and ON/OFF ratio are taken into consideration. Thick and thin regions are 12.0 and 7.8 nm, respectively.

comparison to config. #1, while only slightly reducing the on current from 55 µA/µm to 37 µA/µm. Overall, these improvements in I_{ON}/I_{OFF} and I_{ON} are consistent with expectations based upon the change in band gap and Schottky barrier heights with BP thickness.

The BP heterostructure device concept shown in this work exemplifies the usefulness of the cyclical thinning method in that precise control of the BP thickness at the drain of a MOSFET can be used to improve the subthreshold device performance. This scheme could be used to optimize conventional BP MOSFETs, and improve performance in other as novel electronic devices such as TFETs. For conventional MOSFETs, the heterostructure

can be used to suppress leakage from previously mentioned gate-induced-drain-leakage (GIDL) by increasing the semiconductor band gap in the drain contact region. Not only can this improve I_{ON}/I_{OFF} as we have demonstrated here, but suppression of GIDL could help ensure that the devices can achieve ideal subthreshold slope. Related work by our group has shown that excess GIDL current that occurs before turn-off of the source injection can actually lead to subthreshold slope > 60 mV/decade, particularly at high drain bias [63]. In BP, the absence of band-edge contact metals and a narrow band gap make GIDL current and its effects particularly problematic. It should be noted that thinning can also result in a decrease in mobility in the thinned regions, however, devices could be designed such that only the region directly under the drain is thinned, thereby minimizing any potential impact to the ON-state current of the device. This same heterostructure principle has been used to enable TFETs in other materials systems with sub-60-mV/decade subthreshold slope [95], [96]. In addition to this, TFETs with heterostructure BP channels [72] were introduced in chapter 1 and show potential for achieving high performance.

BP heterostructures similar to the one shown in this work could also have a broad range of applications for optoelectronic devices. Heterostructure BP photodetectors with wide-gap contacts could be used to suppress dark current while utilizing the direct band gap of BP to efficiently absorb light. Perhaps the most exciting possibility in optoelectronics is the potential to realize a double-heterostructure suitable for use in light emitting diodes and lasers. Since it is expected that the band gap increases in an approximately symmetric fashion between conduction and valence bands, this indicates that thin/thick BP heterostructures create type-I heterostructures which are necessary for spatial confinement

of electrons and holes. Efficient BP light emitters could create a whole new platform for 2D photonic circuits and their integration with existing CMOS technology.

2.4 Summary

In this section, BP's inherent reactivity with ambient atmosphere has been utilized to create a cyclical, patternable thinning process. I have shown high resolution (sub-150 nm) patterns which could be scaled further by optimization of the EBL process. The thinning process has produced flakes as thin as 1.6 nm and shows promise for use in visible and near-IR tunable optical devices. The cyclical thinning process was also used to create the first ever heterostructure MOSFET which shows improved I_{ON}/I_{OFF} while maintaining a high ON-current in comparison with homojunction BP MOSFETs.

CHAPTER 3 ELECTROSTATICALLY DOPED BP MOSFETS

In chapter 2, the tunable band gap of BP was used to improve OFF-state performance in BP MOSFETs. In this chapter, electrostatic doping will be explored as a method for improving I_{OFF} in BP MOSFETs while maintaining good I_{ON}. Before the work reported here, most BP MOSFETs reported in the literature utilized Schottky contacts as a consequence of Fermi level pinning. However, as discussed briefly in the introduction, Schottky contacts have been shown to lead to high contact resistance and poor *SS* at high values of drain-to-source voltage (V_{DS}), due to ambipolar carrier injection from the drain electrode [58], [63], [94], [97]. The injection from the drain is enhanced by the small (0.3 eV) direct band gap and light effective mass in the AC crystal direction which both lead to efficient tunneling of carriers from the drain contact back into the BP channel as the device enters the subthreshold regime. Utilizing heavily doped contacts represents a method by which the ambipolar carrier injection from the drain can be reduced, by increasing the tunneling distance of the carriers and by utilizing "band-gap filtering" to cut off the energy states that would be occupied by the high energy "tail" of the Fermi-Dirac carrier distribution. In the literature, surface charge transfer doping [98], [99], bulk doping [100], [101], and electrostatic doping techniques [102] have been utilized in BP devices, showing the ability to enhance hole or electron conduction. In this chapter, local electrostatic doping was used because it allows for gate-tunable hole and/or electron doping concentrations which make a good platform for studying the effects of different electrostatic schemes on device performance. This was done by fabricating a triple-gated device structure which includes separate independent back gates to create electrostatically doped (ES-doped)

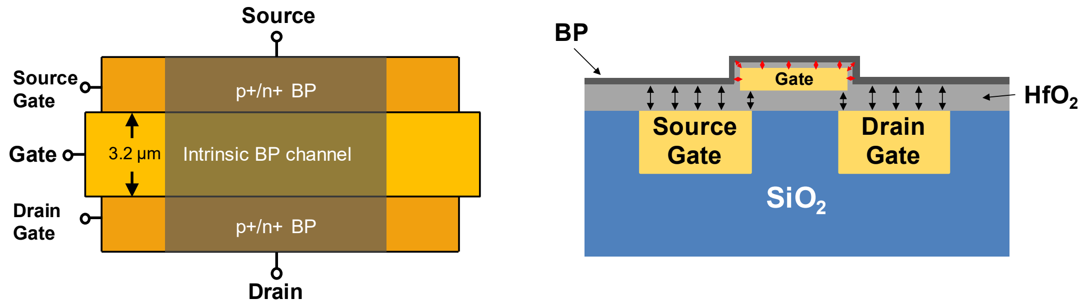


Figure 3.1 Diagram on the left shows a top-view schematic of the triple-gated device structure. On the right, the triple-gated structure is shown with arrows representing electric field lines. These lines demonstrate how the upper gate shields the BP from the fields from the lower gates (black).

source (S) and drain (D) regions and a gate region that is shielded from the S and D-gate fields as in Figure 3.1. This device structure, enabled the demonstration of BP p-MOSFETs and n-MOSFETs with greatly improved SS and I_{ON}/I_{OFF} at high V_{DS} compared to Schottky-contacted BP MOSFETs. Most of the results in this chapter are published in references [103] and [104].

3.1 Fabrication of Triple-Gated FET Structure

In order to create a device that gives independent control of the BP source, drain, and channel doping regions, a device structure was designed and fabricated utilizing 3 independent local back gates. The process flow for the triple gated BP FET is shown in Figure 3.2. E-beam lithography was used for all of the patterning steps and all metal was deposited using electron-beam evaporation followed by lift-off. The process started by patterning quasi-planarized source-gate and drain-gate electrodes consisting of Ti/Pd. ALD was then used to deposit 40-nm of HfO_2. Next, the channel gate electrode was patterned such that it overlaps and shields the source-gate and drain-gates so as to create perfectly adjacent gate interfaces. ALD was again used to deposit the 7-nm of HfO_2 which acted as

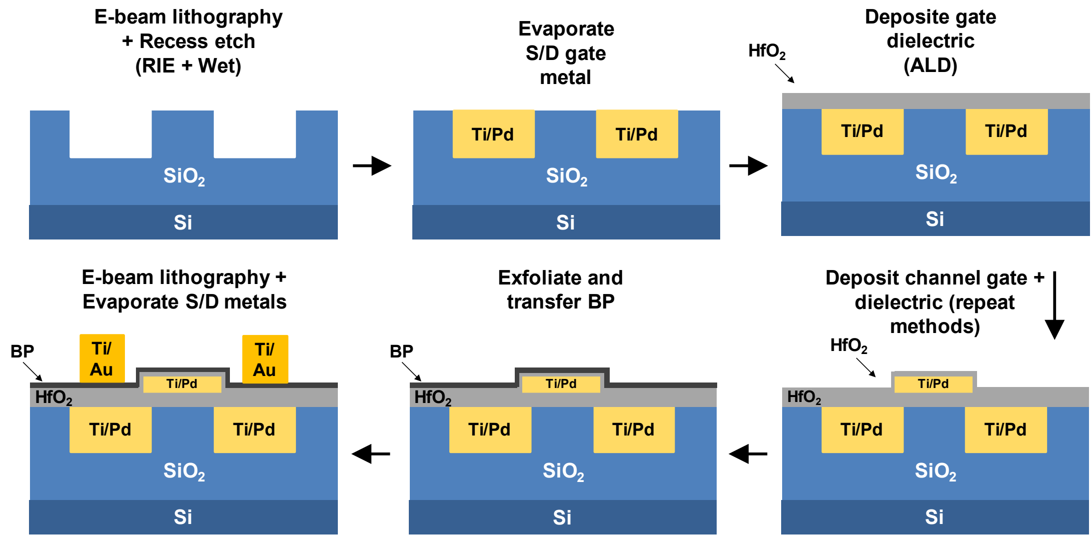


Figure 3.2 Process flow for ES-doped BP MOSFETs using the triple-gated device structure.

the gate oxide. The deposited HfO_2 film gives an EOT of 1.6 nm for the gate oxide. Few-layer BP was exfoliated, then aligned and transferred to the gates using a PDMS stamping method. To minimize the BP degradation, PMMA was immediately spin-coated, acting as a temporary passivation layer and a resist for the following patterning step. Next, Ti/Au contacts were made to the BP and finally a passivation layer of 100 nm of Al_2O_3 was deposited by ALD. An optical micrograph and cross-sectional diagram of a completed device are shown in Figure 3.3. Two devices with BP thicknesses of 5.7 nm and 12.8 nm were fabricated, and AFM was used to extract the BP thickness.

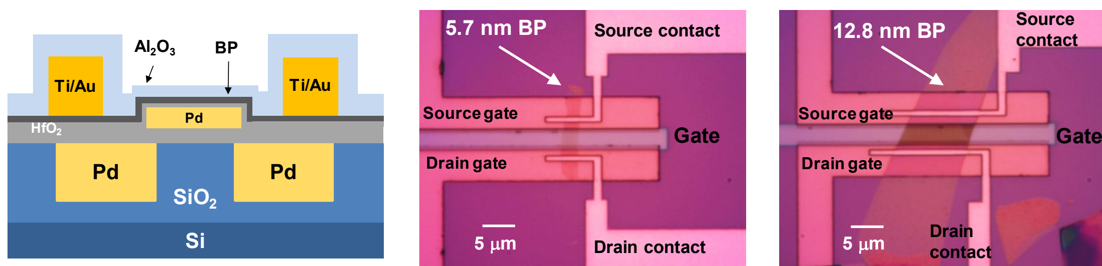


Figure 3.3 Left shows a cartoon cross-sectional view of the completed ES-doped BP MOSFET, The two figures on the right represent optical micrographs of two fabricated ES-doped BP MOSFETs with different BP thicknesses.

3.2 Characterization of ES-doped BP MOSFET

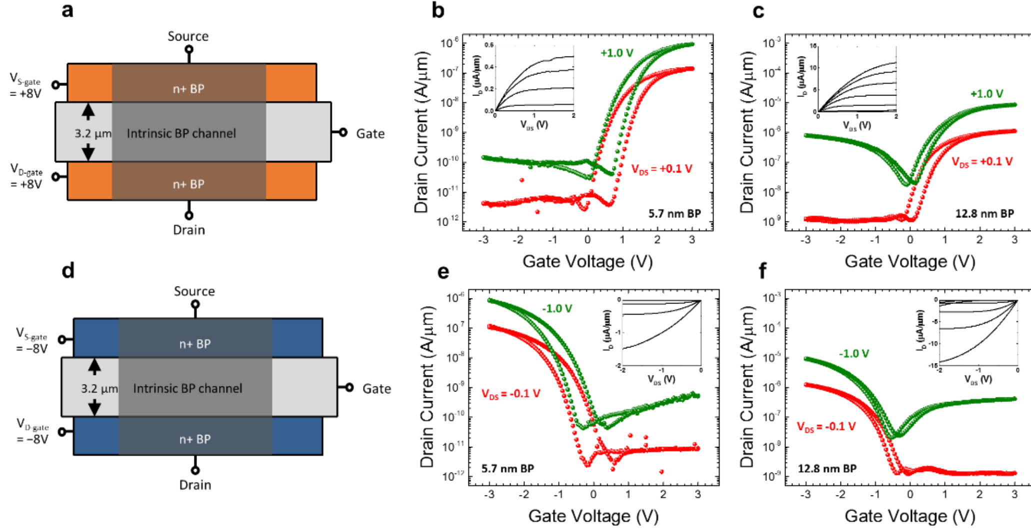


Figure 3.4 Electrostatically doped BP p-MOSFET and n-MOSFET device schematics (a, d) and transfer curves with channel thicknesses of 5.7 nm (b, e) and 12.8 nm (c, f). For p-MOSFETs, V_{SG} and V_{DG} were fixed at –8.0 V and for n-MOSFETs, V_{SG} and V_{DG} were fixed at +8.0 V. The inset plots show the output characteristics for each corresponding device configuration with V_{GS} swept from –3.0 V to 0 at $\Delta V_{GS} = 0.5$ V for the p-MOSFETs and +3.0 V to 0 at $\Delta V_{GS} = 0.5$ V for the n-MOSFETs.

The devices were measured at room temperature using an Agilent B1500A parameter analyzer along with a Keithley 2450 unit as a constant voltage source for the source gate. During test, constant voltages (V_{SG} and V_{DG}) are applied to the "Source Gate" and "Drain Gate" terminals, respectively, to control the BP doping in the source and drain regions. The voltages for conversion between n-type and p-type doping occurred around V_{SG}, $V_{DG} = 0$, so that when V_{SG}, $V_{DG} > 0$, (V_{SG}, $V_{DG} < 0$), the device operated as an n-MOSFET (p-MOSFET). Figure. 3.4 shows the p-MOSFET and n-MOSFET characteristics for ES-doped BP MOSFETs with 5.7 nm and 12.8 nm BP channels. The transfer characteristics show the re-configurability device and strong symmetry between the p-MOSFET and n-MOSFET configurations. It is significant that no ambipolar turn-on is observed at low $|V_{DS}|$ indicating suppressed drain side carrier injection resulting in improved subthreshold

performance. The I_D vs. V_{DS} curves in the insets show good saturation behavior and symmetric p- and n-MOSFETs characteristics, although n-MOSFETs show slightly lower I_{ON}.

The key result from these devices is the improved I_{ON}/I_{OFF} at high V_{DS} values compared with Schottky contacted BP MOSFETs. In the ES-doped BP MOSFETs I_{ON}/I_{OFF} ratios greater than 10^4 for the 5.7 nm BP channel and almost 10^3 for the 12.8 nm BP channel are observed. These I_{ON}/I_{OFF} results are comparable to those of Ti Schottky contacted BP MOSFETs of similar thicknesses in the literature [10]. However, as $|V_{DS}|$ is increased, the Schottky contacted BP MOSFETs show up to two orders of magnitude decrease in I_{ON}/I_{OFF} after $|V_{DS}|$ is increased to 1.5 V[63]. As discussed previously, this degradation of I_{ON}/I_{OFF} is caused primarily by ambipolar current injected back into the channel from the drain as the device is being turned off. In contrast, the BP MOSFETs with ES-doped contacts show considerable improvement, as I_{ON}/I_{OFF} decreases by less than a factor of two when $|V_{DS}|$ is

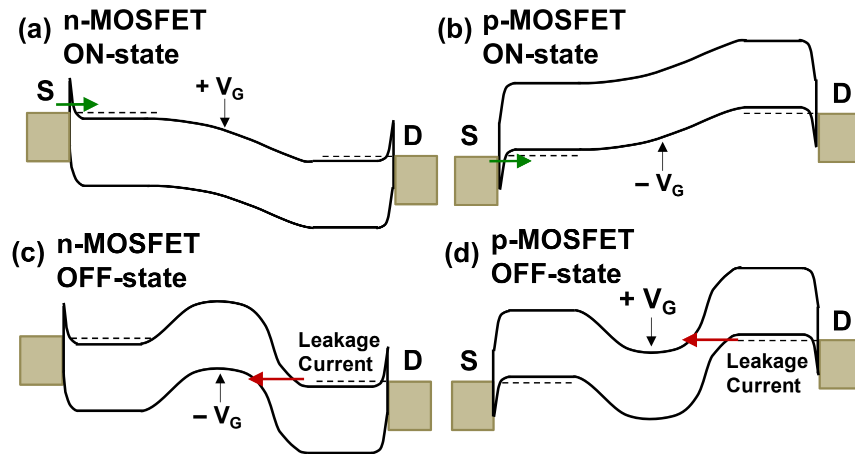


Figure 3.5 (a)-(b) Band diagrams of the ES-doped BP n-MOSFET in the (a) ON and (b) OFF states. (c)-(d) Band diagrams for ES-doped BP p-MOSFET in the (c) ON and (d) OFF states. $|V_{DS}|$ = 0.1 V.

increased from 0.1 to 1.0 V. As shown by the band diagrams in Fig. 3.5, this improvement is due to the fact that, in the ES-doped MOSFET, I_{OFF} is limited for the most part by band-to-band tunneling at high $|V_{DS}|$, creating a longer distance for tunnel current injection from the drain to the channel compared to a Schottky-contacted MOSFET as well as creating the aforementioned filtering effect. In addition to causing an improved I_{ON}/I_{OFF} at high V_{DS}, this suppression of ambipolar current also leads to an improved *SS* at high V_{DS} over Schottky contacted BP MOSFETs. Figure 3.6 shows *SS* plotted vs. I_D for the ES-doped BP MOSFETs showing only minor degradation with increasing V_{DS}. This minor degradation is compared with the larger *SS* degradation with increasing V_{DS} for Ti Schottky contacted BP MOSFETs in Table 3.1 which compares the *SS* characteristics at low and high V_{DS} for the ES-doped and Ti Schottky contacted BP MOSFETs. The Ti Schottky contacts utilize a single local back gate and HfO_2 as the gate oxide. It is important to note that the *SS* values at low V_{DS} for both the ES-doped BP MOSFETs and Schottky contacted BP MOSFETs are far from ideal. It is suspected that this results from a high density of interface trapys (D_{it}) due to the ambient degradation of the bottom BP surface during the transfer process and expect that by performing this step in an inert environment, the D_{it} would be greatly reduced and closer to ideal *SS* could be achieved.

However, the function of the ES-doped contacts in improving the *SS* values at high V_{DS} are still clearly seen when examining the table in Table 3.1. The ES-doped MOSFETs show a 14% and 22% increase in *SS* for the 5.7 nm BP device and 12.8 nm BP device respectively. Schottky contacted devices with similar BP thicknesses from [63] show *SS* increases of 69% and 550% for a 4.5 nm BP device and a 13.8 nm BP device respectively. This marks a substantial improvement and may prove important as future BP MOSFETs

used in practical applications will require high performance at higher V_{DS} values. In future work, it will be important to increase I_{ON} and reduce the hysteresis in the devices. The relatively low I_{ON} is in large part due to the long gate length of 3.3 μm and at shorter gate lengths, Schottky-contacted BP MOSFETs have achieved I_{ON} values over 500

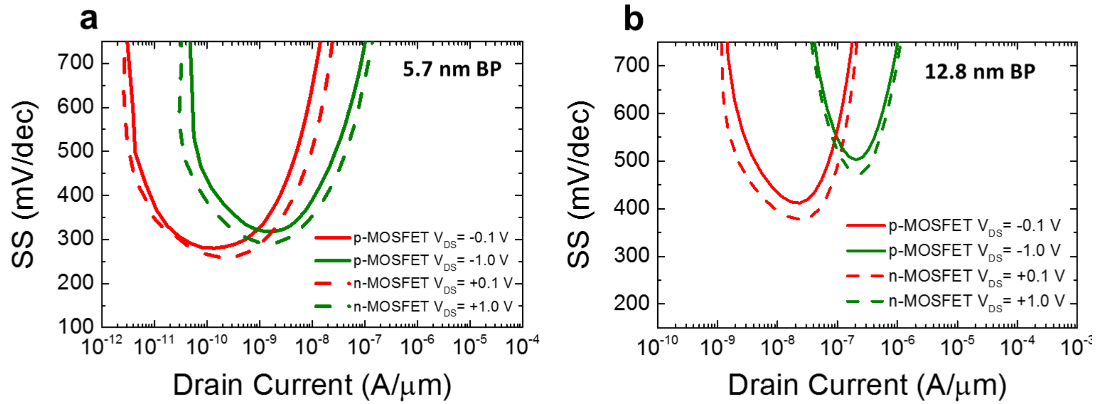


Figure 3.6 Subthreshold slope (SS) plotted versus drain current for ES-doped BP p-MOSFET and n-MOSFETs for channel thicknesses of (a) 5.7 nm and (b) 12.8 nm.

μA/μm [58]. Similar values should be achievable with the ES-doped BP MOSFETs provided the source and drain regions can be doped heavily enough in order to minimize series resistance. Increasing the mobility of the BP channel by minimizing BP oxidation and improving the BP/dielectric interface would also increase I_{ON}. The electron and hole field effect mobilities in this ES-doped BP MOSFET were extracted at $|V_{DS}|$ = 0.1 V from

BP Thickness (nm)	Contact	t_{ox}(nm)	SS_{min}(mV/dec) @ $\|V_{DS}\|$ = 0.1 V	SS_{min}(mV/dec) @ $\|V_{DS}\|$ = 1.0 V	SS(1.0V) / SS(0.1V)
5.7	ES-doped	7	279	317	**1.14**
12.8	ES-doped	7	411	503	**1.22**
4.5	Schottky	15	180	305	**1.69**
13.8	Schottky	10	247	1359	**5.50**

Table 3.1 SS characteristics for ES-doped BP p-MOSFETs compared to Schottky-contacted BP p-MOSFETs from [63].

the transfer characteristics using the peak g_m giving values of 29 $cm^2/V{\cdot}s$ (12.8 nm BP) and 11 $cm^2/V{\cdot}s$ (5.7 nm BP) for electrons and 28 $cm^2/V{\cdot}s$ (12.8 nm BP) and 3.3 $cm^2/V{\cdot}s$ (5.7 nm BP) for holes. These mobility values are relatively low and could be explained by non-idealities at the BP/HfO_2 interface. The observed hysteresis is likely caused by traps in the HfO_2 being charged and discharged as V_{GS} is swept, and has been observed in other reports on 2D-material MOSFETs [58]. This effect is enhanced due to the relatively large voltages (± 3 V) being applied across the 7 nm HfO_2 layer. An interfacial P_xO_y layer is also expected due to surface oxidation during BP transfer which may also contribute to the relatively low mobility and to the gate sweep hysteresis. It is also important to note that these characteristics are not a fundamental problem for this type of device structure and it would be expected that higher quality materials and interfaces would result in higher carrier mobility and lower hysteresis.

While these improvements are compatible with the ES-doping platform, it is important note that high-speed performance could be limited by the parasitic capacitance between the source/drain gates and the central gate electrode. Despite these challenges, the novel ES-doped MOSFET demonstrates a way to substantially improve subthreshold characteristics of BP MOSFETs while introducing no intrinsic on-state performance limitations. As stated previously, this subthreshold performance enhancement comes primarily from an increased tunneling distance at the drain as well as a band gap filtering effect which suppresses thermionic emission of carriers. It is suspected that in the ES-doped BP MOSFET ambipolar current comes primarily from band-to-band-tunneling, especially at higher-V_{DS} values. The next section will explore the transport mechanisms of the ambipolar current more thoroughly by performing low temperature measurements as

well as device modeling. These results will then be used to further explore the benefits of ES-doped BP MOSFETs over Schottky contacted BP MOSFETs.

3.3 Band-to-band-tunneling in ES-doped BP MOSFET

ES-doped BP MOSFETs using the triple-gated device structure allow for the exploration of other transport mechanisms because of the ability to tune the potential profile of the BP in the source, drain, and channel regions. Band-to-band tunneling is one interesting mechanism that occurs when a tunneling window is opened between the valence band and conduction band of adjacent semiconductor regions. This window can be opened by utilizing two adjacent degenerately doped p and n semiconductor regions and tunneling most commonly occurs when the p+/n+ junction is reverse biased. In the triple-gated device structure, this p+/n+ junction is created by electrostatic gating and in the ES-doped MOSFET this occurs when the transistor is biased in the OFF-state. In the OFF-state of the ES-doped p-MOSFET for example the channel is becomes n-type, and the drain is doped p-type. The reverse bias is applied by the negative bias applied at the drain. In this section band-to-band-tunneling in ES-doping BP MOSFETs will be explored using low-temperature characterization and device modeling and show how transistors with ambipolar current limited by BTBT exhibit superior subthreshold performance.

3.3.1 Low-temperature MOSFET Characterization

In order to observe pure BTBT in BP it is necessary to measure the devices at low temperature because at room temperature, trap assisted transport mechanisms like trap-assisted-tunneling (TAT) and Schokley-Reid-Hall (SRH) generation can be dominant over BTBT. These are temperature dependent effects while BTBT is not, so a lack of temperature dependence is a strong indicator of BTBT being the dominant transport

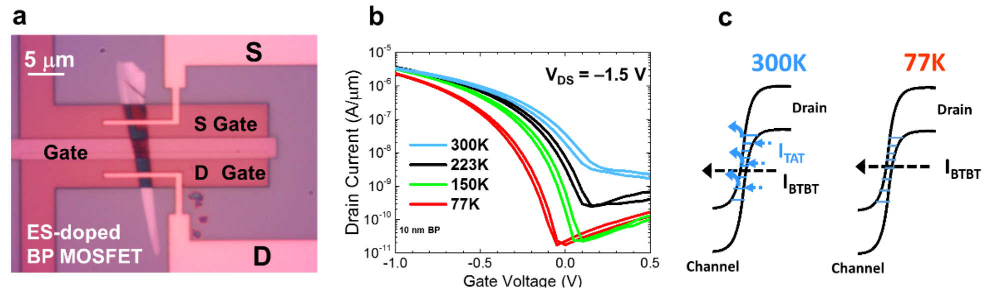


Figure 3.7 (a) Optical micrograph of ES-doped BP MOSFET (10 nm thick BP). (b)Transfer characteristics of ES-doped MOSFET with $V_{SG/DG}$ = −6.0 V at multiple temperatures.(c) band diagrams showing transport mechanisms at T = 300 K and T = 77 K.

mechanism. The ES-doped BP MOSFET shown in the optical micrograph in Figure 3.7(a) was used to explore BTBT tunneling in BP and explore how subthreshold performance is improved over the Schottky MOSFET. The BP thickness in the ES-doped MOSFET was 10 nm, which conveniently allows for the direct comparison between a Schottky MOSFET with a BP thickness of 10 nm. The device was characterized in a Lakeshore Vacuum probe station and the temperature was controlled using a Lakeshore temperature controller with liquid nitrogen flowed through a vacuum transfer line being used as the cooling agent. Figure 3.7(b) shows the transfer characteristics of the device measured at temperatures from T = 300 K to T = 77 K. At T = 300 K, the ambipolar leakage current (at V_{GS} > 0.1 V) shows little V_{GS} dependence and is relatively high, however a large decrease in this leakage

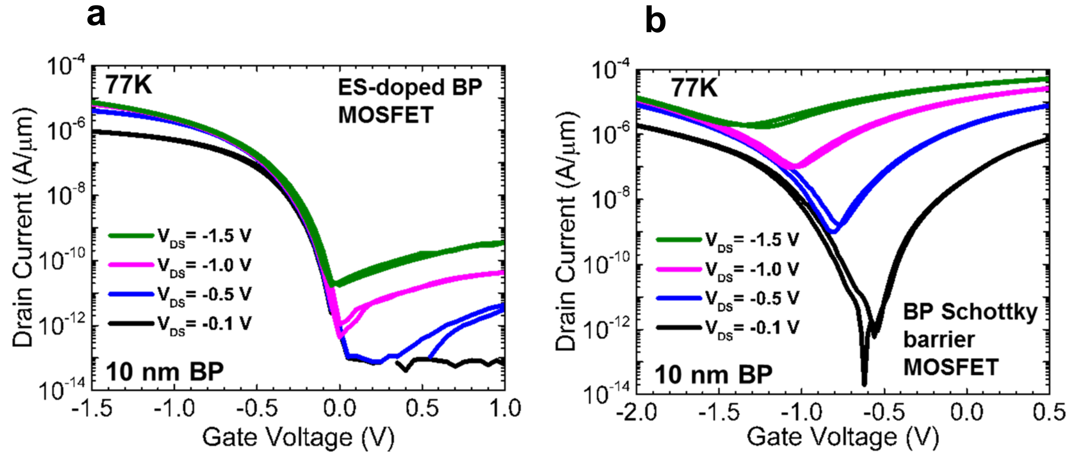


Figure 3.8 (a) Transfer characteristics of the ES-doped MOSFET with $V_{SG/DG} = -6.0$ V at multiple V_{DS} values. I_{MIN} increases with V_{DS} but a high I_{ON}/I_{OFF} of greater than 10^4 is maintained.(b)Transfer characteristics of Schottky contacted MOSFET at multiple V_{DS} values. I_{MIN} is increases by 10^7 at V_{DS} = -1.5 V decreasing I_{ON}/I_{OFF} to less than 10.

current is observed as the temperature decreases to 223 K and 150 K. This lack of V_{GS} dependence and strong temperature dependence at T = 300 K indicates that trap-assisted transport mechanisms like TAT likely dominant at room temperature. However between 150 K and 77 K there is not a significant change in the ambipolar current characteristic as the temperature decreases from 150 K to 77 K. In addition to this, a positive V_{GS} dependence is observed. This lack of temperature dependence and positive V_{GS} dependence indicates that BTBT tunneling is the primary transport mechanism below T = 150 K because BTBT should not show any temperature dependence and because as V_{GS} becomes more positive, it is expected that the tunneling distance between the drain and the channel becomes shorter and BTBT current becomes larger, which would explain the observed positive V_{GS} dependence. The band diagram in Figure 3.7(c) shows how at T = 300 K trap-assisted transport mechanisms are the dominant transport mechanism as carriers tunnel from the valence band in the drain into mid-gap traps where they can then thermally emit (origin of temperature dependence) into the channel conduction band. At T = 77 K, these

traps are frozen out and carriers must tunnel directly from the valence band in the drain into the conduction band of the channel.

Comparing the transfer characteristics of the ES-doped MOSFET and a Schottky contacted BP MOSFET at T = 77 K allows us to observe the advantage of the ES-doped BP MOSFET without trap effects and the ambipolar current is entirely limited by BTBT. Both devices were fabricated using 10 nm-thick BP as the channel with a 7 nm HfO_2 gate dielectric for the ES-doped MOSFET and a 10 nm HfO_2 gate dielectric for the Schottky contacted MOSFET. The transfer characteristics in Figure 3.8 show the dramatic suppression of ambipolar current when it is limited by BTBT current. For example, at V_{DS} = -0.5 V and V_{GS} ~ +1.0 V from V_{MIN} the ambipolar current is more than 5 orders of magnitude higher in the Schottky contacted MOSFET. The suppressed ambipolar current in the ES-doped BP MOSFET also results in lower I_{MIN} and SS, especially at high V_{DS} values (compared quantitatively in Figure 3.9). These results again show superiority of ES-doped MOSFETs over Schottky contacted BP MOSFETs for subthreshold performance.

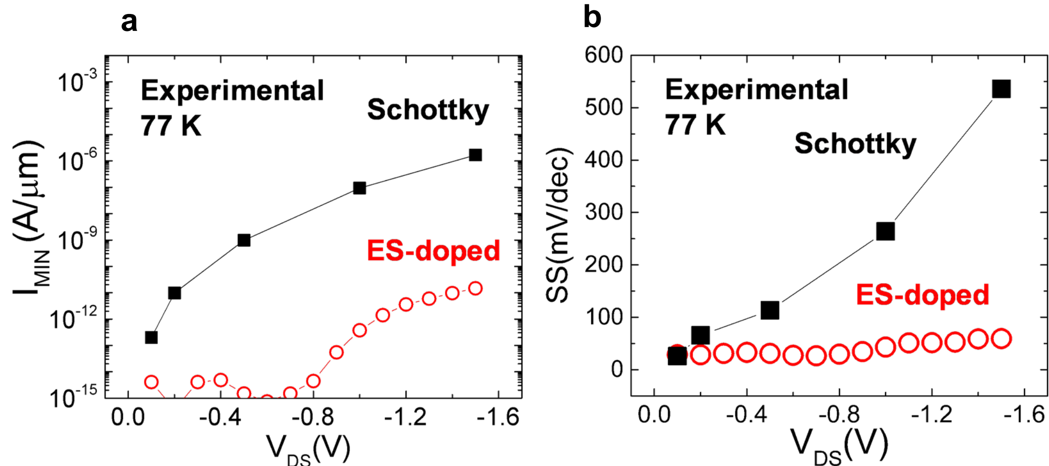


Figure 3.9 I_{MIN} and SS vs. V_{DS} for ES-doped and Schottky contacted BP MOSFETs at T = 77 K when ambipolar current is limited by BTBT. Lower I_{MIN} and SS are observed for ES-doped BP MOSFETs.

In the next section, I will show a device model that helps in understanding of the mechanisms that suppress ambipolar current in ES-doped BP MOSFETs.

3.3.2 Modeling subthreshold transport in ES-doped and Schottky-contacted BP MOSFETs

The device model used to simulate the subthreshold characteristics of ES-doped and Schottky contacted BP MOSFETs is similar to the Shottky-barrier MOSFET (SBM) model developed by Das et al.[105], Penumatcha et al.[94], and Haratipour et al.[63]. The SBM model calculates transport from BTBT, thermionic field emission through a Schottky barrier, and thermionic emission using the 1D WKB approximation with an elliptical model for κ(E), as well as thermionic emission. Potential profiles of the devices were modeled by using approximate solutions to the 2D Laplace equation with the same assumptions as Ilatikhameneh et al. [106] where (1) the space between gates is 0, (2) the thickness of the BP is << then the total thickness of the device, (3) the total thickness of the BP is << than the length of the device, and (4) the total charge in the transport region is small enough to

Parameter	Value
HfO_2 thickness (t_{HfO_2})	**10 nm**
HfO_2 dielectric constant (ε_{HfO_2})	**16.6**
BP thickness (t_{BP})	**10 nm**
BP dielectric constant (ε_{BP})	**8.3**
Orientation	**Zigzag**
Contact Potential (E_v-E_{vdoped})	**0.35 eV**
D_{IT} (#/cm^3)	**0**

Table 3.2 Parameters used in ES-doped and Schottky contacted BP MOSFET model.

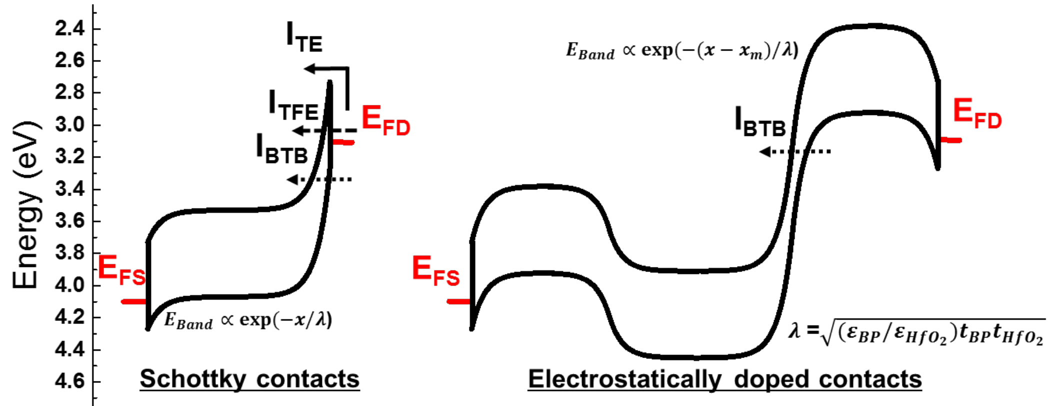


Figure 3.10 Band diagrams representing a Schottky-contacted BP MOSFET (left) and a BP MOSFET with electrostatically doped source and drain regions (left). Device parameters are shown in Table 3.2. Arrows indicate carrier paths for thermionic-emission (TE), thermionic-field-emission (TFE), and band-to-band tunneling (BTBT).

be negligible so that Laplace's equation can be solved instead of Poisson's. The first two assumptions are not necessarily the case in our devices because we are not using monolayer BP, however, the simplification can be made the assumptions can be used to generate a qualitative model. The potential profiles of the devices solved for using these assumptions and the listed device parameters (from Table 3.2) are shown in Figure 3.9. The device parameters represent a typical BP MOSFET, similar to the experimental devices in the previous sections. The model was constructed with MATLAB, using the WKB approximation and Landauer's formalism. First, the total (*S* and *D*) transmission probability at a given energy level was calculated from Equations 3.1 and 3.2.

$$T(E) = \exp(-2\int_{x_1}^{x_2} \kappa(E)dx) \tag{3.1}$$

In these equations, $\kappa(E)$ is calculated from an elliptical model from [107] in equation 3.2.

$$\kappa(E) = \begin{cases} \frac{\sqrt{m_h E(2-E/E_q)}}{\hbar}, \ for\ 0 < E < E_q \\ \frac{\sqrt{m_e(E_g-E)[2-(E_g-E)/(E_g-E_q)]}}{\hbar}, \ for\ E_q < E < E_g \end{cases} \tag{3.2}$$

In equation 3.2, E represents a given energy, m_h and m_e represent the electron and hole effective masses, E_g represents the band gap, and $E_q = E_g m_e/(m_e + m_v)$ is the branch point for continuity. Back in equation 3.1, $x_2 - x_1$ represents the tunneling distance at the source or drain. In the Schottky and ES-doped devices this distance is calculated by solving the following potential profiles in equations 3.3-3.5 for both *x* values at an energy level *E* and taking the difference. These equations are for the drain side, but are roughly symmetric at the source.

$$E_c(x) = E_c(drain)\exp\left(-\frac{x}{\lambda}\right) \qquad Schottky \tag{3.3}$$

$$E_{v-drainregion}(x) = E_v(drain) - \frac{(E_v(drain) - E_v(channel))}{2}\exp\left(-\frac{x}{\lambda}\right) \qquad ES - Doped \tag{3.4}$$

$$E_{c-channelregion}(x) = E_c(channel) + \frac{(E_c(drain) - E_c(channel))}{2}\exp\left(\frac{x}{\lambda}\right) \qquad ES - Doped \tag{3.5}$$

In these equations, E_c and E_v represent the conduction and valence bands of the BP. $E_x(channel)$ equals the energy level at the middle of the channel and $E_x(drain)$ equals the energy at the drain contact. λ is equal to the 2D natural scaling length in Equation 1.2 and x is the distance from the drain. The total tunneling probablility is calculated from both the source and drain tunneling probabilities in equation 3.6.

$$T_{total}(E) = \frac{T_S(E)T_D(E)}{1 - (1 - T_S(E))(1 - T_D(E))} \tag{3.6}$$

Where T_S and T_D represent the tunneling probabilities at the source and drain respectively. This equation for tunneling probability is then used in Landauer's equation (equation 3.7) to calculate the total electron or hole current.

$$I = \frac{2q}{h}\int_{E_c}^{\infty} T_{total}(E)M(E)\big(f_1(E) - f_2(E)\big)dE \tag{3.7}$$

Qualitatively this equation can be described as integrating the current at each energy level which is calculated by multiplying the total tunneling probability ($T_{total}(E)$) by the number of one-dimensional modes in the channel per unit width ($M(E)$) and the Fermi-Dirac distribution difference between the source and the drain ($f_1(E) - f_2(E)$). For holes, the integral goes from $-\infty$ to E_v. The total current is then the electron current plus the hole current.

The simulated room temperature transfer characteristics of the ES-doped BP MOSFET and Schottky contacted BP MOSFET are shown in Figure 3.10. The V_{DS} dependence of I_{MIN} is also simulated and compared with experimental results at T = 300 K and T = 77 K in Figures 3.11 and 3.12. These results show that the trends predicted in the

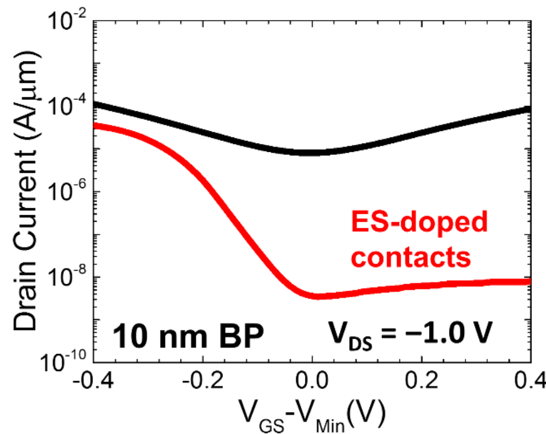


Figure 3.11 Simulated transfer characteristics of BP MOSFETs. Results show that electrostatic contacts reduce the minimum current by > 1000× by only allowing ambipolar transport via BTBT.

model are valid at $T = 77$ K when traps are frozen out but not at 300 K because traps are not included in the model but are present in the experimental devices. The consistency between the model and the experimental results also further validate that the ambipolar current at low temperatures in the BP MOSFET is limited by band-to-band-tunneling. These results also provide more insight into the mechanisms that suppress ambipolar current in ES-doped BP MOSFETs which lead to improved subthreshold performance. The suppression of ambipolar current in BP MOSFETs can be described qualitatively using the band diagrams in Figure 3.9. From these band diagrams, it is apparent the Schottky contacted MOSFET has three transport mechanisms that contribute to the ambipolar current, thermionic emission where carriers emit over the Schottky barrier, thermionic field emission where carriers with energies above the contact valence band and below the conduction band edge tunnel through the triangular barrier, and BTBT where carriers tunnel directly from the valence band to the conduction band. In the ES-doped BP MOSFET with traps frozen out the only ambipolar transport mechanism is BTBT, this is

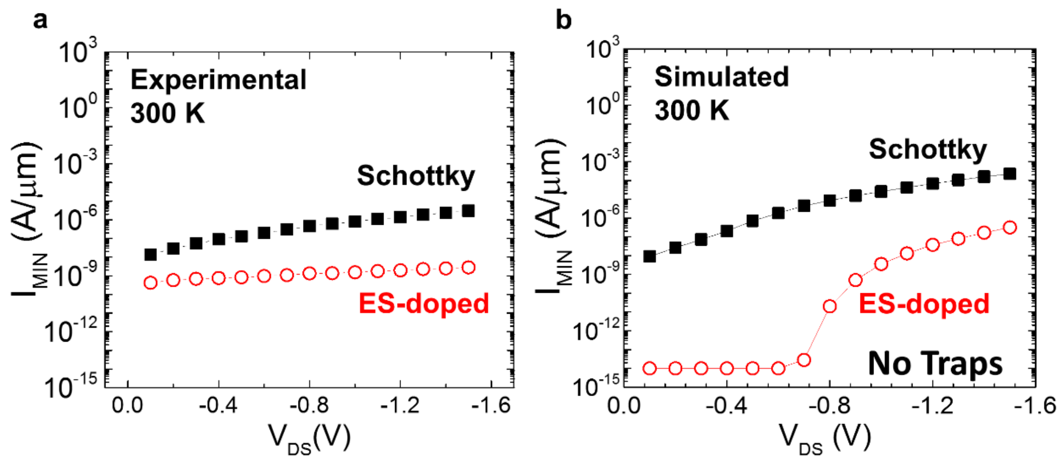


Figure 3.12 I_{MIN} vs. V_{DS} for experimental and simulated ES-doped and Schottky contacted BP MOSFETs at $T = 300$ K.

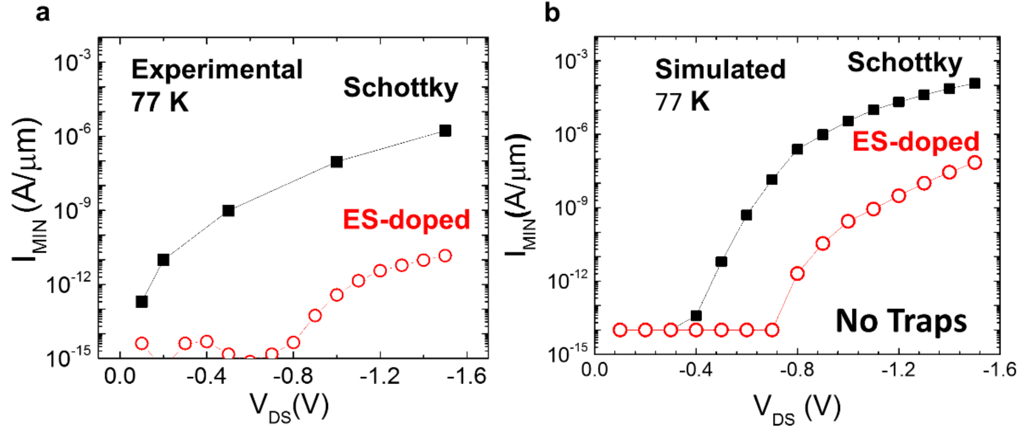


Figure 3.13 I_{MIN} vs. V_{DS} for experimental and simulated ES-doped and Schottky contacted BP MOSFETs at T = 77 K.

because of the band gap filtering effect. Since TE and TFE result in higher transmission probabilities than BTBT, the elimination of these two mechanisms accounts for the substantial suppression of ambipolar current in ES-doped BP MOSFETs.

3.4 Summary

This section presents a novel triple-gated device structure which is used to realize ES-doped BP p and n- MOSFETs that show suppressed ambipolar current and improved subthreshold performance. This device structure was also used to explore band-to-band-tunneling in BP and how the transport being limited to BTBT enables the suppressed ambipolar current. In the next chapter, this device structure and these findings with be expanded upon the demonstrate tunneling-field-effect-transistors using BP.

CHAPTER 4 BLACK PHOSPHORUS TUNNELING-FIELD-EFFECT-TRANSISTORS

Another device that's intended to improve the subthreshold characteristics in transistors is the tunneling-field-effect-transistor. Its discovery was motivated by, rising power consumption in advanced CMOS processors which is a current limitation for the future of scaling. In fact, Dennard scaling, where power consumption stays the same as transistors are made smaller, ended as far back as 2005 resulting in only marginal performance increases over the past decade. As discussed previously, one primary cause for the end of Dennard scaling is the inability to reduce the supply voltage due to the thermal transistor subthreshold slope (SS) limit of 60 mV/dec at room temperature. TFETs present a solution to this because of their potential for achieving SS < 60 mV/dec. In a similar way that was described in the previous chapter, TFETs utilize band gap filtering effectively cut off the high energy "Fermi tail" of the carrier distribution thereby enabling SS < 60 mV/dec. Despite this promise, it has proven difficult to realize TFETs with SS < 60 mV/dec and high on-state performance. One reason is that, when using this filtering effect, the primary transport mechanism becomes band-to-band-tunneling (BTBT) which tends to result in lower I_{ON} values in transistors and is highly sensitive to channel material properties [65], [66].

To understand how to achieve high performance in a TFET (high I_{ON} and steep SS at high I_{ON}) it is important to consider the fundamental transport mechanism of BTBT and that is important to have efficient tunneling from the source into the channel. To understand how to achieve this it is useful to consider that BTBT current is proportional to the

tunneling probability which follows the below proportionality.

$$I_D \propto T \propto e^{(-2*\kappa*x)} \tag{4.1}$$

Where κ is equal to the electron decay constant in the band gap of a semiconductor and x represents the tunneling length. From this, it is apparent that in order to maximize the tunneling efficiency for a given bias condition, it is necessary to minimize κ and x. The electron decay constant κ depends on the semiconductor properties, so in order to minimize it, an appropriate channel material must be chosen. Figure 4.1 shows a graphical

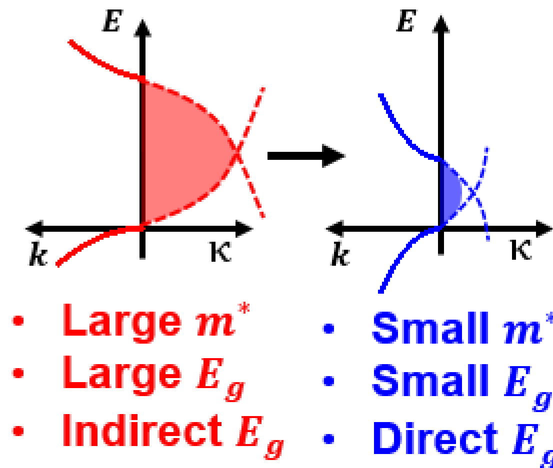


Figure 4.1 Cartoon E-k diagrams representing the band structures of two semiconductors with the solid lines representing the real bands and dashed lines representing the imaginary bands. The shaded reason represents the decay constant κ.

representation of how κ depends on some common semiconductor material properties using typical energy vs. k diagram (real k on left axis and imaginary k on right axis) that show the band structures for a large, indirect band gap semiconductor with a large effective mass (left) and a small direct band gap semiconductor with a small effective. κ in this figure is represented by the area under the dashed lines which represent the imaginary band structure in the band gap of the semiconductor. From this cartoon figure, it is clear that in order to minimize κ a semiconductor with a small effective mass, and a small direct band

gap should be chosen.

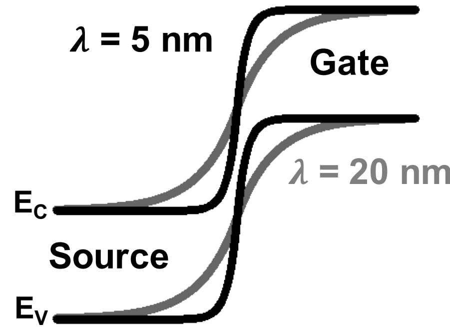


Figure 4.2 Band diagrams representing the band bending between the gate and the source of a TFET. It is apparent that when the scaling length is small the band bending is steeper and the tunneling distance is smaller.

In order to minimize the tunneling distance x the device geometry must be optimized. As shown previously in Section 3.3.2, a first order approximation of the band bending at an interface between two gates says that the band edge increases or decreases exponentially as $e^{(\pm x/\lambda)}$. Where λ again is represented by the natural scaling length in the device. Because steep band bending is desired to decrease the tunneling distance as shown in Figure 4.2, the natural scaling length parameter λ should be minimized in TFETs. For a 2D channel geometry this scaling length is represented by equation 4.2.

$$\lambda = \sqrt{\frac{\epsilon_{Channel}}{2\epsilon_{ox}} t_{Channel} t_{ox}} \tag{4.2}$$

So in order to minimize the tunneling distance, a thin channel material and thin high-k gate oxide is desired. In addition to these properties, some other considerations are important for realizing high-performance TFET devices. For one, it is important to have some source/drain asymmetry to suppress ambipolar current, which similarly to MOSFETs can degrade subthreshold performance. It is also helpful for the semiconductor material to have a large source density of states (DOS) so that high doping concentrations can be achieved

without having to move the fermi level far down into the bands where "band gap filtering" would be less effective. Last but certainly not least is that materials and interfaces should have low defect/trap densities since traps lead to parasitic transport mechanisms which degrade SS and I_{OFF} in TFETs.

In the introduction it was briefly discussed that Si, III/V materials, and III/V heterojunctions have been used as materials for TFETs and that each of these materials systems had flaws that prevented optimum performance and/or manufacturability. For Si, the large effective mass and larger in-direct band gap prevented high I_{ON} from being achieved. In III/V homojunctions, the small, direct band gaps, allow higher I_{ON}, but subthreshold performace is limited by poor interfaces and ambipolar carrier injection from the drain. III/V heterostructures have shown good performance but require complex fabrication process and performance increases are limited by the lack of scalability of the bulk materials used.

Black phosphorus, however presents itself as a potential ideal channel material for TFETs as it has most of the desirable material characteristics such as small effective masses $m_e = 0.16*m_0$ and $m_h = 0.14*m_0$ in the AC direction, a small, direct band gap (0.3 eV (bulk) to 2.0 eV (monolayer)), and it can be scaled below 1 nm. The anisotropic effective mass and thickness dependent band gap can also be utilized to induce source/drain asymmetry, suppressing ambipolar current. In addition the inducing asymmetry, the anisotropic effective mass also leads to a large DOS. Finally, BP could potentially form higher quality interfaces with gate dielectrics because it bonds via the Van der Waals force and does not have any dangling bonds which can lead to trap states. In the introduction, a number of demonstrated, simulation based BP devices were reviewed which showed how these

characteristics could result in TFETs with record performances and channel lengths as small as 2 nm. This chapter presents what was the first experimentally reported BP TFET. This device is enabled by the triple-gated device structure presented in Chapter 3. The triple gated structure allows three independently doped regions so p+/i/n (n-TFET) and n+/i/p (p-TFET) doping profiles necessary for TFETs can be created. To study transport in BP TFETs, we perform temperature dependent measurements and Arrhenius analysis to study the effects of trap-assisted-tunneling and Shockley-Reid-Hall generation, a mechanism which degrades *SS* at room temperature. In addition to this we explore BTBT transport showing BTBT current anisotropy (I_{AC}/I_{ZZ}) as high as ~ 10^3 in BP TFETs. Finally, the subthreshold performance of the BP-TFET in the AC direction will be explored showing *SS* approaching the thermionic limit at low temperature. Many of the results from this section have been published in reference [31].

4.1 Crystal Oriented BP TFET Fabrication

The fabrication process for the BP-TFETs was very similar to the process used for the ES-doped MOSFETs in Chapter three with some slight differences. The main difference is that we decided not to embed the first layer of gates in the SiO_2 because of yield issues that arose due to roughness created from the etch process. Instead, we used a lift-off process with a bi-layer resist to deposit thin Ti/Pd gates (~25 nm). This resulted in thin metal gates with smoothed edges that allowed us to stack multiple layers without

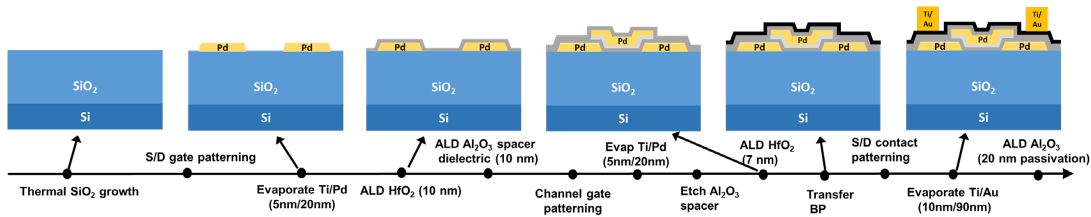


Figure 4.3 Process flow for BP-TFETs.

leakage issues. The process flow is shown in Figure 4.3 and described below. The first step in the process was the patterning of source-gate and drain-gate electrodes using E-beam lithography followed by the deposition of 5 nm Ti /20 nm Pd using electron-beam evaporation. A bi-layer resist consisting of 250 nm of Co-MMA and 150 nm of PMMA was used for E-beam lithography/liftoff process. Next, ALD was used to deposit 10-nm of HfO_2 as a gate dielectric and 10-nm of $A1_2O_3$ as a gate spacer to reduce leakage between the source/drain gates and the channel gate. Next, the channel-gate was patterned using E-beam lithography, designed so that it overlaps the source and drain-gate electrodes. After the deposition of the 5 nm Ti /20 nm Pd channel-gate electrode using E-beam evaporation, the $A1_2O_3$ gate spacer was etched using ammonium hydroxide in the regions not under the gate electrode. Next, ALD was again used to deposit 7 nm of HfO_2 gate oxide. BP was then exfoliated from a bulk crystal and aligned and transferred to the two perpendicular triple-gate structures in a nitrogen purged glove box, using a PDMS stamp. In order to predict the crystal orientation of the exfoliated BP the shapes of BP flakes were examined with the assumption that BP crystals are most likely to cleave along the AC and ZZ orientations. An appropriately shaped flake was found and aligned so that the two perpendicular TFET channels would be aligned along flakes cleavage planes, corresponding to the AC and ZZ orientations.

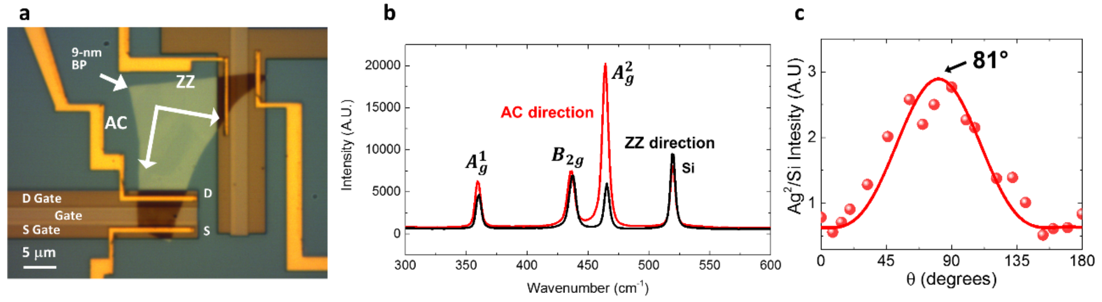


Figure 4.4 (a) Optical micrograph of completed device with arrows representing the BP crystal orientation determined by polarized Raman characterization shown in (c) and (d).

After BP transfer, Ti/Au contacts were made to the BP and finally a passivation layer of 20 nm of $A1_2O_3$ was deposited by ALD. An optical micrograph of the completed device with arrows indicating the AC and ZZ orientation is shown in Figure 4.4. Raman spectra was collected using a 532 nm illumination source linearly polarized aligned to the horizontal electrode at 0 degrees. The sample was rotated clockwise with respect to the polarization direction with spectra collected at different angels between 0 and 180 degrees. Past literature indicates that the A_g^2 peak reaches a maximum when the light polarization is aligned parallel to the AC direction and a minimum when the polarization is parallel to the ZZ direction [108]. Figure 4.4(mid) shows the raman spectra with the maximum and minimum A_g^2 peaks representing the points in which the light is polarized parallel to the AC and ZZ crystal orientations. Figure 4.4(right) shows how the A_g^2 peak magnitude changes as the sample is rotated clockwise with respect to the light polarization. The red points represent experimentally collected data and the solid red line represents a curve fitting in order to extrapolate the maximum. Using this plot, it is apparent that the maximum A_g^2 peak occurs when the sample is rotated 81 degrees clockwise from the initial horizontal orientation. This indicates the BP AC and ZZ orientations are aligned within 10 degrees of

the AC and ZZ BP-TFET transport directions.

4.2 Room Temperature BP TFET Characterization

Device characterization was performed in a vacuum probe station using an Agilent 4156C parameter analyzer with 41501B expander unit enabling the use of a fifth SMU. The triple-gated device structure makes the device reconfigurable so that it can be measured as a MOSFET or a TFET by changing the source doping by changing the source gate voltage. Figure 4.5 shows the I_D vs. V_{GS} of the triple-gated BP FET measured under different source gate voltage conditions. The corresponding bias conditions and band diagrams are shown in Figure 4.5(b). Initially, V_{SG} was set to 0 V (black), which resulted in a p-MOSFET characteristic due to residual p-type doping in the exfoliated BP. As V_{SG} was increased to 1.25 V (blue) the BP source region becomes depleted and the p-MOSFET

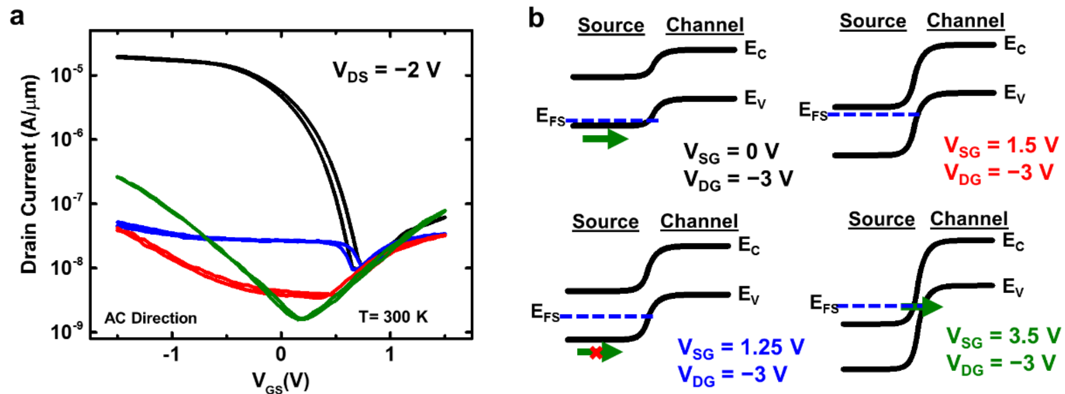


Figure 4.5 Results for BP FET at 300 K and at different values of source gate voltage showing transition from MOSFET to TFET operation. Band diagrams in (b) show transition in transport from thermionic emission to BTBT.

no longer turns on. Increasing V_{SG} further to 1.5 V (red) the source starts to become n-doped and the device starts to show a weak p-TFET turn-on behavior. When V_{SG} is set to 3.5 V (green) the source becomes heavily n-doped and a large increase in current is observed at negative V_{GS}. This large increase in current would be unexpected with thermal

transport since the thermal barrier of the junction is increasing, thus indicating tunneling through the barrier as the primary transport mechanism. This characteristic confirms that we are measuring a BP-TFET. Figure 4.6(b) shows the BP p-TFET I_D vs. V_{GS} characteristics at different V_{DS} values at $V_{SG} = +3V$ and $V_{DG} = -3V$. The characteristics are well behaved with minimal hysteresis and a SS of ~ 300 mV/dec which is limited by trap-assisted transport mechanisms at low V_{DS} and ambipolar tunneling current at higher V_{DS} values. These mechanisms will be explored further in later sections. Figure 4.6(a) shows the output characteristics of the BP p-TFET measured under the same source and drain gate conditions, showing a non-linear turn on behavior commonly seen in TFETs due to fact that increasing V_{DS} also decreases the tunneling distance at the source and opens more available energy states for electrons to tunnel into. I_{ON} in this device is relatively low at −0.9 μA/μm but can be improved in future iterations of the device by scaling the gate oxides and also optimizing the geometry of the triple-gate structure to minimize the topography over the gates. Step heights caused by the gates (25 nm in this device) can create a lower capacitance region because the BP may not conformally cover the step. While these room temperature characteristics show a working BP-TFET, in order to further explore the fundamental transport mechanisms in the device and understand how to optimize performance a temperature dependent measurement was performed.

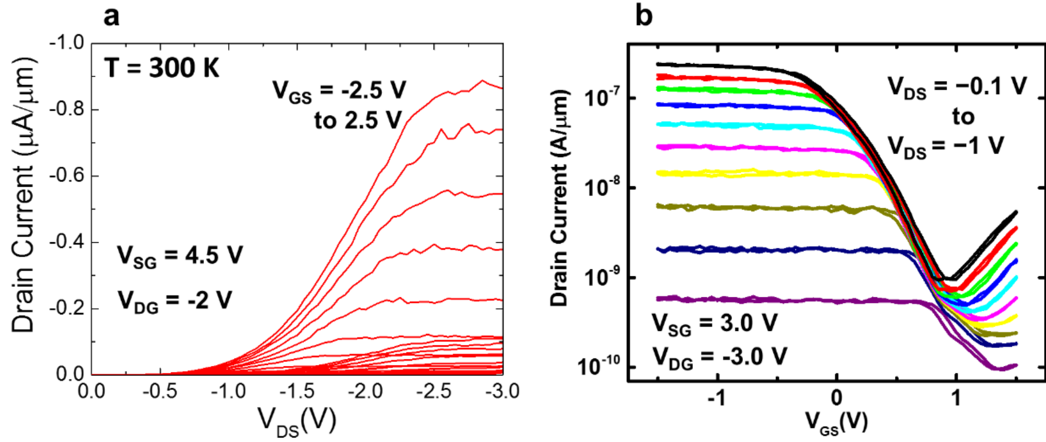


Figure 4.6 Output characteristics and Transfer Characteristics of the BP-TFET at room temperature.

4.3 Temperature Dependent characterization of BP TFETs

Low temperature measurements were again performed in the Lakeshore vacuum probe station using liquid nitrogen as the cooling agent. First, measurements were performed at T = 77 K and compared the results directly with the room temperature characteristics. Figure 4.7 shows the transfer characteristics of the AC BP-TFET at room temperature and T = 77 K. From these characteristics and the fact that BTBT should show

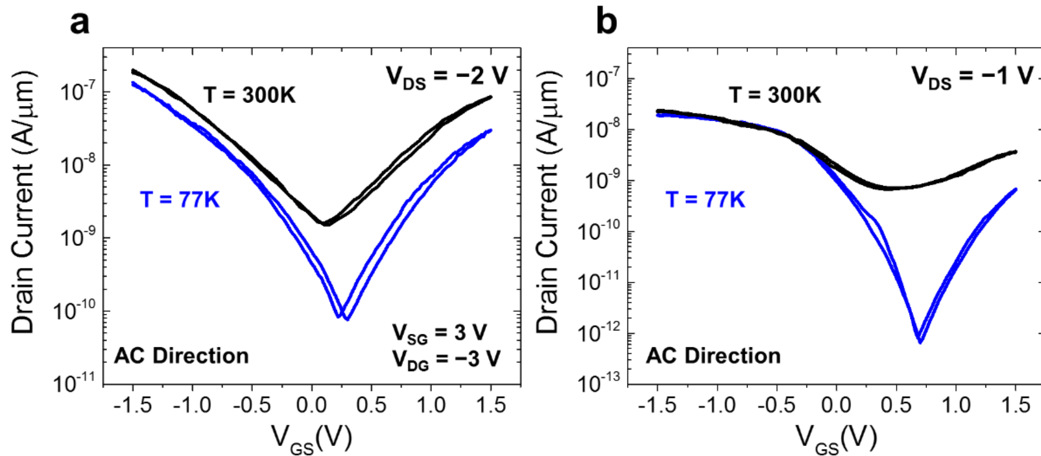


Figure 4.7 (a) RT and 77 K BP TFET transfer characteristics of AC oriented device at V_{DS} = −2.0 V. (b) RT and 77 K BP TFET transfer characteristics of AC oriented device at V_{DS} = −1.0 V.

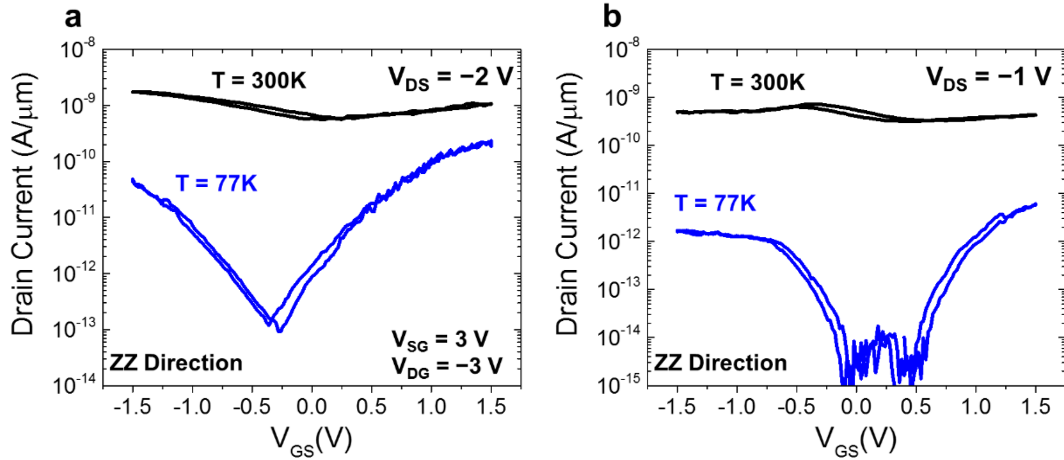


Figure 4.8 (a) RT and 77 K BP TFET transfer characteristics of ZZ oriented device at $V_{DS} = -2.0$ V. (b) RT and 77 K BP TFET transfer characteristics of ZZ oriented device at $V_{DS} = -1.0$ V.

little temperature dependence, it is suspected that when $V_{DS} = -2.0$ V the transport is primarily dominated by BTBT at room temperature and 77 K with a small contribution from trap assisted transport mechanisms at room temperature, particularly at V_{GS} close to 0 V when the device is turning off. At $V_{DS} = -1.0$ V, since the ambipolar current is lower, the OFF-state current is much lower at 77 K than it was at $V_{DS} = -2.0$ V, however at room temperature the OFF-state current is the same as at $V_{DS} = -2.0$ V which indicates that trap-assisted transport mechanisms dominate in the OFF-state at $V_{DS} = -1.0$ V in the AC BP-TFET. Figure 4.8 shows the same characteristics as 4.7 for the ZZ BP-TFET. For this device, at both $V_{DS} = -2.0$ V and $V_{DS} = -1.0$ V a large difference is observed at all V_{GS} values between the room temperature and T = 77 K characteristics. This indicates that at room temperature in the ZZ BP-TFET, all transport is dominated by trap-assisted mechanisms. The reason for this is likely that BTBT current is so low in the ZZ direction that the trap assisted-transport mechanisms, which do not necessarily depend on the BP orientation, dominate transport. From these curves, it appears that at room temperature, a

current floor exists at ~ 10^{-9} A/μm due to these trap-assisted transport mechanisms.

The specifics of these trap-assisted transport mechanisms are investigated further by performing a temperature dependent measurement at low V_{DS} in the AC BP-TFET. Figure 4.9(a) shows the I_D vs. V_{GS} characteristic for the AC BP p-TFET at $V_{DS} = -0.1$V at $V_{SG} = +3$V and $V_{DG} = -3$V at temperatures from $T = 132$ K to $T = 262$ K. It is clear from these characteristics that at lower V_{GS} when the device is in the ON-state ($V_{GS} \sim 0$ V) there is little temperature dependence, a characteristic of band-to-band-tunneling. However at OFF-state bias conditions ($V_{GS} > 0.75$ V) a large temperature dependence is observed, indicative of thermally activated trap-assisted transport mechanisms at higher temperatures. In order to further explore these mechanisms an Arrhenius analysis was performed in Figure 4.9(b) at different V_{GS} extracted from the transfer characteristics in 4.9(a). The analysis was performed using the assumption from reference [109] that the OFF-state current resembles that of a reverse biased P-N junction with equation 4.3.

$$I_D \sim A^* T^{1.5} exp\left[-\frac{E_a}{k_B T}\right] \tag{4.3}$$

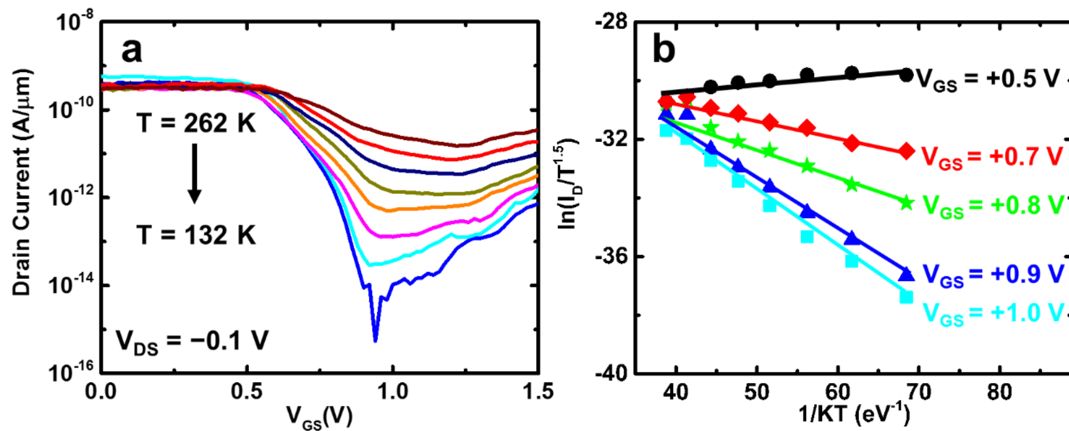


Figure 4.9 (a) Temperature dependent transfer characteristics of the AC BP-TFET. (b) Arrhenius plots extracted from the transfer characteristics in (a).

Where A^* is the modified Richardson constant, E_a is the activation energy, and k_B is Boltzmann's constant. Using this equation we generate the Arrhenius plot $ln\left[\frac{I_D}{T^{1.5}}\right]$ vs. $\frac{1}{k_B T}$ in 4.9(b), the slope of which gives E_a. Figure 4.10 displays the extracted E_a vs. V_{GS} which shows a regime in which E_a is close to zero at $V_{GS} < 0.5$ V, indicating band-to-band-tunneling current and a regime at $V_{GS} > 0.9$ V in which $E_a \sim 0.19$ eV which is approximately equal to the band gap of BP divided by 2. This activation energy indicates that in the OFF-state of the BP TFET the transport is dominated by Shockley Reid Hall (SRH) generation, a mechanism which is driven by carriers recombining in and being generated from mid-gap traps. This trap-assisted transport mechanism puts a lower limit on the BP TFET OFF-current and *SS* at room temperature, indicating that for high performance BP TFETs to be realized at room temperature, bulk and interface trap densities must be reduced. In BP, bulk traps can be caused by imperfect growth process as well as oxidation [110], [111]. Interface traps are likely primarily caused by surface oxidation of BP resulting in a defective phosphorus oxide layer which forms a Van der

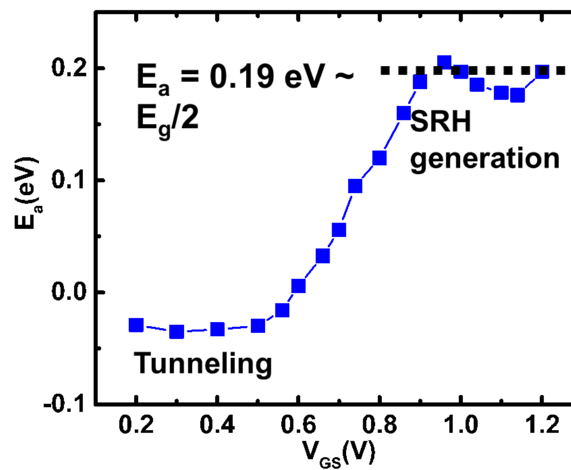


Figure 4.10 Extracted activation energy vs. V_{GS} for the AC BP-TFET at $V_{DS} = -0.1$ V.

Waals interface with the HfO_2 gate dielectric. In order to reduce trap densities, ultra-pure BP crystal growth must be achieved, and additional care must be taken to protect the BP surface from oxidation during transfer. Transferring BP in vacuum may be one way to take extra care during transfer [112]. Fortunately, the effects of trap-assisted transport can be eliminated by measuring the device at low temperature in order to freeze out traps. In the next section we characterize the AC and ZZ BP TFETs at $T = 77$ K to measure the BTBT anisotropy in BP.

4.4 Band-to-band-tunneling Anisotropy in Black Phosphorus

Next, the I_D vs. V_{GS} characteristics of the triple-gated AC and ZZ BP TFET were measured at $T = 77$ K and $|V_D| = 1.5$ V in order to measure the BTBT current anisotropy between the AC and ZZ BP direction. Measuring the device at a high $|V_{DS}|$ of 1.5 V allows us to observe the BTBT on the source side and drain side of the BP TFETs. Figure 4.11(a) shows the transfer characteristics of the AC and ZZ BP devices measured as pTFETs with $V_D = -1.5$ V, $V_{SG} = +3$ V, and $V_D = -3$ V. The V_{SG} and V_{DG} are normalized with respect to the threshold voltage in the V_{SG}/V_{DG} regions of the device. This means +/− 3V represents

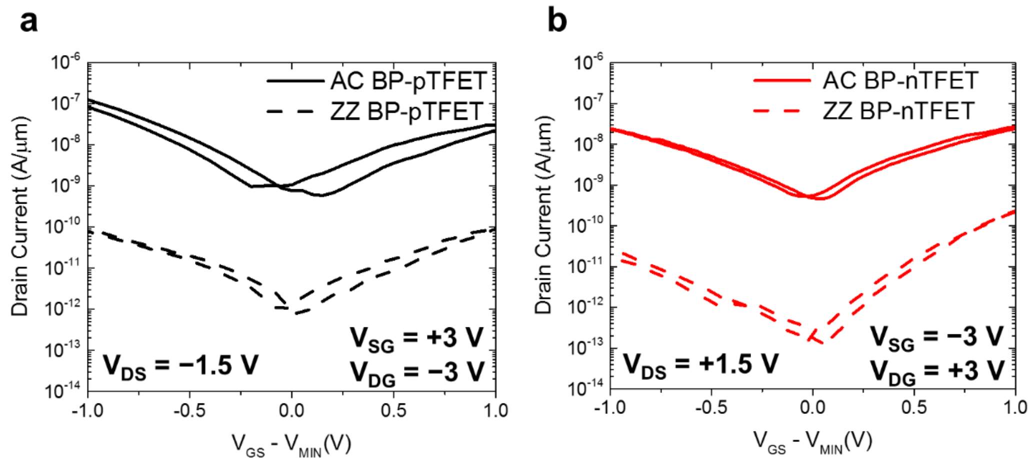


Figure 4.11 Transfer characteristics of the AC and ZZ BP TFETs measured as p-TFETs (a) and n-TFETs at $T = 77K$ at $|V_{DS}| = 1.5$ V.

the difference between the applied voltage and the voltage at I_{MIN} (~1, calculated by measuring I_D vs. V_{GS} of the devices in a pMOSFET configuration where V_{SG} is swept and the other gates are fixed at negative voltage values above threshold. This is done in order to measure the device in a symmetric configuration where the doping in the source and drain regions is approximately the same. The p and nTFET transfer curves in Figure 4.11(a) and (b) show symmetric source and drain tunneling (current at negative and positive V_{GS}) behavior as expected for a homojunction TFET with symmetric source and drain tunneling. Both the AC and ZZ BP p and n-TFETs show I_{ON}/I_{OFF} between ~10^2 and ~10^3 which is limited by the ambipolar BTBT current. Figure. 4.12 shows the extracted BTBT current anisotropy arising from the effective mass anisotropy between the AC and ZZ BP crystal axis. The value extracted is extracted simply by dividing I_{AC}/I_{ZZ} and was around ~10^3 for most of the applied gate voltages in both the nTFET and the pTFET configuration. This value is consistent with what has been calculated in other theoretical works on BP TFETs

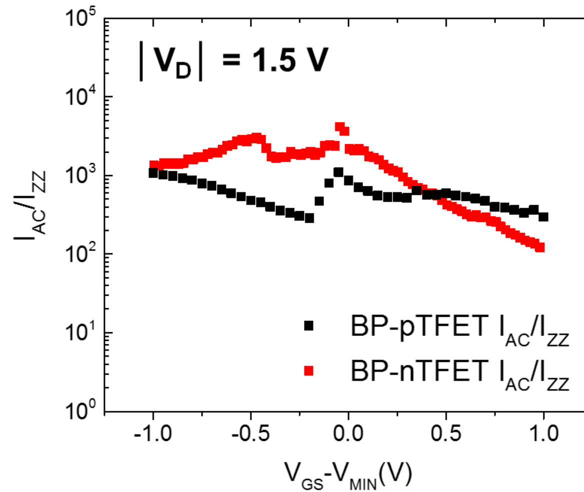


Figure 4.12 BTBT current anisotropy between the AC and ZZ BP crystal orientations. Anisotropy is extracted by dividing I_{AC} by I_{ZZ} for the BP p and n-TFETs at $|V_{DS}|$ = 1.5 V shown in Figure 4.11.

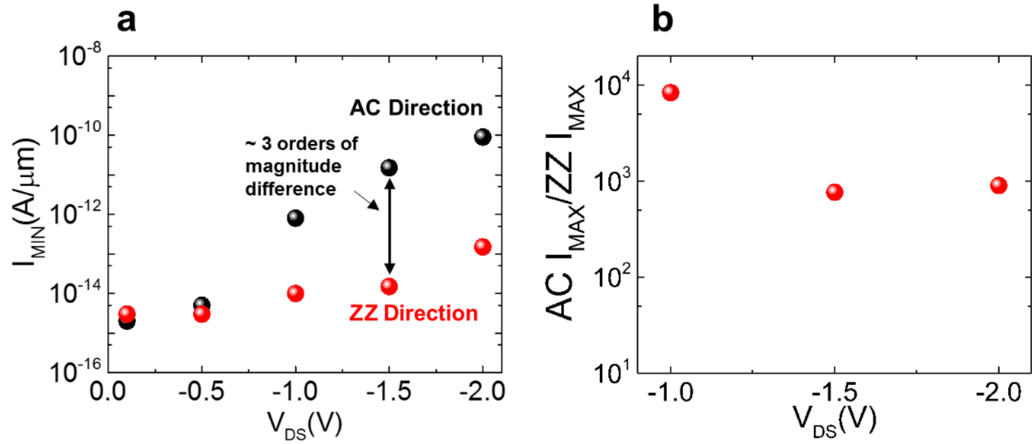


Figure 4.13 (a) I_{MIN} vs. V_{DS} for AC and ZZ BP p-TFETs. (b)BTBT current anisotropy vs. V_{DS} for the BP p-TFETs. Both are measured at T = 77 K.

[113], [75]. I_{MIN} vs. V_{DS} was also extracted for the AC and ZZ BP p-FETs as well as the BTBT current anisotropy vs. V_{DS} in order to study the dependence of BTBT current on V_{DS}. From (a) we can see that at low V_{DS} (0.1 V and 0.5V), both AC and ZZ TFETs have I_{MIN} below the noise floor, however at $V_{DS} > 1.0$ V. I_{MIN} is above the noise floor in both devices and an anisotropy of ~ 10^3 is observed between I_{MIN} of the AC and ZZ BP TFETs. This is significant because it shows that in order to achieve low I_{MIN}, ZZ BP TFETs are more suitable, but from (b) we can see that for high I_{ON}, AC BP TFETs are better. Also from 4.13(b) it is apparent the anisotropy is higher at lower V_{DS}. This can be explained by examining Figure 4.14 in which Kane's tunneling model (Equation 4.3) is used to predict the BTBT current anisotropy at different electric field values. As V_{DS} decreases, the total electric field at the tunneling interface decreases resulting in higher BTBT anisotropy according to Kane's model (equation 4.4).

$$\frac{I_{D(AC)}}{I_{D(ZZ)}} \propto \frac{G_{BTB(AC)}}{G_{BTB\,(ZZ)}} \propto \frac{\sqrt{m^*_{r(AC)}}}{\sqrt{m^*_{r(ZZ)}}} exp^{\left(\pi/3\left(\sqrt{m^*_{r(ZZ)}}-\sqrt{m^*_{r(AC)}}\right)\frac{\sqrt{2m}\,E_g^{3/2}}{eE\hbar}\right)}$$

(4.4)

According to the model, the electric field at the tunneling interface in our devices should be ~ 1 MV/cm which would mean there is 4V (based on max voltage between source-gate

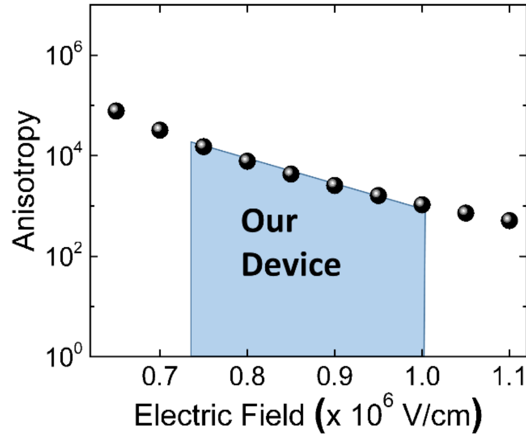


Figure 4.14 Anisotropy vs. E-field according to Kane's model for band-to-band-tunneling. Our device falls somewhere in the blue shaded region according to our measured anisotropy values.

and gate in our device) dropping over ~ 40 nm. This seems to be a reasonable estimate considering the BP may not perfectly conform to the topography of the gate. Next, considering that the AC BP TFET has the higher tunneling efficiency, we measure the AC BP TFET at lower V_{DS} values in order to examine the steepness of the *SS*.

4.5 Armchair Black Phosphorus TFET Subthreshold Performance

Next, the performance of the AC BP TFET was analyzed at low V_{DS} in order to examine the minimum *SS* that can be achieved in the device. The AC direction was studied exclusively due to the low BTBT current in the ZZ direction. At room temperature, the *SS* was over 300 mV/dec due to trap effects, so in order to probe for the ultimate performance in the BP TFET it is important to measure the device at a temperature in which traps are frozen out. This temperature is chosen based on the *SS* vs. *T* characteristics for the AC BP pTFET measured in a symmetric configuration shown in Figure 4.15. Examining this plot, it is observed that the temperature dependence of the *SS* for the BP disappears at a little below T = 150 K. Temperature independence is a sign of the traps being frozen out in TFETs because no *SS* temperature dependence is expect in the absences of traps. Based on Figure 4.15, I decided to characterize the AC BP pTFET at T = 110 K, a temperature where traps are safely frozen out, to probe for sub-thermal *SS* slope. 110 K was chosen instead of

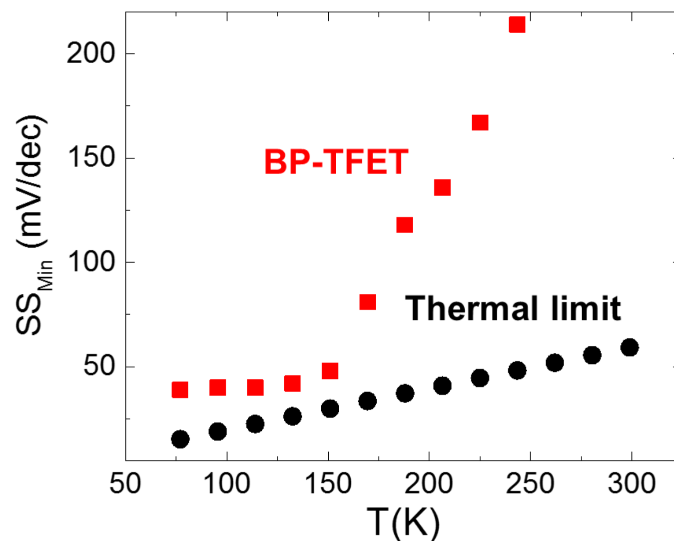


Figure 4.15 SS vs. T for the AC BP p-TFET. The predicted thermal SS limit is represented by the black dots.

77 K because the thermal *SS* is higher at 110 K giving us a better chance at being sub-thermal since the TFET *SS* should be the same at 77 K and 110 K. The transfer characteristic for the device at V_{DS} = 0.1 V and T = 110 K is shown in Figure 4.16. V_{SG} was set to + 3.0 V for this measurement and the drain-gate was left floating which minimized ambipolar current injection. The transfer curve shows no hysteresis and a gate current of ~ 10 fA/μm. This clean characteristic with a low gate current makes it a measurement to use to extract *SS* vs. I_D.

SS vs. I_D is shown in Figure 4.16 and shows a minimum *SS* of ~ 22 mV/dec at current levels above transfer curve was studied more closely in order to determine the minimum obtainable *SS*, and Figure 4.16 shows a hysteresis free transfer curve, where ~10 fA/μm is the minimum current level the *SS* can be reliably measured. *SS* vs. I_D (Figure 4.17) shows a minimum *SS* of ~ 22 mV/dec at current levels above 10 fA/μm indicating the device is approaching the subthermionic regime (< 22mV/dec at 110 K). Sub-thermal operation was

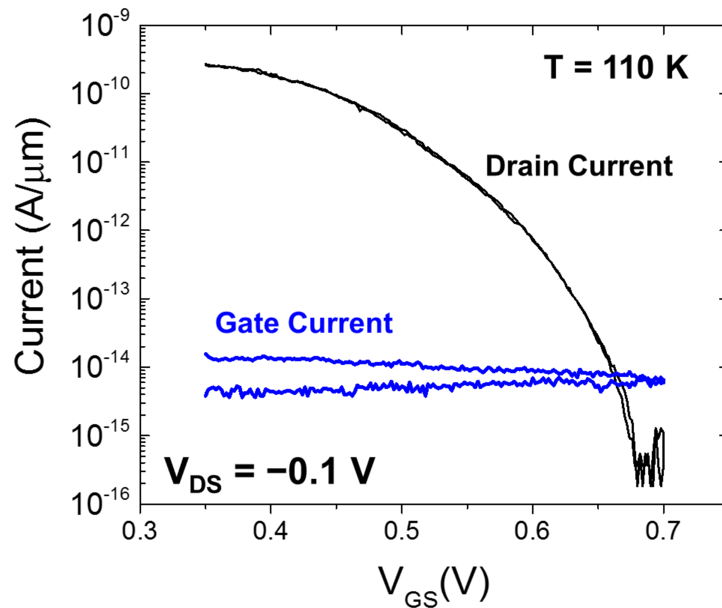


Figure 4.16 AC BP p-tfet transfer curve showing both I_D and I_G vs. V_{GS}. This curve is used to extract SS vs I_D.

likely partially prevented by the geometry of the device which requires the BP to bend over the topography of the gates, likely resulting in a non-conformal covering where there is some vacuum gap between the BP and the HfO_2 gate dielectric. A smoother gate topography could improve this enabling perfectly conformal covering of the BP to the gates, which would result in smaller tunneling distances as the tunneling window opens, leading to a steeper slope at higher current values. There could also be phosphorus oxide between the BP and that which would also reduce the gate capacitance and ultimately result in a larger tunneling distance as the tunneling window opens. We expect that improving the gate geometry and exfoliating BP in an inert or vacuum environment would result in sub-thermal *SS* at higher current levels as well as higher I_{ON}. Improving the BP purity would also reduce D_{it} and should enable steeper subthreshold slopes to be achieve at room temperatures as well.

After extracting the minimum SS in the device at V_{DS} = −0.1 V, the transfer characteristics were measured at different V_{DS} values and SS_{MIN} was extracted for each

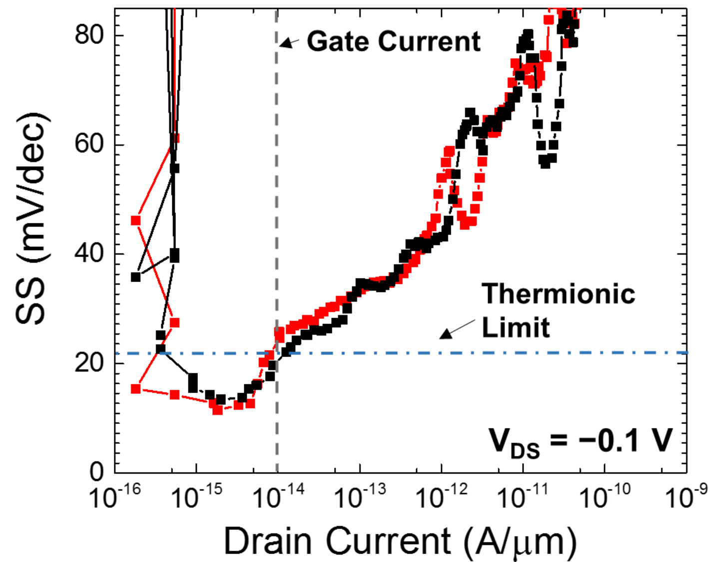


Figure 4.17 SS vs. I_D from fig. 18 transfer curve. SS approaches the thermionic limit at I_D = 10fA/µm.

value. The transfer curves and SS_{MIN} vs. V_{DS} is shown in Figure 4.18. These plots show that even with a floating drain-gate, increasing V_{DS} results in a degraded *SS*. Because of this it is important to induce asymmetry between the source and drain in some other, more effective way. In Chapter 5, I demonstrate source/drain asymmetry induced using the anisotropic effective mass of BP.

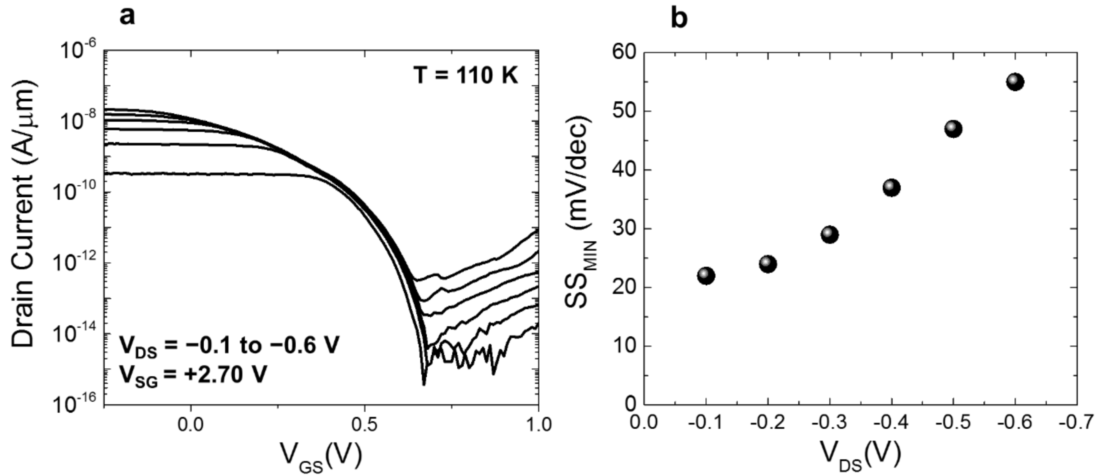


Figure 4.18 (a) Transfer characteristics for the AC BP p-TFET at T = 110 K and V_{DS} values from -0.1 V to -0.6 V. (b) SS_{MIN} vs. V_{DS} extracted from (a).

4.6 Summary

In this chapter, motivated by the material properties which make BP an ideal material for TFETs, I have described the fabrication crystal oriented BP TFETs utilizing the novel triple-gated device structure. It found through temperature dependent characterization that SRH generation dominated the OFF-state at room temperature. By measuring the devices at *T* = 77 K, the BTBT current anisotropy arising from the anisotropic effective was observed to be ~ 10^3 for all gate biases at high V_{DS}. The subthreshold performance of the AC BP p-TFET at *T* =110 K was characterized and a minimum *SS* of 22 mV/dec was observed indicating the device was approaching the thermal *SS* limit. Further device

improvements including geometry optimization to minimize the tunneling distance, improvement of BP quality and interface quality for the reduction of traps, and suppression of ambipolar current would all improve the overall device performance and could potentially enable subthermal SS at room temperature as well as higher I_{ON}. The next chapter will describe my work on suppressing ambipolar current in BP TFETs utilizing the anisotropic effective mass of BP.

CHAPTER 5 L-SHAPED BLACK PHOSPHORUS TUNNELING FIELD-EFFECT-TRANSISTOR

The previous chapter introduced BP as a potential channel material for TFETs which could enable transistors with a *SS* less than the thermal limit of 60 mV/dec at room temperature. Achieving this type of device performance could reignite Dennard scaling, allowing power density reduction in CMOS or performance improvements at equivalent power densities to today. In chapter 4, initial demonstrations of BP TFETs which revealed some of the promising aspects of BP as a TFET channel material such as the effective mass anisotropy as well as some issues that still need to be overcome such as interface improvement, geometry optimization, and methods for suppressing ambipolar current. This chapter aims to address the issue of ambipolar current in BP TFETs by utilizing the effective mass anisotropy of BP.

Common techniques for reducing source/drain asymmetry in TFETs and suppressing ambipolar tunneling current are doping asymmetry [78] or heterostructures [70], [95], however each come with their own unique difficulties. Heterostructures use a small band gap material at the source and a large band gap material at the drain in order to suppress drain side tunneling however these structures typically involve complex growth processes which can impact manufacturability. In addition to this, in bulk heterostructure materal systems lattice constants must be matched in order to achieve low-defect interfaces. BP does offer a potential solution for this with its tunable band gap and ability to produce heterostructures as described in chapter 2, however there have been no experimental demonstrations of heterostructure BP TFETs. Doping asymmetry between the source and

the drain where the source is heavily doped and the drain is lightly doped is a relatively simple way of suppressing ambipolar current since it's easy to control doping in advanced materials like Si and III/V materials. This works because a lightly doped drain will result in a larger depletion region in the drain in the OFF-state of the device. A larger depletion region means a larger distance for potential to drop over and ultimately a larger tunneling distance for carriers. This is effective in reducing drain side tunneling current but the overall effectiveness is limited by the fact that the doping in the drain can only be reduced by so much before it starts degrading ON-state current. The electrostatic doping scheme

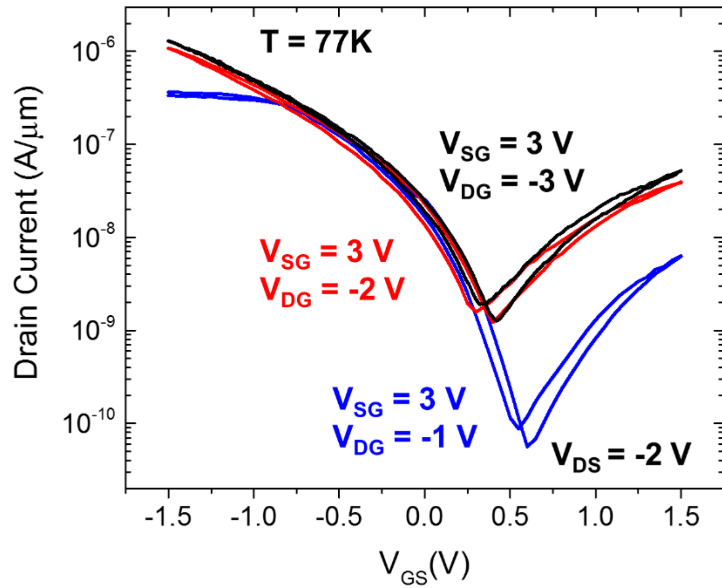


Figure 5.1 Transfer characteristics of the AC BP p-TFET from chapter 4 at different drain-gate voltage values which translates to drain doping concentrations (more lightly doped at smaller biases).

enabled by the triple-gated device structure allows for easy alteration the drain doping in order to induce source/drain asymmetry and analyze the effects on I_{ON}. Figure 5.1 shows transfer characteristics of the AC BP p-TFET from chapter 4 at different drain doping concentrations (controlled by the drain-gate voltage). From this, it is observed that as V_{DG}

is lowered and the drain becomes more lightly doped, the ambipolar current and I_{MIN} are indeed reduced by more than one order of magnitude. However, a decrease in I_{ON} is observed at large negative V_{GS} which albeit is smaller than the decrease in I_{OFF} but is still undesirable. Fortunately, BP has the unique properties such as a tunable band gap and effective mass anisotropy that can be utilized to reduce suppress ambipolar current if the drain side tunneling. The tunable band gap can be used to design a device with larger band gap region at the drain to suppress ambipolar injection. Effective mass anisotropy can also be used by designing the drain tunneling to be along the large mass ZZ direction and designing the source side to be along the light mass AC direction. In fact, in chapter 4 it was observed that tunneling in the ZZ direction is 3 orders of magnitude lower than the AC direction indicating this technique could be highly effective at reducing ambipolar current to insignificant levels. In the introduction, one paper was described that simulated a TFET which utilized the anisotropic effective mass to achieve acceptable performance all the way down to channel lengths of ~ 2 nm which was an exciting result [75]. In this chapter, I will present my work on the first experimental demonstration of an L-shaped BP TFET which utilizes the anisotropic effective mass to induce source/drain tunneling asymmetry and demonstrates improved I_{OFF} and SS over the homojunction BP TFET described in chapter 4 without any reduction in I_{ON}.

5.1 Fabrication of L-Shaped TFET

In order to create an L-shaped BP-TFET, a triple-gated device structure similar to the one described in chapter 4 was fabricated. This time, the source and drain gates were placed orthogonal to each other and the channel gate was patterned as a square to overlap the source and drain gates slightly. The top-view cartoon schematic of the device is shown in

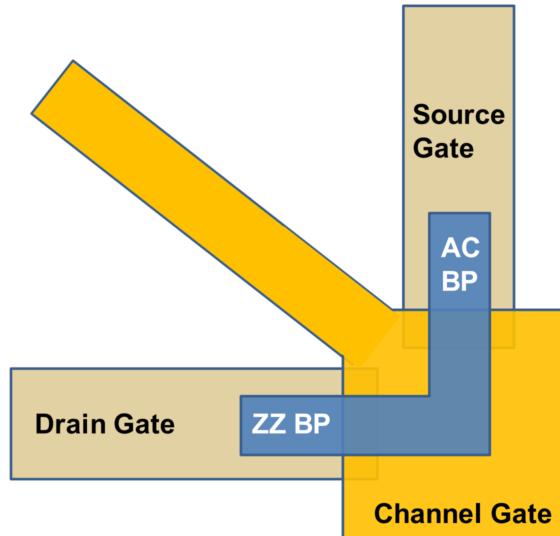


Figure 5.2 Cartoon schematic of the L-shaped BP TFET without contact layer.

Figure 5.2. The fabrication process of this device was done in the same manner to the previous device however a thinner (5 nm) Al_2O_3 gate spacer was used and this time the transferred BP flake was patterned and etched before contact pattering/deposition so that it was only present over the gates. The BP (~12 nm thick) was again transferred using the PDMS transfer process described previously using the shape of the flake to guess the orientation and align the crystal axis to be parallel to the source and drain-gates. E-beam lithography patterning followed by a 4 minute Ar^+ plasma etch (80 W) was used to pattern the BP flake using a reactive ion etching tool (RIE). Due to hardening of the PMMA from the plasma etch step, the sample was sonicated in Acetone for 5 minutes to prevent hardened PMMA from sticking to the substrate. After sonication, the sample was left to soak in acetone overnight for at least 3 hours for the complete removal of PMMA from the BP surface. Figure 5.3(a) shows an optical micrograph of the completed device. It is important to note that while the BP was not patterned into a perfect "L" shape due to the shape of the exfoliated BP flake, the two tunneling interfaces between the source/drain

gates and the channel gates are orthogonal which is what is important because the relevant tunneling transport all occurs at those interfaces. Because the dominant transport

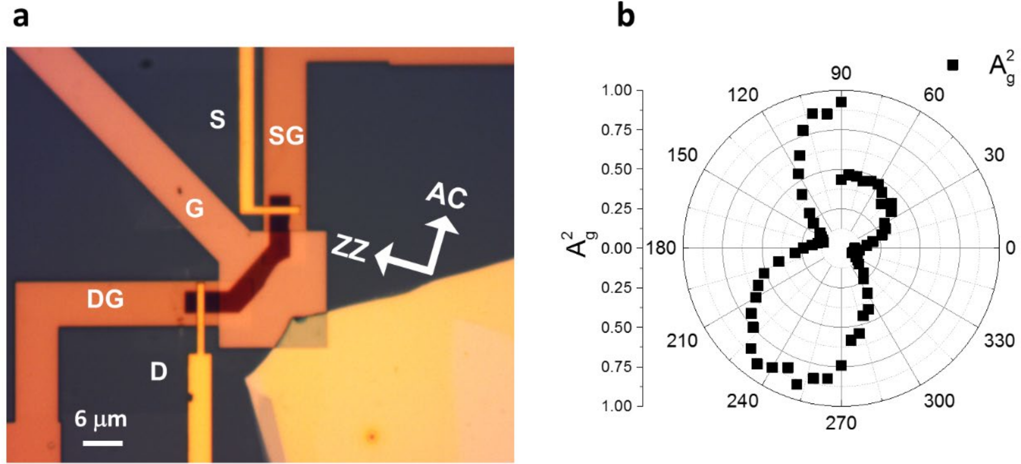


Figure 5.3 (a) Optical micrograph of completed L-shaped BP TFET with 12 nm BP. (b) Normalized A_g^2 vs. incident beam polarization. Total magnitude of peak decreased with number of measurements, perhaps because of BP degradation. The orientation dependent trends however are still clear.

mechanism is BTBT occurring at these orthogonal interfaces, the shape of the channel in-between those two interfaces has little to no influence on the device performance. Raman spectra were again used to retroactively verify the crystal orientation as described in Chapter 4, however this time the sample was fixed to the Raman stage and the polarization of the beam was rotated from 0º to 360º using a rotating half-wave plate. In this device, Raman spectra indicated that the AC and ZZ crystal axis were 18 degrees misaligned to the source and drain gates according to the polar plot in Figure 5.3(b). This is larger than the 9 degrees of misalignment observed in the isotropic AC and ZZ devices, however it is still suitable for making an asymmetric L-shaped BP-TFET and exploiting anisotropic tunneling current between the source and drain for improved device performance.

5.2 Electrical characterization of L-shaped BP-TFET

Devices were electrically characterized in a Lakeshore vacuum probe station at pressures ~ 10^{-5} Torr using Agilent 4156C parameter analyzer with 41501B expander unit enabling the use of a fifth SMU. In chapter 4, we observed that the current floor created by SRH generation at room temperature was ~ 10^{-9} A/μm. Because we are interested in how the ambipolar BTBT current limits I_{MIN} the L-shaped BP TFET was characterized at T = 77 K so that traps were frozen out and the device was operating in the pure BTBT regime.

Figure 5.4 shows the transfer characteristics of the L-shaped BP-TFET measured in the n-TFET and p-TFET configurations, where again the source and drain gate voltages are normalized to the threshold to ensure a symmetric doping profile as described for the previous device in chapter 4. Both devices were measured at $|V_{DS}|$ = 0.5 V and configured so that the source tunneling occurred in the AC direction and the drain tunneling occurred in the ZZ direction (as labelled in Figure 5.3(a)). The plot shows an asymmetric characteristic where the source tunneling current is higher than the drain tunneling current for both n and pTFETs (source tunneling is at positive V_{GS} for nTFETs and negative V_{GS} for pTFETs).

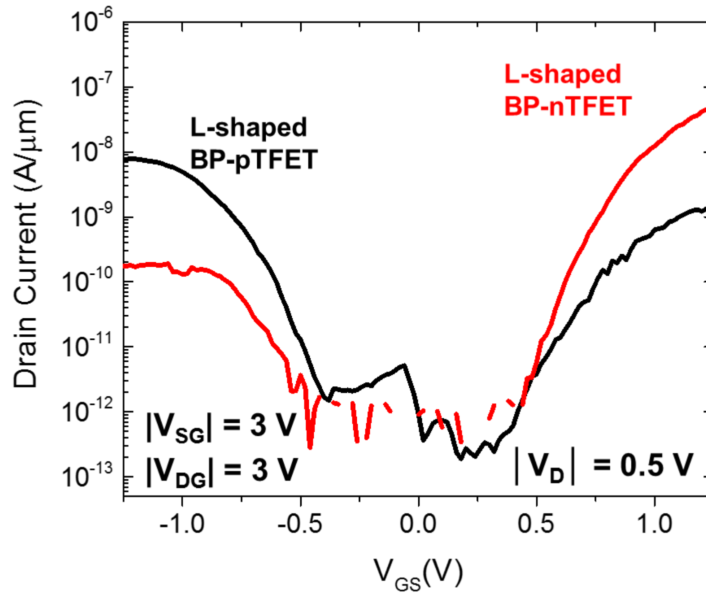


Figure 5.4 Transfer characteristics of L-shaped BP p and nTFETs showing asymmetry between source and drain tunneling.

This type of asymmetry between the source and the drain current is what is expected considering the source is aligned along the low mass AC direction and the drain is aligned along the heavy mass ZZ direction. The ON-current for the nTFET is higher than for the pTFET which could be the result of the threshold chosen from our threshold calibration I_D vs. V_{GS} curves being slightly lower than the actual gate voltage that corresponds to "intrinsic" BP. It is difficult to extract the precise intrinsic point due to the onset of tunneling current or the noise floor and the influence of V_{DS}. However, by comparing the two curves at $V_{GS} = +1$ V and $V_{GS} = -1$ V we can compare the tunneling current in the AC and ZZ direction at bias conditions of equivalent magnitude, that is, the voltages applied at the source-gate and the channel-gate in the nTFET is equivalent to the voltages applied between the drain-gate and the channel gate the pTFET and vis versa. This comparison reveals an anisotropy of ~10^2 between the AC and ZZ directions. This reveals the presence of asymmetry in the L-shaped BP-TFET however this anisotropy appears slightly lower

than what was measured for the isotropic TFETs in chapter 4. This could be due to the slightly larger crystal misalignment in the L-shaped BP TFET (18° vs. 9º) which may cause higher tunneling efficiency in the ZZ direction. After confirming the presence of source/drain asymmetry in the device, it's most interesting to characterize the improvement in the L-shaped BP TFET performance compared with the isotropic BP-TFETs shown in Chapter 4.

Figure 5.5 shows the transfer characteristics of the L-shaped BP n-TFET alongside the isotropic AC and ZZ BP nTFETs at V_{DS} = +1.5V described in Chapter 4. This plot shows the tremendous advantage of the anisotropic L-shaped BP TFET over the isotropic BP-TFETs. The L-shaped BP TFET has I_{ON} roughly equal to the AC BP TFET, however while I_{MIN} is limited to 1 nA/µm by ambipolar carrier injection in the AC BP-TFET, the current in the L-shaped BP decreases all the way down to 1 pA/µm which is roughly equivalent to I_{MIN} for the ZZ BP-TFET. With the L-shaped BP-TFETs we take advantage of the high tunneling efficiency in the low mass AC direction of BP and the lower tunneling

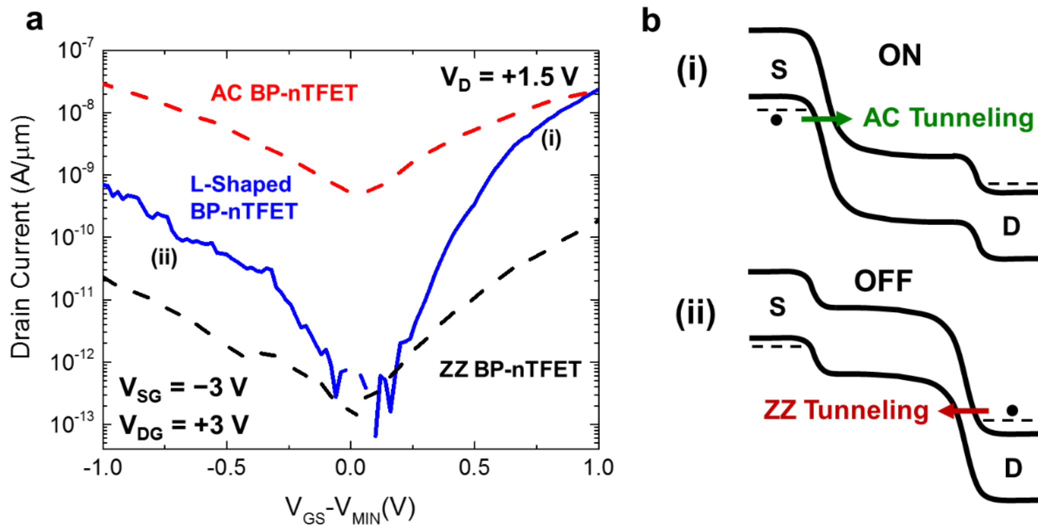


Figure 5.5 Transfer characteristic of the L-shaped BP n-FET alongside the isotropic AC and ZZ BP n-TFETs from Chapter 4. The band diagrams on the right show AC tunneling in ON-state (+ V_{GS}) and ZZ tunneling in the OFF-state (− V_{GS}).

efficiency in the large mass ZZ direction in order to realize TFETs with optimized I_{ON} and I_{OFF}. The device improvement is further characterized by plotting *SS* vs. I_D for the three TFETs and see that the L-shaped has a *SS* twice as steep as the ZZ BP-TFET and four times as steep as the AC BP-TFET. This is because ambipolar carrier injection also degrades *SS* primarily by preventing the device from reaching the true OFF-state (where tunneling at the source is turned off by tuning the channel potential). However, even while the current in the device is dominated by source tunneling, ambipolar carrier injection at the drain can

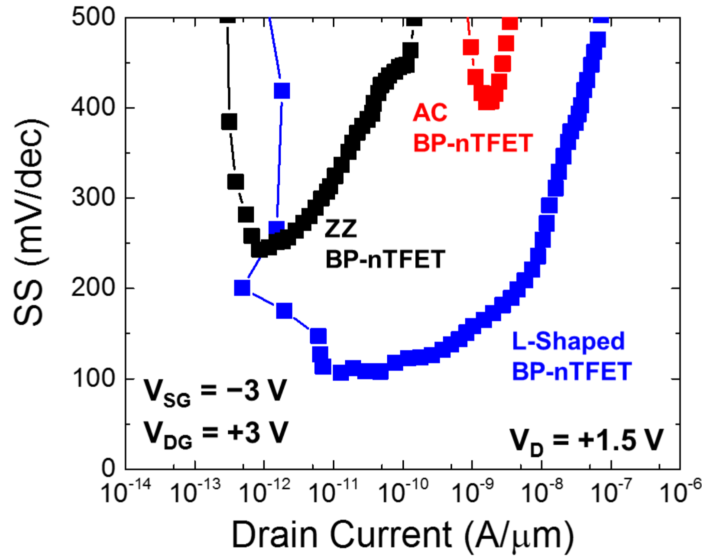


Figure 5.6 SS vs. I_D for the L-shaped BP TFET and isotropic AC and ZZ BP TFETs. L-shaped BP TFET shows improved SS at all current levels.

degrade the SS because the total current at a given gate voltage is equivalent to the electron tunneling at the source (I_n) plus the hole tunneling at the drain (I_h) and as I_n decreases because the tunneling window is closed at the source, I_h increases because the tunneling

window at the drain is widening (see band diagram in Figure 5.5). The L-shaped BP nTFETs are protected against this type of degradation because $|I_n| >> |I_p|$ at equal tunneling distances due to effective mass anisotropy. Table 5.1 shows a summary of key metrics for all three devices and displays that the L-shaped BP TFET is vastly superior in terms of subthreshold characteristics while maintaining the same I_{ON} as the AC BP nTFET. We do note that SS_{MIN} for the L-shaped BP TFET is ~ 107 mV/dec which is still relatively high compared to what would be desired for a TFET (< 60 mV), this is likely due to the same issues discussed in chapter 4. It is expected that this higher than expected *SS* is due to the relatively thick BP (~12 nm) which results in a larger scaling length and may conform less to the gate topography resulting in some gaps between the gate dielectric and the BP. This device was also exposed to air at times in the process which could mean there is a phosphorus oxide layer between the BP and the gate dielectric. The key thing is that none of these issues are fundamental and improved processes and device designs should result in steeper *SS* and higher I_{ON}.

Device	$\mathbf{I_{ON}}$	$\mathbf{I_{ON}/I_{OFF}}$	$\mathbf{SS_{MIN}}$ (mV/dec)
AC n-TFET	23 nA	43	406(@ $2x10^{-9}$A)
ZZ n-TFET	184 pA	$1.4x10^3$	240 (@ $9x10^{-13}$A)
L-shaped n-TFET	24 nA	$1.6x10^5$	107 (@ $2x10^{-11}$A)

Table 5.1 Relevant performance metrics for the L-shaped BP n-TFET, and the isotropic AC and ZZ n-TFETs at V_{DS} = 1.5. I_{ON} and I_{OFF} were taken to be the max and min current values in each device for the given sweep range in Figure 5.5.

5.3 Summary

In this chapter, the anisotropic effective mass of BP was utilizedto realize an L-shaped TFET with asymmetric source/drain tunneling, where the suppressed ambipolar current resulted in two orders of magnitude higher I_{ON}/I_{OFF} over isotropic BP TFETs, as well as over 50% lower SS_{MIN} than isotropic BP TFETs at V_{DS} = 1.5 V. While improvements must be made in order to achieve steeper SS and high I_{ON}. This type of device structure has the potential enable steep slope devices with high ON-state performance. This should drive further research on BP as a channel material for TFETs as well as motivate research on other anisotropic two-dimensional materials which could offer some of the same benefits as BP without some of its shortcomings like instability in air and difficult manufacturability.

CHAPTER 6 CONCLUSION AND OUTLOOK

In this dissertation I have presented my experimental work on engineering novel transistors utilizing the unique properties of black phosphorus to improve OFF-state or subthreshold performance while maintaining good ON-state performance in MOSFETs and TFETs. First, in chapter 2, I presented my work on heterostructure BP MOSFETs which utilize the thickness-tunable band gap of BP to suppress ambipolar carrier injection at the drain, improving OFF-state performance while maintaining good ON-state performance. This device was enabled by the development of a patternable, layer-by-layer thinning process which allowed the BP thickness to be tuned in the MOSFET source and drain regions. Next, in chapter 3, I presented my work on BP MOSFETs with electrostatically doped source and drain contacts. Electrostatically doped contacts enable band-edge like contacts which suppress ambipolar current injection at the drain and improved subthreshold performance is demonstrated. Electrostatic doping was enabled by the design and fabrication of a novel triple-gated device structure which allowed independent gate control in BP source, drain, and channel regions. In chapter 4, I used this electrostatic doping scheme to experimentally demonstrate BP TFETs for the first time resulting in *SS* close to the thermal limit at low temperature as well as the first observation of BTBT current anisotropy in BP. Finally, in chapter 5, I presented an L-shaped BP TFET which experimentally demonstrated the use of the anisotropic effective mass to suppress ambipolar drain tunneling in a BP TFET and improve I_{ON}/I_{OFF} and subthreshold slope compared with isotropic BP TFETs. This work demonstrates how the unique properties of

BP can be used to optimize performance in transistors by engineering novel structures and developing novel processes. It also sets the stage for future work on BP TFETs as well as work on other anisotropic 2D materials which could offer similar benefits as BP but potentially without some of the drawbacks such as instability in air and difficult manufacturability. Some future outlooks will be discussed in the following section.

6.1 Impact and Future Outlook

The primary motivation for this research was to solve the issues that Moore's law will face in the future and also work to reignite Dennard scaling (V_{DD} reduction in CMOS). This work has experimentally displayed the vast potential of black phosphorus in solving some of these key issues facing future CMOS scaling. Prior to this work, much of the promise of BP, especially in TFETs was based on theory. By experimentally demonstrating MOSFETs on sub-10 nm BP with reasonably good I_{ON} and demonstrating methods of improving the subthreshold performance to more acceptable levels using the unique properties of BP this work representations a significant step towards realizing high performance transistors with body thicknesses that would be acceptable for sub-5 nm gate lengths. This work also provides promise for the future of steep slope transistors which could enable the lowering of V_{DD} in CMOS circuits. This promise comes from the demonstration of BP TFETs which gives experimental validation to the many simulations performed on BP TFETs showing their potential superiority to TFETs based on other channel materials. This first step is important because the gap between theory and experiment is large and an experimental demonstration of working BP TFETs proves that these devices are feasible. In addition to this, the demonstration of the L-shaped BP TFET which uses the effective mass anisotropy of BP to improve subthreshold performance

provides experimental backing to the L-shaped BP TFETs simulated which show the ability to enable transistors with 2 nm gate lengths. Overall these demonstrations show that BP is uniquely capable for advanced transistors because its tunable band gap and anisotropic effective mass provides engineers with a way to optimize device performance in ways that other materials cannot and its scalability combined with good electrical properties and versatility (ability to make p and n-FETs) make it applicable for ultra-scaled CMOS devices.

However, in addition to the immense promise that was demonstrated through this work, great experimental challenges were also revealed. First and foremost, the lack of large scale, direct growth of thin film crystalline BP limits its current applicability to strictly research because current exfoliation techniques for transferring BP are not manufactural. Large area growth methods of ultra-thin BP must be realized in order transfer BP from the small lab into the fab. Some methods have been proposed with one being limited by small areas of growth [39] and one being limited in scalability because of the use of ultra-high pressures [40] but more work needs to be done to achieve a more manufacturable process. Another big challenge with black phosphorus which was discussed in this work is its degradation in air. Because of this degradation, the actual achieved performance of BP transistors is worse than predicted because the degradation results in lower mobility and also a high density of traps. These two things together result in poorer ON-state and OFF-state performance. To realize the ultimate potential of BP, devices must be fabricated in oxygen free environments or other techniques must be discovered to prevent degradation in black phosphorus. Going along with these issues is the issue that black phosphorus transistors have yet to be demonstrated with thicknesses of

one monolayer or less. The difficulty in BP growth and degradation of BP in air have made this feat hard to achieve. But in the future it will be of vast importance to fabricate devices using monolayer and bilayer BP because as stated previously, these thicknesses are where BP offers distinct advantages over bulk materials in MOSFETs and TFETs. Overall, the immense promise, is shadowed by these great challenges, however future engineers can and must innovate to solve problems like these and bring exotic materials to the industry.

From a more general perspective, this work has demonstrated a novel fabrication method and a novel device structure which could be of general use to the scientific community. The novel layer-by-layer thinning process based on cyclical oxidation could potentially be adapted to other material systems and present new ways to precisely control thicknesses of materials. The triple-gated device structure provides a novel way of locally controlling doping in thin materials which provides a method of achieving tunable potential profiles which can be useful for exploring novel devices as well as exotic physics. It also can conveniently be used with any transferrable material making it incredibly versatile.

In conclusion, this work demonstrates novel devices based on the unique 2D material black phosphorus. These device demonstrations represent a step towards using novel materials to solve the issues that Moore's law will face in the future and the structures utilized to realize these devices are useful tools for the scientific community.

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APPENDIX A

TERMINOLOGY

Symbol/Acronym	Quantity	Unit (SI)
CMOS	Complimentary-metal-oxide-semiconductor	N/A
BP	Black phosphorus	N/A
μ_{FE}	Field-effect-mobility	$cm^2/v{\cdot}s$
E_g	Band gap	eV
AC	Armchair crystal direction in BP	N/A
ZZ	Zigzag crystal direction in BP	N/A
m_{AC}	Effective mass in the armchair direction	unitless
m_{ZZ}	Effective mass in the zigzag direction	unitless
m_0	Mass of an electron (9.11×10^{-31})	Mass (kg)
FET	Field-effect-transistor	N/A
PDMS	poly-dimethylsiloxane	N/A
CVD	Chemical vapor deposition	N/A
λ	Transistor natural scaling length	Length (nm)
g_m	transconductance	Siemens (L)
I_{ON}/I_{OFF}	Transistor on-to-off current ratio	unitless
SS	Transistor subthreshold slope	mV/dec
GIDL	Gate-induced-drain-leakage	N/A
V_{MIN}	Gate voltage at minimum current value in a transistor	V
MOSFET	Metal-oxide-semiconductor-field-effect-transistor	N/A
V_{DD}	CMOS circuit supply voltage	V
TFET	Tunneling-field-effect-transistor	N/A
BTBT	Band-to-band-tunneling	N/A
I_{60}	Current at which SS = 60 mV/dec	A

E-beam lithography	Electron beam lithography	N/A
PMMA	Poly(methyl methacrylate)	N/A
ALD	Atomic-layer-deposition	N/A
D_{it}	Density of Interface Traps	N/A
TAT	Trap-assisted-tunneling	N/A
SRH	Schokley-Ried-Hall	N/A

APPENDIX B

SELECTED FABRICATION PROCESSES

This section will describe some of the finer details of selected fabrication processes, particularly those which utilized non-standard process steps that would be difficult to replication without the publication of the details of these steps.

B.1 Standard Electron Beam Lithography Recipe

Unless otherwise noted the standard E-beam lithography process used for the fabrication of all devices is as follows.

- Spin PMMA C4 at 3000 rpm for 60 seconds (EBEAM3000 recipe)
- Bake sample at 180° C for 8 minutes.
- Use lower current (1-10 nA) for small features (~ < 10 μm) and larger current (50 – 100 nA) for big features.
- Expose at dose between 1,200-1,600 μC/cm^2 (minimum dose has drifted over the years). Generally exposing larger features with a slightly higher dose (100 μC/cm^2 more) prevents underexposure.
- Develop in 3:1 IPA:MIBK for 90 seconds.

B.2 Standard HfO_2 Gate Dielectric ALD Deposition Recipe

Unless otherwise noted, the below recipe was used for all HfO_2 deposition used for gate dielectrics.

- Savannah Thermal ALD from Cambridge NanoTech
- Precursers: Tetrakis(dimethylamido)hafnium(IV) [TDMAH] and water vapor.

- Recipe: HfO_2_dep_oldversion at 300º C.

B.3 Standard Al_2O_3 BP Passivation ALD Deposition Recipe

Unless otherwise noted, the below recipe was used for all Al_2O_3 deposition used for BP passivation.

- Savannah Thermal ALD from Cambridge NanoTech
- Precursers: Trimethylaluminum [TMA] and water vapor.
- Recipe: Al203_dep at 200° C.

B.4 Patternable Thinning Process Details

Details pertaining to the patternable thinning process.

- Exfoliate BP onto SiO_2 substrate (other substrates could be used)
- Al_2O_3 mask process:
    - Standard E-beam lithography process to pattern PMMA
    - Evaporate 1.3 nm Al using E-beam evaporator
    - Expose sample to air (naturally happens throughout fabrication), Al oxidizes to form ~ 5 nm Al_2O_3.
    - Place sample in Acetone and immediately sonicate on lowest power and lowest frequency available for 5 minutes (prevents thin Al_2O_3 layer from sticking to the substrate).
    - Leave in Acetone at least 3 hours to complete liftoff.
- Perform thinning process (described in main text).
- Passivate with 20 nm ALD Al_2O_3.

B.5 Bi-layer Resist E-beam/Lift-off Process for Triple-gated Device Structure

To eliminate the need for a recessed gate process for the source and drain gates in the triple-gated device structure a bi-layer resist process was developed so that gate metals could be deposited with smooth edges providing reduced gate topography and reduced risk for gate leakage caused by rough metal edges.

- Spin Co-polymer, MMA-MAA (EL9), at 5,000 rpm for 60s (EBEAM5000) and bake at 180º C for 8 minutes. (Resulting film is ~ 250 nm).
- Spin PMMA A3 at 3,000 rpm for 60s (EBEAM3000) and bake at 150º C for 8 minutes. (Resulting film is ~ 150 nm) Note: PMMA concentration of may be slightly higher than 3% in anisole.
- Expose at dose between 900-1,400 $\mu C/cm^2$ (minimum dose has drifted over the years). Generally exposing larger features with a slightly higher dose (100 $\mu C/cm^2$ more) prevents underexposure.
- Evaporate gate metal (Ti/Pd) to desired thickness
- If gate metals are 25 nm thick or less, place sample in Acetone and immediately sonicate on lowest power and lowest frequency available for 5 minutes (prevents thin Ti/Pd layer from sticking to the substrate).
- Leave in Acetone at least 3 hours to complete liftoff.

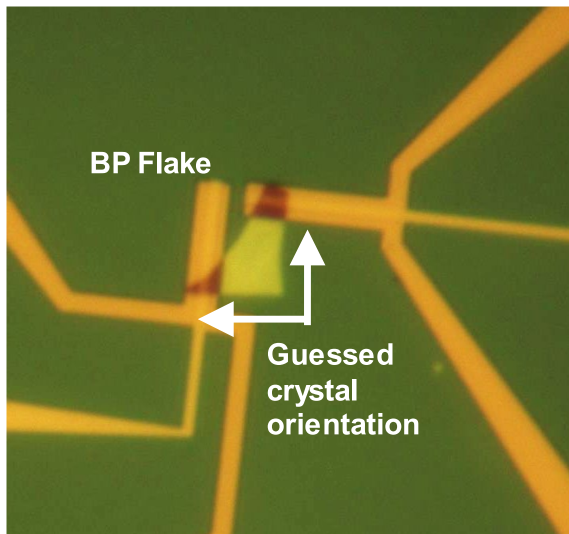
B.6 Gate Spacer Process for Triple-gated Device Structure

In attempt to increase the breakdown voltage of the triple-gated device structure, in particular, the breakdown voltage between the S/D-gates and the channel-gate, a process was developed so that a layer of Al_2O_3 was inserted between the S/D-gates and the channel-gate. The process is as follows.

- Deposition of S/D-gates and first HfO_2 gate dielectric layer (process from main text).
- Use Savannah ALD at 300° C to deposit 10 nm of Al_2O_3 (Al2O3_dep) on whole sample.
- Pattern and deposit channel-gate (process from main text)
- Etch Al_2O_3 from all areas not under channel gate:
  - 30s using 15% ammonium hydroxide in H_2O at 50º C. (etches at 25 nm/min)
- Proceed with final HfO_2 gate dielectric deposition.

B.7 BP Crystal Orientation Guess

For the crystal-oriented BP TFETs, the orientation of BP was guessed in order to transfer a BP flake so that its crystal axis were parallel to the two transport directions in the device(s). The following figure describes this process.



This figure shows how the natural right angle in the BP flake was used to guess the crystal orientation. It was expected that the BP would prefer to break along it's crystal axis and Raman measurements from the main text provided evidence that this was the case.

B.8 BP Mesa Etch

To fabricate the L-shaped BP TFET, the BP channel was patterned and etch to give it an L-shape so that BP would only be present above the gates. The process used is below.

- Standard E-beam lithography to define pattern (BP mesa pattern should be covered with PMMA and BP to be removed should be exposed).
- Ar plasma etch using the AV etcher:
    - Ar flow: 80 Sccm
    - Power: 80 Watts
    - Pressure 150 mTorr
- Etch 30 s to 60 s at a time and check under optical microscope after each etch cycle until BP is removed.
- Remove PMMA by placing sample in Acetone and immediately sonicate on lowest power and lowest frequency available for 5 minutes (prevents thin hardened PMMA layer from sticking to the substrate).
- Leave in Acetone for at least 3 hours to complete lift-off.