

**Modulation, Control and Performance Analysis of
Asymmetrical Modular Multilevel Converters (A-MMCs)**

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Dedication

To all those who believed and stood by me

Abstract

Modular multilevel converters (MMCs) are preferred converters for implementing high-power multilevel systems. The penalty they impose is the high number of devices needed to build them. To offset this challenge, this thesis introduces Asymmetrical Modular Multilevel Converters (A-MMCs). Unlike MMCs, each A-MMC module comprises of two half-bridge submodules, rated at asymmetric voltages. This system offers benefits like: (a) generation of four distinct voltage levels using one module; (b) 33% lesser semiconductor and gate drive requirement; (c) higher system efficiency; (d) reduction in overall cost and size. Hybrid Pulse-Width Modulation (Hybrid PWM) has been deployed to generate the drive pulses. To maintain asymmetric voltages, a novel voltage balancing algorithm has been proposed. Circulating current controller has been designed as well. The operation and performance validation was done using MATLAB Simulink and PLECS Blockset. A comparison, vis-à-vis the MMC, was also performed, based on thermal performance and essential circuit voltages and currents.

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Chapter 1

Introduction

1.1 Renewables and HVDC

The global demand for electricity will reach 30,000 TWh/year by 2030, as per the International Energy Agency [IEA], which is double of the world consumption during 2010 [1]. With this surge in energy demand, it has become imperative to integrate renewable energy sources in the electric grid, to cut down on the greenhouse gases' emission. Among the major renewable energy sources are solar and wind energy and their capacity addition is being done at an unprecedented rate. As per the U.S. Energy Information Administration (EIA), about 70 GW addition is projected in new solar photovoltaic and wind power capacity by 2021. Considering the federal support, these two renewable sources are projected to become the most competitive sources of new generation by 2022 [2]. The addition of this capacity also presents some unique challenges like:

- Long distance transmission from remote renewable generation sites leading to transmission losses
- Intermittency in generation leading to grid instability
- Overloading of the present transmission infrastructure

High Voltage DC (HVDC) Transmission is uniquely positioned to address these problems. Even for conventional long-distance transmission, HVDC is proving to be a

competitor to AC transmission [3]. It offers following advantages, to name a few:

- Reduced real estate, for similar capacity, due to smaller towers and less conductors
- Connectors between asynchronous AC systems, easing inter-country and intra-country transmission
- Reduced losses over longer distances providing for connection between distant geographies
- Better suited for undersea connections enabling bigger offshore wind farms

Hence the demand for HVDC technology [4, 5] has grown immensely; to serve the increasing penetration of renewable energy sources leading to reduction in dependence on fossil fuels [6]. Line-commutated current source and self-commutated voltage source converters (VSCs) are the two basic converter technologies used in HVDC systems [7]. As the semiconductor devices are breaking technology barriers and attaining even higher voltage and power ratings, the VSCs have become a preferred option for HVDC systems. In [8], a comprehensive analysis of various VSC technologies for HVDC systems has been done. In this landscape, modular multilevel converters (MMCs) [9] have become increasingly dominant. Their virtues like modularity, scalability, easy maintenance, non-requirement of large DC-link capacitors, near sinusoidal voltage synthesis (eliminates bulky grid filters), lower switching frequency requirement, etc. [10–14] have made them a preferred choice in HVDC conversion process.

1.2 HVDC Converter Technologies

Being modular in nature, the conventional MMCs widely discussed in literature use half-bridge modules as a building block. These modules, which are maintained at a constant voltage, are connected in series and switched so as to wave-shape the output voltage to the desired form. To impart DC fault current handling capability, the full-bridge or double star modules [15] and clamp double modules [16] have also been discussed, though they come with the penalty of additional component count. To reduce the overall system footprint, multi-level submodule configurations have also been investigated previously [17, 18]. In literature, asymmetric multilevel inverters are already known to achieve

higher number of levels in the output voltage with less number of converter modules. This leads to reduced overall converter size and cost. In [19], this idea was then extended to MMCs. This topology was called as the Asymmetric Modular Multilevel Converter (A-MMC).

1.3 Contribution of the thesis

MMCs have captured a significant share of the HVDC converter market [1]. But one of the cons of using this converter is the large number of semiconductor devices that need to be employed. In the A-MMC, each module has two half-bridge submodules rated at V_C and $2V_C$ voltages respectively. Hence, as will be explained later, it enables generation of more number of output voltage levels with the same number of devices as would be used in the MMC. Apart from offsetting the problem of high component count, this also leads to lower losses, in the conventional regions of operation, since lesser devices are involved.

In this thesis, a hybrid modulation technique is adapted to generate the four distinct voltage levels using one module of the A-MMC. To maintain the voltages of the V_C and $2V_C$ submodules at their rated values, a novel voltage balancing algorithm has also been proposed. As compared to the conventional voltage balancing technique, the proposed method leads to significantly reduced capacitor voltage ripple and successfully stabilizes the voltages at their intended asymmetric values. Like the conventional MMCs, even A-MMCs have circulating currents flowing through their arms. To suppress the dominant second harmonic component of these currents, a circulating current controller has also been implemented.

The simulations for the three-phase A-MMC system, having three modules per arm, were performed in MATLAB Simulink environment, using PLECS blockset. The configuration was designed to generate a maximum of nineteen output voltage levels. Detailed results and current/voltage waveforms have been shown to verify the operation of this new converter. These results were obtained at different conditions like, with/without voltage balancing and with/without circulating current control. This was followed by an exhaustive thermal loss, waveform quality, comparative structural analysis vis-à-vis the conventional MMC.

The thesis is organized in a total of six chapters. It is organized in the following manner -

- Chapter 1 provides the introduction
- Chapter 2 introduces the A-MMC topology and outlines the circuit description and operation
- Chapter 3 explains the proposed modulation and control of the A-MMC. Hybrid modulation technique, voltage balancing algorithm based on normalization of asymmetric voltages in an ASM, and circulating current control is described in this chapter
- Chapter 4 provides the simulation results for the A-MMC, using MATLAB Simulink and PLECS Blockset
- Chapter 5 contains the comparison of conventional MMC and A-MMC, presenting a strong case for further research and eventual adoption of the A-MMC
- Chapter 6 presents the conclusion and discussion of future research avenues

Chapter 2

Topology and Operation

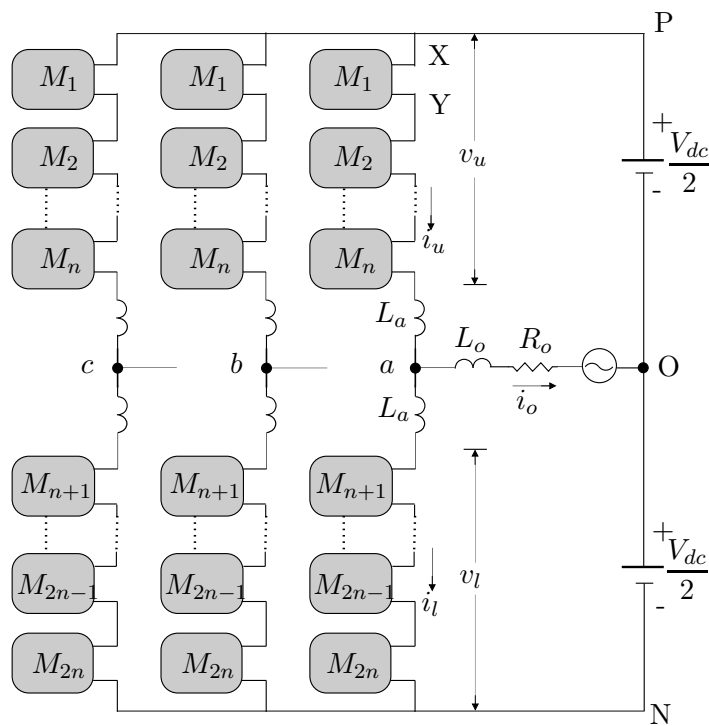


Figure 2.1: Asymmetric MMC topology

2.1 Topology description

The A-MMC has been conceptualized as an MMC which utilizes multi-level generating modules, comprising of asymmetric submodules. Fig. 2.1 depicts a three-phase configuration of the A-MMC. A-MMC has three phase legs in all, and each leg comprises of two arms - upper and lower arms. Each arm comprises of n series connected modules. The output is tapped from the mid-point of the leg and is synthesized by appropriate switching of upper and lower arm modules. Each phase p ($p = a, b, c$) leg also has arm inductors L_a . During the course of the thesis, it's assumed that these arm inductors have series resistance R_a .

The arm currents i_u and i_l flow through upper and lower arms, respectively. Due to instantaneous voltage difference between the arm and the DC-link, a circulating current component is also induced within the arm currents. These, as the name suggests, circulate within the arms and do not affect the output current dynamics. The arm inductors assist in circulating current suppression and also in DC fault current limiting. The modules can be 'inserted' or 'bypassed' based on their switching states. The total voltage obtained due to inserted modules is called the arm voltage, specifically v_u (upper arm) and v_l (lower arm) respectively in each leg. As given by (2.1), the difference of the arm voltages synthesizes the output voltage v_p (v_{aO} for phase a in Fig. 2.1) in that phase.

$$\begin{aligned} \frac{V_{dc}}{2} - v_p - v_u - v_{L_a} &= 0 \\ \frac{V_{dc}}{2} + v_p - v_l - v_{L_a} &= 0 \\ \Rightarrow v_p &= \frac{v_l - v_u}{2} \end{aligned} \tag{2.1}$$

2.2 Module construction

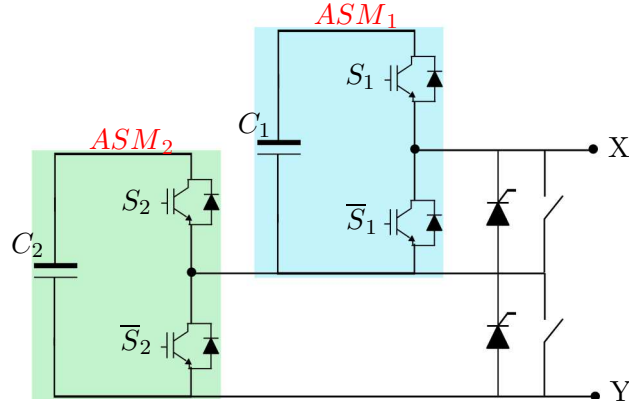


Figure 2.2: Internal structure of one module of A-MMC

Fig. 2.2 depicts the internal structure of a module of the A-MMC. As can be seen, it comprises of two ASMs, ASM_1 and ASM_2 . Their capacitors, C_1 and C_2 , are maintained at asymmetric voltages of V_C and $2V_C$ respectively. The driving state of the devices within ASM_1 and ASM_2 is given by S_1 (and \bar{S}_1) and S_2 (and \bar{S}_2). These switches are driven strictly in the complementary fashion, so as to avoid damage due to shorting out of the high energy capacitors connected across them. Each ASM is also appended with a thyristor, which handles the fault current for the half-bridge ASMs during a DC fault condition. The bypass switches are used to, as the name suggests, bypass the modules which can be useful in scenarios like routine maintenance, without needing to take the whole converter out of operation.

This configuration is unlike the conventional MMC, wherein each half-bridge module is symmetric, that is, they are all held at the same voltage.

2.3 Operation

By appropriate switching of the switches S_1 and S_2 , the output voltage of a module of an A-MMC can reach four voltage levels (0 , V_C , $2V_C$, $3V_C$) following the relationship shown by (2.2). The submodule capacitor voltage V_C can be related to the DC-link

voltage V_{dc} by (2.3).

$$\bar{v}_{XY} = S_1 \cdot V_C + S_2 \cdot 2V_C \quad (2.2)$$

$$n \cdot V_C + n \cdot 2V_C = V_{dc} \implies V_C = \frac{V_{dc}}{3n} \quad (2.3)$$

The Table 2.1 shows the different switching signal combinations and the related voltage level generation from an A-MMC module. The positive current direction is defined such that it charges the capacitors in its path whereas negative current discharges them. As can be seen, the proposed module configuration allows for generation of four distinct voltage levels: 0 , V_c , $2V_c$ and $3V_c$. This is an improvement over the conventional MMC which can generate only three levels with two modules. Fig. 2.3 shows the four distinct switching states, with positive current flowing in the arm.

The asymmetric module configuration can also be used in the full-bridge fashion so as to obtain DC fault current handling capability.

Table 2.1: Truth table: States of operation

S_1	S_2	\vec{i}	v_{C1}	v_{C2}	\bar{v}_{XY}
0	0	≥ 0	=	=	0
		< 0			
1	0	≥ 0	\uparrow	=	V_C
		< 0	\downarrow		
0	1	≥ 0	=	\uparrow	$2V_C$
		< 0		\downarrow	
1	1	≥ 0	\uparrow	\uparrow	$3V_C$
		< 0	\downarrow	\downarrow	

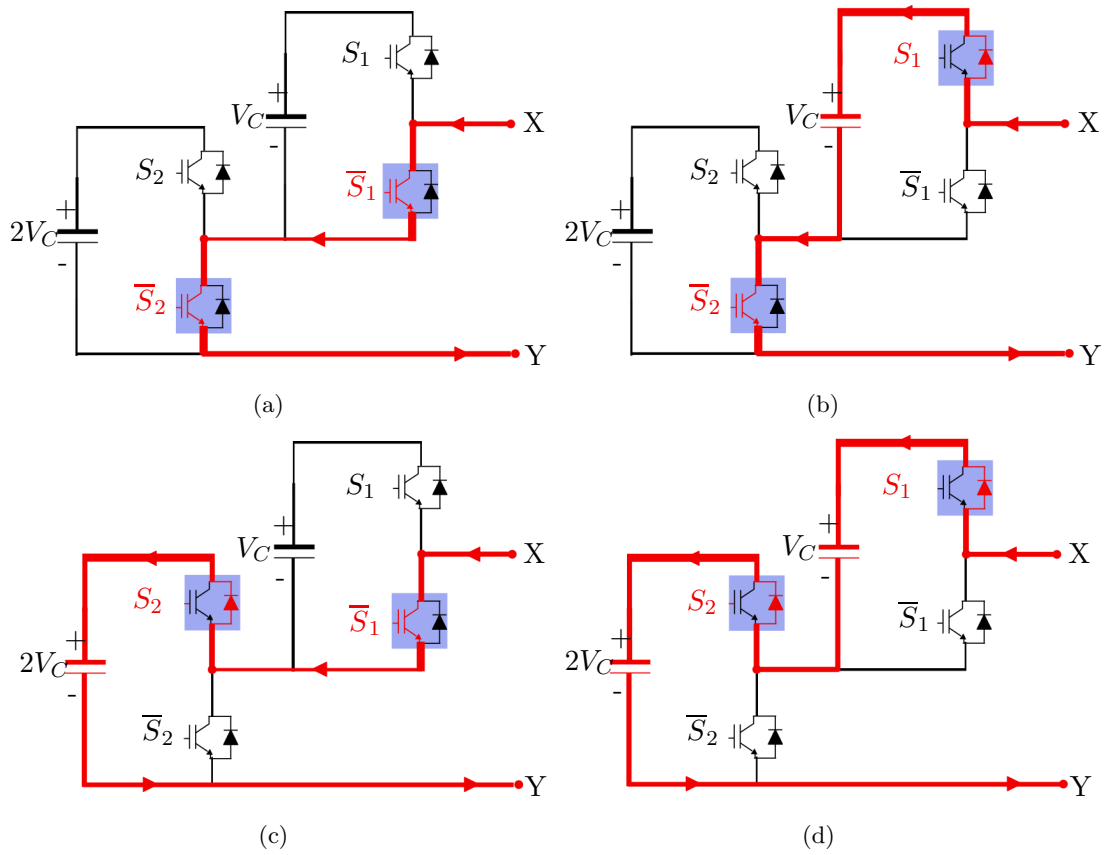


Figure 2.3: States of operation: (a) Bypass state, (b) Level V_C state, (c) Level 2V_C state, (d) Level 3V_C state

Chapter 3

Modulation, Voltage Balancing and Control

The modulation block is responsible for generating ideal drive pulses to drive the switching devices. These pulses, though associated with individual modules, are then supplied to the voltage balancing block, which determines which module is to be inserted/removed. To suppress the circulating currents within the converter arms, a circulating current suppression controller has also been incorporated. This chapter describes the operation of these three blocks in reference to the A-MMC model under study.

3.1 Modulation

The modulation block is responsible for generating the drive pulses at discrete intervals. In conjunction with the reference signals, the modulation block is responsible for wave shaping of the output voltage. Various carrier-based modulation techniques have been described in [20]. These include, level-shifted PWM (LS-PWM), phase-shifted PWM (PS-PWM) and their variations.

3.1.1 Phase Shifted PWM

In context of an MMC with n modules in every arm, PS-PWM consists of n phase-shifted carriers. These carriers are phase-shifted with respect to each other in the time domain, as shown in Fig. 3.1(a). The phase shift is uniform and for carriers corresponding to modules in one arm, it is given by (3.1)

$$\theta = \frac{2\pi}{n} \quad (3.1)$$

PS-PWM offers the advantage of uniform distribution of power across the modules. This aids in voltage balancing. Also, filtering requirements, of an output derived from a PS-PWM driven converter, are lesser since the location of the dominant harmonic, of output voltage, is at n times the switching frequency [21].

3.1.2 Level Shifted PWM

LS-PWM comprises of n carriers, each level (magnitude) shifted with respect to the adjacent carrier and all stacked one above the other, as shown in Fig. 3.1(b). The dominant harmonic in the output voltage is at lower value, than PS-PWM being run at same frequency, and hence filtering requirements are increased. But it offers lower power losses across the devices, chiefly because the effective switching frequency is reduced.

When PS-PWM and LS-PWM are used with MMCs, each carrier is associated with one module in each arm and hence it can be observed that in Figs. 3.1(a) and 3.1(b), modulation signals for nine modules, per arm, are being generated.

3.1.3 Hybrid PWM

Unlike the MMC, within each module of the A-MMC, there is voltage asymmetry since there are two submodules, one at V_C Volts and other at $2V_C$. Hence, each module of the A-MMC can generate four levels in all. PS-PWM or LS-PWM cannot be used directly to generate these voltage levels since carrier-device association assumes symmetry in device voltages. Instead, a hybrid technique is used in [18], called the Hybrid PWM. As can be seen from Fig. 3.1(c), the carriers here comprise of both level and phase-shifted type.

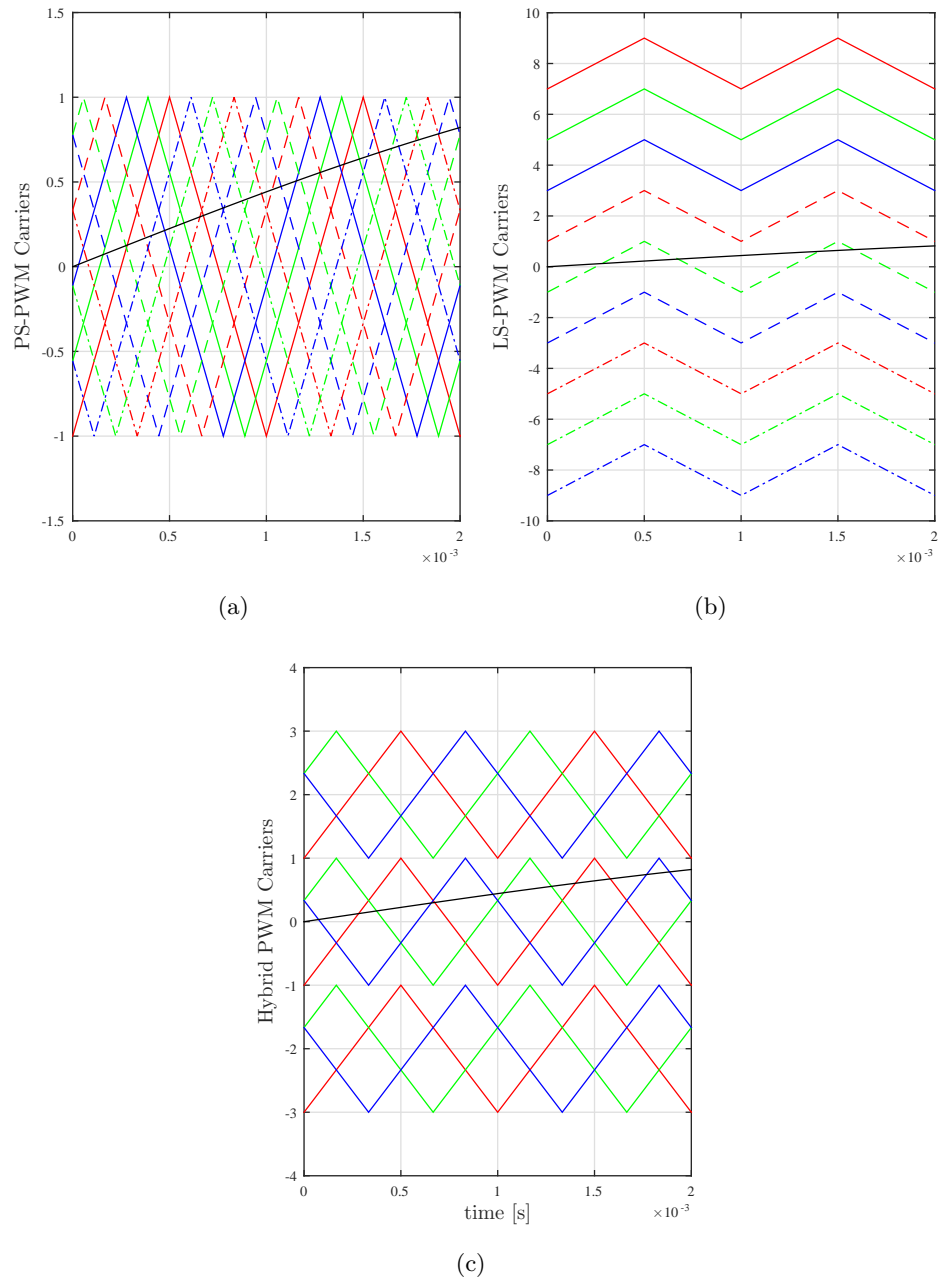


Figure 3.1: (a) PS-PWM carriers; (b) LS-PWM carriers; (c) Hybrid PWM carriers

In Hybrid PWM, in context of a single A-MMC module, three level shifted carriers are first stacked on top of one another and made into a group. To generate four levels

from this single module of the A-MMC, the three triangular carriers come into play. Hence, for n such modules in an arm of the A-MMC, n such groups of three level shifted carriers are used. That is, each module is dedicated one group of level-shifted carriers. These groups are then phase-shifted among themselves by $\frac{2\pi}{n}$. There are two such collections of carriers, one for the upper arms and other for lower arms. Fig. 3.1(c) depicts the Hybrid PWM carriers of an arm of an A-MMC. As evident, there are three groups of level-shifted carriers indicating that this is driving 3 modules per arm.

3.1.4 Carrier Interleaving

Corresponding groups in both these collections, one each dedicated to lower and upper arm respectively, can be phase-shifted relative to each other. The value of this phase shift determines the number of output voltage levels. The introduction of this phase shift is called carrier interleaving. Carrier interleaving is also performed in modulation of conventional MMCs, to obtain higher number of levels. Consider an MMC with n modules. Then the maximum number of output voltage levels can range from $n + 1$ to $2n + 1$ [21] [22]. Hybrid PWM can also be deployed with similar carrier interleaving, with the A-MMC, to generate $3n + 1$ to $6n + 1$ output voltage levels. Let the displacement angle, or phase shift between corresponding upper and lower arm carrier groups, be θ . Then $6n + 1$ levels can be obtained from the A-MMC using (3.2).

$$\theta = \begin{cases} 0, & \text{for odd } n \\ \frac{\pi}{n}, & \text{for even } n \end{cases} \quad (3.2)$$

Thus the A-MMC can generate same number of output voltage levels as the MMC, using one-third the number of modules (or two-thirds the number of switching devices).

3.1.5 Operation of A-MMC with Hybrid PWM

An A-MMC using two modules in each arm was constructed and then driven using Hybrid PWM, as shown in Fig. 3.2. In all, there are four groups of stacked carriers. For each phase p ($p = a, b, c$) of the A-MMC, two normalized sinusoidal reference signals v_u^* (upper arm) and v_l^* (lower arm) are compared with these hybrid triangular carriers to synthesize the output voltage. Four pulses are then generated, corresponding to each

ASM in the entire phase-leg. These pulses are then passed through the digital decoder logic, to generate individual pulses for the submodules within these ASMs. Subsequent plots in Fig. 3.2 show the Hybrid PWM generation and module, arm and output voltages. As can be observed, thirteen levels in all have been generated using only two modules by employing appropriate carrier interleaving condition, using (3.2).

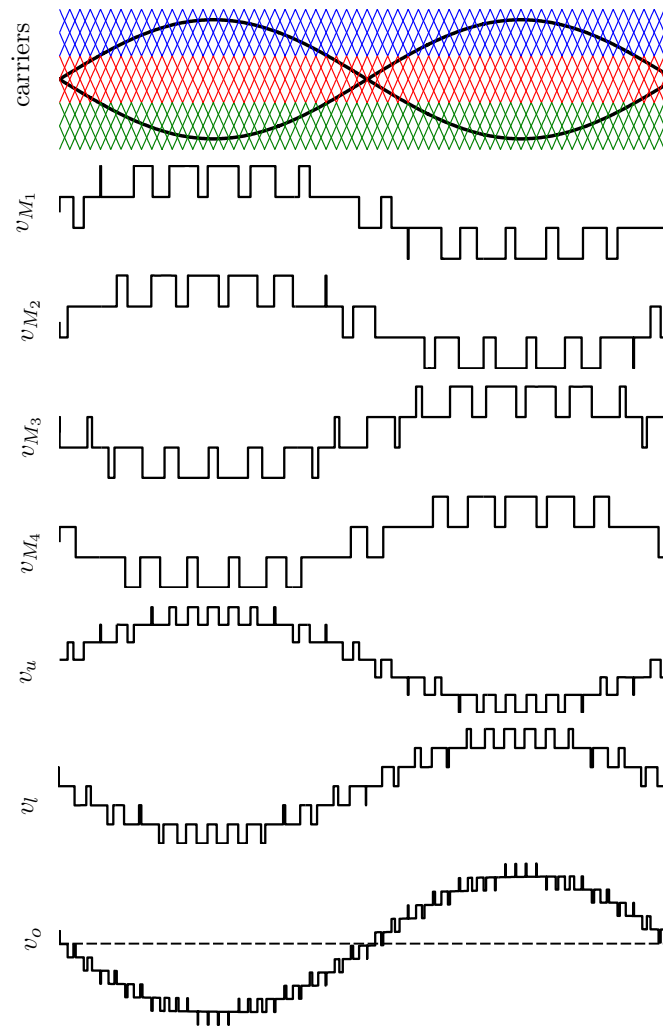


Figure 3.2: Hybrid PWM: Generation of pulses and output voltage

3.2 Capacitor Voltage Balancing

From the switching signals generated using the modulation block, assignment to the appropriate submodule is done in the voltage balancing block as discussed in this section. Due to the presence of asymmetric submodules ASM_1 and ASM_2 , the control algorithm needs to ensure balanced voltages of V_C and $2V_C$ for proper operation of the A-MMC, else the output voltage gets distorted

3.2.1 Conventional voltage balancing technique

The conventional voltage balancing technique [23] is depicted in Fig. 3.3. It relies on the direction of arm current to determine which module to insert/remove. The crux is that depending on the current direction, the module which needs to obtain or dump the most energy, gets preference.

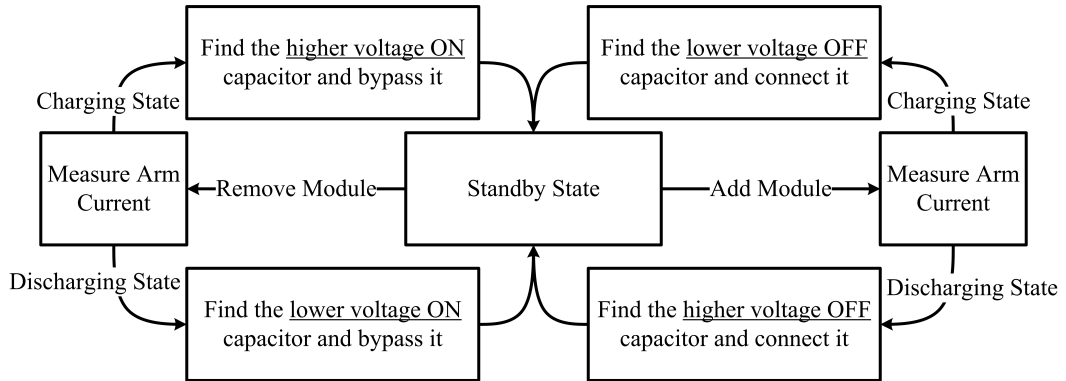


Figure 3.3: Conventional voltage balancing algorithm

3.2.2 Design for new voltage balancing technique

The genesis of the proposed voltage balancing technique lies in the following fundamental observations:

- The modulation technique asks for a voltage insertion/removal only in steps of one voltage level

- Since the ASMs are of two asymmetric voltages, decision of which submodule to insert/remove needs to factor this asymmetry
- Adopting from the conventional technique, the submodule most removed from its rated energy level should get preference to be acted upon
- The voltage asymmetry, unlike the conventional MMC, provides for two different ways of voltage level synthesis, as will be explained later

Expounding on the first observation, at every switching instance, the modulation scheme requires only one voltage level, either to be added or subtracted from the output voltage by PWM operation. This ensures smoothness of the output voltage. If the total number of inserted capacitors is appropriate, the output voltage is synthesized correctly, irrespective of which capacitor is inserted. Hence, in case of conventional MMC with symmetric modules, the voltage balancing algorithm inserts/removes the least or highest voltage module depending on the arm current direction [23]. However, in case of A-MMC, there are two sets of submodules (ASM_1 and ASM_2) in each module which have unequal capacitor voltages. The conventional voltage balancing algorithm, if applied as is to the A-MMC, will distort the output voltage waveform because of asymmetric voltages.

Hence, as drawn from the second observation, the ASM_1 and ASM_2 capacitor voltages need to be normalized so as to compare them on an equal pedestal. This idea of voltage normalization forms the crux of the proposed voltage balancing method. This normalization is done using (3.3), where V_C and $2V_C$ are the intended voltage values.

$$\begin{aligned} v'_{C1} &= v_{C1}/V_C \\ v'_{C2} &= v_{C2}/2V_C \end{aligned} \tag{3.3}$$

Once the normalized values are computed, the decision of which submodule to insert/remove then depends on the direction of current flow. As shown in Table 2.1, a positive current direction charges the capacitor whereas, the current in the opposite direction discharges it. Using the knowledge of current direction then, the capacitor which is farthest from the normalized rated value is selected. Note that the modulation

will demand only one level to be inserted/removed at a time. Thus, as a case, addition of a voltage level in an arm can be done in one of the following two ways:

- Insert any OFF ASM_1 OR
- Bypass any ON ASM_1 and insert any OFF ASM_2

Hence, once the appropriate submodule is selected then it is to be ensured that if the logic flow selects a $2V_C$ capacitor to be inserted/removed, another $1V_C$ capacitor has to be removed/inserted. The selection of this ASM_1 is done on the same basis, that is, which ASM_1 's energy level is most removed from the rated values.

3.2.3 Proposed voltage balancing algorithm

Fig. 3.4 shows the proposed voltage balancing method. Note that there are six such voltage balancing blocks, each working in isolation with one of the six arms of the converter.

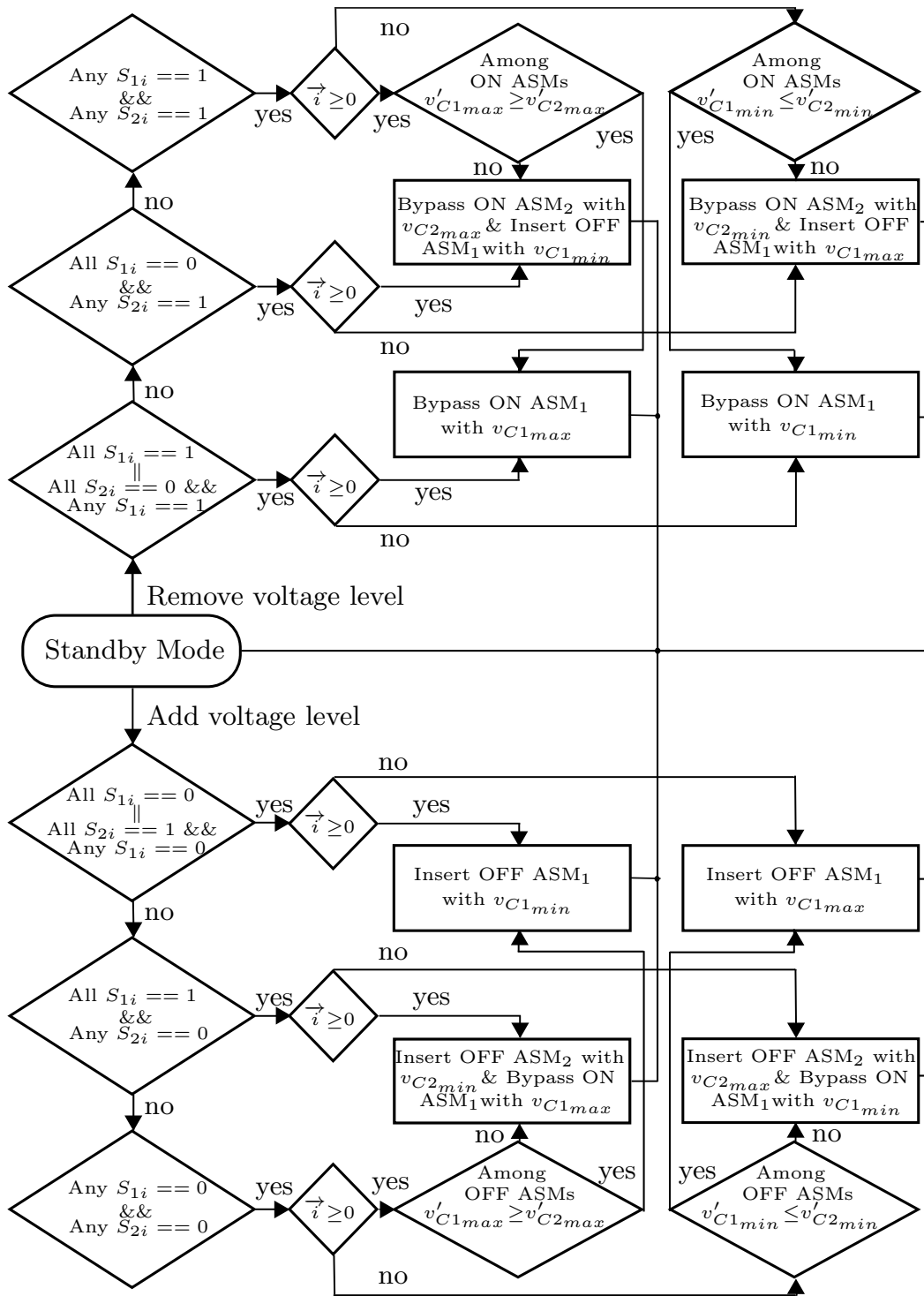


Figure 3.4: Voltage balancing algorithm

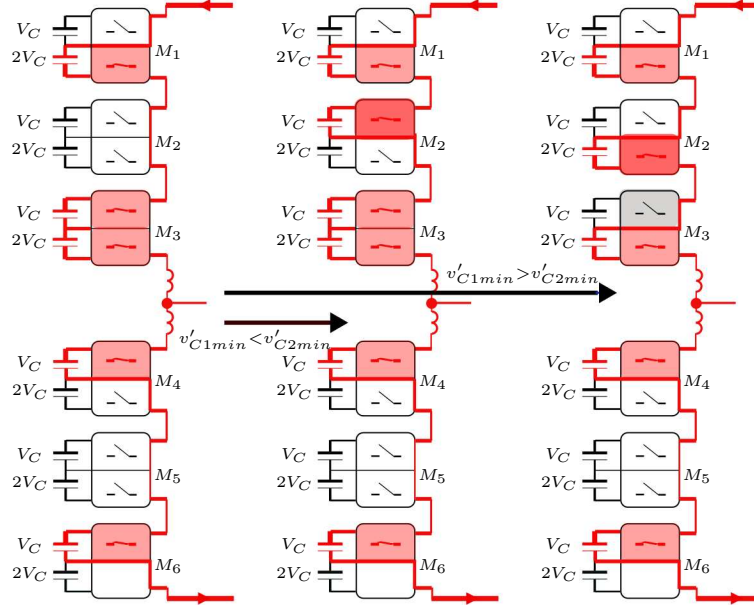


Figure 3.5: Voltage balancing example case for inserting a voltage level

To illustrate this, consider a case when the modulation requires an output voltage to be changed from $-1.5V_C$ to $-2.0V_C$, as seen in Fig. 3.5. Hence, a V_C voltage level needs to be inserted in the upper arm, as deduced from (2.1). Fig. 3.5(left) shows the initial condition of the A-MMC leg. As can be seen, two ASM_1 and one ASM_2 module are bypassed in the upper arm. Looking at the positive current direction then, the algorithm will determine the bypassed ASM capacitor which has least normalized voltage value. Consider the condition 1 from Table 3.1. Note that $v'_{C_{x,i}}$ stands for the normalized voltage of ASM_x 's capacitor in the M_i module. Since $v'_{C_{1,2}}$ has least value, the ASM_1 of M_2 will be inserted, as shown in Fig. 3.5(middle). Whereas, if the condition 2 existed, then $v'_{C_{2,2}}$ being the least, ASM_2 of M_2 will be inserted. Since ASM_1 of M_3 has the highest voltage among inserted ASM_1 , it will be removed, as shown in Fig. 3.5 (right).

Table 3.1: Capacitor voltages, of Fig. 3.5, in ascending order

Upper Arm v'_{C1} and v'_{C2} (Ascending Order)	
Condition 1	Condition 2
$v'_{C1,3}$	$v'_{C2,2}$
$v'_{C1,2}$	$v'_{C2,1}$
$v'_{C2,3}$	$v'_{C2,3}$
$v'_{C1,1}$	$v'_{C1,1}$
$v'_{C2,2}$	$v'_{C1,3}$
$v'_{C2,1}$	$v'_{C1,2}$

Similarly, as per the proposed balancing algorithm, if the current direction is such that it will discharge the capacitors then, for all the OFF submodules:

- $v'_{C1_{max}} \geq v'_{C2_{max}} \Rightarrow$ Insert ASM_1 with $v_{C1_{max}}$
- $v'_{C1_{max}} < v'_{C2_{max}} \Rightarrow$ Insert ASM_2 with $v_{C2_{max}}$ and bypass ON ASM_1 with $v_{C1_{min}}$

Similar decision making is done in the case of submodule removals, as per Fig. 3.4. This technique also accounts for the border cases, where enough V_C or $2V_C$ submodules may not be available for choosing among multiple options.

3.3 Circulating Current Control

3.3.1 Circulating Current Definitions

The floating capacitors in MMC possess voltage ripple which causes the arm voltages to not sum up to be exactly equal to the DC bus voltage. This voltage imbalance induces circulating currents to flow in the arms between the individual phase units [24]. The circulating currents do not affect the dynamics of converter output currents. They comprise of a dominant second harmonic component which distorts the shape of arm currents i_u and i_l . For phase p ($p = a, b, c$), the arm currents (i_u and i_l), phase current i_p and phase difference current i_{pz} are as given in (3.4).

$$\begin{aligned}
i_u &= \frac{I_{dc}}{3} + i_{circ} + \frac{i_o}{2} \\
i_u &= \frac{I_{dc}}{3} + i_{circ} - \frac{i_o}{2} \\
i_p &= i_u - i_l \\
i_{pz} &= 0.5(i_u + i_l) = \frac{I_{dc}}{3} + i_{circ}
\end{aligned} \tag{3.4}$$

The DC component of the phase difference current is responsible for power transfer between DC link and AC output. The additional component i_{circ} results in higher losses.

3.3.2 Circulating Current Control Technique

Various circulating current control algorithms have been proposed in literature for the conventional half-bridge module based MMC [12, 25, 26]. In [27], the arms of the MMC have been treated as controllable continuous voltage sources to derive the circuit model. This is based on the assumption that the number of modules is infinite. This is a good approximation for the MMC which is usually used in applications where number of modules is indeed high. Using this model, a sinusoidal component, at double the fundamental frequency, in the arm voltages was derived in [28]. This component is chiefly responsible for the circulating current. Assuming that other higher frequency circulating current components are insignificant, a second harmonic suppression controller was devised in [23]. The transfer function relating inner unbalance voltage v_{pz} , given by (3.5), to circulating currents was used for the same. It was derived using negative sequence rotational reference frame transformation, for easier controller implementation.

$$v_{pz} = L_a \frac{di_{pz}}{dt} + R_a i_{pz} = \frac{1}{2} (V_{dc} - v_u - v_l) \tag{3.5}$$

The assumption of the converter arm as a controllable voltage source holds true for the A-MMC as well, especially if the number of modules is assumed to be high. Hence, a circulating current controller similar to [23] was used in the A-MMC. By shaping v_z (3.5), applied across arm inductor L_a and arm resistor R_a , differences in voltage between DC bus and the phase leg were minimized, which suppresses the circulating current generation. This led to improved efficiency and system stability.

3.4 Overall System

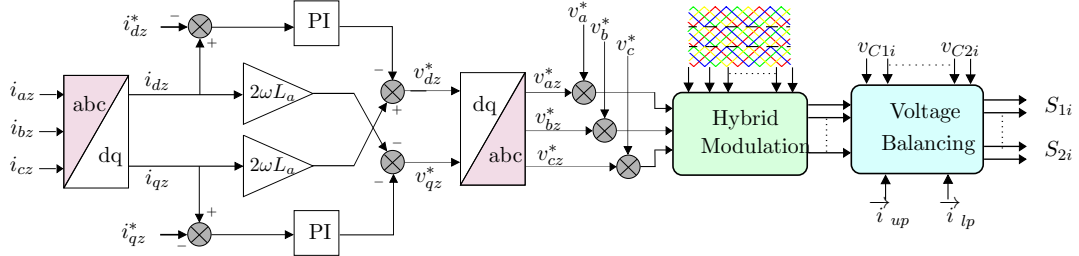


Figure 3.6: A-MMC control blocks

The high level system control block diagram is as shown in Fig. 3.6. In the constructed three-phase A-MMC model, the phase difference currents i_{az} , i_{bz} and i_{cz} are converted into the rotating dq frame to result in DC quantities. A simple PI based controller is then designed to suppress the second harmonic circulating currents, by setting the reference to zero. Feed-forward components, at double the line frequency, are added/subtracted to generate the reference voltage components. The actual reference used for modulation is a sum of the normalized sinusoidal reference (for power transfer) and the component for circulating current suppression ($= v_p^* + v_{pz}^*$). This reference drives the Hybrid PWM block which generates the drive pulses. These are then supplied to the voltage balancing block which selects the appropriate submodules to assign the drive pulses to.

Chapter 4

Simulation Results

4.1 Simulation Parameters

A model of the three-phase A-MMC was built and tested in the MATLAB Simulink environment, along with PLECS Blockset. PLECS was used since it provides for thermal circuits and calculations. They were then used to evaluate the loss figures for comparison between the MMC and A-MMC, which is presented in next chapter. This chapter presents detailed simulation results for the A-MMC. The motive here is to verify the operation of the overall system and the significance of individual control blocks, like voltage balancing and circulating current controller. The essential parameters of the circuit during these simulations were as listed in Table 4.1.

The DC bus was simulated using a stiff DC voltage source of 9 kV. From that, the targeted value of capacitor voltages was evaluated to be 1 kV and 2 kV, for ASM_1 and ASM_2 respectively. The A-MMC contained three modules per arm and was driven with Hybrid PWM. The interleaving of the carriers was such that nineteen levels were produced in the output voltage waveform, at rated modulation index.

Table 4.1: Simulation Parameters

Parameters	MMC	A-MMC
Number of modules/phase	18	6
Modulation technique	Phase-shifted PWM	Hybrid PWM
Modulation index	0.85	0.85
DC bus voltage V_{dc}	9 kV	9 kV
Submodule C_1 capacitor	10 mF	5.66 mF
Submodule C_2 capacitor	-	8.33 mF
Arm inductor L_a	1 mH	1 mH
Arm resistor R_a	0.1 Ω	0.1 Ω
Output frequency	60 Hz	60 Hz
Output power P_o	9.3 MW	9.3 MW
Power factor	0.8	0.8
Switching frequency (f_s)	1 kHz	1 kHz

4.2 Operation at balanced conditions

The output voltage v_o and current i_o are depicted in Fig. 4.1. As was mentioned earlier, the output voltage contains nineteen levels. As can be clearly seen, it's a clean multilevel output which reduces filtering requirements and also uses devices of lower ratings. The i_o has been shown as well and it can be observed that load inductance is enough to filter and obtain a clean sine-wave current. For this simulation, the voltage balancing and circulating current control blocks were enabled right from the start and the ASM capacitors were pre-charged at their intended values. This verifies the operation of MMCs with asymmetric modules.

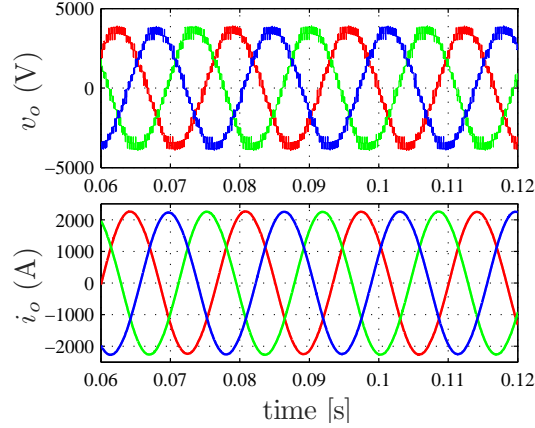
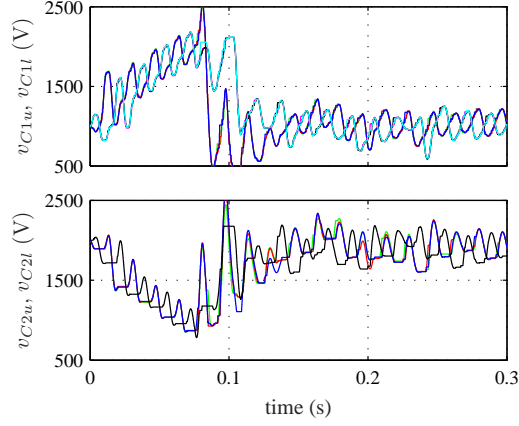


Figure 4.1: (top to bottom) Synthesized three-phase converter output phase voltages v_o , three-phase line currents i_o

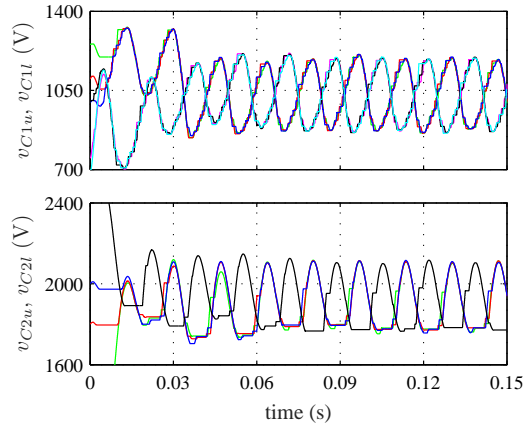
4.3 Verification of proposed voltage balancing technique

The voltage balancing algorithm should be able to maintain the ASMs at their commanded voltage. To verify whether it can do this, two special-case simulations were performed, as illustrated in Figs. 4.2(a) and 4.2(b). In the first simulation, voltage balancing was enabled only at 75 ms and the capacitors were pre-charged with their intended voltages. Before 75 ms, the converter was being driven by the Hybrid PWM pulses, associated with each module, directly. As can be seen, the ASM_2 capacitors are continually discharging whereas the voltage of ASM_1 capacitors keeps rising. These measurements were done for ASMs in the center leg. Note that, this is unlike the MMC, where the voltage balancing block is not necessary (though almost always used) since modulation can alone keep the capacitor voltages around their targeted values due to the symmetry. This emphasizes the importance of this balancing technique, without which the asymmetry of A-MMC cannot be exploited.

In Fig. 4.2(b), effect of balancing with capacitors pre-charged at different values is shown. The proposed voltage balancing technique, which was enabled right from the start, performs well and pulls the capacitor voltages to their intended values and stabilizes them in short time. These results verify the operation of the proposed voltage balancing technique.



(a)



(b)

Figure 4.2: (a) Capacitor voltages in upper and lower arms with balancing activated at $t = 75$ ms (b) Capacitor voltages in upper and lower arms with different precharged voltages

4.4 Comparison of conventional and proposed voltage balancing technique

The performance of the conventional and proposed balancing technique is compared in this section. In conventional technique, the decision of module insertion/removal is taken on the basis of current direction [23]. For example, if the current is flowing such that it charges the inserted capacitors, then capacitors with least/highest

voltage are inserted/removed, as asked by the balancing block. All capacitors are assumed to be identical and no asymmetry is accounted for. This conventional technique was extended to test with the A-MMC. Similar decisions were taken, with the minor tweak being that the normalized values of $2V_C$ and V_C capacitor voltages were used to determine the highest/least voltage capacitors. No ASM_1 insertion/removal was performed, as is demanded by the proposed balancing technique, whenever any ASM_2 was removed/inserted.

As can be seen in Fig. 4.4(a), v_o is severely distorted. The capacitor voltages, though hovering around their intended values, have significant ripple which is the cause of the output distortions. As opposed to this, in Fig. 4.4(b), we see that with the proposed technique, v_o and i_o waveforms are as desired. The capacitor voltage ripple is greatly reduced. This also aids in the harmonic reduction in both output current and voltage, as depicted by the FFTs in Fig. 4.3.

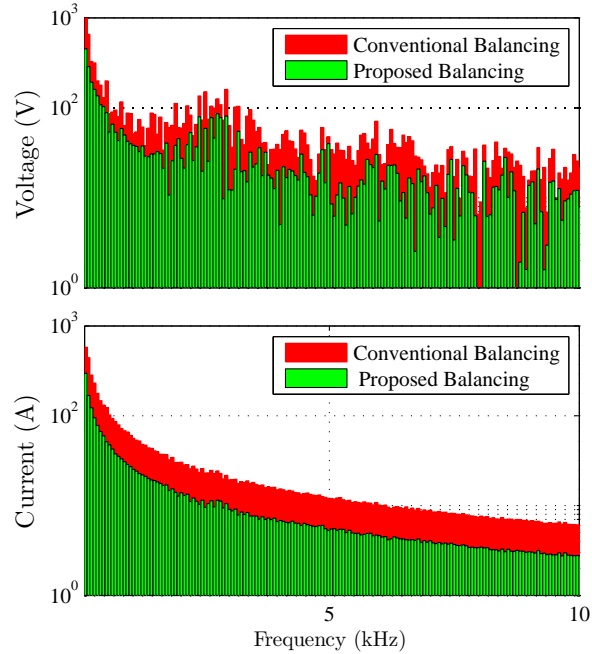
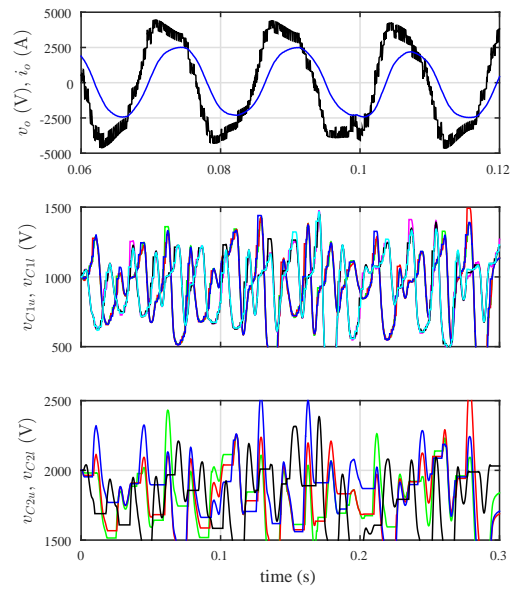
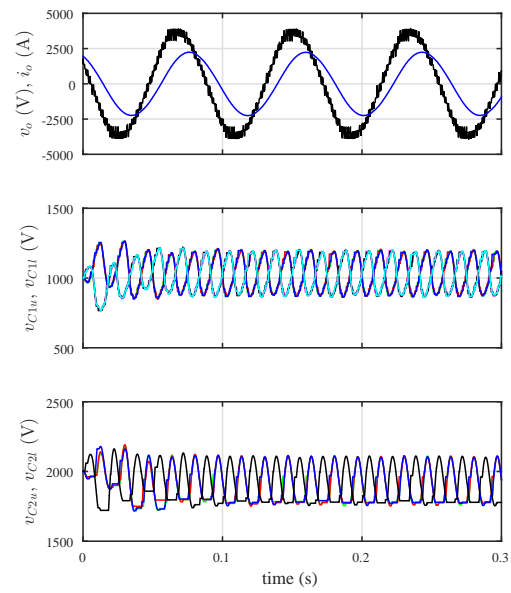


Figure 4.3: FFT analysis of output voltage and current using conventional voltage balancing and proposed voltage balancing



(a)



(b)

Figure 4.4: (top to bottom) Output voltage and current, capacitor voltages of ASM_1 and ASM_2 for (a) conventional voltage balancing; (b) proposed voltage balancing

4.5 Verification of circulating current controller

The upper and lower arm currents, i_u and i_l respectively, and output current i_a (all for phase a) are depicted in Fig. 4.6(a) (top). The arm currents have a significant dominance of the second harmonic component. This is verified from Fig. 4.6(b) (middle), which shows the phase difference current i_{az} . The DC component of i_{az} is responsible for power transfer between the DC link and AC grid. Whereas the sinusoidal ripple, which is a sine wave of second harmonic frequency (120 Hz in our case), is the circulating current. For this simulation (Fig. 4.6(a)), the circulating current control was disabled throughout.

In the second simulation (Fig. 4.6(b)), the A-MMC was simulated with the circulating current controller enabled. The arm currents, in Fig. 4.6(b) (top), show very significant second harmonic suppression. The i_{az} in Fig. 4.6(a) (middle) has a much more dominant DC component now. On contrasting the capacitor voltage ripples in Figs. 4.6(a) (bottom) and 4.6(b) (bottom), we see that even they have significantly reduced now. This is expected since this ripple is also responsible for the voltage imbalance between the arms, which gives rise to the circulating currents in the first place. The second harmonic reduction is also attested by the FFT analysis of i_{az} , as shown in Fig. 4.5. We see that the harmonics are heavily suppressed when the control is enabled. This verifies the circulating current control's operation for the A-MMC.

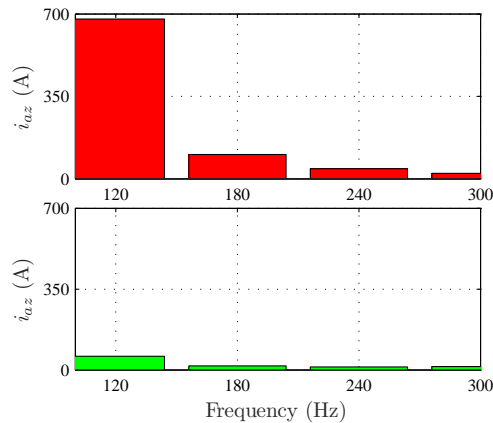
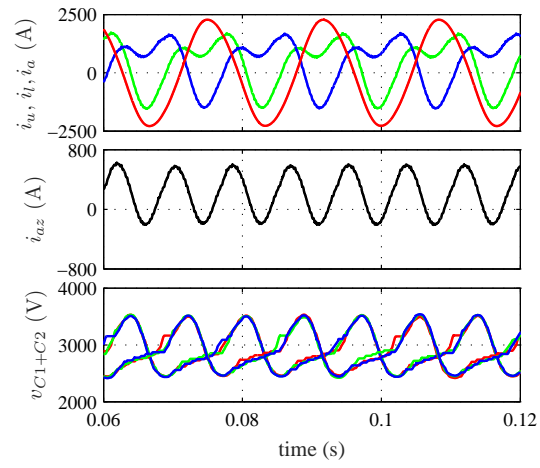
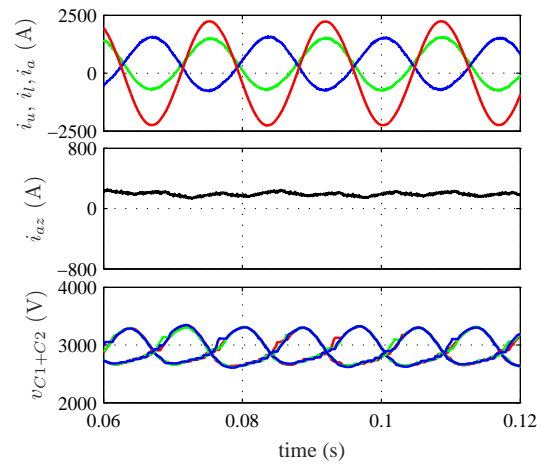


Figure 4.5: FFT of phase difference current: (top) without circulating current control (bottom) with circulating current control



(a)



(b)

Figure 4.6: (top to bottom) Currents in upper arm and lower arm with output phase current, circulating current, capacitor voltages: (a) without circulating current control (b) with circulating current control;

Chapter 5

A-MMC and MMC - A Comparison

The A-MMC topology presents some essential advantages which make it a viable candidate, to be considered as an alternative to the conventional MMC. We build this case by measuring essential circuit parameters, of both the A-MMC and MMC operating in same conditions. In the following sections, an exhaustive comparison is presented using the power dissipation figures, voltage and current harmonic distortions, ripple and arm current variations, all evaluated over a wide range of delivered power, switching frequency and modulation factors. Circuit structure and component count comparison for a variety of multilevel converters is also presented.

5.1 Loss Analysis

PLECS Blockset provides an environment for incorporating thermal models of the circuit components, which can then be used to measure the thermal losses across them. The modulation, balancing and control tasks were done through MATLAB Simulink and the drive signals were then supplied to the PLECS circuit. The switch thermal models were acquired through ABB's model library [29]. ABB 5SNA 1600N170100 and ABB 5SNA 1500E330305 were the switches used for V_C and $2V_C$ rated submodules, respectively, in the A-MMC. Only V_C rated submodules were used in the MMC. The A-MMC contained three modules in each arm whereas MMC was simulated with nine

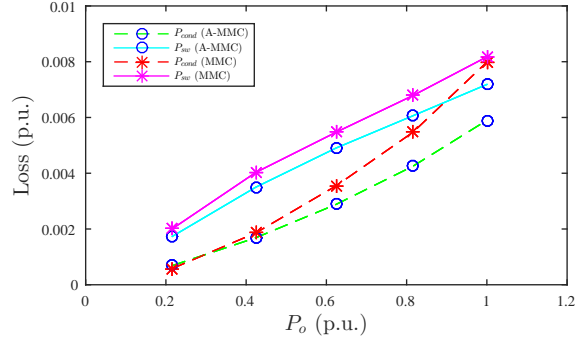
modules per arm.

For both converters, loss figures were calculated over varying P_o (at rated f_s) and f_s (at rated P_o). To provide a common comparison platform, all loss quantities were then converted to per unit (p.u.) basis. The base value for this process was taken to be the output power at maximum P_o (or f_s) of operation for that data set. Other circuit parameters were as listed in Table 4.1.

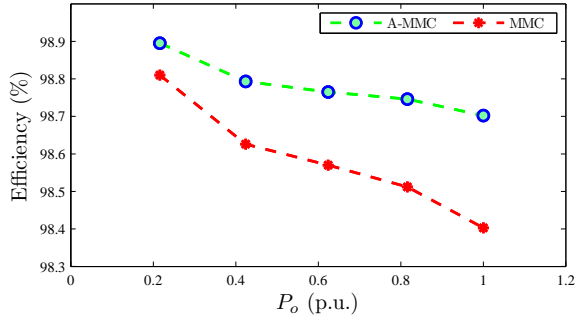
5.1.1 Varying P_o

Conduction and switching losses (P_{cond} and P_{sw}), over varying output power, have been plotted in Fig. 5.1(a), for both the converters. Since the A-MMC has lesser submodules, it presents less resistive path to the arm currents leading to lowered P_{cond} over the entire spectrum. The same is true for P_{sw} , since lesser modules have to be switched. Also, the A-MMC switching loss figure benefits from Hybrid PWM since it necessitates lesser switching transitions than PS-PWM.

In Fig. 5.1(b), the A-MMC and MMC are compared on the basis of efficiency plotted against varying P_o . From Fig. 5.1(b), it can be observed that the efficiency of A-MMC gains an increasing advantage as the output power rises. This can be explained from the fact that, as shown in Fig. 5.1(a), although the contribution of P_{cond} rises for both A-MMC and MMC, it gets steeper at high P_o for the MMC since P_{cond} is dependent on the second degree of arm current. Hence, due to lesser modules in the A-MMC, P_{cond} becomes steeper as P_o rises (arm current rises). On the other hand, from ABB's IGBT datasheets [29], it's observed that the switching energies rise fairly linearly over the range of P_o used here. Hence contribution of P_{sw} rises only linearly.



(a)



(b)

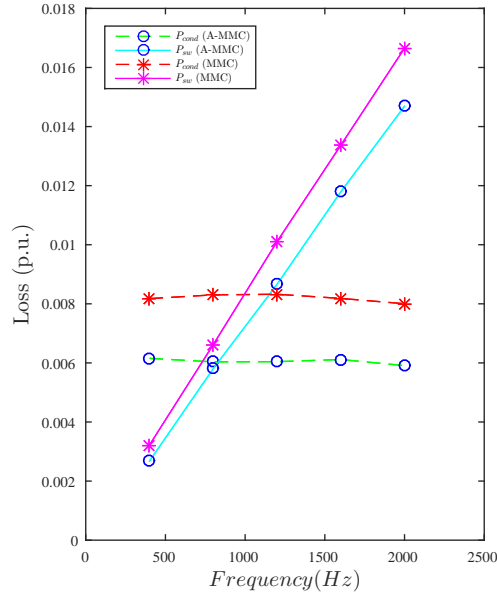
Figure 5.1: (a) Variation of conduction and switching losses with output power; (b) Variation of efficiency with output power

5.1.2 Varying f_s

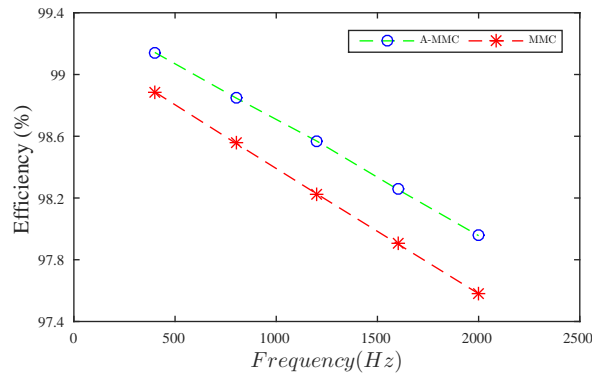
Fig. 5.2(b) depicts the trend of losses over varying frequency. As expected, the P_{cond} for both the converters remains almost constant throughout whereas P_{sw} climbs. Note that the A-MMC modules require more insertions/removals to generate same number of levels as the MMC, since they have lesser modules. Hence, the A-MMC provides more benefits in those scenarios where the conduction loss will assume increasing significance in the total loss figures. Also, new age wide band gap devices can be considered, which provide for significantly lower switching energies resulting in decreased dominance of P_{sw} .

Comparison of efficiency, plotted against f_s , is performed through Fig. 5.2(c). It shows a predictable linear fall. As can be seen from Fig. 5.2(b), the P_{cond} remains

almost constant with f_s whereas P_{sw} linearly rises. Hence there is a linear rise in total loss figures, leading to corresponding drop in efficiency. The slope of P_{sw} for the A-MMC in Fig. 5.2(b), and consequently for efficiency in Fig. 5.2(c), isn't completely aligned with that of the MMC. This can be attributed to the fact that the A-MMC is using two sets of submodules at two different voltages, which possess different switching energy behaviors.



(a)



(b)

Figure 5.2: (b) Variation of conduction and switching losses with switching frequency; (c) Variation of efficiency with switching frequency

5.2 Output Harmonics

The quality of output waveforms is compared in this section. The Total Harmonic Distortion (THD) in output voltage v_o and current i_o is taken as the metric for this purpose. Their THDs are evaluated as a function of the modulation index m and plotted in Figs. 5.3(a) and 5.3(b). Note that in these measurements, the load i_o is maintained at its rated value, over the entire range of m .

Since both converters are set up so as to generate same number of voltage levels, the THD figures of v_o in Fig. 5.3(a) show that they follow closely for both of them. As the number of modules are increased, as will be the case in typical applications, the effect of switching-related harmonics will decrease further and the figures will follow even closely.

On the other hand, the THD for i_o shows a clear difference in favor of the MMC. MMC is being driven by PS-PWM which utilizes n phase-shifted carriers if it needs to generate $n + 1$ levels. Whereas the A-MMC utilizes $n/3$ phase shifted carrier groups to achieve the same. The location of dominant harmonics, hence, is three time higher for an MMC operated using PS-PWM with same f_S as an A-MMC operated using Hybrid PWM. The load inductance then offers thrice the impedance to MMC's i_o harmonics, as opposed to what it offers for the A-MMC, resulting in improved filtering action. This is depicted in Fig. 5.3(b), which shows better current THD performance of the MMC over the entire spectrum of m .

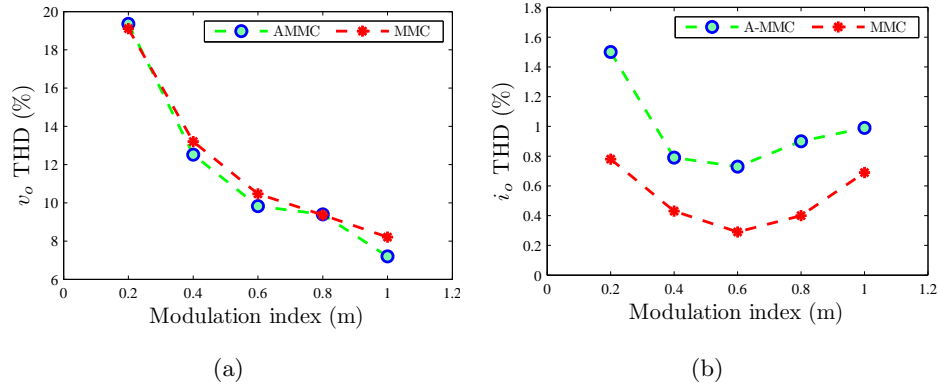


Figure 5.3: Variation of (a) output voltage THD; (b) output current THD; with modulation index

5.3 Capacitor voltage ripple and Circulating current

Capacitor voltage ripple, on per-unit basis, has been plotted against m for both the converters in Fig. 5.4(a). For the MMC, this has been evaluated by finding the average ripple for all modules in the center arm and then per-unitizing the same using the rated V_C value. Whereas for the A-MMC, the ripples for both V_C and $2V_C$ ASMs in the center arm have been added and then averaged. This was then converted to p.u basis using $3V_C$ as the base value. As can be seen, the A-MMC shows superior performance over the entire range of m . These values vary with C_1 and C_2 values and the simulations were performed at their rated values, obtained from Table 4.1.

Fig. 5.4(b) shows the variation of RMS of circulating current i_{circ} , with m . It was evaluated for the center arm. The per-unitization was done with the RMS value of i_o as the base. The values follow closely for both the converters showing sharp deviation only at higher m . These values are dependent on the tuned parameters of the circulating current controller. To ensure uniformity, the i_{circ} in both converters was suppressed using a controller, with same parameters. The key takeaway is that the designed circulating current suppression works well with the A-MMC.

Note that, both these measurements were performed using the rated load at all values of m .

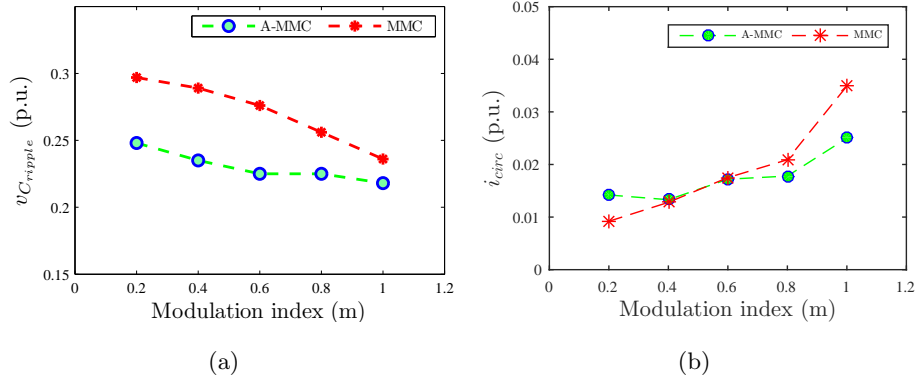


Figure 5.4: (a) Normalized capacitor voltage ripple; (b) Circulating current RMS

5.4 Circuit Structure Components

Multilevel converters are gaining prominence in high power applications [30]. Applications like energy generation/conversion, industrial drives, automotive, locomotive and ship propulsion etc [31–33] are increasingly adopting them. This has given birth to a variety of converters and it becomes essential to have an analytical comparison between them. This usually forms the first step of the design process, to aid in selection of the appropriate technology. A comparison has been done in this section, in Table 5.1, from the viewpoint of circuit component count. As the power rating increases, the converter footprint and subsequent cost becomes a very important factor. Note that, each topology has some unique features which might present advantages in specialized applications and hence such a comparison could differ, based on the parameter of importance.

The Half-Bridge (HB) and Full-Bridge (FB) modules impose an extra 33% component count cost to generate the same number of output voltage levels, over the the A-HB (A-MMC with HB modules, Asymmetric HB) and A-FB (A-MMC with FB modules, Asymmetric FB). The Clamp Double (CD) and FB modules provide fault handling capability but that comes at the expense of extra switches and diodes. This impairs their efficiency as well since it leads to extra losses. A-FB modules can be a credible alternative if fault handling capability is desired. It presents a good balance of relatively lower component count and fault handling capability. The modulation, voltage balancing and circulating current control techniques used in this thesis can be used with the A-FB modules as well. The Neutral-Point Clamped (NPC), Flying Capacitor (FC) and T-type modules can generate three voltage levels as opposed to the A-HB modules, which produce two. But the total number of IGBTs and diodes required to do the same is still near about what the HB modules use. Hence they don't provide any advantage over A-HB modules. Also, lesser switching devices translates to lower numbers of gate drivers required, reducing costs further.

The A-MMC presents unique challenges in terms of the control complexity, especially in terms of voltage balancing. Hence that is an extra cost imposed, as opposed to other module types. But it doesn't scale, unlike the component count which increases with the power rating. Implementation of high power converters also necessitates the usage of additional devices like protection thyristors and bypass switches. These are essential for

safety and bypassing modules during maintenance. The asymmetric modules perform moderately on this count but are advantageous when the comparison is only between the MMC and A-MMC. Interconnection of these modules also requires bus-bars with high current carrying capability. The asymmetric modules are clearly advantageous on this count as well. All these can contribute to lowered capital costs, in an A-MMC based HVDC system. Hence the A-MMC proves to be a credible and a promising alternative for modular converters based HVDC systems of future.

Table 5.1: Comparative analysis between different module structures

Parameter	HB	FB	CD	NPC	FC	T	A-HB	A-FB
No. of modules*	$2m$	$2m$	m	m	m	m	$0.66m^\dagger$	$0.66m^\dagger$
No. of IGBT's	$4m$	$8m$	$5m$	$4m$	$4m$	$4m$	$2.66m$	$5.33m$
No. of diodes	$4m$	$8m$	$7m$	$6m$	$4m$	$4m$	$2.66m$	$5.33m$
No. of thyristors	$2m$	0	0	m	m	m	$1.33m$	0
Bypass switches	$2m$	$2m$	m	m	m	m	$1.33m$	$1.33m$
No. of busbars	$2m$	$2m$	m	m	m	m	$0.66m$	$0.66m$
Semiconductor losses	=	highest	high	high	=	low	lowest	high
No. of Gate drivers	$4m$	$8m$	$5m$	$4m$	$4m$	$3m$	$2.66m$	$5.33m$
Fault handling	X	✓	✓	X	X	X	X	✓
Control complexity	low	low	low	high	med	high	highest	highest

* This is assuming per leg of the MMC is generating the same number of output voltage levels of $2m+1$

† This is considering each module has two unequal asymmetric submodules rated at V_c and $2V_c$ respectively

Chapter 6

Conclusion and Future Scope

HVDC is an enabler for large scale renewable energy generation and transmission. This high power DC technology has seen an increasing deployment of VSC-based solutions. Among the VSCs, the MMC is becoming a preferred choice for HVDC implementations. But MMCs present some challenges, like high component count and system footprint, which partially offset many other advantages like the modularity, scalability and reduced filtering requirements. Other multilevel converters employed for HVDC conversion process suffer from similar drawbacks. With this background, the A-MMC becomes an important converter to project.

The A-MMC is essentially an MMC circuit, with multi-level modules (using submodules at asymmetric voltages) in place of symmetric modules. For controlled operation of this topology, Hybrid PWM was proposed. It combines the features of LS-PWM and PS-PWM and is also able to generate multi-level switching signals essential to drive the A-MMC modules. Once these switching signals were generated, a voltage balancing algorithm had to be designed which could perform the task of balancing the asymmetric voltages. This new technique had to balance two sets of capacitors, within the same arm, at two different voltages. It is essential for the A-MMC operation because, as was shown, without this balancing the capacitor voltages diverge from their intended values. In this condition, the additional level generation capability could not be exploited. The proposed algorithm was successful in ensuring this balancing. As is characteristic of MMCs, A-MMC also suffers from circulating current within the arms, which if not suppressed, cause increased capacitor voltage ripple and thermal losses. Hence, a

circulating current controller was designed for the A-MMC as well. The operation of the overall A-MMC system, and also the performance of individual control blocks, was verified using MATLAB/Simulink and PLECS Blockset.

To project the A-MMC as a superior alternative to the MMC, a comparative study of both the converters was performed. Loss figures were obtained for both and compared over the entire range of output power and switching frequency. An analytical circuit component count comparison among various multilevel converter topologies was also performed. The A-MMC displayed a comprehensive edge over the MMC. Performance was also compared on circuit metrics like output voltage/current THD, capacitor voltage ripple and circulating current values. The A-MMC either followed closely or performed better on these indicators than the MMC. These figures also validated the performance of the modulation, voltage balancing and circulating current control blocks of the A-MMC. Using this foundation, the A-MMC was projected to be a credible alternative to the MMCs in future HVDC implementations, for a more efficient and compact system.

6.1 Future work

To cement the A-MMCs as a stronger VSC candidate, the research could further extend into following directions:

- The existing hardware setup in the lab can be modified to include capacitors across the ASMs, to verify the A-MMC operation using control blocks presented in this thesis
- New age wide-bandgap devices like SiC and GaN could be explored for circuit implementations, since they lead to lesser switching losses. This widens the region of operation of the A-MMCs even more, where they will show clear advantage over the MMCs
- In the class of multilevel modules comprising of two submodules, further innovation can be done by utilizing asymmetric voltages of V_C and $3V_C$. Extracting all voltage levels in this configuration will require communication between voltage balancing blocks of both upper and lower arms

- Full bridge implementation of the A-MMC can be done since it presents a solution which has only a partial component count increment over the half-bridge MMC but offers DC fault current carrying capability, unlike the full-bridge MMC where the component count increment is very significant

References

- [1] Kamran Sharifabadi, Lennart Harnefors, Hans-Peter Nee, Remus Teodorescu, and Staffan Norrga. *Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems*. John Wiley & Sons, 2016.
- [2] Energy Information Administration (US). *Annual Energy Outlook 2017: With projections to 2050*. Government Publishing Office, 2017.
- [3] Muhammad H Rashid. *Power electronics handbook: devices, circuits and applications*. Academic press, 2010.
- [4] N. M. Kirby, Lie Xu, M. Lockett, and W. Siepmann. HvdC transmission for large offshore wind farms. *Power Engineering Journal*, 16(3):135–141, June 2002.
- [5] P. Mitra, L. Zhang, and L. Harnefors. Offshore wind integration to a weak grid by vsc-hvdc links using power-synchronization control: A case study. *IEEE Transactions on Power Delivery*, 29(1):453–461, Feb 2014.
- [6] J.M. Carrasco, L.G. Franquelo, J.T. Bialasiewicz, E. Galvan, R.C.P. Guisado, Ma.A.M. Prats, J.I. Leon, and N. Moreno-Alfonso. Power-electronic systems for the grid integration of renewable energy sources: A survey. *Industrial Electronics, IEEE Transactions on*, 53(4):1002–1016, June 2006.
- [7] M. P. Bahrman and B. K. Johnson. The abcs of hvdc transmission technologies. *IEEE Power and Energy Magazine*, 5(2):32–44, March 2007.
- [8] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades. Vsc-based hvdc power transmission systems: An overview. *IEEE Transactions on Power Electronics*, 24(3):592–602, March 2009.

- [9] A. Lesnicar and R. Marquardt. An innovative modular multilevel converter topology suitable for a wide power range. In *2003 IEEE Bologna Power Tech Conference Proceedings*, volume 3, pages 6 pp. Vol.3-, June 2003.
- [10] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades. Modular multilevel converters for hvdc applications: Review on converter cells and functionalities. *IEEE Transactions on Power Electronics*, 30(1):18–36, Jan 2015.
- [11] Q. Hao, B. T. Ooi, F. Gao, C. Wang, and N. Li. Three-phase series-connected modular multilevel converter for hvdc application. *IEEE Transactions on Power Delivery*, 31(1):50–58, Feb 2016.
- [12] J. Qin and M. Saeedifard. Reduced switching-frequency voltage-balancing strategies for modular multilevel hvdc converters. *IEEE Transactions on Power Delivery*, 28(4):2403–2410, Oct 2013.
- [13] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou. Hybrid design of modular multilevel converters for hvdc systems based on various submodule circuits. *IEEE Transactions on Power Delivery*, 30(1):385–394, Feb 2015.
- [14] M. Saeedifard and R. Iravani. Dynamic performance of a modular multilevel back-to-back hvdc system. *IEEE Transactions on Power Delivery*, 25(4):2903–2912, Oct 2010.
- [15] Makoto Hagiwara, Ryo Maeda, and Hirofumi Akagi. Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (mmcc-dscc). *IEEE Transactions on Power Electronics*, 26(6):1649–1658, 2011.
- [16] Rainer Marquardt. Modular multilevel converter: An universal concept for hvdc networks and extended dc-bus-applications. In *Power Electronics Conference (IPEC), 2010 International*, pages 502–507. IEEE, 2010.
- [17] E. Solas, G. Abad, J.A. Barrena, S. Aurtenetxea, A. Carcar, and L. Zajac. Modular multilevel converter with different submodule concepts x2014;part i: Capacitor voltage balancing method. *Industrial Electronics, IEEE Transactions on*, 60(10):4525–4535, Oct 2013.

- [18] A.K. Sahoo, R. Otero-De-Leon, V. Chandrasekaran, and N. Mohan. New 3-level submodules for a modular multilevel converter based hvdc system with advanced features. In *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, pages 6269–6274, Nov 2013.
- [19] Kartik V Iyer, Ashish Kumar Sahoo, and Ned Mohan. Asymmetrical modular multilevel converter (a-mmc) based hvdc system. In *Energy Conversion Congress and Exposition (ECCE), 2015 IEEE*, pages 4693–4699. IEEE, 2015.
- [20] S. Debnath, Jiangchao Qin, B. Bahrani, M. Saeedifard, and P. Barbosa. Operation, control, and applications of the modular multilevel converter: A review. *Power Electronics, IEEE Transactions on*, 30(1):37–53, Jan 2015.
- [21] Binbin Li, Rongfeng Yang, Dandan Xu, Gaolin Wang, Wei Wang, and Dianguo Xu. Analysis of the phase-shifted carrier modulation for modular multilevel converters. *IEEE Transactions on Power Electronics*, 30(1):297–310, 2015.
- [22] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis. Carrier interleaved pwm techniques in modular multilevel converters: A comparison based on same voltage level waveforms. In *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3725–3730, Sept 2014.
- [23] Qingrui Tu, Zheng Xu, and Lie Xu. Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters. *IEEE transactions on power delivery*, 26(3):2009–2017, 2011.
- [24] Kalle Ilves, Antonios Antonopoulos, Staffan Norrga, and Hans-Peter Nee. Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters. *IEEE transactions on power electronics*, 27(1):57–68, 2012.
- [25] Zixin Li, Ping Wang, Zunfang Chu, Haibin Zhu, Yongjie Luo, and Yaohua Li. An inner current suppressing method for modular multilevel converters. *IEEE Transactions on Power Electronics*, 28(11):4873–4879, 2013.

- [26] Jiangchao Qin and Maryam Saeedifard. Predictive control of a modular multilevel converter for a back-to-back hvdc system. *IEEE Transactions on Power delivery*, 27(3):1538–1547, 2012.
- [27] Antonios Antonopoulos, Lennart Angquist, and Hans-Peter Nee. On dynamics and voltage control of the modular multilevel converter. In *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*, pages 1–10. IEEE, 2009.
- [28] Qingrui Tu, Zheng Xu, Hongyang Huang, and Jing Zhang. Parameter design principle of the arm inductor in modular multilevel converter based hvdc. In *Power System Technology (POWERCON), 2010 International Conference on*, pages 1–6. IEEE, 2010.
- [29] Insulated gate bipolar transistor (igbt) and diode modules with spt and spt+ chips. <http://new.abb.com/semiconductors/igbt-and-diode-modules>. Accessed: 2017-02-10.
- [30] Samir Kouro, Mariusz Malinowski, K Gopakumar, Josep Pou, Leopoldo G Franquelo, Bin Wu, Jose Rodriguez, Marcelo A Pérez, and Jose I Leon. Recent advances and industrial applications of multilevel converters. *IEEE Transactions on industrial electronics*, 57(8):2553–2580, 2010.
- [31] Yu Liu, Alex Q Huang, Wenchao Song, Subhashish Bhattacharya, and Guojun Tan. Small-signal model-based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based statcom. *IEEE Transactions on Industrial Electronics*, 56(6):2259–2269, 2009.
- [32] Paulson Samuel, Rajesh Gupta, and Dinesh Chandra. Grid interface of wind power with large split-winding alternator using cascaded multilevel inverter. *IEEE transactions on energy conversion*, 26(1):299–309, 2011.
- [33] Sergio Daher, Jürgen Schmid, and Fernando LM Antunes. Multilevel inverter topologies for stand-alone pv systems. *IEEE Transactions on Industrial Electronics*, 55(7):2703–2712, 2008.

Appendix A

Nomenclature

Table A.1: List of symbols

Symbol	Meaning
M_i	i^{th} module of A-MMC in a leg
ASM_1	submodule with capacitor at V_C voltage
ASM_2	submodule with capacitor at $2V_C$ voltage
S_{1i}	state of ASM_1 in M_i , inserted or bypassed
S_{2i}	state of ASM_2 in M_i , inserted or bypassed
v_{C1}	capacitor voltage of ASM_1 ($\bar{v}_{C1} = V_C$)
v_{C2}	capacitor voltage of ASM_2 ($\bar{v}_{C2} = 2V_C$)
v'_{C1}	normalized voltage of $ASM_1 = v_{C1}/V_C$
v'_{C2}	normalized voltage of $ASM_2 = v_{C2}/2V_C$
v_{Cxmax}	maximum capacitor voltage among all ASM_x
v_{Cxmin}	minimum capacitor voltage among all ASM_x
$v_{Cx,i}$	capacitor voltage of ASM_x in M_i
C_1, C_2	capacitance of ASM_1 and ASM_2
L_a, R_a	arm inductance and resistance
L_o, R_o	output inductance and resistance