Power Electronic Transformer with Open-End Winding Electric Drive for Wind Energy Conversion Systems

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Dedication

This thesis is dedicated to my parents.

Abstract

Power Electronic Transformers (PETs) provide a reduction in size over line frequency transformers by operating at much higher frequencies than line frequency or grid frequency. Due to their smaller size, they could be useful in renewable energy systems where an interface with the grid is needed. As the name suggests, a power electronic interface is needed to convert line frequency voltages to high frequency voltages before they can be fed to the transformer. A PET topology that has simple control and less number of high voltage devices would be considered desirable due to lower total device cost and easy control implementation. A push-pull based PET topology has been proposed in the past which contains only two high voltage controlled switching devices and the control of those two devices is very simple. This topology could be configured for single stage ac to dc power conversion, to which an open-end winding dc to ac converter could be connected. Alternatively, it could be configured for direct ac to ac power conversion using dual matrix converters.

In the first part of this thesis, the aforementioned push-pull based power electronic topology has been studied for power conversion from ac to dc and vice versa. Both single phase ac to dc and three phase ac to dc variants of the topology have been analyzed for power transfer, rms currents and soft switching. They provide attractive features which include single stage ac to dc bidirectional power conversion, unity power factor operation in open loop and control of dc side voltage using simple PI controllers.

The other part of this thesis deals with open-end winding drives for suppression of common mode voltages at machine terminals. Switching frequency Common Mode Voltages (CMV) are generated by conventional Pulse Width Modulated (PWM) drives at machine terminals, which cause shaft voltage build up leading to bearing currents. These bearing currents are harmful for the machine and also cause Electromagnetic Interference (EMI). Open-end winding drives consist of one electric drive connected on each end of a three phase electric motor with the stator neutral opened up to give three more terminals. Open-end winding drives can be controlled to suppress switching frequency CMV at machine terminals. In this thesis, open-end winding two level Voltage Source Inverter (VSI) drive and open-end winding two level Matrix Converter (MC)

drives have been investigated. Carrier based PWM techniques have been proposed for each of these drives for suppressing CMV. In addition, an improved four step commutation method has been proposed for the open-end winding matrix converter drive to suppress CMV spikes during the commutation process.

Finally, a circuit consisting of the reduced switch PET connected with an open-end winding MC drive has been studied for single stage ac to ac power conversion with open loop power factor control.

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Chapter 1

Introduction

The share of renewable energy generation is increasing in the power production and aggressive targets have been set by countries to rely more and more on renewables rather than conventional power sources [1]. Therefore, it is necessary to make renewable energy generation more cost effective and easier to integrate into the power grid. In case of wind generation, electric drives are an important part of the power conversion system, since they allow control of the generator to enable its smooth operation during varying wind conditions. In addition, a transformer is needed to connect the power conversion system to the grid, in order to provide the required voltage transformation and galvanic isolation. In this chapter, the state of the art topology is discussed and drawbacks are discussed. Then, the proposed topologies are introduced and their benefits are outlined. Finally, the layout of the thesis and its contributions are discussed.

1.1 State of the art

The state of the art system for wind energy conversion systems is shown in Fig. 1.1. It consists of a wind generator, which is a squirrel cage induction machine mechanically coupled with the wind turbine. The wind generator is connected to the two level inverter drive, which controls the generator. The two level inverter is connected to the grid side two level inverter through a dc link. Finally, the grid side inverter is connected to the grid with a step up line frequency transformer.

Typically, the entire power electronics and the transformer are installed at the base

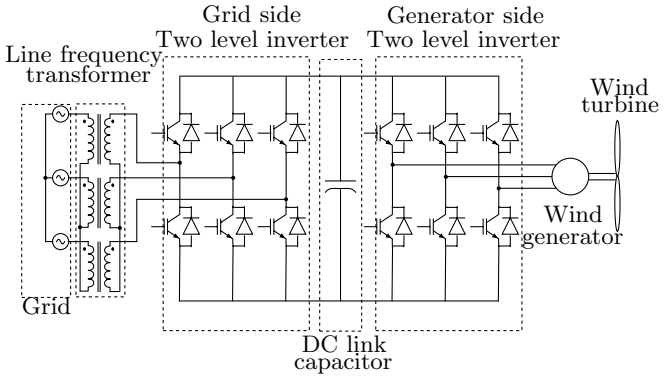


Figure 1.1: State of the art for wind power conversion systems

of the turbine, which means that the generator is connected to the generator side inverter through thick wires that carry large currents. These cables are expensive and have high conduction losses due to the large currents. A solution is to place the entire power electronic structure in the nacelle, as done in some recent turbine models [2]. This is however also an expensive solution, since putting a bulky line frequency transformer in the nacelle increases the infrastructure cost. This is one of the issues with the current state of the art. A power electronic transformer (PET) that operates at much higher frequencies than line frequency is a lot smaller in size than line frequency transformers [3]. Therefore using a PET place of a line frequency transformer in the nacelle could lead to overall size and weight reduction. Multiple PET topologies have been proposed and studied, which provide single stage or multi-stage conversion of power from one desired form to another and attractive features like soft switching of devices and power factor correction. Applications for PETs have been proposed in power distribution, PV vehicle grid interface and grid integration of renewable energy sources [3–10].

Another issue with current technology is the switching common mode voltage (CMV) that the two inverter drive used to control the generator, causes at the terminals of the machine. These voltages have high frequency components, which lead to shaft voltage buildup and bearing currents, which cause wear and tear of the bearings leading to premature failure of the machine [11–15]. There are different solutions to this problem, which include using common mode filters [16–18], ferrite beads, grounding brushes, modified Pulse Width Modulation (PWM) techniques [19, 20] and open-end winding drives [21–23]. The stator of an induction machine can be opened to give three more

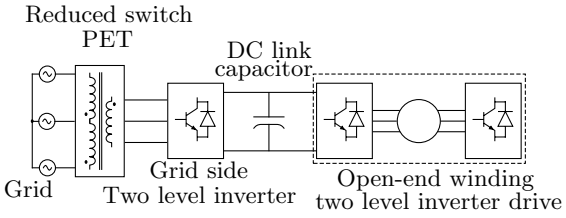


Figure 1.2: Reduced switch ac to dc power electronic transformer with open-end winding two level inverter drive

terminals, thus giving a total of six terminals. An open-end winding drive constitutes two power converters, one connected to each end of the motor. These drives can be regulated using PWM techniques such the common mode voltage at the machine terminals is either zero or devoid of high frequency components [24–33].

1.2 Proposed topologies

A proposed topology is shown in Fig. 1.2. It employs a PET instead of line frequency transformer, which gives the advantage of reduced size. The PET in this topology employes only two switches which are controlled in a very simple manner. A ac to dc converter is converter is connected to the secondary side of the PET. An open-end winding two level inverter drive is connected to the dc link, to control the generator. This drive is operated so as to suppress CMV at the machine terminals, which helps in reducing the wear and tear to the bearings, thus improving reliability of the machine and hence overall system.

The topology in Fig. 1.2 converts ac to dc and then to ac. A second topology is proposed in Fig. 1.3, which uses an open-end winding matrix converter (MC) drive at the transformer secondary, thus providing direct ac to ac power conversion. Just like the open-end winding two level inverter drive, the open-end winding MC drive can be operated to suppress CMV at machine terminals as well.

In order to analyze the three phase AC/DC PET in Fig. 1.2, a single phase variant of the ac to dc PET in is also analyzed as a starting point. Although this topology has been proposed and studied before [34], the power transfer capability obtained in previous studies are relatively low. Therefore, it has been analyzed to improve upon the power transfer capability over previous studies.

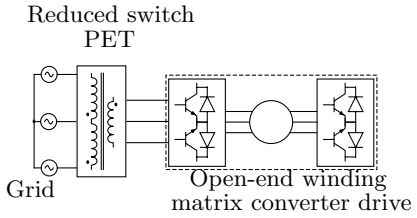


Figure 1.3: Reduced switch ac to ac power electronic transformer with open-end winding matrix converter drive

1.3 Motivation and scope

Power electronic transformers and open end winding drives provide attractive features for application in renewable energy systems. However, they pose challenges of complex control algorithms and increased overall system complexity. The motivation of this thesis is to analyze low switch count PET topologies and to provide solutions for closed loop control for power transfer and unbalanced grid voltage operation. Another objective is to develop carrier based Pulse Width Modulation (PWM) techniques for open-end winding drives with CMV elimination in order to simplify control implementation compared to traditional space vector techniques.

1.4 Contributions

The contributions of this thesis are as follows.

Analysis of single phase ac to dc PET for increased power transfer (compared to [34]), soft switching and low order line frequency harmonic compensation

Analysis of three phase ac to dc PET for increased power transfer (compared to [35]) and soft switching

Analysis of three phase ac to dc PET for closed loop control of dc link voltage over entire operating region (as compared to one mode in [34]) and operation under unbalanced grid voltage

Carrier based implementation of Space Vector PWM for open-end winding two level inverter drive for CMV elimination

Carrier based implementation of Space Vector PWM for open-end winding matrix converter drive for CMV elimination

Modified four step commutation technique for open-end winding matrix converter drive to reduce circulating currents

Analysis of three phase PET with open-end winding matrix converter drive for power transfer and soft switching

1.5 Organization

The first chapter introduces the context and the goals of this thesis.

The second chapter provides detailed analysis of single phase ac to dc PET. The analysis shows that the power transfer capability of the PET can be increased by changing the mode of operation of the PET for a given ac voltage and dc voltage levels, compared to prior art. Analysis has also been done to point out which devices undergo soft switching in this mode of operation. Finally, a technique has been discussed to reduce low order line frequency harmonics in ac current that appear when the PET operates in the new mode.

The third chapter discusses the three phase ac to dc PET. Similar to the single phase ac to dc PET, the three phase variant has been analyzed for operation in new modes which provide increased power transfer capability compared to prior art. Soft switching of the power devices has been also analyzed. Then, a method has been proposed to design a PI controller for regulating the dc link voltage. Finally, operation under imbalanced grid voltage has been discussed and a technique has been proposed to enable constant power transfer during imbalanced grid voltages.

In the fourth chapter, a carrier based implementation of the Space Vector PWM technique has been presented for the open-end winding two level inverter drive for CMV elimination. The carrier based method is simpler to implement than the space vector method.

The carrier based Space Vector PWM technique for open-end winding two level

inverter drive has been extended for open-end winding MC drive in the fifth chapter. A similarity between the techniques for open-end winding two level inverter and open-end winding MC drives for CMV elimination has been established. Finally, a modified four step commutation method has been proposed for suppressing circulating currents in open-end winding MC drives.

In the sixth chapter, the three phase PET with open-end winding matrix converter drive has been analyzed. The technique developed in chapter five has been applied to control the open-end winding matrix converter drive in order to achieve CMV elimination at machine terminals connected to the drive and to achieve soft switching of the primary side switches of the PET.

The seventh and final chapter summarizes and concludes the thesis.

Chapter 2

Single phase AC-DC PET

Power Electronic Transformers (PET) are attractive due to their smaller size compared to line frequency transformers, since they operate at higher frequencies than line frequency. To operate these transformers at a high frequency and connect them with line frequency grid and equipment, a power electronic interface is needed to convert the line frequency voltage to high frequency. There are many different types of interfaces, such as push-pull, half and full bridge with unidirectional and bidirectional switches, matrix converters etc [7, 9, 36]. Several of these PET configurations are operated as a Dual Active Bridge (DAB) for bidirectional power transfer through a transformer. A DAB works on the simple principle of phase shift between two high frequency voltages applied across an inductor for power transfer [37–40]. In Fig. 2.1 a simple form of DAB is illustrated along with the voltage and current waveforms.

The voltage waveforms v_1 and v_2 are phase shifted by a time period δT_s, as shown in Fig. 2.1(b). The sign of the phase shift parameter δ determines the direction of power flow through the inductor. These waveforms are illustrated as square waves, but they could be quasi square waves or multi-level waveforms, obtained using PWM of two level or multi-level converters. Apart from the phase shift parameter δ, PWM and multi-level converters could be used to regulate power flow through the inductor. Apart from the simple principle of phase shift for its operation, a DAB offers the benefit of soft switching for the power electronic switches connected to the transformer, within a certain operating range. This is is highly desirable since it reduces the net losses in the circuit and reduces device stress.

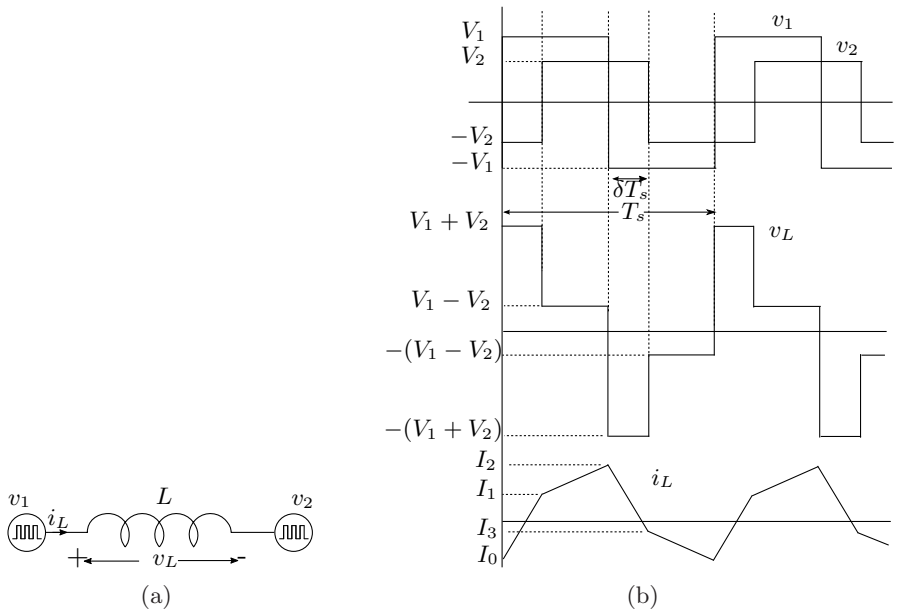


Figure 2.1: (a) Basic DAB circuit (b) Voltage and current waveforms

In this chapter, a push-pull based PET is studied for increased power transfer. This topology provides single stage power transfer from a single phase ac side to a dc side and vice-versa, using the aforementioned DAB principle. The main advantages of this PET are simple control of high side switches, bidirectional power transfer at unity power factor and soft switching of power switches along with single stage power conversion. The PET operates in two modes, one of which known as inner mode has been studied in [34]. The main issue with the inner mode is low power transfer capability for a given voltage level. Hence, investigation has been made into the other mode, called the outer mode for achieving the increased power transfer capability for a given voltage level and other system parameters.

2.1 Topology description and modulation technique

The PET circuit diagram is shown in Fig. 2.2. It utilizes a three winding transformer. The primary side of the transformer has two windings, while the secondary side has one winding. The turns ratio of each primary winding to the secondary winding is $1 : n$. The dot at each winding of the transformer signifies the voltage polarity. The two

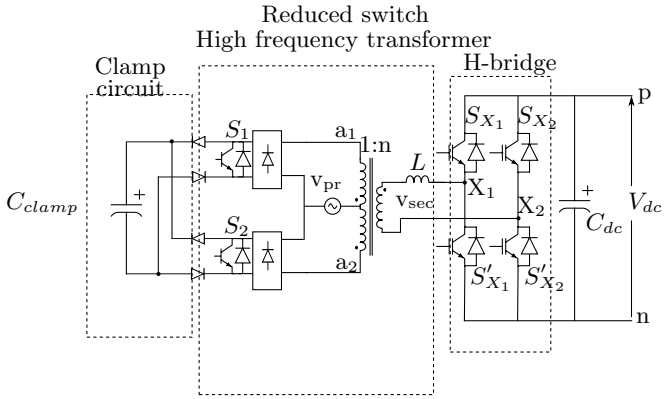


Figure 2.2: Reduced Switch PET

primary windings are connected to the positive terminal of ac voltage source v_{pr} on one end. The amplitude of this voltage is V_{pr}. Note that the dot terminal of one primary winding and other terminal (without a dot) of the second primary winding is connected to the source. On the other end, they are connected to a single phase diode rectifier. The negative terminal of ac source is also connected to the diode rectifiers. The DC side of the diode rectifiers are connected to the IGBTs S_1 and S_2. These IGBTs are connected to a single clamp circuit, for dissipating any transformer leakage inductance energy during commutation. The secondary side of the transformer is connected to an H-bridge through an inductor L. The inductor L is the sum total of all the leakage inductance of the transformer reflected on secondary side and any additional inductance connected to the secondary winding. The H-bridge consists of four IGBTs S_{X_1}, S'_{X_1}, S_{X_2} and S'_{X_2}. It is connected to a dc link with voltage V_{dc}, which could be connected to a power converter connected to a renewable power source, such as a photovoltaic cell array.

2.1.1 Primary side switch modulation

The ac source v_{pr} connected to the primary side of the transformer is a 60 Hz or any other line frequency source. It is defined mathematically below.

$$v_{\text{pr}} = V_{pr} \sin(\omega t) \tag{2.1}$$

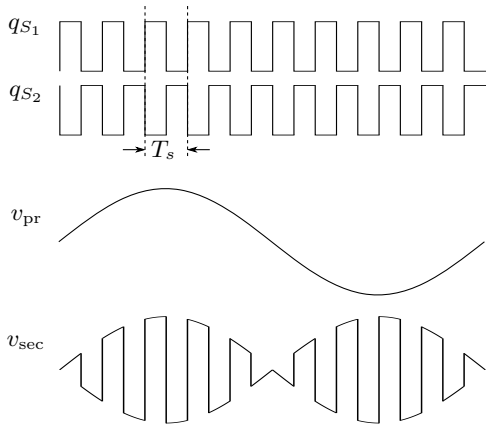


Figure 2.3: Primary side switch pulses and voltage waveforms

The switches S_1 and S_2 are switched in a complimentary manner with 50% duty ratio at a high frequency compared to the line frequency. When S_1 is turned ON, the winding terminal a_1 is connected to ac source negative through S_1. The voltage appearing on the transformer secondary v_{sec} has then the same polarity as v_{pr}. When S_2 is turned ON, the winding terminal a_2 is connected to ac source negative through S_2. Now, the transformer secondary voltage v_{sec} has an opposite polarity to that of v_{pr}. Thus, the secondary voltage appearing at the secondary winding terminals is a high frequency square wave, with a sinusoidal envelope. This is illustrated in Fig. 2.3. The waveforms q_{S_1} and q_{S_2} represent the gate pulses of IGBTs S_1 and S_2 respectively. One switching period for S_1 and S_2 has been denoted T_s. Mathematically, the expression for v_{sec} is given as follows.

$$v_{\text{sec}} = \pm\, n v_{\text{pr}} = \pm \hat{v}_{\text{sec}} \qquad (+ \text{ for } S_1 \text{ ON}, - \text{ for } S_2 \text{ ON}) \tag{2.2}$$

where

$$\hat{v}_{\text{sec}} = n v_{\text{pr}} \tag{2.3}$$

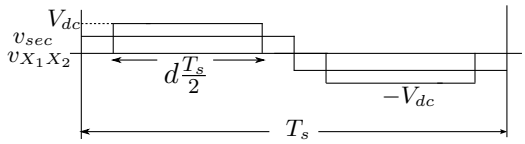


Figure 2.4: Transformer secondary and H-bridge voltage waveforms

2.1.2 Secondary side H-bridge modulation

The voltage waveform generated on the secondary side of the transformer v_{sec} is a high frequency square wave with a low frequency sinusoidal envelope. This is the voltage at one end of the lumped inductor L in Fig. 2.2. In a DAB, switching voltages are generated at each end of an inductor for power transfer. In this case, the voltage at the other end of the inductor is output of the H-bridge $v_{X_1X_2}$. Hence, the H-bridge on the secondary side of the transformer is pulse width modulated so as to generate a quasi square voltage $v_{X_1X_2}$ between the terminals X_1 and X_2. This has been shown in Fig. 2.4. In the figure, the transformer secondary waveform v_{sec} is assumed to be a true square wave with amplitude V_s for one switching period T_s of primary switches S_1 and S_2. This is a valid assumption if T_s is much smaller than the time period of the line frequency voltage v_{ps}, which is the case here. Hence, the sinusoidal envelope of v_{sec} has been ignored for one switching time period. The voltage $v_{X_1X_2}$ is a quasi square wave with an amplitude equal to the dc link voltage V_{dc}.

In the modulation strategy explored in this chapter, the average amplitude of the H-bridge voltage $v_{X_1X_2}$ over half a switching period i.e. $\frac{T_s}{2}$ is the same as that of the transformer secondary voltage v_{sec}. Thus, the width of each pulse of the quasi square wave is $d\frac{T_s}{2}$, where

$$d = \frac{\hat{v}_{\text{sec}}}{V_{dc}} \tag{2.4}$$

The pulses of the four IGBTs of the H-bridge are shown in Fig. 2.5 to demonstrate how the voltage $v_{X_1X_2}$ is generated.

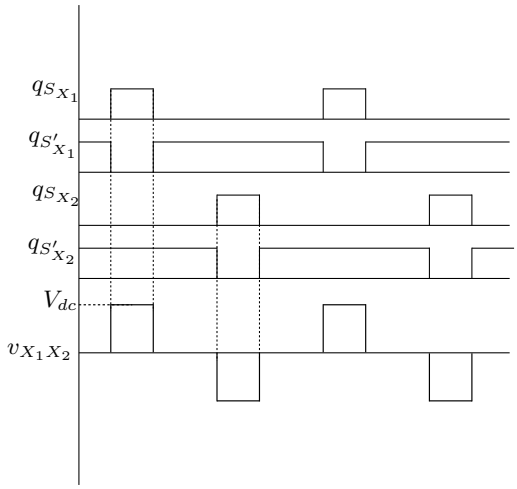


Figure 2.5: H-bridge PWM pulses and voltage waveform

2.2 Analysis of power transfer, currents and soft switching

In Fig. 2.4, the voltages v_{sec} and $v_{X_1X_2}$ are in phase i.e., they have an identical center point in each half of the switching period. If a phase shift of δT_s is introduced between these two voltages, then a power transfer will happen between them through the inductor L, as per the DAB principle. Assuming that the direction of phase shift is positive i.e. the H-bridge voltage $v_{X_1X_2}$ lags the transformer secondary voltage v_{sec}, there are two modes of operation, called Mode 1 and Mode 2 from now on. These two modes are shown in Fig. 2.6. In both of these modes, the voltage $v_{X_1X_2}$ is delayed by time δT_s with respect to voltage v_{sec}. In Mode 1 shown in Fig. 2.6(a), it is observed that the voltage pulses of $v_{X_1X_2}$ are within the same half cycle, i.e. the rising and falling edges of these pulses are within those of v_{sec}. Hence, Mode 1 is known as the inner mode. This is not the case with Mode 2, which is also known as the outer mode. The PET can operate in either of these two modes depending on the system conditions, which will now be discussed further. In addition, it should be noted that there is a hard limit on δ as per the DAB principle that it can't be more than one-fourth of the time period T_s in either direction i.e.

$$-\frac{1}{4} \leq \delta \leq \frac{1}{4} \tag{2.5}$$

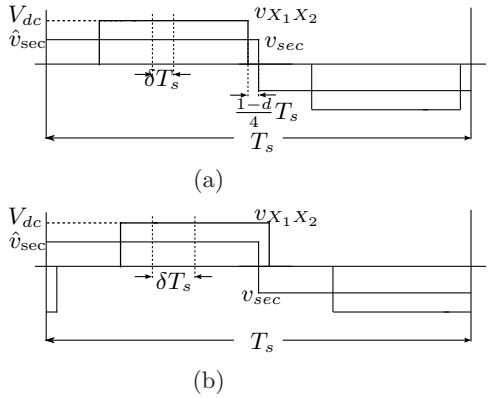


Figure 2.6: Modes of operation of single phase PET (a) Mode 1 (b) Mode 2

The voltage waveform v_{sec} is assumed to be a true square wave in a given switching period. However, it has a sinusoidal envelope at the line frequency and the voltage amplitude $\hat{v}_{\text{sec}}$ of the square wave therefore cannot be assumed constant throughout when it is looked over a line frequency time period. This is clear from (2.1) and (2.3).

Using (2.3) and (2.4), we obtain an expression for time varying duty ratio d as

$$d = \frac{nV_{pr}\sin(\theta)}{V_{dc}} = m\sin(\theta) \tag{2.6}$$

where $m = \frac{nV_{pr}}{V_{dc}}$ is the modulation index such that $0 \leq m \leq 1$, and
$\theta = \omega t$ is the angle of the primary side voltage.
It is observed from equation (2.6), that the width of the voltage pulse of voltage $v_{X_1X_2}$ changes with time and it means that for a given value of δ and m, the PET could swing between between Mode 1 and Mode 2. In Fig. 2.6(b), it can be seen that the PET will stay in Mode 1 as long as the falling edge of voltage pulse of $v_{X_1X_2}$ occurs before that of v_{sec} in a half switching period. The maximum allowable δ for this to be true is such that:

$$\begin{aligned} 0 < & \delta T_s \leq \frac{1-d}{4}T_s \\ \implies 0 < & \delta \leq \frac{1-d}{4} \end{aligned} \tag{2.7}$$

Equation (2.7) gives the condition for the PET to stay in Mode 1. If this condition is not satisfied, i.e. δ goes beyond $\frac{1-d}{4}$, then the PET goes in Mode 2. Thus, the condition for Mode 2 is given as follows:

$$\frac{1-d}{4} \leq \delta \leq \frac{1}{4} \tag{2.8}$$

Equations (2.7) and (2.8) show that the mode of operation of the PET depends on duty ratio d and phase shift parameter δ. However, the duty ratio d itself varies with time and is also dependent on the modulation index m, as shown in (2.6). Hence, the PET can swing between Mode 1 and Mode 2 for a given value of m and δ. Equations (2.7) and (2.8) can be rewritten as

$$1 > 1 - 4\delta \geq d \quad \text{(Mode 1)} \tag{2.9}$$

$$d > 1 - 4\delta \geq 0 \quad \text{(Mode 2)} \tag{2.10}$$

From equations (2.9) and (2.10), it can be seen that as the quantities $(1-4\delta)$ and time t change while keeping modulation index m constant, the PET transitions between Mode 1 and Mode 2. Graphically, this is shown in Fig. 2.7. It is observed that there are two distinct regions of operation i.e. Region 1 and Region 2. Region 1 is for lower values of δ and here, the PET operates exclusively in Mode 1. Region 2 starts when δ goes beyond a value given in (2.11) below.

$$\begin{aligned} \delta &> \frac{1-m}{4} \\ \implies (1-4\delta) &< m \end{aligned} \tag{2.11}$$

Equation (2.11) is obtained by replacing d with m in (2.7), since m is the highest value d can attain and if the PET stays in Mode 1 for that value, it is in Region 1. In Region 2, we can see that the PET operates both in Mode 1 and Mode 2. In Fig. 2.7, it is shown for a value $\delta = \delta_1$. It is observed that the PET stays in Mode 1 for $0 \leq \theta < \phi$, then goes in Mode 2 for $\phi \leq \theta < 180^\circ - \phi$ and then comes back in Mode 1 for $180^\circ - \phi \leq \theta < 180^\circ$. This sequence is then repeated for $180^\circ \leq \theta < 360^\circ$. The angle ϕ is obtained using

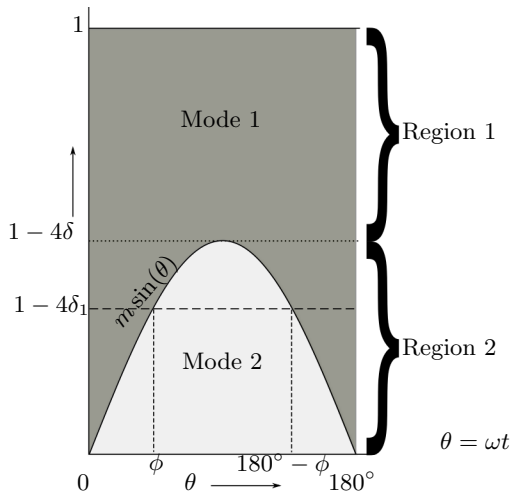


Figure 2.7: Single phase PET operating modes and regions

boundary condition of Mode 1 from (2.9) as follows:

$$\begin{aligned} d = m\sin(\phi) &= 1-4\delta \\ \implies \phi &= \sin^{-1}\left(\frac{1-4\delta}{m}\right) \end{aligned} \tag{2.12}$$

The conditions for the single phase PET to operate in various modes and regions are summarized in table 2.1.

Table 2.1: Regions and Modes of operation of Single Phase PET

Region	Condition on δ	Mode		Mode transition θ expression
		Mode 1	Mode 2	
1	$0 < \delta \leq \frac{1-m}{4}$	$0 < \theta \leq \pi$	N/A	N/A
2	$\frac{1-m}{4} < \delta \leq \frac{1}{4}$	$0 < \theta \leq \phi$ $\pi - \phi < \theta \leq \pi$	$\phi < \theta \leq \pi - \phi$	$\phi = \sin^{-1}\left(\frac{1-4\delta}{m}\right)$

2.2.1 Power transfer and currents in one switching period

The PET operates in two regions, Region 1 and Region 2, as established in the discussion above. Region 1 has been already examined in [34]. To obtain the power transfer and rms current expressions for Region 2, the analysis is first done for one switching period in Mode 1 and Mode 2. Then, the values found are integrated over a line frequency

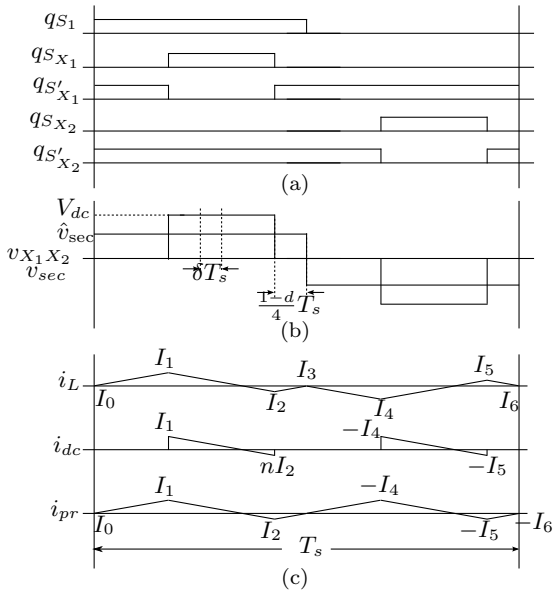


Figure 2.8: Mode 1 operation (a) Gate pulses (b) Transformer secondary and H-bridge voltages (c) Inductor, dc and primary side currents

cycle to get the power transferred over a fundamental cycle and the overall rms currents. The diagrams of gate pulses, voltages and currents for both Mode 1 and Mode 2 are shown in Fig. 2.8 and Fig. 2.9 respectively. It should be noted that for primary side current i_{pr} shown in Fig. 2.8(c) and Fig. 2.9(c), the turns ratio n has been assumed to be unity. Hence, the primary current isn't shown with the factor n, but that will be added later.

The H-bridge is modulated to generate voltage $v_{X_1X_2}$ which is a quasi square wave with average value zero over a switching time period T_s. In addition, the transformer secondary voltage v_{sec} is also a square wave during a switching time period T_s with zero average value (with the sinusoidal envelope being ignored). This causes the net volt-seconds across the inductor L to be zero. Thus, the average value of the inductor current over a switching period is equal to zero. This assumption is used to determine the starting value I_0 for the inductor current i_L both in Fig. 2.8(c) and Fig. 2.9(c). First, the current values at all the voltage transitions are determined in terms of I_0, keeping I_0 as an unknown variable. Then the average current is made zero, yielding the

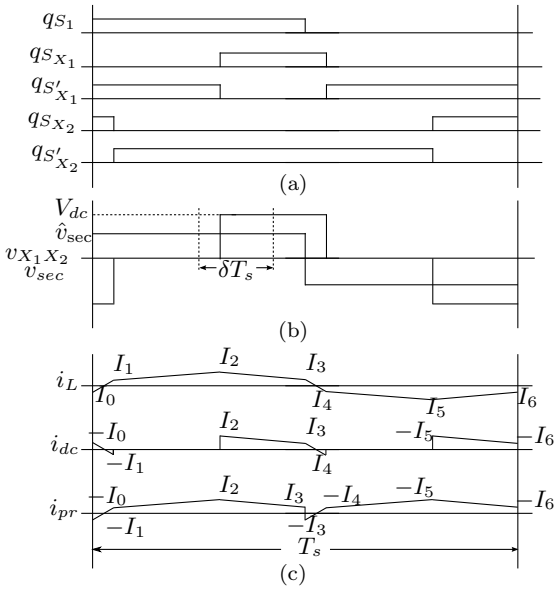


Figure 2.9: Mode 2 operation (a) Gate pulses (b) Transformer secondary and H-bridge voltages (c) Inductor, dc and primary side currents

value of I_0. The values I_0 for Mode 1 and Mode 2 are given as follows.

$$I_0 = 0 \qquad \text{(Mode 1)} \tag{2.13}$$

$$I_0 = -\frac{V_{dc}T_s}{L}\left(\delta - \frac{(1-d)}{4}\right) \qquad \text{(Mode 2)} \tag{2.14}$$

Using equations (2.13) and (2.14), the expressions for values of inductor current i_L can be computed at all voltage transitions during a switching period for both Mode 1 and Mode 2.

The average power transferred during a switching period is given in (2.15) and (2.16). Equation (2.3) and (2.6) have been used to substitute for d and V_{sec} in all the equations

from now on.

$$P_{\text{o,sw}} = \frac{\delta d V_{\text{sec}} V_{dc} T_s}{L} = \frac{\delta (m V_{dc} \sin(\theta) T_s)^2}{L} \quad \text{(Mode 1)} \tag{2.15}$$

$$\begin{aligned} P_{\text{o,sw}} &= \frac{V_{\text{sec}} V_{dc} T_s}{L} \left(\delta(1-2\delta) - \frac{(1-d)^2}{8} \right) \\ &= \frac{m V_{dc}^2 \sin(\theta) T_s}{L} \left(\delta(1-2\delta) - \frac{(1-m\sin(\theta))^2}{8} \right) \text{(Mode 2)} \end{aligned} \tag{2.16}$$

The inductor rms current is useful to know since it gives an idea of the losses that would occur in the inductor and hence useful in the design of the transformer. The value of this current over a switching period for both modes is given as follows.

$$I_{\text{L,sw}} = \frac{T_s V_{dc} m \sin(\theta)}{4\sqrt{6}L} \sqrt{2 + 96\delta^2 + m^2 - m^2\cos(2\theta) - 4m\sin(\theta)} \quad \text{(Mode 1)} \tag{2.17}$$

$$\begin{aligned} I_{\text{L,sw}} = &\frac{T_s V_{dc}}{4\sqrt{6}L} [m\sin(\theta)(2 - 24\delta + 96\delta^2 - 128\delta^3 + m^2 - 12\delta m^2 \\ &+ (-1+12\delta)m^2\cos(2\theta) + 4(-1+12\delta)m\sin(\theta))]^{\frac{1}{2}} \quad \text{(Mode 2)} \end{aligned} \tag{2.18}$$

The rms value of the dc current over a switching period is given as follows.

$$I_{\text{dcrms,sw}} = \frac{T_s V_{dc}}{4\sqrt{6}L} \sqrt{m^3 \sin(\theta)^3 (2 + 96\delta^2 + m^2 - m^2\cos(2\theta) - 4m\sin(\theta))} \text{ (Mode 1)} \tag{2.19}$$

$$\begin{aligned} I_{\text{dcrms,sw}} = &\frac{T_s V_{dc}}{4\sqrt{3}L} [m\sin(\theta)(-(-1+4\delta)^3 - 3(1-4\delta)^2 m\sin(\theta) + \\ &4(1 - 3\delta + 12\delta^2)m^2\sin(\theta)^2 - 3m^3\sin(\theta)^3 + m^4\sin(\theta)^4)]^{\frac{1}{2}} \text{ (Mode 2)} \end{aligned} \tag{2.20}$$

The average value of the dc link current $I_{\text{dcavg,sw}}$ over a switching period is simply calculated by diving the dc power in (2.15) and (2.16) by V_{dc}.

$$I_{\text{dcavg,sw}} = \frac{P_{\text{o,sw}}}{V_{dc}} \tag{2.21}$$

The rms value of the dc ripple current is then given as the difference between the rms

and average values of the dc current. This is given as follows.

$$I_{\text{rpl,sw}} = \frac{T_s V_{dc}}{4\sqrt{3}L}\sqrt{m^3\sin(\theta)^3(-1+m\sin(\theta))(-1-48\delta^2+m\sin(\theta))} \quad \text{(Mode 1)} \quad (2.22)$$

$$\begin{aligned} I_{\text{rpl,sw}} = &\frac{T_s V_{dc}}{16\sqrt{3}L}[m\sin(\theta)(-3m\sin(\theta)(2-16\delta+32\delta^2+m^2- \\ &m^2\cos(2\theta)-4m\sin(\theta))^2+16(-(-1+4\delta)^3-3(1-4\delta)^2 m\sin(\theta)+ \\ &4(1-3\delta+12\delta^2)m^2\sin(\theta)^2-3m^3\sin(\theta)^3+m^4\sin(\theta)^4))]^{\frac{1}{2}} \quad \text{(Mode 2)} \end{aligned} \quad (2.23)$$

2.2.2 Power transfer and currents in one line frequency period

The power and current expressions obtained in previous sections are for one switching period. They need to be integrated over one line frequency period to obtain the overall value of these quantities for one line frequency cycle. In general, for Region 2 operation of the PET, the following equation holds.

$$X_{\text{line-frequency}} = \frac{1}{\pi}\left(\int_0^{\phi} X_{\text{sw,Mode1}}(\theta)d\theta + \int_{\phi}^{\pi-\phi} X_{\text{sw,Mode2}}(\theta)d\theta + \int_{\pi-\phi}^{\pi} X_{\text{sw,Mode1}}(\theta)d\theta\right) \quad \text{(Region 2)} \quad (2.24)$$

where

$X_{\text{line-frequency}}$ = Average value of X over a line frequency cycle

$X_{\text{sw,Mode1}}$ = Average value of X over a switching period T_s in Mode 1

$X_{\text{sw,Mode2}}$ = Average value of X over a switching period T_s in Mode 2

ϕ is taken from (2.12).

The integration is first done without substituting the value of ϕ from (2.12). Once the integration is done and an expression is obtained, the value of ϕ is substituted in it to further simplify the obtained expression. In Region 1, the value of ϕ is $\frac{\pi}{2}$ and hence, the integration is done for only Mode 1 expressions from 0 to π. For the sake of completeness, the expressions for all the quantities in Region 1 [34] are also being given along with expressions for Region 2. The expression for power transfer over a line

frequency period is given below.

$$P_o = \frac{m^2 V_{dc}^2 \delta T_s}{2L} \quad \text{(Region 1)} \tag{2.25}$$

$$P_o = \frac{m V_{dc}^2 T_s}{48 L \pi}\left[-3(4(1-4\delta)^2+3m^2)\sqrt{1-\frac{(1-4\delta)^2}{m^2}} + m\left(m\cos\left(3\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)+ 6\left(\pi - 2(1-4\delta)\sin^{-1}\left(\frac{1-4\delta}{m}\right) + (1-4\delta)\sin\left(2\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right)\right] \quad \text{(Region 2)} \tag{2.26}$$

The expression for inductor rms current averaged over a line frequency period is given below.

$$I_L = \frac{m T_s V_{dc}}{24\sqrt{2\pi}L}\sqrt{-64m + 9m^2\pi + 12(\pi + 48\delta^2\pi)} \quad \text{(Region 1)} \tag{2.27}$$

$$I_L = \frac{T_s V_{dc}}{48 L\sqrt{\pi}}\left[m\left(\left(12(1-4\delta)(12+2(1-4\delta)^2+13m^2)\sqrt{1-\frac{(1-4\delta)^2}{m^2}} + m\left(36(4(1-4\delta)^2+m^2)\sin^{-1}\left(\frac{1-4\delta}{m}\right) - 8\left(16m + 6\pi(1-12\delta) + 9\sin\left(2\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right)\right)\right)\right]^{\frac{1}{2}} \quad \text{(Region 2)} \tag{2.28}$$

The expression for rms dc link current averaged over a line frequency period is given below.

$$I_{dc} = \frac{T_s V_{dc}}{24\sqrt{5\pi}L}\sqrt{m^3(80 + 3840\delta^2 + 64m^2 - 45m\pi)} \quad \text{(Region 1)} \tag{2.29}$$

$$I_{dc} = \frac{T_s V_{dc}}{48\sqrt{5\pi}L}\left[m\left(60(1-4\delta)(2(1-4\delta)^2+13m^2)\sqrt{1-\frac{(1-4\delta)^2}{m^2}} + 2m\left(32m(5+240\delta^2+4m^2) - 45(4(1-4\delta)^2+3m^2)\pi + 90(4(1-4\delta)^2+m^2)\sin^{-1}\left(\frac{1-4\delta}{m}\right)\right)\right)\right]^{\frac{1}{2}} \quad \text{(Region 2)} \tag{2.30}$$

Finally, the dc link ripple current over a line frequency period is given as follows.

$$I_{rpl} = \frac{T_s V_{dc}}{24\sqrt{5\pi}L}\sqrt{m^3(80+64m^2-45m\pi-120\delta^2(-32+9m\pi))} \quad \text{(Region 1)} \tag{2.31}$$

$$\begin{aligned} I_{rpl} =& \frac{T_s V_{dc}}{96\sqrt{10\pi}L}\Bigg[m\Bigg(12(8(-1+4\delta)^3(-9+8\delta(-3+10\delta))+2(1-4\delta)(413+ \\ & 8\delta(-109+130\delta))m^2+(437+300\delta)m^4)\sqrt{1-\frac{(1-4\delta)^2}{m^2}}+4m\Bigg(8m(80+ \\ & 64m^2-45m\pi+120\delta^2(32-9m\pi))-45(8(1-4\delta)^2(5+8\delta(-1+2\delta))- \\ & 4(-11+24\delta(1+2\delta))m^2+5m^4)\cos^{-1}\left(\frac{1-4\delta}{m}\right)\Bigg)\Bigg)\Bigg]^{\frac{1}{2}} \quad \text{(Region 2)} \end{aligned} \tag{2.32}$$

The inductor rms current I_L is the transformer secondary current. The rms current in each of the transformer primary windings is simply given as follows.

$$I_p = n\frac{I_L}{\sqrt{2}} \text{(Both regions)} \tag{2.33}$$

The rms voltage for primary and secondary windings are given (2.34) and (2.35) respectively.

$$V_p = \frac{mV_{dc}}{2n} \tag{2.34}$$

$$V_s = \sqrt{\frac{2m}{\pi}}V_{dc} \tag{2.35}$$

The net VA flowing through the transformer is given as follows.

$$P_t = \frac{1}{2}(V_p I_p + V_s I_L) \tag{2.36}$$

The quantities given in equations (2.25)-(2.36) are converted to per unit before plotting them. The base quantities used are as follows.

$$V_{\text{base}} = V_{dc} \tag{2.37}$$

$$I_{\text{base}} = \frac{V_{dc}T_s}{2\pi L} \tag{2.38}$$

$$P_{\text{base}} = V_{\text{base}} I_{\text{base}} \tag{2.39}$$

The analysis done so far only covers power transfer for positive values of δ. However, the power transfer and current expressions remain same for negative values of δ save for the reverse direction of power flow.

The plots of power transfer and rms currents are given in Fig. 2.10. The graphs shown are for average power transferred, dc ripple current and transformer utilization over a line frequency cycle, for different values of δ and m. In each of the three figures, δ varies along the x-axis, while different solid curves within the figure are for different values of m. A dashed curve is drawn in each of the three figures, which serves as the boundary between the Region 1 and Region 2 of the PET in each figure. In Fig. 2.10(a), it is immediately visible that the maximum power transfer for Region 2 is over four times that of maximum power transfer in Region 1. It is also seen that the highest dc ripple current in Region 2 is over three times the value of the highest ripple current in Region 1. The transformer utilization is calculated as the ratio of average power P_o and rms power P_t and plotted in Fig. 2.10(c). It gives an idea of how much the transformer has to be overdesigned for a certain operating point. It is clear from the graphs in the figure, that the utilization improves in Region 2, if only the highest values of the ratio are seen in each region. However, at maximum power level in Region 2, the transformer has nearly the same utilization as when it is operating at maximum power level in Region 1.

2.2.3 Soft switching

The current waveforms for Mode 1 and Mode 2 of the PET are shown in and Fig. 2.8(c) and Fig. 2.9(c) respectively. In both of these figures, the current flowing through the primary windings of the transformer when the primary side switches S_1 and S_2 are turning ON is designated I_0. The value of this current is given in (2.13) and (2.14) for Mode 1 and Mode 2 respectively. In Mode 1, the value of this current is zero, while in Mode 2, it is a non-zero value. Thus in Mode 1, Zero Current Switching (ZCS) of S_1 and S_2 is achieved, while in Mode 2, these switches are hard switched. In Region 2, the PET operates both in Mode 1 and Mode 2. Therefore, ZCS is achieved in part of the PET operation in a line frequency cycle in Region 2 for primary side switches.

The inductor current when the H-bridge switches S_{X_1}, S'_{X_1}, S_{X_2} and S'_{X_2} are turned ON are designated as I_1, I_2, I_4 and I_5 respectively in Mode 1, as shown in Fig. 2.8(c).

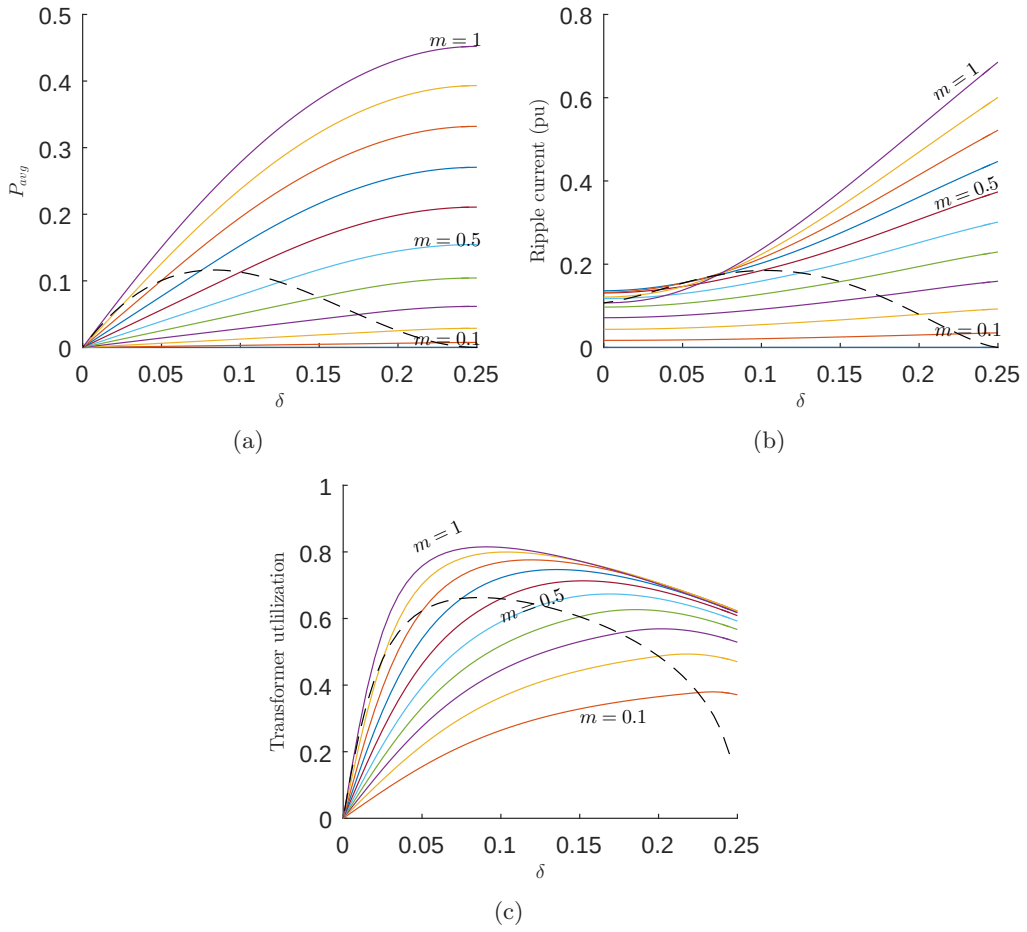


Figure 2.10: Single phase PET characteristics (a) Average power vs δ (b) DC ripple current vs δ (c) Transformer utilization vs δ

These currents are designated as $I_{\mathrm{X_1ON,Mode1}}$, $I_{\mathrm{X_1'ON,Mode1}}$, $I_{\mathrm{X_2ON,Mode1}}$ and $I_{\mathrm{X_2'ON,Mode1}}$ respectively from now on. The expressions for these currents are given below.

$$I_{\mathrm{X_1ON,Mode1}} = \frac{T_s V_{dc} m \sin(\theta)}{4L}(1 + 4\delta - m\sin(\theta)) \tag{2.40}$$

$$I_{\mathrm{X_1'ON,Mode1}} = \frac{T_s V_{dc} m \sin(\theta)}{4L}(-1 + 4\delta + m\sin(\theta)) \tag{2.41}$$

$$I_{\mathrm{X_2ON,Mode1}} = -\, I_{\mathrm{X_1ON,Mode1}} \tag{2.42}$$

$$I_{\mathrm{X_2'ON,Mode1}} = -\, I_{\mathrm{X_1'ON,Mode1}} \tag{2.43}$$

Similarly, the inductor current when the H-bridge switches S_{X_1}, S'_{X_1}, S_{X_2} and S'_{X_2} are turned ON in Mode 2, are obtained as follows.

$$I_{\mathrm{X_1ON,Mode2}} = I_{\mathrm{X_1ON,Mode1}} \tag{2.44}$$

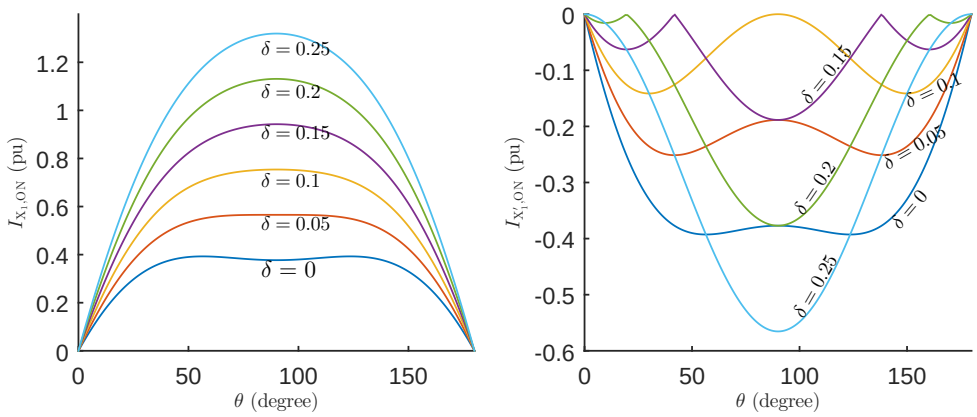
$$I_{\mathrm{X_1'ON,Mode2}} = -I_{\mathrm{X_1'ON,Mode1}} \tag{2.45}$$

$$I_{\mathrm{X_2ON,Mode2}} = -I_{\mathrm{X_1ON,Mode2}} \tag{2.46}$$

$$I_{\mathrm{X_2'ON,Mode1}} = -I_{\mathrm{X_1'ON,Mode2}} \tag{2.47}$$

Combining the operating conditions in table 2.1, with equations (2.40) -(2.44), the direction of current can be determined when each device is turned ON or OFF. If the current direction is such that current flows through a device's anti-parallel diode when it is turning ON, it will undergo Zero Voltage Switching (ZVS). It is found that this condition is true for all four devices of the H-bridge in all modes and regions of the PET. Hence, Zero Voltage Switching (ZVS) is achieved for the H-bridge switches across the entire range of operation of the PET. The currents $I_{\mathrm{X_1,ON}}$ and $I_{\mathrm{X_1',ON}}$ are plotted against θ, for modulation index $m = 0.4$ and for various values of δ in Fig. 2.11. These plots demonstrate how the values of the turn ON currents vary with the angle θ for a fixed δ and also for different values of δ, in all modes and regions. The plots for other values of modulation indexes will be similar in shape.

It should be noted that the plots shown in Fig .2.11 are for $0 \leq \delta \leq \frac{1}{4}$. The plots for $-\frac{1}{4} \leq \delta \leq 0$ are going to be similar to those shown in Fig .2.11 due to symmetrical nature of the circuit. The turn ON current plots of S_{X_1} for negative values of δ will look same as the turn ON plots of S'_{X_1} for positive values of δ i.e. Fig. 2.11(b), but with



(a) (b)

Figure 2.11: Turn ON currents for secondary side H-bridge at modulation index $m = 0.4$ (a) $I_{\mathrm{X_1,ON}}$ (b) $I_{\mathrm{X_1',ON}}$

the sign flipped, i.e. the plots will be lying in the first quadrant instead of the fourth quadrant. Similarly, the turn ON current plots of S'_{X_1} for negative values of δ will look same as the turn ON plots of S_{X_1} for positive values of δ i.e. Fig. 2.11(a), but with the sign flipped, i.e. the plots will be lying in the fourth quadrant instead of the first quadrant. This means turn ON ZVS is achieved for S_{X_1} and S'_{X_1} for negative δ as well. Mathematically, the expressions (in these expressions, *delta* will be substituted as it is, with its sign) for turn ON currents for these switches for negative values of δ are given below.

$$I_{\mathrm{X_1ON,Mode1,-}} = I_{\mathrm{X_1ON,Mode1}} \tag{2.48}$$

$$I_{\mathrm{X_1'ON,Mode1,-}} = I_{\mathrm{X_1'ON,Mode1}} \tag{2.49}$$

$$I_{\mathrm{X_1ON,Mode2,-}} = -I_{\mathrm{X_1ON,Mode1,-}} \tag{2.50}$$

$$I_{\mathrm{X_1'ON,Mode2,-}} = I_{\mathrm{X_1'ON,Mode1,-}} \tag{2.51}$$

It is observed from (2.50)that for negative values of δ, turn ON current expression of S_{X_1} gets flipped in sign when PET goes to Mode 2, as opposed to retaining the same expression for positive values of δ. Similarly, it is seen in (2.51) that turn ON current for S'_{X_1} retains its expression when PET goes to Mode 2 for negative values of δ, as opposed to getting flipped in sign for positive values of δ when Mode 2 occurs. Similarly

the other two switches of the H-bridge will also have turn ON ZVS for negative values of δ.

2.2.4 Harmonic compensation

A simulation of the single phase PET shows that especially at higher power levels, the primary side ac current has significant 3^{rd} harmonic of the line frequency. In order to further understand this, the low frequency value of the primary side current (i.e. neglecting switching harmonics) should be looked at. The first step is to calculate the average value of the primary side current in one half of a switching period for both modes. This is done by piecewise integration of the i_{pr} current waveforms shown in Fig. 2.8(c) and Fig. 2.9(c), over one half of a switching period T_s. The values obtained are as follows.

$$\begin{aligned} i_{\text{pr,avg}} =& \frac{\delta T_s V_{dc}}{L} m \sin(\theta) \quad \text{(Mode 1)} \\ i_{\text{pr,avg}} =& -\frac{T_s V_{dc}}{8L}[(1-4\delta)^2 + m\sin(\theta)(-2+m\sin(\theta))] \quad \text{(Mode 2)} \end{aligned} \tag{2.52}$$

where $0 < \theta \leq \pi$ The equation (2.52) gives the value of primary side current as a function of m, δ and θ, as θ varies between 0 and π. For θ varying between π to 2π, the current waveform attains same values but is opposite in sign. It is clear from equation (2.52), that in mode 1, the current is strictly sinusoidal, whereas going in mode 2, the waveform deviates from sinusoidal shape. Thus, in region 1, where PET operates only in mode 1, the current should be sinusoidal and in phase with the ac voltage (thus proving the unity power factor operation). In region 2, the current deviates from sinusoidal shape as it enters mode 2, which would explain the third harmonic in the primary side current. The amplitude of the third harmonic current in the primary side current is found by doing Fourier analysis. It is given as follows.

$$I_3 = \frac{m^2 T_s V_{dc}}{15L\pi}\left(1-\left(\frac{1-4\delta}{m}\right)^2\right)^{\frac{5}{2}} \tag{2.53}$$

Other harmonic coefficients can also be obtained in a similar fashion. A harmonic factor k_{I3} has been defined as the ratio of harmonic component to the fundamental component

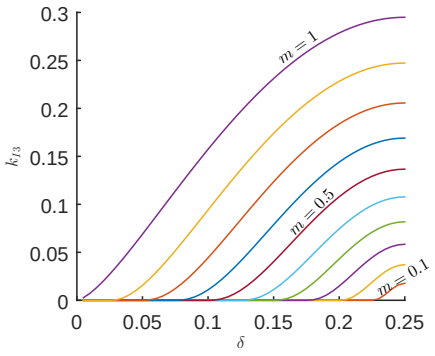


Figure 2.12: Third harmonic factor k_{I3} plots

for a given order. For the third order harmonic, this coefficient is given below.

$$k_{I3} = \frac{I_3}{I_1} \tag{2.54}$$

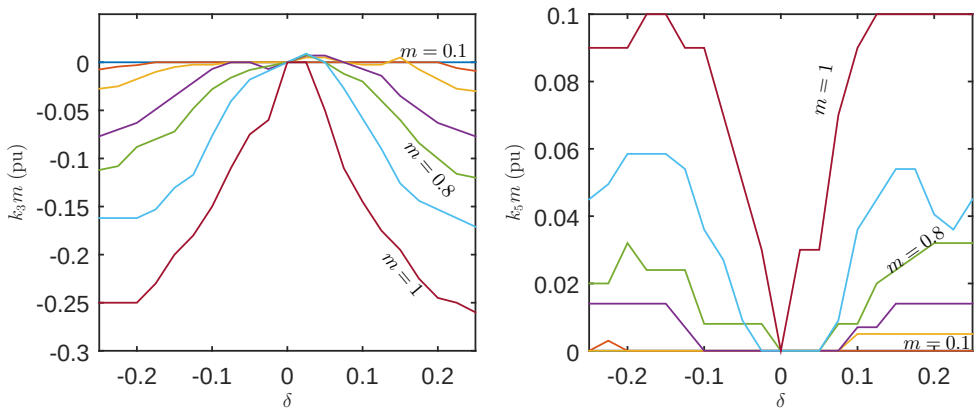
This factor has been plotted for various values of δ and m in Fig. 2.12. In order to reduce this 3^{rd} harmonic current component, a 3^{rd} harmonic component is injected in the modulation signal of the secondary side H-bridge, as seen in the equation below.

$$MI_{\text{comp},3} = m\sin(\theta) + k_3 m\sin(3\theta) \tag{2.55}$$

It is however observed that upon introducing this 3^{rd} harmonic component in the modulation signal, a 5^{th} harmonic component starts to show up in the current. To suppress the 5^{th} harmonic in current, a fifth harmonic component is introduced in the modulation signal of the secondary side H-bridge. The modulation signal then takes the following form.

$$MI_{\text{comp},3,5} = m\sin(\theta) + k_3 m\sin(3\theta) + k_5 m\sin(5\theta) \tag{2.56}$$

It is observed that introducing 3^{rd} and 5^{th} harmonic components in the H-bridge voltage causes a 7^{th} harmonic component to appear in the primary side ac current. However, it is not significant and therefore ignored. In order to estimate the optimum values of k_3 and k_5 at various values of m and δ, multiple simulations were done. Then the values of k_3 and k_5 were chosen from those simulations where the 3^{rd} and 5^{th} harmonic were



(a) (b)

Figure 2.13: Harmonic compensation coefficients' (multiplied by the modulation index) plots (a) k_3m (b) k_5m

found to be least among all the test values. The values of k_3m and k_5m obtained from these simulations have been plotted in Fig. 2.13. It is observed from these graphs that the compensation is needed only in Region 2, since the values of k_3 and k_5 are zero in Region 1. This agrees with the discussion done earlier in this subsection. In addition, the plots in Fig. 2.13(a) appear similar to those in Fig. 2.12, which indicate a relation between the harmonic current amplitude and the compensation voltage to suppress the harmonic.

The impact of using harmonic compensation is that turn ON ZVS is lost for switches S'_{X_1} and S_{X_2} for some range of operation for a given value of modulation index m and phase shift parameter δ. In addition, the power transferred will be lower than the theoretical values obtained in previous section 2.2.2. It should be noted that in order to obtain the exact optimum values for k_3 and k_5 and even higher order harmonic compensation coefficients and the exact magnitude of their impact on power transfer and turn ON ZVS, a complete harmonic analysis of the current waveform is needed which is out of scope of this thesis and has been left for future work.

Table 2.2: Circuit Parameters for Single phase PET simulation and experiments

Parameter	Value
DC link voltage (V_{dc})	80V
Modulation index (m)	0.5, 0.7, 0.8, 0.9
AC voltage frequency	60 Hz
Switching period (T_s)	200μs
δ	[-0.25,0.25] (in steps of 0.05)
Transformer turns ratio	1:1
Secondary side inductance (L)	480 μH

2.3 Simulation and Experimental results

The single phase PET is simulated using Matlab Simulink and Plecs blockset to study its operation. In addition, a laboratory hardware prototype was also built to obtain experimental results. The parameters of the circuit used are given in table 2.2.

Simulation results for power flow through the PET from ac to dc side are given in Fig. 2.14. An LCR filter with $L = 820\mu$H, $C = 20\mu$F and $R = 18\Omega$ was used in these simulations, to filter out switching frequency components from the ac current. These waveforms are taken for $m = 0.9$ and $\delta = 0.225$. It is immediately observed that the ac current is nearly in phase (some phase difference present due to filter) with the ac voltage, demonstrating unity power factor. The current waveforms in Fig. 2.14(a) are without any harmonic compensation. Upon applying harmonic compensation, the current waveforms obtained are shown in Fig. 2.14(b), in which the ac current appears more sinusoidal in nature compared to that without compensation. To further illustrate this, frequency spectra of the ac current with and without harmonic compensation are shown in Fig. 2.14(c), where the third harmonic is not present in when compensation is used. It is also seen that the fundamental component of the current reduces, which is indicative of the lower power transfer for the same value of δ and m. All of these corresponding waveforms and frequency spectrum are also shown for dc to ac power flow in Fig. 2.15.

The experimental results for ac and dc currents with the same settings ($m = 0.9$, $\delta = 0.225$) are shown in Fig. 2.16, for power flow from ac to dc side. The experimental results are similar to the simulation results with regards to unity power factor operation and ac current harmonic content reduction due to harmonic compensation. It should

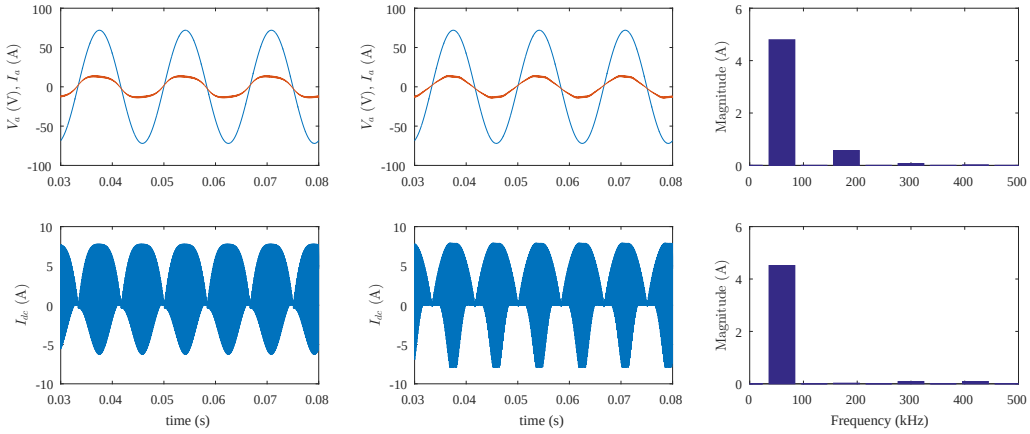


Figure 2.14: Simulation results for power flow from AC to DC side, for single phase PET (a) Without harmonic compensation (AC voltage and filtered ac current(zoomed by factor of 3) (top), DC link current(bottom)) (b) With harmonic compensation (AC voltage and filtered ac current(zoomed by factor of 3) (top), DC link current(bottom)) (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

be noted that due to leakage energy commutation losses on the primary side of the transformer, device drops and winding resistances, the current in experimental results doesn't match the magnitude of that in simulation results. Finally, the experimental results for ac and dc currents for power flow from dc to ac side are shown in Fig. 2.17. These also demonstrate unity power factor operation and also show harmonic content reduction when harmonic compensation is used.

In order to demonstrate that the power flow analysis in section 2.2.2 translates to the actual system, simulations and experiments were performed for the single phase PET at several values of m and δ, as given in table 2.2. The plots are given in Fig. 2.18, with each plot showing analytical, simulated and experimental results for one value modulation index m for various values of δ. It is observed that the various curves in each figure show a similar trend, which shows that the analytical expressions translate to actual system within some margin of error. There are a few differences to be noted however. The first difference is that the simulation values themselves don't exactly match the analytical values at higher values of δ, which accredited to the harmonic

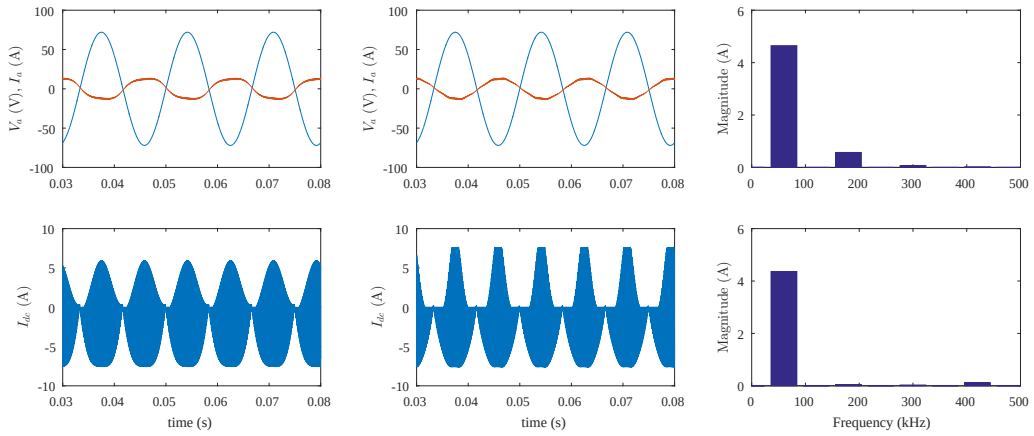


Figure 2.15: Simulation results for power flow from DC to AC side, for single phase PET (a) Without harmonic compensation (AC voltage and filtered ac current(zoomed by factor of 3) (top), DC link current(bottom)) (b) With harmonic compensation (AC voltage and filtered ac current(zoomed by factor of 3) (top), DC link current(bottom)) (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

compensation as the PET enters Region 2 of operation. Then, the ac and dc power values obtained through experiments do not match each other exactly, due to system losses. They also do not match the simulation results due to non-idealities such as device drops, leakage commutation on primary side of transformer and winding losses. It should be noted that for positive value sof δ, where power is transferred from ac to dc side, the ac power input is more than the dc power output (barring for very low values of δ where power transfer is not measurable accurately). The reverse is true for negative values of δ.

The turn ON ZVS of secondary side H-bridge is demonstrated by showing the inductor current and the voltage across the switches as they turn ON. Simulation results are shown in Fig. 2.19 and experimental results are shown in Fig. 2.20. A dead time of 2μs is used for the upper and lower switches of each phase leg of the secondary side H-bridge both in experiments and simulations. It is seen in each figure, that the voltage across a switch is negative when its gate pulse goes high, indicating that the diode is conducting when the device is turned ON. This demonstrates turn ON ZVS for all

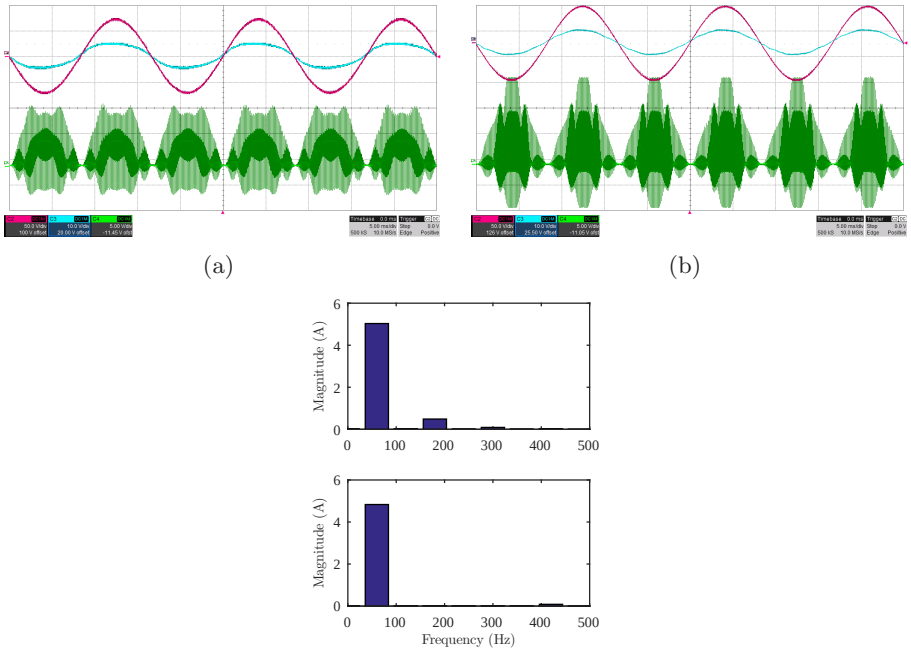


Figure 2.16: Experimental results for power flow from AC to DC side, for single phase PET (a) Without harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (b) With harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

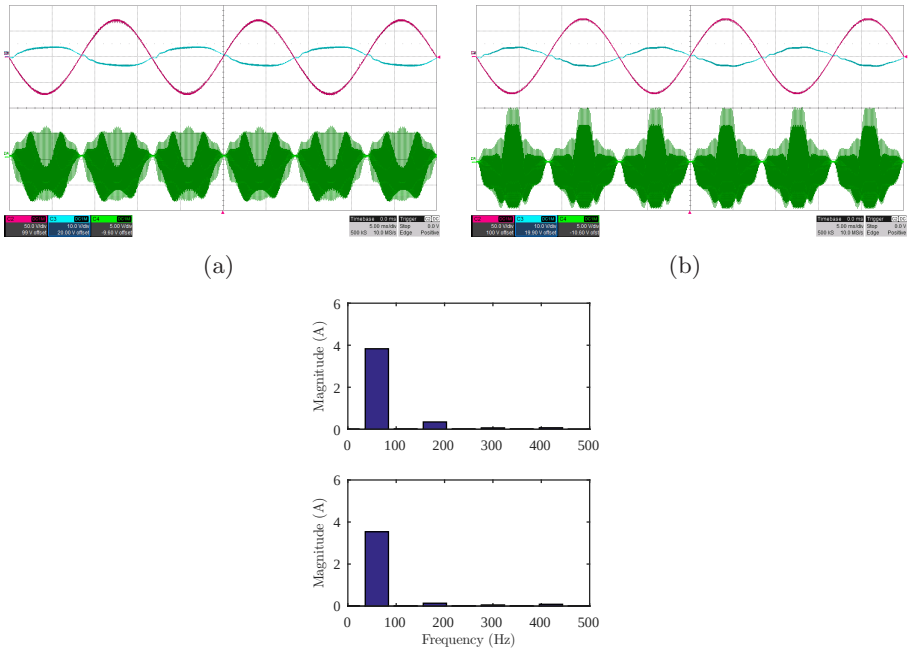


Figure 2.17: Experimental results for power flow from DC to AC side, for single phase PET (a) Without harmonic compensation: AC voltage and filtered AC current (top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (b) With harmonic compensation: AC voltage and filtered AC current(top) [50 V/div, 10 A/div], DC link current(bottom) [5 A/div] (c) AC current Frequency spectra, without compensation (top) and with compensation (bottom)

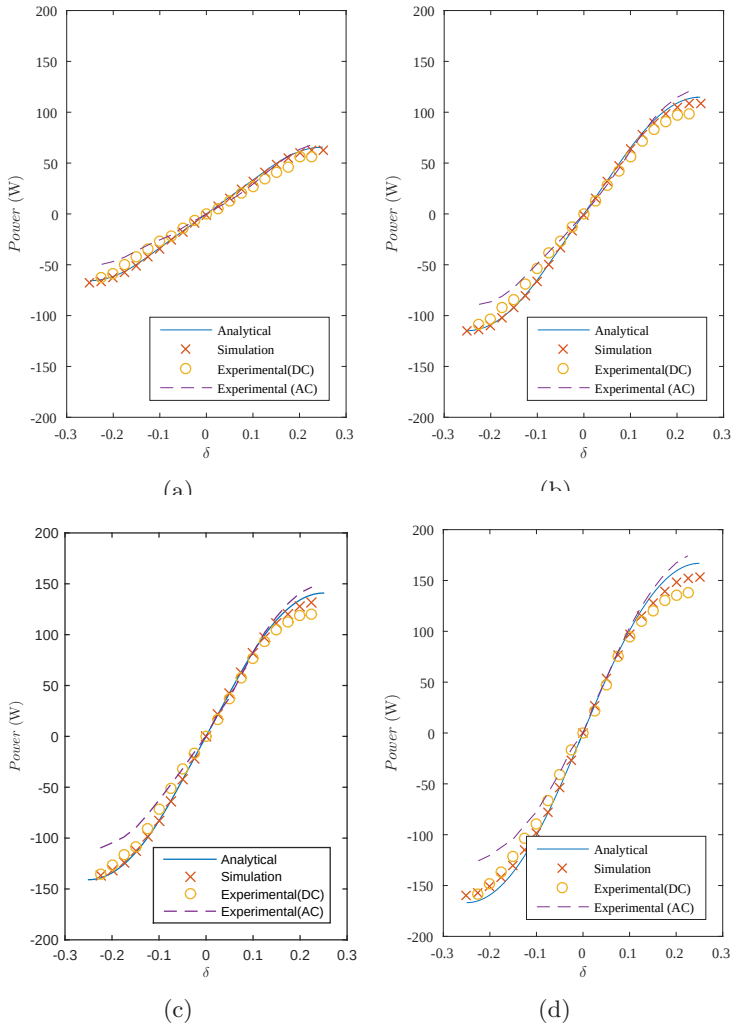


Figure 2.18: Comparison of analytical, simulation and experimental results for power transfer in single phase PET (a) $m = 0.5$ (b) $m = 0.7$ (c) $m = 0.8$ (d) $m = 0.9$

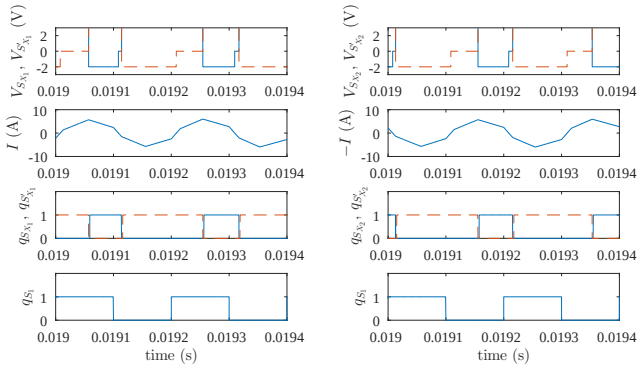
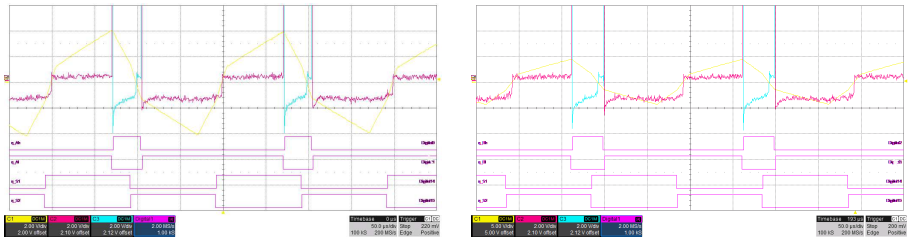


Figure 2.19: Simulation results for turn ON ZVS demonstration on secondary side (a) Voltages across HB switches S_{X_1} and S'_{X_1} (top figure), current through the inductor L (second figure from top), gate pulses for switches S_{X_1} and S'_{X_1} (third figure from top) and gate pulse for primary side switch S_1 (bottom figure) (b) Voltages across HB switches S_{X_2} and S'_{X_2} (top figure), negative of current through the inductor L (second figure from top), gate pulses for switches S_{X_2} and S'_{X_2} (third figure from top) and gate pulse for primary side switch S_1 (bottom figure)

devices of H-bridge.

2.4 Conclusion

In this chapter, a two switch power electronic transformer topology was analyzed for bidirectional power conversion from single phase ac to dc. The power transferred, transformer utilization and ripple current in the dc link were analytically determined, in addition to the soft switching of the power switches in the topology for various modes of operation. It was found that the operation in Region 2 allows more power transfer through the PET than it can be done in Region 1, although it results in loss of ZCS for primary side switches and requires harmonic compensation to get rid of low order harmonics in the ac current. Using simulation and experimental results, these findings were validated within limits of experimental error.



(a) (b)

Figure 2.20: Experimental results for turn ON ZVS demonstration on secondary side (a) Voltages across HB switches S_{X_1} and S'_{X_1} (Channels 2 and 3)[2 V/div], current through the inductor L (Channel 1) [2 A/div], gate pulses for switches S_{X_1} and S'_{X_1} (third figure from top) and gate pulse for primary side switch S_1 (bottom figure) (b) Voltages across HB switches S_{X_2} and S'_{X_2} (Channels 2 and 3)[2 V/div], negative of current through the inductor L (Channel 1) [2 A/div], gate pulses for switches S_{X_2} and S'_{X_2} (third figure from top) and gate pulse for primary side switch S_1 (bottom figure)

Chapter 3

Three phase AC-DC reduced switch Power Electronic Transformer

Integration of renewable energy systems into the grid often requires a transformer due to the voltage level difference between the grid and the renewable energy system. In a wind turbine, the voltage generated is 690 V line-line. In order to step up the voltage, power is transmitted to the ground level from the nacelle, where it is stepped up using a line frequency transformer. In some cases, the transformer is placed in the nacelle itself to eliminate the wires and the losses occurring in them [2]. However, it increases the bulk of the nacelle. A power electronic transformer (PET) would be suitable to place in the nacelle due to its smaller size than a line-frequency transformer. In this chapter, a three phase reduced switch count PET is analyzed. It is a variation of the single phase PET in the previous chapter.

The PET analyzed in this chapter has similar features as the single phase variant. It is a push-pull based topology with dual active bridge principle for power transfer. The main features of this topology are reduced switches on transformer primary side, single stage power conversion, unity power factor in open loop operation and soft switching. The three phase PET operates in a total of five modes when operating it using the proposed control strategy. Out of these five modes, one mode called the inner mode

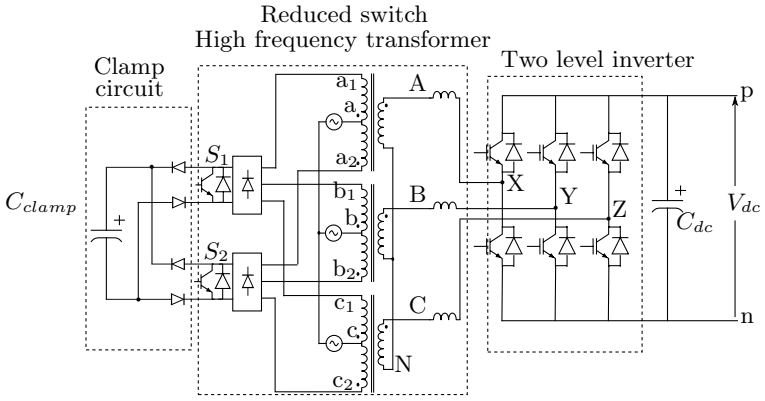


Figure 3.1: Three phase reduced switch PET

has been analyzed in [35]. The other modes are analyzed in this chapter and it will be shown that operating the PET in these modes allows much more power transfer than the inner mode.

3.1 Topology description and modulation technique

The three phase reduced switch PET circuit diagram is shown in Fig. 3.1. It consists of three three-winding transformers with turns ratio $1 : n$, one transformer for each of the three phases. The two primary windings of each transformer are connected to the respective ac source on one terminal. The other terminal of each primary winding goes to a three phase diode rectifier. The switches connected at the dc side of the diode rectifiers are labeled S_1 and S_2. The transformer terminals a_1, b_1 and c_1 are connected to the diode rectifier which is connected to S_1 and the transformer terminals a_2, b_2 and c_2 are connected to the diode rectifier which is connected to S_2. A common clamp circuit consisting of diodes and a clamp capacitor and resistor is connected to the two switches S_1 and S_2.

The total leakage inductance is lumped on the secondary side of the transformer and labeled L for each phase. The transformer secondary terminals behind these inductances are labeled A, B and C. A two-level Voltage Source Inverter (VSI) is connected to the secondary windings of the transformers. The three terminals of the VSI connected to transformer secondaries are labeled X, Y and Z. The VSI is connected to a DC link

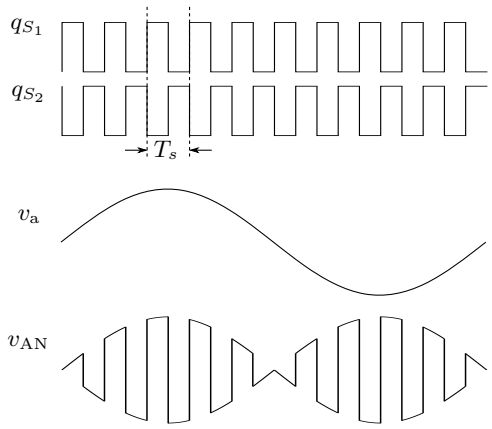


Figure 3.2: Primary side switch gate pulses, transformer primary and secondary voltage

with a capacitor C_{dc}. The positive and negative terminals of the dc link are labeled p and n respectively. The voltage across the dc link is V_{dc}.

3.1.1 Primary side switch modulation

The primary windings of each of the transformers are connected to a phase of a three phase line frequency ac grid, as seen in Fig. 3.1. Based on the dot convention shown in the figure, when the primary side switch S_1 is turned ON, with S_2 being OFF, the winding terminals labeled a_1, b_1 and c_1 are connected by S_1 through the diode rectifier and they form a neutral point. Then, the voltages appearing at the secondary terminals A, B and C are equal (with the turns ratio applied) in magnitude and polarity to the primary side voltages. Similarly, when the switch S_2 is turned ON, the primary winding terminals a_2, b_2 and c_2 are connected by S_2 through the diode rectifier and they form a neutral point. Then, the voltages at A, B and C are equal to negative of the primary side voltages (with the turns ratio applied). In the modulation scheme covered in this chapter, the switches S_1 and S_2 are switched in a complimentary fashion, with a 50% duty ratio, over a switching time period T_s. This creates a secondary voltage that is a square wave in a switching period and has a sinusoidal envelope of line frequency. The switching pulses of q_{S_1} and q_{S_2} of S_1 and S_2 respectively and the secondary and primary voltage are shown in Fig. 3.2.

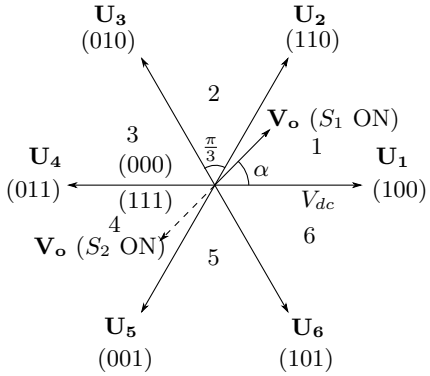


Figure 3.3: Space vectors of a two level VSI

3.1.2 Secondary side VSI modulation

The secondary side VSI is modulated to generate phase voltages v_{XN}, v_{YN} and v_{ZN} which have the same average value as the square waves v_{AN}, v_{BN} and v_{CN} respectively, over one half of switching period T_s. In order to achieve this, space vector modulation is used. The space vector diagram of a two level VSI is shown in Fig. 3.3. There are six active vectors labeled $\mathbf{U_1}$ to $\mathbf{U_6}$, each of magnitude V_{dc}. There are two zero vectors, (000) and (111) where all the phases are connected to the positive dc bus terminal and negative dc bus terminals respectively. The output voltage vector $\mathbf{V_o}$ is the vector formed by the grid secondary voltages and this is the vector to be synthesized by the VSI. In Fig. 3.3, $\mathbf{V_o}$ is in sector 1 when primary side switch S_1 is ON. When the switch S_2 is ON, the secondary voltage polarity is reversed and the voltage vector therefore is rotated by 180° and gets located in sector 4. By utilizing the active vectors in the sector where $\mathbf{V_o}$ is located and the zero vectors, the desired voltage is generated by the VSI. The shape of the voltage waveforms generated by the VSI will be now discussed.

The pole voltages (voltage wrt DC bus negative terminal n) and output phase voltages (voltage wrt neutral point N) are related as given in equation below.

$$v_{\mathrm{kN}} = v_{\mathrm{kn}} - \frac{1}{3}\sum_{j=X,Y,Z} v_{jn} \qquad (\mathrm{k} = \mathrm{X}, \mathrm{Y}, \mathrm{Z}) \tag{3.1}$$

The voltages v_{Xn}, v_{Yn} and v_{Zn} and v_{XN}, v_{YN} and v_{ZN} are given in Table 3.1 for the active and zero space vectors of the VSI. In the modulation scheme used in this chapter,

Table 3.1: Pole and phase voltages for different space vectors of a VSI

Space vector	Pole voltages			Phase voltages		
	v_{Xn}	v_{Yn}	v_{Zn}	v_{XN}	v_{YN}	v_{ZN}
$\mathbf{U_1}$	V_{dc}	0	0	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$
$\mathbf{U_2}$	V_{dc}	V_{dc}	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$
$\mathbf{U_3}$	0	V_{dc}	0	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$-\frac{V_{dc}}{3}$
$\mathbf{U_4}$	0	V_{dc}	V_{dc}	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$
$\mathbf{U_5}$	0	0	V_{dc}	$-\frac{V_{dc}}{3}$	$-\frac{V_{dc}}{3}$	$\frac{2V_{dc}}{3}$
$\mathbf{U_6}$	V_{dc}	V_{dc}	0	$\frac{V_{dc}}{3}$	$-\frac{2V_{dc}}{3}$	$\frac{V_{dc}}{3}$
$\mathbf{U_0}$	0	0	0	0	0	0
$\mathbf{U_7}$	V_{dc}	V_{dc}	V_{dc}	0	0	0

only the $\mathbf{U_0}$ zero vector is used, while $\mathbf{U_7}$ is not used. The benefit of using only $\mathbf{U_0}$ is that one phase can be clamped to zero for one half of a switching period, leading to fewer switching transitions. In sector 1, the active vectors $\mathbf{U_1}$ and $\mathbf{U_2}$ along with the zero vector $\mathbf{U_0}$ are used to synthesize the output voltage vector $\mathbf{V_o}$. In Fig. 3.3, the output voltage vector $\mathbf{V_o}$ makes an angle α degrees from the space vector $\mathbf{U_1}$. The duty ratios of vectors $\mathbf{U_1}$, $\mathbf{U_2}$ and $\mathbf{U_0}$ are d_1, d_2 and d_z respectively. These duty ratios are defined as follows.

$$\begin{aligned} d_1 &= \sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right) \\ d_2 &= \sqrt{3}m\sin(\alpha) \\ d_z &= 1-d_1-d_2 = 1-\sqrt{3}m\cos(\alpha-\frac{\pi}{6}) \end{aligned} \tag{3.2}$$

where

$$\begin{aligned} m &= \frac{1.5nV_{\mathrm{grid}}}{V_{dc}} \\ 0 \le m &\le \frac{1}{\sqrt{3}} \end{aligned} \tag{3.3}$$

V_{grid} is the peak phase voltage of the primary side ac grid.

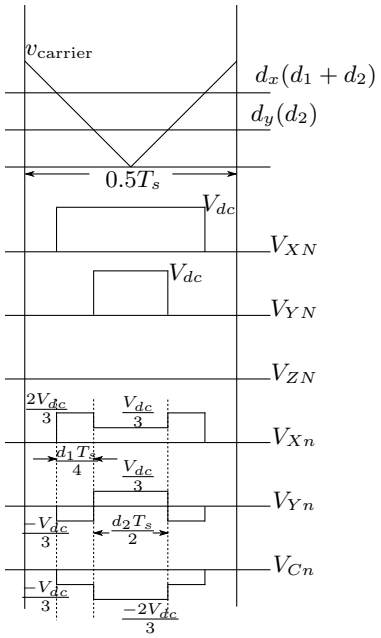


Figure 3.4: VSI pole and phase voltages in sector 1

The pole voltages and phase voltages generated by the VSI in sector 1 are shown in Fig. 3.4. The transformer secondary voltage v_{AN} and the VSI phase voltage v_{XN} are shown in Fig. 3.5(b) for one switching period T_s, when $\mathbf{V_o}$ is in sector 1 with S_1 turned ON. Similarly, the modulation is done in all other sectors and the appropriate voltages are generated.

3.2 Analysis of power transfer, rms currents and soft switching

The transformer secondary and VSI phase voltage waveforms shown in Fig. 3.5(b) don't have any phase shift between them. If a phase shift δT_s is introduced, power transfer will occur between the two voltages, for each of the three phases. The limits on δ are same as those in single phase PET, as given below.

$$-\frac{1}{4} \leq \delta \leq \frac{1}{4} \tag{3.4}$$

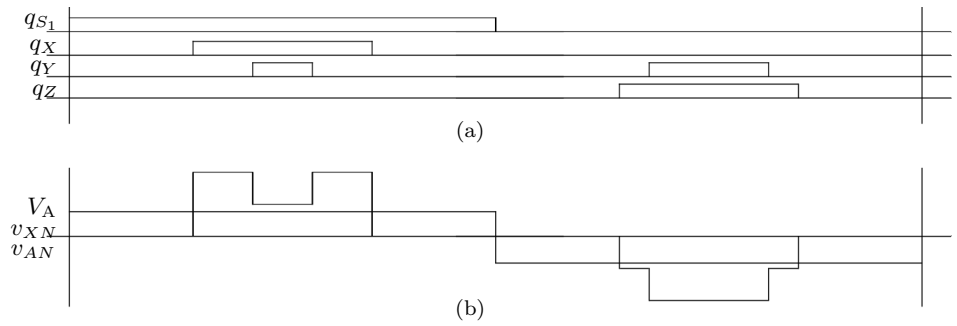


Figure 3.5: Transformer secondary and VSI waveform for phase A, with $\mathbf{V_o}$ in sector 1 (when S_1 is ON)

If only positive values of δ are considered, there are five different modes of operation of the PET based on the relative positions of the transformer secondary voltages and VSI phase voltages. These five modes are called Mode 1 through Mode 5 from now on. They are illustrated for phase A in Fig. 3.6. It is seen that in Mode 1, the voltage pulse generated by the VSI is enclosed within the corresponding half switching period and is therefore also known as inner mode. The other four modes don't have this property and they are also called outer modes.

The condition on δ for all five modes are given below.

$$
\begin{aligned}
0 \leq \delta < \frac{d_z}{4} &\qquad \text{(Mode 1)} \\
\frac{d_z}{4} \leq \delta < \frac{1-d_1}{4} \text{ and } \frac{d_z}{4} \leq \delta < \frac{1-d_2}{4} &\qquad \text{(Mode 2)} \\
\frac{1-d_1}{4} \leq \delta < \frac{1-d_2}{4} &\qquad \text{(Mode 3)} \\
\frac{1-d_2}{4} \leq \delta < \frac{1-d_1}{4} &\qquad \text{(Mode 4)} \\
\frac{1-d_1}{4} \leq \delta < \frac{1}{4} \text{ and } \frac{1-d_2}{4} \leq \delta < \frac{1}{4} &\qquad \text{(Mode 5)}
\end{aligned}
\tag{3.5}
$$

It should be noted that the conditions for different modes seem contradictory, but they actually hold true for different values of the angle α made by $\mathbf{V_o}$ with the VSI space vector at the start of the current sector. The conditions on δ for operation in different

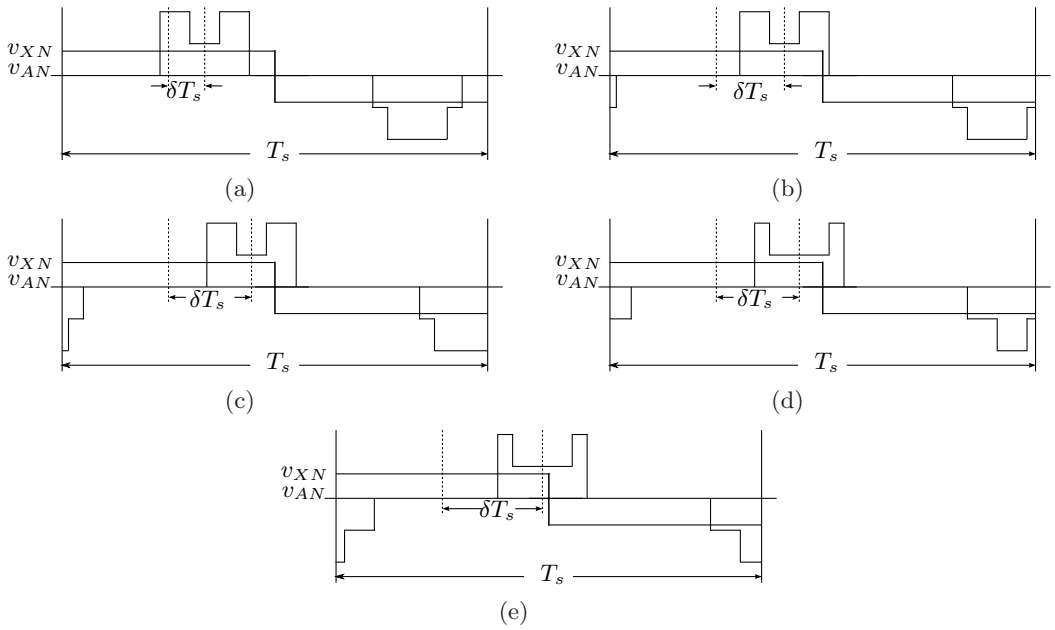


Figure 3.6: Phase A voltage waveforms in three phase PET modes ($\mathbf{V_o}$ in sector 1 with S_1 ON) (a) Mode 1 (b) Mode 2 (c) Mode 3 (d) Mode 4 (e) Mode 5

modes are rewritten as follows.

$$
\begin{aligned}
1 \geq 1 - 4\delta > d_1 + d_2 \qquad & \text{(Mode 1)} \\
d_1 + d_2 > 1 - 4\delta \geq d_1 \text{ and} & \\
d_1 + d_2 > 1 - 4\delta \geq d_2 \qquad & \text{(Mode 2)} \\
d_1 \geq 1 - 4\delta > d_2 \qquad & \text{(Mode 3)} \\
d_2 \geq 1 - 4\delta > d_1 \qquad & \text{(Mode 4)} \\
d_1 \geq 1 - 4\delta > 0 \text{ and} & \\
d_2 \geq 1 - 4\delta > 0 \qquad & \text{(Mode 5)} \qquad (3.6)
\end{aligned}
$$

Substituting the values of d_1 and d_2 from (3.2), we get the following set of equations.

$$
\begin{aligned}
1 \geq 1-4\delta > \sqrt{3}m\cos\left(\alpha-\frac{\pi}{6}\right) \qquad & \text{(Mode 1)} \\
\sqrt{3}m\cos\left(\alpha-\frac{\pi}{6}\right) \geq 1-4\delta > \sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right) \text{ and} & \\
\sqrt{3}m\cos\left(\alpha-\frac{\pi}{6}\right) \geq 1-4\delta > \sqrt{3}m\sin(\alpha) \qquad & \text{(Mode 2)} \\
\sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right) \geq 1-4\delta > \sqrt{3}m\sin(\alpha) \qquad & \text{(Mode 3)} \\
\sqrt{3}m\sin(\alpha) \geq 1-4\delta > \sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right) \qquad & \text{(Mode 4)} \\
\sqrt{3}m\sin\left(\frac{\pi}{3}-\alpha\right) \geq 1-4\delta > 0 \text{ and} & \\
\sqrt{3}m\sin(\alpha) \geq 1-4\delta > 0 \qquad & \text{(Mode 5)}
\end{aligned} \tag{3.7}
$$

As seen from (3.7), the conditions for the PET to operate in a mode depend on the modulation index m, the phase shift parameter δ and the angle α made by $\mathbf{V_o}$ with VSI vector in a sector. For a given value of m, as δ is changed, the PET operates in different regions. In different regions, the PET operates in one or more modes as α varies.

A region is defined by the range of δ for a given value of m, when the PET operates in some specific modes as the angle α changes. If changing the value of δ (for a given value of m) causes the PET to start operating in a new mode, then it is implied that the PET has entered a new region. Visually, these regions are presented in Fig. 3.7, along with the modes of operation in each region. There are a total of four regions, called Region 1 through Region 4. The condition on δ for which the PET will operate in one of the four regions is obtained by putting suitable values of α in the conditions for different modes. The condition on δ for Region 1 for example, is obtained by putting $\alpha = \frac{\pi}{6}$ and substituting it in condition for Mode 1 in (3.7). Then, the condition obtained is given in (3.8).

$$
\begin{aligned}
& 1 \geq 1-4\delta > \sqrt{3}m \\
\implies & 0 \leq \delta < \frac{1-\sqrt{3}m}{4} \text{ (Region 1)}
\end{aligned} \tag{3.8}
$$

It is observed that in Region 1, the PET operates exclusively in Mode 1. This is the inner mode region, as described in [35]. The other regions could be called outer mode

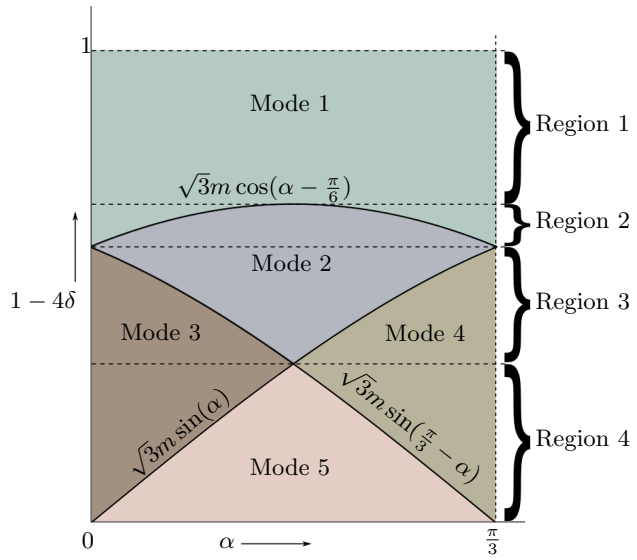


Figure 3.7: Three phase PET regions and modes

regions.

The lower bound for δ to operate in Region 2 is same as the upper bound for δ in Region 1 in (3.8), i.e. $\frac{1-\sqrt{3}m}{4}$. The upper bound for Region 2 is obtained by substituting $\alpha = 0$ in the expression for duty ratio d_1, in the Mode 2 inequality in (3.5). The following condition is obtained.

$$\frac{1-\sqrt{3}m}{4} \leq \delta < \frac{1-1.5m}{4} \text{ (Region 2)} \tag{3.9}$$

In Region 2, the PET operates in Mode 1 as α varies from 0 to a certain value α_1, transitions to Mode 2 at $\alpha = \alpha_1$ and operates there till $\alpha = \frac{\pi}{3} - \alpha_1$ and then comes back to Mode 1 till $\alpha = \frac{\pi}{3}$. Then, the vector $\mathbf{V_o}$ moves to the next sector and the same process is repeated. The expression for α_1 is given by replacing the inequality with an equality sign in the condition for Mode 1 in (3.7).

$$\begin{aligned} 1 - 4\delta &= \sqrt{3}m\cos\left(\alpha_1 - \frac{\pi}{6}\right) = \sqrt{3}m\cos\left(\frac{\pi}{6} - \alpha_1\right) \\ \implies \alpha_1 &= \frac{\pi}{6} - \cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right) \end{aligned} \tag{3.10}$$

The lower bound on δ for PET operation in Region 3 is same as the upper bound on

δ for Region 2. The upper bound on δ for Region 3 is obtained by substituting $\alpha = \frac{\pi}{6}$ in either d_1 or d_2 expression, in either Mode 3 or Mode 4 inequality in (3.5). The following condition is obtained.

$$\frac{1 - 1.5m}{4} \leq \delta < \frac{1 - \frac{\sqrt{3}}{2}m}{4} \text{ (Region 3)} \tag{3.11}$$

In Region 3, the PET operates in Mode 3 till α is less than α_2, then it transitions to Mode 2 and stays there till $\alpha < \frac{\pi}{3} - \alpha_2$ and then transitions to Mode 4 till α reaches $\frac{\pi}{3}$. Then, this whole process is repeated over all the sectors. The value of α_2 is given as follows.

$$\begin{aligned} 1 - 4\delta &= \sqrt{3}m\sin(\alpha_2) \\ \implies \alpha_2 &= \sin^{-1}\left(\frac{1 - 4\delta}{\sqrt{3}m}\right) \end{aligned} \tag{3.12}$$

Finally when δ goes beyond the upper bound in (3.11), the PET enters Region 4. The condition on δ for Region 4 operation is given below.

$$\frac{1 - \frac{\sqrt{3}}{2}m}{4} \leq \delta < \frac{1}{4} \text{ (Region 4)} \tag{3.13}$$

In Region 4, the PET operates in Mode 3 till α is less than α_3, then it transitions to Mode 5 and stays there till $\alpha < \frac{\pi}{3} - \alpha_3$ and then transitions to Mode 4 till α reaches $\frac{\pi}{3}$. Then, this whole process is repeated over all the sectors. The value of α_3 is given as follows.

$$\begin{aligned} 1 - 4\delta &= \sqrt{3}m\sin\left(\frac{\pi}{3} - \alpha_3\right) \\ \implies \alpha_3 &= \frac{\pi}{3} - \sin^{-1}\left(\frac{1 - 4\delta}{\sqrt{3}m}\right) \end{aligned} \tag{3.14}$$

It should be noted that inverse trigonometric functions give values within a certain range only. So, while using (3.10), (3.12) and (3.14), care should be taken to ensure that the value of transition angles obtained are within $[0, \frac{\pi}{6}]$. The results of the analysis done so far on the modes and regions of the three phase PET are summarized in table 3.2.

Table 3.2: Regions and Modes of operation of Three Phase PET

	Region 1	Region 2	Region 3	Region 4
Condition on δ	$0 \leq \delta < \frac{1-\sqrt{3}m}{4}$	$\frac{1-\sqrt{3}m}{4} < \delta \leq \frac{1-1.5m}{4}$	$\frac{1-1.5m}{4} \leq \delta < \frac{1-\frac{\sqrt{3}}{2}m}{4}$	$\frac{1-\frac{\sqrt{3}}{2}m}{4} \leq \delta < \frac{1}{4}$
Mode 1	$0 < \alpha \leq \frac{\pi}{3}$	$0 < \alpha \leq \alpha_1$ $\frac{\pi}{3} - \alpha_1 < \alpha \leq \frac{\pi}{3}$	N/A	N/A
Mode 2	N/A	$\alpha_1 < \alpha \leq \frac{\pi}{3} - \alpha_1$	$\alpha_2 < \alpha \leq \frac{\pi}{3} - \alpha_2$	N/A
Mode 3	N/A	N/A	$0 < \alpha \leq \alpha_2$	$0 < \alpha \leq \alpha_3$
Mode 4	N/A	N/A	$\frac{\pi}{3} - \alpha_2 < \alpha \leq \frac{\pi}{3}$	$\frac{\pi}{3} - \alpha_3 < \alpha \leq \frac{\pi}{3}$
Mode 5	N/A	N/A	N/A	$\alpha_3 < \alpha \leq \frac{\pi}{3} - \alpha_3$
Mode transition α expression	N/A	$\alpha_1 = \frac{\pi}{6} - \cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)$	$\alpha_2 = \sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)$	$\alpha_3 = \frac{\pi}{3} - \sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)$

3.2.1 Analysis in one switching period

The PET operates in five different modes, distributed across four operating regions, as discussed at the start of this section. In order to obtain the average power transfer, transformer rms currents and dc link ripple current over a line frequency period, these values are first obtained over a switching period for all the five modes. Then, these expressions are integrated over appropriate limits of α to obtain the values of the currents over a sector. Now in sector 1, v_{AN} is maximum and v_{BN} and v_{CN} are mid and least of the three phase voltages respectively. When output voltage vector $\mathbf{V_o}$ is in sector 1 when S_1 is ON, it goes to sector 4 when S_1 is OFF. Now when $\mathbf{V_o}$ is in sector 4 when S_1 is ON, it goes to sector 1 when S_1 is OFF. Thus, the analysis done for one switching period with $\mathbf{V_o}$ in sector 1 with S_1 ON also covers the case for $\mathbf{V_o}$ in sector 4 with S_1 ON, yielding identical results. In addition, in sectors 3 and 5 (with S_1 ON), the voltages v_{AN}, v_{BN} and v_{CN} simply interchange positions wrt being maximum, medium and minimum of all three phases. Thus, the analysis done for sector 1 with S_1 ON for all three phases is sufficient to get the currents and power transfer over a complete line frequency period.

The switching pulses for upper switches of the three legs of the VSI are given in Fig. 3.8(a), for Mode 1. The transformer secondary voltage v_{AN} and VSI phase voltage v_{XN} for phase A are given in Fig. 3.8(b) for Mode 1. Finally, the phase A secondary current i_{aL}, dc link current i_{dc} and phase A primary current $i_{\mathrm{a,pr}}$ are given in Fig. 3.8(c) for Mode 1. The turns ratio is assumed to be unity, hence there is no term containing the turns ratio n in $i_{\mathrm{a,pr}}$ in Fig. 3.8(c). All of these waveforms are given for Mode 2 in Fig.

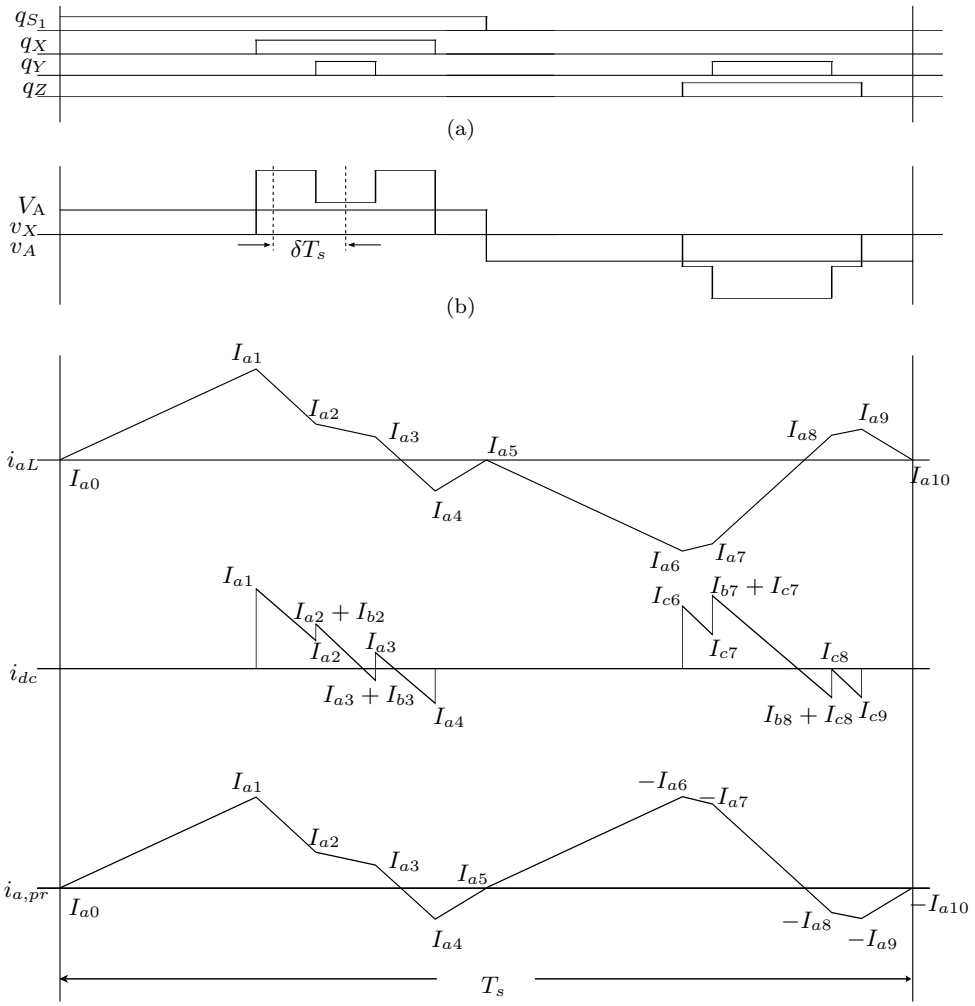


Figure 3.8: Operation of three phase PET in Mode 1

3.9. The waveforms for other three modes can be drawn and will have similar shapes as shown in these two modes.

The starting secondary current I_{a0} for phase A for each mode is first taken as an unknown variable. Then, the values of phase A secondary current are computed at all voltage transitions in one switching period, as expressions containing I_{a0}. Then, the value of I_{a0} is determined for each mode by equating the average secondary current to zero. This is a valid assumption, since the transformer secondary and VSI voltages across each phase have a net zero value over a switching period. This analysis is also done for the other two phases B and C to obtain their respective current expressions at the start of a switching period in all five modes.

The average total power transfer across all three phases over a switching period is given as follows, for all five modes. In all the expressions given from now on for the three phase PET, the terms d_1 and d_2 have substituted by their expressions given in (3.2).

$$P_{\text{o,sw}} = \frac{3\delta m^2 T_s V_{dc}^2}{2L} \text{ (Mode 1)} \tag{3.15}$$

$$P_{\text{o,sw}} = \frac{mT_s V_{dc}^2}{128L}(24(m+4\delta m) - 3(4(1-4\delta)^2 + 9m^2)\cos(\alpha) + 12(1-4\delta)m\cos(2\alpha) - \sqrt{3}(4(1-4\delta)^2 + 15m^2 + 12m((-2+8\delta)\cos(\alpha) + m\cos(2\alpha)))\sin(\alpha)) \text{ (Mode 2)} \tag{3.16}$$

$$P_{\text{o,sw}} = \frac{mT_s V_{dc}^2}{128L}(12(3+4\delta)m - (16(1-4\delta)^2 + 39m^2)\cos(\alpha) + m((12-48\delta)\cos(2\alpha) + 3m\cos(3\alpha) - 2\sqrt{3}(-2+8\delta+3m\cos(\alpha))\sin(2\alpha))) \text{ (Mode 3)} \tag{3.17}$$

$$P_{\text{o,sw}} = \frac{mT_s V_{dc}^2}{128L}(12(3+4\delta)m - 8((1-4\delta)^2 + 3m^2)\cos(\alpha) - 3m^2\cos(3\alpha) - \sqrt{3}(8(1-4\delta)^2 + 21m^2 + 16(-1+4\delta)m\cos(\alpha) + 6m^2\cos(2\alpha))\sin(\alpha)) \text{ (Mode 4)} \tag{3.18}$$

$$P_{\text{o,sw}} = \frac{mT_s V_{dc}^2}{32L}(12m - 3((1-4\delta)^2 + 3m^2)\cos(\alpha) - \sqrt{3}((1-4\delta)^2 + 3m^2)\sin(\alpha)) \text{ (Mode 5)} \tag{3.19}$$

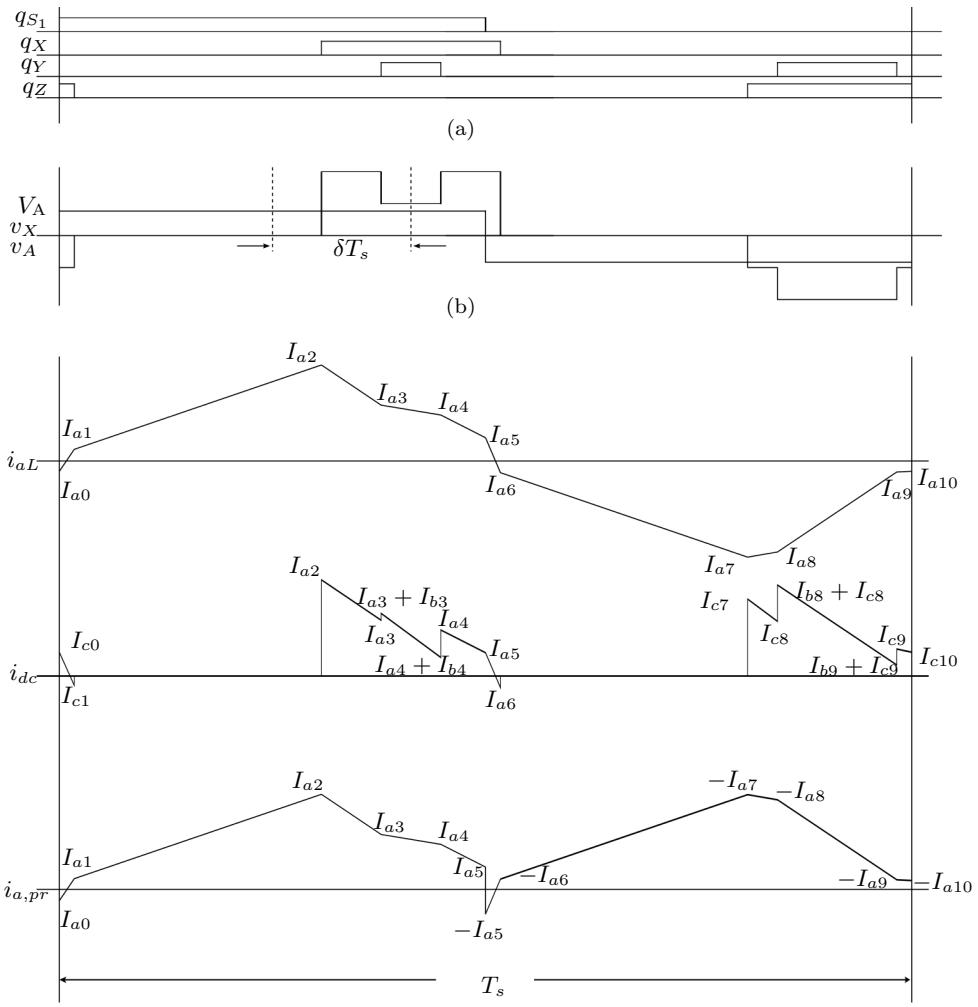


Figure 3.9: Operation of three phase PET in Mode 2

The rms current expressions for phase A for all five modes are given below.

$$I_{\mathrm{aL,sw}} = \frac{mT_sV_{dc}}{48L}(12(4+192\delta^2+9m^2)\cos(\alpha)^2 - 2\sqrt{3}m(7+11\cos(2\alpha))\sin(\alpha)+ 9m\cos(3\alpha)(-3+2\sqrt{3}m\sin(\alpha)) + 9m\cos(\alpha)(-13+ 4\sqrt{3}m\sin(\alpha))) \text{ (Mode 1)} \tag{3.20}$$

$$I_{\mathrm{aL,sw}} = \frac{T_sV_{dc}}{48\sqrt{2}L}[m(3m(-20+96\delta(3+2\delta)+9m^2) - 12(4(-1+4\delta)^3+ 3(-1+30\delta)m^2)\cos(\alpha) + m(3(-20+96\delta(3+2\delta)+9m^2)\cos(2\alpha)- 216\delta m\cos(3\alpha) + \sqrt{3}(24(2-9\delta)m\sin(\alpha) - 9(4(1-4\delta)^2+3m^2)\sin(2\alpha)+ 8(4-27\delta)m\sin 3\alpha]))))]^{\frac{1}{2}} \text{ (Mode 2)} \tag{3.21}$$

$$I_{\mathrm{aL,sw}} = \frac{T_sV_{dc}}{48L}[m(48(-1+12\delta)m + (-32(-1+4\delta)^3 + 9(7-80\delta)m^2)\cos(\alpha)+ m(9(1-16\delta)m\cos(3\alpha) + 2\cos(2\alpha)(-24+288\delta+\sqrt{3}(7-72\delta)m\sin(\alpha))+ \sqrt{3}(2(11-72\delta)m\sin(\alpha) - 6(2(1-4\delta)^2+m^2)\sin(2\alpha)+ 3m^2\sin(4\alpha))))]^{\frac{1}{2}} \text{ (Mode 3)} \tag{3.22}$$

$$I_{\mathrm{aL,sw}} = \frac{T_sV_{dc}}{48\sqrt{2}L}[m(3m(-20+96\delta(3+2\delta)+9m^2) - 8(4(-1+4\delta)^3+117\delta m^2)\cos(\alpha)+ m(36(1-10\delta)m\cos(3\alpha) + \cos(2\alpha)(-60+288\delta(3+2\delta)+27m^2- 8\sqrt{3}m(-8+54\delta+3m\cos(\alpha))\sin(\alpha)) + \sqrt{3}(16(5-27\delta)m\sin(\alpha)- 3(4(1-4\delta)^2+5m^2)\sin(2\alpha))))]^{\frac{1}{2}} \text{ (Mode 4)} \tag{3.23}$$

$$I_{\mathrm{aL,sw}} = \frac{T_sV_{dc}}{48L}[m(-3(8(-1+4\delta)^3+3(-5+72\delta)m^2)\cos(\alpha) + m(-48+576\delta+ 48(-1+12\delta)\cos(2\alpha) + 27(1-8\delta)m\cos(3\alpha) + 2\sqrt{3}m(11-72\delta+ (7-72\delta)\cos(2\alpha))\sin(\alpha)))]^{\frac{1}{2}} \text{ (Mode 5)} \tag{3.24}$$

The rms current expressions for phase B for all five modes are given below.

$$I_{\mathrm{bL,sw}} = \frac{mT_sV_{dc}}{48L}[-(-54m^2 + 36m\cos(\alpha) + 3(4 + 192\delta^2 + 9m^2)\cos(2\alpha) - 2\sqrt{3}m(8 - 27m\cos(\alpha) + 28\cos(2\alpha))\sin(\alpha) + 12(1 + 48\delta^2)(-2 + \sqrt{3}\sin(2\alpha)))]^{\frac{1}{2}} \text{ (Mode 1 and Mode 2)} \quad (3.25)$$

$$I_{\mathrm{bL,sw}} = \frac{T_sV_{dc}}{48L}[m(3m(-4 + 96\delta(1 + 2\delta) + 9m^2) + 4(-2(-1 + 4\delta)^3 + 9(1 - 8\delta)m^2)\cos(\alpha) - 12m(1 + 48\delta^2 + 3m^2)\cos(2\alpha) + 18(-1 + 4\delta)m^2\cos(3\alpha) + 9m^3\cos(4\alpha) + 8\sqrt{3}((-1 + 4\delta)^3 + 6(-1 + 3\delta)m^2)\sin(\alpha) - 6\sqrt{3}m(-2 + 32\delta(1 + \delta) + m^2)\sin(2\alpha) + 2\sqrt{3}(5 + 36\delta)m^2\sin(3\alpha) + 3\sqrt{3}m^3\sin(4\alpha))]^{\frac{1}{2}} \text{ (Mode 3)} \quad (3.26)$$

$$I_{\mathrm{bL,sw}} = \frac{T_sV_{dc}}{48L}[m(3m(-4 + 96\delta(1 + 2\delta) + 9m^2) + (8(-1 + 4\delta)^3 + 18(-3 + 4\delta)m^2)\cos(\alpha) + 3m(8 - 96\delta + 3m^2)\cos(2\alpha) + 18(1 - 4\delta)m^2\cos(3\alpha) - 9m^3\cos(4\alpha) + 2\sqrt{3}(-4(-1 + 4\delta)^3 + 3(7 - 36\delta)m^2)\sin(\alpha) - 3\sqrt{3}m(32\delta(1 + 4\delta) + 7m^2)\sin(2\alpha) + 2\sqrt{3}(5 + 36\delta)m^2\sin(3\alpha) - 3\sqrt{(}3)m^3\sin(4\alpha))]^{\frac{1}{2}} \text{ (Mode 4)} \quad (3.27)$$

$$I_{\mathrm{bL,sw}} = \frac{mT_sV_{dc}}{24\sqrt{2}L}[9(1 - 12\delta)m\cos(\alpha) + (12 - 144\delta)\cos(2\alpha) + \sqrt{3}m(-1 + 36\delta + 8(-1 + 18\delta)\cos(2\alpha))\sin(\alpha) - 12(-1 + 12\delta)(-2 + \sqrt{3}\sin(2\alpha))]^{\frac{1}{2}} \text{ (Mode 5)} \quad (3.28)$$

The rms current expressions for phase C for all five modes are given below.

$$I_{\mathrm{cL,sw}} = \frac{mT_sV_{dc}}{48\sqrt{2}L}[(108m^2 - 126m\cos(\alpha) - 3(8 + 384\delta^2 + 9m^2)\cos(2\alpha) + m(54\cos(3\alpha) - 27m\cos(4\alpha) + 2\sqrt{(}3)(-68 - 22\cos(2\alpha) + 9m(8\cos(\alpha) + \cos(3\alpha)))\sin(\alpha)) + 24(1 + 48\delta^2)(2 + \sqrt{3}\sin(2\alpha)))]^{\frac{1}{2}} \text{ (Mode 1)} \quad (3.29)$$

$$I_{\mathrm{cL,sw}} = \frac{T_s V_{dc}}{48\sqrt{2}L}[m(3m(-20+96\delta(3+2\delta)+9m^2)-6(4(-1+4\delta)^3+ 3(-5+48\delta)m^2)\cos(\alpha)-6m(4+192\delta^2+9m^2)\cos(2\alpha)+216\delta m^2\cos(3\alpha)- 6\sqrt{3}(4(-1+4\delta)^3+(1+72\delta)m^2)\sin(\alpha)+48\sqrt{3}(-1+12\delta)m\sin(2\alpha)+ 8\sqrt{3}(4-27\delta)m^2\sin(3\alpha))]^{\frac{1}{2}} \text{ (Mode 2)} \quad (3.30)$$

$$I_{\mathrm{cL,sw}} = \frac{T_s V_{dc}}{48\sqrt{2}L}[m(3m(-20+96\delta(3+2\delta)+9m^2)-8(2(-1+4\delta)^3+ 9(-1+11\delta)m^2)\cos(\alpha)-12m(-1+24\delta(1+2\delta)+3m^2)\cos(2\alpha)+ 36(-1+10\delta)m^2\cos(3\alpha)+9m^3\cos(4\alpha)-8\sqrt{3}(2(-1+4\delta)^3+ 3(1+15\delta)m^2)\sin(\alpha)+6\sqrt{3}m(-6+16\delta(5+2\delta)+m^2)\sin(2\alpha)+ 8\sqrt{3}(4-27\delta)m^2\sin(3\alpha)-3\sqrt{3}m^3\sin(4\alpha))]^{\frac{1}{2}} \text{ (Mode 3)} \quad (3.31)$$

$$I_{\mathrm{cL,sw}} = \frac{T_s V_{dc}}{48\sqrt{2}L}[m(96(-1+12\delta)m-4(8(-1+4\delta)^3+9(-3+26\delta)m^2)\cos(\alpha)- 6m(-2+48\delta(1+2\delta)+3m^2)\cos(2\alpha)+18(-1+16\delta)m^2\cos(3\alpha)-9m^3\cos(4\alpha)- 8\sqrt{3}(4(-1+4\delta)^3+3(-2+27\delta)m^2)\sin(\alpha)-6\sqrt{3}m(10+16\delta(-7+2\delta)+ m^2)\sin(2\alpha)+2\sqrt{3}(7-72\delta)m^2\sin(3\alpha)+3\sqrt{3}m^3\sin(4\alpha))]^{\frac{1}{2}} \text{ (Mode 4)} \quad (3.32)$$

$$I_{\mathrm{cL,sw}} = \frac{T_s V_{dc}}{48L}[m(48(-1+12\delta)m+3(-4(-1+4\delta)^3+3(5-48\delta)m^2)\cos(\alpha)+ 24(1-12\delta)m\cos(2\alpha)+27(-1+8\delta)m^2\cos(3\alpha)-3\sqrt{3}(4(-1+4\delta)^3+ (-5+96\delta)m^2)\sin(\alpha)+24\sqrt{3}(-1+12\delta)m\sin(2\alpha)+ \sqrt{3}(7-72\delta)m^2\sin(3\alpha))]^{\frac{1}{2}} \text{ (Mode 5)} \quad (3.33)$$

The expressions for rms value of the dc link current for all five modes are given below.

$$I_{\mathrm{dcrms,sw}} = \frac{T_s V_{dc} m}{32\sqrt{3\sqrt{3}}L}[m(-12\sqrt{3}m(21+2\cos(2\alpha)+\cos(4\alpha))+96(1+48\delta^2)\sin(\alpha)+ 3\cos(\alpha)(\sqrt{3}(32+1536\delta^2+75m^2)-96m\sin(\alpha)^3)-8(7+288\delta^2)\sin(3\alpha)+ 9m^2(-\sqrt{3}\cos(5\alpha)+25\sin(\alpha)-4\sin(3\alpha)+\sin(5\alpha)))]^{\frac{1}{2}} \text{ (Mode 1)} \quad (3.34)$$

$$I_{\text{dcrms,sw}} = \frac{T_s V_{dc}}{96L}[m(-288(1-4\delta)^2 m - 972m^3 + 3(-32(-1+4\delta)^3 + 24(13+ 12\delta(-3+16\delta))m^2 + 225m^4)\cos(\alpha) - 72m(2(1-4\delta)^2 + 3m^2)\cos(2\alpha) - 27m^4\cos(5\alpha) + \sqrt{3}(-32(-1+4\delta)^3 + 24(13+12\delta(-3+16\delta))m^2 + 225m^4)\sin(\alpha) - 72\sqrt{3}m(2(1-4\delta)^2 + 3m^2)\sin(2\alpha) - 4\sqrt{3}m^2(-22+ 144\delta(1+4\delta) + 9m^2)\sin(3\alpha) + 9\sqrt{3}m^4\sin(5\alpha))]^{\frac{1}{2}} \text{ (Mode 2)} \quad (3.35)$$

$$I_{\text{dcrms,sw}} = \frac{T_s V_{dc}}{96L}[m((-128(-1+4\delta)^3 + 144(7+4\delta(-5+24\delta))m^2 + 675m^4)\cos(\alpha) + m(-288(1-4\delta)^2 - 918m^2 - 72(4(1-4\delta)^2 + 5m^2)\cos(2\alpha) + 144(1-4\delta)m\cos(3\alpha) - 18m^2\cos(4\alpha) - 27m^3\cos(5\alpha) + 3\sqrt{3}m(128+ 384\delta(-1+4\delta) + 75m^2)\sin(\alpha) - 48\sqrt{3}((1-4\delta)^2 + 5m^2)\sin(2\alpha) - 4\sqrt{3}m(14 + 576\delta^2 + 9m^2)\sin(3\alpha) + 66\sqrt{3}m^2\sin(4\alpha) + 9\sqrt{3}m^3\sin(5\alpha)))]^{\frac{1}{2}} \text{(Mode 3)} \quad (3.36)$$

$$I_{\text{dcrms,sw}} = \frac{T_s V_{dc}}{96L}[m(-288(1-4\delta)^2 m - 918m^3 + (-64(-1+4\delta)^3 + 72(15+ 4\delta(-11+48\delta))m^2 + 675m^4)\cos(\alpha) - 36m(-2(1-4\delta)^2 + 5m^2)\cos(2\alpha) + 144(-1+4\delta)m^2\cos(3\alpha) - 90m^3\cos(4\alpha) - 27m^4\cos(5\alpha) + \sqrt{3}(-64(-1+4\delta)^3 + 24(13+12\delta(-3+16\delta))m^2 + 225m^4)\sin(\alpha) - 12\sqrt{3}m(14(1-4\delta)^2 + 25m^2)\sin(2\alpha) - 4\sqrt{3}m^2(14 + 576\delta^2 + 9m^2)\sin(3\alpha) + 42\sqrt{3}m^3\sin(4\alpha) + 9\sqrt{3}m^4\sin(5\alpha))]^{\frac{1}{2}} \text{ (Mode 4)} \quad (3.37)$$

$$I_{\text{dcrms,sw}} = \frac{T_s V_{dc}}{96L}[m(-288m((1-4\delta)^2 + 3m^2) + 3(-32(-1+4\delta)^3 + 384(1+ 3\delta(-1+4\delta))m^2 + 225m^4)\cos(\alpha) - 36m(2(1-4\delta)^2 + 9m^2)\cos(2\alpha) - 108m^3\cos(4\alpha) - 27m^4\cos(5\alpha) + \sqrt{3}(-32(-1+4\delta)^3 + 384(1+ 3\delta(-1+4\delta))m^2 + 225m^4)\sin(\alpha) - 36\sqrt{3}m(2(1-4\delta)^2 + 9m^2)\sin(2\alpha) - 4\sqrt{3}m^2(50 + 144\delta(-1+4\delta) + 9m^2)\sin(3\alpha) + 108\sqrt{3}m^3\sin(4\alpha) + 9\sqrt{3}m^4\sin(5\alpha))]^{\frac{1}{2}} \text{ (Mode 5)} \quad (3.38)$$

The average dc link current over a switching period can be found by dividing the average

power by the dc link voltage, for all five modes.

$$I_{\text{dcavg,sw}} = \frac{P_{\text{o,sw}}}{V_{dc}} \text{ (Mode 1 through 5)} \tag{3.39}$$

The ripple in the dc link current can be determined by subtracting the average value from the rms value. Ripple current expression is useful to know when choosing a capacitor for the dc link. The expressions for this current for all five modes are given below.

$$\begin{aligned}
I_{\text{rpl,sw}} =& \frac{mT_sV_{dc}}{96L}[m(-108(7+192\delta^2)m + 9(32+1536\delta^2+75m^2)\cos(\alpha)+ \\
& 96\sqrt{3}(1+48\delta^2)\sin(\alpha) + 9m(-8\cos(2\alpha) - 4\cos(4\alpha) - 3m\cos(5\alpha)+ \\
& 2\sqrt{3}(-4\cos(\alpha) - 3m\cos(2\alpha) + 4\cos(3\alpha) + m(11+\cos(4\alpha)))\sin(\alpha))- \\
& 8\sqrt{3}(7+288\delta^2)\sin(3\alpha))]^{\frac{1}{2}} \text{ (Mode 1)}
\end{aligned} \tag{3.40}$$

$$\begin{aligned}
I_{\text{rpl,sw}} =& \frac{T_sV_{dc}}{384L}[m(-9m(-24(m+4\delta m) + 3(4(1-4\delta)^2+9m^2)\cos(\alpha)+ \\
& 12(-1+4\delta)m\cos(2\alpha) + \sqrt{3}(4(1-4\delta)^2+15m^2+12m((-2+8\delta)\cos(\alpha)+ \\
& m\cos(2\alpha)))\sin(\alpha))^2 + 16(-288(1-4\delta)^2m - 972m^3 + 3(-32(-1+4\delta)^3+ \\
& 24(13+12\delta(-3+16\delta))m^2 + 225m^4)\cos(\alpha) - 72m(2(1-4\delta)^2+3m^2)\cos(2\alpha)- \\
& 27m^4\cos(5\alpha) + \sqrt{3}(-32(-1+4\delta)^3 + 24(13+12\delta(-3+16\delta))m^2+ \\
& 225m^4)\sin(\alpha) - 72\sqrt{3}m(2(1-4\delta)^2+3m^2)\sin(2\alpha) - 4\sqrt{3}m^2(-22+ \\
& 144\delta(1+4\delta)+9m^2)\sin(3\alpha) + 9\sqrt{3}m^4\sin(5\alpha)))]^{\frac{1}{2}} \text{ (Mode 2)}
\end{aligned} \tag{3.41}$$

$$\begin{aligned}
I_{\text{rpl,sw}} =& \frac{T_sV_{dc}}{384L}[m(-9m(12(3+4\delta)m - (16(1-4\delta)^2+39m^2)\cos(\alpha)+ \\
& m((12-48\delta)\cos(2\alpha) + 3m\cos(3\alpha) - 2\sqrt{3}(-2+8\delta+3m\cos(\alpha))\sin(2\alpha)))^2+ \\
& 16((-128(-1+4\delta)^3 + 144(7+4\delta(-5+24\delta))m^2 + 675m^4)\cos(\alpha)+ \\
& m(-288(1-4\delta)^2 - 918m^2 - 72(4(1-4\delta)^2+5m^2)\cos(2\alpha)+ \\
& 144(1-4\delta)m\cos(3\alpha) - 18m^2\cos(4\alpha) - 27m^3\cos(5\alpha) + 3\sqrt{3}m(128+ \\
& 384\delta(-1+4\delta)+75m^2)\sin(\alpha) - 48\sqrt{3}((1-4\delta)^2+5m^2)\sin(2\alpha)- \\
& 4\sqrt{3}m(14+576\delta^2+9m^2)\sin(3\alpha) + 66\sqrt{3}m^2\sin(4\alpha)+ \\
& 9\sqrt{3}m^3\sin(5\alpha))))]^{\frac{1}{2}} \text{ (Mode 3)}
\end{aligned} \tag{3.42}$$

$$I_{\text{rpl,sw}} = \frac{T_s V_{dc}}{384L}[m(-9m(-12(3+4\delta)m + 8((1-4\delta)^2 + 3m^2)\cos(\alpha) + 3m^2\cos(3\alpha) + \sqrt{3}(8(1-4\delta)^2 + 21m^2 + 16(-1+4\delta)m\cos(\alpha) + 6m^2\cos(2\alpha)\sin(\alpha))^2 + 16(-288(1-4\delta)^2 m - 918m^3 + (-64(-1+4\delta)^3 + 72(15+4\delta(-11+48\delta))m^2 + 675m^4)\cos(\alpha) - 36m(-2(1-4\delta)^2 + 5m^2)\cos(2\alpha) + 144(-1+4\delta)m^2\cos(3\alpha) - 90m^3\cos(4\alpha) - 27m^4\cos(5\alpha) + \sqrt{3}(-64(-1+4\delta)^3 + 24(13+ 12\delta(-3+16\delta))m^2 + 225m^4)\sin(\alpha) - 12\sqrt{3}m(14(1-4\delta)^2 + 25m^2)\sin(2\alpha) - 4\sqrt{3}m^2(14 + 576\delta^2 + 9m^2)\sin(3\alpha) + 42\sqrt{3}m^3\sin(4\alpha) + 9\sqrt{3}m^4\sin(5\alpha)))]^{\frac{1}{2}} \text{ (Mode 4)} \tag{3.43}$$

$$I_{\text{rpl,sw}} = \frac{T_s V_{dc}}{96L}[m(-288m((1-4\delta)^2 + 3m^2) + 3(-32(-1+4\delta)^3 + 384(1+ 3\delta(-1+4\delta))m^2 + 225m^4)\cos(\alpha) - 36m(2(1-4\delta)^2 + 9m^2)\cos(2\alpha) - 108m^3\cos(4\alpha) - 27m^4\cos(5\alpha) + \sqrt{3}(-32(-1+4\delta)^3 + 384(1+ 3\delta(-1+4\delta))m^2 + 225m^4)\sin(\alpha) - 36\sqrt{3}m(2(1-4\delta)^2 + 9m^2)\sin(2\alpha) - 4\sqrt{3}m^2(50 + 144\delta(-1+4\delta) + 9m^2)\sin(3\alpha) + 108\sqrt{3}m^3\sin(4\alpha) + 9\sqrt{3}m^4\sin(5\alpha))]^{\frac{1}{2}} \text{ (Mode 5)} \tag{3.44}$$

3.2.2 Power transfer and currents in one line frequency period

The quantities obtained in previous subsection for one switching time period are integrated over a sector i.e. the angle α varying from 0 to $\frac{\pi}{3}$, to obtain the values of these quantities averaged over a sector. The average power and dc ripple current is same for each sector, hence integration over a sector gives the value for all sectors. The secondary side phase currents are however interchanging and will be further processed to give the expression for secondary side phase current over a line frequency period, as will be discussed later in this subsection.

The quantities for Region 1 have already been given in [35]. For the sake of completeness however, they will be given in this subsection as well. They are obtained by integrating corresponding Mode 1 quantities over a sector. For Region 2, any quantity (power, rms current) is computed by integration of Mode 1 and Mode 2 quantities,

based on the limits of α where they occur. This is done as follows.

$$X_{\text{sector}} = \frac{3}{\pi}\left(\int_0^{\alpha_1} X_{\text{sw,Mode1}}(\alpha)d\alpha + \int_{\alpha_1}^{\frac{\pi}{3}-\alpha_1} X_{\text{sw,Mode2}}(\alpha)d\alpha + \int_{\frac{\pi}{3}-\alpha_1}^{\frac{\pi}{3}} X_{\text{sw,Mode1}}(\alpha)d\alpha\right) \quad \text{(Region 2)} \qquad (3.45)$$

where

X_{sector} = Average value of X over a sector

$X_{\text{sw,Mode1}}$ = Average value of X over a switching period T_s in Mode 1

$X_{\text{sw,Mode2}}$ = Average value of X over a switching period T_s in Mode 2

α_1 is taken from (3.10).

In a similar fashion, the quantities for Region 3 and Region 4 are computed as follows.

$$X_{\text{sector}} = \frac{3}{\pi}\left(\int_0^{\alpha_2} X_{\text{sw,Mode3}}(\alpha)d\alpha + \int_{\alpha_2}^{\frac{\pi}{3}-\alpha_2} X_{\text{sw,Mode2}}(\alpha)d\alpha + \int_{\frac{\pi}{3}-\alpha_2}^{\frac{\pi}{3}} X_{\text{sw,Mode4}}(\alpha)d\alpha\right) \quad \text{(Region 3)} \qquad (3.46)$$

$$X_{\text{sector}} = \frac{3}{\pi}\left(\int_0^{\alpha_3} X_{\text{sw,Mode3}}(\alpha)d\alpha + \int_{\alpha_3}^{\frac{\pi}{3}-\alpha_3} X_{\text{sw,Mode5}}(\alpha)d\alpha + \int_{\frac{\pi}{3}-\alpha_3}^{\frac{\pi}{3}} X_{\text{sw,Mode4}}(\alpha)d\alpha\right) \quad \text{(Region 4)} \qquad (3.47)$$

where

X_{sector} = Average value of X over a sector

$X_{\text{sw,Mode2}}$ = Average value of X over a switching period T_s in Mode 2

$X_{\text{sw,Mode3}}$ = Average value of X over a switching period T_s in Mode 3

$X_{\text{sw,Mode4}}$ = Average value of X over a switching period T_s in Mode 4

$X_{\text{sw,Mode5}}$ = Average value of X over a switching period T_s in Mode 5

α_2 is defined in (3.12), α_3 is defined in (3.14)

In equations (3.45)-(3.47), the integration is done without substituting the expression for mode boundary α, i.e. α_1, α_2 and α_3. After the integration is done, then the expressions from (3.10), (3.12) and (3.14) are substituted to further simplify the integrated expression.

The expressions for average power transferred over sector 1 (S_1 ON) are given below

for all four regions.

$$P_o = \frac{3\delta m^2 T_s V_{dc}^2}{2L} \text{ (Region 1)} \tag{3.48}$$

$$P_o = -\frac{mT_s V_{dc}^2}{24L}\left((6m^2+(1-4\delta)^2)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} - 12\delta m\pi - 9(1-4\delta)m\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right) \text{ (Region 2)} \tag{3.49}$$

$$P_o = \frac{T_s V_{dc}^2}{144L}\left((-3m(1-4\delta)^2-18m^3)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} - \sqrt{3}((1-4\delta)^3+9m^3) + 18m^2\pi + 27(-1+4\delta)m^2\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right) \text{ (Region 3 and Region 4)} \tag{3.50}$$

These expressions are same for all sectors, hence these are the expressions for power transfer over a line frequency cycle.

The phase A secondary voltage v_{AN} is the maximum during sector 1 (S_1 ON), while the phase voltages v_{BN} and v_{CN} are mid and minimum of the three phase voltages, respectively. So, the phase A, B and C currents averaged over sector 1 (S_1 ON) are the currents flowing through the maximum, mid and minimum phases respectively. The rms value of current through phase with maximum voltage in sector 1 (S_1 ON), averaged over a sector, is therefore obtained by integrating rms current expressions for phase A. The integration is done taking the square of rms currents over a switching period, integrating them over a sector and then putting the square root back.

$$I_{\mathrm{L,max}} = \frac{mT_s V_{dc}}{96\sqrt{2\pi}L}\sqrt{\sqrt{3}(144+6912\delta^2+m(-1616+567m))+48(4+192\delta^2+9m^2)\pi} \text{ (Region 1)} \tag{3.51}$$

$$I_{\mathrm{L,max}} = \frac{T_s V_{dc}}{96\sqrt{2\pi}L}\left[m\left(72(39m^2(1-4\delta)+2(1-4\delta)^3)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} + \sqrt{3}m(144+m(-1616+567m))+48m(4+9m^2)\pi+2304\delta^2 m(3\sqrt{3}+4\pi) - 648m(4(1-4\delta)^2+3m^2)\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right)\right]^{\frac{1}{2}} \text{ (Region 2)} \tag{3.52}$$

$$I_{\mathrm{L,max}} = \frac{T_s V_{dc}}{48\sqrt{2\pi}L}\Bigg[(117m^3(1-4\delta)+6m(1-4\delta)^3)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2}+ 2\sqrt{3}((1-4\delta)^4-24(-1+4\delta)^3m+36(-1+12\delta)m^2+8(4-117\delta)m^3)+ 96(-1+12\delta)m^2\pi+27m^2(4(1-4\delta)^2+3m^2)\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg]^{\frac{1}{2}}$$

(Region 3 and Region 4) (3.53)

The rms value of current through phase with mid voltage in sector 1 (S_1 ON), averaged over a sector, is obtained by integrating rms current expressions for phase B, similar to what is done for $I_{\mathrm{L,max}}$ in equations above. The expressions for $I_{\mathrm{L,mid}}$ are given below for all four regions.

$$I_{\mathrm{L,mid}} = \frac{mT_s V_{dc}}{48\sqrt{\pi}L}\sqrt{-\sqrt{3}(36+1728\delta^2+m(16+81m))+6(4+192\delta^2+9m^2)\pi}$$

(Region 1 and Region 2) (3.54)

$$I_{\mathrm{L,mid}} = \frac{T_s V_{dc}}{24\sqrt{2\pi}L}\Bigg[(117m^3(1-4\delta)+6m(1-4\delta)^3)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2}+ 2\sqrt{3}((1-4\delta)^4+12(-1+4\delta)^3m+18(1-12\delta)m^2+(-67+252\delta)m^3)+ 24(-1+12\delta)m^2\pi+27m^2(4(1-4\delta)^2+3m^2)\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg]^{\frac{1}{2}}$$

(Region 3 and Region 4) (3.55)

The transformer secondary rms current for phase with minimum voltage are obtained by integration of rams currents of phase C. However, they are found to be equal to the maximum phase rms current, for all four regions. This is written below as an equation.

$$I_{\mathrm{L,min}} = I_{\mathrm{L,max}} \text{ (All four regions)} \tag{3.56}$$

The secondary rms current in any of three phases over a line frequency cycle is given as the average of the maximum, mid and minimum currents, since each phase attains one of these positions in two sectors. Thus, the phase currents are computed using

following equation.

$$I_L = \sqrt{\frac{I_{\mathrm{L,max}}^2 + I_{\mathrm{L,mid}}^2 + I_{\mathrm{L,min}}^2}{3}} \text{ (All four regions)} \tag{3.57}$$

The expressions for the phase rms current in all four regions are given below.

$$I_L = \frac{mT_sV_{dc}}{96\sqrt{\pi}L}\sqrt{-560\sqrt{3}m + 27m^2(3\sqrt{3}+8\pi) + 96(\pi + 48\delta^2\pi)} \text{ (Region 1)} \tag{3.58}$$

$$I_L = \frac{T_sV_{dc}}{96\sqrt{\pi}L}\left[m\left((48(1-4\delta)^3 + 936m^2(1-4\delta))\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} + m(\sqrt{3}m(-560+81m) + 24(4+9m^2)\pi + 4608\delta^2\pi) - 216m(4(1-4\delta)^2 + 3m^2)\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right)\right]^{\frac{1}{2}} \text{ (Region 2)} \tag{3.59}$$

$$I_L = \frac{T_sV_{dc}}{48\sqrt{\pi}L}\left((6m(1-4\delta)^3 + 117m^3(1-4\delta))\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} + 2\sqrt{3}((1-4\delta)^4 - 2(17+72\delta)m^3) + 48(-1+12\delta)m^2\pi + 27m^2(4(1-4\delta)^2+3m^2)\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right)^{\frac{1}{2}} \text{ (Region 3 and Region 4)} \tag{3.60}$$

The expressions for dc link ripple current for all four regions are given below.

$$I_{rpl} = \frac{mT_sV_{dc}}{48\sqrt{10\pi}L}\sqrt{m(\sqrt{3}(1160+57600\delta^2+9m(-45+358m)) - 270(7+192\delta^2)m\pi)} \tag{3.61}$$

$$I_{rpl} = \frac{T_sV_{dc}}{96\sqrt{10\pi}L}\left(m\left((-72(1-4\delta)^5 + 960(1-4\delta)^3 + m^2(24192\delta^3 - 139464\delta + 120096\delta^2 + 26982) + m^4(35397+65772\delta))\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2} + m^2(4\sqrt{3}(1160+9m(-45+358m)) - 7560m\pi + 288\delta^2(800\sqrt{3}-720m\pi)) - 135m(8(1-4\delta)^2(19+24\delta(-1+2\delta)) - 12(-35+24\delta(1+14\delta))m^2 + 135m^4)\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\right)\right)^{\frac{1}{2}} \text{ (Region 2)} \tag{3.62}$$

$$I_{rpl} = -\frac{T_s V_{dc}}{192\sqrt{5\pi}L}\Bigg((24m(1-4\delta)^3(13(1-4\delta)^2-20) - 36m^3(1-4\delta)(-100+ 240(1-4\delta)+7(1-4\delta)^2) - 36882m^5 - 59832\delta m^5)\sqrt{3-\left(\frac{1-4\delta}{m}\right)^2}+ \sqrt{3}(8(1-4\delta)^4(-13+12\delta)(7+12\delta)+320(-155+72\delta(9+16(-2+\delta)\delta))m^3+ 405(73+264\delta(-1+2\delta))m^4+144(-425+264\delta)m^5+10935m^6+180(15+ 8\delta(1+14\delta))(m-4\delta m)^2)+360m^2(2(1-4\delta)^2(8+(1-4\delta)^2)+ 3(25+288\delta^2)m^2+9m^4)\pi+270m^2(8(1-4\delta)^4-12(-13+24\delta(1+6\delta))m^2+ 63m^4)\cos^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg)^{\frac{1}{2}} \text{ (Region 3)} \tag{3.63}$$

$$I_{rpl} = \frac{T_s V_{dc}}{96\sqrt{5\pi}L}\Bigg[(-6m(1-4\delta)(2(1-4\delta)^2(-10+7(1-4\delta)^2)+3m^2(50- 120(1-4\delta)+47(1-4\delta)^2))+10179m^5+11124\delta m^5)\sqrt{3-\left(\frac{1-4\delta}{m}\right)}+ \sqrt{3}(4(1-4\delta)^4(59+72\delta(-1+2\delta))-80(-155+72\delta(9+16(-2+\delta)\delta))m^3- 6480(1-3\delta+6\delta^2)m^4+36(425-264\delta)m^5-3645m^6-45m^2(1-4\delta)^2(15+ 8\delta(1+14\delta)))-90m^2((1-4\delta)^2(16+3(1-4\delta)^2)+6(20+3(1-4\delta)^2)m^2+ 27m^4)\pi+135m^2(-4(1-4\delta)^4-96(-1+3\delta+6\delta^2)m^2+9m^4)\sin^{-1}\left(\frac{1-4\delta}{\sqrt{3}m}\right)\Bigg]^{\frac{1}{2}} \text{ (Region 4)} \tag{3.64}$$

The rms current in each of the transformer primary windings is given as follows.

$$I_p = n\frac{I_L}{\sqrt{2}} \quad \text{(All four regions)} \tag{3.65}$$

The rms voltage for primary and secondary windings are given (3.66) and (3.67) respectively, for all four regions.

$$V_p = \frac{mV_{dc}}{2n} \tag{3.66}$$

$$V_s = \sqrt{\frac{2m}{\sqrt{3}\pi}}V_{dc} \tag{3.67}$$

The net VA flowing through the transformer over a line frequency cycle is given as follows.

$$P_t = \frac{3}{2}(V_p I_p + V_s I_L) \tag{3.68}$$

The quantities given in equations (2.25)-(2.36) are converted to per unit before plotting them. The base quantities used are as follows.

$$\begin{aligned} V_{\text{base}} &= V_{dc} \\ I_{\text{base}} &= \frac{V_{dc} T_s}{2\pi L} \\ P_{\text{base}} &= V_{\text{base}} I_{\text{base}} \end{aligned} \tag{3.69}$$

It should be noted that while the analysis done so far is only for positive values of δ, it can be easily extended to the negative range of δ too. For negative values of δ, the power transferred is of same magnitude, but changes sign (i.e., instead of flowing from grid to the dc link, it flows in the opposite direction). Also, the rms quantities retain their expressions for negative δ.

The average power, dc link ripple current and transformer utilization for the three phase PET are plotted against δ, as seen in Fig.3.10. The different curves in each figure are for different values of modulation index m, ranging from $\frac{1}{10\sqrt{3}}$ to the maximum value i.e. $\frac{1}{\sqrt{3}}$. In each of the figures, there are dashed lines to denote the various regions of operation of the PET. From Fig. 3.10(a), it is observed that the maximum power transfer in Region 4 is approximately 0.41 pu, which is more than three times the maximum power transfer of 0.12 pu in Region 1. It should however be noted that the maximum dc ripple current in Region 4 is 0.52 pu, which is also more than three times that of the maximum dc ripple current of 0.14 pu in Region 1, as seen in Fig. 3.10(b). Finally, the transformer utilization in Region 4 is more than that in Region 1, as seen in Fig. 3.10(c) for several operating points. However, if the transformer utilization at values of δ with maximum power transfer is considered, the transformer utilization ration is 0.58 in Region 4 vs 0.69 in Region 1.

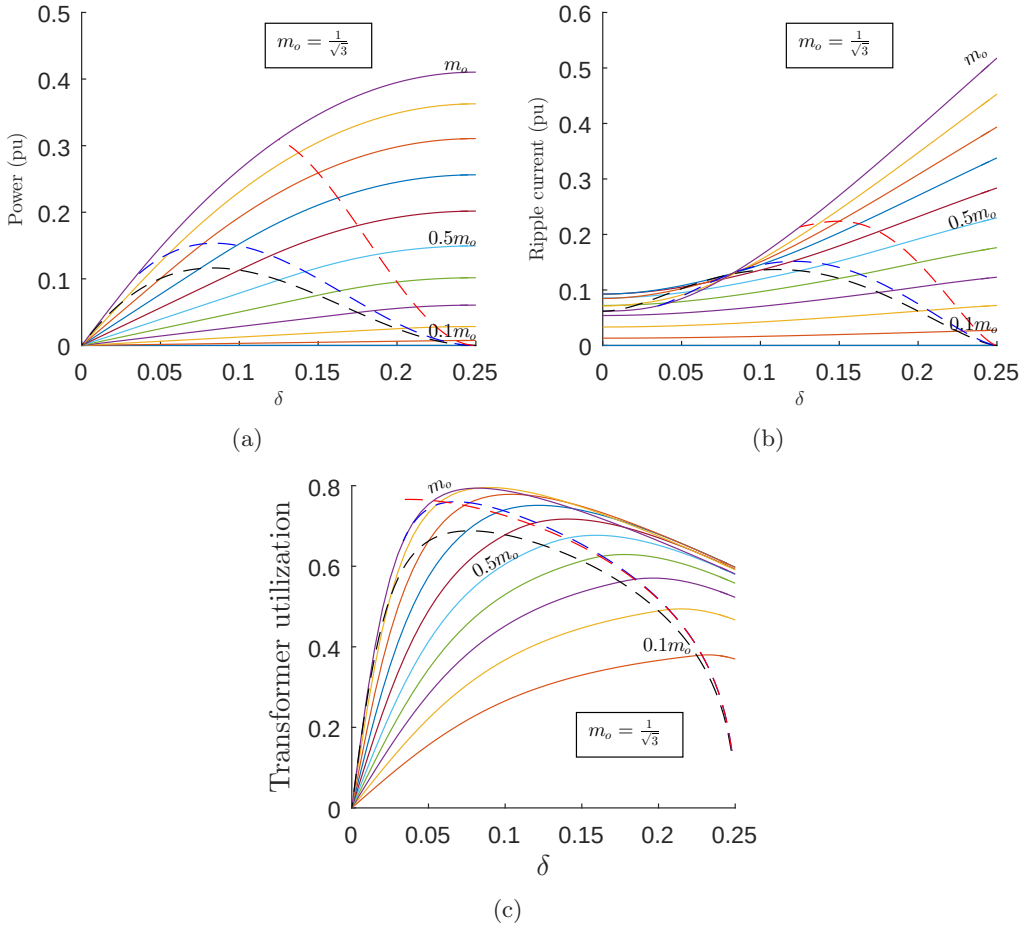


Figure 3.10: Three phase PET characteristics (a) Average power vs δ (b) DC ripple current vs δ (c) Transformer utilization vs δ

3.2.3 Soft switching

The current waveforms of phase A secondary current i_{aL} and primary current $i_{a,pr}$ are given in Fig. 3.8 for Mode 1. It is observed, that the primary current $i_{a,pr}$ is zero when the primary switches S_1 and S_2 are switching. This is also true for phase B and C currents in Mode 1. Therefore, the current through the primary side switches S_1 and S_2 is zero when they switch, which means they undergo Zero Current Switching (ZCS) in Mode 1. This is however not true for the other four modes, as demonstrated in Fig. 3.9 for Mode 2.

The expressions for phase A, B and C secondary currents when the respective secondary side VSI upper switches are turning ON and turning OFF, are given below for sector 1.

$$I_{\text{AON,Mode1}} = \frac{mT_sV_{dc}\cos(\alpha)}{4L}\Big(1+4\delta-\sqrt{3}m\cos\Big(\alpha-\frac{\pi}{6}\Big)\Big) \tag{3.70}$$

$$I_{\text{AOFF,Mode1}} = \frac{mT_sV_{dc}\cos(\alpha)}{4L}\Big(-1+4\delta+\sqrt{3}m\cos\Big(\alpha-\frac{\pi}{6}\Big)\Big) \tag{3.71}$$

$$I_{\text{BON1,Mode1}} = \frac{mT_sV_{dc}}{12L}\Big(3(\sqrt{3}m\sin(\alpha)-4\delta)\cos\Big(\alpha+\frac{\pi}{3}\Big)+\sqrt{3}\sin(\alpha)\Big) \tag{3.72}$$

$$I_{\text{BOFF1,Mode1}} = -\frac{mT_sV_{dc}}{12L}\Big(3(\sqrt{3}m\sin(\alpha)+4\delta)\cos\Big(\alpha+\frac{\pi}{3}\Big)+\sqrt{3}\sin(\alpha)\Big) \tag{3.73}$$

$$I_{\text{BON2,Mode1}} = \frac{mT_sV_{dc}}{12L}\Big(-3\Big(\sqrt{3}m\sin\Big(\frac{\pi}{3}-\alpha\Big)-4\delta\Big)\cos\Big(\alpha+\frac{\pi}{3}\Big)+\sqrt{3}\sin\Big(\frac{\pi}{3}-\alpha\Big)\Big) \tag{3.74}$$

$$I_{\text{BOFF2,Mode1}} = -\frac{mT_sV_{dc}}{12L}\Big(-3\Big(\sqrt{3}m\sin\Big(\frac{\pi}{3}-\alpha\Big)+4\delta\Big)\cos\Big(\alpha+\frac{\pi}{3}\Big)+\sqrt{3}\sin\Big(\frac{\pi}{3}-\alpha\Big)\Big) \tag{3.75}$$

$$I_{\text{CON,Mode1}} = \frac{mT_sV_{dc}}{4L}\Big(1+4\delta-\sqrt{3}m\cos\Big(\alpha-\frac{\pi}{6}\Big)\Big)\sin\Big(\alpha+\frac{\pi}{6}\Big) \tag{3.76}$$

$$I_{\text{COFF,Mode1}} = \frac{mT_sV_{dc}}{4L}\Big(-1+4\delta+\sqrt{3}m\cos\Big(\alpha-\frac{\pi}{6}\Big)\Big)\sin\Big(\alpha+\frac{\pi}{6}\Big) \tag{3.77}$$

It should be noted in equations above that upper switch of phase B of VSI is switched once ON and OFF when S_1 is ON. The currents are these instances are called $I_{\text{BON1,Mode1}}$ and $I_{\text{BOFF1,Mode1}}$ respectively in Mode 1. This phase is again switched ON and OFF when S_2 is ON (during the same switching period). The currents are these instances are called $I_{\text{BON2,Mode1}}$ and $I_{\text{BOFF2,Mode1}}$ respectively in Mode 1. For all the four remaining

modes, the currents for phase B will be denoted similarly.

The expressions for the currents at turn ON and OFF of upper switches of the VSI in Mode 2 are given below, for sector 1.

$$I_{\text{AON,Mode2}} = I_{\text{AON,Mode1}} \tag{3.78}$$

$$I_{\text{AOFF,Mode2}} = -\, I_{\text{AOFF,Mode1}} \tag{3.79}$$

$$I_{\text{BON1,Mode2}} = I_{\text{BON1,Mode1}} \tag{3.80}$$

$$I_{\text{BOFF1,Mode2}} = I_{\text{BOFF1,Mode1}} \tag{3.81}$$

$$I_{\text{BON2,Mode2}} = I_{\text{BON2,Mode1}} \tag{3.82}$$

$$I_{\text{BOFF2,Mode2}} = I_{\text{BOFF2,Mode1}} \tag{3.83}$$

$$I_{\text{CON,Mode2}} = I_{\text{CON,Mode1}} \tag{3.84}$$

$$I_{\text{COFF,Mode2}} = -\, I_{\text{COFF,Mode1}} \tag{3.85}$$

The expressions for the currents at turn ON and OFF of upper switches of the VSI in Mode 3 are given below, for sector 1.

$$I_{\text{AON,Mode3}} = I_{\text{AON,Mode1}} \tag{3.86}$$

$$I_{\text{AOFF,Mode3}} = -\, I_{\text{AOFF,Mode1}} \tag{3.87}$$

$$I_{\text{BON1,Mode3}} = I_{\text{BON1,Mode1}} \tag{3.88}$$

$$I_{\text{BOFF1,Mode3}} = I_{\text{BOFF1,Mode1}} \tag{3.89}$$

$$I_{\text{BON2,Mode3}} = I_{\text{BON2,Mode1}} \tag{3.90}$$

$$\begin{aligned} I_{\text{BOFF2,Mode3}} = {} & \frac{mT_s V_{dc}}{12L}\Big(3\Big(\sqrt{3}m\cos\Big(\alpha+\frac{\pi}{6}\Big)+4\delta\Big)\sin\Big(\alpha-\frac{\pi}{6}\Big)+3\cos\Big(\alpha+\frac{\pi}{3}\Big)- \\ & \sqrt{3}\sin(\alpha)\Big) \end{aligned} \tag{3.91}$$

$$I_{\text{CON,Mode3}} = I_{\text{CON,Mode1}} \tag{3.92}$$

$$I_{\text{COFF,Mode3}} = -\, I_{\text{COFF,Mode1}} \tag{3.93}$$

The expressions for the currents at turn ON and OFF of upper switches of the VSI in

Mode 4 are given below, for sector 1.

$$I_{\text{AON,Mode4}} = I_{\text{AON,Mode1}} \tag{3.94}$$

$$I_{\text{AOFF,Mode4}} = -\, I_{\text{AOFF,Mode1}} \tag{3.95}$$

$$I_{\text{BON1,Mode4}} = I_{\text{BON1,Mode1}} \tag{3.96}$$

$$I_{\text{BOFF1,Mode4}} = \frac{mT_sV_{dc}}{12L}\left(3(\sqrt{3}m\sin(\alpha)+4\delta)\cos\left(\alpha+\frac{\pi}{3}\right)+4\sin\left(\alpha-\frac{\pi}{6}\right)-\cos(\alpha)\right) \tag{3.97}$$

$$I_{\text{BON2,Mode4}} = I_{\text{BON2,Mode1}} \tag{3.98}$$

$$I_{\text{BOFF2,Mode4}} = I_{\text{BOFF2,Mode1}} \tag{3.99}$$

$$I_{\text{CON,Mode4}} = I_{\text{CON,Mode1}} \tag{3.100}$$

$$I_{\text{COFF,Mode4}} = -\, I_{\text{COFF,Mode1}} \tag{3.101}$$

Finally, the expressions for the currents at turn ON and OFF of upper switches of the VSI in Mode 5 are given below, for sector 1.

$$I_{\text{AON,Mode5}} = I_{\text{AON,Mode1}} \tag{3.102}$$

$$I_{\text{AOFF,Mode5}} = -\, I_{\text{AOFF,Mode1}} \tag{3.103}$$

$$I_{\text{BON1,Mode5}} = I_{\text{BON1,Mode1}} \tag{3.104}$$

$$I_{\text{BOFF1,Mode5}} = I_{\text{BOFF1,Mode4}} \tag{3.105}$$

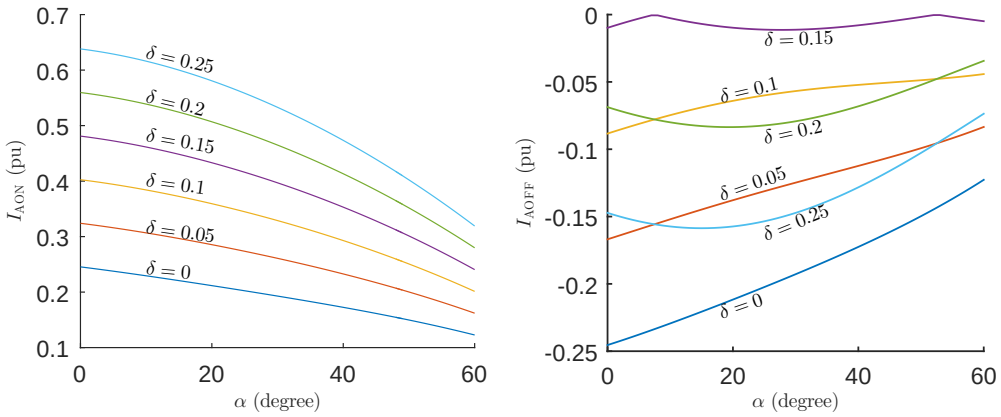
$$I_{\text{BON2,Mode5}} = I_{\text{BON2,Mode1}} \tag{3.106}$$

$$I_{\text{BOFF2,Mode5}} = I_{\text{BOFF1,Mode3}} \tag{3.107}$$

$$I_{\text{CON,Mode5}} = I_{\text{CON,Mode1}} \tag{3.108}$$

$$I_{\text{COFF,Mode5}} = -\, I_{\text{COFF,Mode1}} \tag{3.109}$$

It is determined from the expressions given in equations (3.78)-(3.109) that both the upper and lower switches of VSI phases A and C undergo soft switching for entire range of α between $[0, \frac{\pi}{3}]$ in all regions. However, only the lower switch of phase B of the VSI undergoes soft switching for entire range of α between $[0, \frac{\pi}{3}]$ in all regions. The upper switch of phase B undergoes soft switching for a certain range of α. For all regions, this



(a) (b)

Figure 3.11: Secondary side VSI phase A turn ON and turn OFF currents vs α for modulation index $m = 0.25$ fort various values of δ (a) Turn ON current value (b) Turn OFF current value

range is given as follows.

$$\begin{aligned} I_{\text{BON1}} > 0 \quad &\text{if} \quad \alpha_{ZVS} < \alpha \leq \frac{\pi}{3} \\ I_{\text{BON2}} > 0 \quad &\text{if} \quad 0 < \alpha \leq \frac{\pi}{3} - \alpha_{ZVS} \end{aligned} \tag{3.110}$$

The angle α_{ZVS} is given by the solution of the following equation.

$$(3m\sin(\alpha_{ZVS}) - 4\sqrt{3}\delta)\cos\left(\alpha_{ZVS} + \frac{\pi}{3}\right) + \sin(\alpha_{ZVS}) = 0 \tag{3.111}$$

The plots of the turn ON and turn OFF of the three phases of the VSI are plotted against α in Fig. 3.11, Fig. 3.12 and Fig. 3.13 for modulation index $m = 0.25$. The various curves in each figure show how the value of these currents vary with α for different values of δ. It should be noted that the turn ON and turn OFF currents of phases A for any value of α, as seen in Fig. 3.11, match the turn ON and turn OFF currents of C at the value $(\frac{\pi}{3} - \alpha)$, as seen in Fig. 3.13. The same relation is seen between the turn ON and turn OFF currents of phase B when S_1 is ON (Fig. 3.12(a) and Fig. 3.12(b)) to the turn ON and turn OFF currents of phase B when S_1 is OFF (Fig. 3.12(c) and Fig. 3.12(d)).

It should be noted that the plots shown in Fig .3.11, Fig .3.12 and Fig .3.13are for

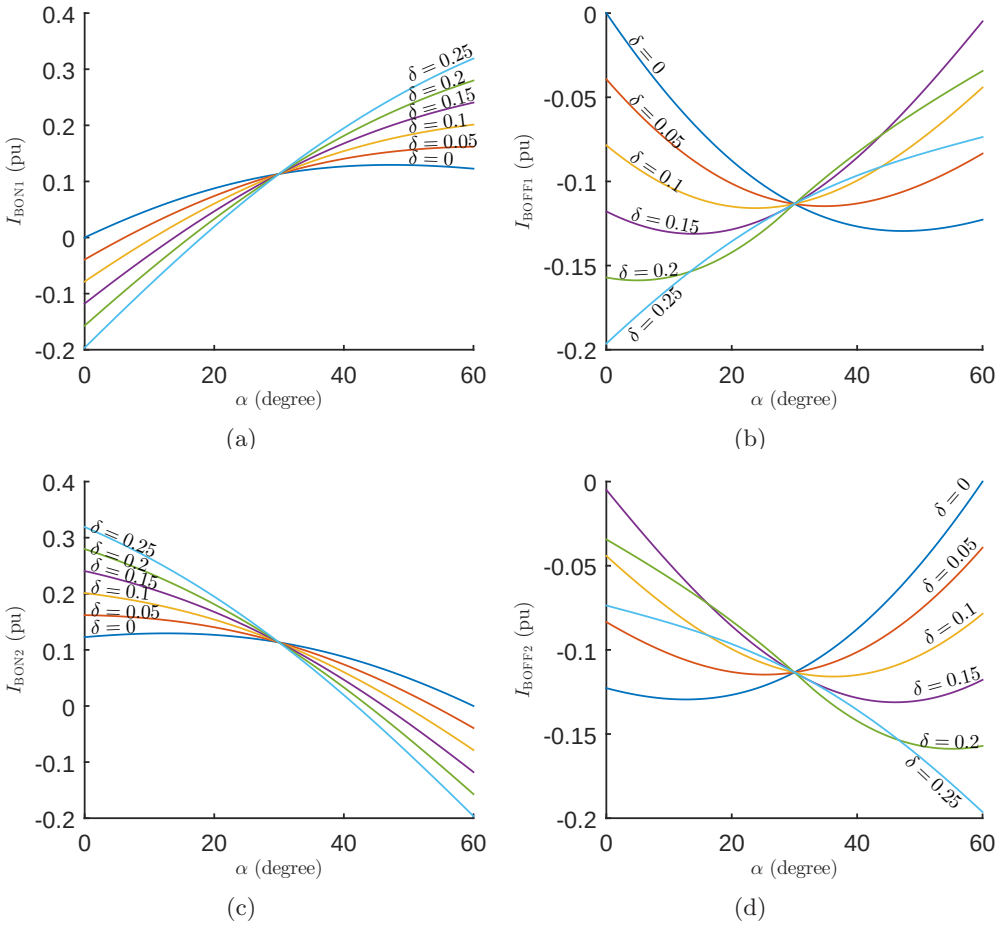


Figure 3.12: Secondary side VSI phase B turn ON and turn OFF currents vs α for modulation index $m = 0.25$ for various values of δ (a) Turn ON current value (when S_1 is ON) (b) Turn OFF current value (when S_1 is ON) (c) Turn ON current value (when S_2 is ON) (d) Turn OFF current value (when S_2 is ON)

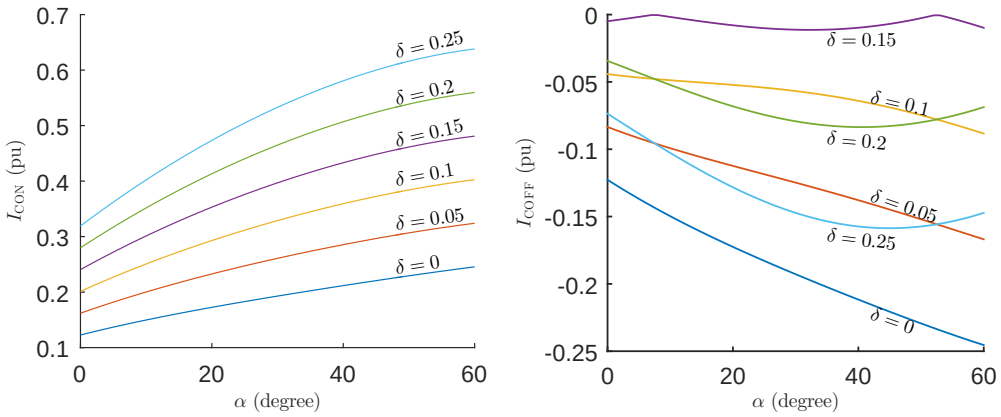


Figure 3.13: Secondary side VSI phase C turn ON and turn OFF currents vs α for modulation index $m = 0.25$ for various values of δ (a) Turn ON current value (b) Turn OFF current value

$0 \leq \delta \leq \frac{1}{4}$. The plots for $-\frac{1}{4} \leq \delta \leq 0$ are going to be similar to those for positive values of δ due to symmetrical nature of the circuit. The turn ON current plots of phase A for negative values of δ will look same as the turn OFF plots of phase A for positive values of δ i.e. Fig. 3.11(b), but with the sign flipped, i.e. the plots will be lying in the first quadrant instead of the fourth quadrant. This means turn ON ZVS is achieved for upper switch of phase A for negative δ as well. Similarly, the turn OFF current plots of phase A for negative values of δ will look same as the turn ON plots of phase A for positive values of δ i.e. Fig. 3.11(b), but with the sign flipped, i.e. the plots will be lying in the fourth quadrant instead of the first quadrant. This means turn ON ZVS is achieved for lower switch of phase A for negative δ as well. Similarly the switches of phase C VSI will also have turn ON ZVS for negative values of δ. For phase B, full ZVS is achieved for achieved for upper switch for negative δ (as opposed to partial ZVS for positive δ) and partial ZVS is achieved for lower switch negative δ (as opposed to full ZVS for positive δ). This analysis is for output voltage vector $\mathbf{V_o}$ being in sector 1 with S_1 ON.

The above analysis is done for all values of δ with output voltage vector $\mathbf{V_o}$ being in sector 1 with S_1 ON. In this sector, phase A voltage is maximum, phase A voltage is in the middle while C voltage is minimum. For other sectors, the three phases simply

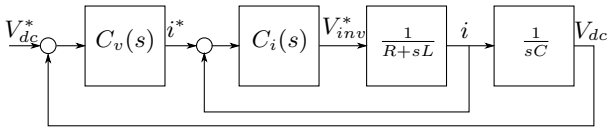


Figure 3.14: Grid tied inverter dc link voltage control scheme

interchange the maximum and minimum positions. The phases which are maximum or minimum at a given sector undergo ZVS for entire duration of that sector, while the mid phase undergoes partial ZVS.

3.3 Closed loop control of DC link voltage

The dc link voltage in a grid tied ac-dc inverter is needed to be regulated to control the power flow between the grid and the system on the other side of the dc link [41–47]. The three phase PET is similar in aspect where the two level VSI is connected to the grid through the transformer and the dc link of the VSI is to be controlled to regulate power flow. In a grid tied inverter, the power flow is regulated in a cascade control scheme, where the inner loop consists of grid current controllers, which regulate currents by generating appropriate voltages at the ac terminals of the inverter. The outer loop consists of the active and reactive power control, where the dc link voltage controller regulates the active power and the reactive power controller regulates the reactive power by controlling the grid currents. The dc link voltage control scheme is shown in Fig. 3.14. The dc link voltage controller $C_v(s)$ ensures to keep the dc link voltage V_{dc} close to the reference V_{dc}^*. It issues the current command i^* and the current controller $C_i(s)$ ensures that the actual grid current i follows this value.

There is however, a key difference between the three phase PET and a grid tied inverter. In a grid tied inverter dc link control, the grid currents controlled and then the inverter voltages are controlled in the inner control loop. This is because the active power is related to the grid currents, which are related to the inverter voltages. In the three phase PET however, while the active power is inherently dependent on grid currents, it is also directly dependent on the parameter δ, given the grid voltage is fixed, as seen in equations (3.48)-(3.50). Thus, by directly issuing a command for δ, the power flow can be regulated and thus the dc link voltage can be regulated. The VSI voltages

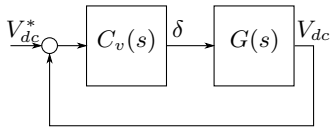


Figure 3.15: Three phase PET dc link voltage control scheme

to be generated are determined by knowing the grid voltage, since the VSI voltage is to be equal to the grid voltage (reflected on transformer secondary) in a switching period. The control scheme is demonstrated in Fig. 3.15. In the figure, the function $G(s)$ is the transfer function of dc link voltage with respect to the parameter δ.

The power transfer function for the three phase PET is a non-linear function, as seen in (3.48)-(3.50). Therefore, in order to design a controller for the PET, the power transfer function is to be linearized about an operating point and then the approximated linear transfer function $G(s)$ is used for deriving the controller parameters. The rate of change of energy stored in the DC link capacitor is a difference of the power coming in from the grid and power absorbed by the load, which is assumed resistive. This can be written mathematically as:

$$\begin{aligned} \frac{d(0.5C_{dc}V_{dc}^2)}{dt} &= P_{grid} - P_{load} \\ \implies C_{dc}V_{dc}\frac{dV_{dc}}{dt} &= f(\delta, V_{grid}, V_{dc}) - \frac{V_{dc}^2}{R_{load}} \end{aligned} \tag{3.112}$$

The grid power is a function of grid voltage V_{grid}, phase shift parameter δ and DC link voltage V_{dc}. The grid voltage is assumed to be fixed. A Taylor's series expansion is done on this function about a given initial operating point (where δ_0, R_{load} and $\hat{V}_{dc}$ are given) and the first order terms are kept while higher order terms are neglected. In addition, the grid voltage is considered fixed, so the term corresponding to disturbance in grid voltage is zero.

$$\begin{aligned} C_{dc}(\hat{V}_{dc}+\tilde{v}_{dc})\frac{d(\hat{V}_{dc}+\tilde{v}_{dc})}{dt} &= f(\delta_0, V_{grid}, \hat{V}_{dc}) + \frac{\partial f}{\partial \delta}|_{\delta=\delta_0}\tilde{\delta} + \frac{\partial f}{\partial V_{dc}}|_{V_{dc}=\hat{V}_{dc}}\tilde{v}_{dc} - \frac{(\hat{V}_{dc}+\tilde{v}_{dc})^2}{R_{load}} \\ \implies C_{dc}\frac{d\tilde{v}_{dc}}{dt} &= p_1\tilde{\delta} + p_2\tilde{v}_{dc} - \frac{2\hat{V}_{dc}}{R_{load}}\tilde{v}_{dc} \end{aligned} \tag{3.113}$$

where $p_1 = \frac{\partial f}{\partial \delta}|_{\delta=\delta_0}$ and $p_2 = \frac{\partial f}{\partial V_{dc}}|_{V_{dc}=\hat{V}_{dc}}$

It should be noted that in the equation (3.113), the quantities $\tilde{v}_{dc}$ and $\tilde{\delta}$ represent small signal disturbances in the dc link voltage v_{dc} and phase shift parameter δ respectively. Taking Laplace transform, the equation (3.113) becomes

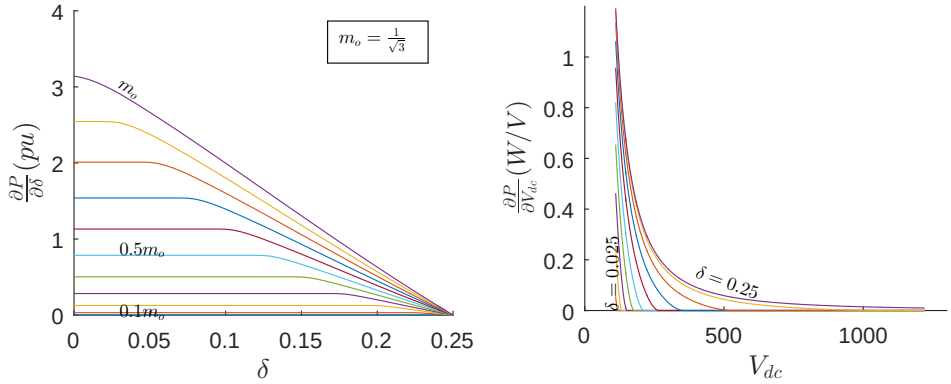
$$\begin{aligned}(sC_{dc} + \frac{2\hat{V}_{dc}}{R_{load}} - p_2)\tilde{v}_{dc}(s) &= p_1\tilde{\delta}(s) \\ \implies G(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{\delta}(s)} &= \frac{p_1}{(sC_{dc} + \frac{2\hat{V}_{dc}}{R_{load}} - p_2)}\end{aligned} \tag{3.114}$$

The transfer function to use for designing the DC link voltage controller is given by equation (3.114). In order to determine the quantities p_1 and p_2, the partial derivatives of power P_o wrt V_{dc} and δ need to be determined around an operating point. For illustration purposes, the plots of $\frac{\partial P}{\partial \delta}$ are shown in Fig. 3.16(a) for different values of δ and m. As with all the quantities plotted so far, this is plotted in per unit (pu) with the base values given in (3.69). In these plots, the dc link voltage V_{dc} is kept fixed, while δ is varied along x-axis and different plots are for different values of modulation index m.

The plots of $\frac{\partial P}{\partial V_{dc}}$ for a given value of the dc link voltage are illustrated in Fig. 3.16(b). In the figure, the various plots are for different values of δ. In these plots, instead of varying m directly, it is varied indirectly as V_{dc} changes along the x-axis while keeping the grid voltage fixed throughout. It should be noted that since the dc link voltage V_{dc} is changing in these plots, the per unit system is not used here. The plots are obtained for peak grid voltage $\hat{V}_{grid} = 61V$, secondary side inductance $L = 480\mu H$ and a range of dc link voltages, ranging from $\left(\frac{\hat{V}_{grid}}{0.55}, \frac{\hat{V}_{grid}}{0.05}\right)$. The turns ratio of the transformer is assumed to be unity. The chosen range of V_{dc} here essentially means that modulation index m varies between $(0.05, 0.55)$, which covers most of the full range between $(0, \frac{1}{\sqrt{3}})$.

3.4 Operation under unbalanced grid voltages

A three phase grid has the voltages of the three phases balanced under normal operation. This means that the voltages of all three phases are of equal amplitude and they are displaced by $\frac{2\pi}{3}$ with respect to each other. This is the assumption so far in the analysis done for the three phase PET in this chapter. However, due to faults or voltage sags,



(a) (b)

Figure 3.16: Partial derivative of three phase PET power transferred (a) vs phase shift parameter δ keeping V_{dc} fixed (b) vs dc link voltage V_{dc} while keeping V_{grid} fixed

the grid voltages can become unbalanced meaning that their amplitudes may no longer be equal and the phase difference could be different than $\frac{2\pi}{3}$. As an example, the unbalanced voltages due to a sag in phase c voltage are shown in Fig. 3.17. It is necessary to understand how a grid tied system works when subjected to unbalanced grid voltages so as to find what corrective measure(s) could be taken to solve the issues observed [48–63].

Unbalanced grid voltages can be split into positive sequence, negative sequence and zero sequence voltages. The conversion of voltages is done using (3.115) from abc voltage phasors ($\overline{V_a}$, $\overline{V_b}$, $\overline{V_c}$) to positive ($\overline{V_+}$), negative ($\overline{V_-}$) and zero sequence ($\overline{V_0}$) voltage phasors.

$$\begin{bmatrix} \overline{V_0} \\ \overline{V_+} \\ \overline{V_-} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} \overline{V_a} \\ \overline{V_b} \\ \overline{V_c} \end{bmatrix} \tag{3.115}$$

where $\alpha = e^{j\frac{2\pi}{3}}$.

Zero sequence voltages do not have a path to flow any currents in three wire systems, which is the case with the three phase PET under study. Hence, from now on, only the positive and negative sequence voltages will be considered for analysis.

Suppose that the positive and negative sequence voltage phasors are $\overline{V_+} = V_+ e^{j\phi_+}$

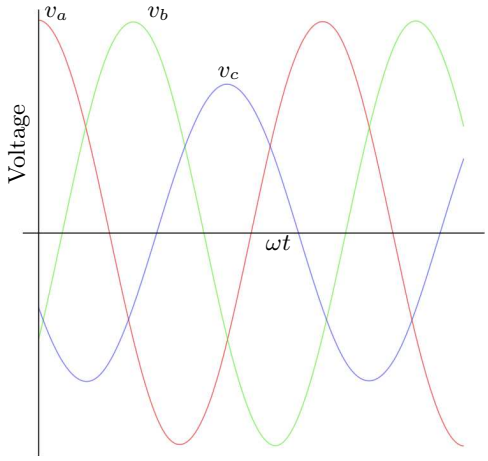


Figure 3.17: Unbalanced three phase voltages

and $\overline{V_-} = V_- e^{j\phi_-}$ respectively. Then, the unbalanced grid voltages v_a, v_b and v_c can be written as shown in equation below.

$$\begin{aligned} v_\mathrm{a} &= V_+ \cos(\omega_\mathrm{grid} t + \phi_+) + V_- \cos(\omega_\mathrm{grid} t + \phi_-) \\ v_\mathrm{b} &= V_+ \cos(\omega_\mathrm{grid} t + \phi_+ - \frac{2\pi}{3}) + V_- \cos(\omega_\mathrm{grid} t + \phi_- + \frac{2\pi}{3}) \\ v_\mathrm{c} &= V_+ \cos(\omega_\mathrm{grid} t + \phi_+ + \frac{2\pi}{3}) + V_- \cos(\omega_\mathrm{grid} t + \phi_- - \frac{2\pi}{3}) \end{aligned} \tag{3.116}$$

Now, assume that there are two separate PET systems, one for the positive sequence and one for the negative sequence. Also, suppose that the phase shift parameters for the positive and negative sequence PET systems are δ_+ and δ_- respectively. Then, suppose that phasors of fundamental grid currents for the positive and negative sequence PET systems are $I_+ e^{\phi_+}$ and $I_- e^{\phi_-}$ respectively. Note that the currents are in phase with the respective voltages since power transfer happens at unity power factor. Now, if the two systems are combined, then the net fundamental grid currents will be as given in

(3.117).

$$\begin{aligned} i_{\mathrm{a}} &= I_+ \cos(\omega_{\mathrm{grid}} t + \phi_+) + I_- \cos(\omega_{\mathrm{grid}} t + \phi_-) \\ i_{\mathrm{b}} &= I_+ \cos(\omega_{\mathrm{grid}} t + \phi_+ - \frac{2\pi}{3}) + I_- \cos(\omega_{\mathrm{grid}} t + \phi_- + \frac{2\pi}{3}) \\ i_{\mathrm{c}} &= I_+ \cos(\omega_{\mathrm{grid}} t + \phi_+ + \frac{2\pi}{3}) + I_- \cos(\omega_{\mathrm{grid}} t + \phi_- - \frac{2\pi}{3}) \end{aligned} \tag{3.117}$$

The net instantaneous power flow will be given as in (3.118).

$$P_{inst} = \sum_{k=a,b,c} v_k i_k = 1.5(V_+ I_+ + V_- I_-) + 1.5(V_+ I_- + V_- I_+) \cos(2\omega_{\mathrm{grid}} t + \phi_+ + \phi_-) \tag{3.118}$$

It is apparent from (3.118) that the power transferred has a constant term and a term with second harmonic of the grid frequency ω_{grid}. In order to eliminate this component, the condition required is given in (3.119).

$$\begin{aligned} V_+ I_- + V_- I_+ &= 0 \\ \implies \frac{V_+}{V_-} &= -\frac{I_+}{I_-} \end{aligned} \tag{3.119}$$

It is clear from (3.119) that the positive and negative sequence sequence currents should be in opposite modes (motoring and regeneration modes), as seen from the $-$ sign in the RHS. Also, the ratio of peak values of these currents should be same as that of peak values of the positive and negative sequence voltages. Thus, the values of δ_+ and δ_- should be chosen to satisfy these conditions to accomplish constant power flow during grid voltage imbalance. As a special case, if the operation of the PET were to be limited to only Region 1 during voltage imbalance (or otherwise), the relation between δ_+ and δ_- is very simple. To illustrate this, the currents I_+ and I_- will be evaluated for Region 1 operation in (3.120).

$$\begin{aligned} I_+ &= \frac{P_o}{1.5V_+} = \frac{3\delta_+ m_+^2 T_s V_{dc}^2}{2L} \frac{1}{1.5V_+} = \frac{V_+ \delta_+ T_s}{L} \text{ (Region 1)} \\ I_- &= \frac{P_o}{1.5V_-} = \frac{3\delta_- m_-^2 T_s V_{dc}^2}{2L} \frac{1}{1.5V_-} = \frac{V_- \delta_- T_s}{L} \text{ (Region 1)} \end{aligned} \tag{3.120}$$

where m_+ and m_- are modulation indexes of positive and negative sequence voltages respectively.

Using (3.119) and (3.120), the relation between δ_+ and δ_- for Region 1 is obtained as follows.

$$\delta_- = -\delta_+ \text{ (Region 1)} \tag{3.121}$$

The solution presented for unbalanced grid voltage operation requires that the voltage pulses for both positive and negative sequence voltages are to be generated by the converter on the secondary side of the transformer. Two possible methods are suggested here.

1. Use a three level VSI instead of a two level VSI on transformer secondary
2. Use a two level VSI (which poses some restrictions as will be discussed below)

The first method is to use a three level VSI to generate these voltages, implying that the two level VSI on the transformer secondary is replaced by a three level VSI. A three level VSI can be operated akin to two series connected two level VSIs. This feature can be used to generate the positive and negative sequence voltage pulses. Since the switches in the three level VSI that are used for generating the positive and negative sequence voltages are separate physical devices, it means that the pulses generated for positive and negative sequence can overlap with each other, as illustrated in Fig. 3.18. This results in having no restriction in the choice of δ_+ and δ_- (the only restriction being that they are within [-0.25,0.25]). This however entails that a full analysis of the PET with three level VSI be done during balanced voltage conditions where the three level VSI is operated as a three level inverter (to get a better voltage waveform) and is left as future work.

The second method involves control of the two level VSI connected at transformer secondary so as to generate voltage pulses for both positive and negative voltages. However, unlike the three level case discussed above, overlapping voltage waveforms shown in Fig. 3.18 cannot be obtained with a two level VSI. This means that there are two restrictions imposed on the choice of δ_+ and δ_-. These are:

1. The voltage pulses generated by the VSI for positive and negative sequences cannot

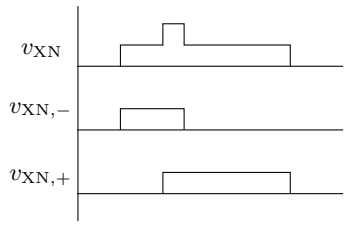


Figure 3.18: Overlapping pole voltages of positive and negative sequence

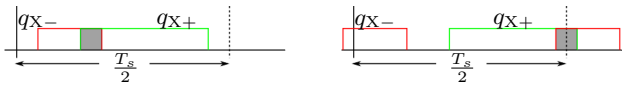


Figure 3.19: Overlapping pulses of positive and negative sequence (a) Within half a switching period T_s (b) Between pulses of adjacent half switching periods

overlap within one half of switching period T_s. This is illustrated in Fig. 3.19(a).

2. The voltage pulses generated by the VSI for positive and negative sequence cannot stretch beyond one half of the switching period T_s, so as to not overlap with pulses from other half of period T_s. This is illustrated in Fig. 3.19(b).

It should be noted that the conditions mentioned above are imposed when the pulses of the same top side switch of the VSI are overlapping, which gets the duty ratio d_1+d_2 for both positive and negative sequences. This situation (of same switch getting the pulses with duty ratio $d_1 + d_2$ for both positive and negative sequences) will however occur in two sectors for any combination of phase angles ϕ_+ and ϕ_- and voltage magnitudes V_+ and V_-. Therefore, the above two conditions are imposed at some point for a given set of imbalanced three phase voltages. Numerically, these conditions will be written as in (3.122).

$$
\begin{aligned}
|\delta_+| + |\delta_-| &> \frac{(d_{1+} + d_{2+} + d_{1-} + d_{2-})}{4} = \frac{\sqrt{3}}{4}\left(m_+ \cos\left(\alpha_+ - \frac{\pi}{6}\right) + m_- \cos\left(\alpha_- - \frac{\pi}{6}\right)\right) \\
|\delta_+| + |\delta_-| &\leq \frac{1}{2} - \frac{(d_{1+} + d_{2+} + d_{1-} + d_{2-})}{4} = \frac{1}{2} - \frac{\sqrt{3}}{4}\left(m_+ \cos\left(\alpha_+ - \frac{\pi}{6}\right) + \right. \\
&\qquad \left. m_- \cos\left(\alpha_- - \frac{\pi}{6}\right)\right) \qquad (3.122)
\end{aligned}
$$

where m_+ and m_- are the modulation indices for the positive and negative sequence

voltages. The angles α_+ and α_- are the space vector angles of positive and negative sequence voltage vectors in any given sector when the quantity $(m_+ \cos(\alpha_+ - \frac{\pi}{6}) + m_- \cos(\alpha_- - \frac{\pi}{6}))$ is largest in a 60 Hz cycle. The quantity is proportionate to the total length of the voltage pulses produced by the VSI for positive and negative sequence voltages at a given instant. The angles α_+ and α_- will be both equal to 30°, if the positive and negative sequence voltages are in phase i.e., $\phi_+ = -\phi_-$. This is because the largest duration pulse for both voltages will occur at $\alpha = \frac{\pi}{6}$ and it will occur simultaneously for both voltages in every sector. If the phase difference ϕ between positive and negative sequence voltages is in multiples of $\frac{\pi}{3}$, then α_+ and α_- will again be equal to $\frac{\pi}{6}$. This happens because when the positive sequence voltage is at the start of say sector 1, then the negative sequence voltage vector is at the start of some other sector. Hence, the duty ratio quantity $d_1 + d_2$ which gives the total length of the voltage pulse generated by the VSI for each voltage vector, maximizes at 30° for both positive and negative sequence voltages. In this case, the limits on $|\delta_+| + |\delta_-|$ are given as follows.

$$\frac{\sqrt{3}}{4}(m_+ + m_-) < |\delta_+| + |\delta_-| \leq \frac{1}{2} - \frac{\sqrt{3}}{4}(m_+ + m_-) \quad \text{(when } \phi_{net} = 0) \tag{3.123}$$

where $\phi_{net} = (\phi_+ + \phi_-) \mod \frac{\pi}{3}$, i.e. the remainder of dividing phase $(\phi_+ + \phi_-)$ by $\frac{\pi}{3}$

The quantity ϕ_{net} as defined above, signifies the phase difference between the starting points of a sector of positive sequence and negative sequence voltage space vectors. If it is zero as stated above, the positive and negative sequence voltage space vectors enter a new sector simultaneously and therefore the voltage pulses for each sequence attain their maximum lengths simultaneously at $\alpha = \frac{\pi}{6}$. It should be noted that the sector entered by the positive and negative sequence voltage space vectors need not be the same. As an example, the positive sequence vector could be entering sector 5, while the negative sequence vector could be entering sector 1 and ϕ_{net} is still equal to zero. An illustration is provided in Fig. 3.20 to give an idea of ϕ_{net}.

When the phase difference $\phi_{net} \neq 0$ i.e. the positive and negative sequence voltage space vectors do not enter a new sector simultaneously, then the limits on $|\delta_+| + |\delta_-|$ are given as follows.

$$\frac{\sqrt{3}}{4}\max(f_1 + f_2) < |\delta_+| + |\delta_-| \leq \frac{1}{2} - \frac{\sqrt{3}}{4}\max(f_1 + f_2) \tag{3.124}$$

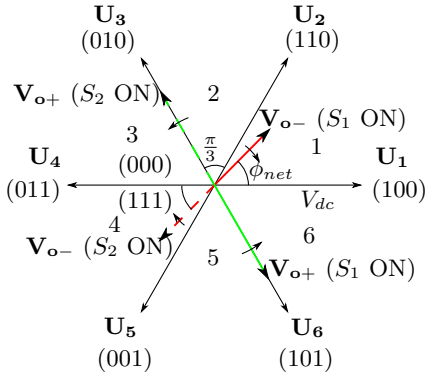


Figure 3.20: Illustration of the concept of ϕ_{net}

where f_1 and f_2 are functions defined below.

$$f_1 = m_+ \cos(\alpha - \frac{\pi}{6}) \qquad 0 < \alpha \leq \frac{\pi}{3} \tag{3.125}$$

$$f_2 = \begin{cases} m_- \cos(\alpha + \frac{\pi}{6} - \phi_{net}) & \text{if } 0 < \alpha \leq \phi_{net} \\ m_- \cos(\alpha - \frac{\pi}{6} - \phi_{net}) & \text{if } \phi_{net} < \alpha \leq \frac{\pi}{3} \end{cases} \tag{3.126}$$

where $\phi_{net} = (\phi_+ + \phi_-) \mod \frac{\pi}{3}$

The functions f_1 and f_2 are proportional to the width of the switching pulses with duty ratio $d_1 + d_2$ for positive and negative sequences respectively. The function $f_1 + f_2$ is divided into two distinct regions, i.e. $0 < \alpha \leq \phi_{net}$ and $\phi_{net} < \alpha \leq \frac{\pi}{3}$. The function is maximized in the region where both f_1 and f_2 attain their respective maxima. f_1 attains its maximum at $\alpha = \frac{\pi}{6}$. The function f_2 will attain its maximum in $\phi_{net} < \alpha \leq \frac{\pi}{3}$ if $\phi_{net} < \frac{\pi}{6}$, otherwise it attains its maximum in $0 < \alpha \leq \phi_{net}$. Thus, $f_1 + f_2$ attains its maximum in $\phi_{net} < \alpha \leq \frac{\pi}{3}$ if $\phi_{net} < \frac{\pi}{6}$, otherwise it attains its maximum in $0 < \alpha \leq \phi_{net}$. This is illustrated in Fig. 3.21.

If $\phi_{net} < \frac{\pi}{6}$, the maximum is attained somewhere at a value α_{max} in $\phi_{net} < \alpha \leq \frac{\pi}{3}$, as discussed in previous paragraph. This angle can be found out by differentiation of the function $f_1 + f_2$ in the second region, equating the differential to zero and solving for α. The value is given as:

$$\alpha_{max} = \frac{\pi}{6} + \tan^{-1}\left(\frac{\frac{m_-}{m_+}\sin(\phi_{net})}{\frac{m_-}{m_+}\cos(\phi_{net}) + 1}\right) \quad (\phi_{net} < \frac{\pi}{6}) \tag{3.127}$$

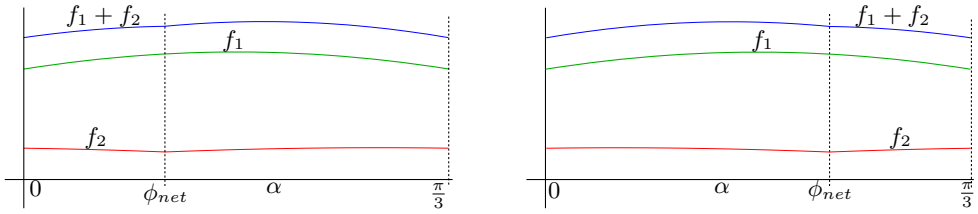


Figure 3.21: Illustration of functions used for determining limits on $|\delta_+| + |\delta_-|$ (a) $\phi_{net} < \frac{\pi}{6}$ (b) $\phi_{net} > \frac{\pi}{6}$

The maximum value of $f_1 + f_2$ is then obtained as below.

$$\max(f_1 + f_2) = m_+\sqrt{1 + k^2 + 2k\cos(\phi_{net})} \qquad (\phi_{net} < \frac{\pi}{6}) \tag{3.128}$$

where $k = \frac{m_-}{m_+}$

If $\phi_{net} \geq \frac{\pi}{6}$, the maximum occurs somewhere in $0 < \alpha \leq \phi_{net}$. The value of α where a maximum occurs in this case can be found out by replacing ϕ_{net} by $\phi'_{net} = \frac{\pi}{3} - \phi_{net}$, finding the value α'_{max} for this ϕ'_{net} using (3.127) and then subtracting α'_{max} from $\frac{\pi}{3}$ to get the required value of α. Thus, it is expressed as:

$$\begin{aligned}\alpha_{max} &= \frac{\pi}{3} - \left(\frac{\pi}{6} + \tan^{-1}\left(\frac{\frac{m_-}{m_+}\sin(\frac{\pi}{3} - \phi_{net})}{\frac{m_-}{m_+}\cos(\frac{\pi}{3} - \phi_{net}) + 1}\right)\right) \\ &= \frac{\pi}{6} - \tan^{-1}\left(\frac{\frac{m_-}{m_+}\sin(\frac{\pi}{3} - \phi_{net})}{\frac{m_-}{m_+}\cos(\frac{\pi}{3} - \phi_{net}) + 1}\right) \quad (\phi_{net} \geq \frac{\pi}{6})\end{aligned} \tag{3.129}$$

The maximum value of the function $f_1 + f_2$ is then obtained as below.

$$\max(f_1 + f_2) = m_+\sqrt{1 + k^2 + 2k\cos\left(\frac{\pi}{3} - \phi_{net}\right)} \qquad (\phi_{net} \geq \frac{\pi}{6}) \tag{3.130}$$

Thus, the procedure to have constant power flow during imbalanced grid voltage is as follows:

1. Compute the positive and negative sequence voltage phasors
2. Compute the net phase shift ϕ_{net}
3. Use equation (3.128) or (3.130) depending on value of ϕ_{net} to compute $\max(f_1+f_2)$

Table 3.3: Circuit Parameters for Three phase PET simulation and experiments

Parameter	Value
DC link voltage (V_{dc})	135V
Modulation index (m)	0.2, 0.25, 0.3, 0.35, 0.4, 0.5
AC voltage frequency	60 Hz
Switching period (T_s)	200μs
δ	[-0.25,0.25] (in steps of 0.05)
Transformer turns ratio	1:1
Secondary side inductance (L)	480 μH

4. Use equation (3.124) to obtain the limits on $|\delta_+| + |\delta_-|$

5. Choose δ_+ and δ_- that satisfy equation (3.119) and the are within the limits found in step 4 in order to have constant power flow

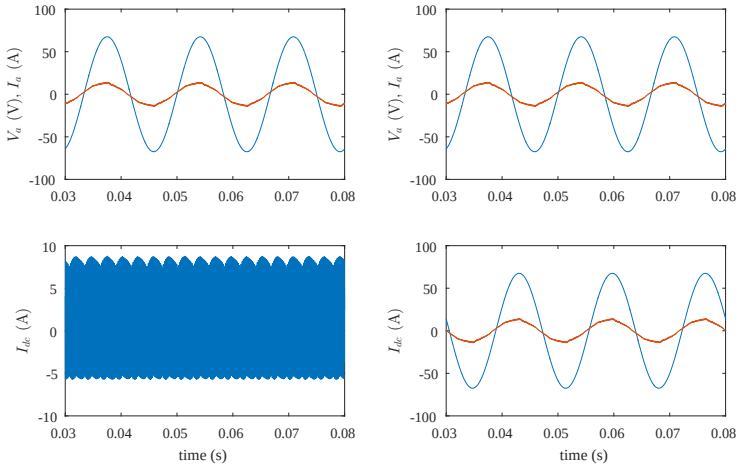
3.5 Simulation and experimental results

3.5.1 Open loop operation and soft switching

The open loop operation of the three phase PET was simulated using MATLAB Simulink with Plecs blockset. The circuit parameters are given in table 3.3. The dc link voltage V_{dc} was held fixed at 135 V and the power transfer was observed at different values of modulation index m and phase shift parameter δ. The transformer turns ratio was taken as unity and the switching deices and transformer were considered ideal.

A laboratory hardware prototype of the three phase reduced switch PET was also developed and the power transfer was observed on this prototype for same values of m and δ as used for the simulations. In the case of the hardware prototype, additional inductance was connected between the transformer secondary and the VSI to bring the total inductance to 480 μH.

The simulation results for open loop operation of the three phase PET for power transfer from ac to dc are given in Fig. 3.22. These figures are obtained for modulation index $m = 0.5$ and $\delta = 0.225$, with the other settings as previously discussed. An LCR filter used to suppress switching frequency components from the ac current, with $L = 820\mu$H, $C = 30\mu$F and $R = 18\Omega$. It is observed from Fig. 3.22(a), that the ac current is in phase with the voltage, demonstrating unity power factor operation. The

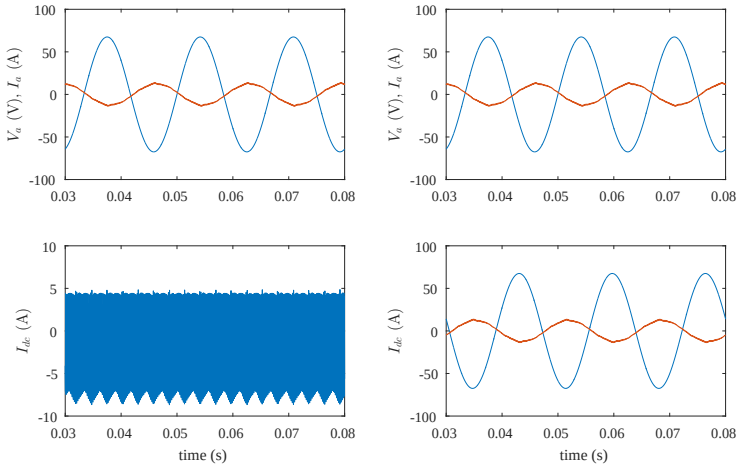


(a) (b)

Figure 3.22: Simulation results for three phase PET for power transfer from ac to dc side (a) Phase a voltage and filtered current (zoomed by 3 times) (top), dc link current (bottom) (b) Phase a voltage and filtered current (zoomed by 3 times) (top), phase b voltage and filtered current (zoomed by 3 times) (bottom)

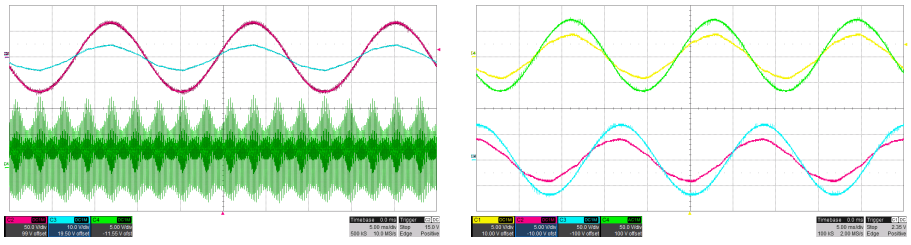
simulation results for power transfer from dc to ac side are shown in Fig. 3.23, where the same ac side filter is used. It is again observed that the ac currents are exactly out of phase with the respective phase voltages, demonstrating unity power factor operation. The experimental results corresponding to all of these simulation results for both power flow directions are shown in Fig. 3.24 and Fig. 3.25, where unity power factor operation is demonstrated.

In order to see how well the analytical values of power transfer translate to the actual PET system, simulations and experiments are done at various values of modulation index m and phase shift parameter δ, as given in table 3.3. The power transfer values obtained by simulations and experiments are then plotted together with the analytical values to observe the trend. These plots are given in Fig 3.26. It is observed that the simulation results match pretty closely with the analytical values. Both ac and dc power are plotted for experimental results, since they are different than each other due to losses in the system, which include switching device losses, resistive losses in the windings and clamp losses due to leakage energy commutation.. It is observed that the input ac power is higher than output dc power for positive values of δ. Similarly, while the output ac



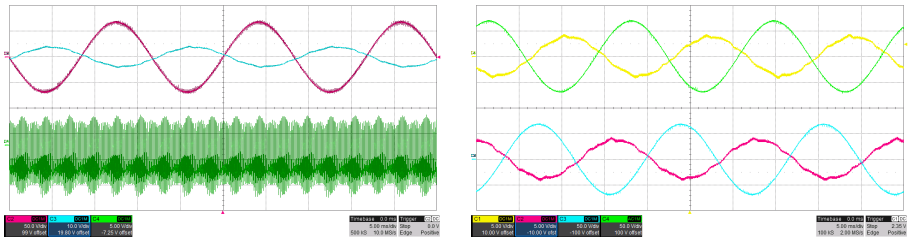
(a) (b)

Figure 3.23: Simulation results for three phase PET for power transfer from dc to ac side (a) Phase a voltage and filtered current (zoomed by 3 times) (top), dc link current (bottom) (b) Phase a voltage and filtered current (zoomed by 3 times) (top), phase b voltage and filtered current (zoomed by 3 times) (bottom)



(a) (b)

Figure 3.24: Experimental results for three phase PET for power transfer from ac to dc side (a) Phase a voltage and filtered current (top), dc link current (bottom) (b) Phase a voltage and filtered current (top), phase b voltage and filtered current (bottom)



(a) (b)

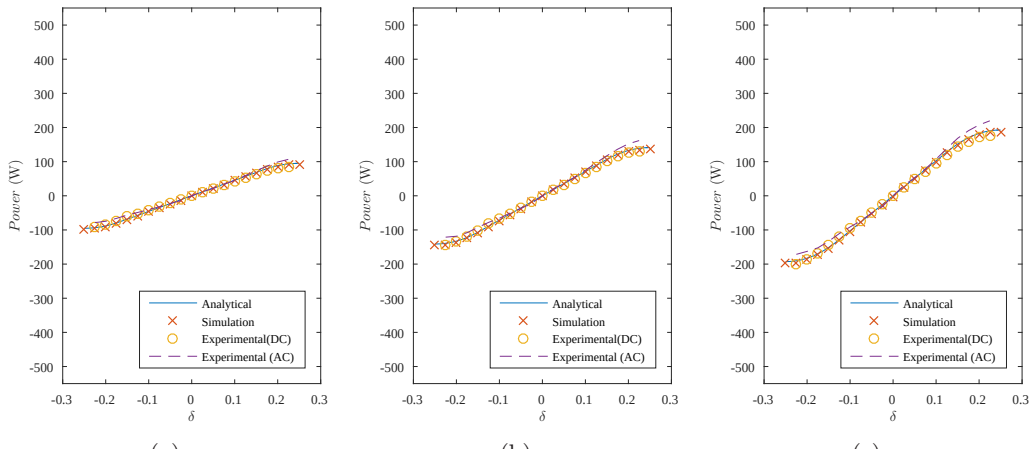
Figure 3.25: Experimental results for three phase PET for power transfer from dc to ac side (a) Phase a voltage and filtered current (top), dc link current (bottom) (b) Phase a voltage and filtered current (top), phase b voltage and filtered current (bottom)

power is lower than the input dc power for negative values of δ. However, it is observed that both of these quantities match the analytical values within reasonable limits and show the same trend as that shown by analytical values.

The simulation results to demonstrate turn ON ZVS of the secondary side VSI are given in Fig. 3.27. The experimental results for the same are shown in Fig. 3.28. A dead time of 2μs is used for the upper and lower switches of each phase leg of the secondary side VSI, both in experiments and simulations. In these figures, it is observed that for all phase X and Z switches and for the lower switch of phase Y, the voltage across a switch is negative when its gate pulse is going high. This indicates that the anti-parallel diode of the switch is conducting when it turns ON, thus achieving turn on ZVS for the switch. However, in the simulation results, in phase Y in Fig. 3.27(b), the voltage across the upper switch is equal to the dc link voltage, when its gate pulse goes high. This demonstrates that for some values of the angle α in a sector, this switch doesn't undergo turn ON ZVS and this is in agreement with the analysis. In the corresponding experimental result ins Fig. 3.28(b), it is captured for a value of α so that this switch is undergoing turn ON ZVS.

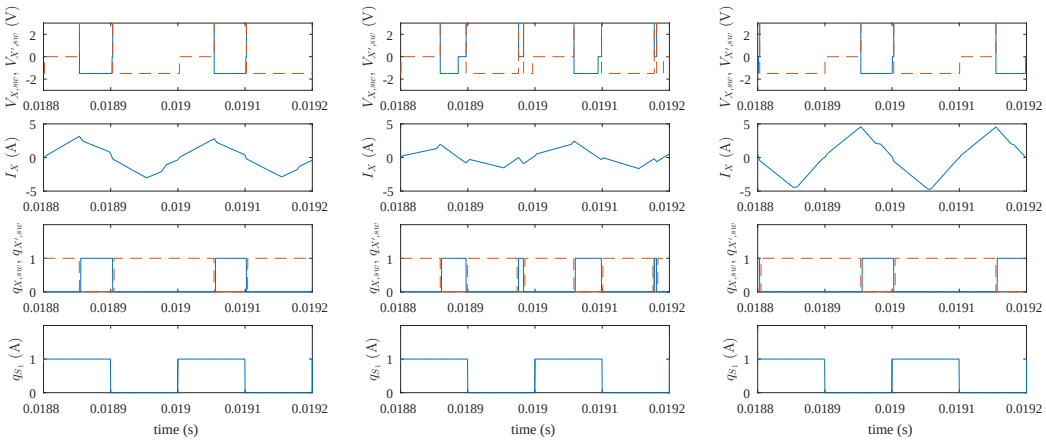
3.5.2 Closed loop operation

The closed loop control of the dc link voltage of three phase PET is simulated and also validated on the hardware prototype. The dc link voltage reference for both simulation and experiments is set to 125 V. The controller is designed about the steady state operating point with peak phase ac voltage $V_{grid} = 43.8$V rms and phase shift parameter



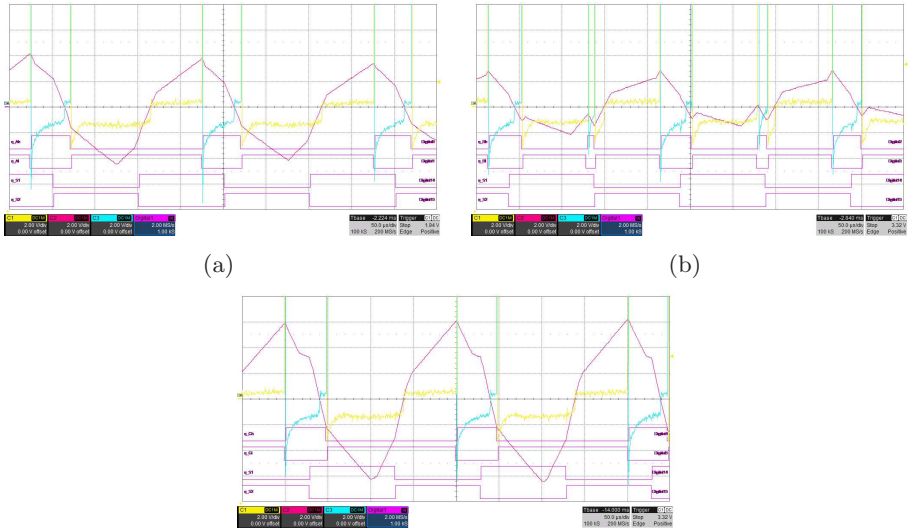
(d) (e) (f)

Figure 3.26: Comparison of analytical, simulation and experimental results for power transfer in three phase PET (a) $m = 0.2$ (b) $m = 0.25$ (c) $m = 0.3$ (d) $m = 0.35$ (e) $m = 0.4$ (f) $m = 0.5$



(a) (b) (c)

Figure 3.27: Simulation results, turn ON ZVS for secondary VSI for three phase PET (a) Voltage across top and bottom switches of phase X (top figure), gate pulses of top and bottom switches of phase X (second figure from top), transformer current through phase A inductor (third figure from top), gate pulses for primary side switch S_1 (bottommost figure) (b) Voltage across top and bottom switches of phase Y (top figure), gate pulses of top and bottom switches of phase Y (second figure from top), transformer current through phase B inductor (third figure from top), gate pulses for primary side switch S_1 (bottommost figure) (c) Voltage across top and bottom switches of phase Z (top figure), gate pulses of top and bottom switches of phase Z (second figure from top), transformer current through phase C inductor (third figure from top), gate pulses for primary side switch S_1 (bottommost figure)



(a) (b)

(c)

Figure 3.28: Experimental results, turn ON ZVS for secondary VSI for three phase PET (a) Voltage across top and bottom switches of phase X (Channels 1 and 3), transformer current through phase A inductor (Channel 2), gate pulses of top and bottom switches of phase X and for primary side switch S_1 (Digital channels) (b) Voltage across top and bottom switches of phase Y (Channels 1 and 3), transformer current through phase B inductor (Channel 2), gate pulses of top and bottom switches of phase Y and for primary side switch S_1 (Digital channels) (c) Voltage across top and bottom switches of phase Z (Channels 1 and 3), transformer current through phase C inductor (Channel 2), gate pulses of top and bottom switches of phase Z and for primary side switch S_1 (Digital channels)

$\delta = 0.17$. The dc link capacitor value was chosen as 2.5 mF. The approximate transfer function is obtained at this operating point using the procedure given in section 3.3 and then the controller is derived using this transfer function with 4Hz crossover frequency and 60° phase margin for the open loop transfer function. The PI controller parameters are obtained as $K_p = 0.0166$ and $K_i = 0.6601$.

The controller obtained as discussed in previous paragraph is used to control the dc link voltage during various transients i.e. dc link current rise and fall and ac voltage rise and fall. The simulation results for these transients are shown in Fig. 3.29 and Fig. 3.32 for ac to dc power transfer and dc to ac power transfer respectively. It should be noted that for all the results in this subsection, the dc link current is shown after the link capacitor (and hence devoid of switching ripple) to show the change in magnitude clearly. In Fig. 3.29(a), the dc link current is dropped from 2.5 A to 0.5 A and is raised back to 2.5 A in Fig. 3.29(b). The ac voltage was held unchanged with 43.8 V rms phase value for these two transients. The PI controller is able to regulate the dc link voltage to 125 V in both these transients. In Fig. 3.29(c), the rms phase ac voltage is increased from 43.8 V to 49.5 V for all three phases and is dropped back to 43.8 V in Fig. 3.29(d), while keeping dc link current unchanged. It is observed that the dc link voltage is regulated to 125 V after each of these transients occur.

The simulation results for closed loop control of dc link voltage for power transfer from dc to ac side are shown in Fig. 3.32. Similar to the ac to dc power transfer case, the control is tested for four types of transients viz. dc link current rise and fall and ac voltage rise and fall. The dc link current is increased from -2.5 A to -0.5 A in Fig. 3.32(b) and then decreased back to -2.5 A in Fig. 3.30(b). The ac voltage was held unchanged with 43.8 V rms phase value for these two transients. Also, the rms phase ac voltage is increased from 43.8 V to 49.5 V for all three phases in Fig. 3.30(c) and then decreased back to 43.8 V in Fig. 3.31(d), while keeping the dc link current unchanged. It is observed that the dc link voltage is regulated to the reference value of 125 V after each of these four transients occur.

The experimental results for closed loop control of the dc link voltage of the three phase PET are shown in Fig. 3.31 and Fig. 3.32 for ac to dc power transfer and dc to ac power transfer respectively. In Fig. 3.31(a), the dc link current is reduced from 2.5 A to 1.8 A by increasing the dc load resistance. The dc link current is increased again

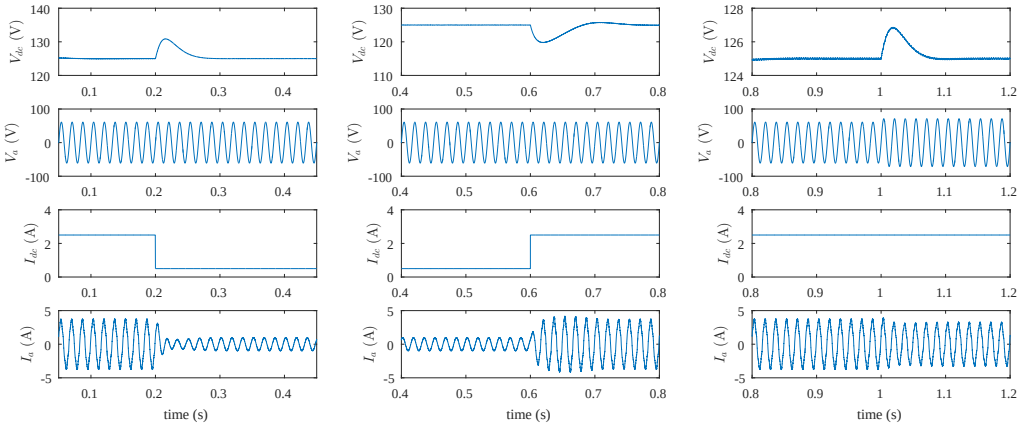
to its previous value by reducing the load resistance as seen in Fig. 3.31(b). The ac voltage was kept unchanged at 48 V rms phase value. In Fig. 3.31(c), the rms phase ac voltage is increased from 43 V to 48 V for all three phases and is again reduced to 43 V in Fig. 3.31(d). It is observed that the dc link voltage is regulated to the reference value of 125 V for all the four transitions.

A dc generator is used a dc current source while testing the closed loop dc link voltage control for dc to ac power transfer. In Fig. 3.32(a), the dc link current is reduced from -4 A to -5 A with the ac voltage held fixed at 48 V rms phase value, while it is increased to -4 A in Fig. 3.32(a), again keeping the ac voltage unchanged. Also, the peak phase ac voltage is reduced from 48 V to 35 V rms phase value (all three phases) as seen in Fig. 3.31(c) and raised back to 48 V, while keeping the dc generator output unchanged. It is observed that the dc link voltage is regulated to 125 V for all four transients.

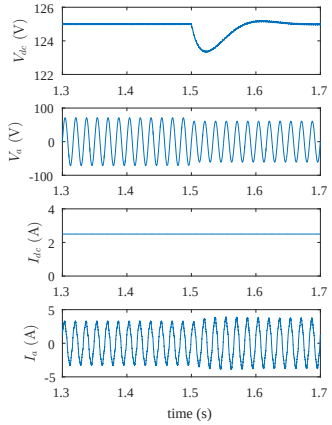
3.5.3 Unbalanced grid voltage operation

The method proposed in section 3.4 for operation of the three phase PET during unbalanced ac voltages on the primary side is tested in simulations and on the laboratory prototype. The dc link voltage was kept at 100 V for these tests. An unbalance in the ac voltages was introduced by reducing the phase c voltage to 14.2 V rms, while keeping phase a and b voltages at 34.5 V rms respectively. The phase angles between the three voltages was kept at 120°. This creates a positive sequence voltage of 28.3 V rms phase value, a negative sequence voltage of 7.1 V rms phase value and a zero sequence voltage with 7.1 V rms phase value. The values of δ for positive and negative sequence were chosen as $\delta_+ = 0.14$ and $\delta_- = -0.13$ respectively for power transfer from ac to dc side. For power flow from dc to ac side, the values of δ are changed in sign, i.e. $\delta_+ = -0.14$ and $\delta_- = 0.13$. The transformer secondary inductance was $L = 480\mu$H.

The simulation results for unbalanced grid voltage operation for the settings discussed above are given in Fig. 3.33 for power transfer from ac to dc side. In Fig. 3.33(a), the VSI generates voltages only for the positive sequence with phase shift $\delta_+ = 0.14$. Thus, power transfer occurs only due to positive sequence, which leads to a second harmonic in the dc link current, as seen in the frequency spectrum in top picture in Fig. 3.33(c). In Fig. 3.33(b), the VSI generates voltages for both positive and negative



(a) (b) (c)



(d)

Figure 3.29: Simulation results for closed loop operation of three phase PET for power transfer from ac to dc side (a) DC link current fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (b) DC link current rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (c) AC voltage rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (d) AC voltage fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure)

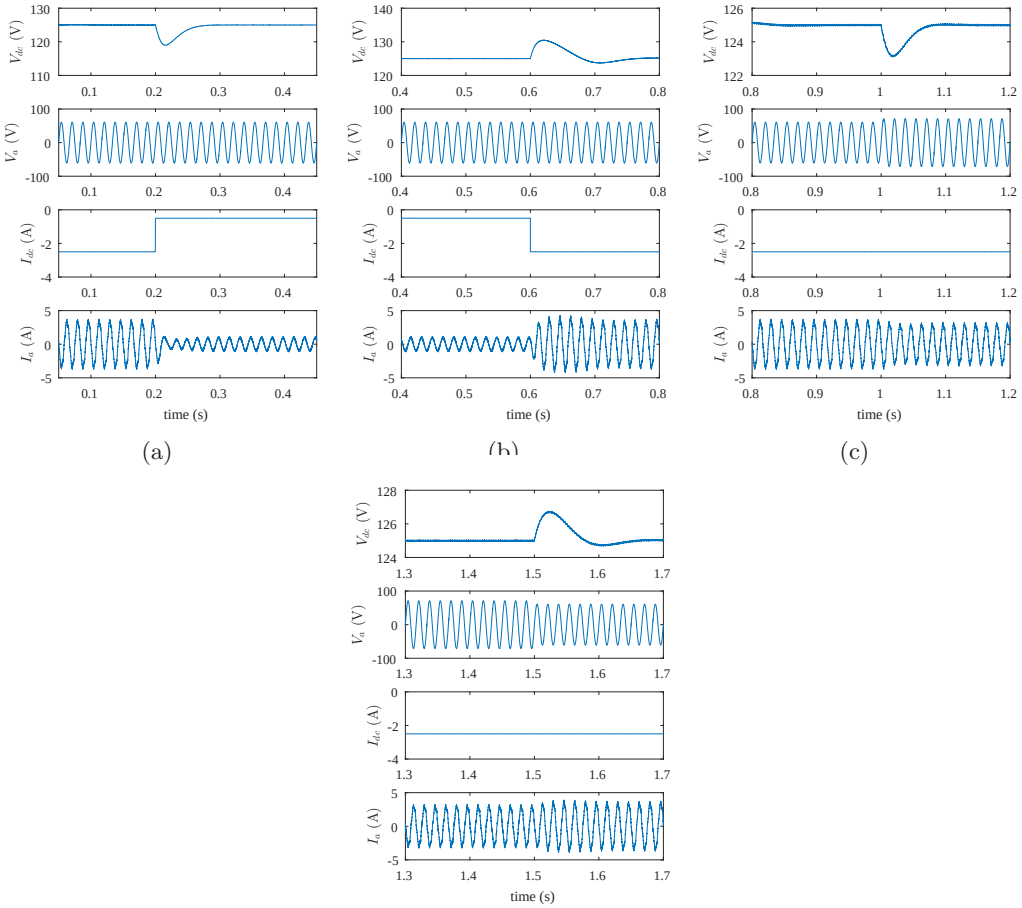
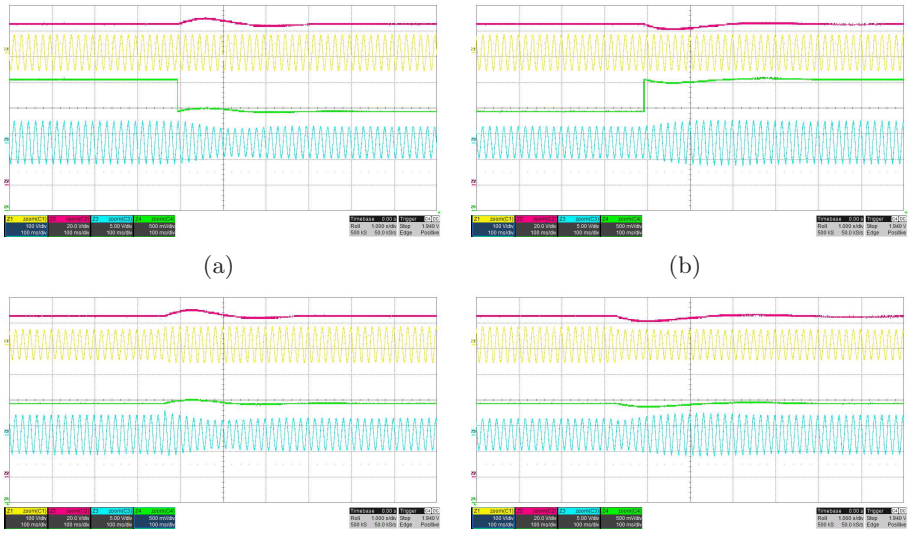


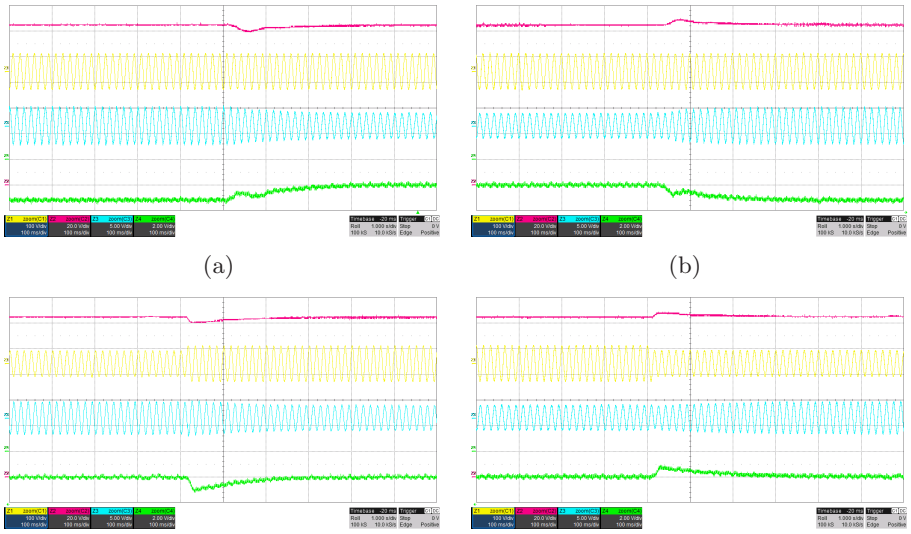
Figure 3.30: Simulation results for closed loop operation of three phase PET for power transfer from dc to ac side (a) DC link current rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (b) DC link current fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (c) AC voltage rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (d) AC voltage fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure)



(a) (b)

(c) (d)

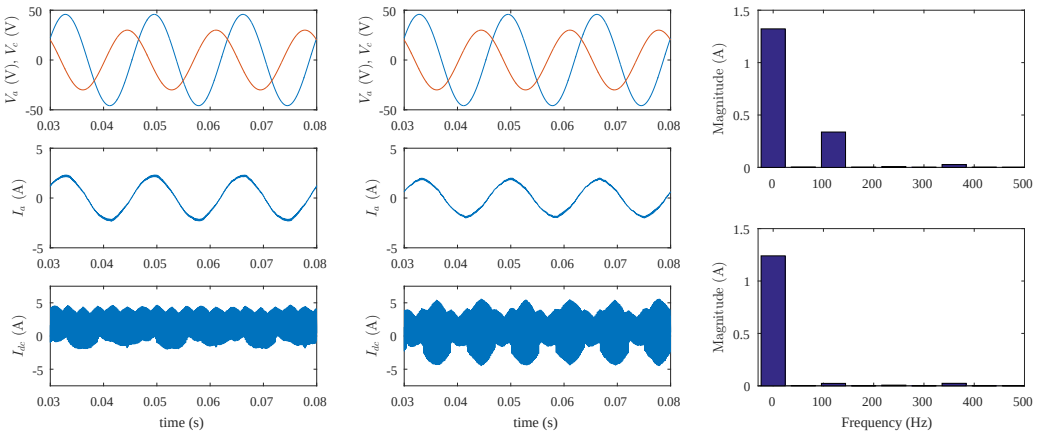
Figure 3.31: Experimental results for closed loop operation of three phase PET for power transfer from ac to dc side (a) DC link current fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (b) DC link current rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (c) AC voltage rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (d) AC voltage fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure)



(a) (b)

(c) (d)

Figure 3.32: Experimental results for closed loop operation of three phase PET for power transfer from dc to ac side (a) DC link current fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (b) DC link current rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (c) AC voltage rise: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure) (d) AC voltage fall: dc link voltage (top figure), phase a ac voltage (second figure), dc link current (third figure), phase a ac current (bottom figure)

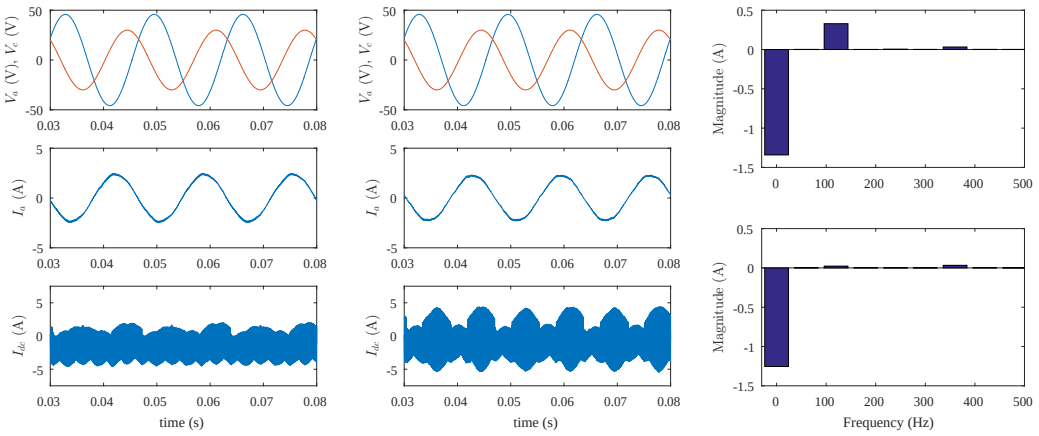


(a) (b) (c)

Figure 3.33: Simulation results for unbalanced grid voltage operation of three phase PET, for power transfer from ac to dc side (a) No compensation used: phase a and c voltages (top picture), phase a ac current (second figure) (b) dc link current (bottom figure) (b) With compensation: phase a and c voltages (top picture), phase a ac current (second figure), dc link current (bottom figure) (c) Frequency spectra of dc link currents without compensation (top figure) and with compensation (bottom figure)

sequence and the second harmonic from the dc link current is nearly gone, as seen in the bottom figure in Fig. 3.33(c). The corresponding simulation results for power transfer from dc to ac side have been presented in Fig. 3.34.

The experimental results for unbalanced grid voltage operation for power transfer from ac to dc side are given in Fig. 3.35. A second harmonic in the dc link current in Fig. 3.35(a) is observed, where the VSI generated only positive sequence voltages. This second harmonic is by a factor of three from 0.36 A to 0.12 A, when the VSI generates voltages for both positive and negative sequences as observed in Fig. 3.35(b). This is seen in the frequency spectra of the dc link currents for both cases, in Fig. 3.35(c). The experimental results are shown in Fig. 3.36 for the case of power transfer from dc to ac side. It is observed that the second harmonic component reduces from 0.34 A to 0.13 A, again by a factor of three when the VSI is used to generate both positive and negative sequence voltages as seen in Fig. 3.36(b), compared to when used only to generate positive sequence voltages as in Fig. 3.36(a). The frequency spectra of the dc currents for the two cases are given in Fig. 3.36(c).



(a) (b) (c)

Figure 3.34: Simulation results for unbalanced grid voltage operation of three phase PET, for power transfer from dc to ac side (a) No compensation used: phase a and c voltages (top picture), phase a ac current (second figure) (b) dc link current (bottom figure) (b) With compensation: phase a and c voltages (top picture), phase a ac current (second figure), dc link current (bottom figure) (c) Frequency spectra of dc link currents without compensation (top figure) and with compensation (bottom figure)

3.6 Conclusion

In this chapter, the operation of the three phase reduced switch PET was studied for ac to dc power conversion. Analytical results showed that the PET power transfer capability is increase nearly by a factor of four when operating the PET in Region 4, as opposed to previously studied Region 1. Simulations and hardware tests were done at multiple operation points and the power transfer values were found to be following the same trend as shown by the analytical expressions, within limits of experimental error. In addition, a method was proposed to design a PI controller to control the link voltage of dc side of the PET and was validated through simulations and experiments. Finally, a technique was developed and proven through simulations and experiments for reducing second harmonic in the dc link current for reduce the variation in power flow during imbalanced grid voltage operation.

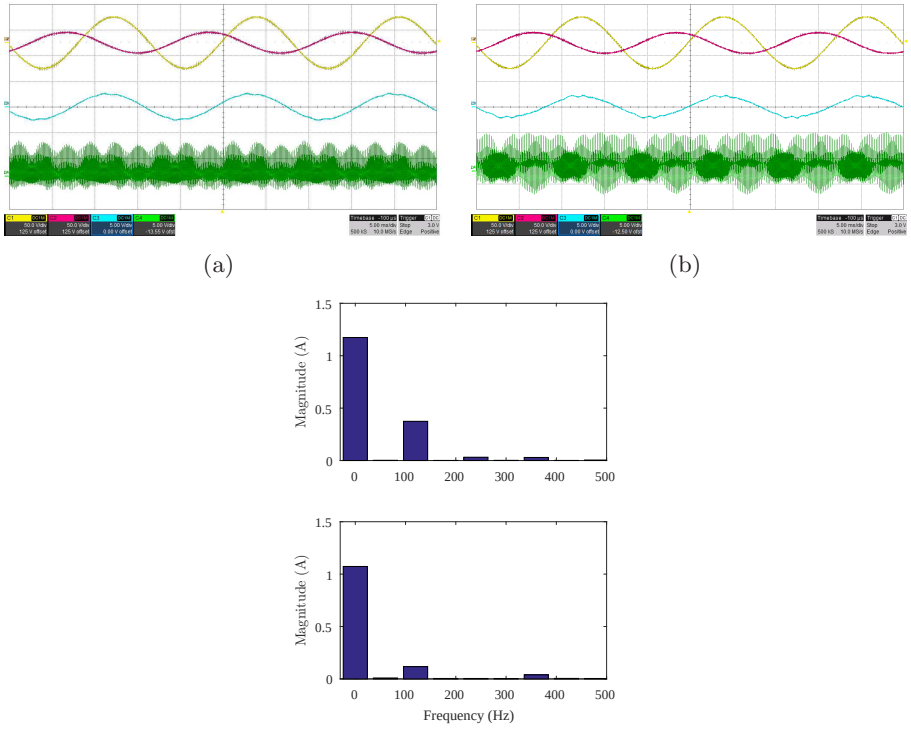


Figure 3.35: Experimental results for unbalanced grid voltage operation of three phase PET, for power transfer from ac to dc side (a) No compensation used: phase a and c voltages (top picture), phase a ac current (second figure) (b) dc link current (bottom figure) (b) With compensation: phase a and c voltages (top picture), phase a ac current (second figure), dc link current (bottom figure) (c) Frequency spectra of dc link currents without compensation (top figure) and with compensation (bottom figure)

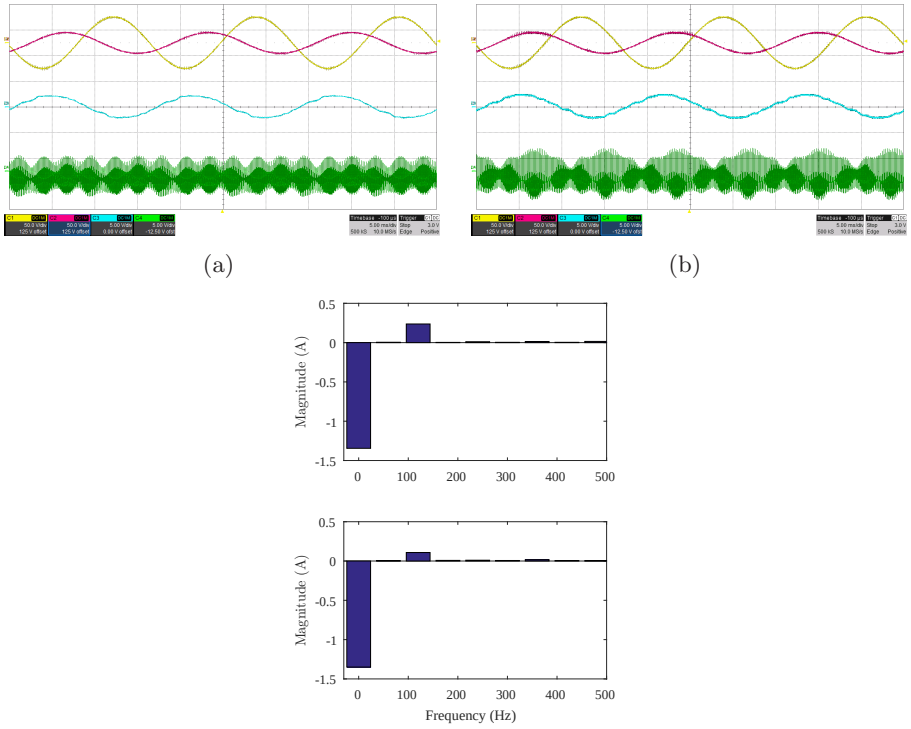


Figure 3.36: Experimental results for unbalanced grid voltage operation of three phase PET, for power transfer from dc to ac side (a) No compensation used: phase a and c voltages (top picture), phase a ac current (second figure) (b) dc link current (bottom figure) (b) With compensation: phase a and c voltages (top picture), phase a ac current (second figure), dc link current (bottom figure) (c) Frequency spectra of dc link currents without compensation (top figure) and with compensation (bottom figure)

Chapter 4

Carrier based implementation of Space Vector Pulse Width Modulation for Open-end Winding Two level inverter drives

Two level voltage source inverters are one of the most widespread power electronic converters, used for dc to 3 phase ac conversion. Pulse Width Modulation or PWM is used to regulate the output voltage in these converters. Conventional Space Vector PWM (CSVPWM) [64, 65] is commonly used to modulate these converters due to high quality of the output voltage waveform. But CSPWM modulated two level VSIs apply switching common mode voltage at load terminals leading to bearing currents, failure of the shaft and conducted electromagnetic interferences [11–13].PWM schemes have been proposed that aim at minimizing or eliminating the common mode voltage switching [66]. It is possible to modulate the VSI without switching the common mode voltage, but such a modulation leads to poor quality of the output voltage waveform along with the reduction in the voltage gain [67]. Multilevel converters have also been explored for common-mode voltage elimination: for example [68], [66] for three level neutral point clamped converter (NPC), [69] for five level NPC and [70] for cascaded multilevel inverters. A dual two level inverter with a PWM scheme proposed in [24]

completely eliminates the switching common mode voltage with a quality of the output voltage waveform similar to CSVPWM. The voltage gain is $\sqrt{3}$ times that of CSVPWM modulated single VSI.

A carrier based implementation of CSVPWM has been presented in [71] and [72]. It obviates the need for output voltage vector's magnitude and position determination and the subsequent calculations needed for duty ratios, thus making the implementation process simpler while giving the same output. The switching signals are obtained directly from the reference modulation signals. In this chapter, a carrier based algorithm will be presented for the dual two level inverter PWM scheme in [24] that leads to common mode voltage elimination. The derivation of the scheme will be described and then the benefits of the carrier based implementation over the space vector will be discussed.

4.1 Dual Two Level Inverter and zero common mode voltage space vectors

A dual two level inverter drive comprises one two level inverter on each side of the three phase load as shown in Fig.4.1.

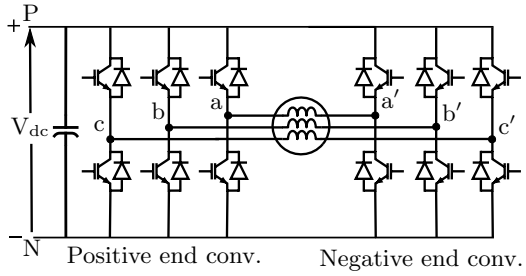


Figure 4.1: Dual 2 level inverter drive

The two inverters are called positive and negative end converters. They share the same dc bus, the positive and negative terminals of which are denoted by P and N respectively. The load terminals connected to positive end and negative end converters are labeled as a, b, c and a′, b′, c′ respectively. The space vectors of positive end and negative end converters are shown in Fig 4.2. We observe that the vectors of the negative end converter are opposite in direction to those of the positive end converter.

The voltage vector synthesized at positive end of the load is given in (4.1).

$$\mathbf{V_{PE}} = V_{aN} + V_{bN}e^{j\frac{2\pi}{3}} + V_{cN}e^{j\frac{4\pi}{3}} \tag{4.1}$$

The positive end converter has six active vectors or switching states, which are produced by the a, b, c terminals connected to either P or N. So when terminal a and b are connected to

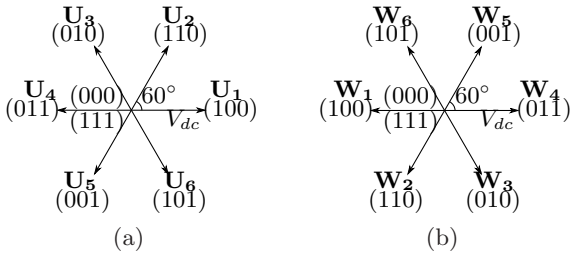


Figure 4.2: Space vectors (a)Positive End conv. (b)Negative End conv.

P while c is connected to N, the voltages V_{aN} and V_{bN} are V_{dc} while the voltage V_{cN} is zero. Thus, the voltage vector $\mathbf{U_2}$ is synthesized which has magnitude V_{dc} at an angle of sixty degrees. Similarly, the voltage vector synthesized by the negative end converter is given in (4.2).

$$\mathbf{V_{NE}} = -(V_{a'N} + V_{b'N}e^{j\frac{2\pi}{3}} + V_{c'N}e^{j\frac{4\pi}{3}}) \tag{4.2}$$

When terminal a$'$ is connected to P while b$'$ and c$'$ are connected to N, the voltage $V_{a'N}$ is V_{dc} while the voltages $V_{b'N}$ and $V_{c'N}$ are zero. Thus, the voltage vector $\mathbf{W_1}$ is synthesized which has a magnitude of V_{dc} and is at an angle of 180 degrees. The positive end common mode voltage is defined as

$$V_{PE,com} = \frac{V_{aN} + V_{bN} + V_{cN}}{3}$$

and the negative end common mode voltage is defined as

$$V_{NE,com} = \frac{V_{a'N} + V_{b'N} + V_{c'N}}{3}$$

Based on above expressions, the vectors $\mathbf{V_1}$, $\mathbf{V_3}$ and $\mathbf{V_5}$ have equal common mode

voltage viz. $V_{dc}/3$ while the vectors $\mathbf{V_2}$, $\mathbf{V_4}$ and $\mathbf{V_6}$ have equal common mode voltage viz. $2V_{dc}/3$. The common mode voltage across the three phase load is given by $V_{PE,com} - V_{NE,com}$. The zero sequence currents through the load should be zero. This implies that the common mode voltage across the load terminals should be zero at all times. In order to eliminate switching common mode voltage, either we can use $\mathbf{U_1}$, $\mathbf{U_3}$ and $\mathbf{U_5}$ from the positive end and $\mathbf{W_1}$, $\mathbf{W_3}$ and $\mathbf{W_5}$ from the negative end converter. Alternatively, we could use the voltage vectors $\mathbf{U_2}$, $\mathbf{U_4}$ and $\mathbf{U_6}$ from the positive end converter and vectors $\mathbf{W_2}$, $\mathbf{W_4}$ and $\mathbf{W_6}$ from the negative end converter. When either of these sets of vectors are being used, the common mode voltage across the load is zero. We will select the first set for our discussion. The six vectors in this set can be combined to produce the resultant six vectors of the dual converter as shown in Fig.4.3.

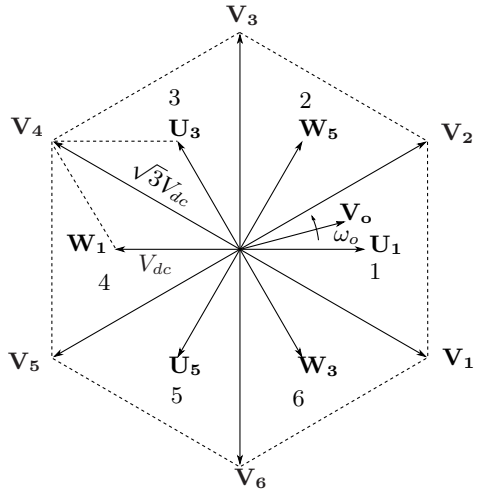


Figure 4.3: Resultant and individual converter space vectors

The resultant vectors are of magnitude $\sqrt{3}V_{dc}$ and are shifted by 30° counterclockwise with respect to the individual converter space vectors. Thus, the sectors are also shifted by the same amount. They form six sectors which are also labeled in the figure as 1 through 6. The average output phase voltages to be synthesized across the load

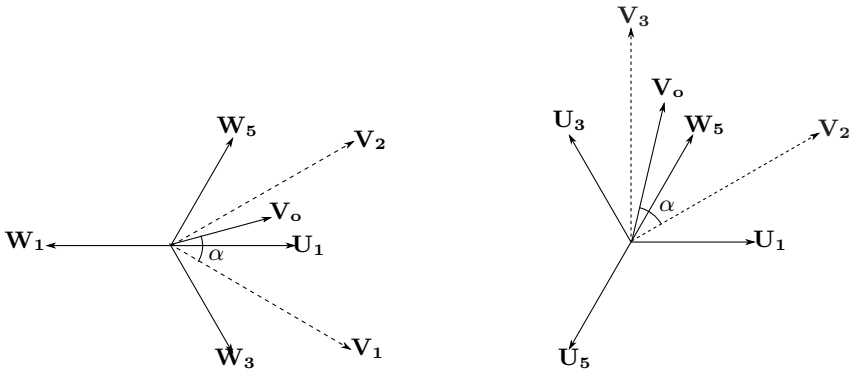
are given by (4.3)

$$\begin{aligned}\overline{v}_{\mathrm{aa'}} &= V_o \cos(\omega t) \\ \overline{v}_{\mathrm{bb'}} &= V_o \cos(\omega t - \frac{2\pi}{3}) \\ \overline{v}_{\mathrm{cc'}} &= V_o \cos(\omega t + \frac{2\pi}{3})\end{aligned} \tag{4.3}$$

where ω is the output angular frequency and V_o is the peak of the output phase voltages. These values can be used to construct the output voltage vector as:

$$\mathbf{V}_o = \overline{v}_{\mathrm{aa'}} + \overline{v}_{\mathrm{bb'}} e^{j\frac{2\pi}{3}} + \overline{v}_{\mathrm{cc'}} e^{j\frac{4\pi}{3}} = \frac{3}{2} V_o e^{j\omega t} \tag{4.4}$$

So, the output voltage vector as in (4.4), is of magnitude $\frac{3}{2}V_o$ and rotates at an angular speed of ω in counterclockwise direction. The output voltage vector can be in any of these six sectors and once the sector is identified, the two adjacent active vectors are used to synthesize the average output voltage vector in one sampling time period. If the total time of active vectors is less than the sampling time period, a zero vector is applied for the remaining time, which is realized by vectors $\mathbf{U_1}$ and $\mathbf{W_1}$ or $\mathbf{U_3}$ and $\mathbf{W_3}$ or $\mathbf{U_5}$ and $\mathbf{W_5}$. Let us consider the case where the output voltage vector is in the first sector. This situation is shown in Fig.4.4(a).



(a) $\mathbf{V_o}$ in Sector 1 (b) $\mathbf{V_o}$ in Sector 2

Figure 4.4: Output voltage vector $\mathbf{V_o}$ in different sectors

In sector 1, output voltage vector is synthesized by the vectors $\mathbf{V_1}$ and $\mathbf{V_2}$ as shown

in (5.12).

$$d_1\mathbf{V_1} + d_2\mathbf{V_2} = \mathbf{V_o} \tag{4.5}$$

where d_1 and d_2 are the duty ratios of $\mathbf{V_1}$ and $\mathbf{V_2}$ respectively. This means that $\mathbf{V_1}$ is applied for time d_1T_s and $\mathbf{V_3}$ is applied for time d_2T_s where T_s is the sample time period. The zero vector used in this sector is obtained by applying $\mathbf{U_1}$ and $\mathbf{W_1}$ for the remaining time period. Thus, we see that the vector $\mathbf{U_1}$ of positive end converter is applied for whole time while the vectors $\mathbf{W_1}$, $\mathbf{W_3}$ and $\mathbf{W_5}$ of negative end converter are ON for times $(1 - d_1 - d_2)T_s$, d_1T_s and d_2T_s respectively.

4.2 Derivation of carrier based expressions for the duty ratios

In the previous sections, the vectors to be used in the modulation have been discussed. The technique to synthesize the output voltage using space vector approach requires following steps:

Determination of the magnitude and angle of the average output voltage vector $\mathbf{V_o}$

Determination of the sector the output voltage vector is in and the angle α made by $\mathbf{V_o}$ with the starting space vector for the determined sector

Determination of the duty ratios d_1 and d_2 and d_z

Determination of the switching states for both two level inverters to be applied for different fractions of sampling period.

The first step in above process requires an inverse trigonometric operation and a square root operation. The third step requires computation with trigonometric functions. In this section, we will discuss the carrier based technique that obviates the need to determine these output voltage vector characteristics and hence the subsequent computations for the duty ratios. The technique is motivated from the min. max. mid. technique used in conventional Space Vector PWM for a two level inverter [71]. We begin by

stating that at any instant the reference output phase voltages across the load i.e. $V_{aa'}$, $V_{bb'}$ and $V_{cc'}$ are balanced, resulting in (4.6).

$$V_{aa'} + V_{bb'} + V_{cc'} = 0 \tag{4.6}$$

Now from Fig.4.4(a), we have

$$\begin{aligned} \mathbf{V_1} &= \sqrt{3}V_{dc}e^{-j\frac{\pi}{6}} \text{and} \\ \mathbf{V_2} &= \sqrt{3}V_{dc}e^{j\frac{\pi}{6}} \end{aligned} \tag{4.7}$$

Using (5.12), (4.4) and (4.7), we get

$$\sqrt{3}V_{dc}(d_1e^{-j\frac{\pi}{6}} + d_2e^{j\frac{\pi}{6}}) = V_{aa'} + V_{bb'}e^{j\frac{2\pi}{3}} + V_{cc'}e^{j\frac{4\pi}{3}} \tag{4.8}$$

Comparing real and imaginary parts in (4.8) and using (4.6), we get (4.9) and (4.10).

$$d_1 = -\frac{V_{bb'}}{V_{dc}} \tag{4.9}$$

$$d_2 = -\frac{V_{cc'}}{V_{dc}} \tag{4.10}$$

The above computation is repeated for all the six sectors and Table 4.1 is obtained.

Table 4.1: Duty ratios d_1, d_2 for six sectors

Sector	d_1	d_2
1	-$m_{bb'}$	-$m_{cc'}$
2	$m_{aa'}$	$m_{bb'}$
3	-$m_{cc'}$	-$m_{aa'}$
4	$m_{bb'}$	$m_{cc'}$
5	-$m_{aa'}$	-$m_{bb'}$
6	$m_{cc'}$	$m_{aa'}$

where

$$m_{ii'} = \frac{\overline{v}_{\mathrm{ii'}}}{V_{dc}},\ i \in \{a, b, c\} \tag{4.11}$$

Next, we identify a pattern in the output voltage waveforms to design an algorithm

to send the duty ratios to the proper power switches. The three phase output reference voltage waveforms is shown in Fig.4.5.

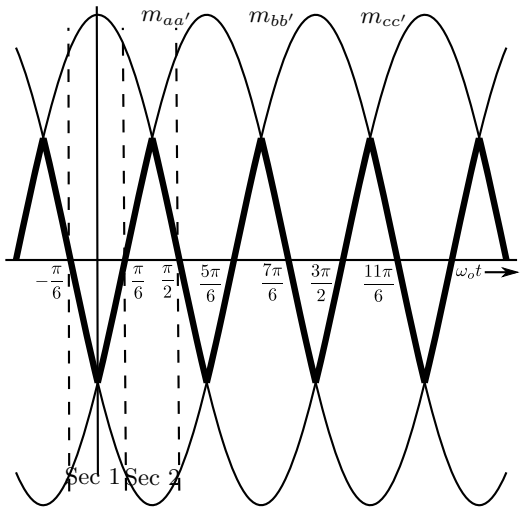


Figure 4.5: 3-phase output reference voltage waveform

The waveform with medium value of the three waves is made bold. The first and second sectors, which span from $\omega t = -\frac{\pi}{6}$ to $\omega t = \frac{\pi}{6}$ and $\omega t = \frac{\pi}{6}$ to $\omega t = \frac{\pi}{2}$ respectively are marked by the vertical dashed lines and labeled **Sec 1** and **Sec 2**. We make the following observations in the first sector:

The medium voltage is negative in sign.

Phase a is maximum. From Fig.4.4(a), the positive end converter is clamped to the switching state (100). Thus, the output leg a of the positive end converter is always ON, i.e. the duty ratio d_a is 1. The other two legs are always OFF, i.e. $d_b = d_c = 0$.

From Fig.4.4(a) and Table 1, the duty ratios for the legs of negative end converter corresponding to non-maximum phases i.e. $d_{b'}$ and $d_{c'}$ are equal to $-m_{bb'}$ $-m_{cc'}$ respectively.

The duty ratio for the leg of the negative end converter corresponding the maximum phase i.e. $d_{a'}$ is $1 - (-m_{bb'} - m_{cc'}) = 1 - m_{aa'}$.

In the second sector, following observations are made:

The medium voltage is positive in sign.

Phase c is minimum. From Fig.4.4(b), the negative end converter is clamped to the switching state (001). Thus, the output leg c′ of the positive end converter is always ON, i.e. the duty ratio $d_{c'}$ is 1. The other two legs are always OFF, i.e. $d_{b'} = d_{c'} = 0$.

From Fig.4.4(b) and Table 1, the duty ratios for the legs of positive end converter corresponding to non-minimum phases i.e. d_a and d_b are equal to $m_{aa'}$ $m_{bb'}$ respectively.

The duty ratio for the leg of the positive end converter corresponding the minimum phase i.e. d_a is $1 - (m_{aa'} + m_{bb'}) = 1 + m_{cc'}$.

Similar observations in other four sectors give Table 4.2.

Table 4.2: Phase duty ratio based on min max values

Duty ratio	mid>0		mid<0	
	a is min	a isn't min	a is max	a isn't max
d_a	$1 + m_{aa'}$	$m_{aa'}$	1	0
$d_{a'}$	1	0	$1 - m_{aa'}$	$-m_{aa'}$
	b is min	b isn't min	b is max	b isn't max
d_b	$1 + m_{bb'}$	$m_{bb'}$	1	0
$d_{b'}$	1	0	$1 - m_{bb'}$	$-m_{bb'}$
	c is min	c isn't min	c is max	c isn't max
d_c	$1 + m_{cc'}$	$m_{cc'}$	1	0
$d_{c'}$	1	0	$1 - m_{cc'}$	$-m_{cc'}$

So, first we need to find the sign of the medium value. Once that is identified, we find which phase is minimum or maximum, depending on whether the medium voltage is positive or negative respectively. Then we can use Table 4.2 to get the duty ratios of all the six legs. This process is shown in flowchart format in Fig.4.6.

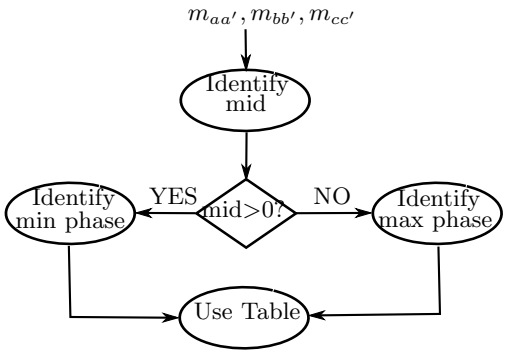


Figure 4.6: Algorithm flowchart

After we have determined the duty ratios for all the six legs of both converters, we can pick duty ratios of two legs for both converters. Then we process them in the following way to produce the gate pulses for three legs:

Add duty ratios d_a and d_b and call it d_{ab}.

Compare d_{ab} and d_a with the carrier to produce pulses q_{ab} and q_a respectively.

The pulse for leg b is given by q_{ab}AND (NOTq_a).

The pulse for leg c is given by NOTq_{ab}

The above process can be repeated with $d_{a'}$ and $d_{b'}$ to produce the gate pulses for the legs of the negative end converter. This method is simple, but it fixes the order of the output phase pulses (order being cbabc in this case) and doesn't keep the zero vector centered. To get the pulses in the 0120210 order, the following method could be used:

Determine the sign of the medium voltage.

If medium voltage is positive, determine which phase is minimum. If medium voltage is negative, determine which phase is maximum. This gives the sector. Based on the tables 4.2 and 4.3, get the duty ratios d_1, d_2 and d_z and which phases they are going to.

Compare the duty ratios with a carrier to produce pulses as shown in Fig.4.7.

Send the pulses based on the the information in second step to the inverter legs.

Table 4.3: Duty ratio distribution based on sector

Mid<0 & Max phase	Sector	Inverter leg q_1 goes to	Inverter leg q_2 goes to	Inverter leg q_z goes to
A	1	b′	c′	a′
B	3	c′	a′	b′
C	5	a′	b′	c′
Mid>0 & Min phase	Sector	Inverter leg q_1 goes to	Inverter leg q_2 goes to	Inverter leg q_z goes to
A	4	b	c	a
B	6	c	a	b
C	2	a	b	c

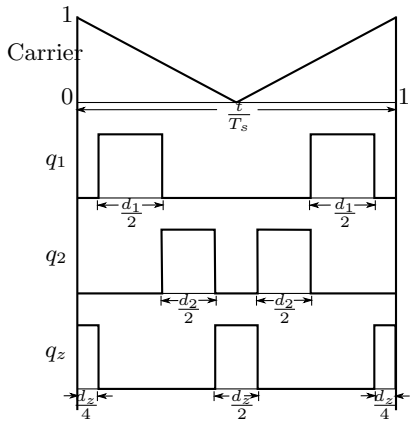


Figure 4.7: Pulses with centering of zero vector

4.3 Simulation and experimental results

The modulation scheme for the dual converter is implemented using the proposed algorithm and simulated on MATLAB Simulink. In addition, the proposed method was also implemented on a laboratory scale hardware prototype. The conditions for the simulation are shown in table below: The simulation results for dual two-level inverter are shown in Fig. 4.8, Fig. 4.9 and Fig. 4.10. The positive end and negative end pole voltages and common-mode voltage are shown in Fig. 4.8(a) and Fig. 4.8(b) respectively. The voltages across output phases and differential common-mode voltage is shown in

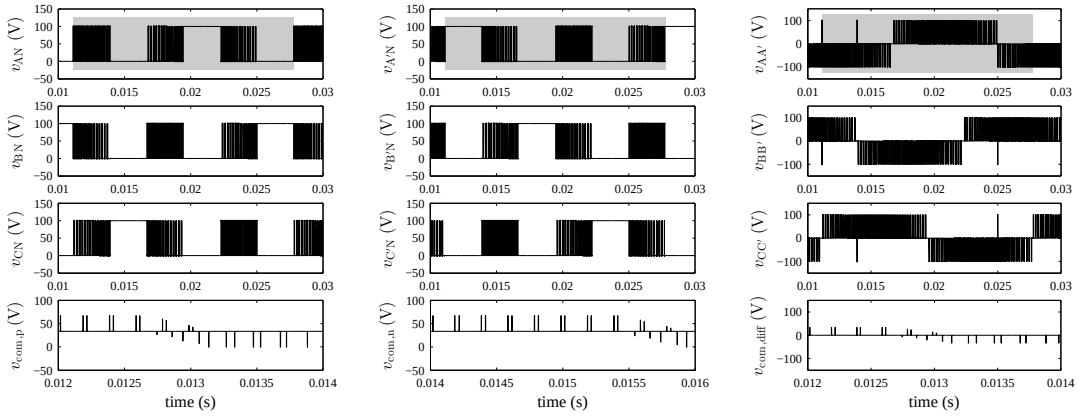
Table 4.4: Simulation and experimental parameters for dual two-level inverter drive

Parameter	Value
DC bus voltage	100 V
Output voltage (line-line rms)	87 V
Output frequency	60 Hz
Switching frequency	5 kHz
Load	$31.0\angle 39.0^\circ\ \Omega$

Fig. 4.8(c). Dead times and device drops have been included in the simulations to remain close to experimental conditions. It is observed that barring the small glitches due to device drops and dead times [73], the positive and negative end common-mode voltages are held flat at 33.33 V, which is equal to $\frac{1}{3}$rd of the dc bus voltage V_{dc}. Thus their average sum and difference should also have constant values (ignoring non-idealities), which should help in mitigating the problems of circulating currents and EMI. In all these figures, a gray patch has been drawn in the top graph to denote one cycle of the output fundamental frequency ω_o. In Fig. 4.9, the positive end and negative end pole voltages and voltage across output phases have been shown for one switching cycle for easier viewing. Fig. 4.10(a) displays the output currents and the circulating current. The output currents appear balanced and sinusoidal as desired, while the circulating current is much smaller than the output currents. The Fourier spectra of voltage $v_{\mathrm{AA}'}$ across output phase A are shown in Fig. 4.10(b) for carrier based and space vector based techniques respectively. The spectra are nearly identical, which implies that the carrier based method generates identical pulses to that of space vector approach.

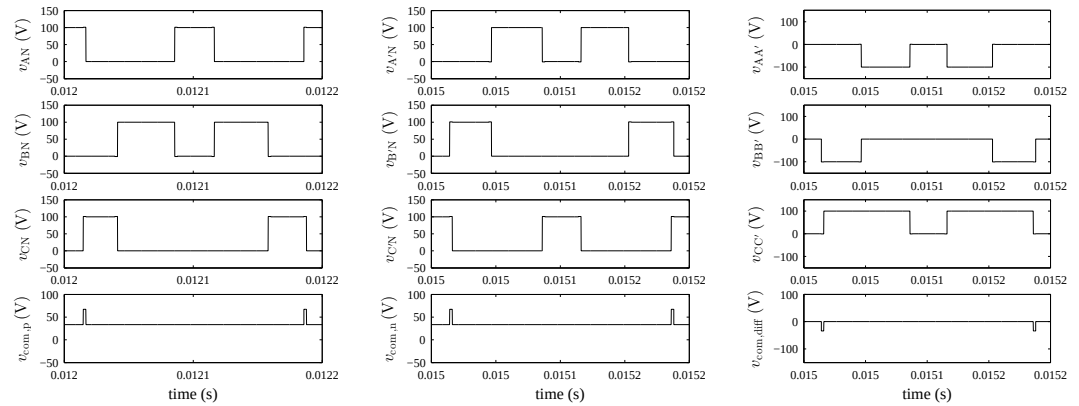
Lastly, the Fourier spectra of voltage across load phase A are shown for dual VSI with CMV elimination and single VSI using conventional SVPWM (all eight vectors) in Fig. 4.10(c). It is seen that they are nearly identical, indicating that the differential mode power quality of dual VSI with CMV elimination is same as that of single VSI with conventional PWM.

The dual two-level inverter was built using two Microsemi APTGF90TA60PG IGBT modules. The gate drivers used are Concept 6SD106EI. The proposed PWM technique was implemented using a Digilent Spartan 3 Starter board with Xilinx XC3S1000 FPGA. A diagram of the circuit is given in Fig. 4.11. A dead band of 2 μs is present between



(a) (b) (c)

Figure 4.8: Simulation results for Dual two-level inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) (b)Negative end pole voltages (top three graphs) and CMV (bottom graph) (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load



(a) (b) (c)

Figure 4.9: Simulation results (Zoomed voltages for Dual two-level inverter) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) (b)Negative end pole voltages (top three graphs) and CMV (bottom graph) (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load

the pulses of upper and lower switch of any leg in the inverter.

The experimental results for dual two-level inverter are given in Fig. 4.12 and Fig.

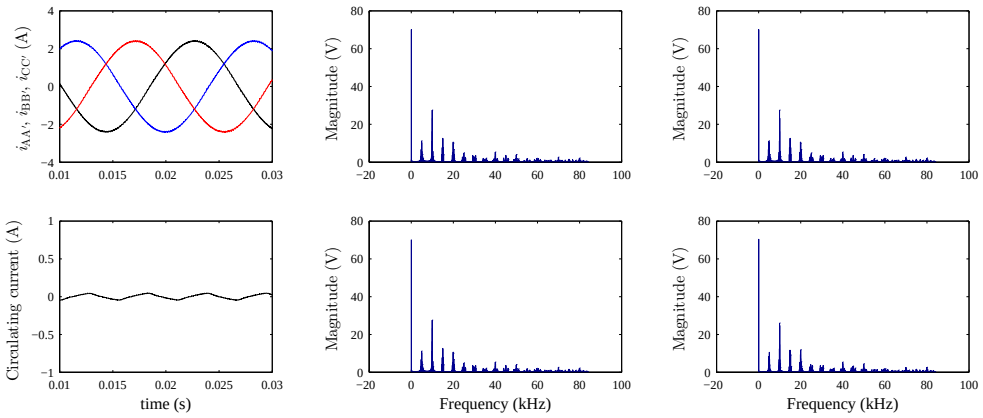


Figure 4.10: Simulation results (dual two-level inverter) (a) Three phase load currents (top graph) and circulating current (bottom graph) (b) Fourier spectrum of voltage $v_{AA'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph) (c) Fourier spectrum of voltage $v_{AA'}$ across phase A for dual VSI (top graph) and Fourier spectrum of output phase voltage v_{An} in single VSI (bottom graph)

4.13. The positive end and negative end pole voltages and common-mode voltage are shown in Fig. 4.12(a) and Fig. 4.12(b). The voltages across output phases and the differential common-mode voltage are shown in Fig. 4.12(c). A gray patch in the top graphs of these three figures indicates one cycle of output fundamental frequency. It is observed that the positive end and negative end common-mode voltages are held at a constant value and the differential common-mode voltage is held at zero, barring the glitches due to dead times and device drops [73]. Zoomed versions of all these voltages are provided in Fig. 4.12(d)-4.12(f) for better viewing. The three phase load currents and circulating current are shown in Fig. 4.13(a). The currents appear as balanced and sinusoidal. The circulating is current non-zero, however much smaller than the load currents. Fourier spectra of the voltage $v_{AA'}$ are given for PWM of dual two-level inverter using carrier based and space vector based approaches in Fig. 4.13(b). It is seen that the spectra are nearly identical and devoid of low order harmonics.

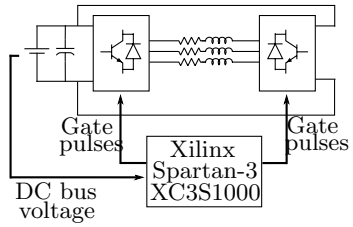


Figure 4.11: Diagram of the experimental setup for dual two-level inverter

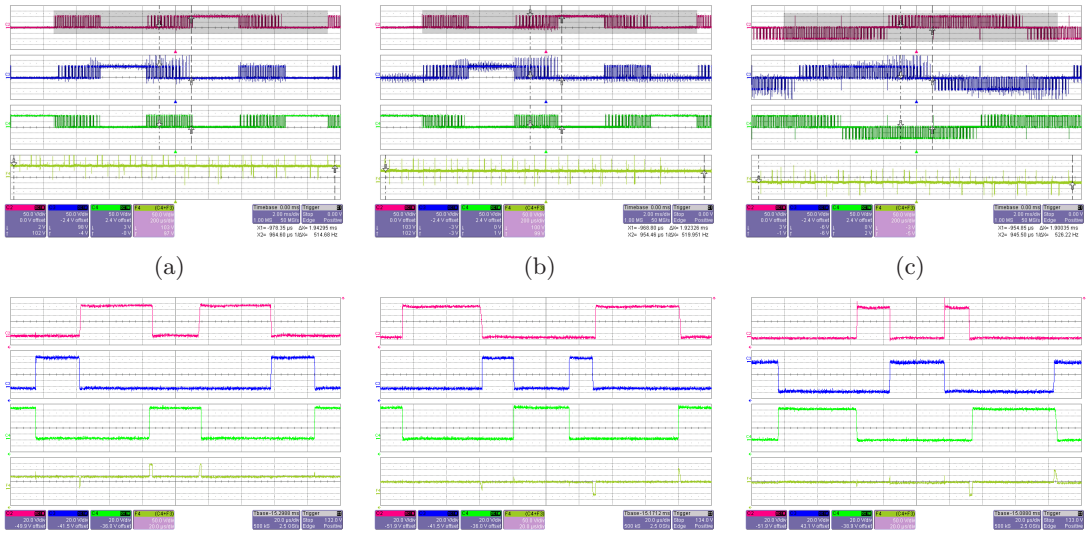
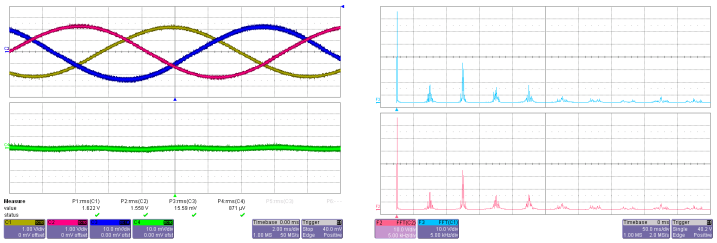


Figure 4.12: Experimental results for Dual two-level inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (b) Negative end pole voltages (top three graphs) and CMV (bottom graph) [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (d)Positive end pole voltages and CMV (zoomed) [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)] (e) Negative end pole voltages and CMV (zoomed) [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)] (f) Phase voltages and CMV across load (zoomed) [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)]



(a) (b)

Figure 4.13: Experimental results (Dual two-level inverter) (a) Three phase load currents (top graph) and circulating current (bottom graph) [X axis: 2 ms/div, Y axis: 1 A/div] (b) Fourier spectrum of voltage $v_{\mathrm{AA}'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph) [X axis: 5 kHz/div, Y axis: 10 V/div]

4.4 Conclusion

A carrier based implementation of a Space Vector PWM scheme for a dual converter is presented. The PWM scheme is aimed at eliminating common mode voltage across the load. The implementation technique doesn't involve any square root or trigonometric calculations. It derives the phase duty ratios directly from reference output phase modulation signals by simple logical operations. A simple technique to sequence the gate pulses is presented that fixes the alignment of output phase pulses for each switching period, but doesn't require any sector information. It is also possible to apply zero vectors centered sequence same as CSVPWM in order to get high quality output voltage waveforms. Although, the application of this sequence requires sector determination, which can be again done by simple logical operations.

Note: Parts of this chapter have been reproduced from IEEE publications [33, 74].

Chapter 5

Pulse Width Modulation schemes and a commutation technique for Open-end Winding Matrix converter drives to suppress Common Mode Voltage

Open-end winding drives present a solution to the issue of switching common mode voltage (CMV) generated by PWM converters. In the previous chapter, dual two level inverter open-end winding has been discussed along with a carrier based implementation of SVPWM for this drive to eliminate common mode voltage at the load. In this chapter, dual matrix converter open-end winding drive has been discussed. Matrix converters (MC) present the advantage of single stage ac to ac conversion, which means not having a dc link capacitor [75], [76]. In addition, they provide open loop unity power factor operation. Combining these advantages with the CMV elimination capability of a dual MC drive makes it an interesting topology to study.

Open-end winding dual MC drive was first proposed in [26], where a space vector based approach was discussed for power factor control and CMV elimination. In this

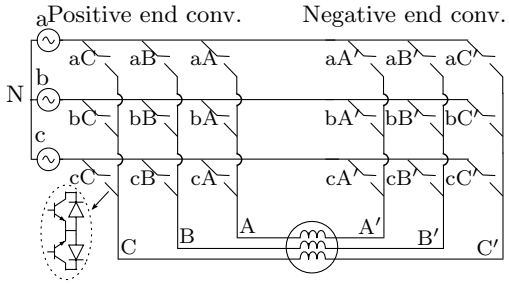


Figure 5.1: Dual matrix converter drive

chapter, carrier based implementation of SVPWM for dual MC drive for CMV elimination has been proposed. In addition, it is shown how the presented PWM method has similarities to that used for dual two level inverter drive in the previous chapter. Finally, a modified commutation algorithm has been proposed to suppress CMV spikes during commutation process and the circulating currents caused by them in dual MC drive.

5.1 Dual matrix converter and synchronous rotating vectors

A dual matrix converter system is shown in Fig.5.1. In the figure, one converter is named positive end converter and the other is named negative end converter. The space vector of positive end converter is defined in (5.1).

$$\mathbf{U} = v_{\mathrm{AN}} + v_{\mathrm{BN}} e^{j\frac{2\pi}{3}} + v_{\mathrm{BN}} e^{j\frac{-2\pi}{3}} \tag{5.1}$$

The voltages v_{AN}, v_{BN} and v_{CN} are voltages of positive end output terminals A, B and C respectively wrt N, the neutral point of the input three phase ac voltage.

A matrix converter can synthesize three phase ac voltage of adjustable frequency and amplitude from a three phase ac voltage source. The converter consists of nine switches (realized with eighteen IGBTs), forming three legs. Each of these three legs can be in three different positions, resulting in twenty-seven total switching states. Thus there are twenty-seven voltage space vectors for a matrix converter. Out of these twenty seven space vectors, three vectors are zero vectors and eighteen vectors are stationary

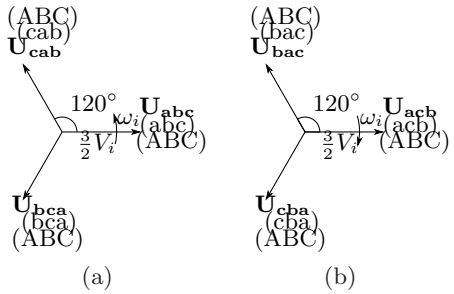


Figure 5.2: Synchronously rotating vectors for positive end matrix converter (a) CCW Vectors (b) CW Vectors

but of varying magnitude in time. These eighteen stationary vectors along with the three zero vectors are used in the indirect matrix converter modulation technique [77]. The remaining six vectors have a constant magnitude of $\frac{3}{2}V_i$ (V_i is input peak phase voltage) but keep rotating uniformly and are known as synchronously rotating space vectors. Three of these rotate in counter-clockwise direction with the input frequency ω_i and are called counter-clockwise (CCW) vectors. The remaining three rotate in clockwise direction with the input frequency ω_i and are known as clockwise (CW) space vectors. The CCW and CW vectors for the positive end matrix converter are shown in Fig. 5.2(a) and Fig. 5.2(b) respectively. As an example, the switching state (cab) implies that the load terminals A, B and C are connected to source terminals c, a and b respectively. This is done by turning ON switches cA, aB and bC and thus the vector $\mathbf{U_{cab}}$ is applied. Similarly, the other vectors are formed.

The CCW and CW vectors for the negative end matrix converter are shown in Fig. 5.3(a) and Fig. 5.3(b) respectively. These are opposite in direction to the CCW and CW vectors of the positive end matrix converter. The space vector of negative end converter is defined in (5.2).

$$\mathbf{W} = -(v_{\mathrm{A'N}} + v_{\mathrm{B'N}}e^{j\frac{2\pi}{3}} + v_{\mathrm{C'N}}e^{-j\frac{2\pi}{3}}) \tag{5.2}$$

The voltages $v_{\mathrm{A'N}}$, $v_{\mathrm{B'N}}$ and $v_{\mathrm{C'N}}$ are voltages of negative end output terminals A′, B′ and C′ respectively wrt N, the neutral point of the input three phase ac voltage in the case of dual matrix converter. When the load terminals A′, B′ and C′ of the load are connected to terminals c, a and b of the source respectively, vector $\mathbf{W_{cab}}$ is synthesized.

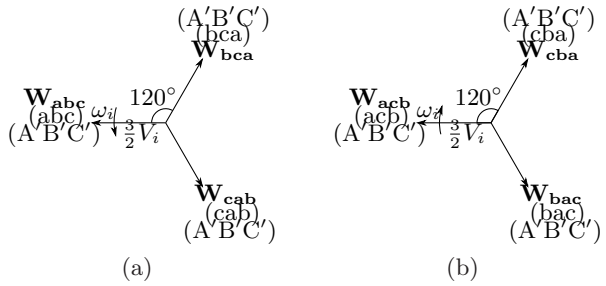


Figure 5.3: Synchronously rotating vectors for negative end matrix converter (a) CCW vectors (b) CW Vectors

The other vectors are formed likewise.

The common-mode voltage at the load terminals is defined by (5.3).

$$\begin{aligned} v_{\text{com,pos}} &= \frac{v_{\text{AN}} + v_{\text{BN}} + v_{\text{CN}}}{3} \\ v_{\text{com,neg}} &= \frac{v_{\text{A}'\text{N}} + v_{\text{B}'\text{N}} + v_{\text{C}'\text{N}}}{3} \end{aligned} \tag{5.3}$$

The differential common-mode voltage $v_{\text{com,diff}}$ defined in (5.4) is what affects circulating currents in open-end winding drives, as explained in [73]. The average of these common-mode voltages defined (5.5) is what affects EMI, as explained in [11].

$$v_{\text{com,diff}} = v_{\text{com,pos}} - v_{\text{com,neg}} \tag{5.4}$$

$$v_{\text{com,sum}} = \frac{v_{\text{com,pos}} + v_{\text{com,neg}}}{2} \tag{5.5}$$

For all of the CCW and CW synchronously rotating vectors (both positive and negative end), one phase of input is connected to only one phase of output at any given time. Hence, assuming that the input voltages are balanced and only synchronously rotating vectors are used for converter control, the common-mode voltages defined in (5.3) for both positive and negative ends will always be zero. Hence, both differential ($v_{\text{com,diff}}$) and average ($v_{\text{com,sum}}$) common-mode voltages are held at zero.

It should be noted that all the space vectors mentioned above have a non-zero magnitude. To create a zero vector (which is required in output voltage control), the same space vector is applied to both positive and negative converters (such as $\mathbf{U_1}$ and $\mathbf{W_1}$) to get zero voltage across the load. This is further discussed in next section.

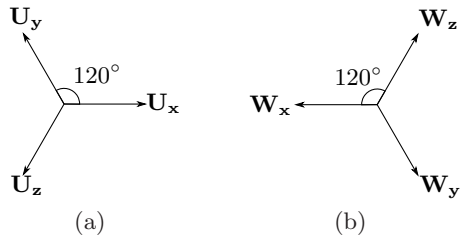


Figure 5.4: (a) Generic positive end space vectors (b) Generic negative end space vectors

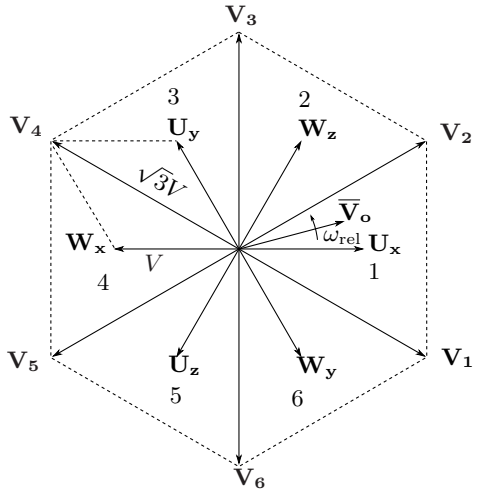


Figure 5.5: Space vectors for dual converter

5.2 Generalized analysis for CCW and CW space vectors

The space vectors for the positive end and the negative end converters (both dual CCW and CW) to generate zero common-mode voltage across the load are shown in Fig. 5.4(a) and Fig. 5.4(b) respectively. It should be noted that the vectors are not denoted with any rotation speed of ω_i either in CW or CCW direction and a single set of vectors is used to denote both CCw and CW vectors. The reason for this will be cleared in the subsequent discussion.

The vectors for the positive and the negative end converters can be combined to give six resultant vectors applied across the three phase load as shown in Fig. 5.5. For example, when space vectors $\mathbf{U_x}$ and $\mathbf{W_z}$ are simultaneously applied, the combined space vector $\mathbf{V_2}$ is obtained.

The instantaneous output voltage vector $\mathbf{V_o}$ of the dual converter is formed by the

sum of the positive end and negative end vectors **U** and **W**, as given in (5.6). It can be seen that this voltage vector is formed by the voltages across the load phases i.e. $v_{\mathrm{AA'}}$, $v_{\mathrm{BB'}}$ and $v_{\mathrm{CC'}}$.

$$\begin{aligned}\mathbf{V_o} = \mathbf{U} + \mathbf{W} &= (v_{\mathrm{AN}} + v_{\mathrm{BN}}e^{j\frac{2\pi}{3}} \\ &+ v_{\mathrm{CN}}e^{-j\frac{2\pi}{3}}) + (-(v_{\mathrm{A'N}} + v_{\mathrm{B'N}}e^{j\frac{2\pi}{3}} + v_{\mathrm{C'N}}e^{-j\frac{2\pi}{3}})) \\ &= v_{\mathrm{AA'}} + v_{\mathrm{BB'}}e^{j\frac{2\pi}{3}} + v_{\mathrm{CC'}}e^{-j\frac{2\pi}{3}} \end{aligned} \tag{5.6}$$

Thus, the reference output voltages across the load phases will be defined between positive and negative end terminals, i.e. $\overline{v}_{\mathrm{AA'}} = V_o\cos(\omega_o t)$, $\overline{v}_{\mathrm{BB'}} = V_o\cos(\omega_o t - \frac{2\pi}{3})$ and $\overline{v}_{\mathrm{CC'}} = V_o\cos(\omega_o t + \frac{2\pi}{3})$. The average output voltage vector $\overline{\mathbf{V_o}}$ (averaged over a switching period) is formed using these voltages. The voltage $\overline{v}_{AA'}$ indicates the voltage across output phase AA' averaged over a single switching period. The voltages $\overline{v}_{BB'}$ and $\overline{v}_{CC'}$ indicate the same for output phases BB' and CC'.

The absolute speed of rotation of the reference output voltage vector is equal to the desired output frequency ω_o.

$$\overline{\mathbf{V_o}} = \overline{v}_{AA'} + \overline{v}_{BB'}e^{j\frac{2\pi}{3}} + \overline{v}_{CC'}e^{-j\frac{2\pi}{3}} = \frac{3}{2}V_o e^{j\omega_o t} \tag{5.7}$$

However in Fig. 5.5, the frequency ω_{rel} of $\mathbf{V_o}$ is the relative frequency of $\mathbf{V_o}$ with respect to the dual converter space vectors ($\mathbf{V_1}$, $\mathbf{V_2}$ etc.). This frequency is defined for the CCW and CW vectors in (5.8) and (5.9) respectively.

$$\omega_{\mathrm{rel}} = \omega_o - \omega_i \quad \text{(for CCW vectors)} \tag{5.8}$$

$$\omega_{\mathrm{rel}} = \omega_o + \omega_i \quad \text{(for CW vectors)} \tag{5.9}$$

As a special case, it can be seen that if input frequency $\omega_i = 0$, then $\omega_{\mathrm{rel}} = \omega_o$. This corresponds to the case of dual two level inverter when considering CMV elimination, as discussed in previous chapter. Thus, for two-level vectors, the relative frequency ω_{rel} can be written as given in (5.10).

$$\omega_{\mathrm{rel}} = \omega_o \qquad \text{(for two-level vectors)} \tag{5.10}$$

Table 5.1: Space vectors for CCW, CW and two-level case

Generic vector	Two-level vector	CCW vector	CW vector
$\mathbf{U_x}$	$\mathbf{U_1}$	$\mathbf{U_{abc}}$	$\mathbf{U_{acb}}$
$\mathbf{U_y}$	$\mathbf{U_3}$	$\mathbf{U_{cab}}$	$\mathbf{U_{bac}}$
$\mathbf{U_z}$	$\mathbf{U_5}$	$\mathbf{U_{bca}}$	$\mathbf{U_{cba}}$
$\mathbf{W_x}$	$\mathbf{W_1}$	$\mathbf{W_{abc}}$	$\mathbf{W_{acb}}$
$\mathbf{W_y}$	$\mathbf{W_3}$	$\mathbf{W_{cab}}$	$\mathbf{W_{bac}}$
$\mathbf{W_z}$	$\mathbf{W_5}$	$\mathbf{W_{bca}}$	$\mathbf{W_{cba}}$

It can be seen that similar to three positive end CCW and CW vectors, there are three positive end two level vectors under consideration, if the modulation technique in previous chapter is used. This brings a similarity to the vectors being used for dual two level inverter and the rotating vectors being used for dual MC drive. The vectors shown in Fig. 5.4 can therefore also be extended to the space vectors of dual two level inverter drive. The space vectors $\mathbf{U_x}$, $\mathbf{W_x}$ and others in Fig. 5.4 can be related to the two-level inverter space vectors and matrix converter CCW and CW vectors using Table 5.1. It will be observed that this similarity further extends to the carrier based PWM techniques for dual MC and dual two level inverter drives. The discussion for carrier based PWM schemes will therefore also mention dual two level drives along with dual MC drives, from now on in this chapter.

The six resultant vectors $\mathbf{V_1}$ to $\mathbf{V_6}$ form six sectors labeled 1 to 6 and their magnitude is $\sqrt{3}$ times the magnitude V of individual converter space vectors, as shown in Fig. 5.5. The magnitude V of the individual converter space vectors is V_{dc} in case of two-level vectors and $\frac{3}{2}V_i$ in the case of CCW and CW vectors. These vectors, along with three zero vectors defined in (5.11), are used to synthesize the reference output voltage vector $\overline{\mathbf{V}}_\mathbf{o}$ (bar indicates average over a switching cycle).

$$\begin{aligned} \mathbf{V_{zero,1}} &= \mathbf{U_x} + \mathbf{W_x} = 0 \\ \mathbf{V_{zero,2}} &= \mathbf{U_y} + \mathbf{W_y} = 0 \\ \mathbf{V_{zero,3}} &= \mathbf{U_z} + \mathbf{W_z} = 0 \end{aligned} \tag{5.11}$$

The output vector could be in one of the six sectors and the two space vectors

bounding that sector are used to synthesize the output voltage vector on an average over a switching cycle. For example in Fig 5.5, the output voltage vector is in sector 1, so the space vectors V_1 and V_2 are to be used to synthesize it. Suppose, the duty ratios of $\mathbf{V_1}$, $\mathbf{V_2}$ and $\mathbf{V_{zero,1}}$ are d_1, d_2 and $d_{zero} = 1-(d_1+d_2)$ respectively. Then the output voltage vector is synthesized as in (5.12).

$$d_1\mathbf{V_1} + d_2\mathbf{V_2} + (1-d_1-d_2)\mathbf{V_{zero,1}} = \overline{\mathbf{V}}_\mathbf{o} \tag{5.12}$$

From (5.11), (5.12) and Fig. 5.5, (5.13) is obtained.

$$\mathbf{U_x} + d_1\mathbf{W_y} + d_2\mathbf{W_z} + (1-d_1-d_2)\mathbf{W_x} = \overline{\mathbf{V}}_\mathbf{o} \tag{5.13}$$

From (5.13), it is observed that the positive end converter vector $\mathbf{U_x}$ is ON for the entire switching period. The negative end converter vectors $\mathbf{W_y}$ and $\mathbf{W_z}$ are ON with duty ratios d_1 and d_2 respectively, while the vector $\mathbf{W_x}$ is ON for the remaining period, i.e. with a duty ratio of d_{zero} in a switching cycle.

It should be noted that in case of dual VSI, the proposed PWM scheme uses only one set of vectors out of $\mathbf{U_1}$, $\mathbf{U_3}$, $\mathbf{U_5}$, $\mathbf{W_1}$, $\mathbf{W_3}$, $\mathbf{W_5}$ and $\mathbf{U_2}$, $\mathbf{U_4}$, $\mathbf{U_6}$, $\mathbf{W_2}$, $\mathbf{W_4}$, $\mathbf{W_6}$. This will lead to an imbalance in conduction losses, since the lower IGBTs (connected to negative terminal N of dc bus) in positive and negative end VSI will have twice the conduction period of upper IGBTs. This can be mitigated by using the two sets in alternate output fundamental frequency periods. This will cause the common-mode voltages at positive and negative end to fluctuate between $\frac{V_{dc}}{3}$ and $\frac{2V_{dc}}{3}$, but at a frequency closer to output frequency rather than at the switching frequency and shouldn't have effect on ground currents mitigation.

The switching losses however will be fairly balanced, because during three sectors, the positive end converter is clamped (both in case of dual MC and dual VSI). The positive end converter is switching during the rest three sectors and by applying the gate pulses such that each leg (in case of dual VSI) or each bidirectional switch (in case of dual MC) switches four times, thus equalizing number of switching transitions in all legs (dual VSI) or bidirectional switches (dual MC). The negative end converter also has the same number of switching transitions. Thus, a dual VSI will have total of four transitions per leg. A single VSI using conventional SVPWM (using all eight vectors)

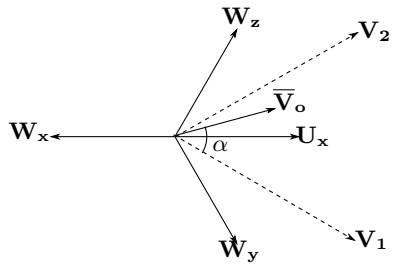


Figure 5.6: $\overline{\mathbf{V}}_\mathbf{o}$ in Sector 1

has only two transitions per leg in a switching period in all sectors. Thus, the dual VSI has twice the number of transitions compared to a single VSI. But as the voltage transfer ratio for dual converter is $\sqrt{3}$ times that of a single VSI we can operate dual VSI at $\frac{1}{\sqrt{3}}$ times the DC bus of the single VSI to achieve same maximum output voltage. Hence, switching losses will increase by $\frac{2}{\sqrt{3}}$ times for the dual converter.

5.3 Derivation of carrier based algorithm

The duty ratios d_1 and d_2 will now be derived in terms of the reference output phase voltages and input phase voltages. Suppose the output voltage vector is in sector 1, as shown in Fig.5.6.

For the CCW vectors, Table 5.1 and (5.13) give (5.14).

$$\mathbf{U_{abc}} + d_1\mathbf{W_{cab}} + d_2\mathbf{W_{bca}} + (1 - d_1 - d_2)\mathbf{W_{abc}} = \overline{\mathbf{V}}_\mathbf{o} \tag{5.14}$$

Using (5.1), (5.2), (5.7), (5.14) and imposing that

$$\overline{v}_{AA'} + \overline{v}_{BB'} + \overline{v}_{CC'} = 0$$

the duty ratios d_1 and d_2 can be derived in terms of input voltages and average output voltages as in (5.15).

$$\begin{aligned} d_1 &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{cN}} + (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ab}}}{3(v_{\mathrm{bN}}v_{\mathrm{ab}} - v_{\mathrm{cN}}v_{\mathrm{ca}})} \\ d_2 &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{bN}} + (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ca}}}{3(v_{\mathrm{bN}}v_{\mathrm{ab}} - v_{\mathrm{cN}}v_{\mathrm{ca}})} \end{aligned} \tag{5.15}$$

The quantity in the denominator is a constant and simplifies to $-\frac{3\times3}{2}V_i^2$. Also, $v_{\mathrm{aN}} = V_i\cos(\omega_i t)$ and $\overline{v}_{\mathrm{AA}'} = V_o\cos(\omega_o t)$ and so on. Using these expressions in (5.15) yields (5.16).

$$\begin{aligned} d_1 &= -\frac{V_o\cos((\omega_o-\omega_i)t-\frac{2\pi}{3})}{\frac{3}{2}V_i} \\ d_2 &= -\frac{V_o\cos((\omega_o-\omega_i)t+\frac{2\pi}{3})}{\frac{3}{2}V_i} \end{aligned} \tag{5.16}$$

After repeating the preceding computations for all six sectors for CCW and CW vectors and using the analysis done in previous chapter for two-level inverter vectors, Table 5.2 is obtained,

Table 5.2: Duty ratios d_1 and d_2 in all 6 sectors

Sector	d_1	d_2
1	$-m_y$	$-m_z$
2	m_x	m_y
3	$-m_z$	$-m_x$
4	m_y	m_z
5	$-m_x$	$-m_y$
6	m_z	m_x

where for CCW vectors, the phase modulation indexes (MIs) m_x, m_y and m_z are given by (5.17).

$$\begin{aligned} m_x &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{aN}} + (\overline{v}_{\mathrm{BB}'}-\overline{v}_{\mathrm{CC}'})v_{\mathrm{bc}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t)}{\frac{3}{2}V_i} \\ m_y &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{cN}} + (\overline{v}_{\mathrm{BB}'}-\overline{v}_{\mathrm{CC}'})v_{\mathrm{ab}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t-\frac{2\pi}{3})}{\frac{3}{2}V_i} \\ m_z &= \frac{3\overline{v}_{\mathrm{AA}'}v_{\mathrm{bN}} + (\overline{v}_{\mathrm{BB}'}-\overline{v}_{\mathrm{CC}'})v_{\mathrm{ca}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o-\omega_i)t+\frac{2\pi}{3})}{\frac{3}{2}V_i} \end{aligned} \tag{5.17}$$

For CW vectors, the MIs m_x, m_y and m_z are given by (5.18).

$$
\begin{aligned}
m_x &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{aN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{bc}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t)}{\frac{3}{2}V_i} \\
m_y &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{bN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ca}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t-\frac{2\pi}{3})}{\frac{3}{2}V_i} \\
m_z &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{cN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ab}}}{\frac{9}{2}V_i^2} = \frac{V_o\cos((\omega_o+\omega_i)t+\frac{2\pi}{3})}{\frac{3}{2}V_i}
\end{aligned}
\tag{5.18}
$$

For dual two-level inverter, the MIs m_x, m_y and m_z are given by (4.11) in previous chapter.

It is immediately observable that the duty ratios are a function of the phase modulation indexes (MIs) m_x, m_y and m_z, in all sectors.

For the dual two-level inverter, the MIs are equal to reference phase voltages ($\overline{v}_{\mathrm{AA'}}$, $\overline{v}_{\mathrm{BB'}}$, $\overline{v}_{\mathrm{CC'}}$) divided by the dc bus voltage (V_{dc}). The frequency of these MIs is equal to output frequency ω_o which is also equal to the relative frequency for two-level case defined in (5.10).

For the dual matrix converter, the amplitude of these modulation indexes is the ratio of peak phase output voltage V_o and 1.5 times of input peak phase voltage V_i. The frequency of the three CCW MIs in (5.17) is equal to relative frequency ω_{rel} defined in (5.8). Similarly, the frequency for the CW MIs in (5.18) is the relative frequency defined in (5.9).

With these observations a common algorithm can be used to find the duty ratios for different phases for both dual matrix converter and dual two-level inverter. Fig. 5.7 shows the three phase modulation indexes against time.

In the figure, the maximum and the minimum modulation indexes are highlighted in alternate sectors e.g. sector 1 and sector 2 (both bounded by vertical dotted lines) have the maximum MI and the minimum MI highlighted respectively. Following observations are made.

> In sector 1, the absolute value of phase modulation index m_x i.e. $|m_x|$ is maximum among absolute values $|m_x|$, $|m_y|$ and $|m_z|$. In sector 1, the phase modulation index m_x is termed as the absolute maximum MI and the other two MIs (m_y and m_z) are termed non-maximum MIs.

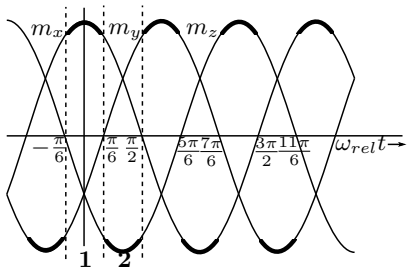


Figure 5.7: Modulation indexes' waveforms

Throughout the sector 1, the positive end converter is clamped and always applies one space vector i.e. $\mathbf{U_x}$ and the modulation index m_x is absolute maximum and positive, as seen in Fig. 5.7. In other sectors as well, the sign of the MI which is absolute maximum decides which converter is clamped (positive for positive end converter and negative for negative end converter). The space vector applied by the clamped converter is corresponding to MI which is absolute maximum., i.e. $\mathbf{U_x}$ in sector 1 and so on.

In sector 1, for the negative end converter, the duty ratios for space vectors corresponding to non-maximum MIs (m_y, m_z) i.e. $\mathbf{W_y}$ and $\mathbf{W_z}$ are equal to d_1 and d_2 respectively. As seen from Table 5.2, $d_1 = -m_y$ and $d_2 = -m_z$, i.e. the negative of non-maximum MIs. In Fig. 5.7, the non-maximum MIs m_y and m_z are negative in sector 1. Hence, $d_1 = |m_y|$ and $d_2 = |m_z|$. Thus, $\mathbf{W_y}$ and $\mathbf{W_z}$ are applied with duty ratios equal to absolute value of corresponding MIs.

In sector 1, the duty ratio of the negative end converter for space vector corresponding to absolute maximum MI (m_x) i.e. $\mathbf{W_x}$ is equal to $1 - (d_1 + d_2) = 1 + (m_y + m_z)$ i.e. $1 - m_x$. This can be rewritten as $1 - |m_x|$ since m_x is positive in sector 1 as seen in Fig. 5.7.

Similar analysis can be done for other sectors to derive the duty ratios for all the vectors. The information for all sectors is summarized in Table 5.3, which gives the duty ratios for all space vectors in terms of MIs m_x, m_y and m_z.

In the table, the duty ratio of space vector $\mathbf{U_x}$ is denoted by $d_{\mathbf{U_x}}$ and so on. $\mathbf{U_x}$, $\mathbf{U_y}$ and other space vectors can be identified using Table 5.1 for CCW, CW and two-level

Table 5.3: Duty ratios in terms of modulation indexes

Duty ratio	MI with maximum absolute value is positive			MI with maximum absolute value is negative		
	m_x	m_y	m_z	m_x	m_y	m_z
$d_{\mathbf{U_x}}$	1	0	0	1-$\lvert m_x\rvert$	$\lvert m_x\rvert$	$\lvert m_x\rvert$
$d_{\mathbf{U_y}}$	0	1	0	$\lvert m_y\rvert$	1-$\lvert m_y\rvert$	$\lvert m_y\rvert$
$d_{\mathbf{U_z}}$	0	0	1	$\lvert m_z\rvert$	$\lvert m_z\rvert$	1-$\lvert m_z\rvert$
$d_{\mathbf{W_x}}$	1-$\lvert m_x\rvert$	$\lvert m_x\rvert$	$\lvert m_x\rvert$	1	0	0
$d_{\mathbf{W_y}}$	$\lvert m_y\rvert$	1-$\lvert m_y\rvert$	$\lvert m_y\rvert$	0	1	0
$d_{\mathbf{W_z}}$	$\lvert m_z\rvert$	$\lvert m_z\rvert$	1-$\lvert m_z\rvert$	0	0	1

inverter vectors. Note that the MIs m_x, m_y and m_z have been defined in (5.17), (5.18) and (4.11) for CCW, CW and two-level inverter cases respectively.

A flow chart for calculating duty ratios using carrier based algorithm for open-end winding matrix converter drive is given in Fig. 5.8. As a preliminary step, the CCW and CW modulation indexes defined in (5.17) and (5.18) respectively are rewritten as shown in (5.19) and (5.20) respectively.

$$\begin{aligned}
m_x &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{aN}} + (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{bc}}}{\frac{9}{2}V_i^2} \\
&= [3k_{AA'}v_{\mathrm{aN}} + (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})v_{\mathrm{bc}}]\left(\frac{2}{9V_i}\right) \\
m_y &= \frac{3\overline{v}_{\mathrm{AA'}}v_{\mathrm{cN}} + (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}})v_{\mathrm{ab}}}{\frac{9}{2}V_i^2} \\
&= [3k_{\mathrm{AA'}}v_{\mathrm{cN}} + (k_{\mathrm{BB'}} - k_{\mathrm{CC'}})V_{ab}]\left(\frac{2}{9V_i}\right) \\
m_z &= -(m_x + m_y)
\end{aligned} \tag{5.19}$$

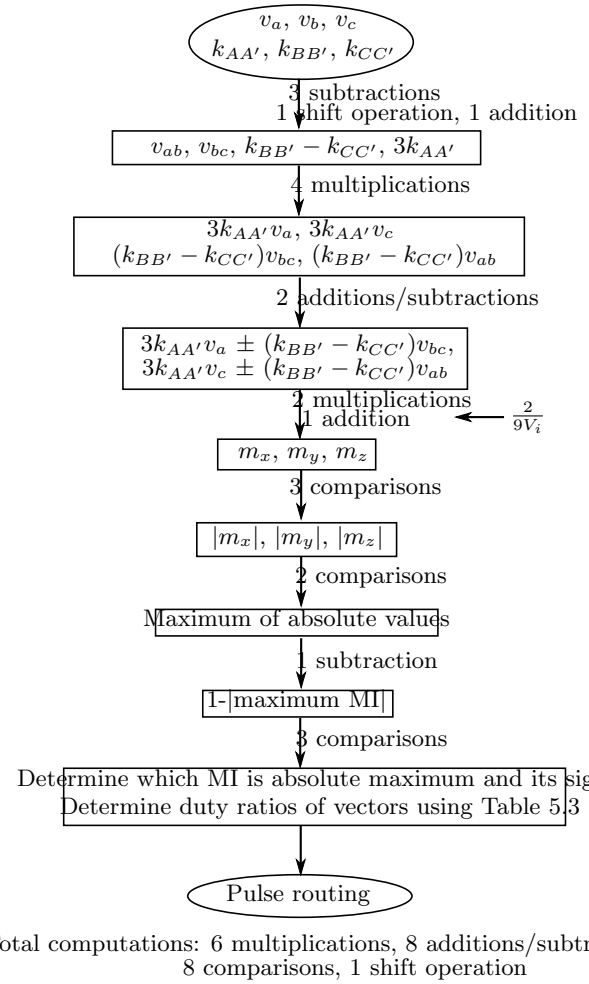


Figure 5.8: Carrier based implementation of matrix converter PWM using CCW and CW vectors

$$
\begin{aligned}
m_x &= \frac{3\overline{v}_{\mathrm{AA'}} v_{\mathrm{aN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}}) v_{\mathrm{bc}}}{\frac{9}{2} V_i^2} \\
&= [3k_{AA'} v_{\mathrm{aN}} - (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{bc}}] \left(\frac{2}{9V_i} \right) \\
m_z &= \frac{3\overline{v}_{\mathrm{AA'}} v_{\mathrm{cN}} - (\overline{v}_{\mathrm{BB'}} - \overline{v}_{\mathrm{CC'}}) v_{\mathrm{ab}}}{\frac{9}{2} V_i^2} \\
&= [3k_{\mathrm{AA'}} v_{\mathrm{cN}} - (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) V_{ab}] \left(\frac{2}{9V_i} \right) \\
m_y &= -(m_x + m_z)
\end{aligned} \tag{5.20}
$$

where

$$
k_{\mathrm{II'}} = \frac{\overline{v}_{\mathrm{II'}}}{V_i} \quad \mathrm{I} = \mathrm{A}, \mathrm{B}, \mathrm{C} \tag{5.21}
$$

Thus, the expression $[3k_{\mathrm{AA'}} v_a \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{bc}}] \left(\frac{2}{9V_i} \right)$ equals CCW MI m_x when $+$ sign is used in place of $\pm$ and equals CW MI m_x when $-$ sign is used in place of $\pm$. Also, expression $[3k_{\mathrm{AA'}} v_c \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) V_{ab}] \left(\frac{2}{9v_i} \right)$ equals CCW MI m_y when $+$ sign is used in place of $\pm$ and equals the CW MI m_z when $-$ sign is used in place of $\pm$.

It is assumed that $k_{AA'}$, $k_{BB'}$ and $k_{CC'}$ defined in (5.21), the input voltages v_{aN}, v_{bN} and v_{cN} and the quantity $\frac{2}{9V_i}$ are given at the beginning of the algorithm. The flowchart in Fig. 5.8 is explained as follows:

1. Compute $3k_{AA'}$ [*1 addition, 1 shift operation*], v_{ab} [*1 subtraction*], v_{bc} [*1 subtraction*] and $k_{\mathrm{BB'}} - k_{\mathrm{CC'}}$ [*1 subtraction*] . [Total: *3 subtractions, 1 addition, 1 shift operation*]

2. Compute $3k_{\mathrm{AA'}} v_{\mathrm{aN}}$, $3k_{\mathrm{AA'}} v_{\mathrm{cN}}$, $(k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{bc}}$ and $(k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{ab}}$, using quantities computed in the previous step. [Total: *4 multiplications*]

3. Compute $3k_{\mathrm{AA'}} v_{\mathrm{aN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{bc}}$ [*1 addition/subtraction*] and $3k_{\mathrm{AA'}} v_{\mathrm{cN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{ab}}$ [*1 addition/subtraction*]. The plus sign $\pm$ is for CCW vectors and the minus sign is for CW vectors. [Total: *2 subtractions/additions*]

4. Compute $(3k_{\mathrm{AA'}} v_{\mathrm{aN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{bc}}) \frac{2}{9V_i}$ [*1 multiplication*] and $(3k_{\mathrm{AA'}} v_{\mathrm{cN}} \pm (k_{\mathrm{BB'}} - k_{\mathrm{CC'}}) v_{\mathrm{ab}}) \frac{2}{9v_i}$ [*1 multiplication*]. This gives CCW MIs m_x and m_y or CW MIs m_x and m_z as explained in (5.19) and (5.20). Calculate $m_z = -(m_x + m_y)$

for CCW vectors or $m_y = -(m_x + m_z)$ for CW vectors [*1 addition*]. Now all the MIs required for duty ratio computation are obtained. [Total: *2 multiplications, 1 addition*]

5. Find $|m_x|$, $|m_y|$ and $|m_z|$. [Total: *3 comparisons*]

6. Compare $|m_x|$, $|m_y|$ and $|m_z|$ to identify maximum of these three. [Total: *2 comparisons*]

7. Find 1-|Maximum MI|. [Total: *1 subtraction*]

8. Determine which is the MI whose absolute value is maximum by comparing $|m_x|$, $|m_y|$ and $|m_z|$ with the absolute maximum MI found in step 6 [*2 comparisons*]. Then, find the sign of this absolute maximum MI [*1 comparison*]. [Total: *3 comparisons*]

9. Use the Table 5.3 to get the duty ratio of individual vectors and hence the individual switches using Table 5.1.

As seen from above explanation, the carrier based algorithm requires a total of *6 multiplications, 8 additions/subtractions, 8 comparisons and 1 shift operation*. These computations have also been shown denoted in Fig. 5.8.

As an example , let $|m_y|$ be maximum and m_y be positive. Then using Table 5.3, the positive end converter is clamped to space vector $\mathbf{U_y}$. The duty ratios of negative end converter's vectors $\mathbf{W_x}$, $\mathbf{W_y}$ and $\mathbf{W_z}$are $|m_x|$, $1 - |m_y|$ and m_z respectively. If the CCW vectors are being used, then using Table 5.1, the positive end matrix converter is clamped to $\mathbf{U_{cab}}$. The duty ratios of space vectors $\mathbf{W_{abc}}$, $\mathbf{W_{cab}}$ and $\mathbf{W_{bca}}$ are $|m_x|$, $1 - |m_y|$ and m_z respectively.

It should be noted that despite using space vector equations to arrive at the carrier based algorithm, the finalized carrier based algorithm mentioned above doesn't require any knowledge of space vectors.

The duty ratio waveforms for the three positive end vectors and the three negative end vectors derived using the carrier based algorithm are shown in Fig. 5.9. In the figure, $d_{\mathbf{U_x}}$ denotes the duty ratio waveform of positive end generalized vector $\mathbf{U_x}$. The other waveforms similarly denote the duty ratios of corresponding generalized vectors. The

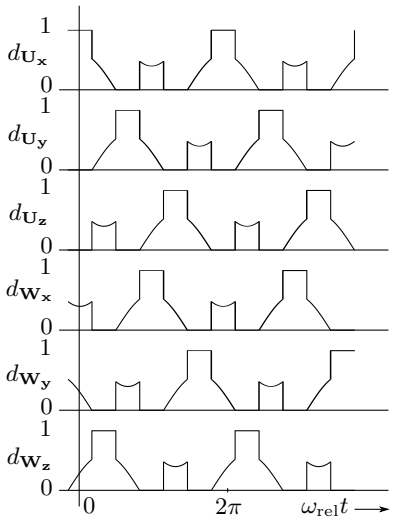


Figure 5.9: Duty ratio waveforms for all positive and negative end space vectors (and switches)

six waveforms are identical in shape and size but are displaced in time. The waveforms $d_{\mathbf{U_y}}$ and $d_{\mathbf{U_z}}$ lag $d_{\mathbf{U_x}}$ by 120° and 240° respectively. The negative end vector duty ratio waveform $d_{\mathbf{W_x}}$ is displaced by 180° wrt to corresponding positive end vector duty ratio waveform $d_{\mathbf{U_x}}$. The negative end vector duty ratio waveforms are also displaced by 120° wrt to each other. It should be noted that the frequency of all these duty ratio waveforms is the relative frequency ω_{rel}.

The waveforms in Fig. 5.9 are duty ratio signals for space vectors. However, in any of the three sets (two-level, CCW, CW), one leg (in case of dual two-level VSI) or one bidirectional switch (in case of dual matrix converter) is related to only one space vector. As an example (using $\mathbf{U_1}$, $\mathbf{U_3}$ and $\mathbf{U_5}$ for modulating positive end converter), in the dual two-level VSI, the leg connected to output phase A is turned ON (or connected to dc bus terminal P) only when vector $\mathbf{U_1}$ is applied and is turned OFF (connected to dc bus terminal N) when any other two vectors ($\mathbf{U_3}$, $\mathbf{U_5}$) are applied. Thus, in Fig. 5.9, the waveform $d_{\mathbf{U_x}}$ corresponds to the duty ratio waveform of $\mathbf{U_1}$ (using Table 5.1) with $\omega_{\mathrm{rel}} = \omega_o$ and hence is the duty ratio waveform for the inverter leg connected to output phase A. In the matrix converter case, when using CCW vectors, the switches aA, bB and cC are turned ON only when the CCW vector $\mathbf{U_{abc}}$ is applied and are OFF when any other CCW vector is applied. In Fig. 5.9, the waveform $\mathrm{d}_{\mathbf{U_x}}$ corresponds to the

Table 5.4: Duty ratios in each sector

Duty Ratio \ Sector	1	2	3	4	5	6
$d_{\mathbf{U_x}}$	1	d_1	0	d_{zero}	0	d_2
$d_{\mathbf{U_y}}$	0	d_2	1	d_1	0	d_{zero}
$d_{\mathbf{U_z}}$	0	d_{zero}	0	d_2	1	d_1
$d_{\mathbf{W_x}}$	d_{zero}	0	d_2	1	d_1	0
$d_{\mathbf{W_y}}$	d_1	0	d_{zero}	0	d_2	1
$d_{\mathbf{W_z}}$	d_2	1	d_1	0	d_{zero}	0

duty ratio waveform of $\mathbf{U_{abc}}$ (using table 5.1) with $\omega_{\text{rel}} = \omega_o - \omega_i$. Hence, this is the duty ratio waveform for switches aA, bB and cC when using CCW vectors. A similar explanation is applicable for CW vectors.

It must be noted, in case of simple carrier based operation of a VSI, modulation/duty ratio signals can be directly compared with a carrier to generate gating waveforms. In this case an additional simple combinatorial operation with the generated pulses is necessary to avoid over lapping of two active pulses in time. For example in a carrier/sampling cycle the pulses for aA ($\mathbf{U_{abc}}$) and cA ($\mathbf{U_{cab}}$) must not overlap in time.

5.4 Comparison between carrier based and space vector approaches for PWM of dual matrix and two-level VSI

An algorithm for the space vector based approach for PWM of open-end winding matrix converter drive using both CCW and CW vectors is shown in Fig. 5.10. It is assumed that $k_{AA'}$, $k_{BB'}$ and $k_{CC'}$ defined in (5.21), the input voltages v_a, v_b and v_c are given at the starting of the computation.

The flowchart for space vector based approach in Fig. 5.10 is explained below:

1. The input phase voltages v_{aN}, v_{bN} and v_{cN} are converted to $\alpha\beta$ axis, using $\text{v}_\alpha = \text{v}_{\text{aN}}$ and $\text{v}_\beta = \frac{\text{v}_{\text{bc}}}{\sqrt{3}}$ [*1 subtraction, 1 multiplication*]. Input voltage phase θ_i is calculated as $\tan^{-1}\frac{v_\beta}{v_\alpha}$ [*1 division, 1* $\tan^{-1}$]. [*Total: 1 multiplication, 1 subtraction, 1 division, 1* $\tan^{-1}$]

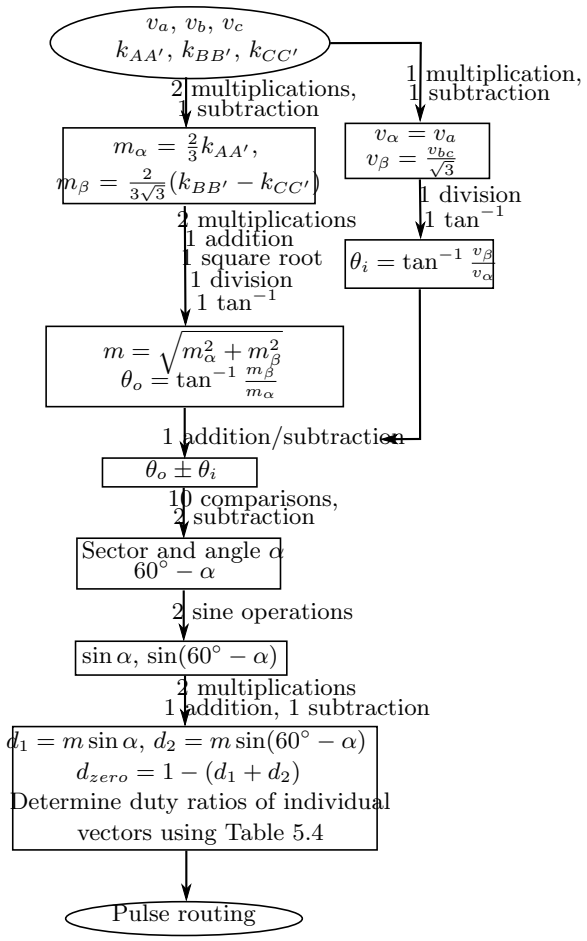


Figure 5.10: Space vector based PWM of dual matrix converter using CCW and CW vectors

2. $m_\alpha = \frac{2}{3}k_{AA'}$ [*1 multiplication*] and $m_\beta = \frac{2}{3\sqrt{3}}(k_{BB'} - k_{CC'})$ [*1 subtraction, 1 multiplication*] are calculated. [*Total: 1 subtraction, 2 multiplications*]

3. The output modulation index $m = \sqrt{m_\alpha^2 + m_\beta^2}$ is computed [*2 multiplications* (for computing m_α^2 and m_β^2), *1 addition, 1 square root*]. Output voltage angle is computed using $\theta_o = \tan^{-1}\frac{m_\beta}{m_\alpha}$ [*1 division, 1* $\tan^{-1}$]. [*Total: 2 multiplications, 1 addition, 1 square root operation, 1 division, 1* $\tan^{-1}$]

4. $\theta_i \pm \theta_o$ is computed (either added for CW vectors or subtracted for CCW vectors). [*1 subtraction/addition*]

5. To determine the sector, $\theta_o \pm \theta_i$ is compared with the upper and lower angular bounds of each sector [*10 comparisons in worst case*]. Then, angle α is determined by subtracting appropriate multiple of $\frac{\pi}{3}$ from θ_o [*1 subtraction*]. Then $(60^\circ - \alpha)$ is computed [*1 subtraction*]. [*Total: 10 comparisons, 2 subtractions*]

6. Compute $\sin\alpha$ and $\sin(60^\circ - \alpha)$. [*2* sin *operations*]

7. Compute duty ratios $d_1 = m\sin(\alpha)$ and $d_2 = m\sin(60^\circ - \alpha)$ [*2 multiplications*]. Calculate $d_{zero} = 1-(d_1+d_2)$ [*1 addition, 1subtraction*]. [*Total: 2 multiplications, 1 addition, 1 subtraction*]

8. With sector, d_1, d_2 and d_{zero} known, Table 5.4 and Table 5.1 are used to determine which space vector is applied with what duty ratio. This part is common with the carrier based algorithm and takes the same computations (a case or if else statement). Hence, it is not be considered in the comparison.

Based on above discussion, the total computations needed for the space vector based implementation of PWM for dual matrix converter using CCW and CW vectors are *1 square root, 2* $\tan^{-1}$*, 2* sin*, 2 divisions, 7 multiplications, 8 additions/subtractions, 10 comparisons*. The flowchart in Fig. 5.8 for carrier based approach for dual matrix converter PWM using CCW or CW vectors is explained in Section IV and the various calculations required for the steps have been explained before as well as shown in the flowchart.

It is observed from the above discussion and the flowcharts that the carrier based approach takes fewer computations than the space vector approach for the PWM control

Table 5.5: Computations required for carrier based and Space vector based approaches for PWM of dual matrix converter

Computation	Carrier based approach	Space vector based approach
Comparison	8	10
Shift operation	1	0
Addition/Subtraction	8	8
Multiplication	6	7
Division	0	2
Sine	0	2
$\tan^{-1}$	0	2
Square root	0	1

Table 5.6: Resource requirements of carrier based and Space vector based approaches for PWM of dual matrix converter

Resource used	Carrier based approach	Space vector approach
No. of slice flip-flops	71 (1%)	2436 (26%)
No. of 4 input LUTs	461 (4%)	2670 (28%)
No. of Logic slices	271 (5%)	1590 (34%)
No. of MULT18X18SIOs	6 (30%)	7 (35%)

of dual matrix converter. The computations required are summarized seen in Table 5.5.

The Verilog code for both the methods was developed and implemented using Xilinx ISE Editor to check the resources. The FPGA used was Xilinx Spartan 3 XC3S500E. The resource requirements of both techniques is given in Table 5.6, which shows that the resource requirements are much more in space vector based approach. The CORDIC IP core from Xilinx was used to do the square root and all trigonometric operations needed by the space vector approach.

The latencies of Verilog code for carrier based and space vector based approaches for open-end winding matrix converter drive are shown in Fig. 5.11(a) and Fig. 5.11(b) respectively. In Fig. 5.11(a), the inputs $k_{AA'}$, $k_{BB'}$ and $k_{CC'}$ (denoted k_AApr, k_BBpr and k_CCpr respectively in the figure) change at the beginning of the shaded region (marked by an arrow). The output $d_{\mathbf{U_z}}$ i.e., the duty ratio of vector $\mathbf{U_z}$ (top signal

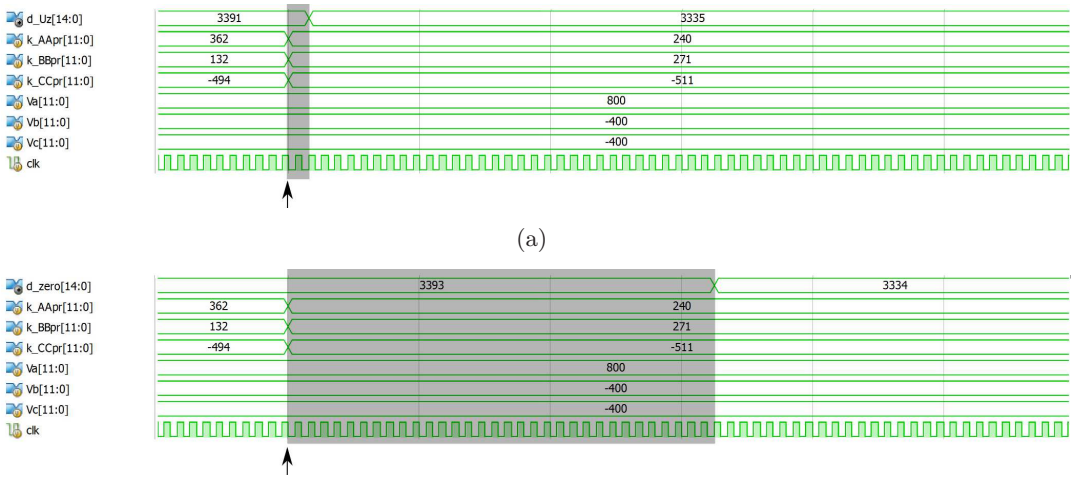


Figure 5.11: Latency in Verilog code for PWM of dual matrix converter (a) Carrier based approach (b) Space vector based approach

denoted as d_Uz in the figure) changes after two clock cycles (shown in the shaded area). In Fig. 5.11(b), the inputs $k_{AA'}$, $k_{BB'}$ and $k_{CC'}$ (denoted k_AApr k_BBpr and k_CCpr respectively in the figure) change at the beginning of the shaded region. The output d_{zero} i.e., the duty ratio of the zero vector (top signal denoted as dz in the figure) in the current sector changes after thirty three clock cycles (shown in the shaded area). Thus, latency of the carrier based algorithm as seen in Fig. 5.8 is two clock cycles. The latency of the space vector based approach as seen in Fig. 5.10 has a latency of thirty three clock cycles, which is much more than that of carrier based approach.

The carrier based and space vector based approaches for PWM of open-end winding two-level inverter drive are special cases of corresponding approaches for PWM of open-end winding matrix converter drive. So, the carrier based and space vector based approaches for PWM of two-level inverter compare similarly.

5.5 Alternative method to implement carrier based SVPWM for dual Matrix Converter drive

In this section, an alternative method to implement carrier based SVPWM for dual MC is discussed. The strategy discussed in section 5.3 and chapter 4 processes the MIs to directly generate the duty ratios for all vectors. However, the dual converter vectors can be mapped to the space vectors of a single two level VSI. Then, the carrier based SVPWM of single two level VSI can be used to generate the pulses. This strategy has been presented in [24] for dual two level inverter drive and will be extended to the dual MC drive in this section.

As discussed above, the dual MC vectors and the relative frequency MIs give a framework similar to a dual two level VSI proposed in [24]. In this system, the dc link voltage of a dual VSI would be equal to $1.5V_i$ and the MIs m_x, m_y and m_z can be used to form the output voltage vector $\overline{\mathbf{V}}_\mathbf{o}$ rotating at ω_{rel}, written in (5.22).

$$\overline{\mathbf{V}}_\mathbf{o} = (m_x + m_y e^{j\frac{2\pi}{3}} + m_y e^{-j\frac{2\pi}{3}})1.5V_i \tag{5.22}$$

The space vector system in Fig. 5.5 is further transformed to that of an imaginary single two level VSI with dc link voltage $1.5V_i$. This transformation is shown in Fig. 5.12. The vectors $\mathbf{V_1}$-$\mathbf{V_6}$ are transformed to vectors $\mathbf{X_1}$ to $\mathbf{X_6}$ and the output voltage vector $\overline{\mathbf{V}}_\mathbf{o}$ is transformed to $\overline{\mathbf{V}}_\mathbf{o1}$. The transformation is done by shifting each vector 30° counter clockwise and multiplying by $\frac{1}{\sqrt{3}}$. The transformation matrix for m_x, m_y and m_z to m_{x1}, m_{y1} and m_{z1} to this system is given by (5.23).

$$\begin{bmatrix} m_{x1} \\ m_{y1} \\ m_{z1} \end{bmatrix} = M_3 M_2 M_1 \begin{bmatrix} m_x \\ m_y \\ m_z \end{bmatrix} = M \times \begin{bmatrix} m_x \\ m_y \\ m_z \end{bmatrix} \tag{5.23}$$

where

$$M_3 = \underbrace{\begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} \end{bmatrix}}_{\alpha\beta \text{ to abc}} \quad M_2 = \underbrace{\frac{1}{\sqrt{3}} \begin{bmatrix} \cos 30^\circ & -\sin 30^\circ \\ \sin 30^\circ & \cos 30^\circ \end{bmatrix}}_{\text{Rotation by } 30^\circ \text{ and scaling by } \frac{1}{\sqrt{3}}}$$

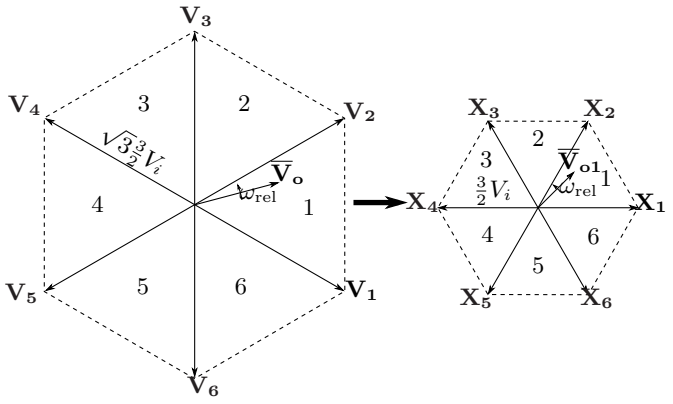


Figure 5.12: Transformation of dual MC vector system to that of single two level VSI

$$M_1 = \underbrace{\begin{bmatrix} 1 & -\frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{\text{abc to } \alpha\beta} M = \frac{1}{3}\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}$$

Now, m_{x1}, m_{y1} and m_{z1} are three reference output MIs in a two level VSI with active vectors $\mathbf{X_1}$ to $\mathbf{X_6}$. Thus, the carrier based method for SVPWM of a single two level VSI, as described in [71] can be used to obtain the gating pulses for $\mathbf{X_1}$ to $\mathbf{X_6}$. The carrier based method of a single two level VSI involves finding duty ratios d_{x1}, d_{y1} and d_{z1} given in (5.24) and comparing them to a carrier to obtain the gating pulses.

$$d_{k1} = 0.5 + 0.5\text{mid}(m_{x1}, m_{y1}, m_{z1}) + m_{k1} \ \text{(k = x, y, z)} \tag{5.24}$$

The pulses obtained for $\mathbf{X_1}$ to $\mathbf{X_6}$ are also the pulses for corresponding dual MC vectors $\mathbf{V_1}$ to $\mathbf{V_6}$, as described in table 5.7. Thus, the pulses for all active vectors $\mathbf{V_1}$ to $\mathbf{V_6}$ are obtained.

The carrier based SVPWM of two level VSI gives the pulses for zero vectors apart from those of active vectors as discussed in previous paragraph. The pulses for zero vector correspond to the three zero vectors in (5.11). To identify which zero vector is to be applied, it is determined which of the three MIs m_{x1}, m_{y1} and m_{z1} is mid and then table 5.8 is used. Thus, the gating pulses for the active and zero vectors of the dual MC are determined.

The proposed algorithm is outlined in following steps. The starting quantities given

are reference output voltages $\overline{v}_{AA'}$, $\overline{v}_{BB'}$ and $\overline{v}_{CC'}$, input phase voltages v_{aN}, v_{bN}, v_{cN} and the inverse of input voltage amplitude $\frac{1}{V_i}$.

1. Compute the MIs m_x, m_y and m_z as given in (5.17) or (5.18) depending on calculation for CCW or CW vectors.

2. Compute the transformed MIs m_{x1}, m_{y1} and m_{z1} using (5.23).

3. Find the mid value of m_{x1}, m_{y1} and m_{z1}. Also, determine which of these three MIs equals the mid value.

4. Compute the duty ratios d_{x1}, d_{y1} and d_{z1} as per (5.24) and compare to a carrier to obtain the pulses for $\mathbf{X_1}$ to $\mathbf{X_6}$ and zero vector.

5. Use table 5.7 to obtain the pulses for dual MC vector $\mathbf{V_1}$ to $\mathbf{V_6}$ from those of $\mathbf{X_1}$ to $\mathbf{X_6}$.

6. Use the information in step 3 and table 5.8 to map the zero vector pulse obtained in step 4 to zero vectors of dual MC.

The general space vector approach would require sector identification, which involves finding the angle of the input and output voltage vectors, leading to operations like division and $\tan^{-1}$. In contrast to this, no trigonometric or square root operation is needed in any of the steps of the algorithm described above. The gating pulses are obtained by some multiplications of given reference voltages and input voltage amplitude inverse, followed by some comparisons and logic operations.

Table 5.7: Pulse mapping for single VSI active vector to dual MC active vector

Single VSI active vector used for reference	Dual MC active vector to be mapped
$\mathbf{X_1}$	$\mathbf{V_1}$
$\mathbf{X_2}$	$\mathbf{V_2}$
$\mathbf{X_3}$	$\mathbf{V_3}$
$\mathbf{X_4}$	$\mathbf{V_4}$
$\mathbf{X_5}$	$\mathbf{V_5}$
$\mathbf{X_6}$	$\mathbf{V_6}$

Table 5.8: Dual MC zero vector to be used based on which MI is mid

Mid MI	Zero vector of dual MC
m_{x1}	$\mathbf{V_{zero3}}$
m_{y1}	$\mathbf{V_{zero1}}$
m_{z1}	$\mathbf{V_{zero2}}$

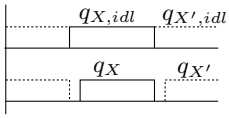


Figure 5.13: Illustration of dead band between the gate pulses of switches is a phase leg of a two level inverter

5.6 Overview of four step commutation and types of commutation

In a practical power converter with real world power devices, any PWM strategy cannot be applied as it is. For example, in a two level inverter, if conventional SVPWM or even sine-triangle PWM is used, the gate pulse of upper and lower switch in an inverter leg are complimentary, i.e. one of them turns ON at the same instant the other one turns OFF in the ideal case. However, due to finite rise and fall times of voltage and current through a power electronic switch, ideal pulses transitioning at the same instant could cause short circuit of the dc bus if one switch hasn't fully turned OFF while the other gets turned ON. To prevent this, a dead band between the two ideal gate pulses is introduced. This is demonstrated in Fig. 5.13, where $q_{X,idl}$ and $q_{X',idl}$ are ideal gate pulses, while q_X and $q_{X'}$ are final gate pulses with a dead band between them. This dead band satisfies two criteria:

1. Prevent short circuit of the input voltage (dc link voltage for two level inverter)

2. Prevent interruption of output current (which is assumed inductive)

For a matrix converter, the first criterion means that no two input phase voltages should be short circuited. The second criterion remains the same. In a matrix converter, bidirectional switches are used. In order to satisfy the above two criteria, a different process needs to be employed instead of a simple dead band like the one in Fig. 5.13.

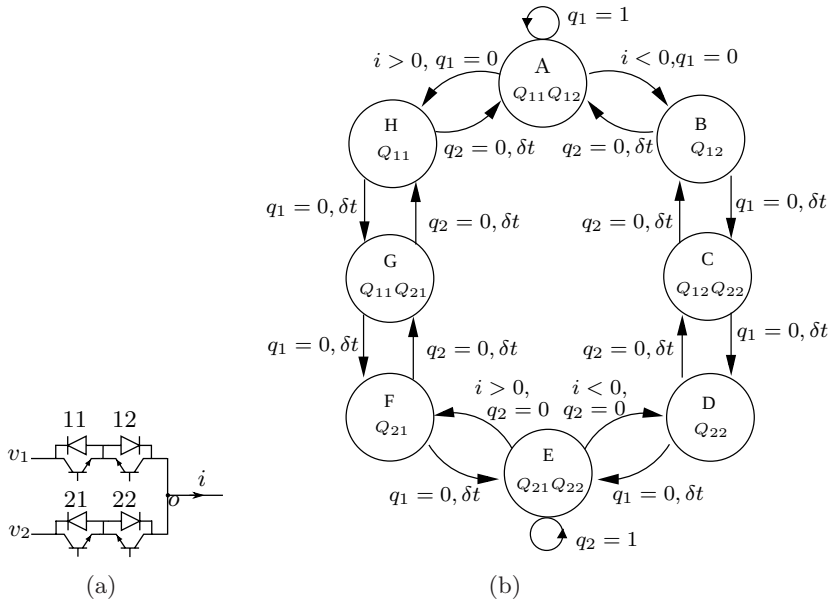


Figure 5.14: Four step commutation (a) Two bidirectional switches undergoing commutation (b) Conventional four-step commutation state machine

Conventional four-step commutation satisfies these two criteria. The state machine of conventional four-step commutation is presented in Fig. 5.14(b). This state machine controls the switching of the individual IGBTs of two bidirectional switches shown in Fig. 5.14(a). In Fig. 5.14(a), v_1 and v_2 are the input voltages, while i is the load current, which is considered positive when flowing in the direction shown in the figure. The states in Fig. 5.14(b) are denoted by alphabets A through H.

The quantities Q_{11}, Q_{12}, Q_{21} and Q_{22} when mentioned in the states in Fig. 5.14(b), denote that IGBTs 11, 12, 21 and 22 respectively are ON, in Fig. 5.14(a). When these quantities are not mentioned, the corresponding IGBT is OFF. For example, in state A in Fig. 5.14(b), Q_{11} and Q_{12} are mentioned which mean that IGBTs 11 and 12 in Fig. 5.14(a) are ON, while other IGBTs, i.e. 21 and 22 are OFF. The quantity δt represents one commutation step time in seconds and q_1 and q_2 are ideal pulses for the bidirectional switches in Fig. 5.14(a).

The conventional four-step commutation algorithm is described below. In the following discussion, the bidirectional switch to be turned ON is called the incoming switch, while the bidirectional switch to be turned OFF is called the outgoing switch.

Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch

Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt

Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt

Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt

In the above description, the active and passive IGBTs are decided by the load current direction.

Now suppose that in Fig. 5.14(a), $v_1 > v_2$ and $i > 0$. Then, the four step commutation process when output voltage is switching from v_1 to v_2 is described below:

Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch. In this case, the passive IGBT of outgoing switch is 12 and this is turned OFF.

Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt. In this case, the active IGBT of incoming switch is 21 and therefore, this IGBT is turned ON. Since $v_1 > v_2$, the diode of IGBT 22 is reverse biased. Thus, the current i keeps flowing through the first bidirectional switch and output voltage still equals v_1.

Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. In this case, the active IGBT of the outgoing switch is 11 and is therefore turned OFF. Due to this, the current i_o doesn't have a path to flow through first bidirectional switch and therefore is force commutated to flow through IGBT 21 and diode of IGBT 22. The output voltage is now equal to v_2.

Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt. The passive IGBT of outgoing switch is 22 and is turned ON.

In the above example, the load current was forced to commutate from v_1 to v_2 when the outgoing switch IGBT was turned OFF. This type of commutation is called forced commutation. The example case for forced commutation discussed above is illustrated in Fig. 5.15(a).

Now suppose that $v_1 < v_2$ and $i > 0$. Then, the four step commutation process when output voltage is switching from v_1 to v_2 is described below:

Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch. In this case, the passive IGBT of outgoing switch is 12 and this is turned OFF.

Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt. In this case, the active IGBT of incoming switch is 21 and therefore, this IGBT is turned ON. Since $v_1 < v_2$, the diode of IGBT 12 is reverse biased and cannot conduct. The current naturally commutates to the second bidirectional switch and starts to flow through IGBT 21 and the anti-parallel diode of IGBT 22. The output voltage thus becomes equal to v_2.

Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. In this case, the active IGBT of the outgoing switch is 11 and is therefore turned OFF.

Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt. The passive IGBT of outgoing switch is 22 and is turned ON.

In the above example case, the current naturally commutates to the second bidirectional switch when the incoming switch IGBT is turned ON. This type of commutation is called natural commutation. The example case for natural commutation discussed above is illustrated in Fig. 5.15(b). It is concluded from this discussion, that natural commutation occurs at the second step, while forced commutation occurs at the third step of the four step process.

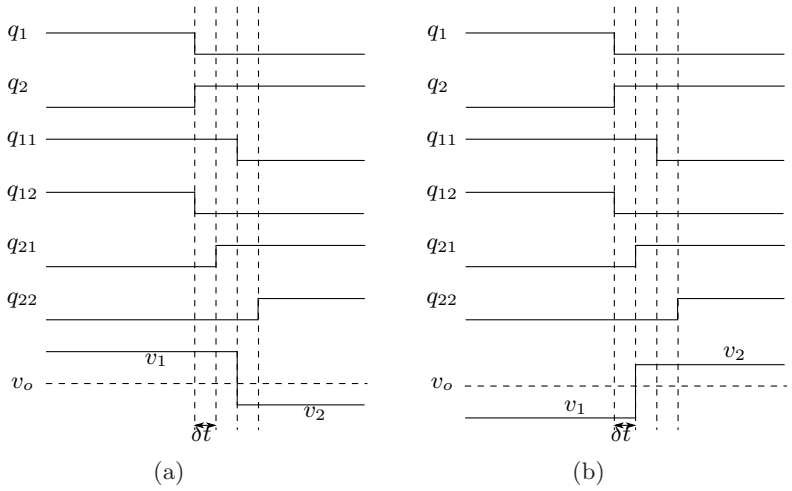


Figure 5.15: Commutation examples (a) Forced commutation (b) Natural commutation

5.7 Single phase analysis for effect commutation on output voltage

Consider a three phase to single phase matrix converter, as shown in Fig. 5.16(a). It consists of three bidirectional switches, each connecting one of the three input phases to the output terminal o. The three input phase voltages are labeled as v_{max}, v_{mid} and v_{min}, to denote that the voltages at the phases are maximum, middle and minimum of the three phases respectively. The direction of the output current i is assumed positive in the direction shown. The output voltage switches between one of these three input voltages at any given time and it is assumed that that all three input voltages are applied twice every switching period. The ideal pulses and the output voltage v_o at point o are shown in Fig. 5.16(b), assuming that the current $i > 0$. As discussed before, δt is the time of one step of the four step commutation process. It is observed in Fig. 5.16(b) that there are three natural commutations (where the voltage v_o jumps to a higher value) and three forced commutations (where the voltage v_o jumps to a lower value). As discussed before, the natural commutations occur δt after the ideal pulse transition while forced commutations occur $2\delta t$ after ideal pulse transition.

If the output voltage v_o matches the ideal switching pulses q_1, q_2 and q_3 exactly i.e. the voltage transitions match the idea pulses, then average value of v_o over a switching

period T_s is equal to the desired output voltage. However, it is seen that the voltage transitions are not occurring at the same instant as the ideal pulses. Now at each voltage transition, when an outgoing voltage is delayed, the average value of v_o over the switching period changes due to it. On the other side, the delay in application of incoming voltage at the same transition causes a net change in average value of the output voltage v_o over the switching period. This is illustrated for the first transition in Fig. 5.16(b). Here, the voltage v_{max} is applied for extra period of $2\delta t$, while the period of application of voltage v_{mid} is reduced by $2\delta t$. Thus, the net change in average value of output voltage from the desired ideal voltage, due to this transition is given in (5.25) as follows.

$$\Delta v_{trans} = \frac{2\delta t}{T_s}(v_{max} - v_{mid}) \tag{5.25}$$

In a similar manner, the net change in the average output voltage due to all transitions in the output voltage V_o over a switching period is calculated as follows.

$$\begin{aligned} \Delta v_{Ts} =& \frac{\delta t}{T_s}[2(v_{max} - v_{mid}) + 2(v_{mid} - v_{min}) + (v_{min} - v_{max}) + 2(v_{max} - v_{min}) + \\ & (v_{min} - v_{mid}) + (v_{mid} - v_{max})] \\ \implies \Delta v_{Ts} =& \frac{2\delta t}{T_s}(v_{max} - v_{min}) = \frac{2\delta t}{T_s} v_{ll,max} \quad (i > 0) \end{aligned} \tag{5.26}$$

It is observed from (5.26) that the net change in the average value of output voltage depends only on the commutation time step δt, switching period T_s and the maximum input line-line voltage $v_{ll,max}$ for the switching period. This analysis was done for a given sequence of ideal gate pulses q_1, q_2 and q_3. Assuming that the pattern of pulses applied remains symmetric, there are a total of six pulse sequences possible. It can be verified that for all the remaining five pulse sequences, the net change in average output voltage is the same as in (5.26) when output current $i > 0$. For $i < 0$, it is found that for all six pulse sequences, the net change in average output voltage is negative of the value in (5.26).

Thus, it is observed that the net change in average output voltage is somewhat like a square wave, where the amplitude of the 'square wave' is decided by the maximum input line-line voltage, while the fundamental frequency of the 'square wave' is decided

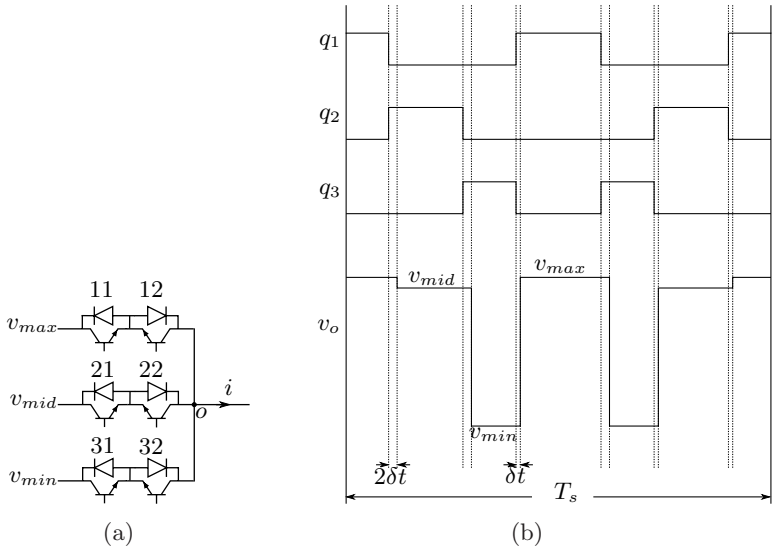


Figure 5.16: (a) Three phase to single phase matrix converter (b) Ideal gate pulses and output voltage for three phase to single phase matrix converter ($i > 0$)

by the output current frequency. Numerically, it is written as follows.

$$\Delta v_{Ts} = sgn(i)\frac{2\delta t}{T_s}v_{ll,max} \tag{5.27}$$

The discussion in this section essentially gives an idea of the low frequency component appearing in the output voltage due to commutation process. It should be noted that this voltage also has a high frequency component, since commutation causes this voltage to appear as pulses which have the average value like the one shown in Fig. 5.17. The effect of commutation process in a three phase to three phase matrix converter is discussed in the next section.

5.8 Effect of Commutation process on Common-Mode Voltage

It has been discussed in section 5.1 that the common-mode voltage can be kept at zero on both ends provided only synchronously rotating vectors are used for PWM.

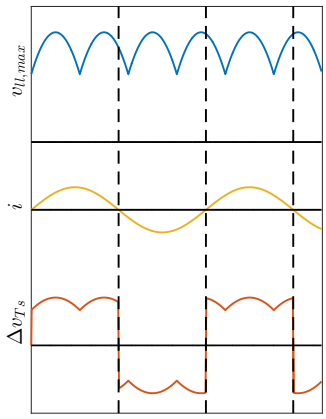


Figure 5.17: Maximum input line-line voltage (top), output current (middle) and change in average output voltage due to commutation (bottom) in a three phase to single phase matrix converter

Table 5.9: Input voltage and load current polarities for example case 1

Parameter	v_{ab}	v_{bc}	v_{ca}	$i_{AA'}$	$i_{BB'}$	$i_{CC'}$
Sign	+	−	+	+	−	−

Table 5.10: Incoming and outgoing positive end matrix converter switches for example case 1

Outgoing switch	aA	bB	cC
Incoming switch	cA	aB	bC

This happens since each input phase is connected to only one output phase, but this condition can be violated during commutation. For example, consider the case when the positive end converter in Fig. 5.1 is being switched from $\mathbf{U_{abc}}$ to $\mathbf{U_{cab}}$ and the current directions and voltage polarities are as given in Table 5.9. The incoming (turning ON) and outgoing (turning OFF) bidirectional switches for each output phase of the positive end converter are given in Table 5.10. The aforementioned four-step commutation algorithm is now applied to this example case, as described below for all three legs of the positive end matrix converter:

Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of

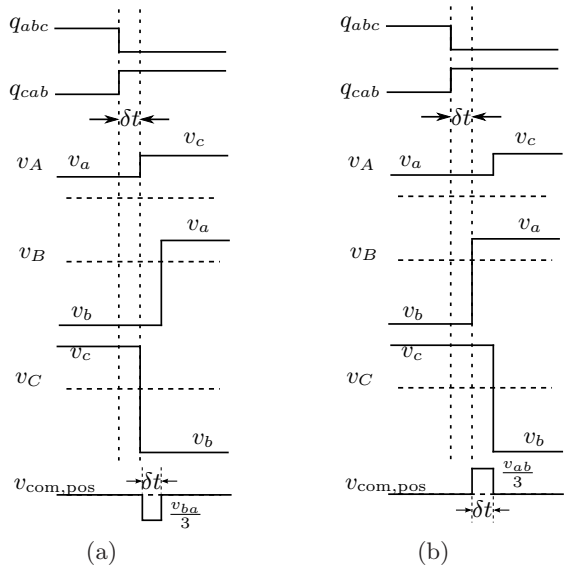


Figure 5.18: Conventional commutation examples (a) Case 1 (b) Case 2

the outgoing bidirectional switch. Based on Table 5.9 and Table 5.10, for output phase A, the IGBT $aA2$ is turned OFF. Similarly for output phase B and C, the IGBTs $bB1$ and $cC1$ are turned OFF, respectively.

Step 2: Turn ON the active IGBT (which will be conducting) of the incoming bidirectional switch after a delay δt. For output phase A, the IGBT $cA1$ is turned ON. Since voltage v_{ca} and current $i_{AA'}$ are positive, the commutation of load current $i_{AA'}$ happens naturally from $aA1$ to $cA1$. For output phase B, the IGBT $aB2$ is turned ON. The voltage v_{ab} is positive and current $i_{BB'}$ is negative, so the current keeps flowing through $bB2$ and commutation doesn't occur yet in phase B. For output phase C, the IGBT $bC2$ is turned ON. The voltage v_{bc} and current $i_{CC'}$ are negative, hence the current $i_{CC'}$ commutates naturally to IGBT $bC2$.

Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. For output phase A, the IGBT $aA1$ is turned OFF. For output phase B, the IGBT $bB2$ is turned OFF. This causes the load current $i_{BB'}$ to commutate to IGBT $aB2$. For output phase C, the IGBT $cC2$ is turned OFF.

Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting)

of the incoming bidirectional switch after a delay δt. For output phases A, B and C, the IGBTs $cA2$, $aB1$ and $bC1$ are turned ON respectively.

In the above steps, the commutation of load currents $i_{AA'}$ and $i_{CC'}$ is natural and happens in the second step of the four step process. However, the commutation of the load current $i_{BB'}$ is forced and takes place in the third step. This causes the input phase b to be connected to the output phases B and C together for one commutation step. Thus, the condition that each input phase is connected to only one output phase is violated for the period of one commutation step, leading to a non-zero common-mode voltage for that duration. The pole voltages v_A, v_B and v_C are shown in Fig. 5.18(a), displaying the glitch in CMV during four-step commutation. Thus, whenever there are two natural commutations and one forced commutation in the three output phases, there is a glitch in the common-mode voltage.

In the above example, suppose the directions of the load currents are reversed (implying $i_{AA'} < 0$, $i_{BB'} > 0$ and $i_{CC'} > 0$), while keeping the input voltage polarities unchanged. Then the commutation of load currents $i_{AA'}$ and $i_{CC'}$ is forced, while the commutation of load current $i_{BB'}$ happens naturally. This causes the pole voltages of phase B to change one commutation step sooner than that of other two phases, as shown in Fig 5.18(b). Thus, the occurrence of two forced commutations and one natural commutation in the three output phases also results in a glitch in the common-mode voltage.

It was discussed in section 5.7 that due to commutation, a 'square wave' with output fundamental frequency and amplitude proportional to the maximum input line-line voltage appears in a three phase to single phase matrix converter. When three of these voltages, phase shifted by $\frac{2\pi}{3}$ are added, a net square wave is obtained which will have a fundamental frequency equal to three times the output frequency and magnitude proportional to maximum input line-line voltage. This voltage is essentially the low frequency component of the CMV glitches due commutation as discussed in this section. This analysis is in agreement with the discussion in [73].

Table 5.11: Conditions for Natural commutation

sgn(v_{12})	sgn(i)	Natural commutation
+	+	Yes
+	−	No
−	+	No
−	−	Yes

5.9 Modified Four-Step Commutation algorithm

In the conventional four-step algorithm, only the load current directions are used for the commutation process. It is seen from the analysis in the previous section, that the spikes in common-mode voltage occur due to a delay in the change in the pole voltage of a leg that is undergoing forced commutation in comparison with that of a leg undergoing natural commutation. Thus, the idea is to delay the natural commutation so that changes in all three output pole voltages occur simultaneously.

The conditions of natural commutation are identified in Fig. 5.14(a) and Table 5.11. It is assumed that initially, IGBTs 11 and 12 are ON, while after the commutation process, IGBTs 21 and 22 are ON. The load current i is positive in the direction shown by the arrow in Fig. 5.14(a). In Table 5.11, voltage $v_{12} = v_1 - v_2$. It is seen from the table that natural commutation occurs when the pole voltage is going up and output current is positive or when pole voltage is going down and output current is negative.

The state machine for modified four-step commutation is shown in Fig. 5.19(a). Similar to Fig. 5.14(b), the states in Fig. 5.19(a) are denoted by alphabets A through H. The quantities Q_{11}, Q_{12}, Q_{21} and Q_{22} when mentioned in Fig. 5.19(a), denote that the IGBTs 11, 12, 21 and 22 respectively are ON in Fig. 5.14(a). When these quantities are not mentioned, the corresponding IGBTs are OFF. For example, in state A in Fig. 5.19(a), Q_{11} and Q_{12} are mentioned, implying that IGBTs 11 and 12 in Fig. 5.14(a) are ON, while IGBTs 21 and 22 are OFF. The modified four-step commutation algorithm is described below.

1. Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch

2. If the condition of natural commutation is met, turn ON the active IGBT (which

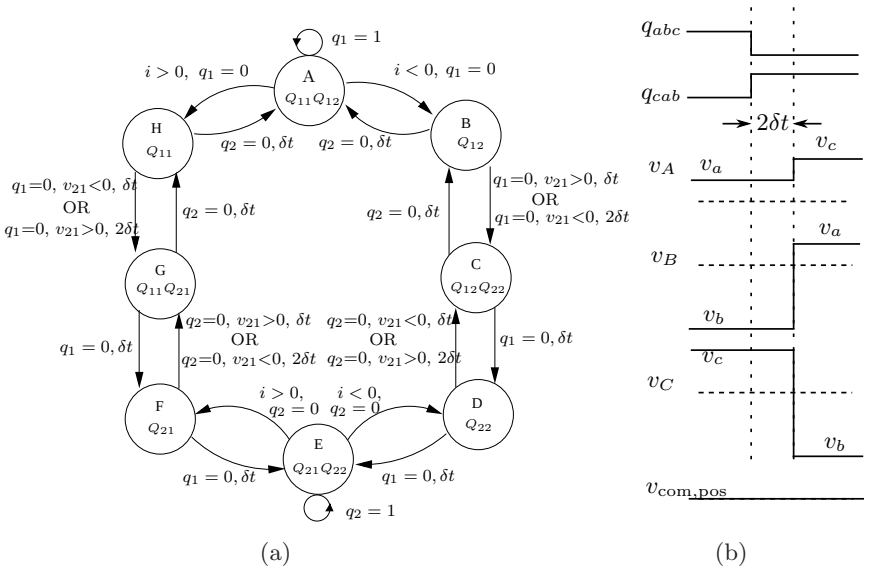


Figure 5.19: (a) State machine diagram for proposed modified four-step commutation (b) Proposed four-step commutation example

will be conducting) of the incoming bidirectional switch after a delay of $2\delta t$, else turn ON the active IGBT after a delay of δt

3. Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay of δt

4. Turn ON the passive IGBT (whose anti-parallel diode will be conducting) of the incoming bidirectional switch

The proposed modified four-step commutation process considers the polarity of voltage between incoming and outgoing bidirectional switches and output current direction and delays the second step of the four-step commutation process by one commutation step (δt) based on that. The delay is introduced when the condition of natural commutation is met. Delaying the second step by an additional δt when natural commutation occurs causes commutation in all phases of a matrix converter to occur together, irrespective of natural or forced nature of the commutation. Thus, a glitch occurring in common-mode voltage due to the commutation process is suppressed by using the proposed modified four-step commutation. The first example discussed in previous section is described again below, this time using the modified commutation algorithm.

Step 1: Turn OFF the passive IGBT (whose anti-parallel diode is conducting) of the outgoing bidirectional switch. Based on Table 5.9 and Table 5.10, for output phase A, the IGBT $aA2$ is turned OFF. Similarly for output phase B and C, the IGBTs $bB1$ and $cC1$ are turned OFF, respectively.

Step 2: Turn ON the active (which will be conducting) IGBT of the incoming bidirectional switch after a delay $2\delta t$ if natural commutation happens, else turn it ON after δt. For output phases A and C, natural commutaion happens. Hence, IGBTs $cA1$ and $bC2$ are turned ON after a delay of $2\delta t$. Thus, the voltage transition in these two phases happens at a delay of $2\delta t$ after the first step. In phase B, natural commutation doesn't happen, so IGBT $aB2$ is turned ON after a delay of δt. The voltage has not yet changed in phase B.

Step 3: Turn OFF the active IGBT (conducting) of the outgoing bidirectional switch after a delay δt. For output phase A, the IGBT $aA1$ is turned OFF. For output phase B, the IGBT $bB2$ is turned OFF. This causes the load current $i_{BB'}$ to commutate to IGBT $aB2$, thus causing the voltage transition in phase B to happen after a delay of $2\delta t$ from the first step. Thus, the voltage transition in all three load phases happens $2\delta t$ after the first step. For output phase C, the IGBT $cC2$ is turned OFF.

Step 4: Turn ON the passive IGBT (whose anti parallel diode will be conducting) of the incoming bidirectional switch after a delay δt. For output phases A, B and C, the IGBTs $cA2$, $aB1$ and $bC1$are turned ON respectively.

As described above, the voltage transition in all three load phases happens $2\delta t$ after the commutation process begins, thus removing the glitch from the common mode voltage. This is illustrated in Fig. 5.19(b). It should be noted, that the modified four step commutation also eliminates the change in low frequency voltage from the output voltage as discussed in section 5.7.

It should be noted, that input voltage sensing is already required for space vector modulation of a matrix converter. Thus, no additional components are required by the proposed commutation process. The state machine in Fig. 5.19(a) corresponds to the commutation between two bidirectional switches. But, it can be expanded to apply to three bidirectional switches for a three-phase to three-phase matrix converter.

Table 5.12: Simulation and experimental parameters for carrier based SVPWM of dual matrix converter open-end winding drive

Parameter	Dual matrix converter
Input voltage (line-line rms)	69.2 V
Input frequency	60 Hz
Output voltage (line-line rms)	69.2 V
Output frequency	28 Hz
Switching frequency	5 kHz
Load	$15.4\angle 36.0^\circ\ \Omega$

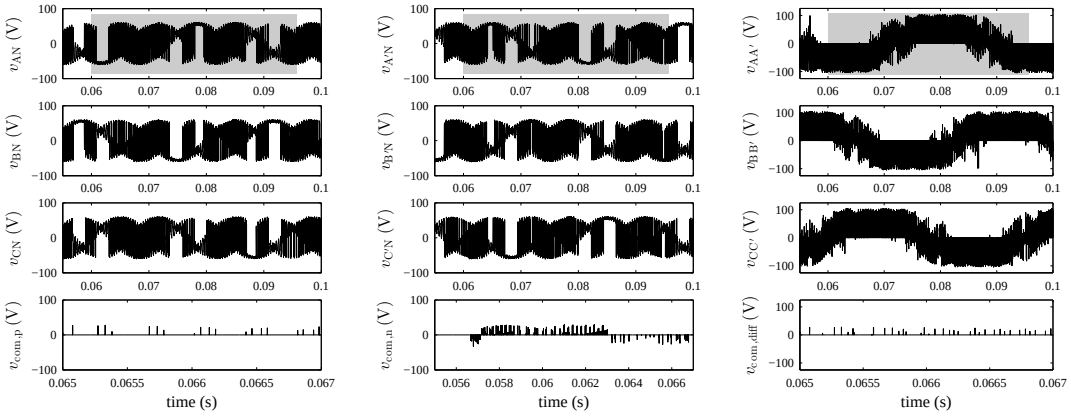
5.10 Simulation and experimental results

5.10.1 Results for Carrier based SVPWM of dual MC

The parameters used for simulation and experimental results for dual matrix converter using carrier based PWM are given in Table 5.12. MATLAB Simulink was used for simulation of the dual MC drive.

The simulation results for carrier based SVPWM of dual matrix converter are shown in Fig. 5.20, Fig. 5.21 and Fig. 5.22. The positive end and negative end pole voltages and common-mode voltage are shown in Fig. 5.20(a) and Fig. 5.20(b) respectively. The voltages across output phases and differential common-mode voltage is shown in Fig. 5.20(c). Commutation periods and device drops have been included in the simulations to remain close to experimental conditions. It is observed that excluding the small glitches due to commutation periods and device drops [73], the positive and negative end common-mode voltages are held flat at 0 V. Thus their average sum and difference should also be zero (ignoring non-idealities), which should help in mitigating the problems of circulating currents and EMI. In all these figures, a gray patch has been drawn in the top graph to denote one cycle of the output fundamental frequency ω_o. In Fig. 5.21, the positive end and negative end pole voltages and voltage across output phases have been shown for one switching cycle for easier viewing. In Fig. 5.22(a), the input voltage v_{aN} and current (filtered and zoomed five times) i_{a} are shown. It can be seen that they are nearly in phase, indicating unity power factor which is due to equal utilization of CCW and CW vectors [26]. Fig. 5.22(b) displays the output currents and the circulating current. The output currents appear balanced and sinusoidal as desired, while the

circulating current is much smaller than the output currents. Finally, in Fig. 5.22(c), the Fourier spectra of voltage $v_{\mathrm{AA}'}$ across output phase A are shown for carrier based and space vector based techniques respectively. The spectra are nearly identical, which implies that the carrier based method generates identical pulses to that of space vector approach.



(a) (b) (c)

Figure 5.20: Simulation results for Dual matrix converter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) (b)Negative end pole voltages (top three graphs) and CMV (bottom graph) (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load

A laboratory prototype was built for experimental validation of the PWM technique. A diagram of the setup is shown in Fig. 5.23. Four step commutation was used with a total commutation period of 1.5 μs. This requires sensing of the load currents. The filter components used are $R_d = 12.5\ \Omega$, $L_f = 1.4$ mH and $C_f = 35\ \mu$F.

The experimental results for dual matrix converter are given in Fig. 5.24 and Fig. 5.25. The positive end and negative end pole voltages and common-mode voltage are shown in Fig. 5.24(a) and Fig. 5.24(b). The voltages across output phases and the differential common-mode voltage are shown in Fig. 5.24(c). A gray patch in the top graphs of these three figures indicates one cycle of output fundamental frequency. It is observed that the positive end, negative end and the differential common-mode voltages are held at zero, barring the glitches due to commutation periods times and

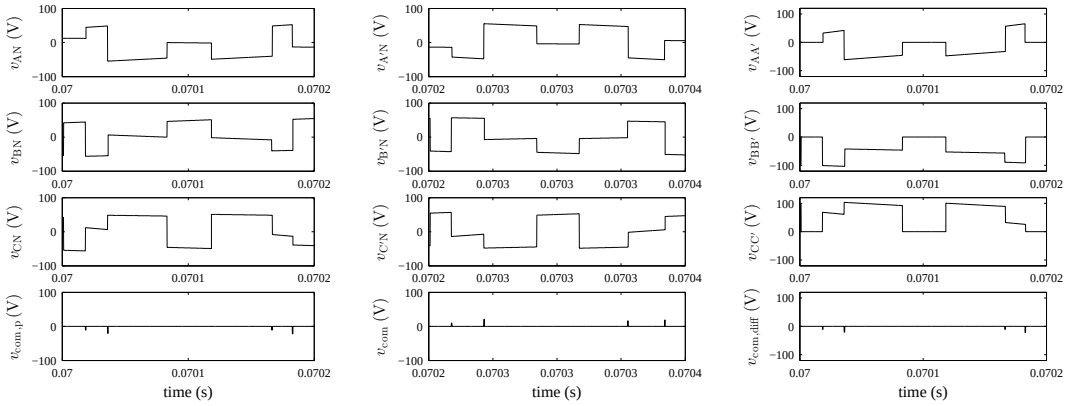


Figure 5.21: Simulation results (Zoomed voltages for Dual matrix converter) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) (b)Negative end pole voltages (top three graphs) and CMV (bottom graph) (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load

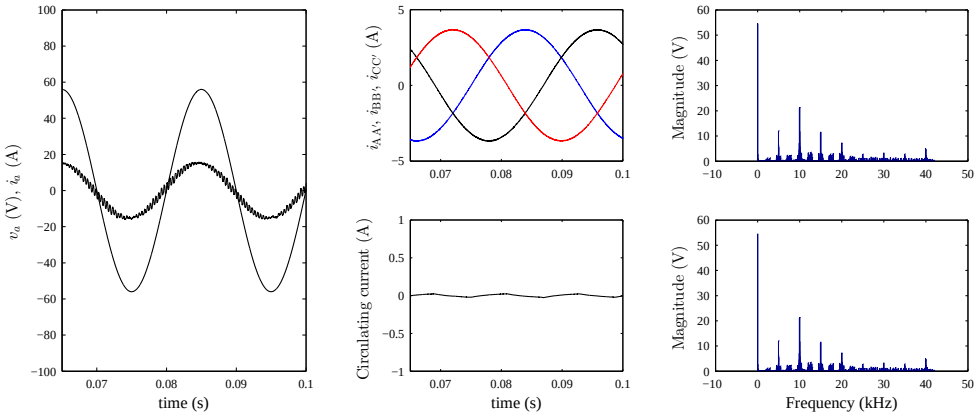


Figure 5.22: Simulation results (Dual matrix converter) (a) Input current (zoomed five times for viewing ease) and voltage of phase a (b) Three phase load currents (top graph) and circulating current (bottom graph) (c) Fourier spectrum of voltage $v_{\mathrm{AA'}}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph)

device drops [73]. Zoomed versions of all these voltages are provided in Fig. 5.24(d)-5.35(a) for better viewing. The input phase voltage v_{aN} and phase current i_{a} are shown

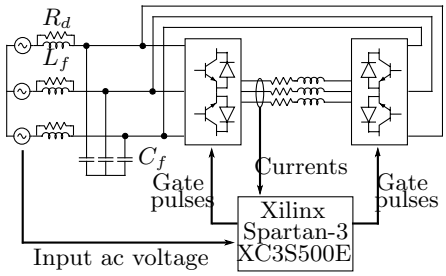


Figure 5.23: Diagram of the experimental setup for dual matrix converter

in Fig. 5.25(a). It can be seen that the input voltage and current (filtered) are nearly in phase (current leads slightly due to input filter), indicating unity power factor due to equal usage of CCW and CW vector [26]. The three phase load currents and circulating current are shown in Fig. 5.25(b). The currents appear as balanced and sinusoidal. The circulating current is non-zero, however much smaller than the load currents. Fourier spectra of the voltage $v_{\mathrm{AA}'}$ are given for PWM of dual matrix converter using carrier based and space vector based approaches in Fig. 5.25(c). It is seen that the spectra are nearly identical and devoid of low order harmonics.

Finally, Fig. 5.26 shows the high frequency spectra of common-mode voltages generated by a single two-level VSI, a dual two-level VSI with common-mode voltage elimination and a dual matrix converter with common-mode voltage elimination. The single VSI and dual VSI were operated at 100 V dc bus voltage and the dual matrix converter was operated with a line-line peak voltage 97.86 V (rms 69.2 V) for this comparison. It can be seen that the high frequency common-mode voltage generated by the dual converters is nearly an order of magnitude lower than that generated by single VSI.

5.10.2 Results for alternative carrier based SVPWM of dual MC drive

The parameters for simulation and experiments for alternative carrier based SVPWM of dual MC drive are given in Table 5.13.

The simulation results for positive end pole voltages and common mode voltage are given in Fig. 5.27(a), while those for negative end are given in Fig. 5.27(b). In both cases, it is observed that the common mode voltage is held at zero, apart from glitches during commutation period, as explained in [73]. In Fig. 5.27(c), the voltage across

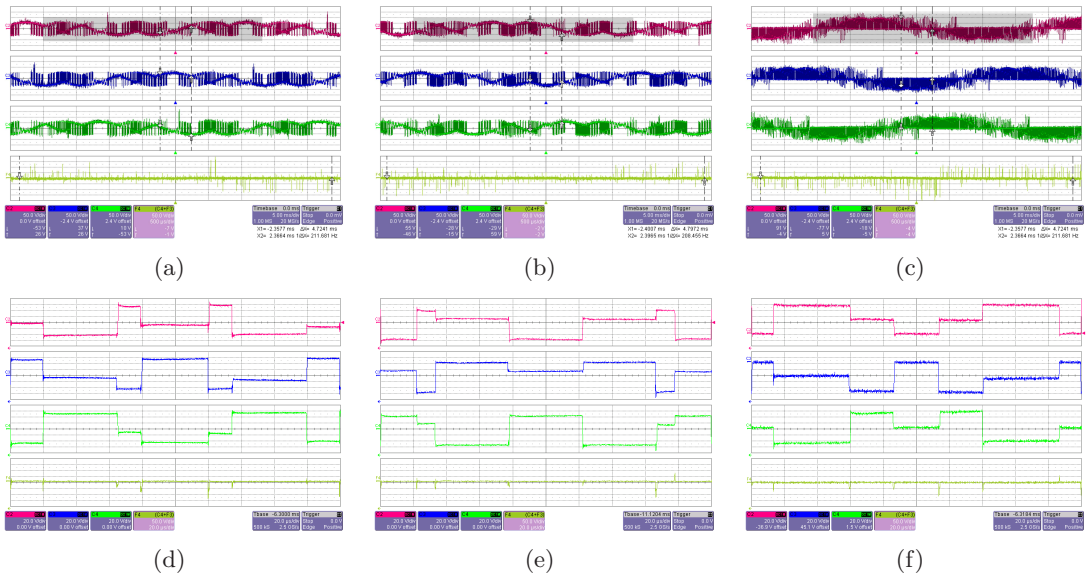
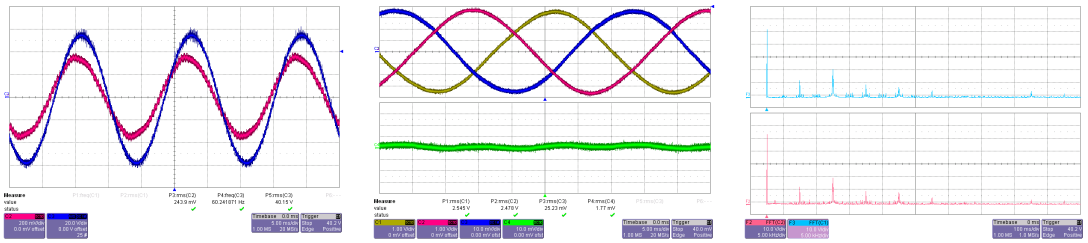


Figure 5.24: Experimental results for Dual matrix inverter (gray patch in top graphs indicates the length of one cycle of output fundamental frequency) (a) Positive end pole voltages (top three graphs) and common-mode voltage (CMV) (bottom graph) [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (b) Negative end pole voltages (top three graphs) and CMV (bottom graph) [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (c) Voltages across load phases (top three graphs) and CMV (bottom graph) across load [X axis: 2 ms/div (top three graphs) 200 μs/div (bottom graph), Y axis: 50 V/div] (d)Positive end pole voltages and CMV [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)] (e)Negative end pole voltages and CMV [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)] (f) Phase voltages and CMV across load [X axis: 20μs/div, Y axis: 20 V/div (top three waveforms) 50V/div (bottom waveform)]

load phase $v_{\mathrm{AA}'}$, current through load phase $i_{\mathrm{AA}'}$, input phase voltage v_{aN} and filtered input phase current i_a are shown. It is observed that the load current is sinusoidal which desirable. The filtered input current i_a is nearly in phase with input phase voltage v_{aN} due to equal utilization of CCW and CW vectors in the modulation [26]. All of these results are further confirmed by experimental findings, as shown in Fig. 5.28.

Finally, the simulation result for Fourier spectra of load phase voltage $v_{\mathrm{AA}'}$ is given in Fig. 5.29. The top graph shows the Fourier spectrum using the proposed algorithm while the bottom algorithm shows the same using general space vector theory. It is



(a) (b) (c)

Figure 5.25: Experimental results (dual matrix converter) (a) Input current and voltage of phase a [X axis: 5 ms/div, Y axis: 20V/div, 2A/div] (b) Three phase load currents (top graph) and circulating current (bottom graph) [X axis: 2 ms/div, Y axis: 1 A/div] (c) Fourier spectrum of voltage $v_{\mathrm{AA}'}$ across load phase A using carrier based method (top graph) and space vector method (bottom graph) [X axis: 5 kHz/div, Y axis: 10 V/div]

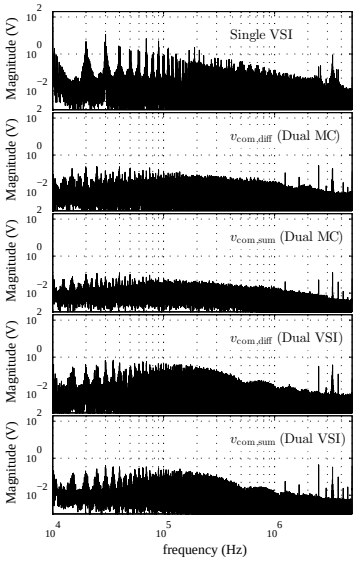
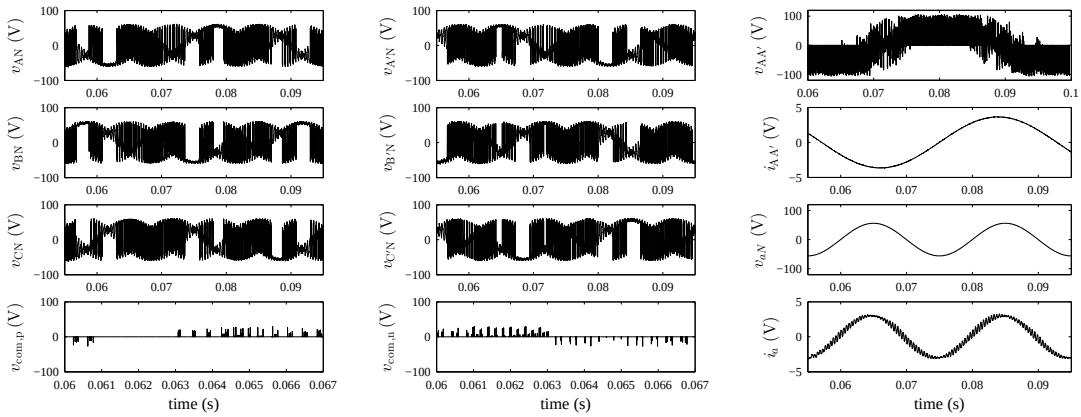


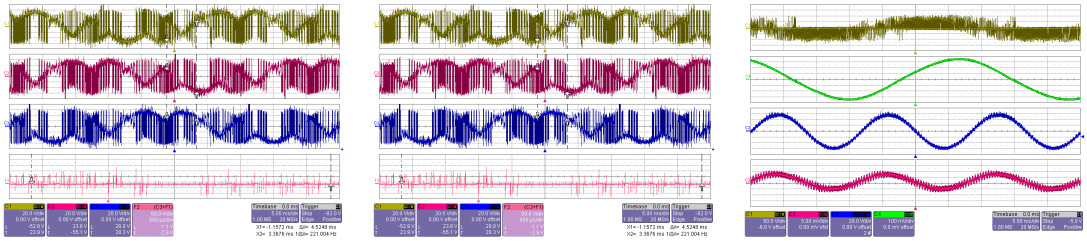
Figure 5.26: High Frequency frequency spectrum of common-mode voltages (CMV) (experimental results): Single VSI (top graph), Differential CMV (Dual matrix converter) (Second graph), Average CMV (Dual matrix converter) (Third graph), Differential CMV (Dual two-level inverter) (Fourth graph), Average CMV (Dual two-level inverter) (Bottom graph)

observed that the Fourier spectra are nearly identical. This is further confirmed by the experimental result shown in Fig. 5.30.



(a) (b) (c)

Figure 5.27: Simulation results (alternative carrier based method for SVPWM) (a) Positive end pole voltages (top three graphs) and common mode voltage (bottom graph) (b) Negative end pole voltages (top three graphs) and common mode voltage (bottom graph) (c) Output phase voltage $v_{\mathrm{AA'}}$, phase current $i_{\mathrm{AA'}}$, input phase voltage v_{aN} and current i_a



(a) (b) (c)

Figure 5.28: Experimental results (alternative carrier based method for SVPWM) (a) Positive end pole voltages (top three graphs) and common mode voltage (bottom graph) (b) Negative end pole voltages (top three graphs) and common mode voltage (bottom graph) (c) Output phase voltage $v_{\mathrm{AA'}}$, phase current $i_{\mathrm{AA'}}$, input phase voltage v_{aN} and current i_a

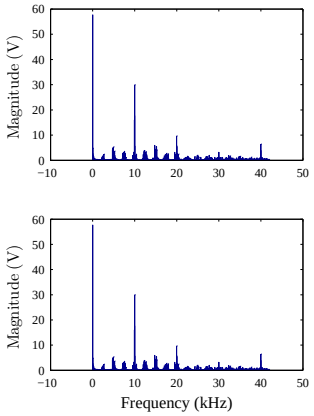


Figure 5.29: Simulation result (alternative carrier based method for SVPWM) for frequency spectra of output phase voltage $v_{\mathrm{AA}'}$ using proposed algorithm (top graph) and general space vector approach (bottom graph)

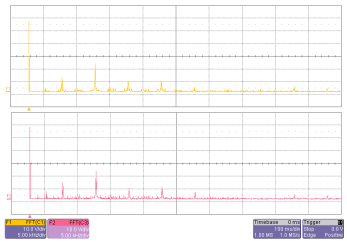


Figure 5.30: Experimental result (alternative carrier based method for SVPWM) for frequency spectra of output phase voltage $v_{\mathrm{AA}'}$ using proposed algorithm (top graph) and general space vector approach (bottom graph)

5.10.3 Results for modified four step commutation

A simulation of a dual matrix converter with the conventional four-step commutation and proposed modified four-step commutation has been done using MATLAB Simulink and the results have been presented for comparison. The simulation was done with 208 V line-line input rms voltage at 60 Hz and 135 V line-line output rms voltage at 15 Hz. The load is 50 kW at 0.8 power factor. The four-step commutation step δt is kept at 4 μs. The switching frequency is kept at 5 kHz.

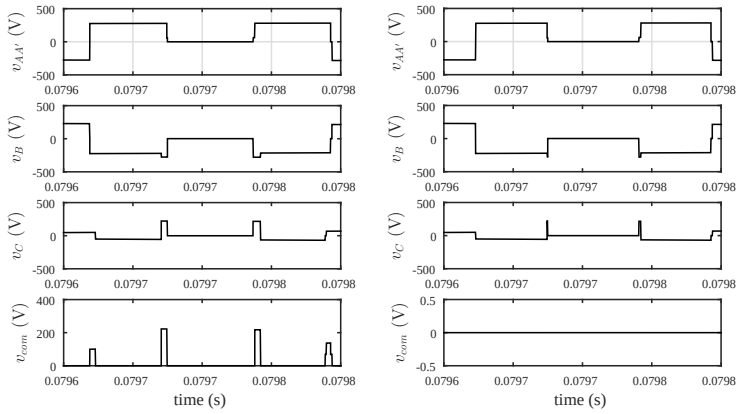


Figure 5.31: Simulation results (a) Load voltages and common-mode voltage for one carrier cycle, using conventional four-step commutation (b) Load voltages and common-mode voltage for one carrier cycle, using modified four-step commutation

In Fig. 5.31(a), the voltages across the three output phases and the common mode

Table 5.13: Simulation and experimental parameters for alternative carrier based SVPWM of dual MC drive

Parameter	Value
Input voltage V_i (line-line rms)	70 V
Input frequency f_i	60 Hz
Output voltage V_o	70 V
Output frequency f_o	30 Hz
Switching frequency f_{sw}	5 kHz
Load	$15.79\angle 37.9°$ Ω

voltage across the load are shown for one switching period, when using conventional four-step commutation. The same have been shown in Fig. 5.31(b) when using modified four-step commutation. Common mode voltage spikes are visible in Fig. 5.31(a) due to voltage transitions not happening at the same time(as discussed in section 5.8), whereas they are eliminated when using the modified four-step commutation, as observed in Fig. 5.31(b) (as discussed in section 5.9).

The three phase load currents and the frequency spectrum of load current in one phase are shown in Fig. 5.32(a) and Fig. 5.32(b) when using conventional and modified four-step commutation algorithms respectively. It is observed that the third harmonic component seen in Fig. 5.32(a) is nearly eliminated in Fig. 5.32(b). Finally, plots of circulating current and its frequency response are shown in Fig. 5.33(a) and Fig. 5.33(b) when using conventional and modified -four step commutation algorithms respectively. The reduction of the circulating current when using modified four-step commutation is clearly visible both in the time domain plots and in the frequency spectra.

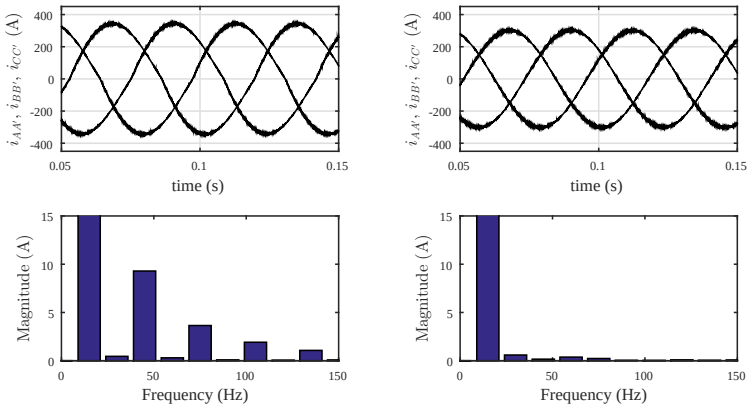


Figure 5.32: Simulation results (a) Three-phase load currents and Fourier spectrum of one load current, using conventional four-step commutation (b) Three-phase load currents and Fourier spectrum of one load current, using modified four-step commutation

The proposed modified four-step commutation and conventional four-step commutation have been implemented on a dual matrix converter drive. The hardware setup diagram is shown in Fig. 5.34. The matrix converter drive was built using Microsemi

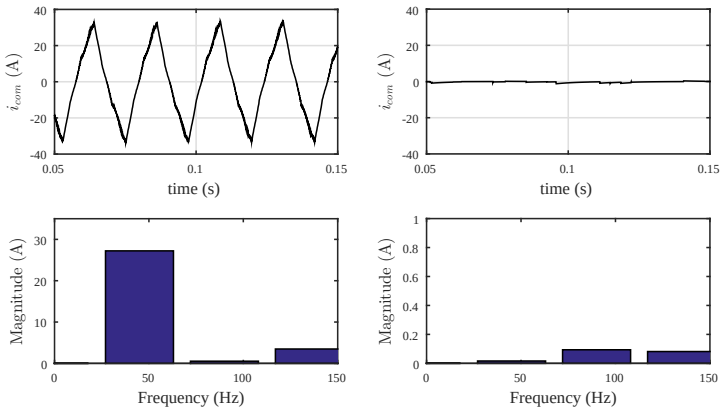


Figure 5.33: Simulation results (a) Circulating current through the load and its Fourier spectrum, using conventional four-step commutation (b) Circulating current through the load and its Fourier spectrum, using modified four-step commutation

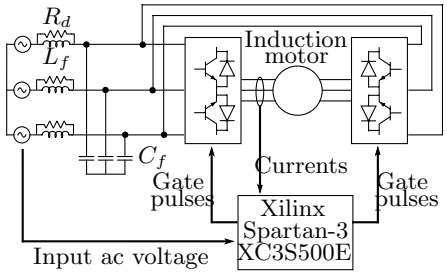


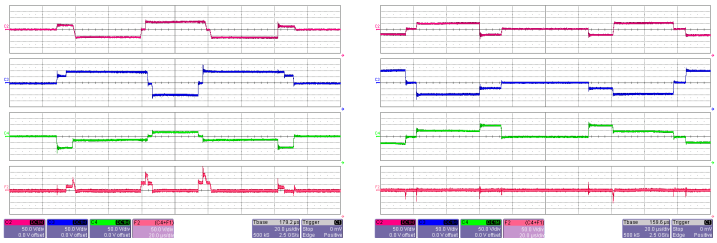
Figure 5.34: Hardware setup diagram for modified commutation tests

APTGT75TDU120PG IGBT modules and Concept 2SD106AI gate drivers. The electric motor used in the drive was a Baldor ZDM3581T, which is a 1 HP, 4 pole induction machine. The filter components used are $R_d = 12.5\ \Omega$, $L_f = 1.4$ mH and $C_f = 35$ μF. The output voltage across the machine was 36.7 V line-line rms at 12 Hz output frequency, while the input voltage was 86 V line-line rms at 60 Hz. The commutation interval δt was kept at 4.5 μs, while the switching frequency was 5kHz.

The voltages across the three output phases and the common mode voltage across the load are shown for one switching period in Fig. 5.35(a) and Fig. 5.35(b). It is seen that glitches appear in common-mode voltage in Fig. 5.35(a) (where conventional four-step commutation is used), as explained in section 5.8 and these glitches are nearly

eliminated in Fig. 5.35(b) when using modified four-step commutation. The three-phase load currents and frequency spectrum of one load current are shown in Fig. 5.36(a) and Fig. 5.36(b). When using conventional four-step commutation as seen in Fig. 5.36(a), the magnitude of the third harmonic, which is at 36 Hz is seen to be nearly equal to 0.62 A. When the same results are taken using the modified commutation as seen in Fig. 5.36(b), the third harmonic reduces to 0.2 A.

The circulating current and its frequency spectrum have been shown in Fig. 5.37(a) when using conventional four-step commutation and in Fig. 5.37(b) when using modified four-step commutation. It is seen that the magnitude of the fundamental component of the circulating current (at 36 Hz) goes from 1.77 A to 0.52 A when using modified four-step commutation.

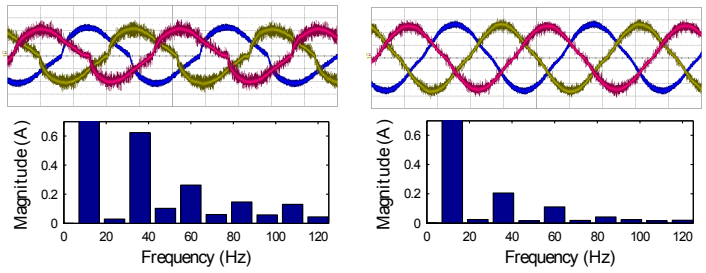


(a) (b)

Figure 5.35: Experimental results (a) Load voltages and common-mode voltage for one carrier cycle, using conventional four step commutation [X-axis: 20 μs/div, Y-axis: 50 V/div] (b) Load voltages and common-mode voltage for one carrier cycle, using modified four step commutation [X-axis: 20 μs/div, Y-axis: 50 V/div]

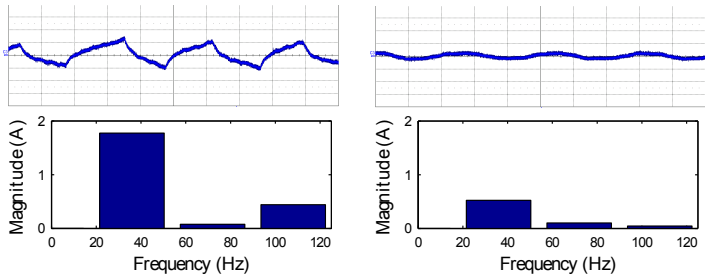
5.11 Conclusion

In this chapter, two methods for carrier based implementation of SVPWM of a dual MC drive were discussed. It was observed that the carrier based implementation is faster in computation speed and takes less resources than the direct space vector based approach. The carrier based methods offer the same benefits of CMV suppression and input power factor control as the space vector based approach. Finally, the effect of commutation in a practical matrix converter drive were analyzed to see how it affects the output voltage and the CMV. A modification in the conventional four step commutation process was



(a) (b)

Figure 5.36: Experimental results (a) Three-phase load currents and Fourier spectrum of one load current, using conventional four step commutation [For load current graphs: X-axis - 20ms/div, Y-axis - 2A/div] (b) Three-phase load currents and Fourier spectrum of one load current, using modified four step commutation [For load current graphs: X-axis - 20ms/div, Y-axis - 2A/div]



(a) (b)

Figure 5.37: Experimental results (a) Circulating current through the load and its Fourier spectrum, using conventional four step commutation [For circulating current graphs: X-axis - 10ms/div, Y-axis - 2A/div] (b) Circulating current through the load and its Fourier spectrum, using modified four step commutation [For circulating current graphs: X-axis - 10ms/div, Y-axis - 2A/div]

proposed which was found to be effective in reducing the CMV glitches and circulating currents due to the commutation process.

Note: Parts of this chapter have been reproduced from IEEE publications [74, 78, 79].

Chapter 6

Reduced Swith Power Electronic Transformer with Open-end Winding Matrix Converter Drive with primary side snubber elimination

In this chapter, the operation of reduced switch Power Electronic Transformer (PET) with dual matrix converter (MC) drive has been explained. The topology was introduced in the first chapter of this thesis. In chapter 5, carrier based PWM techniques were developed to implement SVPWM for a dual MC drive with common mode voltage (CMV) elimination. The dual MC drive is operated with the same method in order to generate zero CMV. In addition, soft switching of primary side switches in the PET will be achieved, as will be shown in the discussion.

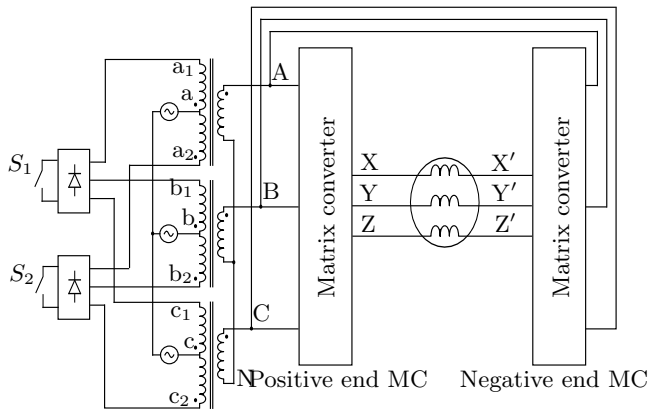


Figure 6.1: Reduced switch count PET with dual matrix converters

6.1 System description

The proposed system consists, as shown in Fig. 6.1, of a reduced switch count high frequency PET based on push-pull principle presented in [80] with dual matrix converters on the secondary side to drive open-end winding loads. The matrix converters have been labeled as positive end and negative end matrix converters.

The switches S_1 and S_2 are switched in complimentary fashion with a 50% duty ratio. This results in the secondary side voltages v_{AN}, v_{BN} and v_{CN} to be chopped sinusoidal waveforms, as demonstrated in Fig. 6.2 for phase a. When gate pulse q_{S_1} is HIGH, the switch S_1 is ON and the voltage v_{AN} equals v_a. When gate pulse q_{S_2} is HIGH, the switch S_2 is ON and the voltage v_{AN} equals $-v_a$. These chopped three phase ac voltages on the secondary side of transformer are fed to the dual matrix converters to synthesize ac voltage of desired frequency at the load terminals. The common-mode voltage $v_{com,p}$ at the positive end load terminals X, Y and Z is defined as in (6.1).

$$v_{com,p} = \frac{v_X + v_Y + v_Z}{3} \tag{6.1}$$

The common-mode voltage $v_{com,n}$ at negative end load terminals X′, Y′ and Z′ is defined as in (6.2).

$$v_{com,n} = \frac{v_{X'} + v_{Y'} + v_{Z'}}{3} \tag{6.2}$$

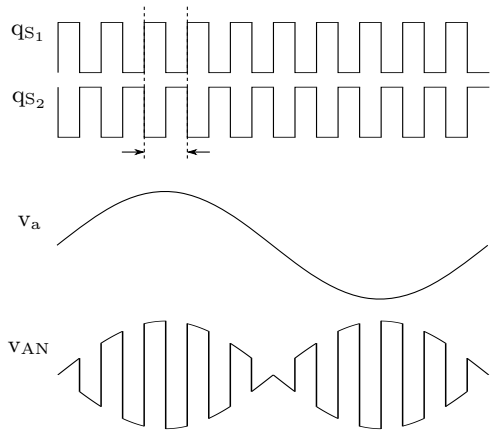


Figure 6.2: Primary side switches' pulses and primary and secondary phase a voltage (switching frequency of S_1 and S_2 is much higher than shown in the figure as compared to fundamental frequency of sine)

In (6.1), v_X is the instantaneous voltage at load terminal X w.r.t. secondary neutral point N in Fig. 6.1. The other quantities in the equations (6.1) and (6.2) are defined similarly.

6.2 PWM strategy to eliminate input snubber requirement and common-mode voltage across load terminals

The synchronously rotating vectors for the positive and negative end matrix converters are shown in Fig. 6.3. There are three counter clockwise (CCW) rotating vectors and three clockwise (CW) rotating vectors for a matrix converter. But due to the switching operation of switches S_1 and S_2 on the primary side of the transformer, there is an additional set of CCW and CW vectors for both matrix converters when S_2 is ON. These vectors are denoted by dotted lines in all sub-figures of Fig. 6.3 and are equal in magnitude and opposite in direction to the vectors represented by solid lines when S_1 is ON. The set of vectors active when S_1 is ON is called set I from here on, while the other set is called set II. The magnitude of all vectors in both sets is $\frac{3}{2}V_i$, where V_i is the amplitude of phase voltage on the primary side. The quantities in brackets indicate the connections of load terminals to transformer secondary terminals when a space vector is applied. For example, in Fig. 6.3(a), when vector $\mathbf{U_{ABC}}$ is active, then

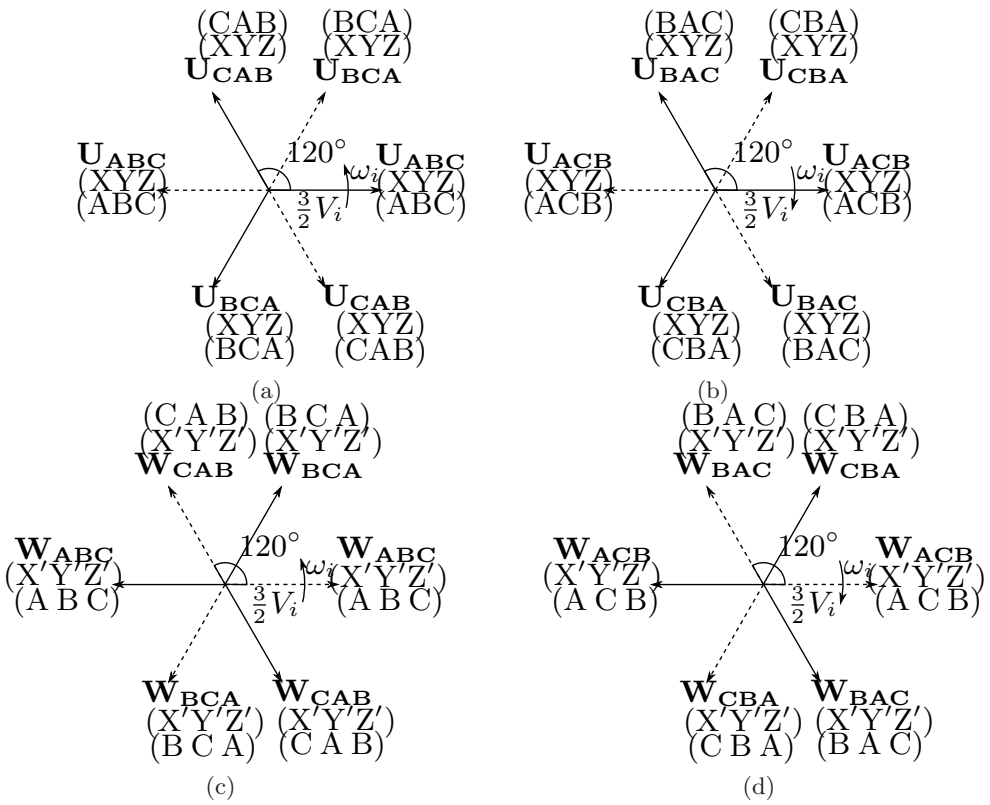


Figure 6.3: Synchronous vectors for positive end and negative end matrix converters (Solid line vectors are active when S_1 is ON while dotted line vectors are active when S_2 is ON) (a)Positive end CCW vectors (b) Positive end CW vectors (c) Negative end CCW vectors (d) Negative end CW vectors

load terminals X, Y and Z are connected to transformer secondary terminals A, B and C respectively.

The synchronously rotating vectors have one transformer secondary terminal (A, B or C) connected to exactly one load terminal on positive end (X, Y or Z). Imposing the condition that the transformer primary side voltages are balanced, the positive end common-mode voltage defined in (6.1) is zero whenever synchronously rotating vectors are applied. The negative end common-mode voltage defined in (6.2) is also zero due to the same reasoning when synchronously rotating vectors are used. Thus, the common-mode voltage at the load is zero whenever synchronously rotating vectors are used for PWM of dual matrix converters.

The zero vectors applied in [81] are connecting all load terminals to a single transformer secondary terminal and it leads to switching common-mode voltage. This can be done for the open-end winding converter too, but in a dual matrix converter, there are additional zero vectors available. These zero vectors are formed by applying the same synchronous vector to both positive end and negative end converter [26]. As an example, the vector $\mathbf{U_{ABC}}$ and $\mathbf{W_{ABC}}$ are being applied to positive and negative end converters. Then, the load terminals X and X$'$ are connected to transformer secondary terminal A and thus, no current flows through the phase a transformer secondary winding. Similarly, the phases b and c have zero currents as well.

Thus, if the zero vectors are applied at the periphery of a switching period, then the transition between S_1 and S_2 will happen during zero vector application, when no current flows on the primary side. This leads to ZCS for S_1 and S_2. Since the PWM can be achieved with zero vectors comprising of synchronously rotating vectors, zero common-mode voltage is achieved at all times at positive ($v_{com,p}$) and negative ($v_{com,n}$) end terminals of the load. Thus, the common-mode voltage v_{com} across the load is always zero.

The positive and negative end CCW vectors in set I can be combined which results in six resultant vectors ($\mathbf{V_1}$ to $\mathbf{V_6}$) of magnitude $\sqrt{3}\frac{3}{2}V_i$, as shown in Fig. 6.4. The CCW vectors in set II also result in the same six resultant vectors. Thus, even though the vectors in set I and set II are only available for 50% of the time (due to S_1 and S_2 having 50% duty ratio), the resultant vectors $\mathbf{V_1}$ through $\mathbf{V_6}$ have 100% availability. Hence, the maximum magnitude of output voltage space vector $\mathbf{V_o}$ that can be synthesized is $\frac{\sqrt{3}}{2} \times \sqrt{3}\frac{3}{2}V_i$ i.e. $2.25V_i$. The amplitude of maximum output phase voltage is $\frac{2}{3}$ times of magnitude of maximum output voltage vector, so it is $\frac{2}{3} \times 2.25V_i$ i.e. $1.5V_i$. This is three times the maximum output voltage that can be synthesized using a single matrix converter as discussed in [81].

The output voltage space vector $\mathbf{V_o}$ can be in any of the six sectors formed by $\mathbf{V_1}$ to $\mathbf{V_6}$. In Fig. 6.4, it is depicted to be in sector 1. The switching strategy is now explained for sector 1. The vectors $\mathbf{V_1}$ and $\mathbf{V_2}$ are used to synthesize $\mathbf{V_o}$ as an average

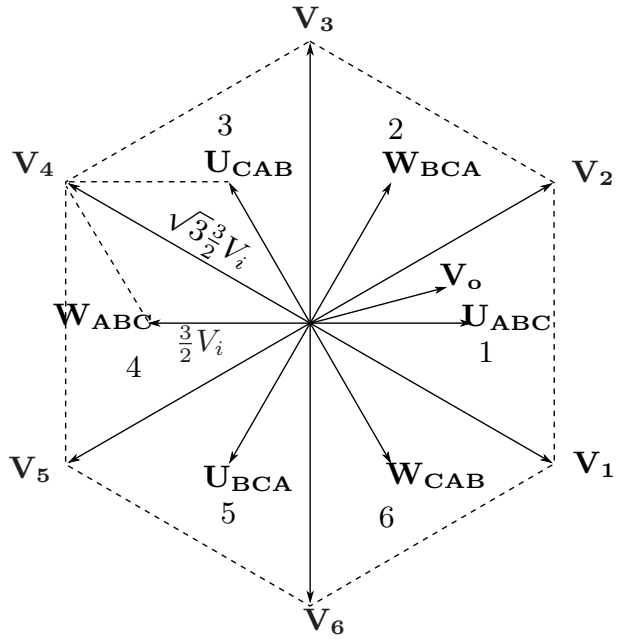


Figure 6.4: Combined space vectors formed by set I CCW vectors

over a switching time period, as given in (6.3).

$$d_1\mathbf{V_1} + d_2\mathbf{V_2} = \mathbf{V_o} \tag{6.3}$$

$$1 - (d_1 + d_2) = d_z \tag{6.4}$$

Once the duty ratios d_1 and d_2 are determined, the set I and set II vectors required to synthesize $\mathbf{V_1}$ and $\mathbf{V_2}$ are applied with these duty ratios. The zero vectors are applied for the remaining period, i.e. with a duty ratio of d_z as defined in (6.4). Using zero vectors at the periphery of a switching time period facilitates ZCS of primary side switches S_1 and S_2, as discussed before in this section. A diagram of the switching pulses is shown in Fig. 6.5. The signals $q_{\mathbf{U_{ABC}}}$ to $q_{\mathbf{W_{CAB}}}$ are the pulses for the CCW vectors at both positive and negative end. It is seen in Fig. 6.5 that the duty ratios of positive and negative end vectors are essentially interchanged as the switch S_1 goes OFF and S_2 is turned ON. The periods when zero vector is applied are denoted by grey regions bounded by the dashed lines in the figure. Any one of the three possible zero vectors can be applied in this period. In the example shown in the Fig. 6.5, the zero vector applied is formed by applying $\mathbf{U_{ABC}}$ and $\mathbf{W_{ABC}}$ at positive and negative end

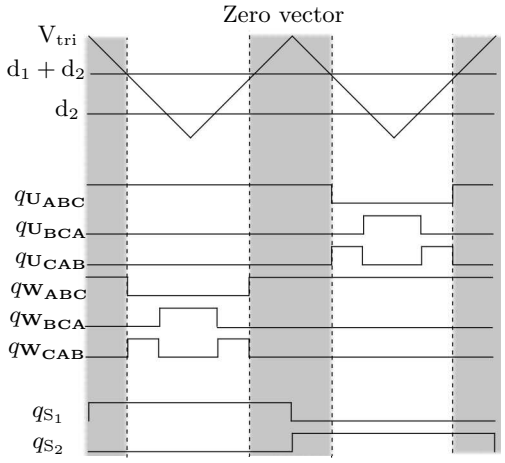


Figure 6.5: Pulses in a switching period in Sector 1

matrix converters respectively. It is also noticed that the transition between S_1 and S_2 happens when the zero vector is active. Based on this analysis, the duty ratios for the active vectors in all sector are summarized in Table. 6.1. Using this table, the active

Table 6.1: Duty ratios of CCW vectors in all six sectors

Vector \ Sector	1		2		3		4		5		6	
	S_1	S_2	S_1	S_2	S_1	S_2	S_1	S_2	S_1	S_2	S_1	S_2
$\mathbf{U_{ABC}}$	1	d_z	d_1	0	0	d_2	d_z	1	0	d_1	d_2	0
$\mathbf{U_{CAB}}$	0	d_1	d_2	0	1	d_z	d_1	0	0	d_2	d_z	1
$\mathbf{U_{BCA}}$	0	d_2	d_z	1	0	d_1	d_2	0	1	d_z	d_1	0
$\mathbf{W_{ABC}}$	d_z	1	0	d_1	d_2	0	1	d_z	d_1	0	0	d_2
$\mathbf{W_{CAB}}$	d_1	0	0	d_2	d_z	1	0	d_1	d_2	0	1	d_z
$\mathbf{W_{BCA}}$	d_2	0	1	d_z	d_1	0	0	d_2	d_z	1	0	d_1

vectors' duty ratios can be determined in a sector once d_1 and d_2 are determined. A zero vector is applied to both matrix converters during remaining period.

The analysis is similar for CW vectors, giving a similar table as Table. 6.1 for duty ratios in all six sectors. By controlling the ratio of CCW and CW vectors, the power factor on the primary side of the transformer can be controlled as explained in [26].

Table 6.2: Simulation parameters

Parameter	Value
Input voltage (line to line rms)	208 V
Input frequency	60 Hz
Output voltage (line to line rms)	260 V
Output frequency	45 Hz
Output power	10 kW
Output power factor	0.8
Matrix converter switching frequency	5 kHz
Transformer turns ratio	1:1:1

6.3 Simulation results

The reduced switch count high frequency PET with dual matrix converters is simulated in MATLAB Simulink. Plecs blockset was used to create the transformer and matrix converter models in Simulink. The simulation parameters are given in Table. 6.2.

The simulation results are shown in Fig. 6.6. Four step commutation has been included for the matrix converters, with 0.5μs being the duration of one step in the four step process. Due to this, there are glitches in common-mode voltages, as explained in [73]. In Fig. 6.6(a), the pole voltages at positive end load terminals (X, Y, Z) are shown in the top three graphs, while the bottom graph shows the positive end common-mode voltage $v_{com,p}$ which is zero, save for the commutation glitches. Similarly, in Fig. 6.6(a), the pole voltages at negative end load terminals (X$'$, Y$'$, Z$'$) are shown in the top three graphs, while the bottom graph shows the positive end common-mode voltage $v_{com,n}$ which is zero, save for the commutation glitches. Since, the common-mode voltages at positive and negative end load terminals are zero, the common-mode voltage across the load is zero as well.

In Fig. 6.6(c), the current through load phase X is shown in the second graph and is sinusoidal. The voltage and filtered current for input phase a are shown and it is observed that the current is nearly in phase with the voltage. This is due to equal utilization of CCW and CW vectors, leading to unity input power factor [26]. Finally in Fig. 6.6(d), the gate pulses for the primary side switches S_1 and S_2 are shown along with the currents flowing through them. It can be seen that when the pulses change their value, the current through the switches is zero, giving zero current switching for

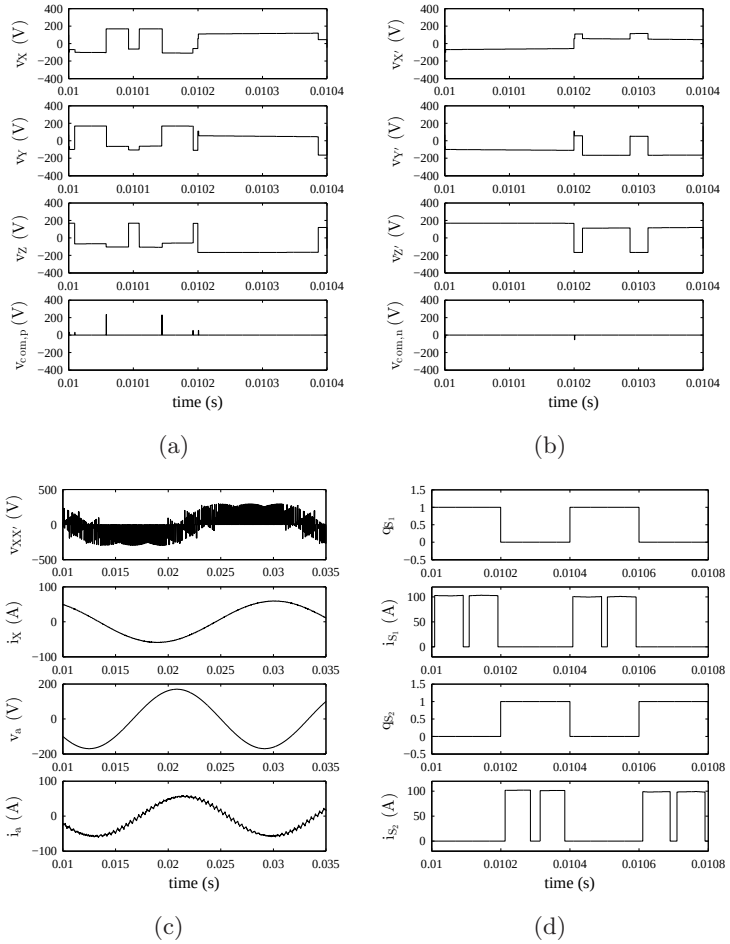


Figure 6.6: Simulation results (a) Voltages at positive end load terminals X, Y and Z and common-mode voltage at positive end for one switching period (b) Voltages at negative end load terminals X′, Y′ and Z′ and common-mode voltage at negative end for one switching period (c) Output voltage across and current through load phase X, input phase a voltage and current (filtered) (d) Gate pulses and currents for primary side switches S_1 and S_2

primary side.

Note: Parts of this chapter have been reproduced from IEEE publication [82].

Chapter 7

Conclusion and Discussion

In this thesis, power electronic transformer topologies based on a push-pull scheme were investigated. In chapters 2 and 3, single phase AC/DC and three phase AC/DC PET topologies were respectively studied and following conclusions were drawn:

1. The power transfer capability of both single phase and three phase PET is much larger in outer mode regions than the inner mode region that was previously studied

2. Soft switching of secondary side switches is achieved in outer mode regions similar to inner mode regions for both single phase and three phase PET

3. Soft switching of primary side switches is lost in outer mode regions for both single phase and three phase cases

4. Single phase PET has a significant third harmonic in the outer mode region, which can be nearly eliminated by appropriate third harmonic injection in the voltage produced by the secondary side H-bridge

5. Closed loop control of dc link in three phase PET is achieved by a simple PI controller, which can be designed by a simple procedure

6. During unbalanced grid voltages, nearly constant power flow can be achieved by generating appropriate negative sequence voltage from the secondary side VSI for the three phase PET. This is useful for a grid connected system where faults can

create unbalanced voltages which could lead to a second harmonic in the power flow, which is highly undesirable.

In chapters 4 and 5, open-end winding dual Voltage Source Inverter (VSI) and dual Matrix Converter (MC) drives were studied. Following conclusions were drawn from these studies:

1. The SVPWM for both dual VSI and dual MC drives for Common Mode Voltage (CMV) elimination has similarities in terms of the space vector setup. These similarities were used to develop a common carrier based strategy for implementing SVPWM for both drives for CMV elimination

2. The carrier based strategy was found to use fewer computations than the conventional space vector approach

3. Conventional four step commutation causes a net change in the output voltage of a matrix converter, which depends on the magnitude of the input voltages and direction of the output current. The low frequency of the excess voltage caused by commutation leads to circulating currents in dual MC drive, while the high frequency component leads to CMV spikes.

4. A modification in the conventional four step method can help in reduction of these CMV spikes and hence in reduction of circulating currents

Finally in chapter 6, a reduce switch AC/AC PET with dual MC drive was proposed which has the advantages of input open loop power factor control, CM elimination at load terminals and soft switching of primary side switches.

Some suggestions for future work related to the topics covered in this thesis are as follows.

1. Design of three winding transformer with minimization of leakage inductance on the primary windings. Lower leakage inductance would lead to fewer losses due to leakage energy commutation.

2. More rigorous analysis of harmonics in the primary side current for the single phase PET and analytical expressions for harmonic compensation coefficients.

3. Reactive power control in three phase and single phase PET. In a grid tied system, reactive power control is important, since the grid might need reactive power support during faults.

4. Study of the three phase PET with multi-level VSI instead of two level VSI. A multi-level VSI can generate more voltage levels, resulting in a smoother current through the inductor and it could lead to lower ripple in dc link current.

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