Power Management Techniques for Supercapacitor Based IoT Applications

A THESIS

SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL

OF THE UNIVERSITY OF MINNESOTA

BY

Xingyi Hua

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

Doctor of Philosophy

Advisor: Professor Ramesh Harjani

January, 2018

Acknowledgements

Firstly, I want to express my great gratitude to my advisor, Prof. Ramesh Harjani. He not only helped me to build solid fundamental knowledge of analog IC design, but also inspired me to do independent research in many ways. Every time I run into a conundrum, he would be very helpful to solve it, by either referring me to previous articles or coming up new ideas. He always sees into the problem and finds out the most critical insights. His strict requirements and high standard demands continuously encourage and impel me to try harder. I feel myself not only being more professional in my major, but also becoming a more responsible person, after this five years.

I also appreciate Prof. Rhonda Franklin, Prof. Chris Kim and Prof. Hubert Lim for reviewing my thesis and participating my Preliminary Oral Exam and PhD Final Defense. I have also taken all the three professors' courses, where I gained very valuable knowledge and enormous guidance.

Thirdly, I must thank my labemates: Martin, Sudhir, Mohammad, Sachin, Rakesh, Ashutosh, Mustafijur, Hundo, Anindya, Saurabh, Qingrui, Naser, Zhiheng, Shiva, etc. All of them are very smart and hard working. They also have been very helpful during my pursuing for my degree. They selflessly shared their techniques of using simulation tools and testing equipment, as well as providing plenty of innovations.

The US Army's Telemedicine and Advanced Technology Research Center (TATRC) has provided great funding support during my research. IC design is a very expensive industry, for the costly fabrication and testing equipment. Without their support, I cannot have access to the superior resources and focus on my research. In addition, ECE department of UMN also provided much logistic, resources and funding help.

Last but not least I wan to thank my parents, my beloved wife and my adorable daughter. They are always there to accompany and support me to get over the humps.

Dedication

To my dear wife and daughter

Abstract

The emerging internet of things (IoT) technology will connect many untethered devices, e.g. sensors, RFIDs and wearable devices, to improve health lifestyle, automotive, smart buildings, etc. This thesis proposes one typical application of IoT: RFID for blood temperature monitoring. Once the blood is donated and sealed in a blood bag, it is required to be stored in a certain temperature range (+2∼+6°C for red cell component) before distribution. The proposed RFID tag is intended to be attached on the blood bag and continuously monitor the environmental temperature during transportation and storage. When a reader approaches, the temperature data is read out and the tag is fully recharged wirelessly within 2 minutes. Once the blood is distributed, the tag can be reset and reused again.

Such a biomedical application has a strong aversion to toxic chemicals, so a batteryless design is required for the RFID tag. A passive RFID tag, however, cannot meet the longevity requirement for the monitoring system (at least 1 week). The solution of this thesis is using a supercapacitor (supercap) instead of a battery as the power supply, which not only lacks toxic heavy metals, but also has quicker charge time (∼1000x over batteries), larger operating temperature range (-40∼+65°C), and nearly infinite shelf life. Although nearly perfect for this RFID

application, a supercap has its own disadvantages: lower energy density (∼30x smaller than batteries) and unstable output voltage. To solve the quick charging and long lasting requirements of the RFID system, and to overcome the intrinsic disadvantages of supercaps, an overall power management solution is proposed in this thesis.

A reconfigurable switched-capacitor DC-DC converter is proposed to convert the unstable supercap's voltage (3.5V∼0.5V) to a stable 1V output voltage efficiently to power the subsequent circuits. With the help of the 6 conversion ratios (3 step-ups, 3 step-downs), voltage protection techniques, and low power designs, the converter can extract 98% of the stored energy from the supercap, and increase initial energy by 96%.

Another switched-inductor buck & boost converter is designed to harvest the ambient RF energy to charge the supercap quickly. Because of the variation of the reader distance and incident wave angle, the input power level also has large fluctuation (5μW∼5mW). The harvester handles this large power range by a power estimator enhanced MPPT controller with an adaptive integration capacitor array. Also, the contradiction between low power and high tracking speed is improved by adaptive MPPT frequency.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 IoT and Energy Harvesting

The term Internet of Things (IoT) has recently become popular to emphasize the vision of a global infrastructure of networked physical objects. Although there are many ways to describe an IoT, we can define it as a worldwide network of uniquely addressable interconnected objects, based on standard communication protocols [4]. With the idea of everything being connected, new applications can be envisioned in all areas, such as health monitoring (implantable medical electronics), smart homes, logistics, industrial manufacturing, active RFID tags and many more [3, 5, 6]. One vital characteristic of these applications in common is that, they are all severely energy constrained, which places significant challenges

on the power components and efficient power management solutions. The typical power requirements of some current small IoT devices are shown in Fig. 1.1.

Figure 1.1: Typical power and lifetime requirements of small electronic products incorporating wireless sensor networks [3]

The need shared by most IoTs for long lifetimes and small form factors does not match up well with the power density of available battery technology. This could limit the use of IoTs due to the need for large batteries. Moreover, the devices may be deployed in large numbers or in locations that are hard to reach, making battery replacement extremely difficult [7]. Energy harvesting is a promising solution. Different environmental energy sources, such as thermal, solar, vibration and RF, can be harvested to charge an energy storage device – battery or supercapacitor (supercap) – to prolong the IoT devices lifetime and even make them autonomous [1]. Solar panel, piezoresistor or RF rectifier are usually used to convert the aforementioned energy sources to electric energy.

One big challenge of energy harvesting is the severe fluctuation of the ambient

energy. Table 1.1 shows that the harvested energy could have wide range of variation depending on the conditions (indoor/outdoor, vibration strength, etc) [1]. This variation brings difficulties to the energy harvesters design.

Table 1.1: Performance of energy harvesters under different conditions [1]

Energy Harvester	**Power Densities**	
	Indoor conditions	Outdoor Conditions
Solar panel	$100\mu W/cm^2$	$10mW/cm^2$
Wind turbine generator	$35\mu W/cm^2$	$3.5mW/cm^2$
Thermalelectric generator	$100\mu W/cm^2$	$3.5mW/cm^2$
Electromagnetic generator	$4\mu W/cm^3$	$800\mu W/cm^3$

This thesis introduces an important application of IoT – RFID. The proposed RFID tag is intended to be attached on a blood bag for environmental temperature monitoring. RF energy harvesting is deployed in the RFID tag to achieve wireless charging.

1.2 Supercapacitor as Power Supply

For biomedical sensor applications specifically, the power source is one of the most difficult elements. Traditionally, biomedical sensors are battery operated, which

enables the circuit to be encapsulated, sealed and self-contained. However, the limited shelf-life, slow charge time and toxicity makes them unattractive for vast future deployment [8]. The recent development of supercapacitors (supercap) have created new possibilities to supply power for biomedical devices, as a replacement for batteries. Though supercapacitors have low energy density they are well suited for our application: quick charge, nearly infinite shelf-life and the lack of toxic heavy metals [9]. Comparison table between supercap and battery is shown in Table 1.2.

Table 1.2: Typical parameter numbers of supercap v.s. Lithium-ion battery

Function	**Supercap**	**Lithium-ion**
Charge time (second)	∼5	∼4000
Internal resistance (ESR)	∼0.01Ω	∼0.2Ω
Energy density (Wh/kg)	∼5	∼150
Instantaneous power density (W/kg)	∼10000	∼2000
Operating temperature	-40∼+65°C	0∼+40°C
Bio compatibility	No harsh chemicals	Harsh chemicals
Shelf life (hours)	∼1000000	∼500

1.3 Blood Temperature Requirements

Whole blood and red cells must always be stored at a temperature between +2°C and +6°C [2]. If not, its oxygen-carrying ability is greatly reduced. The following table summarizes the essential storage conditions for whole blood and packed red cells (red cell concentrates). This can be used as a guidance for the temperature monitoring scenario.

Table 1.3: Storage and transport conditions for whole blood and red cells [2]

Condition	**Temperature range**	**Storage time**
Transport of pre-processed blood	+20∼+24°C	Less than 6 hours
Storage of pre-processed or processed blood	+2∼+6°C	Approx. 35 days
Transport of processed blood	+2∼+10°C	Less than 24 hours

1.4 Organization

In this thesis, a RFID tag for blood temperature monitoring is introduced, with a supercap used as a replacement of batteries. An overall power management solution is proposed for the RFID tag. The rest of the thesis is organized as

follows:

- Chapter 2 introduces the RFID architecture
- Chapter 3 proposes a reconfigurable switched-capacitor DC-DC converter as a PMU for the discharge of the supercap
- Chapter 4 describes a switched-inductor buck-boost converter as a PMU for RF energy harvesting to charge the supercap
- Chapter 5 makes conclusions for this thesis

Chapter 2

RFID Tag for Blood Temperature Monitoring

Previous blood temperature monitoring systems use bar code as the temperature indicator. But this approach does not have real time monitoring and memory capability. In addition, a bar code requires close presence of the reader to read each blood bag. An RFID solution is therefore preferred, as it can provide much finer grained monitoring, with small size, low cost and flexibility, that can be extended to other wireless sensing applications, such as chemical exposure sensing, biological agent sensing, location information, vibration sensing, etc.

2.1 RFID Architecture

The RFID system is shown in Fig. 2.1. After first charged and reset, the RFID tag is attached to the blood bag unit, when donation location, date, donor ID, etc., are recorded. The environmental temperature is measured and stored in the tag's memory periodically (every 10 minutes). After one week or so, the stored information can be queried remotely and the tag can be recharged wirelessly by a reader. When the blood is distributed, the tag can be recycled and reset again for reuse.

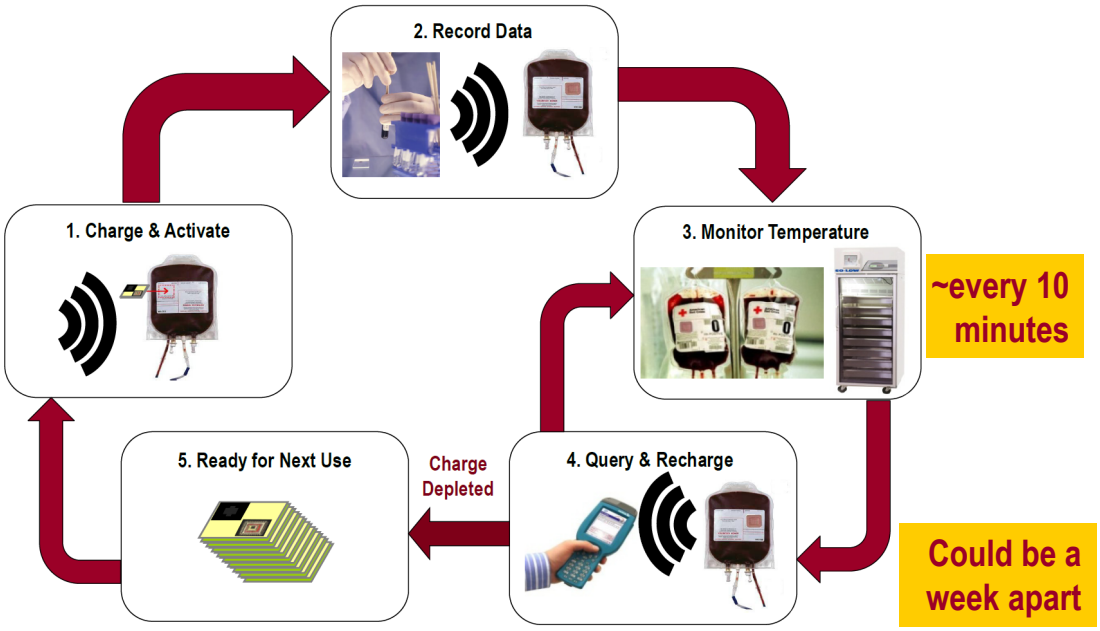


Figure 2.1: The RFID system concept

The proposed RFID tag architecture is shown in Fig. 2.2. The RFID tag

includes antenna, power management, communication, DSP, memory and sensor blocks. This thesis focuses on the pink parts – power management of the RFID tag, which includes an off-chip supercap and two PMUs: one for charging the supercap, and one for discharging.

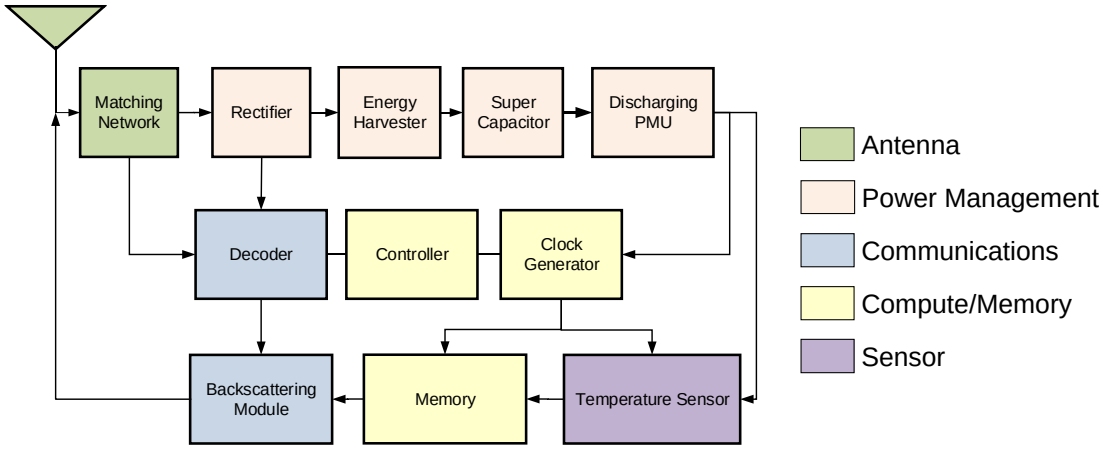


Figure 2.2: The proposed RFID tag architecture

2.2 RFID Energy Budget

The charge and discharge profile is shown in Fig. 2.3. The tag is designed to be charged quickly (∼2 min) when presenting a reader and last for about 1 week. This brings two major challenges for the power management circuit design: efficiently harvesting the ambient RF energy and use the stored energy with extremely low power.

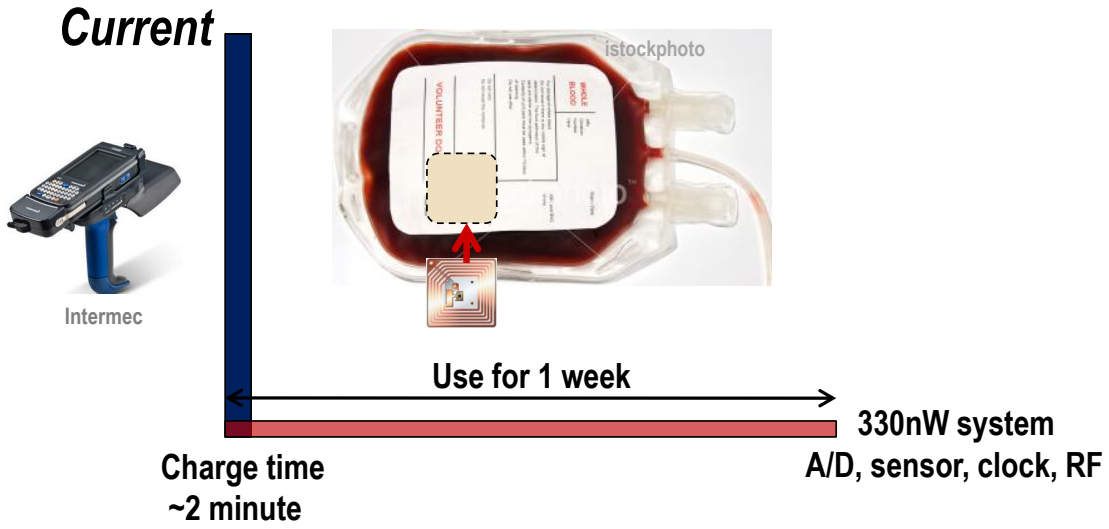


Figure 2.3: Charge and discharge profile of the RFID tag

To be able to continuously monitor the environment, the sensor node has to be duty cycled, meaning that, the tag has two modes: sleep mode and active mode. During the sleep mode, all the active circuits are turned off and the leakage current of the supercapacitor is about 300nA. When the sensor is activated at the end of each cycle, the temperature is measured and stored in the memory, with average active current equal to 3.3μA. Then the tag starts another sleep and active cycle - sleep for 10min, and active for 0.1s. This repeated pattern is shown in Fig. 2.4, where the overall average current would be 300.5nA and is dominated by the leakage current. The supercapacitor provides the 1V supply at an average current of 300.5nA for 7 days resulting in a total energy dissipation of 0.18J. If the supercap can be charged to 3.5V (details provided later), then the capacitance

needed is reduced to 0.03F. The final capacitor value will need to be slight larger to compensate for any inefficiency in the voltage conversion process.

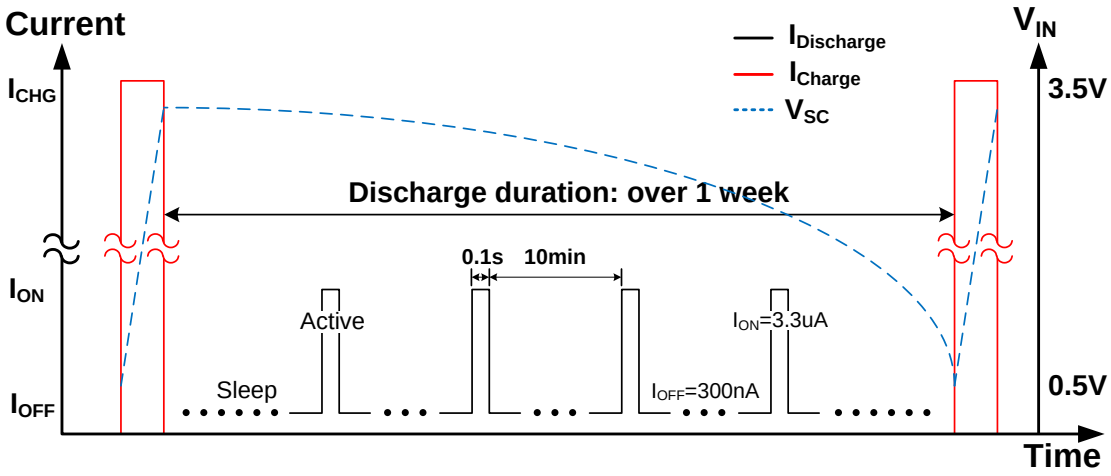


Figure 2.4: Overall charging, active and sleep timing diagram

Chapter 3

Supercap as Substitute of Batteries

3.1 Introduction

As described in the last chapter, a supercap is used for power supply as the substitute of a battery. Supercaps has many advantages over battery and suitable for low power biomedical applications. But unfortunately, supercaps do not maintain a constant output voltage and requires a power management unit (PMU). A supercap is first and foremost a capacitor, whose voltage V is proportional to the stored charge Q/C, such that the output voltage would decay as charge is pulled

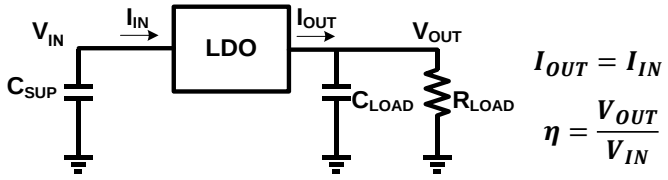
out. In addition, when the supercap voltage drops below the required lowest voltage (1V or lower for modern technologies), the circuit stops working, normally described as the functional end point (FEP), leaving a significant percentage of stored energy unused.

Linear regulators (LDO, Fig. 3.1a) are widely used as PMUs to provide a stable voltage supply. It solves the unstable voltage problem for a supercap, with an efficiency that is no larger than V_{OUT}/V_{IN}. The efficiency is very low at the beginning when V_{IN} is much larger than V_{OUT}, but becomes better when supercap voltage decreases closer to V_{OUT}. Nevertheless, significant amount of energy is still left on the storage device, since the LDO only works when V_{IN} is greater than V_{OUT}, resulting in wasted residual energy given at a minimum by $E = (CV_{OUT}^2)/2$. A potential solution for this problem was suggested in [10], were N supercaps can be stacked in series, then the residual voltage will be reduced by N times and the residual energy is reduced by a factor of N^2. Unfortunately, supercapacitors are physically large and stacking N such capacitors is highly cumbersome and makes this solution area inefficient.

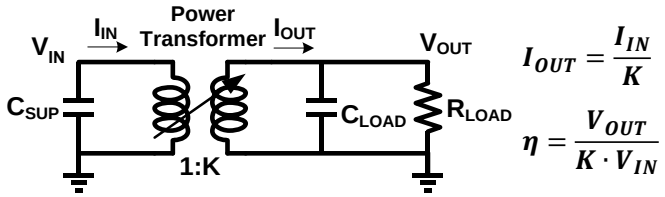
Switched-capacitor DC-DC converters are suitable for low power applications and are easily integrated on-chip. For example, paper [11] describes a reconfigurable switched-capacitor DC-DC converter with a peak efficiency of 81%. This

design attempts to solve the variable input voltage issue by using multiple step-down ratios. However, the maximum input and maximum output voltage is limited. Additionally, it has the FEP issue, i.e., a lot of energy is left unused before the system stops operating.

In this chapter, a multi-mode power transformer (MMPT, Fig. 3.1b) is proposed. The efficiency is improved by tuning the conversion ratio (K) according to the input voltage. The upper limit of the input voltage range for the MMPT is expanded by new voltage protection techniques, and the lower limit is expanded by applying both step-up and step-down conversion ratios [12].



(a)



(b)

Figure 3.1: (a) LDO block diagram; (b) MMPT block diagram

As is shown in Fig. 3.2, the proposed PMU is designed for supercaps, but can also be extended to batteries. The discharge curve for batteries is not as variable as for supercaps, but it also can drop significantly as the stored charge decreases. Moreover, modern technologies typically have a rated supply voltage of sub-1V, while lithium-ion batteries' output voltage ranges from 2.8 to 4.2V [13], making the integration of direct DC-DC converters difficult for digital dominant modern technologies. The voltage protection technique introduced by this chapter solves this problem by increasing the rated voltage of the 65nm process from 2.5V to 3.5V. Additionally, because of the wide-range input voltage, this PMU can potentially also be used for board-mounted point-of-load applications [14].

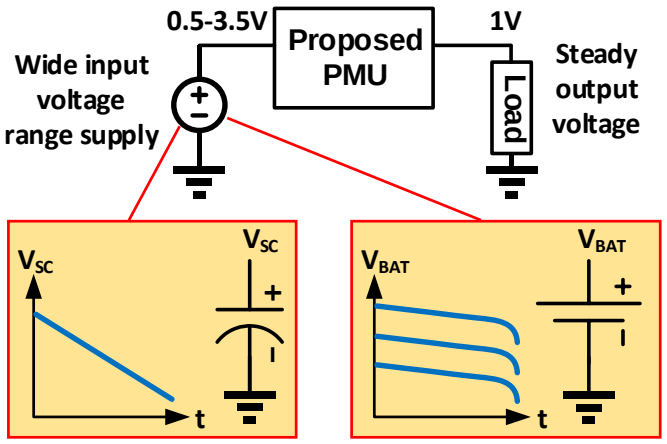


Figure 3.2: PMU to handle different type of supply

3.2 Efficiency Requirements

As described above, the MMPT is designed for a supercap powered RFID tag. Our goal for the MMPT described in this chapter is to have a higher efficiency and leave less residual energy in comparison to an LDO based design. We attempt to make this comparison by analytically considering the active time for the two designs. As shown in Fig. 3.3, the LDO will discharge the supercap linearly, since $I_{IN} = I_{OUT}$. For simplicity we can assume that the FEP for an LDO is V_{OUT} (1V in this case, but actually FEP is at least one overdrive voltage higher than V_{OUT}), the maximum active usage time for the LDO is T_{LDO} given by (3.1), where C_{SUP} is the supercap capacitance, V_{SC0} is the supercap initial voltage, I_Q is the average quiescent current, V_{OUT} and I_{OUT} are the output load voltage and current.

$$T_{LDO} = \frac{C_{SUP}\left(V_{SC0} - V_{OUT}\right)}{I_Q + I_{OUT}} \tag{3.1}$$

Calculating the total time for MMPT is a little more complex, since it has multiple ratios. If we assume the average efficiency of the MMPT is $\overline{\eta}$, the discharging time can be calculated by dividing the total energy with the output power (3.2).

$$T_{MMPT} = \frac{\overline{\eta} C_{SUP} V_{SC0}^2}{2 V_{OUT} I_{OUT}} \tag{3.2}$$

Further, let us assume that at a minimum average efficiency $\overline{\eta}_{min}$, the total duration for the MMPT design falls to the same value as the LDO design, and its

value can be derived as shown in equation (3.3).

$$\overline{\eta}_{min} = \frac{2V_{OUT}\left(V_{SC0} - V_{OUT}\right)}{V_{SC0}^2} \tag{3.3}$$

For any $\overline{\eta} > \overline{\eta}_{min}$, $T_{MMPT} > T_{LDO}$. In this design, $V_{OUT} = 1V$ and $V_{SC0} = 3.5V$, so $\overline{\eta}_{min} = 41\%$. This provides us a lower bound for the converter efficiency that we are trying to design, i.e., if the PMU efficiency is better than 41% then we have an advantage. We show the improved active time for the proposed design in Fig. 3.3, where we nearly double it.

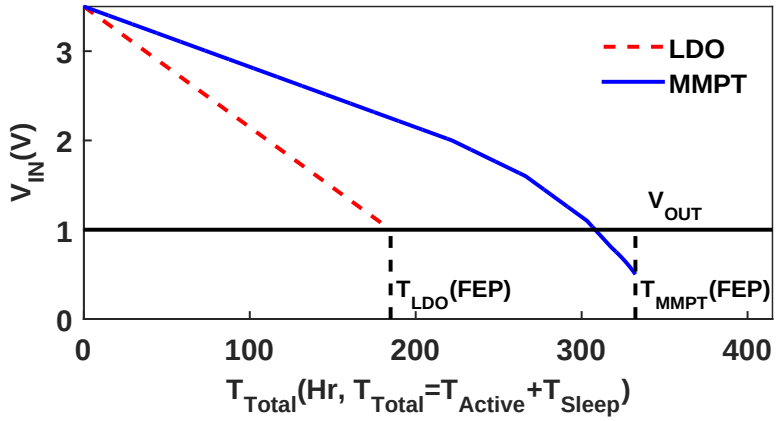


Figure 3.3: Supercap voltage discharge profile using LDO or MMPT

Another mechanism to understand the improvement is to visually see the distribution of useful energy, series loss and residual energy (also lost) as shown in Fig. 3.4. As can be seen, the series loss energy for the LDO design is 51% while that for the MMPT design is only 24%. Additionally, the residual (lost) energy for the MPPT design is about 1/10th the value for the LDO design due to the

lower FEP voltage. This is the reason that the value of T_{MPPT} is nearly twice that of T_{LDO}.

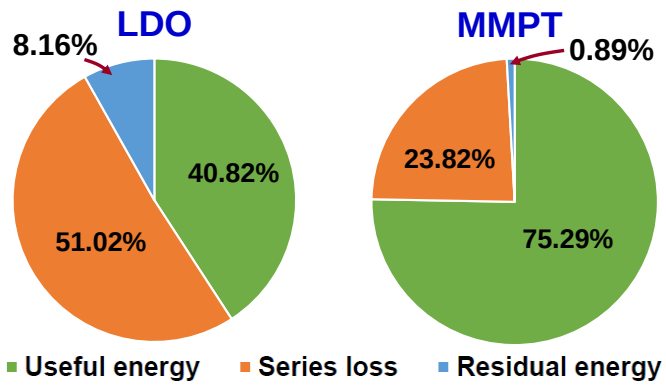


Figure 3.4: Energy usage comparison of LDO & MMPT

3.3 MMPT System Architecture

3.3.1 Basic DC-DC Converter Module

In theory, a converter with just two capacitors can generate more than six conversion ratios (three step-down: 1/2, 2/3, 1; three step-up: 3/2, 2, 3), by connecting the two capacitors in series or in parallel in the two phases [15]. So the starting basis for our converter module starts with this basic topology: 2 capacitors and 11 switches as shown in Fig. 3.5. However, this simple topology has some issues when used as is.

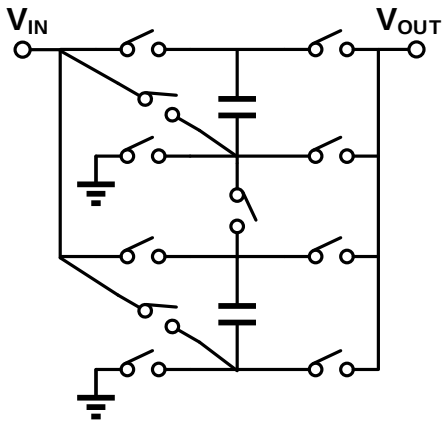


Figure 3.5: Basic multi-mode switched-capacitor converter module

3.3.2 Converter Core

The first problem that arises in the design of Fig. 3.5 is that the input voltage can be as high as 3.5V. To tolerate this high voltage, a single transistor is not sufficient even for I/O devices. One way to solve this problem is by stacking transistors (as in [13, 16]): by stacking one I/O 2.5V transistor and one core 1V transistor, and driving them separately, the branch can sustain a voltage as high as 3.5V. But if every switch is implemented by stacked (cascoded) transistors, the efficiency will drop significantly. Additionally, they are redundant when the input is low. A similar tradeoff also occurs for the choice between I/O devices and core devices: we want to use core devices for higher efficiency but we also want to use I/O devices for thier capability of handling higher input voltages.

In this chapter we resolve these conflicting issues by using separate converters for the different voltage ranges. Specifically, Instead of using a single converter as shown in Fig. 3.5, we separate the design into three converters that operate in the different ranges. When the input is larger than 2.5V, voltage protection is required, so the first converter (Conv1) is a buck converter with a conversion ratio of 1/2 and with voltage protection technique (details provided in later sections). The second converter (Conv2) works when input is in the range of 1V to 2.5V with a conversion ratio of 2/3 and 1, and it is implemented with I/O devices. For input voltages that are below 1V, a boost converter is used (Conv3). Conv3 is implemented with core devices and can be reconfigured to conversion ratios of 3/2, 2 and 3. Fig. 3.6 shows the converter core that combines the three converters and their operating modes.

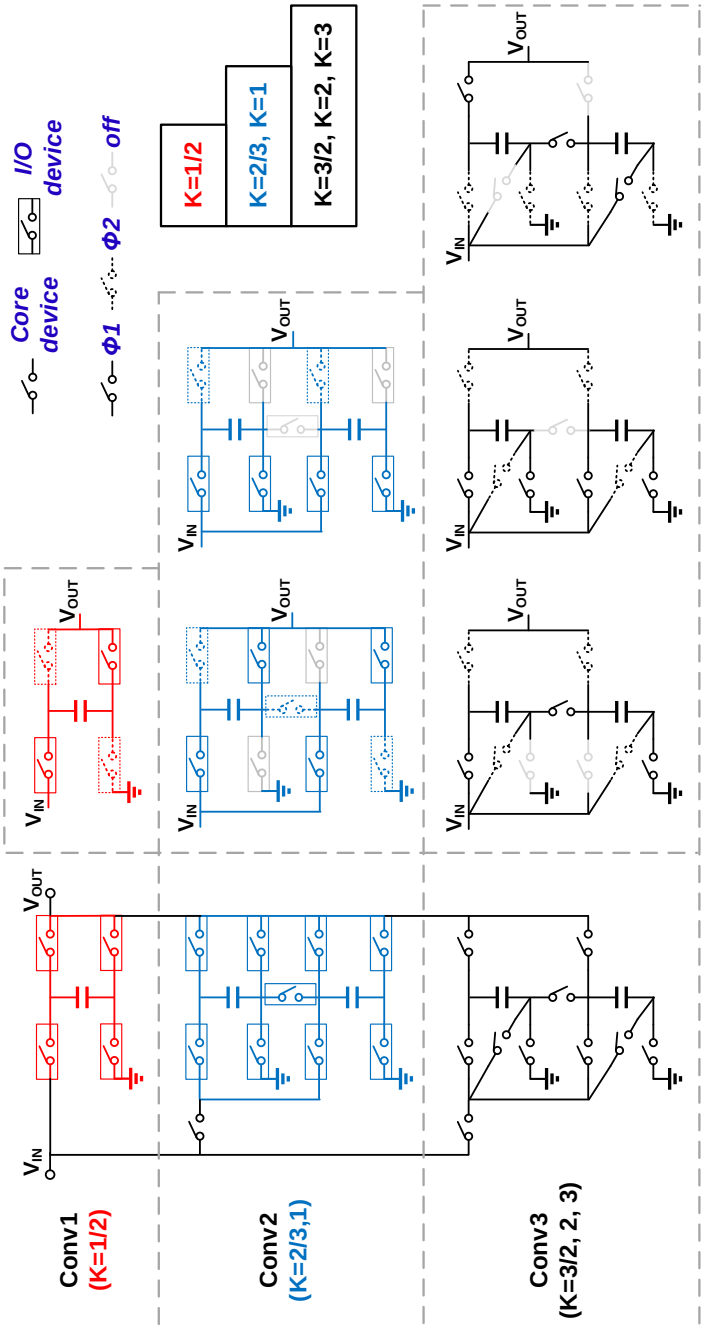


Figure 3.6: Multi-mode switched-capacitor power transformer modes (Conv1: buck converter w/ voltage protection; Conv2: buck converter w/o voltage protection; Conv3: boost converter)

The supercapacitor will be charged up to 3.5V and used as a power supply. During the process of normal usage, the supercap will discharge and the three converters described above will be turned on one by one depending on the voltage level. Fig. 3.7 shows this discharge curve and operating regions for the different converters.

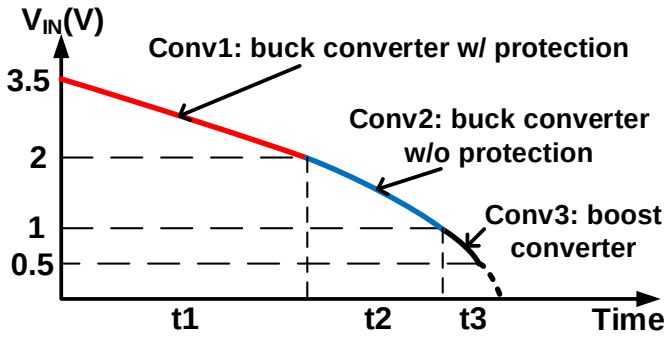


Figure 3.7: Supercap discharge voltage & converter operating regions

3.3.3 Overall System Architecture

A block diagram for the overall system is shown in Fig. 3.8. A voltage detector detects the input voltage range and decides to turn on the appropriate converter with the correct ratio. A V_{IN}/V_{DD} selector is used to isolate the lower voltage converter cores from the high input voltage, and also select the right input to feed to appropriate converter (additional details are provided in later sections).

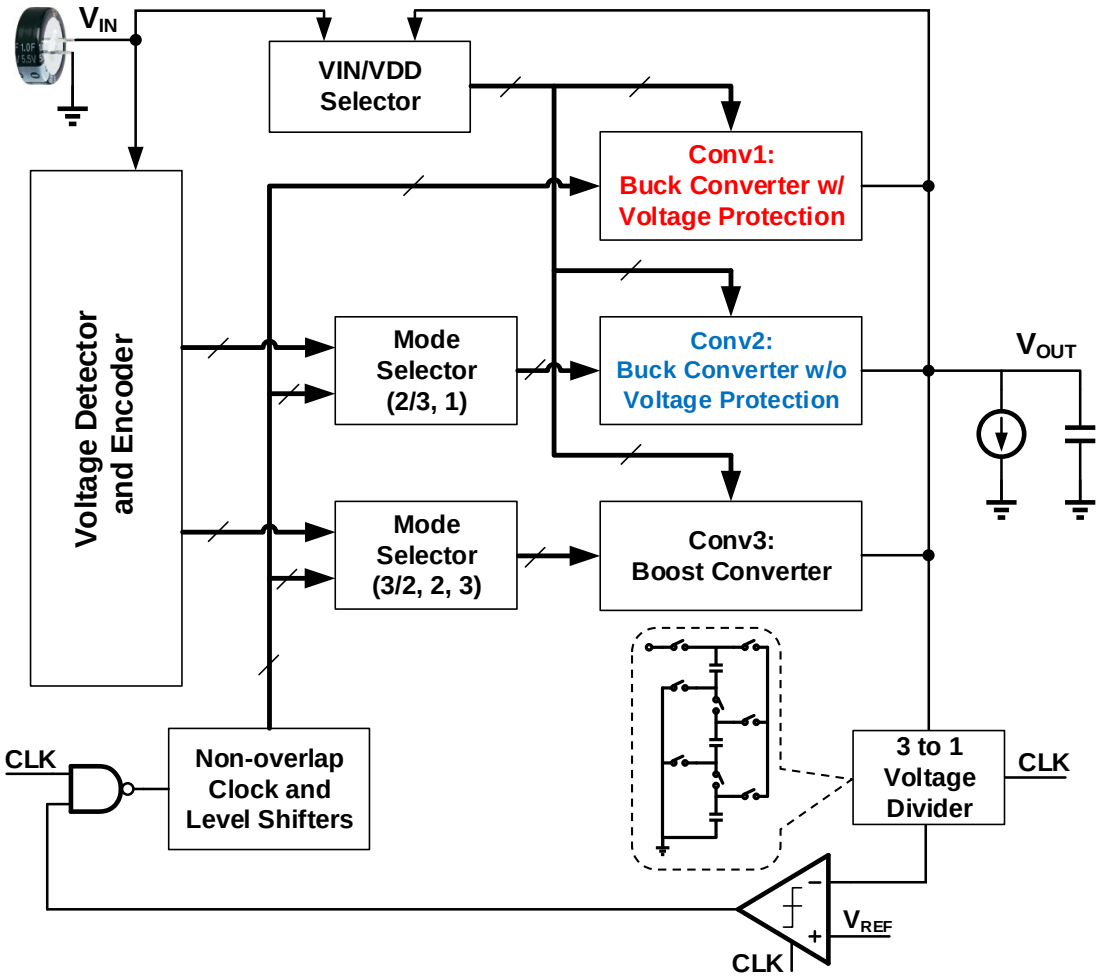


Figure 3.8: Overall system block diagram

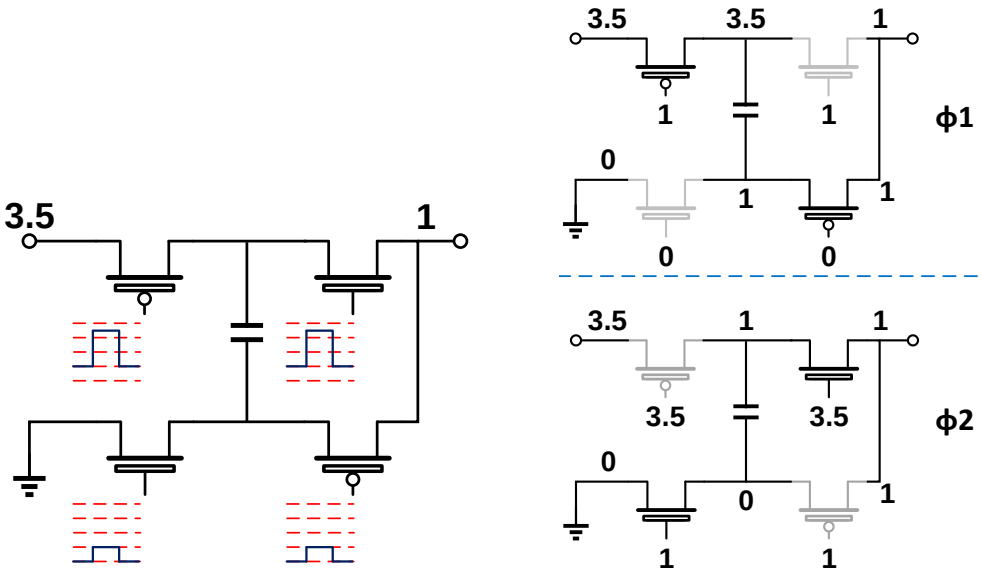
Since the switched-capacitor converter core can only provide discrete conversion ratios, the converter output requires additional voltage regulation to provide a constant 1V output. Here a frequency modulation method is used: applying a comparator and a reference voltage, the converter is turned on and off depending

on the difference of V_{REF} and a fraction (1/3) of V_{OUT}, and thus effectively the frequency of the input clock is modulated and V_{OUT} is clamped to $3 \times V_{REF}$. Instead of using resistor ladder, a switched-capacitor voltage divider is used to improve power and area efficiency. As the modulated clock signal is toggled between 0V and 1V, level shifters are required to correctly drive the higher voltage domain converters (1∼2.5V, 2.5∼3.5V).

3.4 Voltage Protection

3.4.1 Voltage Protection of 1/2 Buck Converter

A buck converter with a conversion ratio of 1/2 is easy to implement as in [15]. Since this converter works at the beginning of a fully charged supercap (3.5V), it must sustain the highest input voltage. The conventional solution is to stack or cascode two or more transistors and drive them separately. However, a more thorough analysis suggests that just one I/O transistor for each switch is adequate. If the transistors (switches) are driven by the clock signals shown in Fig. 3.9a, none of them will see the full 3.5V across any junction in either clock phase (Fig. 3.9b), even though the input voltage may exceed the transistor's rated voltage.



(a) Switch driving signal for Conv1

(b) Voltage level for each node decomposed in two phases

Figure 3.9: Voltage protection for Conv1 (buck converter K=1/2)

3.4.2 V_{IN}/V_{DD} Selector

All three converters have a separate V_{DD}s (used to set the PMOS body or for the local drivers' supply) and separate V_{IN}s. However, they are in different voltage domains. This causes some difficulty when we attempt to combine the charge from the three converters. In particular:

- V_{IN} can be larger than 2.5V (the breakdown voltage of the I/O transistors), so it cannot be fed directly to the converters;

- Either V_{IN} or V_{OUT} can be larger. The larger one of the two should be selected to drive the switch gate voltage as its V_{DD};

- Even when a converter is off, the V_{DD} still needs to be provided so that we can ensure that the switches are completely off.

We can solve all three issues by having a V_{IN}/V_{DD} selector in between the different voltage domains, as shown in Fig. 3.10. The selector is basically two PMOS devices connected together at the drain node.

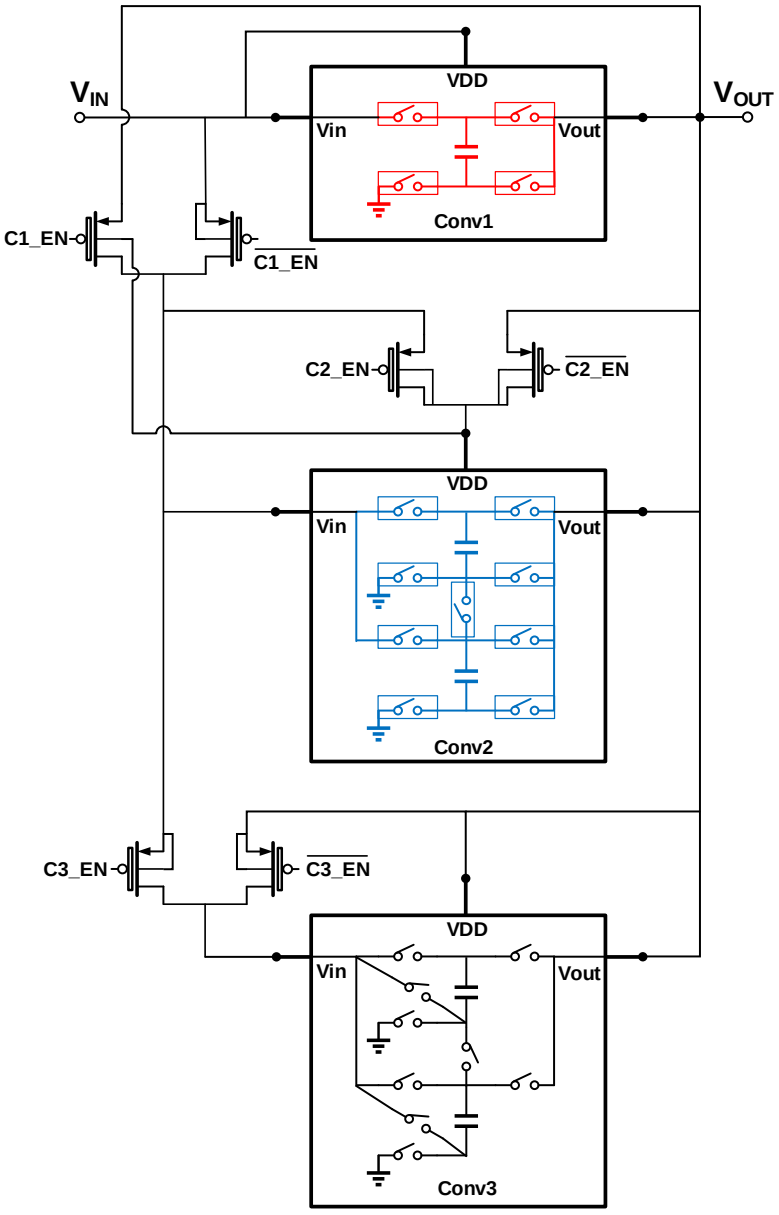


Figure 3.10: V_{IN}/V_{DD} selectors

The appropriate signal can be selected via a digital control signal. The resulting V_{DD} and V_{IN} voltages for the different regions are shown in Fig. 3.11. Note

that the body of the PMOS device should always be tied to the highest voltage, so some are connected to drain, some to the source, while others may be connected to appropriate control nodes. Likewise the digital control signals may need to be level shifted (next section) to generate the appropriate voltages for the different voltage domains.

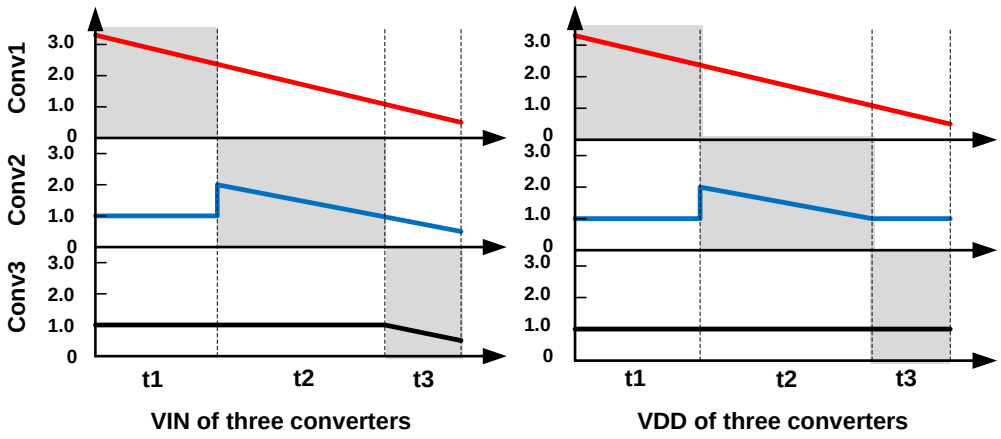


Figure 3.11: V_{IN} and V_{DD} for each converter in the different regions

3.4.3 Level Shifter

Due the multiple voltage domains used in this MMPT, the design of the level shifter is very critical. There are potentially two supplies, V_{IN} and V_{OUT}, that can be used in any one of converters. V_{OUT} is 1V and constant, so it is a good power supply for the boost converter with the core devices and other basic digital circuits, such as the mode selector and the oscillator. We call this LVDD. On the

other hand, V_{IN}, keeps changing and can at the beginning be higher than 2.5V and can also be lower than 1V as it approaches FEP. In general we will be using V_{IN} as our supply at the start, and anytime it is higher than V_{OUT}. We will call this HVDD. We now have to judiciously decide on the control and switch driving signals.

Since the original clock signal is in the range of 0 to V_{OUT} (or LVDD), we also need a clock signal in the range of 0 to V_{IN} (or HVDD), and V_{OUT} to V_{IN} (or LVDD to HVDD), to drive the two buck converters. Similarly, the original digital signals (mode selection signal, enable signal, reset signal, etc) are also generated in the range of 0 to LVDD, so solutions are required to bring these signals to the higher voltage ranges. The clock signals toggle regularly, while digital signals changes sporadically. This characteristic enforces different level shifter design for clocks and digital signals.

The level shifter for the clock signal is shown in Fig. 3.12. The original clock signal is AC coupled to a higher voltage domain (between LVDD and HVDD). Transistor M1 and M2 are used to avoid short circuit current since the voltage at node A only has a swing of 1V and node B is 2.5V. The resistor between node A and B is used for setting the DC operating point. The two switches inserted are used to prevent short circuit current when the clock signal is disabled. The higher path (HCLK_out) and the lower path (LCLK_out) are implemented with different

type of transistors and have different voltage domains. This, unfortunately, means that the logic delays for the two paths may not match and driving signal can potentially overlap. We can solve this problem by: a) increasing the delay of the lower path to compensate for any delay mismatch, b) increasing the dead time of the non-overlapping clock generator so as to tolerate higher variation. The level shifter proposed here, has some limitations in that it cannot operate at very slow clock speeds, as resistor provides a path to discharge the coupling capacitor and potentially causing a short circuit.

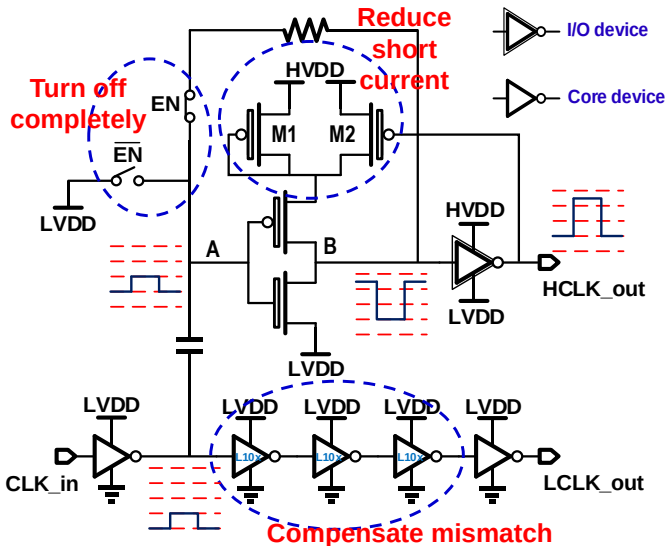
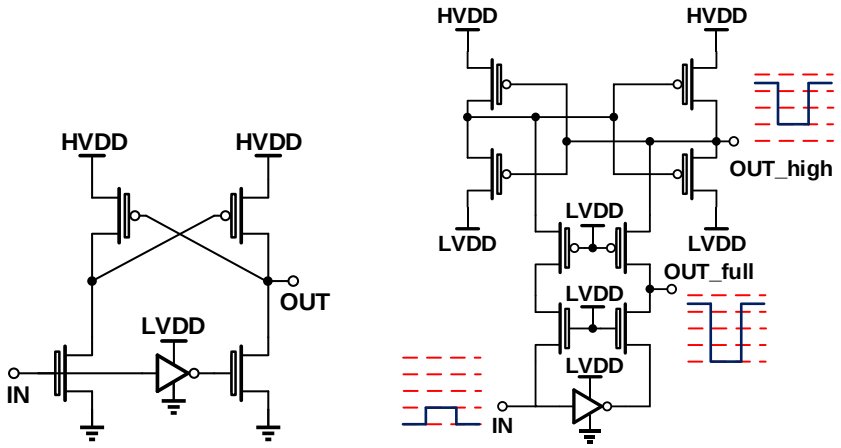


Figure 3.12: Clock level shifter circuit

The digital signal level shifter works for steady state conditions. A conventional digital level shifter is shown in Fig. 3.13a, but cannot tolerate voltages

above 2.5V. The proposed level shifter is a modified version of [17], and is shown in Fig. 3.13b. It can provide both full scale output (between 0 and HVDD, OUT_full) and high voltage domain output (between LVDD and HVDD, OUT_high).



(a) Conventional level shifter

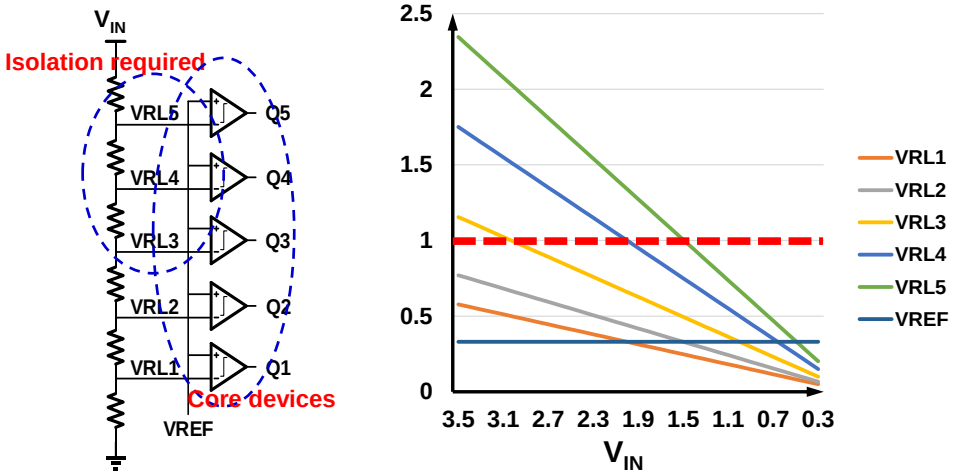
(b) Over-voltage level shifter

Figure 3.13: Digital level shifter circuit

3.4.4 Mode Selector

The mode selector in this design is implemented using a flash ADC as is shown in Fig. 3.14a. This architecture is straightforward and easy to design. By adjusting the resistance value, the decision voltage points can be set. One thing that needs to be noticed is that all the comparators are in the low voltage domain and use core devices. When the input voltage decreases from high to low, the internal

node from VRL1 to VRL5 also drops, as shown in Fig. 3.14b. Three of them (VRL3/4/5) exceed the 1V limit, meaning that the three comparators need to be protected from the high voltage.



(a) (b)

Figure 3.14: (a) Input voltage range detector (flash ADC); (b) Internal node voltages as V_{IN} decreases

3.4.5 Comparators

As described above, three of the comparators need to be protected from the high input voltage. Notably, the voltage stress should not exceed 2.5V, so a single I/O transistor will solve the problem. As shown in Fig. 3.15a, the negative input is isolated from VRL3/4/5 by an I/O transistor. Only when the previous comparator

is triggered, the current comparator can be turned on and connected to a fraction of input. This trigger technique not only protects the comparator from the high voltage stress, but also saves power, with the help of the power saving gate and one additional transistor at the output that is used to pull the output to ground when it is turned off. To further save power, the comparator is implemented as a clocked strong-arm comparator that only consumes dynamic power (Fig. 3.15b [18]).

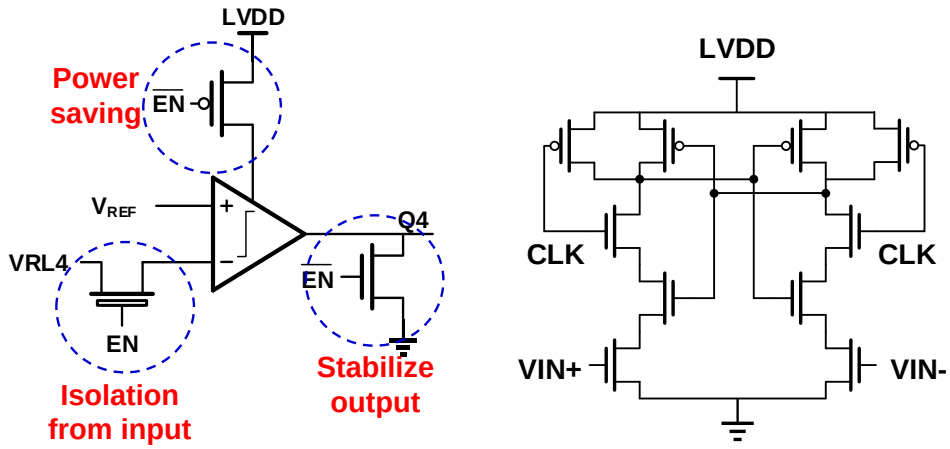


Figure 3.15: (a) Voltage protection and power saving for comparator; (b) Strong-arm comparator

3.5 Efficiency Analysis

The proposed DC-DC converter is designed for RFID applications, where the average load current is as low as $3.3\mu A$. The efficiency becomes very important to ensure longer operating time for the RFID tag. The different loss mechanisms and efficiency limitations will be analyzed in this section. The loss mechanisms in a switched-capacitor DC-DC converter is mainly from four sources: a) conduction loss; b) switch gate loss; c) bottom/top plate loss; and d) control overhead.

3.5.1 Conduction Loss

Conduction loss is the most significant loss mechanism. It is caused by the energy loss that occurs during the charge redistribution between capacitors. The power efficiency (considering no other losses) of a switched-capacitor DC-DC converter is given by (3.4).

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}}{V_{MAX}} = \frac{V_{OUT}}{K \cdot V_{IN}} \tag{3.4}$$

here K is the conversion ratio. So as V_{IN} decreases, the efficiency increases for a fixed conversion ratio, as depicted in Fig. 3.16. We can choose the transition points according to this figure and make sure that the converter always operates at the highest efficiency.

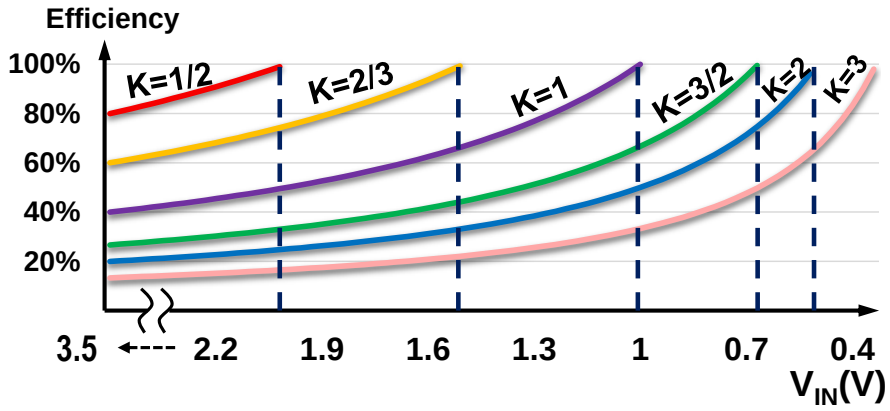


Figure 3.16: Switched-capacitor DC-DC converter efficiency for the different conversion ratios (only conduction loss)

3.5.2 Switching Loss

Switching loss is caused by the clock signal periodically charging and discharging the parasitic capacitors associated with the switches. These capacitors include the gate capacitor of switches, drivers and non-overlap clock generator. The switching loss is proportional to switching frequency and total capacitance that is switched during each clock period.

3.5.3 Bottom/Top Plate Loss

All the MIM-caps have bottom plate and top plate parasitics. In 65nm CMOS technology used for this design as an example, the top plate is negligibly small

and bottom plate is about 1% of the MIM-cap value. In [19], the impact of such bottom/top plate parasitic is derived in detail. We will use these models directly to calculate their impact.

3.5.4 Control Overhead

All the control circuit such as resistor ladders, comparators, finite state machines, etc, would consume power as a quiescent current or leakage or other switching losses. Since this design is for a low power application (3.3μW), any leakage would be critical and the control circuits are preferred to be as simple as possible.

3.5.5 Efficiency Calculation

We will include all the losses listed above to calculate the expected efficiency based on the model. Let us take K=3/2 for example, the model circuit is shown in Fig. 3.17. This model includes the switching loss and control loss as a load resistance of $1/(C_{ctl3} + C_{sw3})f_{sw}$, connected to the output, and the bottom plate loss as a load resistor ($1.5\beta C_{bucket} f_{sw}$) connected to the input, where β is the bottom plate factor (1.3% in this case), C_{ctl3} is the effective parasitic capacitance of the control circuit, C_{sw3} is the total parasitic capacitance of switches/drivers/non-overlap clock generator, C_{bucket} is the bucket/flying capacitance and f_{sw} is the switching frequency. The subscript has a number of 3 meaning that this is the

control circuit or switching circuit of Conv3 - the boost converter with core devices. The R_{OUT} for this model is $1/2C_{bucket}f_{sw}$ at K=3/2.

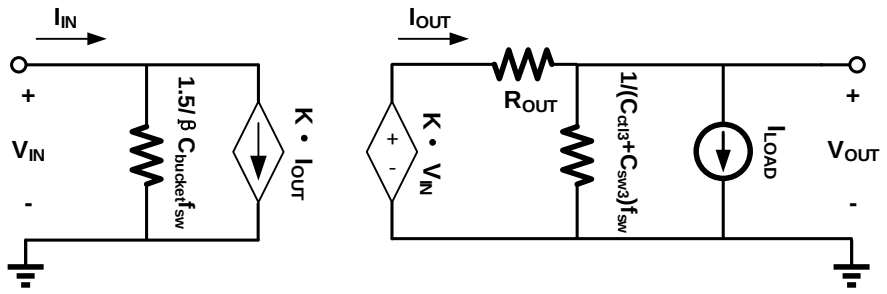


Figure 3.17: Model for efficiency calculation (K=3/2)

We can now calculate the I_{IN}, I_{OUT}, I_{LOAD} and substitute them with V_{IN} and V_{OUT}, and express efficiency η as function of V_{IN} and V_{OUT}.

$$I_{OUT} = \frac{KV_{IN} - V_{OUT}}{R_{OUT}} = \frac{3V_{IN}/2 - V_{OUT}}{1/2C_{buckert}f_{sw}} = (3V_{IN} - 2V_{OUT})\, C_{bucket}f_{sw} \tag{3.5}$$

Using KCL:

$$\begin{aligned} I_{LOAD} &= I_{OUT} - V_{OUT}\,(C_{ctl3} + C_{sw3})\, f_{sw} \\ &= \left[3V_{IN} - \left(2 + \frac{C_{ctl3} + C_{sw3}}{C_{bucket}}\right) V_{OUT}\right] C_{bucket}f_{sw} \end{aligned} \tag{3.6}$$

$$I_{IN} = \frac{2}{3}V_{IN}\beta C_{bucket}f_{sw} + KI_{OUT} = \left[\left(\frac{2}{3}\beta + 4.5\right) V_{IN} - 3V_{OUT}\right] C_{bucket}f_{sw} \tag{3.7}$$

The overall efficiency can now be expressed as:

$$\eta = \frac{V_{OUT}I_{LOAD}}{V_{IN}I_{IN}} = \frac{V_{OUT}\left[3V_{IN} - \left(2 + \frac{C_{ctl3}+C_{sw3}}{C_{bucket}}\right) V_{OUT}\right]}{V_{IN}\left[\left(\frac{2}{3}\beta + 4.5\right) V_{IN} - 3V_{OUT}\right]} \tag{3.8}$$

In comparison to equation (3.4), which only considers conduction losses, this efficiency equation is a lot more complex as many more non-ideal factors are considered. Substituting all the parameters in (3.8) with design values (Table 3.1), and then plotting and comparing (3.4) and (3.8) in Fig. 3.18, we can find out that after considering all the non-ideal factors, the efficiency is much lower. This is particularly true as V_{out} approaches V_{max} for each of the different converter topologies. Unlike high power applications (1∼1000mA, [20, 14, 21, 22]), where the efficiency can approach 90%, low power applications are hard to maintain high efficiency since any small leakage/overhead/parasitic has significant impact ([23, 24]).

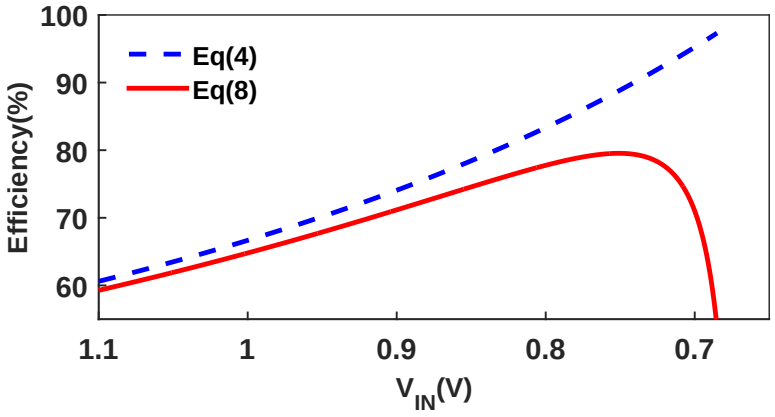


Figure 3.18: Efficiency comparison using (3.4) & (3.8)

Table 3.1: Design parameters for efficiency model (C_{bucket}: capacitance of bucket capacitor; $C_{ctl1/2/3}$: parasitic capacitance of control circuit for Conv1/2/3; $C_{sw1/2/3}$: parasitic capacitance of switches and driving circuit for Conv1/2/3; f_{sw}: switching frequency; β: ratio of bottom plate parasitic capacitance)

Parameter	**Value**	**Parameter**	**Value**
V_{IN}(V)	3.5∼0.5	V_{OUT}(V)	1.0
C_{bucket}(pF)	5.2	$C_{ctl1/2/3}$(fF)	70.4
$C_{sw1/2/3}$(fF)	46.3/204.9/56.8	f_{sw}(MHz)	2.0
β	1.3%	–	–

All the efficiency equations at the different conversion ratios are listed in Table 3.2. They will be plotted and compared with measurements in next section. What is noteworthy is that, there is an exponential factor in the efficiency equation for Conv1. The reason is that the leakage of the level shifter is exponential to V_{IN}, which is also the reason for its relatively lower efficiency.

Table 3.2: Efficiency model for all six modes

	K	Efficiency
Conv1	1/2	$\frac{V_{OUT}\left(2V_{IN}-\frac{\beta+4+C_{ctl1}}{C_{bucket}}V_{OUT}\right)}{V_{IN}\left[\left(1+\frac{C_{sw1}}{C_{bucket}}\right)V_{IN}-\left(2+\frac{C_{sw1}}{C_{bucket}}\right)V_{OUT}+\frac{6\times10^{-14}\exp(5.4V_{IN})}{f_{sw}C_{bucket}}\right]}$
Conv2	2/3	$\frac{V_{OUT}\left[3V_{IN}-\left(\frac{2}{3}\beta+4.5+\frac{C_{ctl2}}{C_{bucket}}\right)V_{OUT}\right]}{V_{IN}\left(2+\frac{C_{sw2}}{C_{bucket}}V_{IN}-3V_{OUT}\right)}$
	1	$\frac{V_{OUT}\left[2V_{IN}-\left(2+\frac{C_{ctl2}}{C_{bucket}}\right)V_{OUT}\right]}{V_{IN}\left[\left(2+\frac{C_{sw2}}{C_{bucket}}\right)V_{IN}-2V_{OUT}\right]}$
Conv3	3/2	$\frac{V_{OUT}\left[3V_{IN}-\left(2+\frac{C_{ctl3}+C_{sw3}}{C_{bucket}}\right)V_{OUT}\right]}{V_{IN}\left[\left(\frac{2}{3}\beta+4.5\right)V_{IN}-3V_{OUT}\right]}$
	2	$\frac{V_{OUT}\left[4V_{IN}-\left(2+\frac{C_{ctl3}+C_{sw3}}{C_{bucket}}\right)V_{OUT}\right]}{V_{IN}[(2\beta+8)V_{IN}-4V_{OUT}]}$
	3	$\frac{V_{OUT}\left[1.5V_{IN}-\left(0.5+\frac{C_{ctl3}+C_{sw3}}{C_{bucket}}\right)V_{OUT}\right]}{V_{IN}[(3\beta+4.5)V_{IN}-1.5V_{OUT}]}$

3.6 Measurement Results

The test setup is shown in Fig. 3.19. The on chip variable load resistor ranges from 150 to 1000KΩ. A dummy load resistor is placed in parallel with the MMPT load to measure the real load current. When an input voltage of 3.5V to 0.5V is applied to the MMPT, V_{OUT} is fixed to 1V. The measured efficiency is plotted in Fig. 3.20 (blue), together with the calculated model in Section IV (red). The

comparison shows that measured efficiency follows the model equations trend, but has lower values, especially for Conv1. The reason for this discrepancy is that there are still other effects that are not considered by the model. For example the leakage of the ESD, substrate loss, transient short circuit, etc.

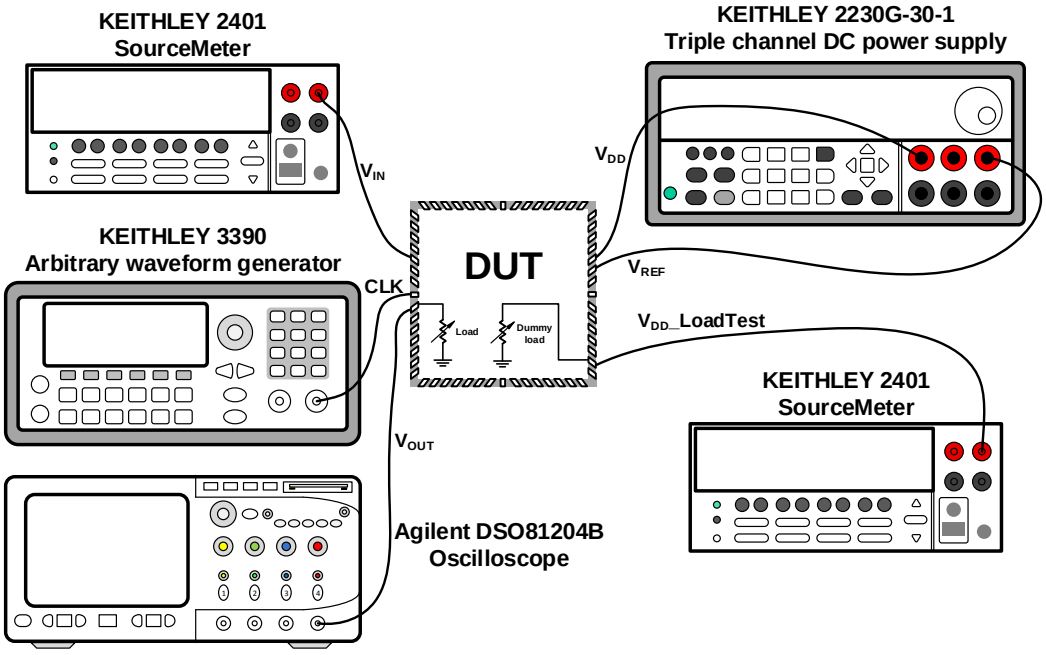


Figure 3.19: MMPT test setup

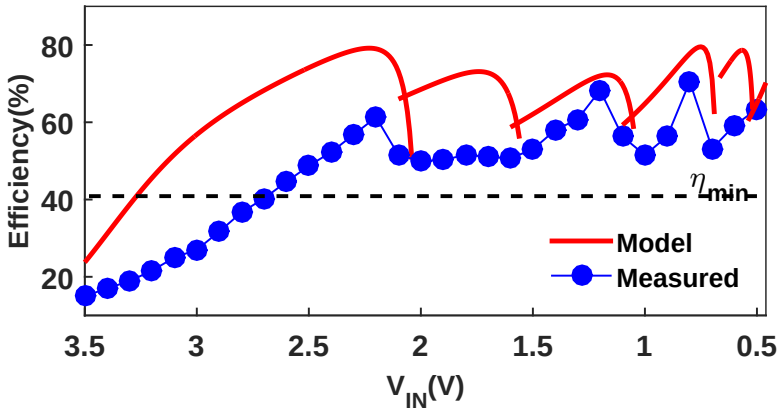


Figure 3.20: Measured efficiency vs V_{IN} for V_{IN} =3.5∼0.5V

In separate tests the level shifter in Fig. 3.13b has proven to be very leaky when the input voltage is high and causes the majority of the efficiency drop. This can be improved if a better level shifter is designed. A peak efficiency of 70.4% is measured at V_{IN}=0.8V. Fig. 3.21 shows the measured efficiency v.s. conversion ratio together with results from some other publications. It can be seen that, other switched-capacitor DC-DC converters are either buck or boost only. This chapter has an enlarged conversion ratio range that is more suitable for supercaps, where the input voltage variation can be large.

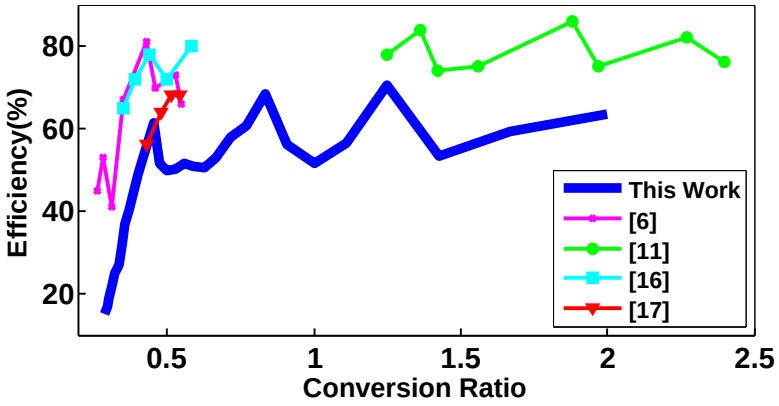
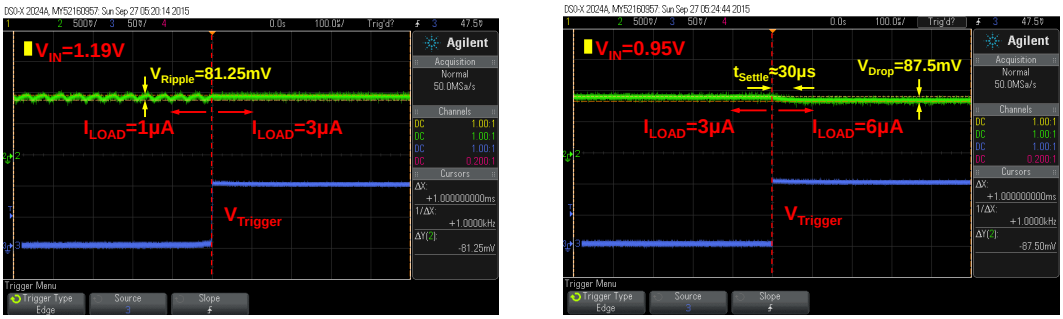


Figure 3.21: Measured efficiency vs conversion ratio

The transient response is shown in Fig. 3.22. The highest ripple voltage is 81.25mV, which happens when load current is low because of lower effective frequency. When load current increases from 3.3μA to 6μA, V_{OUT} drops by 87.5mV. The transient response time is about 30μs to an step change in the load.



(a) I_{LOAD} from 1μA to 3μA

(b) I_{LOAD} from 3μA to 6μA

Figure 3.22: Transient response of MMPT

As mentioned previously, it is significanlty more challenging to improve the

efficiency for low power applications. Fig. 3.23 shows the trend that, the higher the load current, the more efficient the design can be. The main reason is that higher load current allows more control overhead and results in more complicated and sophisticated control circuits. [20] in this figure has a much higher efficiency than the trend line. Reason is that it uses ferroelectric capacitors as the bucket capacitor, which has much less bottom plate parasitic than regular MIM-cap. Our work is about 12% above the trend line.

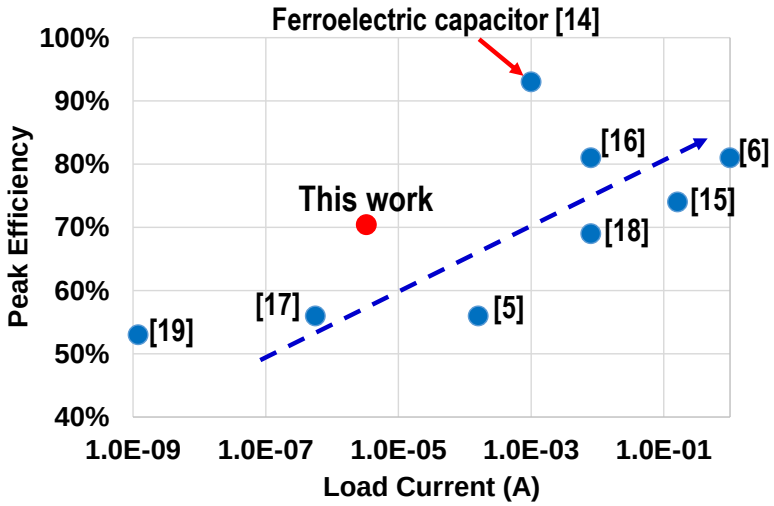


Figure 3.23: Efficiency comparison with other published designs

Table 3.3 compares this work with other published results. This works achieves the highest input voltage range with good efficiency, combining both up and down conversion and voltage protection techniques. The voltage protection techniques allow us to nearly double the energy stored on the supercapacitor. Fig. 3.24

depicts the input voltage range as an FOM under different load currents. The chip operates at 2MHz clock frequency and occupies an area of 0.48mm^2 (micrograph of the die is shown in Fig. 3.25, the size of tank capacitor is also indicated).

Table 3.3: Measurement result summary and comparison with prior art

Ref	Tech (nm)	Active Area (mm^2)	Switching Freq. (MHz)	Input Voltage (V)	Output Voltage (V)	Load Current	Peak Efficiency (%)	Step Up/Down
[10]	180	1.82	1.5	1.25∼2.5	1	0∼160μA	56	Down
[11]	32	0.38	∼400	2	0.4∼1.2	1A	81	Down
[14]	180	11.55	–	1.5∼12	1.5	0∼1A	92	Down
[20]	130	0.37	∼8.2	1.5	0.4∼1.1	20μA∼1mA	93	Down
[21]	90	0.25	50	1.2∼2	0.7	8mA	81	Down
[22]	45	0.16	30	1.8	0.8∼1	8mA	69	Down
[23]	130	0.26	2	2.5∼3.6	0.444	5nA∼560nA	56	Down
This Work	65	0.48	2.0	0.5∼3.5	1	3.3μA	70.4	Up&Down

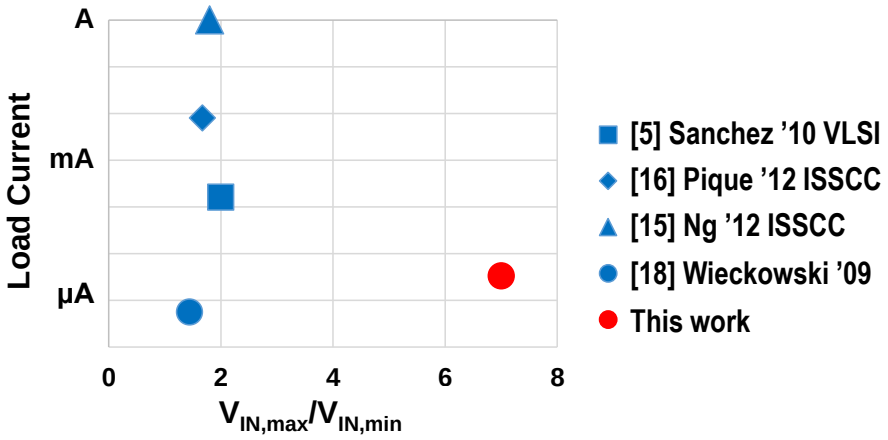


Figure 3.24: Input voltage range comparison with other published designs

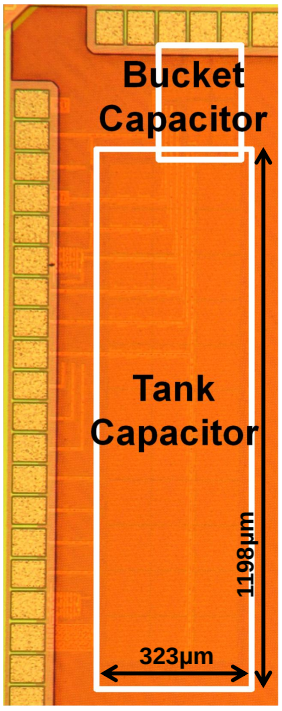


Figure 3.25: Die micrograph

3.7 Conclusions

This chapter proposes a wide input range, fixed output voltage multi-mode power transformer based on switched-capacitor DC-DC converters, for low power, supercapacitor powered RFID applications. With voltage protection technique, the converter increases the highest tolerable input voltage from 2.5V to 3.5V, raising the storage energy by 96%. This design also combines three converters, obtaining six conversion ratios (3 step-ups and 3 step-downs). The functional end point (FEP) is reduced from from 1V to 0.5V reducing the amount of energy that is left on supercap unused. As a result, it nearly doubles the usage time, by increasing the useful energy from 40.8% to 75.3%. The chip fabricated in TSMC's 65nm GP CMOS technology, operates at 2.0MHz and occupies an area of 0.48mm^2. The new design can extract 98% of the stored energy from an 80mF supercap, which lasts for 8.5 days between charging with the measured efficiency and an average load current of 300.5nA (3.3μA for active mode and 300nA for sleep mode). Although the proposed MMPT is designed specifically for RFIDs and supercapacitors, the converter is also suitable for other energy starved applications and other power sources. Because the output voltage of some battery power sources also changes significantly, this converter can be used to stabilize the output voltage. Additionally, for batteries that have a voltage that is higher than what can be tolerated by

modern CMOS technology, the proposed voltage protection techniques are also good candidate to solve integration difficulty of the PMU and DSP/baseband circuits.

Chapter 4

RF Energy Harvesting for Supercapacitor

4.1 Introduction

IoT has wide range of applications, as mentioned in previous chapters. However, the devices may be deployed in large numbers or in locations that are hard to reach, making battery replacement extremely difficult [7]. Different environmental energy sources, such as thermal, solar, vibration and RF, can be harvested to charge an energy storage device – battery or supercapacitor (supercap) – to prolong the IoT devices lifetime and even make them autonomous [1]. Solar panel, piezoresistor or RF rectifier are usually used to convert the aforementioned energy

sources to electric energy a DC voltage. No matter what the energy source and what the harvester type are, a subsequent PMU (or harvester) is indispensable to charge the storage device efficiently. This chapter proposes an inductive buck & boost DC-DC converter for RF rectifiers to harvest RF energy and charge a supercap for RFID applications.

The ambient energy intensity can have a very wide variety range (μW$\sim$W), due to the variation of irradiance level, vibration strength, incident angle, etc. To achieve the maximum output power, the converter's control parameters (duty cycle, switching frequency, pulse width, etc) has to be adjusted to the highest overall efficiency point along with the fluctuation of the ambient energy. This point is called maximum power point (MPP) and the algorithm to track MPP is known as maximum power point tracking (MPPT), which is conventionally implemented with a voltage meter, a current meter, ADC and DSP [25], very power hungry. Reference [26] introduces a teqnique called Q-modulation, that puts a switch in paralell with the load resistance to modulate the load and obtain a higher overall efficiency. However, this approach has extra loss in the paralell switch, which is not preferred. One widely used integrated MPPT algorithm is fractional open circuit voltage method (FOCV), which is simple to implement and suitable for low power applications [27, 28, 29]. But the assumption of MPP occurs where the output voltage is a fraction (usually 1/2) of open circuit voltage only holds true

if the harvester is a linear system. For example, a diode based RF wave rectifier and photovoltaic harvester are not linear [30]. The perturb and observe (P&O) method or 'hill climbing', is more promising for an energy harvesting system with nonlinear impedance sources [31]. Reference [30] proposed a low power time-based power monitor with a P&O algorithm. However, the time-based approximation is only valid for high conversion ratios. Reference [32] achieved a more precise P&O MPPT implementation with pulse integration (PI-MPPT). This approach is able to track well over a small power range (∼20x) as it relies on a single capacitor to store the MPP information, which can either be made sensitive or is easily saturated. Reference [33] combines FOCV and P&O to achieve a higher power range, which unfortunately complicates the system design. This chapter proposes a low power, adaptive current-integration (CI-MPPT) implementation that expands the MPPT range to ∼1000x.

The proposed RFID tag [12] is intended to be attached on a blood bag for temperature monitoring, during transportation or storage. When an RFID reader approaches the tag, the RF signal is transmitted to the tag and rectified to a low DC voltage. The proposed harvester up converts this small voltage to a higher value to charge up the supercap. The goal is to charge an 80mF supercap to 3.5V within 2 minutes, so the harvester needs to handle a maximum input power level of at least ∼5mW. And to ensure operation in all scenarios the harvester also

should be able to extract extreme lower as well (e.g. $\sim 5\mu$W).

Other than the high power range requirement, the supercap is designed to be charged to a higher voltage (3.5V) to increase the stored energy. Same as the reason described in last chapter, voltage protection techniques are introduced to extend the output voltage of the DC-DC converter to 3.5V. This chapter focuses on the DC-DC converter (or harvester) within the RFID tag.

4.2 Converter System Architecture

As is shown in Fig. 4.1, when an RFID reader approaches the RFID tag, an RF (AC) signal is transmitted to the tag through the antenna and rectified to a DC voltage to charge to a supercap. Due to the variation of reader distance and angle, the incident power fluctuates from 5μW to 5mW. Fig. 2.2 shows the RFID tag architecture, in which the proposed charging energy harvester (DC-DC converter) is in between of the AC-DC rectifier and the storage device (supercap). The rectified DC voltage, ranging from 0.7V to 1.2V, is fed to the converter, and up-converted to 3.5V and charged to the supercap. Then, once the supercap is fully charged, the converter will be disconnected from it and ready to supply the other circuitry of the RFID tag (temperature sensor, memory, DSP, etc).

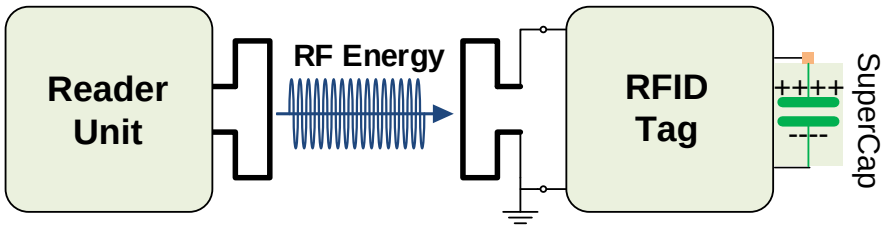


Figure 4.1: RFID system concept

4.2.1 Power Train

The block diagram of the proposed harvester is shown in Fig. 4.2. The power train includes both a buck and a boost converter, with an off-chip 200μH inductor. The buck converter switches, on the left side of the inductor, are implemented by core devices. While the boost converter switches, on the right side, are both stacked by one core device and one I/O device, to handle the high stress when charging the output node (further reason will be discussed in later sections). Previous designs have suggested that a single boost converter is enough for charging a supercap [34]. However, as is shown in Fig. 4.3, when output voltage is 0V initially and is charged by a single boost converter, the voltage across the inductor is kept same for the two phases. Then the current of the inductor will keep increasing, until the power switches are saturated, regardless of the PWM signal. The converter then becomes uncontrollable and may operate at the point that is far away from the target MPP. A voltage detector at the output decide either buck or boost

converter should be used during the charging process.

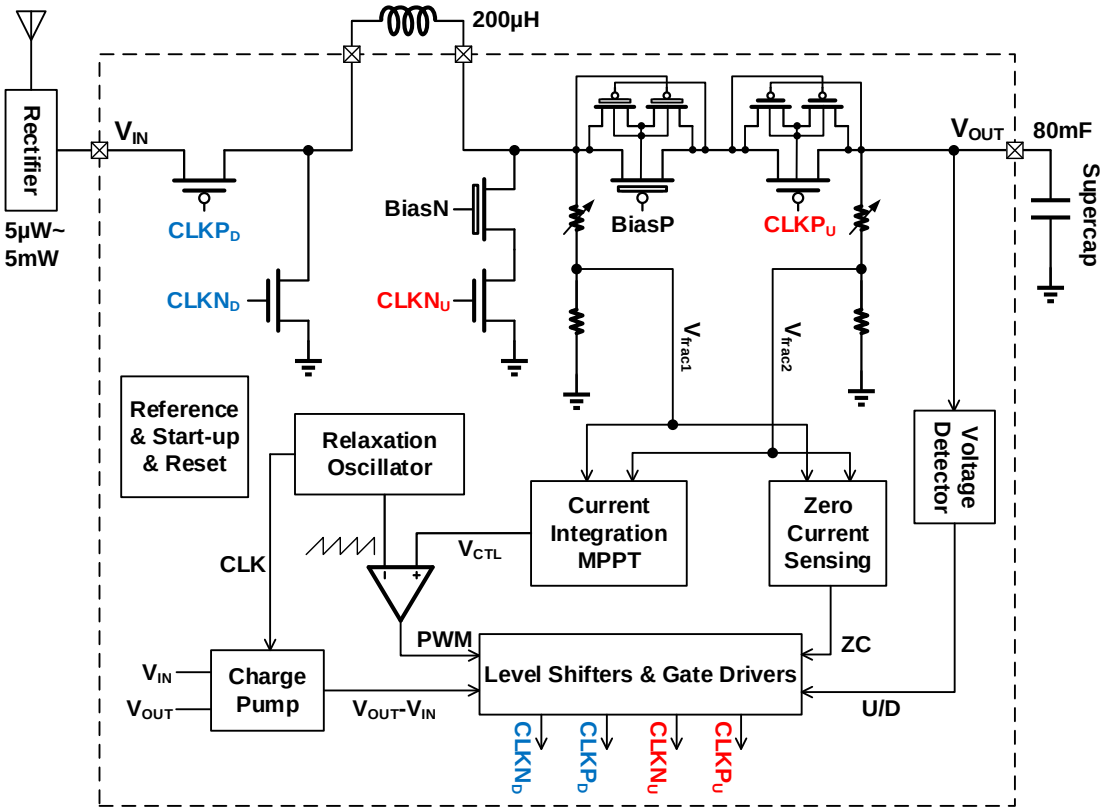


Figure 4.2: Proposed RF energy harvester block diagram

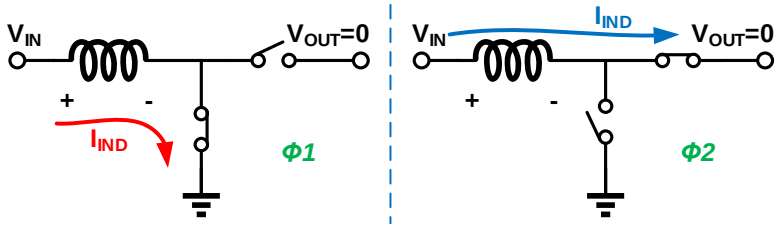


Figure 4.3: Charge 0V with boost converter

4.2.2 Control Loop

There are two loops in the system: one for pulse width modulation (PWM), one for discrete conduction mode (DCM). Both using current mode control, the output current is sensed and fed to the two control loop. Unlike other designs that insert a resistor in the power train [33], this design uses the PMOS power switch as the sensing resistor. Then the differential voltage is divided down by two resistor ladders by a factor of k_{RL}. So the differential voltage of V_{frac1} and V_{frac2} is proportional to load current I_L:

$$\Delta V_{frac} = R_{on} k_{RL} I_L \tag{4.1}$$

where R_{on} is the on resistance of the power switch. The resistor ladders ratio k_{RL} are both tunable, which will be further explained in the voltage protection section.

During ϕ_1, one power switch is turned on (PMOS for buck converter, NMOS for boost converter). The current-integration MPPT controller generates a control voltage V_{CTL}, whose algorithm will be described in detail later. The relaxation oscillator generates both the clock for the converter and a ramp signal for the PWM control. By comparing the ramp signal with V_{CTL}, the pulse width is modulated: $D = V_{CTL} V_{ref}$, where D is the duty cycle, and V_{ref} is the up-bound reference voltage for the ramp signal. This PWM signal is fed to level shifters and

switch buffers to drive the four power switches. One important situation is that, at the beginning, V_{CTL} is zero, and so is the duty cycle. The pulse width is then 0, meaning no switch is turned on, so that the control loop fail to work. To avoid this situation, the PWM scheme has a lowest pulse width, 5ns, to ensure a soft startup, but at the cost of lower efficiency at extreme low input power.

After a short dead time, the other power switch is turned on (NMOS for buck converter, PMOS for boost converter) during ϕ_2. When I_L drops to 0, ΔV_{frac} also transits from positive to negative. The zero current sensor then turns all the power switches off to ensure DCM.

4.2.3 Charge Pump and Level Shifters

Worthy to be notice that the switches for the buck converter operate in the range of 0∼1.2V, but for the boost converter, the switches see V_{OUT}, which can be 0∼3.5V. To turn on the PMOS for the boost converter, the gate voltage should be at least $V_{OUT} - V_{th,p}$. This could be a negative voltage when V_{OUT} is 0 at the beginning. In that case, a charge pump is required. The charge pump generates a voltage of $V_{OUT} - V_{IN}$, and the level shifters can shift the clock signal toggling between 0 and V_{IN}, to the level between $V_{OUT} - V_{IN}$ and V_{OUT}. Circuit details will be described later.

4.3 Voltage protection

Since the energy stored in a supercap is proportional to V_{SC}^2, it is preferred to increase the fully charge voltage to increase capacity. However the rated voltage for 65nm I/O devices is only 2.5V. If we can increase the number to 3.5V, the stored energy would increase nearly by 100% ($3.5^2/2.5^2$=1.96). Most previous designs resorted to either BCD technology or HV-CMOS to solve the high stress [32, 35]. But these technologies are more expensive and less integrateable than standard CMOS. This chapter proposes voltage protection techniques for TSMC 65nm CMOS. Without a separate harvester chip, this design can be integrated with other RFID blocks, and handle the 3.5V high voltage stress.

4.3.1 Power Switches

As is mentioned above, the power switches need to be protected from the high voltage. So both the PMOS and the NMOS are implemented by stacking one core device and one I/O device. The body of each PMOS power switch is kept connected to the highest voltage node through two PMOS helpers. As is shown in Fig. 4.4, $CLKN_U$ toggles between 0 and V_{IN} (1V for example), and $CLKP_U$ between $V_{OUT} - V_{IN}$ (2.5V in this case) and V_{OUT} (3.5V). For each clock phase, the internal nodes voltage are denoted in Fig. 4.4. It can be found that all core

devices only see V_{GS} or V_{GD} less than 1V, and those of I/O devices are less than 2.5V.

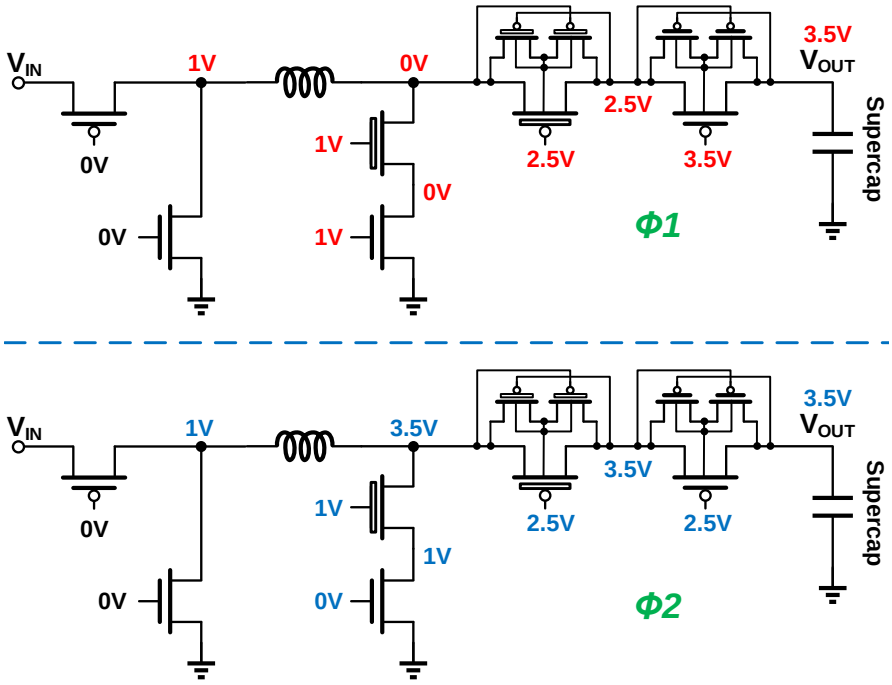


Figure 4.4: Voltage protection for boost converter

4.3.2 Resistor Ladder

Eq. (4.1) shows that, R_{on} and k_{RL}, are preferred to be large so that the sensitivity for load current is also higher. R_{on} depends on the transistor size, which is already fixed. So we can only increase k_{RL}. However, when V_{OUT} is close to fully charged ($\sim$3.5V), to make sure $V_{frac1/2}$ to be less than 1V (required by subsequent circuits), a low k_{RL} ($<2/7$) is needed. To solve this contradiction, the resistor ladder

is designed to be tunable: when V_{OUT} is low, k_{RL} is set higher (1/2) for higher sensitivity; when V_{OUT} is high, k_{RL} is set lower (2/7) for voltage protection. The implementation of the resistor ladder is shown in Fig. 4.5, where resistors are actually not resistors, but reverse biased diodes. This can reduce area and quiescent current, especially at high voltages. Additional bypass MOS caps are added to reduce frequency dependence caused by parasitic.

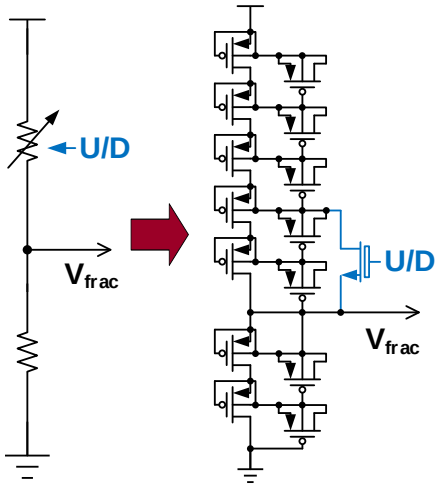


Figure 4.5: Resistor ladder implementation

4.3.3 Zero Current Sensing Comparator

Because of the fact that V_{OUT} has a wide range and the tunable k_{RL} design, $V_{frac1/2}$ varies from 0 to 1V. So the zero current sensing comparator has to be rail-to-rail. The comparator is shown in Fig. 4.6. To prevent it from constant

power consumption, the comparator is duty cycled, as shown in Fig. 4.7. Worthy of pointing out that, the delay cell in the pulse generator is different from conventional inverter chain delay or RC delay. It is a newly designed low power delay cell, which consumes 5x lower power than a simple inverter chain based delay.

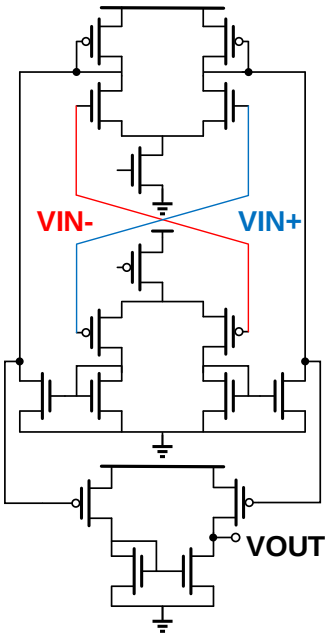


Figure 4.6: Rail-to-rail zero current sensing comparator

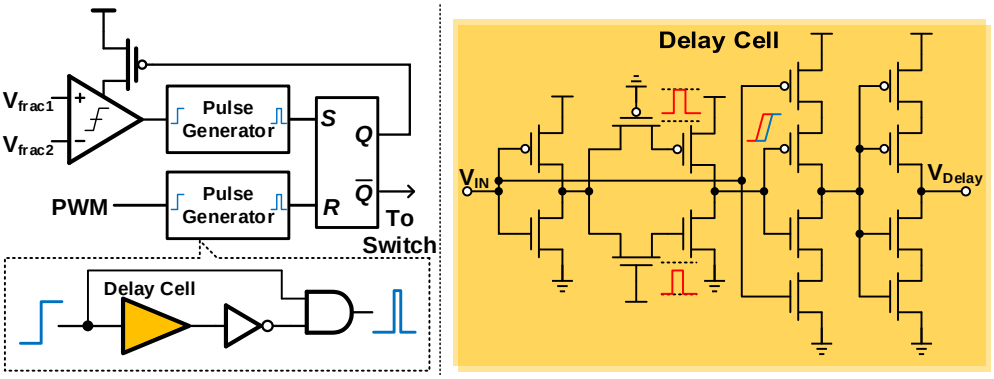


Figure 4.7: Low power zero current sensing circuit

If $k_R L$ is a fixed number (has to be 2/7 for voltage protection), the effective transconductance of the comparator $g_{m,eff} = k_{RL} \times (g_{m,p} + g_{m,n})$. As is shown in the blue line of Fig. 4.8, during the process of charging, V_{OUT} increases from 0 to 3.5V, and $g_{m,eff}$ increases first and then decreases. As described above, k_{RL} is set higher when V_{OUT} is low to improve sensitivity ($g_{m,eff}$). The red line shows the $g_{m,eff}$ for k_{RL}=1/2. The overall $g_{m,eff}$ is shifted from red to blue during the charging process, and is improved with the tunable k_{RL} design.

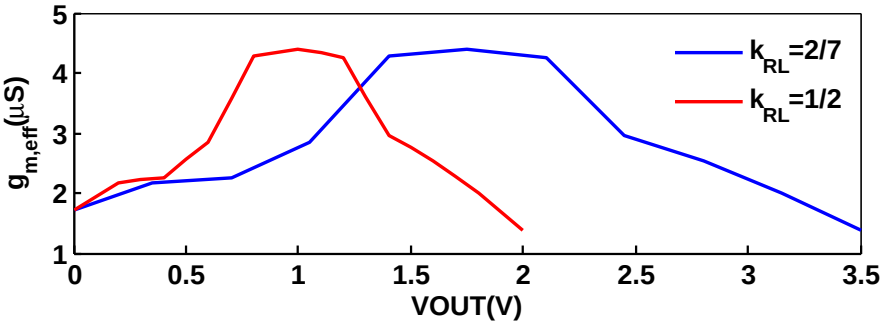


Figure 4.8: Effective g_m of the rail-to-rail comparator during charging process

4.3.4 MPPT OTA

Similar to the zero current sensing comparator, the OTA (input stage) in the MPPT controller also requires linear rail-to-rail operation. Same with [36], the implementation is shown in Fig. 4.9.

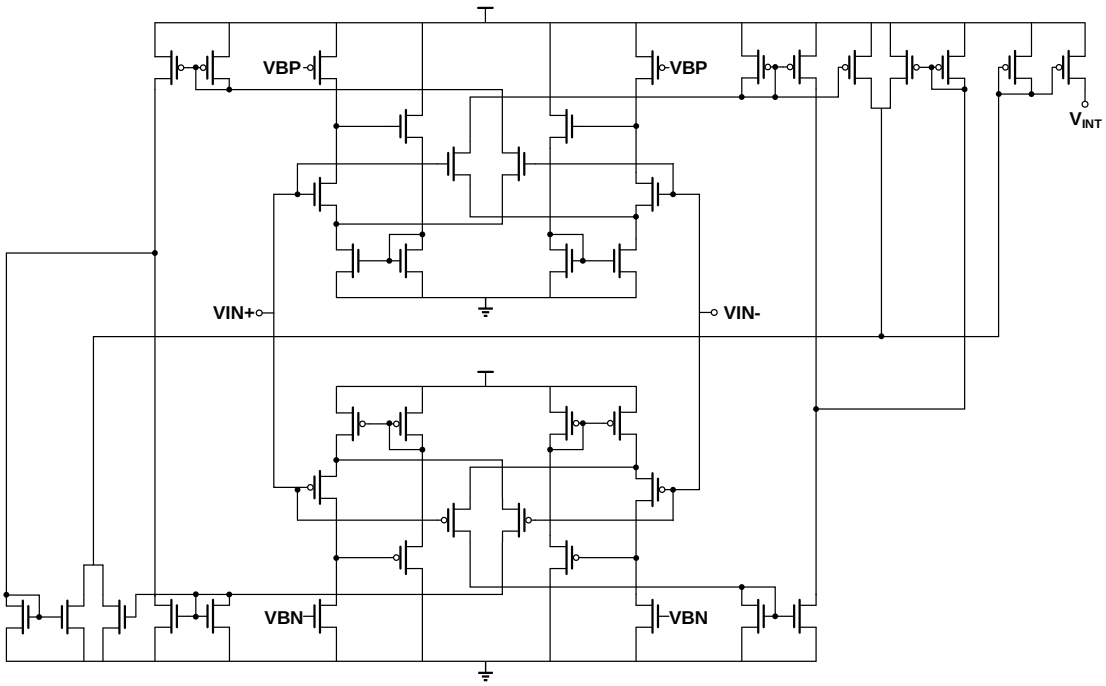


Figure 4.9: rail-to-rail linear GmC integrator OTA

4.3.5 Charge Pump

Subsection 4.3.1 mentions that the power train requires a voltage level of $V_{OUT} - V_{IN}$. So a charge pump is designed to generate that voltage efficiently (Fig. 4.10). Different from traditional charge pump, this design generates four non-overlapping

clock phases, which significantly reduces short circuit current (%? simulation). Two NMOS helpers are added to prevent body diode conduction leakage. The NMOS are implemented by deep N-well devices.

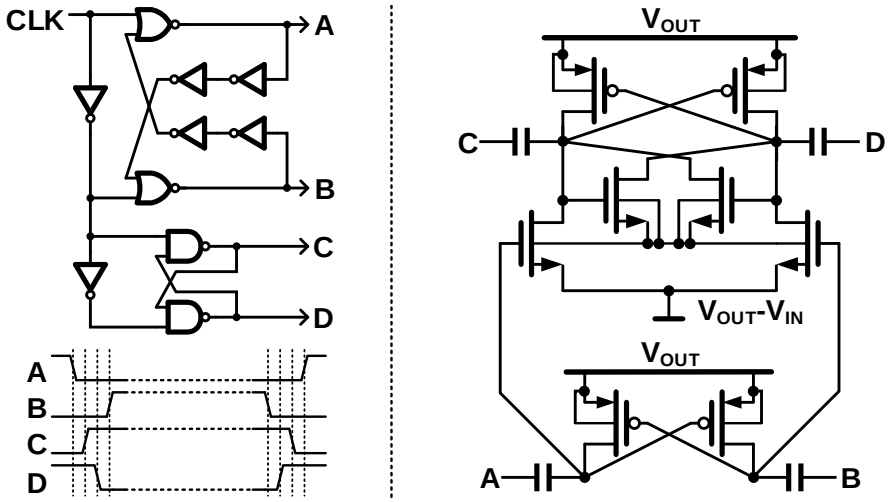


Figure 4.10: Low power negative voltage charge pump

4.4 Current-Integration Based MPPT Controller

Wide range of power range is a key factor for the MPPT controller. To make sure the harvester can handle an input power as low as 5μW, the MPPT controller itself must consumes less power. This is a fairly difficult task, since there are several indispensable analog blocks in the controller, even though they are duty cycled. A common practice for saving power, is to run the MPPT controller at a frequency that is much lower than the switching frequency of the power train [7]. The

MPPT frequency is then usually set by the lowest power and significantly reduces the tracking speed. This chapter proposes an enhanced MPPT controller that has a built-in power estimator to adaptively tune the MPPT frequency. A lower MPPT frequency is set to save power for low power inputs, while a higher MPPT frequency is set to accelerate the tracking speed at high power inputs. Fig.4.11 shows a system level simulation of a fixed frequency based MPPT harvester (blue line) and our proposed adaptive MPPT harvester (red line). In this figure, there is a step change in input power from 10μW to 3mW at 1000μS. The new adaptive algorithm rapidly increases the MPPT frequency, resulting in an 8x increase in tracking speed and 35% additional energy being accumulated during the charging transient.

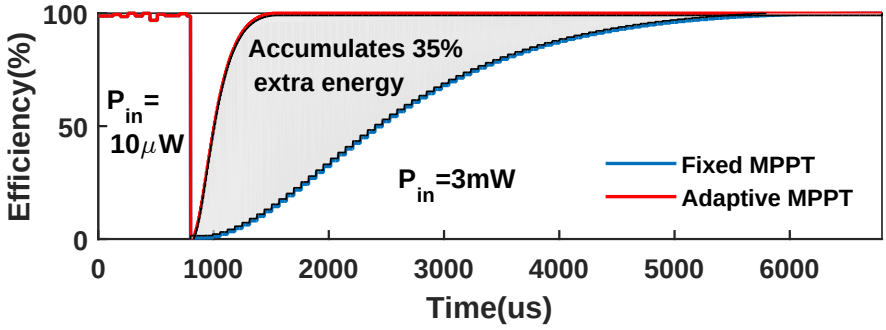


Figure 4.11: Transient MPPT efficiency for fixed v.s. adaptive MPPT

4.4.1 Current-Integration MPPT

Conventional MPPTs measure both the voltage and current, and use their production (power) as the optimization target [32]. However, for charging a supercap, because of its large value, the output voltage does not change much during one cycle (max of 1mV at 5mW input power). So the voltage is relatively constant for a certain time frame and only the current needs to be measured and optimized. Another way to understand this is that, to charge a capacitor, only the charge that is delivered to the supercap in one cycle is of merit regardless of the voltage. The MPPT module is shown in Fig. 4.12. A gm-C integrator (described in last section) converts the fractional voltage from the resistor ladder ($V_{frac1/2}$) to a current and integrates it onto two capacitors (C_A & C_B) alternately. Some conventional designs integrate on one capacitor and flip it after perturbation [37]. But this approach has intrinsic offset, since the integrator sees different voltages before and after the perturbation. Two capacitor approach can easily solve this problem, at the cost of some extra area.

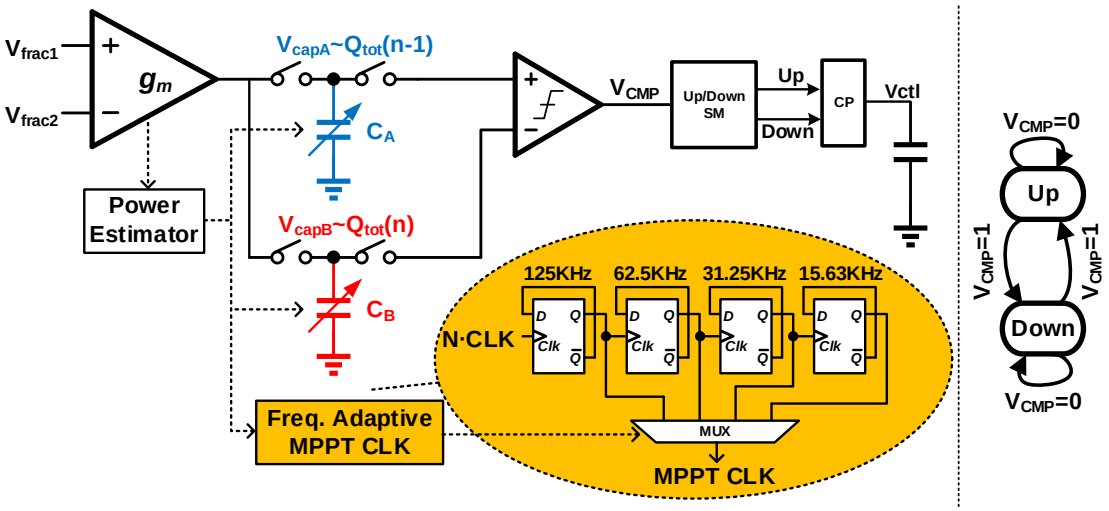


Figure 4.12: Proposed analog MPPT controller & state graph

If the load current is $I_L(t)$, and the charge delivered to the supercap in one cycle is Q_{tot}, the integrated voltage on $C_{A/B}$ after one cycle is:

$$V_{capA/B} = \frac{R_{on}k_{RL}g_m}{C_{A/B}} \int_0^T I_L(t)dt = \frac{R_{on}k_{RL}g_m}{C_{A/B}} Q_{tot} \tag{4.2}$$

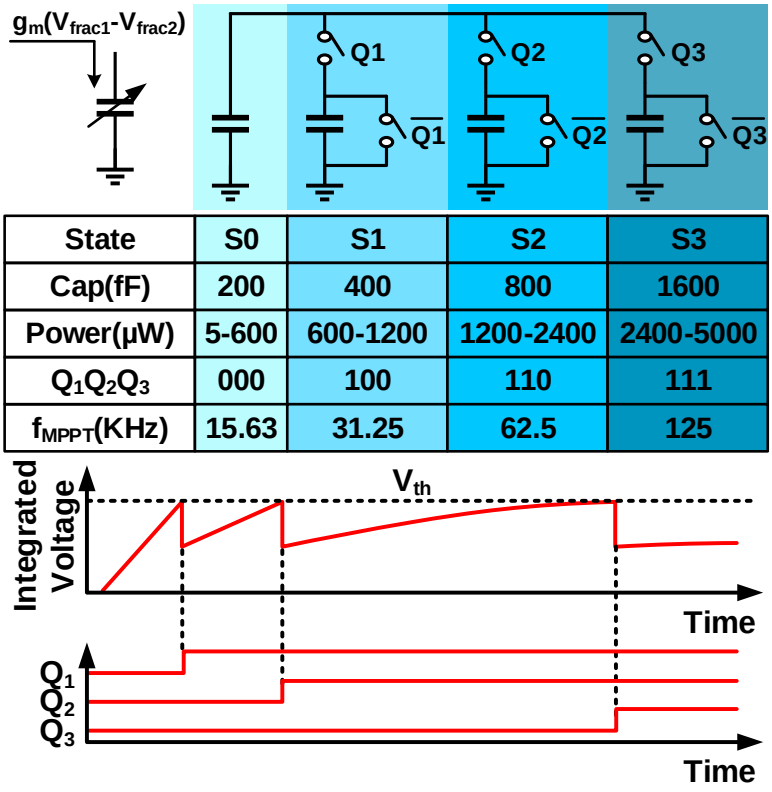
Since only the voltage difference between C_A and C_B is critical, any variation of R_{on}, k_{RL} and g_m are common mode and can be ignored.

V_{capA} represents the power before perturbation ($Q_{tot}(n-1)$) and V_{capB} represents that after perturbation ($Q_{tot}(n)$). If $Q_{tot}(n-1) < Q_{tot}(n)$, meaning the extracted power is improved after the previous perturbation, the perturbation direction is correct. The state machine then will decide the perturbation direction in next cycle (pull-up or pull-down V_{CTL} by the charge pump), according to the

observed information.

4.4.2 Adaptive Capacitor Array

Another insight from eq. (4.2) is that, when the capacitance of $C_{A/B}$ is large, the integrated voltage becomes too small to be detected. On the other hand, if the capacitance is too small, $V_{capA/B}$ can increase rapidly and easily saturate the OTA, especially when incident power is high. To solve this problem, a capacitor array is used instead of a single capacitor, as is shown in Fig. 4.13. Only the smallest capacitor is connected at the beginning, and every time the voltage reaches V_{th}, an additional capacitor is added and the voltage drops to half of the previous value. Fig. 4.13 also shows the integrated voltage waveform and the switch signal $Q_{1\sim3}$. To be aware that each time a switch is turned on and one more capacitor is added, there is charge injection introduced by the switch. Although can be mitigated by implementing both NMOS and PMOS, the effect cannot be ignored and may cause an offset between V_{capA} and V_{capB}. Further solutions are describe later.



State	S0	S1	S2	S3
Cap(fF)	200	400	800	1600
Power(μW)	5-600	600-1200	1200-2400	2400-5000
$Q_1Q_2Q_3$	000	100	110	111
f_{MPPT}(KHz)	15.63	31.25	62.5	125

Figure 4.13: Capacitor array for large power range and power estimation

4.4.3 Power Estimator and Adaptive MPPT Frequency

Adaptive MPPT frequency can solve the contradiction between tracking speed and sensitivity. As is shown in Fig. 4.12, there is a power estimator to adapt both the capacitor tank value and the MPPT frequency. However, the power estimator is not really a separate module, but reusing the existing capacitor array. When the incident power reaches a certain level, the integrated voltage will increase and turn on one or more switches. As a benefit, the input power level can be

estimated easily by finding how many switches are turned on. As is shown in Table of Fig. 4.13, the switch control bits $Q_{1\sim3}$ indicate the input power range, and thus, the MPPT clock frequency can be selected through a MUX (Fig. 4.12). At low powers (Q=000), the MPPT controller is operated at low speeds ($\sim$15KHz) to save power, at the cost of tracking speed. While at high power (Q=111), the MPPT controllers speed is boosted to $\sim$125KHz through a MUX, to speed up tracking by $\sim$8x. There are four possible frequency steps (15.63, 31.25, 62.5 and 125kHz).

4.4.4 MPPT Timing

Fig. 4.14 shows critical signals for the MPPT scheme for low incident power (Q=000) in one cycle. There are 5 phases in each MPPT cycle: power-estimation, pre-power-measurement, perturbation, post-power-measurement and observation. Φ_1 is the power estimation phase and the current is integrated on C_A. Since input power is low, no switches are turned on and C_A is retained at its smallest value. So the blue waveform of V_{capA} does not have the saw-tooth shape as was shown in Fig.4.13. Φ_2 is the pre-power-measurement phase. However, since no switches are turned on in Φ_1, Φ_2 has no difference with Φ_1, and is skipped in this case. A perturbation occurs at Φ_3, when V_{CTL} is pulled-up or pulled-down a little (up in this case). Because of the increase of V_{CTL}, the converter duty cycle increases

proportionally. More current is extracted from the source, so V_{IN} drops gradually. After V_{IN} becomes stable, the load current (output power) is measured and integrated again onto C_B, in Φ_4, with the same Q from Φ_1 (000 in this case). By comparing the voltages on the two capacitors, namely during the observation phase (Φ_5), the direction of the V_{CTL} perturbation for the next cycle is determined. Fig. 4.15 shows the critical signals for high incident power (Q=111). Now all three switches are turned on and the blue waveform of V_{capA} has the saw-tooth shape as in Φ_1. Charge injection of theses switches may cause an offset in the final voltage, so C_A is reset and integrated again in Φ_2, with Q and capacitance inherited from Φ_1. Its counterpart in Fig. 4.14 is skipped. Φ_3 to Φ_5 are similar to those in Fig. 4.14. As shown in the state transition chart of Fig. 4.13, current direction of perturbation (up or down) depends on two things: previous state and observation result (V_{CMP}). If V_{CMP}=0, $Q_{tot}(n) > Q_{tot}(n-1)$, then the previous perturbation direction is correct, so it will be retained (down->down or up->up). While, if V_{CMP}=1, the perturbation direction will be flipped (down->up or up->down). Thus, V_{CTL} is maintained around the optimum point, i.e. the MPP. The state machine, shown in Fig. 4.12, executes the described MPPT logic.

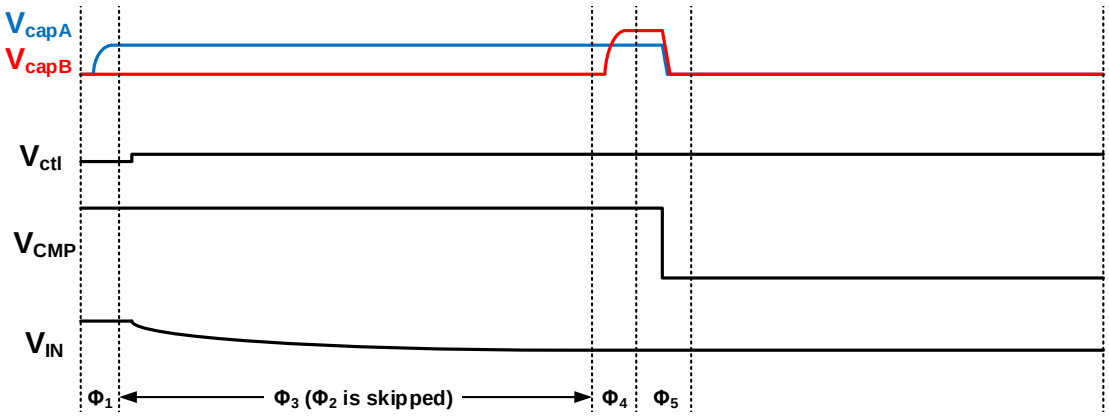


Figure 4.14: Critical signals at low power (Q=000, f_{MPPT} ~15KHz)

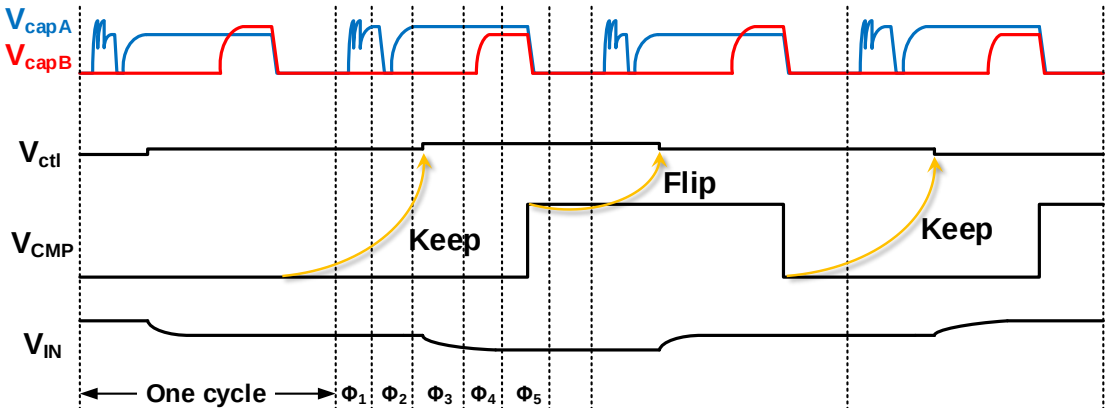


Figure 4.15: Critical signals at high power (Q=111, f_{MPPT} ~125KHz)

4.5 Measurement Results

The design was fabricated in TSMCs 65nm GP process.The die photo is shown in Fig. 4.16. The test setup is shown in Fig. 4.17. There is a 1.2V Zener diode connected to V_{IN} and a 3.5V Zener diode connected to V_{OUT}, in order to prevent

V_{IN} or V_{OUT} exceeds the rated range. If, for some reason, V_{IN} is over 1.2V or V_{OUT} is over 3.5V, the extra power would be dumped to ground through the Zener diodes. The overall efficiency would drop but at least the circuit is ensured to operate functionally. A TPS3808 (TI supervisor) is used to reset the whole circuit if detecting a sudden drop of V_{IN}. Working as a power on reset (POS) block, the TI supervisor can be designed and integrated on chip. But the design routine is skipped by using commercial available chips.

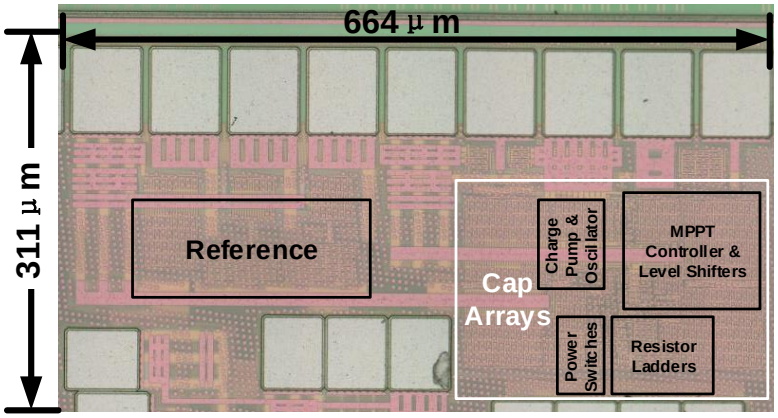


Figure 4.16: Die photo

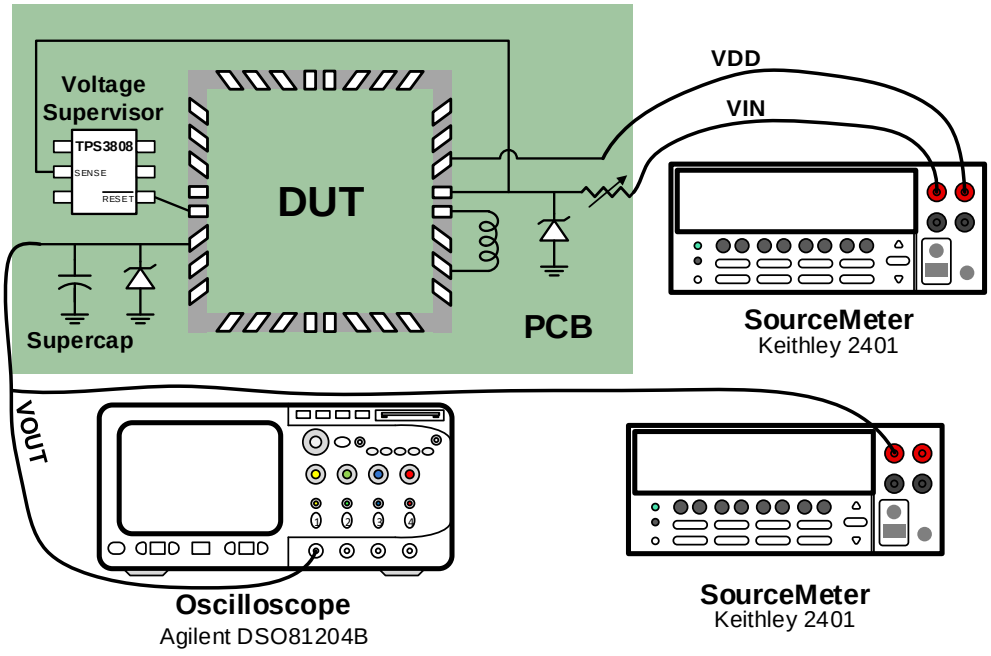


Figure 4.17: Testing setup

The power source is modeled by a 2V voltage source (V_S) and a trimmer as source resistance (R_S). By changing the trimmer resistance, the available power is changed ($P_{av} = V_S/4R_S$) and the proposed harvester can be tested under different conditions. The input impedance of the harvester varies during the charging transient, such that the input voltage seen by the harvester varies between 0.6V$\sim$1.2V. Fig. 4.18 shows the measured conversion efficiency and MPPT efficiency versus V_{OUT} at P_{av}=220μW, while Fig. 4.19 shows them versus P_{av} at V_{OUT}=2V.

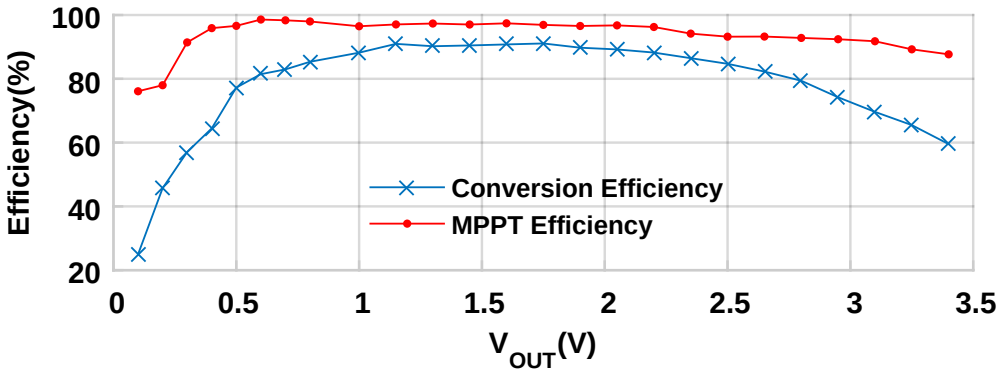


Figure 4.18: Efficiency v.s. V_{OUT} @P_{av}=220μW

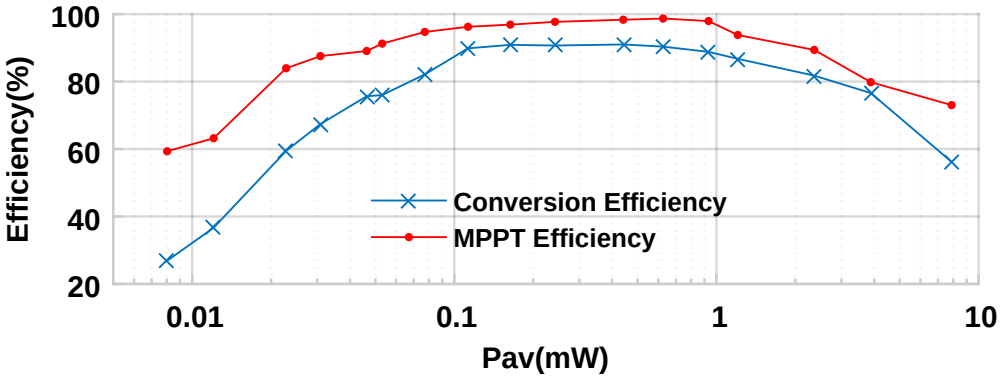


Figure 4.19: Efficiency v.s. P_{av} @V_{OUT}=2V

Table 4.1 compares this design with prior art. As discussed earlier, it is difficult to simultaneously accommodate a large power range with fast response, e.g. [32] has the fastest track time but has the lowest power range. As was shown in Fig. 4.11, an MPPT controller that may have high steady state efficiency but has a slow track time could significantly reduce overall efficiency during charging transients. So we have defined an FOM that considers the ratio of max and min

power and the inverse of the response time. $FOM = P_{av,max}/(P_{av,min}T_{track})$. This design has the highest FOM, as is shown in Fig. 4.20, and the largest output voltage in standard CMOS while maintaining high efficiency.

Table 4.1: Measurement result summary and comparison with prior art

Ref	Tech	Input Voltage	Output Voltage	Input Power	Track Time	Architecture	MPPT Algorithm	Peak Efficiency
[27]	0.35μm BCD	1∼7V	1∼8V	33μW∼ 10mW	20ms	Buck-Boost PFM	One Cycle FOCV	80%
[32]	0.35μm HV	7∼43V	15V	0.4∼ 21.1W	350μs	Buck, PFM	PI, Global Search	94.2%
[33]	0.35μm	0.5∼2.4V	3.5V	650μW ∼1W	2.9ms	Boost, PWM	AZ-PI, SRE-FOCV	92.6%
[34]	0.25μm	0.5∼2V	0∼5V	5μW∼ 10mW	–	Boost, PSM	P&O	87%
[35]	0.25μm BCD	5∼60V	2∼5V	25μW∼ 1.6mW	800ms	Buck, PFM	VS-P&O	88.9%
This Work	65nm	0.6∼1.2V	0∼3.5V	5μW∼ 5mW	584μs	Buck-Boost, PWM	CI, P&O	91%

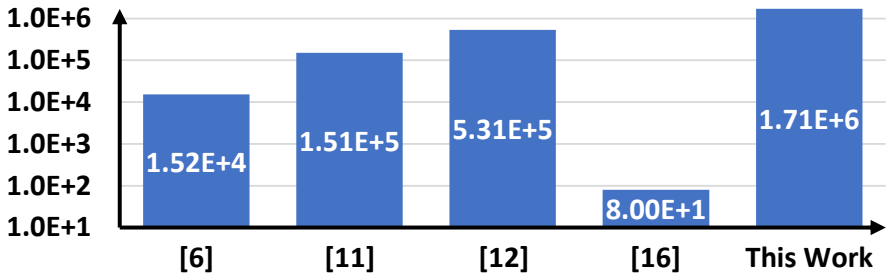


Figure 4.20: $FOM = P_{av,max}/(P_{av,min}T_{track})$ (log scaled)

The relaxation oscillator operates at 1MHz and is fed to the power train switches. While the MPPT frequency is adapted beteen 15∼125KHz. The chip occupies an active area of 0.15mm^2.

4.6 Conclusions

This chapter describes an inductive buck-boost DC-DC converter for energy harvesting. This harvester is used on an RFID for blood temperature monitoring, up-converting the rectified RF signal to charge a supercap as the power supply. A built-in power estimator adapts the MPPT frequency and sampling capacitors with the input power level. This improves the input power range to 1000x, reduces the track time by 8x and improves transient efficiency. Voltage protection techniques extend the maximum output voltage to 3.5V (in a 65nm CMOS GP process), resulting in a 100% increase in the stored energy. The circuit has a peak

conversion efficiency of 91%, and an peak MPPT efficiency of 98.7%. The proposed harvester is designed for RFID tags RF energy harvesting. But the concept can be extended to other energy harvesting systems (solar panel, piezoresistor) and other technology nodes.

Chapter 5

Conclusion

In this thesis, power management techniques are introduced for a supercap based RFID tag for blood temperature monitoring system. The RFID tag is intended to be attached on a blood bag. When a reader approaches, it is charged and reset within 2 minutes at the blood donation time, and ready to be distributed. During the process of transportation and storage, the RFID tag continuously monitors the blood bag's temperature for at least one week. When the reader approaches again, the tag can be recharged, and the temperature data can be read out to make sure the blood product is always kept in the temperature requirements. The power management is critical to ensure the quick charge ($\sim$2 min), and long last monitoring ($\sim$1 week). So two power management units are proposed in this thesis – one for charging, the other for discharging the RFID tag's energy storage

device.

Supercaps are near ideal for low power biomedical applications as supplement or substitute for batteries, as its quick charge, nearly infinite shelf-life, and the lack of toxic heavy metals. But it also has some intrinsic disadvantages: lower energy density and unstable voltage.

To solve the first problem, the supercap can be charged with a higher voltage (3.5V in this thesis), as the stored energy in a capacitor is $CV^2/2$. However, the high voltage exceeds the RFID tag's chip fabrication process's rated voltage limit (2.5V for TSMC 65nm GP). In order not to lose the integrity of the PMUs with other circuitry, voltage protection techniques are introduced to extend the voltage tolerance. As a result, the stored energy is doubled, the chip is more compact and the manufacturing cost is reduced as no extra chip or high voltage processes are required. These techniques are also useful for other applications, such as the PMU for lithium-ion powered (2.8$\sim$4.2V) modern technology SoCs (sub-1V).

The continuously decreasing voltage for the supercap is converted to steady 1V by a discharge PMU to power other circuitry. The proposed discharge PMU implemented by a reconfigurable switched-capacitor DC-DC converter. By combining both buck and boost converters, the discharge PMU can realize fairly flat efficiency profile and low residual energy, resulting an increase of useful energy from 40.8% to 75.3% compared with an LDO.

Similar to all other energy harvesting applications, the proposed RFID tag needs to harvest the RF energy that has large range of power variation (5μW$\sim$5mW). To achieve the large power range, a new MPPT controller is proposed. The MPPT has adaptive MPPT frequency (15.6KHz$\sim$125KHz) and adaptive integration capacitor array (200fF$\sim$1600fF). Not only solving the power range problem, the adaptive MPPT design also solves the contradiction between low power and high speed requirements of the controller, achieving a highest FOM compared with previous publications (considering both tracking time and power range). Both of the adjustment are realized by a built-in power estimator, that reuses existing circuits to achieve low power and simple architecture. This technique can also be extended to other energy harvesting systems (thermal, vibration, solar, etc).

5.1 Research Contributions

- Introduced an overall power management solution for supercap based RFID applications
- A reconfigurable switched-capacitor DC-DC converter is proposed to convert the unstable supercap voltage to a stable 1V voltage
- Increased voltage tolerance of TSMC 65nm GP process from 2.5V to 3.5V, resulting in a 96% improvement of stored energy

- Extracted 98% of energy from a supercap
- Doubled the usage time of a supercap
- A switched-inductor buck & boost DC-DC converter is proposed to harvest RF energy to charge the supercap quickly
- Improved MPPT controller by built-in power estimator enhancement
- Solved contradiction between low power and high speed requirements for MPPT controller, by adaptive MPPT frequency
- Achieved wide input power range by adaptive capacitor array, instead of a single capacitor
- Techniques are all scalable and extendable to other processes and other low power IoT applications.

References

[1] Z. Wan, Y. Tan, and C. Yuen, "Review on energy harvesting and energy management for sustainable wireless sensor networks," in *Communication Technology (ICCT), 2011 IEEE 13th International Conference on.* IEEE, 2011, pp. 362–367.

[2] W. H. Organization *et al.*, "Safe blood and blood products: manual on the management, maintenance and use of blood cold chain equipment," 2005.

[3] R. J. Vullers, R. Van Schaijk, H. J. Visser, J. Penders, and C. Van Hoof, "Energy harvesting for autonomous wireless sensor networks," *IEEE Solid-State Circuits Magazine*, vol. 2, no. 2, pp. 29–38, 2010.

[4] L. Mainetti, L. Patrono, and A. Vilei, "Evolution of wireless sensor networks towards the internet of things: A survey," in *Software, Telecommunications and Computer Networks (SoftCOM), 2011 19th International Conference on.* IEEE, 2011, pp. 1–6.

[5] A. Roy *et al.*, "A 6.45μW self-powered SoC with integrated energy-harvesting power management and ULP asymmetric radios for portable biomedical systems," *IEEE transactions on biomedical circuits and systems*, vol. 9, no. 6, pp. 862–874, 2015.

[6] D. Bandyopadhyay and J. Sen, "Internet of things: Applications and challenges in technology and standardization," *Wireless Personal Communications*, vol. 58, no. 1, pp. 49–69, 2011.

[7] G. Yu, K. W. R. Chew, Z. C. Sun, H. Tang, and L. Siek, "A 400 nW single-inductor dual-input–tri-output DC-DC buck-boost converter with maximum power point tracking for indoor photovoltaic energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 11, pp. 2758–2772, 2015.

[8] P. Aqueveque and J. Barboza, "Wireless power system for charge supercapacitors as power sources for implantable devices," in *Emerging Technologies: Wireless Power (WoW), 2015 IEEE PELS Workshop on.* IEEE, 2015, pp. 1–5.

[9] A. Shukla, S. Sampath, and K. Vijayamohanan, "Electrochemical supercapacitors: Energy storage beyond batteries," *CURRENT SCIENCE-BANGALORE-*, vol. 79, no. 12, pp. 1656–1661, 2000.

[10] W. Sanchez, C. Sodini, and J. L. Dawson, "An energy management IC for bio-implants using ultracapacitors for energy storage," in *VLSI Circuits (VLSIC), 2010 IEEE Symposium on*. IEEE, 2010, pp. 63–64.

[11] H.-P. Le *et al.*, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm^2 at 81% efficiency," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*. IEEE, 2010, pp. 210–211.

[12] X. Hua and R. Harjani, "3.5-0.5V input, 1.0V output multi-mode power transformer for a supercapacitor power source with a peak efficiency of 70.4%," in *Custom Integrated Circuits Conference (CICC), 2015 IEEE*. IEEE, 2015, pp. 1–4.

[13] S. Bandyopadhyay, Y. K. Ramadass, and A. P. Chandrakasan, "20μA to 100mA DC-DC converter with 2.8-4.2V battery supply for portable applications in 45nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2807–2820, 2011.

[14] V. Ng and S. Sanders, "A 92%-efficiency wide-input-voltage-range switched-capacitor DC-DC converter," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*. IEEE, 2012, pp. 282–284.

[15] R. Balczewski and R. Harjani, "Capacitive voltage multipliers: A high efficiency method to generate multiple on-chip supply voltages," in *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*, vol. 1. IEEE, 2001, pp. 508–511.

[16] A. Biswas, Y. Sinangil, and A. P. Chandrakasan, "A 28nm FDSOI integrated reconfigurable switched-capacitor based step-up DC-DC converter with 88% peak efficiency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1540–1549, 2015.

[17] B. Serneels, M. Steyaert, and W. Dehaene, "A high speed, low voltage to high voltage level shifter in standard 1.2V 0.13μm CMOS," *Analog Integrated Circuits and Signal Processing*, vol. 55, no. 1, pp. 85–91, 2008.

[18] B. Razavi, "The strongarm latch [a circuit for all seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.

[19] R. Harjani and S. Chaubey, "A unified framework for capacitive series-parallel DC-DC converter design," in *Custom Integrated Circuits Conference (CICC), 2014 IEEE Proceedings of the*. IEEE, 2014, pp. 1–8.

[20] D. El-Damak, S. Bandyopadhyay, and A. P. Chandrakasan, "A 93% efficiency

reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*. IEEE, 2013, pp. 374–375.

[21] G. V. Piqué, "A 41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90nm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*. IEEE, 2012, pp. 98–100.

[22] Y. Ramadass, A. Fayed, B. Haroun, and A. Chandrakasan, "A 0.16mm^2 completely on-chip switched-capacitor DC-DC converter using digital capacitance modulation for LDO replacement in 45nm CMOS," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*. IEEE, 2010, pp. 208–209.

[23] M. Wieckowski, G. K. Chen, M. Seok, D. Blaauw, and D. Sylvester, "A hybrid DC-DC converter for sub-microwatt sub-1V implantable applications," in *VLSI Circuits, 2009 Symposium on*. IEEE, 2009, pp. 166–167.

[24] S. Bandyopadhyay, P. P. Mercier, A. C. Lysaght, K. M. Stankovic, and A. P. Chandrakasan, "A 1.1nW energy-harvesting system with 544pW quiescent power for next-generation implants," *IEEE journal of solid-state circuits*, vol. 49, no. 12, pp. 2812–2824, 2014.

[25] C. Hua, J. Lin, and C. Shen, "Implementation of a DSP-controlled photovoltaic system with peak power tracking," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 1, pp. 99–107, 1998.

[26] M. Kiani, B. Lee, P. Yeon, and M. Ghovanloo, "A power-management ASIC with Q-modulation capability for efficient inductive power transmission," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[27] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30 μW to 10 mW piezoelectric energy harvesting system with 9.09 ms/V maximum power point tracking time," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2367–2379, 2015.

[28] H.-J. Chen, Y.-H. Wang, P.-C. Huang, and T.-H. Kuo, "An energy-recycling three-switch single-inductor dual-input buck/boost DC-DC converter with 93% peak conversion efficiency and 0.5 mm^2 active area for light energy harvesting," in *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*. IEEE, 2015, pp. 1–3.

[29] J.-P. Im, S.-W. Wang, S.-T. Ryu, and G.-H. Cho, "A 40 mV transformer-reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp.

3055–3067, 2012.

[30] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, 2012.

[31] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE transactions on power electronics*, vol. 20, no. 4, pp. 963–973, 2005.

[32] S. Uprety and H. Lee, "A 43V 400mW-to-21W global-search-based photovoltaic energy harvester with 350μs transient time, 99.9% MPPT efficiency, and 94% power efficiency," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE, 2014, pp. 404–405.

[33] S. Uprety and H. Lee, "A 93%-power-efficiency photovoltaic energy harvester with irradiance-aware auto-reconfigurable MPPT scheme achieving >95% MPPT efficiency across 650μW to 1W and 2.9 ms FOCV MPPT transient time," in *Solid-State Circuits Conference (ISSCC), 2017 IEEE International*. IEEE, 2017, pp. 378–379.

[34] Y. Qiu, C. Van Liempd, B. O. het Veld, P. G. Blanken, and C. Van Hoof,

"5μW-to-10mW input power range inductive boost converter for indoor photovoltaic energy harvesting with integrated maximum power point tracking algorithm," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2011 IEEE International*. IEEE, 2011, pp. 118–120.

[35] S. Stanzione *et al.*, "A self-biased 5-to-60V input voltage and 25-to-1600μW integrated DC-DC buck converter with fully analog MPPT algorithm reaching up to 88% end-to-end efficiency," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE International*. IEEE, 2013, pp. 74–75.

[36] C.-C. Hung, K. Halonen, V. Porra, and M. Ismail, "Low-voltage CMOS GM-C filter with rail-to-rail common-mode voltage," in *Circuits and Systems, 1996., IEEE 39th Midwest symposium on*, vol. 2. IEEE, 1996, pp. 921–924.

[37] R. Enne, M. Nikolic, and H. Zimmermann, "A maximum power-point tracker without digital signal processing in 0.35 μm CMOS for automotive applications," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*. IEEE, 2012, pp. 102–104.