Dynamics and Structure-Property Relationships in Organic Single Crystal Electrical Double Layer Transistors

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Dedication

This work is dedicated to my wife Caitlin for all the love and support she has shown me throughout all of my graduate career and also to my parents Craig and Linda for fostering a spirit of curiosity in me from a young age.

Abstract

The goal of this dissertation is to gain a deeper understanding of the factors governing electrical double layer transistor (EDLT) performance. Specifically, the effects of ion structure on EDLT performance are examined in detail towards the end of this work (Chapters 7, 8, and 9). A deep understanding of structure property relationships is fundamental to both being able to design novel high-performance ionic liquids for EDLT applications as well as being able to choose an ideal ionic liquid for a targeted application. Ion structure is a crucial factor determining a wide variety of ionic liquid and EDLT properties with simple structural modifications leading to changes in many ionic liquid and device properties simultaneously.

Chapters 1-4 provide background knowledge helpful for understanding the research presented in Chapters 5-8. Chapter 5 explores dynamics of electric double layer formation in ionic liquid-based devices and provides insight about the relevant time scales involved. Chapter 6 focuses on work done to study free charge in EDLTs through spectroscopic means. Chapter 7 explores the effects of ion volume on various EDLT performance metrics. Chapter 8 digs deeper into an interesting observation made in the work of Chapter 7 involving ion volume and EDLT threshold voltage ultimately leading to an examination of the effects of ion adsorption on threshold voltage. This work is but a drop in the bucket required to gain a thorough understanding of these exceedingly complex systems, and Chapter 9 covers the many avenues of continued research that exist.

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Chapter 1: Introduction

1.1 Motivation

Inorganic semiconductors form the basis of nearly all currently used electronic devices. Specifically, silicon, due to both its abundance and its ability to form a useful native-oxide, is particularly ubiquitous. Compared with single crystalline silicon (a not particularly high-performing inorganic semiconductor), even the best current organic semiconductors cannot hope to compete in terms of carrier-mobility and switching frequency. For many applications, however, the ideal semiconductor is not necessarily the one with the highest electrical performance but the one that performs adequately at the lowest cost.

Low cost electronics is one of the largest driving forces behind organic semiconductor research. Some of the applications that stand to benefit most from advancements in cheaper electronic device fabrication are disposable sensors for use in patient health and food safety monitoring; radio frequency identification tags (RFID) for use in logistics and inventory management; organic light-emitting diodes (OLED) for use in television, cell phone, and other displays; and organic photovoltaics (OPV) for use in cheap, flexible solar panels to meet growing energy needs worldwide.[1-2] The structure of inorganic semiconducting materials is comprised primarily of covalent or ionic bonds. These strong bonds give these materials robust mechanical properties; however, breaking these strong bonds requires significant energy input. To form single crystalline silicon wafers, the materials must be heated to 1500 degrees Celsius for many hours. The high

usage of energy and long periods of time are reflected in the price of silicon wafers. Organic semiconductors; however, are held together predominantly by very weak intermolecular Van der Waals interactions. The weak intermolecular bonding allows organic semiconductors to be readily dissolved in a wide variety of solvents. This allows for organic thin-film transistors (TFTs) to be formed via more cost-effective methods such as casting, spin-coating, low temperature vapor deposition, and printing.[3-6] Printing, in particular, could prove to be a very cost-effective manufacturing technique for large area electronics. Traditional electronic fabrication relies on photolithography and lift-off processes which are subtractive in nature. This means that material is coated over the entire substrate surface and then removed where it is not needed leading to high amounts of material waste. It is also a process that requires a large number of steps. Printing, on the other hand, is an additive process that is essentially a single step. Material is only added where it is needed, so very little material is wasted; therefore, printing has the potential to save money on materials and steward the Earth's resources better than photolithographic manufacturing.

Like printing, roll-to-roll manufacturing is another highly-desirable, cost-effective manufacturing technique that would greatly benefit large-area device manufacturing. The nature of roll-to-roll manufacturing allows all processing steps to be conducted continuously instead of relying on batch processes as is necessary with silicon wafer fabrication. This results in a significant increase in throughput, which translates to lower cost products. Flexible substrates are a requirement for roll-to-roll manufacturing. The cheapest and most widely available flexible substrate material is plastic. Flexible plastics

inherently have low melting temperatures and large coefficients of thermal expansion due to the weaker bonding and coiled polymer chains that give them their flexibility. This increased sensitivity to temperature makes flexible plastic substrates largely incompatible with inorganic semiconductor deposition techniques. The lower processing temperatures required to evaporate and anneal organic thin films make organic semiconductors a much more suitable material for use in roll-to-roll manufacturing. Additionally, as mentioned before, the ability to print or coat films of organic semiconductors from solution without the need for a high-temperature sintering step provides alternative low-temperature deposition techniques also compatible with a roll-to-roll process.

While organic semiconductors show great promise with regard to cheap and flexible electronics, many things remain unknown about charge transport within these materials. Charge transport in organic semiconductors is fundamentally different than charge transport in inorganic semiconductors. In inorganic semiconductors charge predominantly flows through the network of covalent bonds comprising the structure of the material. By contrast, in organic semiconductors charge predominantly flows through a π-bond system. The charge flow can either be along a conjugated system within a single molecule or between overlapping p-orbitals of adjacent molecules.

To further differentiate inorganic and organic semiconductors, inorganic semiconductors tend to have structures comprised of atoms while organic semiconductors have structures comprised of molecules. One consequence of this is that inorganic charge transport is relatively isotropic (the same in all directions) while organic charge transport can be highly anisotropic (different depending on direction).

Another significant difference arises from the difference in dielectric constants between inorganic and organic semiconductors. Inorganic materials tend to have higher dielectric constants than organic materials. This means that electric fields are better screened over a shorter distance in inorganic semiconductors than in organic semiconductors. Another way to state this is that the Coulomb force between two charges is smaller in inorganic semiconductors compared to organic semiconductors. This property becomes very important when considering organic semiconductors for use photovoltaics (PV). In a photovoltaic, light is absorbed by a semiconductor to generate positive and negative charge which are then separated by an applied voltage creating a current. When an inorganic PV absorbs light, an electron is excited into the conduction band becoming free of its host atom which now is host to a positively charged electron hole. Due to the higher dielectric constant, the electron and hole are not strongly attracted to each other. This allows the electron and hole to be easily separated with an applied voltage. Because of the lower dielectric constant of organic semiconductors, the electron and hole are much more strongly attracted together. When light is absorbed in an OPV, the electron never effectively breaks free from the resulting hole. They remain loosely bonded together and are in this state called an exciton. Excitons have a finite lifetime (on the order of nanoseconds) before the electron and hole recombine. If the electron and hole recombine, no useful energy is obtained by the OPV; therefore, a good OPV must separate as many excitons as possible to minimize the amount of energy lost to recombination. In order to separate an electron from a hole, current technology focuses on using an interface between two materials with different electron affinities and ionization energies called a

heterojunction. The heterojunction essentially creates a strong local electric field capable of separating the electron and hole. While the heterojunction effectively separates charge, the main issue is ensuring the exciton reaches the interface before it recombines. The short lifetime of excitons means that excitons are only capable of diffusing on the order of tens of nanometers before they recombine. Engineering heterojunctions that minimize losses due to recombination is one of the most active areas of research within the OPV community.

One final difference between charge transport in inorganic and organic semiconductors can be attributed to the relative strength of bonding within the materials. When an electron or hole is injected into a semiconductor, atoms near this charge are attracted to this charge due to dispersion/polarization. This induces structural deformation as local atoms are pulled towards the charge. This structural deformity is called a polaron. Because inorganic semiconductors are generally composed of strong, rigid covalent bonds (as well as a higher dielectric constant) the deformation induced by a charge carrier is relatively small. By contrast, the Van der Waals bonding in organic semiconductors is weak and readily deformable. When a charge is injected into an organic semiconductor, the structure of material will deform around the charge much more significantly leading to a much larger polaron. The presence of large polarons is very important with regards to how charge moves through the material. Deforming the structure to such a degree takes a large amount of energy. As the charge moves through the semiconductor, the charge will also be followed by the large structural distortions of the polaron meaning that it is relatively more difficult and energy intensive for charges to move through an organic

semiconductor than an inorganic semiconductor.

Considering all of the factors above, it is easy to see that charge transport in organic semiconductors is both very different from that in inorganic semiconductors as well as significantly more complicated. Understanding charge transport, however, is paramount to being able to develop novel high-performing organic semiconductors. One active and important push to understand charge transport is through work being done to understand structure-property relationships. Structure-property relationships explain how certain aspects of the physical structure of the semiconductor (chemical composition, bond angles, layer spacing, etc.) affect the charge transport properties of the semiconductor (conductivity, charge carrier mobility, resistance-temperature behavior, etc.). Material defects (grain boundaries, vacancies, dopants, etc.) can drastically affect charge transport behavior making it difficult to study structure-property relationships using amorphous or polycrystalline organic thin-film transistors (OTFT), though these devices have significant appeal for real world applications. In order to more clearly elucidate structure-property relationships in lieu of defects, an important research tool, single crystal organic field effect transistors, are used.[7] More information is provided on these devices in Chapter 2.

Besides structure, free charge carrier density is another factor that can significantly affect charge transport behavior. Free charge carrier density is one of the main parameters affecting electronic phase transitions in semiconductors, insulators, and superconductors.[8-9] Electronic phase transitions refer to things like insulator-to-metal transitions where, at low charge density, the resistance of the material increases towards infinity as it is cooled towards absolute zero (insulating transport), but at high charge density the resistance of the

material decreases towards a finite value as it is cooled towards absolute zero (metallic transport). By increasing free charge density it is even possible to induce a superconducting state in materials that are not natively superconducting. Examples of this include alkali doped picene and C_{60} crystals as well as field-induced superconductivity in $SrTiO_3$.[10-14] Figure 1.1 provides examples of the types of electronic phase transitions observed in organic materials as well as the charge density required to observe the transitions.

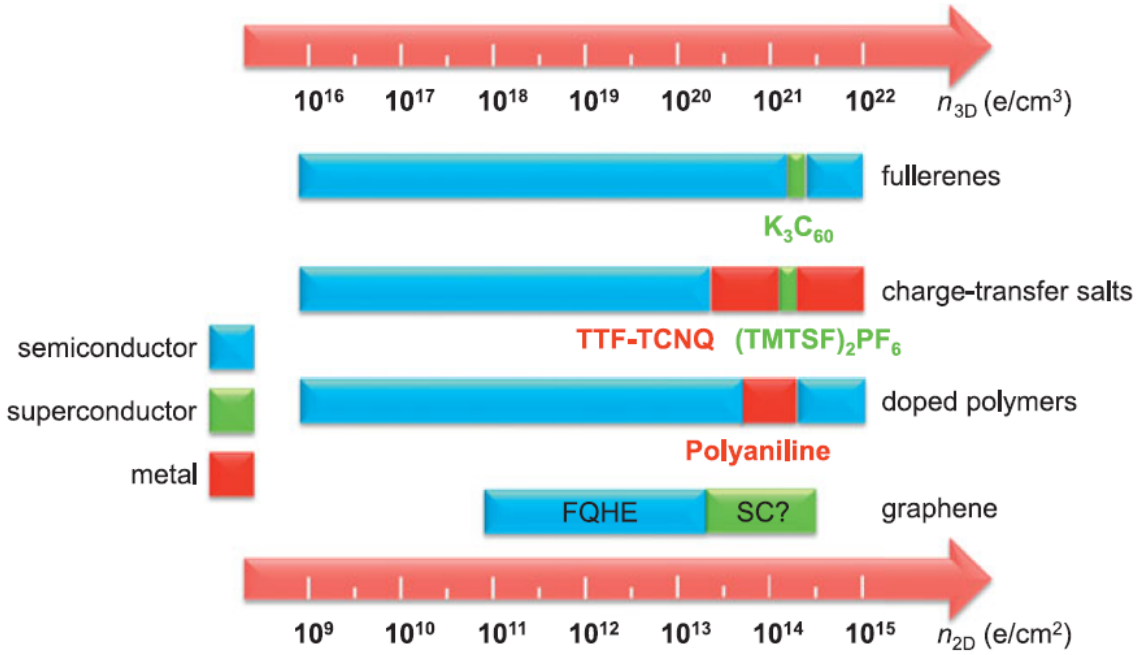


Figure 1.1 Required charge densities to observe different electronic phases in various organic materials. Minimum charge density to observe novel charge transport behavior is on the order of 10^{13} cm^{-2}.[15]

As described above, the injection of high densities of free charge carriers can expand the behaviors and capabilities of a given material; therefore, it is of fundamental interest to study how organic semiconductors behave when injected with a high density of charge carriers. Injecting large amounts of charge into a material usually requires the use of a high capacitance dielectric material. In order to reach the 10^{13}-10^{15} cm^{-2} charge density required for many of the unique, observed electronic phase transitions, a dielectric layer with a specific capacitance on the order of $\mu F/cm^2$ is required. To reach this value of specific capacitance in a traditional silicon transistor using a solid dielectric, a very thin, pinhole-free, high-k dielectric with a high breakdown voltage needs to be used. While this is possible to make, it requires a high-degree of engineering to obtain, and this engineering process would likely need to be unique for each different semiconductor material you wanted to test. Electrolyte gating is a much simpler alternative approach capable of achieving the required charge densities.[16] This concept involves using an ionic liquid as the dielectric material in a transistor. The resulting device is called an electrical double layer transistor (EDLT). EDLTs prove to be a useful research tool to explore charge transport behavior at high-charge density. EDLTs, however, also show potential in a more practical role with regards to manufacturing devices via printing or roll-to-roll processes. More information regarding electrical double layer transistors is found in Chapter 3.

The ultimate goal of this thesis is to further fundamental understanding of electrical double layer transistors in order to improve their performance both in research and practical applications. To achieve this goal three main routes of research were pursued: 1) characterization of the different dynamics and time scales involved in the operation of

electrolyte gated devices through electrical measurements and modeling; 2) spectroscopic study of electrolyte gated devices, used in conjunction with electrical measurements, to better characterize free charge carrier injection; and 3) systematic study of ion structure-EDLT device property relationships.

1.2 Thesis Overview

Chapter 2 focuses on basic concepts about organic field effect transistors (OFETs). This includes their origin, structure, principles of operation, and electrical characterization. In particular, single crystal OFETs receive attention due to their use as a test-bed to study intrinsic transport properties though OTFTs receive some attention as well due to their importance in practical applications.

Chapter 3 focuses on concepts about electrolyte gating and EDLTs. This includes discussion about geometries and structures of various electrolyte gated devices, useful applications, ionic liquid structure and properties, electrical double layer structure, electrical characterization, recent studies, and more.

Chapter 4 comprises the experimental methods used throughout this thesis. Included is discussion about growth of organic single crystals, fabrication of device substrates, structural characterization of crystals and substrates, and electrical characterization methods.

Chapter 5 summarizes work done to better understand the different dynamics and time scales involved in electrolyte gated devices. Specifically, a gold-ionic liquid-gold capacitor was electrically characterized across many orders of magnitudes of time scales

using impedance analysis and displacement current measurements. Sha Shi, under supervision of P. Paul Ruden, developed an equivalent circuit model to well describe the experimental data. The key result from this work is that while most of the double layer formation happens on the order of microseconds, a significant portion of charge relaxation is occurring long beyond this timescale with some measurable charge relaxation still occurring on the order of seconds. This work has been previously published as Elliot Schmidt, Sha Shi, P. Paul Ruden, and C. Daniel Frisbie, "*Characterization of the Electric Double Layer Formation Dynamics of a Metal/Ionic Liquid/Metal Structure*", Appl. Mater. Interfaces **2016**, 8 (23), 14879-14884.

Chapter 6 summarizes work done to understand free charge carrier injection in EDLTs. Rubrene EDLTs were analyzed both with DC electrical measurements and IR spectroscopy. Electrical characterization, while useful, measures all charge injection into a system and does not distinguish between free and trapped charge. Because free charge has a distinct IR absorbance compared to trapped charge, the free charge contribution to charge injection could be identified using IR spectroscopy. The key observation in this work focuses on the presence of a large density of free charge in the system in absence of an applied gate bias. Further elucidation for this phenomenon is provided in Chapter 8. Crystal growth, device fabrication, and electrical measurements were performed by Elliot Schmidt in conjunction with Timothy Atallah. IR spectroscopy measurements were performed by Timothy Atallah and Martin Gustafsson. This work has been previously published as Timothy L. Atallah, Martin V. Gustafsson, Elliot Schmidt, C. Daniel Frisbie, and X.-Y. Zhu, "*Charge Saturation and Intrinsic Doping in Electrolyte-Gated Organic*

Semiconductors", J. Phys. Chem. Lett**. 2015**, 6 (23), 4840-4844.

Chapter 7 summarizes work done to understand the effect of ion volume on the performance of EDLTs. Ionic liquids were systematically chosen to identify two sets of ionic liquids that varied in ion pair volume while minimizing variations in any confounding structural variables like chemical functionality, shape, and bonding. Of the two sets, one set has a fixed anion with cations that varied in volume while the other set has a fixed cation with anions that varied in volume. This was done to explore the impacts of anion and cation volume independently. Key results show an increase in EDLT conductivity as ion volume decreased in both the case of cations and anions, though the dependence is stronger for anions. The resultant conductivity increase is a result both of an increase in capacitance and charge carrier mobility as ion size decreases. Interestingly a correlation in threshold voltage and ion volume was also observed; however, the trend was not monotonic indicating other confounding factors played a significant role. This observation is further explored in Chapter 8.

Chapter 8 summarizes work done to understand the significant shift in threshold voltage observed in EDLTs made with ionic liquids with different ion pair volumes. The non-monotonic nature of the threshold voltage-ion volume relationship discussed in Chapter 7 indicated that ion volume may not be the driving force behind threshold voltage shifts but rather a correlating/confounding factor. Ion adsorption at device interfaces was identified as a possible explanation for the observed threshold voltage shifts. To quantify ion adsorption interactions, potential of zero charge measurements were conducted on gold (representing the gate electrode of an EDLT) via the immersion method. A strong

monotonic, nearly 1-to-1, relationship was found between shifts in the potential of zero charge on gold and the threshold voltage shifts in rubrene EDLTs using the same ionic liquids. This indicates that ion adsorption not only seems to play a role in threshold voltage determination, it also appears to be one of the most important factors in its determination with the ability to shift threshold voltages by nearly 1 volt in devices with operating windows of only a few volts.

Chapter 9 presents promising directions for future work that will continue to grow our understanding of the dynamics and relationships governing EDLT performance. In particular, further routes for continued study of ionic liquid structure-EDLT property relationships are presented.

Chapter 2: Organic Field Effect Transistors

2.1 Charge Transport in Organic Semiconductors

Charge transport in organic semiconductors is inherently different than charge transport in inorganic semiconductors. Three of the main reasons for this difference are the molecular nature of organic semiconductors (small molecules and polymers), lower dielectric constants, and the Van der Waals bonding holding these materials together. Together, these differences lead to organic semiconductors having many unique characteristics such as reduced delocalization of charge carriers, stronger exciton formation, and larger polaron formation. Further detail regarding charge transport in organic semiconductors is explored within this section.

2.1.1 Molecular Orbitals

Organic materials, be they single crystalline, polycrystalline, or amorphous, are all (with few exceptions) made up of molecular sub-units. Because molecules are the basis of organic materials, it is important to first understand the electronic structure of individual molecules.

The theory of linear combination of atomic orbitals states that when two half-filled atomic orbitals, each with its own discrete energy states, combine to form a molecular orbital, two new energy states are created called the bonding and anti-bonding states (Figure 2.1). The bonding state is lower in energy than either of the two initial atomic

orbitals providing the energetic impetus to form and maintain the bond. The anti-bonding state is so named as it is higher in energy than either of the two initial atomic orbitals. Electrons in the anti-bonding state would energetically prefer to go back into the isolated atomic orbitals and therefore provide an impetus to break the molecular bond. In the ground state, the two electrons (one from each of the original half-filled atomic orbitals) will occupy the lowest energy state, which is the molecular bonding orbital.

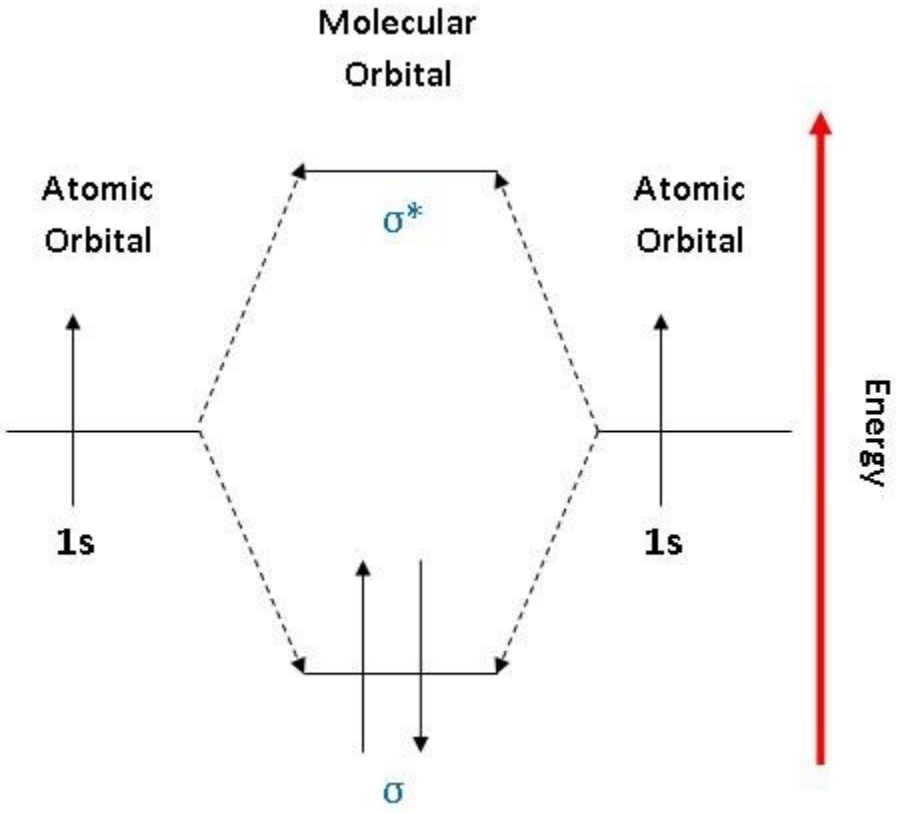


Figure 2.1 Energy level diagram showing the resulting bonding (σ) and anti-bonding (σ*) states created by combining two half-filled 1s atomic orbitals. The electrons from the atomic orbitals move into the lower energy bonding state creating a bond between the two atoms.[17]

The system portrayed in Figure 2.1 is a simple case representative of bonding in H_2. When bonds involve larger atoms with more filled orbitals, capable of forming multiple bonds, as is the case for carbon atoms in organic small molecules and polymers, then orbital hybridization becomes a factor. When considering carbon bonds, the s- and p-orbitals hybridize to form sp^3, sp^2, and sp orbitals which are involved in single, double, and triple bonds respectively. A schematic of sp^2 hybridization is shown in Figure 2.2. A sp^2 hybridized atom has two of its three p-orbitals and one of its s-orbitals hybridized. When carbon forms a double bond with another carbon atom, a sp^2 hybridized orbital on one carbon atom overlaps linearly with a sp^2 hybridized orbital on the neighboring carbon atom forming a σ-bond. The remaining un-hybridized p-orbitals on the neighboring carbon atoms overlap in a parallel fashion forming a π-bond. The energy levels of the molecular orbitals resulting for a double bond are shown in Figure 2.2.

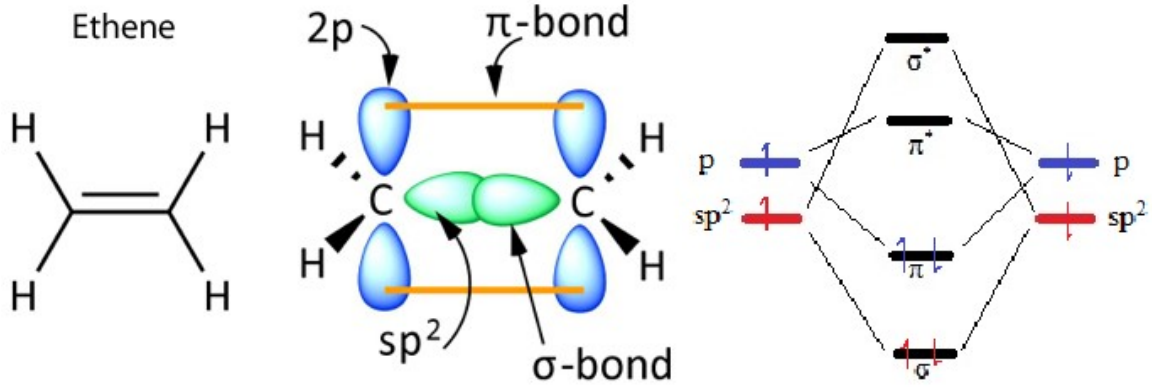


Figure 2.2 (Left) Structure of ethylene. (Center) Schematic of the carbon-carbon double bond of ethylene. The double bond is formed of two components: a σ-bond between the sp^2 hybridized orbitals of each carbon atom and a π-bond between the $2p_z$ orbitals. (Right) Schematic showing energy of the molecular orbitals resulting from the carbon-carbon double bond.[18]

The π-bonding state is the highest energy level state filled with electrons and so is called the highest occupied molecular orbital (HOMO) which can be thought of similar to the valence band of inorganic semiconductors. Conversely, the π^*-anti-bonding state is the lowest energy state without any electrons in it and is called the lowest unoccupied molecular orbital (LUMO), which is similar to a conduction band in inorganic semiconductors.

Sp^2 hybridization is of particular importance due to the ubiquity of conjugated double bonding in organic semiconductors. As shown in Figure 2.3, in a system with conjugated double bonds the p-orbitals of carbon atoms overlap with both of the p-orbitals of the neighboring carbon atoms forming a continuously connected network. Any electrons within this network are free to delocalize across carbon atoms, which allows charge to move easily through the system. This is the key structural property that allows organic semiconductors to conduct charge.

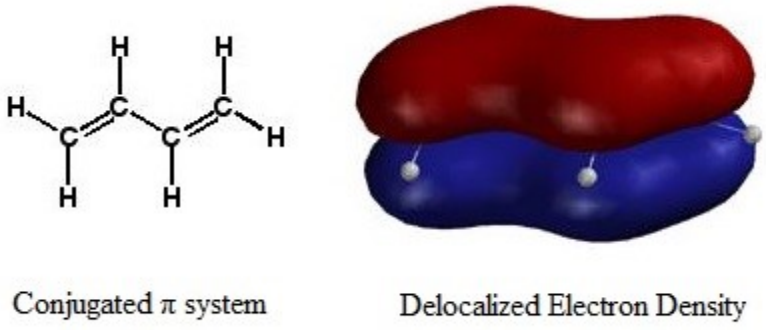


Figure 2.3 Conjugated structure of butadiene and electron density of butadiene π system. The π bonds on neighboring carbon atoms overlap forming a continuous network over which π electrons may delocalize and move freely.[19]

2.1.2 Electronic Structure of Organic Semiconductors

As discussed in the previous section, when two atoms or molecules form a bond, new orbitals with distinct energies are created including the HOMO and LUMO. The origin of these two states has its roots in the Paul exclusion principle, which states that two or more identical fermions (in this case electrons) cannot occupy the same quantum state. Practically this means that when two atomic orbitals combine, they split energetically such that each quantum state has a discrete energy. The difference in energy between the HOMO and LUMO states will be referred to as the band gap. The band gap for an isolated molecule, however, is different than the band gap for a molecular solid with a large number of molecules bonded together. When a large number of molecules are bonded together, a huge number of energy states are created, each with discrete energy, to accommodate the increased number of electrons as seen in Figure 2.4.

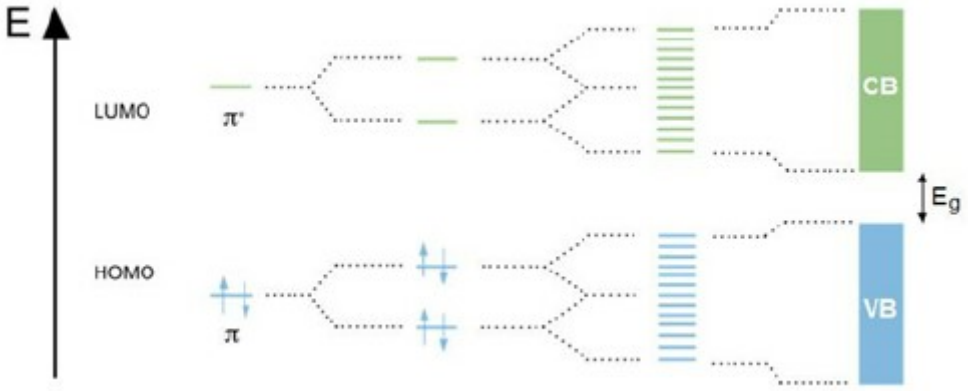


Figure 2.4 Energy band formation due to splitting of molecular orbital energy levels as a result of the Pauli exclusion principle.[20]

Due to the large number of molecules in the solid, the spacing between one energy level and the next is extremely small. The result is a near-continuity of energy states referred to as an energy band. The continuity of states below the HOMO in energy are referred to as the valence band, and the continuity of states above the LUMO in energy are referred to as the conduction band.

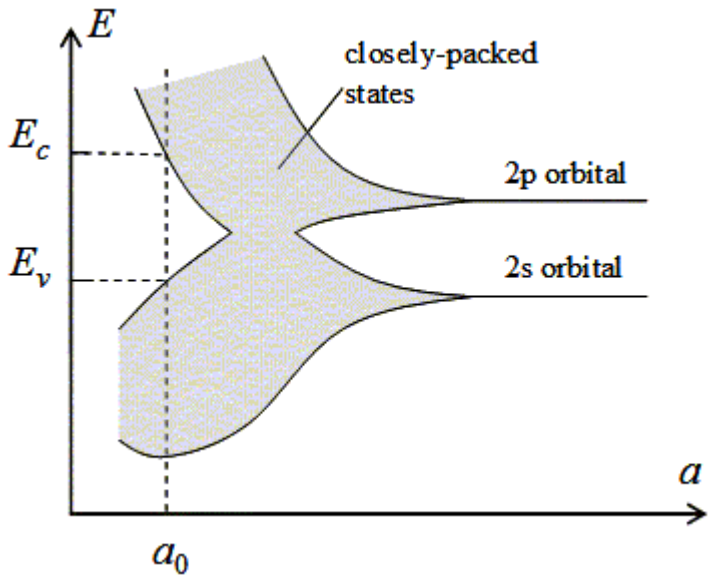


Figure 2.5 Energy of molecular states as a function of interatomic spacing, ***a***. When ***a*** is large, atoms are isolated from one another and can maintain states of equal energy. As ***a*** shrinks the orbitals of the atoms begin to overlap and the Paul exclusion principle comes into effect splitting energy levels more and more as orbital overlap increases and leading to the formation of energy bands.[21]

The bandwidth is the difference in energy between the highest energy state within a band and the lowest energy state within a band. As shown in Figure 2.5, bandwidth increases as neighboring atoms get closer together. This is because the overlap of neighboring orbitals increases, which increases the magnitude of energy splitting that

occurs. Increased overlap of neighboring orbitals also serves to increase the delocalized nature of electrons in the system by facilitating transfer of electrons between host atoms/molecules. Covalently bonded inorganic semiconductors have band widths on the order of 1+ eV while Van der Waals bonded organic semiconductors have band widths on the order of 500 meV. The large difference in band widths is indicative of the difference in inter-atomic/molecular orbital overlap in these systems (as well as the strength of the interactions). Single crystalline silicon has a Si-Si bond length of 2.3 Å while the inter-layer spacing of rubrene (the highest mobility organic semiconductor known) is 3.63 Å. The difference in overlap of orbitals with neighboring atoms/molecules is one of the factors that contributes to the difference in mobility between an inorganic semiconductor like silicon ($\mu_e > 1000$ cm^2/Vs) and an organic semiconductor like rubrene ($\mu_h \sim 20$ cm^2/Vs).

2.1.3 Polarons

Though the degree of orbital overlap plays a significant role in charge transport, polaron formation is another significant factor. Polaron formation intrinsically occurs in electrical materials simply by having excess charge (electrons or holes) in the system. As shown in Figure 2.6, excess charge polarizes the electron clouds on nearby atoms creating an attraction between the charge and the surrounding atoms. This attraction distorts the crystal lattice around the charge carrier. This lattice distortion follows the charge as it travels through the semiconductor. A polaron refers to the combination of the charge carrier and the lattice distortion of the charge carrier.

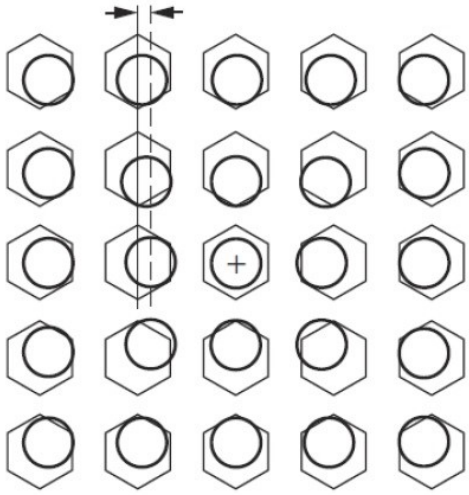


Figure 2.6 Polaron formation caused by a positive charge polarizing neighboring atoms and distorting the crystal structure nearby.[22]

Polarons come in two varieties, large and small. Large polarons have dimensions that are larger than the lattice constant of the material while small polarons have dimensions on the order of or smaller than the lattice constant of the material. Small polarons are typically found in inorganic materials. This is due to both a combination of bonding and dielectric constant. Because of the large dielectric constant in inorganic materials, electric fields are generally screened over a short distance and only the closest neighboring atoms will be polarized significantly. Additionally, the stronger covalent or ionic bonds in these materials do not distort significantly. Large polarons typically form in organic semiconductors both due to the small dielectric constant (less electric field screening) and the presence of weak Van der Waals bonds. Large polarons and small polarons are referred to as Fröhlich and Holstein polarons respectively. They are named after Herbert Frölich (who developed a Hamiltonian for large polarons) and Theodore Holstein (who developed a Hamiltonian for small polarons).[23-29]

2.1.4 Band Transport

Charge transport in semiconductors generally comes in two types, band transport and hopping transport. This section covers the fundamentals of band transport. Band transport generally refers to the condition when charge carriers are delocalized over a large range (across many atoms/molecules/lattice constants). The simplest model of band transport is the Drude model. The Drude model describes the motion of an electron moving through a solid in terms of how often it scatters and how quickly it is travelling. Scattering is caused by defects like vacancies in the crystal lattice, impurities in the crystal lattice and phonons. The Drude model essentially models electrons as hard spheres and scattering sites as hard spheres and then explains how the electron moves through such a system while being pulled along by an electric field. This setup is illustrated in Figure 2.7.

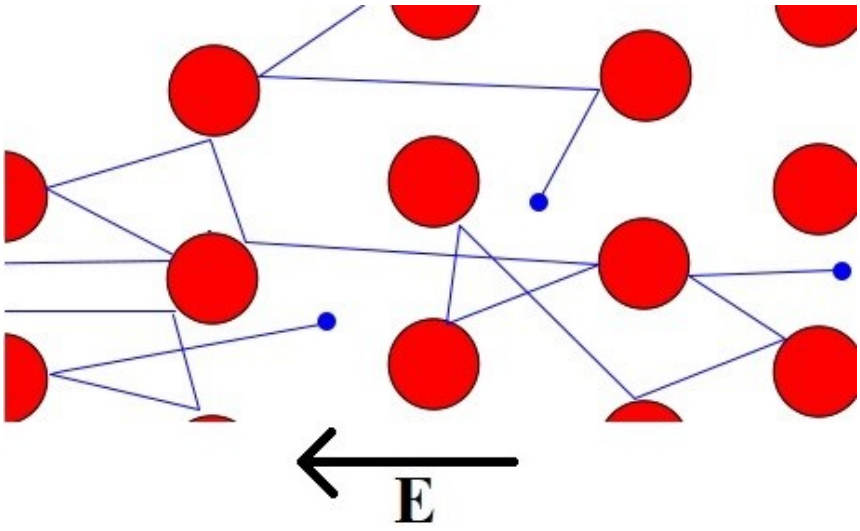


Figure 2.7 Representation of the Drude model with electrons (blue) scattering off localized impurities (red). The speed of the electron is a function of electric field, the number of scattering sites, and the effective mass of the electron in the material.

The speed of an electron travelling through such a system scales linearly with the electric field strength (up until the point of saturation). How strongly the speed of a charge carrier scales with electric field is quantified as the mobility of the charge carrier, μ. Mobility is a function of the time between scattering events in the material (which is indicative of the density of scattering sites within the material) and the effective mass of the charge carrier in the material (which determines how quickly the charge accelerates after a scattering event). The charge carrier mobility in the Drude model can be written as:

$$\mu = \frac{e\tau}{m^*} \tag{2.1}$$

where e is the elementary charge constant, τ is the mean time since the last scattering event, and m^* is the effective mass of a charge carrier in the material.

The temperature dependence of μ is a bit obfuscated at first glance; however, it lies within the τ term, which itself quantifies scattering events. Furthermore, the temperature dependence of μ also is dependent upon which type of scattering is dominant in the system. Scattering due to ionized impurities is one common scattering mechanism. The strength of a scattering event is based off the duration of the coulombic interaction between the charge carrier and the charged impurity. A charge carrier that is moving faster interacts for a shorter amount of time with an ionized impurity and experiences a weaker scattering event. Increasing temperature increases the thermal velocity of the charge carriers; therefore, mobility is directly proportional to temperature, specifically $\mu \propto T^{3/2}$. Phonon scattering is another common type of scattering event. Because the number of phonons (and hence scattering sites) increases with increasing temperature, the phonon-dependent

component of μ is inversely proportional to temperature. The exact correlation is a bit complex due to the existence of both acoustical and optical phonons each with its own temperature dependence. Both phonons play a role in transport; however, the size of the role each plays is dependent on the crystal lattice and hence the material. The exact temperature scaling of μ with temperature is therefore material dependent. Typical dependencies are $T^{-2.4}$ for electrons in Silicon, $T^{-1.7}$ for electrons in Germanium, and $T^{-1.0}$ for electrons in Gallium Arsenide.

The band model is usually applied to highly ordered systems with low defect and impurity densities. As such, mobility in systems exhibiting band transport is dominated by phonon interactions and is inversely proportional to temperature (mobility increases as the device is cooled). Such a temperature dependence is said to be indicative of band transport. Though this temperature behavior is common in inorganic semiconductors, a few organic semiconductors also exhibit a mobility that is inversely proportional to temperature.[30-31] Whether an organic semiconductor can truly be referred to as having band transport is still unclear though. A very high mobility organic semiconductor ($\mu \sim 20$ cm^2/Vs) has a mean free path on the order of a nanometer. Given that the lattice constant of many of these molecular materials is also on the order of the nanometer, the charge carriers do not appear to be delocalized much past one unit cell compared to inorganic semiconductors where a charge can be delocalized across many unit cells. Given this distinction, transport in organic semiconductors that exhibit a mobility that is inversely proportional to temperature is often referred to as "band-like" transport rather than true band transport.

2.1.5 Hopping Transport

Hopping transport arises from the localization of a charge on a given atom or molecule. Localization of charge can occur either due to poor orbital overlap of neighboring sites or a high degree of disorder in the system from impurities and defects.[32] Because the electrons are localized to a given atom or molecule, in order to conduct the electron must hop between individual sites. Due to the high disorder in the system and resultant breakdown of a continuous energy bands, there exists large energy differences between nearest neighbor states. In order to hop to a neighboring state of higher energy, the charge carrier must become thermally activated. Materials conducting via hopping transport therefore have a mobility that increases with increasing temperature. The simplest representation of thermally activated transport is an Arrhenius relationship:

$$\sigma \propto \exp(-E/k_bT) \tag{2.2}$$

Nevill Mott expanded upon this simple nearest neighbor hopping model by also including conduction contributions from distance-related tunneling phenomena.[33] This model is called the variable range hopping model and exhibits the following dependency:

$$\sigma \propto \exp(-T^{-1/4}) \tag{2.3}$$

2.2 Organic Field Effect Transistors (OFETs)

Field effect transistors form the basis of nearly all modern electronics. They function as on-off switches that are used to construct logic gates that are the foundation of modern computation. This chapter focuses on the basics of transistor structure, operation, and characterization.

2.2.1 Transistor Structure

A transistor is a device that modulates the conductivity between two electrodes (called the source and drain) by controlling the amount of charge in the semiconducting channel with application of voltage at a third electrode called the gate.

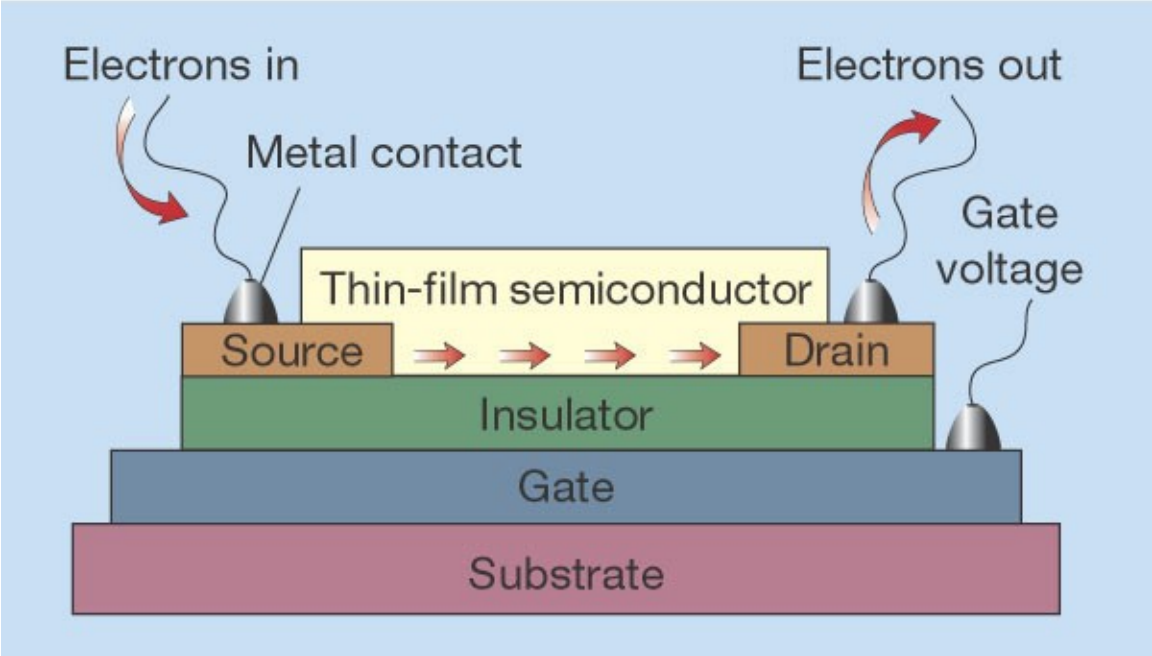


Figure 2.8 Side-view schematic of a typical thin film transistor (TFT). Key components include a semiconducting channel, three electrodes (Source, Drain, and Gate), and a dielectric layer used to inject charge into the semiconductor.[34]

A schematic of a transistor is shown in Figure 2.8. In particular, the transistor in Figure 2.8 is a thin film transistor (TFT), which means it uses thin layers of materials deposited upon an insulating substrate. Thin films can be deposited by a wide variety of methods including vapor deposition, sputtering, spin coating, and printing. TFTs are of interest here as organic semiconductors, in practical applications, will almost always come in the format of a thin film rather than a freestanding single crystal like a silicon wafer. There are many reasons why this is; however, cost is a significant factor. As mentioned in chapter 1, one of the biggest drivers of organic semiconductor research is the production of cheap electronics utilizing novel manufacturing methods such as aerosol and inkjet printing and roll-to-roll manufacturing. All of these manufacturing methods involve the deposition of a thin layer of organic semiconductor onto a cheap insulating substrate (flexible plastic or otherwise).

2.2.2 Charge Injection

As stated in the previous section, the primary mechanism governing the conductivity of the semiconducting channel is the accumulation or depletion of charge via application of a voltage at the gate electrode. A schematic of this process can be seen in Figure 2.9 for a simple metal-insulator-semiconducting capacitor (which is an integral subcomponent of a transistor). When materials are brought together in absence of an external electric field, electrons or holes flow between the materials until the Fermi energies are brought into alignment. In other words, in equilibrium, the Fermi energies of any two materials in contact are equal assuming no potential is applied to the system. If a

potential is applied to the metal relative to the semiconductor, however, the Fermi energy of the metal shifts according to the magnitude of the potential. The Fermi energy in the semiconductor remains fixed; however, the position of the energy bands near the oxide interface bend in the presence of the potential. If the potential applied at the metal electrode causes the bands to bend upwards near the oxide-semiconductor interface, then it becomes energetically favorable for holes to accumulate in the upward bend of the valence band. If instead the potential applied at the metal causes a downward bending of the energy bands at the oxide-semiconductor interface then electrons will preferentially accumulate in the conduction band as it is energetically favorable for them to do so. It is this process of energy band bending (or HOMO/LUMO shifts in the case of organic semiconductors) that allows application of a gate bias to modulate the number of charges in the semiconductor.

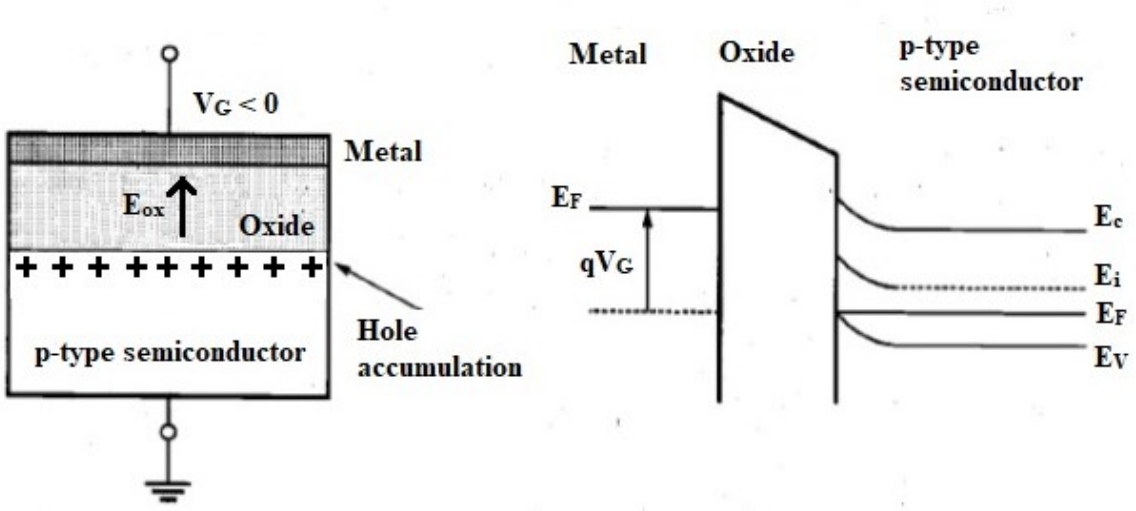


Figure 2.9 Charge accumulation and band bending in a semiconductor-insulator-metal capacitive structure. When a voltage, V_G, is applied to the metal electrode, the Fermi energy in the metal shifts relative to the Fermi energy in the semiconductor causing band bending and charge accumulation in the semiconductor near the oxide interface.

The relationship dictating how much charge is injected into the semiconductor via a gate bias is simply determined by the relationship $Q = CV_G$ where Q is the number of coulombs of charge in the semiconductor, C is the capacitance of the dielectric layer, and V_G is the bias applied at the gate relative to the semiconductor. This can be expressed in a more useful intrinsic (per unit area) form as $p = C_iV_G/e$ where p is charge density in the semiconductor, C_i is the specific capacitance of the dielectric, and e is the elementary charge constant. In a solid dielectric, like silicon dioxide, C_i is a function of the thickness of the layer as well as the dielectric constant of the material.

2.2.3 Electrical Characterization

The primary electrical characterization performed on a transistor is called a transfer curve measurement (Figure 2.10). A transfer curve measurement involves measuring the drain current, I_D, while linearly sweeping the gate voltage, V_G. This measurement characterizes how the conductivity of the channel varies as a function of the gate voltage. If the drain voltage (V_D) is much less than the gate voltage ($V_D << V_G$) the device is said to be in the linear regime. In the linear regime, the gradual channel approximation is valid, which states that the charge density along the semiconducting channel is essentially constant as shown in Figure 2.11. In the linear regime, drain current has the following relationship:

$$I_{D,Linear} = C_i\mu_{Linear}V_D[(V_G - V_T) - \frac{V_D}{2}]\frac{W}{L} \quad (2.4)$$

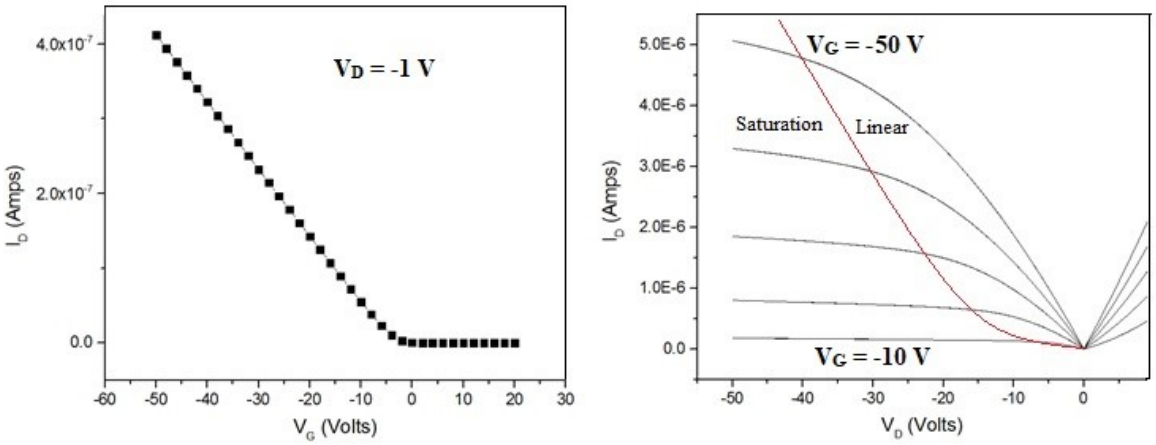


Figure 2.10 (Left) Transfer curve (I_D – V_G relationship) of a rubrene single crystal air gap transistor at low drain voltage. (Right) Output curves (I_D – V_D relationship) of the same device at different gate voltages. The red curve shows the onset of saturation.

where $I_{D,Linear}$ is the drain current measured in the linear regime, C_i is the specific capacitance of the dielectric layer, μ_{Linear} is the charge carrier mobility in the linear regime, V_D is the drain voltage (relative to a grounded source electrode), W and L are the width and length of the semiconducting channel respectively, and V_T is the threshold voltage of the device. Threshold voltage is the voltage at which conductivity begins to increase rapidly. In other words, it is the voltage at which the device truly begins to "turn on". In practice, threshold voltage is usually estimated by a linear extrapolation of the drain current to the gate voltage axis. The point of intersection with the axis is the estimation of V_T. Quantitatively, threshold voltage is the point when there exists some finite amount of free charge, Q_0, in the semiconducting channel. The number of free charges is affected by a wide number of factors. Most obviously, the number of free charges is affected by the voltage on the gate and capacitance of the dielectric as discussed previously. There are other relevant factors though including the difference between the Fermi energy in the

semiconductor and work function of the gate electrode, charge traps (like ionized impurities), atmosphere, temperature, and even the presence of light during measurement. For simplicity of example, let Q_0 = 10 q where q is a single charge carrier. Then threshold is reached when 10 free holes are accumulated in a p-type semiconductor. Then let us assume the following scenario, the work function-Fermi energy difference contributes 3 q into the system and charge traps consume 2 q of any injected charge. In this scenario, to reach threshold we need 10 q – 3 q + 2 q = 9 q of additional charge. If we assume all the remaining charge comes from gate voltage and assume each -1 V of gate voltage gives 1 q of charge then V_T = -9 V for this device. If we now assume for a different device our growth conditions were slightly different and so have more traps that now consume 4 q of charge then we need 10 q – 3q + 4 q = 11 q of charge to reach threshold meaning that V_T = -11 V for this device. Because there are so many factors that can affect the amount of free charge in a device, threshold voltage can shift significantly between two seemingly similar semiconductor devices if fabrication and testing conditions are not rigorously controlled.

Differentiating equation (2.4) with respect to gate voltage yields the transconductance, g_m:

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu_{Linear} C_i V_D \frac{W}{L} \tag{2.5}$$

Rearranging equation (2.5) we can solve for the mobility in terms of the slope of the transfer curve ($\partial I_D / \partial V_G$):

$$\mu_{Linear} = \frac{\partial I_D}{\partial V_G} \frac{L}{C_i V_D W} \tag{2.6}$$

In the case where $V_D >> V_G$, the device is said to be operating in the saturation regime. In the saturation regime, the gradual channel approximation breaks down and charge density varies significantly between the source and drain electrodes. This is because the potential drop between the source and drain electrodes is now as large as or larger than the potential drop between the gate and drain electrode.

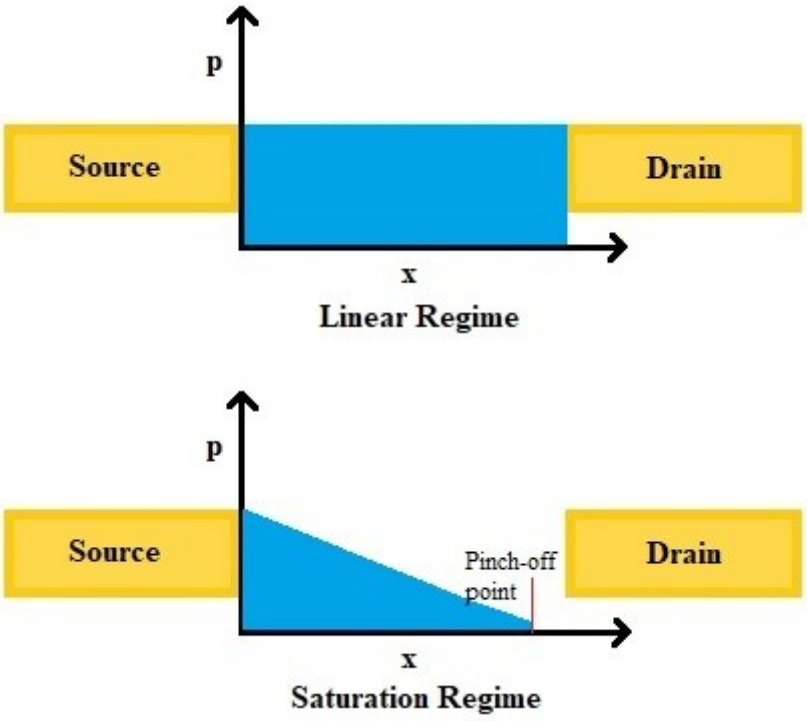


Figure 2.11 Charge density, p, as a function of the distance between the source and drain electrodes, x. (Top) Linear regime, $V_D << V_G$, with a near constant charge density across the semiconductor channel. (Bottom) Saturation regime, $V_G >> V_D$, where charge density decreases linearly across the semiconductor channel to a point of zero charge called the punch-off point.

The most unique phenomenon of saturation is the formation of a pinch-off point near the drain electrode. Beyond the pinch-off point, the charge carrier density induced by the gate voltage is zero. In the saturation regime, increasing the drain voltage leads to little

or no increase in drain current. In the saturation regime drain current has the following relationship:

$$I_{D,Sat} = \frac{\mu_{Sat} C_i}{2} \frac{W}{L} (V_G - V_T)^2 \tag{2.7}$$

Rearranging equation (2.7) yields the following relationship for μ_{Sat}:

$$\mu_{Sat} = \frac{2L}{WC_i} \left[\frac{d\sqrt{I_{D,Sat}}}{dV_G} \right]^2 \tag{2.8}$$

2.3 Organic Single-Crystal Field Effect Transistors (SC-OFETs)

As discussed in section 2.1, impurities and structural disorder can significantly affect charge transport by disrupting charge carrier delocalization and creating trap states that impede charge carrier movement. Thin films of organic semiconductors usually contain a large amount of impurities and structural defects in the form of entrapped solvent (if solution processed), grain boundaries, and vacancies. As such, thin-films of organics remain functionally useful; however, they pose a challenging system in which to study intrinsic charge carrier transport behavior due to the convoluting influences of impurity and structural disorder. Organic single crystals, on the other hand, provide a highly-ordered and high purity in which intrinsic transport can be studied with much more clarity. As such, much of the current research into organic semiconductor properties has been focused on organic single crystals.[7, 35-59] This section will cover the growth of single crystals, fabrication of devices using single crystals, and general characteristics of common single crystal organic semiconductors.

2.3.1 Single Crystal Growth

In general, single crystals of organic semiconductors can be grown using many of the same methods developed to grow single crystals of inorganic semiconductors. Namely these methods include solution growing, physical vapor transport, and melt growth processes like the Bridgeman and Czochralski methods. Which method is used for a give semiconductor depends upon a number of factors, and some methods aren't compatible with certain semiconductors.

Solution growing of single crystals is perhaps the most straight forward crystal growth method. The only particular requirement is that the organic material is fairly soluble in some solvent (typically organic and with a reasonable vapor pressure). A super-saturated solution of the organic material in the solvent is prepared and placed into a beaker or dish. The container is usually lightly covered such as to allow a slow and moderated rate of solvent evaporation. A small amount of heat can be applied depending on the solvent and desired evaporation rate. As the solvent evaporates, small crystals nucleate. Once crystal nucleation happens, much of the growth in the system tends to go towards growing the existing crystals rather than nucleating additional crystals. One permutation of this method is to force nucleation of the crystals not with solvent evaporation but with temperature changes. Solubility generally decreases with temperature. This can be exploited to grow crystals by preparing a saturated solution of the semiconductor at room temperature or slightly above and then slowly cooling the solution. As the temperature decreases, the solubility of the semiconductor in solution also decreases and crystals begin to nucleate.[60-62] Solution growth has the benefits of being relatively simple, easy to control,

and able to grow reasonably large crystals. Many crystal samples for X-ray crystallography are grown via solution. The downside of solution growth is that inevitably some amount of solvent is trapped within the crystal structure. As stated previously, electronic transport is extremely sensitive to disorder. Trapped solvent distorts the crystal structure and can significantly impact charge transport. Therefore, better electronic performance is usually obtained through other crystal growth methods.

Melt growth and/or zone refining methods are capable of producing ultra-pure single crystals of very large size making semiconductors grown via these methods particularly high performing and desirable. These types of processes are the same ones used to grow the extremely high purity, high quality wafers of silicon and other inorganics used throughout the semiconductor industry. In a melt growth process, like the Czochralski method, the whole of the semiconductor material (and any desired dopants) is melted in a crucible or ampoule. A seed crystal is then used as the starting point of crystal growth that proceeds due to a very gradual temperature gradient in the system. One variant of this process, the Bridgeman method[63], has been used to grow a number of organic semiconductor materials including naphthalene,[64] tetracene,[65] anthracene,[66] and pyrene.[60] Zone refining is a bit different of a process. During zone refinement, only a small portion of the semiconductor material is molten at any given time. This is typically done by moving the material (sealed in an ampoule) through a temperature gradient that increases slowly, reaches a peak temperature just above the melting point of the material in a very narrow region, and then slowly cools beyond this zone. The molten zone therefore proceeds slowly along the ampoule length. At any given moment there is a small molten

bit of crystal interfaced with a solid portion of the crystal. Generally, impurities tend to be more soluble in the liquid phase of the material than the solid phase of the material. Therefore as the molten region moves along the length of the ampoule, it tends to extract and drag away impurities with it. The impurities then all get concentrated toward one end of the crystal. The zone refinement process can be repeated multiple times to produce crystals of unparalleled purity.[67] Both the Bridgeman and zone refinement processes can be seen in Figure 2.12.

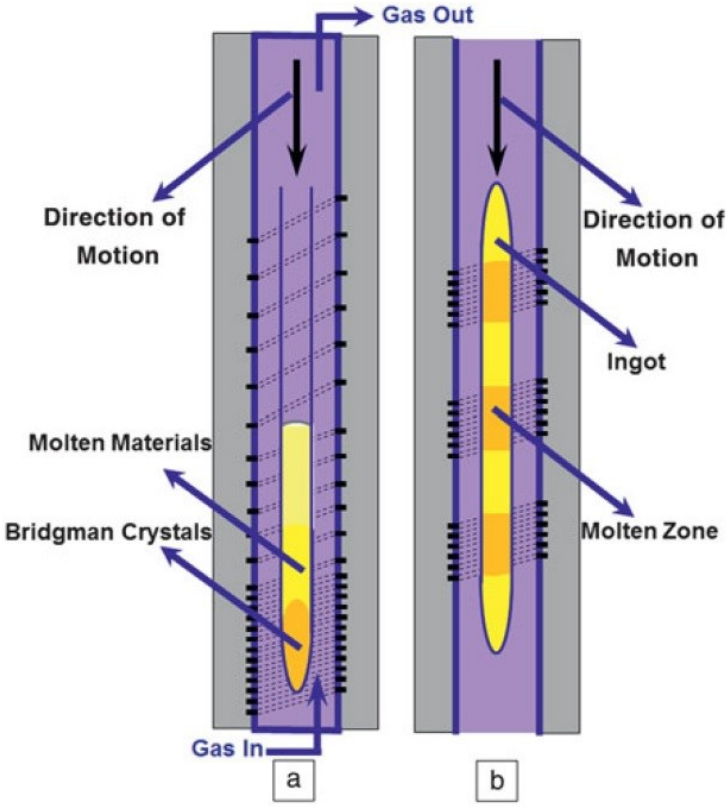


Figure 2.12 (a) Bridgeman growth and (b) zone refinement processes. Bridgeman growth focuses on a total melt and slow nucleation at one end via temperature gradient while the zone process melts only a small portion of the crystal at any given time.[60]

Though melt growth and zone refinement can produce extremely high quality crystals, it remains difficult to apply this growth method to many organic materials. Unlike inorganic semiconductors, organic semiconductors are inherently molecular in nature. While a semiconductor like silicon can be safely melted without any damage to the building blocks of the material (namely the silicon atoms), excessive temperature can readily break the bonds which hold the molecular building blocks of organic semiconductors together. This process is called thermal degradation. Therefore, for an organic semiconductor to be a suitable candidate for either melt growth or zone refinement, the molecules composing the material must be able to withstand temperatures in excess of the melting point of the crystal without changing or breaking in any way. This is a relatively difficult condition for many organic semiconductors to meet and so only a fraction of organic semiconductors can be grown using these processes.

Physical vapor transport (PVT) is a third method used to grow organic single crystals. PVT involves placing a source boat of organic material in a closed tube (often quartz or metal) and then heating the area around the source boat to create a significant amount of organic material in the vapor phase. The organic vapor is then pushed down a temperature gradient within the tube by a gentle flow of ultra-pure gas, usually H_2, N_2, or Argon. The cooling of the vapor causes the molecules entrained in the vapor phase to nucleate crystals that deposit on the walls of the substrate tube and continue to grow. PVT not only serves to grow crystals but also to purify material. Compounds are separated at different distances based upon their weights. With a properly set temperature gradient, heavier compounds than the target crystal will remain in the source boat (as they tend to

be less volatile) while less massive impurities will be pushed further down the tube before solidifying on the tube walls. Figure 2.13 shows a schematics of the PVT process.

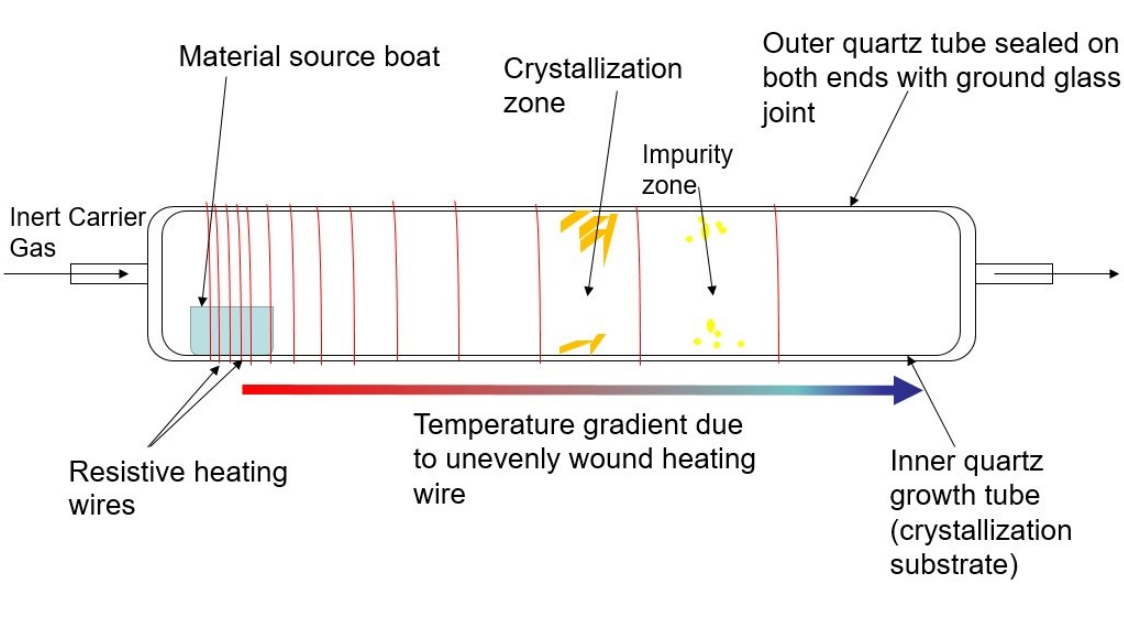


Figure 2.13 Schematic of the physical vapor transport growth method. Organic powder is heated to produce a large amount of vapor that is pushed down a temperature gradient causing the molecules entrained in the vapor to nucleate. The process also purifies the material as compounds deposit at different distances from the source boast based upon weight.

PVT produces high quality, purified crystals without the solvent entrapment of solution growth and at lower temperatures than melt growth as the melting point of the compound does not need to be reached. Because of this PVT is a growth method often used to make SC-OFETs. PVT, however, is not without drawbacks. The organic molecule must have a significant vapor pressure below its degradation temperature, which is not always a given. Furthermore crystal size can often be both small and highly variable compared to other methods. For the current benchmark organic semiconductor Rubrene, however, PVT growth works very well.

2.3.2 Fabrication of SC-OFETs

Though organic single crystals have intrinsically high order and purity, putting the crystal in a device that is able to measure the crystals properties is not without challenges. Namely, by placing the single crystal in a device architecture, significant disorder and impurities cannot be added into the system else the reason for using a highly ordered single crystal is defeated, because the transport properties will be dominated by the disorder from the other components of the device. Particularly troublesome areas are any location the single crystal interfaces with another material, as trap states can often form at interfaces. In the case of a SC-OFET, interfaces between the semiconductor and source/drain electrodes and the semiconductor and the dielectric need to be considered.

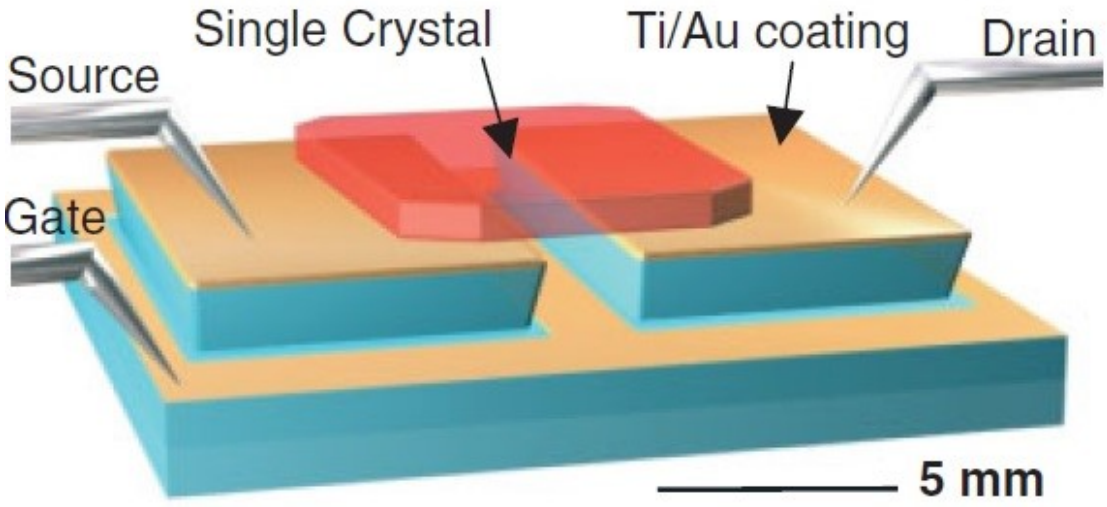


Figure 2.14 Schematic of a vacuum gap dielectric, single crystal organic field effect transistor. The substrate is polydimethylsiloxane (a rubbery material) coated with a thin layer of gold. Organic single crystals will readily laminate on the substrate due to Van der Waals interactions.[68]

One particularly high-performing SC-OFET geometry is the vacuum gap transistor shown in Figure 2.14. The most problematic interface (concerning the addition of charge

traps to the system) is the semiconductor-dielectric interface. In part this is because the semiconductor-metal interface is involved in a significantly smaller part of charge transport than the semiconductor-dielectric interface because the vast majority of the charge injection occurs right at the edge of the electrode but occurs over the full length of the semiconductor-dielectric interface. The vacuum gap transistor prevents the formation of trap states between two materials by simply not placing a dielectric material in contact with the single crystal. Vacuum is the dielectric in this device. Due to the low dielectric constant of vacuum, the capacitance of the device is lower than when using a different dielectric and larger voltages (tens of volts) must be applied to obtain the same charge densities. Given that these devices are primarily research tools, this is of little concern.

2.3.3 Charge Transport in SC-OFETs

As discussed in Section 2.1, one of the ways that the structure of organic semiconductors is unique compared to that of inorganic semiconductors is their molecular, rather than atomic, building blocks. As a result, organic semiconductors tend to have highly anisotropic (depends on direction) conductivity and charge carrier mobility when compared to inorganic semiconductors. As an example, consider the organic semiconductor rubrene (Figure 2.15).

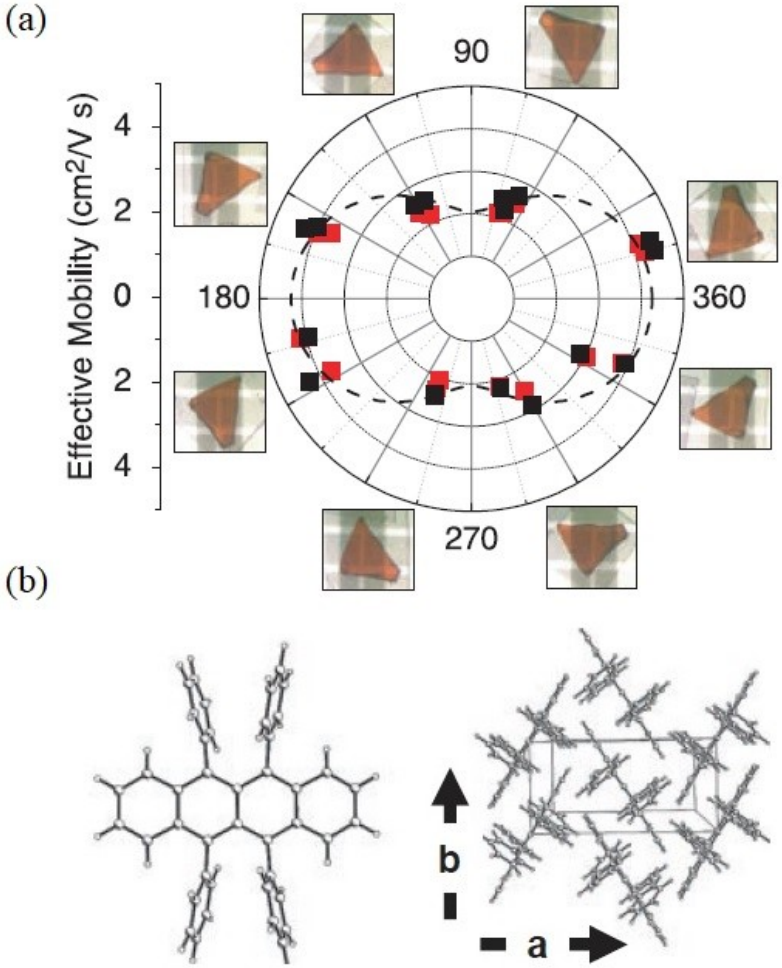


Figure 2.15 (a) Hole mobility in rubrene as a function of crystal orientation along transistor channel. (b) Molecular structure and crystallographic packing of rubrene.[69]

Rubrene consists of an aromatic, flat tetracene backbone with four side phenyl groups rotated perpendicular to the tetracene backbone. Rubrene packs in a herringbone pattern with and interlayer spacing of 3.6 Å. Each layer is also shifted about half the length of the molecule along the tetracene backbone. Conduction occurs primarily through overlapping pi-orbitals between adjacent rubrene layers along the b-axis as shown in Figure 2.15. In the b-direction, rubrene has a hole mobility up to 20 cm^2/Vs. Along the a-axis, orbital overlap is significantly minimized compared to the b-axis and hole mobility is about

five times lower along the a-axis. The c-axis (into the plane of the packing structure in Figure 2.15 (b)) has essentially no orbital overlap between neighboring layers of rubrene molecules. As a result, the hole mobility along the c-axis is 2-3 orders of magnitude lower than the hole mobility along the b-axis. Interestingly, there is often a correlation between crystal shape and mobility as the same structural features that promote charge transport tend to also promote crystal growth. This is evident in the shape of the often lathe-like rubrene crystals with a long b-axis, skinny a-axis, and very thin c-axis. Conversely, the more isotropic transport in dinaphtho-thieno-thiophene (DNTT) often yields a platelet type structure.

Though conductivity and charge carrier mobilities in organic semiconductors tend to be significantly lower than those of inorganic semiconductors, certain high performing organics are capable of achieving band-like transport. This has been confirmed in a number of ways including mobility temperature dependence measurements,[30] Hall effect,[40] ultraviolet photoelectron spectroscopy,[54] and infrared spectroscopy.[70-71] Example materials that exhibit band-like transport include rubrene (p-ytpe),[30] tetramethyltetraselenafulvalene (TMTSF) (p-type), and dicyanoperylene-3,4:9,10-bis(dicarboximide) (p-type),[72] (PDIF-CN_2) (n-type).[73]

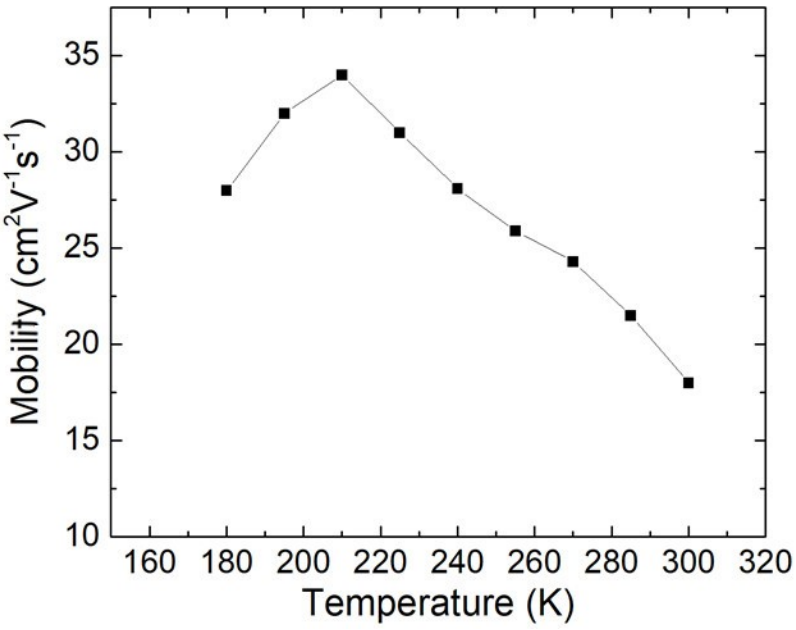


Figure 2.16 Temperature dependence of hole mobility for a rubrene SC-OFET. Mobility initially increases with decreasing temperature, indicating band-like transport. Eventually mobility begins to decrease with decreasing temperature indicating hopping transport due to increased effects from shallow traps.

In organic materials that do exhibit band-like transport, the behavior only holds over a finite temperature range as shown in Figure 2.16. In other words, below some critical temperature, carrier mobility begins to decrease with decreasing temperature indicating thermally activated transport. The explanation for this behavior can be found in the multiple trap and release (MTR) model, which states that shallow traps within a few tens of millivolts of the band edges become significant as thermal energy is removed from the system.[74] At room temperature, thermal energy is sufficiently high to release any charge carriers that fall into the shallow energy traps nearly instantaneously; therefore, charges effectively do not get stuck in the traps for any appreciable amount of time and mobility is unaffected. As temperature is decreased, there is less thermal energy in the

system and charges that fall into the shallow traps take significantly longer to thermally excite out of the trap. The effective mobility of the charge carrier is therefore lower, because its average speed is slower. Effective mobility can be expressed as the following:

$$\mu_{eff} = \mu_0 \frac{\tau}{\tau + \tau_{tr}} \tag{2.9}$$

where μ_{eff} is the effective hole mobility, μ_0 is the band-like mobility, τ is the time the charge is freely moving, and τ_{tr} is the time the charge spends in shallow traps. At high temperatures, μ_{eff} and μ_0 become effectively equal as τ_{tr} approaches 0. Conversely, at low temperatures, $\tau_{tr} >> \tau$ and we have $\mu_{eff} = \mu_0(\tau/\tau_{tr})$ which states that the effective mobility is directly proportional to the ratio of time the charge is moving compared to the time it is trapped.

Charge carrier mobility in SC-OFETs also exhibits a strong dependence on the dielectric constant of the dielectric material used in the device. Specifically, in rubrene SC-OFETs an inverse relationship between mobility and dielectric constant has been observed (Figure 2.17).[75] The mobility changes from 20 $cm^2V^{-1}s^{-1}$ in a vacuum gap device ($\varepsilon_r = 1$) to 1 $cm^2V^{-1}s^{-1}$ in a Ta_2O_5 device ($\varepsilon_r = 25$). Furthermore, vacuum gap devices exhibit band-like transport while higher dielectric constant gate insulators exhibit only thermally activated transport. The origins of this phenomenon are not well understood. One possible explanation is that the interface of a highly polarizable dielectric with a low polarizability organic can create Frölich polarons, which serve as a localizing force for the charge carriers.

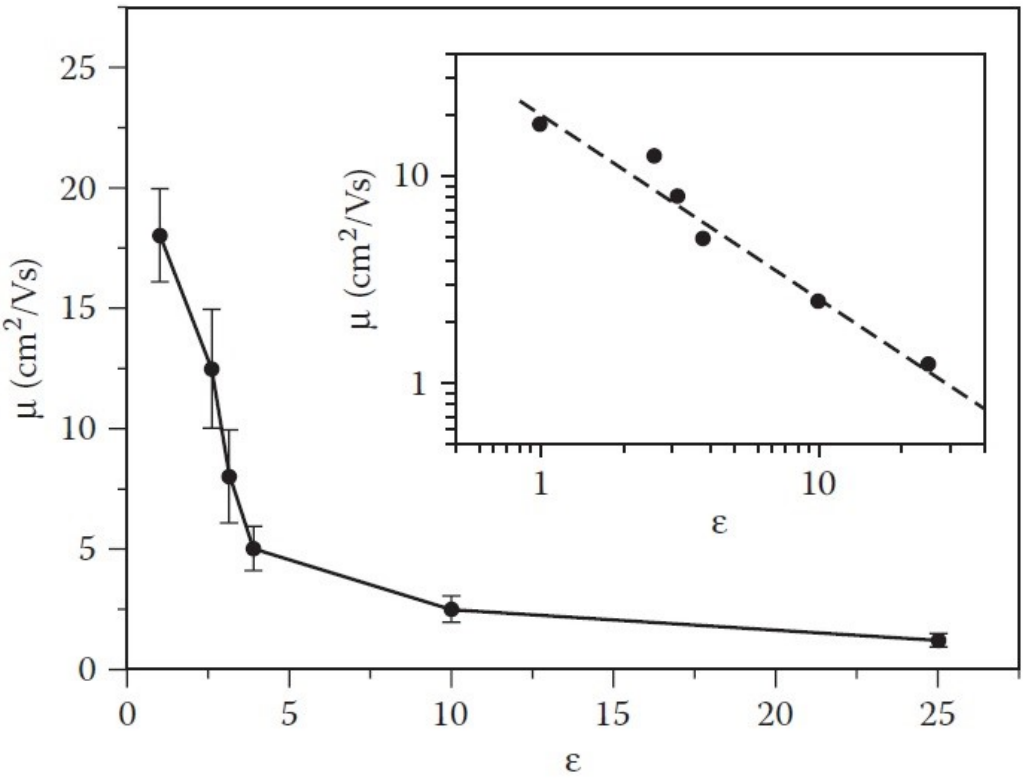


Figure 2.17 Effect of dielectric constant of the gate dielectric on the hole mobility in rubrene single crystal field effect transistors.[75]

Chapter 3: Electrical Double Layer Transistors

3.1 Principles of Electrolyte Gating

As discussed in Chapter 1, unique electronic phenomena like insulator-to-metal transistors and superconductivity are accessible in some materials simply by injecting extremely high densities of charge, on the order of 10^{13}-10^{15} charges per cm^2. Solid dielectrics typically are limited to charge densities of 10^{12} cm^{-2}. The use of very high-k ferroelectric dielectrics are capable of reaching charge densities on the order of 10^{14} cm^{-2}; however, the fabrication is complex, dependent upon substrate and/or semiconductor material, and fails completely in the presence of pin-hole defects.[76] To easily reach the required charge densities to see novel electronic phase behavior, the use of electrolytes (in particular ionic liquids) as gate dielectrics in OFETs has been employed in recent years. The resulting device is called an electrical double layer transistor (EDLT). This section explores the principles of electrolyte gating that allow EDLTs to reach extremely high charge densities.

3.1.1 Ionic Liquids

Room temperature ionic liquids (RTILs) are molten salts at room temperature. They are a liquid soup of positive and negative ions. If table salt (NaCl) were a molten at room temperature, it would be a RTIL. For simplicity, any further mention of ionic liquids refer specifically to RTILs. Unlike traditional electrolyte solutions (e.g. NaCl dissolved in water), which are also liquid soups of positive and negative ions, ionic liquids contain no solvent molecules. When completely pure, ionic liquids contain only positive cation

species and negative anion species. Common ionic liquid cations and anions can be seen in Figure 3.1.

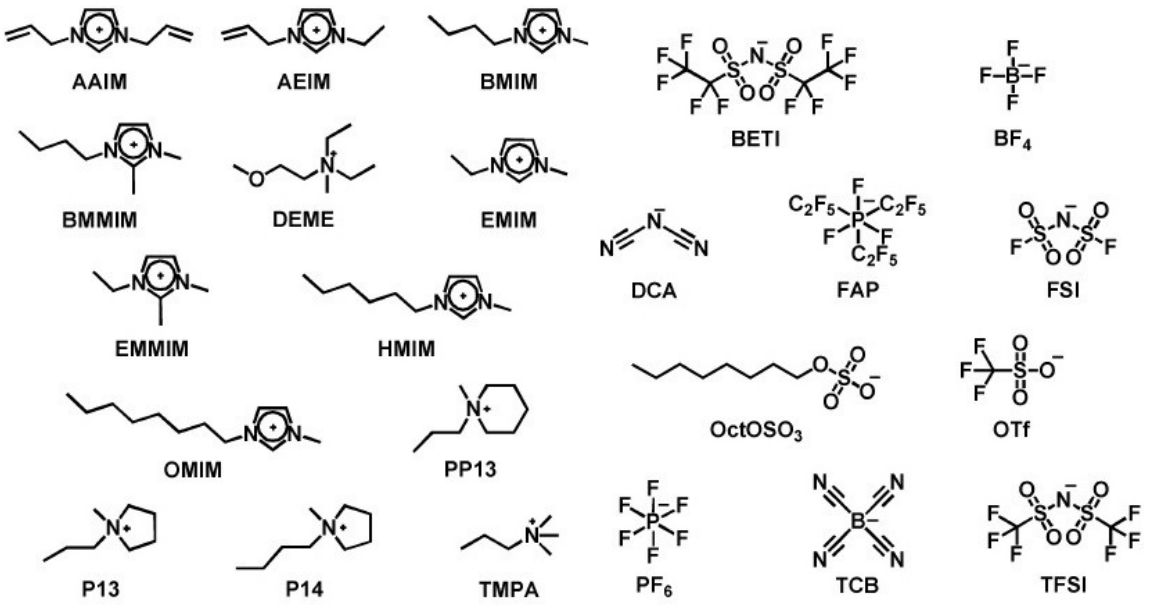


Figure 3.1 Common cations (left half) and anions (right half) comprising the most commonly used ionic liquids.[16]

Ionic bonding is generally a strong type of bonding with ionic solids often having high melting temperatures (T_m = 801°C for NaCl and T_m = 2852°C for MgO). To make an ionic compound liquid at room temperature, the coulomb interaction between the cations and anions needs to be significantly weakened. This is done effectively in two ways. The first way is to increase the distance between the cations and anions in solution as electric field strength decays with distance. To accomplish this, anions and cations in ionic liquids are usually quite large when compared to something like a sodium or chloride ion. Often the ions are organic and use long alkyl chains and tails as steric spacing units preventing the charge centers of the ions from drawing to near to one another as can be seen in many ions in Figure 3.1. The second way that bonding is frustrated is through symmetry. Highly

symmetric molecules have an easier time coordinating with multiple neighbors. Conversely, molecules of low symmetry cannot coordinated well with multiple neighbors. Melting temperatures can be suppressed by several hundred degrees Celsius by a simple symmetry lowering modification.

Ionic liquids have many desirable characteristics. Perhaps the most unique property ionic liquids possess is an extremely low vapor pressure. A microliter-sized droplet of ionic liquid may be placed inside a vacuum chamber for a month with seemingly no change in size. The low vapor pressure is the result of the strong ionic interactions that remain between cations and anions even though the material remains a liquid. The low volatility makes ionic liquids extremely appealing as green solvents to replace volatile organic compounds (VOCs) that cause health or environmental damage.[77] Ionic liquids also have a wide electrochemical window compared to many electrolytes, which also makes them desirable in many electrochemical applications. Specific capacitance in ionic liquids is similar to that of electrolytes, on the order of μFcm^{-2}, which is large compared to the $nFcm^{-2}$ specific capacitance of many thin solid dielectric layers. The combination of all three of these properties make ionic liquids particularly well suited for use in EDLTs.

3.1.2 Electrical Double Layer Formation and Structure

As mentioned in the previous section, ionic liquids have extremely high specific capacitances. The origin of the high capacitance is in the mobility of the ions. First, however, consider the case of a solid dielectric like silicon dioxide (Figure 3.2).

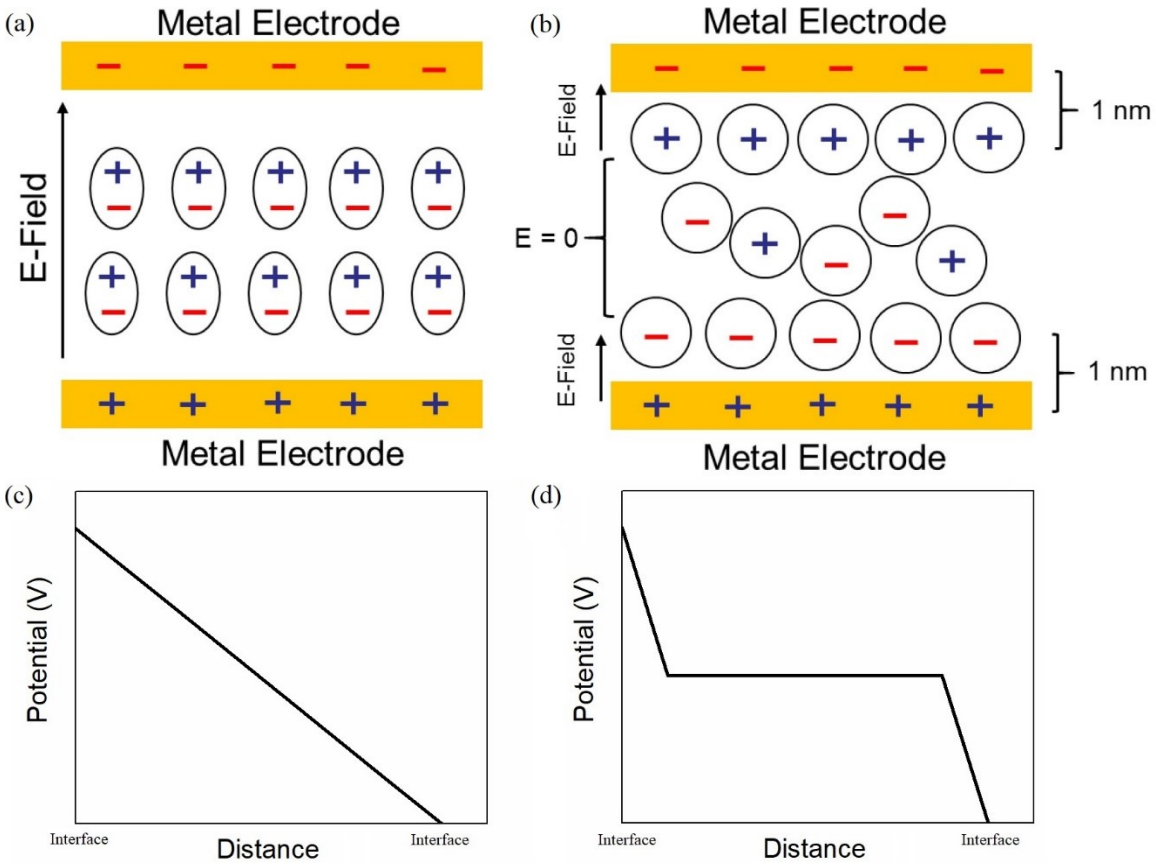


Figure 3.2 (a) Polarization of electron clouds in a solid dielectric under bias. (b) Electrical double layer formation in an ionic liquid under bias. (c) Potential as a function of distance from interface in a solid dielectric. (d) Potential as a function of distance from interface in an ionic liquid.

When a voltage bias is applied across a solid dielectric, the electrons move in response to the electric field leading to a polarization of the dielectric. The field of the resulting dipole minimizes the effective electric field in the device. The higher the

dielectric constant of the material, the lower the electric field strength, and the greater the amount of charge able to be stored on the capacitor. Assuming a simple parallel plate capacitor model, the electric field is constant at any point in the solid dielectric between the two metal plates. This means that the potential being applied across the two plates is being dropped linearly across the whole dielectric thickness as shown in Figure 3.2 (c). The gradient of the potential drop (i.e. electric field) is therefore proportional to the dielectric thickness; hence, capacitance is a function of dielectric thickness for traditional solid dielectrics.

Consider now the case of an ionic liquid dielectric. Unlike the electrons in silicon dioxide that are tightly bound to their host atom and only able to slightly polarize under influence of an electric field, ions in ionic liquids are fully mobile and able to move freely in response to an electric field. What occurs is the formation of what are called electrical double layers at each of the two interfaces as shown in Figure 3.2 (b). Electrical double layers are two layers of opposite charge spaced a short distance (~1 nm) apart. One layer of charge is comprised of charges in the electrode and the other layer is comprised of oppositely charged ions in the ionic liquid. As shown in Figure 3.2 (d), the potential across an ionic liquid dielectric is dropped only at the two interfaces (the amount of which is proportional to the relative areas of the two interfaces). This occurs because the mobile ions fully screen the charge in the bulk of the ionic liquid leading to there being no net electric field in the bulk of the ionic liquid and therefore no potential drop. An electrical double layer can crudely, for the point of illustration, be modeled as a parallel plate capacitor. The specific capacitance of a parallel plate capacitor is $C'=\varepsilon/d$ where ε is the

dielectric constant of the insulator and d is the spacing between the two plates of opposite charge. Because specific capacitance is inversely proportional to the spacing of the charge layers and the charge layers are only about 1 nm apart, the specific capacitance of electrolyte and ionic liquid systems is huge, on the order of μFcm^{-2} as mentioned previously.

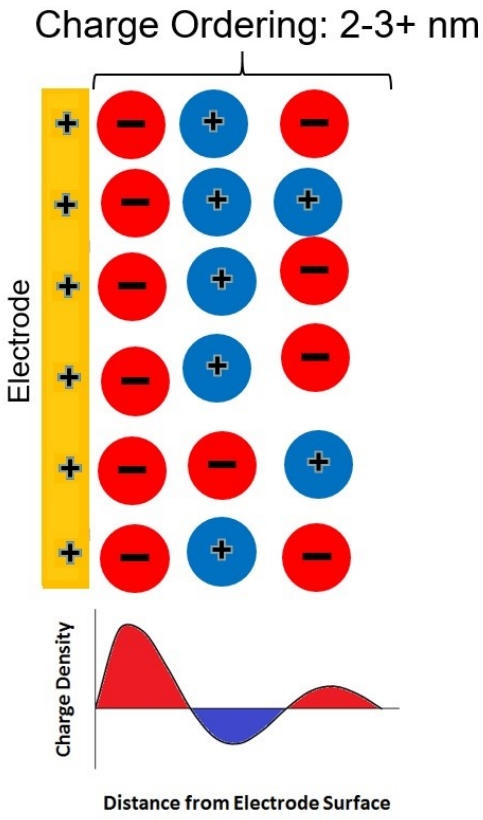


Figure 3.3 Ionic liquid double layer structure and associated net charge density as a function of distance from the electrode surface.

While the idea of a single layer of counter ions adhered to an electrode surface serves as a simple model, electrical double layers in ionic liquids are inherently more complex due to the extreme charge concentrations involved. A lot of recent work has gone

into trying to better understand ionic liquid double layer structure through methods such as X-ray diffraction, in-situ STM and AFM, and computational modeling.[78-85] The structural picture that has emerged from this work is represented in Figure 3.3. An ionic liquid electrical double layer actually consists of many layers ordered in a lamellar structure of alternating charge density that decreases in magnitude away from the electrode surface. The lamellar structure is on the order of a few nanometers thick (possibly more depending on the ionic liquid and the time scales involved).

3.1.3 Electrical Double Layer Device Structures

Ionic liquids can be used in several different device architectures as shown in Figure 3.4. Each architecture has advantages and disadvantages.

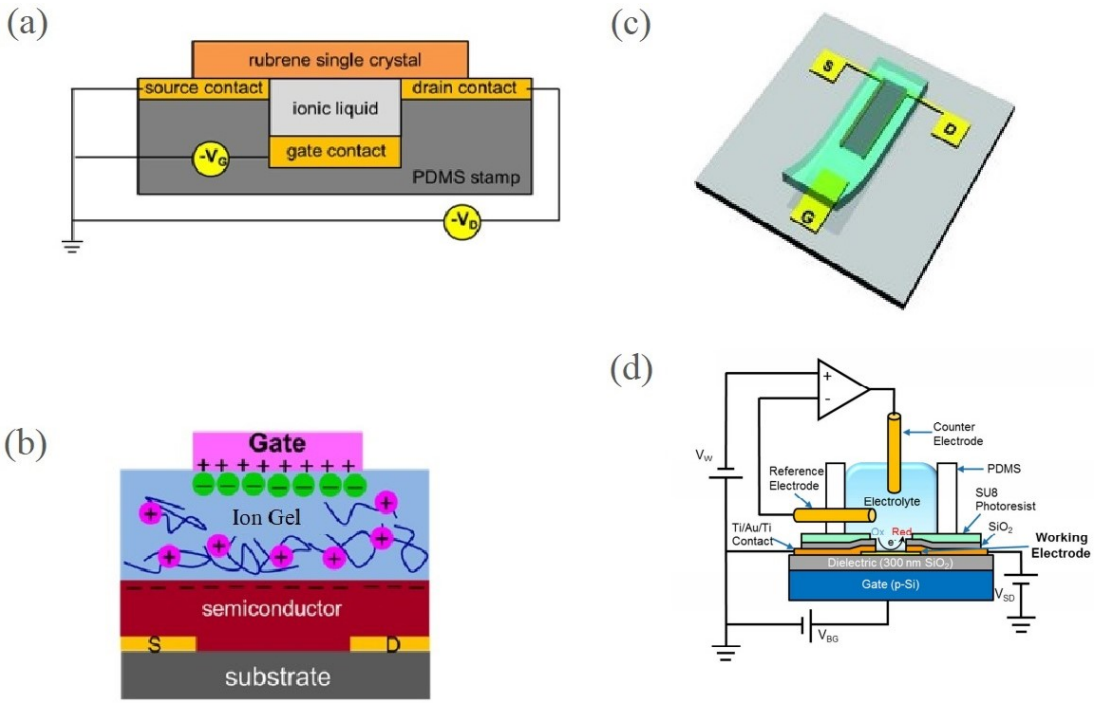


Figure 3.4 Different electrical double layer transistor device architectures. (a) Bottom gate using ionic liquid; (b) Top gate using ion gel; (c) Side gate using cut-and-stick ion gel; (d) Top (and bottom) gated using ionic liquid or electrolyte for use in an electrochemical cell.[44, 86-88]

Figure 3.4 (a) shows a bottom gated device using an ionic liquid dielectric layer. This type of device is commonly used when studying single crystal OFETs. A vacuum gap device, as shown in Figure 2.14, can easily be converted into this type of device simply by filling the vacuum gap with an ionic liquid. Fabrication of such devices is important to the work in this thesis and will be discussed in detail in chapter 4. One advantage of this architecture is being able to directly compare performance of an air/vacuum dielectric to that of an ionic liquid dielectric using the same crystal. This is possible as the gap between the semiconductor and gate is relatively small (~few μm) and therefore has enough capacitance to turn on the device even when using a vacuum dielectric. The other architectures in Figure 3.4 are incapable of turning on without the ionic liquid, and so the impact of the ionic liquid cannot be as accurately assessed. Another advantage of this architecture is that it greatly minimizes parasitic capacitance. Due to the high capacitance of the ionic liquid, any overlap of the ionic liquid with the source and drain electrodes creates a large parasitic capacitance. This architecture largely eliminates any possible contact of ionic liquid with source or drain electrodes and leads to lower parasitic capacitance than found in other architectures.

Figure 3.4 (b) shows a top gated device using an ion gel dielectric. Ion gels are a blend of polymer (~20 wt%) and ionic liquid (~80 wt%). Typically triblock copolymers (Figure 3.5) are used with the middle block being soluble in ionic liquid and the end blocks being relatively less soluble in ionic liquid. Ion gels give structure and rigidity to the formerly liquid material. One advantage to the architecture in Figure 3.4 (b) is that, unlike the device it 3.4 (a), it can be printed using ink jet or aerosol jet methods.[89] Use of ion gel

instead of ionic liquid is key as it allows a stable, solid surface on which to print the gate electrode that would otherwise penetrate an ionic liquid and short to the semiconductor. Another advantage is that the ion gel has a definite form and is not prone to move or run across the surface as opposed to a liquid dielectric. One disadvantage of this architecture is that ionic conductivity is reduced slightly in ion gels compared to the liquids due to the presence of polymer impeding ion movement. This translates to slower operating speeds. A second disadvantage is that parasitic capacitance is larger due to inevitable overlap of the ion gel and source/drain electrodes. The ion gel must be printed with a slight overlap of the electrodes to ensure the semiconductor is gated across its entire length. The parasitic capacitance is further compounded due to overspray of the printing nozzles.

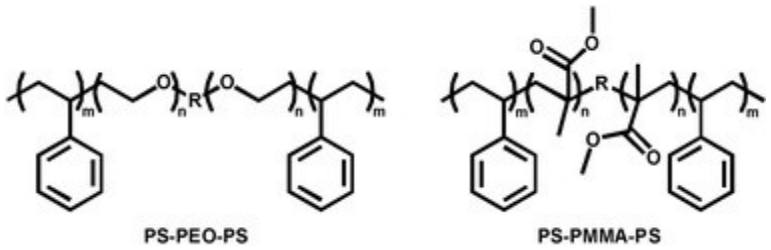


Figure 3.5 Commonly used triblock copolymers used to create gels of ionic liquids.

Figure 3.4 (c) shows a side-gated transistor using a cut-and-stick ion gel.[87] The main advantage to this architecture is its ease of fabrication. No special equipment is required to create an EDLT using this setup beyond a pair of tweezers and a razor blade. Electrodes can be placed on a semiconducting crystal or material using silver or graphite paint, a piece of ion gel (prepared simply by mixing ingredients in a petri dish) is then cut and placed carefully such that it overlaps the semiconductor and gate while minimizing overlap of the source/drain electrodes. Disadvantages of this architecture include lack of resolution when placing the gate dielectric and increased distance between the gate

electrode and semiconducting channel when using a side gate (as is common). In a top or bottom gate device, it is easy to place your gate and channel on the order of 1 μm apart; however, distances in side gate device are usually on the order of mm. As discussed in the last section, this increased distance will not affect the capacitance of the interfaces (as the potential is dropped only across the two interfaces); however, the increased distance greatly increases the ionic resistance of the dielectric leading to slower device performance.

The final device architecture, Figure 3.4 (d), shows a novel use-case of EDLTs as a charge-transfer modulator during electrochemical reactions.[88] In this setup, the semiconducting channel is gated both from the bottom (through a thin oxide dielectric) and from the top through the electrolyte via the potential difference between the working electrode (which is the semiconductor) and the counter electrode. This particular EDLT geometry shows promise in the field of catalysis as it allows for the reversible modulation of the energy bands allowing the energy bands to be aligned precisely with the targeted oxidation or reduction reaction. Charge transfer rates can be modified by over two orders of magnitude using this type of device.

3.2 Device Characterization

3.2.1 Figures of Merit

One of the most important figures of merit for an electrolyte, in regards to device performance, is the RC time constant. The RC time constant of an ionic liquid dielectric is the product of the resistance to ionic conduction and the capacitance. It represents the time required to charge the capacitive circuit to ~63%. If we rewrite the RC time constant in terms of intrinsic properties of the ionic liquid we have $RC = tC'/\sigma$, where t is the thickness of the dielectric, C' is the specific capacitance of the ionic liquid, and σ is the ionic conductivity of the ionic liquid. While the specific capacitance and ionic conductivity of the ionic liquid are very important, these components do not wholly determine the RC time constant in a capacitor as the resistance and capacitance are extrinsic properties that depend on device geometry and dimension. As the above equation indicates, the thickness of the ionic liquid layer is very important as the resistance increases linearly with increasing thickness; therefore, a very thin ionic liquid layer leads to a faster charging capacitor with no change in capacitance. Given typical values for ionic conductivity ($\sigma \sim 10^{-3}$ S/cm) and specific capacitance ($C' \sim 10$ μFcm^{-2}), sub-microsecond RC time constants (and therefore > 1 MHz operating frequencies) are theoretically possible in a well-constructed EDLT. Often actual performance is limited by other factors including parasitic capacitance caused by various non-idealities such as ionic liquid/ion gel overlap of the source drain electrodes. Parasitic capacitance increases capacitance and proportionally the RC time constant as well. Other non-idealities in the system that lower device operating frequency include slow

adsorption and desorption of ions on electrode surfaces, ion penetration into porous surfaces, and charge carrier mobility in the semiconductor.

A second figure of merit for electrolytes is the loss tangent, otherwise called dielectric loss or the dissipation factor. This quantity is defined as:

$$tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{3.1}$$

where ε′ and ε″ are the real and imaginary parts of the electrical permittivity and δ is the loss angle which characterizes, in an AC system, how far the phase angle between the current and voltage waveforms deviates from the ideal 90 degrees for a capacitor. Dielectric loss is typically only relevant in AC systems and specifically quantifies the energy dissipated through resistive means versus the energy stored electrically in the capacitor. The causes of this resistive loss can be many but are related to energy lost as heat generation from charges being displaced through a dielectric medium in response to a constantly changing electric field. Loss tangents are inherently higher in ionic liquid dielectrics (tanδ ~ 0.1) than conventional solid dielectrics (tanδ ~ 0.001) due primarily to the slow/resistive movement of ions through a charge medium compared to the comparatively less resistive electron cloud polarization.

A common way of analyzing dielectric loss in a circuit involves modeling a real capacitor as a series combination of an ideal lossless capacitor and a resistor called the equivalent series resistance. When taking this approach, loss tangent can be defined as:

$$tan\delta = \omega RC \tag{3.2}$$

where ω is the angular operating frequency of the device, R is the equivalent series resistance, and C is the capacitance of a lossless capacitor. It is important to note here that

the values of R and C do not necessarily directly translate to exact resistances or capacitance values within the circuit but serve as part of a model. Nevertheless increasing resistance or capacitance of the dielectric increase R and C in the model as well, and therefore it is possible to see that the RC time constant is also relevant in determining the dielectric loss in a device.

Realistically, an ionic liquid device cannot be characterized by a single RC time constant; a wide distribution of relaxation events are involved in the operation of an ionic liquid device with time scales spanning from microseconds well into seconds.[90] Rough electrode surfaces and slow ion adsorption and desorption events are likely contributors to this phenomenon.[91] A model providing insight into the time scales involved in ionic liquid devices is contained in chapter 5.

3.2.2 Charge Density Measurements

Charge density determination in inorganic FETs is relatively simplistic. It can often be well estimated simply by assuming the capacitive stack in the transistor behaves like a parallel plate capacitor (therefore $C = \varepsilon A/d$) and then using $Q = CV$, which in terms of charge density, p, is simply $p = CV/A$. The only real caution required is that ε is frequency dependent, and therefore the value used must be appropriate for the frequency domain of interest. Charge density in EDLTs is much more complicated to determine and cannot be easily estimated with a formula. The reason for this is that capacitance is not only highly frequency dependent in EDLTs but is also highly voltage dependent as well. Often capacitance in EDLTs is discussed in terms of differential capacitance:

$$C_{diff} = \frac{\partial p}{\partial V} \tag{3.3}$$

where C_{diff} is differential capacitance, p is charge density on the capacitor, and V is voltage across the capacitor. The capacitance's dependence upon voltage relates to how double layer structure changes as voltage increases. Differential capacitance actually reaches a minimum value at the point of zero charge (PZC)[92-93] as shown in Figure 3.6.

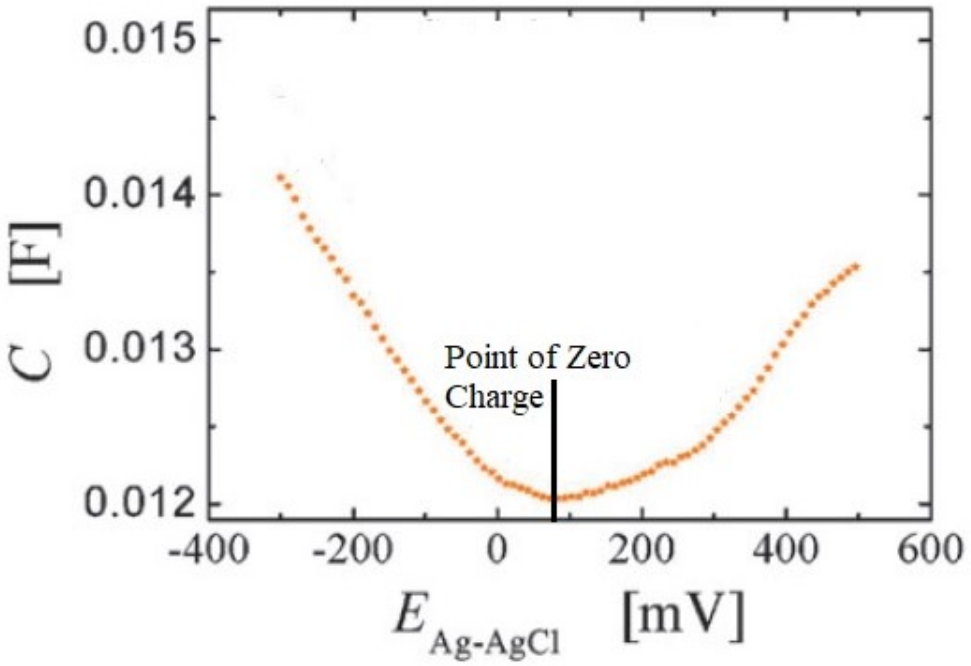


Figure 3.6 Differential capacitance as a function of potential versus a Ag-AgCl reference electrode for a 0.7M solution of NaF on a carbon aerogel electrode.[94]

To understand this phenomenon, potential of zero charge must first be understood. The potential of zero charge is fundamental to the concept of ion adsorption and depends upon both the electrolyte used as well as the composition of the electrode surface. When an electrode is immersed in an electrolyte, adsorption of ions occurs inherently. It is likely that either cations or anion preferentially adsorb to the surface more than their counter ion

and so a net charge density exists on the surface. It is important to note that both species are adsorbed but the quantity of anions versus cations adsorbed is different. The potential of zero charge is then the potential that needs to be applied to the electrode surface in order to bring the surface to charge neutrality. This is not to say that there are no more charges adsorbed but rather that the amount of positive and negative adsorbed charge is now equal. At the potential of zero charge, charges are not pulled strongly towards the surface and the average distance of a charge from the surface is therefore at a maximum. Assuming a simple parallel plate model, capacitance is inversely proportional to the separation distance of the charges; therefore, if separation distance is maximized at the PZC due to the weak potential felt near the surface, then the differential capacitance is minimized at this point.

Charge density can be measured in EDLTs using four different methods: step potential charging, impedance analysis, linear voltage ramp displacement current measurements, and Hall effect measurements.

Step potential charging, as seen in Figure 3.7, involves applying a sudden change in potential (a potential step) to the capacitor while measuring the current flowing to charge or discharge the capacitor. Step potentials are useful for determining the equilibrium charge density in a device in a static, DC state. Charge density is determined in this method by integrating charging current as a function of time (area under curve in Figure 3.7):

$$p = \frac{Q}{A} = \frac{\int Idt}{eA} \tag{3.4}$$

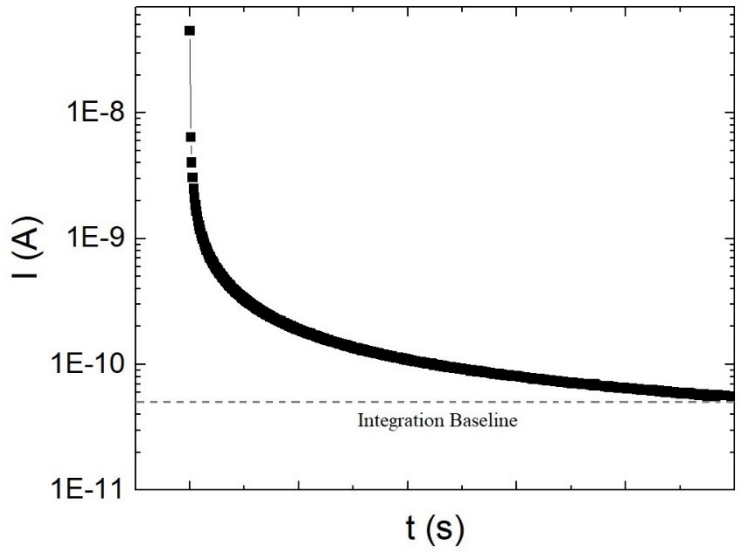


Figure 3.7 Charging current as a function of time for an Au/$[P14]^+[teFAP]^-$/Au capacitive structure in response to a step voltage.

Using an ideal dielectric, charging current exponentially decays with time according to:

$$I = I_0 e^{(-\frac{t}{RC})} \tag{3.5}$$

In a relatively ideal solid dielectric charge density can be calculated accurately and quickly by measuring charging current in response to a step potential for a few seconds, fitting the resulting data to equation 3.5 and integrating the fit with respect to time out to infinity. In the case of ionic liquids, charge determination by step potential is a much more time-intensive process as ionic liquids do not behave like ideal capacitors with exponentially decaying current. Charging current typically displays a very long, slowly decaying tail. As a result, to determine charge density, measurements need to be carried out over extended periods of time (tens of minutes or more) until current has decayed to a relatively flat plateau. This plateau value represents leakage current (current not contributing to charging the capacitor, such as leakage through a resistor in parallel with the capacitor) and is often

attributed to slow electrochemical phenomena. This leakage current value serves as an integration baseline that is subtracted from all measured currents before integrating using equation 3.4.

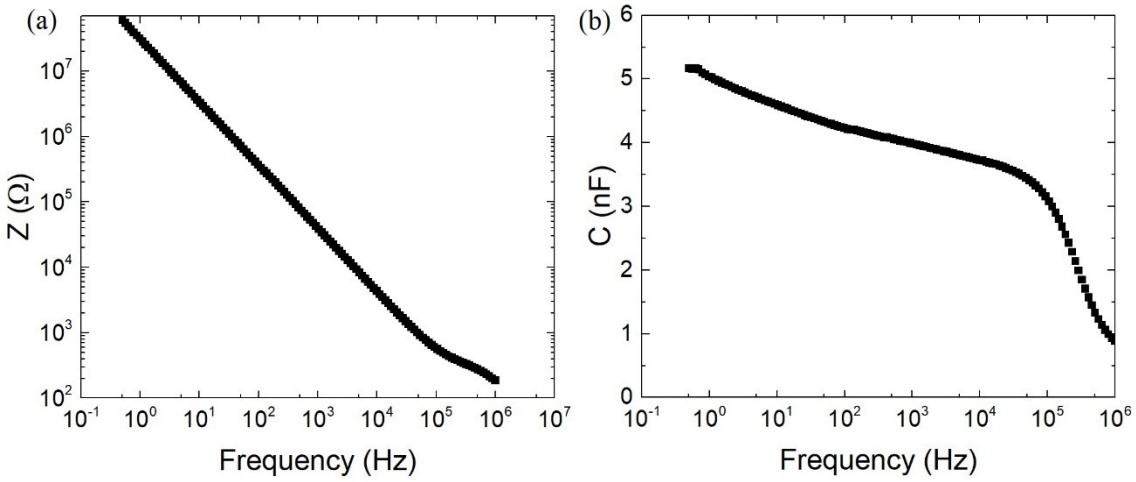


Figure 3.8 (a) Impedance as a function of frequency for an Au/$[P14]^+[teFAP]^-$/Au capacitive structure as determined by impedance analysis. (b) Capacitance as a function of frequency.

Impedance analysis serves as a second useful tool for analyzing charge density in EDLTs. Impedance analysis characterizes the AC performance of a device. In impedance analysis, a sinusoidal alternating voltage (superimposed on a DC voltage offset) is sourced to the device and the current is measured in response. In an AC system instead of V=IR we have V=IZ where Z is the impedance (AC analogue of resistance). The phase angle, ϕ, (phase shift in the voltage and current waveforms) is also tracked. The phase angle allows the total impedance, Z, to be broken down into its real and imaginary parts, Z' and Z'' respectively, according to the equations $Z'=\cos(\phi)|Z|$ and $Z''=\sin(\phi)|Z|$. Figure 3.8 (a) shows total impedance as a function of frequency for an ionic liquid capacitor.

Using impedance analysis, charge density is determined by characterizing the differential capacitance of the device over a range of frequencies and voltages rather than by integrating current. To determine capacitance from impedance and phase angle data, an equivalent circuit model must be assumed for the device. Typically a simple series R-C circuit is used to characterize EDLTs at low frequencies (< ~10 kHz). In a series RC circuit the following relationships hold:

$$Z' = R \tag{3.6}$$

$$Z'' = \frac{-i}{2\pi f C} \tag{3.7}$$

It is important to note here that R and C are effective device values only valid at a particular frequency; therefore, each frequency has a unique R and C associated with it.

Using equations 3.6 and 3.7, it is possible to take the impedance data from Figure 3.8 (a) and plot it in terms of effective capacitance as seen in Figure 3.8 (b). Of particular interest is the roll off in capacitance at high frequency. Capacitance decreases at high frequency as the field is switching so quickly that the ions can barely begin to move in one direction before the field changes direction and the ions are being pulled the opposite direction. Effectively ions stand still at high frequency and are no longer able to move to form a double layer. Ionic conductivity has a significant effect on the frequency at which the capacitance begins to roll off with low conductivity ionic liquids beginning to roll off near 1 kHz and high conductivity ionic liquids rolling off near 100 kHz.

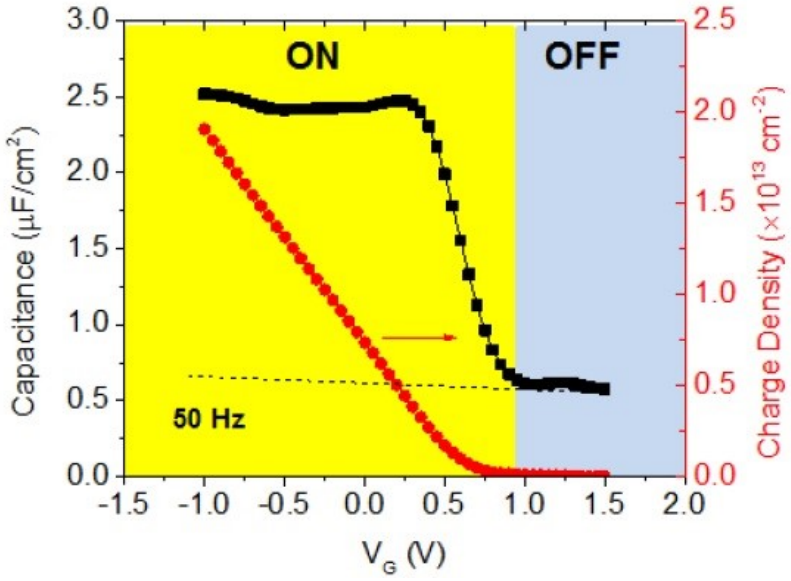


Figure 3.9 Capacitance (black) and charge density (red) for a rubrene EDLT as determined via impedance analysis.[95]

Of particular interest with regard to charge density is the dependence of capacitance on voltage as shown in black in Figure 3.9 for a rubrene EDLT. Using impedance analysis, impedance and phase angle can be measured at a fixed AC oscillation frequency (typically the standard operating frequency of the device being tested) and amplitude while the DC voltage offset is swept linearly. Using equation 3.7, the capacitance can be determined at each voltage. The resulting capacitance curve can then be integrated with respect to gate voltage to give charge density:

$$p = \int \frac{C}{eA} dV_G \tag{3.8}$$

The third method commonly used to determine charge density in EDLTs is called the displacement current measurement (DCM). To perform a DCM, the source and drain contacts of the EDLT are typically shorted to ground and a linearly ramping voltage is applied to the gate electrode while current is measured.

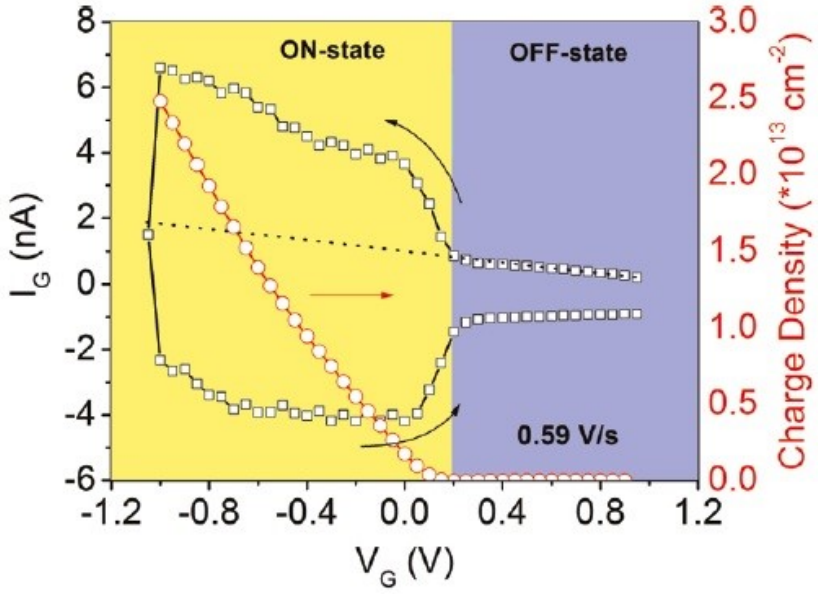


Figure 3.10 Gate current (black) and charge density (red) from a displacement current measurement (DCM) performed on a rubrene EDLT.[44]

Charge density can be obtained from a DCM by integrating current with respect to gate voltage:

$$p = \frac{Q}{eA} = \frac{\int I_{disp} dV_G}{r_V eA} \tag{3.9}$$

where I_{disp} is the displacement current, r_V is the gate voltage sweeprate, e is the elementary charge, and A is the area of the channel. When performing DCMs on an EDLT, there is a distinct off-to-on transition (Figure 3.10) as the conducting channel forms. An integration baseline is usually taken as the current measured in the off regime and is subtracted before the current is integrated. The baseline is used to account for parasitic capacitance in the device that is not due to the gate-ionic liquid-semiconductor capacitive stack. DCM is particularly useful when determining charge carrier mobility (covered in detail in the next section) because the gate voltage sweep conditions (linear ramp) are identical to the

conditions when performing a transfer curve measurement. This is important due to the sweep rate dependency of capacitance and better ensures that charge density measured by DCM at a given gate voltage is a reasonable estimation of charge density during a transfer curve measurement performed using the same sweep rate.

DCM can also be used to accurately measure capacitance. Capacitive current (the current going into charging the capacitor) can be defined as:

$$I_C = \frac{\partial Q_C}{\partial t} = \frac{\partial (CV_G)}{\partial t} = C\frac{\partial V_G}{\partial t} \tag{3.10}$$

where I_C is the capacitive component of the current, C is capacitance, and dV_G/dt is the gate voltage sweep rate. Realistically the whole of the displacement current is not all capacitive current, so we have:

$$I_{disp} = I_C + I_{Res} \tag{3.11}$$

where I_{Res} is the residual component of the displacement current that does not go into charging the capacitor. I_{Res} is typically leakage current due to electrochemistry or other phenomena and does not scale with gate voltage sweep rate. We can write the total displacement current as a linear function of gate voltage sweep rate:

$$I_{disp} = C\frac{\partial V_G}{\partial t} + I_{Res} \tag{3.12}$$

Plotting total displacement current as a function of sweep rate (at a specific gate voltage value) yields a line with a slope equal to the capacitance and a y-intercept equal to the leakage current as shown in Figure 3.11.

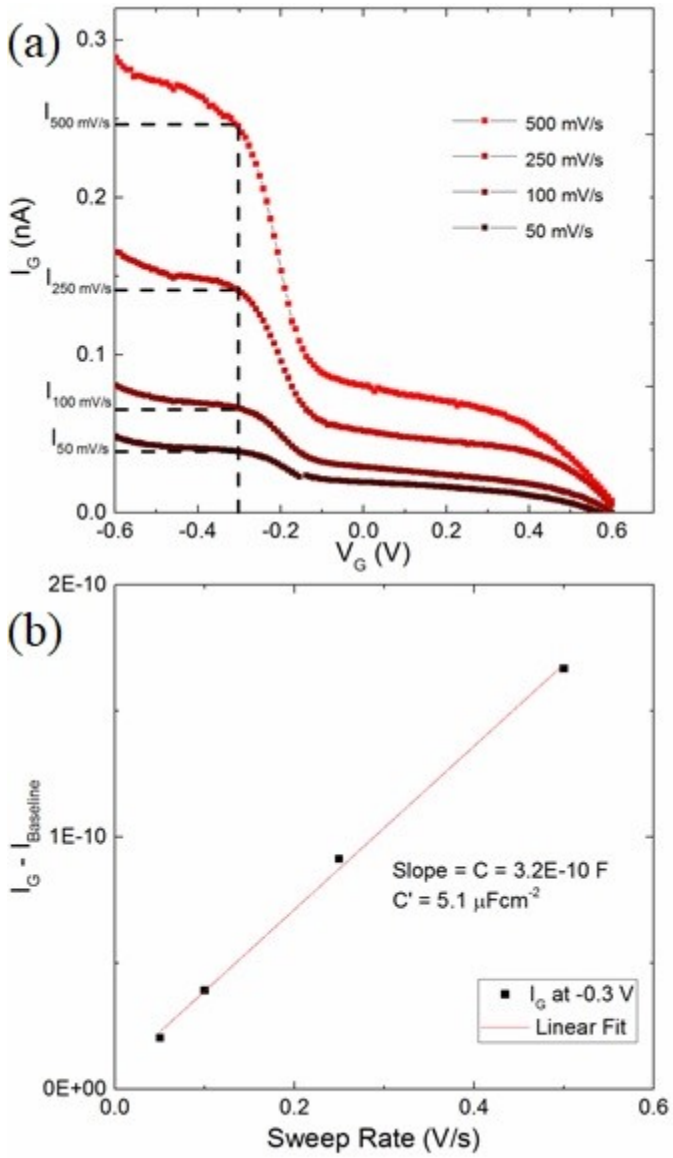


Figure 3.11 (a) Forward sweep of a displacement current measurement (DCM) of a rubrene EDLT. (b) Plot of displacement current vs gate voltage sweep rate.

Capacitance values calculated via DCM and impedance analysis (at ~0.5 Hz) tend to align well as shown in Figure 3.12 for many different ionic liquids tested in an Au/IL/Au capacitor.

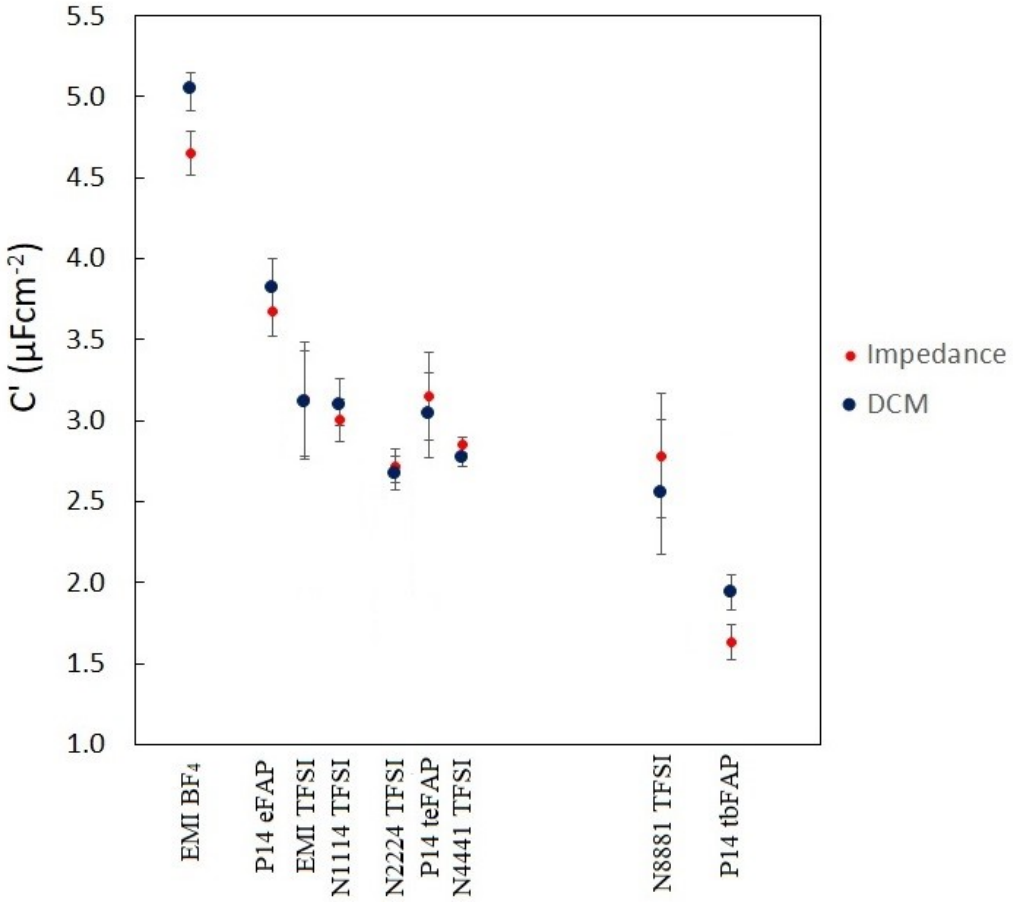


Figure 3.12 Comparison of specific capacitance values obtained in an Au/IL/Au capacitor for different ionic liquids using the DCM and impedance analysis techniques.

The final method employed to determine charge density in EDLTs is the Hall effect measurement. Hall effect measurement is predicated on use of the Lorentz force, which is a force exerted on a charged particle moving through a magnetic field. If a charge carrier moving down the length of the semiconductor channel is subjected to a magnetic field perpendicular to the motion of the charge, the charge will deflect in a direction perpendicular to both its motion and the magnetic field. This causes a net density of charge to build up on one side of the semiconductor channel that creates a potential difference

between the two sides of the semiconductor channel. This potential difference is called the Hall voltage and is defined as:

$$V_H = \frac{I_x B_z}{pe} \tag{3.13}$$

where V_H is the Hall voltage, I_x is the current in the x-directoin, B_z is the magnetic field in the perpendicular z-direction, p is charge carrier density, and e is the elementary charge constant. By measuring V_H, I, and B, charge density can be determined. Additionally, the sign of the Hall Voltage indicates whether conduction occurs primarily by hole or electron transport.

Hall effect measurements are the most accurate way to determine charge density; however, they are challenging to perform in organic EDLTs both due to the extreme charge density (because the Hall voltage is inversely proportional to charge density) and low charge carrier mobility (because the charges generally need to be relatively delocalized for Lorentz deflection to occur reproducibly). Nevertheless, Hall effect measurements have been successfully carried out in a number of organic semiconductors using both conventional[40, 73] and ionic liquid[96-97] dielectrics.

3.2.3 Mobility Measurements

Due to the voltage dependent capacitance, the mobility equations (Eq. 2.6 and 2.8) for solid dielectric-based FETs no longer hold for EDLTs. Instead, going back to the definition of conductivity as $\sigma=ep\mu$, mobility can be written as $\mu=\sigma/ep$. This can then be written in terms of currents, voltages, and device dimensions:

$$\mu = \frac{I_D}{epV_D}\frac{L}{W} \tag{3.14}$$

where I_D is drain current, V_D is drain voltage, e is the elementary charge constant, p is the charge density, L is the length of the semiconducting channel, and W is the width of the semiconducting channel. Charge density can be determined as a function of gate voltage simply by integrating a DCM (performed at the same sweep rate as the transfer curve) to a range of desired gate voltages. The mobility can then be plotted as a function of gate voltage as shown in Figure 3.13.

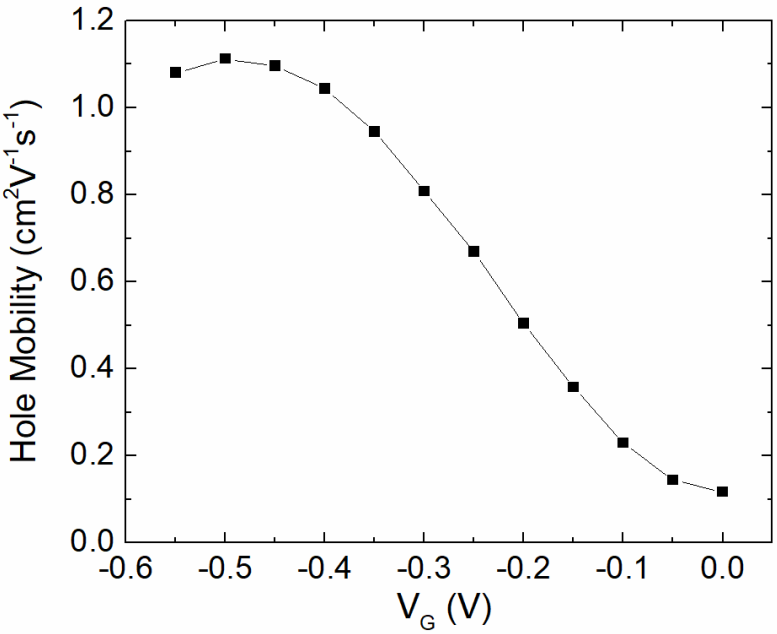


Figure 3.13 Hole mobility as a function of gate voltage for a rubrene EDLT using $[P14]^+[teFAP]^-$ as the gate dielectric.

Figure 3.13 illustrates a unique phenomenon that occurs in organic EDLTs: the existence of a peak in the mobility – gate voltage relationship. The subsequent decrease in the mobility at gate voltages past the peak becomes so extreme that conductivity in organic

OFETs also exhibits a peak even though charge density continues to increase. Put another way, the decrease in mobility with gate voltage becomes proportionally larger than the increase in charge density with gate voltage leading to an overall decrease in conductivity with gate voltage. Such conductivity peaks have been observed for both organic thin-film EDLTs[98-99]as well as organic single crystal EDLTs[44, 97]. Interestingly, in inorganic EDLTs, such as ZnO, a conductivity peak is not usually observed.[100] The origins of this peak are not well understood. It is possible that the local electric fields of ions near the semiconductor interface serve as charge localizing traps. Increasing gate voltage increases the number and proximity of ions to the surface and therefore increase the number and depth of traps. This effect could be more significant for organic semiconductors due to lower dielectric constants and hence reduced field screening. Other possibilities include sudden rearrangements in charge ordering at the semiconductor interface that occurs at elevated gate voltages and changes the potential landscape of the charge carriers in such a way that makes the charges less mobile.

Chapter 4: Experimental Methods

4.1 Single Crystal Growth Procedures

Single crystals used throughout work in this thesis were grown by the PVT method described in section 2.3.1. In particular Rubrene, Figure 4.1, was used extensively due to its benchmark hole mobility among organic semiconductors and the ability to easily grow high quality single crystals using PVT. Crystals were grown in the PVT setup shown in Figure 4.2.

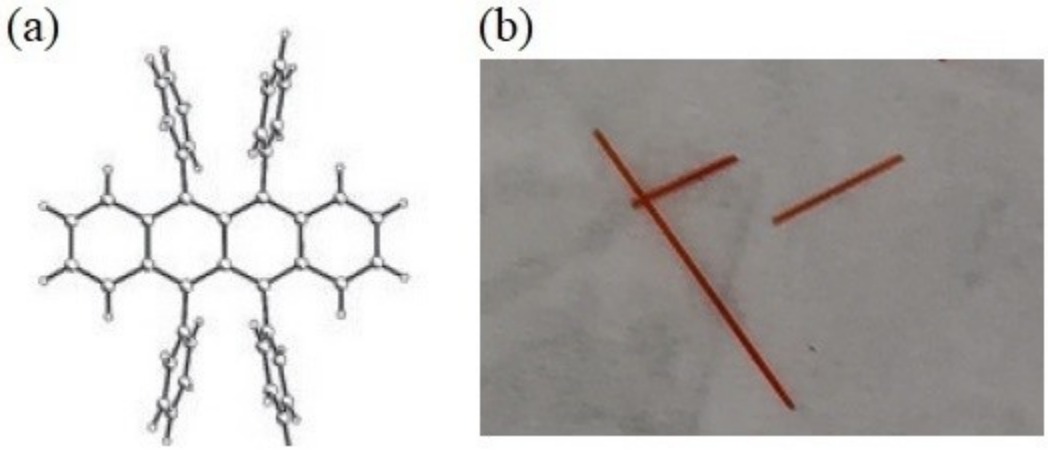


Figure 4.1 (a) Structure of rubrene molecule. (b) Photograph of rubrene crystals grown by PVT.

Heating was produced through a combination of heating tape wrapped around an outer glass tube focused near the source material and nichrome wire wrapped unevenly down the length of the inner glass tube in order or produce a temperature gradient. Temperatures were controlled by adjusting the voltage across the heating tape and nichrome wire using Variac variable transformers. Temperatures were monitored with digital thermometers using k-type glass braid thermocouples. A quartz growth tube, on which the crystallization occurs, is placed within the inner heating glass tube. A source

boat of rubrene powder is placed towards one end of the quartz growth tube and is centered underneath the heating rope coil, which is the zone of highest temperature.

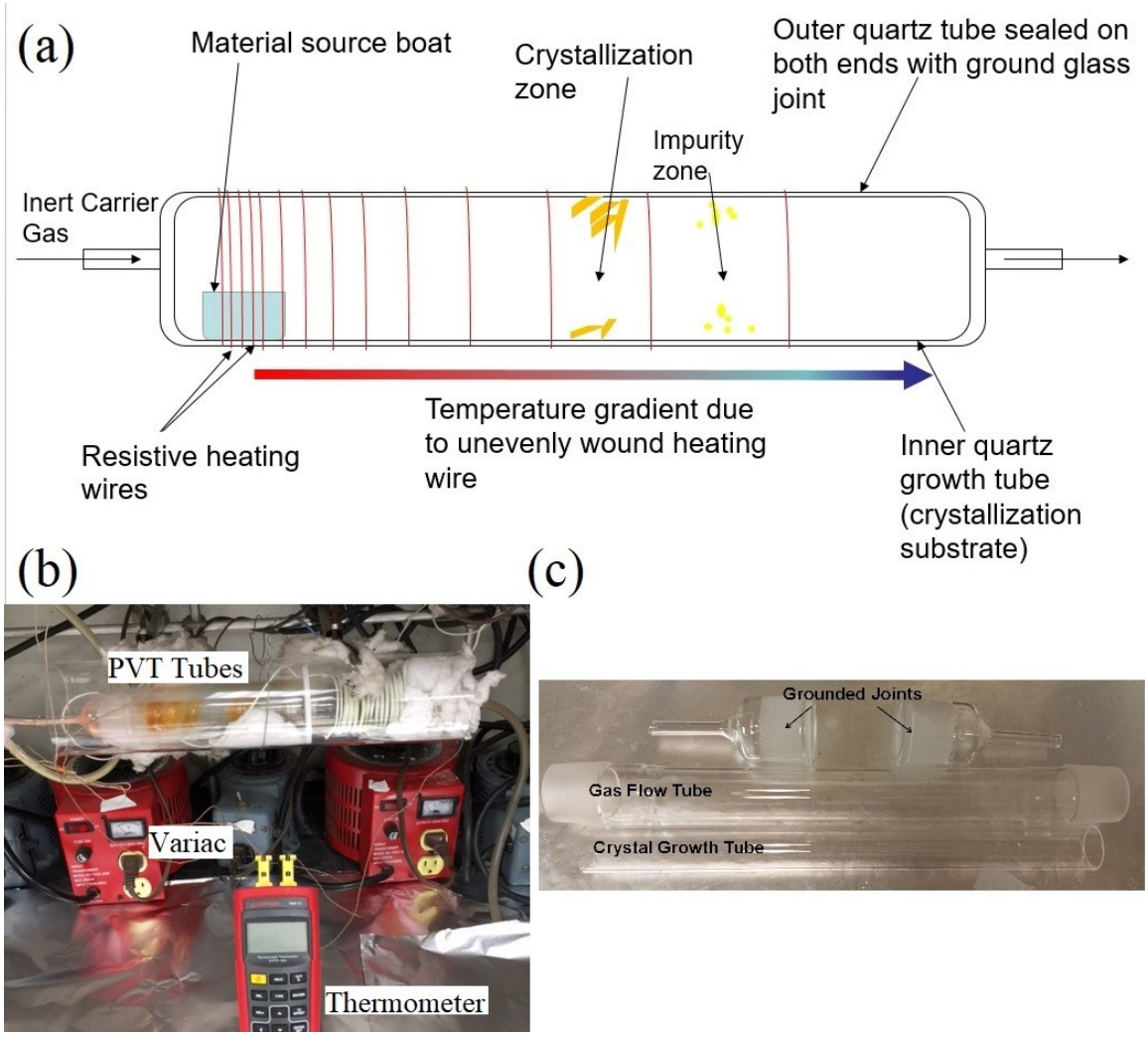


Figure 4.2 (a) Schematic of PVT process. (b) Photograph of PVT growth setup including thermometer and Variacs. (c) Photograph of glassware used in PVT setup

The temperature of the setup involves adjusting the two heating zones (heating rope and nichrome wire) such that the hottest point, T_{source}, (underneath the heating rope) is ~300°C. This temperature is slightly variable depending on if you want a very slow crystal growth for thicker crystals (T_{source}=280-290°C) or very thin crystals (T_{source}=305-310°C).

Thicker crystals are more mechanically robust and easier to handle; however, thin crystals have the ability to flex and conform to substrate surfaces better and are therefore much better for use on hard substrates like silicon wafer. Crystallization of rubrene from the vapor phase occurs around 250 °C, so the temperature gradient is adjusted so that the distance from the source boat to the crystallization zone is on the order of several inches. A gradual temperature gradient better separates the impurities from the pure rubrene crystals. Ultra-pure argon is used as the carrier gas as it yield high quality crystals and does not have the same safety concerns as use of H_2 gas, even though H_2 gas yields slightly higher quality crystals.[22] Gas flow rates are typically set between 10-100 mL/min depending on whether thick (slow gas flow) or thin (high gas flow) are desired. Thin crystals are on the order of hundreds of nanometers thick and thick crystals can be on the order of 100 microns thick.

4.2 Characterization of Crystals

To verify the quality and single-crystalline state of PVT grown crystals, two methods were employed. Polarized light microscopy is the first and is the quickest and simplest quality check. Crystals polarize light, and the angle of polarization is determined by the orientation of the crystal grain. In a polycrystalline material (with a wide array of grain orientations) only a selection of the total number of grains will be visible through a polarized filter at a given time. As the polarized filter is rotated, grains come in and out of view depending on if the grains polarize light in a way that aligns with the polarized filter or not. A single crystalline material lacks grain structure, and so the entirety of the crystal will be visible or not visible for a given position of polarized filter.

X-ray Diffraction (XRD) is the second method used to analyze crystallinity and crystal quality. XRD experiments were conducted using a (PANalytical X'pert Pro using 0.154 nm Cu Kα radiation). Figure 4.3 shows a wide angle 2θ scan of a rubrene single crystal. High quality crystals are indicated by the following factors: obtaining the predicted Bragg peaks, having narrow peak widths, and having many higher order peaks. Rocking curve analysis (ω-scan) is performed by setting the angle between the crystal and detector to the 2θ value of the desired peak and then rocking the sample (ω-angle) relative to the fixed detector. The full-width-at-half-maximum (FWHM) is characterized as a function of ω. The wider the peak, the higher the mosaicity. Mosaiscity is the deviation of crystallographic planes from being parallel/flat to one another.

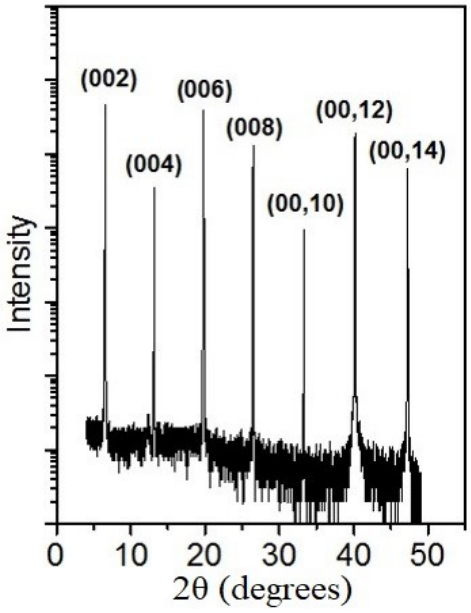


Figure 4.3 XRD pattern of a rubrene single crystal grown by PVT.

4.3 Fabrication of Vacuum Gap SC-OFETs

The following recipe was used to fabricate the substrates for SC-OFET devices with a 5 μm vacuum gap. Vacuum gap depth can be adjusted by using different SU-8 photoresists. Exposure parameters and possible bake times will need to be increased as photo resist thickness increases.

1. A cleanroom environment is highly recommended as dust can both cause device shorting and prevent good crystal adhesion to the substrate.
2. Make a bright-field mask in an autoCAD software. The chromed regions of the mask will become the raised regions of the final substrate (i.e. source and drain electrodes and any voltage sensing probes).
3. Fabricate a master wafer mold using a 4 inch wafer with at least one polished side. All other parameters are unimportant to fabrication of the stamp.
    - Clean the wafer in piranha solution (H2SO4:H2O2) for 10 mins. Rinse thoroughly with DI water and then place the wafer cassette into the cassette dryer and run a rinse-dry cycle of approximately 2 min. rinse, 5 min. dry.
    - Pre-bake: 65 ˚C for 1 min.
    - Spin coat SU8-2005 for 30 sec, 2500 rpm, resulting in ~5 μm in thickness.
    - Soft bake: 95 ˚C for 2 mins.
    - Exposure (total dose needed is 105 mJ/cm2, soft contact, gap 25 μm, expose for 9 secs if using the MA-BA-6 Karl Suss contact aligner with 12 mW/cm2 lamp).
    - Post-exposure bake: 95 ˚C for 3 mins.

- Develop with SU8 developer for 50 ~ 55 secs.
- Rinse with IPA thoroughly for 2 ~ 3 mins and nitrogen dry.
- Hard bake: 150 ˚C for > 5 mins.

4. Check the height of the vacuum gap (raised pad heights) using surface profilometry.
5. Place silicon wafer in vacuum chamber with a small petri dish containing 1 mL of Trichloro(1H,1H,2H,2H-perfluorooctyl)silane. Pump for 2 minutes to vaporize the silane then turn off the pump and leave the vacuum chamber sealed for at least two hours (overnight preferable). This should be done in a well-ventilated area or fume hood as the silane can irritate the nose and eyes due to formation of hydrochloric acid upon contact with water. The silane layer makes the stamps significantly easier to remove from the wafer surface and is highly recommended.
6. Make PDMS stamps from wafer master mold:
   - Put the master wafer in clean petri-dish (preferably glass) with the patterned side facing up.
   - Tape or epoxy the wafer flat onto the bottom of the dish to ensure the wafer remains level
   - Mix (stir > 5 mins) PDMS prepolymer (Sylgard 184, Dow Corning) and curing agent (10:1 wt%) and pour it into the petri dish. A ~0.3 centimeter thick stamp is obtainable by pouring ~45 grams of mixed Sylgard 184 into a fresh 6 inch petri dish. Subsequent stamps using the same mold will require only 20-25 grams of Sylgard 184 if the PDMS around the outer edge of the wafer was not removed from the previous pour.

- Degas the PDMS in a vacuum chamber for 2-3 hours (until no bubbles are visible).
- Bake in oven at 100 ˚C for 2 hours. A high temperature cure increases the elastic modulus of the PDMS significantly creating a more robust stamp.
- Carefully cut out the PDMS stamp and peel it from the surface of the wafer. Cutting just inside the edge of the silicon wafer makes it much easier to peel off.

7. Emboss the pattern on the PDMS surface by covering the patterned side with Scotch tape. This greatly enhances the ability to see the pattern, which facilitates cutting of the stamps.
8. Cut individual device patterns from the PDMS stamp and place each pattern on a piece of dust-free (cleaned via scotch tape) glass slides. The cleanliness of the slide is extremely important to ensure good adhesion of the stamp to the glass substrate during the subsequent evaporation process.
9. Remove embossing scotch tape from the surface of the individual patterns prior to evaporation. This tape is usually left on until this point to minimize the amount of dust on the surface prior to evaporation.
10. Using an e-beam evaporator deposit a 30 Å adhesion layer of chromium onto the surface followed by a 200 Å conduction layer of gold. Deposition rate is 1.0 Å /sec for chromium and 2.0 Å/sec for gold.
11. Let stamps sit in atmosphere for 1 month+ before use. High contact resistance and device degradation is observed if this step is not followed. This likely results from

a combination residual pre-polymer residue in the stamp that dissolves the contact regions of the crystal as well as the need for the gold to "dirty" in the air, which seems to reduce contact resistance.[101]

12. Carefully laminate a single crystal across the source and drain electrodes. To ensure good lamination the substrate must be dust free and the crystal must be very flat as evidenced by a uniform surface reflection when examining the crystal.

4.4 Fabrication of Au-IL-Au Capacitors

The Au-IL-Au capacitors used in Chapter 5 are fabricated in a very similar fashion to the vacuum gap SC-OFET devices. The main deviation comes from laminating a piece of gold coated silicon wafer on the raised electrodes of a PDMS vacuum gap substrate in place of a single crystal. The pieces of gold coated wafer are prepared in the following fashion:

1. Clean a silicon wafer using piranha etch and rinse using the same procedures in section 4.3 (only constraint is that at least one side of the wafer needs to be polished)
2. On the polished side of the wafer, using an e-beam evaporator, deposit 25 Å of chromium and 170 Å of gold at 1 Å/s and 2 Å/s respectively.
3. Coat the gold coated surface of the wafer in Shipley 1805 photoresist by spin coating for 30 sec at 3000 rpm.
4. Resist can be baked but no exposure is required as this is merely a temporary surface protection layer.

5. Place the wafer on a square of UV-releasing temporary bonding tape. Using a wafer saw, dice the gold coated wafer into ~750 μm wide by 2000 μm rectangles. Cut completely through the wafer but not completely through the tape layer.
6. Expose the tape to UV until wafer can be peeled off with a slight amount of effort.
7. As needed, remove pieces of wafer from the tape and rinse them thoroughly in acetone, followed by methanol, followed by IPA in order to remove the photoresist layer. Dry in nitrogen.
8. Place gold coated side of the wafer face down across raised electrodes. The substrate must be superbly clean (even more than in the rubrene crystal case) else the wafer piece will not form a good seal.

4.5 Electrical Characterization

All electrical measurements were made in a Lakeshore TTP4 cryogenic probe station that is inside of a nitrogen-filled glovebox with O_2 levels of less than 0.1 ppm. Temperature was controlled using a Lakeshore 330 temperature controller. DC measurements were carried out using a variety of Keithley SMUs (236, 237, 2612b, and 6517a). AC measurements were carried out using a Newton's 4^{th} PSM 3750 frequency response analyzer in conjunction with the IAI2 impedance attachment.

Chapter 5: Dynamics of Metal/Ionic Liquid/Metal Capacitors

This chapter focuses on gaining a deeper understanding of the dynamics of ionic liquid gating. Due to the inherent complexity of ionic liquids, a very simple capacitive system is analyzed consisting of two gold electrodes with ionic liquid between them. The system is analyzed on a wide variety of time scales using three different methods: step potential measurements, displacement current measurements (DCMs), and impedance analysis. An equivalent circuit model is then proposed that well describes the dynamics of the device. The parameters of the model are determined by a fit to the impedance vs frequency data and subsequently verified by calculating the current vs. voltage characteristics for the applied potential profiles. The data analysis indicates that the dynamics of the structure are characterized by a wide distribution of relaxation times spanning the range of less than microseconds to longer than seconds. Possible causes for these time scales are discussed. This worked was published as Schmidt, E.; Shi, S.; Ruden, P. P.; Frisbie, C. D. Characterization of the Electric Double Layer Formation Dynamics of a Metal-Ionic Liquid-Metal Structure. *ACS Appl. Mater. Interfaces* **2016**, 8, 14879-14884.

5.1 Introduction

Ionic liquids (ILs) have found use as excellent high capacitance 'dielectrics' for electronic devices in the last several years.[15-16, 102-103] The high capacitance of an IL can be attributed to the formation of electrical double layers (EDLs). When a bias is applied across

an IL, the cations migrate towards the negative electrode and the anions migrate toward the positive electrode resulting in an EDL at each electrode as well as the structuring of an oscillating multilayer of ions near the electrode surface.[104] The capacitance of an EDL is large because, in a steady state, the total applied bias is dropped only across the double layer thickness (~1 nm in thickness) with the bulk of the ionic liquid remaining charge neutral. The resulting specific capacitance is on the order of $\mu F/cm^2$, which allows field effect transistors using ionic liquids as gate 'dielectrics' to reach very high charge carrier densities on the order of 10^{13}-10^{14} cm^{-2}.[44, 105-107] At these high charge densities unique phenomena, such as insulator-to-metal transitions and field effect induced superconductivity, can occur.[13-14, 108]

Despite impressive accomplishments achieved with the use of ionic liquids in various devices in the last several years, a comprehensive understanding of ionic liquid dynamics in electronic systems still appears to be elusive. One-dimensional models for EDL formation in dilute electrolyte solutions, such as the Helmholtz and Gouy-Chapman, or more advanced models that include steric and electric correlation effects,[109-117] are often used to give some insight into the behavior of an ionic liquid in an electronic device; however, their success in explaining experimental data is limited as the one-dimensional models cannot predict three-dimensional structuring.[118-119] The lack of solvent molecules and the much higher concentration of ions make ILs a more difficult system to model than dilute electrolytes.

One poorly understood phenomenon of particular interest to the electric double layer transistor (EDLT) community is a sweep rate-dependent linear change in

displacement current while linearly ramping voltage.[15, 107] Displacement current measurements (DCMs) are a method used to determine charge density in capacitive structures and EDLTs.[120] DCMs are particularly useful as a secondary check on charge density values obtained by impedance analysis or as an alternative to Hall effect charge density measurements in systems exhibiting hopping transport. A near-ideal capacitor, like one using a SiO_2 dielectric, has a perfectly flat displacement current-voltage relationship. The sweep-rate dependent slope in the displacement current-voltage relationship for capacitors and EDLTs using an ionic liquid "dielectric" is attributable to slow, complex relaxation processes at the electrode surfaces. A good understanding of the dynamics of double layer formation could facilitate the minimization of the effective relaxation time and could therefore improve the switching speeds of EDLTs.

In this work, we present a comprehensive study of IL dynamics over a wide range of time scales through the use of frequency dependent impedance analysis as well as current voltage measurements for different voltage profiles in order to better understand the timescales of relaxation in these systems. An equivalent circuit model is constructed that well replicates the dynamics of a metal/IL/metal structure, including the sweep-rate and voltage dependence of the displacement current, and gives some insight into the distribution of relaxation times that characterizes the dynamics of this system.

5.2 Device Structure

Rubber stamps with two raised pads separated by a channel were prepared by pouring polydimethylsiloxane prepolymer (purchased from Ellsworth Adhesives) onto a patterned silicon wafer according to procedures in Sections 4.3 and 4.4. A 2.5 nm adhesion

layer of chromium followed by a 17 nm thick layer of gold were evaporated onto the rubber stamps (using a CHA electron beam system) to form a pair of raised electrodes with another electrode below. RMS surface roughness of the gold film was measured to be ~ 3 nm (averaged over three linear scans of 100 μm) using a Tencor P-17 profilometer. A piece of a silicon wafer was also coated with 2.5 nm Cr/17 nm Au by the same evaporation process with a measured RMS roughness of ~1 nm. This piece of silicon was then physically adhered to the raised electrodes of the stamp to form the MIM structure shown in Figure 5.1 (a). The area of the device was 1.7×10^{-3} cm^2 and the distance between the top and bottom electrodes was 5 μm. A conductivity test was then performed between the two raised pads to verify good adhesion of the gold-coated silicon top layer to the stamp. A subsequent test was performed between the raised pads and the bottom electrode to verify that no measurable leakage current existed (<1pA at 100 mV applied bias). After testing, a tiny droplet of ionic liquid was dragged and touched to the gap between the top and bottom electrodes using a metal probe. The ionic liquid was easily wicked into the small gap via capillary action and filled it completely. The ionic liquid used (Figure 5.1 (b)) was 1-butyl-1-methyl pyrrolidinium ($[P14]^+$) tris-(pentafluoroethyl)trifluorophosphate ($[FAP]^-$) and was purchased from EMD Millipore. $[P14]^+[FAP]^-$ was chosen as it is a proven IL that is particularly hydrophobic, and it is an IL with which we have experience in the context of organic EDLTs.[44] The IL was baked in a vacuum oven to minimize any possible water content.

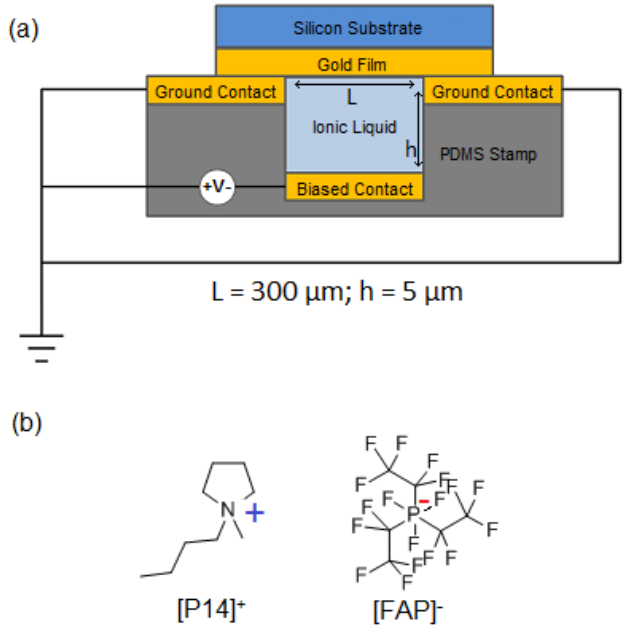


Figure 5.1 (a) Cross section of metal-insulator-metal (MIM) structure using gold electrodes and ionic liquid (IL) as the insulator. (b) Chemical structure of the ionic liquid 1-butyl-1-methyl pyrrolidinium tris-(pentafluoroethyl)trifluorophosphate ($[P14]^+[FAP]^-$).

5.3 Electrical Measurements

All measurements were made in a Lakeshore TTPX probe station inside of a nitrogen glovebox in order to prevent contamination of the ionic liquid with water. Measurements were made at 300K controlled by a Lakeshore 331 temperature controller in conjunction with a low liquid nitrogen flow and a heating element.

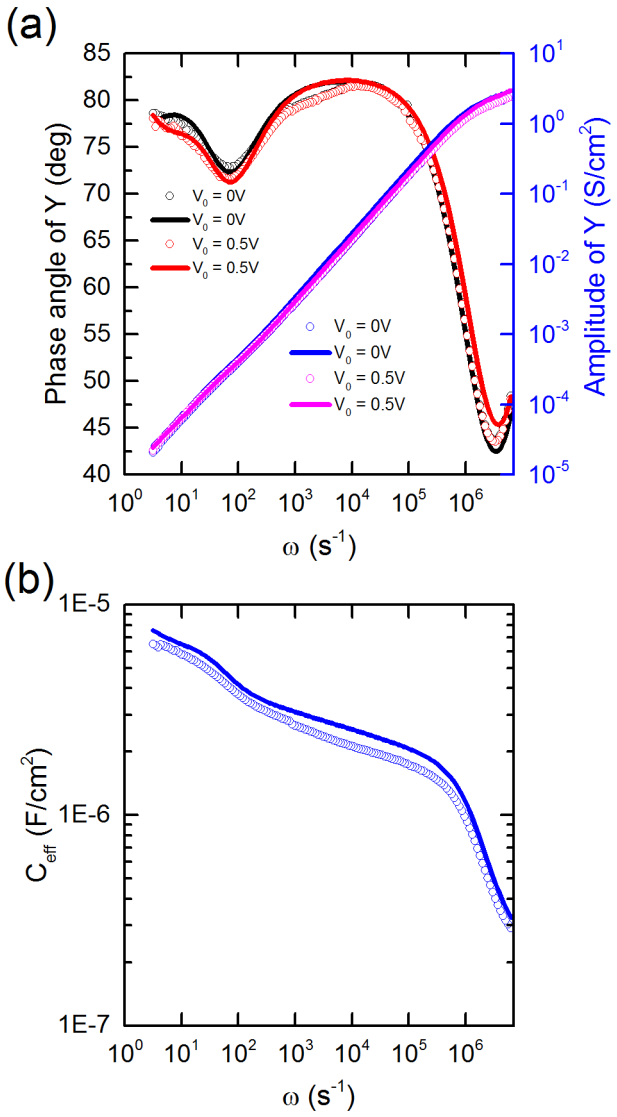


Figure 5.2 Open circles are experimental data while solid lines are the results of the proposed model. (a) Phase angle-frequency (red and black) and admittance-frequency (pink and blue) relations for $[P14]^+[FAP]^-$ in an Au/IL/Au structure. (b) Effective capacitance-frequency characteristic of $[P14]^+[FAP]^-$ in an Au/IL/Au structure.

Impedance measurements were made using a N4L PSM 3750 frequency response analyzer with the IAI2 impedance analysis attachment. Impedance and phase angle were measured as a function of frequency in the range of 0.5 Hz to 1.0 MHz. Figure 5.2 (a) is a

Bode plot of a typical Au/IL/Au device. The red and black circles show the admittance phase angle vs. frequency relationship for the same device under two different DC biases, and the red and black solid lines are the result of the model discussed in the following section. Similarly, the pink and blue circles show the admittance magnitude vs. frequency relationship for an actual device and the solid pink and blue lines show the result of the model. Capacitance due to instrumentation and cabling causes the phase angle to begin to increase at frequencies above $\omega = 10^6$ sec^{-1} and also accounts for the admittance reaching a maximum of 3 S/cm2.

To give an impression of the potential switching speed of such a capacitor structure, Figure 5.2 (b) shows the effective capacitance vs. frequency relationship for a typical device with experimental data represented by circles and a solid line representing the results of the model. The effective capacitance of the device as a whole is taken to be $C_{eff} = Im(Y)/\omega$. C_{eff} initially decreases gradually as the frequency increases (about one order of magnitude decrease when ω increases by six orders of magnitude) before dropping more rapidly above $\omega = 10^6$ sec^{-1}.

Time dependent current vs. voltage measurements (both linear ramp and step) were made using a Keithley 2612b source measure unit. During the linear ramp, V = 0 at t = 0 and is swept to V = -0.5 V at various fixed rates and then swept back to V = 0 at the same rate. For an ideal capacitor with a small series resistance, this measurement would result in a constant positive current when sweeping in one direction and constant negative current of equal magnitude when sweeping in the opposite direction. In Figure 3 we can see a linearly ramped displacement current measurement for a typical Au/IL/Au device. There

is an initial turn on transient, related to the RC time constant of the device, where the current steeply increases. This is followed by a linear current vs. voltage relationship with a modest slope. The slope increases with increasing voltage ramp rate. Different voltage ramp rates sample different parts of the frequency response characteristics of the device, and device characteristics vary dramatically with frequency as shown by admittance data. Results of the equivalent circuit model are able to replicate the measurements satisfactorily (solid lines in Fig 5.3).

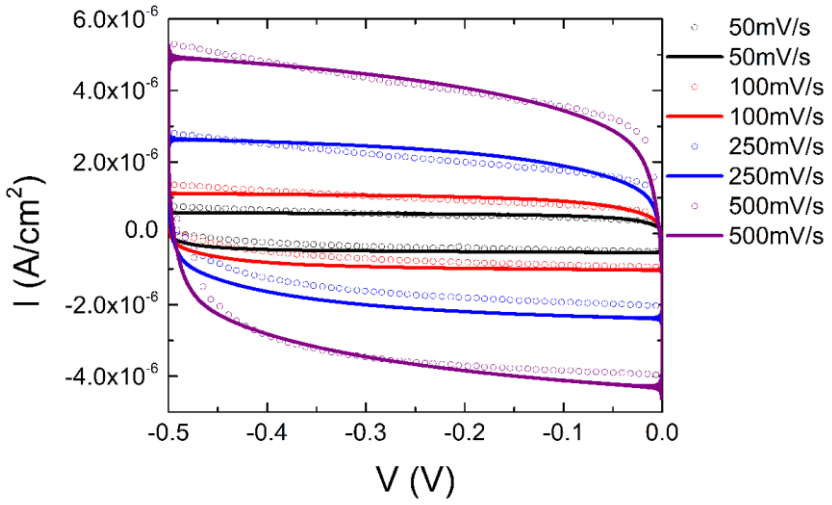


Figure 5.3 Displacement current measured while linearly varying the voltage from 0 V to -0.5 V back to 0 V at varying rates. Open circles are experimental data and solid lines are the results of the proposed model.

Figure 5.4 shows the device's current response to the application of voltage steps. The Au/IL/Au capacitor is initially charged by applying a -0.5 V bias at t = 0 s while simultaneously measuring the current. This bias is held for 15 s at which point the capacitor is discharged by applying 0 V at t = 15 s and measuring the current for another 15 s. After

long times (tens of seconds) current decayed to levels below the resolution of our instrumentation (~1pA).

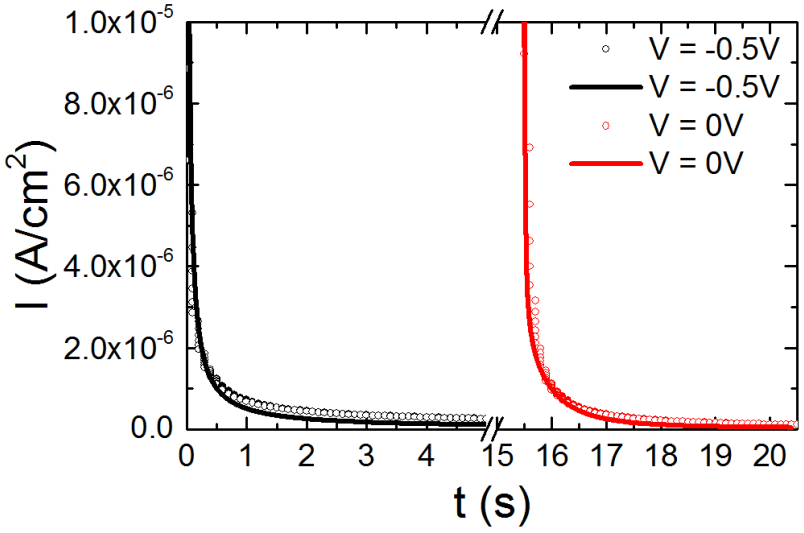


Figure 5.4 Displacement current measured when applying a -0.5 V step potential at t = 0 sec and holding the bias for 15 s before stepping to 0 V at t = 15 sec and holding 0 V for 15 s. Circles are experimental data while solid lines are the result of the proposed model.

5.4 Equivalent Circuit Model and Discussion

It is evident from the admittance data displayed in Figure 5.2 that the dynamical response of the metal/IL/metal device structure is rather complex. At very high frequencies, $\omega > 10^7\ s^{-1}$, ion motion is not expected to follow the time varying applied electric field and the device response is dominated by the probe and cable capacitance of what under those conditions is essentially a low capacitance metal/dielectric/metal structure. Effective formation of EDLs is expected for lower frequencies, $\omega < 10^5\ s^{-1}$. Under these conditions, simple first-order models would indicate that the device should act

as a very large capacitor. However, it is noted that the phase angle of the admittance is significantly less than $\pi/2$. This is a rather well studied phenomenon for EDLs in solid or liquid electrolytes. It frequently is attributed to roughness of the electrodes that leads to a distribution of essentially parallel capacitances that are accessible to the ions of the electrolyte.[121] The effect can be represented by so-called constant phase elements (CPE) in an equivalent circuit.[122] Here this approach is adopted for the metal/IL/metal structure under study. As there are two distinct gold surfaces with different roughnesses, different edges, different substrate materials, and different surface topographies, and for a given polarity they are exposed to different ions of the IL, we incorporate two CPEs into our model each representing a metal/IL interface. A CPE is a linear circuit element with an admittance of $Y_{CPE} = Q^{-1}(i\omega)^{1-\alpha}$, with $0 \leq \alpha \leq 1$.

The proposed equivalent circuit model for an Au/IL/Au device is shown in Figure 5.5. R_Ω is the resistance of the ionic liquid, and C_g is the geometric capacitance (including contributions from cabling and instrumentation). Each CPE is representative of the relaxation processes of ions occurring at an electrode where an EDL is formed. By fitting the admittance and phase angle data in Figure 5.2 (a) for applied DC voltages of 0 V and -0.5 V we extracted the parameters seen in Table I. The fits were conducted by first fitting α, and subsequently Q, for the CPEs. Then R_p and C_p were adjusted to fit low frequency behavior. R_Ω and C_g were fixed and were calculated from IL conductivity values and measurements of instrumentation capacitance respectively.

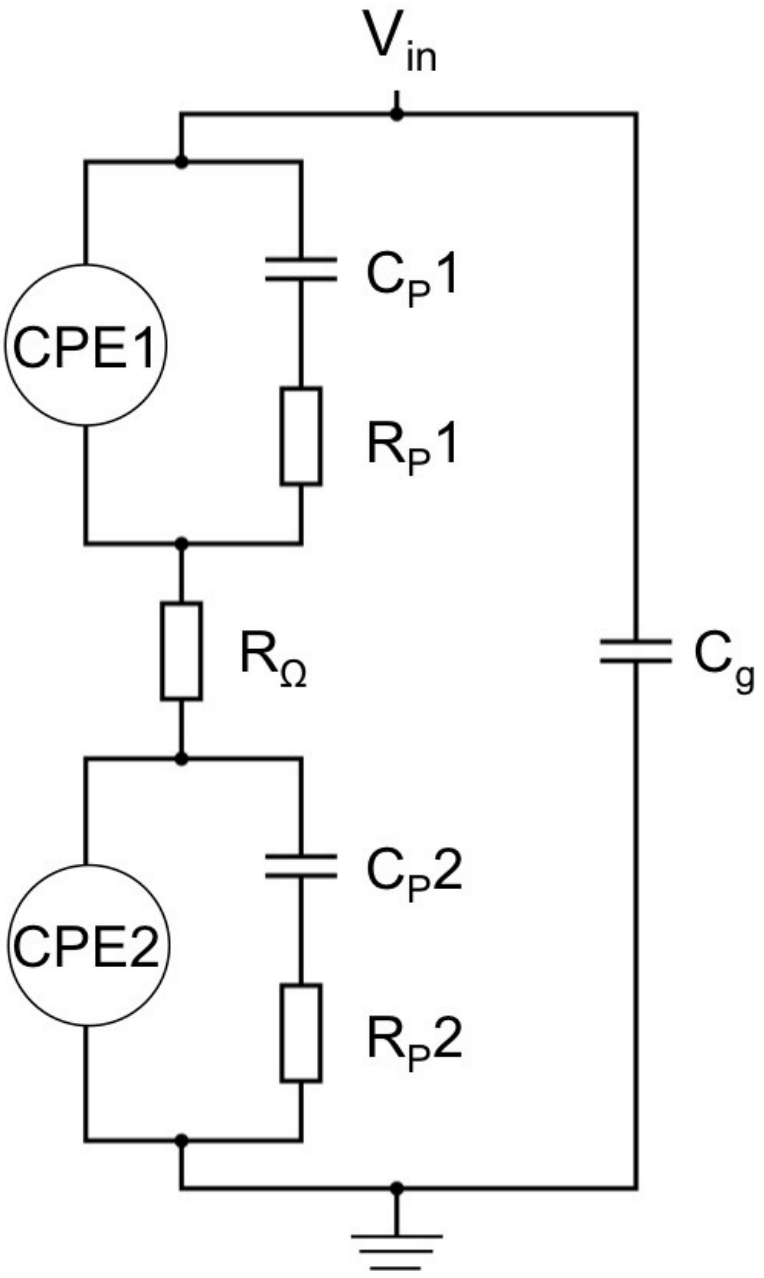


Figure 5.5 Equivalent circuit model for a Au/IL/Au device. The constant phase elements (CPEs) represent the distribution of relaxation times for ions to equilibrate on the electrode surfaces. R_Ω is the ionic liquid resistance, and C_g is the geometric capacitance, which includes contributions from equipment and cabling.

TABLE I. Fit parameters for the equivalent circuit model.

Device	α_1 α_2	Q_1 Q_2	R_{P1} R_{P2}	R_Ω	C_g C_{P1} C_{P2}
$V_0 = 0\ V$	0.09	$1.16 \times 10^5\ \Omega cm^2 s^{-(1-\alpha)}$	$4.1 \times 10^3\ \Omega \cdot cm^2$	$0.4455\ \Omega \cdot cm^2$	$2.7 \times 10^{-7}\ F/cm^2$
	0.09	$5.78 \times 10^4\ \Omega cm^2 s^{-(1-\alpha)}$	$6.6 \times 10^4\ \Omega \cdot cm^2$		$6.06 \times 10^{-6}\ F/cm^2$
					$1.21 \times 10^{-5}\ F/cm^2$
$V_0 = 0.5\ V$	0.09	$1.35 \times 10^5\ \Omega cm^2 s^{-(1-\alpha)}$	$4.1 \times 10^3\ \Omega \cdot cm^2$	$0.4455\ \Omega \cdot cm^2$	$2.7 \times 10^{-7}\ F/cm^2$
	0.09	$6.93 \times 10^4\ \Omega cm^2 s^{-(1-\alpha)}$	$4.1 \times 10^4\ \Omega \cdot cm^2$		$6.06 \times 10^{-6}\ F/cm^2$
					$1.21 \times 10^{-5}\ F/cm^2$

The distribution of relaxation times G(τ) for both of the CPEs is plotted in Figure 5.6 (a) and (b).[122] Here, $\tau G(\tau) = \frac{1}{2\pi} \frac{2\sin(\alpha\pi)}{\exp[(1-\alpha)s]+\exp[-(1-\alpha)s]-2\cos(\alpha\pi)}$, and $s = \ln(\tau/\tau_0)$. The parameters τ_0 for CPE_1 and CPE_2 are equal to $(Q_1^{-1} R_\Omega/2)^{\frac{1}{1-\alpha}}$ and $(Q_2^{-1} R_\Omega/2)^{\frac{1}{1-\alpha}}$, respectively.[123] In the limit of $\alpha \to 0$, the CPEs reduce to the EDL capacitances for the two interfaces and $G(\tau)$ becomes extremely sharply peaked at τ_0. However, $\alpha > 0$ implies that $G(\tau)$ extends far into the range of long relaxation times, as is seen in the plots on logarithmic scale, Figure 5.6 (b).

We note that even the presence of two CPEs (and R_Ω) cannot account for all of the complex structure of the phase angle in the range $\omega < 10^4\ s^{-1}$. Specifically, the minimum of the phase angle near $10^2\ s^{-1}$ and the low phase angle near $3\ s^{-1}$ require the introduction of parallel current paths. Evidently, the distribution of relaxation times to be associated with the CPEs does not contain sufficient weight on long relaxation times, on the order of 10^{-2} s or even 1 s. We therefore add suitable RC paths in parallel to the CPEs. With these

additional elements the low frequency admittance spectrum can be represented by the model.

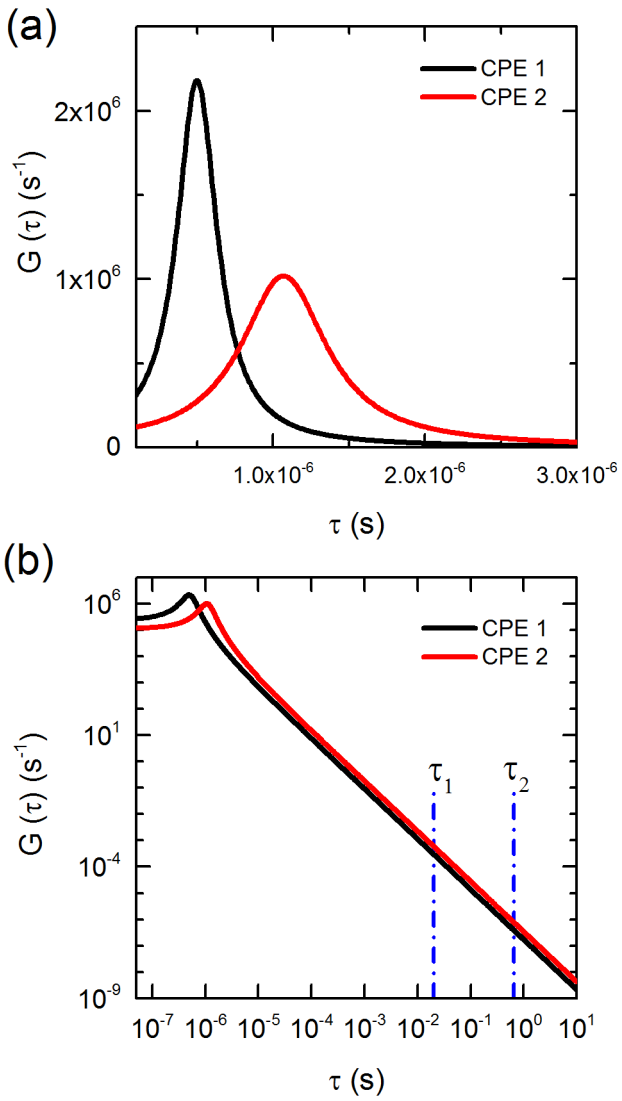


Figure 5.6 (a) Distributions of relaxation times for CPE1 and CPE2 when the applied voltage is 0 V on linear scale. (b) The same distributions on logarithmic scale also indicating the relaxation times associated with the current paths parallel to the CPEs.

In order to create the fits for the current vs. voltage experiments with a linear voltage ramp (Figure 5.3), the periodic zigzag voltage is Fourier transformed, $V(\omega) =$

$\mathcal{F}\{V(t)\}$, and the current is subsequently calculated using the admittance $Y(\omega)$ obtained from the fits shown in Figure 5.2:

$$I(t) = \mathcal{F}^{-1}\{V(\omega) * Y(\omega)] \tag{5.1}$$

A slight improvement in the accuracy is obtained by interpolating linearly between the $Y(\omega)$ fits obtained at DC bias voltage of 0 V and -0.5 V. In order to create the fits for the displacement current with a step voltage (Figure 5.4), an analogous procedure is used. Overall, the results obtained from the equivalent circuit model are in satisfactory agreement with the measured data.

As indicated above, the CPEs with the parameters obtained here can be viewed as representing certain distributions of relaxation times. These distributions are plotted in Figure 5.6. Both distributions have peaks in the vicinity of 1 μs, which may be thought of as the ideal EDL RC time. However, both distributions also have significant magnitude at much longer times. These longer relaxation times may be associated with the penetration of ions into intergranular grooves in the electrodes, or it may simply be an effect associated with ion-ion correlation, which is clearly important due to the very high ion density.[85, 119, 124] Finally, we remarked that additional longer relaxation times are apparently needed to account for the low frequency response. These times are indicated as τ_1 and τ_2 in Figure 5.6. We may speculate that they arise either at device edges where the establishment of an optimized ion distribution is particularly difficult, or perhaps they are associated with ion adsorption effects.

Although we do not expect significant charge transfer between the ions of the liquid and the gold contacts, such a faradaic process may exist. Because of the very slow

relaxation a true DC current is difficult to measure. Based on the step voltage response data obtained here we estimate that a faradaic current component would be less than 10^{-7} A/cm^2 at 0.5 V, corresponding to a parallel resistance of 10^7 Ωcm^2. This additional current path would primarily impact the dynamics at very low frequencies. However, as is seen in the current response to the linear voltage ramp, the present model appears to hold up well down to $\omega \sim 0.3$ s^{-1}.

5.5 Conclusion

We characterize the dynamics of a pyrrolidinium fluoroalkylphosphate ionic liquid in a M/IL/M structure based on experimental data and an equivalent circuit model. The admittance spectrum shows a rich frequency dependence indicative of rather complex relaxation processes that can describe the formation and removal of EDLs at the two electrode/IL interfaces. The range of frequencies for which the admittance was measured was $3\ \text{sec}^{-1} < \omega < 10^7\ \text{sec}^{-1}$, and these data were used to determine the parameters of an equivalent circuit model. Subsequent comparison of the results of that model with current vs. voltage measurements for different V(t) profiles yielded satisfactory agreement, even though the latter relies on extrapolated admittance values for frequencies lower than those of the experimental data range. It is clear that the dynamical response of devices that contain ILs as an effective 'dielectric' is quite complex. The structure examined here was particularly simple inasmuch as the effect of the gold electrodes on the dynamics could be taken to be instantaneous. This is not the case for organic field effect transistors gated with the help of an IL. In that case, charge carrier transit times in the organic material may be comparable to the response times of the IL and disentangling these effects will present

challenges.[35] Further work is underway to determine how electrode roughness, surface topography, ion sizes, and temperature affect the distribution of relaxation times found in these complex systems.

Chapter 6: Charge Accumulation in Electrical Double Layer Transistors

This chapter covers a study of the ionic liquid/semiconductor interface of organic EDLTs through the use of charge-modulation Fourier transform infrared spectroscopy in conjunction with electrical measurements. Specifically the system characterized was a rubrene single crystal/ion-gel interface. A spectroscopic signature for free charge carriers in the organic semiconductor was observed. Additionally it is unambiguously shown that a high density of free charge carriers exist on the rubrene/ion-gel interface even in absence of gate bias (V_g = 0V). Spectroscopy also reveals the saturation of free charge carrier density at the rubrene/ion-gel interface at Vg < −0.5 V, which is commensurate with the negative transconductance seen in transistor measurements. This work was published as Atallah, T. L.; Gustafsson, M. V.; Schmidt, E.; Frisbie, C. D.; Zhu, X. Y. Charge Saturation and Intrinsic Doping in Electrolyte-Gated Organic Semiconductors. *J. Phys. Chem. Lett.* **2015**, 6, 4840-4844.

6.1 Introduction

Organic thin film transistors (OTFTs) are central to low-cost, flexible, and/or disposable electronic and optoelectronic devices. A limitation to the large-scale application of OTFTs is the high gate voltages required to make the devices conduct. One successful strategy to overcome this constraint is to use electrolyte gating.[16, 125-127] The gate electrolytes, including ionic liquids and ion gels (in the presence of polymer matrices), achieve large capacitance ($C = 1 - 10\ \mu F \cdot cm^{-2}$) through the formation of a nanometer-

thick electric double layer at its interface with the organic semiconductor. This results in a high surface charge density ($\sigma = 10^{13} - 10^{14}$ cm^{-2}) accumulating in the semiconductor channel. Indeed, electrolyte-gated OTFTs have shown turn-on voltages < 1 V and represent promising routes to printed electronics.[89] The high capacitance of ionic liquid has also enabled the demonstration of gate-induced superconductivity[14, 128] and insulator-metal transitions[100, 129] in inorganic solids.

Despite the extensive use of electrolyte gating in OTFTs, little is known about the nature of the electrolyte/organic semiconductor interface. In the case of polymeric semiconductor thin films, such as poly(3-hexylthiophene) (P3HT), it has been shown that electrolyte gating can result in electrochemical mixing at the interface.[130-132] For single crystalline organic semiconductors, extensive mixing is unlikely, but Frisbie and coworkers demonstrated negative transconductance in electrolyte gated rubrene at a doping level of 10^{13} holes per cm^2.[36, 97, 133] These authors attributed the anomalous transport behavior to carrier localization at high doping densities, but the physical nature of the interface remains unclear.

Here we use charge-modulation Fourier transform infrared (CM-FTIR) spectroscopy[70-71, 134] to uncover the nature of electrolyte-gated doping of organic semiconductors at the model interface between single crystal rubrene and ion gel (IG). FTIR spectroscopy has been used before to great success in unveiling the band-like transport and low effective mass of holes injected into single crystal rubrene at lower charge densities ($\sim 10^{12}$ holes per cm^2) with SiO_2, parylene, or poly(para-xylylene) as dielectrics.[70-71, 134] Here, we apply the technique to the higher doping density enabled by electrolyte-gating. The ability to

optically monitor charge (hole) density in the organic semiconductor, in conjunction with electrical measurements, allows us to make two discoveries. Firstly, we show that a high surface hole density ($\sim 2 \times 10^{13}$ cm^{-2}), as measured from the free-carrier like hole absorbance in CM-FTIR spectroscopy, is formed in the organic semiconductor upon formation of the ion-gel/rubrene interface, in the absence of gate bias. Applying a positive gate voltage, $V_{appl} > 0$ V, we extract the free-carrier like holes introduced by this intrinsic doping. Secondly, we find that with an increasingly negative applied voltage, the change in surface free-carrier like hole density measured by optical absorption, $\Delta\sigma_{IR}$, reaches a plateau at $\sim 3 \times 10^{13}$ holes cm^{-2}, while the injected total charge density determined electrically, $\Delta\sigma_E$, continues to rise linearly. This saturation in the free-hole density on the rubrene crystal correlates well with the drop in conductance observed in transport measurements.[36, 97]

6.2 Device Structure and Electrical Measurements

The samples used in this study are fabricated from single crystals of rubrene. To enable the spectroscopic experiments, each rubrene crystal (roughly 3 mm × 1 mm × 50 μm) is glued at one end to (and not in electrical contact with) a thin film of Au deposited on a glass slide. The Au film serves both as a reflector for IR radiation and as a contact to the ion gel. Half of the top surface of the rubrene crystal is in contact with the ion gel, and the other half is coated with a thin film of Au which serves as a ground electrode.

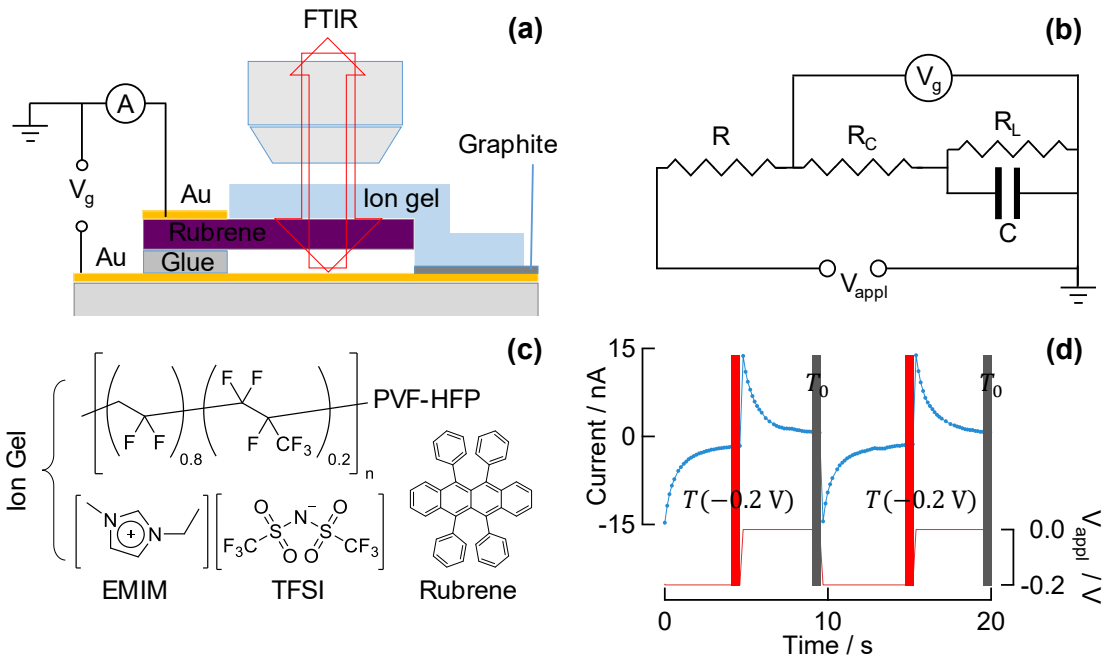


Figure 6.1 (a) Sample setup for the CM-FTIR experiment: A 40 nm Au thin film is deposited onto part of a rubrene crystal via a shadow-mask. The sample is glued and spaced from a gold electrode/mirror substrate (100 nm Au on glass). A piece of ion-gel is placed on top of the exposed rubrene (001) surface and part of the ion-gel is electrically contacted to the Au mirror with or without graphite paste. The device is connected with gold wires to a Keithley 6517a voltage source and electrometer. IR light is focused onto the device and, after reflection from the Au mirror, re-passes through the device and directed to the detector. (b) The equivalent circuit of the device. The applied gate voltage, V_{appl}, is from the Keithley 6517a, which also gives total current. A known resistor, $R = 11\ \text{M}\Omega$, is used in series with the ion-gel/rubrene capacitor. Quantitative modeling of the device gives a leakage resistance through the capacitor of $R_L = 1.0 - 0.2\ \text{G}\Omega$ (for $V_{appl} = -0.1$ to $-0.8\ \text{V}$) and a negligible contact resistance of $R_C \sim 2\ \text{M}\Omega$ (SM1). (c) Molecular structures of the ion gel and of rubrene. The ionic liquid consists of 1-ethyl-3-methylimidazolium (EMIM) cations and bis(trifluoromethylsulfonyl)amide (TFSI) anions. The polymer matrix is poly(vinylidene fluoride-co-hexafluoropropylene) (PVF-HFP). (d) The upper, blue graph shows the current, $\left(\frac{V_{appl}-V_g}{R}\right)$, flowing through R for two charging ($V_{appl} = -0.2\ \text{V}$) and discharging ($V_{appl} = 0\ \text{V}$) cycles. The lower, red graph shows the applied voltage, V_{appl}, of the corresponding cycles. The light red shade corresponds to when an CM-FTIR spectrum, $T(-0.2\ \text{V})$, is acquired after charging, while the grey shade corresponds to when an CM-FTIR spectrum, T_0, is acquired after discharging.

In the spectroscopic experiments, we apply a voltage between the two metallic contacts and measure the charging and discharging characteristics of the capacitor by

electrical methods, while simultaneously measuring the IR absorbance spectra of the ion-gel/rubrene structure. Figure 6.1 (a) shows the sample design and the experimental setup, and Figure 6.1 (b) shows the equivalent electrical circuit. Because the leakage resistance (R_L) through the device is one to two orders of magnitude higher than other resistances in the circuit, we have $V_g \approx V_{appl}$ in the steady-state. Figure 6.1 (c) illustrates the molecular structure of the ion-gel and rubrene.

Figure 6.1 (d) shows a typical I/V profile over several cycles of charging and discharging the capacitor with sharp steps in the gate voltage. We obtain the total injected charge density, $\Delta\sigma_E$, from the charging and discharging parts of the I/V curve as $\Delta\sigma_E = \frac{1}{A}\int I(t)\mathrm{d}t$, where A is the interface area between rubrene and ion-gel and $I(t)$ is the current. As we show below in Figure 6.3, a plot of $\Delta\sigma_E$ versus V_g shows a linear relationship, which gives a specific capacitance of $C = 8 \pm 3\ \mu\mathrm{F}\cdot\mathrm{cm}^{-2}$, in agreement with reported values.[87]

6.3 Spectroscopic Measurements

At the end of each charging/discharging cycle, we measure the optical transmission of the rubrene in a wide band of mid-IR wavelengths. The change in optical density due to the applied voltage is calculated as

$$\Delta OD = 1 - \frac{T(V_g)}{T_0} \tag{6.1}$$

where $T(V_g)$ and T_0 are the transmission spectra with the capacitor charged and discharged, respectively. Figure 6.2 shows how ΔOD changes over a range of applied voltages.

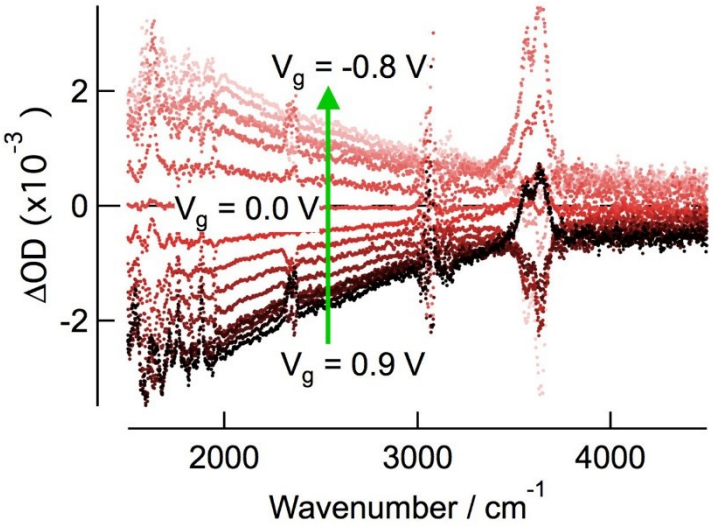


Figure 6.2 IR absorption spectrum at difference applied voltage across the rubrene capacitor, V_g: from bottom to top, V_g = 0.9 V to V_g = -0.8 V. All spectra are referenced to that at V_g = 0 V. The broad spectral feature, which increases with decreasing wavenumber, is assigned to free-hole absorption in crystalline rubrene. The sharp peaks on top of the broad feature are vibrational peaks of the ion-gel and rubrene. We note the presence of extraneous features at 3600 cm^{-1} (broad) and below 1600 cm^{-1} and then at 2500 cm^{-1} that correspond to atmospheric fluctuations in water and CO_2 respectively. The very low signal-to-noise ratio at just above 3000 cm^{-1} corresponds to C-H stretches in the rubrene and ion gel absorbing all of the photons of that energy range.

For negative applied bias ($V_g < 0$ V), we see an induced absorption ($\Delta OD > 0$) over a wide spectral range, with a magnitude that increases with decreasing wavenumber. This is a clear optical signature of free-carrier-like holes in rubrene, as shown by Li *et. al.*[134] With increasingly negative bias, the IR absorption increases, in proportion to the amount of injected holes.[38]

For positive bias, we expect the rubrene to be depleted of holes and hence the IR spectrum to remain unchanged with respect to $V_g = 0$. On the contrary, we find that this bias regime exhibits bleaching, which precisely mirrors the induced-absorption features seen for $V_g < 0$ V. This bleaching shows that free-carrier like holes are already present in the rubrene at $V_g = 0$, and gradually get expelled as we increase the bias voltage.

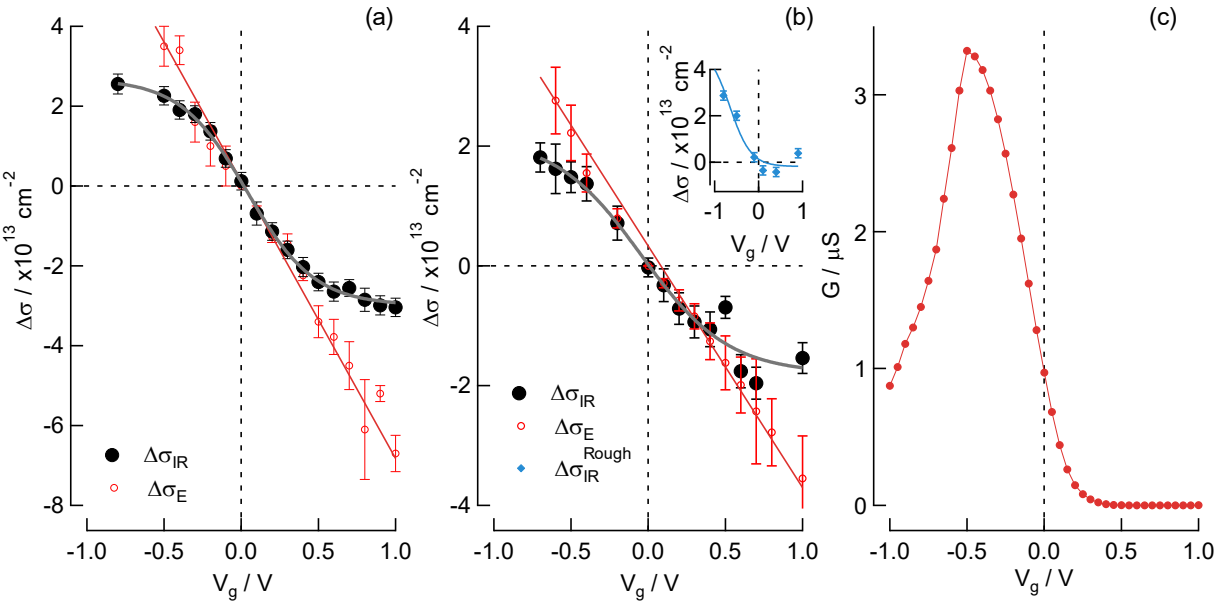


Figure 6.3 Fig. 3. Surface charge density in rubrene, $\Delta\sigma$, as a function of gate bias, V_g for a device with (a) graphite and (b) gold contact to the ion gel. The solid black circles are derived from the spectroscopic signature of free-holes in rubrene, $\Delta\sigma_{IR}$, and the solid grey curves are sigmoidal fits as guides for the eye. The red dots are obtained from electrical charging/discharging measurements, $\Delta\sigma_E$ and are used to calibrate the spectroscopy data (SM 3). Error bars are the standard error of the mean determined by the averaging of charge modulation measurements. Inset in (b) shows spectroscopic $\Delta\sigma$ obtained for a device fabricated from a rough rubrene crystal and the blue curve is a sigmoidal fit as guides for the eye. (c) Conductance, G, defined as the drain current, $I_d(V_g)$, divided by the source-drain voltage, $V_{sd} = -0.1$ V, of a rubrene [EMIM][TFSI] gated transistor as fabricated in reference [13]. The device turns on when $V_g > 0$ V due to the intrinsic doping of free charge carriers seen spectroscopically. The drop in conductance when $V_g < -0.5\,V$ corresponds to the saturation of free charge carriers observed in the CM spectra.

To trace the density of mobile holes at the rubrene surface as a function of bias voltage, we integrate ΔOD over the spectral range of the broad peak. For each spectrum (*i.e.* each value of V_g), this integral gives a scalar which is proportional to the density of optically accessible holes, $\Delta\sigma_{IR} \propto \int \Delta OD(\omega)\mathrm{d}\omega$. Since we know the total amount of charge injected into the device from the concurrent electrical measurement, we can calibrate $\Delta\sigma_{IR}$ to $\Delta\sigma_E$ in the low-bias regime (-0.2 V $< V_g <$ 0.2 V) where both data sets are linear in V_g. The resulting $\Delta\sigma_{IR}$ *vs.* V_g is plotted in Figure 6. 3 (a) and (b), along with the corresponding $\Delta\sigma_E$

vs. V_g, for two different samples. These devices were made with different materials for the electrical contact to the IG, but nonetheless show similar results.

In both samples, we see $\Delta\sigma_{IR} < 0$ for $V_g > 0$ V, that is, holes getting removed from the rubrene as the bias voltage increases from zero. The depletion only saturates for $V_g >$ 0.9 V, which marks the point where (nearly) all delocalized holes have been expelled from the rubrene. This corresponds to a density of $\sim 2 \times 10^{13}$ mobile holes per cm^2 present at the rubrene surface at $V_g = 0$ V.

We note that $\Delta\sigma_{IR}$ saturates also for strongly negative bias, $V_g < -0.5$ V, whereas the total amount of injected charge $\Delta\sigma_E$ (determined from the electrical data) remains linear in V_g over a wider range. The broad IR absorbance feature (Figure 6.2) through the semiconductor selectively probes the density of mobile and delocalized carriers. Thus, the excess injection/extraction of charge beyond the saturation points in $\Delta\sigma_{IR}$ is attributed to population and depletion of more localized sites, such as deep traps or small polarons, as discussed further below.

The intrinsic (zero-bias) doping at the rubrene interface is orders of magnitude higher than any residual doping in the bare crystal, and appears upon the formation of the semiconductor/ion-gel interface. This phenomenon is also observed in transport measurement, which shows conductivity through electrolyte-gated single-crystal rubrene transistors also in the absence of applied gate voltage.[36, 97] An example of such a measurement is shown in Figure 6.3 (c). This kind of intrinsic doping has not been observed in rubrene devices gated with conventional dielectrics (without mobile ions).[38, 68, 135] We

conclude that there is a thermodynamic driving force for capacitive charging of the organic semiconductor/ion-gel interface.

Upon forming the rubrene/ion-gel interface, the holes can latch to the surface of rubrene to stabilize the anions on the ion-gel side. This is followed by additional hole injection from the metal electrode (contacting rubrene) to reach a thermodynamic equilibrium. The opposite situation, i.e., the accumulation of electrons at the rubrene surface to stabilize cations in the electrolyte, does not occur because rubrene is predominantly a hole conductor. Holes move through rubrene with little trapping and a high mobility ($\mu h > 1$ cm2 V−1 s−1), while electron mobility is low ($\mu e < 1$ cm2 V−1 s−1) and is easily trapped. As such, there is a thermodynamic penalty for the electrons to detrap and reach the interface. Furthermore, injecting electrons into rubrene from the Au electrode is also unlikely due to a large energetic offset between the rubrene conduction band and the Au Fermi level.[136-137]

Support for this interpretation can be found in the work of Podzorov and co-workers who demonstrated the spontaneous accumulation of mobile holes and the healing of hole traps at the crystalline interfaces between organic semiconductors, including rubrene, and an inert polymer containing polar groups with large local dipole moment.[138] In their case, the intrinsically doped holes are stabilized by the local dipoles on the polymer chain, and the time profile of this doping process reflects the relaxation dynamics of the polymer chain.

Further support for this intrinsic doping mechanism emerges from a comparison between devices made from optimized rubrene single crystals with smooth surfaces

(Figures 6.3 (a) and (b), main panels) and crystals with rough surfaces (Figure 6.3 (b), inset). We obtain the latter by growing rubrene single crystals at temperatures and flow rates higher than those at optimal conditions.[139] Under these conditions, layer-by-layer growth in the rubrene *a*-*b* plane is less favorable, resulting in a rough crystalline surface topology with steps in the *c*-crystalline direction. The device with rough rubrene shows no intrinsic doping: the $\Delta\sigma_{IR}^{Rough}$ versus V_g curve shows an onset of injected hole density at $V_g = 0\,\mathrm{V}$. Since the hole mobility along the *c*-direction is much lower than that along the *a*-*b* plane and is nearly the same as electron mobility,[140] the transport of holes along the rough rubrene crystalline surface must overcome a large number of energy barriers due to steps along the *c*-direction. As a result, hole transport does not kinetically out-compete electron transport. Thus, an electric double layer cannot form without gate bias.

Having discussed the origin of the intrinsic doping, we now address the differences between $\Delta\sigma_E$ and $\Delta\sigma_{IR}$ for $|V_g| > 0.5\,\mathrm{V}$, as seen in Figure 6.3 (a) and (b). While spectroscopic measurements reveal saturation in $\Delta\sigma_{IR}$ at both the positive and negative extremes of V_g, the electrical data indicate a linear dependence of $\Delta\sigma_E$ on V_g in the gate bias range investigated. To explain this, it is important to note that the broad IR absorbance measures mobile carriers, while the electrical measurement counts the total charge. Hence, we conclude that holes injected at $V_g < -0.5\,\mathrm{V}$ occupy states that are too localized to be detected in the IR absorption. A related phenomenon is seen in measurements of electrical transport through transistor devices (Figure 6. 3 (c)), where the drain-source conductance shows a decrease under moderately to strongly negative gating. Previous publications have attributed this conductance drop to trapping by anion clusters forming at larger applied

biases, a model which is consistent with our data.[36, 97] In the positive saturation regime, $V_g > 0.5$ V, where the IR spectroscopy tells us that the rubrene is depleted of mobile holes, the linear relation between V_g and $\Delta\sigma_E$ still persists. This indicates further extraction of localized holes, *e.g.* from deep traps, which are IR-invisible and do not contribute to transport (Fig. 3c). Although transport measurements have generally shown the rubrene-electrolyte interface to be robust,[97] we cannot rule out electrochemical contributions to the capacitor charging current.[141]

6.4 Conclusion

In summary, we carry out combined spectroscopy and electrical measurements on a model electrolyte gated organic semiconductor interface: single crystal rubrene/ion-gel. We show unambiguously the presence of a high density of intrinsic doping at the organic semiconductor/ion-gel interface. We explain this intrinsic doping as resulting from a thermodynamic driving force. Spectroscopic measurements also reveal the saturation of free-hole like carrier density at the rubrene/ion-gel interface at $V_g < -0.5$ V, which is commensurate with the negative transconductance seen in transistor measurements.

Chapter 7: Ion Volume Effects in Electrical Double Layer Transistors

The work in this chapter explores the effects of ion volume (of the ions in the ionic liquid (IL) dielectric) on the performance of electrical double layer transistors (EDLTs). The complex environment of ILs at a charged interface is poorly understood due to complexities of ion mobility and extreme charge concentration. Currently, fundamental IL structure-device property relationships remain unclear. Here we explore the relationship between ion volume and several EDLT performance metrics. A set of ILs was carefully selected with differing ion pair volumes while keeping constant other structural elements. By changing ion pair volume, peak conductivity, capacitance, and mobility were tunable by a factor of 2-3. Surprisingly, by changing ion pair volume, a full volt shift in threshold voltage was possible, which is large compared to the few volt operating window of IL devices. This effect is explored in further detail in Chapter 8. Ion volume proves to be an important structural aspect in determining EDLT performance; however, other, as yet unexamined, factors appear to be significant as well. All work in this chapter was conducted by Elliot Schmidt in conjunction with C. Daniel Frisbie.

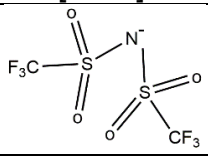
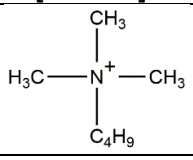
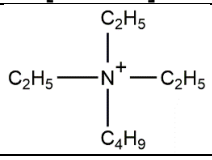
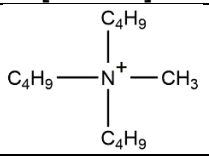
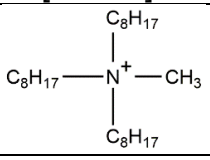
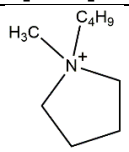
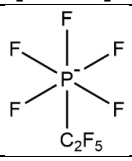
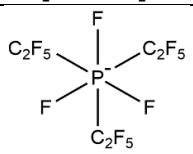
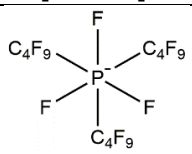
7.1 Introduction

Within the past decade, electrolyte gating, using ionic liquid dielectrics, has emerged as a simple way to inject a large amount of charge into semiconductors. Electrical double layer transistors (EDLTs) use an ionic liquid as the gate dielectric and have been

useful in fundamental transport studies.[100, 102, 106, 142-143] Charge densities as high as 10^{14}-10^{15} cm^{-2} have been observed in EDLTs.[14, 44, 144-145] Despite the benefits of ionic liquid dielectrics being known, our understanding of the structure-property relationships at work at charged electrode-ionic liquid interfaces is stark compared to our understanding of solid dielectrics. The mobility of the ions, coupled with the extremely high concentration of charge, poses a challenge for the development of double layer models. When it comes to choosing ionic liquids optimized for EDLT performance (low sheet resistance, high mobility, etc.), studies have often simply adopted a "shotgun" approach, testing a number of ionic liquids of various compositions before identifying the best one.[44, 105, 146-148] While this is currently the most practical method given the lack of understanding of these systems, learning more about how size/volume, functional groups, shape/bonding, and other structural properties affect EDLT performance will lead to the ability to both design novel high-performance ionic liquids as well as aid in choosing an ideal ionic liquid for a targeted application.

In this work, we seek to better understand how the structure of the ions comprising an ionic liquid (in particular here, their size) affects EDLT properties. To accomplish this, a set of volume-varying cations (with a common anion) and a set of volume-varying anions (with a common cation) were selected with the goal of minimizing the contribution of other confounding structural variables (Table 7.1). Here volume will refer specifically to the ion pair volume of a cation-anion pair. Ion pair volume is simple to measure and is defined as $V_{\mathrm{IonPair}} = \frac{M_w}{\rho \cdot Av}$ where M_w is the molecular weight of the ionic liquid, ρ is the density of the ionic liquid, and Av is Avogadro's number.

TABLE 7.1. Ionic liquid structures and associated ion pair volumes.

Set 1	**Anion**	**Cations**			
Name	[TFSI]$^-$	[N1114]$^+$	[N2224]$^+$	[N4441]$^+$	[N8881]$^+$
Structure					
$V_{IonPair}$ (nm^3)	--	0.47	0.56	0.63	0.94
Set 2	**Cation**	**Anions**			
Name	[P14]$^+$	[eFAP]$^-$	[teFAP]$^-$	[tbFAP]$^-$	
Structure					
$V_{IonPair}$ (nm^3)	--	0.38	0.61	1.09	

Within either set of ionic liquids in Table 1, the volume-varying ions are chemically similar (e.g. all cations in Set 1 are ammonium-based) and structurally similar with regards to shape/bonding.

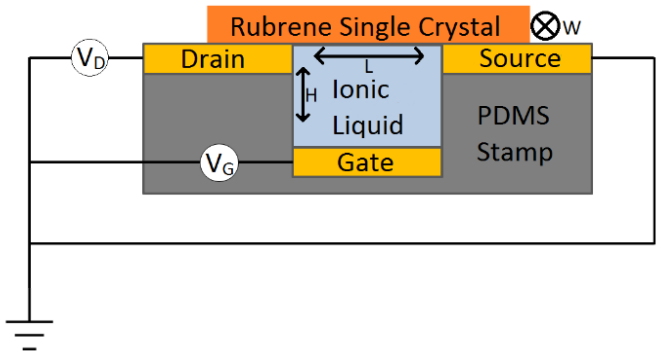


Figure 7.1 Cross section of rubrene single crystal electrical double layer transistor (EDLT). Dimensions are L = 50 μm, H = 5 μm, and W = width of rubrene crystal (variable).

The devices tested were single crystal rubrene EDLTs (Figure 7.1). These devices used the ionic liquids listed in table 1 as the dielectric material and were fabricated according to procedures found in Chapter 4.3.

7.2 Electrical Measurements

Charge transport behavior was characterized by drain current-gate voltage (I_D-V_G) measurements (Figure 7.2) and channel formation was characterized by the displacement current measurement (DCM) method.[44, 120, 149]

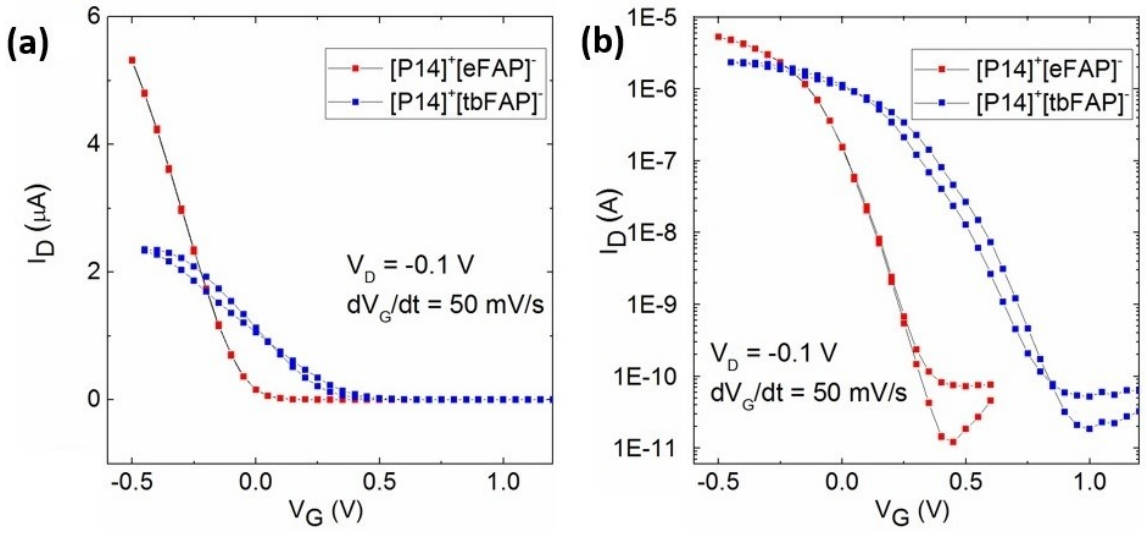


Figure 7.2. I_D-V_G curves for EDLTs using the smallest and largest anions of the Set 2 ionic liquids plotted in linear (a) and semi-log (b) scales.

Figure 7.2 well illustrates the strong effect that ion volume can have on performance, affecting multiple properties of the EDLT. The smaller $[eFAP]^-$ anion EDLT has both a distinctly higher maximum conductivity as well as less hysteresis than the larger $[tbFAP]^-$ anion EDLT. Interestingly, it is much more difficult to turn off the $[tbFAP]^-$

device. Typical I_D-V_G measurements can be found for all ionic liquids in Set 1 and Set 2 in Figures 7.3 and 7.4 respectively.

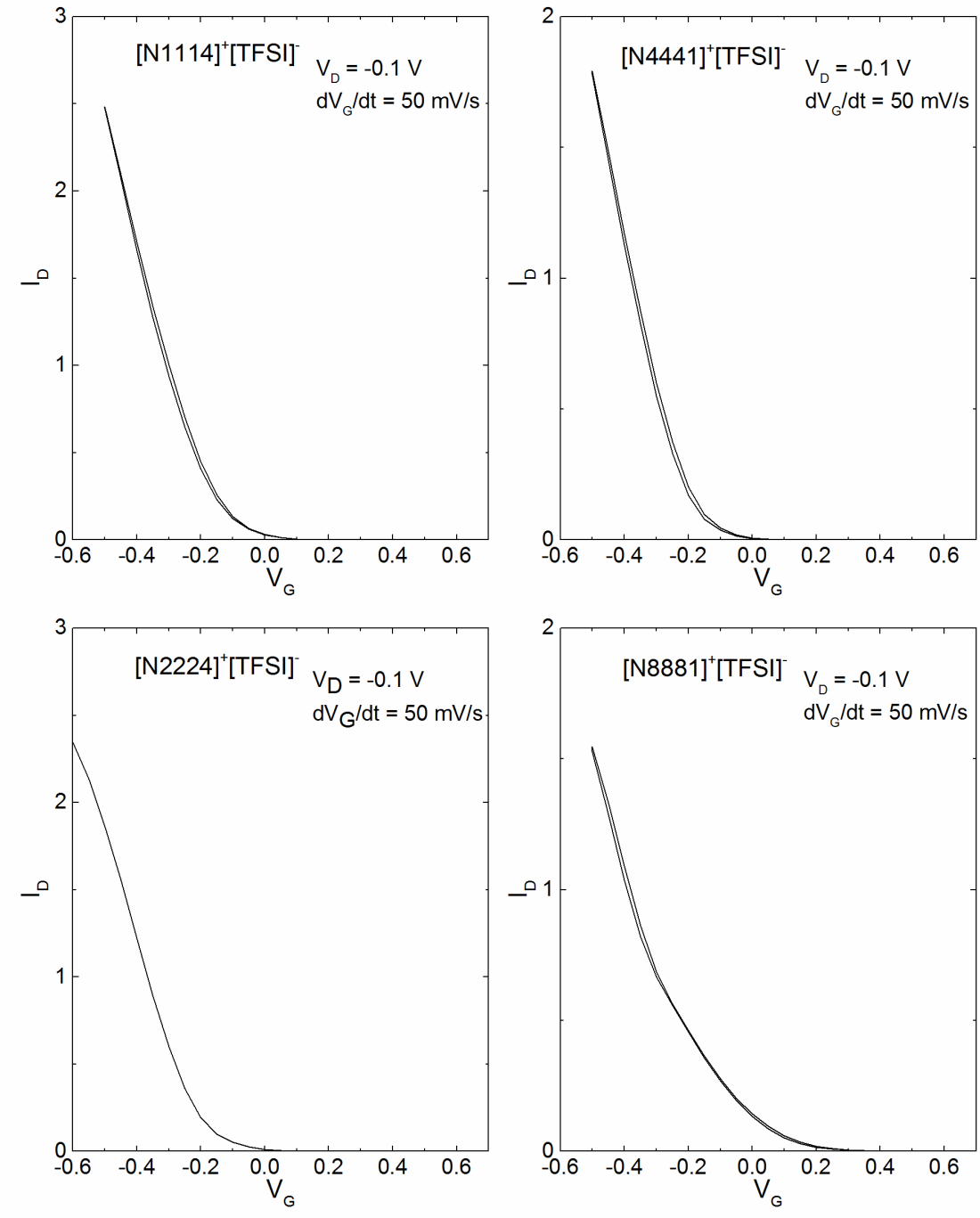


Figure 7.3 Typical I_D – V_G curves for EDLTs made with ionic liquids from Set 1.

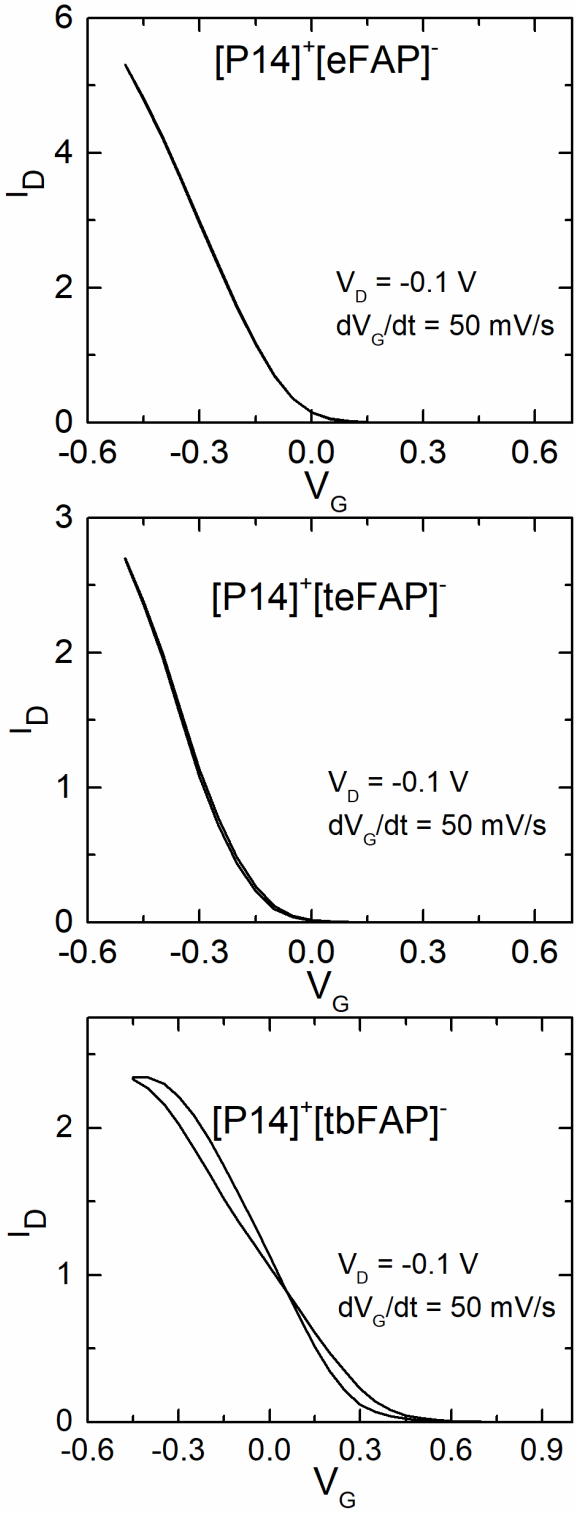


Figure 7.4 Typical I_D – V_G curves for EDLTs made with ionic liquids from Set 2.

Threshold voltage in metal-oxide-semiconductor field effect transistors (MOSFETs) is typically determined by linear extrapolation of the drain current (in the on-regime) to the voltage axis. This works well as MOSFETs exhibit a very linear I_D-V_G relationship in the linear regime ($V_D << V_G$). As can be seen in Figures 7.2, 7.3, and 7.4, however, the I_D-V_G relationship for EDLTs can have significant curvature even in the linear regime. This makes linear extrapolation of the drain current an extremely poor way to define threshold voltage as the value obtained from the extrapolation will depend upon at what point on the curve the extrapolation originated.

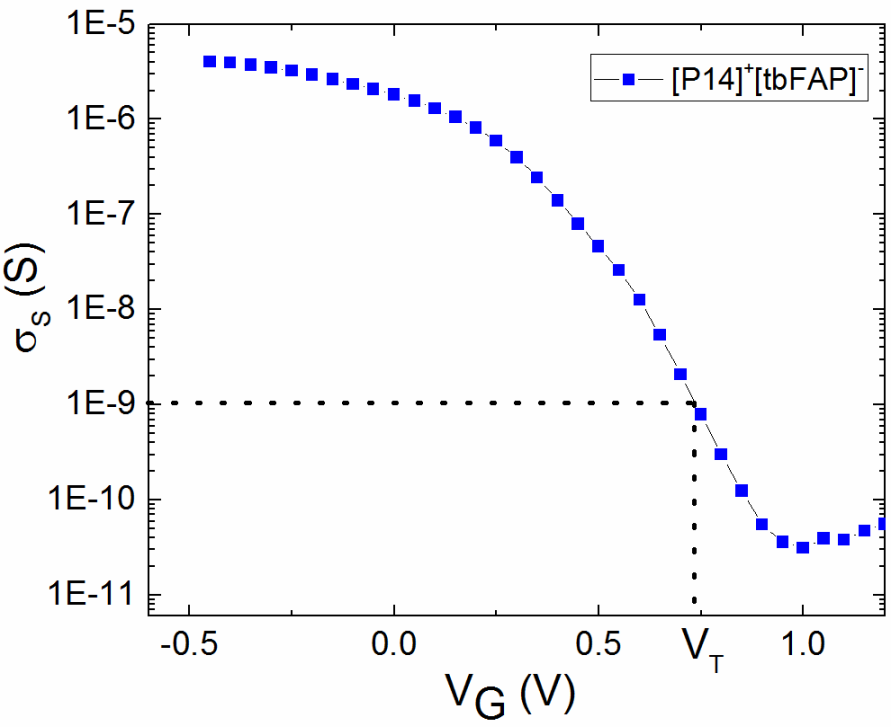


Figure 7.5 Determination of threshold voltage from an I_D-V_G curve of an EDLT. Threshold voltage (V_T) is taken to be the value of the gate voltage (V_T) when the sheet conductance = 10^{-9} S.

In order to have a more consistent, less subjective foundation on which to compare threshold voltage shifts between different ionic liquids, this work defines threshold voltage as the gate voltage at which the sheet conductance first exceeds 10^{-9} S when sweeping from positive gate voltage to negative gate voltage. This process is depicted in Figure 7.5.

The process of determining charge density through displacement current measurements is depicted in Figure 7.6. Displacement current measurements involve sweeping the gate voltage of the device linearly while simultaneously measuring current through the shorted and grounded source and drain electrodes. The displacement current is essentially the current going toward charging the capacitive gate electrode/ionic liquid/semiconductor stack. More information on this measurement can be found in Section 3.2.2.

Charge density is determined at a specific gate voltage by integrating a displacement current sweep in accordance with Equation 3.9. Prior to integration, the displacement current is corrected to account for parasitic charging effects. In order to do this in a consistent manner, the value of the displacement current when the gate voltage is equal to the threshold voltage ($V_G = V_T$) while sweeping from positive to negative is taken as the integration baseline (Figure 7.6 (b)). This current value is then subtracted from all displacement currents and integration of these correct currents occurs starting at the threshold voltage and ending at the voltage for which the charge density is desired. Charge density values as a function of ion size is shown in Figure 7.6 (c).

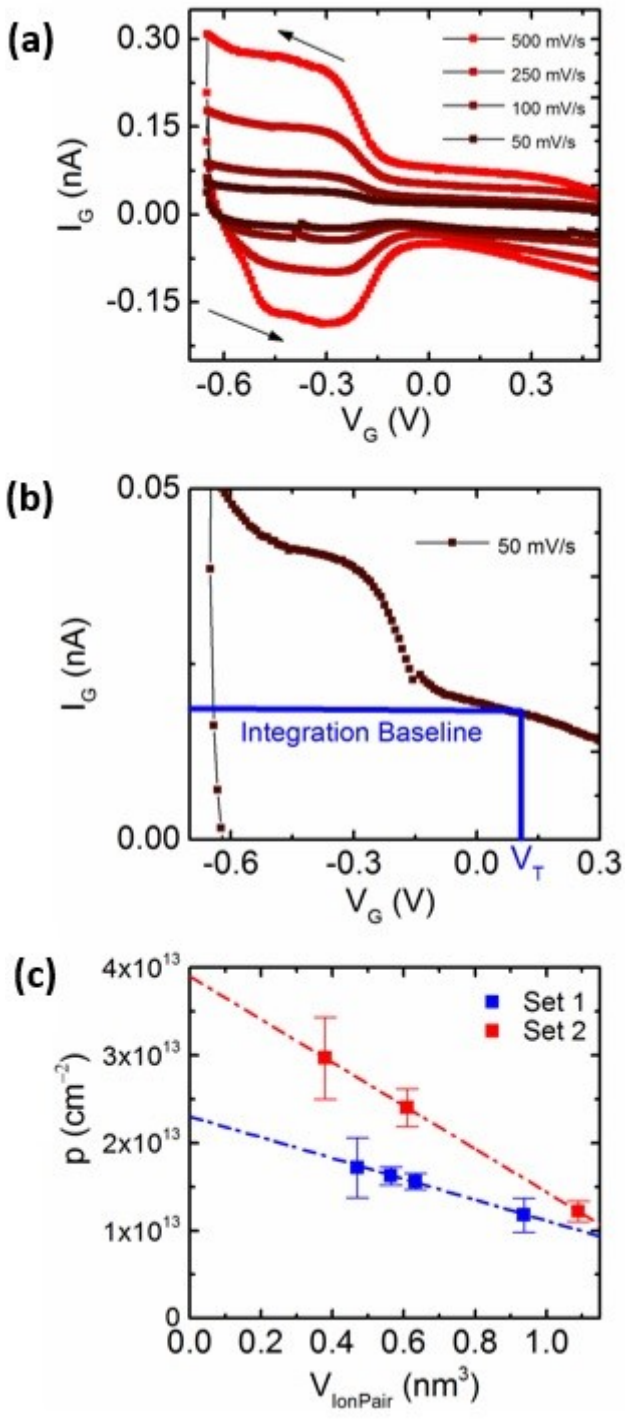


Figure 7.6 (a) Displacement currents of a $[N4441]^+[TFSI]^-$ EDLT at different sweep rates. (b) Baseline of displacement current integration taken to be current value at threshold voltage (V_T). (c) Charge density as a function of ion pair volume.

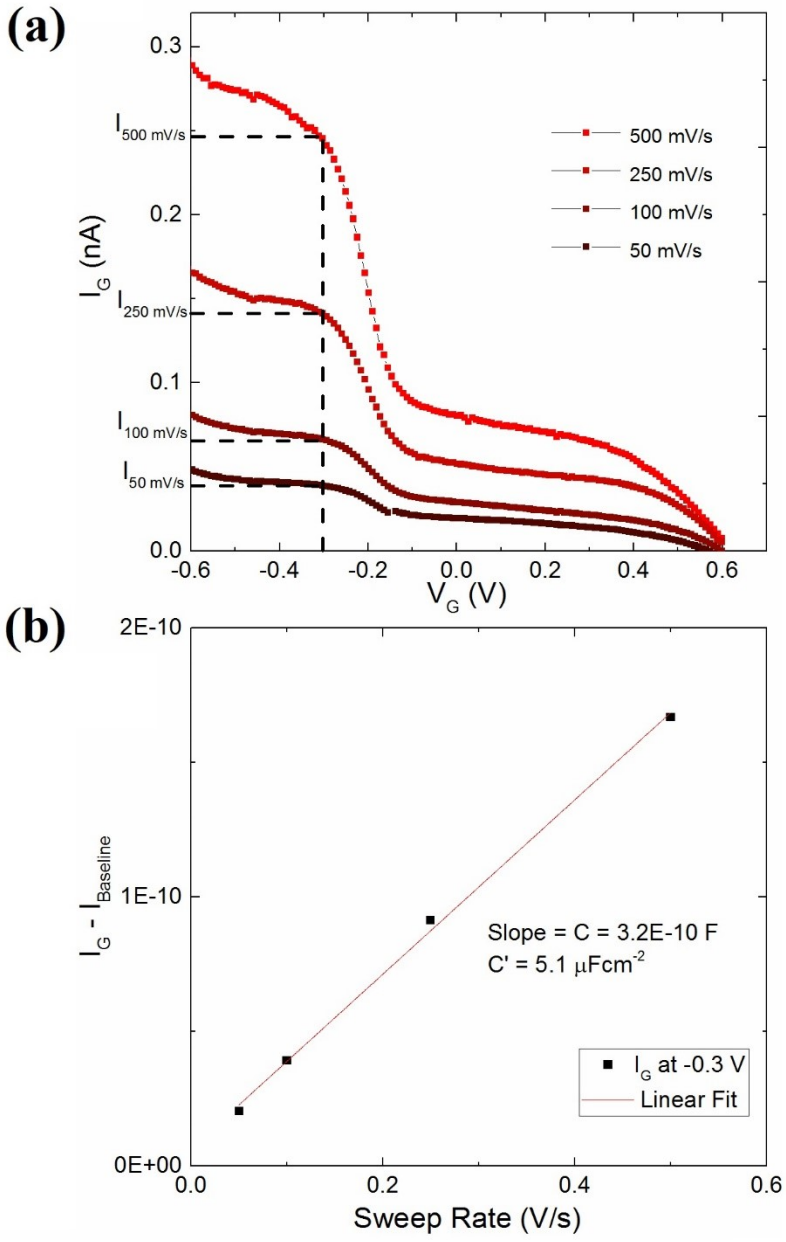


Figure 7.7 (a) Forward sweeps of a displacement current measurement of a $[N4441]^+[TFSI]^-$ EDLT at different sweep rates. (b) Capacitance determined from the slope of the displacement current versus sweep rate plot.

Capacitance is also determined from displacement current data and more in-depth information can be found in Section 3.2.2. The displacement current can be broken down

into two components, a capacitive component that goes into double layer formation and a residual component that goes into leakage of various kinds (resistive, faradaic reactions, etc.). As derived in Section 3.2.2 (Equation 3.12), we can write the total displacement current as:

$$I_{disp} = C\frac{\partial V_G}{\partial t} + I_{Res} \tag{7.1}$$

where I_{disp} is the total displacement current, C is the capacitance of the device, dV_G/dt is the sweep rate, and I_{Res} is the residual component of the current due to leakage mechanisms. The capacitive portion of the current is $C(dV_G/dt)$. Equation 7.1 is linear, and by plotting the I_{disp} (taken at specific value of V_G, shown in Figure 7.7 (a)) as a function of sweep rate, the capacitance (at specific value of V_G) is the slope of the resulting line as shown in Figure 7.7 (b).

7.3 Results and Discussion

Due to the non-ideal behavior of EDLTs compared to traditional metal oxide transistors (e.g. EDLT I_D-V_G curves in the "linear regime" have some curvature), there can be some ambiguity when determining carrier mobility from I-V data. In order to analyze volume effects first in the absence of this ambiguity, minimum sheet resistance was examined as a function of ion pair volume (Figure 7.8 (a)).

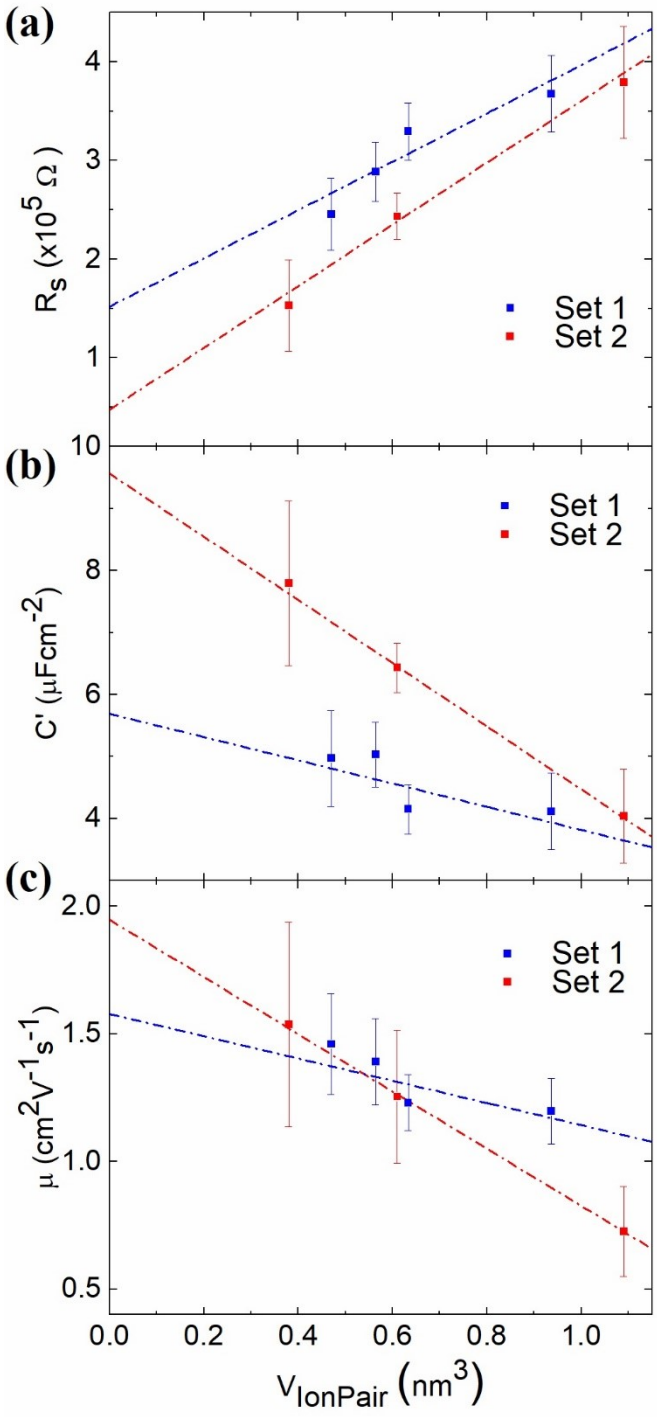


Figure 7.8 Minimum sheet resistance (a), capacitance (b), and hole mobility (c) as a function of ion pair volume in rubrene EDLTs using ionic liquids from Set 1 (blue) and Set 2 (red).

Sheet resistance was simply determined from the drain current, drain voltage, and device dimensions. As Figure 7.8 (a) shows, when either cation or anion volume increased, an increase in the minimum sheet resistance was observed, or, more simply put, increasing the volume of an ion in the ionic liquid made devices less conductive when fully on. The effect was stronger for anion variation as opposed to cation variation. In order to understand the effect of ion volume on conductivity, we must look separately at both the effects of ion volume on capacitance as well as charge carrier mobility.

The effect of ion volume on specific capacitance of the EDLTs is shown in Figure 7.8 (b). Increasing the volume of cations or anions led to lower capacitance EDLTs. This effect is likely due to being able to accommodate fewer ions in the double layer as ion volume increases.[147] Once again, this effect is more pronounced in the case of anions. This is not surprising as anions are the predominant ion nearest the semiconductor when the device is under negative gate bias. Because the anions are at a higher concentration than cations at the ionic liquid-semiconductor interface, anion volume changes will affect double layer structure more significantly than cation volume changes.

The effect of ion volume on charge carrier mobility is shown in Figure 7.8 (c). Carrier mobility in organic EDLTs is not constant with gate voltage and exhibits a distinct peak.[44] The value plotted in Figure 7.8 (c) is the maximum mobility measured in the voltage range of V_G = -0.3 V to -0.5 V. Mobility is determined through a rearrangement of Ohm's Law:

$$\mu = \frac{L}{W}\frac{I_D}{epV_D} \tag{7.2}$$

where L is the length of the semiconducting channel, W is the width of the rubrene crystal, I_D is the drain current, e is the elementary charge constant, p is charge density, and V_D is the drain voltage. All parameters were directly measured, except for charge density which was determined by DCM as described in section 7.2. While increases in cation and anion volume both lead to decreases in carrier mobility, changes in anion volume affect the mobility to a greater degree than changes in the cation volume. Changes in ion size likely affect the corrugation in local potential seen by charge carriers at the semiconductor/ionic liquid interface. This potential corrugation arises due to the fact that the ions at the interface are not infinitely small. For a sheet of dense, infinitesimal charge, the potential will be perfectly smooth. The potential of a sheet of discrete charge with finite spacing (e.g. ions at a surface) will exhibit a potential corrugation that depends upon the distance between charges. As the distance between charges increases (e.g. ion volume increase) the magnitude of the potential corrugation does as well. Potential corrugation can serve as charge trapping or scattering sites, negatively affecting charge carrier mobility. Because anion density is higher than cation density near the semiconductor (under negative gate bias), changes in anion volume likely have a greater effect on the potential corrugation than changes in cation volume.

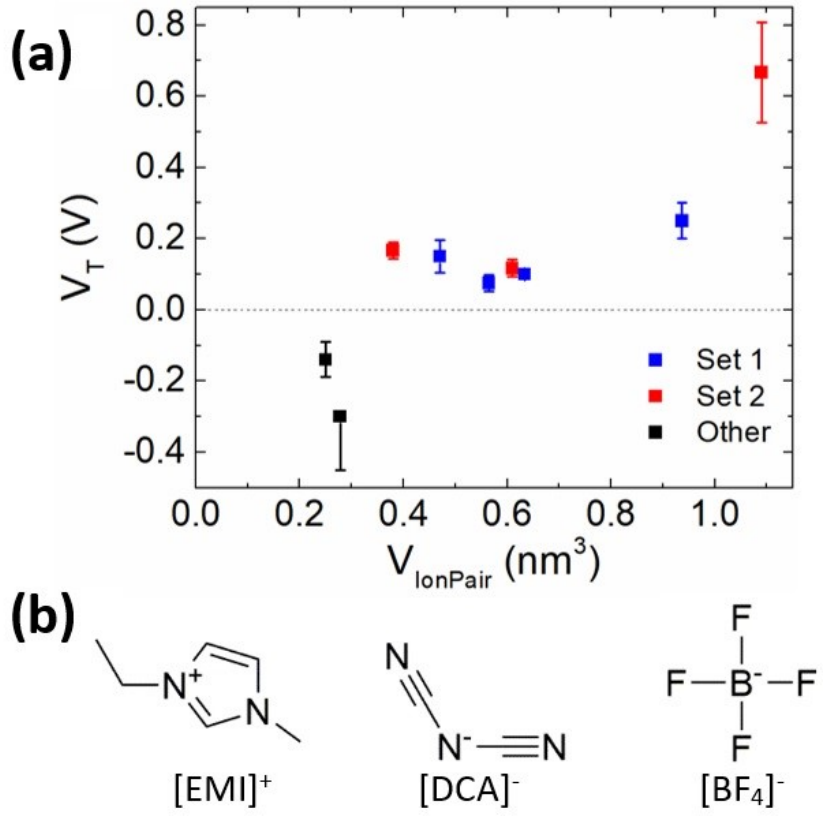


Figure 7.9 (a) Threshold voltage in a rubrene EDLT vs ion pair volume for the ionic liquids in Table 1 in addition to $[EMI]^+[DCA]^-$ ($V_{IonPair}$ = 0.28 nm^3) and $[EMI]^+[BF_4]^-$ ($V_{IonPair}$ = 0.25 nm^3). (b) Structures of $[EMI]^+$, $[DCA]^-$, and $[BF_4]^-$.

The effect of ion volume on threshold voltage is shown in Figure 7.9 (a). V_T was determined according to procedures found in Section 7.2. Interestingly, the threshold voltages of nearly all ionic liquids in Set 1 and 2 were relatively similar (~V_T = +0.1 V); however, the threshold voltage differed significantly for the largest cation and largest anion, which had a V_T of +0.3 V and +0.7 V respectively. To better ascertain if V_T depends on ion volume, two additional ionic liquids (Figure 7.9 (b)) with very small ion pair volumes were tested: $[EMI]^+[BF_4]^-$ ($V_{IonPair}$ = 0.25 nm^3) and $[EMI]^+[DCA]^-$ ($V_{IonPair}$ = 0.28 nm^3). Both of these small ionic liquids had negative threshold voltages. Looking at the

data as a whole, it appears that there exists some correlation of V_T with ion volume. By changing ion volume, threshold voltage was shifted by an entire volt, which is extremely significant given the operating range of EDLTs is often just a few volts. The relationship, however, is not completely monotonic indicating that there are other important confounding factors. Interfacial adsorption likely plays a non-negligible role in these systems, and variations in ion size are known to affect ion adsorption.[150-151] Differences in the specific adsorption of ions would lead to differing amounts of charge in the system in the absence of an external bias, and indeed, mobile charge has been observed spectroscopically in such devices without bias applied.[152] Ascertaining the origin of the significant differences in threshold voltage remains an active area of work.

7.4 Conclusion

It is apparent that ion volume changes have a significant effect on transistor performance with the ability to tune parameters like mobility and capacitance in EDLTs by a factor of 2 or more with currently available ionic liquids. Additionally, by comparing properties of EDLTs made with $[Ammonium]^+[TFSI]^-$ ionic liquids with those made with $[P14]^+[PerfluoroalkylPhosphate]^-$ ionic liquids it is also apparent that, for the same ion pair volume, there are significant differences in sheet resistance and capacitance (Figure 7.8). In other words, there are other equally important physical attributes of these ions that affect device performance besides their volume. This both reinforces the importance of keeping attributes like shape and chemical functionality fixed during this study in order to better isolate the specific effects of volume, and points to continued avenues of research required

to fully understand all structure-property relationships at work in ionic liquid-based devices. The apparent correlation of threshold voltage and ion pair volume is another continued area of work and is of significant interest given that a threshold voltage shift of 1 V was obtainable in devices with narrow operating windows of a few volts. This phenomenon is explored further in Chapter 8. While the role of ion size appears to be significant, much work is yet required to gain a full understanding of all structure-property relationships in ionic liquid-based devices.

Chapter 8: Effect of Ion Adsorption on Threshold Voltage in Electrical Double Layer Transistors

This chapter presents work done to explore the effects of ion adsorption and threshold voltage in rubrene single crystal electrical double layer transistors (EDLTs). The potential of zero charge (PZC) on a gold electrode is measured for nine ionic liquids of varying composition and size. Plotting the PZC of these ionic liquids on gold as a function of threshold voltage (V_T) for the same liquids in a rubrene EDLT using a gold gate electrode shows a close to 1:1 linear correspondence. Furthermore it is shown that it is the choice of the anion in the ionic liquid that largely determines both the PZC of the ionic liquid on gold as well as the threshold voltage of the rubrene EDLT. Computational modeling is ongoing; however, early results using a simple density functional theory hard sphere model with image charge effects indicate that while changes in ion volumes can change PZC significantly (100s of mVs), image charge effects alone cannot recreate the asymmetry of the PZC shift in the case of cation volume variation compared to anion volume variation. Ongoing work is focused on determining the origins of the cation/anion asymmetry. Experimental data was collected by Elliot Schmidt in conjunction with C. Daniel Frisbie, conceptual insight was contributed by Sha Shi and P. Paul Ruden, and computational modeling was performed by Kyeong-jun Jeong in conjunction with JR Schmidt and Arun Yethiraj.

8.1 Introduction

Electrical double layer transistors (EDLTs) show promise both for enabling discovery of novel electronic phase transitions as well as use in cheap and flexible printed or roll-to-roll manufactured electronics as described in Chapter 3. EDLTs have very beneficial properties such as being able to operate at low voltages and reach high conductivity levels. EDLTs also display some negative attributes compared to transistors made with more traditional solid dielectrics or vacuum dielectrics such as lower charge carrier mobility and lower operating frequencies due to large RC time constants.

Gaining a better understanding of the structure-property relationships at work in these devices can provide a route to minimizing the negative attributes of EDLTs and maximizing the positive attributes. Specifically, here structure-property relationship refers to how the structure of the ion (size, shape, composition, etc.) affects the performance properties of the EDLT (conductivity, mobility, threshold voltage, etc.).

As discussed in the previous chapter, ion pair volume appears to correlate roughly with observed changes in threshold voltage in rubrene single crystal EDLTs (Figure 7.9). The trend between ion pair volume and threshold voltage, however, does not appear to be monotonic. This indicates that there are likely other attributes of the ionic liquids that are a more direct cause of the threshold voltage shift but with which ion volume is also correlated.

Ion adhesion at the ionic liquid/gate electrode interface was identified as a possibly significant factor. In order to explore the effects of this interaction, the potential of zero

charge (PZC) on a gold electrode was measured for nine different ionic liquids using the immersion method.[153-155] The PZC of these ionic liquids on gold was then compared to the threshold voltage of rubrene single crystal field effect transistors using the corresponding ionic liquid and a gold gate electrode.

Computational modeling, to better understand the experimental results, is ongoing. Initial simple classical density functional theory models were created that approximate the ions in the ionic liquid as hard, charged spheres of varying diameters. The results of these models can successfully represent the magnitude of the PZC shift observed based upon ion volume changes; however, they cannot yet recreate the asymmetric nature of the PZC shift between cation and anion volume changes. More complex models are being developed as continued work is being done to understand the origins of this asymmetry.

8.2 Experimental Methods

EDLT device structure used for this work is identical to that in Chapter 7 and is shown below in Figure 8.1. Rubrene single crystals were grown by physical vapor transport according to procedures in Section 4.1. The gold-coated polydimethylsiloxane (PDMS) substrates were fabricated according to procedures found in Section 4.3. The structures of the nine ionic liquids used in this study and their associated ion pair volumes are shown in Figure 8.2. Ion pair volume is simple to measure and is defined as $V_{IonPair} = \frac{M_w}{\rho \cdot Av}$ where M_w is the molecular weight of the ionic liquid, ρ is the density of the ionic liquid, and Av is Avogadro's number.

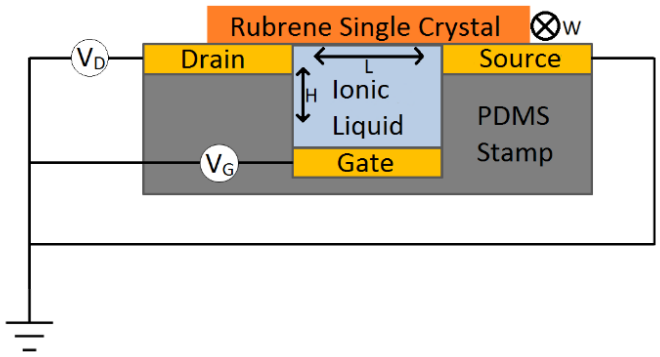
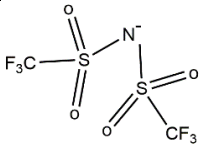
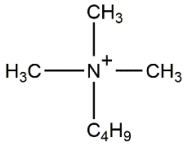
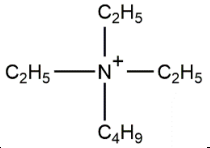
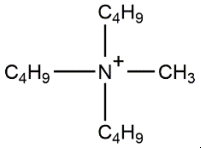
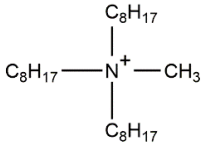
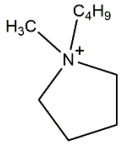
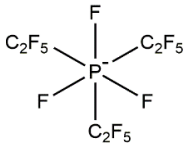
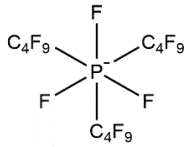
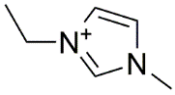
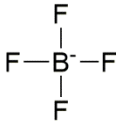
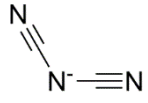
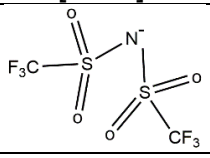


Figure 8.1 Cross section of rubrene single crystal electrical double layer transistor (EDLT). Dimensions are L = 50 μm, H = 5 μm, and W = width of rubrene crystal (variable).

Table 8.1 Structures and ion pair volumes of all ionic liquids studied in this work

Set 1	**Anion**	**Cations**			
Name	$[TFSI]^-$	$[N1114]^+$	$[N2224]^+$	$[N4441]^+$	$[N8881]^+$
Structure					
$V_{IonPair}$ (nm^3)	--	0.47	0.56	0.63	0.94
Set 2	**Cation**	**Anions**			
Name	$[P14]^+$	$[teFAP]^-$		$[tbFAP]^-$	
Structure					
$V_{IonPair}$ (nm^3)	--	0.61		1.09	
Set 3	**Cation**	**Anions**			
Name	$[EMI]^+$	$[BF_4]^-$	$[DCA]^-$	$[TFSI]^-$	
Structure					
$V_{IonPair}$ (nm^3)	--	0.25	0.28	0.43	

Potential of zero charge measurements were conducted by the immersion method. The immersion method is closely related to the dropping mercury electrode method of determining the PZC; however, it works for any solid electrode material. The definition of the PZC is the potential of the electrode at which the concentration of the cations and anions adsorbed to the electrode surface are equal. Another way of phrasing this is that at the PZC, the net charge density of adsorbed species is zero.

When an electrode is immersed in ionic liquid, charge flows to the electrode surface as a result of ion adsorption at the surface. Due to the different specificities of adsorption for the cations and anions, one species will adhere more than the other leading to a net charge on the electrode surface. The effective specificity of adsorption of the cation and anion species can be tuned by the potential of the electrode surface. The potential of the electrode surface can thus be set such that the cations and anions bind in equal number. At this potential (the PZC), the image charge densities of the adsorbed species cancel leading to no charge density on the electrode surface.

Now consider the case of an electrode immersed in ionic liquid that suddenly increases in area exposing clean electrode surface. Immediately ionic species will adsorb to the electrode surface inducing compensating image charges on the electrode surface. If the electrode is not at the PZC then current must flow to create the net compensating image charge. If, however, the electrode is at the PZC, then the sum of positive and negative image charges is 0 meaning no compensating current flows to the electrode surface.

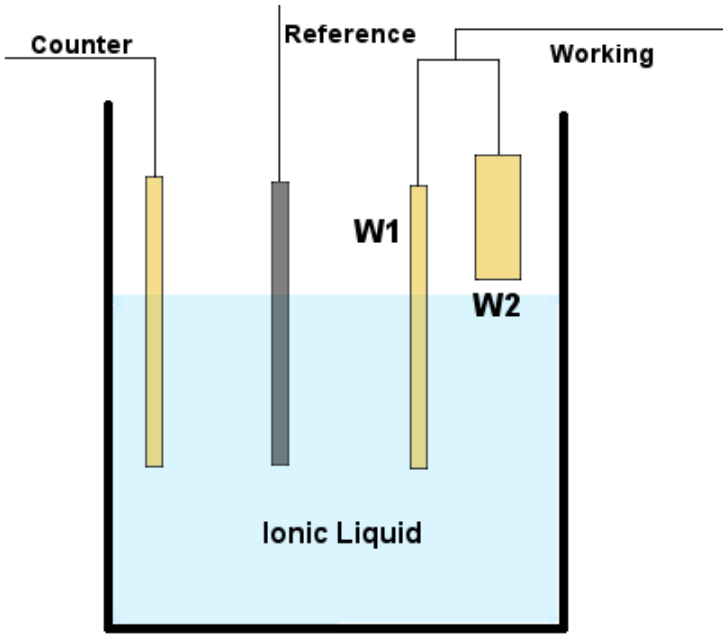


Figure 8.2 Schematic of the electrochemical cell used to make PZC measurements of different ionic liquids on a gold surface using the immersion method. The reference electrode was $Ag/AgNO_3$ (10 mM in acetonitrile) and the counter and working electrodes were gold.

The immersion method (Figure 8.2) involves measuring current flowing to the counter electrode as a working electrode (W2) is immersed into the ionic liquid while being held at a specific potential relative to the reference electrode. The working electrode in this setup is actually split into two parts, W1 and W2, which are shorted together. W1 starts in the ionic liquid solution and creates the electrical pathway to the reference and counter electrodes that allows for varying the potential of the working electrodes relative to the reference. The experiment begins by applying a voltage to W1 relative to the reference electrode. Because W1 and W2 are shorted together by a wire, W2 is at the same potential relative to the reference as W1. As this potential is applied, current is monitored

as a function of time. As the initial potential is applied, current spikes slightly as a result of changes in the charge density of the double layer at W1 (t = 0, Figure 8.3). This current decays rapidly, and after the initial current spike has decayed sufficiently the immersion of W2 in the ionic liquid begins. When the immersion is conducted at a constant rate, the current quickly increases and then roughly plateaus until the electrode is fully immersed at which point the current decays. The sign of the current during immersion indicates whether the electrode is positive or negative of the PZC and the total area under the current curve during immersion is indicative of how far the electrode potential is from the PZC. When no current is measured while the working electrode is immersed into the ionic liquid, then the working electrode is at the PZC.

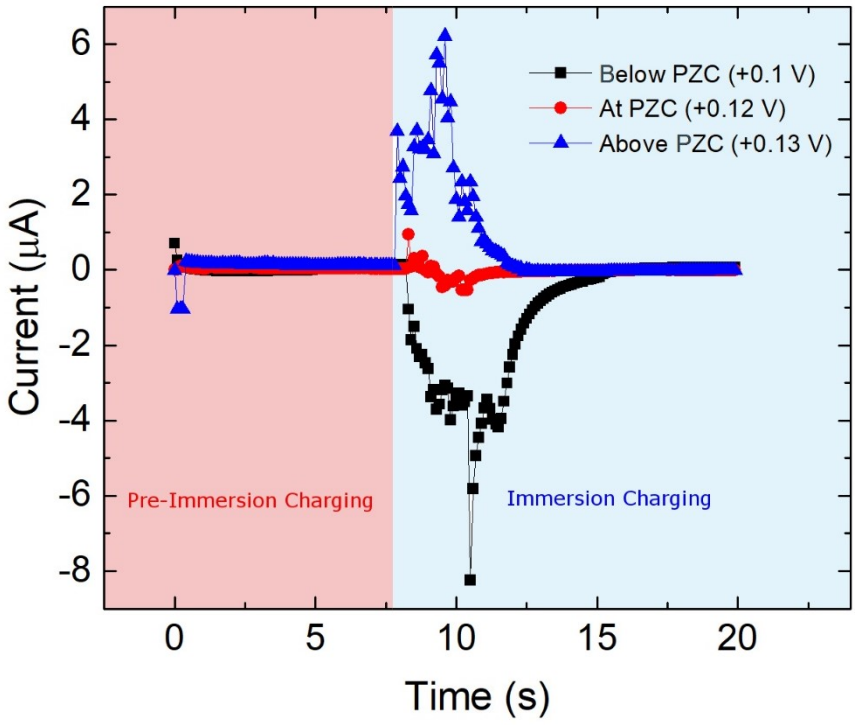


Figure 8.3 PZC determination via immersion method. The PZC is identified as the voltage at which there is no current flow when the electrode is immersed in the ionic liquid.

Threshold voltages were determined from I_D-V_G measurements (Figure 8.4). Drain current (I_D) was measured as a function of gate voltage (V_G) as the gate voltage was linearly swept from positive to negative and back to positive at a sweep rate of 50 mV/s and a drain voltage (V_D) of -0.1 V. Due to the non-linear behavior of EDLTs in the "linear regime" ($V_G >> V_D$), the threshold voltage cannot be reliably determined from linear extrapolation of the drain current. Instead, threshold voltage here is defined as the value of V_G at which the device first reaches a sheet conductance of 10^{-9} while sweeping V_G from positive to negative.

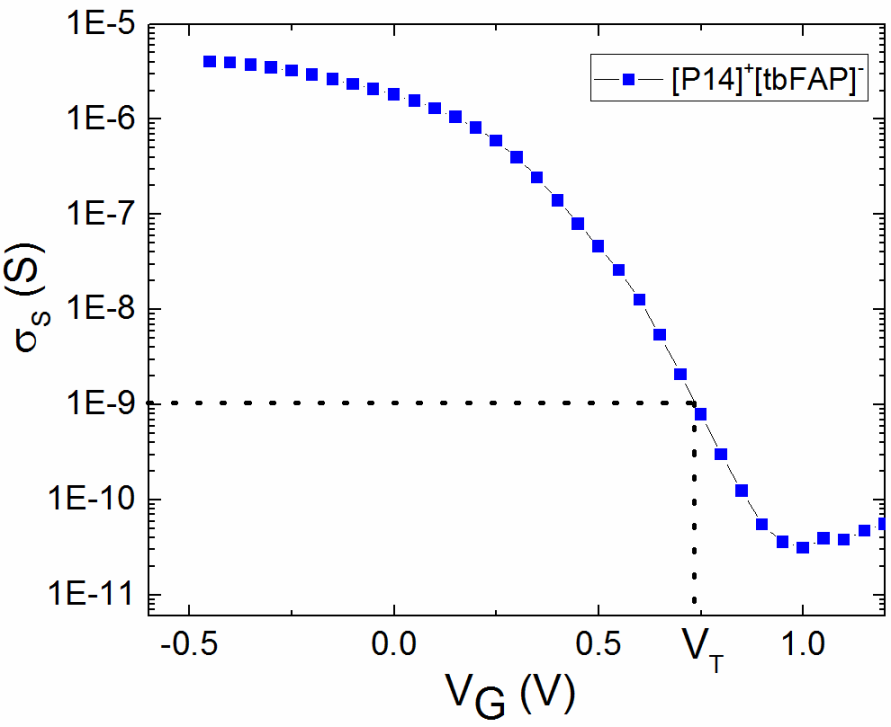


Figure 8.4 Determination of threshold voltage from an I_D-V_G curve of an EDLT. Threshold voltage (V_T) is taken to be the value of the gate voltage (V_T) when the sheet conductance = 10^{-9} S.

8.3 Discussion of Results

A plot of the PZC on gold as a function of threshold voltage in a single crystal rubrene EDLT is shown in Figure 8.5 for the nine ionic liquids listed in Table 8.1.

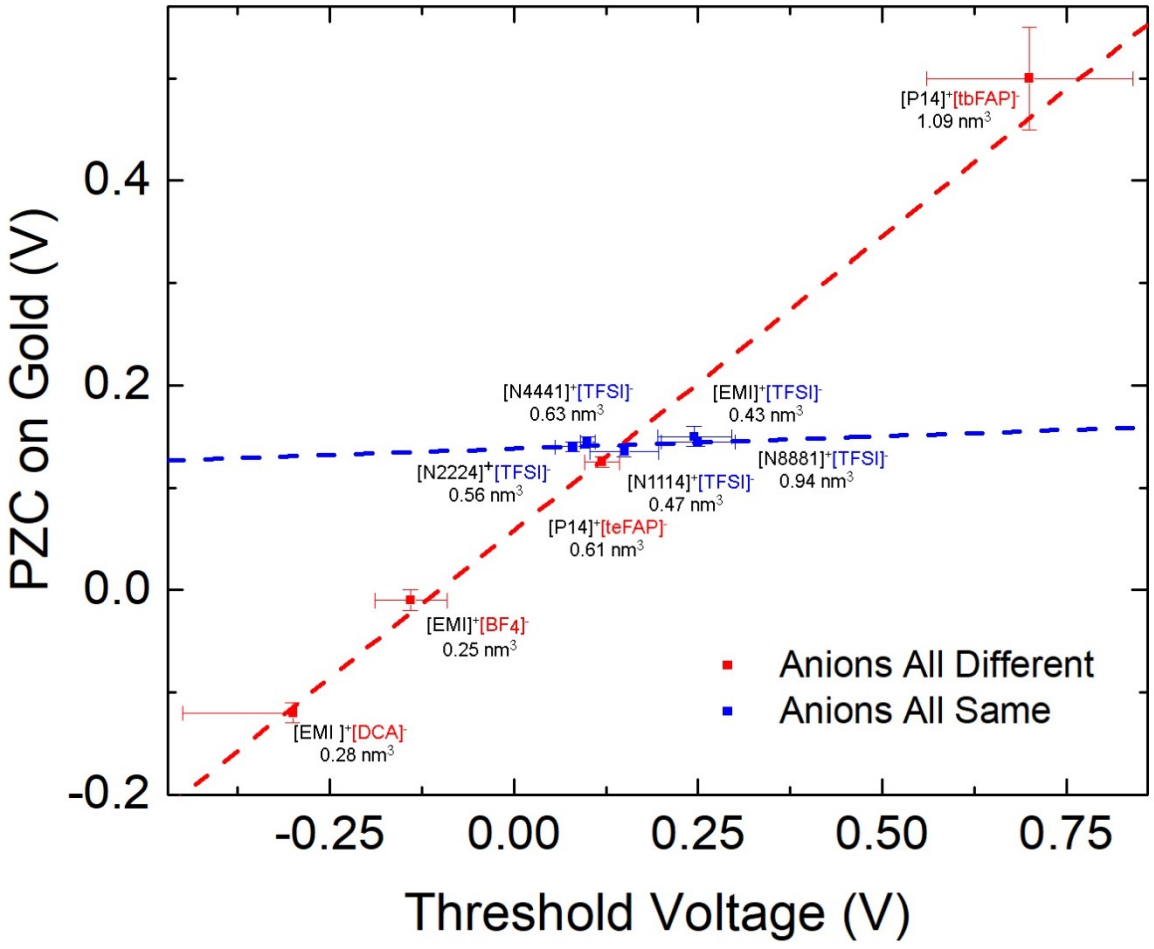


Figure 8.5 Potential of zero charge on a gold electrode (versus a 10 mM $Ag/AgNO_3$ reference electrode) as a function of threshold voltage shift in a single crystal rubrene EDLT for the nine ionic liquids listed in Table 8.1. The red and blue dashed lines are linear regressions of ionic liquid subsets that have all different or all the same (TFSI) anions respectively. Changing anions appears to significantly affect both PZC and threshold voltage while changing cations essentially has no effect on PZC and a small effect on threshold voltage.

Several interesting features can be noted in this plot. Foremost, there appears to be a strong, nearly 1:1 relationship between the potential of zero charge and threshold voltage for the various ionic liquids. To phrase this another way, ion adsorption is likely one of the most significant factors determining threshold voltage in rubrene EDLTs.

Interestingly, changing the anion in the ionic liquid has both a substantial effect on the PZC as well as the threshold voltage; however, changing the cation in the ionic liquid while holding the anion constant has essentially no effect on the PZC as well as only a small effect on the threshold voltage. The strong dependence of the PZC on anion structure and weak dependence of the PZC on cation structure has been shown previously for electrolyte solutions on gold and mercury electrodes by Bodé et al.[156-157] The strong relationship between PZC and threshold voltage for changes in anion structure specifically indicates that adsorption of anions is a very significant factor in these EDLTs. The small, but not insignificant, threshold voltage shift measured for cation variation coupled with the negligible change in PZC for cation variation indicates, however, that there is still a non-negligible contribution to threshold voltage from sources other than ion adsorption.

In order to better understand the effect of ion structure on ion adsorption, classical density functional theory models are being developed in work that is still on-going. Figure 8.6 shows the results of a preliminary model where ions near a gold electrode surface were modeled as simple hard spheres of differing diameters. Differential capacitance was calculated as a function of potential. The potential of zero charge is located at the local minimum in the differential capacitance versus potential plot. The reason that there is a

local minimum in differential capacitance at the potential of zero charge is because the magnitude of the charge density on the electrode is minimized (zero) at the potential of zero charge. As a result, the Coulombic attraction of the ions to the surface is also minimized, and therefore the average distance between the ions and the surface is at a maximum. If you simplistically model the surface and the closest layer of ions as the two plates of a parallel plate capacitor, then it logically follows that as the distance between the plates reaches a maximum, the capacitance reaches a minimum.

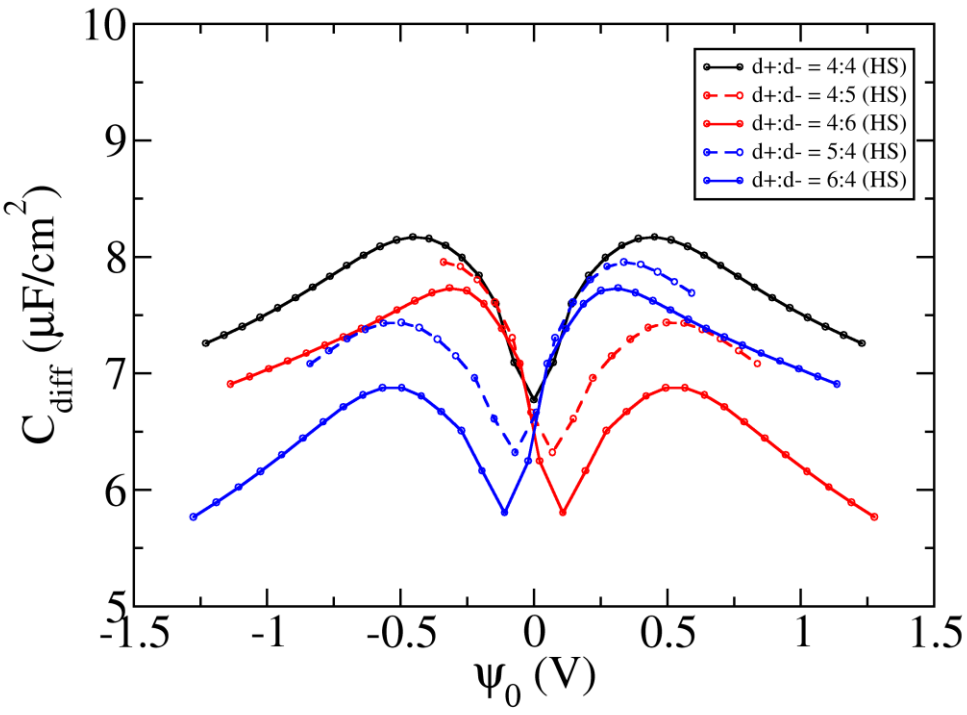


Figure 8.6 Differential capacitance as a function of potential for various diameter ratios of cations and anions. The potential of zero charge is the value of Ψ_0 at the local minimum in the differential capacitance of each curve.

Specifically, Figure 8.6 shows differential capacitance curves as a function of potential for a variety of cation diameter to anion diameter ratios (d+:d-). Comparing the d+:d- = 4:6 and the d+:d- = 6:4 curves, the PZC shifts by ~220 mV, which is on the same order of magnitude as the ~600 mV shift in PZC measured experimentally for the smallest and largest anions. These preliminary hard sphere model results allude to size being a major factor determining ion adsorption. What the hard sphere models currently fail to replicate, however, is the asymmetry of the PZC shift as cations and anions change size. The experimental results presented in Figure 8.5, and those of Bodé et al.[156], show almost no influence of the cation size on the PZC; however, the model shows an equally large shift in PZC for cation size changes and anion size changes. Next steps include trying to replicate the asymmetry of the cation and anion PZC shifts, possibly with the incorporation of a Leonard-Jones potential in the model, and if successful, further explore what specific structural elements contribute to the asymmetry.

8.4 Conclusion

A strong correlation between ion adsorption and threshold voltage for single crystal rubrene EDLTs was shown providing evidence that ion adsorption is one of the main factors determining threshold voltage in these devices. Specifically, potential of zero charge measurements on gold electrodes, conducted via the immersion method, were correlated with threshold voltage measurements for rubrene EDLTs using gold gate electrodes for nine different ionic liquids. Anion adsorption was found to play a more prominent role in threshold voltage shifts than cation adsorption, though small changes in

threshold voltage with cation variation and no corresponding change in the potential of zero charge with cation variation indicates that there are other contributions (if not quite as significant) to threshold voltage from factors other than ion adsorption. To better understand the experimental results, computational models are being constructed in work that is on-going. Preliminary results indicate that ion size differences are capable of PZC shifts on the same order of magnitude as measured experimentally (100s of mV). Continued work focuses on recreating the asymmetry in the cation/anion variation behavior and gaining a better understanding on the origin of this asymmetry.

Chapter 9: Directions for Continued Work

9.1 Structure-Property Relationships in EDLTs

Electrical double layer transistors show immense promise as both research tools and components of cheap, printable or roll-to-roll manufactured electronics due to the high capacitance, printability, and low-temperature processability of ionic liquid dielectrics. The benefits of EDLTS; however, do not come without drawbacks. In order to improve viability in commercial applications, several performance aspects of these devices must be addressed.

First and foremost, stability is a concern that must be addressed in EDLTs. Here specifically, stability refers to the ability for the ionic liquids to slowly (or sometimes quickly) dissolve or etch organic semiconductors over time[158] (inorganic semiconductors generally show a reduced solubility in ionic liquids, and so device degradation is a lesser concern). Ionic liquids can act as powerful solvents and indeed are being explored extensively as non-volatile, green solvents in the field of organic chemistry.[77, 159] Understanding how the structure of ions in the ionic liquid affects its ability to dissolve different classes of semiconducting material will be of utmost importance to being able to pair compatible ionic liquids and semiconductors for long device lifetimes.

Besides dissolution of the semiconductor surface, electrochemical reactions between the ionic liquid and the semiconductor surface is also a concern. As can be seen in Figure 9.1, reactions between ionic liquids and crystal surfaces can significantly affect the surface potential at the surface of the semiconductor leading to significant changes in charge transport behavior. Ion structure appears to be very closely tied to the

electrochemical window and reactivity of ions.[147] For instance, saturated ions appear to have significantly larger electrochemical windows than those containing aromatic groups. Additionally, larger ions may also show an increase in stability. Much of this work is very preliminary, however, and a significant amount of work remains to optimize ion structure to minimize electrochemical reactions with the semiconductor surface.

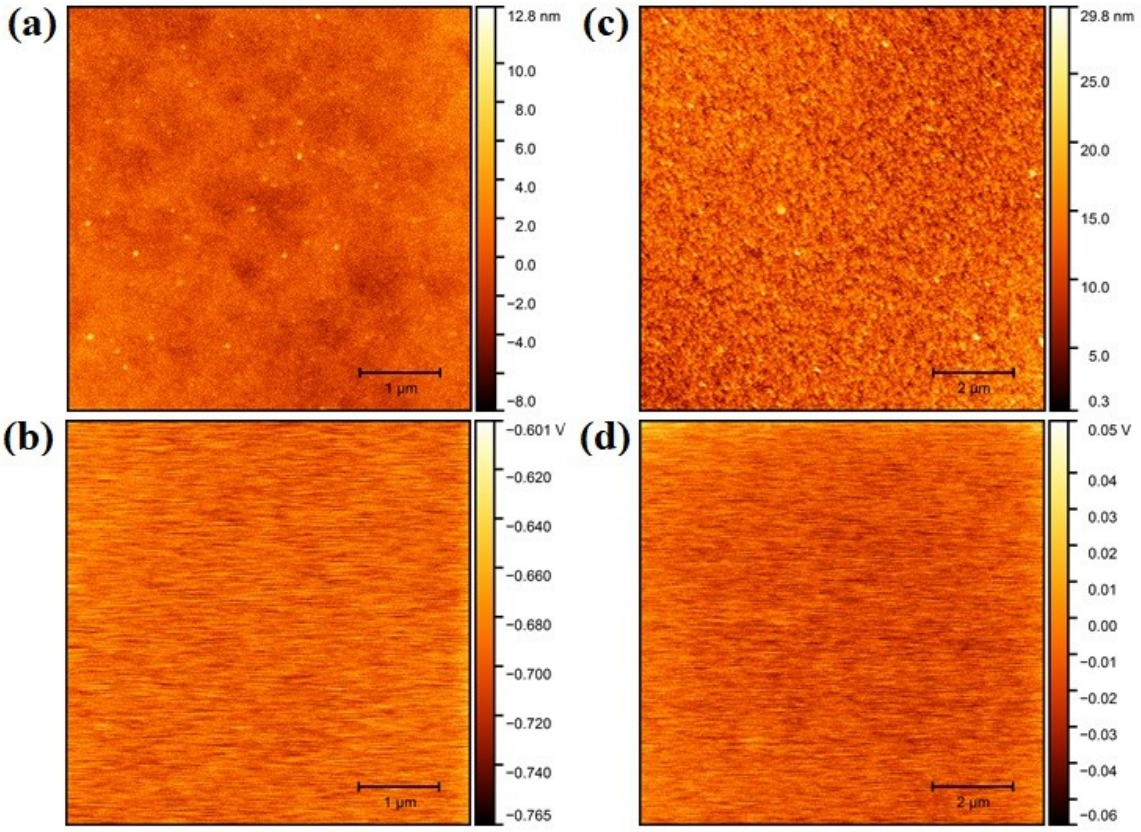


Figure 9.1 Surface height (a) and surface potential (b) mapping of a C60 crystal before contact with ionic liquid and surface height (c) and surface potential (d) of a C60 crystal after gating for 1 hour in DEME-TFSI. Note the increased surface roughness and positive shift in surface potential after gating.

As discussed in Chapter 3, the RC time constant of EDLTs is currently large compared to metal oxide-based transistors and, as such, limits the operating frequency of

EDLTs. Both the ionic conductivity and the double layer capacitance of the ionic liquid contribute to the total RC time constant of an EDLT. Both of these properties are deeply tied to ion structure. Generally speaking, larger ions have a larger cross-sectional area and stronger intermolecular dispersion forces leading to a higher viscosity and lower conductivity ionic liquid. As shown and discussed in Chapter 7, capacitance is generally larger for smaller ions simply because the charge center of the ion is capable of getting closer to the electrode surfaces.

Ion size is not the only significant factor affecting device capacitance. The ability of an ionic liquid to wet can play a significant role in the total capacitance of the ionic liquid on all but the most perfectly planar electrodes. On rougher, more porous electrodes it is possible to have an ionic liquid with large ions to have a higher total capacitance than an ionic liquid with smaller ions even if the larger ion liquid has a lower specific capacitance than one with smaller ions. Such differences can be due to difference in the ability of a large ion ionic liquid to wet small pores and pits in an electrode more effectively, due to its lower surface energy, which translates to a larger accessible electrode area than in the case of the ionic liquid with smaller ions.

Large capacitance is generally viewed as a positive attribute of ionic liquids as it allows for low operating voltage; however, having the largest possible capacitance is not necessarily the ideal scenario. In applications where frequency is important and operating voltage requirements are less stringent, a lower capacitance ionic liquid may be the ideal candidate as the RC time constant will be reduced allowing for faster switching. The design specification for operating frequency and permissible operating voltage will differ on a per-

application basis and therefore ideal capacitance values will vary on a per-application basis as well; thus, it is important to have a more well-developed sense how structure affects capacitance rather than simply the simple notion that smaller ions lead to a higher capacitance.

EDLTs also face the unique situation that, unlike metal oxide transistors, cooler temperatures can be as detrimental to performance as higher temperatures. In something like a computer processor, lower temperatures will almost always ensure the ability to run the processor at even higher frequencies due to increases in carrier mobility. While carrier mobility in some EDLTs increases with decreasing temperatures, a decrease in temperature will significantly decrease the conductivity of ions in the ionic liquid leading to a larger RC time constant for the device. Such a phenomenon is not observed in solid dielectrics. Additionally, the capacitance of ionic liquids is dependent on temperature as well. Furthermore, ionic liquids are capable of freezing if temperatures are decreased sufficiently leading to a completely non-functional transistor. Many ionic liquids have melting temperatures between -50 °C and 0°C; however, many also have melting points very near to room temperature. A low melting point is desirable in near-room temperature applications. Melting points in ionic liquids are a complicated combination of molecular symmetry, coulombic interactions, and dispersion interactions. Generally speaking, the less symmetric the ions of an ionic liquid are, the lower the melting point is, and consequently many of the common ionic liquids have a long alkyl chain tail and a short alkyl chain tail that produces asymmetry. Simple symmetry reducing changes can change the melting temperature of ionic liquids hundreds of degrees.

The primary intermolecular interaction between the ions in ionic liquids is the Coulombic interaction between the charge centers of the ions. Ionic liquids are only able to remain liquids at room temperature due to structural elements that disrupt the normally strong Coulomb interaction that exists in ionic materials. Specifically, the ion structures serve to keep the charge centers of opposite charges further apart than they would be in an ionic solid like NaCl, and this increase in distance weakens the ionic attraction enough for the ionic material to remain in a liquid state at room temperature. The primary means for increasing the distance between charges is simply to do so sterically by increasing the size of the ions. Consequently, there are exceedingly few known room temperature ionic liquids where one of the constituent ions is a single atom and none where both constituent ions are single atoms.

Melting point, however, does not simply continue to decrease with increasing ion size. While Coulombic interactions between ions continue to decrease with increasing size, dispersion interactions increase in strength as ions grow in size. This interaction is strong enough to raise the melting point of the ionic liquid well above room temperature. There, therefore, exists a "sweet spot" for ion size where the ionic liquid reaches its minimum melting temperature, all other structural elements being equal. Obviously size and symmetry are not the only factors affecting melting temperatures of ionic liquids. The chemical composition of the ions likely plays a significant role in melting temperature as would structural elements like aromatic rings.

Charge carrier mobility in the semiconductor is another property that seems to also be linked to the ion structure of ionic liquids as evidenced by the work in Chapter 7.

Specifically, it seems that smaller ions could lead to smaller potential corrugations at the semiconductor surface and a correspondingly larger mobility due to shallower charge traps. It is not clear if this phenomenon carries to other semiconductors and ionic liquids, which presents an interesting path for future work. At a minimum, ion structure effects on charge carrier mobility should not be discounted when seeking to optimize EDLT performance.

Hopefully it has been made exceedingly clear all of the structure-property relationships that exist in ionic liquids, how important they are, how complex they are, and how little is known about them. Now consider this: almost every single structural change made to an ion in an ionic liquid affects not just a single property, such as capacitance, but also every other property discussed as well…often in an inverse or undesirable way. Invariably then, choosing an ideal ionic liquid for an application will be a game of compromises…to figure out how to gain as much as possible while losing as little as possible. In order to be able to choose an ideal ionic liquid in such a complex system, the "rules of the game" must be known exceedingly well. Additionally, the development of novel high-performing ionic liquids would benefit greatly from a vastly increased understanding of structure-property relationships. Promising structural archetypes would be able to be identified and a range of promising candidates synthesized around it. Our current understanding of current ionic liquid structure-device property relationships remains wholly insufficient to accomplish this. Vast avenues of promising research have yet to be explored in regards to ion structure-device property relationships in EDLTs.

References

1. Dimitrakopoulos, C. D.; Malenfant, P. R., Organic Thin Film Transistors for Large Area Electronics. *Adv. Mater.* **2002,** *14*, 99-117.
2. Allard, S.; Forster, M.; Souharce, B.; Thiem, H.; Scherf, U., Organic Semiconductors for Solution-Processable Field-Effect Transistors. *Angew. Chem. Int. Ed.* **2008,** *47*, 4070-4098.
3. Kuribara, K.; Wang, H.; Uchiyama, N.; Fukuda, K.; Yokota, T.; Zschieschang, U.; Jaye, C.; Fischer, D.; Klauk, H.; Yamamoto, T.; Takimiya, K.; Ikeda, M.; Kuwabara, H.; Sekitani, T.; Loo, Y. L.; Someya, T., Organic transistors with high thermal stability for medical applications. *Nat. Commun.* **2012,** *3*, 723.
4. Saudari, R.; Frail, P. R.; Kagan, C. R., Ambipolar transport in solution-despoited pentacene transistors enhanced by molecular engineering of device contacts. *Appl. Phys. Lett.* **2009,** *95*, 023301.
5. Müller, C. D.; Falcou, A.; Reckefuss, N.; Rojahn, M.; Wiederhirn, V.; Rudati, P.; Frohne, H.; Nuyken, O.; Becker, H.; Meerholz, K., Multi-color organic light-emitting displayas by solution processing. *Nature* **2003,** *421*, 829-833.
6. Torrisi, F.; Hasan, T.; Wu, W.; Sun, Z.; Lombardo, A.; Kulmala, T. S.; Hsieh, G.-W.; Jung, S.; Bonaccorso, F.; Paul, P. J.; Chu, D.; Ferrari, A. C., Inkjet-Printed Graphene Electronics. *ACS Nano* **2012,** *6* (4), 2992-3006.
7. Boer, R. W. I. d.; Gershenson, M. E.; Morpurgo, A. F.; Podzorov, V., Organic single-crystal field-effect transistors. *Physica Status Solidi* **2004,** *201* (6), 1302.
8. Ahn, C. H.; triscone, J.-M.; Mannhart, J., Electric Field Effect in Correlated Oxide Systems. *Nature* **2003,** *424*, 1015.
9. Ahn, C. H.; Di Ventra, M.; Eckstein, J. N.; Frisbie, C. D.; Gershenson, M. E.; Goldman, A. M.; Inoue, I. H.; Mannhart, J.; Millis, A. J.; Morpurgo, A. F.; Natelson, D.; Triscone, J.-M., Electrostatic modification of novel materials. *Rev. Mod. Phys.* **2006,** *78*, 1185-1212.
10. Hebard, A. F.; Rosseinsky, M. J.; Haddon, R. C.; Murphy, D. W.; Glarum, S. H.; Palstra, T. T. M.; Ramirez, A. P.; Kortan, A. R., Superconductivity at 18 K in Potassium-doped C60. *Nature* **1991,** *350*, 600.
11. Kelty, S. P.; Chen, C.-C.; Lieber, C. M., Superconductivity at 30-K in cesium-doped C60. *Nature* **1991,** *352*, 223-225.
12. Kortan, A. R.; Kopylov, N.; Glarum, S.; Gyorgy, E. M.; Ramirez, A. P.; Fleming, R. M.; Thiel, F. A.; Haddon, R. C., Superconductivity at 8.4 K in calcium-doped C60. *Nature* **1992,** *355*, 529-532.
13. Mitsuhashi, R.; Suzuki, Y.; Yamanari, Y.; Mitamura, H.; Kambe, T.; Ikeda, N.; Okamoto, H.; Fujiwara, A.; Yamaji, M.; Kawasaki, N.; Maniwa, Y.; Kubozono, Y., Superconductivity in alkali-metal-doped picene. *Nature* **2010,** *464*, 76.
14. Ueno, K.; Nakamura, S.; Shimotani, H.; Ohtomo, A.; Kimura, N.; Nojima, T.; Aoki, H.; Iwasa, Y.; Kawasaki, M., Electric-field induced superconductivity in an insulator. *Nature Materials* **2008,** *7*, 855.

15. Xie, W.; Frisbie, C. D., Electrolyte gated single-crystal organic transistors to examine transport in the high carrier density regime. *Mater Res. Bull.* **2013,** *38*, 43-50.
16. Fujimototo, T.; Awaga, K., Electric-double-layer field-effect transistors with ionic liquids. *PCCP* **2013,** *15*, 8983.
17. Linear Combination of Atomic Orbitals. https://byjus.com/chemistry/linear-combination-of-atomic-orbitals/ (accessed 2017).
18. Orbital Hybridization. http://www.chromacademy.com/lms/sco534/images/P3-orbital-hybridization-6.jpg.
19. Pagenkopf, D. B. An Introduction to Molecular Orbitals. http://www.cm.utexas.edu/academic/courses/Spring2001/CH610B/Iverson/index.html (accessed 2017).
20. Banerji, A.; Tausch, M. W.; Scherf, U., Classroom Experiments and Teaching Materials on OLEDs with Semiconducting Polymers. *Educ. quim.* **2013,** *24* (1), 17-22.
21. Zeghbroeck, B. V., Principles of Semicondcutor Devices. 2011. http://ecee.colorado.edu/~bart/book/book/chapter2/ch2_3.htm.
22. Bao, Z.; Locklin, J., *Organic Field-Effect Transistors*. CRC Press: Boca Raton, 2007.
23. Frölich, H., Electrons in Lattice Fields. *Adv. Phys.* **1954,** *3*, 325-361.
24. Frölich, H., Interaction of Electrons with Lattice Vibrations. *Proc. R. Soc. Lond. Ser. Math. Phys. Sci* **1952,** *215*, 291-298.
25. Holstein, T., Studies of Polaron Motion: Part I. The Molecular-crystal Model. *Ann. Phys.* **1959,** *8*.
26. Holstein, T., Studies of Polarion Motion: Part II. The "small" Polaron. *Ann. Phys.* **1959,** *8*, 343-389.
27. Yamashita, J.; Kurosawa, T., On Electronic Current in NiO. *J. Phys. Chem. Solids* **1958,** *5*, 34-43.
28. Emin, D.; Holstein, T., Studies of Small-polaron Motion IV. Adiabatic Theory of the Hall Effect. *Ann. Phys.* **1969,** *53*, 439-520.
29. Emin, D., Transport Properties of Small Polarons. *J. Solid State Chem.* **1975,** *12*, 246-252.
30. Podzorov, V.; Menard, E.; Borissov, A.; Kiryukhin, V.; Rogers, J. A.; Gershenson, M. E., Intrinsic Charge Transport on the Surface of Organic Semiconductors. *Physical Review Letters* **2004,** *93* (8), 086602.
31. Karl, N., Charge Carrier Transport in Organic Semiconductors. *Synth. Met.* **2003,** *133*, 649-657.
32. Sze, S.; Ng, K. K., *Physics of Semiconductor Devices*. 3rd ed.; Wiley-Interscience: 2008.
33. Mott, N. F., Conduction in non-crystalline materials. *Phil. Mag* **1969,** *19*.
34. More, A. Thin Film Semicondcutor Solutions for Energy-Efficent Future. https://www.semiwiki.com/forum/content/6418-thin-film-semiconductor-solutions-energy-efficient-future.html (accessed 2017).
35. Liu, F.; Xie, W.; Shi, S.; Frisbie, C. D.; Ruden, P. P., Coupling of channel conductance and gate-to-channel capacitance in electric double layer transistors. *Applied Physics Letters* **2013,** *103* (19), 193304.

36. Xia, Y.; Xie, W.; Ruden, P. P.; Frisbie, C. D., Carrier Localization on Surfaces of Organic Semiconductors Gated with Electrolytes. *Physical Review Letters* **2010,** *105*, 036802.
37. Xie, W.; McGarry, K. A.; Liu, F.; Y., W.; Ruden, P. P.; Douglas, C. J.; Frisbie, C. D., High-Mobility Transistors Based on Single Crystals of Isotopically Substituted Rubrene-d28. *J. Phys. Chem. C.* **2013,** *117*.
38. Gershenson, M. E.; Podzorov, V., Colloquium: Electronic transport in single-crystal organic transistors. *Reviews of Modern Physics* **2006,** *78*, 973.
39. Podzorov, V., Organic singe crystals: Addressing the fundamentals of organic electronics. *Materials Research Society Bulletin* **2013,** *38*, 15.
40. Podzorov, V.; Menard, E.; Rogers, J. A.; Gershenson, M. E., Hall Effect in the Accumulation Layers on the Surface of Organic Semiconductors. *Physical Review Letters* **2005,** *95*, 226601.
41. Rang, Z.; Nathan, M. I.; Ruden, P. P.; Podzorov, V.; Gershenson, M. e.; Newman, C. R.; Frisbie, C. D., Hydrostatic pressure dependence of charge carrier transport in single-crystal rubrene devices. *Applied Physics Letters* **2005,** *86*, 123501.
42. Reese, C.; Bao, Z., Organic single-crystal Field-effect Transistors. *Mater. Today* **2007,** *10*.
43. Jiang, L.; Dong, H.; Hu, W., Organic Single Crystal Field-effect Transistors: Advances and Perspectives. *J. Mater. Chem.* **2010,** *20*, 4994.
44. Xie, W.; Frisbie, C. D., Organic Electrical Double Layer Transistors Based on Rubrene Single Crystals: Examining Transport at High Surface Charge Densities above 10^{13} cm^{-2}. *J. Phys. Chem. C.* **2011,** *115* (29), 14360.
45. Hasegawa, T.; Takeya, J., Organic Field-effect Transistors Using Single Crystals. *Sci. Technol. Adv. Mater.* **2009,** *10*, 024314.
46. Irkhin, P.; Biaggio, I., Direct Imaging of Anisotropic Exciton Diffusion and Triplet Diffusion Length in Rubrene single Crystals. *Phys. Rev. Lett.* **2011,** *107*, 017402.
47. Najafov, H.; Lee, B.; Zhou, Q.; Feldman, L. C.; Podzorov, V., Observation of Long-range Exciton Diffusion in HIghly Ordered Organic Semiconductors. *Nat. Mater.* **2010,** *9*, 938-943.
48. Chen, Y.; Lee, B.; Fu, D.; Podzorov, V., The Origin of a 650 nm Photoluminescence Band in Rubrene. *Adv. Mater.* **2011,** *23*, 5370-5375.
49. Pernstich, K. P.; Rössner, B.; Batlogg, B., Field-effect-modulated Seebeck Coefficient in Organic Semiconductors. *Nat. Mater.* **2008,** *7*, 321-325.
50. Okada, Y.; Mori, Y.; Takeya, J., Low-temperature Thermal Conductivity of Bulk and Film-like Rubrene Single Crystals. *Phys. Rev. B.* **2011,** *83*, 113305.
51. Reyes-Martinez, M. A.; Ramasubramaniam, A.; Briseno, A. L.; Crosby, A. J., The Intrinsic Mechanical Properties of Rubrene Single Crystals. *Adv. Mater.* **2012,** *24*, 5548-5552.
52. Chapman, B. D.; Checco, A.; Pindak, R.; Siegrist, T.; Kloc, C., Dislocations and Grain Boundaries in Semiconducting Rubrene Single-crystals. *J. Cryst. Growth* **2006,** *290*, 479-484.

53. Wakabayashi, Y.; Takeya, J.; Kimura, T., Sub-Å Resolution Electron Density Analysis of the Surface of Organic Rubrene Crystals. *Phys. Rev. Lett.* **2010,** *104*, 066103.
54. Machida, S.; Nakayama, Y.; Duhm, S.; Xin, Q.; Funakoshi, A.; Ogawa, N.; Kera, S.; Ueno, N.; Ishii, H., Highest-Occupied-Molecular-Orbital Band Dispersion of Rubrene Single Crystals as Observed by Angle-Resolved Ultraviolet Photoelectron Spectroscopy. *Phys. Rev. Lett.* **2010,** *104*, 156401.
55. Nakayama, Y.; Machida, S.; Minari, T.; Tsukagishi, K.; Noguchi, Y.; Ishii, H., Direct Observation of the Electronic States of Single Crystalline Rubrene Under Ambient Condition by Photoelectron Yield Spectroscopy. *Appl. Phys. Lett.* **2008,** *93*, 173305.
56. Li, H.; Tee, B. C.-K.; Giri, G.; Chung, J. W.; Lee, S. Y.; Bao, Z., High-Performance Transistors and Complementary Inverters Based on Solution-Grown Aligned Organic Single-Crystals. *Adv. Mater.* **2012,** *24*, 2588-2591.
57. Braga, D.; Campione, M.; Borghesi, A.; Horowitz, G., Organic Metal-Semiconductor Field-Effect Transistor (OMESFET) Fabricated on a Rubrene Single Crystal. *Adv. Mater.* **2010,** *22*, 424-428.
58. Kaji, T.; Takenobu, T.; Morpurgo, A. F.; Iwasa, Y., Organic Single-Crystal Schottky Gate Transistors. *Adv. Mater.* **2009,** *21*, 3689-3693.
59. Lezama, I. G.; Nakano, M.; Minder, N. A.; Chen, Z.; Di Girolamo, F. V.; Facchetti, A.; Morpurgo, A. F., Single-crystal Organic Charge-transfer Interfaces Probed Using Schottky-gated Heterostructures. *Nat. Mater.* **2012,** *11*, 788-794.
60. Jiang, H.; Kloc, C., Single-crystal Growth of Organic Semiconductors. *Mater Res. Bull.* **2013,** *38*, 28-33.
61. Mas-Torrent, M.; Durkut, M.; Hadley, P.; Ribas, X.; Rovira, C., High Mobility of Dithiophene-Tetrathiafulvalene Single-Crystal Organic Field Effect Transistors. *J. Am. Chem. Soc.* **2004,** *126*, 984-985.
62. Jiang, H.; Yang, X.; Cui, Z.; Liu, Y.; Li, H.; Hu, W.; Liu, Y.; Zhu, D., Phase Dependence of Single Crystalline Transistors of Tetrathiafulvalene. *Appl. Phys. Lett.* **2007,** *91*, 123505.
63. Bridgman, P. W., Certain physical properties of single crystals of tungsten antimony, bismuth, tellurium, cadmium, zinc, and tin. *Proceedings of the American academy of arts and sciences* **1925,** *60*, 305-383.
64. Warta, W.; Stehle, R.; Karl, N., Ultrapure, High Mobility Organic Photoconductors. *Appl. Phys. A.* **1984,** *36*, 163-170.
65. Niemax, J.; Tripathi, A. K.; Pflaum, J., Comparisons of the electronic properties of sublimation- and vapor-Bridgman-grown crystals of tetracene. *Appl. Phys. Lett.* **2005,** *86*, 122105.
66. Robinson, P. M.; Scott, H. G., Tilt Boundaries in Deformed Anthracene Single Crystals. *Phys. Stat. Sol.* **1967,** *20*, 461.
67. Hong, I. H.; Tan, K. J.; Toh, M.; Jiang, H.; Zhang, K.; Kloc, C., Impurities in zone-refining anthracene crystals. *J. Cryst. Growth* **2013,** *363*, 61-68.
68. Menard, E.; Podzorov, V.; Hur, S.-H.; Gaur, A.; Gershenson, M. E.; Rogers, J. A., High-Performance n- and p-Type Single-Crystal Organic Transistors with Free-Space Gate Dielectrics. *Advanced Materials* **2004,** *16*, 2097.

69. Sundar, V. C.; Zaumseil, J.; Podzorov, V.; Menard, E.; Willett, R. L.; Someya, T.; Gershenson, M. E.; Rogers, J. A., Elestomeric Transistor Stamps: Reversible Probing of Charge Transport in Orgnic Crystals. *Science* **2004,** *303*, 1644-1646.
70. Fischer, M.; Dressel, M.; Gompf, B., Infrared spectroscopy on the charge accumulation layer in rubrene single crystals. *Appl. Phys. Lett.* **2006,** *89*, 182103.
71. Uchida, R.; Yada, H.; Makino, M.; Matsui, Y.; Miwa, K.; Uemura, T.; Takeya, J.; Okamoto, H., Charge modulation infrared spectroscopy of rubrene single-crystal field-effect transistors. *Appl. Phys. Lett.* **2013,** *102*, 093301.
72. Xie, H.; Alves, H.; Morpurgo, A. F., Quantitative analysis of Density-dependent Transport in Tetramethyltetraselenafulvalene Singly-crystal Transistors: Intrinsic Properties and Trapping. *Phys. Rev. B.* **2009,** *80*, 245305.
73. Minder, N. A.; Ono, S.; Chen, Z.; Facchetti, A.; Morpurgo, A. F., Band-Like Electron Transport in Organic Transistors and Implication of the Molecular Structure for Performance Optimization. *Advanced Materials* **2012,** *24*, 503.
74. Horowitz, G., Organic Field-effect Transistors. *Adv. Mater.* **1998,** *10*, 365-377.
75. Stassen, A. F.; Boer, R. W. I. D.; Iosad, N. N.; Morpurgo, A. F., Influence of the Gate Dielectric on the Mobility of Rubrene Single-crystal Field-effect Transistors. *Appl. Phys. Lett.* **2004,** *85*, 3899.
76. Ahn, C. H.; Gariglio, S.; Paruch, P.; Tybell, T.; Antognazza, L.; Triscone, J.-M., Electrostatic Modulation of Superconductivity in Ultrathin $GdBa_2Cu_3O_{7-x}$ Films. *Science* **1999,** *284*, 1152-1155.
77. Ríos, A. P. d. l.; Irabien, A.; Hollmann, F.; Fernádez, J. H., Ionic Liquids: Green Solvents for Chemical Processing. *J. Chem.* **2013,** *2013*, 402172.
78. Perkin, S.; Albrecht, T.; Klein, J., Layering and Shear Properties of an Ionic Liquid, 1-Ethyl-3-Methylimidazolium Ethylsulfate, Confined to Nano-Films between Mica Surfaces. *PCCP* **2010,** *12*, 1243-1247.
79. Endres, F.; Borisenko, N.; El Abedin, S. Z.; Hayes, R.; Atkin, R., The Interface Ionic Liquid(S)/Electrode(S): In Situ Stm and Afm Measurements. *Farad. Discuss* **2012,** *154*, 221-233.
80. Atkin, R.; Borisenko, N.; Druschler, M.; El Abedin, S. Z.; Endres, F.; Hayes, R.; Huber, B.; Rolin, B., An in Situ Stm/Afm and Impedance Spectroscopy Study of the Extremely Pure 1-Butyl-1-Methylpyrrolidinium Tris(Pentafluoroethyl) Trifluorophosphate/Au(111) Interface: Potential Dependent Solvation Layers and the Herringbone Reconstruction. *PCCP* **2011,** *13*, 6849-6857.
81. Zhang, X.; Zhong, Y.-X.; Yan, J.-W.; Su, Y.-Z.; Zhang, M.; Mao, B.-W., Probing Double Layer Structures of Au (111)-Bmipf6 Ionic Liquid Interfaces from Potential-Dependent Afm Force Curves. *Chem. Commun.* **2012,** *48*, 582-584.
82. Black, J. M.; Okatan, M. B.; Feng, G.; Cummings, P. T.; Kalinin, S. V.; Balke, N., Topological Defects in Electric Double Layers of Ionic Liquids at Carbon Interfaces. *Nano Energy* **2015,** *15*, 737-745.
83. Mezger, M.; Schroder, H.; Reichert, H.; Schramm, S.; Okasinski, J. S.; Schroder, S.; Honkimaki, V.; Deutsch, M.; Ocko, B. M.; Ralston, J.; Rohwerder, M.; Stratmann, M.; Dosch, H., Molecular Layering of Fluorinated Ionic Liquids at a Charged Sapphire (0001) Surface. In *Science*, 2008; Vol. 322, p 424.

84. Uysal, A.; Zhou, H.; Feng, G.; Lee, S. S.; Li, S.; Fenter, P.; Cummings, P. T.; Fulvio, P. F.; Dai, S.; McDonough, J. K.; al., e., Structural Origins of Potential Dependent Hysteresis at the Electrified Graphene/Ionic Liquid Interface. *J. Phys. Chem. C* **2014,** *118*, 569-574.
85. Fedorov, M. V.; Kornyshev, A. A., Ionic Liquids at Electrified Interfaces. *CHEMICAL REVIEWS* **2014,** *114*, 2978-3036.
86. Choi, J.-H.; Xie, W.; Gu, Y.; Frisbie, C. D.; Lodge, T. P., Single Ion Conducting Polymerized Ionic Liquid Triblock Copolymer Films: High Capacitance Electrolyte Gates for n-type Transistors. *ACS Appl. Mater. Interfaces* **2015,** *7*, 7294-7302.
87. Lee, K. H.; Kang, M. S.; Zhang, S.; Gu, Y.; Lodge, T. P.; Frisbie, C. D., "Cut and Stick" Rubbery Ion Gels as High Capacitance Gate Dielectrics. *Adv. Mater.* **2012,** *24*, 4457-4462.
88. Wang, Y.; Kim, C.-H.; Yoo, Y.; Johns, J. E.; Frisbie, C. D., Field effect modulation of heterogenous charge transfer kinetics at back-gated 2D MoS electrodes. *Nano Lett.* **2017,** *17*.
89. Cho, J. H.; Lee, J.; Xia, Y.; Frisbie, C. D., Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic. *Nat. Mater.* **2008,** *7*, 900-906.
90. Schmidt, E.; Shi, S.; Ruden, P. P.; Frisbie, C. D., Characterization of the Electric Double Layer Formation Dynamics of a Metal/Ionic Liquid/Metal Structure. *ACS Appl. Mater. Interfaces* **2016,** *8* (23), 14879-14884.
91. Pajkossy, T., Impedance of Rough Capacitive Electrodes. *J. Electroanal. Chem.* **1994,** *364*, 111-125.
92. Lockett, V.; Sedev, R.; Ralston, J., Differential Capacitance of the Electrical Double Layere in Imidazolium-Based Ionic Liquids: Influence of Potential, Cation Size, and Temperature. *J. Phys. Chem. C* **2008,** *112* (19), 7486-7495.
93. Stojek, Z., *Electroanalytical Methods*. Springer: 2002.
94. Shao, L.-H.; Biener, J.; Kramer, D.; Viswanath, R. N.; Baumann, T. F.; Hamza, A. V.; Weissmüller, J., Electrocapillary maximum and potential of zero charge of carbon aerogel. *PCCP* **2010,** *12*, 7580-7587.
95. Xie, W. Charge Transport in Single Crystal Organic Semiconductors. PhD. Dissertation, Univeristy of Minnesota, Minneapolis, 2013.
96. Wang, S.; Ha, M.; Manno, M.; Frisbie, C. D.; Leighton, C., Hopping Transport and the Hall Effect Near the Insulator-metal Transistion in Electrochemically Gated Poly(3-hexylthiophene) Transistors. *Nat. Commun.* **2012,** *3*, 1210.
97. Xie, W.; Wang, S.; Zhang, X.; Leighton, C.; Frisbie, C. D., High Conductance 2D Transport around the Hall Mobility Peak in Electrolyte-Gated Rubrene Crystals. *Physical Review Letters* **2014,** *113* (24), 246602.
98. Panzer, M. J.; Frisbie, C. D., Polymer Electrolyte Gate Dielectric Reveals Finite Windows of High Conductivity in Organic Thin Films Transistors at High Charge Carrier Densities. *J. Am. Chem. Soc.* **2005,** *127*, 6960-6961.
99. Paulsen, B. D.; Frisbie, C. D., Dependence of Conductivity on Charge Density and Electrochemical Potential in Polymer Semiconductors Gated with Ionic Liquids. *J. Phys. Chem. C* **2012,** *116*, 3132-3141.

100. Yuan, H.; Shimotani, H.; Tsukazaki, A.; Ohtomo, O.; Kawasaki, M.; Iwasa, Y., High-Density Carrier Accumulation in ZnO Field-Effect Transistors Gated by Electric Double Layers of Ionic Liquid. *Adv. Funct. Mater.* **2009,** *19* (7), 1046-1053.
101. Zimmerling, T.; Batlogg, B., Improving charge injection in high-mobility rubrene crystals; From contact-limited to channel-dominated transistors. *J. Appl. Phys.* **2014,** *1145*, 164511.
102. Ue, M.; Takeda, M.; Toriumi, A.; Kominato, A.; Hagiwara, R.; Y., I., Application of Low-Viscosity Ionic Liquid to the Electrolyte of Double-Layer Capacitors. *J. Electrochem. Soc.* **2003,** *150*, A499.
103. Sato, T.; Masuda, G.; Takagi, K., Electrochemical Properties of Novel Ionic Liquids for Electric Double Layer Capactior Applications. *Electrochim. Acta* **2004,** *49*, 3603-3611.
104. Vatamanu, J.; Borodin, O.; Smith, G. D., Molecular simulations of the electric double layer structure, differential capacitance, and charging kinetics for N-methyl-N-propylpyrrolidinium bis (fluorosulfonyl) imide at graphite electrodes. *J. Phys. Chem. B.* **2011,** *115* (12), 3073.
105. Ono, S.; Miwa, K.; Seki, S.; Takeya, J., A comparative study of organic single-crystal transistors gated with various ionic-liquid electrolytes. *Appl. Phys. Lett.* **2009,** *94*, 063301.
106. Ono, S.; Seki, S.; Hirahara, R.; Tominari, Y.; Takeya, J., High-mobility, low-power, and fast-switching organic field-effect transistors with ionic liquids. *Appl. Phys. Lett.* **2008,** *92*, 103313.
107. Panzer, M. J.; Frisbie, C. D., Polymer Electrolyte-Gated Organic Field-Effect Transistors: Low-Voltage, High-Current Switches for Organic Electronics and Testbeds for Probing Electrical Transport at High Charge Carrier Density. *J. Am. Chem. Soc.* **2007,** *129* (20), 6599-6607.
108. Asanuma, S.; Xiang, P. H.; Yamada, H.; Sato, H.; Inoue, I. H.; Akoh, H.; Sawa, A.; Ueno, K.; Shimotani, H.; Yuan, H.; Kawasaki, M.; Iwasa, Y., Tuning of the metal-insulator transistion in electrolyte-gated NdNiO3 thin films. *Applied Physics Letters* **2010,** *97*, 142110.
109. Eigen, M.; Wicke, E., The Thermodynamics of Electrolytes at Higher Concentration. *J. Phys. Chem.* **1954,** *58* (9).
110. Kornyshev, A. A.; Vorotyntsev, M. A., Conductivity and Space Charge Phenomena in Solid Electrolytes with One Mobile Charge Carrier Species, a Review with Original Material. *Electrochim. Acta* **1981,** *26*, 303-323.
111. Penfold, R.; Nordholm, S.; Jonsson, B.; Woodward, C. E., A simple analysis of ion-ion correlation in polyelectrolyte solutions. *J. Chem. Phys* **1990,** *92*.
112. Groot, R., Ion condensation on solid particles: Theory and simulations. *J. Chem. Phys* **1991,** *95* (12).
113. Diehl, A.; Tamashire, M.; Barbosa, M. C.; Levin, Y., Density-functional theory for attraction between like-charged plates. *Physica A* **1999,** *274*.
114. Antypov, D.; Barbos, M. C.; Holm, C., Incorporation of exluded-volume correlations into Poisson-Boltzmann theory. *Phys. Rev. E.* **2005,** *71*.

115. Kornyshev, A. A., Double-Layer in Ionic Liquids: Paradigm Change? *J. Phys. Chem. B* **2007,** *111*, 5545-5557.
116. Jiang, J.; Cao, D.; Jiang, D.; Wu, J., Time-Dependent Density Functional theory for Ion Diffusion in Electrochemical Systems. *J. Phys. Condens. Matter* **2014,** *26*, 284102.
117. Jiang, J.; Cao, D.; Jiang, D.; Wu, J., Kintetic Charging Inversion in Ionic Liquid Electric Double Layers. *J. Phys. Chem. Lett.* **2014,** *5*, 2195-2200.
118. Velikonja, A.; Kralj-Iglic, V.; Iglic, A., On Asymmetric Shape of Electric Double Layer Capacitance. *Int. J. Electrochem. Sci.* **2015,** *10*.
119. Kornyshev, A. A.; Qiao, R., Three-Dimensional Double Layers. *J. Phys. Chem. C* **2014,** *118*, 18285-18290.
120. Ogawa, S.; Naijo, T.; Kimura, Y.; Ishii, H.; Niwano, M., Displacement Current Measurement as a Tool to Characterize Organic Field Effect Transistors. *Synth. Met.* **2005,** *153*, 253-256.
121. Bottelberghs, P. H.; Broers, G. H. J., Interfacial Impedance Behavior of Polished and Paint Platinum Electrodes at Na_2WO_4-Na_2MoO_4 solid electrolytes. *J. Electroanal. Chem. Interfacial Electrochem.* **1976,** *16*, 155-167.
122. Hirschorn, B.; Orazem, M. E.; Tribollet, B.; Vivier, V.; Frateur, I.; Musiani, M., Constant-Phase-Element Behavior Caused by Resistivity Distributions in Films. *J. Electrochem. Soc.* **2010,** *157*, C452-C457.
123. Brug, G. J.; Eeden, A. L. G. v. d.; Sluyters-Rehbach, M.; Sluyters, J. H., The Analysis of Electrode Impedance Complicated by the Presence of a Constant Phase Element. *J. Electroanal. Chem. Interfacial Electrochem.* **1984,** *176*, 275-295.
124. Kornyshev, A. A.; Luque, N. B.; Schmickler, W., Differential capacitance of ionic liquid interface with graphite: the story of two double layers. *J. Solid State Electrochem.* **2014,** *18*, 1345-1349.
125. *Organic Electronics II: More Materials and Applications*. John Wiley & Sons: 2012.
126. Kim, S. H.; Hong, K.; Xie, W.; Lee, K. H.; Zhang, S.; Lodge, T. P.; Frisbie, C. D., Electrolyte-Gated Transistors for Organic and Printed Electronics. *Adv. Mater.* **2013,** *25*, 1822-1846.
127. Hong, K.; Kim, Y. H.; Kim, S. H.; Xie, W.; Xu, W. D.; Kim, C.-H.; Frisbie, C. D., Aerosol Jet Printed, Sub-2 V Complementary Circuits Constructed from P - and N - Type Electrolyte Gated Transistors. *Adv. Mater.* **2014,** *26*, 7032-7037.
128. Ye, J. T.; Inoue, S.; Kobayashi, K.; Kasahara, Y.; Yuan, H. T.; Shimotani, H.; Iwasa, Y., Electric-Field Induced Superconductivity in an Insulator. *Nat. Mater.* **2010,** *7*, 855-858.
129. Dhoot, A. S.; Israel, C.; Moya, X.; Mathur, N.; Friend, R., Large Electric field Effect in Electrolyte-Gated Manganites. *Phys. Rev. Lett.* **2009,** *102*, 136402.
130. Kaake, L. G.; Paulsen, B. D.; Frisbie, C. D.; Zhu, X.-Y., Mixing at the Charged Interface of a Polymer Semiconductor and a Polyelectrolyte Dielectric. *J. Phys. Chem. Lett.* **2010,** *1*, 862-867.
131. Lee, J.; Kaake, L. G.; Cho, J. H.; Zhu, X.-Y.; Lodge, T. P.; Frisbie, C. D., Ion Gel-Gated Polymer Thin-Film Transistors: Operating Mechanism and Characterization of

Gate Dielectric Capacitance, Switching Speed, and Stability. *J. Phys. Chem. C* **2009,** *113*, 8972-8981.
132. Kaake, L. G.; Zou, Y.; Panzer, M. J.; Frisbie, C. D.; Zhu, X.-Y., Vibrational Spectroscopy Reveals Electrostatic and Electrochemical Doping in Organic Thin film Transistors Gated with a Polymer Electrolyte Dielectric. *J. Am. Chem. Soc.* **2007,** *129*, 7824-7830.
133. Xie, W.; Liu, F.; Shi, S.; Ruden, P. P.; Frisbie, C. D., Charge Density Dependent Two-Channel Conduction in Organic Electric Double Layer Transistors (EDLTs). *Adv. Mater.* **2014,** *26*, 2527-2532.
134. Li, Z. Q.; Podzorov, V.; Sai, N.; Martin, M. C.; Gershenson, M. E.; Di Ventra, M.; Basov, D. N., Light Quasiparticles Dominate Electronic Transport in Molecular Crystal Field-Effect Transistors. *Phys. Rev. Lett.* **2007,** *99*, 016403.
135. Hulea, I. N.; Fratini, S.; Xie, H.; Mulder, C. L.; Iossad, N. N.; Rastelli, G.; Ciuchi, S.; Morpurgo, A. F., Tunable Frölich Polarons in Organic Single-Crystal Transistors. *Nat. Mater.* **2006,** *5*, 982-986.
136. Bisri, S. Z.; Takenobu, T.; Takahashi, T.; Iwasa, Y., Electron Transport in Rubrene Single-Crystal Transistors. *Appl. Phys. Lett.* **2010,** *96*, 183304.
137. Takenobu, T.; Takahashi, T.; Takeya, J.; Iwasa, Y., Effect of Metal Electrodes on Rubrene Single-Crystal Transitors. *Appl. Phys. Lett.* **2007,** *90*, 013507.
138. Lee, B.; Chen, Y.; Fu, D.; Yi, H. T.; Czelen, K.; Najafov, H.; Podzorov, V., Trap Healing and Ultralow-Noise Hall Effect at the Surface of Organic Semiconductors. *Nat. Mater.* **2013,** *12*, 1125-1129.
139. Ullah, A. R.; Micolich, A. P.; Cochrane, J. W.; Hamilton, A. R., The Effect of Temperature and Gas Flow on the Physical Vapour Growth of Mm-Scale Rubrene Crystals for Organic FETs. In *Microelectronics, MEMS, and Nanotechnology*, Tan, H. H.; Chiao, J.-C.; Faraone, L.; Jagadish, C.; Williams, J.; Wilson, A. R., Eds. International Society for Optics and Photonics: Bellingham, WA, 2007.
140. Pundsack, T. J.; Haugen, N. O.; Johnstone, L. R.; Frisbie, C. D.; Lidberg, R. L., Temperature Dependent c-Axis Hole Mobilities in Rubrene Single Crystals Determined by Time-of-Flight. *Appl. Phys. Lett.* **2015,** *106*, 113301.
141. Yokota, Y.; Hara, H.; Harada, T.; Imanishi, A.; Uemura, T.; Takeya, J.; Fukui, K., Structural Investiagion of Ionic Liquid/rubrene Single Crystal Interfaces by Using Frequency-Modulation Atomic Force Microscopy. *Chem. Commun.* **2013,** *49*, 10596-10598.
142. Sota, T.; Masuda, G.; Takagi, K., Electrochemical properties of novel ionic liquids for electric double layer capacitor applications. *Electrochim. Acta* **2004,** *49* (21).
143. Shimotani, H.; Asanuma, H.; Takeya, J.; Iwasa, Y., Electrolyte-gated charge accumulation in organic single crystals. *Appl. Phys. Lett.* **2006,** *89*, 203501.
144. Yuan, H. T.; Toh, M.; Morimoto, K.; Tan, W.; Wei, F.; Shimotani, H.; Kloc, C.; Iwasa, Y., Liquid-gated electric-double-layer transistor on layered metal dichalcogenide, SnS_2. *Appl. Phys. Lett.* **2011,** *2011*, 012102.
145. Onose, Y.; Yoshimi, R.; Tsukazaki, A.; Yuan, H.; Hidaka, T.; Iwasa, Y.; Kawasaki, M.; Tokua, Y., Pulsed Laser Deposition and Ionic Liquid Gate Control of Epitaxial Bi_2Se_3 Thin Films. *Appl. Phys. Express* **2011,** *4* (8).

146. Thiemann, S.; Sachnov, S.; Porscha, S.; Wasserscheid, P.; Zaumseil, J., Ionic Liquids for Electrolyte-Gating of ZnO Field-Effect Transistors. *J. Phys. Chem. C* **2012,** *116*, 13536-13544.
147. Mousavi, M. P. S.; Wilson, B. E.; Kashefolgheta, S.; Anderson, E. L.; He, S.; Bühlmann, P.; Stein, A., Ionic Liquids as Electrolytes for Electrochemical Double-Layer Capacitors: Structures that Optimize Specific Energy. *ACS Appl. Mater. Interfaces* **2016,** *8*, 3396-3406.
148. Singh, M.; Manoli, K.; Tiwari, A.; Ligonzo, T.; Di Franco, C.; Cioffi, N.; Palazzo, G.; Scamarcio, G.; Torsi, L., The double layer capacitance of ionic liquids for electrolyte gating of ZnO thing film transistors and effect of gate electrodes. *J. Mater. Chem. C* **2017,** *5*.
149. Liang, Y.; Frisbie, C. D.; Chang, H.-C.; Ruden, P. P., Conducting Channel Formation and Annihilation in Organic Field-Effect Structures. *J. Appl. Phys.* **2009,** *105*, 024514.
150. Lian, C.; Liu, K.; Van Aken, K. L.; Gogotsi, Y.; Wesolowski, D. J.; Liu, H. L.; Jiang, D. E.; Wu, J. Z., Enhancing the Capacitive Performance of Electric Double-Layer Capacitors with Ionic Liquid Mixtures. *ACS Energy Lett.* **2016,** *1*, 21-26.
151. Lauw, Y.; Horne, M. D.; Rodopoulos, T.; Nelson, A.; Leermakers, F. A. M., Electrical Double-Layer Capacitance in Room Temperature Ionic Liquids: Ion-Size and Specific Adsorption Effects. *J. Phys. Chem. B* **2010,** *114*, 11149-11154.
152. Atallah, T. L.; Gustafsson, M. V.; Schmidt, E.; Frisbie, C. D.; Zhu, X.-Y., Charge Saturation and Intrinsic Doping in Electrolyte-Gated Organic Semiconductors. *J. Phys. Chem. Lett.* **2015,** *6* (23), 4840-4844.
153. Bockris, J. O. M.; Argade, S. D.; Gileadi, E., The Determination of the Potential of Zero Charge on Solid Metals. *Electrochim. Acta* **1969,** *14*, 1259-1283.
154. Müller, C. D.; Vesztergom, S.; Pajkossy, T.; Jacob, T., Immersion measurements of potential of zero total charge (pztc) of Au (100) in an ionic liquid. *Electrochim. Acta* **2015,** *188*, 512-515.
155. Kim, S. H., Immersion Method for the Potential of Zero Charge Determination. An Electrode Pretreatement. *J. Phys. Chem.* **1973,** *77*, 2787-2789.
156. Bodé Jr., D. D.; Andersen, T. N.; Eyring, H., Cation Effects on the Potential of Zero Chrage of Gold, Silver, and Mercury Electrodes. *J. Electrochem. Soc.* **1967,** *114*, 72-74.
157. Bodé Jr., D. D.; Andersen, T. N.; Eyring, H., Anion and pH Effects on the Potentials of Zero Charge of Gold and Silver Electrodes. *J. Phys. Chem.* **1967,** *71* (4), 792-797.
158. Yokota, Y.; Hara, H.; Harada, T.; Imanishi, A.; Takafumi, U.; Takeya, J.; Fukui, K., Structural investigation of ionic liquid/rubrene single crystal interfaces by using frequency-modulation atomic force microscopy. *Chem. Commun.* **2013,** *49*, 10596.
159. Yoo, C. G.; Pu, Y.; Ragauskas, A. J., Ionic liquids: Promising green solvents for lignocellulosic bbiomass utilization. *Curr. Opin. Green Sust. Chem.* **2017,** *5*, 5-11.