Digital Intensive Mixed Signal Circuits with In-situ Performance Monitors

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Dedication

This thesis is dedicated to my parents

Abstract

Digital intensive circuit design techniques of different mixed-signal systems such as data converters, clock generators, voltage regulators etc. are gaining attention for the implementation of modern microprocessors and system-on-chips (SoCs) in order to fully utilize the benefits of CMOS technology scaling. Moreover different performance improvement schemes, for example, noise reduction, spur cancellation, linearity improvement etc. can be easily performed in digital domain.

In addition to that, increasing speed and complexity of modern SoCs necessitate the requirement of in-situ measurement schemes, primarily for high volume testing. In-situ measurements not only obviate the need for expensive measurement equipments and probing techniques, but also reduce the test time significantly when a large number of chips are required to be tested.

Several digital intensive circuit design techniques are proposed in this dissertation along with different in-situ performance monitors for a variety of mixed signal systems. First, a novel beat frequency quantization technique is proposed in a two-step VCO quantizer based ADC implementation for direct digital conversion of low amplitude bio-potential signals. By direct conversion, it alleviates the requirement of the area and power consuming analog-frontend (AFE) used in a conventional ADC designs. This prototype design is realized in a 65nm CMOS technology. Measured SNDR is 44.5dB from a 10mVpp, 300Hz signal and power consumption is only 38μW.

Next, three different clock generation circuits, a phase-locked loop (PLL), a multiplying delay-locked loop (MDLL) and a frequency-locked loop (FLL) are

presented. First a 0.4-to-1.6GHz sub-sampling fractional-N all digital PLL architecture is discussed that utilizes a D-flip-flop as a digital sub-sampler. Measurement results from a 65nm CMOS test-chip shows 5dB lower phase noise at 100KHz offset frequency, compared to a conventional architecture. The Digital PLL (DPLL) architecture is further extended for a digital MDLL implementation in order to suppress the VCO phase noise beyond the DPLL bandwidth. A zero-offset aperture phase detector (APD) and a digital-to-time converter (DTC) are employed for static phase-offset (SPO) cancellation. A unique in-situ detection circuitry achieves a high resolution SPO measurement in time domain. A 65nm test-chip shows 0.2-to-1.45GHz output frequency range while reducing the phase-noise by 9dB compared to a DPLL. Next, a frequency-to-current converter (FTC) based fractional FLL is proposed for a low accuracy clock generation in an extremely low area for IoT application. High density deep-trench capacitors are used for area reduction. The test-chip is fabricated in a 32nm SOI technology that takes only $0.0054mm^2$ active area. A high-resolution in-situ period jitter measurement block is also incorporated in this design.

Finally, a time based digital low dropout (DLDO) regulator architecture is proposed for fine grain power delivery over a wide load current dynamic range and input/output voltage in order to facilitate dynamic voltage and frequency scaling (DVFS). High-resolution beat frequency detector dynamically adjusts the loop sampling frequency for ripple and settling time reduction due to load transients. A fixed steady-state voltage offset provides inherent active voltage positioning (AVP) for ripple reduction. Circuit

simulations in a 65nm technology show more than 90% current efficiency for 100X load current variation, while it can operate for an input voltage range of 0.6V – 1.2V.

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Chapter 1. Introduction

Over the last few decades, due to the significant development in the CMOS process technology scaling, there has been a dramatic improvement in the performance e.g. speed, power consumption, area of modern integrated circuits and systems which have a wide range of applications in telecommunication, automotive, healthcare etc. These integrated systems typically consist of many mixed-signal blocks to perform data conversion (ADC, DAC etc.), clock generation (PLL, MDLL etc.) and voltage regulation (LDO, DC-DC converters etc.). An example in Fig. 1.1 shows a generic block diagram of an integrated system containing different mixed signal blocks. These mixed signal blocks, as evident from its name, have both digital components such as digital controller, logic units etc. as well as analog amplifiers, filters etc. Taking the benefits of advanced technology, digital components are scaled down significantly; while the analog components are lagging behind, as these specialized circuits have to be custom hand-designed and minimum device sizes no longer be used in order to meet their design specifications e.g. gain, bandwidth, noise etc. In addition to that, the increase of device non-idealities such as leakage current, process-voltage-temperature (PVT) variations etc. with the technology scaling makes the analog designs even more challenging. Therefore, different digital intensive circuit design techniques are proposed in this thesis that can achieve the functionality of the analog blocks using digital components and thereby obviate the requirement of analog circuits in any mixed-signal block.

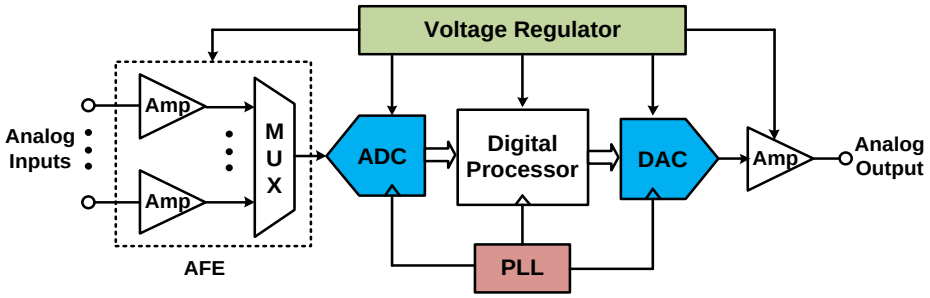


Fig. 1.1: A generic block diagram of an integrated system showing different mixed signal blocks.

Furthermore, increasing speed and complexity of modern multi-GHz mixed signal systems imposes significant challenge on the measurements of the circuit performances such as clock jitter, skew etc. For a clock period of less than 1ns, the clock jitter/skew is in the order of only a few picoseconds range. Therefore, off-chip measurements with sub-picosecond accuracy require expensive high-speed test equipments and dedicated off chip drivers (OCD) connected to high frequency probes or packages of the chip. This can introduce errors in the measured results and at the same time severely limits the measurement time. As a result, in-situ measurement schemes are employed in this research not only to alleviate the need for external measurement equipments and probing techniques, but also to expedite the measurement cycle when a large number of samples are tested. These measurement circuits are realized in a compact area and generate high-resolution digital outputs.

Benefits of proposed design techniques are demonstrated in working test-chips implemented in advanced CMOS technologies (e.g. 32nm high-k metal gate SOI, 65nm low-power) and the circuit performances are compared with the state-of-the-art designs.

1.1 Direct Digital Conversion of Bio-potential Signals

Data acquisition systems for bio-potential signals such as ECG, EEG, EMG etc. require compact and energy efficient analog-to-digital converters (ADCs). Although there has been a significant development in the design of low power ADC designs, the biggest bottleneck in making these systems low power and area efficient is the overhead of the analog front end (AFE) circuits such as low noise amplifier and variable gain amplifier which are required to amplify the low swing bio-potential signals to full rail-to-rail before applying it to the ADC. The primary goal of this work is to develop a high-resolution novel time-based ADC solution for small voltage input and achieve an amplifier-less bio-signal acquisition. This greatly relaxes the circuit complexity and the power consumption associated with AFE design. The impact will be substantial especially for multi-channel applications where hundreds of such amplifiers are conventionally used. A beat-frequency scheme is explored by converting the signal into time domain using a voltage controlled oscillator (VCO) and comparing it with a reference clock. To improve the resolution further, a two-step approach is proposed where the first step is for coarse conversion and the second step performs fine conversion. The proposed two-step ADC is demonstrated in a 65nm LP CMOS process.

1.2 Clock Generators with In-situ Performance Monitors

One of the major drawbacks in traditional analog phase-locked loop (PLL) based clock generators is the large area of the passive analog loop filter. Therefore, fully digital implementation of PLLs is gaining popularity by replacing the analog sub-components

with their digital counterparts. By replacing the phase-detector and the charge-pump with a time-to-digital converter (TDC) enables the loop-filter implementation in digital domain, reducing the area significantly. To further alleviate the design complexity and power consumption of high resolution TDC, in this work, a bang-bang or binary phase detector (BBPD) is utilized that acts as a 1-bit TDC. Moreover, sub-sampling mechanism is incorporated without using any frequency divider in the feedback path.

The performance is further improved by extending the PLL design for multiplying delay-locked loop (MDLL) operation, which has been recently researched actively. The working principle of an MDLL is similar to that of a PLL but has superior noise performance as it periodically resets the VCO noise using the clean reference clock. However, MDLLs suffer from spurious tones at the output due to the offset between the reference and the output phase. An offset cancellation technique is proposed to reduce this spur. A unique in-situ detection scheme is also employed to measure this offset very precisely without the requirement of any high-speed measurement set up. The PLL and MDLL circuits are also implemented in 65nm CMOS process and performance is verified with the measurement results.

In order to address the large area requirement of an analog PLL, a novel frequency-to-current converter (FTC) based fractional frequency synthesizer is proposed for low accuracy clock generation in internet-of-things (IoT) application. High capacitance density of deep-trench capacitor is utilized to minimize the chip area further. An on-chip jitter measurement circuit is designed to measure the period jitter of the output clock. The

complete design is fabricated in 32nm high-K metal gate SOI process and measurements are performed for a wide variation of operating voltage and temperature.

1.3 Time-based Digital Voltage Regulator

Increasing number of independent power supply domains in a single chip necessitate the requirement of high-efficiency compact on-die voltage regulators. Moreover, the use of dynamic voltage and frequency scaling (DVFS) for low power digital circuits demands dynamically adaptive voltage regulators providing wide load current dynamic range. In this thesis, a digital low-dropout (LDO) regulator is proposed to achieve all these requirements. A time-based quantizer utilizing the beat frequency scheme (as mentioned in section 1.1) is employed for digital implementation of the LDO. The loop operation frequency is adaptive depending on the transient variation in voltage. Active voltage positioning (AVP) mechanism is also incorporated to reduce the voltage transient variations in the output during a large change in load current. The LDO circuit is implemented in 65nm LP CMOS technology.

1.4 Summary of Dissertation Contribution

Several contributions have been made in this thesis to improve the performance of the state-of-the-art mixed signal circuit designs. Proposed techniques are applied in three different types of mixed signal circuits: analog-to-digital converter, clock generator and low dropout voltage regulator.

To summarize the key contributions of this research: 1) the proposed ADC can eliminate the requirement of the high area and power consuming AFE circuit in a bio-

potential acquisition system. 2) Different clock generation architectures utilizing digital sub-sampling mechanism, reference spur cancellation technique, frequency-to-current conversion etc. can provide a stable accurate clock over a wide output frequency range while consuming low silicon area and power consumption. 3) In-situ measurement schemes in high-speed clock generation circuits can measure the clock jitter and phase offset precisely. 4) A compact and energy efficient time-based digital LDO is proposed for dynamically adaptive voltage regulation over a wide variation in output load current.

The remainder of this thesis is organized as follows. Chapter 2 illustrates the design of a two-step time-based ADC utilizing a beat frequency quantizer for direct-conversion of low amplitude bio-potential signals. Chapter 3 and 4 present a digital intensive PLL and MDLL architectures respectively with in-situ measurement schemes. The design of a fractional frequency synthesizer with on-chip clock jitter measurement circuit is proposed in chapter 5. The time-based digital LDO design is explained in chapter 6. Finally chapter 7 provides a summary of the thesis.

Chapter 2. Beat Frequency Quantizer based Two-step ADC

2.1 Introduction

Multi-channel data acquisition systems for bio-signals such as ECG, EEG, and EMG typically consist of filters and amplifiers (together known as analog frontend) for signal pre-conditioning; an analog multiplexer for channel selection, and a shared analog-to-digital converter (Fig. 2.1). The power consumption and area overhead of analog frontend (AFE) circuits are major limiting factors, as evident from the pie-diagrams in Fig. 2.2 obtained from recent state-of-the-art ASIC implementations [1]-[5]. Analog-to-digital converters (ADCs) on the other hand, account for a smaller portion of the total system power and area. The reason why AFE circuits cannot be simplified is because traditional ADCs operate under the assumption that a high quality rail-to-rail analog signal is available. Therefore, ADC circuits that can alleviate the requirements of the AFE block, or even work without a full AFE, can be effective in reducing the chip area and power consumption.

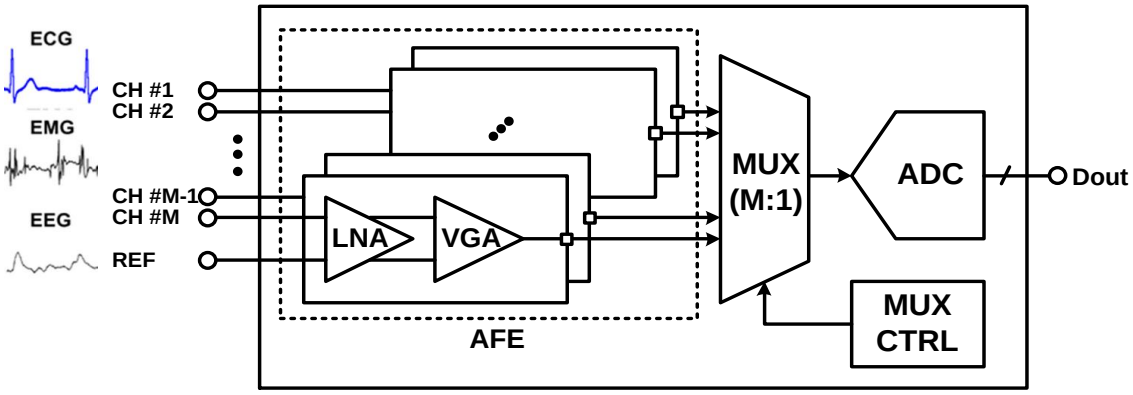


Fig. 2.1: Simplified block diagram of a multi-channel bio-signal acquisition ASIC.

Time based quantization using a voltage controlled oscillator (VCO) that converts the signal from voltage domain to time domain [8], [9], is recently gaining popularity for high resolution ADC designs due to its digital intensive approach and thereby, utilizes the benefits of technology scaling. A beat frequency based ADC (BF-ADC), first proposed in [10] and shown in Fig. 2.3, converts the signal into time domain by a VCO and compares it with a reference clock. Frequency difference (i.e. beat frequency) between the signal and the reference, detected by a BF quantizer, is utilized for achieving 6-7 Effective Number Of Bits (ENOB) for direct conversion of sub-millivolt bio-potential signals. The resolution of the BF-ADC is further improved in [11] by employing multiple phases of the VCO and achieving first-order noise shaping in the BF quantizer. One major shortcoming in existing BF-ADC implementations is that quantization noise increases rapidly as the difference between the reference frequency and signal frequency (Δf) increases. That limits the input range of the signal to a few mV for the BF quantizer. On the other hand, the amplitude and common-mode variation of most bio-potential signals are in the range of 5-10mV [12]. Hence, the BF-ADC performance can degrade due to

this large input voltage variation. Another limitation in the previous BF-ADC is that the output of the BF quantizer is updated once in every beat period, which directly depends on the input signal amplitude. Therefore, output data needs to be re-sampled with a fixed sampling clock (CK_S) before transferring the output code to a digital processor. However, direct sampling of the BF quantizer output with CK_S can cause meta-stability issues and generate errors at the final output.

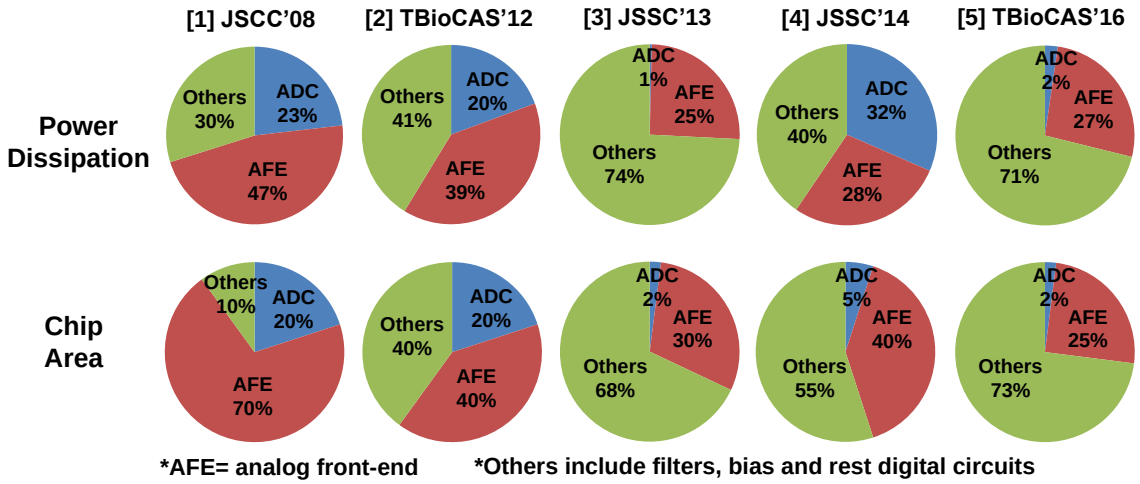


Fig. 2.2: Power and area breakdown of bio-potential ASICs published in recent literatures [1]-[5]. The AFE block accounts for a significantly larger portion of the total system power and area compared to the ADC itself.

In this work, a two-step BF-ADC architecture is proposed that addresses the previously explained limitations associated with BF-ADCs [13]. The proposed two-step approach employs multiple references and selects the appropriate one depending on the signal voltage in order to keep the Δf small irrespective of the signal swing and thereby, achieves high resolution under large amplitude and common-mode variation. In addition, a triple-sampling technique is employed to overcome the meta-stability issue as

mentioned above while sampling with CK_s. Finally, a detailed methodology to calculate the quantization noise and signal-to-noise ratio (SNR) is presented and the performance is compared with a conventional VCO based linear ADC. Also the impacts of VCO noise or jitter on ADC performance are explained in details.

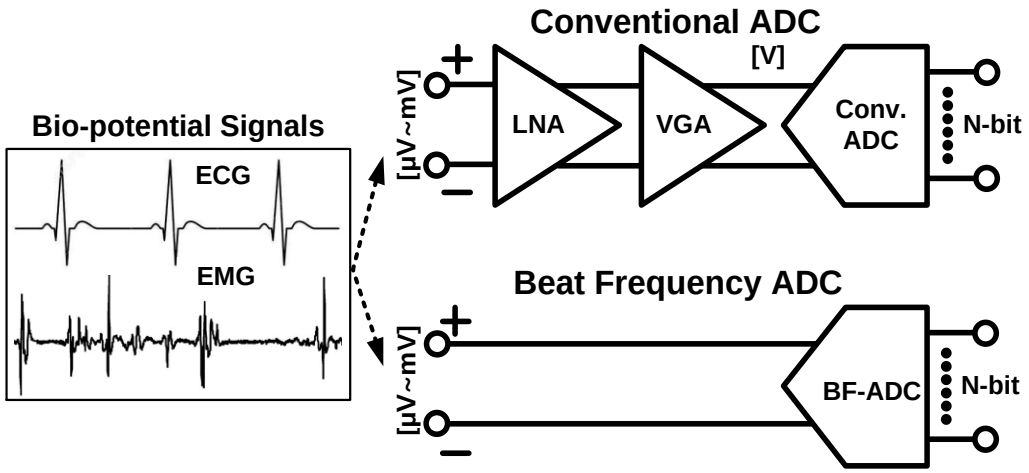


Fig. 2.3: AFE overhead reduction is possible by direct conversion of sub- 10mV swing bio-potential signals using the proposed beat-frequency ADC.

The remainder of this chapter is organized as follows. Section 2.2 describes the basic concept of a conventional linear VCO based quantizer, the previous single-step BF quantizer and the proposed two-step BF quantizer. Mathematical details for calculating quantization noise and SNR are provided in Section 2.3. The impact of VCO clock jitter on the BFADC performance is explained in section 2.4. Section 2.5 describes the triple sampling synchronization technique. Circuit implementation details and measurement results are provided in section 2.6 and 2.7 respectively, followed by conclusions in section 2.8.

2.2 Beat Frequency based Time Quantizer

2.2.1. *VCO based Linear Quantizer*

A linear VCO based quantizer as shown in Fig. 2.4(a) consists of a VCO, a counter and D-flip-flops (DFFs). The VCO converts the input analog signal (SIG) to a proportional frequency (f_{SIG}) and the counter counts the number of VCO clock cycles in each sampling clock (CK_s) period. As a result, the output code D_{OUT} is proportional to the input voltage generating linear input to output transfer characteristics (Fig. 2.4(b)). Since each quantization step (Δ) is constant, the quantization noise Δ_q vs. f_{SIG}, as plotted in Fig. 2.4(c), looks like a saw-tooth wave having fixed maximum value ($\pm\Delta/2$) independent of f_{SIG}. For good SNR, the raw input signal must be amplified to a rail-to-rail signal prior to the conversion.

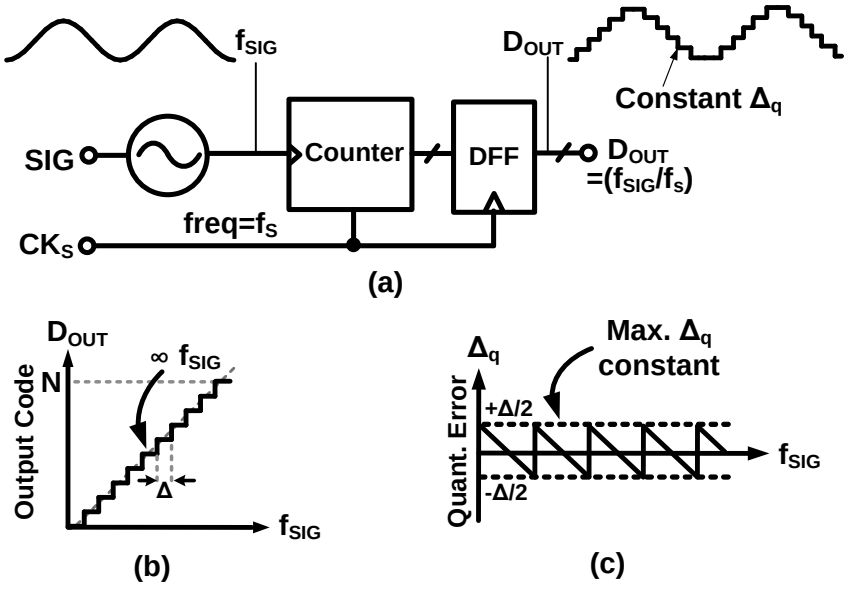


Fig. 2.4: (a) Conventional VCO based linear quantizer. (b) Output count is proportional to input voltage. (c) The maximum quantization error is fixed irrespective of signal swing.

2.2.2. *Beat Frequency based Quantizer*

Fig. 2.5 explains the basic principle of the beat frequency based quantization technique. A frequency subtractor, implemented using a DFF, generates the beat frequency (i.e. $\Delta f=f_1-f_2$) of the two input clocks (CK_{SIG}, CK_{REF}) and the counter quantizes the time period of the beat frequency clock CK_{BF}. CK_{BF} is highly sensitive to the input voltage variation as illustrated in the timing diagram of Fig. 2.5. Suppose the initial frequency difference (Δf) between CK_{SIG} and CK_{REF} signals is 1%. Then, the beat frequency count (D_{OUT}) is 100 as it takes 100 cycles for the two signals to pass each other. Now, if Δf increases to 1.5%, D_{OUT} decreases to 67. Similarly, if Δf becomes 2%, D_{OUT} reduces to only 50. Therefore, a 1% change in the frequency difference translates into an output count difference of 50%. In contrast, the output count of a linear quantizer would only change by 1% for the same change in the frequency difference. The count difference can be further increased by making the initial frequency difference less than 1%. The high input sensitivity of beat frequency quantization can be utilized for direct conversion of a low swing signal. This means that the AFE block can be simplified or even removed. The beat frequency detection technique was originally proposed for measuring circuit-aging effect [14]. More recently, a true random number generator was demonstrated based on the beat frequency detection circuit [15].

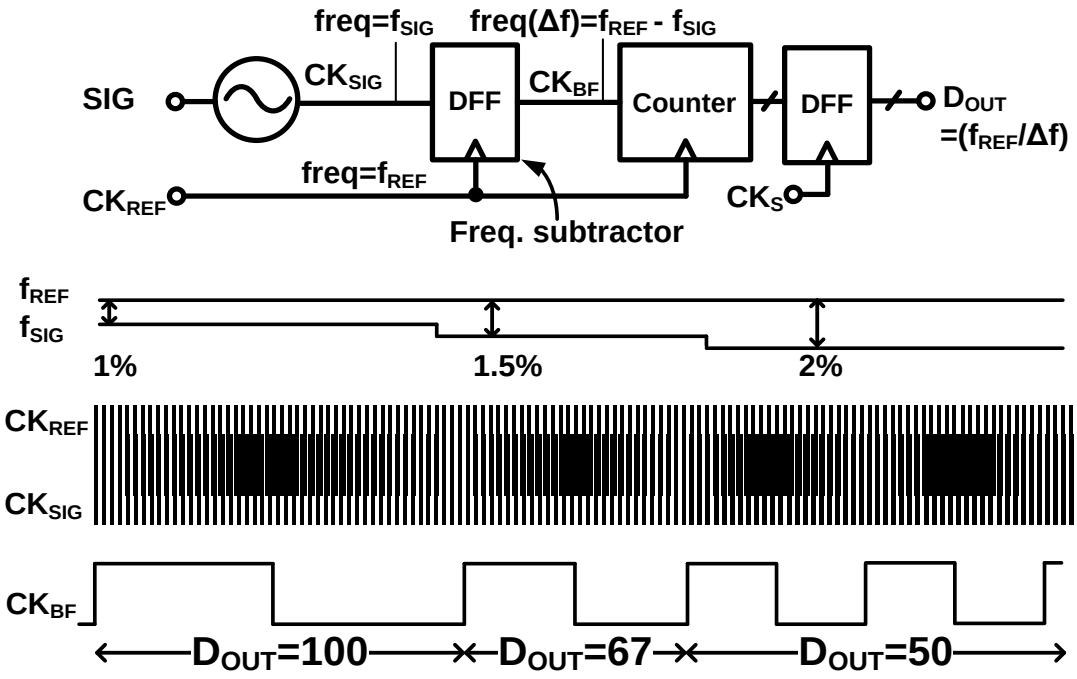


Fig. 2.5: Beat frequency based signal detection [14]. For an initial frequency difference of 1%, an additional 1% change in input frequency can change the output code by 50%. In contrast, the same change in input frequency would result in a 1% change in the output code for the conventional VCO based linear quantizer in Fig. 2.4.

Fig. 2.6(a) illustrates how a low swing sinusoidal input causes large variation at the output of the BF quantizer. Since D_{OUT} is inversely proportional to Δf (Fig. 2.6(b)), it is very sensitive to input variation (i.e. the slope in the transfer characteristic is high) for a small Δf. Quantization step (Δ_i) is directly dependent on the count value i of D_{OUT} . As a result, Δ_q is very low for small Δf achieving high resolution for low swing input signal. When Δf increases, as evident from output waveform in Fig. 2.6(a) and also from the Δ_q vs. f_{SIG} plot in Fig. 2.6(c), That is, D_{OUT} becomes less sensitive to Δf, increasing Δ_q and degrading the resolution of the BF quantizer.

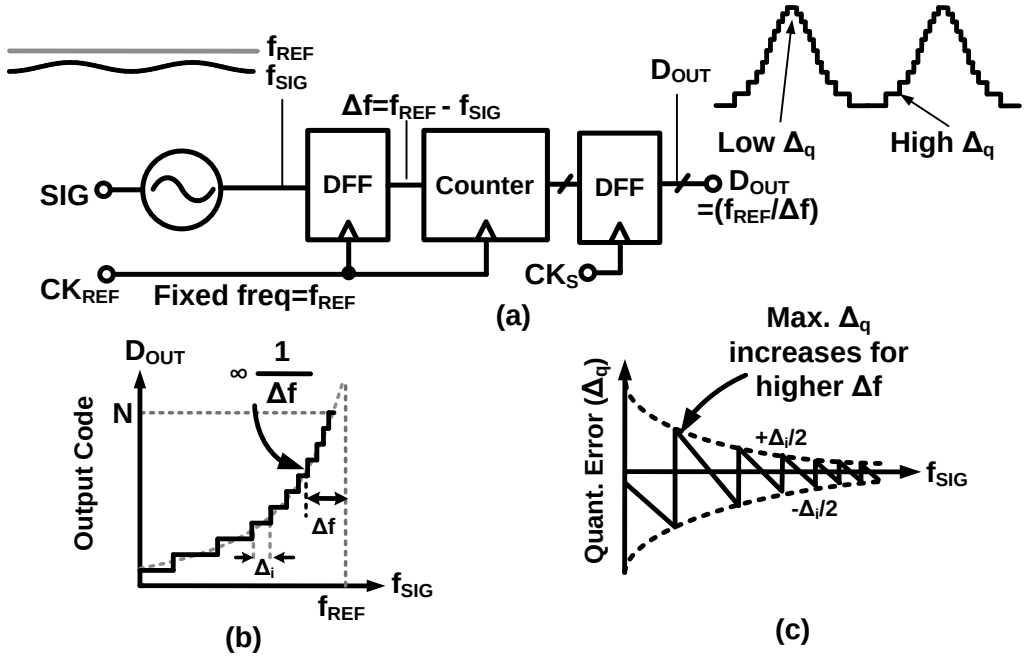


Fig. 2.6: (a) Beat frequency based single-step quantizer. (b) Output code is inversely proportional to signal-to-reference voltage difference. (c) Quantization step size is higher for lower f_{SIG} and that effectively degrades resolution.

Further improvements can be made on the simple BF-ADC quantizer, such as introducing first order noise shaping as described in Fig. 2.7. In the first BF-ADC implementation [10] the VCO resets after each BF clock period and as a result, the quantization error information is lost. In contrast, the BF quantizer implementation in this work which is similar to [11], measures the BF count continuously in every BF cycle without resetting the VCO as shown in Fig. 2.7(a). As a result, the quantization error information is preserved and accounted in the subsequent BF cycle. BF quantizer output in Fig. 2.7(b) for an input ramp shows the noise shaping behavior similar to a first-order delta-sigma modulator.

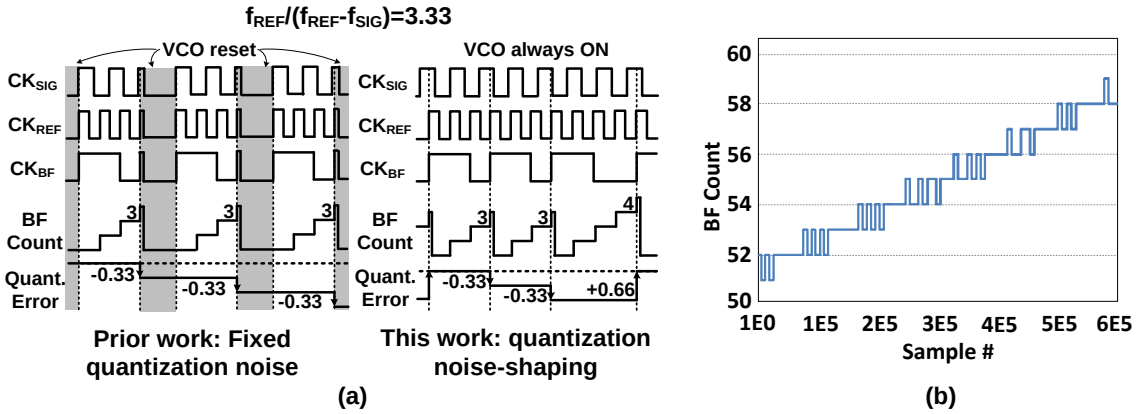


Fig. 2.7: (a) Quantization noise shaping enabled by continuous beat-frequency counting. (b) Output code for an input ramp, showing noise-shaping behavior similar to a first order delta-sigma modulator.

2.2.3. *Two-step Beat Frequency Quantizer*

A two-step BF quantizer in Fig. 2.8(a) employing multiple clock references (CK_0-CK_{n-1}) to address the issue of degraded resolution under large input variation is proposed in this work. The quantization is performed in two steps. The first step is similar to the previously explained BF quantizer with a fixed reference clock (CK_0) and it is used to detect the signal level using a rough estimation of the BF count (D_{OUT1}). Therefore very high resolution is not essential here. Once the signal level is known, the reference frequency (f_{REF2}), which is closest to f_{SIG}, is picked by the selection logic and a MUX. Final quantization is performed at the second step generating a high output count (D_{OUT2}) even for a larger signal swing. In this way, a small reference to signal beat frequency (Δf_2) is always maintained, minimizing Δ_q over a wide dynamic range (Fig. 2.8(b,c)). Even though f_{REF2} varies with the input, its value corresponding to each D_{OUT2} is known from D_{OUT1} so the signal can be reconstructed accurately. The number of reference levels

and the frequency spacing among them can also be adaptively controlled depending on the type of bio-potential signal and its maximum voltage swing.

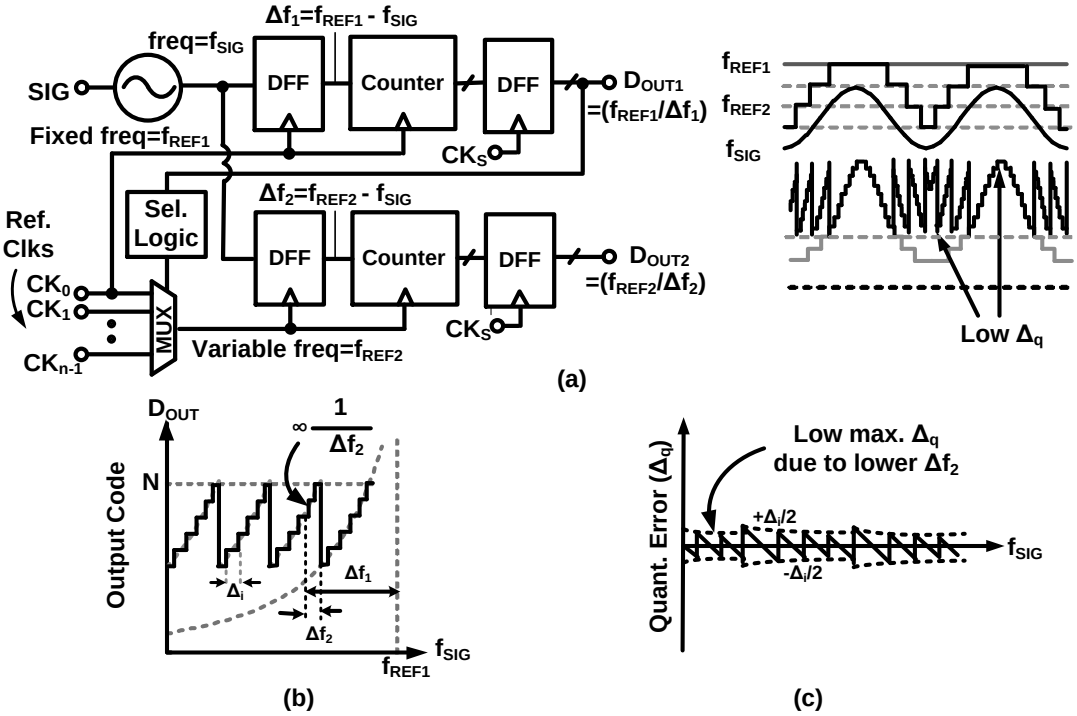


Fig. 2.8: (a) Proposed two-step beat frequency quantizer using multiple references. (b) BF count is always high irrespective of the signal swing. (c) Quantization step-size is always very small ensuring higher resolution for a wider input range.

2.3 Calculation of Quantization Noise and SNR

The quantization step size in BF-ADC, as explained in previous section, depends on the beat frequency count. Therefore, the calculation for quantization noise and SNR is different from a conventional linear ADC. The following section discusses the procedure to calculate these parameters for both the single-step and the two-step BF-ADC comparing the results with a VCO based linear ADC. Since we are only focusing on

VCO based quantizers where signals are converted from voltage domain to frequency domain, a frequency is treated as an equivalent voltage and then SNR is calculated. This doesn't alter the actual SNR result, as it is simply the ratio between signal and noise power canceling the voltage to frequency transformation factor; i.e. VCO gain K_{VCO}:

2.3.1. *VCO based Linear ADC*

First consider the case of an ideal linear VCO based ADC from Fig. 2.4(a). The counter output varies between 0 to N for a rail-to-rail input. Now, for an input frequency change of f_C, if output count changes by 1 LSB, the quantizer frequency resolution, as shown in Fig. 2.9(a), can be written as:

$$\Delta = f_C \tag{2.1}$$

Therefore, the full scale or rail-to-rail swing is Nf_C. Since the quantization error Δ_q varies between $+\Delta/2$ to $-\Delta/2$, for a uniform distribution of Δ_q, the quantization noise power can be expressed as the mean square of Δ_q :

$$P_n = \overline{\Delta_q^2} = \frac{\Delta^2}{12} = \frac{f_c^2}{12} \tag{2.2}$$

If a sinusoidal input (f_{SIG}) of amplitude A_{sig}, generates a peak-to-peak count variation of M, signal swing is expressed as:

$$2A_{sig} = Mf_C \tag{2.3}$$

Its total power is equal to:

$$P_{sig} = \frac{A_{sig}^2}{2} = \frac{M^2 f_c^2}{8} \tag{2.4}$$

Thus, SNR at the output is:

$$SNR = \frac{P_{sig}}{P_n} = \frac{3}{2}M^2 \tag{2.5}$$

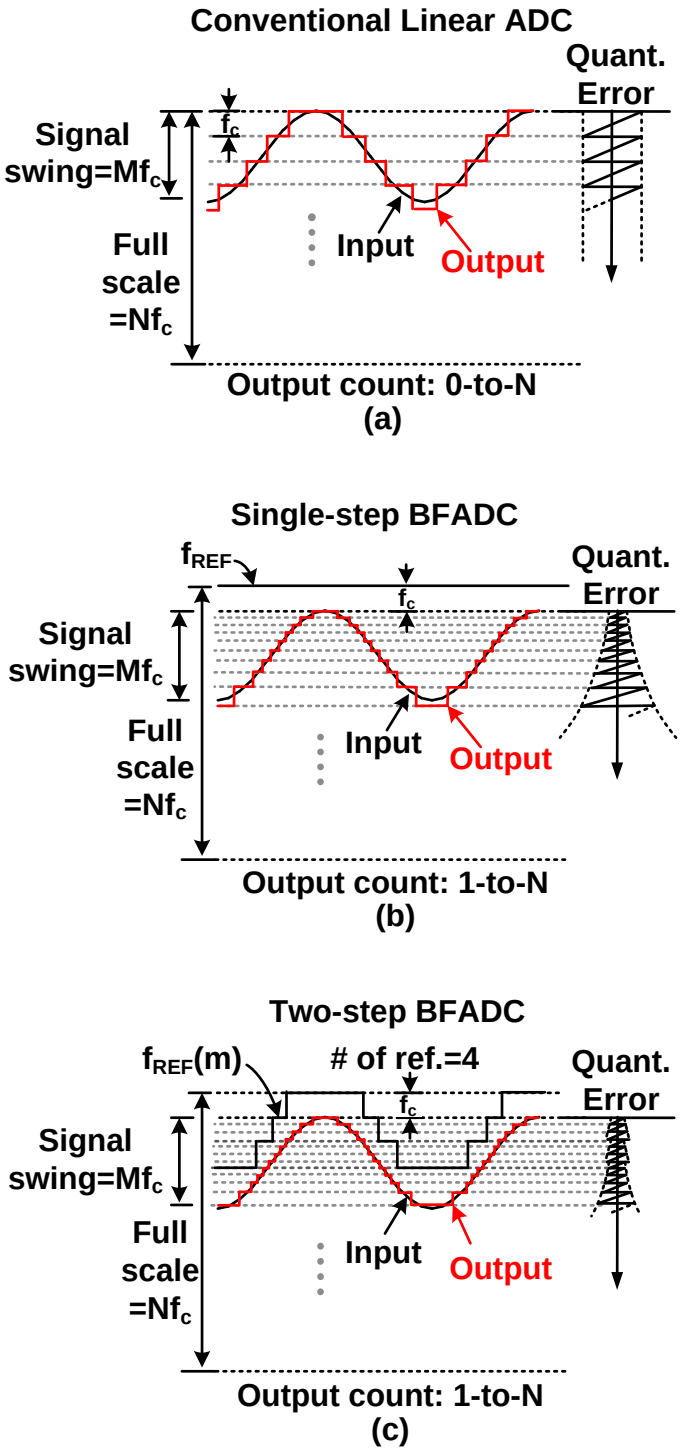


Fig. 2.9: Quantization noise and SNR calculation of conventional linear ADC, single-step and two-step BF-ADC

Equation (2.5) shows that SNR is proportional to the square of the input amplitude with a peak SNR $= \frac{3}{2}N^2$ for a rail-to-rail input. If the signal is only 1% of the rail-to-rail which is quite possible in bio-potential signals, SNR will be 40dB below the peak value.

2.3.2. *Single Step BF-ADC*

Next, let's assume the same input is applied to a BF quantizer of Fig. 2.6(a). The maximum BF count (N), decided by the minimum Δf (i.e. Δf_{min}) between the reference (f_{REF}) and the signal (f_{SIG}) is written as:

$$N = \frac{f_{REF}}{\Delta f_{min}} \tag{2.6}$$

As shown in Fig. 2.9(b), $\Delta f_{min}=f_C$ to keep the full scale (0 to f_{REF}) range Nf_C, same as used in linear VCO analysis for a fair comparison. Since, the quantization step size (Δ_i) is not fixed and depends on the BF count (i), Δ_i can be calculated from the effective input change to increase the counter output from i to i+1, which is:

$$\Delta_i = f_{REF}\left(\frac{1}{i} - \frac{1}{i+1}\right) = Nf_C\left(\frac{1}{i} - \frac{1}{i+1}\right) \tag{2.7}$$

It is clear from equation (2.7) that Δ_i reduces as i increases and vice-versa. For an input signal having peak-to-peak swing Mf_C (from equation (2.3)), BF count at the input minima is $i_{min}=f_{REF}/(M+1)f_C=N/(M+1)$. Therefore i can have the value between i_{min} to N-1, depending on the input. If N/(M+1) is not an integer, i_{min} will toggle between its two nearest integers generating an average value of N/(M+1). Now, the peak-to-peak signal swing in terms of Δ_i is expressed as:

$$\sum_i \Delta_i = 2A_{sig} = Mf_C, \quad \text{for} \quad i = i_{min}, i_{min}+1, \ldots., N-2, N-1 \tag{2.8}$$

For the signal residing within Δ_i, the quantization noise (Δ_{qi}) lies between + $\Delta_i/2$ to - $\Delta_i/2$, generating quantization noise power:

$$P_{ni} = \frac{\Delta_i^2}{12} = \frac{N^2 f_C^2}{12}\left(\frac{1}{i} - \frac{1}{i+1}\right)^2 \tag{2.9}$$

Considering the signal to be uniformly distributed among each Δ_i having quantization noise P_{ni}, the total quantization noise power can be expressed as:

$$P_n = \frac{\sum_i \Delta_i P_{ni}}{\sum_i \Delta_i} = \frac{N^3 {f_c}^2}{12M}\sum_i \left(\frac{1}{i} - \frac{1}{i+1}\right)^3 \tag{2.10}$$

Signal power remains the same as derived in equation (2.4) of the linear ADC analysis. Therefore SNR is written as:

$$SNR = \frac{P_{sig}}{P_n} = \frac{3}{2}\left(\frac{M}{N}\right)^3 \frac{1}{\sum_i \left(\frac{1}{i} - \frac{1}{i+1}\right)^3} \tag{2.11}$$

It is evident from the equation (2.11) that SNR is dependent on both signal amplitude and BF counts.

2.3.3. *Two Step BF-ADC*

The above methodology to calculate the quantization noise and SNR of a single-step BF-ADC can be extended to the proposed two-step BF-ADC as well. Since reference frequency depends on signal level, it can be represented as:

$$f_{REF}(m) = f_{REF} - mf_C = (N - m)f_C \tag{2.12}$$

Here frequency difference between two adjacent references is assumed to be f_C to simplify the calculation. f_{REF}=Nf_C is the reference frequency for the first-step of BF quantization and m is a variable whose value is decided by the instantaneous level of the input signal, as shown in Fig. 2.9(c). If the signal peak-to-peak swing (Mf_C) is less than

f_C, m is equal to 0. For Mf_C lies between f_C and $2f_C$, m switches between 0 or 1 depending on the input and so on. Let's assume the maximum value of m for any give Mf_C is m′. Δ_i in this case can be expressed as:

$$\Delta_i = f_{REF}(m)\left(\frac{1}{i} - \frac{1}{i+1}\right) = (N - m)f_C\left(\frac{1}{i} - \frac{1}{i+1}\right) \tag{2.13}$$

The BF count at the input minima for the peak-peak swing Mf_C is:

$$i_{min} = \frac{f_{REF}(m')}{(M+1-m')f_C} = \frac{N-m'}{M+1-m'} \tag{2.14}$$

In the two-step BF-ADC, whenever Δf reaches a maximum value of $2f_C$, m increments reducing Δf to f_C. Therefore BF count cannot reach below N/2. However, we can only have a few reference signals available due to the implementation issues and BF count may go below N/2 when m=m′. Therefore, count i varies between i_{min} to N-1 when m= m′ and between N/2 to N for other values of m. The peak-to-peak swing can be written as:

$$\sum_i \Delta_i = 2A_{sig} = Mf_C, \qquad \text{for } i = \{i_{min}, i_{min}+1, \ldots., N-1\}, \{\frac{N}{2} \ldots., N-1\}, \ldots.\{\frac{N}{2}, \ldots., N-1\} \tag{2.15}$$

Quantization noise power for a uniform distribution of signal among each Δ_i is:

$$P_n = \frac{\sum_i \Delta_i P_{ni}}{\sum_i \Delta_i} = \frac{{f_c}^2}{12M}\sum_i (N-m)^3\left(\frac{1}{i} - \frac{1}{i+1}\right)^3 \tag{2.16}$$

Therefore, the SNR at the output of the two-step BF-ADC is given as:

$$SNR = \frac{P_{sig}}{P_n} = \frac{3}{2}M^3 \frac{1}{\sum_i (N-m)^3\left(\frac{1}{i} - \frac{1}{i+1}\right)^3} \tag{2.17}$$

Maximum quantization step size (Δ_i), normalized to f_C, obtained from equations (2.1), (2.7) and (2.13) for different input amplitudes are plotted in Fig. 2.10(a) for N=128.

SNR calculated using equations (2.5), (2.11) and (2.17) are plotted in Fig. 2.10(b). X-axis input amplitude is expressed in dBFS i.e. 20log(M/N). The number of references in two-step ADC is assumed to be four, which is same as in the actual test chip implementation.

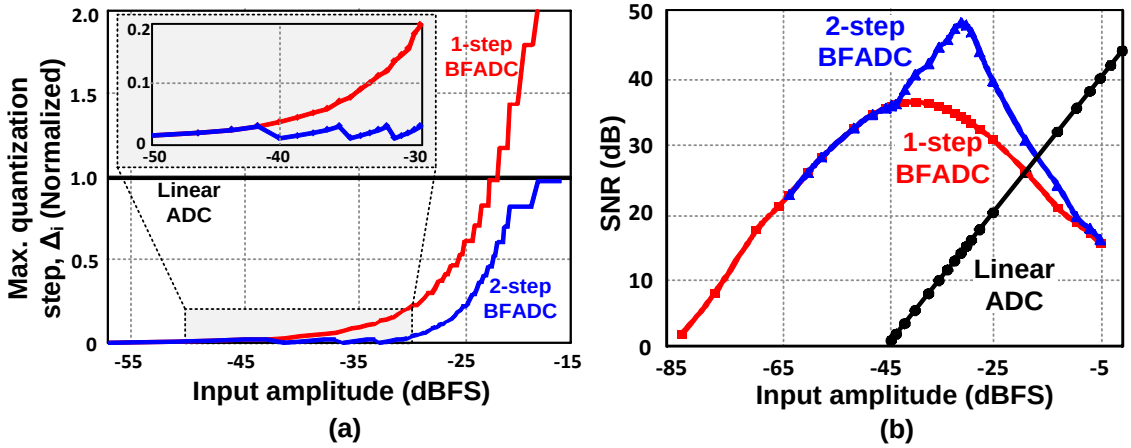


Fig. 2.10: Quantization step size and SNR calculated for different signal amplitude using the derived model. For two-step BF-ADC, the number of references is assumed to be four, as used in the actual chip implementation

2.3.4. *First Order Noise Shaping*

The quantization noise, P_n so far in the analysis is assumed to be white, which implies, it is uniformly distributed between 0 to $f_s/2$ in the output frequency spectrum (f_s is the sampling clock frequency). However in actual scenario, due to the first-order noise shaping property of the quantizer, which is described in section 2.2.2, the quantization noise power is shaped by the transfer function $|1\text{-}z^{-1}|^2$ before appearing at the output. Therefore, for an input signal bandwidth of f_{BW}, total in-band quantization noise (P_{ns}) after first order noise shaping can be calculated as:

$$P_{ns} = \frac{P_n}{f_s/2}\int_0^{f_{BW}} |1 - z^{-1}|^2 df \qquad (2.18)$$

Now $|1-z^{-1}|\approx 2\pi fT$ where $T=1/f_s$. For a given oversampling ratio (OSR), which is $f_s/2f_{BW}$, equation (2.18) can be simplified to:

$$P_{ns} \approx \frac{P_n}{f_s/2}\int_0^{f_s/2OSR}\left(\frac{2\pi f}{f_s}\right)^2 df = P_n\frac{\pi^2}{3}(OSR)^{-3} \qquad (2.19)$$

Equation (2.19) and the formulas derived in equation (2.2), (2.10) and (2.16) can be utilized to recalculate the SNR (i.e. P_{sig}/P_{ns}) with 1st order noise shaping. Fig. 2.11 plots the SNR for OSR of 4 and N=128.

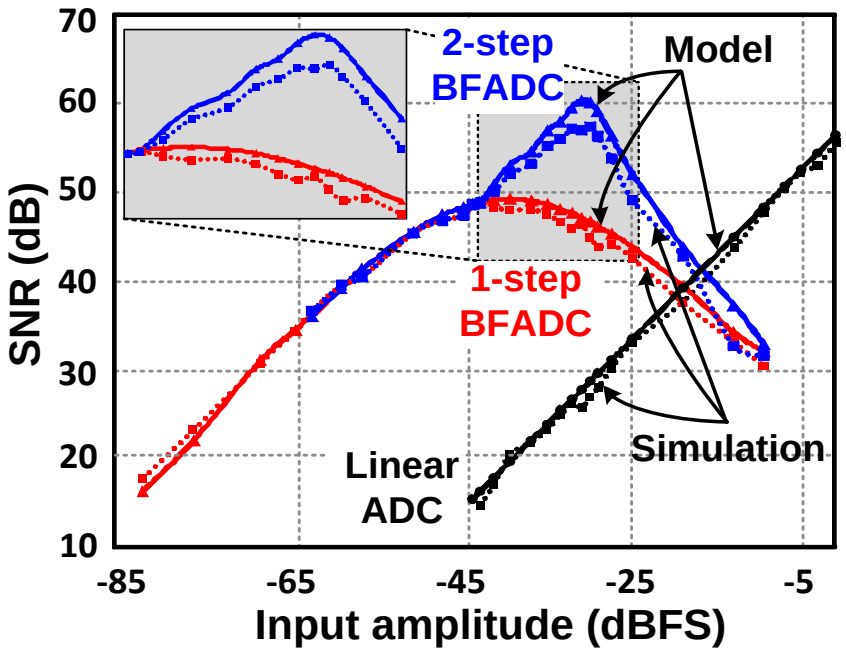


Fig. 2.11: Calculated SNR considering 1st order noise shaping by the quantizer. SNR values obtained from the mathematical model (solid line) is compared with the behavioral transient simulation results (dotted line) in Matlab for OSR=4.

In order to verify the proposed analysis, behavioral transient simulations are performed using Matlab for a 300Hz sinusoidal input. Signal bandwidth for SNR calculation is 1.2kHz and sampling frequency is 9.6kHz to make OSR=4. Here one thing to note that since the SNR is primarily dependent on the OSR value and the input

amplitude; 300Hz input or 1.2kHz bandwidth has no impact on the calculated SNR when OSR is fixed. These values are picked to keep consistency with the measurement set-up, which will be discussed in section VI. The SNR calculated from behavioral simulations show good agreement with the mathematical model as evident from in Fig. 2.11. Simulated output FFT plots for both one-step and two-step BF ADCs are shown in Fig. 2.12 for input amplitude of -30dBFS. SNR calculated from the FFT are 46.5dB and 57.3dB in one-step and two-step case respectively.

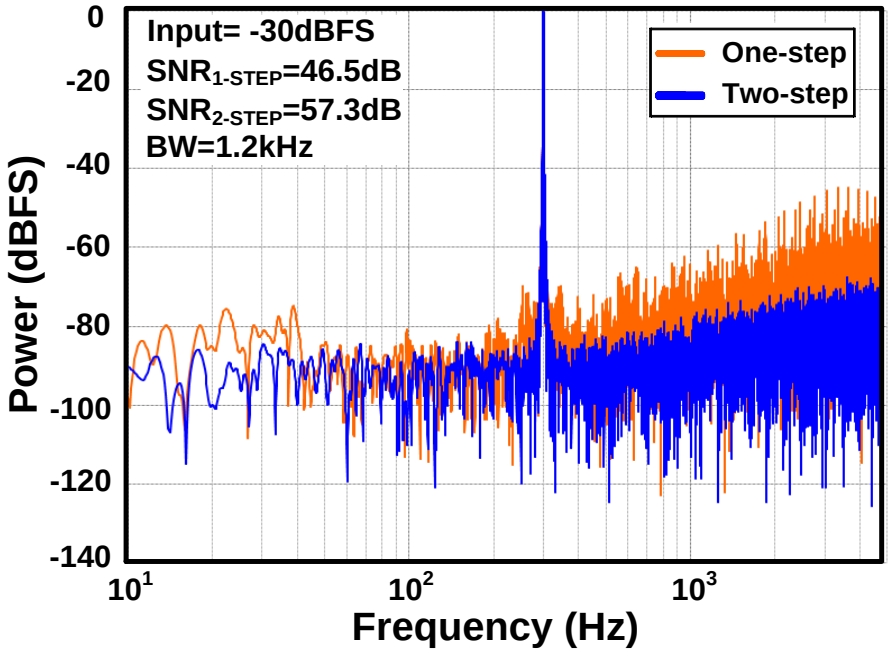


Fig. 2.12: FFT plot from the behavioral transient simulation using a 300Hz sinusoidal input with OSR=4.

2.4 Impact of VCO Jitter in the BFADC Performance

This section discusses the impact of VCO clock jitter in the BFADC performance. The analysis of clock jitter impact in a VCO based linear ADC design is explained in

[16]. As shown in Fig. 2.13, in a conventional VCO based linear ADC the VCO converts the input x(t) to a clock having frequency $f_{in}(t) = K_{VCO}.x(t) + f_0$. Here f_0 and K_{VCO} are the VCO free running frequency and gain respectively. The n^{th} sample of the quantizer output (Out[n]) is the integer ratio of the average VCO frequency, $\overline{f_{in}}[n]$, to the sampling clock frequency, $f_S[n]$, within the time interval nT_S to $(n+1)T_S$. In an ideal case i.e. without any clock jitter, $\overline{f_{in}}[n] = \frac{1}{T_S}\int_{nT_s}^{(n+1)T_s} f_{in}(t)dt$ and $f_S[n] = 1/T_S$. Therefore, the output of a linear quantizer is expressed as:

$$Out[n] = \frac{\overline{f_{in}}[n]}{f_S[n]} + Q[n] = \int_{nT_s}^{(n+1)T_s}(K_{VCO}.x(t) + f_0).dt + Q[n] \qquad (2.20)$$

where Q[n] is the quantization error. Out[n], a function of input phase, can be written as:

$$Out[n] = \frac{1}{2\pi}\left(\Phi_x[n] + \Phi_q[n-1] - \Phi_q[n]\right) \qquad (2.21)$$

$\Phi_x[n] = \int_{nT_s}^{(n+1)T_s} 2\pi(K_{VCO}.x(t) + f_0).dt$ is the phase domain representation of the input x(t). Due to the first order noise shaping of the quantizer, $Q[n] = \frac{1}{2\pi}\left(\Phi_q[n-1] - \Phi_q[n]\right)$, where $\Phi_q[n]$ is the phase quantization error. Since the effect of quantization error is already discussed in previous section, here the focus is only on $\Phi_x[n]$.

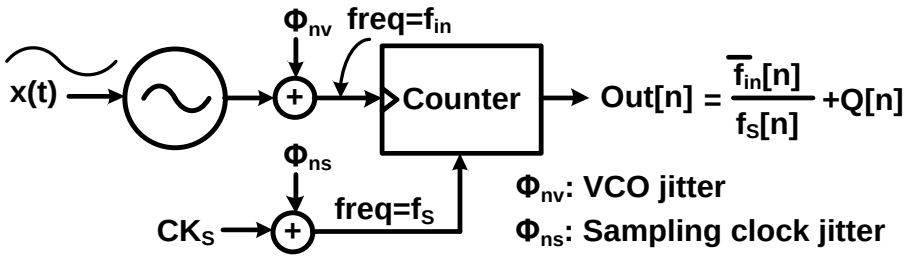


Fig. 2.13: VCO and sampling clock jitter impact in linear VCO based ADC

The impacts of sampling and VCO clock jitters in a linear VCO based ADC, as shown in Fig. 2.13, are summarized below:

1. Sampling clock jitter (Φ_{ns}): The sampling clock jitter has two effects. a) The absolute jitter ($t_{aj}[n]$) causes sampling uncertainty and creates a skirt around the signal in the frequency spectrum. b) The period jitter ($t_{pj}[n] = t_{aj}[n+1] - t_{aj}[n]$) causes error in the integrated output due to variation in integration time and raises the noise floor of the frequency spectrum.

   $\Phi_x[n]$, with the sampling clock jitter, can be written as:

$$\Phi_{x,ns}[n] = \int_{nT_s+t_{aj}[n]}^{(n+1)T_s+t_{aj}[n+1]} 2\pi(K_{VCO}.x(t) + f_0).dt \tag{2.22}$$

2. VCO clock jitter (Φ_{nv}): The accumulated jitter over the sampling period (T_S) creates integration error. As a result the noise floor in the output frequency spectrum increases.

   Considering the accumulated VCO jitter, $\Phi_{nv}[n] = \int_{nT_s}^{(n+1)T_s} 2\pi K_{VCO}.v_n(t).dt$, where $v_n(t)$ is input referred VCO voltage noise, the expression for $\Phi_x[n]$ is:

$$\Phi_{x,nv}[n] = \int_{nT_s}^{(n+1)T_s} 2\pi\big(K_{VCO}.ref + f_0 + K_{VCO}v_n(t)\big).dt \tag{2.23}$$

Above analysis, which is also explained in [16], can be extended for the proposed BFADC design. Similar to the linear case, BFADC also has two separate clock sources: the input VCO and the reference VCO as shown in Fig. 2.14. Since the sampling clock i.e. the beat frequency (CK_{BF}) is derived from both the VCOs, the impact is different than the linear case.

Similar to equation (2.20) and (2.21), the output of the BF quantizer can be represented as:

$$\mathrm{Out}[n] = \frac{\overline{f_{ref}}[n]}{f_{BF}[n]} + Q[n] = \frac{1}{2\pi}\left(\Phi_x[n] + \Phi_q[n-1] - \Phi_q[n]\right) \qquad (2.24)$$

where $\overline{f_{ref}}[n]$ is the average reference VCO frequency between n^{th} and $(n+1)^{th}$ rising edge of the BF clock appearing at time $T_0[n]$ and $T_0[n+1]$ respectively when there is no clock jitter. The frequency of the n^{th} beat period is $f_{BF}[n] = \frac{1}{T_0[n+1]-T_0[n]}$ which is also equal to $K_{VCO}\left(ref - \overline{x(T_0[n])}\right)$, as it is the frequency difference between the reference and input VCOs. $\overline{x(T_0[n])}$ is the average of x(t) in the time interval $T_0[n]$ to $T_0[n+1]$ and ref is the fixed reference VCO input voltage.

As a result, ignoring the VCO jitter, $\Phi_x[n]$ is expressed as:

$$\Phi_x[n] = \int_{T_0[n]}^{T_0[n+1]} 2\pi(K_{VCO}.\,ref + f_0).\,dt = \frac{2\pi(K_{VCO}.ref+f_0)}{K_{VCO}\left(ref-\overline{x(T_0[n])}\right)} \qquad (2.25)$$

Now the jitter contribution of each VCO in the BFADC is explained separately.

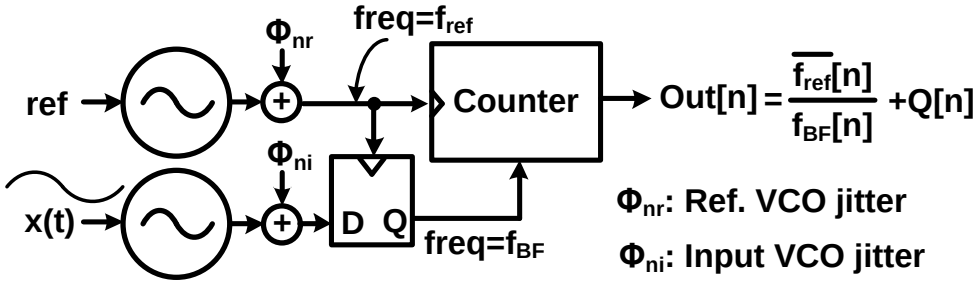


Fig. 2.14: The impact of the reference and the input VCO jitter in BFADC

2.4.1. *Reference VCO jitter (Φ_{nr})*

The reference VCO output (CK_{ref}) is utilized for the beat frequency generation as well as incrementing the counter. Since the beat frequency clock, CK_{BF} is synchronized to the rising edge of CK_{ref}, any jitter in reference VCO modulates both CK_{ref} and CK_{BF} by the same amount and there is no change in output count (Out[n]). Fig. 2.15 explains how the correlated noise keeps the count value independent of the VCO jitter. However, the absolute jitter ($t_{aj}[n]$) introduces error due to sampling uncertainty.

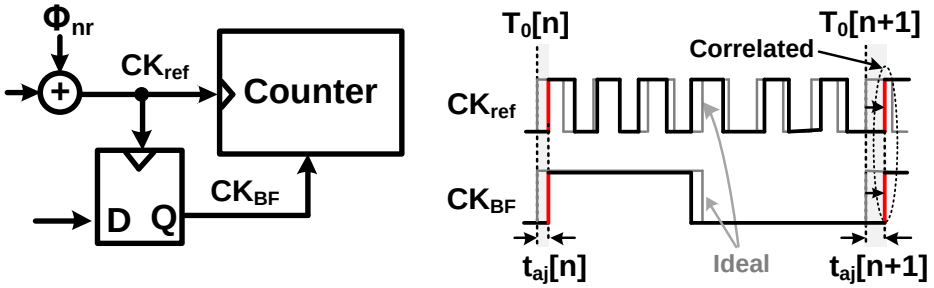


Fig. 2.15: The effect of the reference VCO jitter. Correlated noise present in Φ_{ref} and Φ_{BF} doesn't change Out[n], but causes sampling uncertainty.

The effect of above explained reference VCO jitter is analyzed mathematically. The phase noise of the reference VCO, Φ_{nr} in Fig. 2.14 can be expressed in terms of the input referred voltage noise, $v_{nr}(t)$ and they are related as: $\Phi_{nr}(t) = \int_0^t 2\pi K_{VCO} v_{nr}(t)dt$. Φ_{nr} introduces jitter in both CK_{ref} and CK_{BF}. The absolute jitter $t_{aj}[n]$ is defined as the time difference between the n^{th} edge of the ideal and the practical BF clock i.e. CK_{BF}. Therefore, the n^{th} edge of CK_{BF} now appears at $T_0'[n] = T_0[n] + t_{aj}[n]$. As a result, with the presence of Φ_{nr}, equation (2.25) can be modified as:

$$\Phi_{x,nr}[n] = \int_{T_0'[n]}^{T_0'[n+1]} 2\pi\left(K_{VCO}.\,ref + f_0 + K_{VCO}v_{nr}(t)\right).dt$$

$$= \int_{T_0'[n]}^{T_0[n+1]+t_{aj}[n]} 2\pi(K_{VCO}.\,ref + f_0).dt + \int_{T_0[n+1]+t_{aj}[n]}^{T_0'[n+1]} 2\pi(K_{VCO}.\,ref + f_0).dt +$$

$$\int_{T_0'[n]}^{T_0'[n+1]} 2\pi K_{VCO}v_{nr}(t).dt \tag{2.26}$$

The second term in the above equation i.e. $\int_{T_0[n+1]+t_{aj}[n]}^{T_0'[n+1]} 2\pi(K_{VCO}.\,ref + f_0).dt$ represents the phase integration error in CK_{ref} due to the BF period jitter, which is $t_{aj}[n+1] - t_{aj}[n]$. The third term i.e. $\int_{T_0'[n]}^{T_0'[n+1]} 2\pi K_{VCO}v_{nr}(t).dt$ is the accumulated phase error over the beat period that introduces the period jitter of $t_{aj}[n+1] - t_{aj}[n]$. Since Φ_{nr} introduces equal error in CK_{ref} and CK_{BF} edge, second and third term will cancel each other keeping only the first term, which is written as:

$$\Phi_{x,nr}[n] = \int_{T_0[n]+t_{aj}[n]}^{T_0[n+1]+t_{aj}[n]} 2\pi(K_{VCO}.\,ref + f_0).dt \tag{2.27}$$

Since the time integral range is same as the ideal beat period i.e. $T_0[n+1] - T_0[n]$, but time shifted by $t_{aj}[n]$, above equation can be expressed as:

$$\Phi_{x,nr}[n] = \frac{2\pi(K_{VCO}.ref+f_0)}{K_{VCO}\left(ref-\overline{x\left(T_0[n]+t_{aj}[n]\right)}\right)} \tag{2.28}$$

$\overline{x\left(T_0[n] + t_{aj}[n]\right)}$ is the average of x(t) in the time interval $T_0[n] + t_{aj}[n]$ to $T_0[n+1] + t_{aj}[n]$. Assuming $T_0[n+1] - T_0[n] >> t_{aj}[n]$, we can write: $\overline{x\left(T_0[n] + t_{aj}[n]\right)} \approx \overline{x(T_0[n])} + \frac{dx}{dt}t_{aj}[n]$. Therefore, equation (2.28) can be simplified as:

$$\Phi_{x,nr}[n] = \frac{2\pi(K_{VCO}.ref+f_0)}{K_{VCO}\left(ref-\left(\overline{x(T_0[n])}+\frac{dx}{dt}t_{aj}[n]\right)\right)} \tag{2.29}$$

Since x(t) is inversely proportional to Out[n], $\left(\Phi_{x,nr}[n]\right)^{-1}$ is our interest considering the fact that signal must be reconstructed from Out[n] by inverse transformation. Therefore, using equation (2.25) and (2.29):

$$\left(\Phi_{x,nr}[n]\right)^{-1} = (\Phi_x[n])^{-1} + \frac{K_{VCO}}{2\pi(K_{VCO}.ref+f_0)}\left(\frac{dx}{dt}\right)t_{aj}[n] \quad (2.30)$$

Second term in the RHS of the above equation corresponds to the phase error due to sampling uncertainty ($\Phi_{su}[n]$) which is dependent on the absolute jitter $t_{aj}[n]$ and the input slew rate. The effect is similar to the conventional voltage based linear ADC [17].

The Fourier transform of $(\Phi_{su}[n])^{-1}$ i.e. $\Phi_{su}^{-1}(\omega)$, obtained by convolving the frequency spectrum of x(t) and $t_{aj}[n]$, is written as:

$$\Phi_{su}^{-1}(\omega) = \frac{K_{VCO}}{2\pi(K_{VCO}.ref+f_0)}\omega X(\omega) * T_{aj}(\omega) \quad (2.31)$$

$X(\omega)$ and $T_{aj}(\omega)$ are the frequency spectrum of x(t) and $t_{aj}[n]$ respectively. Due to the frequency domain convolution, $T_{aj}(\omega)$ is upconverted to the signal frequency and forms a skirt around it.

2.4.2. *Input VCO jitter (Φ_{ni})*

The input VCO generates output (CK_{in}) of frequency proportional to the input x(t) that is utilized for CK_{BF} generation by a DFF. Therefore, the jitter introduced by the VCO phase noise (Φ_{ni}) appears at CK_{BF}. This causes both sampling uncertainty due to the absolute jitter ($t_{aj}[n]$) and integration error due to the period jitter ($t_{pj}[n]$), similar to the sampling clock jitter in a conventional VCO based linear ADC explained previously.

However, CK_{in} is resynchronized to the positive edge of CK_{ref} by the DFF during CK_{BF}. As a result, the jitter present in CK_{in} is quantized by CK_{ref}. For example, absolute

jitter ($t_{aj}[n]$) between 0 to T_{ref} present in CK_{in} translates into a period jitter of either 0 or T_{ref} in CK_{BF}. This mechanism, as explained in Fig. 2.16, is similar to a bang-bang phase detector [18] where input phase difference translated into binary output of 0 or 1. The random noise or jitter present in CK_{in} helps to linearize the input to output jitter transfer function. Following the gain calculation method of a BBPD derived in [18] for a long time window, the absolute jitter present at the n^{th} rising edge of CK_{BF} can be approximated as:

$$\hat{t}_{aj}[n] \approx \sqrt{\frac{2}{\pi}\frac{T_{ref}}{\sigma_{tj}}}\, t_{aj}[n] \tag{2.32}$$

where σ_{tj} is the RMS value of the absolute jitter in CK_{BF}.

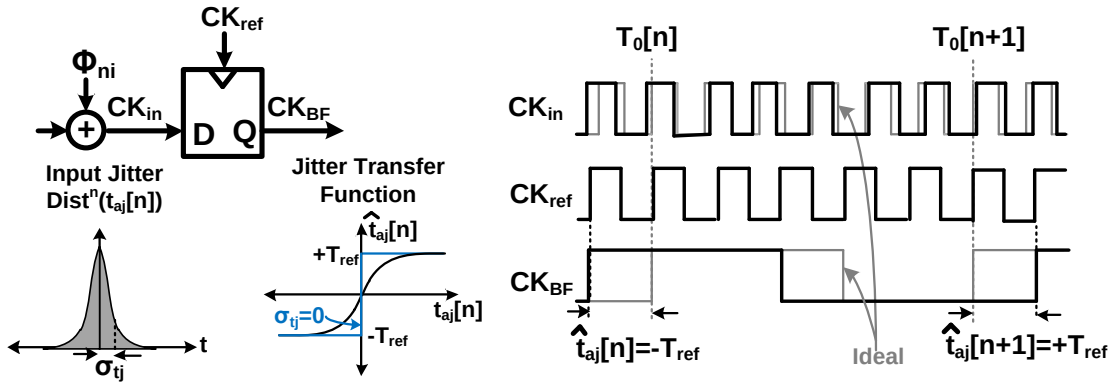


Fig. 2.16: The jitter present in reference VCO is quantized by the BF detector.

Similar to the previous analysis, $\Phi_x[n]$ under the presence of input VCO noise Φ_{ni} is expressed as:

$$\Phi_{x,nr}[n] = \int_{T'_0[n]}^{T'_0[n+1]} 2\pi(K_{VCO}.\,ref + f_0).\,dt \tag{2.33}$$

In this case, $T_0'[n] = T_0[n] + \hat{t}_{aj}[n]$ is the time of n^{th} rising edge of CK_{BF}. Since $\Phi_{ni} = 0$ in this analysis, the reference frequency is constant at $K_{VCO}.\,ref + f_0$. Equation (2.30) can be decomposed in the following way:

$$\Phi_{x,nr}[n] = \int_{T_0[n]+\hat{t}_{aj}[n]}^{T_0[n+1]+\hat{t}_{aj}[n]} 2\pi(K_{VCO}.\,ref + f_0).\,dt$$

$$+ \int_{T_0[n+1]+\hat{t}_{aj}[n]}^{T_0[n+1]+\hat{t}_{aj}[n+1]} 2\pi(K_{VCO}.\,ref + f_0).\,dt$$

$$= \int_{T_0[n]+\hat{t}_{aj}[n]}^{T_0[n+1]+\hat{t}_{aj}[n]} 2\pi(K_{VCO}.\,ref + f_0).\,dt + 2\pi(K_{VCO}.\,ref + f_0).\,\hat{t}_{pj}[n] \qquad (2.34)$$

Here, $\hat{t}_{pj}[n] = \hat{t}_{aj}[n+1] - \hat{t}_{aj}[n]$ is the period jitter of the n^{th} period in CK_{BF}. Therefore, the first term in the RHS of equation (2.34), which is identical to equation (2.25) in the reference VCO case, represents the sampling uncertainty due to absolute jitter $\hat{t}_{aj}[n]$ and the second term is the phase integration error generated from the period jitter $\hat{t}_{pj}[n]$.

In order to verify the aforementioned mathematical analysis, a behavioral transient simulation is performed in Matlab with and without the VCO clock jitter and their output FFT plots are compared in Fig. 2.17. Input signal is 300Hz while each VCO is operating at 10MHz. The VCO RMS absolute jitter is assumed to be 1ns (1% of VCO time period). Signal bandwidth and sampling frequency are 1.2kHz and 9.6kHz respectively which makes OSR=4. As expected, the skirt centered around the input frequency in the FFT plot is due to the sampling uncertainty caused by the absolute jitter in two VCOs. The noise floor is raised due to the integration error generated from the input VCO jitter as well as the sampling uncertainty caused by both VCOs. As a result, SNDR is degraded from 46.5dB to 41dB.

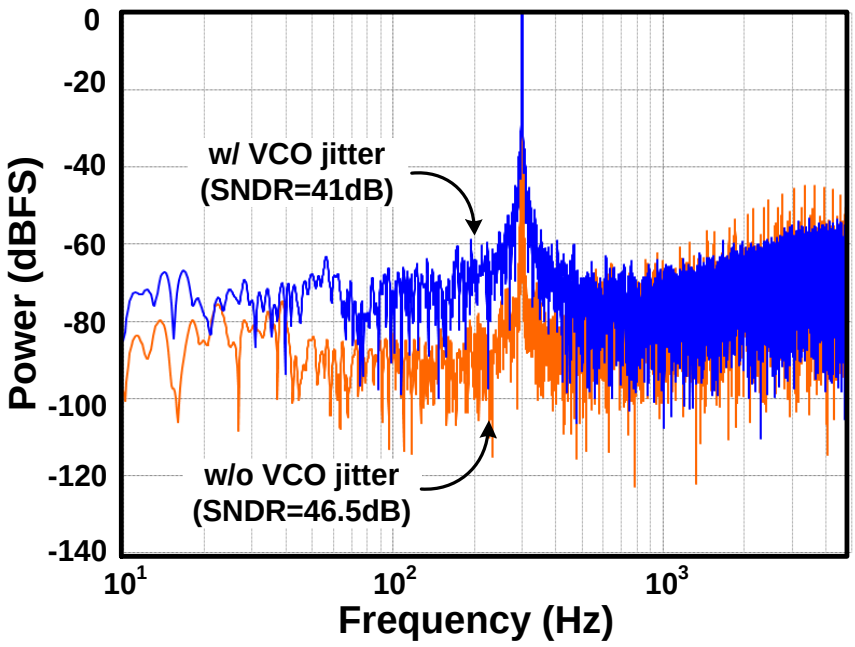


Fig. 2.17: Simulated FFT plot of BFADC without and with VCO jitter.

2.5 Triple Sampling Synchronization

In most ASICs, the ADC is followed by a digital signal processing (DSP) module for data processing, storage, and communication. The DSP module operates at a fixed sampling rate, but the BF quantizer output, is updated at every beat period, which is directly dependent on the input signal and the VCO frequency. Therefore, the BF quantizer output needs to be resampled with a fixed sampling clock (CK_S). Direct sampling of the BF quantizer output by CK_S [10], [11] can generate errors due to the meta-stability issue arising from DFF setup time violation and the delay mismatch among the BF data paths. In this work, a triple-sampling technique is employed to sample the output correctly at a fixed sampling rate. Fig. 2.18 illustrates the operating principle of

this technique. Incoming data (D_{BF}) is sampled consecutively three times by the three phase shifted versions (CK_1–CK_3) of CK_S [19]. Utilizing three data samples (OUT_1–OUT_3), the decision block can determine whether a data transition is present. For example, OUT_1 will be different from OUT_2 and OUT_3, if the data transition occurs between the rising edges of CK_1 and CK_2. In the absence of data transition, all three samples are equal. Data transition timing conditions and selected correct sample are shown with a timing diagram example in Fig. 2.18.

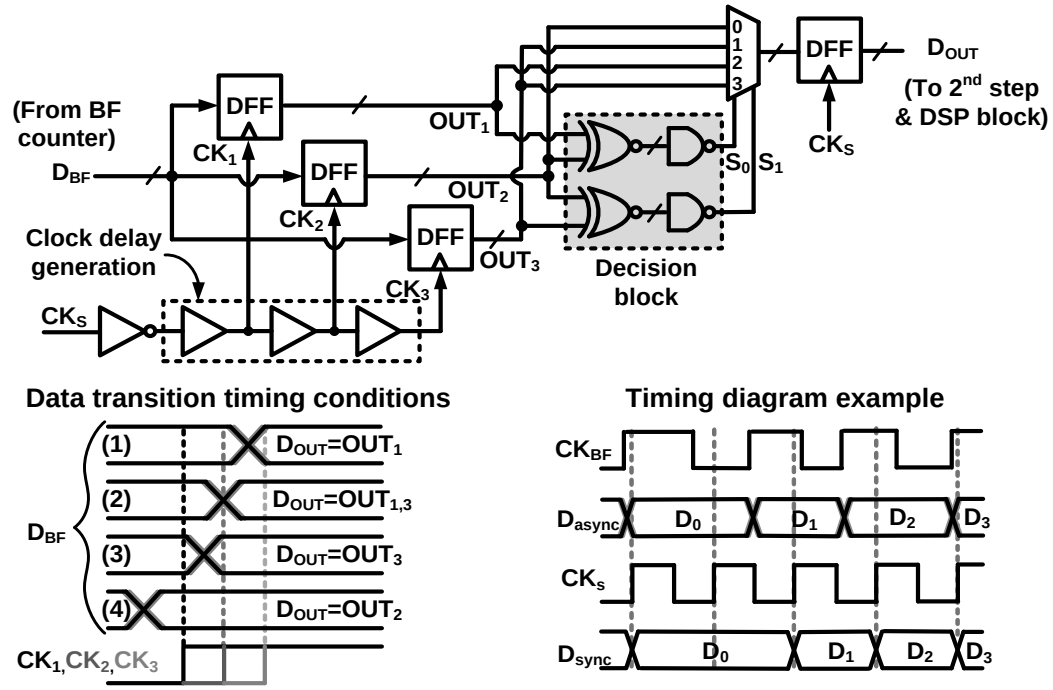


Fig. 2.18: Triple sampling technique is employed to sample the beat frequency data with an external sampling clock without meta-stability issues.

2.6 Circuit Implementation

The complete block diagram of the proposed two-step BF-ADC is described in Fig. 2.19. The differential input pair SIGP and SIGN provides the supply voltage of the two ring oscillators and generates input clocks (CK_{SIGP}, CK_{SIGN}) having frequencies linearly dependent on the input analog voltages. The VCO gain (K_{VCO}) is lower than the one implemented in [10], [11] in order to cover at least 10mVpp input range without degrading the resolution significantly. The input pairs are AC coupled to cancel the dc differential electrode offset. The common-mode voltage (V_{CM}) is adjusted with an external bias signal.

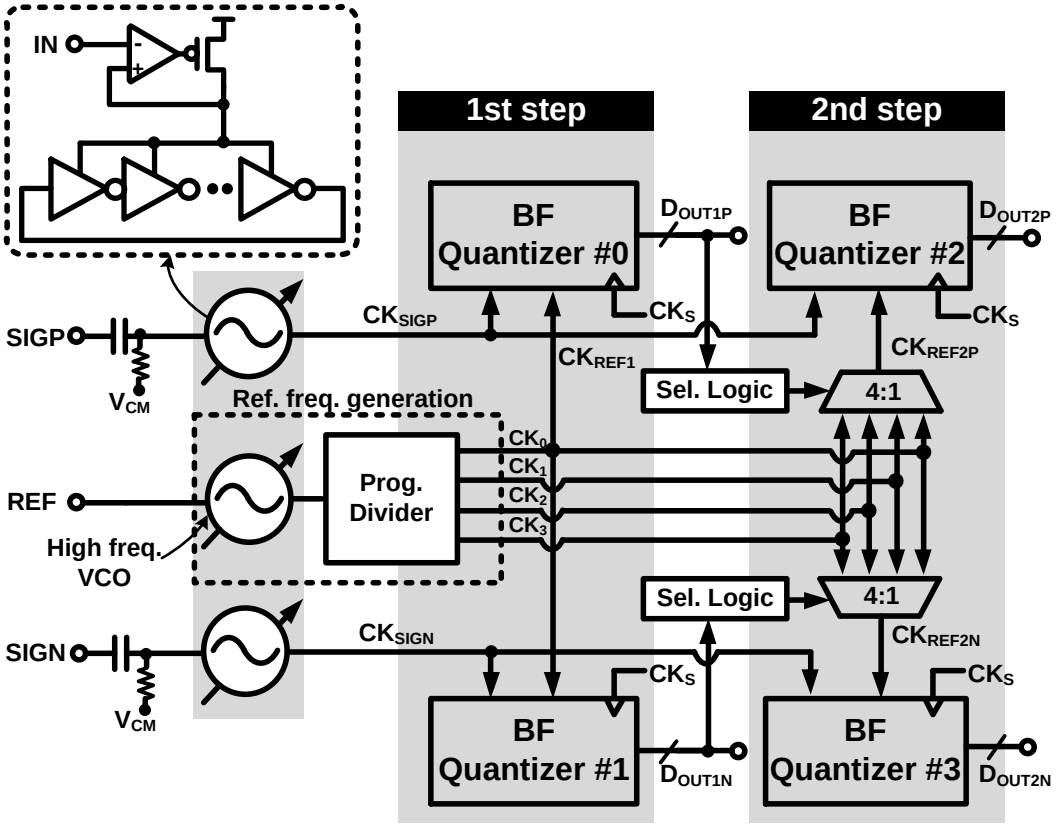


Fig. 2.19: Block diagram of proposed differential two-step beat-frequency ADC.

Multiple reference clocks (CK_0-CK_3) having a fixed frequency difference for the two-step operation can be generated in a number of ways. 1) A phase-locked loop (PLL) with programmable feedback divider where division factor is decided by the first step of ADC operation can be utilized. 2) Multiple voltage reference generated with the help of a low-dropout regulator (LDO) having programmable output voltage and applying it to a VCO can also generate multiple reference frequencies. 3) A high frequency oscillator with a programmable frequency divider is another way to implement this block. Since the primary focus of this work is the ADC implementation, option 3 is selected to avoid the design complexity of a PLL or an LDO, but at the cost of the power consumption of the high frequency VCO. However, a single reference generation block can be shared among multiple channels of the bio-potential ASIC reducing the overhead associated with it. Also worth mentioning is that even with a modest increase in power due to the additional clock generation block, the overall ASIC system complexity and power can be reduced as the AFE circuits can be simplified or even removed. Four reference clocks are generated simultaneously in this implementation and one of them is selected using a 4:1 multiplexer. This helps to share the same reference generation block between each half of the differential second step operation. The frequency difference between two adjacent references is adaptively controlled for different peak-to-peak input swings, by changing the frequency division factor.

BF quantizer #0 and #1 in Fig. 2.19 form the differential first-step while #2 and #3 are used for the second-step of the BF-ADC. The reference clock that has highest frequency i.e. CK_0 is utilized in the first step as the reference (CK_{REF1}). BF counts D_{OUT1P}

and D_{OUT1N} generated from the first step selects the appropriate reference for the second-step (CK_{REF2P}, CK_{REF2N}) using a pair of selection logic and a 4:1 multiplexer. The differential output at the second-stage (D_{OUT2P}, D_{OUT2N}) is the final BF-ADC output.

Each BF quantizer, as illustrated in Fig. 2.20, consists of a DFF to generate the beat frequency clock (CK_{BF}), a 10-bit counter whose output is read and reset by a short-pulse generator in every beat period, and an asynchronous-to-synchronous converter. Resetting the counter using a short pulse after reading the count keeps the VCO always oscillating and thereby, achieves first order quantization noise shaping. As the counter increments at every rising edge of CK_{REF}, read and reset operation must finish before the next rising edge of CK_{REF}. Finally, the output (D_{BF}) is resampled by a triple sampling asynchronous-to-synchronous converter explained in section IV to generate a 10-bit ADC output at a fixed sampling rate.

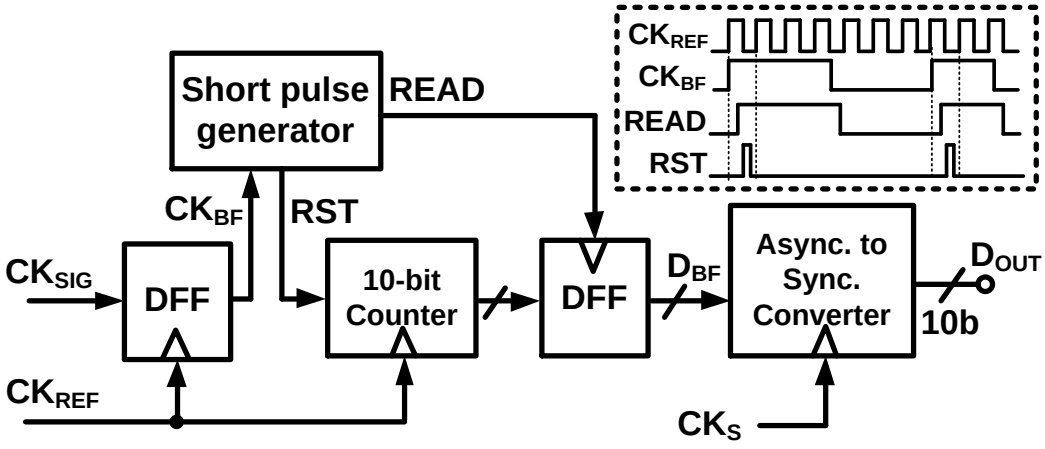


Fig. 2.20: Implementation of each BF quantizer using a short-pulse generator.

2.7 Experimental Results

The proposed two-step BF-ADC was fabricated in a 65nm LP CMOS process. A differential sinusoidal signal of 300Hz, 10mVpp is used as the input of the BF-ADC. Fig. 2.21 shows the VCO frequency-tuning characteristic and the gain, K_{VCO} obtained is 25kHz/mV. As the VCO operating frequency is roughly 11.5MHz and maximum BF count targeted to be 128, minimum beat frequency will be 90kHz. Since the first and second-step operation occur sequentially with the sampling clock, sampling period should be longer than a beat period. This limits the maximum sampling frequency to 90kHz. Keeping some margin for VCO noise and other non-idealities, a 50kHz external clock is employed for sampling. Both the differential first and second step outputs are measured for comparison purposes.

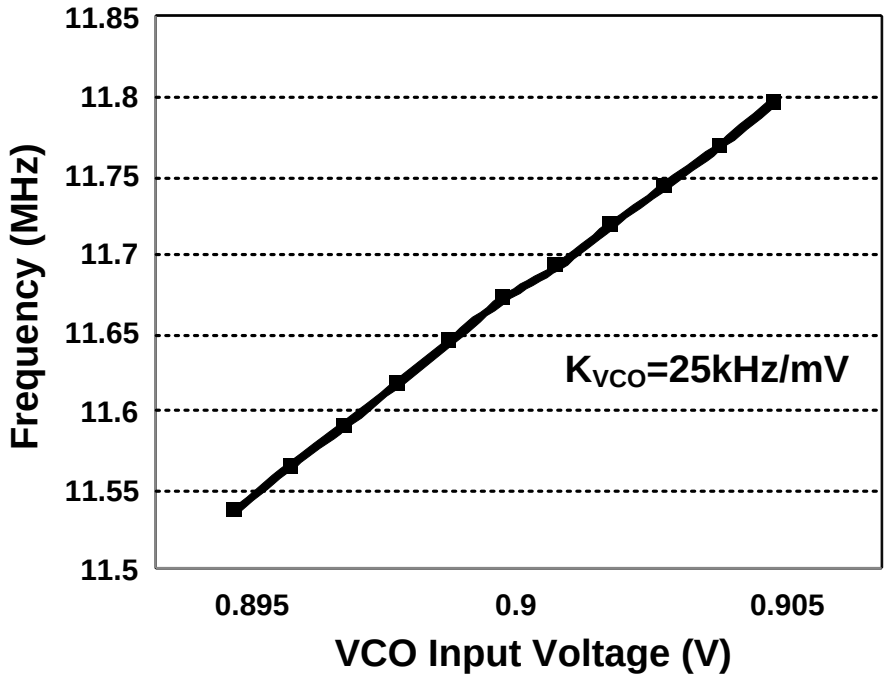


Fig. 2.21: Measured VCO tuning characteristic.

Fig. 2.22 shows the measured BF count and the reconstructed output observed from one side of the differential outputs. The two-step output clearly shows lower quantization noise, especially when the signal level is near its minimum. The 65536-point FFT of the output is plotted in Fig. 2.23. A 10mVpp input is equivalent to -41.5dBFS for a rail-to-rail supply voltage of 1.2V. The signal-to-noise and distortion ratio (SNDR) calculated for a 1.2kHz signal bandwidth is 44.5dB and 38.9dB for the two-step and one-step output, respectively. Quantization noise shaping is not clearly visible here due to the device thermal noise and the low frequency device flicker noise. Measured spur-free dynamic range (SFDR) is 57dB.

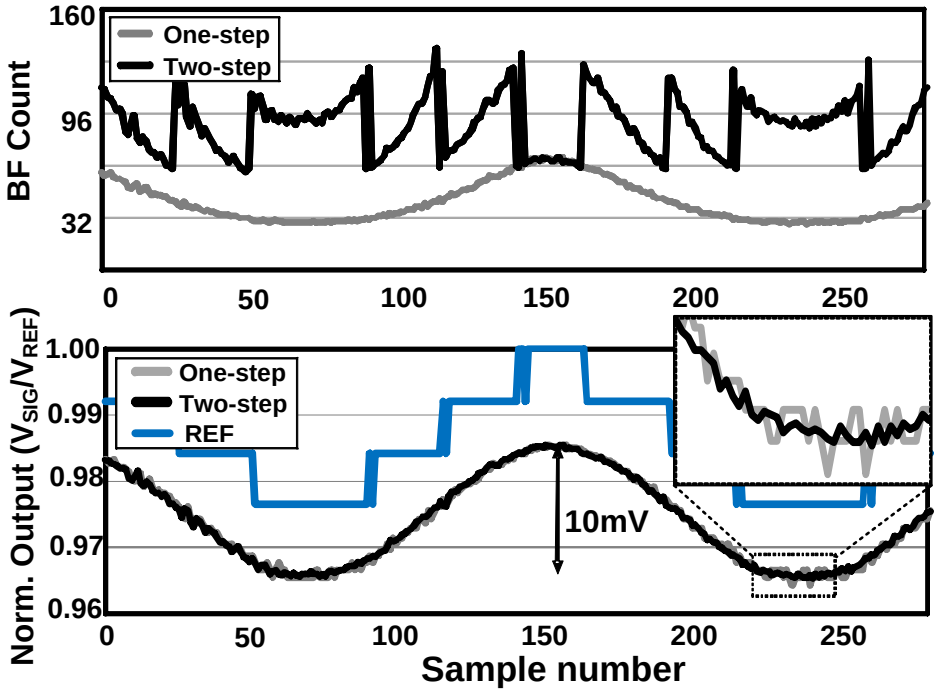


Fig. 2.22: Measured beat frequency count and reconstructed output for a 10mVpp, 300Hz input.

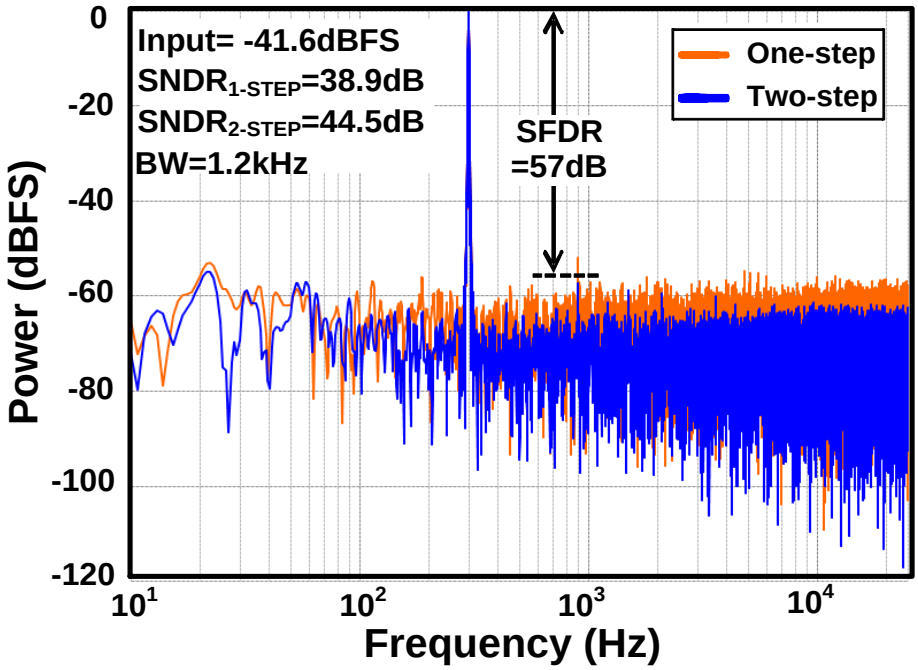
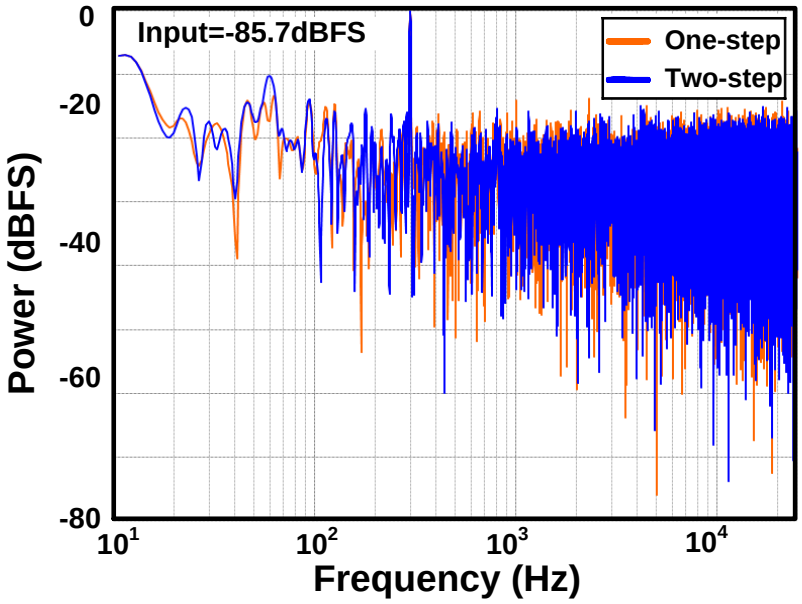
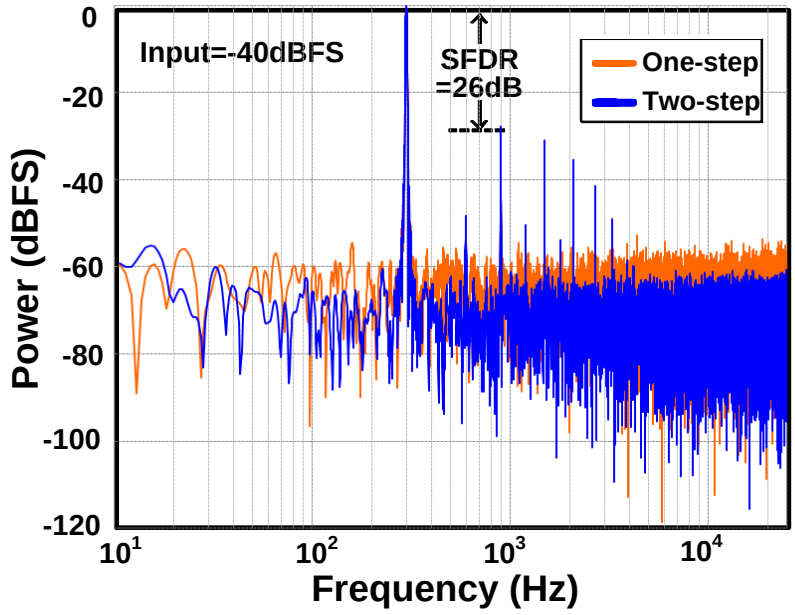


Fig. 2.23: Measured FFT for a 10mVpp (i.e. -41.6dBFS) 300Hz input. The sampling frequency is 50kHz. Measured SNDR is 38.9dB and 44.5dB for one-step and two-step BF-ADC, respectively.

Fig. 2.24 (a) plots the FFT for a 62.5µVpp (=-85.7dBFS) input voltage, which is the minimum detectable signal. For larger input amplitude, as evident from Fig. 2.24 (b), odd harmonics appear at the output due to VCO nonlinearity, degrading both SFDR and SNDR. Therefore, input amplitude should be limited to 12mVpp i.e. -40dBFS achieving a 45.7dB dynamic range. Fig. 2.25 shows the measured SNDR plot by sweeping the input signal amplitude. The maximum BF count in each measurement is kept constant at 128 by adjusting the common-mode voltage (V_{CM}). The proposed two-step technique clearly outperforms the one-step approach for larger signal amplitude (e.g. -60 to -40 dBFS). An ideal linear VCO based ADC having a maximum count of 128 has much lower SNDR when the input amplitude is below -40dBFS.



(a)



(b)

Fig. 2.24: (a) Measured FFT at minimum (62.5µVpp i.e. -85.7dBFS) and (b) maximum (12mVpp i.e. -40dBFS) input signal achieving a 45.7dB dynamic range.

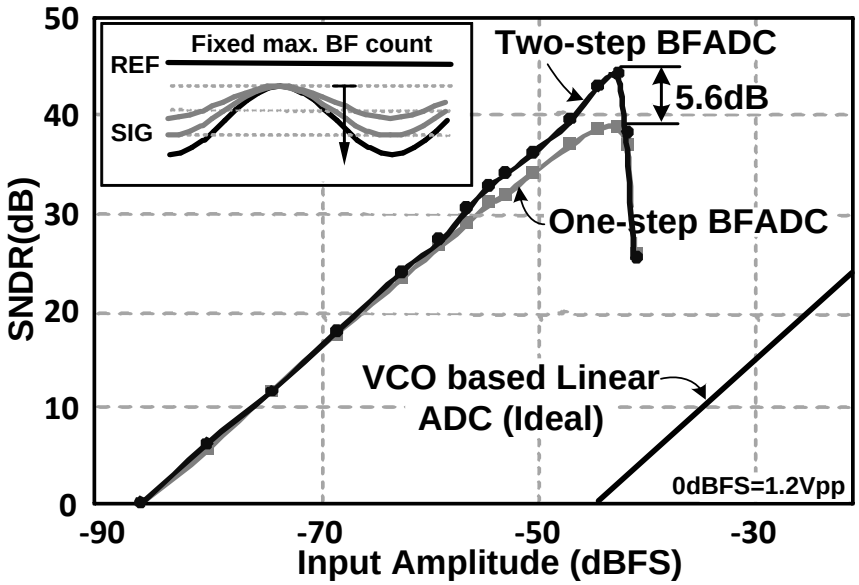


Fig. 2.25: Measured SNDR plot for different signal amplitude for a fixed maximum BF count. An ideal linear ADC has much lower SNDR when the input amplitude is lower than -40dBFS.

The die photo showing an active core area of 0.096mm^2 is shown in Fig. 2.26. The ADC core consumes a 38µW power (without the contribution of the reference frequency generation block) from a 1.2V power supply. The input VCO pair consumes a total power of 30µW while the switching power consumption of each differential BF quantizer step is only 4µW. Fig. 2.27 compares the ADC performance with other state-of-the-art designs for direct conversion of 10mVpp input signal. [10], [11] is not included for this comparison as their operation is limited to only 6mVpp.

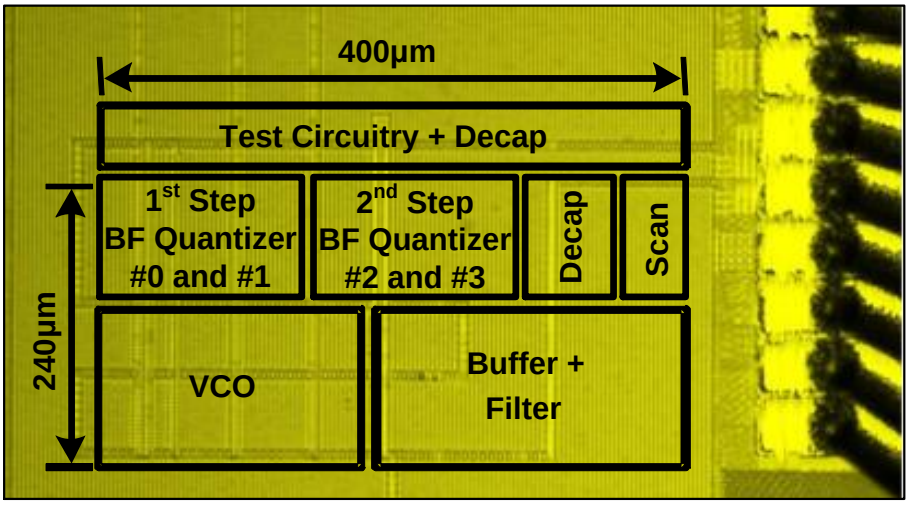


Fig. 2.26: 65nm test chip micrograph.

Parameters	This Work		[6] ESSCIRC'11	[9] VLSI'11	[20] VLSI'12	[21] CICC'14
ADC Type	One- step Beat freq.	Two- step Beat Freq.	CT- ΣΔ	VCO Based	Two-step ΣΔ	PWM Based ΣΔ
Process/Supply	65nm/1.2V		0.18µm/1.4V	90nm/1.15V	0.13µm/1.2V	0.18µm/1.8V
Input freq./BW	300Hz/1.2kHz		21Hz/256Hz	30kHz/8MHz	500kHz/5MHz	221.5kHz/1MHz
Sampling Rate	50kHz		57kHz	640MHz	80MHz	144MHz
IN_{0dB}[dBFS]*	-86		-80	-65	-71	-54
$SNDR_{10mVpp}$**	38.9dB	44.5dB	40dB	20dB	22dB	20dB
$ENOB_{10mVpp}$**	6.17	7.1	6.35	3.03	3.36	3.03
Power	34µW	38µW	13.3µW	4.3mW	8.1mW	2.7mW
FoM_{10mVpp}[pJ/Conv]***	197	115	318	33	79	165.3
Chip area	0.096mm^2		0.51mm^2	0.1mm^2	0.37mm^2	0.0275mm^2

**Input amplitude at SNDR=0dB, **SNDR/ENOB for 10mVpp, ***FoM =* $\frac{Power}{2^{ENOB_{10mVpp}} * 2 * BW}$

Fig. 2.27: Performance comparison.

Chapter 3. Digital Sub-sampling PLL

3.1 Introduction

Digital phase locked loops (DPLLs) [22]-[25] are gaining popularity over traditional analog PLLs as they have favorable scaling properties in advanced CMOS technology nodes. DPLLs can be implemented in a smaller chip area due to the absence of large analog loop filters, and performance improvement techniques such as phase-noise reduction and spur cancellation can be realized in the digital domain. A sub-sampling PLL, first introduced in [26], uses a sub-sampler as the phase detector (PD) that directly samples the sinusoidal output voltage of the voltage controlled oscillator (VCO) without any frequency divider in the feedback path. The PD gain in this case is higher than a conventional phase-frequency detector gain. As a result, in-band phase noise is suppressed significantly. A sub-sampling DPLL was implemented in [27] using a differential latched sense-amplifier as the sub-sampler for binary phase detection. This design however, operates only in an integer-N mode. A divider-less PLL architecture was proposed in [28], but it requires a high-resolution time-to-digital converter (TDC) and a counter instead of the frequency divider.

In this work, a fractional-N sub-sampling DPLL circuit is implemented. The binary or 1-bit sub-sampling phase detector (SSPD) is similar to the one proposed in [27], however, a standard D-flip-flop (DFF) is used here instead of a latched sense-amplifier for ease of implementation. Unlike the analog sub-sampler where the sinusoidal output

voltage of the VCO is directly sampled, the 1-bit SSPD samples the square wave ring oscillator output and generates a binary output of 1 or 0 irrespective of the frequency divider in the PLL feedback path. As a result, the increase in PD gain and its effect in output phase noise in a digital sub-sampling PLL are different from the analog case. Although the explanation of in-band noise reduction in analog sub-sampling PLL is present in existing literatures, the behavior in binary PD based sub-sampling DPLL is not discussed. Therefore, a detailed mathematical analysis with phase noise modeling is performed in this work. Finally, a wide detection range fractional frequency detector is proposed for fractional-N frequency locking. This has lower design complexity and power consumption compared to a TDC based fractional frequency detector [28]. It consists of a glitch-free phase selection block that periodically selects the proper clock phase [22], [29] of a 10-bit digitally controlled ring oscillator (i.e. ring-DCO) and a high-speed edge counter. The designed ring-DCO has a highly linear gain over a wide frequency tuning-range. The remainder of this chapter is organized as follows. Section 3.2 briefly explains the operation of a DFF based sub-sampling DPLL. Section 3.3 discusses the binary PD gain enhancement and in-band noise reduction due to sub-sampling. Circuit implementation details are given in section 3.4, followed by measurement results in section 3.5. Finally, we conclude the chapter in section 3.6.

3.2 Operation of a Digital Sub-sampling PLL

Fig. 3.1 (top) shows the simplified block diagram of a sub-sampling DPLL where a DFF is used as a 1-bit digital sub-sampler. For an N times frequency multiplying DPLL, DFF samples once in every N DCO output (OUT) cycles using a reference clock (REF)

to decide whether the OUT edge is leading or lagging the REF edge and generates an output of 1 or 0 respectively. The phase tracking behavior is explained in Fig. 3.1 (bottom) for N=3. If the k^{th} rising edge of OUT lags the reference edge, DFF samples a 0 at the output (e[k]), increasing the DLF code (d[k]). This increases the DCO frequency to reduce the phase error between OUT and REF. Similarly, when OUT leads REF, DFF samples a 1, reducing d[k] to delay the OUT edge. Under locked condition, OUT edge wanders around the REF edge, toggling e[k] in every reference cycle to generate a time average output i.e. <e[k]>=1/2. The example shown here is under the assumption that there is no random noise in the system. Since DFF simply ignores (N-1) OUT edges in every reference cycles, generating a binary output, loop dynamics doesn't change with or without frequency divider in the feedback path. However, thermal noise of the divider impacts the phase detector gain, which is described in section III.

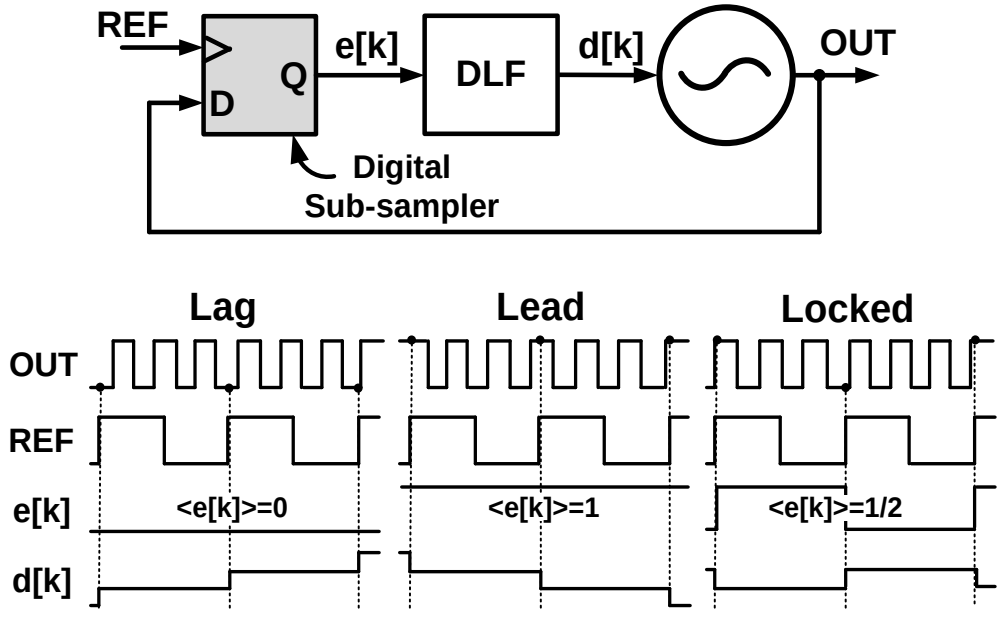


Fig. 3.1: Digital sub-sampling PLL block diagram and waveforms for the late, early and locked state phase detection by the digital sub-sampler (N=3).

3.3 In-band Phase-noise Reduction in Binary PD based Sub-sampling DPLL

In-band phase noise at the output of a DPLL is mainly contributed by two noise sources: PD quantization noise and feedback divider noise. Therefore, the absence of a feedback divider in the sub-sampling DPLL directly reduces in-band noise. At the same time, it also enhances the binary PD gain indirectly. Fig. 3.2 explains how the absence of a feedback divider increases the binary PD gain. Ideally, a binary PD gain is infinite as it detects which one of its two input signals (i.e. the feedback and the reference) leads or lags the other one. But the feedback divider's white thermal noise and the high pass filtered noise coming from the DCO dithers the feedback clock (DIV) that appears at the PD input. As a result, a linearized model similar to a linear multi-bit TDC can be established for the binary PD. If the k^{th} rising edge of DIV leads the reference clock (REF), the time error $\Delta t[k]$ will be positive and PD output will be e[k]=1. But the random noise can move the rising edge of DIV and make e[k]=0. $P_{\Delta t}$ is the Gaussian jitter distribution with an RMS value $\sigma_{\Delta t}$, referred to DIV. The time average of e[k] i.e. <e[k]> is written as:

$$< e[k] > \propto \int_{-\infty}^{+\Delta t} P_{\Delta t} dt \tag{3.1}$$

The characteristic of <e[k]> can be approximated with a linear gain K_{pd} around $\Delta t[k]=0$ with input range $2\sigma_{\Delta t}$ and the PD gain, as mentioned in [30], is:

$$K_{pd} = \frac{d<e[k]>}{d\Delta t[k]} = \frac{\sqrt{2}}{\sigma_{\Delta t}\sqrt{\pi}} \tag{3.2}$$

It is evident from equation (3.2) that K_{pd} is inversely proportional to $\sigma_{\Delta t}$. Therefore, the absence of feedback divider noise in a sub-sampling DPLL reduces $\sigma_{\Delta t}$ of the jitter distribution, increasing K_{pd}.

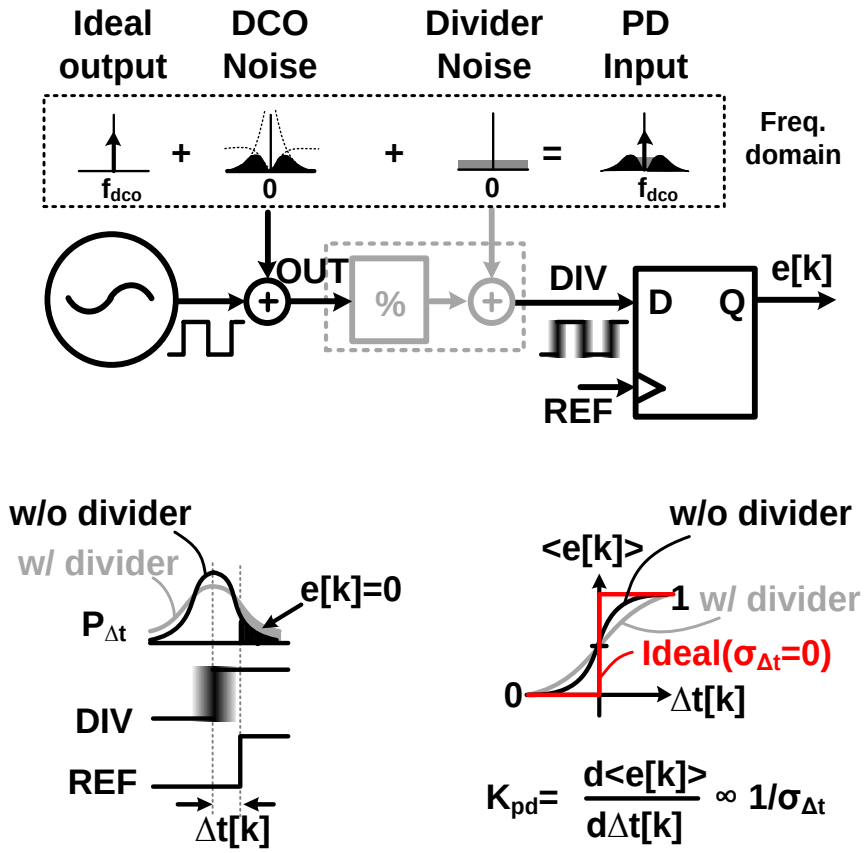


Fig. 3.2: Binary PD gain with and without feedback divider.

Now the impact of PD gain and quantization noise on the sub-sampling DPLL output can be derived from the noise model in [31]. In analog sub-sampling PLL, PD gain directly depends on the slew-rate of the sinusoidal VCO output. Therefore, the absence of the feedback divider increases the PD gain by a factor of N and this property is incorporated in the PLL model by introducing a virtual frequency multiplier in the

reference path instead of a feedback divider [26]. However, in a digital sub-sampling PLL, as the ring-DCO output is a square wave and PD generates binary output of 1 or 0, loop dynamics doesn't change with the absence of the feedback divider. As a result, a virtual frequency divider in the feedback path will still be present in the model as shown in Fig. 3.3.

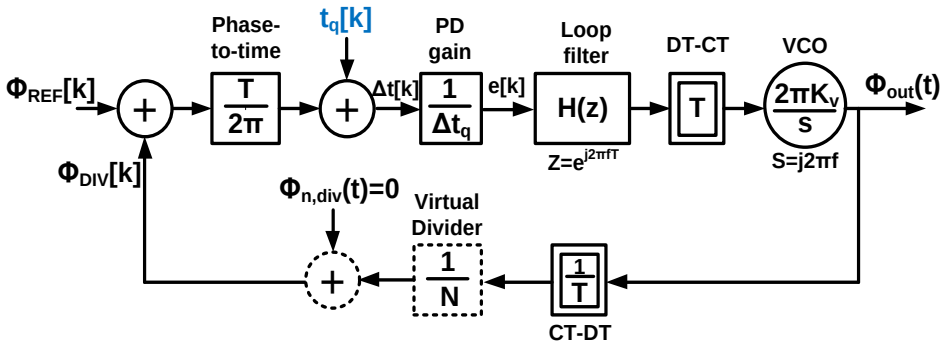


Fig. 3.3: Binary PD gain with and without feedback divider.

A linear TDC based PD of time resolution Δt_q has a gain $K_{pd}=1/\Delta t_q$, because the output code changes by 1 LSB for an input time change of Δt_q. The binary PD can be modeled as a linear TDC with resolution $\Delta t_q = \sqrt{(\pi/2)}\sigma_{\Delta t}$ (equation (3.2)). For a reference clock period T, a VCO gain K_V and a frequency division of N, the PD to output close-loop PLL transfer function is:

$$\frac{\phi_{out}}{t_q} = \frac{\frac{1}{\Delta t_q}H(e^{j2\pi fT})\frac{K_V T}{jf}}{1+\frac{1}{\Delta t_q}H(e^{j2\pi fT})\frac{K_V T}{j2\pi fN}} = \frac{2\pi NA(f)}{1+A(f)} = 2\pi NG(f) \qquad (3.3)$$

A(f) and G(f)=A(f)/(1+A(f)) are the open-loop transfer function and closed-loop parameterizing transfer function, respectively. So G(f)≈1 at low frequencies.

Since the phase noise is expressed as the ratio between signal-to-noise power spectral densities, a time error Δt_q in the PD introduces an equivalent quantization noise of $\Delta t_q/T$. For a uniform random distribution, the PD quantization noise becomes:

$$N_q = \frac{(\Delta t_q/T)^2}{12} = \frac{1}{12}\left(\frac{1}{K_{pd}T}\right)^2 \tag{3.4}$$

N_q is uniformly distributed across the frequency band from 0 to 1/T. So the PD noise power spectral density is:

$$S_q(f) = \frac{N_q}{1/T} = \frac{1}{12T}\left(\frac{1}{{K_{pd}}^2}\right) \tag{3.5}$$

Therefore, the DPLL output phase noise due to PD quantization noise is given as:

$$S_{PD,\phi_{out}}(f) = |2\pi NG(f)|^2 S_q(f) = \frac{1}{12T}\left|\frac{2\pi NG(f)}{K_{pd}}\right|^2 \tag{3.6}$$

From equations (3.5) and (3.6), it is clear that the effect of PD quantization noise on the DPLL output will reduce with the increase in K_{pd}.

Similar to equation (3.3), the divider to output transfer function is NTG(f). For the divider noise power spectral density of $S_{div}(f)$, the output phase noise of the divider is:

$$S_{div,\phi_{out}}(f) = |NTG(f)|^2 S_{div}(f) \tag{3.7}$$

Fig. 3.4 (left) explains the impact of PD quantization noise and divider noise on the PLL output phase noise. Using equation (3.6) and (3.7), the expression for total in-band phase-noise reduction due to sub-sampling is derived as:

$$\Delta PN|_{dB} = 10\log_{10}\left(\frac{S_{PD,\phi_{out}}(f)|_{w/\ div} + S_{div,\phi_{out}}(f)}{S_{PD,\phi_{out}}(f)|_{w/o\ div}}\right) \tag{3.8}$$

Equation (3.8) can be further simplified as:

$$\Delta PN|_{dB} = 20\log_{10}\left(\frac{\sigma_{\Delta t}\ w/\ div}{\sigma_{\Delta t}\ w/o\ div}\right) + PN_{div}|_{dB} \quad (3.9)$$

$PN_{div}|_{dB}$ is calculated from the difference in the output phase-noise, expressed in dB, with and without taking $S_{div,\phi out}(f)$ into consideration. Noise contribution of other sources such as input reference, DCO quantization etc. will appear in both the numerator and denominator of equation (3.8), modifying $PN_{div}|_{dB}$ factor of equation (3.9). Here one thing to remember is that the above analysis is valid only under the assumption that the binary PD is linear. A very high K_{pd} i.e. low $\sigma_{\Delta t}$ makes the PD nonlinear, which again translates into the limit cycle spur at the PLL output. Interestingly, the ring VCO in this implementation ensures good linearity of the binary PD due to their inferior noise performance compared to an LC VCO.

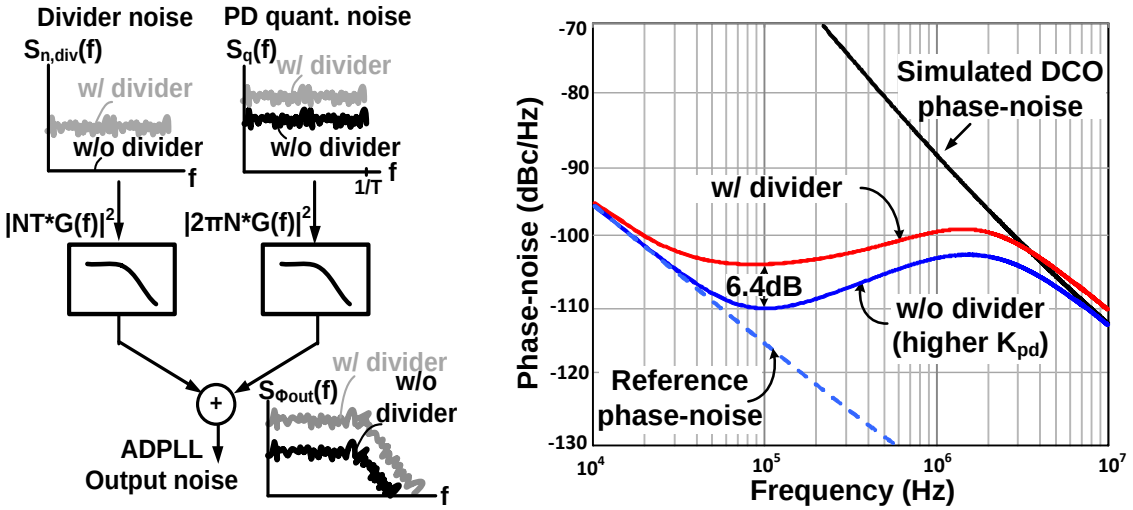


Fig. 3.4: Effect of PD quantization noise and divider noise on PLL output simulated in Matlab.

To confirm our analysis, noise simulations are performed in Matlab at 1.6GHz and N=16 using the PLL model explained above. Design parameters such as K_V and H(z) are

obtained from the circuit implementation. First, simulated phase noise of the DCO and the divider is incorporated into the PLL model to estimate the output integrated RMS jitter ($\sigma_{\Delta t}$), which will be used for K_{pd} calculation. Multiple iterations are required to match the $\sigma_{\Delta t}$ used in K_{pd} with the one obtained by integrating output phase noise. This results in $\sigma_{\Delta t}$=3ps. Then close loop phase noise is obtained without the noise contribution of the feedback divider and $\sigma_{\Delta t}$ obtained is 2.4ps. Finally, simulation with $\sigma_{\Delta t}$=2.4ps (i.e higher K_{pd}) is performed. Fig. 3.4 plots the phase noise of the DCO, output referred reference noise and the close loop PLL noise for both with and without divider. The sub-sampling PLL shows 6.4dB lower phase noise at 100kHz offset. From equation (3.9), the increased K_{pd} due to reduction of $\sigma_{\Delta t}$ from 3ps to 2.4ps reduces the in-band noise by 2dB. The additional 4.4dB reduction is due to the absence of feedback divider noise ($PN_{div}|_{dB}$). However, it is noted that the noise of the power supply, output buffers etc. will add during actual measurement degrading this noise difference and increasing $\sigma_{\Delta t}$.

3.4 Circuit Description of Proposed DPLL

Fig. 3.5 shows the block diagram of the proposed fractional-N DPLL circuit. As the 1-bit SSPD only detects phase difference, a separate frequency-locking path, which consists of a fractional frequency detector and an integrator, is used to set the operating frequency of the PLL. INT<7:0> and FRAC<1:0> set the integer and fractional portions of the frequency multiplication factor, respectively. A 5:1 MUX periodically selects 1 of 5 DCO phases to generate fractional N at the multiples of 1/5. Glitches at the MUX output during phase selection create error in the frequency detection. This is taken care of by the MUX selection logic.

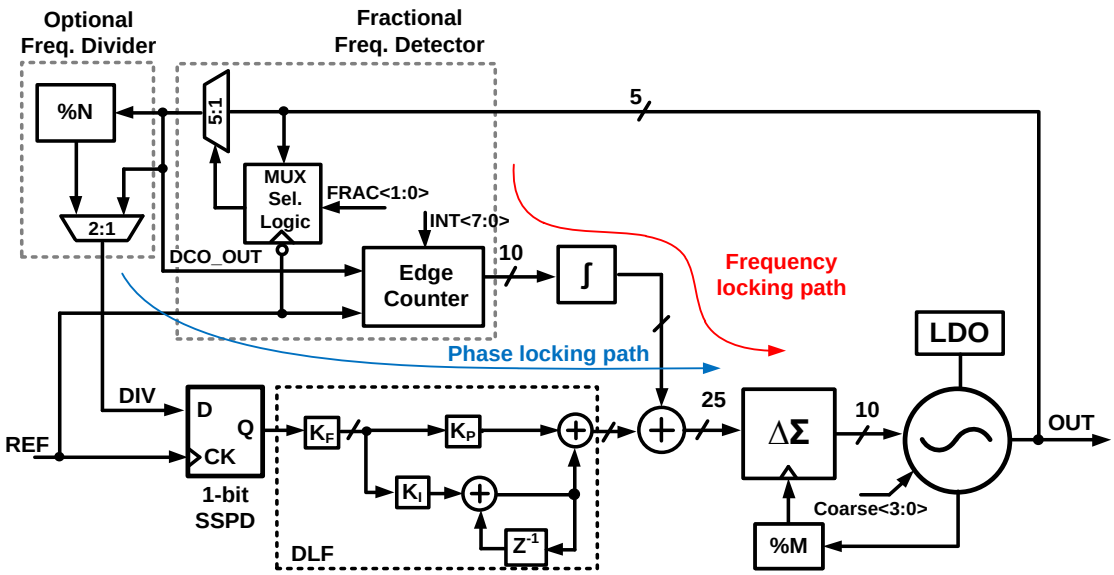


Fig. 3.5: Block diagram of the proposed fractional-N DPLL.

Once the frequency is locked, frequency-locking path is turned off and the phase locking path becomes active. The phase locking path consists of a DFF that acts as a digital sub-sampler, a digital loop filter (DLF) and a ΔΣ-modulator (DSM). The DLF consists of a proportional path and an integral path of gain K_P and K_I, respectively. Gains are easily programmable to ensure stability and optimum performance over wide operating frequencies. A DSM at the input of the DCO reduces its quantization noise. An optional frequency divider can be enabled to operate the PLL in the conventional mode allowing the performance comparison with the sub-sampling mode. Due to the periodic nature of DCO phase selection; there will be spurs in the PLL output at the multiples of $f_{REF}/5$, which is sufficiently higher than the PLL bandwidth and automatically suppressed by the loop without the requirement of any DSM for phase selection. Since a 100MHz clock is used as reference, frequency resolution i.e. the minimum frequency step at the

output is 20MHz. For better resolution, we need more clock phases, which can be generated by increasing the number of inverter stages in the ring oscillator and using the phase interpolator. However, low frequency fractional spur could be an issue in that case, requiring a DSM to randomize the DCO phase selection.

The details of the frequency detector and the ring-DCO are explained below.

3.4.1. *Fractional Frequency Detector*

Conventionally, fractional frequency detection in divider-less PLLs is performed using a counter for the integer part and a high resolution TDC for the fractional part [28]. This increases the circuit complexity and power consumption. In our implementation, we have a very wide detection range edge counter [32] based fractional frequency detector that counts the number of rising edges of DCO in a given reference period. This edge counter consists of a full-adder based high-speed synchronous counter that increment at every DCO edge (shown in Fig. 3.6). Count values of two consecutive reference cycles are stored in two 8-bit registers and subtracted to get the number of DCO edges (DCO_OUT) in one reference period. Finally, this value is compared with INT<7:0>. FRAC<1:0> generates different fractional values (F) by changing the order of the DCO phase selection. Glitches in DCO_OUT during phase switching change the count value. Therefore a 'MUX Selection Logic' performs the glitch-free phase selection. As shown in the example of Fig. 3.6, phase transition from DCO<0> to DCO<1> must happen after the rising edge of DCO<1> and before the falling edge of DCO<0> to make it glitch free. Hence SEL is sampled by the DCO<1> rising edge, which is generated by another 5:1 MUX.

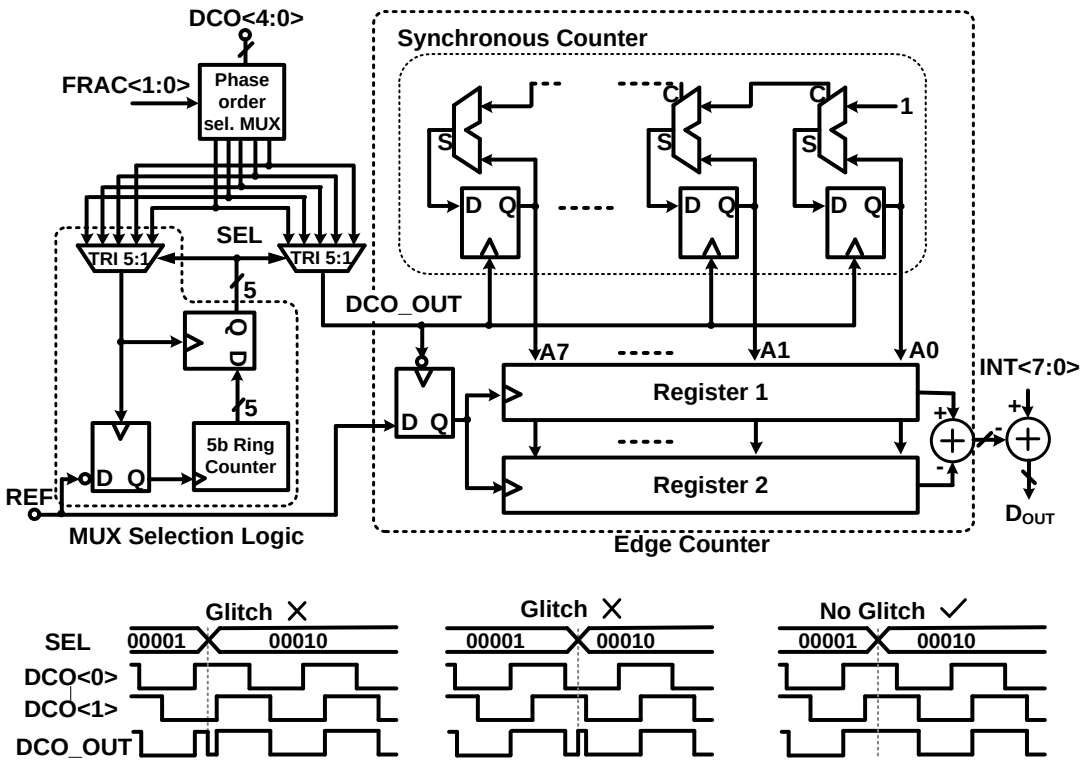


Fig. 3.6: Fractional frequency detector implementation and the timing for glitch free periodic phase selection achieved by MUX selection logic.

3.4.2. *5-stage Ring DCO*

Fig. 3.7 shows the implementation of a 5-stage ring oscillator. Each stage consists of 16 parallel tri-state inverters enabled by the coarse tuning codes to achieve wide tuning range. A fine frequency resolution is obtained by using drain junction of a minimum sized PMOS as a unit switched-capacitor element [33]. 1024 such elements, controlled by 10-bit fine-tuning codes, are then distributed and connected to the internal nodes of the 5-stage ring-oscillator such that load remains balanced at each stage to achieve a linear DCO gain. Layout is also made completely symmetric to reduce parasitic mismatches.

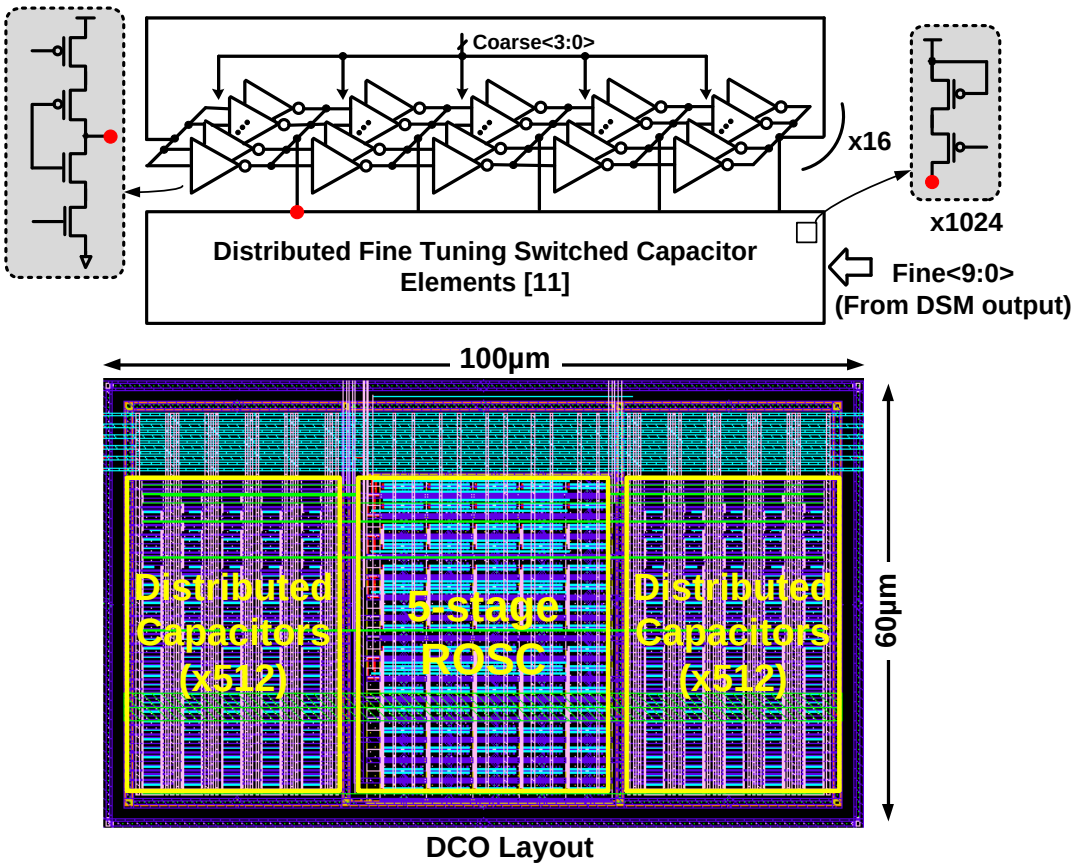


Fig. 3.7: 10-bit ring-DCO circuit with distributed capacitor and layout with balanced loading at each inverter stages.

An on-chip low dropout regulator (LDO) is designed for powering the DCO to minimize the supply sensitivity of the PLL. A higher LDO bandwidth is essential for better supply noise rejection. Fig. 3.8 shows the simulated output spectrum with a 20mVpp, 10MHz sinusoidal supply noise.

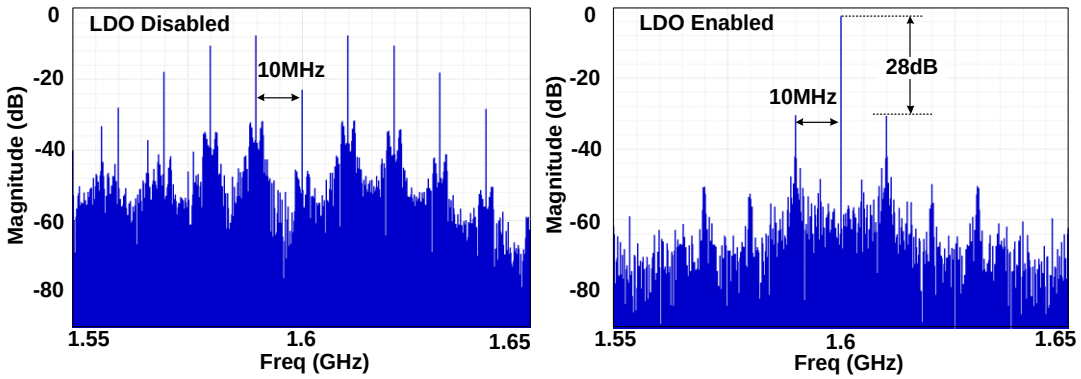


Fig. 3.8: Simulated PLL output spectrum for a 20mVpp 10MHz supply noise.

3.5 Measurement Results

A test chip of the proposed sub-sampling DPLL was implemented in a 1.2V, 65nm CMOS technology to demonstrate in-band phase noise reduction. Fig. 3.9 shows the measured output power spectrum of both the conventional and the sub-sampling DPLL in integer-N (N=16) mode operation at 1.6GHz.

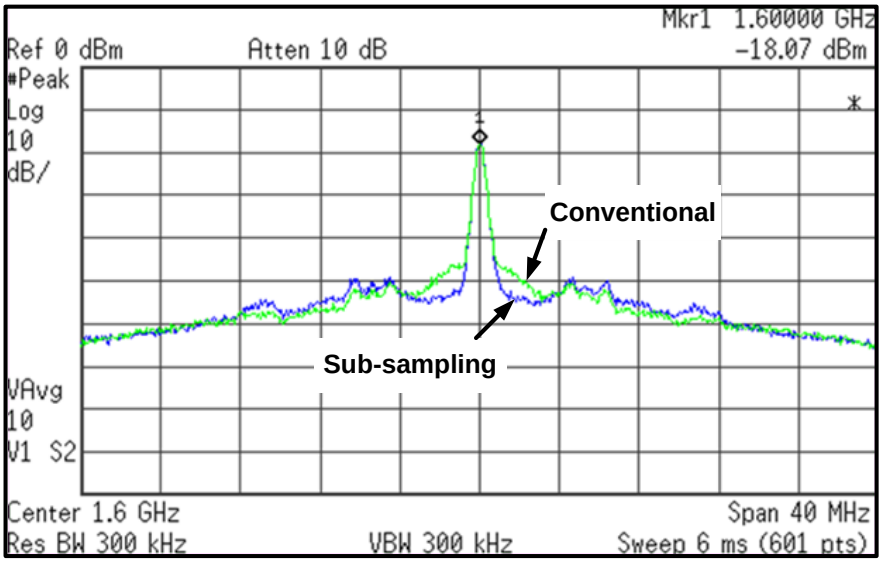


Fig. 3.9: Measured integer-N mode output spectrum (f_{out}=1.6GHz, N=16).

Output power spectrum in fractional-N mode for N=16.2 is shown in Fig. 3.10. As expected, the fractional spurs at $f_{in}/5$=20MHz is suppressed (36dB lower than carrier) by the PLL loop.

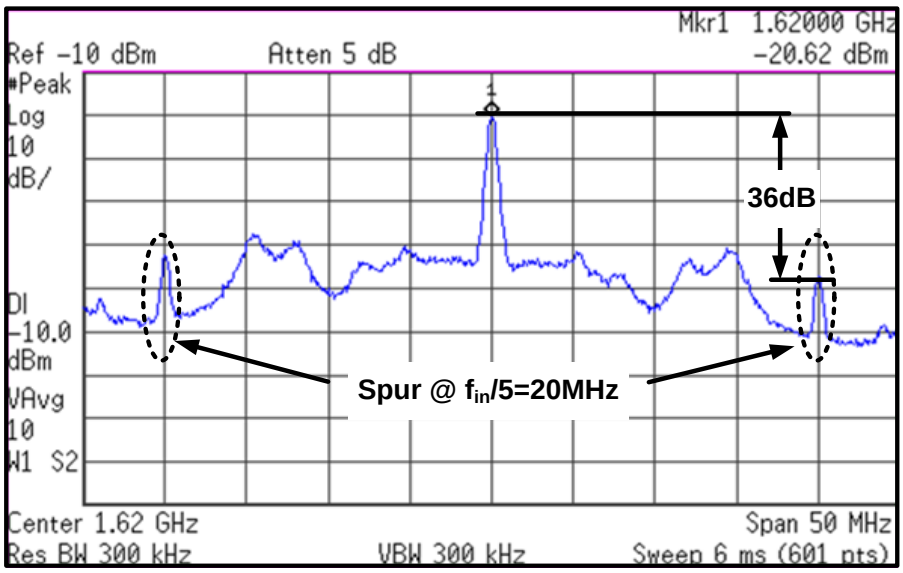


Fig. 3.10: Measured output spectrum in fractional-N mode (f_{out}=1.62GHz, N=16.2) showing fractional spur at fin/5.

Fig. 3.11 plots the measured phase noise. In-band noise of the sub-sampling DPLL is -97dBc/Hz and -95dBc/Hz at 100kHz offset in integer-N and fractional-N mode respectively. These values are about 5dB lower than the conventional PLL mode operation.

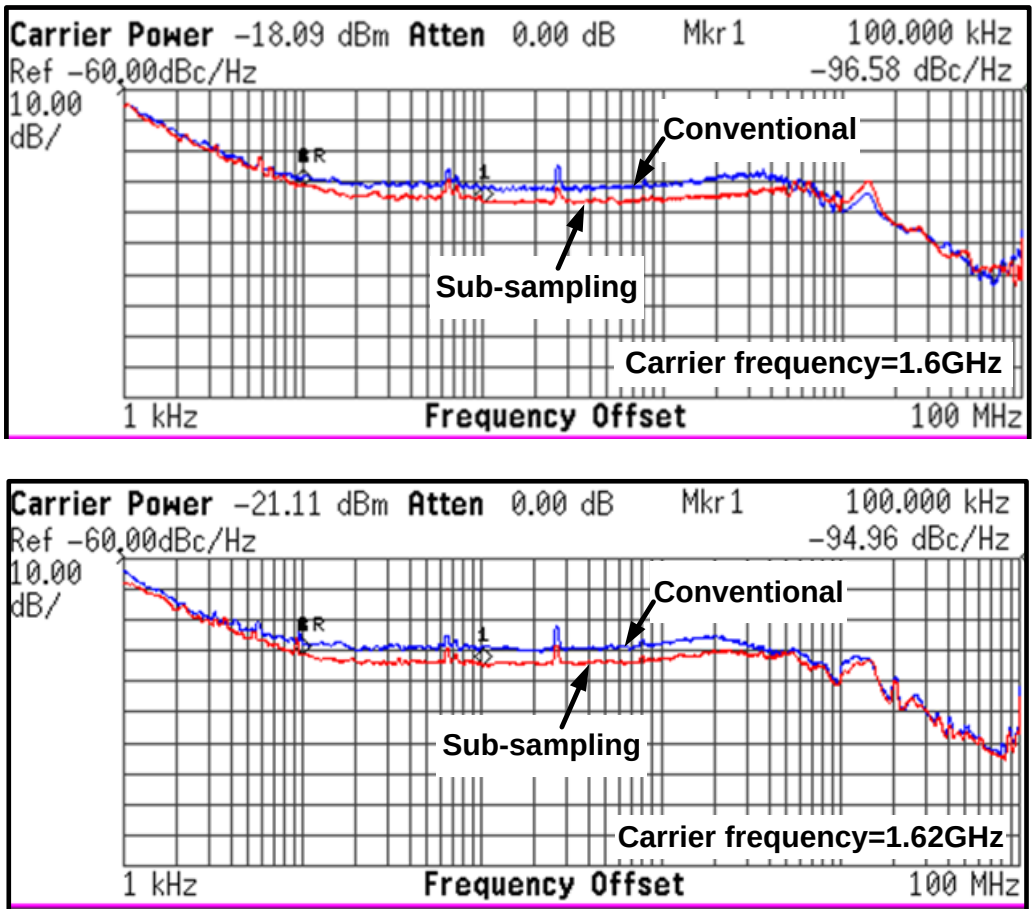


Fig. 3.11: Phase noise plot in integer-N (top) and fractional-N mode (bottom).

Integrated RMS jitters are calculated over 10kHz to 10MHz bandwidth for all different fractional values and the results are plotted in Fig. 3.12. The chip micrograph with a performance summary table is shown in Fig. 3.13. Total chip area including decoupling capacitors, LDO, and test circuitry is 0.073mm^2 while DPLL core is only 0.037mm^2. Total power consumption is 5.5mW from a 1.2V supply at 1.6GHz, of which DCO consumes 4.8mW. Normalized in-band phase-noise and figure-of-merit considering jitter and total power [34] are -201 dBc/Hz^2 and -215.5 dB, respectively.

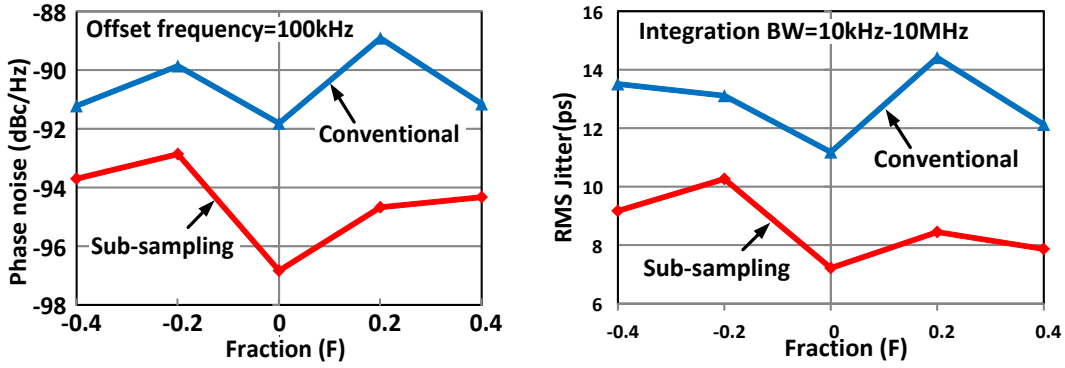
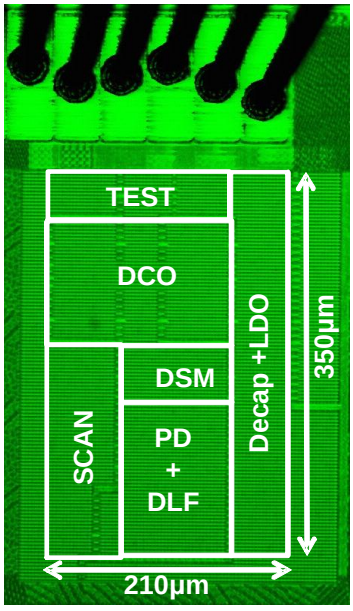


Fig. 3.12: Phase noise and RMS jitter for different fractional value (N=16+F).



		Sub - sampling	Conventional
Technology		CMOS 65nm	
Output freq.		1.6 GHz	
Ref. freq.		100MHz	
PLL Type		Fractional-N	
DCO Type		5 stage ring oscillator	
In- band PN(dBc /Hz)		-97@100kHz	-92@100kHz
*Normalized in - band PN(dBc /Hz^2)		-201@100kHz	-196@100kHz
Integrated RMS Jitter (10kHz – 10MHz)		7.2ps	11.2ps
Power	DCO	4.8mW	
	Total	5.5mW	5.7mW
**FOM (dB)		- 215.5	- 211.5
Total chip area		350µmX210µm	

*$L_{norm}=L_{in\_band} - 10\log(f_{ref}N^2)$ **FOM=20log(σ/1s)+10log(P/1mW)

Fig. 3.13: Chip micrograph and result summary.

Fig. 3.14 compares the performance of this work with other state-of-the-art ring DPLL designs. FoM is improved by at least 5.5dB compared to other designs.

	This work	ISSCC'10 [22]	ISSCC'12 [23]	ISSCC'13 [24]	ISSCC'14 [25]
Technology	65nm	65nm	32nm	28nm	20nm
Output freq.	1.6GHz	0.4GHz	1.5GHz	0.96GHz	1.23GHz
Ref. freq.	100MHz	26MHz	26MHz	30MHz	25MHz
In-band PN (dBc/Hz)	-97	-93	-89	-92	-86
Norm. in-band PN(dBc/Hz^2)	-201	-191	-198	-197	-193
RMS Jitter* (10kHz-10MHz)	7.2ps	17ps	20ps	16ps	30ps
Power (mW)	5.5	3.2	2.5	5.3	2.4
FOM (dB)	-215.5	-210	-210	-208.5	-206
Area(mm^2)	0.037	0.027	0.012	0.026	0.012

*Calculated from phase-noise plot

Fig. 3.14: Chip micrograph and result summary.

3.6 Conclusion

A 0.4-1.6GHz fractional-N DPLL circuit is implemented in 65nm CMOS technology. In-band phase-noise reduction mechanism in binary PD based sub-sampling DPLL is explained and verified with the Matlab noise model simulations results. An edge counter based fractional frequency detection circuitry is proposed to lock the operating frequency of the PLL precisely. A 10-bit distributed fine-tuning switched capacitor based ring-DCO is used to achieve a linear DCO gain over wide tuning range. Finally, the performance is verified with the measurement results.

Chapter 4. Digital MDLL with In-situ Offset Measurement

4.1 Introduction

The design of highly digital phase-locked loops (DPLL) architectures [24, 25, 30, 33] is gaining traction in nanoscale CMOS processes by obviating the need for an area consuming analog loop filter and circumventing the voltage headroom issue of the charge-pump. Other benefits of the digital implementation include immunity to process, voltage and temperature (PVT) variations, easier portability to technology migration, and flexibility in performance optimization by reconfiguring the loop parameters. A classical digital implementation replaces the phase-frequency detector (PFD) and the charge-pump (CP) present in an analog PLL with a time-to-digital converter (TDC). The digital loop filter (DLF), on the contrary to an analog one, can be realized in a compact area and the loop parameters can easily be tuned for a wide operating condition.

However, the fundamental limitation of any PLL to achieve low phase-noise or jitter is the loop bandwidth, which cannot exceed $1/10^{th}$ of the reference clock frequency in order to satisfy the discrete-time stability limit, also known as Gardner's criteria. As the noise of the voltage-controlled oscillator (VCO) is high-pass filtered by the PLL loop, this sets a limit on the maximum VCO phase noise suppression at the PLL output. To overcome this drawback, the multiplying delay locked loop (MDLL) was introduced

recently as an alternative [35] – [38]. Fig. 4.1 shows a simplified block diagram of an MDLL. The multiplexer in the VCO replaces the output edge (OUT) with the clean reference edge (REF) when the multiplexer selection (SEL) goes high. This periodic replacement of OUT with REF prevents the jitter accumulation over multiple reference cycles and suppresses the VCO phase-noise beyond the PLL bandwidth, as illustrated in Fig. 4.1 (right).

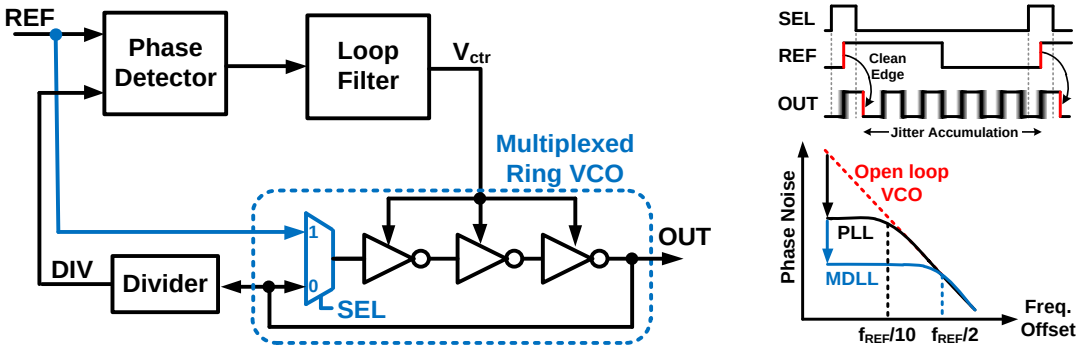


Fig. 4.1: Block diagram of MDLL circuit. VCO phases are periodically replaced by the clean reference clock phase. This prevents the VCO jitter from accumulating over multiple reference cycles, suppressing VCO phase-noise with frequencies beyond the PLL bandwidth.

In spite of superior noise performance, one major drawback of an MDLL is the reference spur that is generated at the output due to the static phase offset (SPO) between the REF and the OUT edge. This SPO is difficult to cancel precisely due to the inherent offset associated with any digital phase detector (PD) or TDC. The circuit technique employed in [38] uses a sampling phase detector and different analog voltage offset cancellation schemes e.g. auto-zeroing, chopper stabilization etc. to minimize SPO. However, these sophisticated analog design techniques are limited to analog PLLs only, and may not be reliable in advanced technology nodes under large PVT variations and

leakage. The reference spur cancellation technique proposed in [35] relies on correlated double sampling, but it requires a high resolution and high linearity gated ring oscillator (GRO) based TDC that increases the design complexity and the power consumption.

Another limitation in all previous implementations was that the SPO is measured off-chip from the spur at the output frequency spectrum using a dedicated high frequency measurement set up, such as, high frequency probes or packages, off-chip drivers (OCD), connectors and spectrum analyzer. Each of these components introduces some inaccuracy in the measurement. Moreover, the measured spur in frequency domain needs to be converted to the time domain to estimate the SPO present in the circuit.

In this work [39], we propose a fractional-N digital MDLL with a reference spur cancellation loop that precisely aligns the REF and the DCO edge utilizing a digital-to-time converter (DTC) and a zero-offset aperture phase detector (APD). An in-situ offset detection circuit is also employed to measure the phase offset in time domain accurately without relying on high-speed off-chip measurements. Furthermore, we have derived a mathematical expression to calculate reference spur generated at the output spectrum for a given SPO. Calculation is performed for a wide variation of SPO. Fractional frequency multiplication is achieved by periodic phase rotation of multiple DCO phases, which is similar to the injection locking technique proposed in [40], but the subsampling method is utilized for in-band phase noise reduction while reducing the power consumption.

The rest of this chapter is organized as follows. Section 4.2 describes the reference spur issue in an MDLL and the mathematical details for calculating reference spur generated from SPO. The proposed reference spur cancellation technique and the in-situ

offset detection circuit are explained in Section 4.3 and 4.4 respectively. Circuit implementation details of the MDLL are described in section 4.5, followed by measurement results in section 4.6. Finally, section 4.7 concludes the work.

4.2 Reference spur issue in MDLL

While providing superior phase noise performance compared to a traditional PLL, an MDLL suffers from the reference spur issue due to the SPO between the injected reference edge and the DCO edge. As explained in Fig. 4.2, one of the contributors of this offset in bang-bang phase detector (BBPD) based digital MDLLs [36] is the set up time of the D flip flop (ΔT_1) used for phase comparison. The delay of the frequency divider (ΔT_2) in the feedback path increases this offset further. As a result, a fixed offset (ΔT) is generated between the reference and the DCO edge under phase locked condition. In MDLL operation, when reference is inserted into the ring oscillator path, it modulates the DCO period to $T+\Delta T$ instantaneously, creating a deterministic jitter of ΔT (T is the output period when there is no SPO). This behavior repeats in every reference cycle. This additional ΔT in one clock cycle is compensated by the next N-1 cycles, assuming a frequency-multiplication factor of N. ΔT can be significantly large, depending on the operating frequency and the circuit implementation, severely degrading the performance.

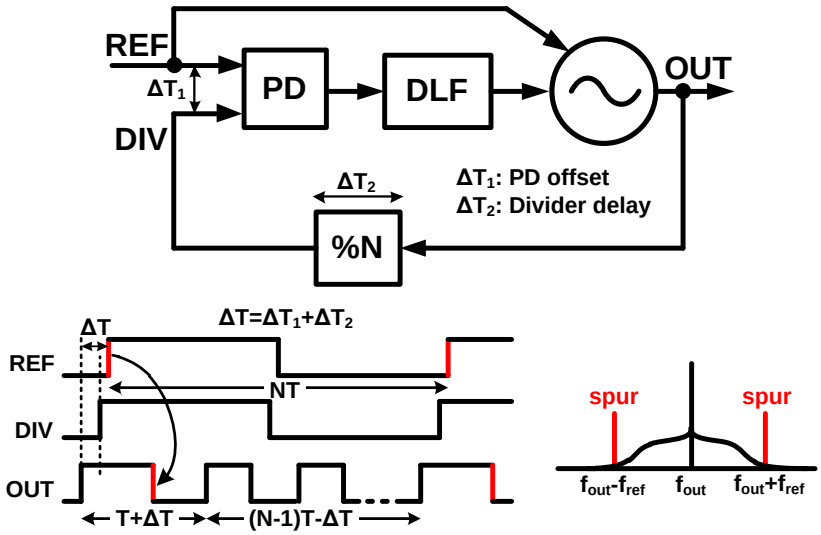


Fig. 4.2: Phase detector inherent offset and feedback divider delay generate a static offset between the DCO phase and the injected reference. This static phase offset creates reference spurs at the output of the MDLL.

The expression of reference spur at the output spectrum generated due to ΔT offset is derived next. As discussed above and also evident from Fig. 4.3, the ΔT offset makes the first MDLL output period T+ΔT. The remaining N-1 periods in every reference cycle are adjusted to $T_e = T - \frac{\Delta T}{N-1}$, in order to maintain the phase relationship between the input reference and the output. Since the pattern repeats in every reference period, T_{ref}, we need to consider each MDLL output pulse separately within one reference cycle and convolve it with a train of impulses of period T_{ref} to represent the periodic nature of MDLL output.

To start with the first MDLL pulse ($x_1(t)$) that stays at 1 for the duration T/2+ΔT, output after convolution with the impulse train can be written as:

$$y_1(t) = x_1(t) * \sum_{k=-\infty}^{+\infty} \delta(t - kT_{ref}) \qquad (4.1)$$

Fourier transformation of $y_1(t)$ to convert the signal into frequency domain gives:

$$Y_1(\omega) = X_1(\omega)\frac{1}{T_{ref}}\sum_{k=-\infty}^{+\infty}\delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) = \left(\frac{1-e^{-j\omega\left(\frac{T}{2}+\Delta T\right)}}{j\omega T_{ref}}\right)\sum_{k=-\infty}^{+\infty}\delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) \qquad (4.2)$$

$X_1(\omega)$ is a sync-function having nulls at the multiples of $1/(T/2+\Delta T)$ and it is sampled at an interval of $1/T_{ref}$, as represented in Fig. 4.3.

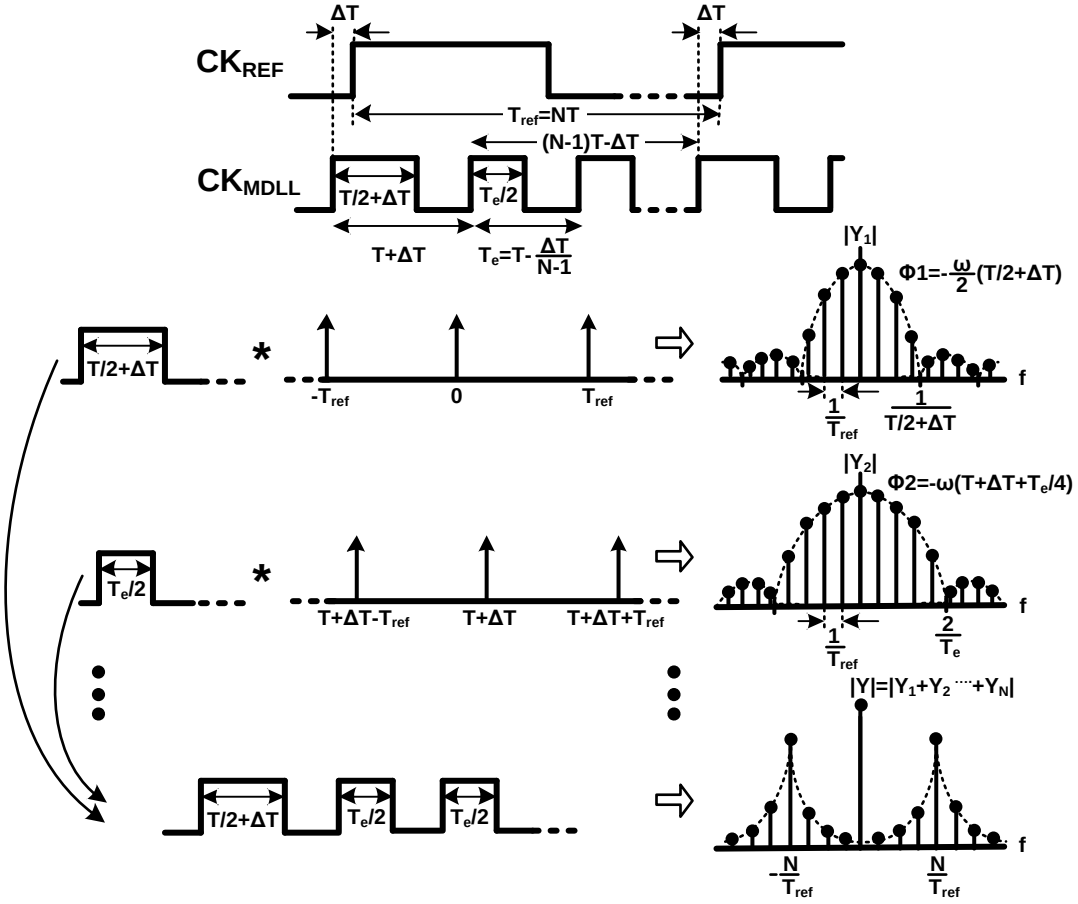


Fig. 4.3: Calculation of the output reference spur for a given phase offset between the VCO and the injected reference. Fourier transform of each output pulse in a given reference period can be utilized to calculate the spur accurately.

Similarly, the convolution of the second pulse ($x_2(t)$) of width $T_e/2$ with the same impulse train but time-shifted by $T+\Delta T$ results:

$$Y_2(\omega) = \left(\frac{1-e^{-j\omega T_e/2}}{j\omega T_{ref}}\right) e^{-j\omega(T+\Delta T)} \sum_{k=-\infty}^{+\infty} \delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) \quad (4.3)$$

As evident from equation (4.3), the first term in the right-hand side is the Fourier transformation of $x_2(t)$ that has nulls at the multiples of $2/T_e$ and a $T+\Delta T$ time shift in impulse train introduces an additional phase factor of $e^{-j\omega(T+\Delta T)}$ in the expression of $Y_2(\omega)$. Using the same procedure, the impulse train for the third sample will be time shifted by $T_e+T+\Delta T$ and so on. Since all the remaining N-1 pulses after the first pulse in every reference cycle has same pulse width of $T_e/2$, their Fourier function will be same as obtained in equation (4.3), except the phase factor that will be different in each pulse. Therefore, the Fourier function of the m^{th} pulse where m=2, 3, …. N can be expressed as:

$$Y_m(\omega) = \left(\frac{1-e^{-j\omega T_e/2}}{j\omega T_{ref}}\right) e^{-j\omega[(m-2)T_e+(T+\Delta T)]} \sum_{k=-\infty}^{+\infty} \delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) \quad (4.4)$$

The complete expression for the MDLL output can be calculated by adding the Fourier expression of all the pulses in one reference cycle and this is as follows:

$$Y(\omega) = Y_1(\omega) + \sum_{m=2}^{N} Y_m(\omega) \quad (4.5)$$

Using equation (4.2) and (4.4), we get:

$$Y(\omega) =$$

$$\frac{1}{j\omega T_{ref}}\left[1 - e^{-j\omega\left(\frac{T}{2}+\Delta T\right)} + \left(1 - e^{-j\omega\frac{T_e}{2}}\right)\sum_{m=2}^{N} e^{-j\omega[(m-2)T_e+(T+\Delta T)]}\right]\sum_{k=-\infty}^{+\infty}\delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) \quad (4.6)$$

$$Y(\omega) = \frac{1}{j\omega T_{ref}}\left[1 - e^{-j\omega\left(\frac{T}{2}+\Delta T\right)} + (1 - e^{-j\omega\frac{T_e}{2}})e^{-j\omega(T+\Delta T)}\left(\frac{1-e^{-j\omega(N-1)T_e}}{1-e^{-j\omega T_e}}\right)\right]\sum_{k=-\infty}^{+\infty}\delta\left(\omega - \frac{2\pi k}{T_{ref}}\right) \quad (4.7)$$

Since $T_{ref}=NT$, equation (4.7) can be simplified to:

$$Y(k) = \frac{1}{j2\pi k}\left[1 - e^{-j\frac{2\pi k}{N}\left(\frac{1}{2}+\frac{\Delta T}{T}\right)} + \left(1 - e^{-j\frac{\pi k T_e}{N\ T}}\right) e^{-j\frac{2\pi k}{N}\left(1+\frac{\Delta T}{T}\right)} \frac{1-e^{-j\frac{2\pi k(N-1)T_e}{N\ T}}}{1-e^{-j\frac{2\pi k T_e}{N\ T}}}\right] \quad (4.8)$$

From the above equation, the fundamental frequency component ($f_{out}=N/T_{ref}$) of the output can be obtained by calculating the magnitude of Y(k) for k=N i.e. |Y(k=N)|. The ratio of the frequency component at two sidebands i.e. for k=N±1 to the fundamental component gives the reference spur at the MDLL output and it is expressed as:

$$spur_{MDLL}\ (f_{out} \pm f_{ref}) = 20\log\left(\frac{|Y(k=N\pm1)|}{|Y(k=N)|}\right) \quad (4.9)$$

Under the assumption of $\Delta T \ll T$ in equation (4.8), the expression for the fundamental and the sidebands magnitude can be approximated as:

$$|Y(k = N)| \approx \frac{1}{\pi} \quad \text{and} \quad |Y(k = N \pm 1)| \approx \frac{1}{\pi}\frac{\Delta T}{T} \quad (4.10)$$

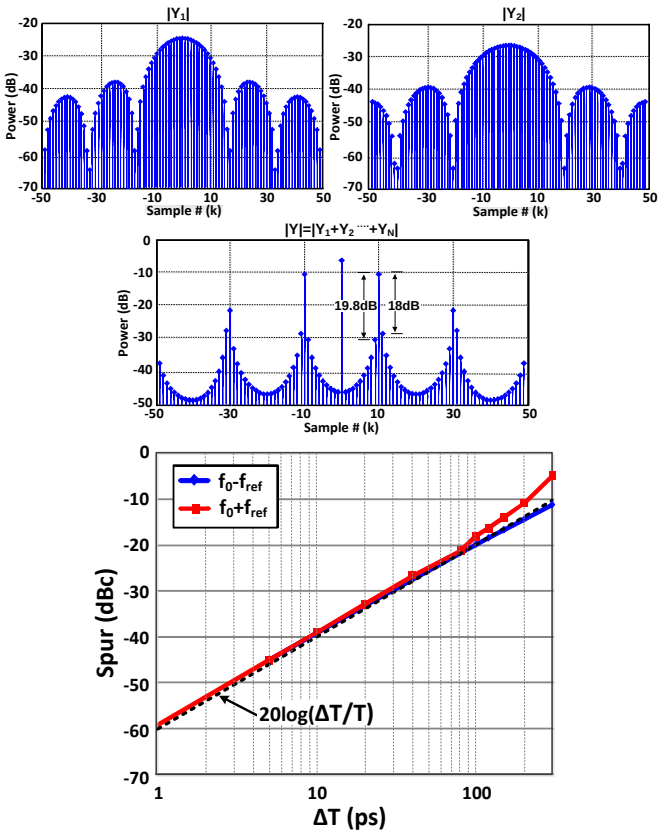
Therefore, using equation (4.10), the simplified expression for reference spur, calculated from equation (4.9) is:

$$spur_{MDLL}\ (f_{out} \pm f_{ref}) \approx 20\log\left(\frac{\Delta T}{T}\right) \quad (4.11)$$

Above equation matches the expression derived in [41]. However, the assumption is valid only when the SPO is very small compared to the MDLL output time period, which may not be always the case.

An example is shown in Fig. 4.4(a) for an MDLL output frequency of 1GHz, N=10 and offset ΔT=100ps. The plot for $|Y_1|$, $|Y_2|$ and |Y| are obtained from equation (4.2), (4.3) and (4.8) respectively. The magnitude of fundamental component is |Y(k=10)|=0.312. |Y(k=9)|=0.032 and |Y(k=11)|=0.039 are two sidebands relative to the fundamental which results reference spur of -19.8dB and -18dB respectively. The difference in the spur levels in two side bands is due to the contribution of the higher

order harmonics (i.e. at $2f_{out}$, $3f_{out}$ etc.) present in the output square wave. In this case, the 9^{th} and 11^{th} harmonic of the reference spur generated from the 2^{nd} harmonic of the output ($2f_{out}$) overlaps with the two sidebands of the fundamental causing the mismatch in the spur levels. The analysis in [41] assumes the output to be a sinusoidal signal, neglecting the impact of higher order harmonics. Reference spur calculated using equation (4.11) is -20dB. Fig. 4.4(b) plots the calculated reference spur when ΔT is varied from 1ps to 300ps. The values are compared with the approximate results obtained from equation (4.11) and it is clear that this approximation is valid when the offset is below nearly about 80ps i.e. 8% of the output time period.



(a) **(b)**

Fig. 4.4: (a) Output reference spur calculated for a 100ps phase offset in a 1GHz MDLL output with N=10. (b) Reference spur plot for a time offset ranging from 1ps to 300ps.

4.3 Reference Spur Cancellation Using Zero-offset APD

The main source of SPO, as already explained, is the delay mismatch between the phase detection path and the reference injection path. Therefore, additional delay in one of the paths can mitigate this mismatch. In this work, a digital-to-time converter (DTC) is utilized in the phase detection path for the reference and DCO phase alignment, as shown in Fig. 4.5. Referring to Fig. 4.2, a ΔT offset is created between the edges of REF and OUT signals, which causes the reference spur. Now in the timing diagram of Fig. 4.5, the REF is delayed by the DTC to generate REF' and it is then compared with DIV by the PD. So the ΔT offset will now be present between the edges of REF' and OUT. If the DTC delay is precisely set to ΔT, REF can be perfectly aligned with OUT, cancelling the spur completely.

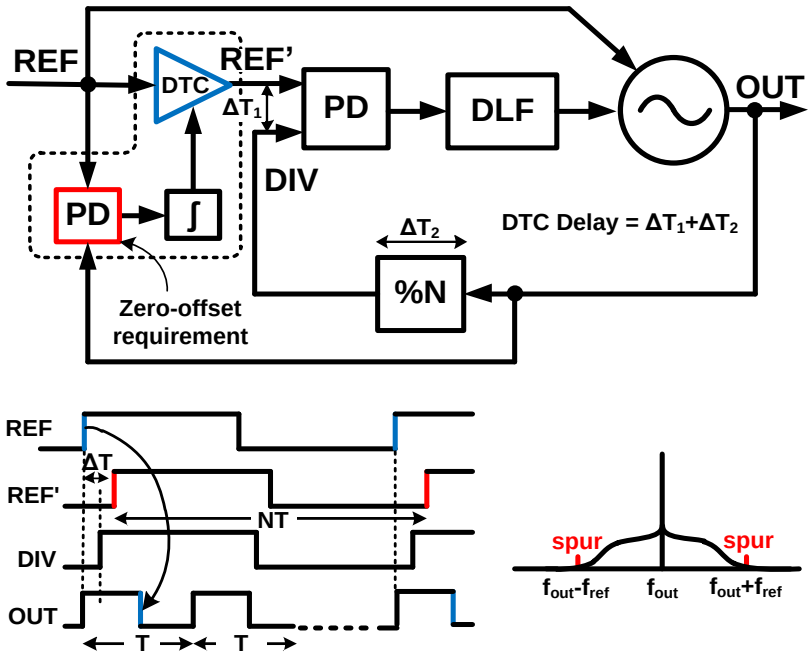
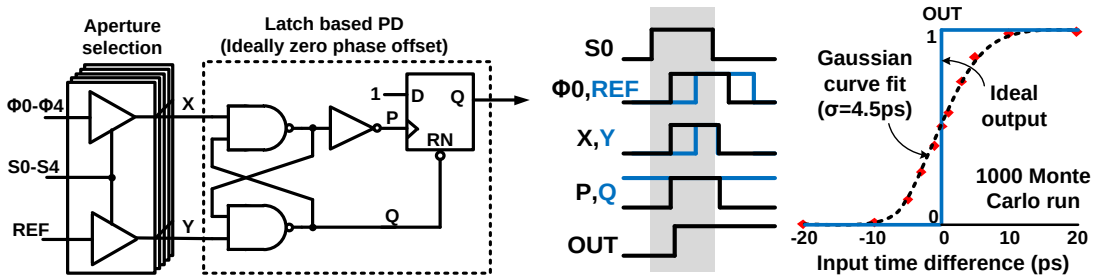


Fig. 4.5: Reference spur cancellation technique. The DTC delay can precisely align the injected reference and the DCO phase. Accurate cancellation requires a zero-offset phase detector.

However, perfect phase alignment is practically impossible due to the nonzero resolution of the DTC and other parasitic mismatches present in the circuit, creating a very low magnitude of spur. In order to track the ΔT offset under PVT variations, a spur cancellation loop is present that consists of a PD and a digital accumulator to adjust the DTC delay, if there is any change in ΔT. Since the rate of variation of ΔT is much slower, the bandwidth of this loop is set much lower than the MDLL bandwidth to keep the complete system stable. The PD compares the phase difference between the REF and the OUT to decide which one is leading or lagging. However if there is any inherent offset present in this PD, it will directly appear at the output as STO, lowering the accuracy of the spur cancellation circuit.

Fig. 4.6(a) shows the implementation of a zero-offset APD to address the issue explained above. A NAND-gate SR-latch is utilized to compare the phases of two input clocks without introducing any offset. Since a latch is sensitive to both the rising and the falling edges of the input signals, an aperture selection block is placed before the latch to capture only the rising edges for phase detection. Only one out of five DCO phases (Φ0-Φ4) is selected at a time by the enable signals S0-S4. The SR-latch is followed by a D flip-flop (DFF) that stores the detected value for the reference period. Depending on the latch output state, the DFF either samples 1 or resets to 0. An example in Fig. 4.6(b) shows the state of different nodes of the APD when the DCO phase leads the reference. Although APD has no offset under nominal condition, process mismatch can introduce

some phase offset in the latch. Therefore, we performed 1000 run Monte-Carlo mismatch simulations by sweeping the time difference between two input clock edges and counting the number of occurrences of 1 at the APD output. An RMS phase offset of 4.5ps is obtained after the Gaussian curve fitting on simulated result, which is shown in Fig. 4.6 (c). The layout of the APD is made symmetric to minimize any additional systematic offset due to parasitic mismatches.



(a) **(b)** **(c)**

Fig. 4.6: (a) Zero-offset phase detector implementation utilizing a latch. Aperture selection block captures only the rising edges of two input clocks for phase comparison. (b) Example timing diagram of latch internal nodes when VCO phase arrives earlier than reference. (c) Monte-carlo simulation result to estimate the input offset due to device mismatch.

4.4 In-situ Offset Detection Circuit

Phase offset in an MDLL is conventionally measured from the reference spur in the output frequency spectrum. Equation (4.11) in section 4.2 can be used to calculate ΔT from the measured spur. However, a high frequency off-chip test set-up may introduce measurement error. For example, a 1dB error in spur measurement is equivalent to 11% error in the offset calculation. Therefore, we propose an in-situ detection scheme to measure SPO accurately in time domain.

Fig. 4.7 shows the schematic of the proposed MDLL offset detection circuit. The programmable delay block generates a variable delay (T_P), which is close to the time period (T_{CKMDLL}) of the input clock. The DFF that acts as a phase detector, compare T_{CKMDLL} with T_P at every rising edge of the input clock and generates an error pulse at the output when T_P is larger than T_{CKMDLL}. Output remains at 0 otherwise. Error rate is calculated by measuring T_{CKMDLL} and the average time period of the error output i.e. avg(T_{BER}) [43]. A 10-bit counter is used to divide the output frequency when the error rate is high. An error rate plot can be obtained by sweeping T_P and the transition from low error rate to high error rate in the plot happens when T_P is near T_{CKMDLL}. Therefore, this error rate plot captures the time-period of any input clock. This property is utilized for the phase offset measurement at the output of an MDLL. Using this circuit, the period of every N^{th} clock cycle of the MDLL can be measured separately. Counter selection block selects a particular MDLL period in every reference cycle.

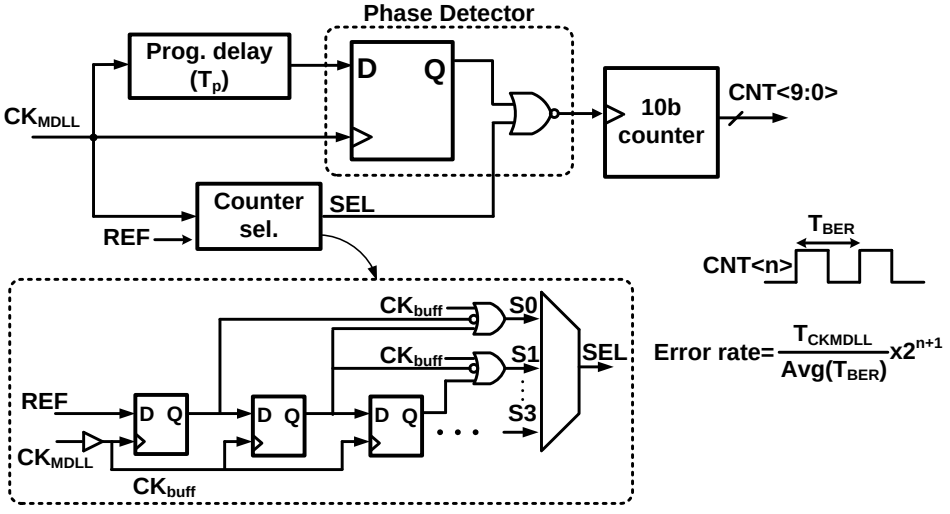


Fig. 4.7: Proposed in-situ SPO measurement circuit based on error rate calculation. Counter selection block selects a given output period at a time in every reference cycle.

As an example for N=4, shown in Fig. 4.8(a), S0 selects the first clock period to measure the error rate of the previous cycle and thereby, low to high error rate transition happens near T-ΔT/3. Similarly, for S1 selection, transition happens near T+ΔT. Since only the first clock period is different from the remaining periods in a reference cycle, the error rate plot for S1 selection will be skewed relative to the others (i.e. S0, S2, S3). The amount of skew is equal to the time period difference between the first period and the remaining periods which is N/(N-1)*ΔT, where ΔT is the phase offset and N is the frequency multiplication factor of the MDLL (shown in Fig. 4.8(b)). Upon ΔT cancellation by the reference spur cancellation circuit, S1 aligns with others eliminating any skew. Average time period of the error i.e. avg.(T_{BER}) is calculated off-chip using an oscilloscope. As the error output frequency is very low after the 10-bit counter, the measurement set-up doesn't involve any high frequency signals.

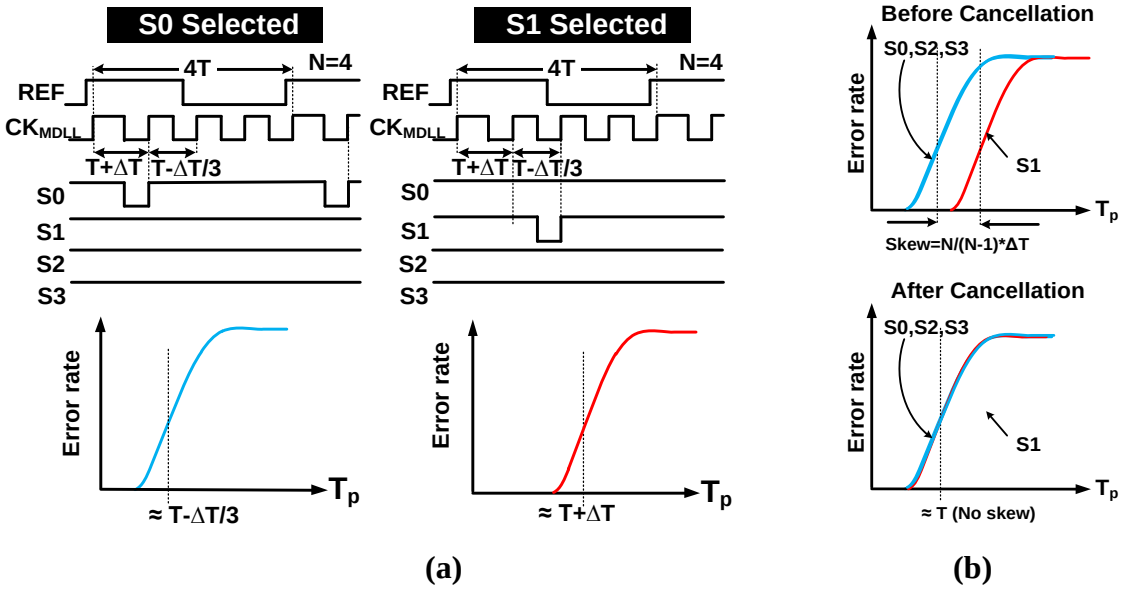
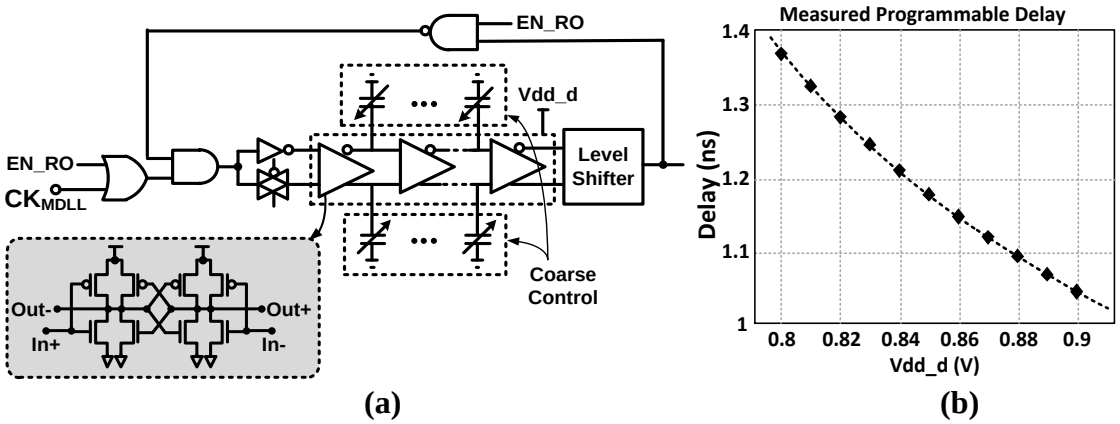


Fig. 4.8: (a) Timing diagram and error rate plot of S0 and S1 selection cases. Transition from low to high error rate happens near T- ΔT/3 and T+ ΔT for S0 and

S1 selection, respectively. (b) Before spur cancellation, error rate plot of S1 selection will be skewed by N/(N-1)*ΔT where N is the frequency multiplication factor.

The programmable delay generation block is critical here, as it directly affects the resolution of the phase-offset measurement. Fig. 4.9 (a) explains the implementation of this circuit. Delay stages are made differential to minimize supply noise sensitivity. 8-bit switched-capacitors perform coarse delay tuning to cover wide input clock frequency range while the supply of the delay line (Vdd_d) is varied for fine delay tuning. To measure the absolute delay, the delay stages are connected in a ring oscillator configuration by setting EN_RO=1 and the oscillation time period is calculated. Measured delays from the implemented test chip for different Vdd_d values are plotted in Fig. 4.9 (b).



(a) **(b)**

Fig. 4.9: (a) Programmable delay circuit implementation. (b) Measured delay vs. Vdd_d plot.

4.5 MDLL Implementation Details

Fig. 4.10 shows the complete block diagram of the proposed MDLL. Similar to the architecture explained in chapter 3.4, a separate frequency-locking path, comprised of a fractional frequency detector (FD) and a digital integrator is employed to set the operating frequency of the sub-sampling MDLL. The integer and fractional portion of the frequency multiplication factor is set by INT<7:0> and FRAC<1:0> control signals, respectively. A 5:1 multiplexer (MUX) and selection logic block in the fractional FD selects one out of five phases of the DCO periodically without creating a glitch during phase transition to achieve the desired fractional frequency ratio at the multiple of 1/5. After frequency locking, the integrator output is stored and the feedback path is disabled, turning on the phase locking path. A DFF in the phase locking path sub-samples the high frequency DCO output with the input reference clock and adjusts the DCO frequency by increasing or decreasing the DLF codes. Upon phase lock, the reference and the DCO rising edges appears within the time window of the APD (i.e. when any one of S0-S4 is 1) and the reference spur cancellation circuit cancels any SPO present between the reference and the DCO phase by tuning the 6-bit DTC delay. Once the DTC codes settle and the SPO is cancelled, the reference injection path is turned on for the MDLL operation. The in-situ detection circuit explained in section 4.4 detects the phase offset before and after cancellation to measure the accuracy of the spur cancellation circuit.

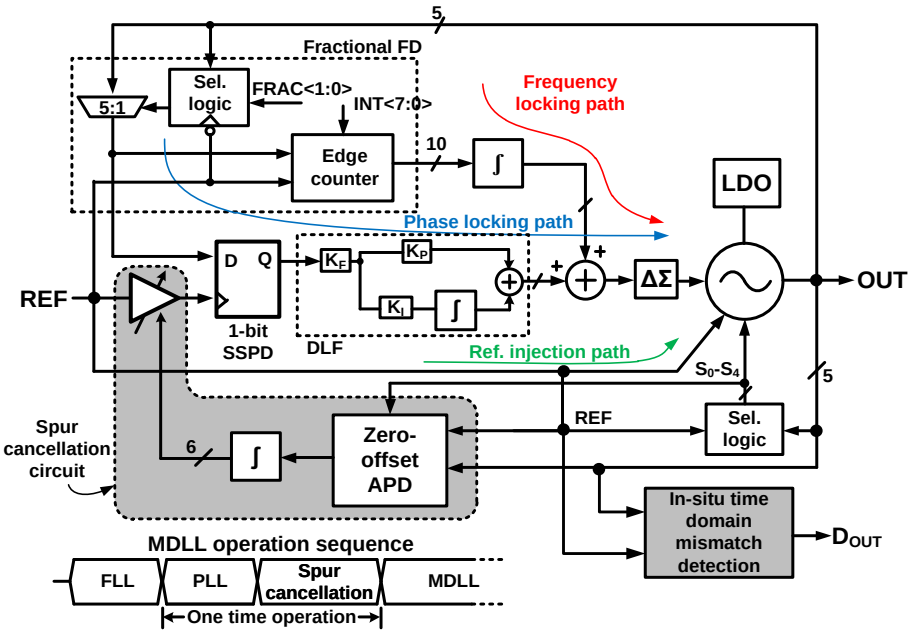


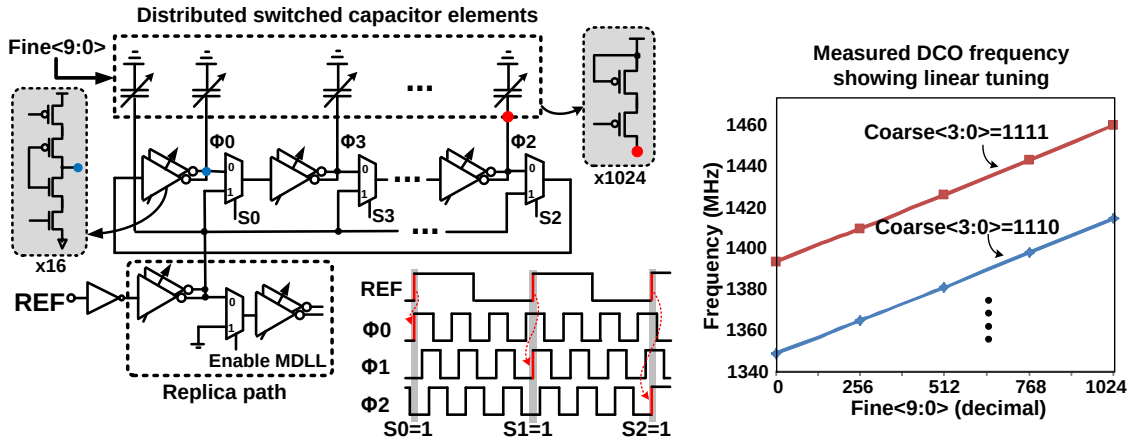
Fig. 4.10: Block diagram of the sub-sampling fractional-N digital MDLL with the proposed zero-offset aperture PD based spur cancellation loop and in-situ SPO measurement circuit.

The implementation of the multiplexed ring-DCO that realigns the DCO phase with the reference and the fractional frequency detector in the frequency-locking path are discussed below.

4.5.1. *Reference Realigned DCO*

Fig. 4.11(a) shows the schematic of the reference realigned DCO. Each stage of the five-stage ring oscillator consists of an inverter and a MUX. When the MUX selection goes to 1, the clean edge of the reference is inserted into the ring oscillator path. Since the fractional N is generated by the periodic rotation of the DCO phases for phase detection, the appropriate DCO phase needs to be replaced by the reference. For example, when Φ0 phase is selected by the 5:1 MUX for phase detection, S0 goes to 1 for a small duration, replacing Φ0 with the reference in the DCO loop. The same signals (S0- S4) that enable

the APD, described in section 4.3, are also used here for MUX selection. Each inversion stage of the ring oscillator consists of 16 parallel tri-state inverters enabled by the coarse tuning codes (Coarse<3:0>) to achieve a wide tuning range. 10-bit binary weighted switched capacitor branches are used for fine frequency tuning that locks the MDLL. The frequency resolution is improved by utilizing the drain junction of a minimum sized PMOS transistor as a unit switched-capacitor element [33]. All 1024 such elements are uniformly distributed across the 5-inverter stages to achieve good frequency linearity. A completely symmetric layout strategy is also incorporated to minimize device-to-device mismatch. Measured frequency tuning characteristic in Fig. 4.11(b) verifies the high linearity of the DCO. The replica path for the reference matches its rise time with the DCO internal phases, so that the APD can precisely detect the offset without any dependence on its threshold crossing.



(a) **(b)**

Fig. 4.11: (a) Reference realigned DCO schematic with distributed switched-capacitor branches for linear frequency tuning. (b) Measured DCO frequency verifying linear tuning characteristics.

The power supply noise sensitivity is minimized with an on-chip low dropout regulator (LDO) for the DCO supply. Although the supply noise within the PLL bandwidth can be automatically tracked by the loop itself, high frequency noise beyond the PLL bandwidth is suppressed by the LDO. Therefore, a higher LDO bandwidth (about 10X of the PLL bandwidth) is essential for better power supply noise suppression.

4.5.2. *Fractional Frequency Detector*

The fractional FD in a divider-less PLL is conventionally realized using a high resolution TDC and a counter to detect the fractional and integer portions, respectively [28]. TDC enhances the fractional frequency resolution but increases the design complexity and power consumption. In this work, as shown in Fig. 4.12, a wide detection range edge counter [32] counts the number of rising edges of the DCO (DCO_OUT) between two reference edges and a 5:1 MUX periodically selects DCO phases for different fraction generation. Here, the edge counter and the MUX together perform the fractional frequency detection. The edge counter comprises an 8-bit full adder based high-speed synchronous counter that is triggered by every rising edge of the DCO. The counter outputs (A7-A0) are sampled and stored once in every reference cycle. In order to avoid meta-stability issues, the reference clock (REF) is resynchronized to the falling edge of the DCO before sampling. Register 1 stores the recent value of the counter, while register 2 stores the value of the previous reference cycle. The number of DCO edges in any given reference cycle is obtained by subtracting the values stored in two registers. Finally, this value is compared with INT<7:0> so that under frequency locked condition, the 8-bit output (D_{OUT}) of the fractional FD settles to 0.

FRAC<1:0> controls the fractional part of the frequency multiplication factor by changing the order of the DCO phase selection. As an example, for generating 1/5 as a fraction, Φ0 is selected in first reference cycle, Φ1 second, Φ2 third and so on. However, during the transition from one DCO phase to another, unwanted glitches can appear, as evident from the timing diagram in Fig. 4.12. These glitches alter the counter output, locking the loop to an undesired frequency. In order to avoid this, the phase transition should happen when both signals are either 0 or 1. For example, during phase transition from Φ0 to Φ1, MUX selection (SEL) should change between the rising edge of Φ1 and the falling edge of Φ0. The 'MUX Selection Logic' is used for this purpose. It basically resynchronizes the REF with the appropriate DCO phase and generates SEL using a 5-bit ring counter.

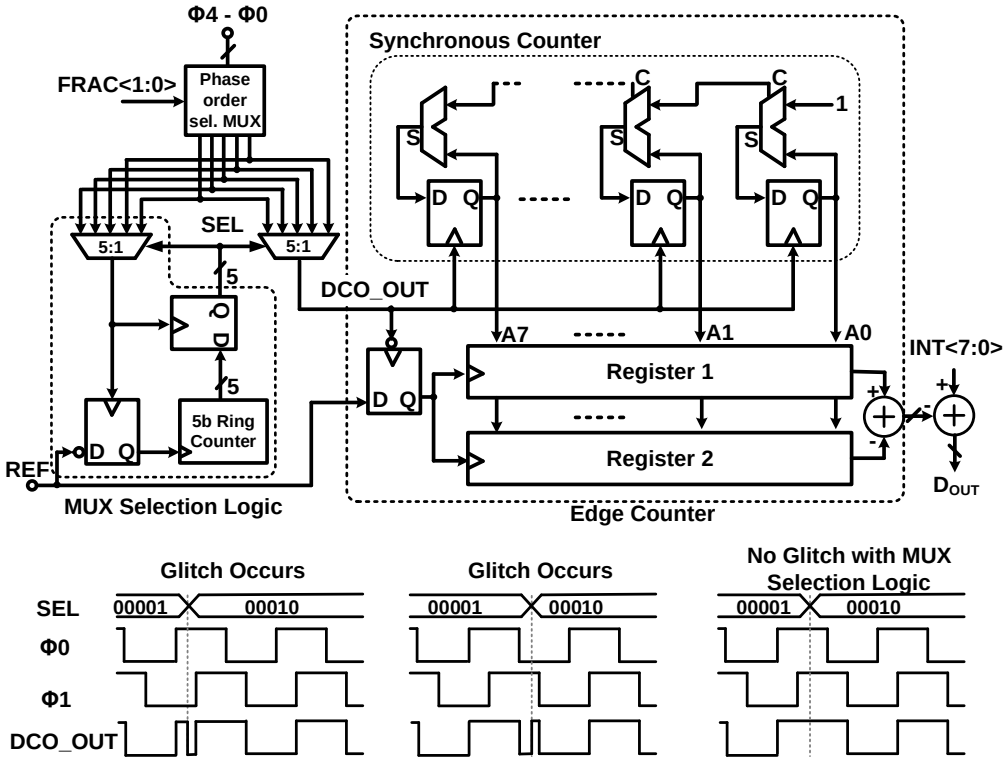


Fig. 4.12: Fractional frequency detector with glitch free DCO phase transition for precise frequency locking. The MUX selection logic ensures no glitches are present in the DCO output.

4.6 Measurement Results

The proposed MDLL is realized in a 1.2V, 65nm LP CMOS process. Fig. 4.13 shows the measured error rate plot obtained from the in-situ detection block by varying the programmable delay, T_p, for an output frequency of 800MHz while using a 100MHz input reference. When the spur cancellation loop is inactive, the error plot for S1 selection is skewed by 131ps than others. This corresponds to an STO of 115ps. Upon activation of the spur cancellation loop; the skew is reduced to only 6ps, which is contributed by the small offset present in the APD due to process mismatch. As expected, the error rate plots for PLL doesn't show any noticeable skew. These time-domain measurement results are compared with the frequency domain reference spur at 900MHz, which shows -23dB and -47dB of reference spur before and after cancellation respectively while it is -48dB during PLL mode of operation.

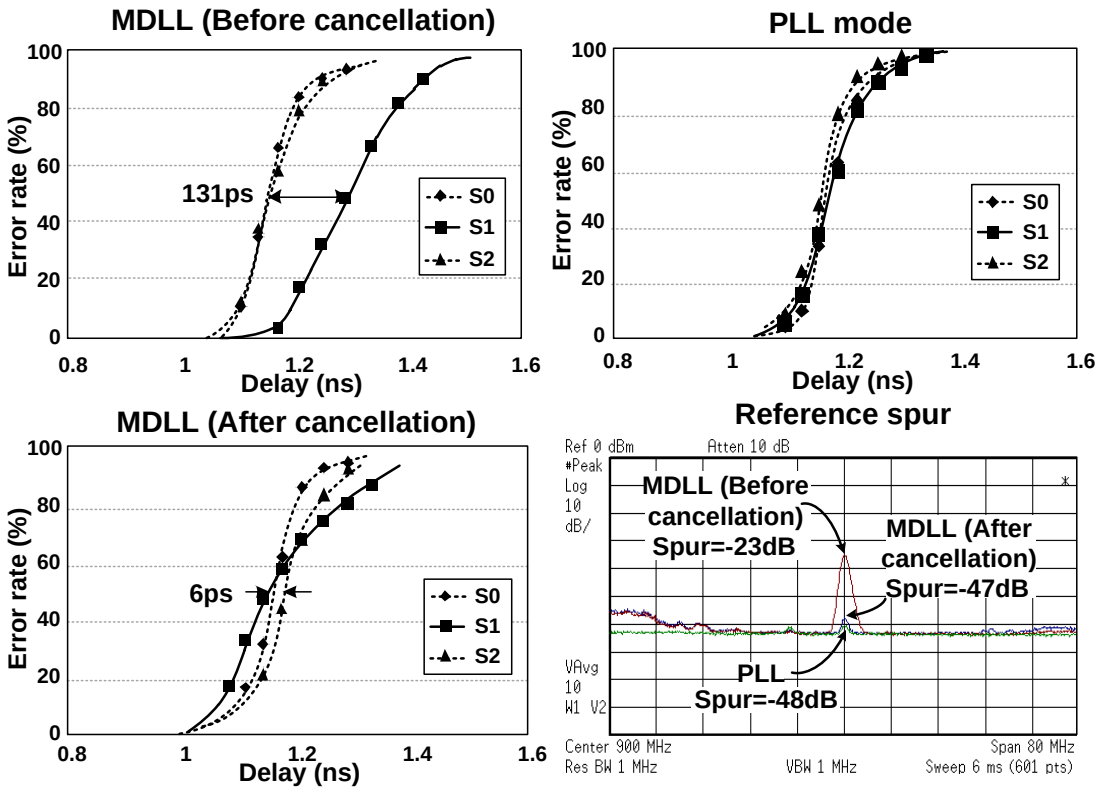
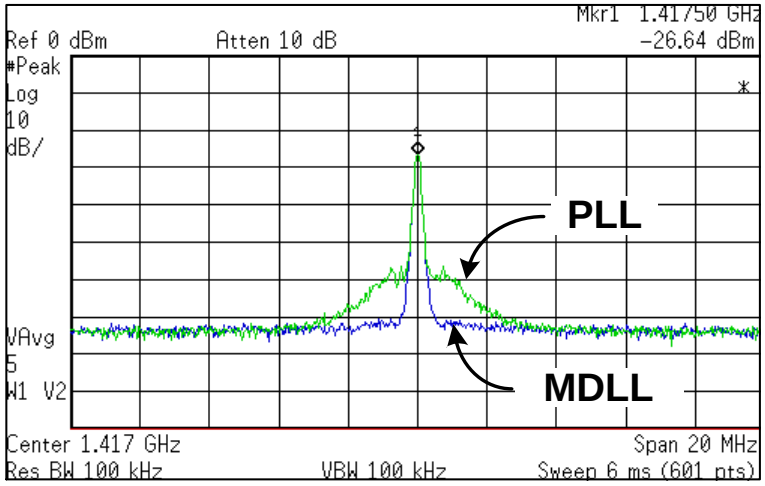
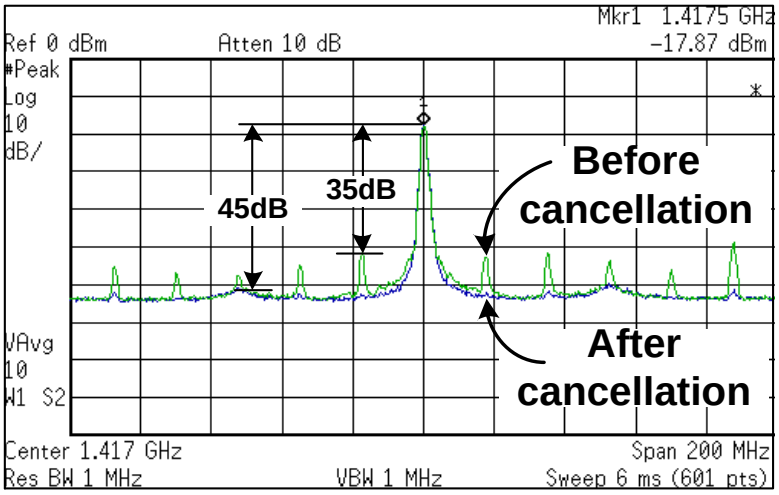


Fig. 4.13: Measured error rate from the in-situ offset detection circuit in MDLL mode (before and after spur cancellation), and in PLL mode. Reference spur for an 800MHz clock using a 100MHz reference is also shown.

Output frequency spectrums are plotted in Fig. 4.14 (a) comparing the performance between the PLL and the MDLL mode of operation at output frequency of 1.4175GHz for an input reference of 87.5MHz. It clearly shows higher noise suppression in MDLL mode. Output reference spur at the multiples of $f_{REF}/5$=17.5MHz are plotted in Fig. 4.14 (b) before and after reference spur cancellation. Reference spur before cancellation was -35dB while it reduces to -45dB after cancellation.



(a)



(b)

Fig. 4.14: (a) Measured output spectrum and (b) MDLL fractional spur before and after reference spur cancellation.

Fig. 4.15 shows the measured phase-noise plot for both integer and fractional mode at output frequency of 1.4GHz and 1.4175GHz, respectively. The MDLL shows about 16dB and 9dB lower phase-noise compared to a PLL having identical operating conditions at 100kHz offset in integer and fractional modes, respectively.

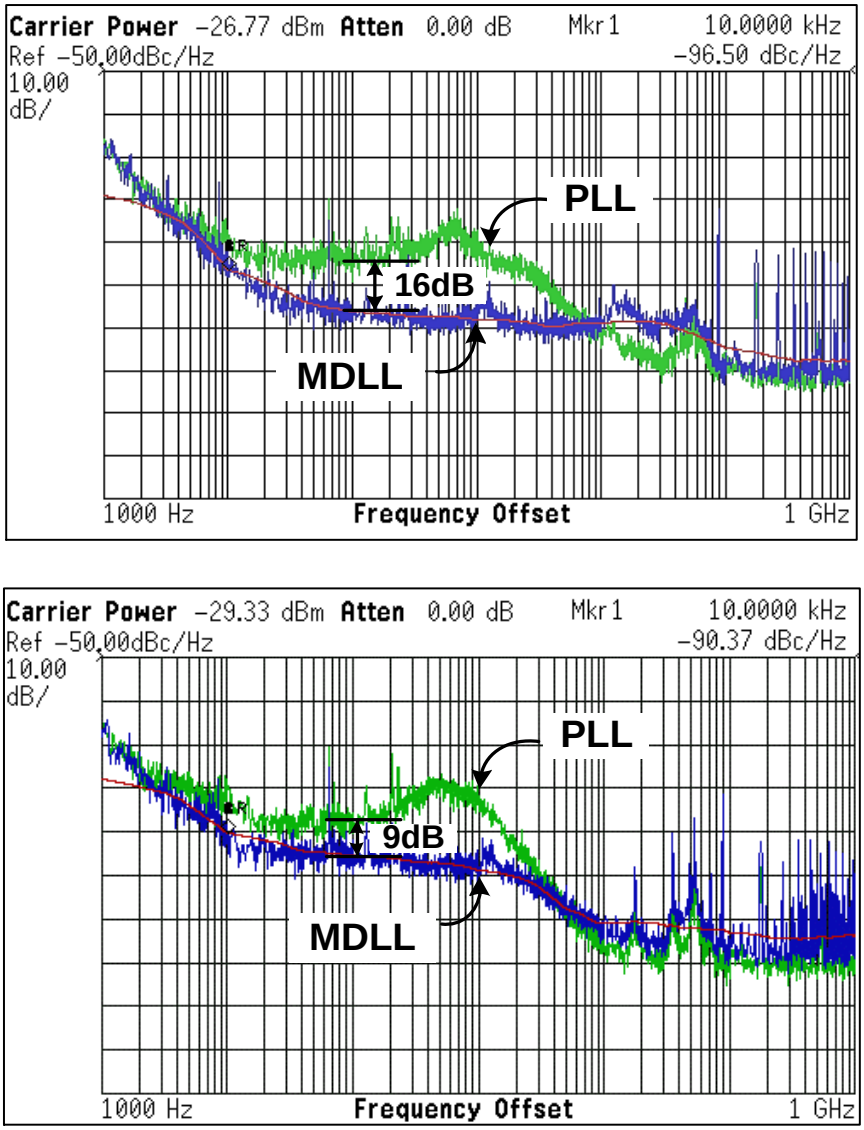
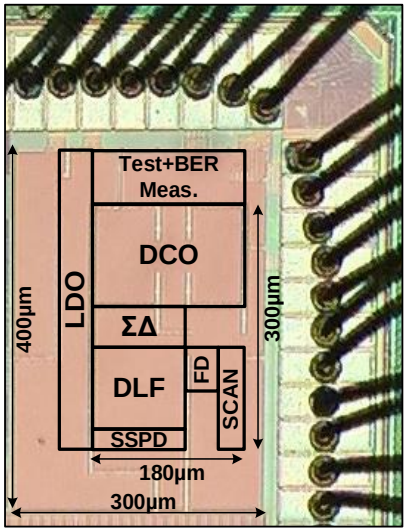


Fig. 4.15: Measured phase noise in PLL and MDLL mode of operation. MDLL shows 16dB and 9dB lower phase noise than PLL at 100kHz offset frequency in integer (top) and fractional (bottom) mode respectively.

Fig. 4.16 shows the chip micrograph with a performance summary table. The overall chip area is 0.12mm^2, of which the MDLL/PLL core is only 0.054mm^2. Output frequency range is 0.2-to-1.45GHz, while total core power consumption is 8mW from a 1.2V supply at 1.4GHz. Fig. 4.17 compares the performance of this work with other

state-of-the-art inductor-less fractional-N frequency synthesizers. The plot in Fig. 4.18 compares the FoM with the recently published PLL and MDLL designs.



		PLL mode	MDLL mode
Technology		CMOS 65nm, 1.2V	
Output frequency		Integer: 1.4GHz Fraction: 1.4175GHz	
Frequency range		0.2–1.45 GHz	
DCO type		5-stage ring oscillator	
In-band PN (dBc/Hz @100kHz)	Integer	-92	-108
	Fraction	-87	-96
Integ. RMS jitter (10kHz-10MHz)	Integer	8.1ps	2ps
	Fraction	11.7ps	2.8ps
Power (mW)	DCO	4.5	
	Total	8.0	
FOM (dB)	Integer	-212.8	-225
	Fraction	-209	-222
Area	Core	180µm x 300µm	
	Total	300µm x 400µm	

Fig. 4.16: Test chip micrograph and performance summary.

	This Work	Song [45] ISSCC'15	Deng [44] ISSCC'15	Marucci [37] ISSCC'14	Liu [25] ISSCC'14	Jang [24] ISSCC'13	Park [40] ISSCC'12
Architecture	MDLL	FF- PLL*	Soft IL-PLL**	MDLL	PLL	PLL	IL- PLL**
Process	65nm	14nm	65nm	65nm	20nm	28nm	65nm
Output frequency /Range (GHz)	1.4175 /(0.2 –1.45)	1 /(0.032– 2)	1.5222 /(0.8–1.7)	1.651 /(1.6– 1.9)	1.2487 /(0.025–1.6)	0.962 /(0.032 – 2)	0.581 /(0.58– 0.611)
Ref. frequency (MHz)	87.5	32	380	50	25	30	32
Power (mW)	8	2.1	3	3	2.5	5.3	10.5
Intg. RMS jitter (ps) Intg. range	2.8 (0.39%) (10kHz – 10MHz)	18.8 (1.88%) (1kHz – 100MHz)	3.6 (0.55%) (1kHz – 100MHz)	1.4 (0.23%) (30kHz – 30MHz)	28 (3.5%) (20kHz – 40MHz)	19.3 (1.85%) (20kHz – 40MHz)	8 (0.46%) (100Hz – 40MHz)
FoM*** (dB)	-222	-211	-224	-232	-207	-207	-211
Area (mm^2)	0.054	0.009	0.048	0.4	0.012	0.026	0.083

*FF= Feed-forward **IL=Injection-locked ***FoM=20log(σ/1s)+10log(P/1mW)

Fig. 4.17: Performance comparison with other state-of-the-art fractional-N ring oscillator based frequency synthesizers.

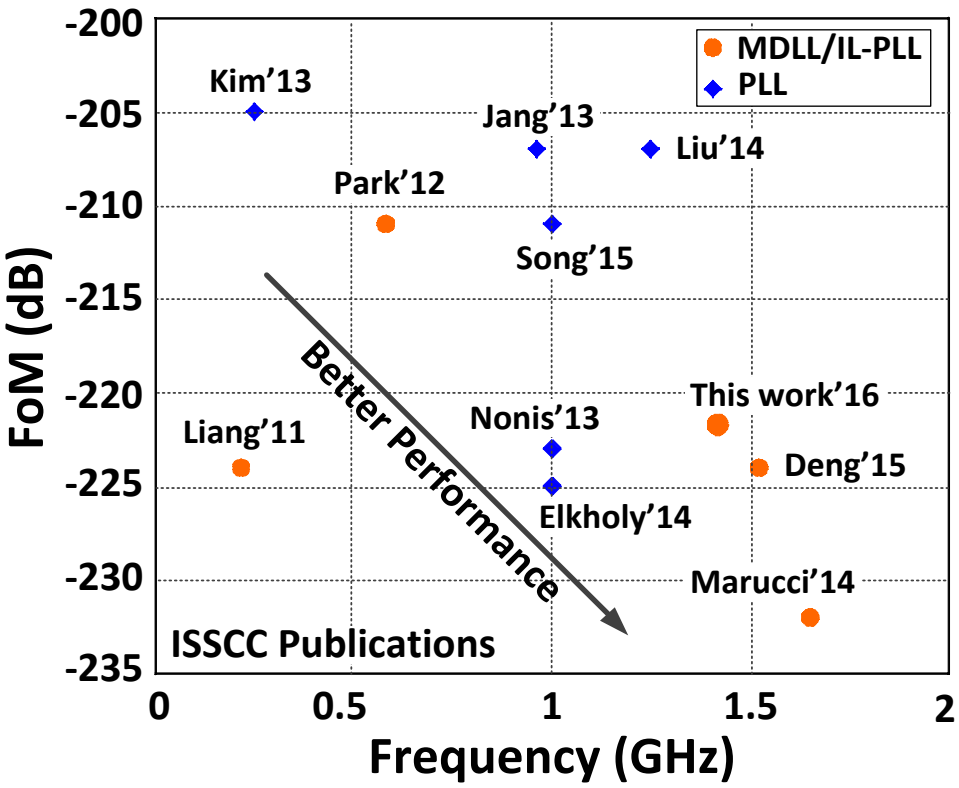


Fig. 4.18: Figure-of-merit (FoM) comparison with the recently published PLL and MDLL designs.

4.7 Conclusion

A fractional N sub-sampling digital MDLL is presented that eliminates the reference spur utilizing a DTC and a zero-offset APD. An in-situ detection circuit measures the SPO of MDLL very precisely in time domain without requiring any high-speed off-chip measurement set up. This work also addresses the reference spur issue in an MDLL based clock generation circuit, deriving a mathematical model to estimate the reference spur due to STO. A wide frequency range ring DCO achieves good linearity by utilizing a uniformly distributed switched-capacitor elements for frequency tuning and a completely symmetric layout design approach. Finally, the proposed concepts are verified

with the measurement results obtained from a prototype chip implemented in a 65nm LP CMOS technology. Phase noise measurement result shows about 9dB additional noise suppression in MDLL compared to a PLL at 1.4175GHz.

Chapter 5. Area Efficient Frequency Synthesizer with In-situ Jitter Monitor

5.1 Introduction

Integrated circuits for Internet-of-Things (IoT) applications such as health care monitoring inventory tracking, automotive sensors, smart grid, and robotic systems require medium frequency accuracy clock with low power consumption and small form factor. These systems typically require multiple clocks with frequencies ranging from a few Hz (e.g. low frequency internal wakeup timers) to 100's of MHz (e.g. memory or signal processing) [46]. Crystal oscillators generate a clean clock, but use of multiple crystals increases form factor and cost. Therefore, high frequency clocks are typically generated using frequency synthesizers that multiply the frequency generated from an external low frequency crystal oscillator.

Phase-locked loops (PLL) are conventionally used to generate very accurate frequency multiplications. However, maximum bandwidth limitation [47] requires large loop filter area and higher settling time. High power consumption, insufficient stability over wide frequency range are other key challenges for PLL design in scaled technologies. All digital PLLs [31] have been gaining popularity for area reduction, but it requires a high resolution Time to Digital Converter (TDC) that increases power consumption, quantization noise and output frequency spurs. To address these limitations

of PLL, [48] proposes a duty-cycled integer-N PLL that scarifies frequency accuracy to reduce power and settling time. In [49] and [50], free running oscillators are used with periodic frequency calibration. However, these approaches suffer from inaccurate output frequencies. A frequency-to-voltage converter based frequency synthesizer is proposed in [51] by capacitive charge redistribution. But voltage generation will have large inaccuracy due to leakage in advanced technologies. On top of that, depending on the input and output frequency, comparator input voltages may vary over a large range and that can change comparator gain and frequency accuracy. Also this implementation is not verified with actual chip measurement results. In this work [52], a circuit technique based on frequency-to-current conversion is proposed that can replace a PLL or the use of multiple crystal oscillators in a single chip, for medium accuracy frequency synthesis over a wide frequency range (e.g. 10X). This technique uses multiple current branches to tune output frequency very precisely. Proposed technique is implemented in 32nm SOI technology and performance is verified from measurement results. Unlike other compensated ring oscillator based architectures [55] that rely on the accuracy of the reference generation circuit and the capacitor, here capacitance ratio in the final frequency expression cancels any PVT variations of capacitor. High-density deep trench capacitors that can significantly reduce silicon area because of their 3-D nature are used for loop stability. A detailed mathematical model of the loop is derived for stability analysis. In addition, a high-resolution digital on-chip jitter measurement circuit is implemented to measure clock periodic jitter accurately.

Section 5.2 describes the proposed architecture of the frequency synthesizer. Section 5.3 provides the circuit implementation details. Small signal loop model and stability analysis are performed in section 5.4. On-chip jitter measurement circuit is covered in section 5.5. Section 5.6 shows the measurement results, followed by conclusion in section 5.7.

5.2 Proposed Frequency Synthesizer

Fig. 5.1 shows the proposed architectures of frequency synthesis technique by a frequency-to-current converter (FTC) circuit. In this current multiplication based divider-less architecture, input frequency (F_{in}) is converted to an equivalent current by an FTC of gain K_1 and then multiplied by a factor of N to generate current I_i. The oscillator output frequency (F_{out}) is converted to an equivalent current (I_{fb}) by an FTC with a gain of K_2. A high gain amplifier is used to make these two input currents equal by adjusting the VCO frequency. If the loop gain is high, input and output frequency relationship can be written as:

$$F_{out} = N\frac{K_1}{K_2}F_{in} \tag{5.1}$$

The frequency multiplication factor here is $N*K_1/K_2$. As N can be implemented in the analog domain by current mirrors, it can be designed to be very large without increasing hardware complexity as in the case of a digital PLL. Also fractional-N can be easily generated without any fractional frequency divider or delta-sigma modulator [53]. However, due to process mismatch, N cannot be exact. Monte-carlo simulation shows a 2.2% σ/μ variation in N due to process mismatch. Therefore additional process-trimming

current branches are required to compensate this mismatch effect. Number of branches can be tuned during initial frequency calibration by comparing F_{out} with desired output frequency. As frequency multiplication factor depends on the K_1/K_2 ratio, any PVT dependencies of FTCs get cancelled. Both K_1, K_2 can be minimized to reduce power consumption keeping K_1/K_2 ratio fixed.

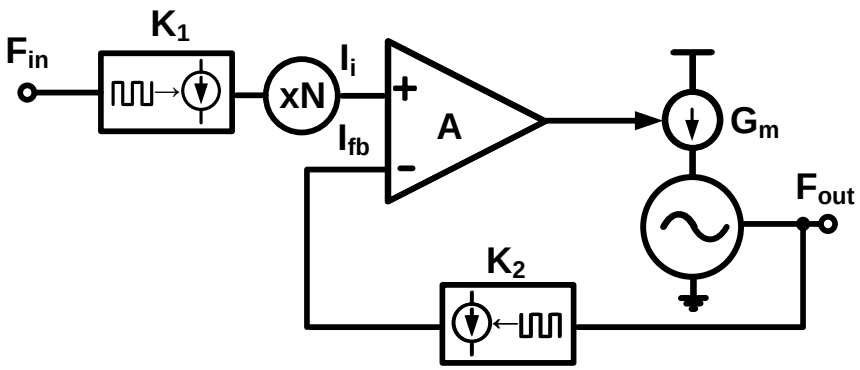


Fig. 5.1: Proposed frequency synthesizers based on current multiplier.

5.3 Circuit Implementation

Fig. 5.2 shows the circuit implementation of the proposed frequency synthesizer. Stage 1 converts input frequency (F_{in}) to proportional current by an FTC of gain $K_1=C_1V_{bint}$. Current multiplication is performed in stage 2 using a current mirror. Additional current branches are used to compensate process mismatch in the circuit. In layout design, common centroid technique is used to minimize process mismatch. A high gain comparator is used to detect the difference between multiplied input current (I_i) and the feedback current (I_{fb}) generated from output frequency by an FTC of gain $K_2=C_2V_{bint}$. Therefore frequency multiplication factor here is $N*C_1/C_2$. As V_{bint} gets cancelled in final

expression, it can be generated simply by dividing the supply voltage. Also capacitance ratio makes output frequency insensitive to temperature variation.

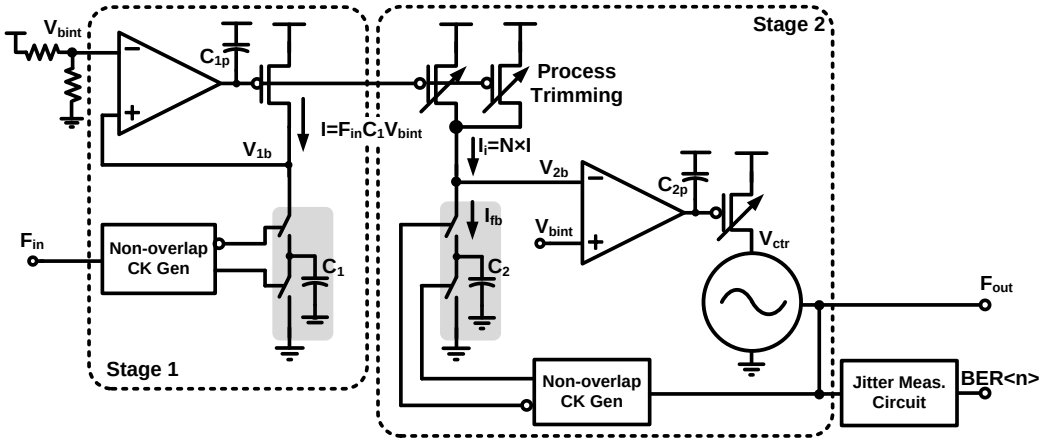


Fig. 5.2: Proposed current multiplier based frequency synthesizer schematic with on-chip periodic jitter measurement circuit.

5.3.1. *Frequency to Current Converter (FTC)*

As shown in Fig. 5.3, frequency-to-current conversion is performed by a switched capacitor resistor combined with a voltage-to-current converter [55] that produces an output current proportional to the input clock frequency. In this design C_1=8pF, C_2=1pF is used considering the effect of switch parasitic capacitances. Two FTCs are placed together in layout design to minimize process mismatch.

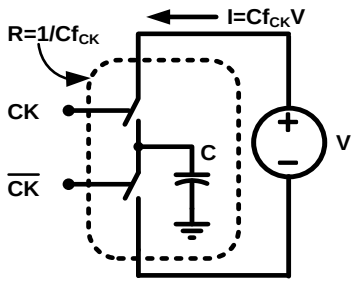


Fig. 5.3: Frequency-to-current conversion circuit.

5.3.2. *High Gain OTA*

Fig. 5.4 shows the schematic of the high gain telescopic Operational Transconductance Amplifier (OTA) used in each stage of the frequency synthesizer. The circuit was designed to operate at the nominal supply voltage of 0.9V. A low voltage internal bias circuit is used to keep every transistor in saturation mode under PVT variations. Input pair operates near threshold voltage region to achieve maximum gain. OTA voltage gain varies between 45dB at FF, 100°C to 50dB at SS, -40°C in simulation (which is equivalent to only 0.05% output frequency change) while consuming 10µA of static current.

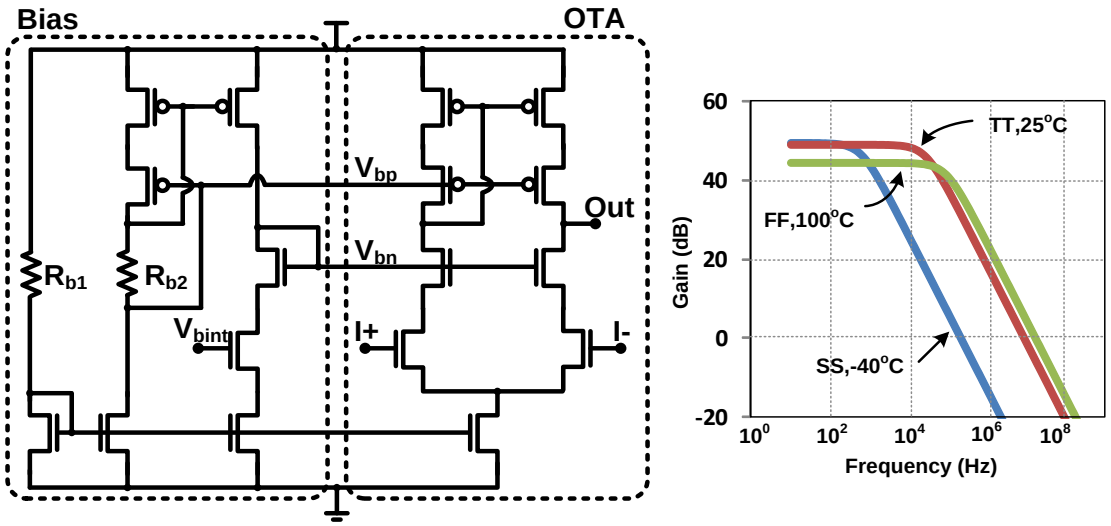
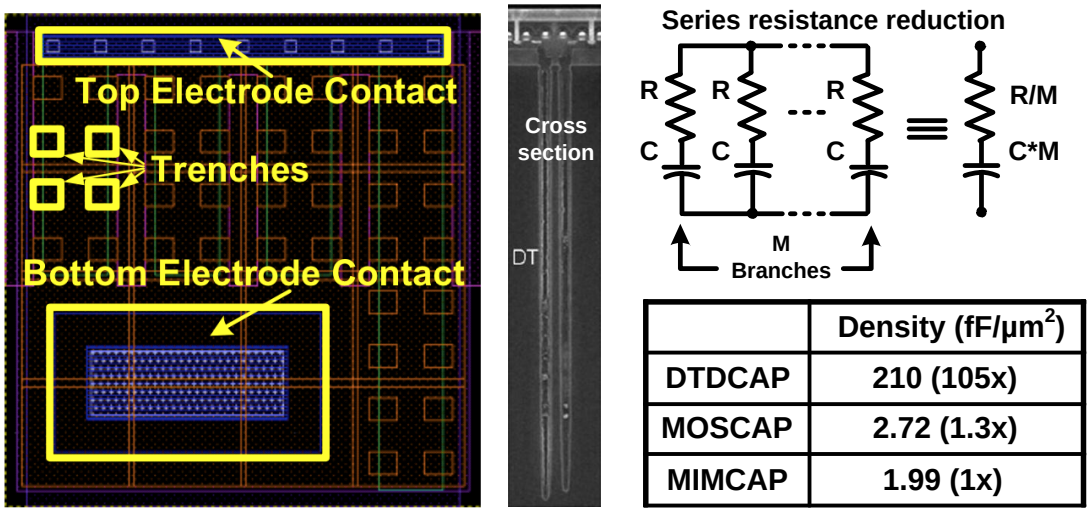


Fig. 5.4: High gain OTA schematic and simulated gain plot.

5.3.3. *Deep Trench Capacitor*

C_{1p} and C_{2p} of 50pF and 60pF respectively are used to ensure loop stability. A PLL of comparable bandwidth and output frequency range using the same VCO would require

at least 2nF loop filter capacitor for a 20μA charge-pump current [53]. Small capacitors (<10pF) are added at V_{1b} and V_{2b} nodes to remove high frequency switching noise. All capacitors (including C_1 and C_2) used in this design are based on deep trench capacitors (dtdcap) available in this process which are roughly 80X denser than standard MOS capacitors and hence significantly reduces area. Due to higher density, two capacitors can be placed very close to each other providing better matching and reducing parasitic. Leakage current is also lower than MOS capacitors due to thicker dielectric. Fig. 5.5 shows a cross-sectional view of the deep trench capacitor [54] along with a 4x4 deep-trench array layout. There is a parasitic series resistance associated with each trench capacitor that can be minimized by simply connecting multiple trenches in parallel.



	Density (fF/μm^2)
DTDCAP	210 (105x)
MOSCAP	2.72 (1.3x)
MIMCAP	1.99 (1x)

Fig. 5.5: Deep trench capacitor for area reduction.

5.3.4. *Voltage Controlled Oscillator (VCO)*

The VCO is a 5-stage current starved ring oscillator. Trans-conductance of this current source is made proportional to N in order to maintain a nearly constant loop gain for a wide output frequency range. However, TT corner simulation shows 5X change in VCO gain for 10X (16-156MHz) frequency change, due to large V_{ctr} variation.

5.4 Model for Loop Stability Analysis

The small signal model of the current multiplier based frequency synthesizer is shown in Fig. 5.6. Only stage 2 is considered here, as stage 1 operation will not be affected by the output frequency change. Small signal input (f_{in}) and output (f_{out}) frequencies are represented in terms of equivalent voltages, and FTCs are replaced by voltage controlled current sources. A(s) denotes the small signal ac gain of the OTA while G_m denotes the trans-conductance of the VCO current source which is made proportional to N (i.e $G_m=g_mN$) to keep the loop gain constant over the entire frequency range. F_{in} and F_{out} are the fixed input and output operating frequencies respectively. The comparator output's pole is made dominant by adding C_{2p}. The switched capacitor pair is represented by a resistor R with a value of $1/NF_{in}C_1$, which remains nearly constant at a given operating point of small signal analysis. R and C_{2b} (i.e. $Z_1(s)$) will create a non-dominant pole. $Z_2(s)$ is the input impedance of the VCO looking from the node V_{ctr}. It will also introduce another high frequency non-dominant pole. Expression for the low frequency small signal input current, output frequency and feedback current are as follows:

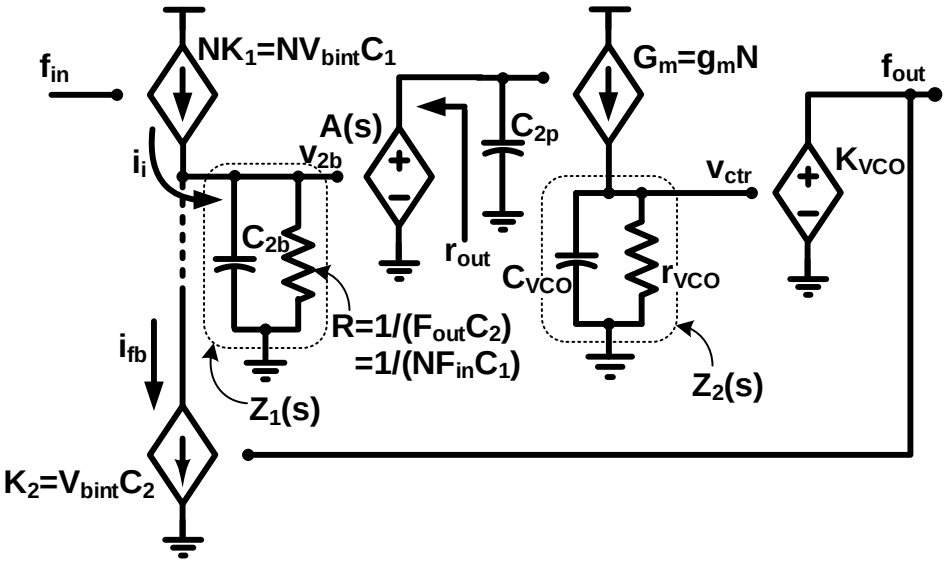


Fig. 5.6: Equivalent small signal model for loop stability analysis.

$$i_i = NV_{bint}C_1 f_{in} \tag{5.2}$$

$$f_{out} = G_m K_{VCO} A(s) Z_1(s) Z_2(s) i_i \approx \frac{G_m K_{vco} A(s) r_{VCO}}{NC_1 F_{in}} i_i \tag{5.3}$$

$$i_{fb} = V_{bint} C_2 f_{out} \tag{5.4}$$

Therefore, open-loop gain can be calculated as:

$$\left.\frac{i_{fb}}{i_i}\right|_{OL} = \frac{V_{bint} C_2 f_{out}}{NV_{bint} C_1 f_{in}} = \frac{C_2}{C_1} \frac{g_m K_{vco} A(s) r_{VCO} V_{bint}}{F_{in}} \tag{5.5}$$

If $A(s)=A/(1+s/\omega_{3dB})$, where ω_{3dB} is 3dB bandwidth of OTA, close-loop frequency transfer function is given by:

$$\left.\frac{f_{out}}{f_{in}}\right|_{CL} = N\frac{C_2}{C_1}\left.\frac{i_{fb}}{i_i}\right|_{CL} = N\frac{C_2}{C_1}\frac{G_0}{1+G_0}\frac{1}{1+\frac{s}{\omega_{3dB}(1+G_0)}} \tag{5.6}$$

G_0 is the dc open-loop gain obtained from eq. (5.5) for A(s)=A. $\omega_{3dB}G_0$ is the unity gain bandwidth (UGB). The steady-state frequency error can also be calculated as:

$$\left.\frac{\Delta f_{out}}{f_{in}}\right|_{s\to 0} \approx \frac{1}{G_0} = \frac{1}{\frac{C_1 g_m K_{vco} A r_{VCO} V_{bint}}{C_2 \quad F_{in}}} \tag{5.7}$$

Hence, depending on the frequency accuracy requirement, circuit parameters can be tuned. Loop gain and phase response of the model for maximum and minimum operating frequencies are plotted in Fig. 5.7 showing the phase-margin. Loop gain is 65dB and bandwidth varies between 200 – 500 kHz for a frequency variation between 16-156MHz.

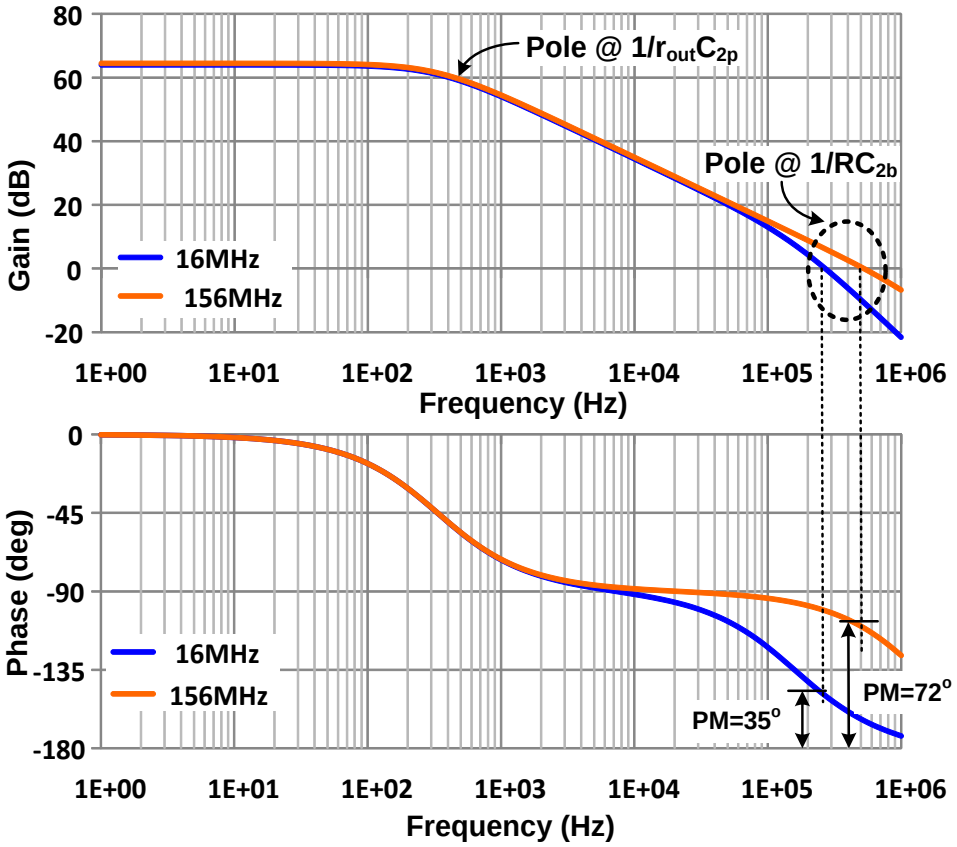


Fig. 5.7: AC simulation plot of loop model.

Transient start-up simulation of the actual circuit is shown in Fig. 5.8 for an output frequency of 76MHz. Stage 1 initially takes 5µs to settle and stage 2 takes 3.5µs to reach the desired frequency. Settling time can be reduced further by increasing the loop bandwidth.

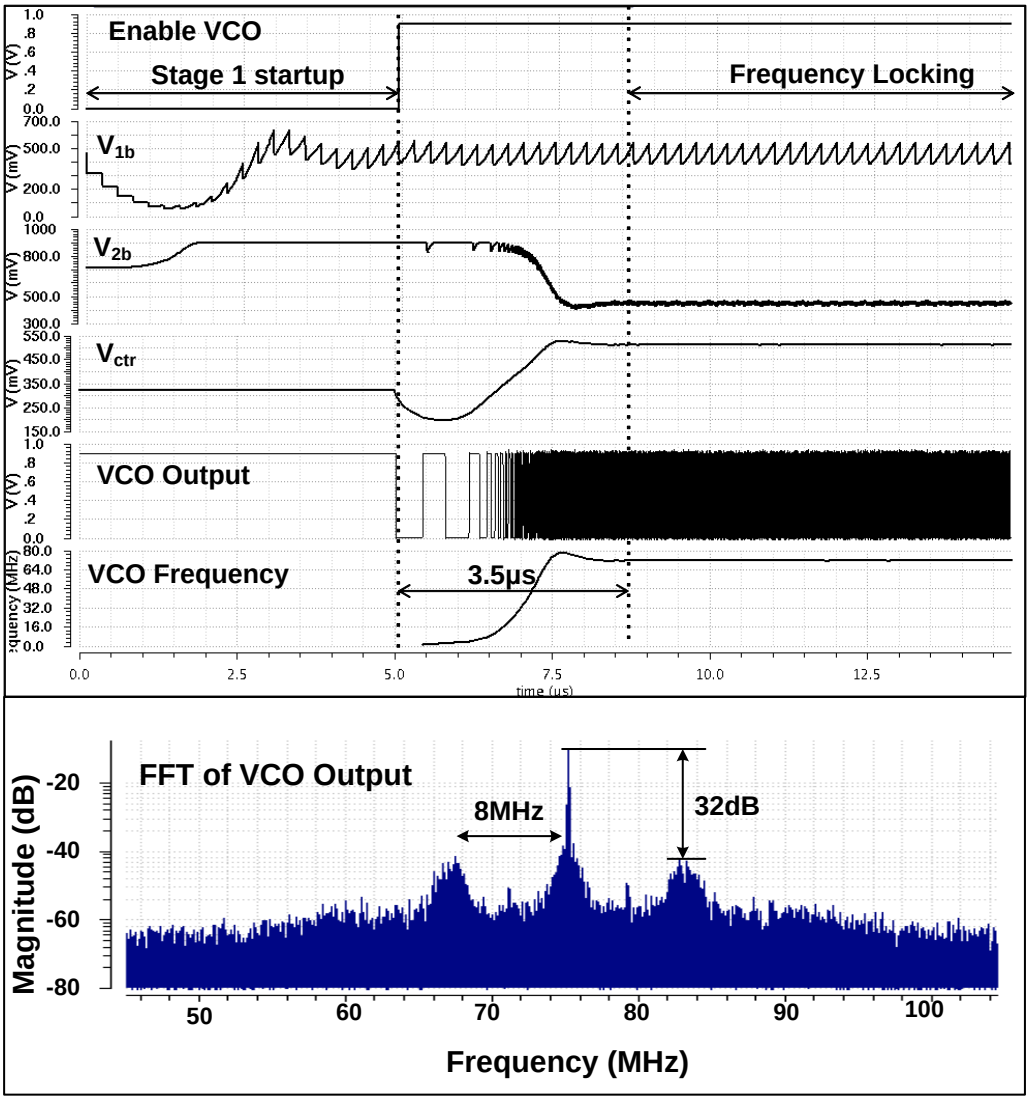


Fig. 5.8: Frequency synthesizer transient response and output FFT (simulation).

5.5 In-situ Periodic Jitter Measurement Circuit

An in-situ periodic jitter measurement circuit is implemented using the concept of bit error rate (BER) measurement [56]. Fig. 5.9 shows the proposed jitter measurement

circuit. Timing error is detected by the BER monitor when the programmable delay is longer than the instantaneous clock period. A BER plot is obtained by sweeping this delay precisely by changing its supply voltage V_{DD_SEP} and calculating the average time period of the divided output clock BER<n>. Error detection is similar to other on-chip measurement scheme [58]. However the off-chip time period calculation gives much accurate BER value, as it is no longer limited to the maximum count of the on-chip counter. Slope of this curve gives the RMS periodic jitter (measured BER plot shown later in Fig. 5.13). The programmable delay is measured by connecting it in ring oscillator fashion (i.e. EN_RO=1) and measuring its frequency.

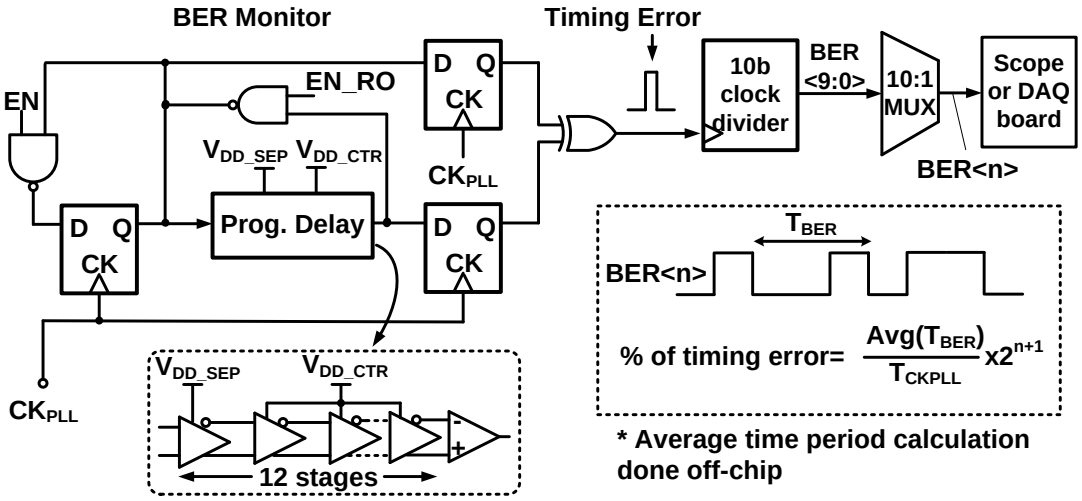


Fig. 5.9: In-situ periodic jitter measurement circuit [56].

5.6 Measurement Results

A test chip is implemented in 0.9V, 32nm SOI technology to demonstrate the performance of the proposed frequency synthesizer under PVT variations. Die photo and

core layout are shown in Fig. 5.10 indicating a core area of 0.0054mm^2. The frequency synthesizer core consumes 116µW and 209µW at 48MHz and 76MHz, respectively.

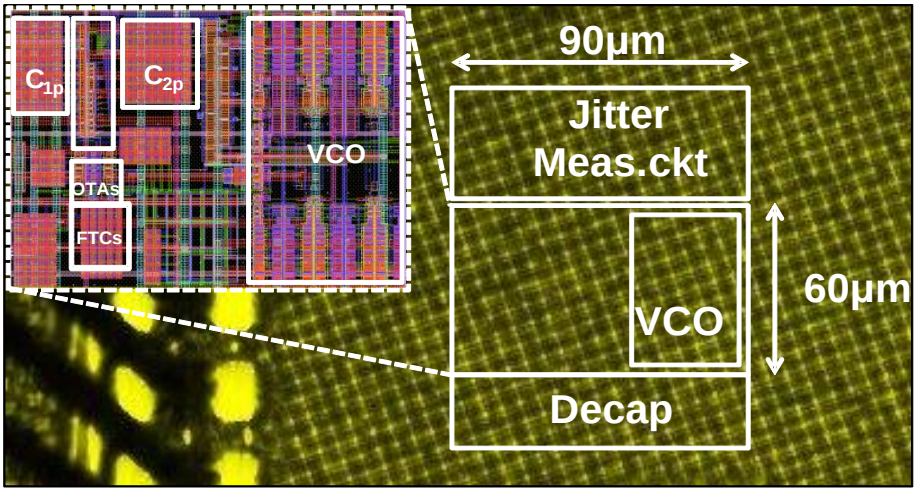


Fig. 5.10: 32nm test chip die photo and core layout.

Measured output frequencies and corresponding systematic offset are shown in Fig. 5.11. One time process trimming is required at each frequency point to minimize this systematic offset. Frequency resolution of $F_{in}/5$ i.e. 0.8MHz for 4MHz input clock is achieved by precisely controlling current multiplication factor (N).

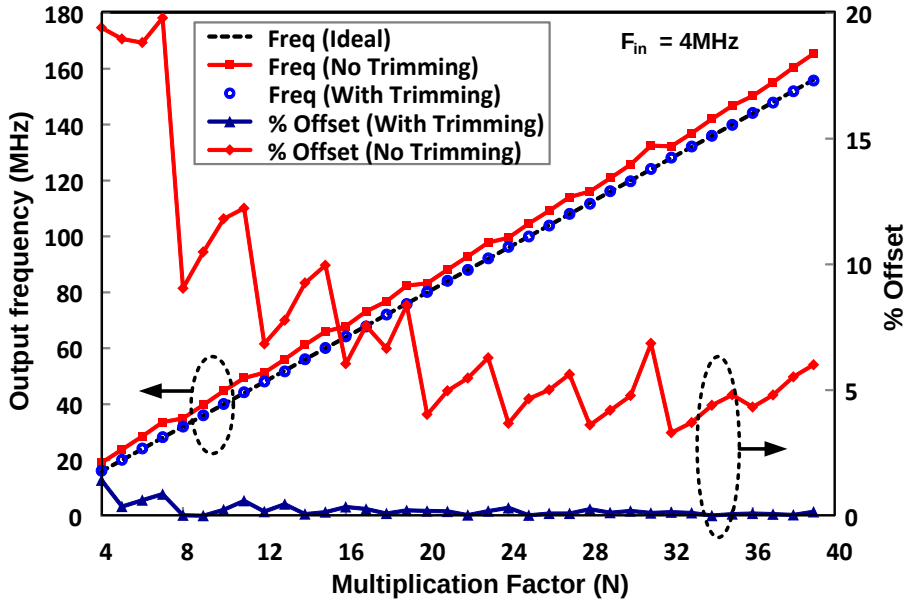


Fig. 5.11: Process trimming results.

Fig. 5.12 compares measured voltage and temperature dependency of the frequency synthesizer (i.e. close-loop) with the free running open-loop VCO. Close-loop shows only ±0.22% frequency variation compared to ±13% frequency variation of free running oscillator for 100mV supply variation. Frequency spread due to temperature sweep from -40^{o}C to 90^{o}C is ±0.14% i.e. 21ppm/^{o}C for close-loop and ±7% i.e. 1076ppm/^{o}C for open loop oscillator. Maximum spread is 70ppm/^{o}C at 150MHz measured over entire frequency range.

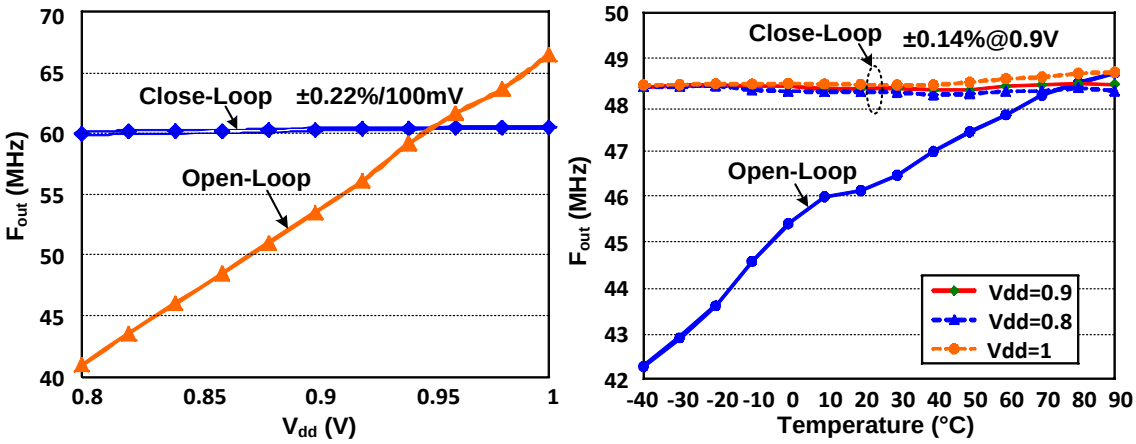


Fig. 5.12: Measured voltage and temperature dependency.

Fig. 5.13 shows the BER plot and its slope obtained from on-chip jitter measurement circuit at 76MHz. First programmable delay is measure for different V_{DD_SEP} and V_{DD_CTR} by connecting the delay in ring oscillator mode. Finally BER is calculated for different delays. RMS periodic jitter is 115ps i.e. 0.88% of time period, obtained by Gaussian curve fitting on the measured data. Fig. 5.14 compares the performance with other clock generators. Figure-of-merit (FoM) [50] is 2.4µW/MHz calculated at 48MHz.

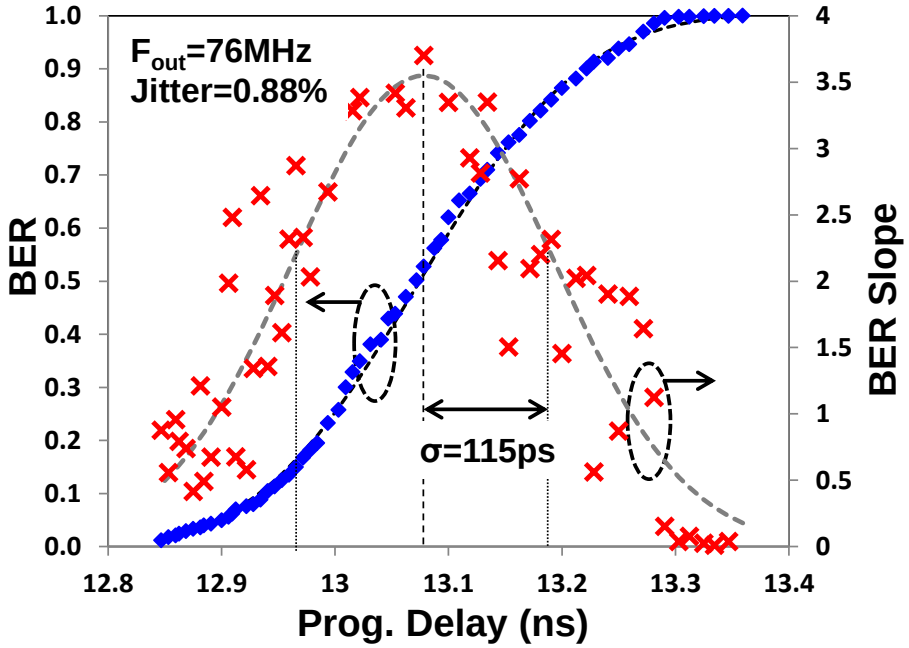


Fig. 5.13: BER and periodic jitter from on-chip jitter measurement block.

Parameters	This Work	Jee ISSCC'13	Ueno ESSCIRC'09	Smedt JSSC'09	Lee VLSI'09
Technique	Freq.-to-Curr. ROSC	Leakage ROSC MDLL	Temp. comp. Resistor	Wienbridge oscillator	Temp. comp. Feedback
Technology	32nm SOI	65nm	0.35µm	65nm	180nm
Frequency	48MHz (16- 156 MHz)	3.2MHz	30MHz (2- 100MHz)	6MHz	10MHz
Ref. Freq.	4MHz	32kHz	-	-	-
Temp. Coefficient	22ppm/°C (-40° to 90°C)	None	90ppm/°C (-40° to 100°C)	86ppm/°C (0° to 100°C)	57ppm/°C (-20° to 120°C)
Voltage Regulation	3.6%/V	None	4%/V	NA	0.06%/V
Start- up Time	8.5µs	~400µs	2.5µs	NA	NA
RMS Period Jitter[%]	1.27%	2.5%*	NA	NA	NA
Power (µW)	116	0.42	180	66	80
FoM (µW/MHz)	2.4	0.132	6	11	8
Chip area (mm^2)	0.0054	0.026	0.08	0.03	0.22

*10kHz to 1MHz integrated rms jitter

Fig. 5.14: Performance comparison.

Fig. 5.15 compares FoM with state-of-the-art on-chip clock generators of comparable frequencies. 4 different samples were tested to verify the stability with chip-to-chip variation.

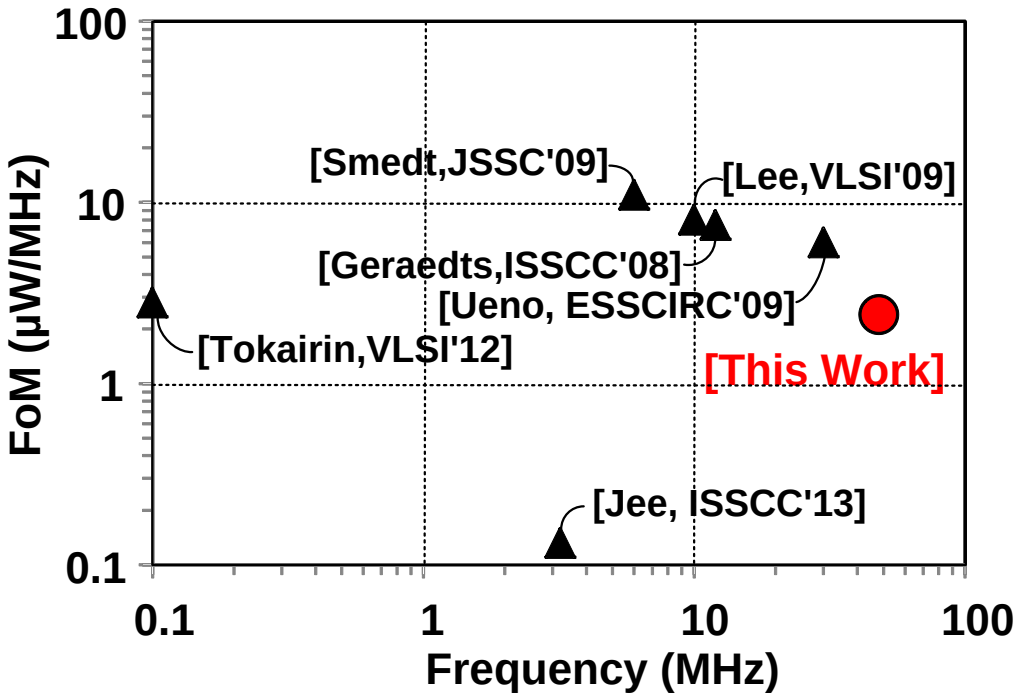


Fig. 5.15: FoM comparison with other clock generators.

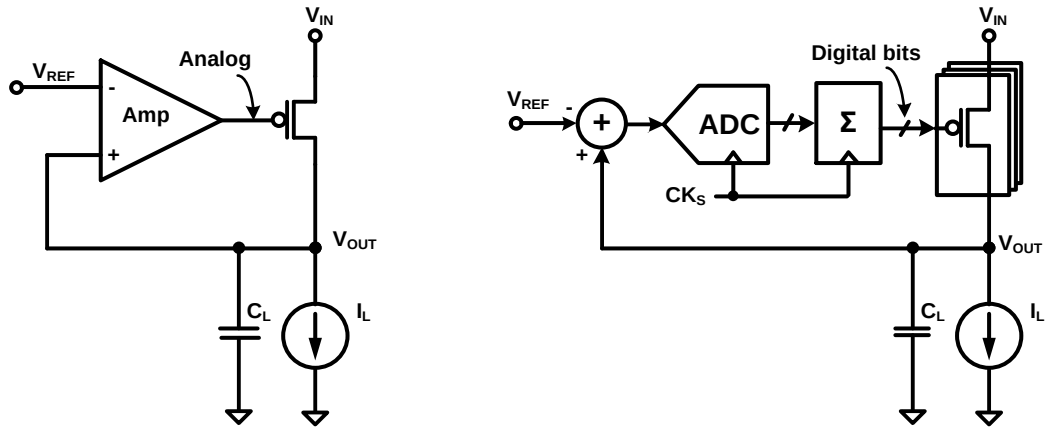
Chapter 6. Time-based Adaptive Digital Low Dropout Regulator

6.1 Introduction

The design of multi-core systems and system-on-chips with multiple voltage domains become essential to reduce the power consumption by individually controlling the supply voltage of each core based on its workload, which is also known as dynamic voltage and frequency scaling (DVFS). However, this necessitates the requirement of a highly efficient integrated voltage regulator with not only fine grain power delivery over a wide load current dynamic range and input/output voltage, but also spatial and temporal control of performance and power dissipation. The design of conventional analog low dropout (LDO) regulators [59] poses several challenges in order to meet all these power delivery constraints. Therefore, the implementation of all digital LDOs is recently explored [60] – [65] due to their compactness, process scalability, immunity to PVT variations and easy programmability for design optimization under different operating conditions.

A conventional analog LDO shown in Fig. 1(a) consists of an operational amplifier and a power transistor. High gain analog loop keeps V_{OUT} close to the desired reference voltage, V_{REF} for different load current. With the decreasing supply voltage, the design of the high gain amplifier becomes increasingly difficult under a wide variation in load

current and input/output voltages. This has motivated the design of digital LDOs (DLDO). A discrete-time implementation of DLDO typically consists of an analog-to-digital converter (ADC), a digital accumulator and a digitally controlled output stage [61]. The ADC converts the error voltage i.e. $V_{OUT} - V_{REF}$ to digital bits. The digital accumulator integrates the digital error bits in every cycle of the sampling clock (CK_s). The digital accumulator makes the low frequency loop gain infinity at DC. The output bits of the accumulator control the transistor switch arrays in the output stage that needs to be turned on for a given V_{OUT} and load current (I_L). The output stage therefore acts as a resistance controlled digital-to-analog converter (DAC). The gain of the accumulator is controlled to optimize the design in terms of stability and settling time.



(a) **(b)**

Fig. 6.1: Low dropout regulator circuit: (a) Analog, (b) digital. Analog error-amplifier is replaced by an ADC followed by an accumulator in digital implementation.

Previously proposed DLDO implementations [60] – [64] uses a 1-bit comparator or ADC and a fixed sampling clock for the loop operation. Although a 1-bit comparator is easy to design, it requires many clock cycles to reach the steady state, requiring a high

frequency sampling clock for faster settling. However, the selection of sampling clock frequency is critical, as it directly impacts the DLDO performance. Higher sampling speed reduces the settling time of the loop, but at the cost of high switching power consumption and it makes the ADC design more challenging at the same time. In addition to that, increasing sampling frequency moves the open-loop pole closer to the unit circle in the discrete or z-domain causing stability issues [65]. This limits the maximum sampling frequency to be nearly five times of the DLDO bandwidth. To address the trade-off among settling-time, stability and dynamic power consumption, the technique proposed in [62] uses multiple VCOs for sampling purposes and it requires additional detection circuit and control logic to enable the appropriate VCO depending on the output droop/overshoot. [64] proposes a coarse-fine-tuning technique, which is again controlled by a droop/overshoot detection circuit. However, introduction of additional detection circuitry and control blocks in these techniques increases the design complexity and the power consumption.

In this work, a time-based quantizer using a pair of VCOs is utilized for digital intensive implementation of the ADC. Multi-bit output of the ADC provides settling in a fewer clock cycles than a 1-bit comparator. This relaxes the sampling clock frequency significantly. As a result the stability of the DLDO can be ensured over a wide operating conditions. The dynamic power consumption due to switching is also reduced, increasing the efficiency of the DLDO. The frequency of the VCOs can also be tuned to optimize the efficiency depending on the load current. For example, the VCO operating frequency can be set to a lower value to reduce the power consumption, when the load current is

small. On the other hand, high VCO frequency is essential to minimize the droop due to large change in instantaneous load current and also for faster settling. Moreover, the beat-frequency technique for quantizer implementation enables adaptive control of the sampling frequency depending on the amount of voltage droop or overshoot in V_{OUT}. This also reduces the settling time significantly. The inherent active voltage-positioning (AVP) feature due to the offset voltage under steady state condition helps to reduce the peak-to-peak transient variations in V_{OUT} due to load current change.

The design of the proposed time quantizer based DLDO is described in section 6.2. Active voltage positioning technique is illustrated in section 6.3 followed by the circuit implementation details in section 6.4. Section 6.5 summarizes the simulation results and section 6.6 concludes the discussion.

6.2 Proposed Time Quantizer based Adaptive Digital LDO

A time-based quantizer is utilized for fully digital implementation of ADC without requiring analog comparators for digital output bits generation. A pair of VCOs, as shown in Fig. 6.2, converts the voltages (V_{REF}, V_{OUT}) to equivalent clocks (CK_{REF}, CK_{OUT}) of proportional frequency and the digital time quantizer calculates the frequency difference between them to generate digital codes. The operation is similar to a frequency-locked loop (FLL). Fig. 6.3 explains the conventional linear quantizer [16] and the beat-frequency based quantizer [10, 14, 15]. In case of a linear quantizer, a counter counts the number of clock cycles of the signal clock (CK_{OUT}) in each sampling period (CK_s), which is generated by dividing the output frequency of a reference oscillator. If the frequency division factor is N, the output count $N_{OUT}=Nf_{OUT}/f_{REF}$, where f_{OUT} and f_{REF}

are the frequencies of signal and reference VCOs respectively, is proportional to the signal frequency f_{OUT}. Therefore, N_{OUT}=N when two frequencies are equal. Since two VCOs are identical, the impact of PVT variations will be same for both, without affecting the performance of the DLDO significantly. Higher N improves the ADC resolution and reduces switching power, but makes the loop response slower due to low sampling clock frequency.

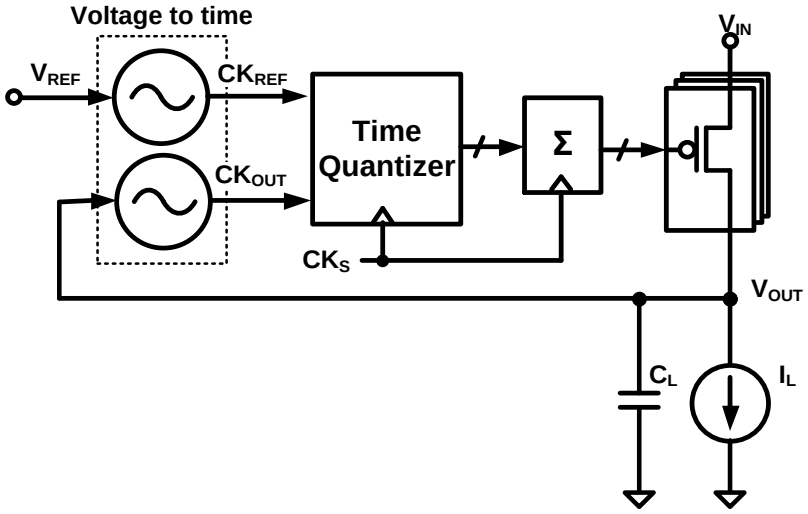
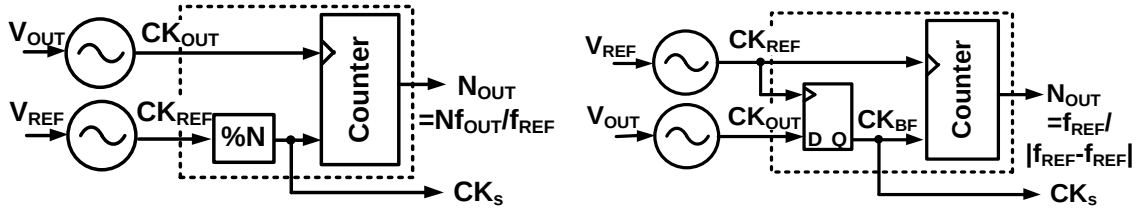


Fig. 6.2: Time quantizer based digital LDO. VCO is used to convert the voltage into time domain.

Proposed beat-frequency based time-quantizer or BF quantizer generates a sampling clock with dynamically adaptive clock frequency. Fig. 6.3 (b) explains the implementation of the BF quantizer. A DFF generates the beat frequency (CK_{BF}) between two input frequencies ($f_{BF}=|f_{REF}-f_{OUT}|$), which is used as the sampling clock of the DLDO. The counter counts the number of reference period in each CK_{BF} period, generating an output $N_{OUT}=f_{REF}/|f_{REF}-f_{OUT}|$. Therefore, for a specific N, a fixed offset of f_{REF}/N is created at the quantizer input under steady state. During the occurrence of voltage

droop/overshoot, frequency difference increases, increasing the sampling clock frequency for faster settling. However, in steady state condition, the difference is very small reducing the sampling clock frequency. This improves the quantizer resolution to lock the output voltage very precisely and at the same time reducing the switching power consumption.



(a) **(b)**

Fig. 6.3: Implementation of the time quantizer. (a) Conventional linear quantizer, (b) proposed beat frequency based quantizer. Beat frequency quantizer can generate dynamically adaptive sampling clock frequency.

Simplified block diagram of the proposed beat-frequency quantizer based DLDO is shown in Fig. 6.4. The output code of the BF quantizer is compared with external code N, so that during steady state N_{OUT} settles to N generating fixed voltage offset ($\Delta V=V_{OUT}-V_{REF}$). As the BF quantizer is unable to detect the polarity of the two inputs, ΔV can be positive or negative depending on the initial state of V_{OUT}. For example, when a droop occurs, as illustrated in the timing diagram of Fig. 6.4, V_{OUT} goes below V_{REF} generating a negative ΔV in steady state. It also shows how the sampling frequency is modulated for faster recovery of the droop.

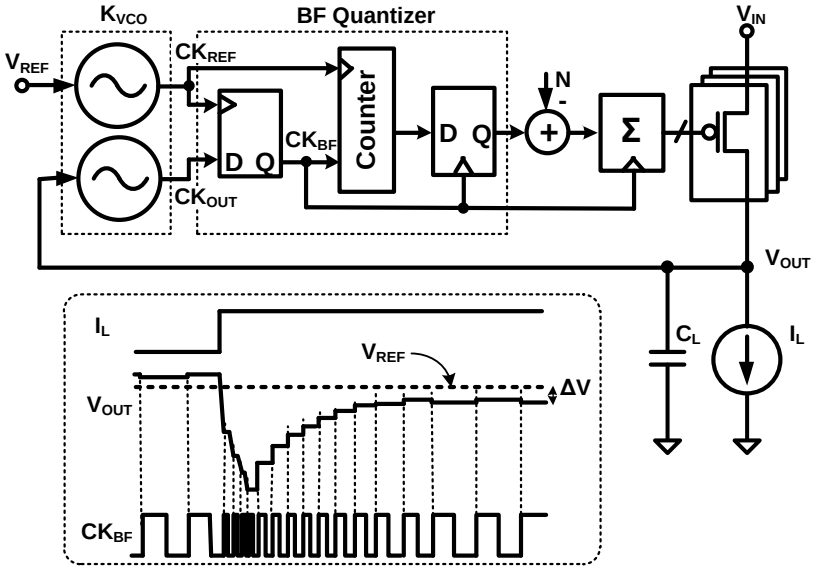


Fig. 6.4: Proposed beat frequency quantizer based all digital LDO having dynamically adaptive sampling clock frequency depending on the amount droop in V_{OUT}.

6.3 Active Voltage Positioning

Transient variation or ripple in power supply is one of the key performance parameters in a voltage regulator. In order to reduce the output ripple during voltage transients due to load step, 'active voltage positioning' (AVP) is commonly used [66]. In this technique, the regulator is intentionally made imperfect by adjusting the output voltage depending on the load current. In other words, the steady state or DC regulation is compromised to significantly improve the transient deviation. Simple waveforms in Fig. 6.5 show how AVP reduces the peak-to-peak output excursion for the same amount of droop or overshoot due to load step. At minimum load, V_{OUT} is set at a slightly higher voltage than its nominal value. Similarly, at maximum load, V_{OUT} is slightly lower than nominal value. During minimum to maximum load transition, output starts dropping from

higher voltage and settles at a lower voltage than nominal. As a result the effective droop in supply from its nominal value is reduced.

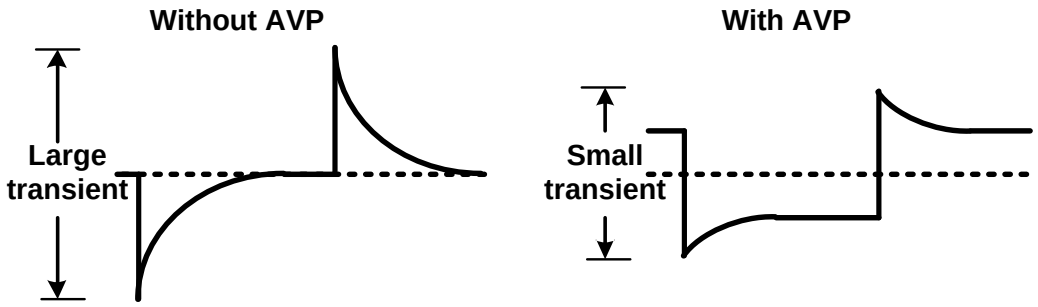


Fig. 6.5: Active voltage positioning (AVP) to reduce the transient variation in V_{OUT} [66].

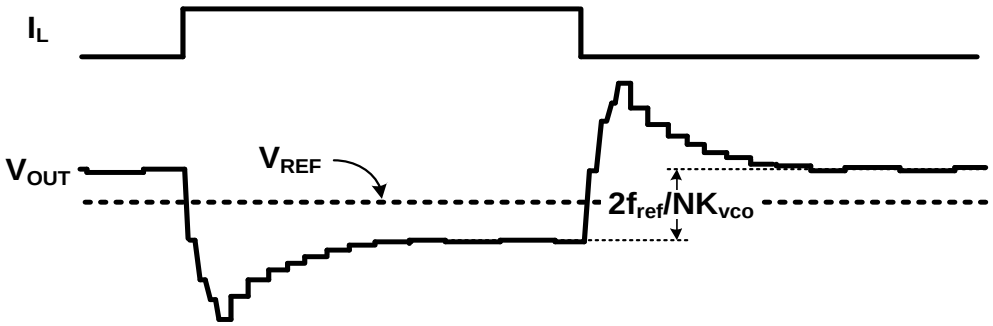


Fig. 6.6: Fixed voltage offset in steady state provides inherent AVP. ΔV can be easily tuned by controlling the value of N.

In BF quantizer based digital LDO implementation; a fixed voltage offset in steady state condition, as mentioned previously, provides inherent AVP for ripple reduction. During minimum to maximum load current (I_L) transition V_{OUT} settles to a slightly lower than nominal voltage of V_{REF}. The offset voltage generated between V_{OUT} and V_{REF} is:

$$\Delta V = \frac{f_{ref}}{NK_{vco}} \tag{6.1}$$

Here f_{ref} is the reference VCO frequency of gain K_{vco}. ΔV can be flexibly controlled by the external code N depending on the maximum and minimum load current.

6.4 Circuit Implementation Details

Fig. 6.7 illustrates the architecture of the proposed time-based DLDO design implemented in a 65nm CMOS technology. It comprises of the conventional linear quantizer as a baseline and the proposed BF quantizer, to compare the performances while keeping all parameters identical. The output bits of the quantizer is compared with the external code N and the difference goes to a 10-bit accumulator to control 1024 number of PMOS resistors at the output stage to keep V_{OUT} nearly constant irrespective of the load current. As the BF quantizer detects the absolute voltage difference (ΔV) between V_{REF} and V_{OUT}, loop feedback becomes positive when ΔV changes its polarity. Therefore, during BF quantizer operation a digital comparator is used to detect the voltage polarity and to keep the loop always in negative feedback configuration irrespective of the polarity of ($V_{REF} - V_{OUT}$).

The circuit implementation details of different building blocks of the DLO are explained below.

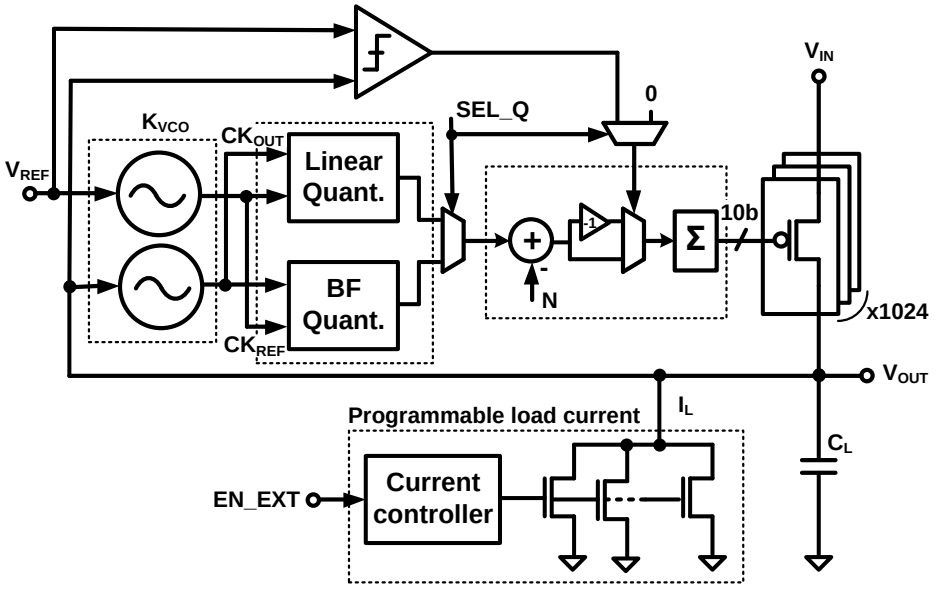


Fig. 6.7: The schematic of the proposed time-based digital LDO circuit with programmable load current. Both the linear and the BF quantizer are included for performance comparison.

6.4.1. *Voltage Controlled Oscillator*

Fig. 6.8 (left) shows the design of the VCO. It is composed of a voltage-to-current converter followed by a 5-stage ring oscillator based current-controlled oscillator (CCO). A 3-bit coarse tuning, by controlling the number of tri-state inverter in each stage of the ring oscillator, achieves wide tuning range to control the VCO frequency depending on the load current to maximize efficiency [62]. The 4-bit switched capacitor branches perform the fine frequency tuning in order to minimize any frequency variation between two VCOs due to device mismatch. A part of the CCO current is dependent on the input control voltage (V_{ctr}), while the remaining portion is kept fixed to ensure output oscillation during DLDO start-up. The VCO frequency-tuning plots for different coarse code are shown in Fig. 6.8 (right).

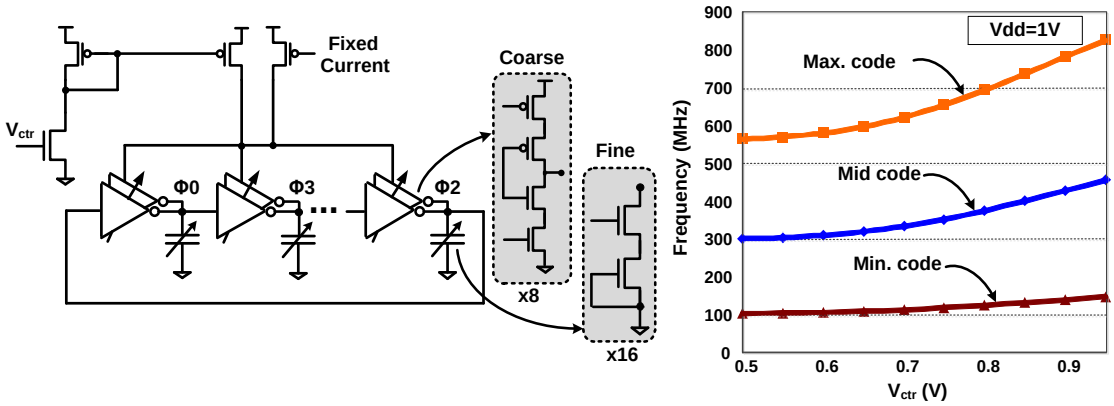


Fig. 6.8: Voltage controlled oscillator schematic (left) and post-layout tuning range simulation (right).

6.4.2. *Uniformly Distributed PMOS Switch Array in Output Stage*

1024 PMOS switch arrays controlled by 10-bit binary codes (C[9:0]) form the output stage of the DLDO. Since each of these switches acts as a resistor, matching is critical to reduce any device-to-device mismatch and parasitic resistance mismatch due to additional metal routing while connecting the source and drain nodes. This is taken care of by a uniformly distributed layout design as evident from Fig. 6.9. Entire area is divided into 4x4 subgroups each having 32 branches controlled by C[9], 16 branches by C[8] and so on. Multiple dummy transistors are also added to keep the layout uniform as well as to match the loading of all bits.

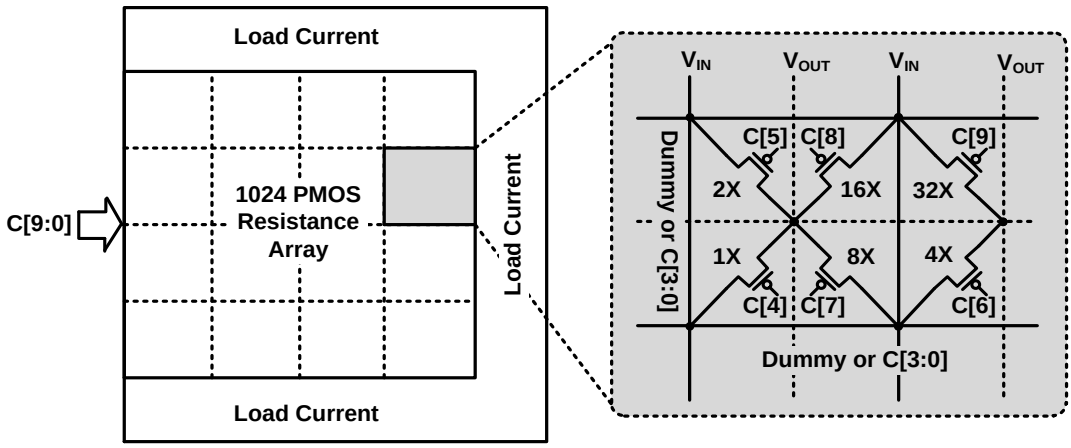


Fig. 6.9: The uniform distribution of 1024 PMOS resistors.

6.4.3. *Programmable On-chip Load Current*

In order to verify the operation of the DLDO over a wide operating condition, an on-chip programmable load current block with varying magnitude and rise/fall time is incorporated. An NMOS transistor based load current unit elements are designed. The current flowing though each elements and the total number of such elements are made programmable for a wide variation in load current. While some elements provide a fixed minimum load current, remaining elements are sequentially turned on/off using a test oscillator, as shown in Fig. 6.10. Frequency of the test oscillator and the number of shift register stages control the magnitude of the total load current and its rise and fall time. Test oscillator frequency varies between 12-to-800MHz and the number of shift-register stages are made programmable between 12-to-96. As a result the load current can vary between 1mA to 400mA and its rise time can also be controlled between 15ns to 8µs.

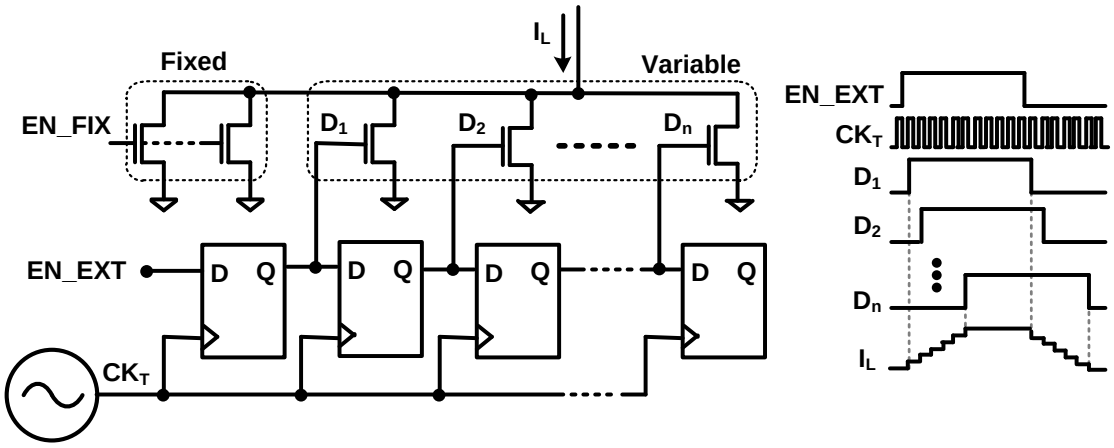


Fig. 6.10: Implementation of the on-chip programmable load current. A test VCO and a chain of shift register stages control the magnitude of the load current and its rise/fall time.

6.5 Simulation Results

The DLDO circuit is implemented in a 65nm LP CMOS process and simulations are performed to verify the proposed techniques. The load current that the DLDO can provide is dependent on the PMOS switch resistance in the output stage and the dropout voltage i.e. $V_{IN}-V_{OUT}$. The load current expression is as follows:

$$I_L = \frac{V_{IN}-V_{OUT}}{R_{ON}} \tag{6.2}$$

R_{ON} is the resistance of the output stage when a given number of PMOS switches are on. The minimum resistance of the output stage i.e. when all 1024 branches are on decides the maximum load current. Simulated load current for different V_{IN} and V_{OUT} are plotted in Fig. 6.11. Therefore, the load current should be within this calculated range for the DLDO operation. For example, when V_{IN} is 1V, output load current should be within 10mA to 165mA for desired V_{OUT}=0.9V.

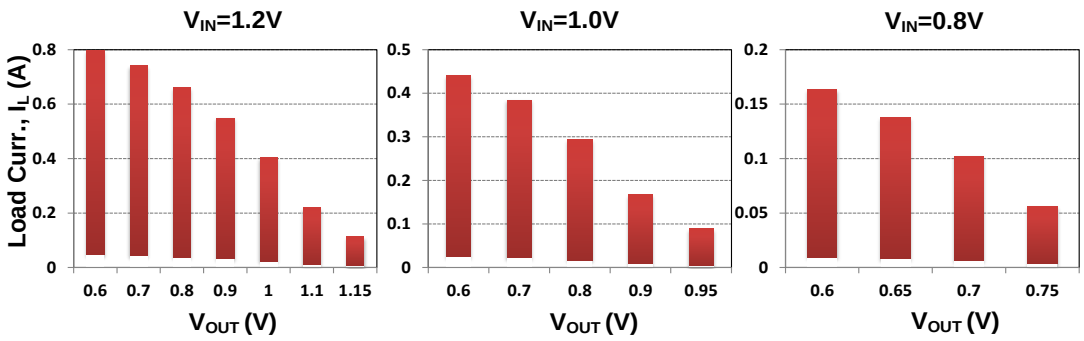


Fig. 6.11: Simulated load current requirement for DLDO operation for different V_{IN} and V_{OUT}. Maximum load current is decided by the minimum resistance i.e. when all 1024 PMOS branches are on in the output stage.

Fig. 6.12 shows the transient response for a step in V_{REF} from 850mV to 950mV. The load current is fixed at 30mA. As evident, the sampling frequency automatically goes to a high value due to large voltage difference between V_{REF} and V_{IN}. This helps in faster settling. The settling time is 5µs while operating VCOs at 300MHz. Fig. 6.13 (left) shows the load regulation behavior for a load current change of 50mA. For a large load current i.e. 80mA in this case, V_{OUT} settles at 7mV lower voltage than V_{REF}, but goes back to 7mV higher than V_{REF} when load current is 30mA. This verifies the AVP behavior. Line regulation is simulated for a 100mV step in V_{IN} for a fixed load current at 40mA and results are plotted in Fig. 6.13 (right).

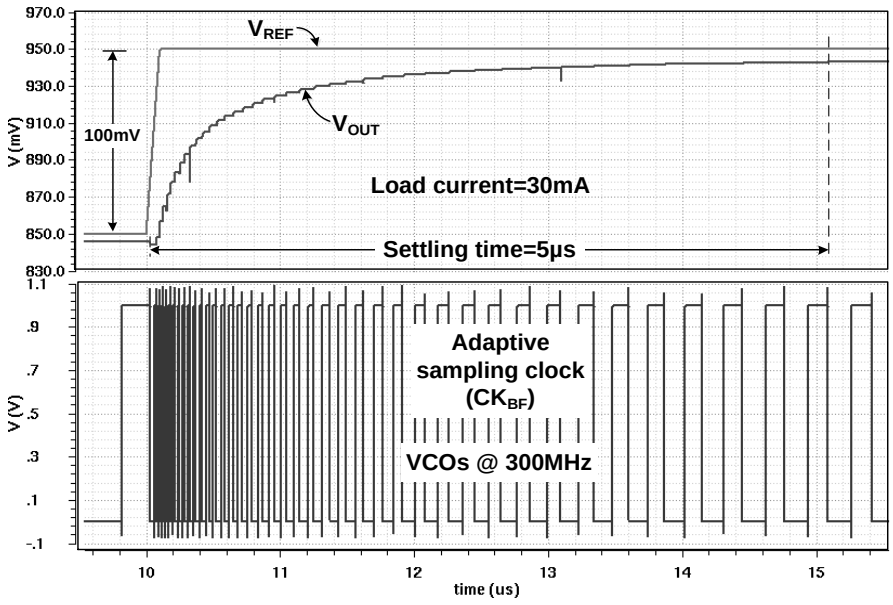


Fig. 6.12: Transient response of the DLDO for a step in V_{REF}. Load current is fixed at 30mA and VCOs operate nearly at 300MHz.

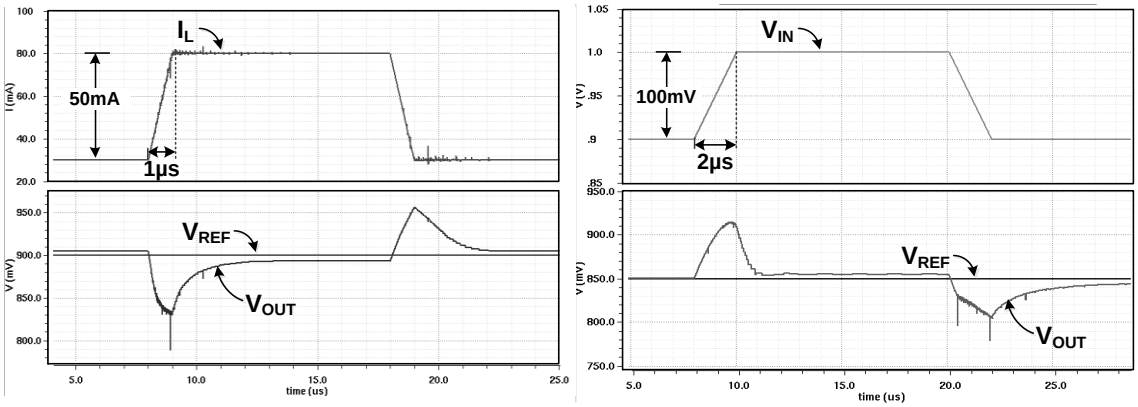


Fig. 6.13: Simulated load regulation (left) and line regulation (right).

The frequency of the VCOs can also be tuned to adjust the settling time and voltage transients. As shown in Fig. 6.14 the voltage droop reduces from 110mV to 54mV and settling time from 6µs to 1.95µs when VCO operating frequency is increased from 120MHz to 1120MHz. However this reduction in voltage droop and settling time can be

achieved at the cost of higher VCO power consumption increases DLDO quiescent current consumption (I_Q) that will eventually affect the regulator efficiency.

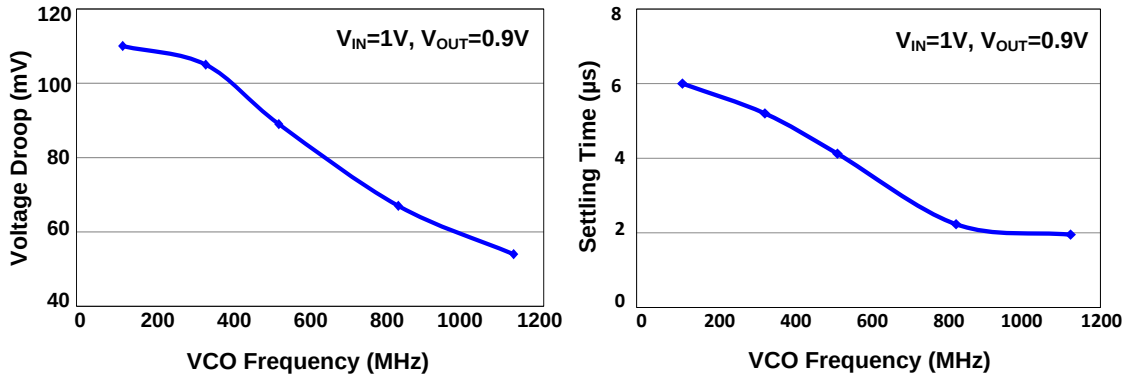


Fig. 6.14: Voltage droop and settling time plot for different VCO frequencies for a load current step from 30mA to 80mA within 500ns. Higher VCO frequencies reduces settling time and droop, but at the cost of increased power consumption.

Current efficiency, which is the ratio of load current to total current, is plotted in Fig. 6.15 for a load current variation from 1mA to 100mA at three different frequencies. Higher VCO frequencies although improve the settling and voltage transient variations, but affects the current efficiency. Therefore, VCO frequencies can be adjusted depending on the load current conditions: low, normal or high, as indicated in the plot, for optimum performance under a wide variation in load current. Power efficiency is also calculated by sweeping V_{OUT} from 0.5V to 0.95V for V_{IN}=1V and I_L=30mA. VCO frequency is 340MHz for V_{OUT}=0.9V. Results are plotted in Fig. 6.16. The core layout with active area of 110µmx350µm is shown in 6.17. A performance summary table is also provided.

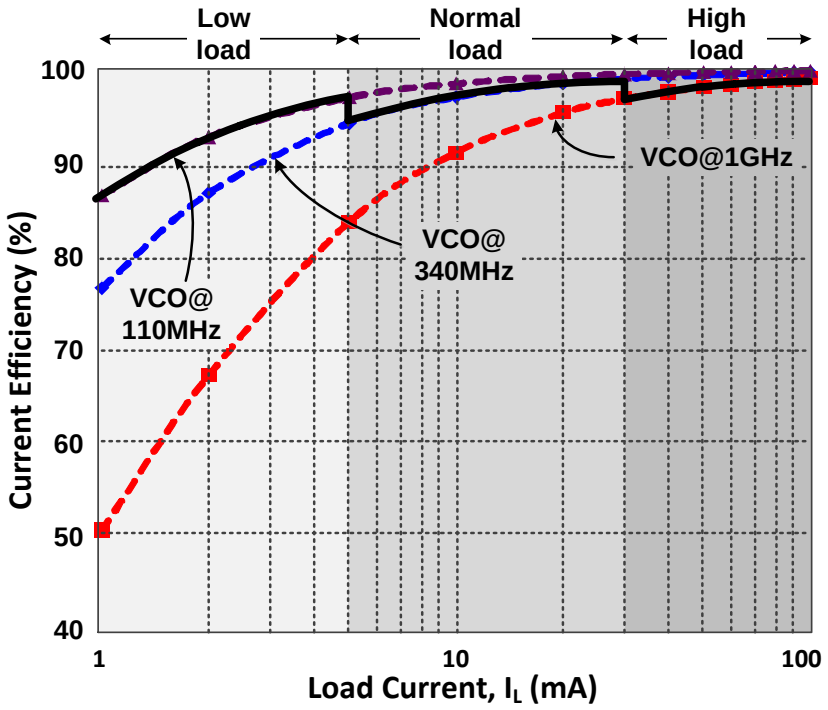


Fig. 6.15: Current efficiency plot for a load current sweep from 1mA to 100mA using three different VCO frequencies. VCO frequency can be adjusted depending on the load current.

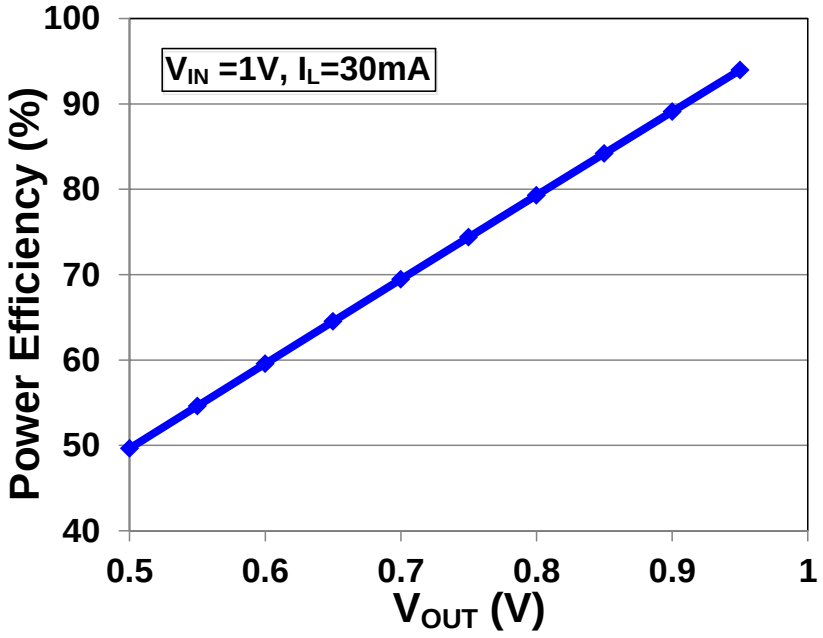
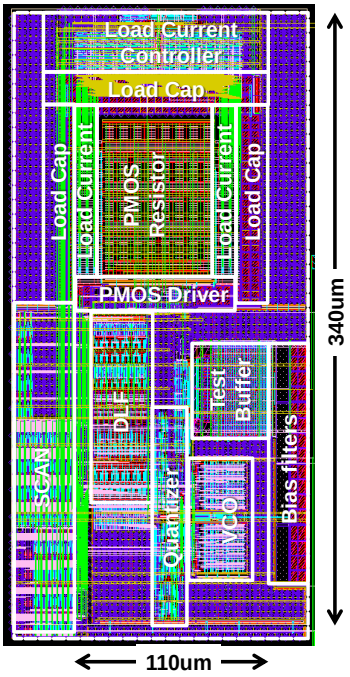


Fig. 6.16: Power efficiency as a function of V_{OUT}. V_{IN} and I_L are fixed at 1V and 30mA respectively. VCO frequency is 340MHz when V_{OUT}=0.9V.



Result Summary	
Technology	65nm
V_{IN} range	0.6 – 1.2V
V_{OUT} range	0.5 – 1.15V
Max. I_{LOAD}	100mA
I_Q	350 – 600µA
Max. Current Efficiency	99.4%
Max. Power Efficiency	95.2% @ I_{LOAD}=100mA
Active Area	110µmx340µm

Fig. 6.17: Core layout and performance summary of the DLDO.

6.6 Conclusion

This work presents a digital low dropout regulator having dynamically adaptive sampling clock frequency depending on the output voltage transient response to achieve faster settling, low droop/overshoot and low steady-state quiescent current consumption at the same time. A beat frequency detection mechanism is incorporated to generate the dynamically adaptive sampling clock. Steady state voltage offset provides inherent active voltage positioning to reduce large transient voltage ripples during load variation. An on-chip current generator provides load current that can be varied over a wide range and the rise/fall times are also made programmable to verify the DLDO functionality in different operating conditions. The regulator circuit is implemented in a 65nm CMOS technology. It can operate in a wide output voltage (0.5V – 1.15V) and load current (1mA – 400mA)

range. The VCO operating frequencies are adjusted depending on the load current to achieve more than 90% current efficiency for about 100X variation in load current.

Chapter 7. Summary

In this thesis, several digital intensive circuit design techniques are proposed to improve the performance of the state-of-the-art mixed-signal systems. Proposed concepts are applied in different mixed signal circuits such as data-converters, clock generators (FLL, PLL, MDLL) and low dropout regulators. Their performance are verified with the measurement results obtained from working test chips implemented in 32nm SOI and 65nm LP CMOS technologies. Moreover, in-situ measurement schemes employed in these circuits enable accurate performance measurement without requiring sophisticated measurement setup.

Chapter 2 introduces a two-step VCO quantizer based ADC design that utilized beat frequency detection mechanism to achieve high SNR and ENOB for direct conversion of low swing bio-potential signals. This direct digital conversion makes area and power consuming analog front-end (AFE) redundant that is typically used in conventional designs. A detailed theoretical analysis for calculating SNR and the impact of clock jitter in the ADC performance are also discussed A 65nm test chip of the proposed two-step ADC demonstrates a SNDR of 44.5dB (i.e. 7.1 ENOB), which is 5.6dB higher than the previously proposed single step scheme, for a 10mVpp input differential signal sampled at 50 kHz.

A digital intensive sub-sampling PLL design is proposed in chapter 3. It utilized a D-flip-flop as a digital sub-sampler. The in-band phase-noise reduction mechanism is explained in this chapter. Measurement results from a 65nm test chip shows 5dB lower

phase-noise due to sub-sampling. Proposed technique is extended for a digital sub-sampling MDLL design for further reduction of phase-noise. A zero-offset aperture phase-detector and a digital-to-time converter (DTC) are used for reference spur cancellation due to static phase offset. An in-situ detection scheme accurately measure the static phase offset in time domain. A test chip, implemented in a 1.2V, 65nm CMOS process, covers an output frequency range of 0.2-to-1.45GHz, occupying a core area of 0.054mm^2. Phase noise at 100kHz offset is -95dBc/Hz, which is 9dB lower than in PLL mode.

A frequency-to-current converter based area efficient frequency synthesizer design technique for IoT application is presented in chapter 5. Proposed technique alleviates the requirement of an area consuming loop filter, which is used in traditional PLL. High open-loop gain ensures precise frequency locking. Deep-trench capacitors are used in this design for area reduction. The circuit is implemented in a 32nm SOI technology and consumes only 0.0054mm^2 area. Frequency spread over temperature variation is only 22ppm/^{o}C, measured at 48MHz. An on-chip period jitter measurement circuit is incorporated in the design for performance verifications and the jitter obtained is 115ps at 75MHz.

Finally a time quantizer based digital LDO design technique is discussed in chapter 6. A fully digital LDO design provides flexible control of the loop parameters to achieve optimum performance over wide operating conditions. The beat frequency detection mechanism enables adaptive control of the sampling clock frequency dynamically, depending on the output voltage transient. A 65nm circuit implementation achieves more

than 90% current and power efficiency, while driving a maximum load current of 100mA. The output voltage of the LDO can achieve a wide range from 0.5V to 1.15V.

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