Common-Mode Noise Reduction in Wide Band Gap Device Based Motor Drives

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Dedication

To my parents and all those who stood by me over the years.

Abstract

Wide band gap (WBG) devices are the latest trend in the power electronics industry. MOSFETs built using WBG materials offer numerous benefits to power electronic circuits. The various benefits of WBG based devices are apparent at breakdown voltages $\geq 600\,\mathrm{V}$, where Silicon IGBTs are typically used due to their combination of high breakdown voltage and low conduction losses. Compared to Silicon IGBTs, WBG MOSFETs offer faster switching rates, which reduces switching losses while also enabling significantly higher switching frequencies.

This thesis will explore the application of WBG MOSFETs to motor drives, where higher switching frequencies reduce motor losses and torque ripple and allow higher control bandwidth, thus enabling greater output frequencies needed to operate motors at higher speeds. It is well known that common-mode voltage (CMV) is generated in pulse width modulated (PWM) based drives. These voltages are responsible for bearing deterioration, shaft voltage build up and electromagnetic interference (EMI). Various software techniques like space vector modulation provide reduction in common-mode voltage. Hardware solutions like shielded cables, common-mode filters etc... also reduce common-mode currents. Hence for analyzing the effects of shaft voltage and common–mode currents, two-level voltage source inverters (VSI) utilizing Silicon Carbide (SiC) MOSFETs are constructed to operate a 1 HP induction motor. Experimental results are presented which show that the short turn-ON and turn-OFF transients as well as high switching frequencies lead to increased shaft voltage and ground currents. Elimination of ground currents is necessary to increase the lifetime of the bearings. Mitigation techniques of open-end winding drive and clamp-on ferrite chokes are evaluated in this thesis. The shaft voltage and ground currents are found to be best suppressed in an open-end winding drive utilizing clamp-on ferrites. Simulation results of loss analysis is presented for a conventional two-level VSI and dual two-level VSI to understand the thermal requirements of the Si and SiC based drives. The advantages and disadvantages of WBG based conventional two-level inverter and the various mitigation techniques are discussed.

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Chapter 1

Introduction

1.1 Current State of the Art

Pulse width modulated inverters have enabled highly efficient and easy control of adjustable field drives. These PWM based ac drives coupled with the parasitic capacitances is a major cause for electro magnetic interference (EMI), shaft voltage build up and high frequency ground currents [1–9]. The shaft voltage can result in sparks due to discharge events, which pose a major risk in combustible environment [7, 10]. Ground currents, which include bearing currents, is also responsible for premature bearing failures in motor based applications [1–9]. The stator frame is typically grounded and the DC power rails of the VSI are coupled to ground, forming a potential conduction path for common-mode currents to flow (Fig. 1.2(a)). Literature says that eighty percent of motor failures are caused due to bearing damage [11]. The shaft of the machine is supported via ball bearings. The bearings are present between the inner and outer races using grease which have an insulating effect. The charge accumulates on the rotor until the dielectric capability of the grease is reached. A resistive path is formed when the shaft voltage exceeds the lubricant's breakdown voltage. This results in a localized spike of high current density through the bearings which is called electrical discharge machining (EDM). The after effects of the EDM phenomena is pitting and fluting in the bearings [12]. The cause of the above mentioned effects is the switching common mode voltage that appears across the motor terminals which interact with the parasitics of the machine. The degree to which EDM currents are a problem depends upon 1) the

machine design: the lubricants dielectric strength and film thickness determining the breakdown voltage; and 2) the common-mode voltage output of the inverter coupling to the shaft through the machine capacitances, determining the magnitude of shaft voltage. A voltage source inverter (VSI) generates pulses with high dV/dt during switching transitions. The level of dV/dt produced by each switching device ranges from 5kV/μs to 15kV/μs and is solely responsible for charge and discharge of impulse currents [13]. High frequency oscillations as a result of parasitic resonance can reach 50-300 kHz [14] Capacitive coupling paths exists between the stator windings and the rotor body, he rotor body and the grounded stator frame and finally between the stator windings and the grounded stator frame [3, 6, 15]. The common-mode equivalent circuit of an AC induction motor is shown in Fig. 1.1. It is seen that the circuit consists of LC branches. At the resonant frequencies of these LC networks, the inverter would see little impedance resulting in a high common-mode current, were the common-mode voltage will consist of components at frequencies close to the resonant frequency The high dV/dt leads to long cable reflective wave phenomena [14]. The voltage distortion in the machine is caused due to the non-linear characteristics of the device such as dead-time, voltage drop across the device. The voltage stresses caused due to CMV on the motor windings that can cause premature insulation breakdown leading to winding short circuit and inter-turn faults [13]. CMV also leads to EMI noise ranging from 535 kHz - 1.7 MHz. Because the occurrence of EDM currents depends on the instantaneous lubricant thickness and the shaft voltage, they occur at seemingly random intervals, unlike the capacitive common-mode currents which occur during the common-mode voltage transitions. Therefore, to evaluate the degree to which common-mode EMI is a problem, this thesis considers both, shaft voltage and conducted ground currents. To improve the life of the motor it is important to minimize thee effects of common-mode noise. Various techniques have been suggested to minimize/eliminate common-mode currents in inverters. Earliest of the solutions being, shaft grounding brushes [7] or insulating either one of the bearings or both the bearings [1]. Other hardware methods include passive and active common-mode filters [9], snubber circuits etc. These techniques increase hardware complexity and compromise the dynamic response of the system. Reference [16] suggests a effective choke design that reduces the ground currents and dampens the long cable reflections. To minimize the hardware complexity various software solutions have been introduced.

Earliest of the techniques described consists of compensation technique based on the average value theory [17] . New dead time compensation techniques for voltage-fed PWM inverters have been suggested in [17], [18]. More advanced software solutions include varying modulation techniques in multilevel inverters [19] to balance the neutral voltage. The main drawback of this technique would be under-utilization of the DC bus due to lower modulation range [20].

1.2 Wide band gap devices

Wide band gap (WBG) based devices; such as Silicon carbide (SiC) and Gallium Nitride (GaN); are one of the latest trends in the field of power electronics. They offer superior properties such as 1) high critical electric fields, which enables devices to have high doping concentration and thinner blocking voltages, resulting in lower on state resistance 2) wider energy band gap, results in lower leakage currents and high operating temperatures 3) high electronic saturation voltage which leads to high switching speeds, and 4) high thermal conductivity which allows operation at high power densities, compared to conventional devices [21–23]. SiC and GaN devices are commercially available in the market by various manufacturers [24–26]. SiC inverter modules are also available in the market by manufacturers , e.g. General Electric. Literature shows the use of SiC based devices for high frequency and high temperature applications. Reference [27] suggests design and fabrication of an SiC inverter for aircraft applications. A new space vector modulation technique for high switching frequency control for three- level SiC inverters is suggested in [28].

1.3 Contribution of the thesis

Previously, Silicon based IGBT's were extensively used by designers for applications when the DC bus voltage exceeded 600 V. Si IGBT relatively operate at slower switching speeds to obtain lower conduction losses. At relatively similar ON-state voltage drop WBG based devices operate at higher switching frequencies. The increase in switching speeds reduces harmonic losses and torque ripple in the machine. Higher switching frequencies also allows higher bandwidth control of power electronic inverters that results

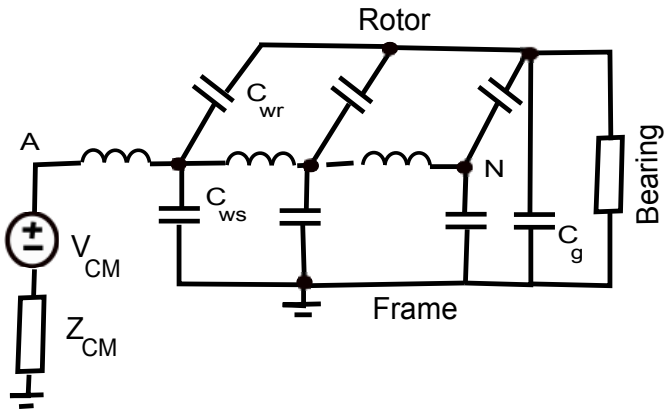
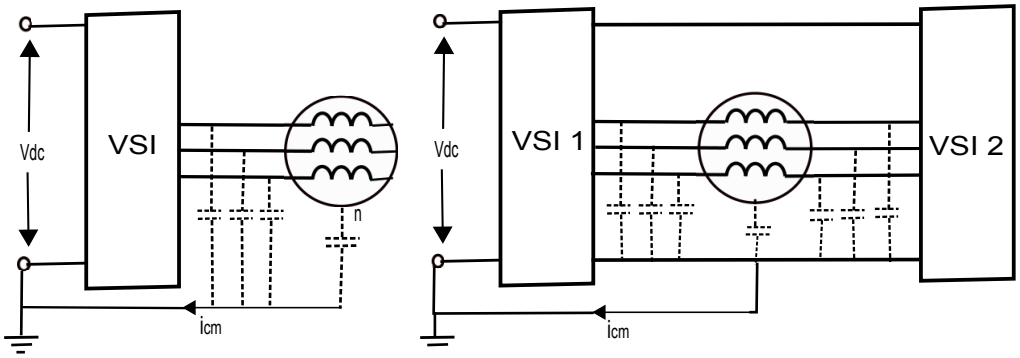


Figure 1.1: Common-mode equivalent circuit of an AC induction motor [3]

in higher output fundamental frequencies for high speed machines e.g. [29] and higher pole-count machines. High speed operation and larger number of poles, improve the motor power density [30].

To obtain maximum benefits of WBG based devices it needs to be operated at high switching speeds and faster switching rates. This device characteristic leads to high dv/dt which is harmful for motor drives and lead to excessive bearing damage in a conventional two-level VSI. This thesis explores the effect of using WBG based devices for motor drive applications.Since the occurance of EDM currents depends on the magnitude of the shaft voltage and the instantaneous lubricant thickness, they occur at random intervals,unlike the capacitive common-mode currents which occur



(a) Conventional two-level VSI (b) Dual two-level open-end winding drive

Figure 1.2: Common-mode equivalent circuit with the motor and cable capacitances

during common-mode voltage transitions. Therefore,to evaluate the degree to which common-mode EMI is a problem, this thesis considers both shaft voltage and conducted ground currents. Mitigation techniques to minimize/eliminate ground currents have been suggested using open-end winding configuration and ferrite bead chokes. Open-end winding drives provide certain advantages like higher modulation index and net zero common mode voltages at the cost of higher number of switches and associated losses [20, 31]. Few applications have the inverters connected to a common DC source and few with an isolated DC source [32]. Some drive configurations with open end windings for medium and high power applications have been suggested [33, 34]. Many multilevel inverter topologies have been proposed for the open drive applications [35]. Fig. 1.2(a) shows the cable and motor capacitances of an open-end winding drive and the path of the common-mode currents when the negative rail of the DC bus is connected to the ground. Reference [36] proposes that another issue that still persists in open-end winding drives is the phenomenon of EDM currents which can be eliminated using hybrid PWM techniques. A major issue with this configuration is the presence of circulating currents due to dead times and voltage drops in devices [34]. This thesis also discusses about how dead time to switching time (Td/Ts) ratio and the output frequency effect the magnitude of circulating currents. It also shows how increase in dead time at a given switching frequency change the magnitude of common-mode currents. For further mitigation of common-mode noise, ferrite bead chokes are cost effective solutions. These are clamp on chokes that minimize the high frequency ground currents with less hardware complexity.

This thesis is organized in the following manner:

- Chapter 1 provides an introduction to the thesis.
- Chapter 2 briefly explains about the hardware experimental setup and the various operating points results are provided.
- Chapter 3 discusses the effect of WBG based devices on shaft voltage and ground current when a conventional two-level VSI is operated with a motor load.
- Chapter 4 studies and discusses the various mitigation techniques to eliminate shaft voltage and ground currents while operating with a motor load.

- Chapter 5 shows a comparison study of losses using Si based IGBT and SiC based MOSFET's for a conventional two-level and dual two-level inverter.
- Chapter 6 presents a final discussion of using WBG-based devices for motor based applications and presents the future work.

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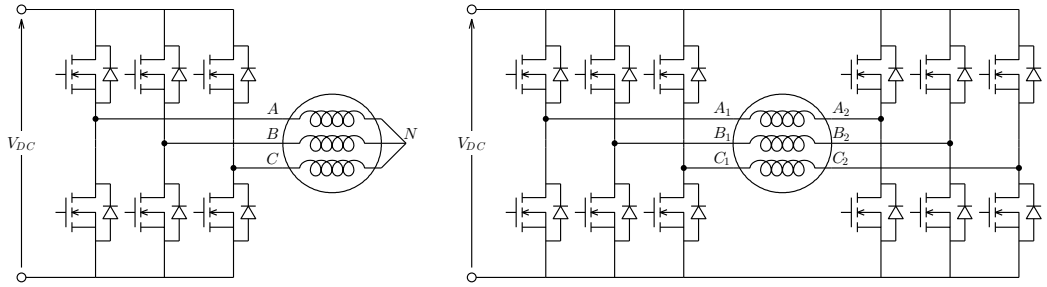
Chapter 2

Experimental set up and Operating points

The experimental setup consists of SiC Power MOSFET-based half-bridge circuits and a 1 hp AC induction motor (ACIM). Three half-bridge 'phase legs' are mounted on a set of DC rails to form the voltage source inverter (VSI). Two identical VSIs are used to realize the dual VSI open-end winding drive. The ACIM is modified such that it can be used either as a wye-connected, or as an open-end winding machine. The ACIM is coupled to a 1 hp DC motor that serves as a mechanical load. The MOSFET SCH2080KE (ROHM Semiconductor) is used to build the phase legs. A detailed description about the phase leg circuit design an be found in [23]. The circuit diagrams of the drive configurations and a photograph of the experimental setup are shown in Fig. 2.1 and Fig. 2.2 respectively. The operating points used for the results included in this thesis are shown in Table 2.1.

Symmetric SVPWM [37] is used to drive the machine in the wye-connected configuration (Fig. 2.1(a)). The open-end winding configuration of Fig. 2.1(b) uses carrier-based PWM for dual-VSI open-end winding drives [38] and is explained in detail in Chapter.4.

The shaft voltage is measured using a non-isolated probe and a brush that is electrically isolated from the motor body (Fig. 2.3). A grounding braid connects the motor body to the DC bus negative rail which is also connected to the earth ground. The



(a) Conventional two-level VSI drive (b) Dual two-level VSI based open-end winding drive

Figure 2.1: Experimental setup: Circuit diagrams

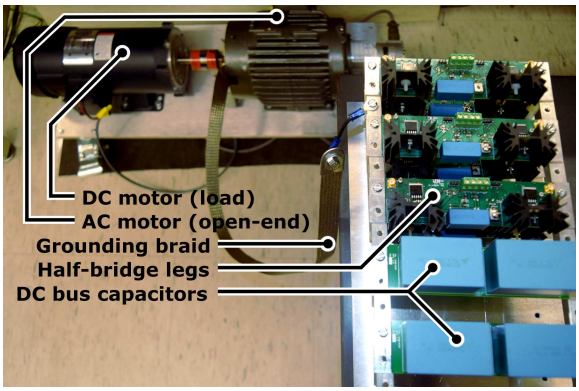


Figure 2.2: Picture of the setup showing VSI's and ACIM coupled to the DC motor load

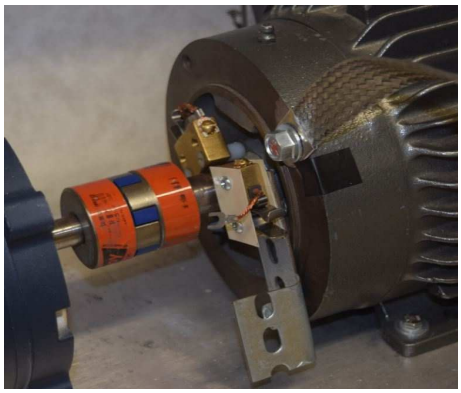


Figure 2.3: Picture of the setup showing the brush isolated from the motor body

	Switching frequency f_{sw}	Dead-time t_d	Output fundamental f_{out}	Output voltage V_{out}
OP1	5 kHz	2 μs	15 Hz	45 V (ll, rms)
OP2	5 kHz	2 μs	30 Hz	90 V (ll, rms)
OP3	20 kHz	1 μs	15 Hz	45 V (ll, rms)
OP4	20 kHz	1 μs	30 Hz	90 V (ll, rms)
OP5	100 kHz	100 ns	15 Hz	45 V (ll, rms)
OP6	100 kHz	100 ns	30 Hz	90 V (ll, rms)
OP6′	100 kHz	500 ns	30 Hz	90 V (ll, rms)

Table 2.1: Operating points used for experiments.

motor set is otherwise isolated from the earth ground. A low-bandwidth voltage differential probe is used for common mode voltage measurements. A high-bandwidth current probe from Pearson (400 Hz – 200 MHz) is employed to measure the high-frequency common-mode current entering the motor terminals. Another current probe from Pearson suitable for lower frequencies (1 Hz – 20 MHz) is used to measure any circulating currents [34] that may flow in the open-end winding configuration.

The output of the high-bandwidth current probe is the total common-mode current. For a conventional VSI drive, this current is $\sum i_{\text{CM}} = i_A + i_B + i_C$ where A, B, C are the load terminals. For an open-end winding drive, this current is $\sum i_{\text{CM}} = i_{A_1} + i_{B_1} + i_{C_1} + i_{A_2} + i_{B_2} + i_{C_2}$ where the load terminals $A_1, \ldots$ are marked in Fig. 2.1(b).

In both configurations, the current $\sum i_{\text{CM}}$ must flow through the grounding braid, into the earth ground. Therefore $\sum i_{\text{CM}}$ is synonymous with the ground current. Circulating currents in an open-end winding drive is the current flowing through a single inverter, $\sum i_{\text{CC}} = i_{A_1} + i_{B_1} + i_{C_1}$ where the load terminals A_1, B_1, C_1 are from the first inverter. To distinguish the measurements made with the high-bandwidth probe and the lower bandwidth probe in the open-end winding drive, identifiers HF and LF have been used.

For the elimination of common-mode currents a ferrite bead choke has been used. For a conventional two-level inverter, the chokes are clamped around all three output phases of the inverter. On the other hand, for an dual two-level open end winding drive the ferrite chokes needs to be clamped on the output of both sides of the inverter.

Chapter 3

Shaft voltage and common-mode currents in a two-level VSI

3.1 Introduction

Two-level VSI is one of the most widely used topology for various industrial applications. VSIs are classified into various categories: Pulse width modulated inverters, Square wave inverters and Single phase inverters with voltage cancellation. The various PWM techniques are Sine PWM, Space vector PWM etc are used as a modulation strategy for operation of the inverter. Conventional SVPWM technique is employed as a switching strategy for the single phase inverter [39].

The space vector diagram comprises of six active vectors (V_1 - V_6), and two zero vectors (V_0 , V_7) as shown in Fig. 3.1 . The vectors and each sector are displaced by 60^o from one another. The switching states of a switch $S_x(x = A, B, C)$ is defined as $S_x = 1$ when the switch is ON and $S_x = 0$ when the switch is OFF. At any given instance only one switch should be ON in each leg and therefore the switching states of the lower leg is complimentary to the upper leg ($\overline{S}_x$). In Fig. 3.1 the space vectors have their defined switching states shown. For e.g. $V_1 = (1\ 0\ 0)$ defines $S_A = 1$ implying the upper leg of phase A is switched ON and is connected to positive pole of V_{DC} and $S_B = 0$, $S_C = 0$ meaning the upper leg of phase A is switched OFF and is connected to negative pole of V_{DC} which is GND . The reference voltage is generated with two active vectors and one zero vector belonging to each sector. If the duty ratios for the voltage vectors V_1,

V_2 and V_z are dV_1, dV_2 and dV_z respectively, solutions to these duty ratios is shown in (3.2) which is obtained by solving (3.1). Here $m_V = V_o/V_{DC}$ is the modulation index of the VSI, α is the angle the reference voltage makes with the first vector, V_o is the peak output voltage that is synthesized and V_{DC} is the average DC-link voltage. The maximum modulation index achieved in a conventional VSI is $m_V = 1/\sqrt{3}$. Hence the maximum output voltage generated using space vectors is $m_V{}^*V_{DC}$.

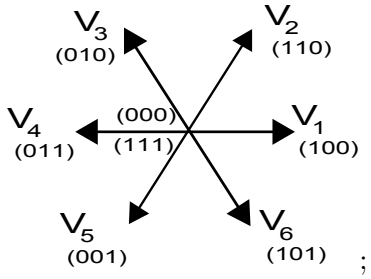


Figure 3.1: Space vector diagram of a Conventional VSI

$$\begin{aligned} dV_1 \times \overline{V}_1 + dV_2 \times \overline{V}_2 + dV_z \times 0 &= \overline{V}_o \\ dV_1 + dV_2 + dV_z &= 1 \end{aligned} \tag{3.1}$$

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha \\ dV_z &= 1 - dV_1 - dV_2 \end{aligned} \tag{3.2}$$

3.2 Common mode voltage

The CMV of a VSI depends on its switching states and the magnitude of V_{DC} and is given as 3.3, where v_{AN}, v_{BN} and v_{CN} are the output phase voltages. For example, the output phase voltages when space vector $V_1 = (1,0,0)$ is applied is given in 3.4 and the CMV is calculated as 3.5. The CMV of the space vectors are consolidated and presented

in Table.3.1.

$$V_{CM(VSI)} = \frac{1}{3}\left(v_{AN} + v_{BN} + v_{CN}\right) \tag{3.3}$$

For active voltage vector V_1,

$$\begin{aligned} V_{AN} &= S_A \times v_{dc} = v_{dc} \\ V_{BN} &= S_B \times v_{dc} = 0 \\ V_{CN} &= S_C \times v_{dc} = 0 \end{aligned} \tag{3.4}$$

The CMV is calculated as,

$$\begin{aligned} V_{CM(VSI)} &= \frac{1}{3}\left(S_A v_{dc} + S_B v_{dc} + S_C v_{dc}\right) \\ &= \frac{1}{3}\left(v_{dc}\right) \end{aligned} \tag{3.5}$$

Table 3.1: Instantaneous CMV of the VSI

Voltage space vector	S_A, S_B, S_C	$V_{CM(VSI)}$
V_0	$0, 0, 0$	0
V_1	$1, 0, 0$	$v_{dc}/3$
V_2	$1, 1, 0$	$2v_{dc}/3$
V_3	$0, 1, 0$	$v_{dc}/3$
V_4	$0, 1, 1$	$2v_{dc}/3$
V_5	$0, 0, 1$	$v_{dc}/3$
V_6	$1, 0, 1$	$2v_{dc}/3$
V_7	$1, 1, 1$	v_{dc}

CMV of a conventional two-level VSI at any given output frequency consists of third harmonic components and high frequency components which is a multiple of switching frequency. The triplen harmonics are necessary to improve the DC bus utilization. The two-level VSI is operated at 15Hz and 30Hz. The hardware results of the CMV when a conventional two-level VSI is operated at 15Hz and 30Hz is shown in Fig. 3.4. It is noted that the higher order harmonics increases at higher switching frequencies. The simulation results of a conventional VSI is shown which complies with the hardware

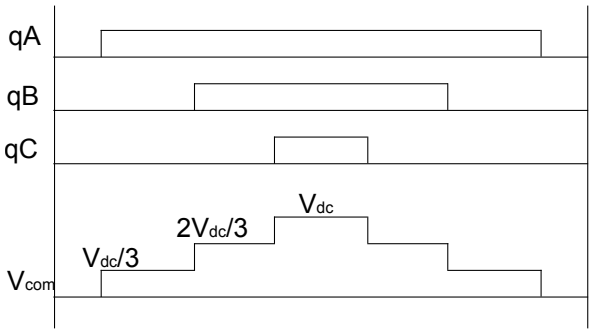
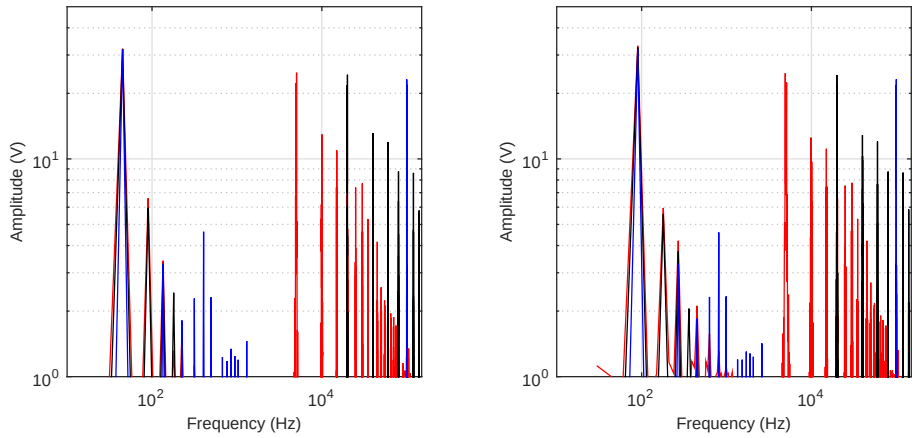


Figure 3.2: An example of varying CMV in a single VSI over a switching period

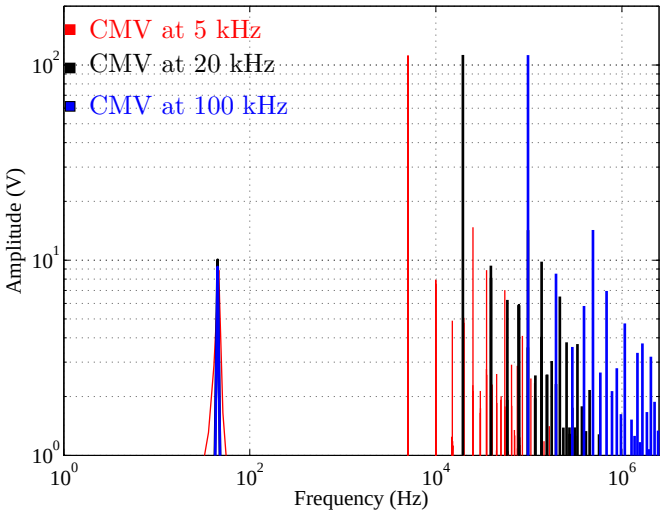
results and indicates the presence of ;pw frequency third harmonic component and higher order switching harmonics. It is to be noted that the simulation results of CMV are observed using an RL load and the device characteristics and parasitics of motor load are not considered. The probe used for measurements of CMV is a low frequency probe and hence the high frequency component measurements can have discrepancies. An example of the common mode voltage applied over one switching interval is shown in Fig. 3.2. The rate of change of the common mode voltage is determined by the speed at which the devices turn-ON and turn-OFF.



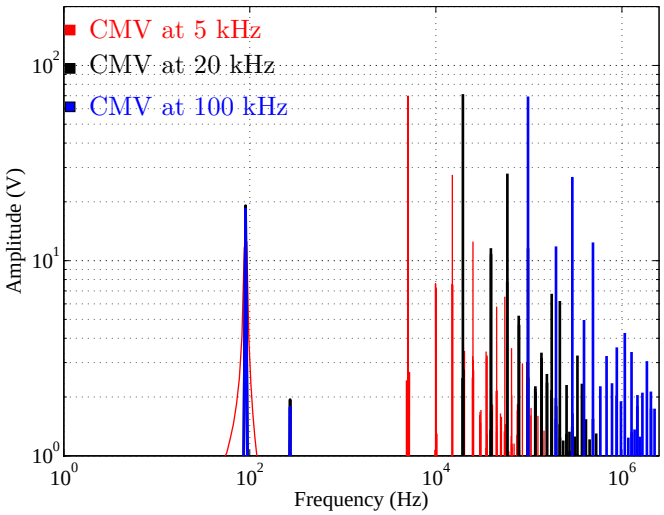
(a) Operation at 15 Hz

(b) Operation at 30 Hz

Figure 3.3: Simulation: Common mode voltage of a conventional VSI at 15 Hz and 30 Hz



(a) Operation at 15 Hz



(b) Operation at 30 Hz

Figure 3.4: Hardware: Common mode voltage of a conventional VSI at 15 Hz and 30 Hz

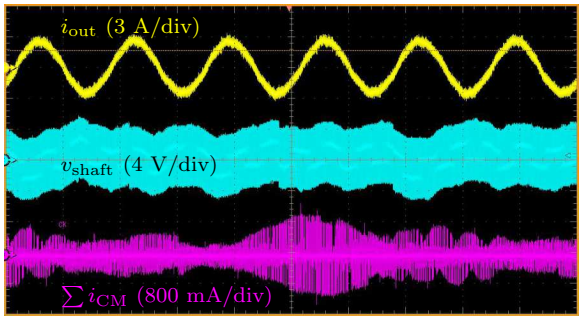
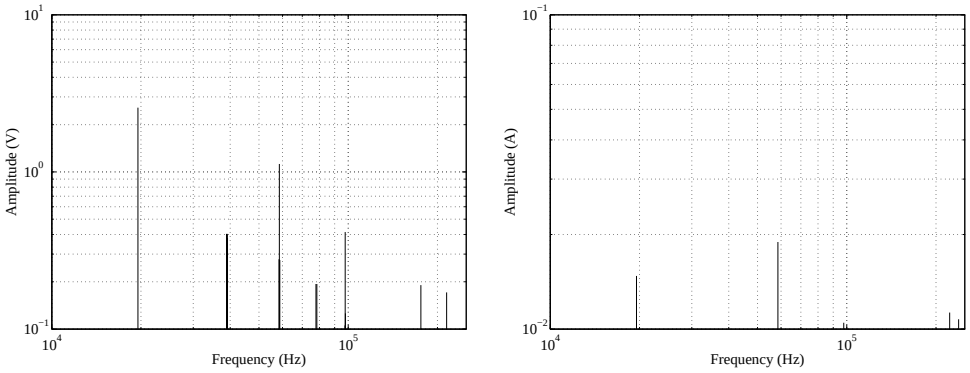


Figure 3.5: Experimental results of shaft voltage and common-mode currents at $OP4$

3.3 Shaft voltage and common-mode currents

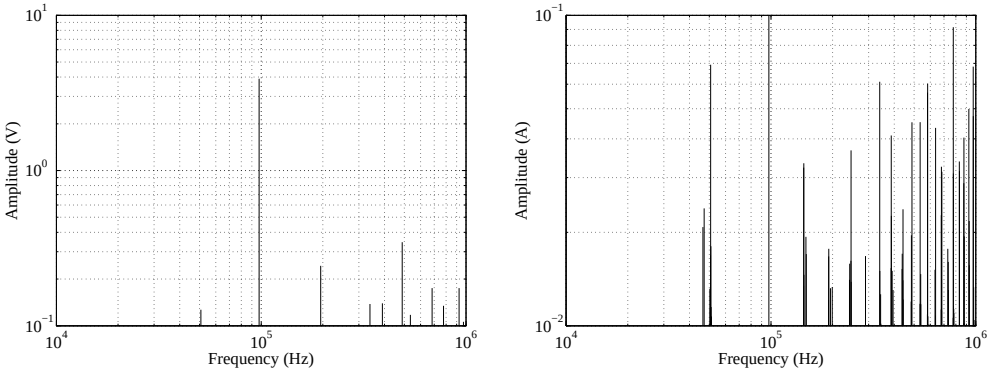
The magnitude of common-mode currents is larger at OP6 (Fig. 3.6(b) and 3.9(b)) which is consistent with the literature: higher PWM frequencies will exacerbate the effects of the inevitable common-mode voltage generated by a typical PWM VSI drive.



(a) Shaft voltage at OP4

(b) Common-mode currents at OP4

Figure 3.6: Shaft voltage and common-mode current FFT's of a conventional two-level VSI at $OP4$



(a) Shaft voltage at OP5 (b) Common-mode currents at OP5

Figure 3.7: Shaft voltage and common-mode current FFT's of a conventional two-level VSI at $OP5$

Since the motor is operated using V/f control there is slight variation in the common mode voltage and hence not a significant change in ground currents and shaft voltage (Fig. 3.7 and 3.9). It is observed that the variation of dead time at a given switching frequency does not bring a significant change in the magnitudes of shaft voltage and ground currents as shown in Fig. 3.10.(Note: The sampling rate of the measurements are higher to observe a higher range of frequencies). This is because the primary cause of common-mode currents is due to the fast changing common-mode voltages of the intentionally applied space vectors, and not due to the unintentional space vectors applied during the dead-time interval.

3.3.1 Effect of switching rate of the device

WBG based devices have an ability to switch at higher speeds and lower dead times. This section explores the disadvantages of operating a device at faster switching speeds.

This effect of increased dv/dt or di/dt in WBG based device is demonstrated in a conventional two-level VSI by operating the VSI at OP2 and observing the output voltage of phase A and common-mode currents under the following conditions:

- Case I : Gate resistance $R_G = 5.11\Omega$ and no external capacitance across the gate
- Case II : Gate resistance $R_G = 33\Omega$ and no external capacitance across the gate

- Case III : Gate resistance $R_G = 33\Omega$ and $C_{GS} = 10nF$

The three cases are chosen to observe how a SiC based conventional two-level VSI vary the magnitude of common-mode currents when it is switched at slow and fast rates. Increasing the capacitance across the gate results in slower charge and discharge rate of the gate during turn ON and turn OFF respectively.

It is clearly observed that the reduced gate resistance has a higher di/dt when compared to a larger gate resistance (Fig.3.12 , Fig. 3.13 , Fig. 3.14 and Fig.3.15). Case III can be compared to a Si device which has slower switching rates and hence reduced common-mode currents when compared to WBG based devices with faster switching speeds as shown in Case I. The FFT's of the common-mode currents (Fig. 3.11) clearly shows the increase in high frequency common-mode currents, with smaller gate resistances.

The increase in switching rates with reduced gate resistances is observed in another scope and the results are consistent. (Fig. 3.16, Fig. 3.17 and Fig. 3.18).

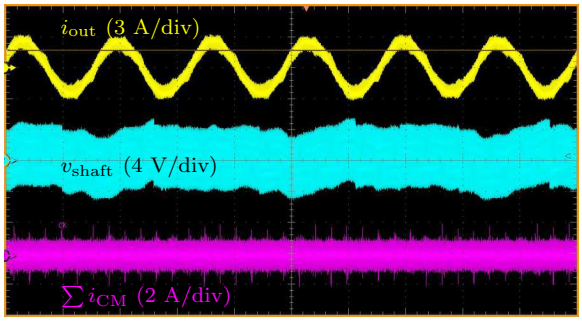
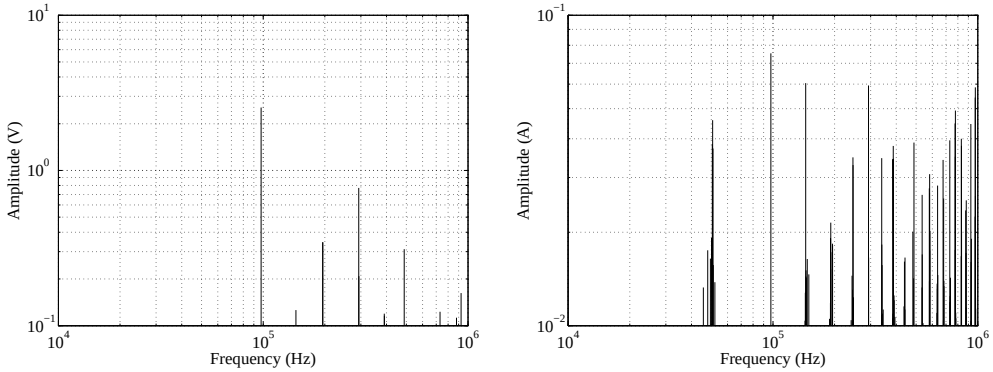
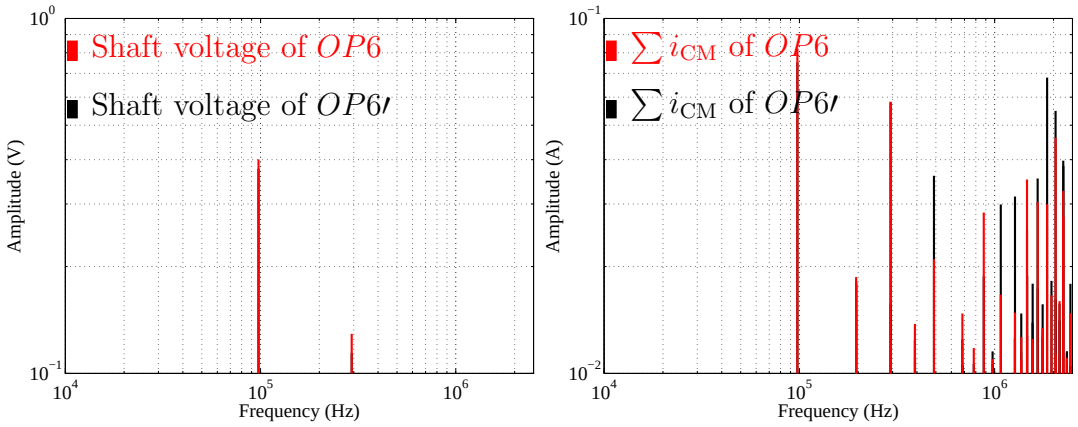


Figure 3.8: Experimental results of shaft voltage and common-mode currents at $OP6$



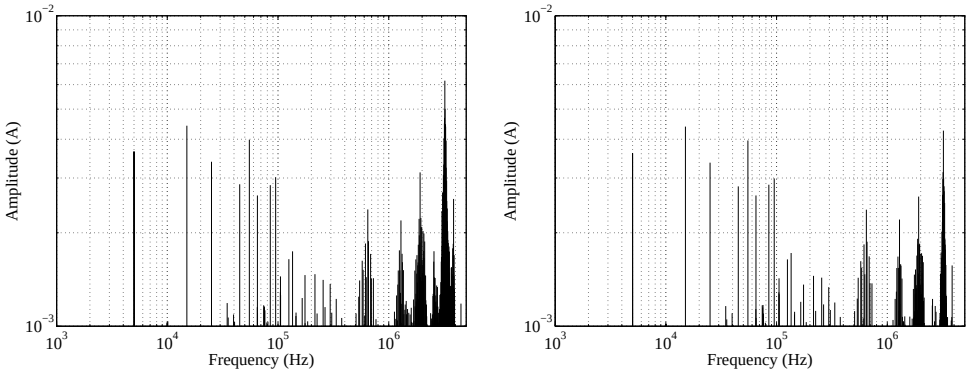
(a) Shaft voltage at OP6 (b) Common-mode currents at OP6

Figure 3.9: Shaft voltage and common-mode current FFT's of a conventional two-level VSI at $OP6$



(a) Spectra of shaft voltage (b) Spectra of common-mode currents

Figure 3.10: Comparison of shaft voltage and common mode current FFT's of a conventional two-level VSI at $OP6$ and $OP6\prime$



(a) Common-mode currents in Case I (b) Common-mode currents in Case III

Figure 3.11: Common-mode currents at $OP2$ to be observed at Case I and Case III

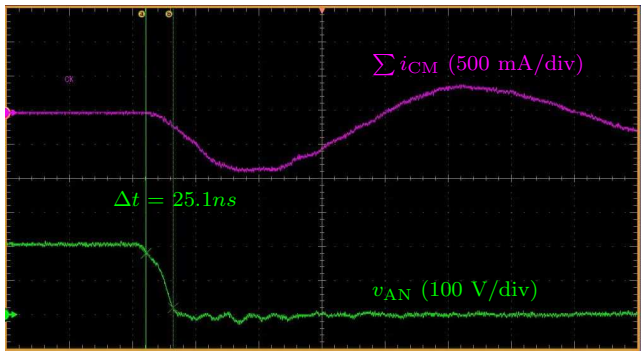


Figure 3.12: Scope snap shots of output voltage and common mode currents at $OP2$ - Case I to measure Δt

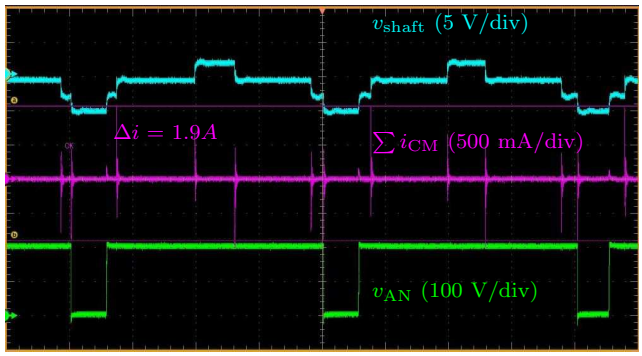


Figure 3.13: Scope snap shots of output voltage and common mode currents at $OP2$ - Case I to measure Δi

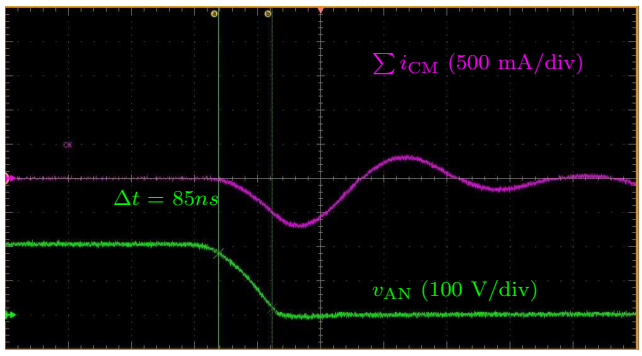


Figure 3.14: Scope snap shots of output voltage and common mode currents at $OP2$ - Case III to measure Δt

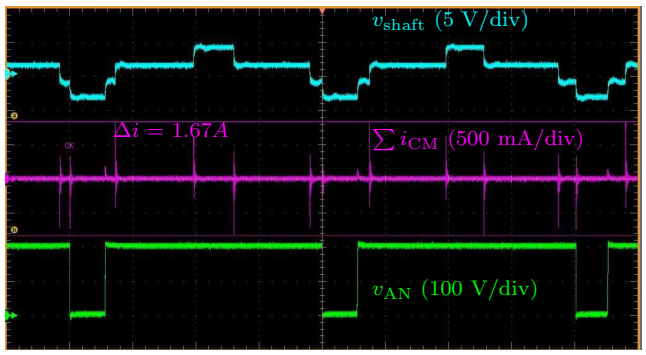
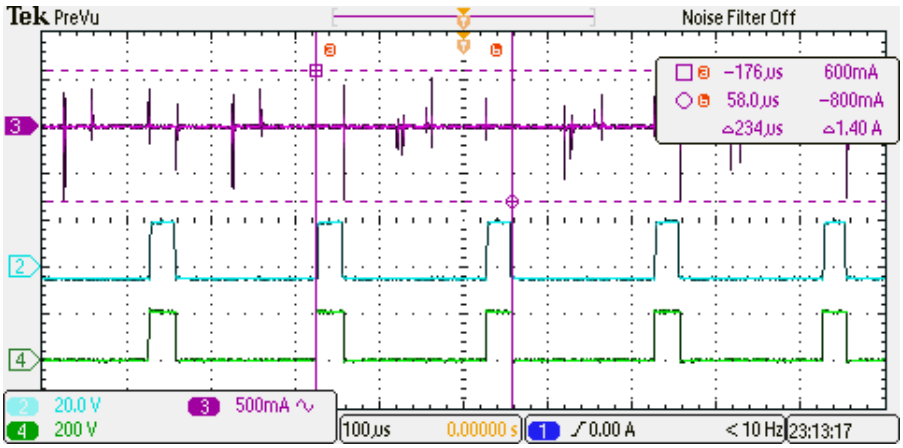
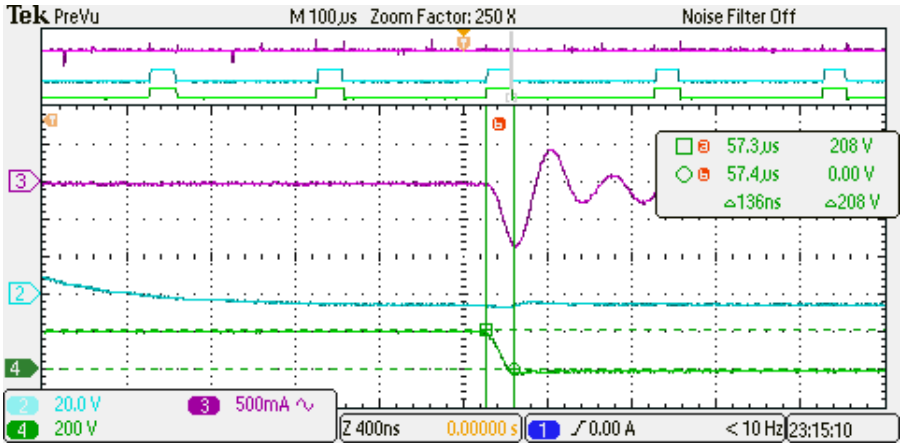


Figure 3.15: Scope snap shots of output voltage and common-mode currents at $OP2$ - Case III to measure Δi

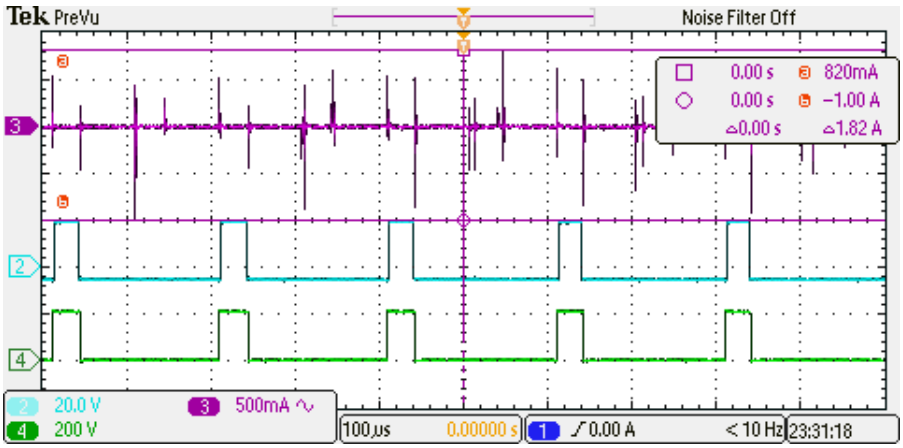


(a) The peak to peak magnitude of common-mode currents (Δi)

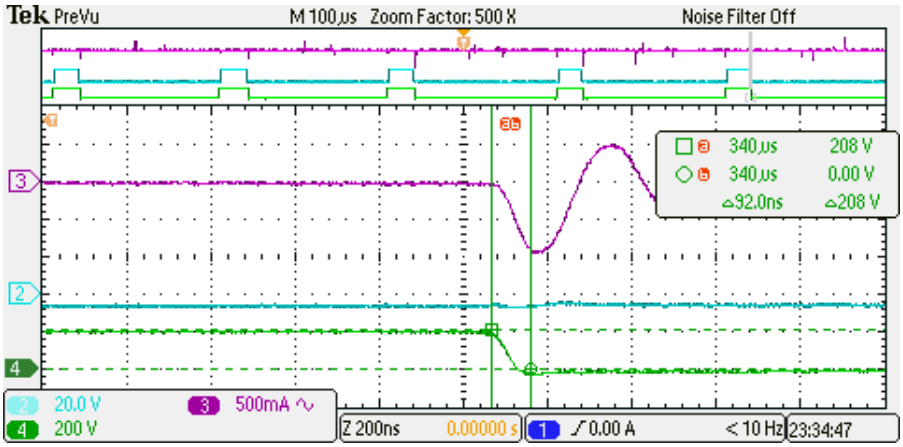


(b) Measurement of Δt

Figure 3.16: Scope snap shots of output voltage and common-mode currents at $OP2$ - Case I to measure Δt and Δi

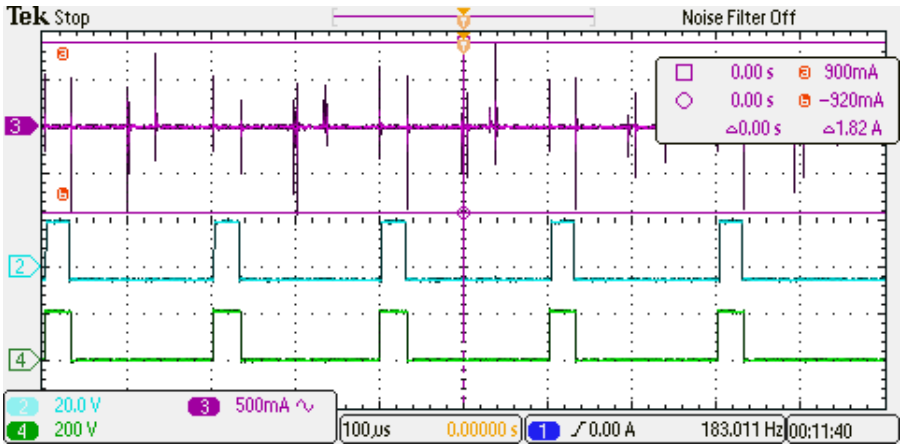


(a)

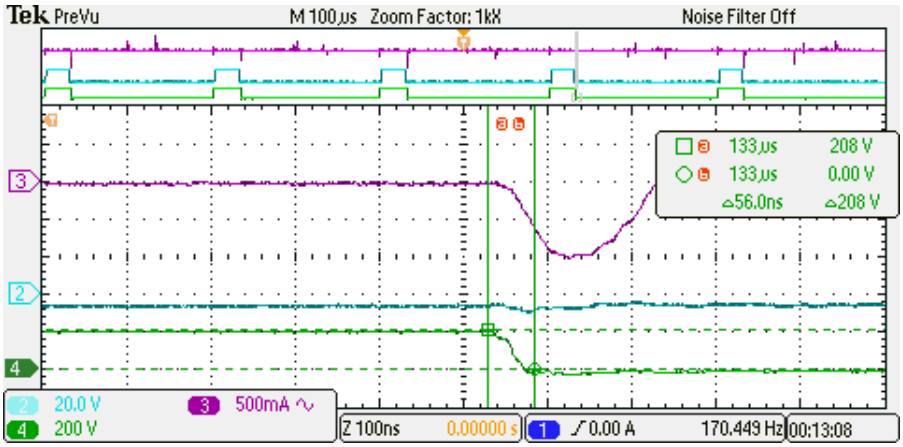


(b)

Figure 3.17: Scope snap shots of output voltage and common-mode currents at $OP2$ - Case II to measure Δt and Δi



(a)



(b)

Figure 3.18: Scope snap shots of output voltage and common-mode currents at $OP2$ - Case III to measure Δt and Δi

3.4 Conclusion

Common-mode noise reduction is necessary for increased life of motor drives. WBG based devices exacerbate the effects of common-mode voltage to a large extent. The reduction in common-mode currents should not be the reason to operate a WBG based inverter at lower switching frequencies and longer dead-time intervals. This does not provide us with the expected performance. Therefore, to fully exploit the attributes offered by the wide band gap devices and utilize the advantages discussed in Chapter 1, the switching frequency needs to be increased. The next chapter focuses on the various mitigation techniques for reducing the effects of shaft voltage and common-mode currents for WBG based motor drive systems.

Chapter 4

Mitigation techniques of shaft voltage and common-mode currents

4.1 Introduction

Various hardware and software based mitigation techniques have been used for common-mode voltage reduction/elimination. This thesis focuses on using the two approaches for common-mode current reduction: 1) the use of dual VSIs with an open-end winding motor to nearly eliminate switching common-mode voltages; and 2) the use of common-mode impedance to suppress currents from flowing in response to the common-mode voltage.

4.1.1 Open-end winding drives

Open-end winding machines have been used in various drive applications. It offers certain advantages over conventional drives, the main being reduction of common-mode voltage across the drive while obtaining a good modulation index (m_v= 1). These advantages are obtained at the cost of increased number of switches thereby increasing the switching and conduction losses [34]. Hence, the open-end topology is an alternative to the more complex multilevel inverters. An optimal switching strategy to minimize

torque ripple using direct torque control is discussed in [40]. In [32] a zero sequence elimination technique has been suggested for a dual-two-level inverter using a single DC link voltage.This technique does not eliminate CMV. In [20] a space vector technique has been presented for an open-end dual two-level VSI to eliminate CMV. A space vector technique for an induction motor with dual windings is presented in [31].

In a dual two-level inverter it consists of two inverters namely positive-end and negative-end inverters. These inverters are connected to a common DC link. Each inverters has six active vectors and two zero vectors. The space vector of the positive and negative end inverter is shown in Fig. 4.2. The space vectors of the negative end inverter is rotated by 180°. The output voltage of each inverter is shown in 4.1. The common mode voltage of the positive and negative inverter is shown in 4.2. There are two voltages associated with an open-end drive : differential and common mode voltage given in 4.3. When space vectors V_1 , V_3 , V_5 , $V_{1\prime}$, $V_{3\prime}$ and $V_{5\prime}$ is applied to the inverter the CMV is $V_{dc}/3$ and when space vectors V_2 , V_4 , V_6 , $V_{2\prime}$, $V_{4\prime}$ and $V_{6\prime}$ is applied to the inverter the CMV is $2V_{dc}/3$. The space vectors used for an open-end drive for the positive and negative end inverter is such that the $V_{diff} = 0$. When space vectors V_1, V_3, V_5, $V_{1\prime}$, $V_{3\prime}$ and $V_{5\prime}$ are used we obtain reduced common-mode voltage and hence these vectors are used for the space vector technique of the open-end inverter.

$$\begin{aligned} V_{o1} &= V_{A1N} + V_{B1N}e^{j2\pi/3} + V_{C1N}e^{-j2\pi/3} \\ V_{o2} &= -(V_{A2N} + V_{B2N}e^{j2\pi/3} + V_{C2N}e^{-j2\pi/3}) \end{aligned} \tag{4.1}$$

$$\begin{aligned} V_{com1} &= \frac{1}{3}\left(v_{A1N} + v_{B1N} + v_{C1N}\right) \\ V_{com2} &= \frac{1}{3}\left(v_{A2N} + v_{B2N} + v_{C2N}\right) \end{aligned} \tag{4.2}$$

$$\begin{aligned} V_{diff} &= V_{com1} - V_{com2} \\ V_{com} &= \frac{1}{2}\left(V_{com1} + V_{com2}\right) \end{aligned} \tag{4.3}$$

The resultant voltage obtained from the positive and negative end inverter is given

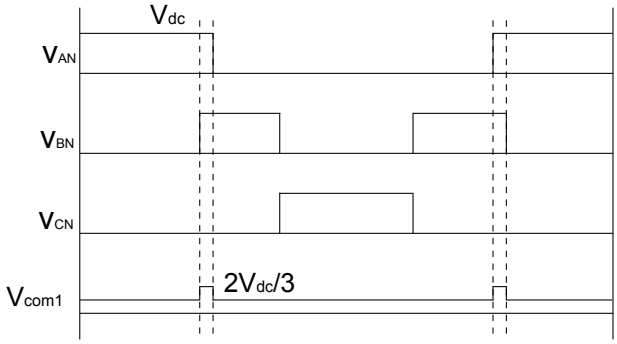


Figure 4.1: CMV glitch in dual VSI due to dead band

by equation 4.4. The resultant space vector diagram is shown in Fig. 4.2. There is a total of 6 sectors and the magnitude of the resultant space vectors is $\sqrt{3}\mathrm{V_{DC}}$.At any given sector, only one inverter is fed 2 active vectors and a zero vector while the other inverter has only one active vector applied. For example in sector 1, the positive end inverter has only one active vector applied $\mathrm{V}_1 = (1, 0, 0)$ and the negative end inverter switches with active vectors $\mathrm{V}_{3\prime}$, $\mathrm{V}_{5\prime}$ and zero vectors. A carrier based algorithm of the switching strategy is described in [38].

$$\begin{aligned} V_o &= V_{o1} + V_{o2} \\ &= (V_{AA\prime} + V_{BB\prime}e^{j2\pi/3} + V_{CC\prime}e^{-j2\pi/3}) \end{aligned} \tag{4.4}$$

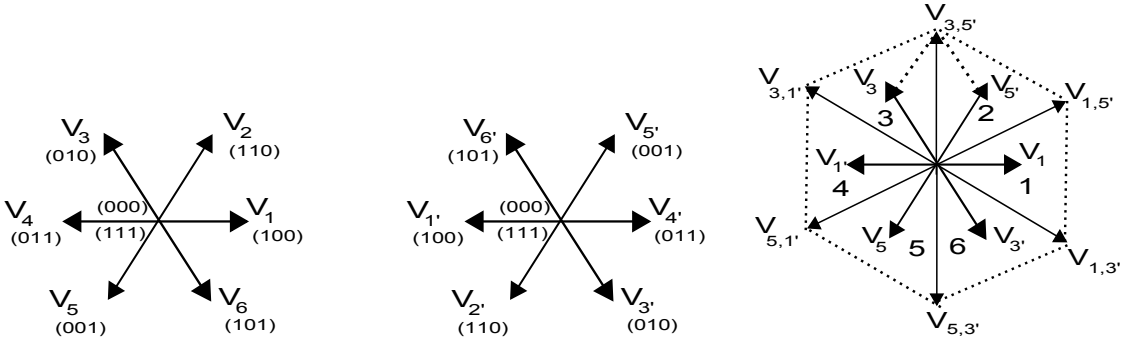


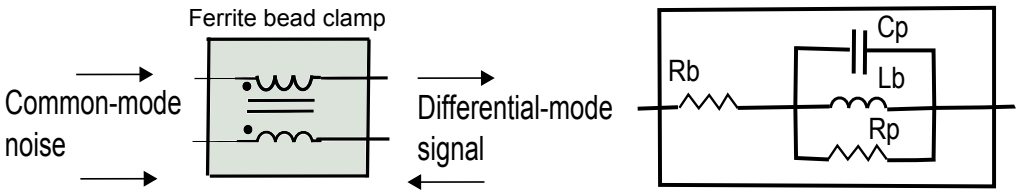
Figure 4.2: Space vector diagram for an open-end VSI (a) Positive-end inverter, (b) Negative-end inverter, (c) Resultant space vector

4.1.2 Ferrite bead clamp-on chokes

The elimination of common-mode currents at higher switching frequencies can be done using ferrite clamp chokes. These chokes along with dual two-level VSI nearly eliminates the common-mode currents and is discussed in detail in the following sections. Common-mode currents are the currents that flow through different conductors and do not cancel out each other while the differential mode signals flow in the opposite direction as shown in Fig.4.3(a). The ferrite bead choke can be represented as a circuit of a series resistive and an inductive component. The inductive component has some parasitic capacitances and resistances. At lower frequencies, the ferrite bead acts as an inductive element and rejects common-mode currents due to its inductive reactance. As frequency increases, the impedance becomes more resistive and the bead absorbs the currents, dissipating them as heat. The ferrite bead consists of three regions : inductive, resistive and capacitive. To effectively use the ferrite bead choke, it must be operated in the resistive region. The ferrite bead choke is connected to the circuit in series with the noise source and load (Fig.4.3(c)). For effective performance of the ferrite beads for high frequency common-mode elimination, the number of bead should be more than 1 and be placed close to each other [41]. This would increase the impedance in the network and eliminate common-mode noise. These cokes can be in the form of a clamp-on ferrite that encircles the connecting cable of all three phases or a continuous core upon which the three phase wires will be wound. These chokes are effective for high frequency components and hence could be effectively used for inverters utilizing WBG devices.

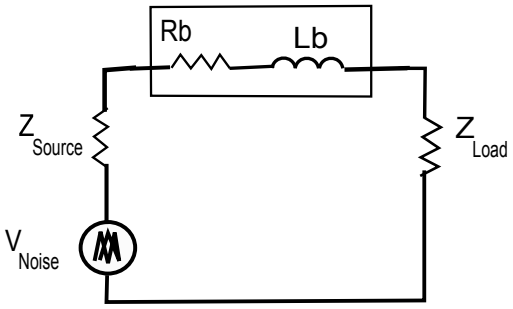
4.2 Circulating currents in a dual two-level VSI

One of the issues with a dual two-level VSI is the presence of circulating currents. Circulating currents occurs in an dual two-level VSI due to the presence of V_{diff}. The presence of V_{diff} is because of the presence of device drops and dead times provided to avoid short circuiting the DC bus [34]. During the dead-time intervals, the output space vectors at the motor terminals are not necessarily the vectors intended by the modulation; the output vectors are instead determined by the motor currents direction and the freewheeling diodes that carry these currents during the dead-time. Hence these lead to differential common-mode voltage which in-turn produce low frequency current



(a) Ferrite bead clamp

(b) Ferrite bead choke with the parasitics



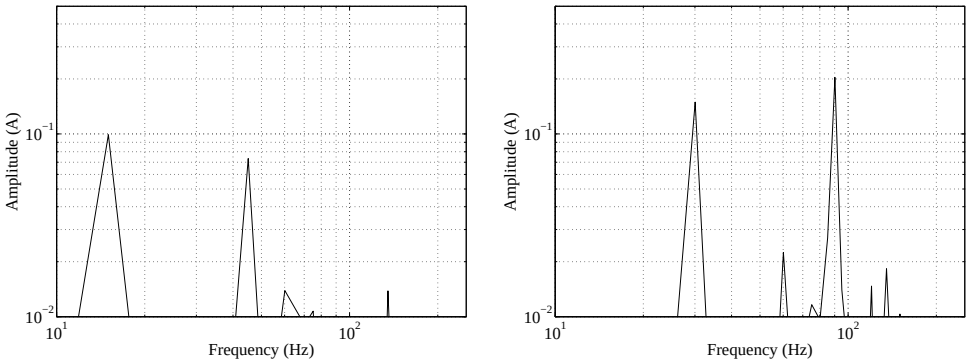
(c) Equivalent circuit of a system with a ferrite bead choke

Figure 4.3: Ferrite bead choke

components that increase the losses in the drive.The magnitude of circulating currents decrease the following ways:

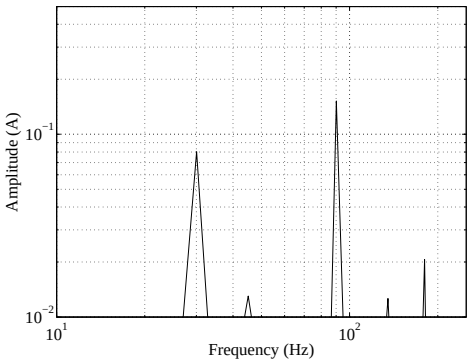
- decreasing the ratio of dead time to the switching time t_d/T_s
- increasing the output frequency.

It is observed from Fig. 4.5(a) and Fig.4.5(b) that the magnitude of low frequency circulating currents reduce with the increase in output frequency. When Fig. 4.5(b) is compared with Fig. 4.6 it is seen that the magnitude of low frequency circulating currents increases at OP4. This is because the T_d/T_s ratio is higher at OP4 than OP2. At higher switching frequencies of OP6 the trend of low frequency common-mode currents do not show a significant variation with decrease in dead time (Fig. 4.4(b) and 4.4(c)) and also at lower output frequencies the third harmonic magnitude shows a decrease. It is also observed that the magnitude of the output frequency component at $15Hz$ is more than what is observed at $30Hz$ as shown in Fig. 4.4(a) and 4.4(b). The ferrite bead chokes do not eliminate any low frequency components is proved (Fig.4.4(d)). These

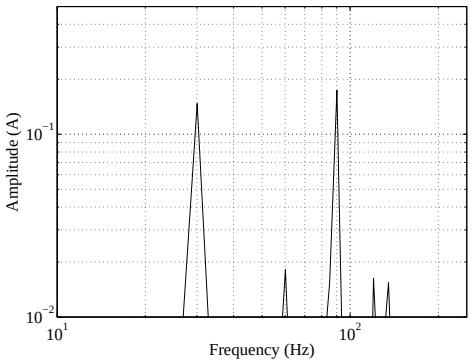


(a) Circulating currents at $OP5$

(b) Circulating currents at $OP6$



(c) Circulating currents at $OP6'$



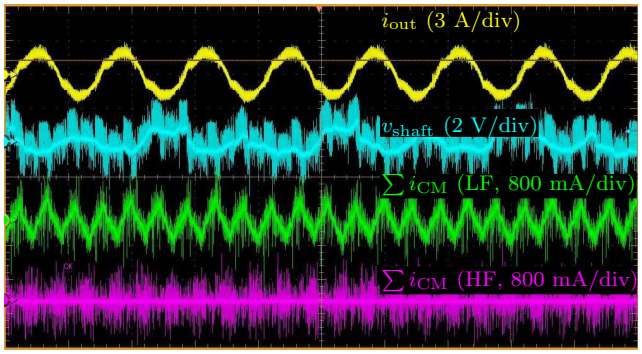
(d) Common-mode currents at $OP6$ with choke

Figure 4.4: Circulating current FFT's of a dual two-level VSI open-end winding drive at (a) $OP5$, (b) $OP6$, (c) $OP6$ and (d) $OP6$ with choke

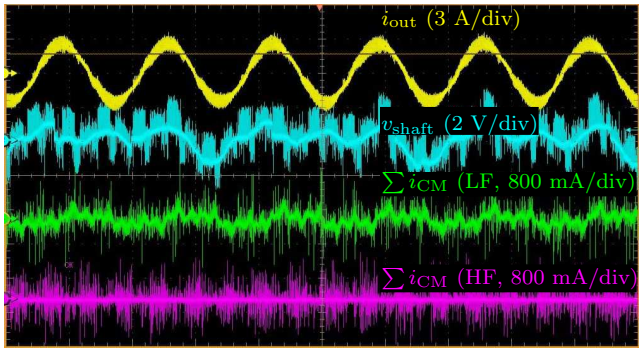
trends in circulating currents could be due to higher switching frequencies and smaller dead times and needs to be further investigated.

4.3 Shaft voltage and common-mode currents

As there is a reduction in common-mode voltage using dual two-level VSI, the magnitude of shaft voltage and high frequency common-mode currents significantly reduce (Fig. 4.9 and Fig. 4.11). It is also observed that as the dead time increases, at a given switching frequency, the magnitude of shaft voltage and high frequency common-mode currents increases (Fig. 4.13). This is because the as dead time increases the common-mode voltage appearing across the inverter's output increases. As mentioned in the previous



(a) Circulating currents at OP1



(b) Circulating currents at OP2

Figure 4.5: Scope shots of circulating currents of a dual VSI open-end winding drive at OP1 and OP2

section common-mode voltage is the major cause for shaft voltage and common-mode currents. Hence this shows the dependence of dead times in the magnitude of shaft voltage and ground currents in an dual two-level VSI and shows the advantageous of being able to go to small dead-times.

Magnitude of shaft voltage and ground currents does not show a significant variation with decrease in the output frequency as shown in Fig. 4.13. This is because the voltage across the terminals remains the same irrespective of the frequency as V/f control is employed.

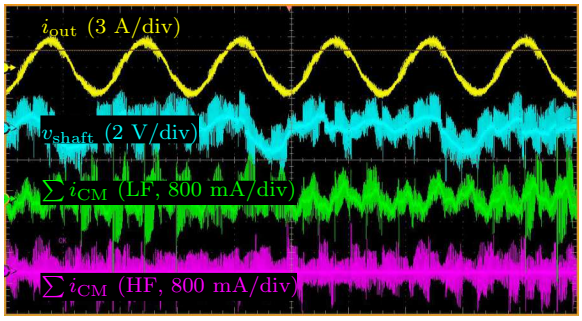
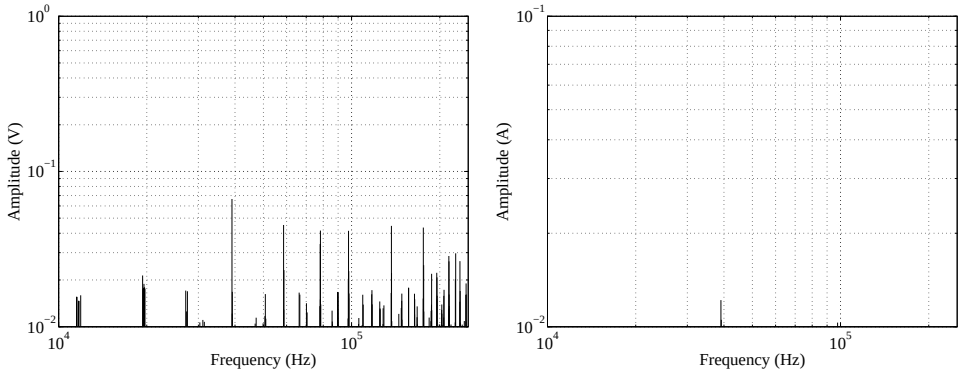


Figure 4.6: Scope shots of shaft voltage and ground current of an dual VSI open-end winding drive at OP4

4.4 Elimination of common-mode currents in a two-level VSI

The ferrite bead choke is clamped on to all the three output phases of the VSI as shown in Fig.4.14(a). For improved performance of the choke, 4 ferrite bead clamps are used in series. This diagram shows the common-mode choke acts as a common-mode transformer with a dissipative secondary. The secondary of the transformer consists of a RL branch that appears in series to the equivalent common-mode circuit. It is



(a) Shaft voltage spectrum at OP4 (b) $\sum i_{CM}$ (HF) spectrum at OP4

Figure 4.7: Shaft voltage and ground current for a dual VSI at OP4

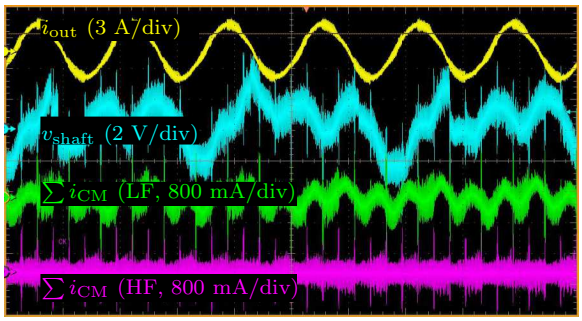
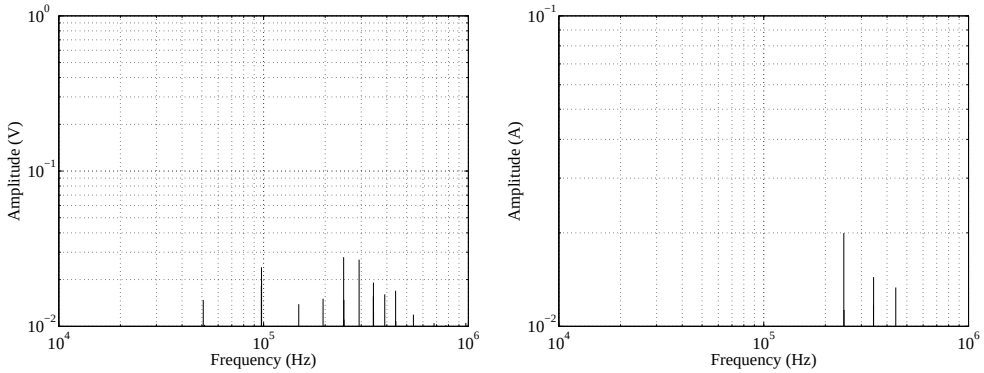


Figure 4.8: Scope shots of shaft voltage and common-mode current of a dual VSI open-end winding drive at OP6



(a) Shaft voltage spectrum at OP6

(b) $\sum i_{CM}$ (HF) spectrum at OP6

Figure 4.9: Shaft voltage and ground current for a dual VSI at OP6

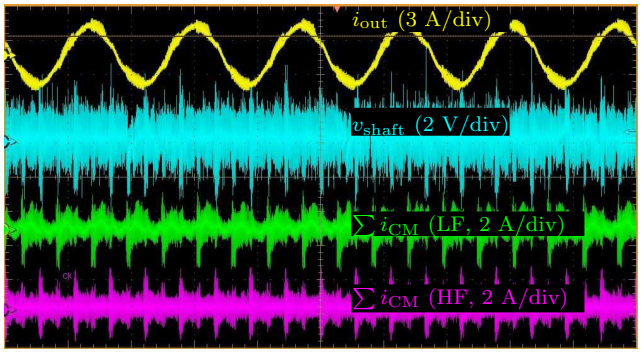
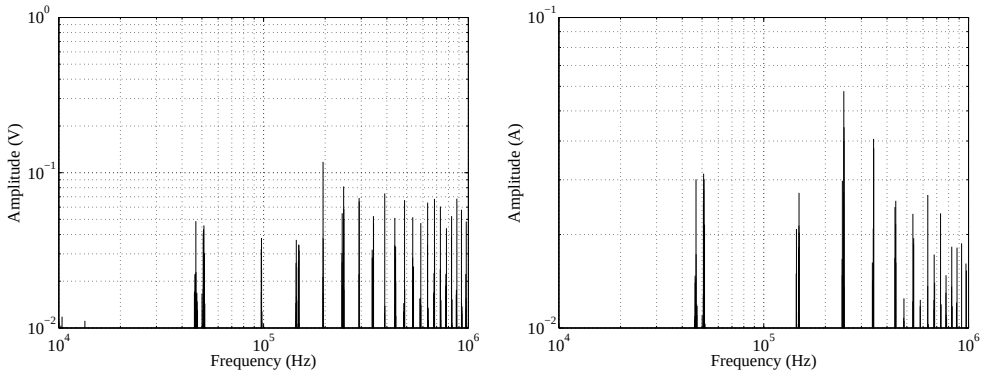


Figure 4.10: Scope shots of shaft voltage and common-mode current of a dual VSI open-end winding drive at OP6′



(a) Shaft voltage spectrum at OP6′ (b) $\sum i_{CM}$ (HF) spectrum at OP6′

Figure 4.11: Shaft voltage and ground current for a dual VSI at OP6′

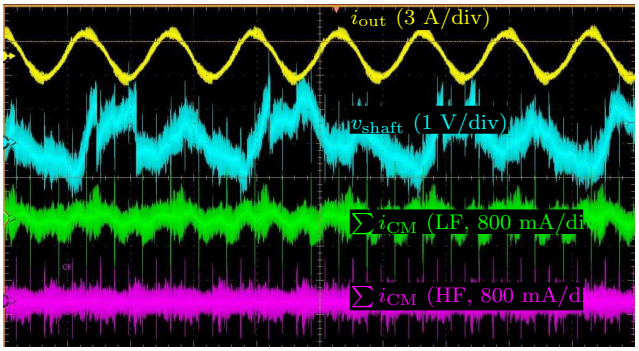
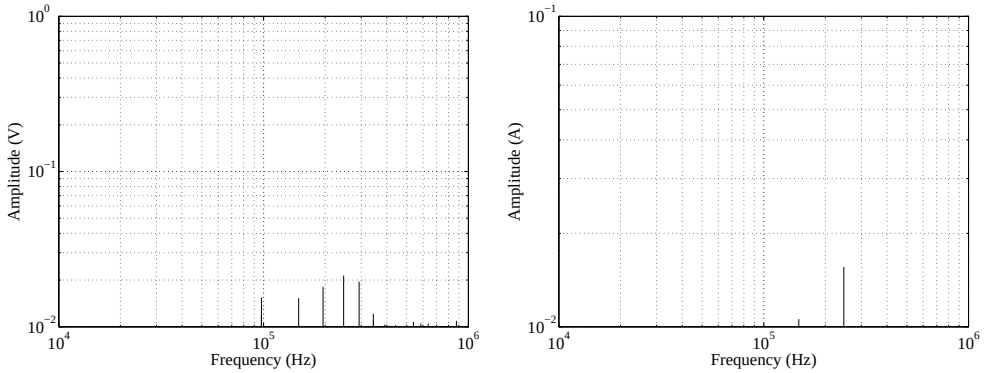
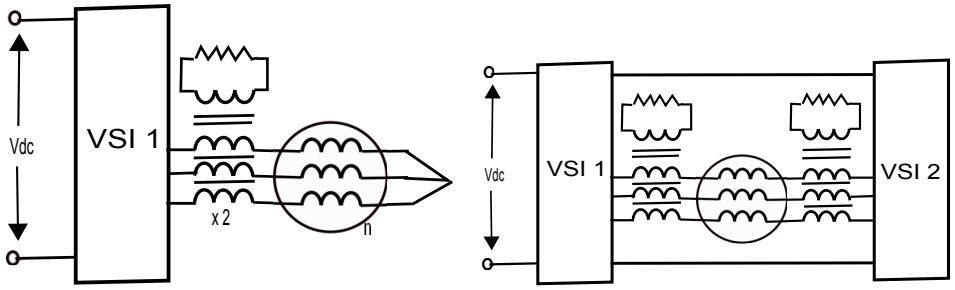


Figure 4.12: Scope shots of shaft voltage and common-mode current of a dual VSI open-end winding drive at OP5



(a) Shaft voltage spectrum at OP5 (b) $\sum i_{\mathrm{CM}}$ (HF) spectrum at OP5

Figure 4.13: Shaft voltage and ground current for a dual VSI at OP5



(a) Conventional two-level setup (b) Dual two-level VSI open-end winding drive setup

Figure 4.14: Experimental setup : Ferrite bead clamp connected to a conventional two-level VSI ((a)) and dual two-level VSI ((b))

clearly observed that the high frequency components are not nearly eliminated (Fig. 4.16(b)). Hence, a solution to eliminate the high frequency ground currents and to avoid further spurious effects of common-mode voltage is to use an dual two-level VSI open-end winding drive with the ferrite bead clamps which is further discussed in the next section.

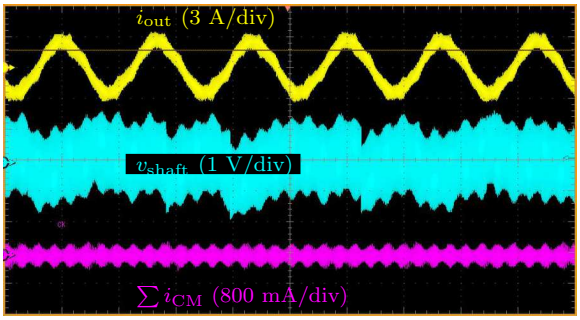
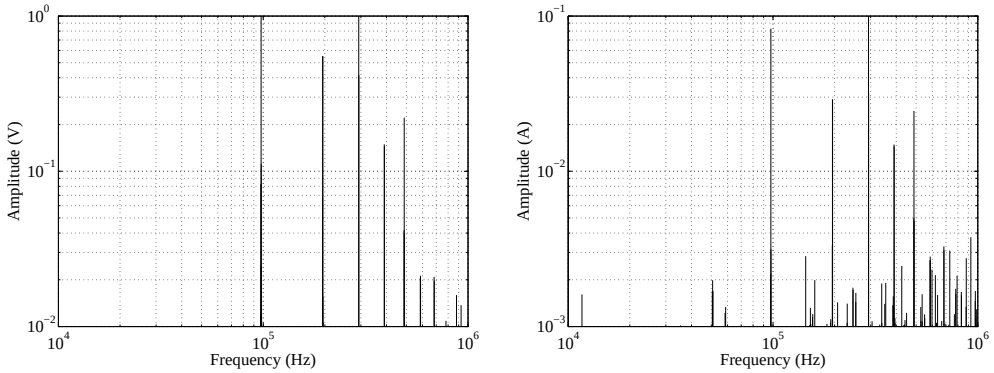


Figure 4.15: Scope snapshot: Shaft voltage and common-mode current FFT's of a conventional VSI at $OP6$ with ferrite clamp chokes.



(a) Shaft voltage at $OP6$ with choke (b) Common-mode currents at $OP6$ with choke

Figure 4.16: Experimental setup : Shaft voltage and common-mode current FFT's of a conventional VSI at $OP6$ with ferrite clamp chokes.

4.5 Elimination of common-mode currents in a dual two-level VSI

The ferrite bead clamp chokes needs to be connected to both ends of inverter for cancellation of common-mode noise (Fig..4.14(b)). If not, we can observe the common-mode current contribution from a single inverter. Even though the magnitudes of shaft voltage and high frequency common-mode currents have significantly decreased using dual two-level open-end winding drive, it can be further eliminated using ferrite bead clamps

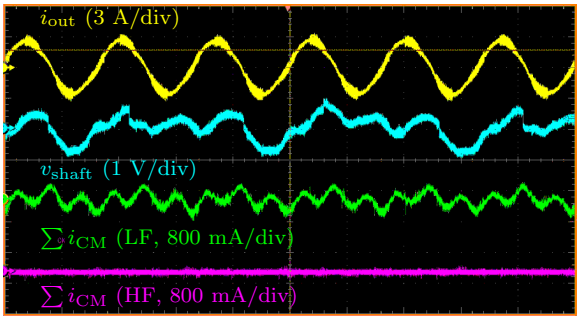
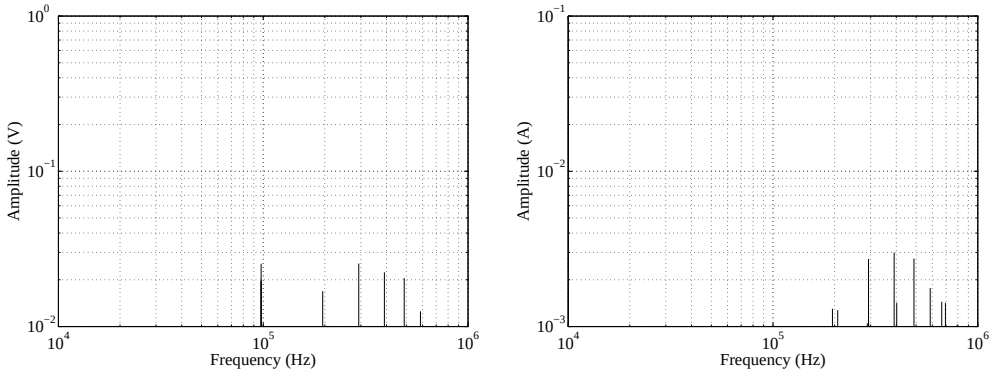


Figure 4.17: Scope snapshot: Shaft voltage and common mode current FFT's of a dual two-level open-end winding drive at $OP6$ with ferrite clamp chokes.



(a) Shaft voltage at $OP6$ with choke (b) Common-mode currents at $OP6$ with choke

Figure 4.18: Experimental setup : Shaft voltage and common-mode current FFT's of a dual two-level open-end winding drive at $OP6$ with choke

(Fig. 4.18(b)). It is also noted that the reduction in the magnitudes of common-mode currents in a conventional two-level VSI using ferrite bead clamps was not as significant when used with a dual two-level VSI (Fig.4.16(b)).

4.6 Conclusion

Near elimination of common-mode currents is achieved when a dual two-level VSI open-end winding drive is combined with ferrite bead clamps. It is observed that reducing

dead times helps us minimize the common-mode currents at higher switching frequencies. The next section discusses about losses of a conventional two-level and dual two-level VSI using Si and SiC switches.

Chapter 5

Comparison of Losses for a Si and SiC based Inverter

5.1 Introduction

For the past two decades there has been significant research on SiC MOSFETs based on 6H-SiC and 4H-SiC, for high voltage high frequency converter applications due to higher efficiency and high speed operation. Motor drive applications in high voltage electric vehicles have a voltage range from 300 V and 750 V [42]. To achieve high blocking voltage in Si MOSFETs , its n region must be lightly doped which results in higher ON-state resistance and limits the voltages below 300 V. On the other hand, Si IGBTs can be operated at 1200 V due to injection of electrons into the lightly doped n-region and reducing the forward voltage. IGBT's are optimal for high voltage and high power applications but operates at lower switching frequencies. Some drawbacks of using IGBT is the removal of accumulated charge in the drift region during reverse recovery [43]. This leads to high tail current which increases the turn-ON and turn-OFF losses. Another drawback is the positive temperature coefficient in IGBTs which makes it difficult to parallel [44]. SiC MOSFETs have negative thermal coefficient; which avoids thermal run-away; and no tail current [43].

This chapter focuses on comparing the conduction and switching losses of a conventional two-level VSI and dual two-level VSI using a Si IGBT [45] and SiC MOSFET [46]. The conduction and switching losses have been analyzed for different system conditions

Switching frequency	5 kHz , 20 kHz , 100 kHz
Output frequency	30 Hz , 60 Hz
Dead time	2 μs , 1 μs, 500 ns, 100 ns
Modulation index	0.25 , 0.51 , 0.9

Table 5.1: Simulation conditions for loss analysis

as stated in Table. 5.1. Due to the characteristics of the Si IGBT the switching frequency is limited to 20 kHz and dead time to 1 μs.The inverter is operated at a DC bus voltage of 200 V and the load connected to the inverter is a R-L load ($R = 10\Omega$ and $L = 46mH$).The losses are analyzed with respect to the switching frequency, output frequency and dead time. The loss analysis is done using the thermal modeling tool in PLECS. The assumptions made during the thermal modeling are as follows:

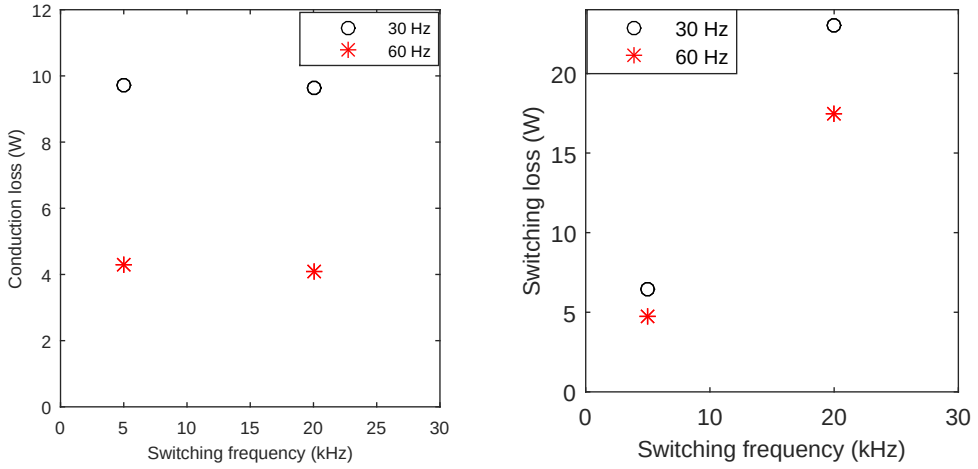
- The switch voltage is linearly proportional to the switching loss.
- The junction temperature is independent of switching loss.
- The diode losses of a SiC device is negligible.

In addition to these assumptions the effect of gate resistance and the gate driver losses have not been taken into account and the effect of output capacitance C_{oss} is not considered for loss calculations. The Cauer network for the thermal modeling of the heat sink in Plexim is subjected to inaccuracies.

5.2 Loss analysis of a Si based inverter

5.2.1 Two level inverter

The variation of conduction losses with respect to output frequency and dead time does not show a signifcant variation with it's increase as shown in Fig.5.1(a) and Fig. 5.2(a) respectively. It is also noticed that the switching losses decreases with the decrease in the output frequency (Fig. 5.1(b)). This is because as the output frequency increases the load current decreases.The switching losses with respect to dead time does not show a variation with change in the dead time (Fig. 5.2(b)). As the modulation index



(a) Conduction loss wrt output frequency

(b) Switching loss wrt output frequency

Figure 5.1: Conduction and switching losses of a Si based two-level VSI with respect to output frequency at m = 0.51 and dead time of 2μs

decreases the magnitude of the output voltage decreases hence the conduction losses and switching losses decrease (Fig. 5.3). It is observed that the conduction losses do not show a significant variation with increase in the switching frequency and the switching losses increases with the increase in switching frequency.

5.2.2 Dual two-level inverter

The losses of a dual two-level VSI will increase when compared to a conventional two-level VSI because the number of switches is doubled. There is an imbalance in the conduction losses as the lower IGBT's conducts two times more than the upper IGBT's. The switching transitions of a single leg in a dual two-level VSI doubles when compared to a conventional two-level. The conduction losses of a dual two-level VSI increases by almost two times when compared to the two-level VSI and The conduction loss wrt to output frequency shows a slight decrease with increase in output frequency Fig. 5.4(a)). The switching losses also decrease with the increase in output frequency as shown in Fig. 5.4(b). It is noted that the switching losses increases by one and a half times more when compared to a conventional VSI. The conduction losses shows a slight decrease with the decrease in the dead time (Fig. 5.5(a)). The switching losses on the other

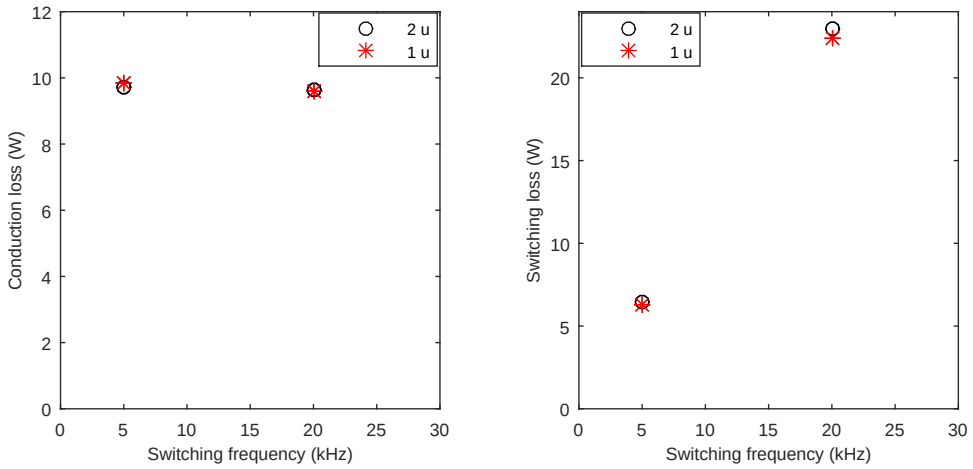
hand increases with the decrease in dead time as shown in Fog. 5.5(b). It is also observed that the conduction losses and switching losses increases with the increase in modulation index (Fig. 5.6). The conduction losses show a slight decrease with the increase in the switching frequency and the switching losses follows a similar trend as that of a conventional two-level inverter.

5.3 Loss analysis of a SiC based VSI

SiC MOSFET's have reduced switching and conduction losses when compared to Si IGBT's of similar rating. This is because of the numerous advantages of SiC based devices as stated in Chapter 1. For a SiC based VSI, loss analysis have been done at an higher switching frequency of 100 kHz and lower dead times of 100 ns and 500 ns.

5.3.1 Two level VSI

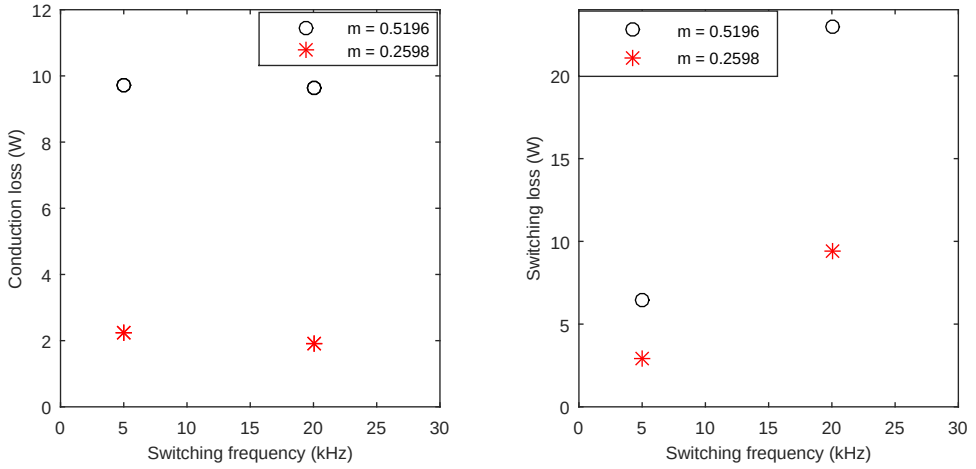
It is observed that the conduction losses and switching losses with respect to output frequency shows a slight decrease; when there is a increase in output frequency; up to frequencies of 20kHz and further decreases at higher switching frequencies (Fig. 5.7).



(a) Conduction loss wrt dead time

(b) Switching loss wrt dead time

Figure 5.2: Conduction and switching losses of a Si based two-level VSI with respect to dead time at m = 0.51 and f_o = 30Hz



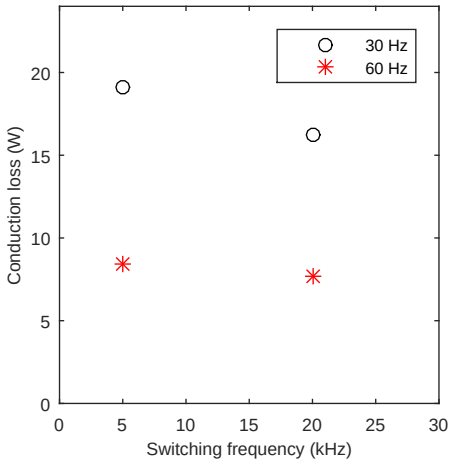
(a) Conduction loss wrt modulation index (b) Switching loss wrt modulation index

Figure 5.3: Conduction and switching losses of a Si based two-level VSI with respect to modulation index at $f_o = 30$ Hz and dead time of 2μs

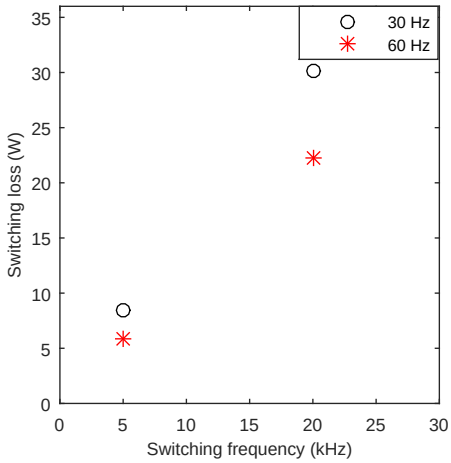
The variation of conduction losses with respect to dead time is shown in Fig. 5.8(a) shows that at higher switching frequencies and higher dead times losses are comparatively high. The trend observed in the switching losses (Fig. 5.8(b)) is similar to what is observed with conduction losses. The conduction loss and switching loss with respect to modulation index follows a similar trend to that of a Si based two-level VSI.

5.3.2 Dual two-level VSI

The losses of a dual two-level VSI increases when compared to a two-level VSI, similar to that of a Si based VSI. The conduction losses and switching losses show a decrease with the increase in the output frequency ((Fig. 5.10). The magnitude of conduction loss and switching loss increases by 2 times and $\frac{4}{3}$ times respectively. The conduction losses and switching losses wrt to dead time and modulation index follows a similar pattern as that of a SiC based two-level inverter (Fig. 5.11 and Fig. 5.12).It is also observed that the conduction losses show a slight variation in magnitude at higer switching frequencies..

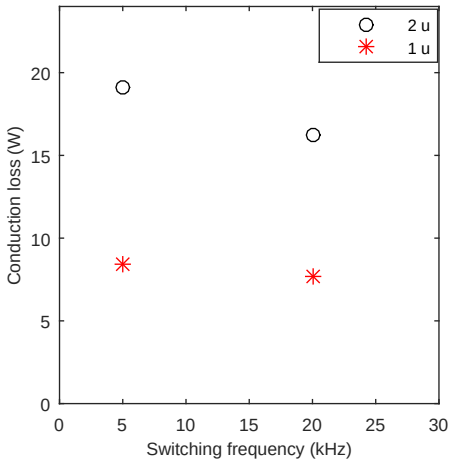


(a) Conduction loss wrt output freqeuncy

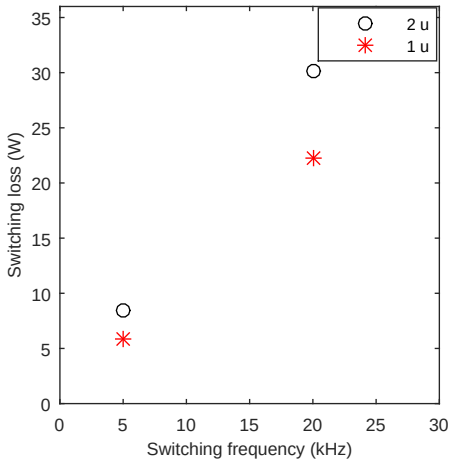


(b) Switching loss wrt output frequency

Figure 5.4: Conduction and switching losses of a Si based dual two-level VSI with respect to output frequency at m = 0.51 and dead time of 2μs

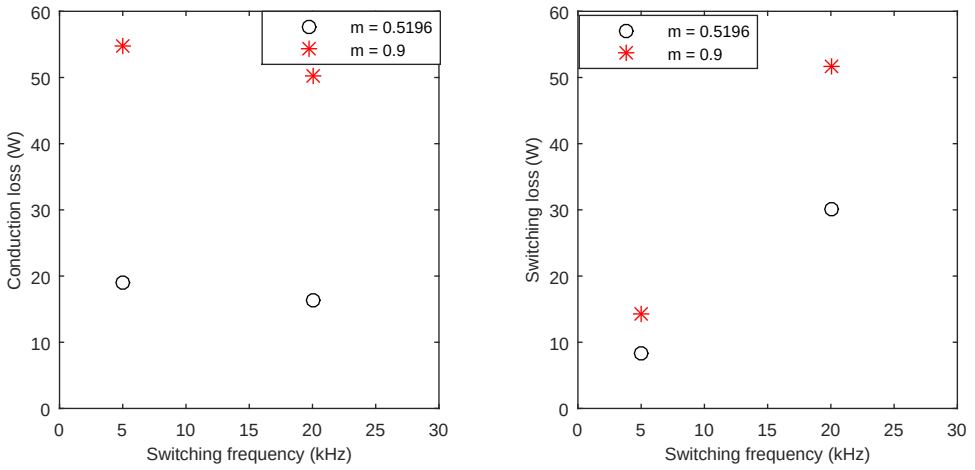


(a) Conduction loss wrt dead time



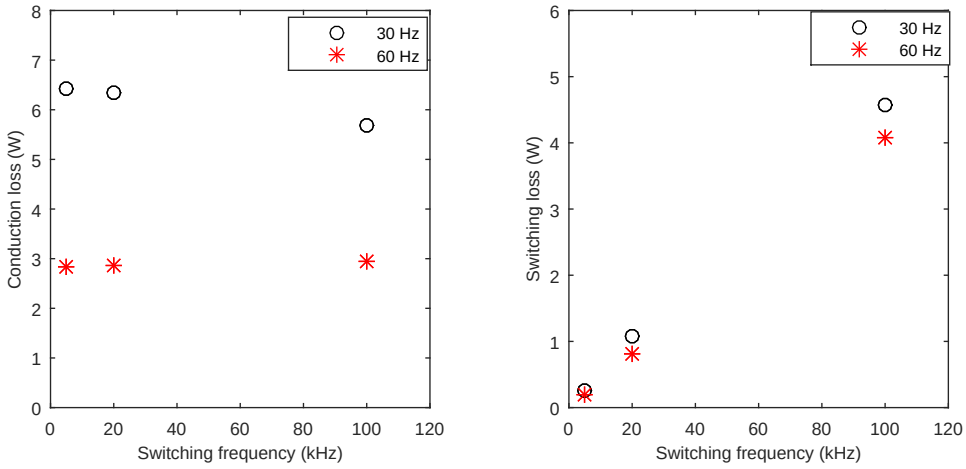
(b) Switching loss wrt dead time

Figure 5.5: Conduction and switching losses of a Si based dual two-level VSI with respect to dead time at m = 0.51 and f_o = 30Hz



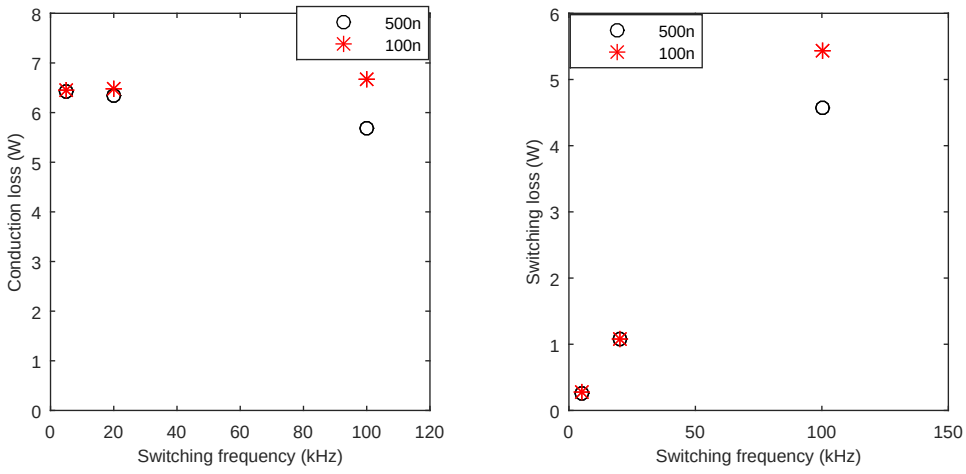
(a) Condcution loss wrt modulation index (b) Switching loss wrt modulation loss

Figure 5.6: Conduction and switching losses of a Si based dual two-level VSI with respect to modulation index at $f_o = 30$ Hz and dead time of 2μs



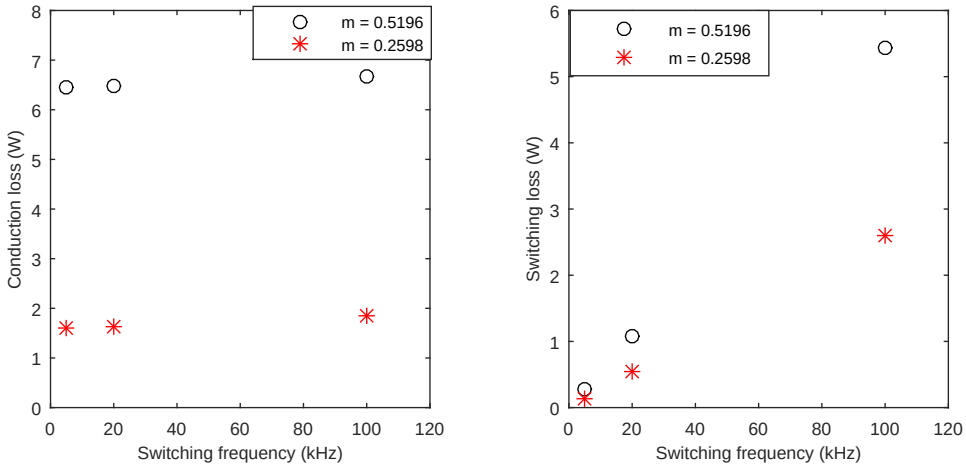
(a) (b)

Figure 5.7: Conduction and switching losses of a SiC based two-level VSI with respect to output frequency at m = 0.51 and dead time of 100ns



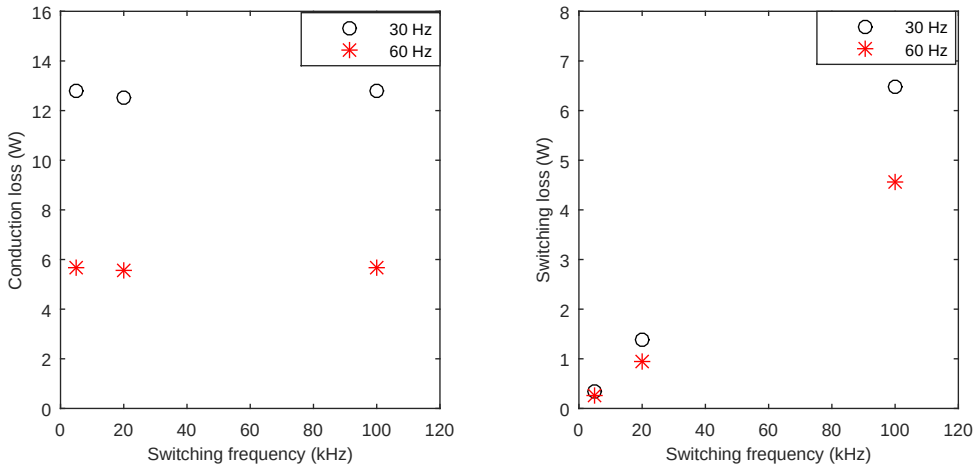
(a) (b)

Figure 5.8: Conduction and switching losses of a SiC based two-level VSI with respect to dead time at m = 0.51 and f_o = 30Hz



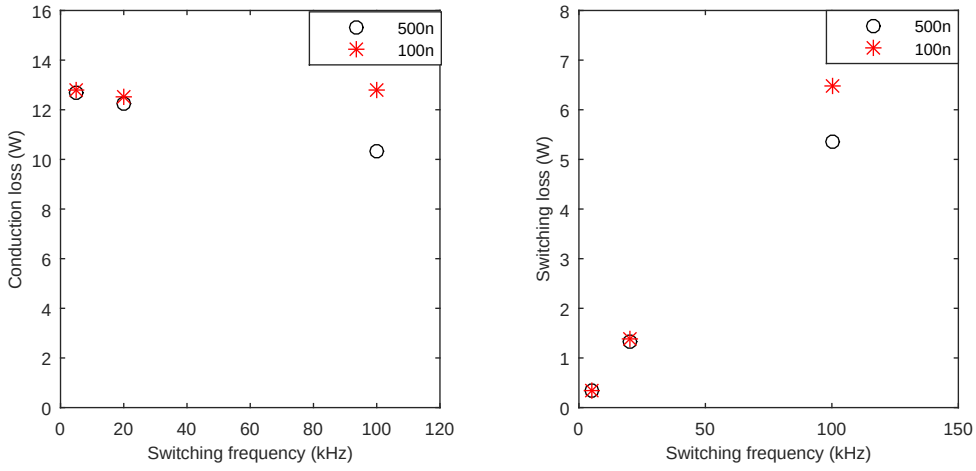
(a) (b)

Figure 5.9: Conduction and switching losses of a SiC based two-level VSI with respect to modulation index at f_o = 30 Hz and dead time of 100ns



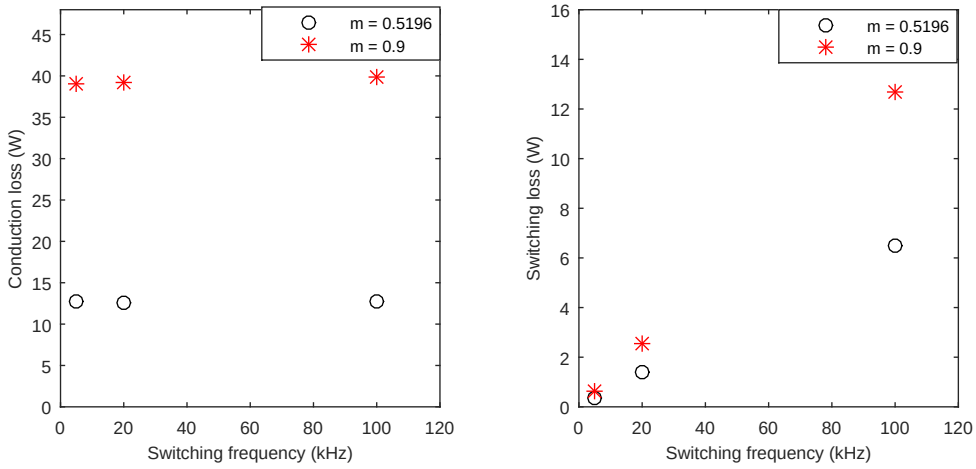
(a) (b)

Figure 5.10: Conduction and switching losses of a SiC based dual two-level VSI with respect to output frequency at m = 0.51 and dead time of 100ns



(a) (b)

Figure 5.11: Conduction and switching losses of a SiC based dual two-level VSI with respect to dead time at m = 0.51 and f_o = 30Hz

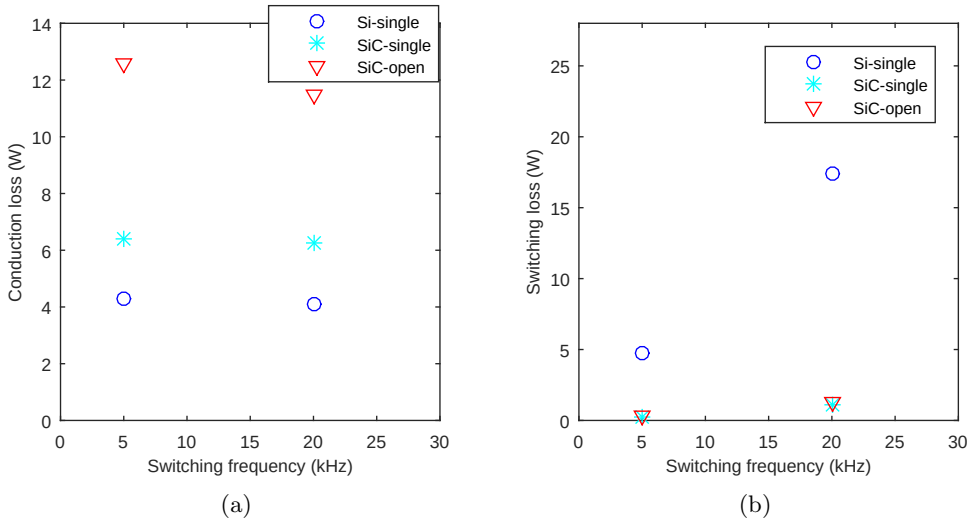


(a) (b)

Figure 5.12: Conduction and switching losses of a SiC based dual two-level VSI with respect to modulation index at $f_o = 30$ Hz and dead time of 100ns

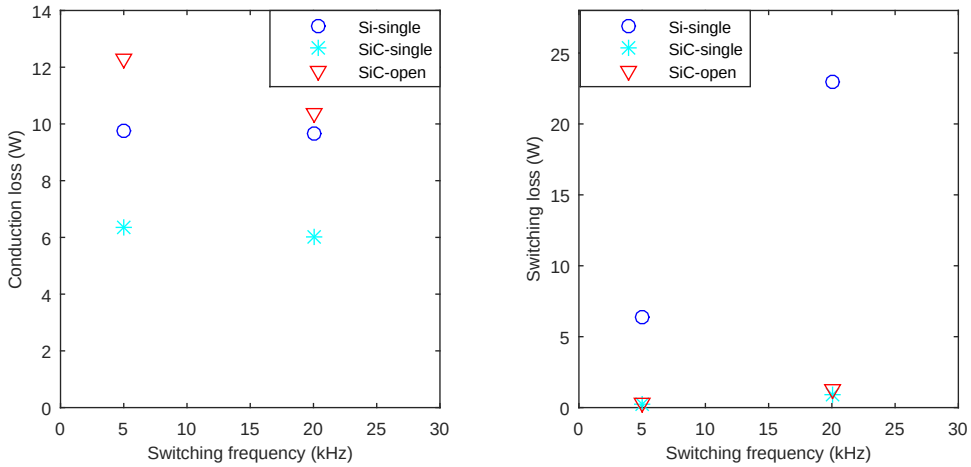
5.4 Comparison of Si and SiC VSI

The conduction and switching losses with respect to dead time of a Si based two-level VSi and SiC based two-level and dual two-level VSI have been compared in this section. It is observed that the variation in dead time does not impact the conduction losses for conventional two-level VSI's. There is a small reduction in conduction losses at higher switching frequencies for dual two-level VSI's. The magnitudes of the conduction and switching losses with respect to a Si based two-level inverter has reduced by one-third and one-fourth times respectively at similar switching frequencies.The dual two-level SiC based VSI has the maximum conduction losses while the two-level Si based VSI has the maximum switching losses. At any given frequency the two-level SiC based VSI performs better than the two-level Si VSI. Also, the SiC based dual two-level VSI performs better than a Si based two-level VSI. Thus, the SiC based dual two-level VSI has lower losses to the Si based two-level VSI. Hence the heat sink design for the SiC based dual two-level VSI will lead to smaller heat sinks when compared to a Si based VSI. This also shows that SiC based VSIs can be used for lower and higher range of switching frequencies for more compact and thermally efficient systems.



(a) (b)

Figure 5.13: Comparison of switching and conduction losses with respect to switching frequency at 1μs dead time



(a) (b)

Figure 5.14: Comparison of switching and conduction losses with respect to switching frequency at 2μs dead time

Chapter 6

Conclusion and Future Work

Common-Mode Voltage is a very significant issue with motor drive systems. Higher values of CMV results in shaft voltage build up, high frequency ground currents , electromagnetic discharge and EMI problems. The ground currents in particular result in premature failure of motors due to high common-mode noise. Mitigation techniques using active/passive filters and several various modulation techniques have been implemented to eliminate CMV. Hardware solutions of shielded cables , shaft grounding brush etc have also been implemented. WBG based devices are in extensive research for the past two decades due to its innumerable benefits such as high switching speeds and faster switching rates. The ability to operate at higher junction temperatures and reduced switching losses makes it possible to generate a thermally efficient system. This thesis focuses on discussing the advantages and disadvantages of using WBG based device in a motor drive system. It is observed that the WBG devices are expected to have more pronounced common-mode related issues. The reduction in dead-time does not bring a significant change in the shaft voltage or ground currents for a conventional two-level VSI. It is also noted that for a Si based device which has slower switching rate leads to less spurious ground current effects. Due to higher switching frequencies, clamp-on ferrites may be used to reduce the common-mode currents; a potentially simpler and cost effective solution compared to common-mode chokes. These require additional space and impose constraints on the type of cabling used for the drive. No special design of ferrite core was conducted to select these components. These were selected based on the frequency range the chokes would provide a common-mode impedance. Another

technique to reduce high frequency common-mode currents is the use of an open-end winding drive. This solution offers the benefit of reduction of CMV at the cost of additional switches and increase in losses. The open-end winding drive also have the presence of low-frequency common-mode currents (circulating currents) that occurs at the third harmonics of the output frequency. It is also observed that reduction of dead time in an open-end winding drive reduces the high frequency common-mode currents. Attenuation of common-mode currents were observed in a conventional VSI. But when a dual two-level VSI open-end winding drive combines with ferrite clamp chokes, a near elimination of high frequency common-mode currents is observed.

The losses of a Si based IGBT and a SiC based MOSFET in a conventional two-level VSI and dual two-level VSI have been analyzed and comparison plots have been provided. It is observed that SiC based devices have very low switching losses. When a SiC based conventional two-level VSI is compared to a dual VSI two-level topology the conduction show a significant increase and the switching losses remains almost similar, under the same operating conditions. At higher switching frequencies the losses of SiC based topology increases but the increase is not as significant as the losses produced using Si based topology. This limits the operation of Si IGBT's at higher switching frequencies.The losses of a Si based dual two-level VSI is extremely high compared to The other topologies. Hence, a comparison of Si based two-level VSI , SiC based two-level VSI and dual two-level VSI are analyzed for switching frequencies till 20kHz. The total losses at a switching frequency of 5kHz and 20kHz for an open-end winding drive is lower when compared to the losses of Si based conventional VSI under similar conditions. It can also be concluded that SiC based conventional two-level inverter is highly efficient than a Si based conventional two-level inverter. SiC based MOSFET's can be preferred for high efficiency and simpler heat sink designs. Therefore, the low losses in WBG devices, combined with high temperature ratings , a dual two-level VSI can be constructed at a small volume and weight with investment toward extended bearing life and reduced EMI. Even though, these are obtained at the cost of additional components, the problems due to common-mode noise is far more impact full.

6.1 Sources of Error

There can be error in measurements caused due to the current and voltage probes. Oscilloscopes could also contribute to additional measurement error. Another source of error is the sampling rate of the measurements. The loss modeling in PLEXIM have accuracy errors due to the assumption of switching losses not varying with temperature and being considered proportional to the voltage. The switching loss and conduction loss data interpolation can have errors as they are datasheet values. The Cauer network used for thermal modeling is subjected to inaccuracies.

6.2 Future Work

- Comparison of shaft voltage and high-frequency common-mode currents for a Si based conventional two-level VSI and dual two-level VSI.
- Discuss in detail about circulating currents of a dual two-level VSI open-end winding drive and implement pulse based dead time compensation in the modulation strategy to minimize circulating currents
- Model the parasitics of a motor and create a common-mode equivalent circuit for open-end winding drives and perform simulation analysis.
- Hardware results of loss analysis of Si and SiC based conventional two-level and open-end winding drive.

Chapter 7

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