# Modeling and Fabrication of Low Power Devices and Circuits Using Low-Dimensional Materials

A DISSERTATION

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# Dedication

To my father, Uttam H. Kshirsagar who first introduced me to the field of electrical engineering, and ensured my academic and intellectual development.

To my mother, Vidya U. Kshirsagar for her care and support.

To my brother, Omkar U. Kshirsagar for his sincere encouragement.

To my sister, Gayatri A. Dasari for her constant confidence in me.

I can think. I can wait. I can fast. - Siddhartha by Hermann Hesse

# Abstract

As silicon approaches its ultimate scaling limit as a channel material for conventional semiconductor devices, alternate mechanisms and materials are emerging rapidly to replace or complement conventional silicon based devices. Attractive semiconducting properties such as high mobility, excellent interface quality, and better scalability are the properties desired for materials to be explored for electronic and photonic device applications. Two of such approaches are studied in detail using modeling, to understand and explore alternative semiconductor devices in particular for low power applications. Hybrid III-V semiconductor based tunneling field effect transistors (TFETs) can provide a strong alternative due to their attractive properties such as subthreshold slopes less than 60 mV/decade, which can lead to aggressive power supply scaling. Here, InAs/SiGe/Si based TFETs are studied in detail. Simulations predict that subthreshold slopes as low as 18 mV/decade and on currents as high as 50 μA/μm can be achieved using such a device. However, the simulations also show that the device performance is limited by (1) the low density of states in the source which induces a trade-off between the source doping and the subthreshold slope, limiting power supply scaling, and (2) direct source-to-drain tunneling which limits gate length scaling. Another approach to explore low power alternatives to conventional semiconductor device can be to use emerging two-dimensional (2D) materials. In particular, the transition metal dichalcogenides (TMDs) are promising material group that, like graphene, these material exhibit 2D nature, but unlike graphene, have a finite band gap. This latter feature makes them an excellent alternative material for

electronic and photonic applications. One such material, $MoS_2$, is studied and modelled for low power device and circuit applications. In this work, the off-state characteristics are modelled for $MoS_2$ MOSFETs (metal–oxide–semiconductor field-effect transistors), and their circuit performance is predicted. $MoS_2$ MOSFETs have been fabricated and shown to exhibit subthreshold slope < 75 mV/decade showing that an excellent interface with high-K dielectric can be achieved. Due to its higher effective masses and large band gap compared to silicon it is shown that $MoS_2$ MOSFETs are well suited for dynamic memory applications. Two of such circuits, one transistor one capacitor (1TIC) and two transistor (2T) dynamic memory cells have been fabricated for the first time. Retention times as high as 0.25 second and 1.3 second for the 1T1C and 2T cell, respectively, are demonstrated. Moreover, ultra-low leakage currents less than femto-ampere per micron are extracted based on the retention time measurements. These results establish the potential of 2D $MoS_2$ as an attractive material for low power device and circuit applications.

# Table of Contents

# List of Tables

# List of Figures

# Chapter 1 :

# Introduction

## 1.1 Background

Since its emergence, one of the major limiting factors in semiconductor technology has been power consumption of the devices. Although silicon has been the dominant material among semiconductors, primarily due to its near perfect interface with $SiO_2$ and its abundance in nature, the type of technology used for making devices and circuits using silicon is driven primarily by power consumption of the devices and circuits. Although most of the power delivered to the circuits is used in either digital, analog or RF operations, some of the energy delivered by the power source also gets converted into heat dissipation through Joule heating and other mechanisms. Therefore, power consumption also leads to heat dissipation in the circuits, and both active and passive leakage power have become important. As shown in Figure 1-1, the transition from bipolar to complementary metal oxide semiconductor (CMOS) technologies has been driven by a need to control power consumption, and in particular, leakage power. However, today, power consumption in state of the art CMOS technology is currently reaching the same heat flux density as prior generations of bipolar technology. Therefore, it is expected that there needs to be a similar radical change in technology that will enable reduction in power consumption and heat

dissipation of the chip. There are various potential solutions that are being explored to enable reduced power consumption, which will be discussed latter in this chapter.

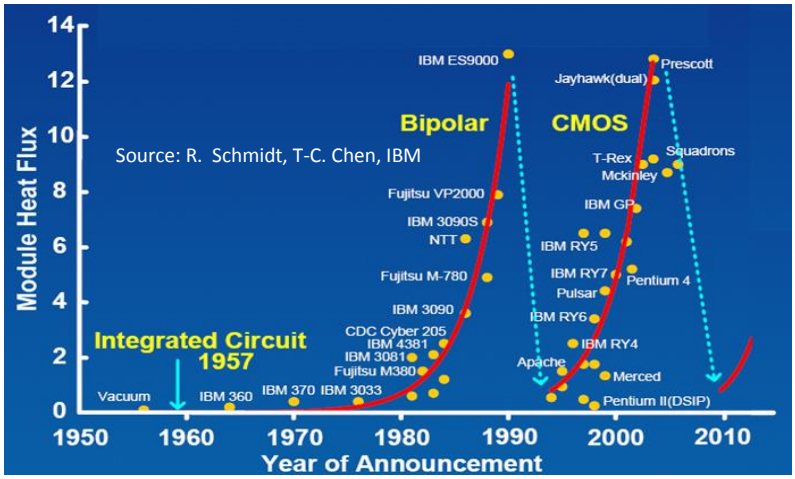



**Figure 1-1:** Plot of module heat flux vs. time for logic integrated circuit technologies. The exponential increase in heat flux density, over time, eventually has led to change in technology [1]. © 2004 IEEE.

The comparison of this exponential increase in power dissipation with scaling with some of the power density levels is shown in Figure 1-2. It can be seen that current state of the art technology leads to power density (and therefore heat generation) that is comparable in density to that of a rocket nozzle. Therefore, there is a sense of urgency in tackling this problem and coming up with ways to curb this power consumption at various levels, including the device, circuit and architectural levels.

The need for low power consumption also arises due to the proliferation of mobile applications. For these applications, low power consumption leads to longer battery life. With computing and communicating devices becoming more and more mobile, demand for longer battery life is increasing.

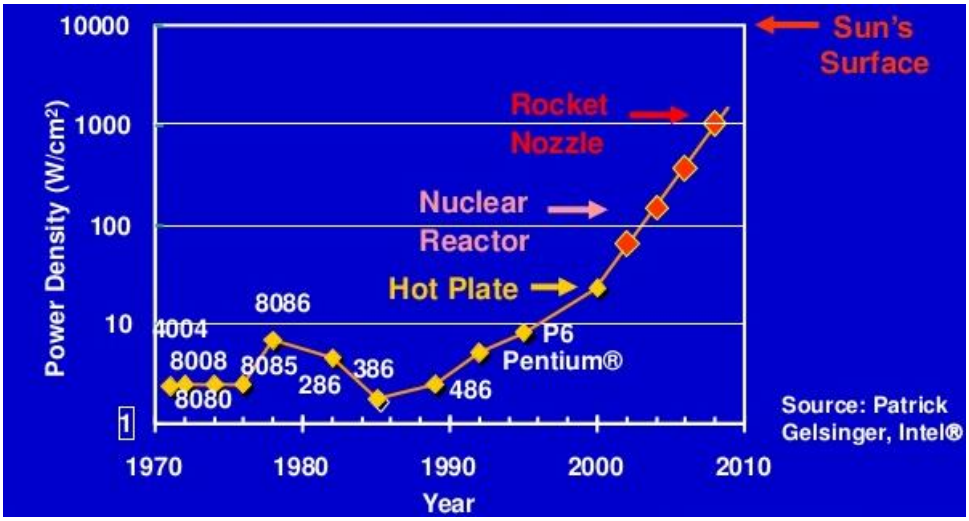



**Figure 1-2:** Plot of power density vs. time for various Intel microprocessor technologies. The increase in the power density trend begins to approach fundamental limits [2]**.** © 2001 IEEE.

Although historically most of the power consumption occurs due to operation of the logic part of the circuits, the need for low-power devices extends beyond logic devices. Memory components of processors / controllers can benefit from low power devices as well. Low power devices can also find applications in a range of non-conventional emerging electronics products which include wearable electronics, flexible electronics, medical devices, as well as some defense and space applications.

## 1.2 Low Power Electronics

There are two major factors of power consumptions: active power consumption and passive power consumption. Active power consumption is mainly due to charging and discharging of capacitive elements in the circuit, while passive power consumption arises due to the

imperfect nature of the devices used as switches. Since the logic part of the system involves more data operations and transitions, logic components are usually dominated by active power consumption. On the other hand, memories are mainly used for storing the data, making static power consumption the primary concern.

One of the important factors in power consumption is reducing the power supply itself. As power consumption is dependent on voltage supply as follows:

$$P = \alpha C V_{DD}^2 f + V_{DD} I_{leak}\,, \tag{1-1}$$

where,

$P$ = Power consumed per transistor

$\alpha$ = Activity factor

$C$ = Switched capacitance in the circuit

$V_{DD}$ = Supply voltage

$f$ = Clock frequency

$I_{leak}$ = Leakage current

The first term in equation (1-1) represents the dynamic power consumption, while the second term is the static power consumption. It can be observed that scaling the supply voltage, $V_{DD}$, can reduce both components of the power consumption.

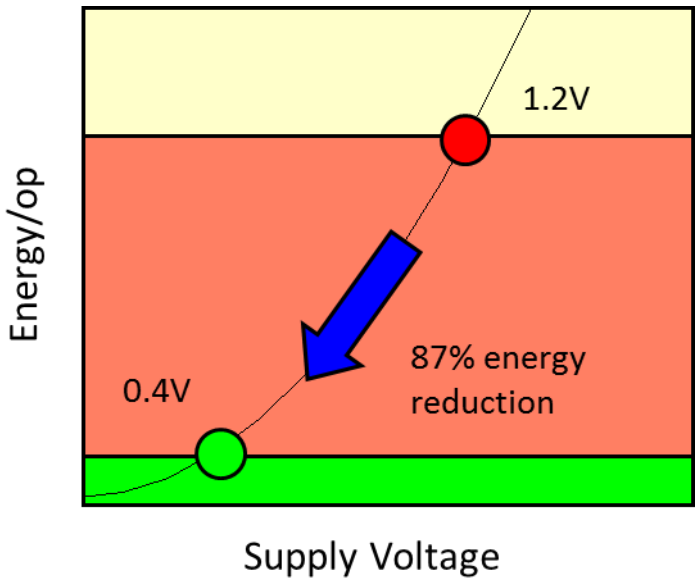



**Figure 1-3:** Plot of active energy vs. supply voltage. The plot shows that supply voltage scaling can lead to substantial reduction in power consumption. For instance, reducing the supply voltage from 1.2 V to 0.4 V can reduce active power consumption, and hence the energy per operation by 87 %.

As shown in Figure 1-3, reducing $V_{DD}$ from 1.2 V to 0.4 V can reduce dynamic power consumption by 87%. However, the reducing power supply without improving subthreshold leakage of the device can lead to an exponential increase in static power consumption in the form of increased leakage current. Therefore, a solution to the power problem must lead to a device that would allow $V_{DD}$ scaling without increasing leakage.

There are various approaches at different levels being explored in order to tackle the power consumption problem (Figure 1-4). At the device level, new materials and new device principles are being explored. At the circuit level multi $V_{th}$ and other new circuit architectures are being tried. While at architecture level, multi-core design and matching of computation and architecture can be employed. In this thesis, device-level solutions to the power consumption problem are developed.

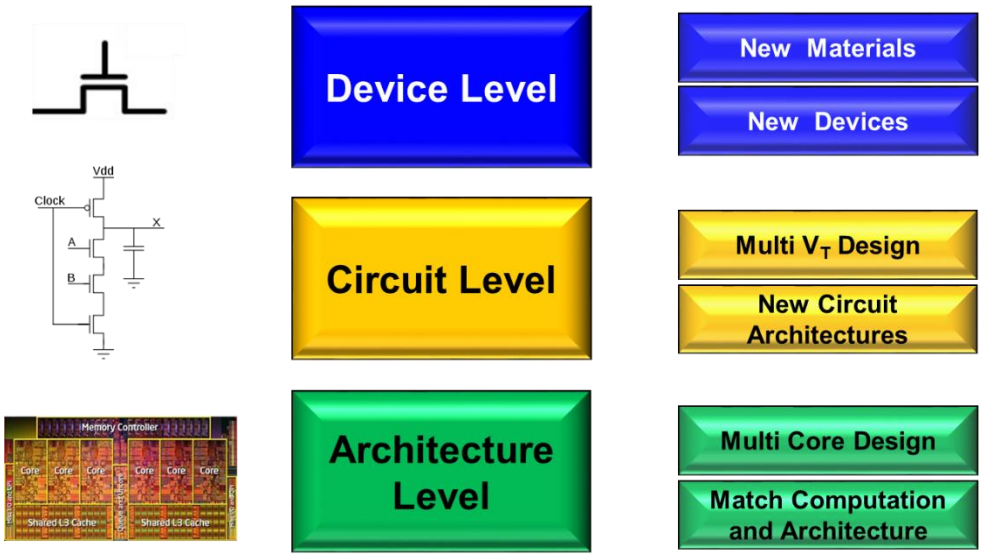



**Figure 1-4:** Approaches to tackle power consumption, efforts are being made at architecture, circuit and device level to reduce power consumption.

The challenge to reducing power consumption in scaled MOSFETs is control and minimization of various sources of leakage currents that occur in the off-state of the transistor. Some of the most important components of off-state leakage in MOSFETs are:

1. Sub-threshold leakage
2. Gate leakage
3. Gate induced drain leakage
4. Generation / recombination

Each of these components is described briefly below.

**1.2.1 Subthreshold Leakage:** Ideally, it would be desirable if a transistor could turn off abruptly below the threshold voltage (as shown in green curve in Figure 1-5). However, due to the thermionic nature of the turn-off mechanism, the turn off is limited by thermionic

emission of carriers leading to a finite voltage swing needed to turn off the transistor. The slope of the drain current vs. gate-to-source voltage ($I_{DS}$-$V_{GS}$) curve at a voltage below threshold is termed the subthreshold slope, and it can be shown that at room temperature, the subthreshold slope is limited to a maximum value of 60 mV/decade as shown in equation (1-2). Here $k$ is Boltzmann's constant, $T$ is temperature and $q$ is charge. This slope can degrade depending on the presence of trap charges at the interface, and parasitic capacitance as shown in equation (1-3). Here, $C_d$ is depletion layer capacitance, which includes the interface density traps and $C_{ox}$ is the gate oxide capacitance.

$$SS = \frac{10 \times I_{DS}}{I_{DS}} = \frac{kT}{q}\ln(10) = (26mV) \times (2.303) \approx 60\, mV/Dec \tag{1-2}$$

$$SS = \frac{kT}{q}\ln(10)\left(1 + \frac{C_d}{C_{ox}}\right) \tag{1-3}$$

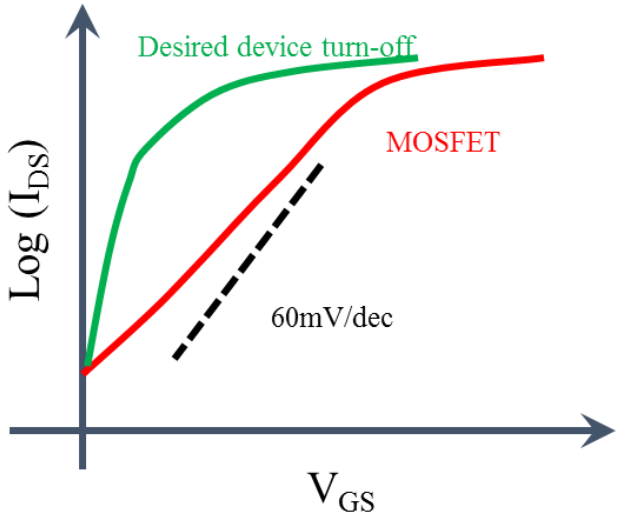



**Figure 1-5:** Sub-threshold leakage, desired vs achievable, steeper subthreshold slope can enable aggressive supply voltage scaling.

**1.2.2 Gate Leakage:** As scaling progressed during the last few decades, all dimensions, including gate oxide thickness have scaled down proportionately. With aggressive scaling, we are in the regime where gate oxide can be only few atomic layers thick. In such thin oxides, quantum mechanical effects can become an important factor. Specifically, direct tunneling from the gate contact into the channel can be a major contributor to off-state leakage. This gate leakage can be composed of both direct tunneling and Fowler-Nordheim (FN) tunneling components. As shown in Figure 1-6, direct tunneling occurs through a thin oxide, while FN tunneling occur in presence of high electric field through the triangular barrier. While new dielectric materials such as high-k dielectric with metal gate (HKMG) have been introduced to minimize leakage currents and enable gate oxide scaling, direct tunneling from the gate into the channel still remains a challenge.

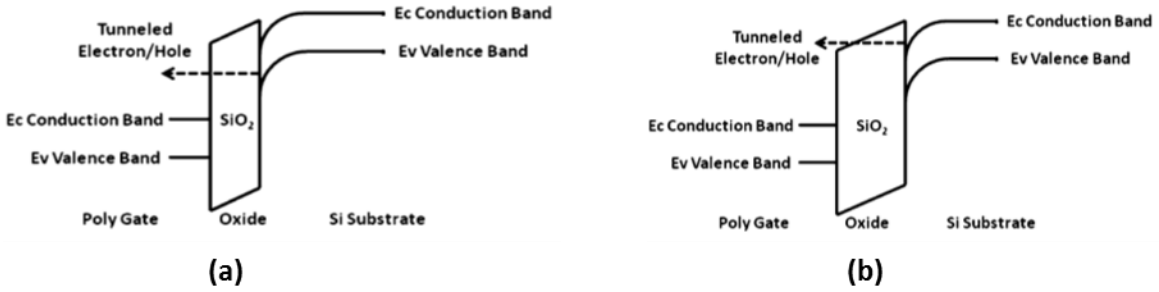



**Figure 1-6:** Gate leakage mechanisms, (a) Direct Tunneling (b) Fowler-Nordheim tunneling [3]. With permission of Springer.

**1.2.3 Gate Induced Drain Leakage:** Another important component in the off state of a transistor is gate induced drain leakage (GIDL). As the name suggests, this leakage is induced by the gate bias and manifests as excessive drain current caused by band-to-band tunneling from the drain into the channel. As the gate voltage is lowered, the valance band

of the channel region is slowly pulled up by the gate voltage. When the valance band of the channel region crosses over the conduction band of the drain region, the band-to-band tunneling probability from the drain into the channel increases. As more electrons undergo band to band tunneling, the drain leakage increases.

**1.2.4 Generation/Recombination Current:** Even though generation / recombination current component is usually not important in conventional fully-depleted silicon devices, it cannot be ignored in the limit of extremely low leakage currents. Especially in the case of alternate materials that are being explored, this component can also play a role in leakage current. In the off-state of a MOSFET, generation within the channel-to-drain junction can occur. In particular, if defects are present, then the Shockley-Read-Hall (SRH) mechanism can dominate where generation occurs through localized states such as deep level traps. This will be discussed more in chapter 4.

## 1.3 Potential Solutions

There can be two prominent approaches to tackle the power consumption issue and to design devices and circuits to consume less power. One way is to explore new operating mechanisms and new phenomenon to improve performance radically (Figure 1-7). Some physical phenomenon such as quantum mechanical tunneling[4][5] and impact ionization[6][7] can lead to subthreshold characteristics that are not limited by thermionic limit of 60 mV/decade[8]-[11]. Mechanical properties can also be used to make mechanical switches with steep switching behavior. Some recent developments such as negative

capacitance[12] can also be utilized for low power device applications. Another approach towards solving power consumption issue is to use better electrostatics or new materials that will lead to more ideal subthreshold behavior leading to lower power consumption while keeping the operating principle the same[13]-[15]. One can also use more than one approaches to obtain better and improved results for low power applications. For instance, better electrostatics can be employed along with use of new operating mechanism to give even better performance.

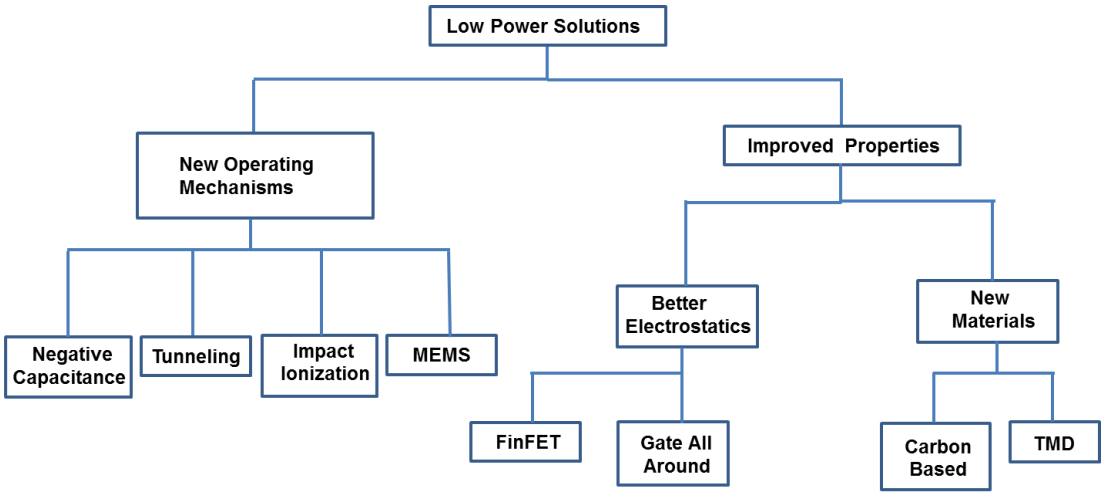



**Figure 1-7:** Possible approaches and alternatives at device level to reducing power consumption. Various approaches can also be combined for more effective solution.

## 1.4 Research Objectives

The research objective of this thesis are to explore low power devices using nanoscale materials through simulation and experiment and evaluate them for realistic applications. This thesis aims at exploring some of those, and recommend one or more of them objectively. A simulation / modelling based approach is developed to estimate performance enhancement using various methods, and based on the results, circuit performance can be

predicted as well. Finally, a process can be developed to fabricate the devices and circuits in most reliable way to validate the predicted performance advantages.

## 1.5 Outline of the Thesis

This thesis is organized as follows. A brief introduction to concepts and the problem is given in this chapter. Chapter 2 describes a tunneling field-effect transistor (TFET) based approach towards achieving a low power device. This includes modelling an InAs / SiGe/Si based TFET, and estimating is performance limitations. Chapter 3 serves as a bridge into the other approach toward achieving low power devices. It introduces various low dimension materials, and their features and potential applications. Chapter 4 discusses one such material ($MoS_2$) and predicts its circuit performance based on a developed model. Chapter 5 elaborates on process development, device optimization, fabrication and DC characterization of devices and circuits based on $MoS_2$ as the channel material. Chapter 6 reports experimental results of such $MoS_2$ based devices and circuits. Detailed discussion and analysis of the results are also presented. Finally a summary of the thesis and future work are presented in chapter 7.

# Chapter 2 :

# Hybrid III-V/SiGe Tunneling Field Effect Transistors

## 2.1 Motivation

As discussed in Chapter 1, one of the approaches towards achieving low power consumption is to use devices that have improved turn off characteristics. This can be achieved by using a new operating mechanisms instead of a conventional thermionic emission based approach. One such physical phenomenon that can be utilized in achieving better turn off is quantum mechanical tunneling.

The device that utilizes quantum mechanical tunneling and in turn provides better turn off and lower power consumption is called a tunneling field-effect transistor (TFET)[10] [11]. TFETs typically have source-channel-drain doping configuration that is either p-i-n or n-i-p, where the doping of the drain region defines the operation type (n- or p-type) of the TFET device. For instance, an n-i-p device will exhibit p-type FET characteristic. The operation of a TFET is explained in Figure 2-1. Here, as in the case of MOSFETs, the gate voltage controls the potential in the channel region. However, instead of relying on thermionic emission of carriers, TFETs operate based on band-to-band tunneling from the source into the channel. As the gate voltage is reduced the Fermi-Dirac distribution function in the source is filtered by the band gap of the material in the source. This allows the turn-off of the device to be steeper than 60 mV/decade, since the filtering of the “tail”

of the distribution function eliminations the $kT/q$ factor as in case of conventional MOSFET. Therefore, TFETs are not limited to 60 mV/dec subthreshold slope.

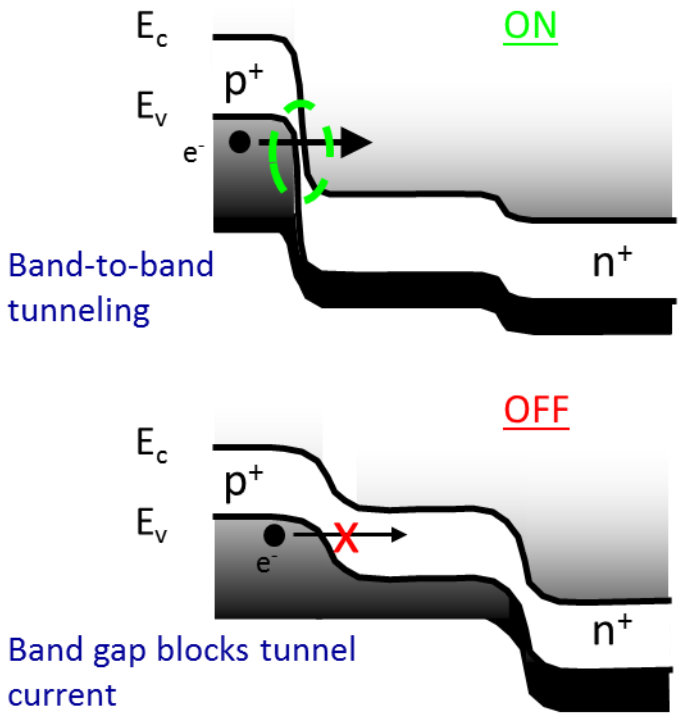



**Figure 2-1:** Operating principle of an n-type tunneling FET. Carriers tunnel into channel from source when device is on, while the bandgap of the material filters out the Fermi-Dirac distribution function from the source when the device is turned off.

TFETs are of great interest for advanced logic applications due to their potential for sub-60-mV/decade subthreshold slope. This could enable supply voltage scaling beyond what is practical for conventional MOSFETs. However, TFETs based upon tunneling in Si suffer from low on current, $I_{ON}$, and fail to provide steep slope at high current levels [16] [17]. III-V TFETs are more promising due to their potential for high drive current, but the poor gate oxide quality remains a significant challenge [18]–[22]. To address these limitations, a hybrid III-V-on-Si approach [23] had been proposed as a potential solution

to this problem, whereby the small effective band gap, $E_{geff}$, of the InAs/Si heterojunction could increase $I_{ON}$, while preserving the high-quality Si/dielectric interface in the channel. Experimental demonstrations of nanostructured InAs-on-Si Esaki diodes and TFETs suggest this approach is feasible (Figure 2-2) [23][24]. In that work, InAs nanowires were grown using selective epitaxy on a silicon substrate within a confined area. Furthermore transistors made using these III-V / silicon based nanowires were also demonstrated, but the performance was non-ideal. Therefore, this brings about the question of whether or not this hybrid TFET concept could be improved to provide the performance needed for practical applications. The remainder of this chapter explores that possibility.

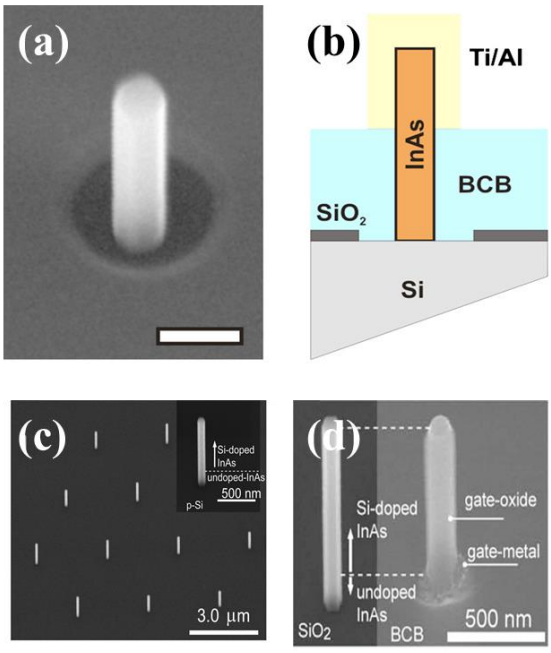



**Figure 2-2:** Prior fabricated devices based on hybrid III-V/Si diodes and TFETs, (a) Scanning electron micrograph of a vertical as-grown InAs nanowire on a Si substrate, (b) Schematic cross section of a Si–InAs heterojunction diode [23],(c) SEM image of vertical InAs NWs with n+-InAs/undoped axial junction on p+-Si substrate, (d) SEM image of InAs-Si based TFET [24]. Reproduced with permission from [23, 24]. Copyright [2010, 2011], AIP Publishing LLC.

## 2.2 Channel Material and Device Parameters

There are several parameters that need to be carefully chosen during designing device for certain applications including the channel material, geometry, and source doping profile. As discussed above, InAs-on-Si heterostructures still exhibit relatively large $E_{geff}$ (~ 0.4 eV in unconfined geometries) and quantum effects increase $E_{geff}$ substantially in confined geometries. Therefore, in this work, SiGe is proposed as a channel material to reduce $E_{geff}$ and thus provide improved performance compared to prior work. A nanowire geometry is utilized similar to the prior demonstration, but leads to quantum confinement which needs to be accounted for in considering the band structure of the device. The effect of quantization was analytically calculated using the Schrödinger equation in cylindrical coordinates

$$-\frac{\hbar}{2m^*}\left(\frac{\partial^2}{\partial r^2}+\frac{1}{r}\frac{\partial}{\partial r}+\frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}\right)\psi(r,\theta)=E\psi(r,\theta) \quad \textbf{(2-1)}$$

The calculated Eigenstates were utilized to modify the material parameters in Synopsis Sentaurus Device™ to capture the effect of quantization in the nanowire. The figure below (Figure 2-3) shows the calculated value of $E_{geff}$ as function of Ge fraction as well as the nanowire diameter. It can be seen that $E_{geff}$ can be substantially reduced using SiGe as the channel material.

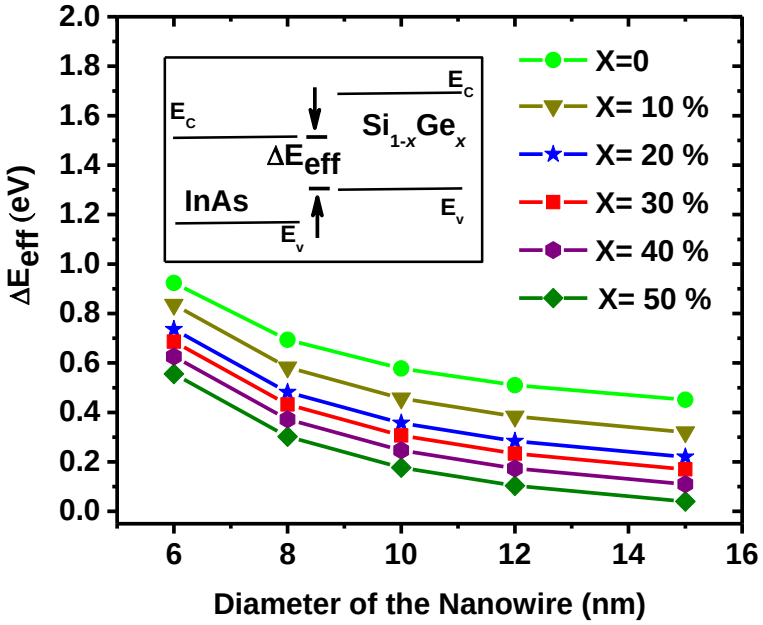



**Figure 2-3:** Calculated InAs/$Si_{1-x}Ge_x$ effective band gap, $E_{geff}$, vs. diameter for different Ge fraction ($x$). It can be observed that increasing Ge fraction can reduce effective band gap substantially.

In terms of geometry, a gate-all-around device structure provides for superior electrostatic control of the channel compared to planar or double-gate geometries. Therefore, a nanowire p-TFET geometry with an InAs source, $Si_{1-x}Ge_x$ channel and Si drain was considered (Figure 2-4).

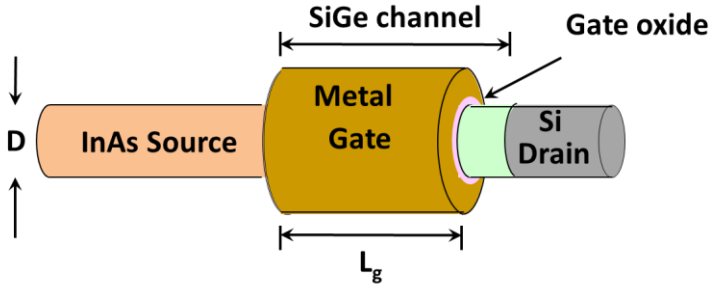



**Figure 2-4:** Schematic diagram of a simulated device structure. Device consists of InAs source, SiGe as the channel material, and silicon as the drain. Various parameters considered in the device simulations are in the table below.

| Parameter | Range of the values |
|---|---|
| Source Doping (n) | $1 \times 10^{18}$ $cm^{-3}$ – $2 \times 10^{19}$ $cm^{-3}$ ($5 \times 10^{18}$ $cm^{-3}$) |
| Channel Doping (p) | $1 \times 10^{15}$ $cm^{-3}$ |
| Drain Doping (p) | $1 \times 10^{21}$ $cm^{-3}$ |
| Gate dielectric thickness ($t_{ox}$) | 1 nm |
| Gate Length ($L_g$) | 20 nm |
| Diameter (D) | 6 nm – 15 nm (10 nm) |
| Composition (X) | 0 – 50 % (50 %) |

**Table 2-1:** Structural parameters utilized for InAs/SiGe/Si TFET device simulation shown in Figure 2-4. The values in bracket indicates the parameter values for a nominal device.

In the initial simulations, source doping concentration and channel Ge composition, *x*, were varied, while the other device parameters remained fixed. The nominal gate length, $L_g$, and the Ge composition, *x*, were fixed as 20 nm and 50%, respectively, while the remainder of the structural parameters are shown in the Table 2-1. Material parameters used for the modeling are listed in Table 2-2. To avoid ambipolarity, an underlap was provided between Si/SiGe interface and gate.

| Material | Parameter | Value |
|---|---|---|
| InAs | $m_c(\Gamma) / m_0$ | 0.023 |
| | $E_g$ (eV) | 0.354 |
| SiGe | $m_v$ (perp.) / $m_0$ | 0.28 - 0.23 |
| | $m_v$ (ll) / $m_0$ | 0.21 - 0.1 |
| | $E_g$ (eV) | 0.828 - 1.108 |

**Table 2-2:** Material properties considered in the simulation [6][7]. SiGe parameters are changed according to the Ge fraction in the SiGe.

Comprehensive 3D simulations were carried out using Synopsys Sentaurus Device™. A non-local tunneling model was utilized. Here, a hydrodynamic model for transport was

used, along with a non-local band-to-band model for tunneling. A multi-valley model along with non-parabolicity and density integral model were also employed to include the non-parabolicity of InAs. High field saturation and vertical electric field models are used to determine the mobility of the carriers. The InAs was assumed to be relaxed, while the SiGe was assumed to be under biaxial compressive strain. The relaxed state of InAs is reasonable considering the results in [23] and [14] that show that InAs grown on Si produces an array of misfit dislocations at fixed lattice spacing. Nonparabolicity and quantum confinement effects were computed analytically and the band parameters adjusted accordingly for a given nanowire diameter. Interface traps were not considered in this study, since an improved understanding of the physical nature of the SiGe/InAs interface traps is necessary in order to properly model their effect on carrier transport. As seen in Figure 2-5, using SiGe as the channel material instead of Si can greatly reduce the effective tunneling band gap, and therefore can increase tunneling current.

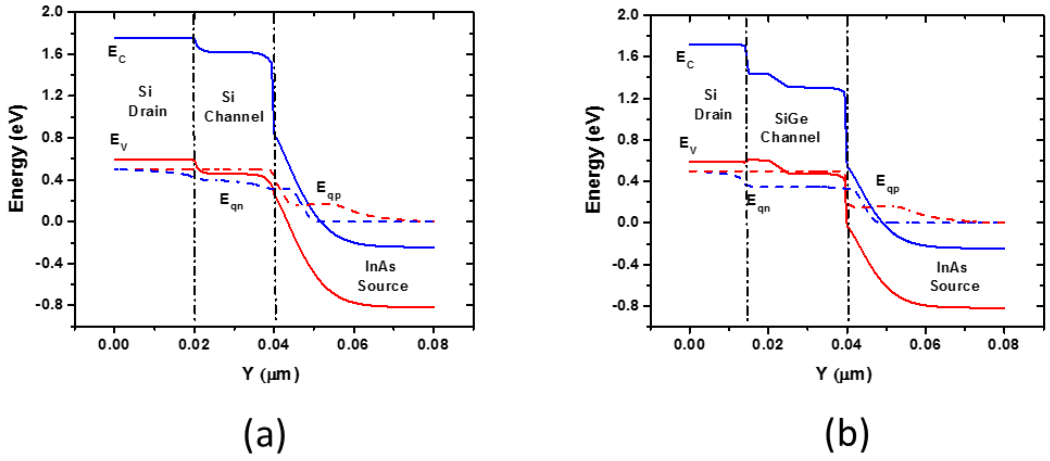



**Figure 2-5:** Band diagram of (a) Si – InAs device at on state (b) Si – SiGe -InAs device at on state. Substantial decrease in effective tunneling band gap can be observed by introducing SiGe as the channel material.

3D visualization of spatial variation and concentration of band-to-band tunneling based generation can be performed using technology computer aided design (TCAD). This can be seen in Figure 2-6 below. As expected, most of the tunneling is concentrated at the source and channel junctions.

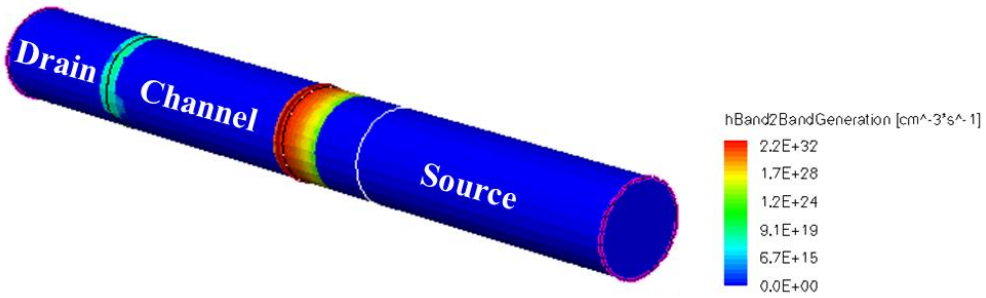



**Figure 2-6:** 3D visualization of band-to-band generation in various regions of the device. It can be observed that most of the tunneling based generation is near source and channel junction.

## 2.3 Results and Discussion

To understand the behavior of TFET device and to optimize its performance various simulation studies are conducted. First among these studies is the study of source doping on the device performance, followed by analysis of the Ge concentration dependence and finally a study of the geometric parameters on the device performance. Since source doping affects the degeneracy and in turn the device characteristics itself, it provides useful insight into the properties of the TFETs. The $I_{DS}$ vs. $V_{GS}$ curves for various source doping values based on TCAD simulations are shown in Figure 2-7. It can be observed that there are two

limiting constraints for these devices: on one hand, low doping reduces the $I_{ON}$ of the device, while on the other hand, and high doping degrades the subthreshold slope.

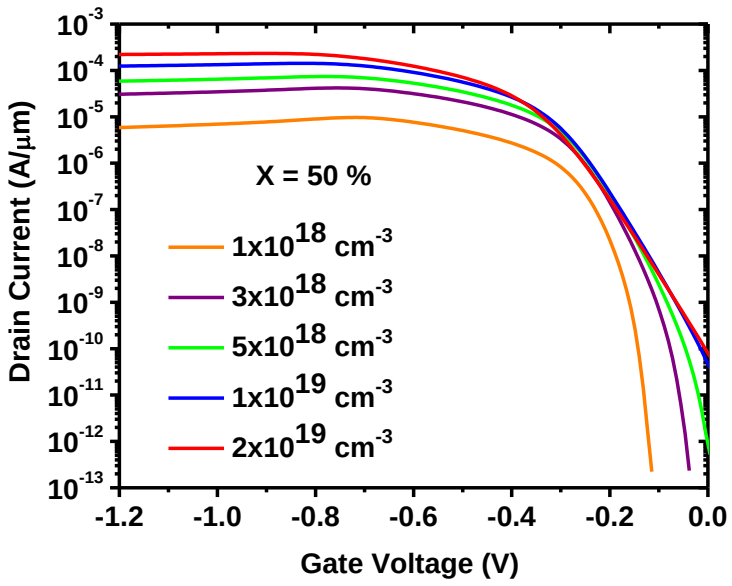



**Figure 2-7:** $I_{DS}$ vs. $V_{GS}$ for nominal device ($L_g$ = 20 nm and $x$ = 50%) for different source doping levels. It can be seen that *SS* degrades with increased doping level, while the on current improves with the increased doping level.

The reason for this behavior can be understood in Figure 2-8. When the source doping is low, the source resistance is high, and this also increases the depletion in the source induced by the gate electrode. These effects limit the maximum current that can be achieved. If the source doping is made higher, the series and tunneling resistance are reduced. However, particularly in InAs, the source can become highly degenerate at high doping concentrations. This is due to low density of states in InAs. As a result, tunneling current is dominated by carriers that are in the tail of Fermi-Dirac distribution, degrading the subthreshold slope of the device (Figure 2-8).

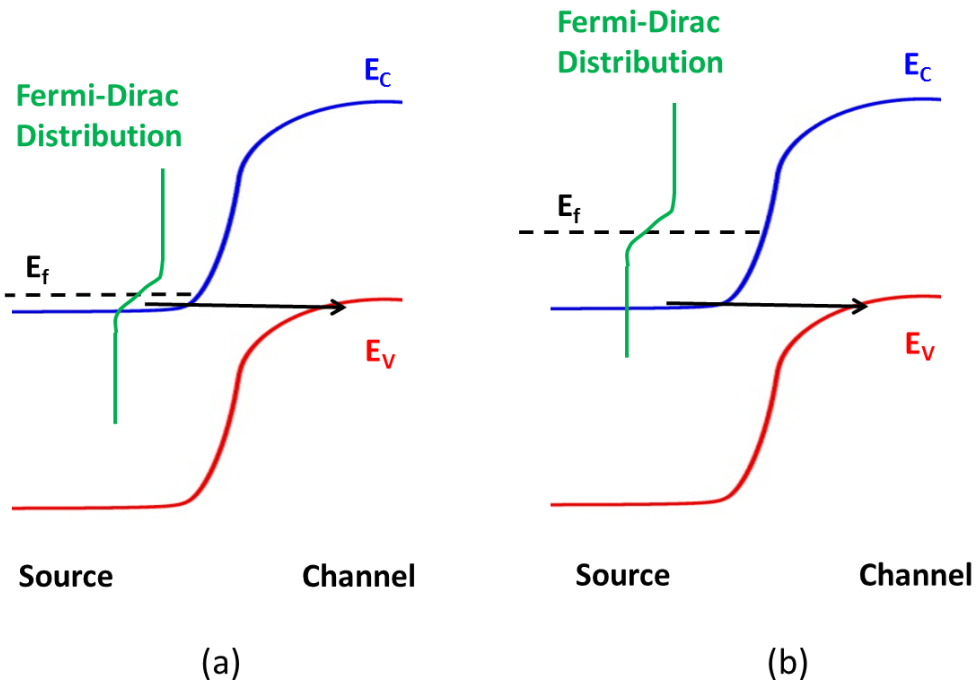



**Figure 2-8:** Effect of doping, (a) low degeneracy leads to carriers tunneling from center of the fermi function while (b) high degeneracy leads to carriers tunneling through *kT* dependent tail of the Fermi function, leading to degradation of subthreshold slope.

The source degeneracy effect can further be examined by analyzing the subthreshold slope at various currents and various doping level. Figure 2-9 shows the subthreshold slope vs. drain current at various source doping levels. It can be seen that, as the degeneracy is increased with doping, the subthreshold slope, *SS*, degrades from 18 mV/dec to the thermal limit of 60 mV/dec, at which point the Boltzmann "tail" of the Fermi-Dirac distribution dominates the tunneling current. Therefore, it is important to study the degeneracy effect of the source material of the TFETs, in particular in the case of p-TFETs as most of the n-type source materials tend to have lower density of states, leading to high degeneracy.

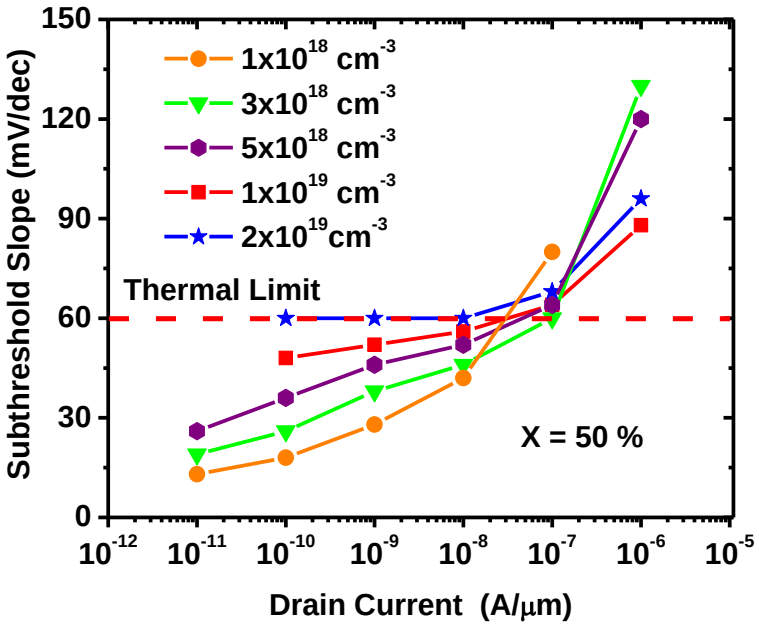



**Figure 2-9:** *SS* vs.log($I_{DS}$) for nominal device with different source doping levels. Strong degenerate doping limits *SS* to ~ 60 mV/dec.

Based on this analysis, one can expect this combined effect of subthreshold slope and on current trade of to reflect into $I_{ON}$-$I_{OFF}$ characteristics of the device. To confirm this, $I_{ON}$-$I_{OFF}$ characteristics of the device were examined. Figure 2-10 shows the $I_{ON}$-$I_{OFF}$ characteristic for various doping levels in the source. The plot shows that higher $I_{ON}$ at fixed $I_{OFF}$ is achievable with increased doping, at a $V_{DD}$ = 0.5 V. However, when $V_{DD}$ is reduced to 0.25 V, the trade-off between source degeneracy and depletion leads to an optimum source doping level, as shown in Figure 2-11. This shows that at very low power supply voltages, there is an optimum doping level that gives best $I_{ON}$ at a fixed $I_{OFF}$. This highlights the importance of doping-dependent degeneracy effects, and their impact on device characteristic.

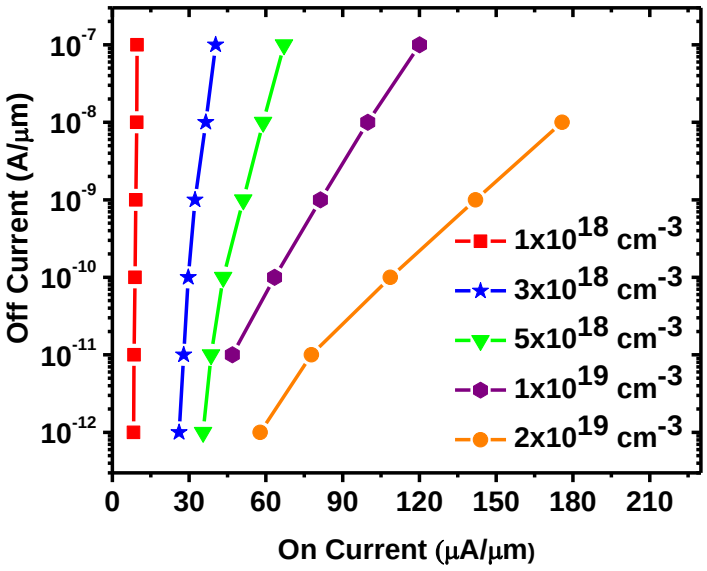



**Figure 2-10:** Plot of log ($I_{OFF}$) vs. $I_{ON}$ at $V_{DD}$ = 0.5 V for different source doping levels. Increasing source doping improves the on current for a fixed off current.

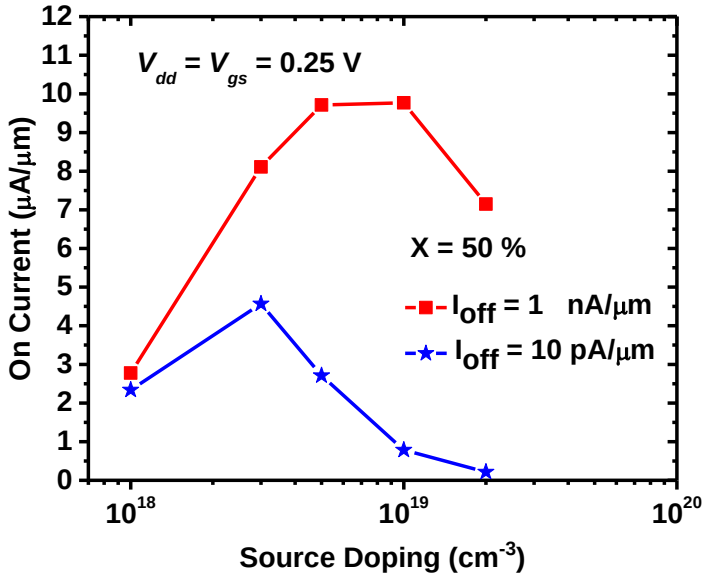



**Figure 2-11:** $I_{ON}$ at fixed $I_{OFF}$ for various source doping levels at $V_{DD}$ = 0.25 V. Here, initially on current increases with increase in doping, as source resistance decreases. However, continued increase in source doping lead to lower on current, as excessive degeneracy degrades the *SS*.

Another factor that may play an important role in this device is the Ge concentration in the channel material (SiGe). To study the impact of this, Ge composition was varied from 0 to 50 % and simulations of the device characteristics were performed. Figure 2-12 and Figure 2-13 show the $I_{DS}$-$V_{GS}$ and subthreshold slope behavior for pure silicon and at various Ge compositions. As expected, increased Ge concentration is beneficial both in terms of better subthreshold slope and higher on currents. Figure 2-14 shows the on current at various $I_{OFF}$ values at $V_{DD}$ = 0.5 V. It can be seen that the drive current improves by 5× for $I_{OFF}$ = 1 nA/μm as the Ge composition is increased from 0 to 50 %.

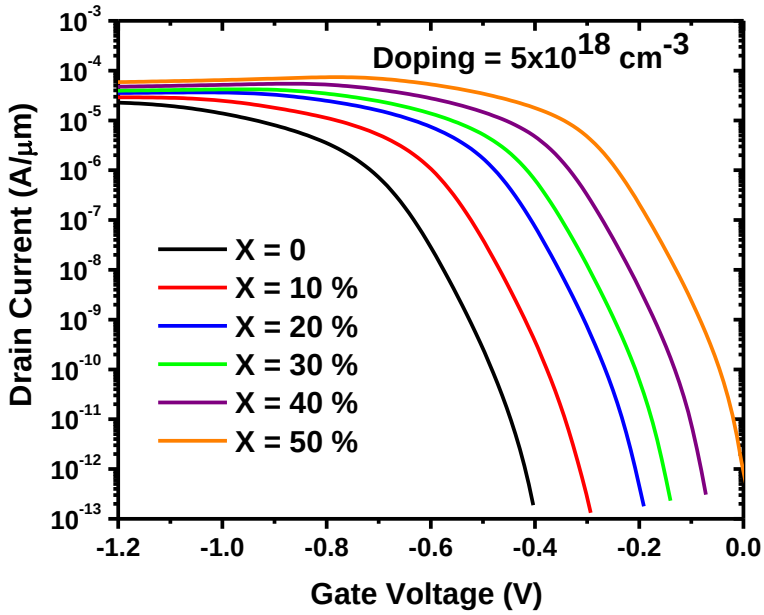



**Figure 2-12:** $I_{DS}$ vs. $V_{GS}$ for nominal device ($L_g$ = 20 nm, source doping, $N_d$ = 5 x $10^{18}$ $cm^{-3}$) at different channel Ge concentrations ($x$).

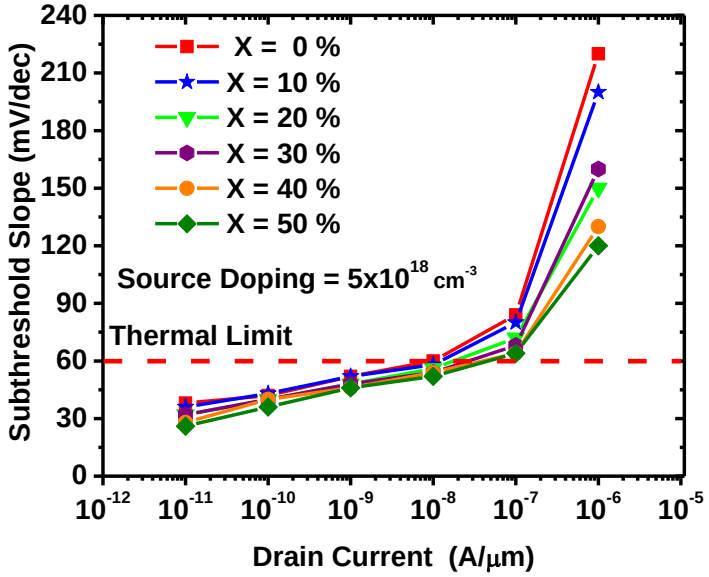



**Figure 2-13:** *SS* vs. log($I_{DS}$) for nominal device with different channel Ge concentrations ($x$). It can be observed that the *SS* improves substantially with increased Ge concentration ($x$).

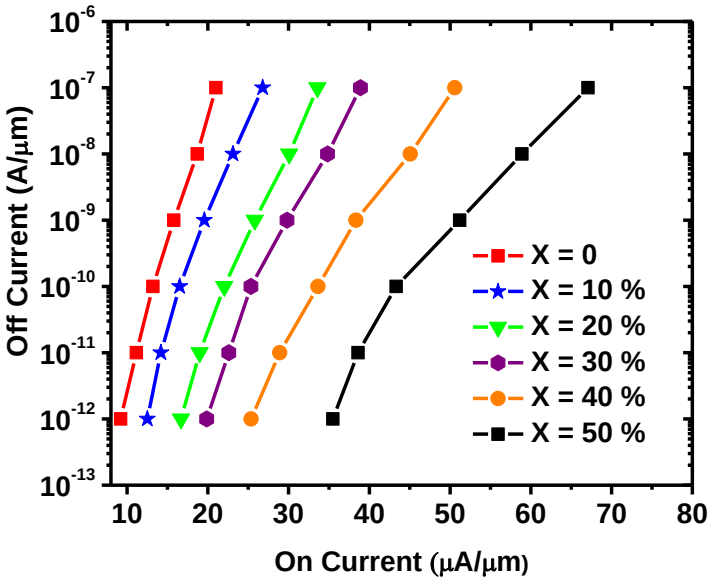



**Figure 2-14:** Plot of $I_{ON}$ vs. log($I_{OFF}$ ) at $V_{DD}$ = 0.5 V for different Ge concentration values ($x$). It can be observed that at $V_{DD}$ = 0.5 V, increasing Ge concentration values ($x$) also lead to higher on current for given off current.

Now, lastly, geometry of the device can play a role in the device characteristics. There are few aspects to this. One of them being change in quantum confinement of the nanowire based on diameter of the device (as discussed in section 2.2), as this can change the effective tunneling bandgap (Figure 2-3). And the other is the scaling of the gate length itself can affect the device characteristics, as Source and Drain come closer to each other, affecting their functions.

Figure 2-15 shows the on current at 10 % and 50 % of Ge concentration at two fixed off current values. A strong dependence of $I_{ON}$ on the diameter is also observed, and the utilization of SiGe in the channel allows the reasonable drive currents to be maintained with increased confinement.

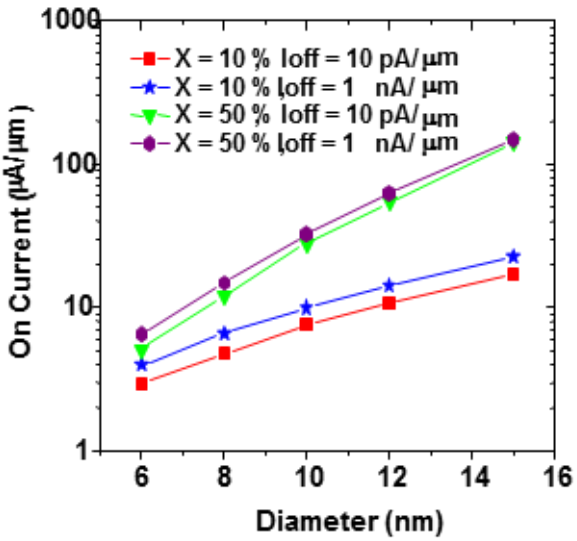



**Figure 2-15:** On current for different nanowire diameter at source doping, $N_d$ = 3x $10^{18}$ $cm^{-3}$ and $V_{DD}$ = 0.5 V. Strong dependence on nanowire diameter can be observed.

To see the effect of gate length scaling, simulations were performed keeping the other parameters constant. The subthreshold slope comparison as a function of channel length at

supply voltage of 0.5 V at two different current levels is shown in Figure 2-16. Good short-channel behavior for the nominal devices (10 nm diameter) is observed, while the relatively-large band gap, $E_g$, of SiGe suppresses direct source-to-drain tunneling for $L_g$ > 10 nm (Figure 2-16). However, there is some degradation in subthreshold behavior at shorter channel lengths due to direct tunneling from source into drain. This ultimately is another factor limiting the scaling of the device.

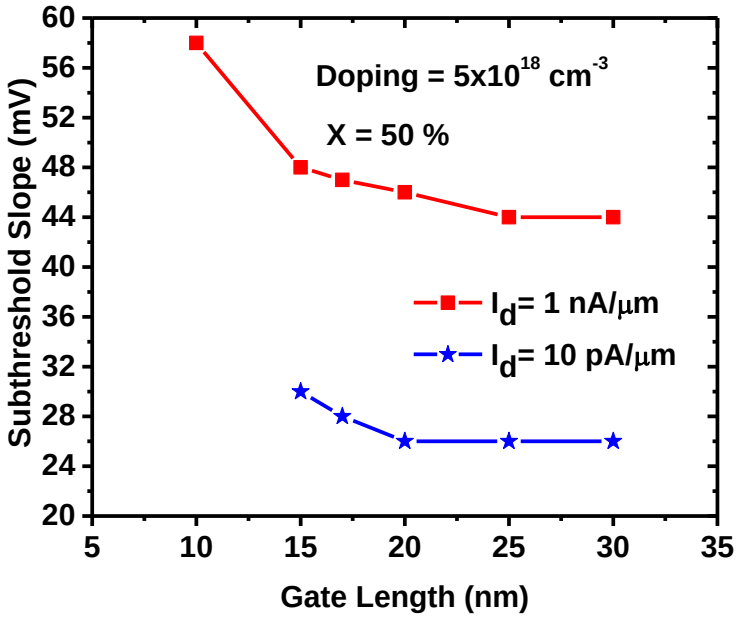



**Figure 2-16:** Effect of gate length scaling on subthreshold slope for nominal device at $V_{DD}$= 0.5 V. It can be observed that shorter channel devices exhibit degradation in *SS*.

## 2.4 Conclusions

In conclusion, these results show that hybrid InAs/SiGe p-TFETs may lead to improved drive currents and steeper subthreshold slope compared to InAs/Si devices. On currents as high as 150 µA/µm at 1 nA/µm and $V_{DS}$ = 0.5 V are possible using 50% SiGe. However,

p-TFETs have a fundamental trade-off between the source doping and the subthreshold slope which limits the maximum $I_{ON}$ and $I_{ON}/I_{OFF}$ ratios that can be obtained. This trade off occurs in the p-TFET devices because of material properties of the n-type source material. The low density of states leads high degeneracy in the n-type source, which in turn leads to a reversion of the subthreshold slope to the thermionic limit as a result of tunneling form the "tail" of the Fermi-Dirac distribution function.

This learning of this study is not limited to the specific InAs/SiGe geometry analyzed, but provides insights fundamental to all TFETs and could be applied to other material systems as well. For instance, it has highlighted the importance of electrostatic gate control, the need for low effective band gap, and the problem of source degeneracy. The ultimate scaling limits of TFETs in terms of both supply voltage scaling and the gate length scaling have also been elucidated by this work. This study underlines the importance of detailed analysis for optimizing the device based on various parameters.

# Chapter 3 :

# Emerging 2D Materials

## 3.1 Need for 2D Materials

As discussed in chapter 1, one of the approach to solve short channel effects and the power consumption problem is to improve the properties of existing MOSFETs. This involves improving electrostatics to gain better gate control over the channel and/or using materials that have improved properties. In order to improve gate control over the channel various methods can be used. One of the method to improve gate control is to isolate the silicon from the substrate, and reduce the silicon thickness itself. This is done using silicon-on-insulator (SOI) substrates[25]-[27]. Depending on the thickness of the silicon that is over insulator, there can be mainly two types of SOI devices. If the thickness of silicon layer is larger, only part of silicon is depleted, this is termed as partially depleted SOI (PDSOI)[28][29]. However, if silicon layer over insulator is very thin, all of the silicon is depleted, this type of substrate is called fully depleted SOI (FDSOI)[30][31] or extremely thin SOI (ETSOI) [32][33]. Apart from providing better gate control over the channel, SOI devices also eliminate the unwanted parasitic capacitances from the bulk substrate. One way to further improve the control of the gate, is to build 3D transistors on either bulk or SOI with gate wrapping around all three sides of the channel[34]–[36]. New materials such

as carbon nanotubes (CNTs) can also be used to improve the performance. These ways to improve device performance are depicted in Figure 3-1 [37].

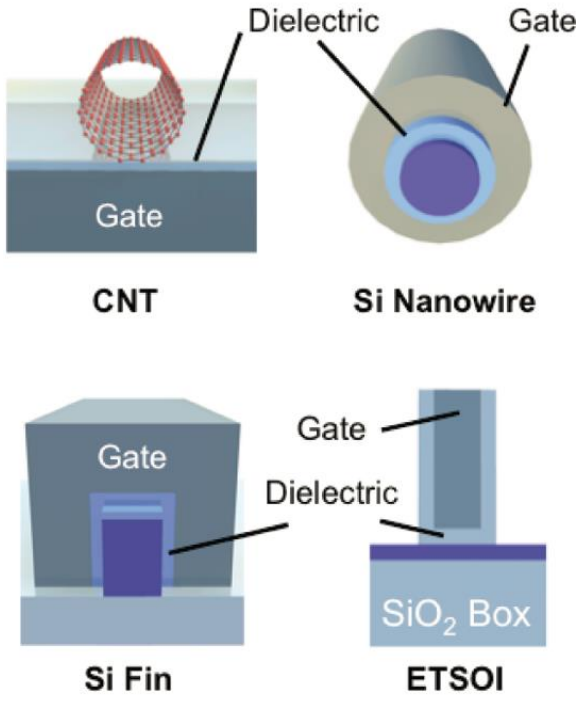



**Figure 3-1:** Various gating techniques and materials being considered in the field of devices. Clockwise from top left, carbon nanotube device, gate all around silicon nanowire based device, Silicon based finFET, and Silicon based SOI device [37]. Reprinted with permission from [37]. Copyright 2012 American Chemical Society.

All these methods discussed in the last paragraph improve the channel length scaling of the device, the parameter that can best be used to quantify this scaling ability is called the scaling length [38]-[40]. Scaling length is the characteristic length at which the drain-to-channel electric field decays and can predict the ultimate scaling limit of the device. For scaling silicon further, the thickness of the silicon layer has to be scaled proportionately. This is because the scaling length, $\lambda$, of the device can be expressed as [40]

$$\lambda = \sqrt{\left(\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\right) \times t_{ox} \times t_{Si}} \quad (3\text{-}1)$$

where,

$\varepsilon_{Si}$ = Dielectric constant of silicon

$\varepsilon_{ox}$ = Dielectric constant of the gate oxide

$t_{Si}$ = Thickness of silicon

$t_{ox}$ = Thickness of gate oxide

However, there are limitations on how much silicon thickness can be scaled. Silicon mobility degrades substantially below about 5 nm of body thickness [41][42]. Another problem with scaling the silicon body thickness is quantum confinement. As the silicon thickness is scaled down, the quantum confinement in vertical direction causes threshold voltage variations. An alternative to scaling silicon may be use of III-V materials [43][44]. However, quantum confinement effects in III-V materials are even more severe. In addition III-V materials suffers from a substantial amount of interfacial defects impacting performance of the devices [18]–[22].

Carbon based materials has been studied and explored extensively in recent years due to their excellent transport properties[45]–[48]. However, challenges to make high volume devices and circuits using these materials still remains a roadblock. Carbon nanotubes suffer from separation issue between metallic and semiconducting wires [49]–[51]. Also, graphene is a semimetal with zero bandgap [46] making it difficult create devices that has good turn off characteristics.

## 3.2 Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDs) are a combination of group II and group VI elements as shown in Figure 3-2[52]. There are over 40 such material combinations possible that are stable. These include $MoS_2$, $MoSe_2$, $MoTe_2$, $WS_2$, $WSe_2$, $TiSe_2$, and many others. These TMDs exhibit attractive features such as a finite band gap (~ 1eV-2 eV), and layered structure. Due to its layered structure, these can be easily exfoliated into fewer layers, down to single monolayer of material.

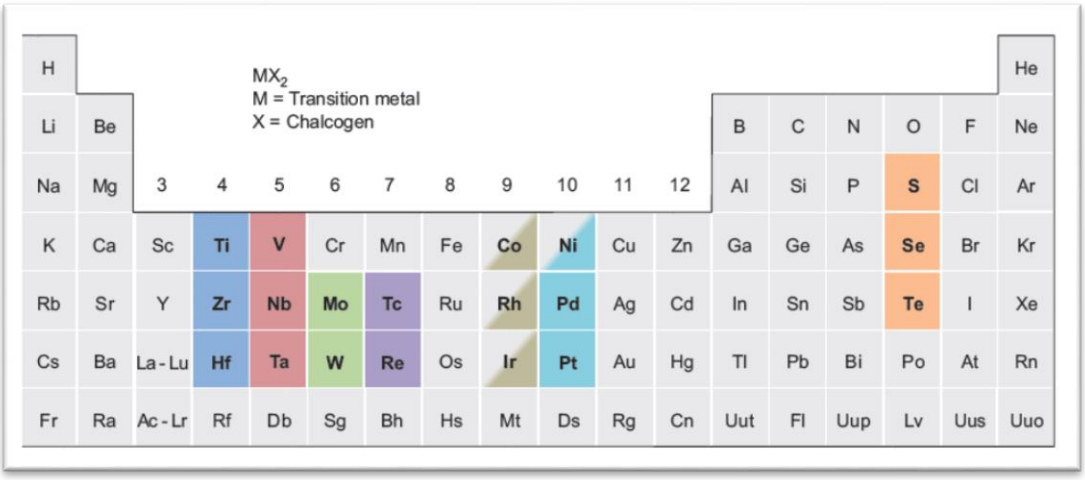



**Figure 3-2:** The transition metals and the three chalcogen elements that predominantly crystallize in those layered structure are highlighted in the periodic table. Partial highlights for Co, Rh, Ir and Ni indicate that only some of the dichalcogenides form layered structures [52]. Adapted by permission from Macmillan Publishers Ltd: [52], copyright (2013).

In TMDs, 2D layers of material are bound together with weak van der Waals forces. This makes these materials suitable for mechanical exfoliation (for instance, using the Scotch-tape method) of single- or few-layer sheets. Moreover, what makes these materials more interesting is changes in its physical properties as the material is thinned down. For instance, the band gap of $MoS_2$ in bulk is about 1.2 eV [53], however when it is thinned

down to monolayer, it transforms into material with a band gap of about 1.8 eV. In Figure 3-3 below, the band gaps and band alignment of few of the TMDs are shown [53].

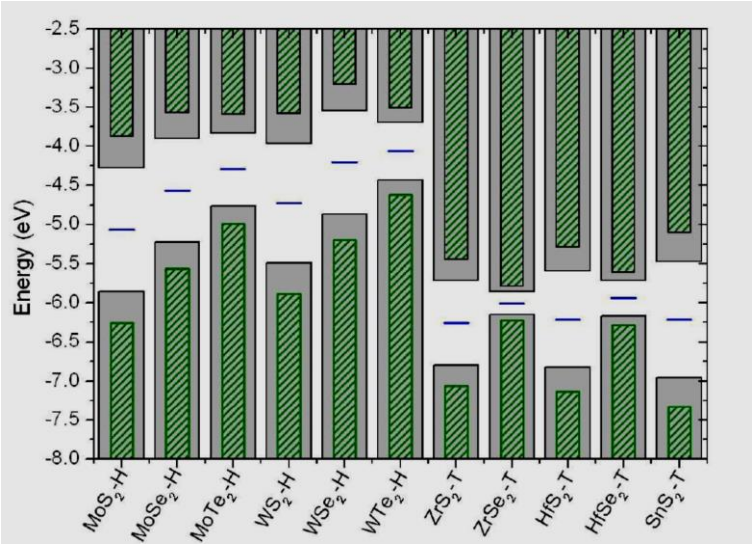



**Figure 3-3:** Band alignment of monolayer semiconducting TMDs. The Fermi level is indicated by the blue horizontal line and the vacuum level is at 0 eV [53] . Reprinted with permission from [53].Copyright 2013 American Chemical Society.

The crystal structure of TMDs also sets it apart from other semiconducting materials. Unlike carbon based materials, bulk TMDs exhibit a variety of polymorphs and stacking polytypes (a specific case of polymorphism) because an individual $MX_2$ monolayer, which itself contains three layers of atoms (X–M–X), can be in different phases [54]. There are mainly three polymorphs: 1T, 2H and 3R where the letters stand for trigonal, hexagonal and rhombohedral, respectively, and the digit indicates the number of X–M–X units in the unit cell (that is, the number of layers in the stacking sequence). Two of such crystal arrangements for $MoS_2$ are shown in the figure 3-4 below [54].

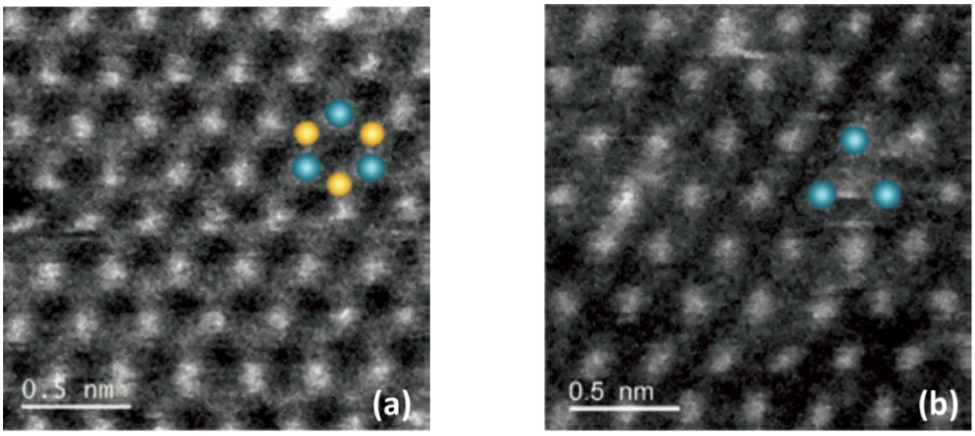



**Figure 3-4:** Dark-field scanning transmission electron microscopy image of single-layer $MoS_2$ showing the contrast variation of 1H (a) and 1T (b) phases [54]. Reprinted with permission from [54]. Copyright 2012 American Chemical Society.

The electronic structure of TMDs strongly depends on the coordination environment of the transition metal and its d-electron count. This gives rise to an array of electronic and magnetic properties as summarized in Table 3-1 below [52]. In both 1H and 1T phases, the non- bonding d bands of the TMDs are located within the gap between the bonding and antibonding bands of M–X bonds.

| Group | M | X | Properties |
|---|---|---|---|
| 4 | Ti, Hf, Zr | S,Se,Te | Semiconducting, Diamagnetic. |
| 5 | V,Nb,Ta | S,Se,Te | Narrow band metals or semimetals. Supercoducting. Paramagnetic, antiferromagnetic, or diamagnetic. |
| 6 | Mo,W | S,Se,Te | Semiconducting (S,Se) or semimetalic (Te). Diamagnetic. |
| 7 | Tc,Re | S,Se,Te | Small-gap semiconductors. Diamagnetic. |
| 10 | Pd,Pt | S,Se,Te | Semiconducting (S,Se) or metallic (Te). Diamagnetic (S,Se) or paramagnetic (Te). |

**Table 3-1:** Electronic characteristics of TMDs [52], properties of TMDs changes drastically depending on various factors discussed.

## 3.3 $MoS_2$ Material Properties

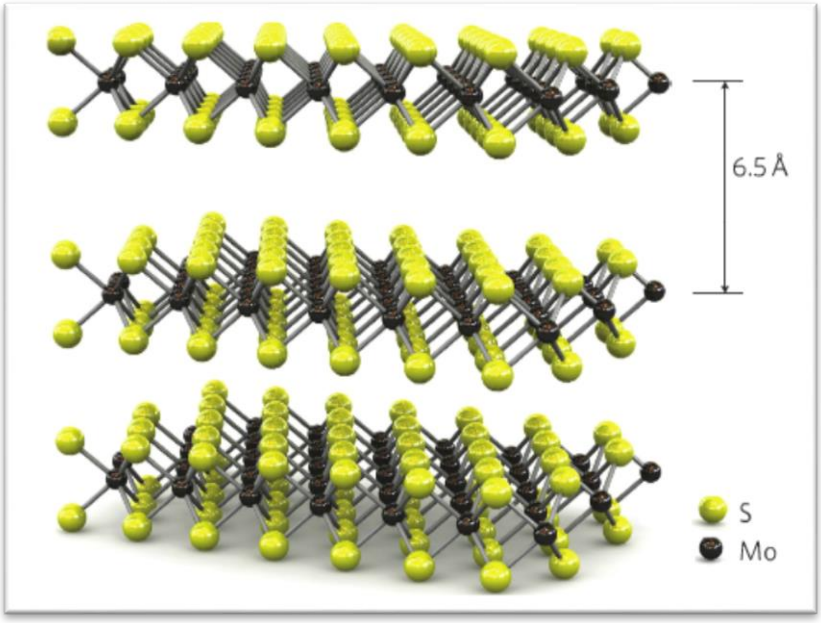



**Figure 3-5:** Three dimensional structure of $MoS_2$. Single layers, 6.5Å thick, can be extracted using scotch tape-based exfoliation [55].

$MoS_2$ is a typical example from the layered transition-metal dichalcogenide family of materials. Crystals of $MoS_2$ are composed of vertically stacked, weakly interacting layers held together by van der Waals interactions (Figure 3-5)[55]. Single layer is about 6.5 Å thick, and can be extracted using scotch tape based exfoliation. As discussed earlier, there can be various stacking sequences in TMDs. Natural $MoS_2$ is commonly found in the 2H phase where the stacking sequence is AbA BaB (The capital and lower case letters denote chalcogen and metal atoms, respectively). Synthetic $MoS_2$, however, often contains the 3R phase where the stacking sequence is AbA CaC BcB. In both cases, the metal coordination is trigonal prismatic.

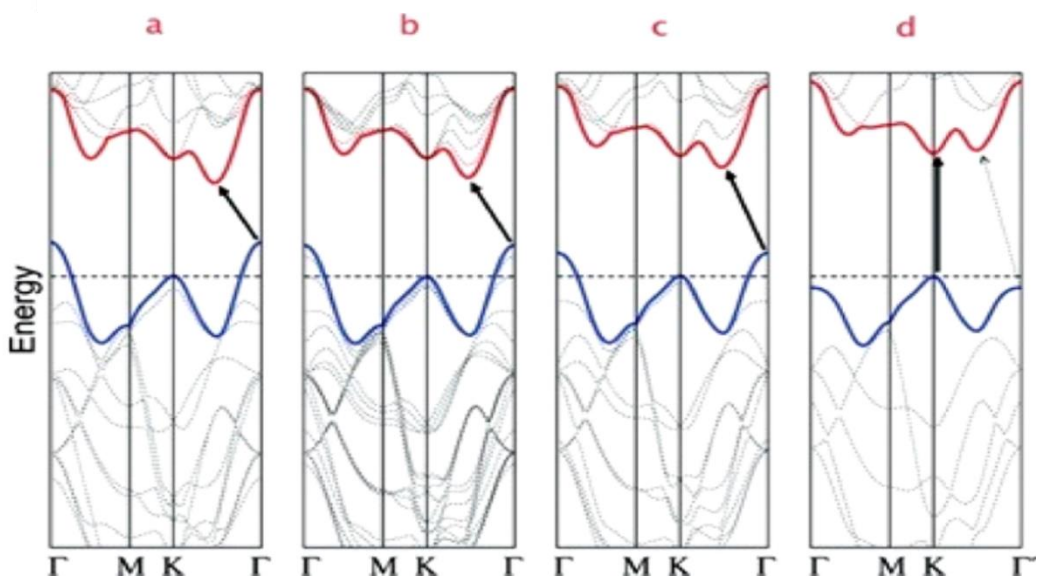



**Figure 3-6:** Transition of the band structure of $MoS_2$ from indirect to direct band gap, (a) Bulk $MoS_2$ (b) quadrilayer $MoS_2$ (c) Bilayer $MoS_2$ and (d) Monolayer $MoS_2$ [56]. Reprinted with permission from [56]. Copyright 2010 American Chemical Society.

In case of multi-layer $MoS_2$, each 2D crystal layer of $MoS_2$ has a plane of hexagonally arranged molybdenum atoms sandwiched between two planes of hexagonally arranged sulfur atoms, with the covalently bonded S-Mo-S atoms in a trigonal prismatic arrangement forming a hexagonal crystal structure. As $MoS_2$ is thinned down from bulk to monolayer, the band diagram of the $MoS_2$ changes due to quantum confinement effect. The transition of $MoS_2$ from indirect to direct band gap is shown in Figure 3-6 [56], as seen before, the most commonly found crystal symmetry configurations for $MoS_2$ are hexagonal and octahedral structures. Hexagonal is semiconducting, while octahedral is metallic. The hexagonal is more stable than the latter. Making $MoS_2$ primarily semiconducting material. The Mo-S bond length is 2.4Å, the crystal lattice constant is 3.2 Å, and the distance between the upper and lower sulfur atoms is 3.1 Å. The hexagonal Brillouin zone of the $MoS_2$ along with symmetry points is shown in [57] below :

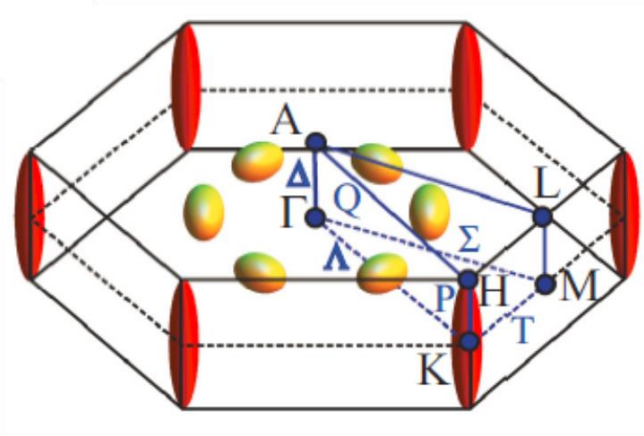



**Figure 3-7:** The hexagonal Brillouin zone of $MoS_2$ with symmetry points [57].

Bulk $MoS_2$ has an indirect band gap of 1.29 eV (see Figure 3-6). The band structure and band gap of $MoS_2$ are strongly influenced by quantum confinement owing to its ultrathin 2D crystal structure. The valence band maximum is located at the Γ point, while the conduction band minimum is located almost halfway along the ΓK direction, which establishes the indirect band gap transition. When the $MoS_2$ is thinned down, layer number decreases, the lowest band in the conduction band moves upward, increasing the overall band gap. As the conduction band states at the K point are mainly due to the d-orbitals of the molybdenum atoms and are relatively unaffected by interlayer interactions, the direct band gap at the K point only increases by about 0.05-0.1 eV. The states near the Γ point on the conduction band are due to hybridization between pz-orbitals of sulfur atoms and the d-orbitals of molybdenum atoms and are affected by interlayer interactions. Thus the bands at Γ are more affected by a decrease in layer number. In the monolayer, the indirect transition gap is larger than the direct transition gap, and the smallest band gap is thus the

direct band gap at K point of about 1.9 eV. This transition from an indirect to a direct band gap semiconductor makes these materials very interesting.

As the band gap changes with the number of layers, so does the effective mass. Although not as dramatic as the band gap, the effective mass estimated at various points in E-K diagram is listed below in table. Here $\Lambda_{min}$ represents the conduction band minimum between Γ and K point as we saw before. It can be observed that effective masses of the $MoS_2$ are relatively higher compared to silicon.

| Hole masses | | | | | |
|---|---|---|---|---|---|
| | K[Δ] | K[T] | K[P] | Γ[Σ]=Γ[Δ] | Γ[Δ] |
| **Bulk** | 0.43 | 0.47 | 1.73 | 0.62 | 0.8 |
| **Monolayer** | 0.44 | 0.48 | | 2.8 | |

| Electron masses | | | | | | |
|---|---|---|---|---|---|---|
| | K[Δ] | K[T] | K[P] | Δmin [Δ] | Δmin [⊥Δ] | Δmin [\|\|c] |
| **Bulk** | 0.47 | 0.45 | >100 | 0.53 | 0.73 | 0.49 |
| **Monolayer** | 0.37 | 0.38 | | 0.57 | 0.97 | |

**Table 3-2:** Effective masses (per electron mass $m_0$) for the unstrained system for bulk and monolayer $MoS_2$ [57]

## 3.4 Prior Work in $MoS_2$ and Other TMDs

As discussed previously, transition metal dichalcogenides (TMDs) have been of great interest recently for a wide range of electronic and photonic device applications [58]-[62]. One of the most promising TMDs for scaled transistors is molybdenum disulfide ($MoS_2$), and several recent reports have shown promising performance and scalability for $MoS_2$

MOSFETs [63]. The first attempt to fabricate $MoS_2$ based device demonstrated extremely low leakage currents and good mobility [55]. Since then various efforts are being made to study and understand material, device and contact properties of $MoS_2$. Along with $MoS_2$ some other TMDs are also being extensively explored [62][64].

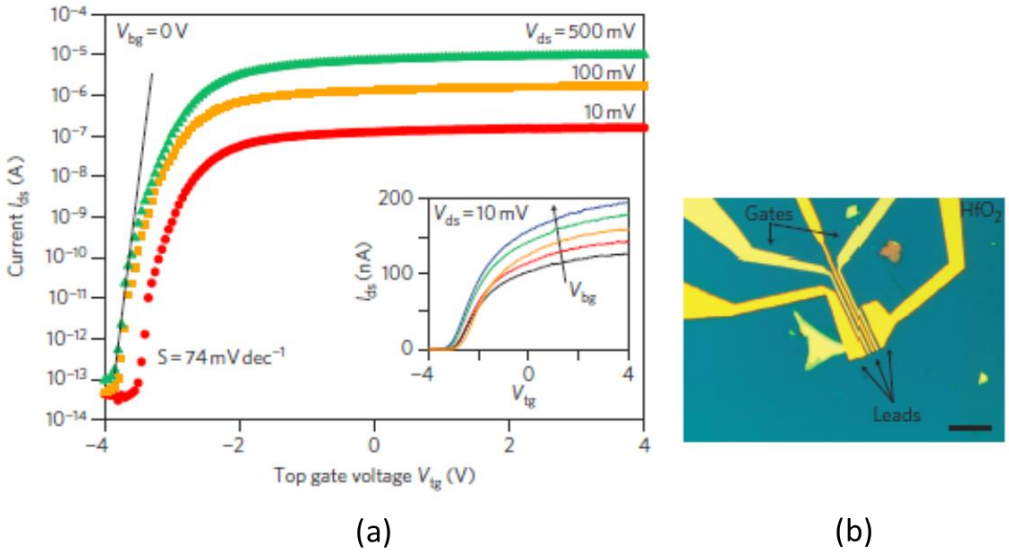



**Figure 3-8:** First demonstration of monolayer $MoS_2$ based FET [55], (a) $I_{DS}$-$V_{GS}$ characteristics of monolayer $MoS_2$ based FET, (b) Optical image of the device.

Attempts are being made to fabricate and explore various applications of such TMD based FETs [55], [62], [65]–[70]. Combinations of such TMD materials are also being explored. Recent demonstration of invertors [71][72], logic circuits [58], [73]–[76] and memory devices [77][78] are some of the examples of such attempts. Although these initial demonstrations have generated interest in these materials, there is a need of identifying specific applications best suited for particular TMD materials or material combinations based on their electronic properties.

One aspect of $MoS_2$-based devices that has not received significant attention is their potential for extremely-low leakage operation. Due to its large band gap, ultra-thin channel, and high effective mass, short channel effects (SCEs) and gate induced drain leakage (GIDL) are expected to be substantially suppressed compared to silicon, making $MoS_2$ suitable for extremely-low leakage static and dynamic memories [79]. Next, we will explore such low power application using $MoS_2$ as channel material for devices and circuits.

# Chapter 4 :

# $MoS_2$ MOSFETs for Low Power Memory Applications

## 4.1 Requirements in Low Power Electronics

To quickly summarize our discussion in chapter 3, each of the TMDs have their own unique physical properties, therefore, it is important to understand these properties thoroughly and identify the possible application best suited for each TMD. One of the most promising TMDs that can be used as the channel material for scaled transistors is molybdenum disulfide ($MoS_2$), and several recent reports have shown promising performance and scalability for $MoS_2$ based MOSFETs [55][63]. However, one aspect of these devices that has not received significant attention is their potential for applications requiring extremely-low leakage operation.

In memory applications, particularly in the case of dynamic memories, the MOSFET leakage requirements can be quite different from those in logic circuits. In the latter, the most important figure of merit is the subthreshold slope, which ensures the lowest possible off-state current (at zero gate bias) while still maintaining acceptable drive current. Furthermore, for logic devices, there are severe constraints on the supply voltage, $V_{DD}$, which must be kept as low as possible, since these devices have high activity factor, and the active power consumption goes as $V_{DD}^2$. However, for memory applications, the $V_{DD}$ requirement can be relaxed substantially, since the activity factor is much lower. For

instance, it is typical for static random accesses memory (SRAM) circuits to operate at higher $V_{DD}$ than the accompanying logic in order to allow higher threshold devices and thus lower leakage currents. Further still, in dynamic memory circuits, negative supply voltages are often utilized for the word line bias, in order to further ensure that the access transistor can be operated at a gate voltage that provides the minimum leakage current. Therefore, for many memory applications, it is the minimum current, $I_{MIN}$, rather that *SS*, that is the most important figure of merit for low-power operation.

Industry uses both deep trench capacitor technology based 1T1C as well as CMOS compatible versions of the embedded DRAM[80]. However, 1T1C cell with deep trench capacitor has a limitation in terms of ease of scaling with technology. To address this issue, transistor-only memory cells have been proposed which utilize the gate electrode of a MOSFET itself as the storage capacitor. These types of cells, such as the three transistor (3T) gain cell in reference have the advantage that the read and the write operation are de-coupled, thus allowing non-destructive read and further allowing the transistor's inherent gain to increase the read current. However, such cells have the disadvantage of a low storage node capacitance and thus higher refresh rates. There are various configurations possible among CMOS compatible embedded DRAM cells[81]–[85]. These are usually few transistor cells optimized in terms of area and performance to give highest performance. One of the prominent among them is 3T gain cell configuration. This has an advantage of read and write operation being de-coupled, which allows independent read and write operations. The time duration over which the cell retains the stored data in order

to reliably read as the same data as written, is termed as the retention time of the memory cell. This in turn makes it a configuration that allows nondestructive read. In order to enable low power consumption in such embedded DRAM cells, it is desirable to have retention time as large as possible, so that the cell needs minimum refresh, and in turn minimizes the power consumption. In gain cell configuration, one can hold the storage node at a desirable bias that may lead to least leakage losses. However, in gain cell configuration, large deep trench capacitance of 1T1C cell is replaced with smaller intrinsic capacitance of the transistor. In which case having low leakage in pass transistor as well as storage transistor becomes vital. Therefore, a material that can provide minimum current in its off state is highly desirable in such applications. $MoS_2$ can be an ideal candidate for such applications.

Ensuring the lowest possible minimum current is particularly important in embedded dynamic random access memories (eDRAMs) where the fabrication process must be kept compatible with that of the logic circuitry, thus placing some constraints on the size of the storage node capacitor. Therefore, in order for such memories to be viable for practical implementation, orders of magnitude improvements in the leakage current are needed, making $MoS_2$ an ideal candidate for such applications.

In such applications, requirements are low minimum current and long refresh time (Figure 4-1). Here transistor can be biased at a gate voltage such that the leakage of the transistor is minimum. Therefore, here, it is important to get absolute value of minimum current as small as possible. Although high on current is also a useful property that can be utilized, but it is not entirely essential as high on current will only affect write times, whereas

retention time, which is time for which data can be held in the cell is more important factor in such applications. So, $I_{ON}$ can be traded off for much smaller off current. Retention time as high as 1.25 ms [84] has been reported for high end processor applications. While some of the eDRAMs developed for biomedical application, where area cost per bit can be relaxed, can have up to 1-10 ms[86] of the retention time. To achieve better retention times to improve performance of such eDRAM cells, off currents of the order of few femto-Amperes are required.

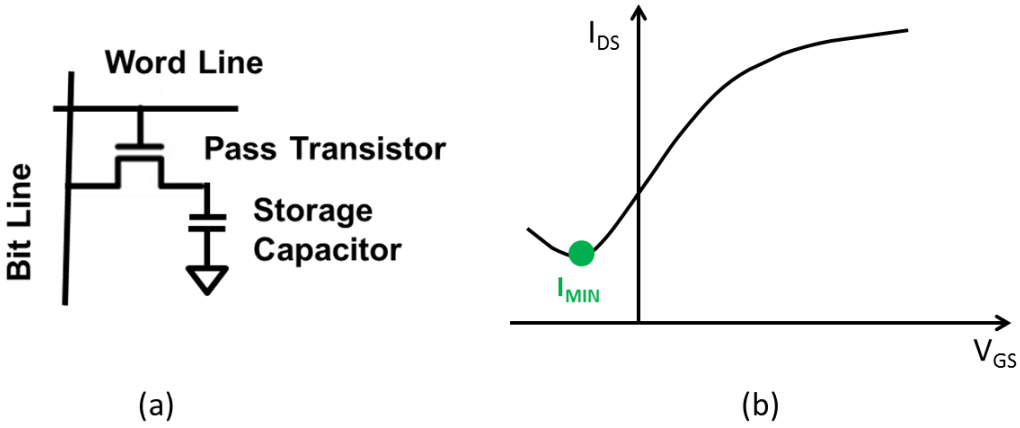



**Figure 4-1:** Requirements for access pass transistors in dynamic memory, (a) Schematic diagram of a 1T1C cell, (b) $I_{DS}$-$V_{GS}$ charecteristics of a pass transistor, with desirable minimum current.

The large band gap of $MoS_2$ delays onset of band-to-band tunneling, which can be exploited in such applications. Moreover the heavy mass minimizes band-to-band tunneling leading to reduced leakage current. The thin (few layer or monolayer thickness) of $MoS_2$ also enables low drain induced barrier lowering (*DIBL*) and steep subthreshold slope, as seen in equation 3-1 in chapter 3, as it enables stronger gate control. This then enables improved scalability and higher density. All these properties make $MoS_2$ a strong candidate for embedded DRAM memory applications.

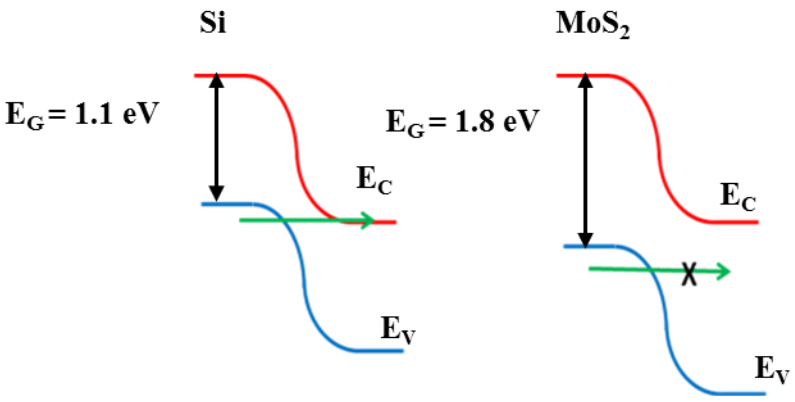



**Figure 4-2:** Band diagram comparison depicting motivation for $MoS_2$ as a low-leakage transistor channel material. Larger bandgap of monolayer $MoS_2$ (compared to Si ) can drastically reduce band to band tunneling, and hence GIDL current.

If we were to compare and contrast $MoS_2$ properties with that if silicon, one of the first important difference is the inherent nature of the material. While silicon prefers to form a 3D crystal structure, $MoS_2$ on the other hand is a layered material, with each layer loosely couples via van der Waals forces, making it a suitable material for mechanical exfoliation. The mobility of $MoS_2$ is slightly lower than silicon, while the bulk band gap of $MoS_2$ is

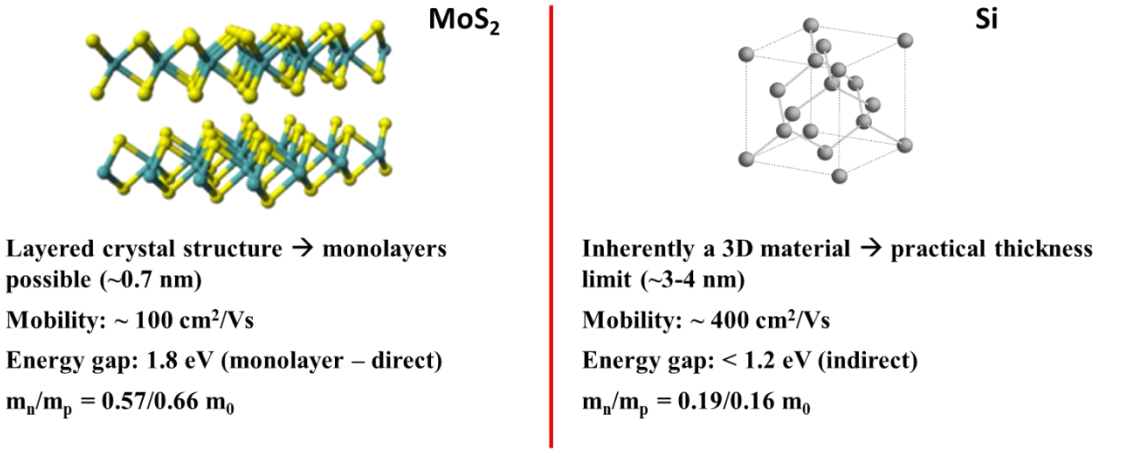



**Figure 4-3:** Comparison of $MoS_2$ and Si properties. Properties indicate that compared to silicon, $MoS_2$ can be a material better suited for low power applications.

about 1.2 eV and is indirect, but if $MoS_2$ is scaled to monolayer, the bandgap of $MoS_2$ changes to having a direct band gap of about 1.8 eV. This increased bandgap can be useful in suppressing Gate Induced Drain Leakage (GIDL) current in the devices. $MoS_2$ also has heavier effective masses compared to silicon which can lead to lesser tunneling currents. This also suppresses tunneling current as tunneling current is exponentially inversely proportional to effective mass of the material.

In order to realize its potential for low-leakage applications, careful simulation, modeling and design space analysis is needed. The design space required to realize two-dimensional (2D) $MoS_2$ low-leakage MOSFETs can be explored. A combined approach using TCAD electrostatic simulations with an analytical transport model to predict the subthreshold performance of $MoS_2$ MOSFETs can be used to develop a device model. This model can be applied to a dynamic memory cell design and benchmark the performance advantages compared to conventional low-leakage silicon technology.

## 4.2 Modelling Approach

To model the device characteristics, physical properties of the $MoS_2$ were utilized to develop an analytical model. This was done both using semi empirical formulas and use of self-consistent electrostatic solver like TCAD. Finally, this model can be applied to predict and estimate the circuit performance for low power applications (Figure 4-4). As discussed earlier, since such memory applications rely mainly on low off current regime, only off state current of the device is modelled.


**Figure 4-4 :** Modelling approach for an analytical device model using semi-empircal formula with assitance from TCAD.

Since this model is mainly used to evaluate and examine low current regime of the device, only currents below threshold voltage are considered, and on current is not considered in this model. Three current components considered are 1. Thermal subthreshold leakage current ($I_{therm}$), 2. Gate Induced Drain Leakage (GIDL) current, and 3. Shockley-Read Hall (SRH) current. These components then can be added together to give total current in the low current regime of the device. Gate leakage can also be one of the component in the current. However, it is shown latter that for the oxide thicknesses under consideration, gate leakage is not a dominant factor in the low current regime.

The device geometry investigated in this study utilized an $HfO_2$ gate dielectric thickness, $t_{ox}$, of 10.3-15.4 nm (Effective oxide thickness = 2-3 nm) and gate length, $L_g$, in the range of 15-40 nm. Monolayer $MoS_2$ based channel is considered. In this regime, conventional models for the scaling length [39] are not valid (Figure 4-6, Figure 4-7) due to the nearly 1:1 aspect ratio of the gate-to-drain and gate-to-channel separations.

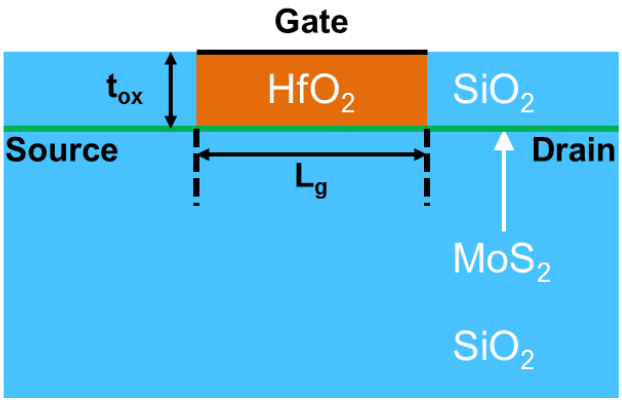



**Figure 4-5:** Schematic of the device under consideration. Monolayer $MoS_2$ is considered as channel material with thick high-k material based gate oxide. Range of parameters considered are shown in Table 4-1.

| Parameter | Value |
|---|---|
| Channel thickness ($t_{Si}$) | 0.65 nm |
| Gate dielectric thickness ($t_{ox}$) | 10.3-15.4 nm |
| Oxide dielectric constant | 20 |
| Channel dielectric constant | 4 |
| Gate Length ($L_g$) | 16 - 40 nm |
| $MoS_2$ band gap | 1.8 eV |
| Electron Affinity | 4 eV |
| $m^*_n$ / $m^*_h$ | $0.57m_0$ / $0.66m_0$ |

**Table 4-1:** Device geometry, and material parameters utilized for electrostatic simulations. Dielectric thickness and gate length is varied to understand and predict the device perfoemance.

Instead, TCAD simulations using Synopsys Sentaurus Device™ were used to extract the electrostatic scaling parameters utilized in the analytical device model. The TCAD simulations were compared to results using NEGF (non-equilibrium Greens function) simulations [65] and found to give comparable results for the subthreshold performance. The lateral electric field in the channel can be an indication of scaling length. Therefore, lateral electric field as a function of distance in the channel at different equivalent oxide

thickness (*EOT*) is plotted, and the slope of such a plot can determine the scaling length (Figure 4-6).

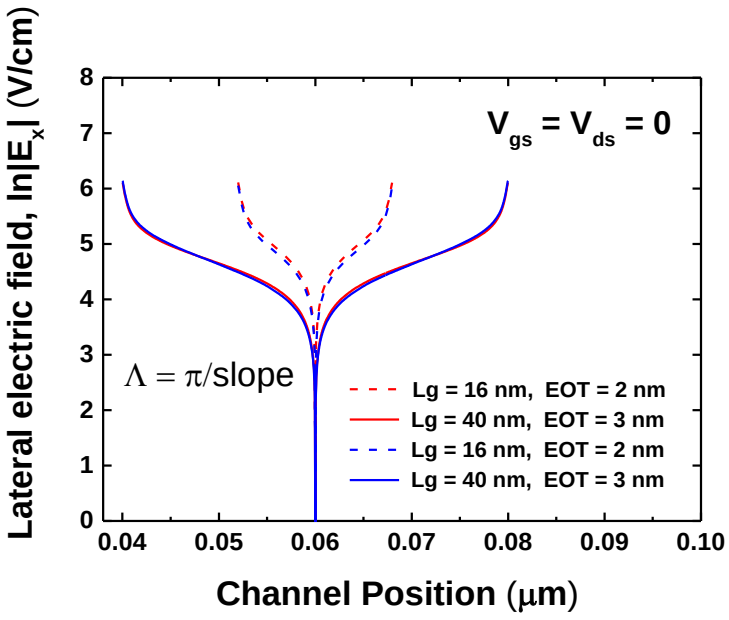



**Figure 4-6:** Traditional scaling length extraction based upon the slope of the lateral electric field in the device channel.

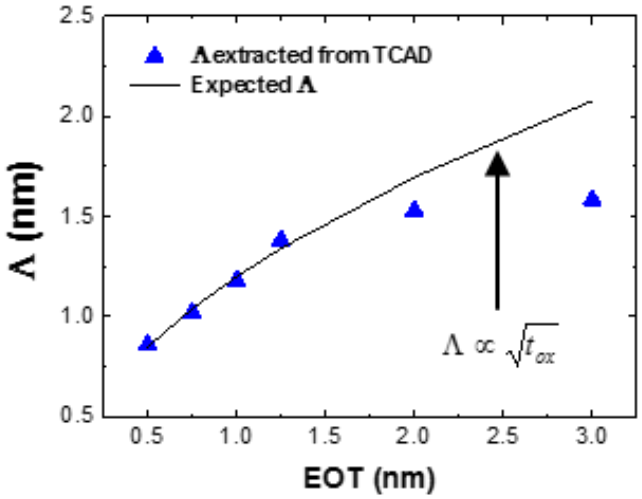



**Figure 4-7:** Comparison of scaling parameter, $\Lambda$, from TCAD vs. standard theory. The deviation at high equivalent oxide thickness (*EOT*) indicates that standard scaling theory does not apply in this regime.

Figure 4-7 shows plot of extracted scaling length as function of equivalent oxide thickness (*EOT*). It can be seen that the scaling length diverges from expected square root dependence on *EOT*. Therefore, the scaling length dependence on the physical parameters needs to be re-defined for the new material based on the range of the gate lengths and *EOT*s of interests. Since the application under consideration is embedded DRAM cells, oxide thicknesses of about 2-3 nm *EOT* and gate lengths between 20-40 nm are considered for this work. After extracting scaling lengths for the gate lengths and *EOT*s of interest, electrostatic simulations were performed to estimate the drain induced barrier lowering (*DIBL*) and the subthreshold slope (*SS*) and the results are shown in Figure 4-8 and Figure 4-9 for the $L_g$ and $t_{ox}$ range described above.

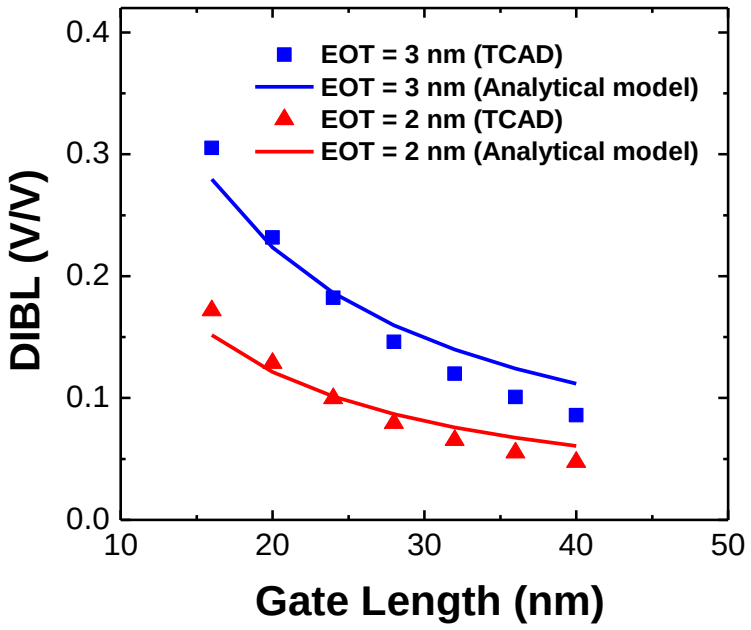



**Figure 4-8:** Comparison of analytical model and extracted drain induced barrier lowering (*DIBL*) from TCAD.

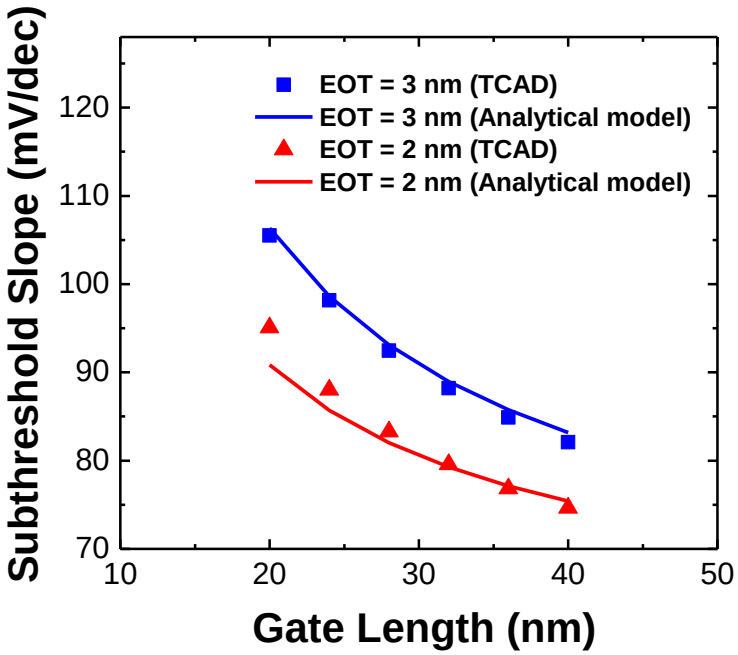



**Figure 4-9:** Comparison of analytical model and extracted subthreshold slope (*SS*) from TCAD.

The simulated *DIBL* and *SS* results were then fit using an empirical model that was found to provide a good fit over the range of $L_g$ and $t_{ox}$ values of interest.

Based on the fit, the *DIBL* and the body factors were found to be as follows:

$$\eta = 0.205 \cdot \left( \frac{t_{ox}}{L_g} \cdot \sqrt{\frac{\varepsilon_S t_{ox} t_S}{\varepsilon_{ox}}} \right), \tag{4-1}$$

$$m = 1 + 2.79 \cdot \left( \frac{t_{ox}}{L_g} \sqrt{\frac{\varepsilon_S}{\varepsilon_{ox}} t_S} \right), \tag{4-2}$$

where,

$\varepsilon_S$ = Dielectric constant of semiconductor, in this case $MoS_2$

$\varepsilon_{ox}$ = Dielectric constant of oxide, in this case $HfO_2$

$t_S$ = Thickness of semiconductor

$t_{ox}$ = Thickness of dielectric (oxide)

$L_g$ = Gate length of the device

Finally, in order to determine the subthreshold current, a 2D analytical model composed of three separate current components was utilized: i) subthreshold current, ii) gate induced drain leakage (GIDL) arising from band-to-band tunneling and iii) Shockley-Read-Hall (SRH) generation from drain to the body.

## 4.3 Sub Threshold Current Components

In order to calculate subthreshold current, semi-empirical current equations can be developed where the 2D density of states is included and considered in the equation. This can be done by including a prefactor in the subthreshold current equation which represents the constant 2D density of states.

The equation can be written as:

$$I_{subth} = \mu \cdot \frac{2q^2 m^*}{\pi \hbar^2} \cdot \frac{W_g}{L_g} \cdot V_T^2 \cdot \exp\left(\frac{V_{GS} - V_{th} + \eta \cdot V_{DS}}{m V_T}\right) \cdot \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \quad (4\text{-}3)$$

$$V_T = kT/q \quad (4\text{-}4)$$

$$m^* = 0.57 m_0 \quad (4\text{-}5)$$

where,

$\mu$ = Effective mobility of the carriers

$q$ = Charge on electron

$m^*$ = Effective mass of the carriers.

$\hbar$ = Planks constant

$W_g$ = Width of the device

$L_g$ = Length of the device

$V_T$ = Thermal voltage at temperature $T$

$k$ = Boltzmann's constant

$T$ = Temperature of the device

$V_{GS}$ = Gate to source voltage

$V_{th}$ = Threshold voltage of the device

$V_{DS}$ = Drain to source voltage

$\eta$ = *DIBL* factor

$m$ = Body factor

Both GIDL and SRH current components are dependent on the drain to channel electric field and alignment of the bands in that junction. In order to calculate these components analytically, an approximation is used that assumes constant electric field near the drain channel junction. This in turn assumes the bands to have constant slope as shown in Figure 4-10. With this, the electric field, $E_{drain}$, in the drain to channel region can be calculated as

$$\mathrm{E}_{drain} = \frac{V_{DS} - V_{GS} + V_{th}}{4.098\Lambda}, \tag{4-6}$$

where $\Lambda$ is scaling parameter, as calculated in Figure 4-6.

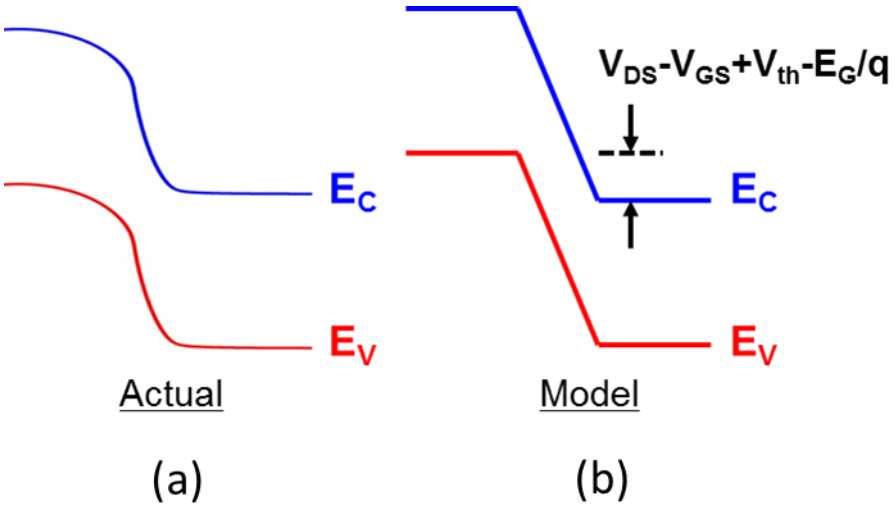



**Figure 4-10:** Tunneling window and constant electric field approximation. The actual band bending at the drain and channel junction is as shown in (a). Approximation assumes constant electric field at the drain and channel junction, implying a constant slop of the conduction and valance band as shown in (b).

The value of $E_{drain}$, was extracted from TCAD and the results were subsequently used to calculate the band-to-band tunneling rate. GIDL current starts to be a dominant factor when the valance band in the channel region crosses over the conduction band of the drain region, opening a window of states in the conduction band where tunneling can occur. Such a window is also shown in Figure 4-10. Since we know the band gap and threshold voltage, the energy window size can be calculated as $V_{DS} - V_{GS} + V_{th} - E_G/q$, where $E_G$ is the band gap of the material. It is assumed that the tunneling occurs only when this window is open, and tunneling current is zero otherwise. Based on this assumption, the tunneling probability can be calculated as:

$$I_{b-b} = qW_g A \cdot \exp\left(-\frac{B}{\mathrm{E}_{drain}}\right) \cdot \left(\frac{V_{DS} - V_{GS} + V_{th} - E_G/q}{\mathrm{E}_{drain}}\right), \quad V_{DS} - V_{GS} + V_{th} > E_G/q \qquad (4\text{-}7)$$

$$I_{b-b} = 0, \quad V_{DS} - V_{GS} + V_{th} \le E_G/q \qquad (4\text{-}8)$$

where,

$$A = \frac{\sqrt{2}}{18} \cdot \left( \frac{q\mathrm{E}_{drain}}{\hbar} \right)^{3/2} \cdot \left( \frac{m_r}{E_G} \right)^{1/4} \tag{4-9}$$

$$B = \frac{\pi^2}{qh} \sqrt{m_r} E_G^{3/2} \tag{4-10}$$

$$m_r = 0.31 m_0 \tag{4-11}$$

and $A$ and $B$ are constants based on physical parameters and the electric field in the drain region. $W_g$ is width of the device, $V_{DS}$ is drain to source voltage, $V_{GS}$ is gate to source voltage, $V_{th}$ is threshold voltage of the device, $m_r$ is reduced mass derived from electron and hole effective masses

$$m_r = \frac{m_e \times m_h}{m_e + m_h} . \tag{4-12}$$

The band-to-band tunneling current calculated using this analytical formula based on the WentzeI-Kramers-Brillouin (WKB) approximation and input from TCAD (in the form of $E_{drain}$) forms the GIDL component of the current.

SRH current depends on the depletion width, $W_{dep}$, which in turn depend on the electric field at the drain-channel junction. This again can be estimated as follows:

$$W_{dep} = \frac{V_{DS} - V_{GS} + V_{th}}{E_{drain}} . \tag{4-13}$$

This depletion region can be used to calculate the SRH generation current. Since the junction is reverse biased, generation will occur. To calculate SRH current a generation time constant of 200 ps was used from available literature [87]. The generation current can be calculated as

$$I_{SRH} = \frac{qn_i W_g W_{dep}}{2\tau_0} \quad , \tag{4-14}$$

where,

$\tau_0$ = generation time constant (~ 200 ps)

$n_i$ = intrinsic carrier density of the material

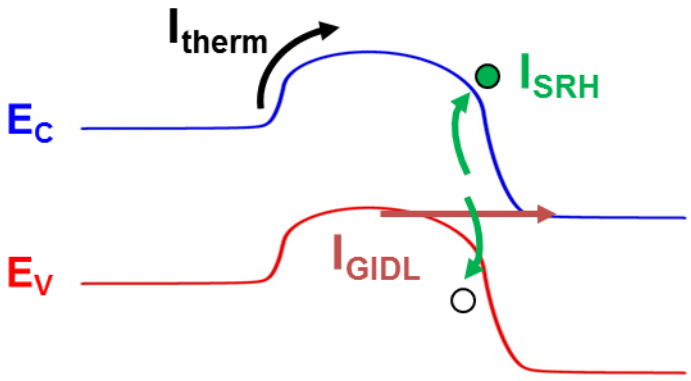



**Figure 4-11:** Leakage mechanisms and current components. Here, thermal component, $I_{therm}$ is due to thermionic emmision of the carriers over the barrier, $I_{SRH}$ is the generation current due to Shockley-Read-Hall generation-recombination, and $I_{GIDL}$ is the band to band tunneling component termed as gate induced drain leakage.

The three components of the current used in our model are depicted in Figure 4-11. Based on these components, the total current was calculated as a function of gate voltage and drain voltage for 20 nm and 40 nm of gate lengths is shown in Figure 4-12. The drain current vs. gate voltage characteristics at different drain voltages (Figure 4-12) show that, at low $V_{DS}$, the current is limited by either subthreshold or SRH current and not GIDL, while at higher $V_{DS}$, GIDL becomes a factor.

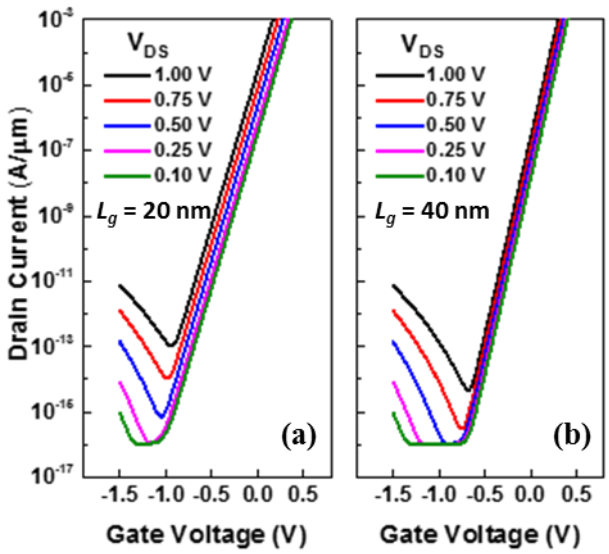



**Figure 4-12:** Modeled subthreshold currents for $MoS_2$ MOSFETs for *EOT* = 3 nm at (a) $L_g$ = 20 nm and (b) $L_g$ = 40 nm.

The gate leakage current was calculated by fitting and extrapolation of leakage currents in commercial high-K Si DRAM devices (IBM 32 nm model). A comparison of gate leakage current with the calculated currents is shown in Figure 4-13. It can be observed that the minimum leakage current $I_{MIN}$ is dominated by either GIDL current or in some cases SRH generation current. Therefore gate leakage is not expected to be a major factor in the range of oxide thicknesses under consideration. However, more careful consideration for gate leakage has to be given at thinner values of *EOT*.

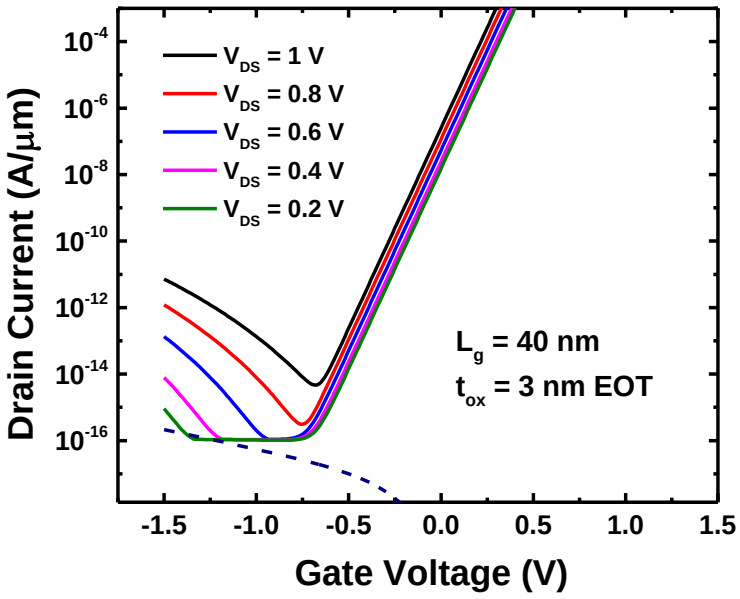



**Figure 4-13:** Comparison of gate leakage (dotted line) with other leakage mechanisms. It can be observed that $I_{MIN}$ is not limited by gate leakage current in the range of oxide thicknesses under consideration**.**

## 4.4 3T eDRAM Memory Cell and Estimation of Retention Time

The intended application considered in this work is 3T embedded DRAM cell [84]. The cell consists of write transistor (NW), storage transistor (NS) and read transistor (NR). Notice that the cell can have all 3 transistors either n-MOSFETs or p-MOSFET. In case of $MoS_2$ based cell, all transistors are considered to be n-MOSFETs. Data is written into the cell using write word line (WWL) and write bit line (WBL), and data is read using read word line (RWL) and read bit line (RBL). This de-couples read and write operation, which is one of the advantage of using 3T memory cell over using 1T1C memory cell. As shown in figure 4-14, the write transistor (NW) is turned on during the write operation by applying pulses at gate (WWL) and drain (WBL). This enables writing data onto the storage node.

During hold mode, the gate (WWL) of the write transistors can be biased to have minimum leakage in the devise. This is the operation where very low $I_{MIN}$ of the device is utilized to hold the data for long time.

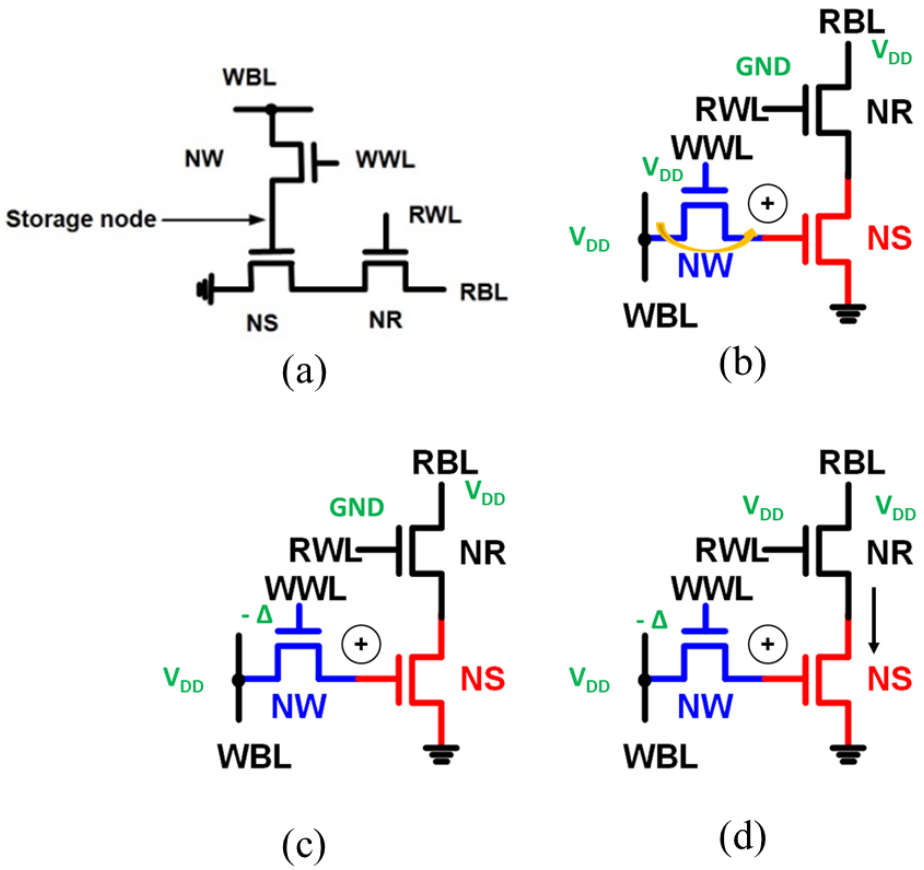



**Figure 4-14:** Diagram showing 3-transistor gain cell utilized for subsequent performance analysis. Here WWL and WBL denotes write word line and write bit line respectively, and RWL and RBL indicates read word line and read bit line respectivvely. Charges are transferred into the storage node via transistor NW, which can utilize a negative WWL voltage to minimize the subthreshold leakage. Diagrams indicate write (b), hold (c) and read(d) operations.

During read operation, read transistor (NR) is turned on and data is read. In this type of cell, subthreshold leakage and GIDL for the write transistor are critical parameters due to the small amount of stored charge, while gate leakage is important when a '1' is stored in

the cell. We utilize $CV/I_{MIN}$ as a performance benchmark for this circuit, which provides an estimate of the maximum possible discharge time, and this parameter should be as large as possible. Where $C$ is the capacitance of the device, $V$ is the applied drain to source voltage onto the device, and $I_{MIN}$ is the minimum current during the hold operation.

## 4.5 Results and Discussion

Calculated $CV/I_{MIN}$ is plotted against different values of $L_g$ (Figure 4-15). Very high discharge delays ~ 1 sec possible at $L_g$ = 40 nm. Scaling to $L_g$ = 20 nm reduces retention time to ~ 1 msec. Optimal $V_{DS}$ for maximum retention is reduced for thinner gate oxides. Here, as we reduce $V_{DS}$, initially, leakage current reduces substantially as $V_{DS}$ is scaled. However, as current hits the SRH current floor, the minimum leakage current is almost constant while, $V_{DS}$ is still reducing, leading to overall reduction in $CV/I_{MIN}$ delay. Therefore, reducing $V_{DS}$ will not always lead to increased retention time, but there is an optimum $V_{DS}$ value. Therefore, there is an optimum $V_{DS}$ which provides the longest retention time. The maximum retention times are found to be orders-of-magnitude higher than conventional Si-based circuits (~250 μs) at comparable dimensions [84].

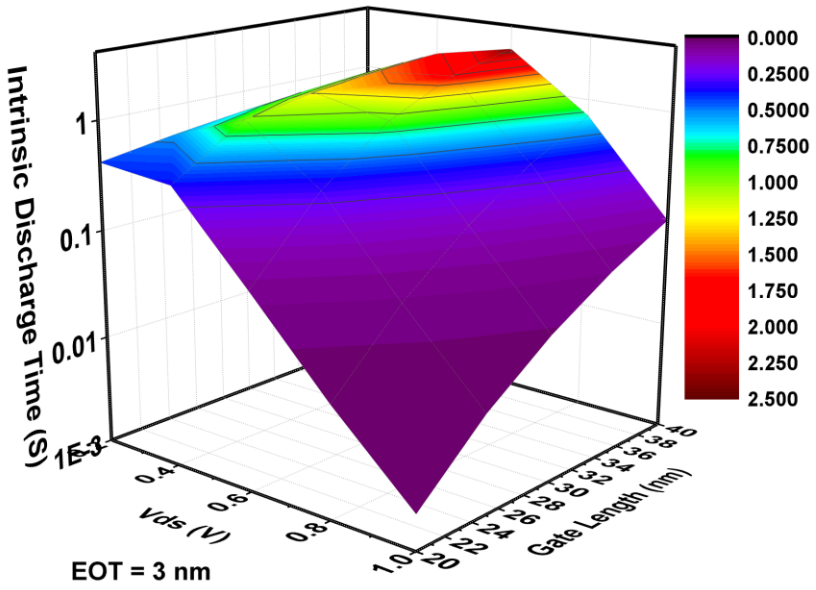



**Figure 4-15:** Intrinsic discharge time plotted vs. supply voltage and gate length at fixed *EOT* of 3 nm.

Similar optimum $V_{DS}$ can also be observed when *EOT* is varied at a fixed gate length (Figure 4-16). Although that optimum $V_{DS}$ can change with the *EOT* of the device. This is mainly due to change in the *DIBL* and other short channel effects with *EOT* for a fixed gate length device. As *DIBL* increase with reduction of *EOT* and the *SS* degrades with reduction of *EOT*, the optimum $V_{DS}$ value rises slightly.

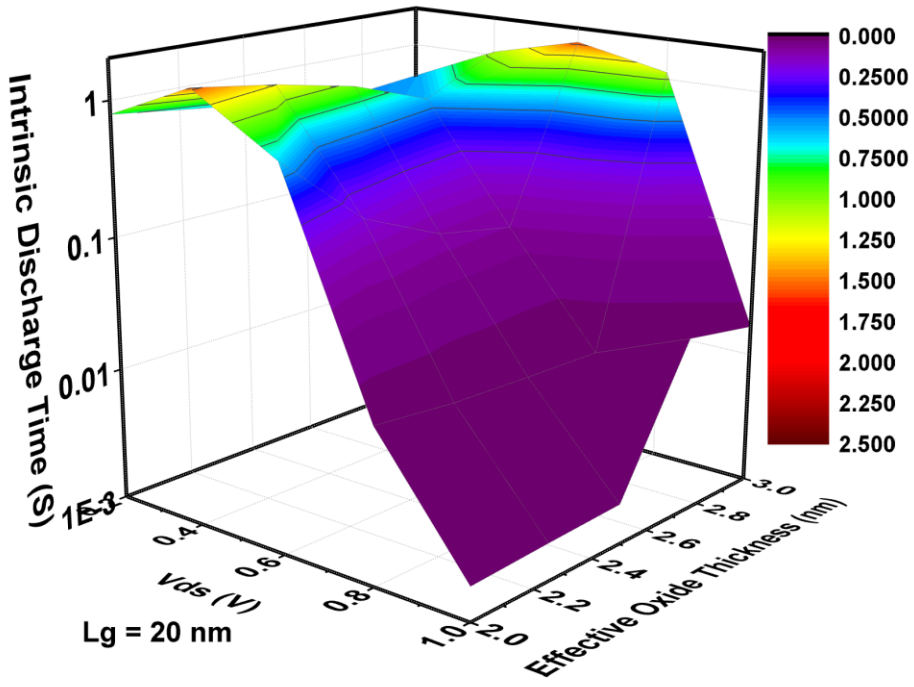



**Figure 4-16:** Intrinsic discharge time plotted vs. supply voltage and *EOT* at fixed gate length of 20 nm.

## 4.6 Conclusions

In conclusion, a semi-empirical analytical model for 2D $MoS_2$-channel MOSFETs has been developed, and applied to dynamic memory circuit. It is found that $MoS_2$ can greatly enhance the retention time / scalability trade-off of dynamic memory circuits. Unlike silicon, the minimum leakage current in monolayer $MoS_2$ can be limited by SRH generation current instead of GIDL current, which can lead to extremely low leakage currents in the off state. Maximum retention times (~ 1 sec) are found to be orders-of-magnitude higher than conventional Si-based circuits (~250 μs) at comparable dimensions [84]. While the effect of gate leakage on retention time needs to be studied in more detail,

the results clearly show that 2D $MoS_2$ MOSFETs are a promising technology for embedded memory applications.

With these encouraging results from modelling efforts indicating superior circuit performance for low power applications, the next two chapters of the thesis will describe the fabrication and characterization of the embedded DRAM cells using $MoS_2$ as channel material.

# Chapter 5 :

# Process Development and Circuit Applications

## 5.1 Global Back Gated FETs

As chapter 4 concluded, simulations show that $MoS_2$ FETs can have useful applications in the low power circuits. In this chapter, the next step is taken to fabricate $MoS_2$ based devices to verify the performance capabilities. As a first step towards making optimized devices, global back gated devices are fabricated. The schematic of one such device is shown in Figure 5-1. The device fabrication started from a Si wafer, boron doped with resistivity of 1-5 Ω-cm. About 90 nm of thermal oxide is grown over the silicon substrate which will act as back gate oxide. A mask with alignment marks to locate the exfoliated flakes is then prepared. Electron beam lithography (EBL) is then used to pattern the alignment marks and Ti/Au is evaporated and lifted off. $MoS_2$ is then exfoliated from a bulk crystal and transferred onto the substrate. Flakes with appropriate thickness of ~ 5-10 nm are identified using an optical microscope. The flakes are them mapped using the alignment marks and a design is prepared based on located flakes for source / drain deposition. EBL is used again to pattern the source / drain contacts and pads and Ti/Au source / drain metal is deposited and lifted off. An image of one such fabricated device is shown in Figure 5-1 below. The final step in the fabrication process is removal of the thermal oxide from the backside of the wafer. Here, photoresist is spun onto the top side

of the device and baked. Then, the substrate is dipped into 10:1 buffered oxide etch (BOE) solution. The hydrophobic nature of the surface is then checked to confirm removal of all the oxide, followed by metal deposition using electron beam evaporator. Finally, the top-side resist is removed using solvents.

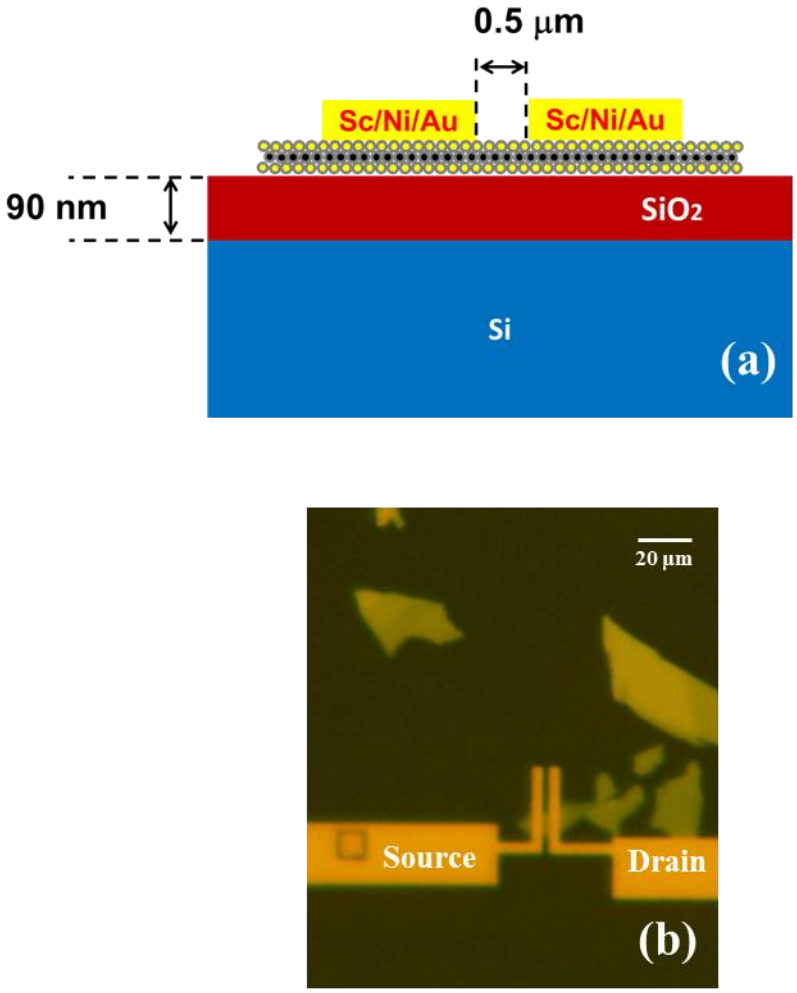



**Figure 5-1:** $MoS_2$ backgated MOSFET. (a) The illustration of a typical global back gated $MoS_2$ device. (b) Optical image of the $MoS_2$ transistor.

To measure and understand the device characteristics of the $MoS_2$ based FETs, DC characteristics are measured using an Agilent B1500A semiconductor parameter analyzer.

Figure 5-2 below shows the transfer characteristics of the transistor. Here, the threshold voltage $V_{th}$ is extracted using constant current definition at a current of 1 nA/µm. It can be observed that device exhibits very low off current.

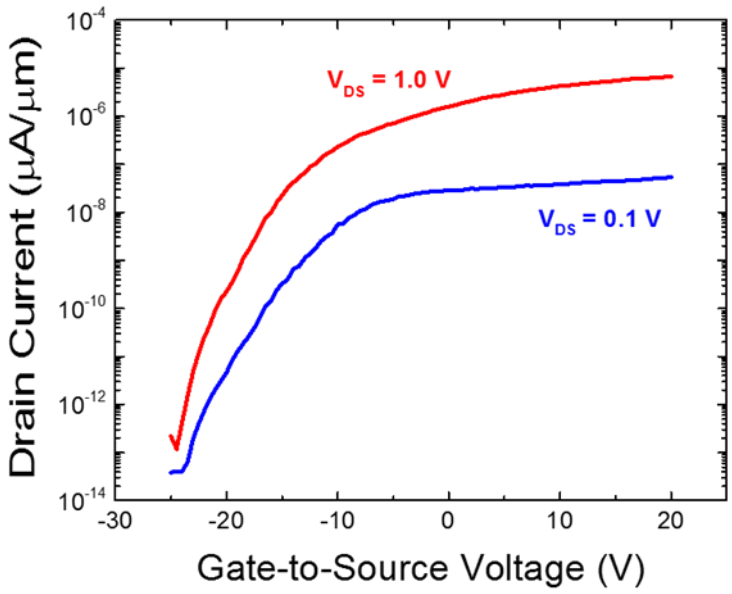



**Figure 5-2:** $I_{DS}$-$V_{GS}$ characteristics of global back gated device. Inset shows the image of the device. This indicates transistor behavior of back gated transistors with $MoS_2$ as the channel material. The device dimensions are 2.13 µm x 0.5 µm. The extracted $V_{th}$ based on constant current definition at a current of 1 nA/µm is -18.5 V. $I_{on}$ and $I_{off}$ observed is 2.5 µA / µm and 0.1 pA / µm respectively.

The output characteristics of the global back gated device (Figure 5-1) are shown below in Figure 5-3. These measurements show that the device has a somewhat non-linear turn-on, indicative of a high-resistance Ohmic contacts. However, for memory applications, the high resistance is not a major problem, since off-state leakage current is the most important parameter in memory circuits. In the next section, the fabrication process and device characteristics locally back gated devices are discussed.

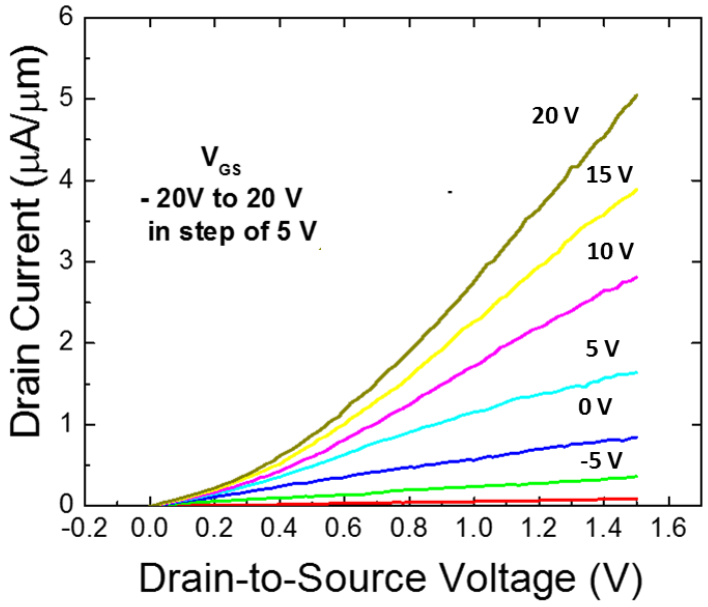



**Figure 5-3:** $I_{DS}$-$V_{DS}$ characteristics of global back gated device. $V_{GS}$ is varied in the steps of 5 V from – 20 V to 20 V.

## 5.2 Local Back Gated FETs

Local back gated devices have a metal gate below $MoS_2$ formed locally by etching the oxide, and depositing metal. It has thin high-K oxide grown over the metal to form gate oxide. This enables much better gate control over channel, much like state of the art devices. Process also involves aligned exfoliation of $MoS_2$ over the local back gates. The detailed process for making local back gated device is as follows:

The device fabrication began by growing ~ 100 nm of $SiO_2$ on p-type silicon substrate. Alignment marks were then patterned using electron beam lithography (EBL) and Ti/Au metal was used to form alignment marks for subsequent process steps. Next, a local back gate was patterned using EBL and a combination of dry and wet etch was used to etch

about 40 nm of $SiO_2$, followed by deposition and lift off of Ti (10 nm) / Pd (30 nm) using electron beam evaporation. To form the gate dielectric, 20-nm of $HfO_2$ was deposited at 300°C using atomic layer deposition (ALD). Mechanical exfoliation of multi-layer $MoS_2$ was then performed to position separate $MoS_2$ flakes over the buried gate electrodes. Finally, Ti (10 nm) / Au (100 nm) was deposited to form source and drain contacts as well as to form interconnect metallization between the two transistors. All devices had a source-to-drain contact separation of 0.5 μm. The $MoS_2$ thickness varied slightly from device to device, but was estimated to be in the range of 6 nm to 10 nm for all devices. Stand-alone $MoS_2$ n-MOSFETs, 1T1C and 2T memory circuits were fabricated. Figure 5-4 shows a schematic diagram of an individual $MoS_2$, and an optical micrograph of a stand-alone device is shown in Figure 5-4.

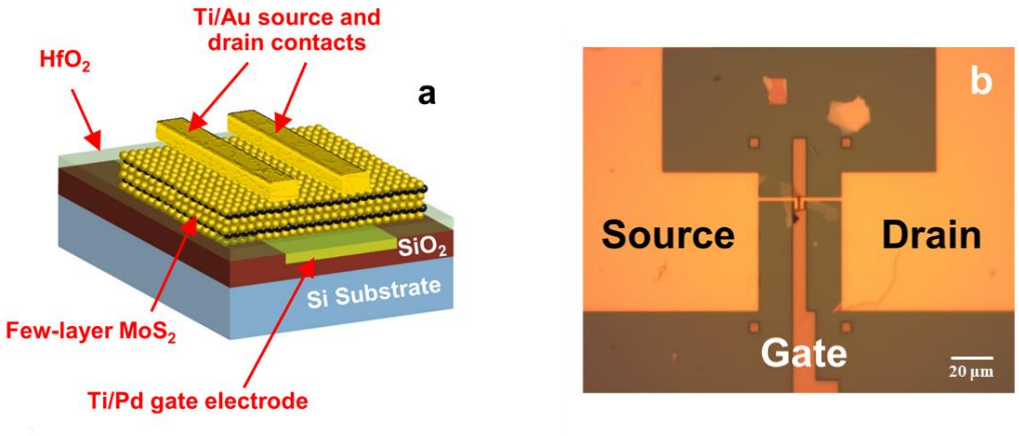



**Figure 5-4:** $MoS_2$ based local back gated device. (a) Illustration of a typical $MoS_2$ MOSFET showing source, drain and gate electrodes. (b) Optical image of the $MoS_2$ MOSFET showing source drain and gate electrode configuration.

The transfer characteristics of the device is as shown below (Figure 5-5). With better gate control, the device exhibit much better DIBL and subthreshold slope performance.

These local back gated $MoS_2$ based devices exhibit exceptional performance. Sub-threshold slope below 75 mV / decade and interface trap density of about 0.4 - 1.5 × $10^{12}$ $cm^{-2}$/eV is routinely achieved. This implies excellent electrostatics and good quality interface between $MoS_2$ and the gate oxide.

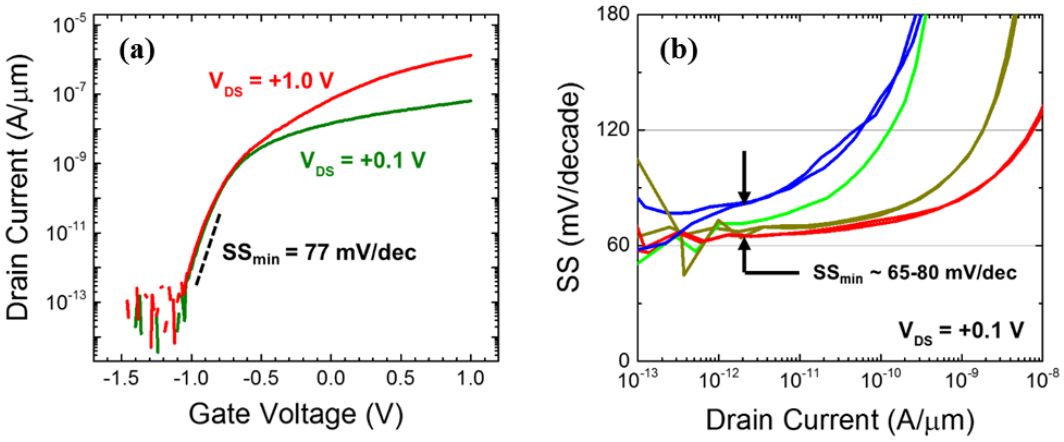



**Figure 5-5:** Local back gated device characteristics: (a) $I_{DS}$-$V_{GS}$ characteristics for a typical $MoS_2$ MOSFET at $V_{DS}$ = +0.1 V and +1.0 V. The subthreshold slope at $V_{DS}$ = +0.1 V was 77 mV/decade and showed virtually no change at higher $V_{DS}$. (b) Subthreshold slope vs. drain current for several $MoS_2$ MOSFETs. The devices had minimum subthreshold slopes between 65-80 mV/decade, corresponding to interface trap density values of 0.4-1.5 × $10^{12}$ $cm^{-2}$/eV.

Within local back gate devices, there can be two possible configurations (Figure 5-6). One where source / drain contacts are overlapping over the gate, while other with underlap. Two possible configurations are shown in the figure below. Underlap process can be more reliable as it avoids overlap over gate leading to less possibility of short between source drain and gate. However, the $MoS_2$ in the underlap region does not get gated by the local back gate, therefore exhibit high series resistance, leading to overall lower current and lesser gate control. Therefore, overlapped devices are preferred over underlap devices.

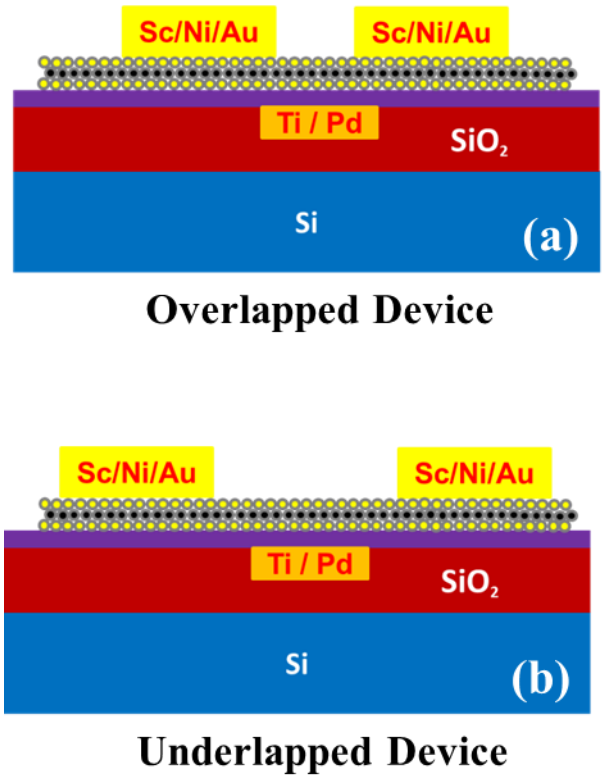



**Figure 5-6:** Schematic of local back gated device: (a) overlapped and (b) underlapped. Part of $MoS_2$ in the underlap leads to additional series resistance leading to lower currents.

These devices can also be passivated using either $HfO_2$ or $Al_2O_3$. Such passivation serves two purposes. One, it reduces the traps during the oxidation process. Also since this a thermal process, it also acts as an annealing process. Combined effect of these two is to reduce the hysteresis of the transfer curve and shift $V_{th}$. The transfer characteristics of the device with 25 nm of $HfO_2$ are shown in Figure 5-7 below. Substantial increase in on current can also be observed after the passivation.

However, it can be observed that subthreshold slope degrades after the passivation, this is due to the traps and imperfections at the interface. Since in memory application we are primarily interested in achieving lowest possible off current, having good subthreshold

slope is vital. Therefore, it was decided to not use passivation technique during the fabrication of memory circuit.

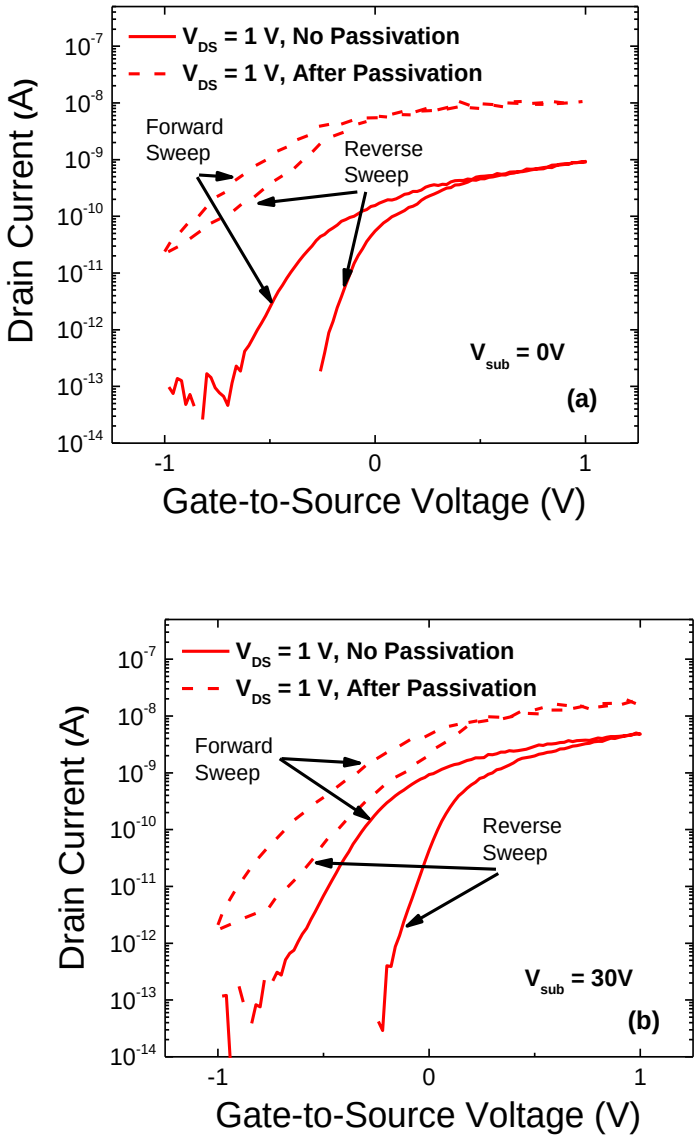
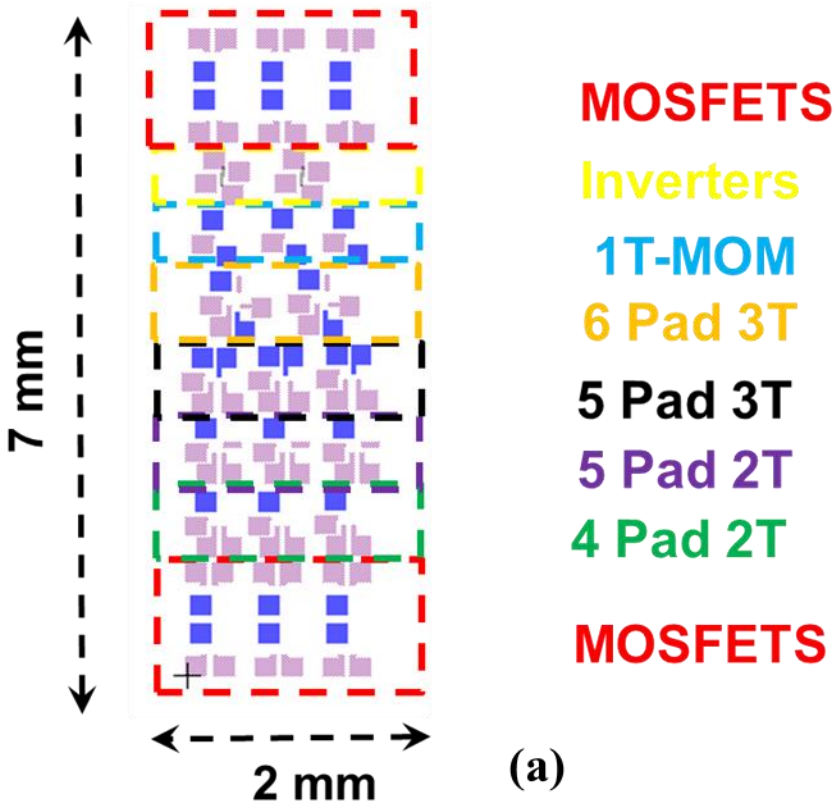



**Figure 5-7:** $I_{DS}$-$V_{GS}$ characteristics of underlapped local back gated device with and without passivation: (a) at no substrate bias,(b) at substrate bias of 30 V.

## 5.3 Layout Considerations

A generic back gated layout is designed with various assorted combination of devices and circuits. The back gated die is re-usable from exfoliation onwards of the process flow. The layout used in this work is shown below. This contains discrete MOSFETs at both ends, along with some variations of 1T1C, 2T and 3T memory cells. It also has invertor circuit on it.

Reusability of the back gated die gives flexibility of making discrete devices and test structures, verifying that process flow is working and resulting into desirable devices, and then going for making actual memory cells on the same back gated die. The layout of some of the individual memory cells are shown below. There are two versions of 2T cell, one is with 4 pads (2 write and 2 read lines), and other is 5 pad 2T cell. In 5 pad 2T cell, an extra probing pad is used to probe the storage node. Such pad is smaller (70 µm × 70 µm) than standard pad sizes used (200 µm × 200 µm). This is to minimize the parasitic capacitance of the probing pad. As probing pad itself can act as capacitance and lead to steal some of the charge on the storage charge. Therefore, this pad is only useful mainly to troubleshoot the circuit in case it is not working. It may not be useful in making actual measurements, as the interpreted stored charge may not be accurate due to parasitic capacitance of the pad itself.



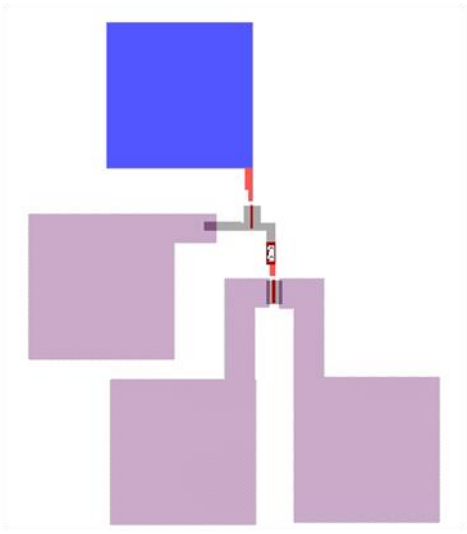




**Figure 5-8:** Layout design: (a) Back gate re-usable layout of the full sample, (b) 4 terminal 2T cell layout.

## 5.4 Test Structures

In order to develop reliable via based process to connect two transistors, test structures can be used to confirm that the via connections are working. In the circuit intended to be fabricated, in particular in 2T cell, drain of one device has to be connected to gate of another device. Therefore, via has to connect through the gate oxide. In order to enable electrical connection between the two transistors, via openings needed to be formed. In order to realize these, oxide based hard mask is used. After gate oxide deposition ($HfO_2$), an additional $Al_2O_3$ layer was deposited by ALD, and via opening were patterned in PMMA using EBL. The $Al_2O_3$ was then etched over the extrinsic portion of the gate electrode using a wet etch and then reactive ion etching was used to etch the $HfO_2$. After this etch, the PMMA was removed and the $Al_2O_3$ hard mask was stripped using wet etch.

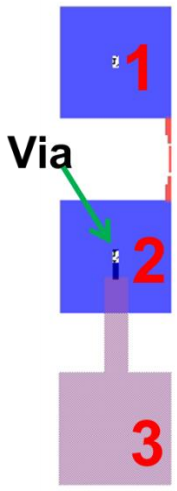



**Figure 5-9:** Test structure connecting two metal layers through via. Contact point 1 and 2 are directly connected with source and drain contact metal level, while contact points 2 and 3 (Gate metal level) are connected through a via. A good contact between 1 and 3 ensures working via contact.

Since troubleshooting a circuit is more complex task, a test structure connecting two pads at different metal layers to be connected through the oxide is added into the layout. This enables independent verification of successful or unsuccessful realization of the via. One such via layout connecting two different metal layers through gate oxide is shown in Figure 5-9 above.

With this test structure, I-V characteristic can be swept between point 1 and 2 and between 1 and 3. If the I-V characteristic between 1 and 3 does not exhibit substantially large resistance, it is safe to conclude that via is connecting the two metal layers. Figure 5-10 below shows comparison of such I-V curve between points 1 and 2 and point 1 and 3. Based on this curve, it can be concluded that via is working.

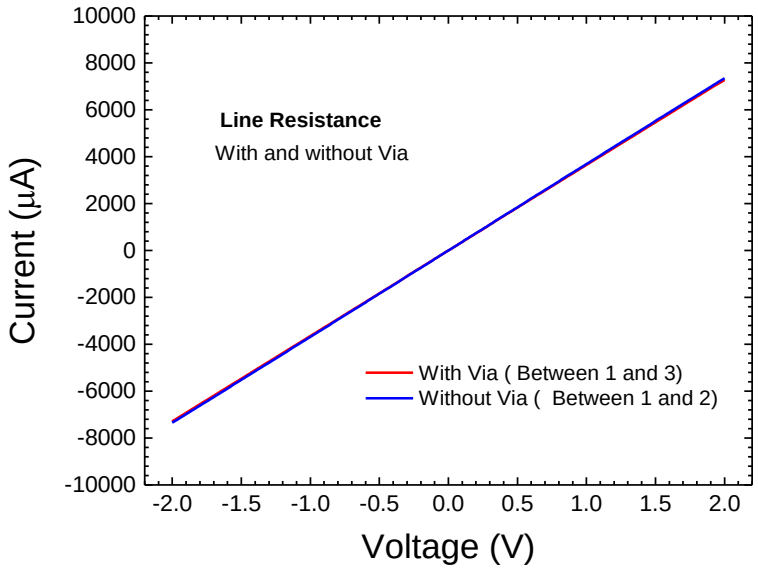



**Figure 5-10:** *I-V* characteristics of the resistance between pads with and without via. Close resemblance of the two curve indicates the via resistance is negligible. Probing points are as shown in Figure 5-9.

## 5.5 1T1C and 2T Circuits

After step by step development of process, starting from global back gated device, to local back gated device, and identifying some test structures to verify come process steps, this section will describe in detail the fabrication process used for realizing 1T1C and 2T memory cells based on $MoS_2$ as the channel material.

The fabrication of our 1T1C and 2T memory cell started with dry thermal oxidation of about 110-nm-thick $SiO_2$ layer on a Si substrate. Alignment marks were first patterned on the substrate by spinning poly methyl methacrylate) (950 ka.u. PMMA) and then patterning with electron-beam lithography (EBL) using a Vistec EBPG 5000+ system. After development in 1:3 MIBK:IPA and rinsing in IPA; Ti / Au (10 nm / 100 nm) was deposited using electron-beam evaporation followed by a solvent liftoff in acetone followed by an IPA rinse. Next; the local back gate contacts were patterned. Once again; 950 ka.u. PMMA was spin-coated on the wafer and EBL was used to pattern 3-μm wide; 80-μm long stripes connected to enlarged pad regions for wafer probing. After development in 1:3 MIBK:IPA; the sample went through a 5sec oxygen plasma to remove PMMA residues and a reactive ion etching with $CHF_3/CF_4/Ar$ to create about 40-nm deep recess in the $SiO_2$ layer. The sample was then etched in a 1:10 buffer oxide etch (BOE) for 12 seconds to create a roughly 50-nm recess in the $SiO_2$; and the recess depth was determined using a surface profilometer (KLA-Tencor P-7) before Ti / Pd (10 nm / 40 nm) was evaporated using electron-beam evaporation. After liftoff in acetone / IPA; 20 nm of $HfO_2$ was deposited using atomic layer deposition (ALD) using Tetrakis(dimethylamido) hafnium(IV) and water vapor as the

precursors. To form via, a hard mask of $Al_2O_3$ is deposited using ALD. Vias were patterned using EBL using PMMA as mask. PMMA is left onto the sample, and $Al_2O_3$ is etched using 1:10 BOE solution for about 120 seconds. This is followed by about 180 second STS etch of $HfO_2$. The etch thicknesses were verified using profilometer. PMMA is then removed by submerging sample into acetone overnight, and rest of the $Al_2O_3$ is etch out using 1:10 BOE solution for about 120 seconds. $MoS_2$ (purchased from SPI) mechanically exfoliated onto Polydimethylsiloxane (PDMS) stamps activated on glass slides. With a specially designed optical alignment station; few-layer $MoS_2$ flakes were aligned and transferred onto the same gate finger on the $HfO_2$-coated substrate. A solvent clean was performed to remove PDMS residue and then PMMA was spin-coated right after transferring to prevent air degradation of the BP; and the sample was then stored in a black jar filled with desiccant. PMMA was spin-coated and EBL was then performed to open source and drain contact. Ti / Au (10 nm / 80 nm) metallization was again evaporated and lifted-off in acetone/IPA to complete the circuit fabrication. After completion of the lift off; the sample was loaded into the vacuum chamber of the Lakeshore cryogenic probe station for testing. No surface passivation was utilized. Fabricated 1T1C and 2T cells are shown below in Figure 5-11 and Figure 5-12.

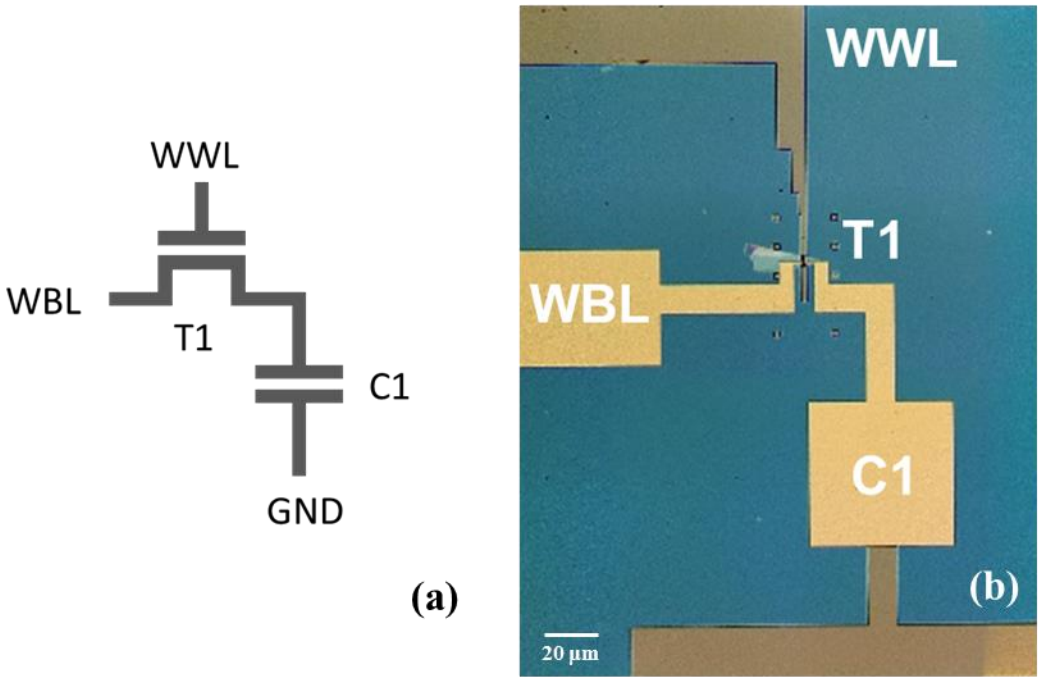



**Figure 5-11:** Fabricated 1T1C memory cell. (a) Schematic diagram and (b) image of the fabricated cell.

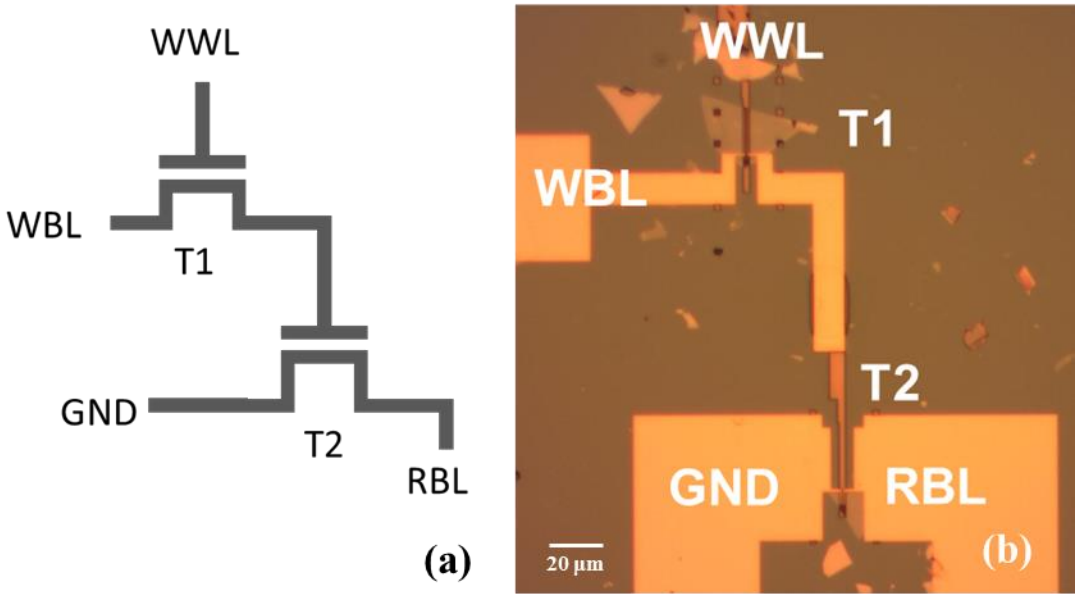



**Figure 5-12:** Fabricated 2T memory cell. (a) Schematic diagram and (b) image of the fabricated cell.

## 5.6 DC Characteristics

To test the basic functionality of the 2T cell, DC measurements can be utilized. Since 2T cell is a combination of a pass transistor and a storage transistor, pass transistor can be turned on, and bias on storage transistor can be varied. Here when the write transistor is turned on by applying 1V at $G_w$, the voltage swept on $D_w$ acts a gate voltage applied to storage transistor. Therefore the nature of the DC sweep is similar to a standard transfer curve of the transistor. The DC characteristic of the 2T memory cell is shown in Figure 5-13.

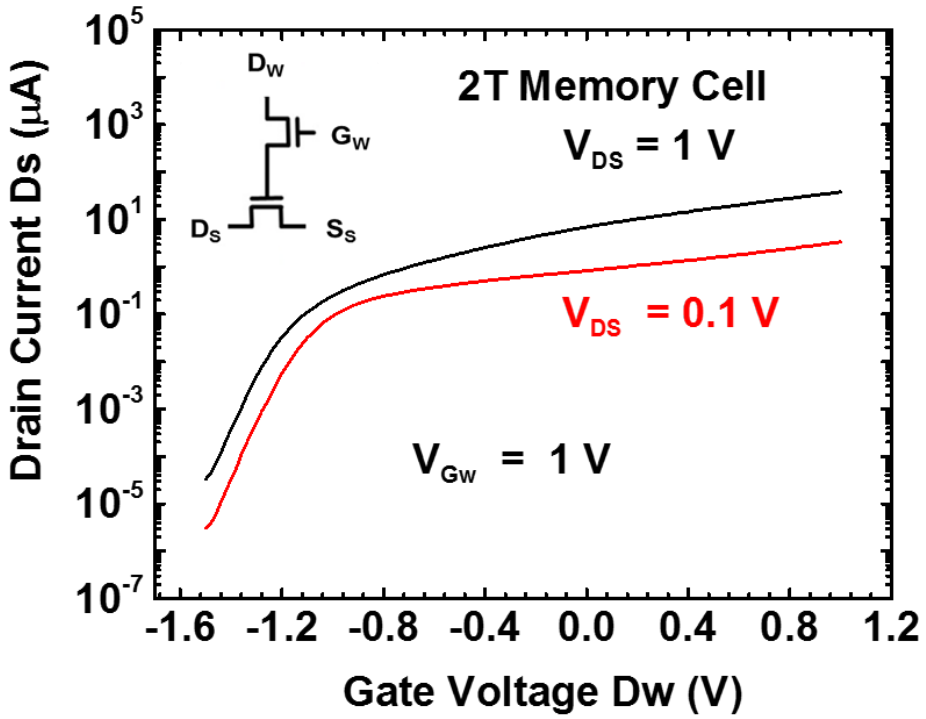



**Figure 5-13:** DC response of the 2T memory cell (as shown in inset) confirming its functionality. Here, write transistor is turned on by applying 1V to Gw terminal, and Dw is swept to measure the current at the drain of storage transistor Ds.

While this characteristics is predominantly shows the characteristics of storage transistor, the write transistor also has to work to get the full DC transfer curve. Therefore, this acts a verification of having both write and storage transistor working as desired. Unfortunately, since there is no extra pad taken out for 1T1C cell, such verification is not possible for 1T1C cell.

## 5.7 Conclusions

This chapter demonstrated fabrication of global back gated, local back gated devices and memory cell circuits. This verifies that $MoS_2$ material can be used along with exfoliation technique to make devices as well as more complex via based circuits. DC characterization for both devices and circuit is presented. Local back gated overlapped devices provide better gate control as well as excellent electrostatic. With verification of the functional via based 2T cell based on $MoS_2$ as the channel material, the cell is ready to be tested for retention time and other time dependent analysis.

# Chapter 6 :

# Memory: 1T1C and 2T Circuits

## 6.1 1T1C and 2T Cells

The last chapter described the process development and DC behavior of the 1T1C and 2T $MoS_2$ based memory cells. This chapter is focused towards understanding and characterizing time dependent behavior of the $MoS_2$ based memory cell. To do so, we begin with understanding working principles and practical consideration of the memory cell. Figure 6-1 below shows the schematic of the 1T1C cell. In a real memory system, there is an array of the cells and actual operations are performed at the word line and bit line level rather than individual cell. However, we have fabricated individual cells and so it is important to describe their operating principle and the ways to characterize the individual cell.

A single 1T1C memory cell consists of a pass transistor connected to a storage capacitor. When the pass transistor is turned on, data is stored on the capacitor (storage node). Due to various leakage mechanisms (described in chapter 4), this stored charge leaks over time, leading to loss of data if not refreshed periodically. Therefore, data needs to be re-written (or "refreshed") at a fixed time interval. The duration of time over which data can reliably be retained on the storage node is called the retention time. Longer retention time is desirable, as it leads to less frequent refresh, and thus lower power consumption.

Now, in order to read the stored data, the pass transistor is again turned on, and data is read. This means that data is compared with half of the supply voltage, and based on the stored voltage on capacitor, the nature of the stored data is determined. It is important to notice that in a 1T1C cell, read and write functions are performed by the same bit and word lines, which means data is destroyed during the read operation.

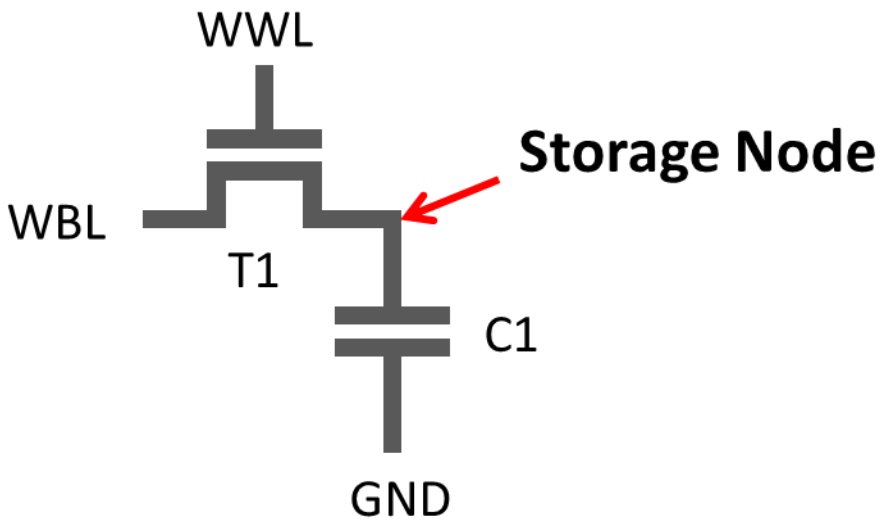



**Figure 6-1:** 1T1C memory cell schematic. Here WWL and WBL denotes write word line and write bit line respectively. Capacitor is used as charge storing device here, with one of the terminal of the capacitor C1 acting as a storage node.

Instead of using a capacitor, a 2T memory cell uses another transistor as the storage device. The schematic of one such memory cell is shown in Figure 6-2 below. As described in the previous chapter, 2T cells have an advantage of being CMOS compatible. Another advantage of the 2T cell is it uses a de-coupled write and read scheme. This means that, unlike the 1T1C cell, the 2T cell does not use same bit and word lines to read and write.

Rather the 2T cell has separate write and read word / bit lines which enables non-destructive readout of the data from the memory cell.

To write the data into a 2T cell, the write pass transistor (T1) is turned on, and data is transferred to the storage node. To read the data, the read bit line is turned on (active low), and data is read. Although the 2T cell has advantage in terms of CMOS compatibility, non-destructive read and decoupled read and write, the storage capacitance value is much lower than that of in the case of 1T1C cell. This underscores the need for the low leakage devices which will lead to higher retention time.

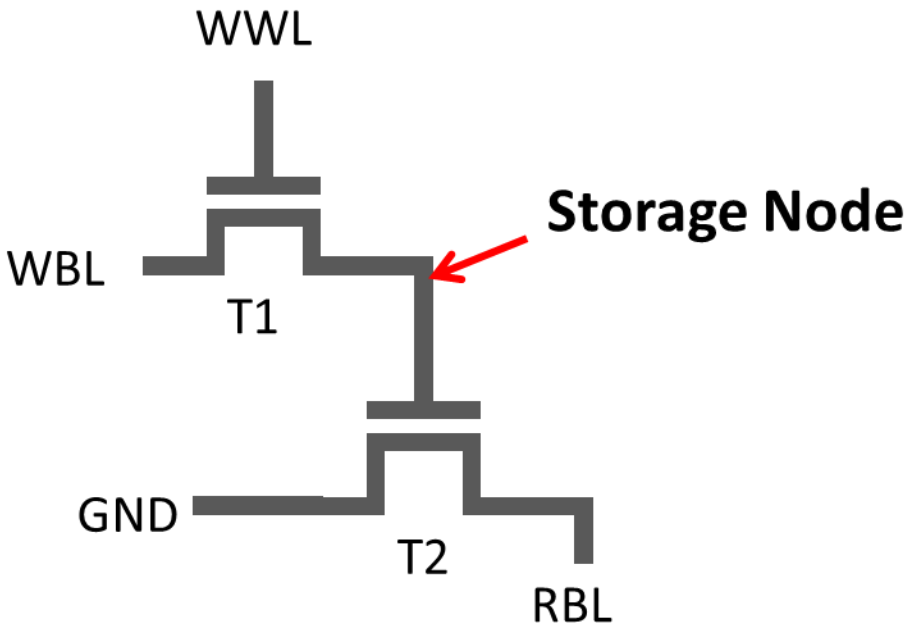



**Figure 6-2:** 2T memory cell schematic. The capacitor in 1T1C cell is replace by a transistor (T2) here. T2 acts as charge storing device with gate terminal as the storage node. Here WWL and WBL denotes write word line and write bit line respectively, and RBL indicates read bit line.

In this work, we demonstrate for the first time the capability of ultra-low (~ 1 fA/μm) leakage currents in $MoS_2$ through the use of dynamic memory cell circuits. In particular,

both one transistor one capacitor (1T1C), and two transistor (2T) configurations have been realized, and the retention times are characterized for both systems. Based upon the measured retention times, and the estimated capacitance of the device geometry, our results reveal leakage currents far below the noise floor of conventional dc measurements. There are four major component that can dominate the low current regime in semiconductor devices. These are: subthreshold leakage, gate induced drain leakage (GIDL), Shockley-Read-Hall (SRH) generation/recombination current and direct tunneling current from the gate. In highly scaled silicon devices, the low current regime is usually dominated by GIDL, gate leakage and subthreshold leakage. Interestingly, the leakage current does not follow the trends expected for contact-limited current injection, but instead has a constant minimum current suggestive of Shockley-Read-Hall (SRH) as the mechanism limiting the leakage current. This implies that measurement methods that can go further down into the low current regime need to be developed in order to analyze and understand new materials and devices fully.

## 6.2 Parameters and Measurement Setup for 1T1C

As discussed in section 4.1, one of the requirements of low power memory cell is to have lower $I_{MIN}$. The device then can be biased at that minimum current point to minimize the leakage current and maximize retention time. The voltage at which the device can be biased to hold the data is termed as the hold voltage ($V_{HOLD}$), and the time for which the data is held (the delay between write and read pulses) is called the hold time ($t_{HOLD}$). Here,

initially, a gate voltage of -1.5 V gate is chosen as the hold voltage. During the write operation, the drain voltage of the transistor (bit line) is raised from 0 V to 1 V, and the gate voltage of the transistor (word line) is raised from -1.5 V to 1 V. The drain voltage (bit line) is raised about 10 μsec earlier, and drops down to zero about 10 μsec latter than the gate voltage such that it encompasses the gate voltage (word line) signal. During the write operation, the transistor is in the on state and so it charges the capacitor. To read the data, the conditions that occur in an actual array-based memory are mimicked. In a 1T1C memory array, the stored voltage is compared with one half of the bit line voltage, and the value of the stored data is determined based upon whether the voltage level rises or lowers at the bit line. To imitate this, in our measurements, a 0.5 V pulse is provided to the drain of the transistor during the read operation, and the gate is turned back on as in the case of write operation. The input write and read pulses can be seen in Figure 6-3. During the read operation, the bit line voltage is at 0.5 V, and the potential on the capacitor changes as the hold time is changed. If the hold time is small, the charge will be retained on the capacitor, leading to higher voltage across the capacitor compared to 0.5 V applied at the bit line. In this case, current flows out of the charged capacitor. This current is transformed into a voltage by connecting a 20 kΩ resistor between the capacitor and ground. The voltage across this resistor indicating data retention is shown in the Figure 6-3. If the hold time is large, various leakage mechanisms may lead to discharge of the capacitor. This will lead to loss of charge on the storage capacitor, which in turn can lead to loss of stored data. In this case, the voltage across the capacitor will drop below the applied voltage of 0.5 V on

the bit line during the read operation. This means that current will flow into the capacitor to charge it, leading to a change in the sign of the voltage across the resistor (Figure 6-3).

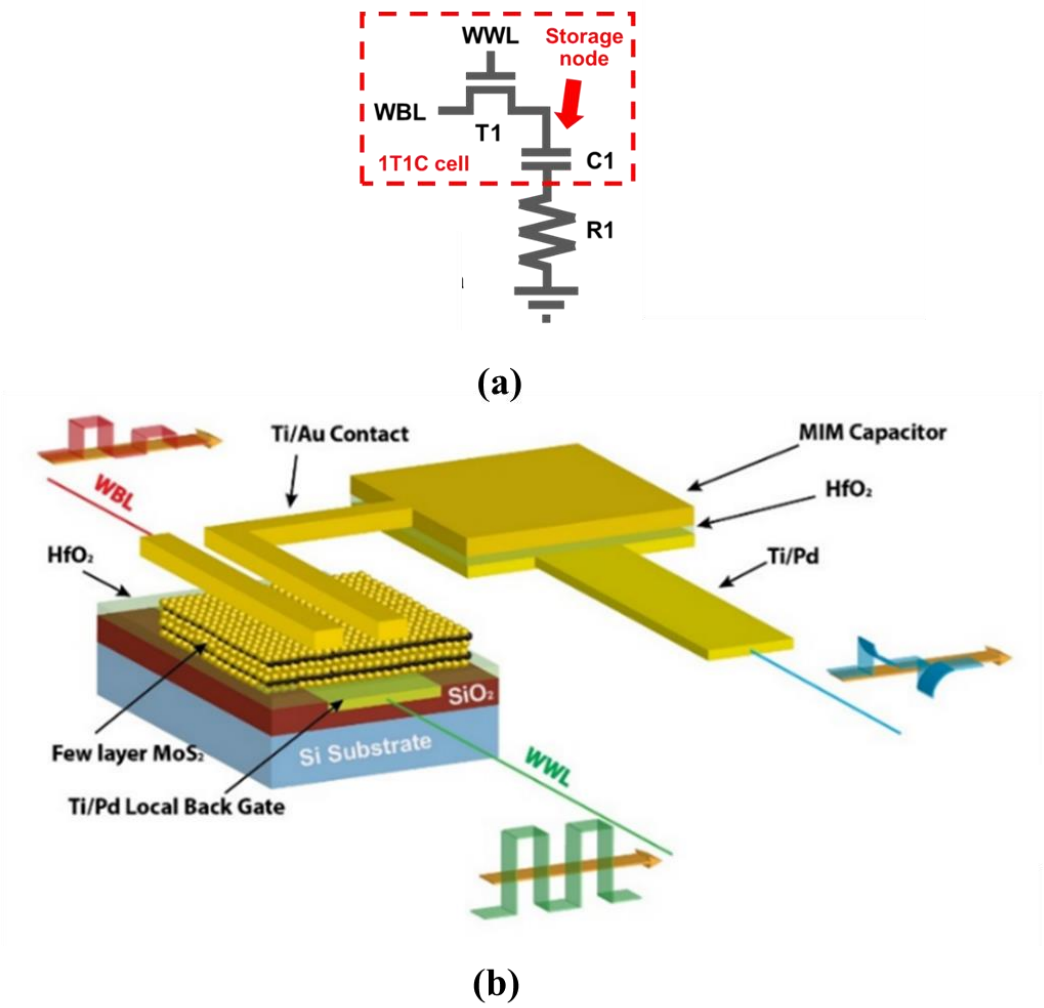



**Figure 6-3:** 1T1C memory cell description and measurement results. (a) Circuit schematic of 1T1C circuit. (b) Illustration of 1T1C memory cell operation showing input and output signals at the write and read lines. Here WBL and WWL are the inputs, and output is measured at the storage capacitor.

Therefore, depending on whether the data is retained or not, the direction of change in voltage across the resistor during the read operation will be either positive or negative. This can be used to characterize the retention time of the 1T1C cell. For measurement of 1T1C

cell retention time, automated measurements were performed using a Keysight 33500 Waveform Generator, and Tektronix 3000C Oscilloscope. Pulses are generated to enable data writing and reading (Figure 6-4). The measurement results are discussed in the next section.

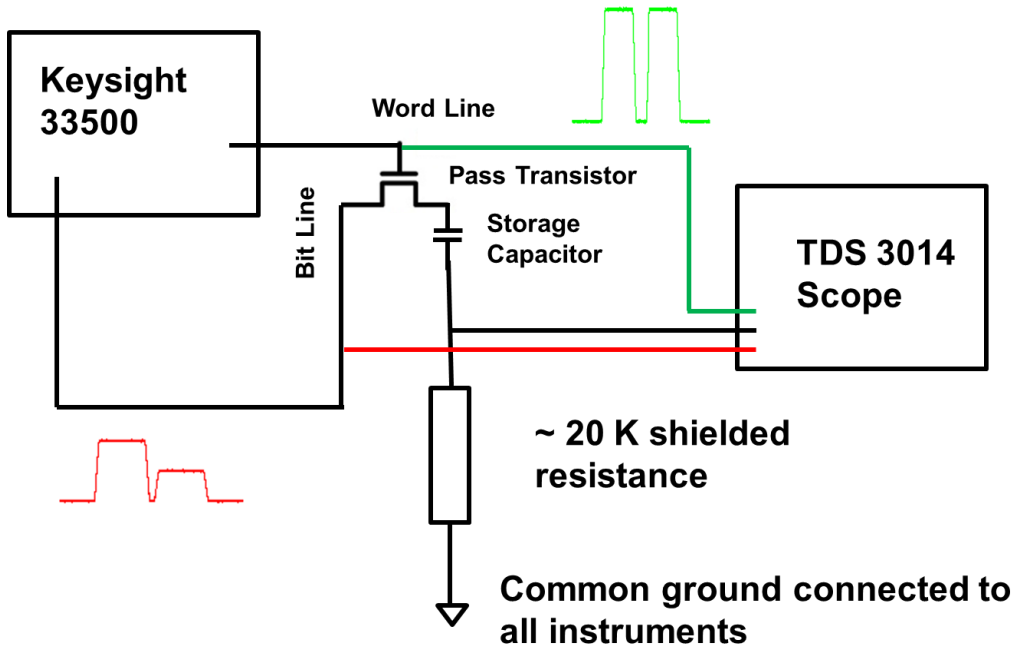



**Figure 6-4:** Measurement setup for 1T1C time dependent measurements. A 20 kΩ shielded resistor was used to estimate the current direction and value through the storage capacitor.

## 6.3 Retention Time Measurements for 1T1C Circuit

To characterize the precise retention time of the 1T1C cell, automated measurements are performed where write and read pulses are applied in succession with varying hold time (delay between write and read pulses). Hold time is varied from 10 µs to 1 s at a fine true log scale with 20 points in a decade. Change in direction of output voltage is observed at 251.1 ms retention time value. To confirm this, another way to estimate the retention time

is to calculate the charge stored onto the storage capacitor. When charge stored on the capacitor reaches to near zero, data is lost. Stored charge on the capacitor can be estimated by converting the voltage across the resistor back to current, and integrating the current over time. Figure 6-5 shows the calculated charge vs the hold time for the 1T1C cell.

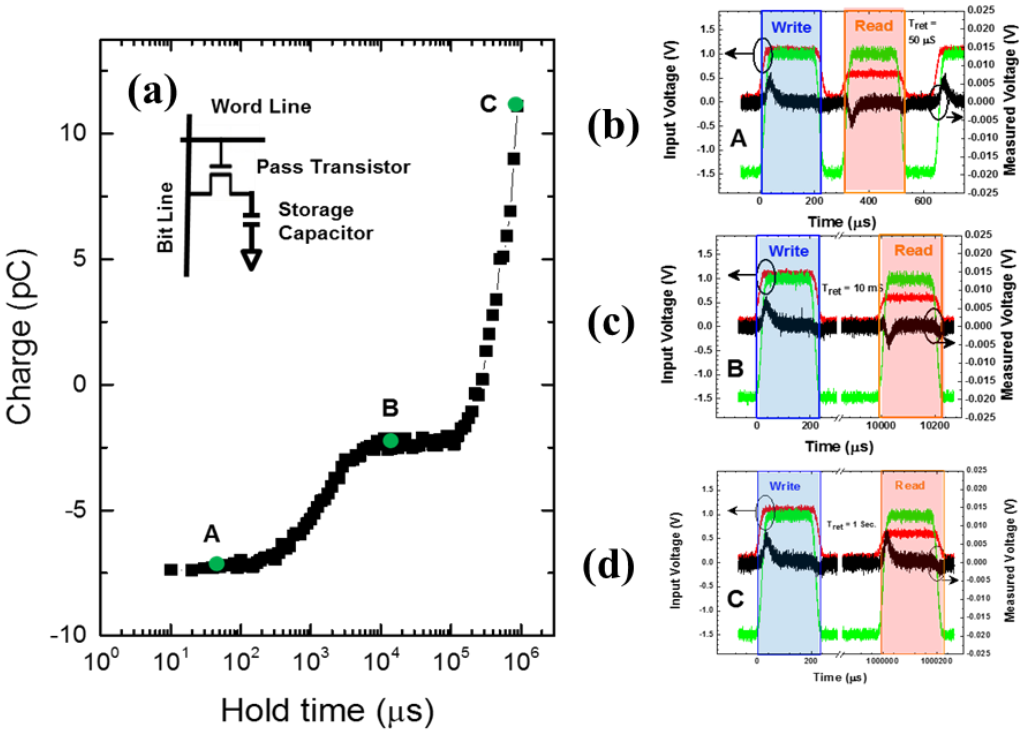



**Figure 6-5:** Waveforms and integrated charges of 1T1C Cell : (a) Integrated charges of the 1T1C Cell based on output waveforms (as shown at points A, B,C).(b) Write and read operation waveform at point A. Here since data is retained, there is negative spike in read operation. Integration of that negative spike gives charge stored on capacitor which is plotted in (a), (c) Write and read operation waveform at point B, (d) Write and read operation waveform at point C. Here since data is not retained, there is positive spike in read operation. Integration of that negative spike gives charge stored on capacitor which is plotted in (a).

It can be observed that the stored charge changes its sign for a hold time of 251.1 ms, indicating this value is a good estimate of the maximum retention time for this $MoS_2$ based

1T1C cell. Similarly, the hold voltage $V_{HOLD}$ can be changed from -1.5 V to lower voltages and experiment can be repeated. Based on the integration of current, the estimated charge as a function of hold time is shown in Figure 6-6 for different values of $V_{HOLD}$. As expected, as the hold voltage is made more positive, there is more leakage in the pass transistor, leading to a reduction in the retention time.

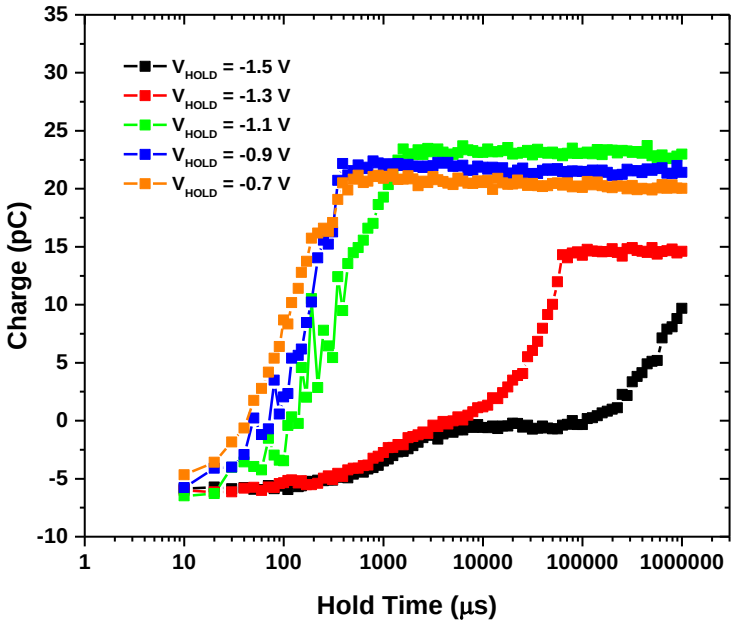



**Figure 6-6:** Charge stored on capacitors with write 1 at variour hold voltage $V_{HOLD}$. Here Black, red, green, blue and orange curves represents $V_{HOLD}$ of -1.5, -1.3, -1.1, -0.9, -0.7 V respectively.

## 6.4 Pulsed Readout Measurements for 2T Cell

A depiction of the $MoS_2$ based 2T cell is shown in Figure 6-7. This cell consists of two transistors, a write transistor (T1), and a storage/read transistor (T2). The cell operates as follows: when transistor T1 is turned on, data is written onto the gate of transistor T2, where

this gate performs the same function as the storage capacitor in a 1T1C cell. In this cell, the charge stored on the gate of transistor T2 changes its conductance, and so the memory state can be read out simply by measuring the current through T2. However, since the overall capacitance of the storage node is significantly less than that of the 1T1C, the retention time is also lower. While for practical applications, this is a disadvantage since it leads to shorter retention times, this can be beneficial for our measurements since the shorter retention times allow the extraction of lower leakage current values.

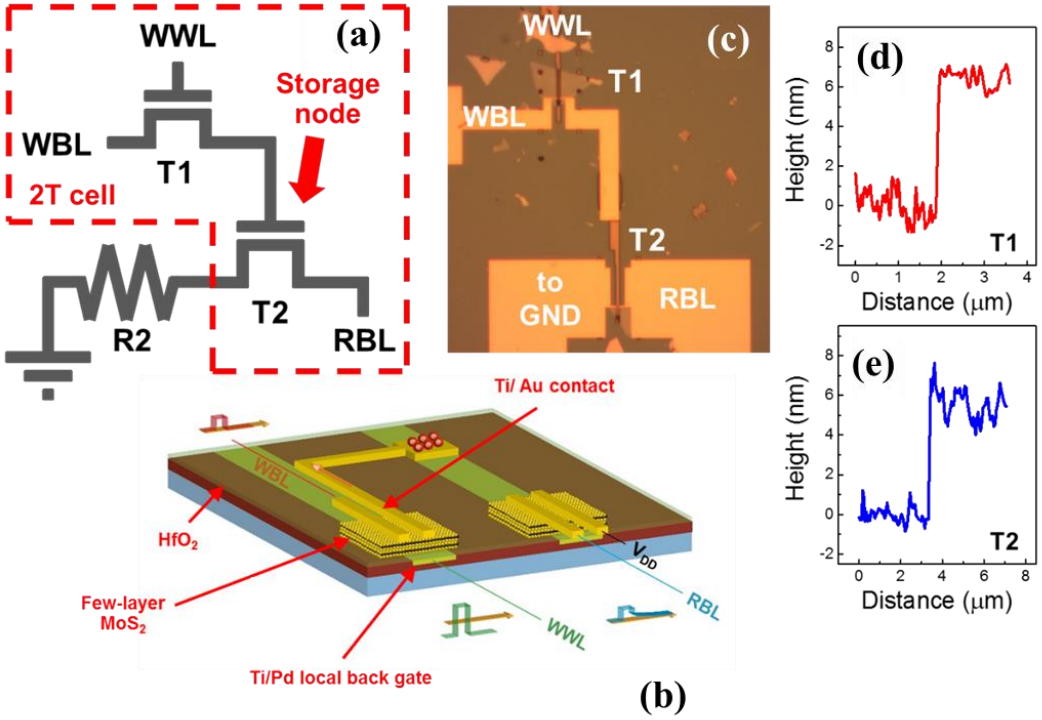



**Figure 6-7**: Two transistor (2T) memory cell description. (a) Circuit schematic of 2T memory circuit. (b) Illustration of 2T memory cell operation showing input and output signals at the write and read lines. (c) Optical image of 2T cell using showing both $MoS_2$ MOSFETs. The resistor, R2, is connected externally.(d) AFM line scan of MoS2 used for transistor T1. (e) AFM line scan of $MoS_2$ used in transistor, T2.

An estimate of the retention time of the 2T cell can be made by writing data into the storage transistor and observing the discharge of the current over time. This discharge is a

direct indicator of the leakage performance of the write transistor. Lower leakage will take higher time for current to discharge. To measure this, a resistor of 20 kΩ value is connected in series with the storage transistor (details of the measurement setup are in the chapter 5), and data is written onto the storage transistor with one of its terminal connected to $V_{DD}$ (as shown in Figure 6-7(a)). We here considered the retention time to be the time required for the voltage to drop down to 50% of its original value at the end of the write pulse. This retention time changes based on the retention voltage chosen. This is because the leakage current through the write transistor changes drastically with the retention voltage. We performed two sets of measurements in order to extract the leakage current, $I_{LEAK}$, in the 2T geometry. As shown in Figure 6-8 in our initial set of measurements, synchronized pulses were applied to the bit line and word line, and then the resulting change in current through transistor T2 was observed by measurement the voltage across a 20 kΩ resistor which was connected in series with T1.

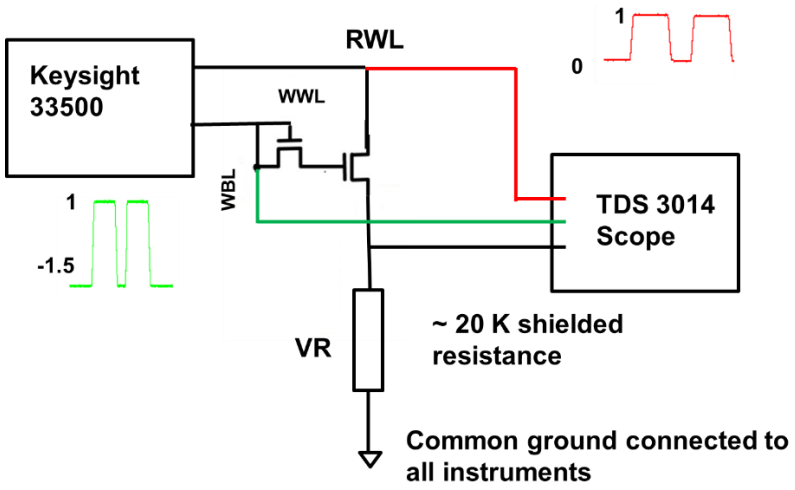



**Figure 6-8:** Measurement setup for 2T time dependent measurements. A 20 kΩ shielded resistance can be used to estimate the leakage current through the storage transistor.

The retention time measurement results are shown in Figure 6-9, where the current is plotted vs. time on a log scale for $V_{HOLD}$ = -1 to -1.6 V. The retention time, $\tau$, based upon the required time for the current to drop to 50 % of its original value at the end of the write pulse for different values of the hold voltage, $V_{HOLD}$, applied to the gate of transistor write transistor, is shown in Figure 6-10.

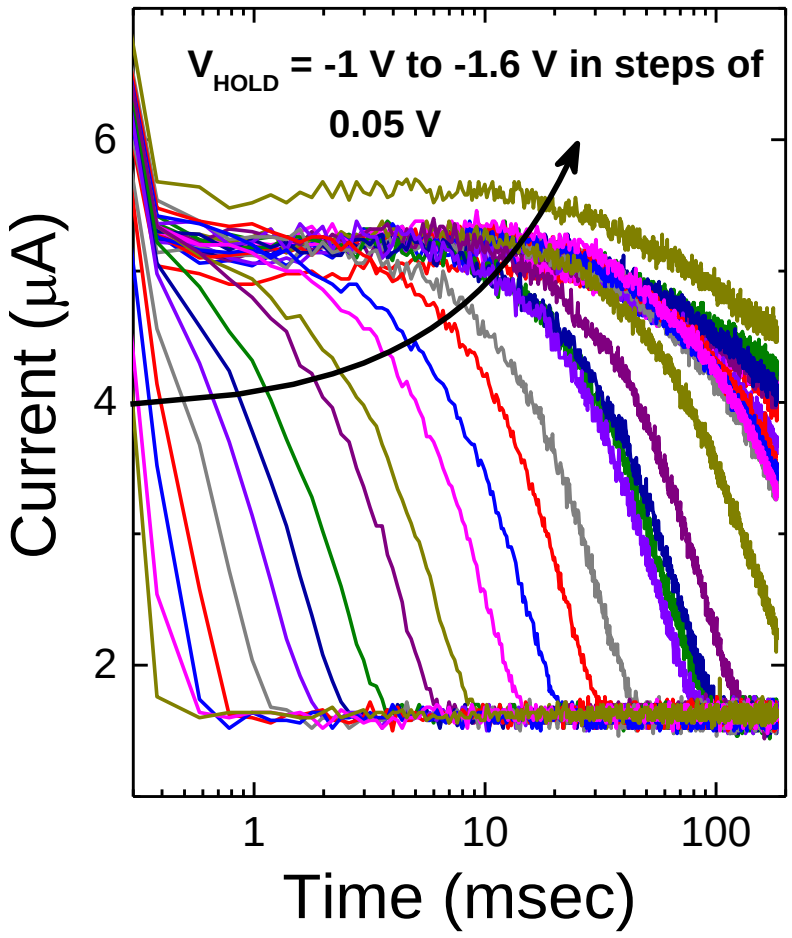



**Figure 6-9 :** Output current of 2T Cell with varying $V_{HOLD}$ at log scale starting from -1 V to -1.6 V at 0.05 V steps. Substantial change in retention time (at log scale) can be observed.

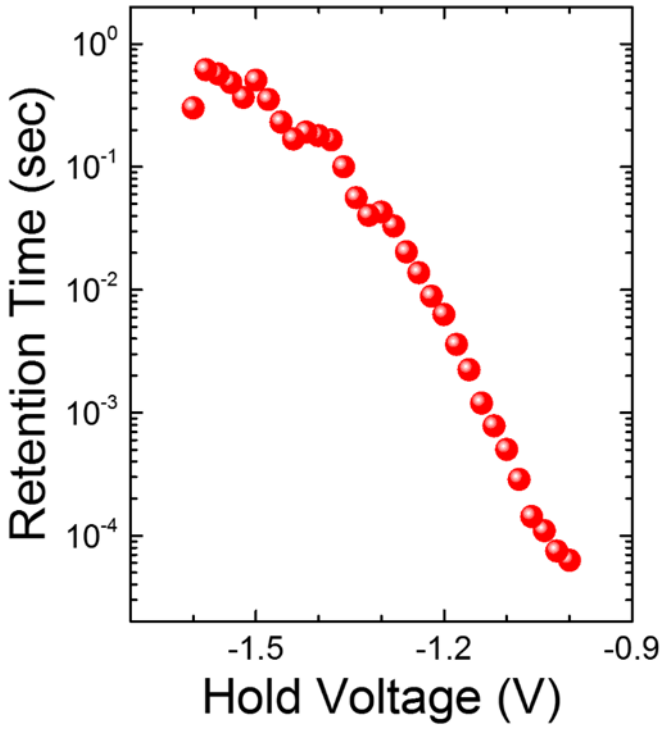



**Figure 6-10:** Extracted retention time based on waveforms in Figure 6-9.

## 6.5 DC Readout Measurements for 2T Cell

Another way to characterize the effect of $V_{HOLD}$ on the retention time is to perform a direct measurement of the current through transistor T2 using a semiconductor parameter analyzer. This can be done by measuring discharge current using the measurement setup (Figure 6-11) and estimating the retention time based upon the same criterion used for the pulsed measurements as shown in Figure 6-12.

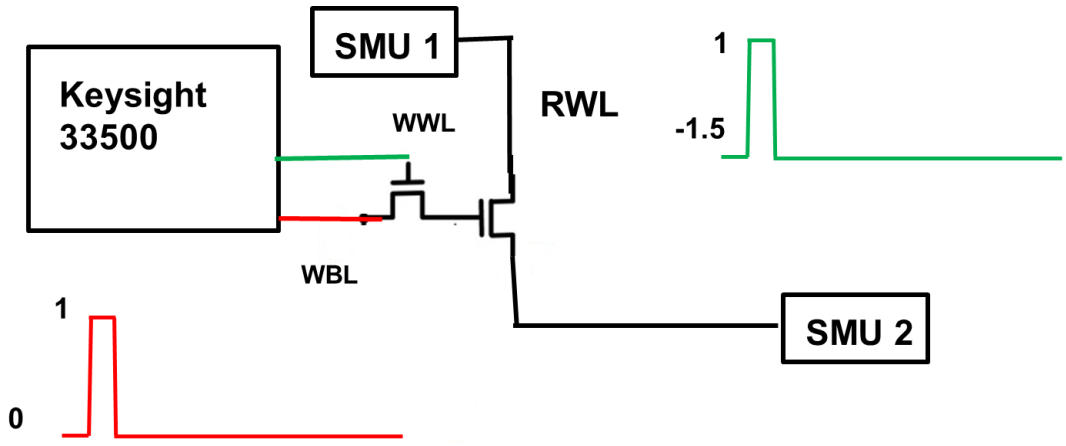



**Figure 6-11:** Measurement setup for 2T time dependent direct current measurements using source–measurement units (SMUs) of the Agilent B1500A. Here, 20 kΩ resistance is eliminated, and leackage current is directly measured using SMU 2.

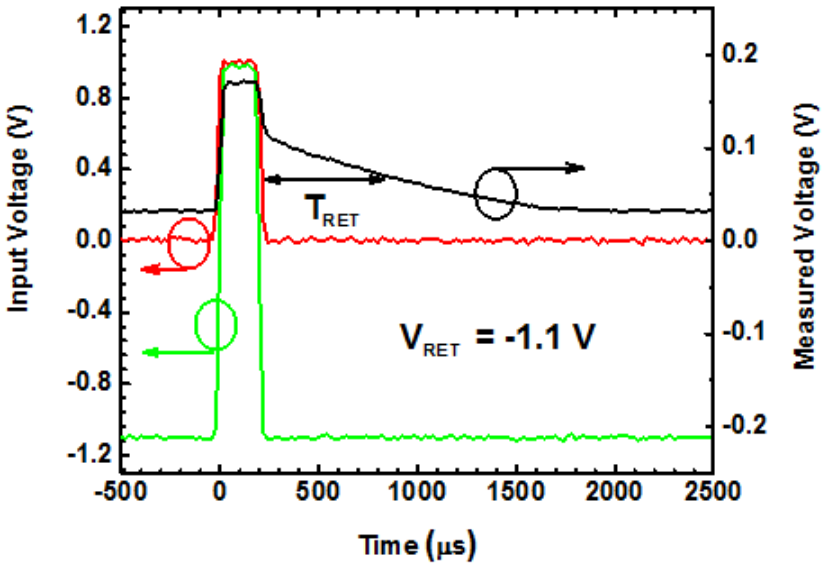



**Figure 6-12:** Typical input and output curves, and retention time defination for 2T Cell. Red curve indiacates write bit line, and green curve indicates the write word line (left Y axis). Black line shows measured voltage across the resistance (right Y axis) which is estimation of leackage through the storage transistor.

The quasi-DC method of measuring the current in transistor 2T was utilized to allow retention times > 1 sec to be characterized. In this methodology, the retention time of the 2T cell was made by writing data into the storage transistor and simply observing the

discharge of the current over time using an Agilent B1500A (Figure 6-11). The results for a series of measurements of the current through transistor T2 vs. time for values of $V_{HOLD}$ from -1.2 to -2.2 V are shown in Figure 6-13. Here, it is clear that retention times longer than 1 second can be obtained.

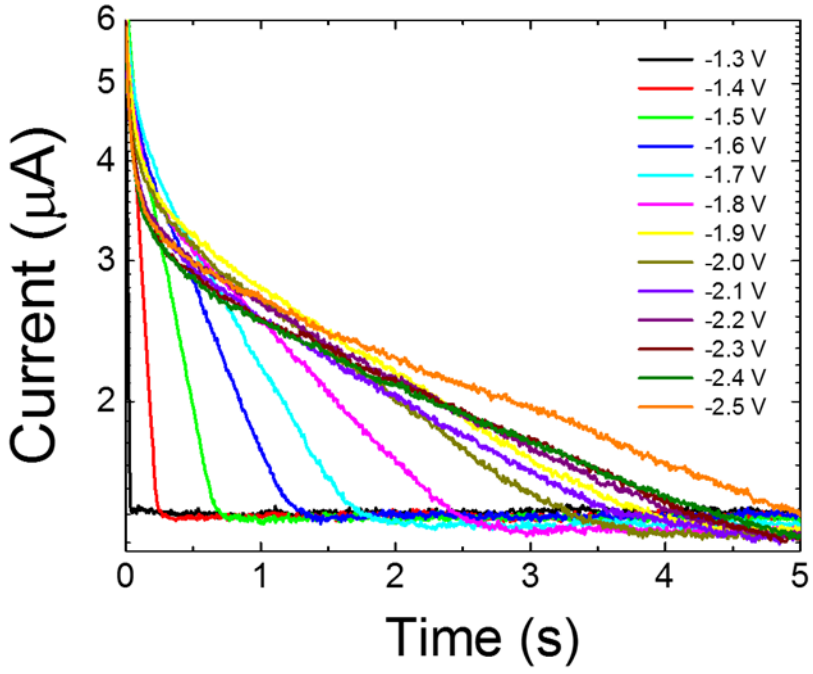



**Figure 6-13:** Discharged current from 2T memory cell at 300 K, with $V_{HOLD}$ varying from −1.3 V to −2.5 V in steps of -0.1V. It can be observed that cell dempsntrates very large retention times. Also there is some change in retention time, it is not as dramatic as seen in Figure 6-9.

## 6.6 Temperature Dependence

As seen in chapter 5, changing temperature can change the characteristics of the device substantially. This should also reflect in the memory cell performance. To test this, the temperature-dependent measurements were performed there the temperature was varied from 210 K to 330 K, and the retention time of the 2T cell was observed. As shown in

Figure 6-14 below, there is an increase in the retention time with the reduction in the temperature, and the retention time at 210 K was found to be much higher compared to 330 K. This strong dependence of retention time on temperature suggests a possible thermally active mechanism for the leakage current, supporting our hypothesis that the SRH mechanism is the primary limiting leakage mechanism at large negative gate bias values.

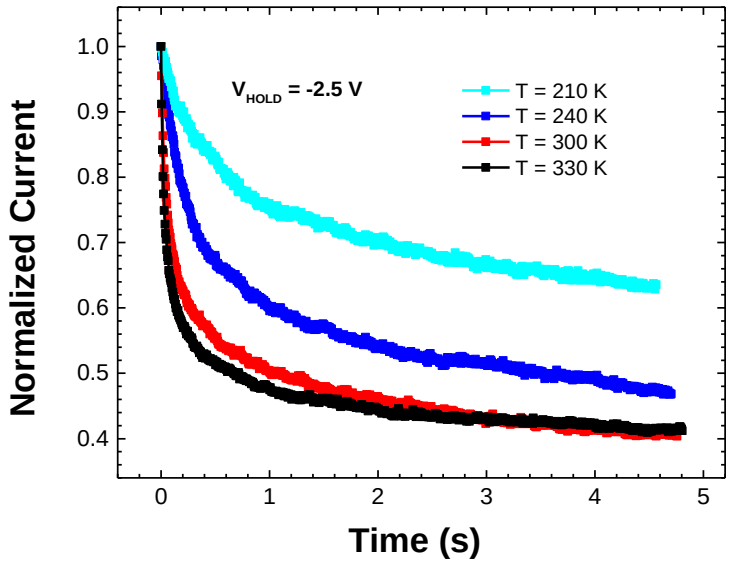



**Figure 6-14:** Normalised discharged current from 2T memory cell at varied tempereatures. It can be seen that retnetion time increases with the reduction in the temperature.

## 6.7 Estimation of Leakage Current

Memory storage time can be converted into an equivalent leakage current, as there is direct correlation of retention time and the leakage currents in the circuit. For instance, the trend in retention time of the 1T1C cell and the I-V curve of a $MoS_2$ based FET is compared (Figure 6-15), and it can be observed that the inverse retention time follows similar a

similar shaped curve vs. hold voltage. Similarly, a 2T cell based retention time can be converted into an estimated leakage current and compared to an $I_{DS}$-$V_{GS}$ of a $MoS_2$ transistor. This can be done by estimating the write transistor leakage current using: $I_{LEAK} = C_2V_2/\tau_2$, where $\tau_2$ is the retention time of the 2T cell, $C_2$ is the storage node capacitance, and $V_2$ is the write voltage. Here, $C_2$ is much lower than the corresponding capacitance for the 1T1C cell and has a value of $C_2$ = 0.051 pF. Based upon this extraction method, we determine the leakage current of the write transistor (T1) vs. $V_{HOLD}$ and these results are shown in Figure 6-16. It can be observed that the estimated current goes below the noise level of the measuring instrument ( ~ 0.1 - 1 pA range). Therefore, this technique can provide a way to estimate very low leakage currents below a typical noise floor for DC measurements. However, lower values of $V_{HOLD}$ could not be probed, due to the due to limitations of the synchronous measurement technique.

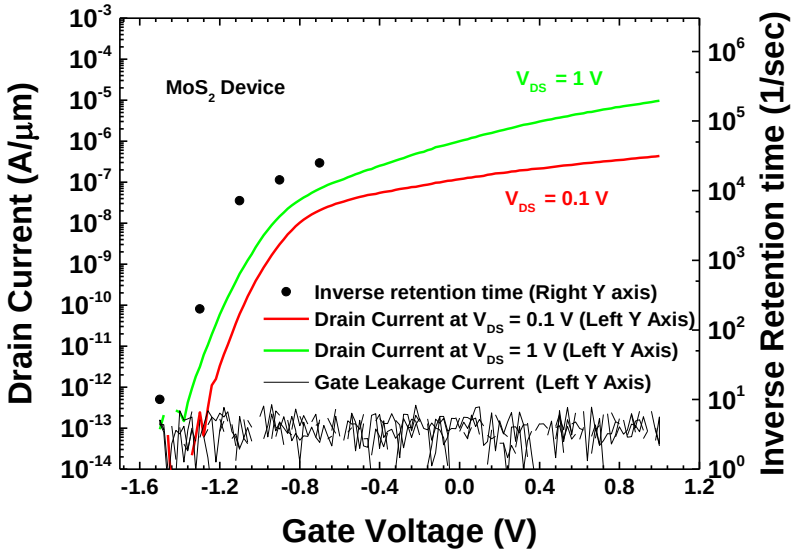



**Figure 6-15:** Comparison of retention time extracted from 1T1C memory cell and $I_{DS}$-$V_{GS}$ curves of a $MoS_2$ based transistor. The black curve below is the gate leakage noise floor.

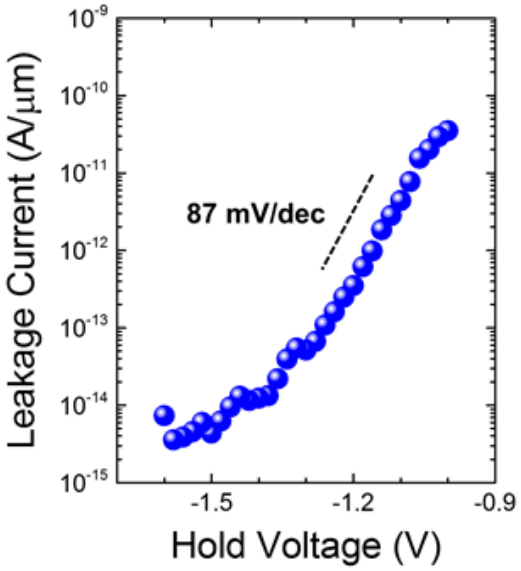



**Figure 6-16:** Estimated leakage current as a function of $V_{HOLD.}$ It can be observed that the leakage follow the typical shape of the stand-alone transfer characteristic.

Therefore, in order to determine the ultimate retention time, and extract the equivalent leakage current, the results from the quasi-DC method of measuring the 2T memory cell retention time (shown in Figure 6-13) were utilized. We once-again determined the retention time to be the time required for the current to drop by 50% of its original value at the end of the write pulse. The extracted leakage current vs. $V_{HOLD}$, using the same methodology as described previously (DC read out method) along with pulsed readout method discussed in section 6.4, is shown in Figure 6-17, where values of $V_{HOLD}$ from −1.2 V to −2.5 V were characterized. The leakage current does not continue to sharply decline for $V_{HOLD}$ < −1.8 V, and levels off to a constant value, where the average value of the leakage current between $V_{HOLD}$ = −1.8 V and −2.4 V is 1.70 $\pm$ 0.22 fA/μm

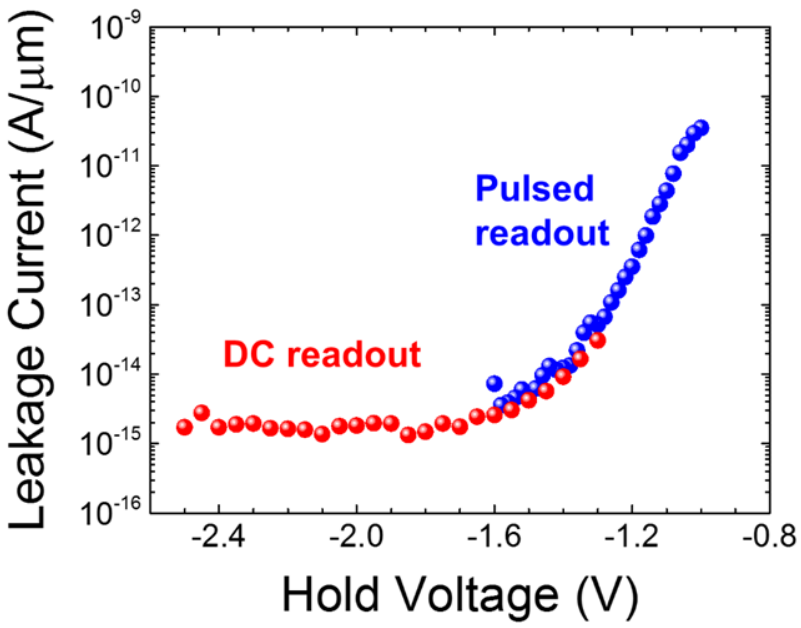



**Figure 6-17:** Estimated leakage current as a function of $V_{HOLD}$ with 50 % discharge as a criterion for retention time. Here, blue dots represents leakage currents extracted from the pulsed readout measurements, while the red dots represent DC current measurements using the Agilent B1500A.

## 6.8 Conclusions

Time dependent measurements of 1T1C and 2T cells based on $MoS_2$ based channels were performed. The retention time up to 250 ms for 1T1C cell and about 1.3 seconds for 2T cell was measured. This verifies that the properties of 2D materials such as $MoS_2$ can be utilized for applications in low power electronics to achieve improved performance. Monolayer $MoS_2$ with increased band gap could provide even better performance. Perhaps more importantly, characterization of these circuits allows exploration of current levels difficult to achieve with conventional methods. In particular, we have demonstrated the measurement of leakage currents on the order of 1-2 fA/μm with the prospect to explore

lower currents in future experiments. Furthermore, we show that the minimum leakage current is not dominated by tunneling or thermionic currents, but is likely due to SRH generation, possibly arising from defects in the $MoS_2$ or the $MoS_2$/dielectric interfaces. These results could be important for the future understanding of $MoS_2$ MOSFETs for low standby power applications.

# Chapter 7 :

# Conclusion and Outlook

## 7.1 Summary of the Work

We have seen the importance of reducing leakage and improving the power / performance trade-off of novel semiconductor devices and circuits. As consumer electronics move toward wireless and portable devices, it is going to be more vital to have energy efficient devices and circuits. We discussed various approaches that can be taken in order to reduce the power consumption. Two of the major approaches, one using tunneling field-effect transistors (TFETs), and other using two-dimensional (2D) materials were explored and examined in detail. Each approach has its own merits and disadvantages. While TFETs offer a new operating mechanism which can overcome the subthreshold slope limit of 60 mV/ decade, these devices suffer from lower on current, and a tradeoff between the on current and the subthreshold slope, particularly for p-TFETs. This is mainly because most of the n-type source material which can suffer from low density of states.

On the other hand, 2D materials such as transition metal dichalcogenides (TMDs) provide an attractive alternative to conventional silicon in some applications. Complementary circuits are possible using TMDs, and these materials have advantages of having better scalability, thin body, and better interfaces. One such material, $MoS_2$ is explored here for making memory circuits with ultra-low leakage. The performance was

predicted for highly scaled $MoS_2$ based 2T memory cell circuit based on the device model developed. Process development and optimization is performed to fabricate 1T1C and 2T memory cell based on $MoS_2$ as channel material. DC and AC characterization is performed on the memory cell. Long retention time up to 0.25 sec and 1.3 sec were observed for 1T1C and 2T memory cell. Effect of passivation and temperature is studied. Furthermore, ultra-low currents of the order of femto-ampere were predicted based on the retention time obtained using the 2T memory cells. Demonstrated operation and performance of 2T cell acts as a test vehicle towards realizing and implementing 3T gain cell based memory. This adds another missing piece of puzzle in the larger picture of logic and memory design using transition metal dichalcogenides. Furthermore, excellent performance of these embedded DRAM cell implies $MoS_2$ can be a promising material for low power application domain.

## 7.2 Outlook

TMD based circuits are still an evolving field of research, and the unique properties of such 2D materials needs to be connected with suitable applications. More work is needed in understanding material, interfaces, modeling its properties, identifying and implementing some of the circuit applications. Based on this study, some of the recommendations for future work can be listed in context of this particular material and circuit. They are as follows:

1. Real advantage of using $MoS_2$ as channel material may be clearer with using a single monolayer $MoS_2$ based channel as the material for the devices. It is

possible to grow single layer $MoS_2$ using CVD method which then can potentially be transferred onto an SOI substrate to facilitate a device and circuit fabrication flow similar to the one used in this work. Such a study will bring out the full potential of $MoS_2$ as a channel material for low power applications.

2. In embedded memory chips, memory cells are in form of arrays and with arrays comes additional considerations that can modify / degrade the cell performance. To estimate actual performance one may get out of such 2D material based memory cell, arrays of such cells need to be fabricated and tested. A similar process flow for the array can be followed, however, this may require additional circuitry to mimic the actual read out circuits and to characterize the performance at the array level.
3. Since TMDs exhibit varied properties in terms of bandgaps and band alignments, heterojunctions can be formed among the layered TMDs. Such systems can lead to various devices, such as tunneling FETs, solar cells, resonant tunneling diodes. Some of the devices (such as TFETs) are already being explored by the researchers. Although interfaces among TMDs still need to be studied in detail.
4. Due to ultra-low leakage properties of $MoS_2$, its performance may be highly influenced by the interface traps and radiation effects. Therefore it will also be useful to characterize and understand radiation induced effects on $MoS_2$ as well as other TMDs.

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