Investigation of a High-Frequency Link Single-Stage Asymmetrical Multilevel Converter for Grid Integration of Renewable Energy Systems

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Dedication

To those who held me up over the years

Abstract

Different power electronic converter topologies have been investigated to integrate renewable energy systems to the grid. Cascaded multilevel converters with a high-frequency link have emerged as a viable candidate for such applications. Electrical isolation can be provided using a compact high-frequency transformer connected in the link thus avoiding a bulky line frequency transformer. The use of cascaded modules allows the generation of a multilevel voltage having low total harmonic distortion (THD) but increases the overall system size. In this thesis, a fifteen level high-frequency AC-link single-stage asymmetrical multilevel converter for grid integration is proposed. The single-stage conversion approach eliminates the DC-link capacitors, resulting in a reduced footprint. The asymmetrical module voltages are generated by the multi-winding transformer having unequal turns on each of the secondaries. This allows the generation of fifteen output voltage levels, using only three modules in each phase. A modified uni-polar modulation strategy is proposed to generate multilevel output voltage. A modified hybrid modulation technique using triangular level shifted carriers based on the high frequency link is also investigated for this topology. Unlike previously used technique, the proposed modulation shifts the dominant harmonics in the output voltage to the sidebands of multiples of twice the switching frequency, thereby reducing the output filter size.

However, the incorporation of the switch non-idealities requires the implementation of a commutation strategy for the single-stage conversion. A detailed circuit analysis showing different modes of operation to generate a specific output voltage level, taking into account the switch non-idealites is outlined in the thesis. The analysis aids in the real-time implementation of the converter and, it also explains the distortion in the ideal output voltage profile. The analysis in general can be used for any isolated single-stage converter. The effect of switch non-idealities on the output voltage is analyzed and two compensation techniques are developed to improve the voltage profile.

A multi-winding high-frequency transformer is a critical component in the proposed converter topology. A four-winding transformer is designed and characterized using Ansys 3-D Finite Element Analysis and Network Analyzer measurements. The presence of transformer leakage inductance will require a clamp circuit to dissipate the leakage energy during commutation. A detailed circuit analysis showing the various modes of operation considering both the switch and transformer non-idealities is presented.

Comprehensive analysis is done for ensuring the generation of balanced currents in case of a module failure. A look up table is provided to operate the proposed topology for all

possible cases. The presented concepts are verified by simulation and further validated experimentally on a three-phase fifteen level converter prototype.

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Chapter 1

Introduction

1.1 Conventional interface to integrate renewables to grid

Recent efforts to reduce the dependence on fossil fuels have caused utilities worldwide to increase the integration of the power generated from renewable energy systems [1]. This interconnection of renewable systems requires the use of grid tied inverters. A conventional utility interface utilizes two level inverters in conjunction with a line frequency transformer (LFT) to generate the required voltage as shown in Fig. 1.1. Such two level inverters have high total harmonic distortion (THD) in the generated output voltage and hence require the use of large filters. Also, the presence of common mode voltages with large $\frac{dv}{dt}$ require expensive common mode chokes or design of active filters [2]. Multilevel topologies with a single DC source and several LFTs to generate multilevel three-phase output voltage with low THD and reduced filter requirements have been proposed in literature [3]. However, in all of these topologies, the usage of LFTs increases the overall footprint of the system.

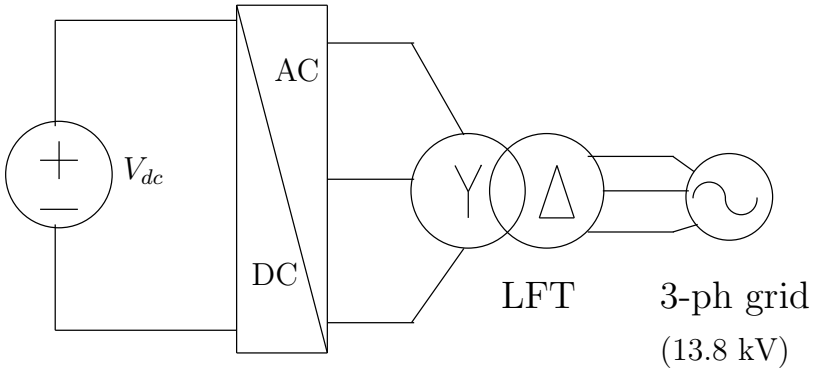


Figure 1.1: Conventional topology to interface low voltage DC to three-phase high voltage AC

1.2 Conventional interface for all electrified ships

With the advancements in variable speed drives, electrified ship propulsion systems as shown in Fig. 7.2 have become increasingly popular as they offer a compact size, increased fuel efficiency and reduced emissions in comparison to the mechanically propelled ships [4].

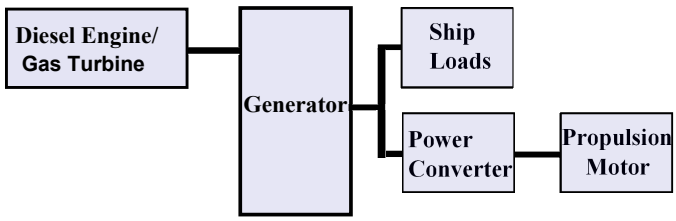


Figure 1.2: Electrified Ship Propulsion Systems.

These advantages have led to an increased interest in all electrified ships (AES) [5–9]. In an AES, the propulsion systems (power generation module, power conversion module, electric propulsion module) and ship load systems are unified to form an integrated system. With the availability of renewable energy resources and advancements in power electronics, more flexibility is available through an integrated system [9, 10]. Recently, a lot of research has been done on different ways to integrate renewables and Battery Energy Storage Systems (BESS) to the upcoming electrified ships depending on the electrical distribution system [11–15]. The electrical distribution in a ship can either be completely DC, both DC and AC (hybrid), or it could be completely AC.

In ships proposed with MVDC distribution [11], the energy storage systems are integrated to the MVDC bus using a bi-directional DC-DC converter [16, 17]. Certain ships which employ hybrid distribution systems [12] the propulsion motors are connected to the AC distribution using a two stage AC-DC-AC converter (power converter shown in Fig. 1.1) with a DC-link capacitor. In these ships, it is proposed that the energy storage systems can be integrated to the DC-link capacitor directly, thereby eliminating an additional converter [18].

In some ships with AC distribution systems [13,19], the propulsion motors (synchronous) are connected directly to the distribution system, using a single stage converter. In such systems, the power converter (shown in Fig. 1.1) is either a thyristor controlled cycloconverter [17, 20] or any other direct AC-AC converter with bi-directional switches [21, 22]. The direct AC-AC conversion eliminates the DC-link capacitor, resulting in a more compact system with reduced maintenance [20]. In such ships, the low voltage energy storage systems require a Line Frequency Transformer (LFT) to interface with the high voltage AC distribution system(6.6 kV, 13.8 kV) [6, 17, 23]. The use of LFT in such a system counters the advantage that is attained by direct AC-AC conversion [23].

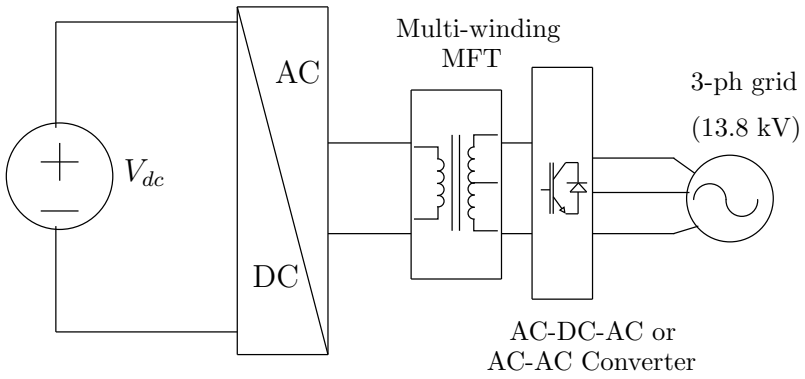


Figure 1.3: Proposed topology to interface low voltage DC to three-phase high voltage AC

1.3 Proposed interface using high-frequency transformers

At these power levels, high-frequency transformers (HFT) are envisioned to replace such LFTs [24, 25]. The use of HFTs reduces the size of magnetics but also necessitates a secondary side converter to generate line frequency AC from the high-frequency. This conversion can be accomplished either by a high-frequency AC-DC-line frequency AC, which is a two stage conversion process utilizing an electrolytic capacitor at the DC link [26–31] or a direct single-stage conversion from high-frequency AC-line frequency AC [32–38] as shown in Fig. 1.3. In case of the two stage conversion process, different topologies and modulation strategies have been investigated in the literature. In [26, 29, 30], the generated high frequency voltage across the transformer is converted to DC using a diode bridge and then phase shifted carriers are used to generate a multilevel voltage using series connected hard switched H-bridge modules. Dual active bridge topologies have been very common for isolated DC-DC conversion due to the inherent advantage of soft-switching. A review of various modulation strategies based on dual active bridge principle has been outlined in [39]. Recently, for isolated DC-DC application, instead of full bridge on two sides of the HFTs, MMCs (Modular Multilevel Converters) have also been investigated on one side [40, 41] and even on both sides [42]. Topologies have been proposed which extend the DAB principle to multi-port [43] systems, for DC-AC [27, 44] and also AC-AC applications [45], [46]. Nevertheless, the DAB topologies suffer with low efficiency when operating at non-optimal condition due to high circulating current and incomplete ZVS [39]. To overcome the limitations and hence improve the efficiency, different control techniques for operation under non-optimal conditions [47, 48] and topologies with additional switching stages have been proposed in literature [49]. In any case, to interface with high voltage line frequency AC, a number of converter modules, each connected to an isolated secondary winding are cascaded in series similar to the multilevel structure [26,27,32]. But such a system will require a large

number of isolated secondaries and converter modules if lower voltage rating devices are used. With the advancement of high voltage switches, [28] the number of converter modules and the transformer secondaries can be reduced [50]. However, the absence of several series connected modules, increases the THD and will either require large filters or the design of more complex filters like LCL [51] or LLCL [52].

Asymmetrical multilevel inverters allow to achieve, higher number of levels in the output voltage with less number of converter modules. Asymmetrical converters can be broadly classified according to the source of asymmetry. In literature, topologies have been investigated in which the asymmetry is introduced in the DC voltage source [53–57]. Several unequal voltage sources have to be used to provide the required asymmetric input voltage. Recently, topologies have been proposed which have extended the asymmetric voltage configuration to modular multilevel converters [58]. Another scheme of generating asymmetric voltages is by using a single DC voltage source with a multi-winding transformer with unequal turns on each secondary. The asymmetry introduced in the LFT turns ratio have been previously presented [59,60]. However, as explained earlier, use of LFT increases the system size. Topologies with the asymmetry introduced in the high-frequency transformer turns ratio have been presented for drives [61]; traction [62] and for grid-tied applications [31,63–65]. In such two stage topologies, a high voltage DC input is still required for the main converter and the high-frequency transformer is used for auxillary converters [61, 62]. But as stated, the two stage conversion requires a DC-link capacitor. An asymmetrical multilevel converter topology having nine secondary windings has been proposed, but the results do not incorporate switch non-idealities and its effect on the output voltage profile [63].

In this thesis, a multilevel converter topology to interface a low voltage DC to a three-phase high voltage grid with three multi-winding HFTs is presented. The asymmetry is introduced in the HFT turns ratio (the three transformer secondary windings in each phase have an unequal turns ratio of 1:2:4). Such an asymmetry results in higher number of levels in the output voltage with only three series connected modules per phase. The single-stage conversion approach requires AC-AC converter modules. The proposed topology has the following benefits: (i) eliminates the bulky LFT; (ii) allows bi-directional power flow; (iii) generates fifteen output voltage levels, using only three AC-AC converter modules in each phase; and (iv) removes the need for a dc link capacitor, resulting in a reduced footprint. This converter can be used to integrate the energy storage system to HV AC distribution system as shown in Fig. 1.4.

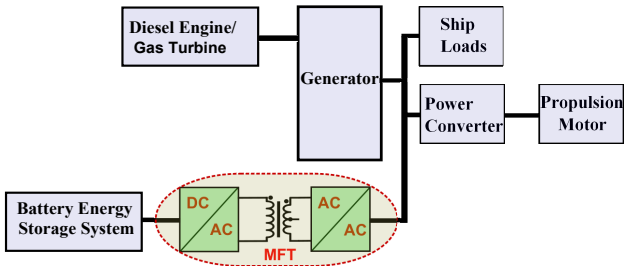


Figure 1.4: High-frequency transformer isolated single stage topology to interface BESS to electrified ships.

1.4 Modulation and commutation strategies

Different modulation strategies have been investigated in the literature for cascaded H-bridge systems [66,67]. Phase shifted carriers are used to generate signals in high frequency link isolated single/two stage cascaded H-bridge systems to interface energy storage systems to the three-phase grid [26,27,68]. Primarily, two modulation techniques exists in the literature for asymmetrical cascaded H-bridge converter. These converters as mentioned above utilize the LFT turns ratio for generating the asymmetry and require a diode-bridge and a DC-link capacitor at the input of the H-bridge. Conventional hybrid modulation technique [69] and Uni-polar modulation technique [70]/hybrid frequency carrier based PWM [71] are the two techniques. The conventional hybrid modulation technique [69] allows to generate a multilevel output voltage with the dominant voltage harmonics at the sidebands of multiples of twice the switching frequency. However, the technique causes a rise of the DC-link capacitor voltage because of the negative DC-link current and requires a controlled rectifier at the input. The implementation of the uni-polar modulation rather than the conventional hybrid modulation technique in such a converter allows to get rid of the above disadvantages [70].

The single stage converter under study consists of AC-AC converter modules formed using bi-directional switches. The presence of bi-directional switches requires either a commutation strategy or a free-wheeling commutation path during each switching transition. As shown in the literature, the incorporation of a commutation strategy minimizes the losses in comparison to the freewheeling circuit [72]. Several strategies like the current based [73], voltage based [74] and hybrid [75] commutation have been investigated in the literature which can be classified as under:

- Current Based Commutation [73] strategy based on the output current sensing performs the commutation in four steps.
- Voltage Based Commutation [74] strategy based on input AC voltage sensing allows

the commutation in two steps.

- Hybrid Commutation [75] strategy requires both input AC voltage and output current sensing. It allows to reduce the commutation delay time because of single step commutation.

A detailed comparison of different current and voltage commutation strategies on the basis of efficiency and hardware requirement [76] show the superiority of four-step commutation strategy over other described strategies. However, the incorporation of four-step commutation algorithm can cause glitches in the voltage as shown in the literature [77, 78]. In literature, commutation strategies have been implemented to incorporate the non-idealities of the bi-directional switch in a single stage isolated two-level [79] and multi-level converter [80]. However, the non-ideal behavior of the switches of both the input H-bridge and the output single stage converter and the resulting effect on the output voltage profile has not been reported [32, 64, 79, 80].

A detailed description of various modes of circuit operation for a particular switching transition, highlighting the cause and effect of the glitch is demonstrated. The thesis proposes two compensation techniques to improve the output voltage profile, by modifying the commutation algorithm to negate the glitches in the output voltage. The switching of AC-AC converter module will result in square currents through the transformer winding [81] with a low frequency sinusoidal envelope. The presence of the transformer leakage inductance and square link currents require a clamp circuit in parallel to the transformer windings to avoid any over-voltage. However, the HFTs can be designed to achieve low leakage inductance [82–84]. The thesis also shows a winding design and characterization of a multi-winding transformer to achieve low leakage inductance.

The modified version of the uni-polar pulse width modulation technique is investigated for the single stage converter in [63]. However, the adoption of both the uni-polar modulation technique [71] and its modified version [64] to the subsequent converter topologies, result in voltage harmonics at the sidebands of the multiples of the switching frequency.

The single stage converter topology introduced in this thesis does not have an electrolytic capacitor at the DC-link. The absence of such a DC-link capacitor allows to investigate the hybrid modulation technique which has the aforementioned advantage. The hybrid modulation technique is modified based on the high-frequency link. The thesis investigates this modified modulation technique on a single stage isolated asymmetrical converter. Unlike previously used techniques, the proposed modulation shifts the dominant harmonics in the output voltage to the sidebands of multiples of twice the switching frequency, thereby reducing the output filter size. The thesis presents a detailed description for the generation of the ideal switch signals using the reference and carrier signals and also provides a qualitative

analysis to explain the harmonic spectrum of the output voltage.

The incorporation of the switch non-idealities requires the implementation of a commutation strategy. The thesis demonstrates the effect of the non-idealistic nature of the switch on the output voltage profile with a step-by-step modification in the switching signals as shown in the later sections. A detailed circuit description including the switch non-idealities to explain a particular switching transition is presented. The analysis explains the distortions in the output voltage as a result of switch non-idealities in comparison to the ideal output voltage. The analysis in general can be used for any isolated single stage converter and will also aid in the real-time implementation of the converter.

- Chapter 1 gives an introduction.
- Chapter 2 briefly presents the proposed circuit topology and the circuit description.
- In Chapter 3 the two investigated ideal modulations are presented along with a comparison based on output voltage THD and the harmonics.
- Chapter 4 explains the effect of switch non-idealities on the output voltage profile. Two glitch compensation techniques have been described in detail to improve the output voltage profile.
- In Chapter 5 a high-frequency four winding transformer design is detailed. Comprehensive analysis has been done to determine the transformer leakage inductances using 3-D Finite Element Analysis and using Network Analyzer.
- Chapter 6 demonstrates the operation of the proposed converter in case of a module failure. Also, a filter design comparison is outlined for the two different modulations.
- Chapter 7 shows the hardware setup and the detailed simulation and experimental results to validate the proposed concepts.
- Chapter 8 outlines two different circuit variations derived from the proposed topology and the basic simulation results.
- Chapter 9 gives the conclusion and the future work.

Chapter 2

High-Frequency Link Single-Stage Converter

2.1 Multilevel converter with high-frequency transformer (HFT) isolation

2.1.1 Circuit configuration

As shown in Fig. 2.1, in order to interface low voltage renewables having nominal dc voltage, V_{in} with a high voltage three-phase grid, full-bridge modules on the primary side of multi-winding HFTs of all three-phases are connected in parallel and on the secondary side AC-AC converter modules of each phase are connected in series. The number of AC-AC converter modules (N_m) required in each phase to interface with a three-phase grid, can be computed using (8.1). The voltage on the secondary side of the multi-winding transformer is $n_{si}V_{in}$, where, $n_{si} : i \, \epsilon \, \{1, 2...N_m\}$ is the turns ratio of each isolated secondary winding to primary winding. N_m depends on v_{ll}, the rms line-line voltage of the three-phase grid and nV_{in}, the voltage across the secondary winding of the HFT. Considering, close to 50% de-rating of the switches, v_r the rating of the IGBTs that will be used to design the AC-AC converter module is given by (8.3). N_m, series connected modules in each phase will result in a phase-neutral output voltage having n_l number of levels as given by (2.3). Each AC-AC converter module consists of eight IGBTs, and hence, the total number of IGBTs in each phase is N_{sw} and can be computed using (2.4).

$$N_m = \frac{\sqrt{2}v_{ll}}{\sqrt{3}nV_{in}} \tag{2.1}$$

$$v_r = \frac{nV_{in}}{0.5} \tag{2.2}$$

$$n_l = 2N_m + 1 \tag{2.3}$$

$$N_{sw} = 8N_m \tag{2.4}$$

Typically, in a cascaded system, all the converter modules are symmetrical. Suppose, Fig. 2.1 is considered to be a symmetrical converter topology, then all the transformer secondary windings, $n_{s1} = n_{s2} = ...n_{sN_m} = n$ will have identical turns ratio. Also, the IGBTs in all the series connected AC-AC converter modules will have the same voltage rating. However, it is also possible to design the multi-winding transformer such that all the isolated secondary windings have unequal turns ratio; $n_{s1} \neq n_{s2} \neq ...n_{sN_m}$. This will result in higher number of output voltage levels with less number of converter modules. However, each of the AC-AC converter module needs to have IGBTs rated at different voltages.

2.1.2 Evaluation of circuit configuration based on system complexity

Table 2.1 shows a comparison of the number of IGBTs and transformer secondary windings required to realize the grid voltage based on the voltage rating of the IGBT. The number of AC-AC converter modules to be connected in series, the number of output voltage levels and the total number of IGBTs in each phase are calculated using (8.1), (2.3) and (2.4) respectively and shown in Table 2.1. In Table 2.1, *a* refers to the case in which the grid voltage is realized using 6.5 kV IGBTs. This results in only five levels in the output voltage resulting in a high output voltage THD. As shown in case *b* and *c*, with the symmetrical modules, the number of output voltage levels can be increased by selecting lower voltage rating IGBTs. However, this will increase the number of IGBTs and the transformer secondary windings as shown in Table 2.1. Table 2.1 case *d*, is of the proposed asymmetrical converter topology in which the turns ratio of the secondary windings are asymmetrical. Several configurations of single-stage symmetrical and asymmetrical multilevel converters (7- S: 7-level symmetrical converter; 7- AS: 7- level asymmetrical converter and so on) have been compared based on system complexity as shown in Table 2.2. The number of switches along with the associated isolated gate-drivers and digital signals, the number of isolated secondary windings, the number of arithmetic and logical operations to generate the ideal switch signals and the resulting THD of a three-phase system have been summarized in Table 2.2. Based on the data, a normalized index is computed using [26] and shown in Table

2.3. As seen from Table 2.2, in comparison to 15- AS configuration only 7-S and 7-AS configurations have lower control complexity. However, the THD of a seven level converter is much higher. The normalized index in Table 2.3, shows that the control complexity (based on ALOs) in particular in asymmetrical fifteen level configuration though not the minimum, but in terms of normalized index and overall system performance is superior compared to other configurations.

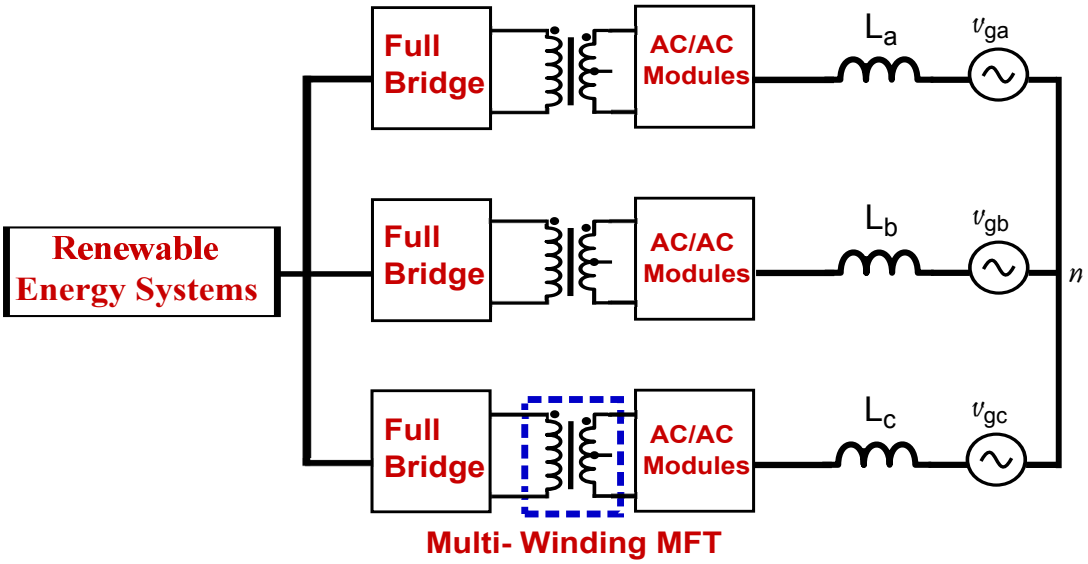


Figure 2.1: Block diagram of proposed topology.

Table 2.1: Switch count for 500 kW/7.2 kV interface

Case	Output Voltage	Switch Rating	Isolated Secondary	N_{sw}
a.	5	6.5 kV	2	16
b.	9	3.5 kV	4	32
c.	15	1.7 kV	7	56
d.	15	6.5 kV	1	8
		3.5 kV	1	8
		1.7 kV	1	8

Table 2.2: System Complexity

Levels	Switches	THD	ALO	Sec. Windings
7- S	84	19.61	114	3
7- AS	60	19.61	90	2
9- S	108	14.81	150	4
11- S	132	12.02	186	5
15- S	180	8.62	258	7
15- AS	84	8.62	150	3
17- S	204	7.59	294	8
27- AS	108	4.66	210	4

Table 2.3: Normalized index value

Levels	Switches	THD	ALO	Sec. Windings	Total
7- S	0.17	1	0.12	0.17	1.46
7- AS	0	1	0	0	1
9- S	0.33	0.68	0.29	0.33	1.63
11- S	0.5	0.49	0.47	0.5	1.96
15- S	0.83	0.26	0.82	0.83	2.74
15- AS	0.17	0.26	0.29	0.17	0.89
17- S	1	0.2	1	1	3.2
27- AS	0.33	0	0.59	0.33	1.25

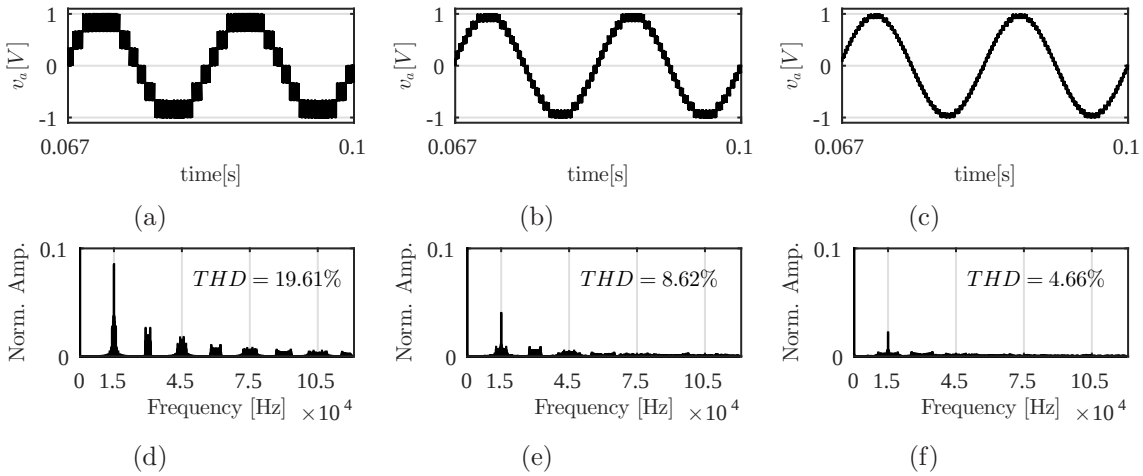


Figure 2.2: Ideal output voltage: (a) seven level;(b) fifteen level; (c)twenty seven level; Harmonic spectrum of ideal output voltage: (d) seven level;(e) fifteen level; (f)twenty seven level

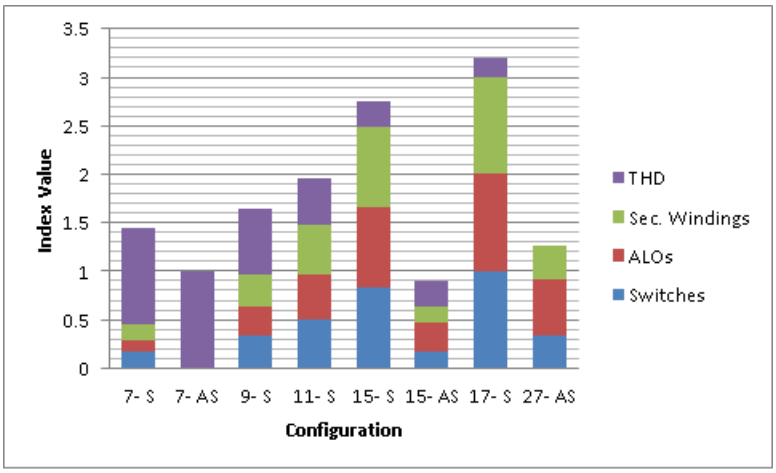


Figure 2.3: Comparison of different configurations based on normalized index parameters for: control complexity, number of switches, transformer secondary windings and THD

2.1.3 Description of the circuit configuration

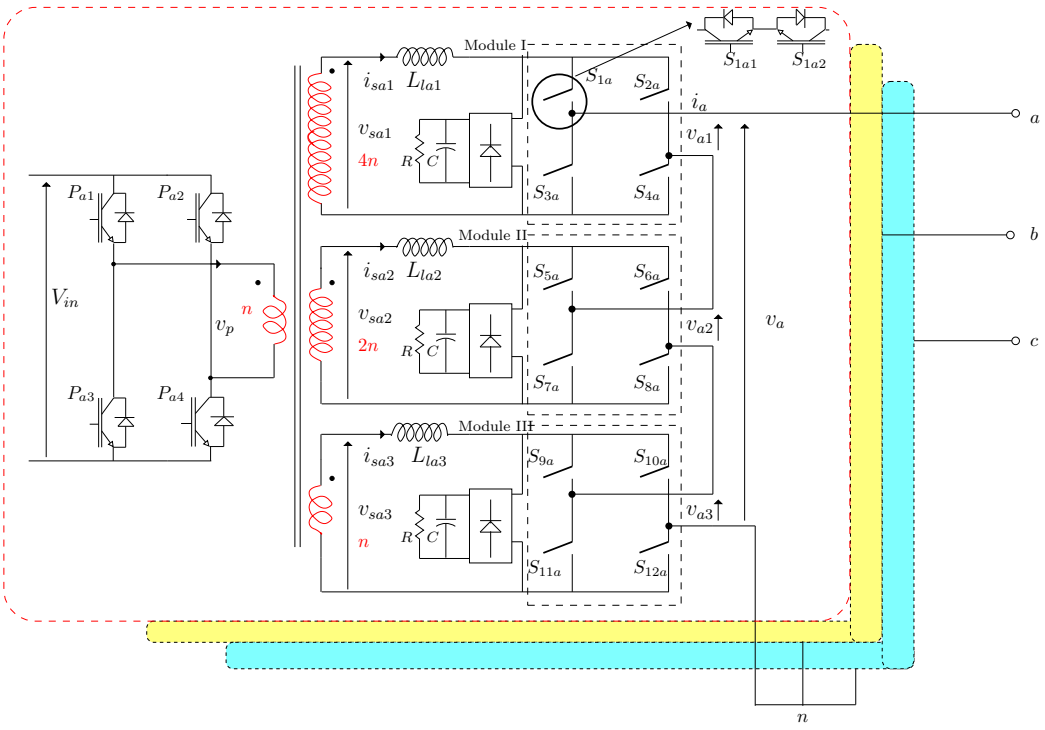


Figure 2.4: Detailed per-phase circuit diagram of isolated asymmetrical multilevel converter topology.

Fig. 2.4 shows the per phase circuit configuration of the proposed converter topology. In each phase $i : a, b, c$, the full-bridge module consists of switches P_{i1}-P_{i4}. The output of the full-bridge is connected to the primary winding of a HFT having three secondary

windings with an asymmetrical turns ratio of n:$2n$:$4n$ as shown in Fig. 2.4 (highlighted in red). Such an asymmetry, results in fifteen levels in the output voltage, same as in Table 2.1 case c, but with only three series connected AC-AC converter modules and three transformer secondaries per phase. Each AC-AC converter module is connected to an isolated transformer secondary winding. As shown in Table 2.1, case d and Fig. 2.4, the AC-AC converter Module I should have IGBTs rated at 6.5 kV, whereas Module II should have IGBTs rated at 3.5 kV and Module III at 1.7 kV. Each module consists of four bi-directional switches S_{1a}-S_{4a}. The bi-directional switch, S_{1a} can be realized by connecting two anti-parallel IGBTs (S_{1a1} and S_{1a2}) in a common emitter configuration as shown in Fig. 2.4. In each phase, all the AC-AC converter modules are connected in series on the output side. The module output voltage of Modules I, II and III are v_{a1}, v_{a2} and v_{a3} respectively. The net phase-neutral output voltage of the three series connected modules is v_a. The square currents through the leakage inductance of the transformer due to the switching of AC-AC converter module requires a clamp circuit. The circuit comprises of a diode full-bridge connected in parallel to the transformer windings to avoid any over-voltage.

Chapter 3

Ideal Modulation

3.1 Modulation-I: Modified Unipolar Modulation

3.1.1 Modulation of primary side full-bridge converter

The primary side full-bridge consists of four unidirectional switches $P_{a1} - P_{a4}$. In each leg, the two switches are regulated in a complementary manner to avoid the short-circuit of input dc voltage. The switches are regulated at 50% to generate a square voltage across the transformer primary winding. Switches P_{a1} and P_{a4} are controlled by signal, p_1 and the other two switches are controlled by signal p_2. The switching strategy leads to a generation of $+V_{in}$ (when signal p_1 is high) and $-V_{in}$ (when signal p_2 is high) voltage at the transformer primary winding terminal (v_p). Hence, the voltages across the three isolated secondary windings will be as given in (3.1), (3.2) and (3.3) respectively.

$$v_{sa1} = \pm 4nV_{in} \tag{3.1}$$

$$v_{sa2} = \pm 2nV_{in} \tag{3.2}$$

$$v_{sa3} = \pm nV_{in} \tag{3.3}$$

3.1.2 Modulation of secondary side AC-AC converter modules

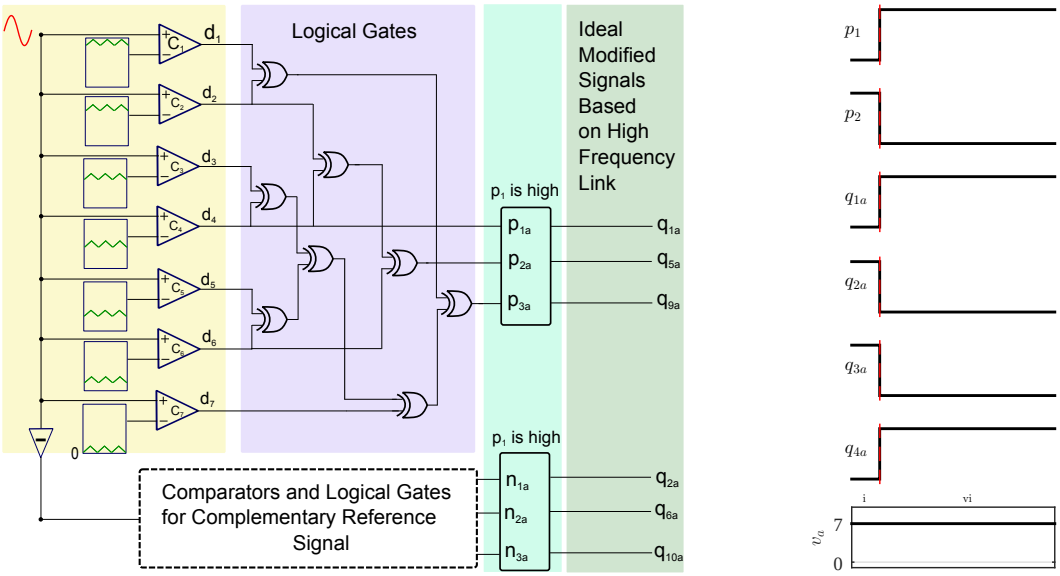
The three AC-AC converter modules connected to each of the three isolated secondary windings, have to be controlled, so as to generate the multilevel phase-neutral output voltage from the link voltage that is present across the terminals of each secondary winding. The ideal modulation strategy for the proposed converter topology for phase, a is explained. Same modulation strategy will apply for phase, b and c. Fig. 3.1a shows the implementation

circuit for the generation of the ideal signals of the switches of the AC-AC converter module. Two complementary sinusoidal references are compared with seven level shifted carriers to obtain seven digital signals, d_1 - d_7, as in a uni-polar modulation [71]. The carrier waveform used to generate the ideal digital signals, is at the link frequency. As shown in Fig. 3.1a, three ideal signals, p_{1a} - p_{3a} are generated from the logical operation of seven digital signals. Similarly, from the digital signals obtained by comparing the complementary sinusoidal reference with the level shifted carriers as shown in Fig. 3.1a, three more signals $n_{1a} - n_{3a}$ can be generated. In order to generate positive module output voltages, when the link voltage, v_{pa} is positive (that is, when signal p_1 is high), p_{1a}, p_{2a} and p_{3a} are q_{1a}, q_{5a} and q_{9a} signals respectively and n_{1a}, n_{2a} and n_{3a} are q_{2a}, q_{6a} and q_{10a} signals respectively as shown in Fig. 3.1a. When the link voltage turns negative (that is, when signal p_1 is low), the signals are interchanged to generate the required output voltage. The modulation is similar to the uni-polar modulation technique [71] except that the signals are modified based on the high-frequency link polarity. The modified signals are then given to the switches in the three AC-AC converter modules in each phase.

$$p_{1a} = d_4 \tag{3.4}$$

$$p_{2a} = d_2 \oplus d_4 \oplus d_6 \tag{3.5}$$

$$p_{3a} = d_1 \oplus d_3 \oplus d_5 \oplus d_7 \oplus p_{2a} \tag{3.6}$$



(a) (b)

Figure 3.1: (a) Generation of ideal modified signals;(b) Switching signals of primary side full-bridge and AC-AC converter Module I followed by the phase-neutral output voltage, v_a: Ideal signals without four-step commutation of secondary side bi-directional switches and no dead time of primary side switches.

3.1.3 Generation of specific output voltage level

Module I, v_{a1}	Module II, v_{a2}	Module III, v_{a3}	Output Voltage, v_a
$4nV_{in}$	$2nV_{in}$	$nV_{in} \leftrightarrow 0$	$7nV_{in} \leftrightarrow 6nV_{in}$
$4nV_{in}$	$2nV_{in} \leftrightarrow 0$	$0 \leftrightarrow nV_{in}$	$6nV_{in} \leftrightarrow 5nV_{in}$
$4nV_{in}$	0	$nV_{in} \leftrightarrow 0$	$5nV_{in} \leftrightarrow 4nV_{in}$
$4nV_{in} \leftrightarrow 0$	$0 \leftrightarrow 2nV_{in}$	$0 \leftrightarrow nV_{in}$	$4nV_{in} \leftrightarrow 3nV_{in}$
0	$2nV_{in}$	$nV_{in} \leftrightarrow 0$	$3nV_{in} \leftrightarrow 2nV_{in}$
0	$2nV_{in} \leftrightarrow 0$	$0 \leftrightarrow nV_{in}$	$2nV_{in} \leftrightarrow nV_{in}$
0	0	$nV_{in} \leftrightarrow 0$	$nV_{in} \leftrightarrow 0$

Table 3.1: Module and total phase-to-neutral output voltages

Table 8.1 shows the output voltage across each of the three AC-AC converter module to generate seven positive levels in the phase-neutral output voltage. As shown in Table 8.1, for a particular output voltage level generation, if the module output voltage is constant then it will switch only when the the link voltage switches otherwise it will switch even

though the link voltage is constant. Fig. 3.2 shows the output voltage across Modules I, II and III followed by the total phase-neutral voltage, v_a depicting the fifteen levels, with three AC-AC converter modules in each phase. To illustrate with an example for phase a, consider the generation of the output voltage $7nV_{in} \leftrightarrow 6nV_{in}$. Fig. 3.1b shows the switching signals of the primary side full-bridge switches followed by the ideal signals of the bi-directional switches in Module I. The signals q_{1a}-q_{4a} correspond to bi-directional switches S_{1a}-S_{4a} respectively. In case of ideal switches, both uni-directional switches S_{1a1} and S_{1a2} forming a bi-directional switch, S_{1a} can be controlled using one signal, q_{1a}. As shown in Table 8.1, irrespective of the link voltage being positive or negative, Modules I and II have to generate a constant voltage of $4nV_{in}$ and $2nV_{in}$ respectively and Module III has to generate a voltage that is pulsating between nV_{in} and zero. The left leg switches of the AC-AC converter module are controlled by p_1 signal whereas, the right leg switches are controlled by p_2. This implies that as shown in Fig. 3.1b, when the link voltage switches from negative (signal p_2 is high) to positive (signal p_1 is high), the bi-directional switches that are conducting, transition from (S_{2a} and S_{3a}) in Module I; and (S_{6a} and S_{7a}) in Module II to (S_{1a} and S_{4a}) in Module I; and (S_{5a} and S_{8a}) in Module II to maintain a constant module output voltage of $4nV_{in}$ and $2nV_{in}$ respectively. Switching in Module III will be similar to obtain nV_{in}. But Module III also generates a zero voltage across the output terminals as shown in Table 8.1. For this, both the bottom bi-directional switches will be ON to provide a path for the output current to free-wheel, irrespective of the link voltage being positive or negative. In a similar manner, the switches are controlled to achieve other voltage levels.

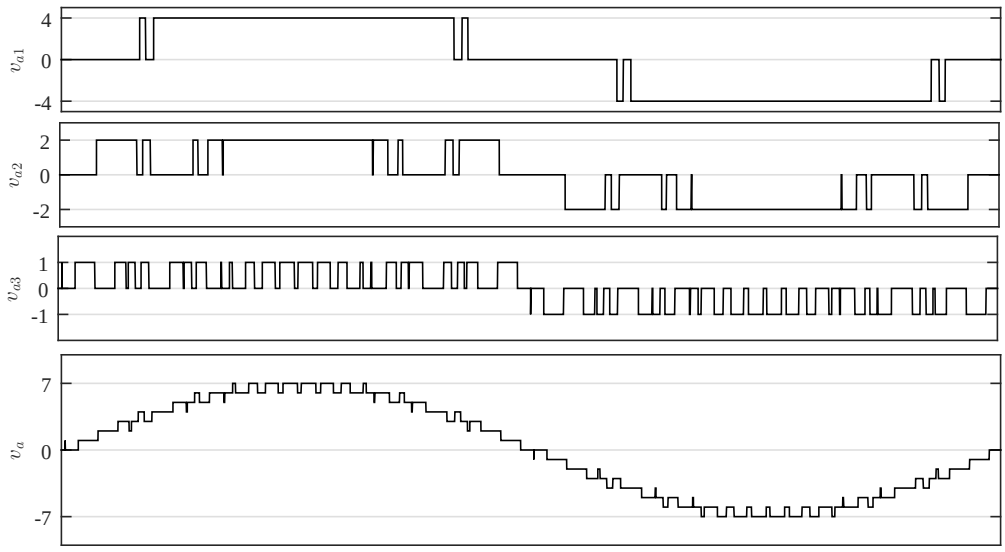


Figure 3.2: Voltage waveforms for case 3.1b for 1 pu V_{in} and n= 1

3.2 Modulation-II: Modified Hybrid Modulation

3.2.1 Modulation of primary side converter

The ideal modulation technique for phase, a is described in this section. Same applies for phase, b and c. In the primary side H-bridge, each diagonal pair of switches is regulated in a complementary manner at 50 % duty ratio. Diagonal pair of switches P_{a1} and P_{a4} is controlled by signal p_1 and the other diagonal pair of switches is controlled by p_2 resulting in a following link voltage, v_{pa} across the transformer primary winding:

$$v_{pa} = \begin{cases} +V_{in} & p_1 = 1, p_2 = 0 \\ -V_{in} & p_1 = 0, p_2 = 1 \end{cases} \tag{3.7}$$

$$m_a = \frac{\hat{V}_{a,1}}{7nV_{in}} \tag{3.8}$$

where, $\hat{V}_{a,1}$ is the peak value of the fundamental output voltage.

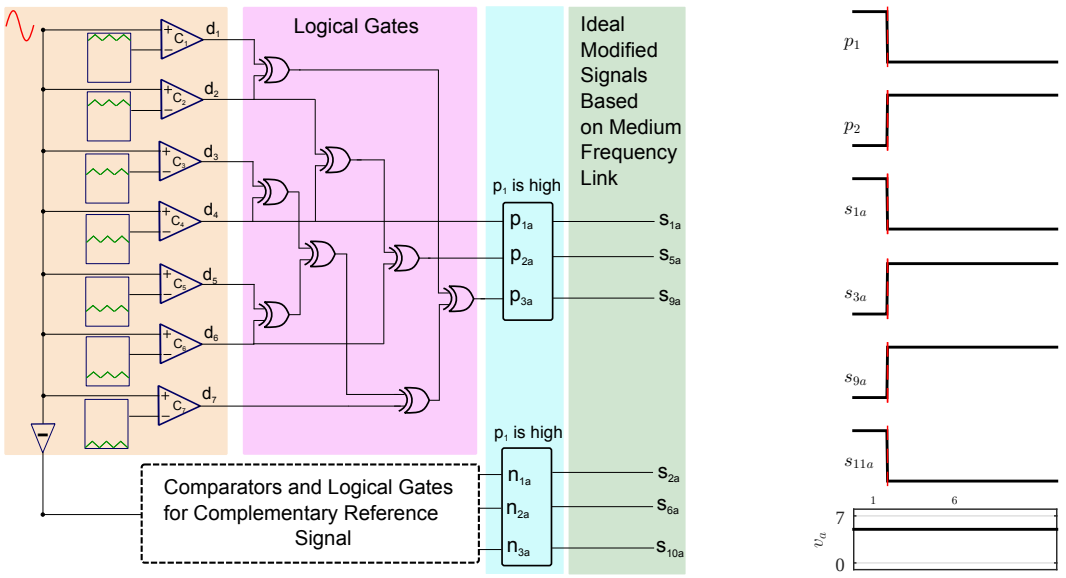
3.2.2 Signal generation for switches of secondary side modules

The voltages across the three isolated secondary windings, v_{sa1}, v_{sa2} and v_{sa3} will be $4n$ v_{pa}, $2n$ v_{pa} and n v_{pa} respectively. The three AC-AC converter modules connected to each of

the three isolated secondary windings, are modulated, so as to generate a multilevel phase-to-neutral output voltage. The modulation index, m_a is given in (7.2). Table 3.2 shows the output voltage across each of the three AC-AC converter modules to generate a multilevel output voltage. For simplicity, the switches of the AC-AC converter modules are considered to be ideal. Similar to the primary side H-bridge modulation, two bi-directional switches of each leg are controlled in a complementary fashion to avoid shorting of the transformer secondary winding.

Table 3.2: Modulation Technique for Different Positive Levels in Phase-to-Neutral Output Voltage

Module I	Module II	Module III	Output Voltage
$4nV_{in}$	$2nV_{in}$	$nV_{in} \leftrightarrow 0$	$7nV_{in} \leftrightarrow 6nV_{in}$
$4nV_{in}$	$2nV_{in}$	$0 \leftrightarrow -nV_{in}$	$6nV_{in} \leftrightarrow 5nV_{in}$
$4nV_{in}$	$2nV_{in} \leftrightarrow 0$	$-nV_{in} \leftrightarrow 0$	$5nV_{in} \leftrightarrow 4nV_{in}$
$4nV_{in}$	$0 \leftrightarrow -2nV_{in}$	$0 \leftrightarrow nV_{in}$	$4nV_{in} \leftrightarrow 3nV_{in}$
$4nV_{in}$	$-2nV_{in}$	$nV_{in} \leftrightarrow 0$	$3nV_{in} \leftrightarrow 2nV_{in}$
$4nV_{in}$	$-2nV_{in}$	$0 \leftrightarrow -nV_{in}$	$2nV_{in} \leftrightarrow nV_{in}$
$4nV_{in} \leftrightarrow 0$	$-2nV_{in} \leftrightarrow 0$	$-nV_{in} \leftrightarrow 0$	$nV_{in} \leftrightarrow 0$



(a) (b)

Figure 3.3: (a) Generation of ideal modified signals;(b) Switching signals of primary side full-bridge and AC-AC converter Module I followed by the phase-neutral output voltage, v_a: Ideal signals without four-step commutation of secondary side bi-directional switches and no dead time of primary side switches.

Hence, ideally each leg of the AC-AC converter module can be controlled with one switching signal. Signals s_{1a} and s_{2a} are for the top bi-directional switch in left and right leg respectively of Module I (shown in Fig. 2.1). Similarly, s_{5a} and s_{6a} are signals for the switches of Module II and s_{9a} and s_{10} of Module III. The ideal switch signals are generated using seven level shifted carriers and two complementary sinusoidal reference signals as shown in Fig. 3.4a. In order to generate seven positive levels in the output voltage these carriers are compared with a sinusoidal reference as shown in Fig. 3.3a; such that whenever the sinusoidal reference is greater than the carrier the logic is 1, otherwise 0. As shown in Fig. 3.3a, three ideal signals, p_{1a} - p_{3a} are generated from the logical operation of seven digital signals as under:

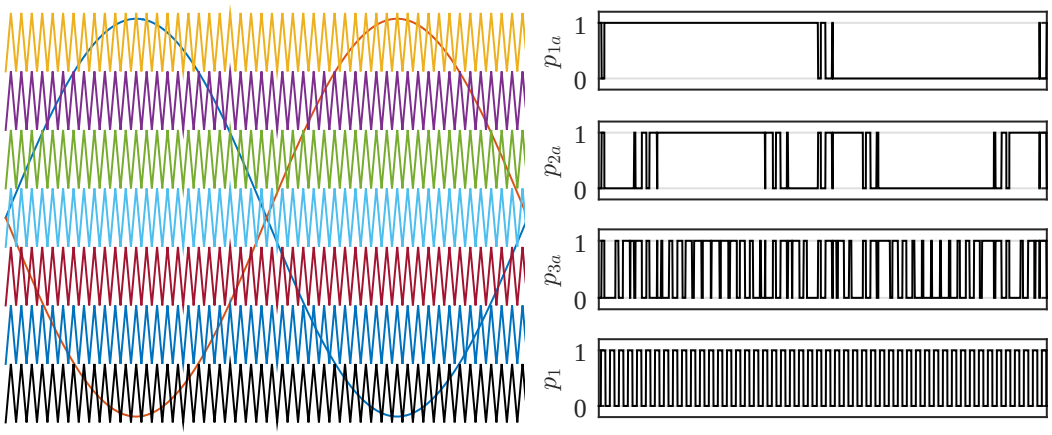


Figure 3.4: (a) Seven carrier signals and two complementary references to generate fourteen digital signals.(b) Three ideal signals derived from seven digital signals to generate fifteen levels using three modules.

These three signals are shown in Fig. 3.4b. Similarly, as shown in Fig. 3.3a, three more signals $n_{1a} - n_{3a}$ can be generated from seven other digital signals obtained by comparing the complementary sinusoidal reference with the level shifted carriers. In order to generate positive module output voltages, when the link voltage, v_{pa} is positive (that is, when signal p_1 is high), p_{1a}, p_{2a} and p_{3a} are s_{1a}, s_{5a} and s_{9a} signals respectively and n_{1a}, n_{2a} and n_{3a} are s_{2a}, s_{6a} and s_{10a} signals respectively as shown in Fig. 3.3a. When the link voltage turns negative (that is, when signal p_1 is low), the signals are interchanged to generate the required output voltage. It is to be noted that, if according to Table 3.2, the module has to generate a constant voltage for a specific output voltage level, v_a, it will switch only when the link voltage changes polarity. However, if the module has to generate a pulsating voltage (signal p_{3a}), then as shown in Fig. 3.4b it will switch even though the link voltage is constant.

3.2.3 Generation of specific output voltage level

To illustrate with an example for phase a, consider the generation of the output voltage $6nV_{in} \leftrightarrow 5nV_{in}$. As shown in Table 3.2, irrespective of the link voltage polarity, Modules I and II have to generate a constant voltage of $4nV_{in}$ and $2nV_{in}$ respectively, and Module III has to generate a voltage that is pulsating between 0 and $-nV_{in}$. Fig. 3.3b shows the ideal switching signals of the primary side H-bridge switches, p_1 and p_2 followed by the signals of the two bi-directional switches in the left leg: (s_{1a} and s_{3a}) of Module I and (s_{9a} and s_{11a}) of Module III in order to generate v_a=$5nV_{in}$. Fig. 4.13 shows a detailed circuit diagram highlighting different modes of operation in order to maintain an output voltage of $5nV_{in}$ even though the link voltage changes from $+V_{in}$ to $-V_{in}$. As modules I and II switch

only when the input H-bridge converter changes state, the signals (s_{1a} and s_{5a}) of the left leg top bi-directional switch and signals (s_{2a} and s_{6a}) of the right leg top bi-directional switch of both modules follow signals p_1 and p_2 respectively. Mode 1 of Fig. 3.3b shows that signal p_1 is high, corresponding to a link voltage, v_{pa}=$+V_{in}$ as explained earlier. Mode 1 of Fig. 4.13a shows the corresponding bi-directional switch set in both modules that are ON resulting in module output voltages of $4nV_{in}$ and $2nV_{in}$ respectively. As Module III needs to generate a voltage of $-nV_{in}$, the switching signals will be complimentary as shown in Fig. 3.3b. Similarly, as shown in Fig. 4.12a, when the signal p_2 is high, the corresponding bi-directional switch set in all three modules are ON, such that the phase-to-neutral output voltage is still $5nV_{in}$. In order to generate $6nV_{in}$, Module III has to generate a zero voltage. Whenever a zero voltage is to be generated, two bi-directional switches of both legs in Module III: S_{11a} and S_{12a} are ON to provide a free-wheeling path to the current irrespective of the link voltage being positive or negative. In a similar manner, the switches are controlled to achieve other levels.

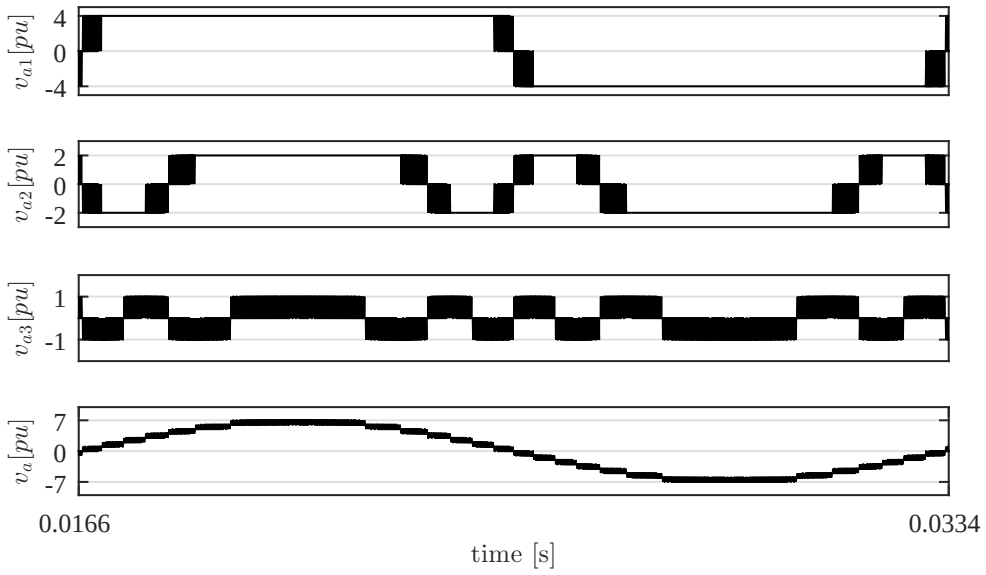


Figure 3.5: Output voltages, v_{a1}, v_{a2} and v_{a3} across each of the three Modules I, II and III respectively, followed by the total phase-to-neutral output voltage, v_a, with a switching frequency of 15 kHz using the proposed modulation

3.3 Harmonic spectrum of voltage for both modulation techniques

3.3.1 Spectrum of module output voltage: Modulation-I

Fig. 3.6 shows the module output voltages and the harmonic spectrum for the modified uni-polar modulation technique. As shown in Fig. 3.6a the leg voltage, v_{l1} generates both positive and zero output voltage during four of the seven positive output voltage levels in a fundamental cycle. As the modulation technique is implemented on the converter topology proposed in [63], the right leg also generates both negative and zero voltage during four of the seven positive output voltage levels. This is different as compared to the conventional modulation techniques with no zero voltages. However, as shown in Fig. 3.6b, the extra switching of the right leg to generate the positive output voltage level still has dominant voltage harmonics at the switching frequency and its sidebands not only for the two leg voltages but also for the module voltage, v_{a1}. Fig. 3.6c shows the two leg voltages and the module output voltage, v_{a1} during the PWM operation. As it can be clearly seen the right leg of the module does generate a negative voltage but as shown in Fig. 3.6d, the harmonics remain at the sidebands of 15kHz.

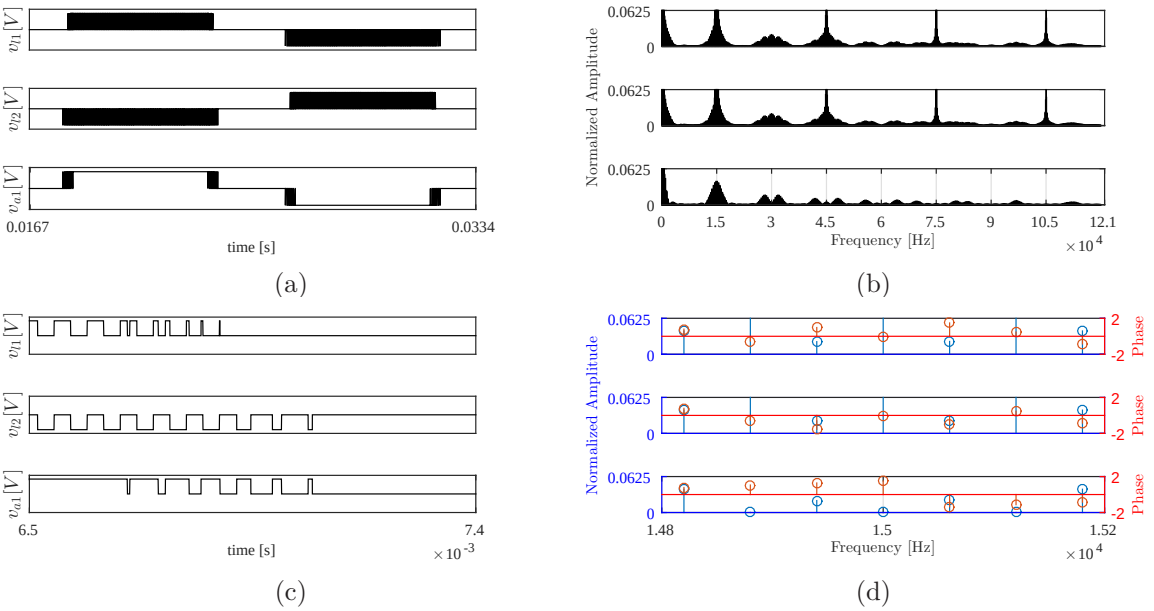


Figure 3.6: Leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1} using modified uni-polar modulation technique (a) Fundamental cycle; (b) Harmonic spectrum ; (c) zoomed in to show the voltage profile during PWM operation; (d) Harmonic spectrum at 15kHz to show that the switching frequency harmonic component is not canceled in the module output voltage, v_{a1}.

3.3.2 Spectrum of module output voltage: Modulation-II

Fig. 3.7 shows the module output voltages and the harmonic spectrum for the modified hybrid modulation technique. As shown in Fig. 3.7a the leg voltage, v_{l1} generates both positive and zero output voltage throughout the seven positive output voltage levels in a fundamental cycle. As the modulation technique is implemented on the converter topology, the right leg also generates both negative and zero voltage during all the seven positive output voltage levels. As shown in Fig. 3.7b, the output voltage has dominant voltage harmonics at the sidebands of twice the switching frequency although the two leg voltages have dominant harmonic at the switching frequency and its sidebands. Fig. 3.7c shows the two leg voltages and the module output voltage, v_{a1} during the PWM operation. As it can be clearly seen both the left and the right leg of the module switch and this results in the output voltage having multiple pulses in a 15kHz interval. Hence, as shown in Fig. 3.7d, the harmonics cancel out at 15kHz and its sidebands.

3.3.3 Spectrum of output voltage

Fig. 3.8a and Fig. 3.8b shows the output voltage across each of the three modules followed by total voltage, v_a using the proposed modulation and the modified uni-polar modulation technique by considering ideal switches of both the primary side H-bridge and the AC-AC converter modules. Fig. 3.8c shows the harmonic spectrum of the output voltage, v_a shown in Fig. 3.8a. As shown in the Fig. 3.8c, the dominant harmonics are at 30kHz which is twice the switching frequency. Fig. 3.8d shows the harmonic spectrum of the output voltage, v_a shown in Fig. 3.8b. As shown in the Fig. 3.8d, the dominant harmonics are at the switching frequency of 15kHz. The harmonic spectrum of the output voltage using both the techniques show that, the proposed modulation allows to achieve the dominant harmonics at twice the switching frequency which leads to a smaller grid filter inductance.

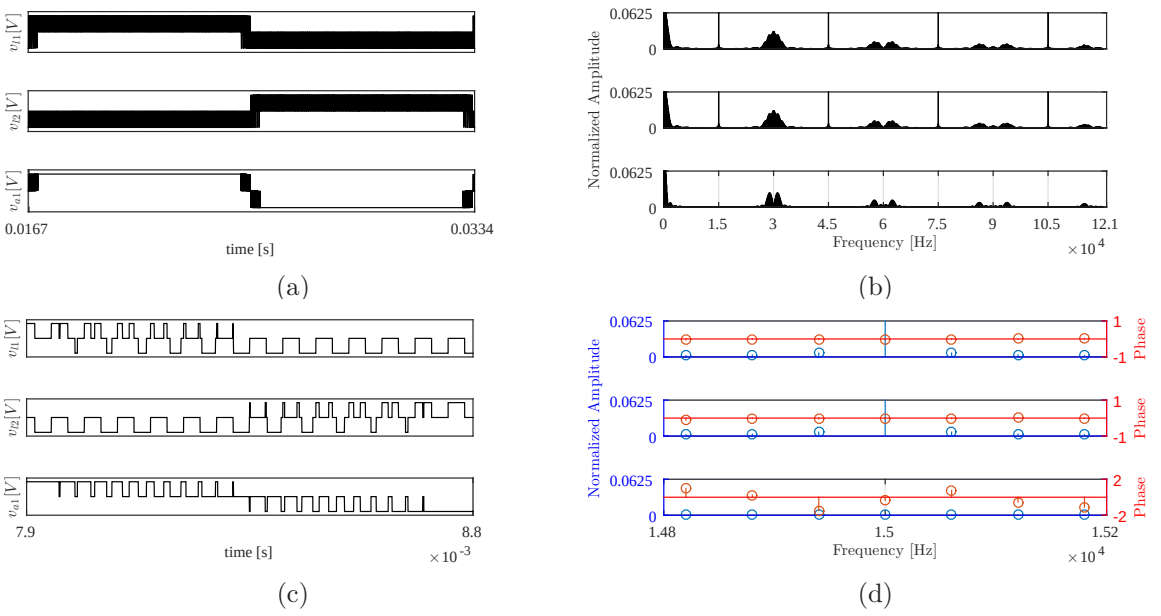


Figure 3.7: (a)Leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1}; (b) Harmonic spectrum of the leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1}; (c)Leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1} zoomed to show the switching during PWM operation; (d) Harmonic spectrum of the three voltages at 15kHz to show the cancellation of the switching frequency harmonic component in the module output voltage, v_{a1}.

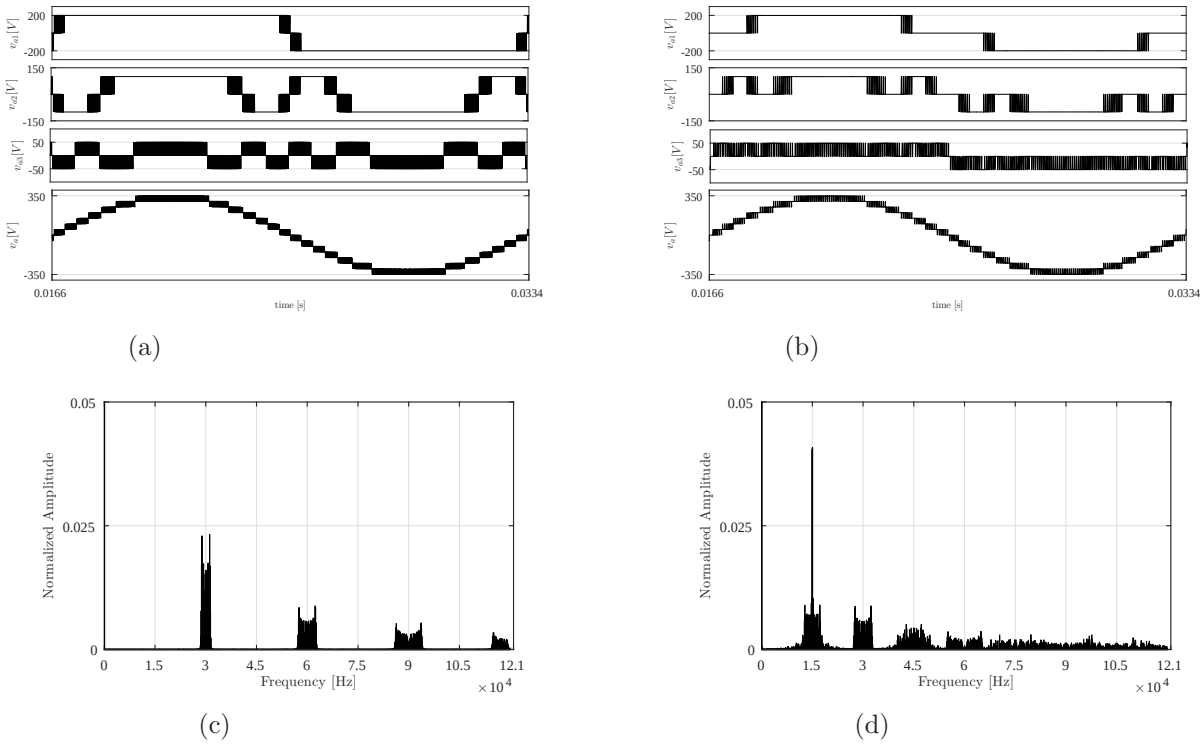


Figure 3.8: Output voltages, v_{a1}, v_{a2} and v_{a3} across each of the three Modules I, II and III respectively, followed by the total phase-to-neutral output voltage, v_a, with a switching frequency of 15 kHz. (a) Proposed Modulation (b) Modified uni-polar modulation presented in [63]. Harmonic spectrum of the output voltage with a switching frequency of 15 kHz(c) Proposed Modulation (d) Modified uni-polar modulation technique

Chapter 4

Non-Ideal Modulation

4.1 Modulation-I: Incorporation of Four-step commutation and Dead-time

4.1.1 Effect on output voltage profile

The previous chapter described the process of the ideal switching from the bottom bi-directional switch S_{3a} to S_{1a} in the left leg of Module I when the link switches from $-V_{in}$ to $+V_{in}$ in order to maintain constant $7nV_{in}$ output voltage. In this section, the effect of switch non-idealities on the phase-neutral output voltage is investigated. The primary side full-bridge switches are controlled using signals a and b with a dead-time interval. On the secondary side each leg of AC-AC converter module follows a four-step commutation algorithm, so that the continuous output current is not interrupted and the isolated secondary windings are not short-circuited. Hence, both uni-directional switches S_{1a1} and S_{1a2} forming a bi-directional switch are controlled independently using q_{1a1} and q_{1a2} respectively. For this case, the same switching transition occurs in all AC-AC converter modules. Hence, the switching transition is described by considering only the primary side full-bridge module and Module I of phase-a. Fig. 4.1a shows the switching signals of the primary side switches and the bi-directional switches of Module I followed by the phase-neutral output voltage for that switching transition. The transition will occur in six modes of operation depicted below as mode I to mode VI in Fig. 4.2: blue indicates the gate signal and red indicates the current path. The output current direction is as shown in Fig. 4.2, and assumed to be positive. A detailed description of different modes is explained below:

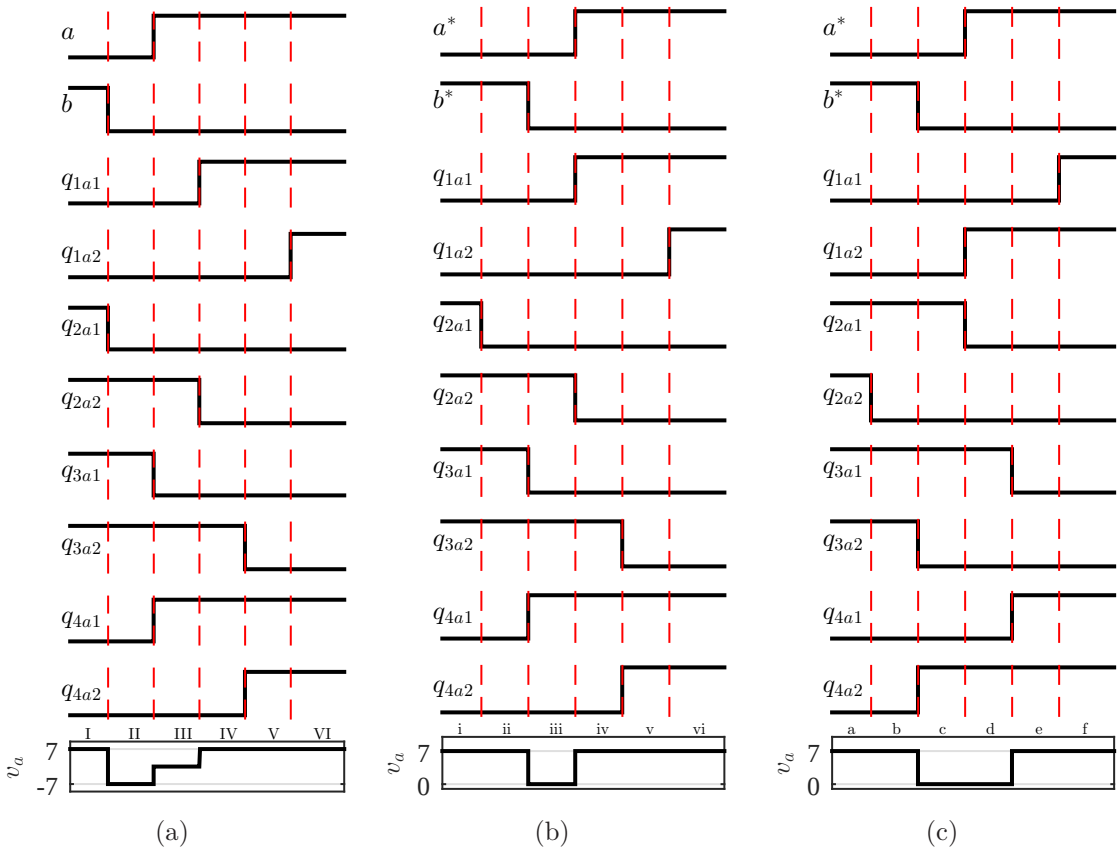


Figure 4.1: Switching signals of primary side full-bridge and AC-AC converter Module I followed by the phase-neutral output voltage, v_a: (a) with four-step commutation of secondary side bi-directional switches and dead time of primary side switches (b) with four-step commutation of secondary side bi-directional switches and dead time of primary side switches along with glitch compensation-I (c) with four-step commutation of secondary side bi-directional switches and dead time of primary side switches along with glitch compensation-I for reverse power flow

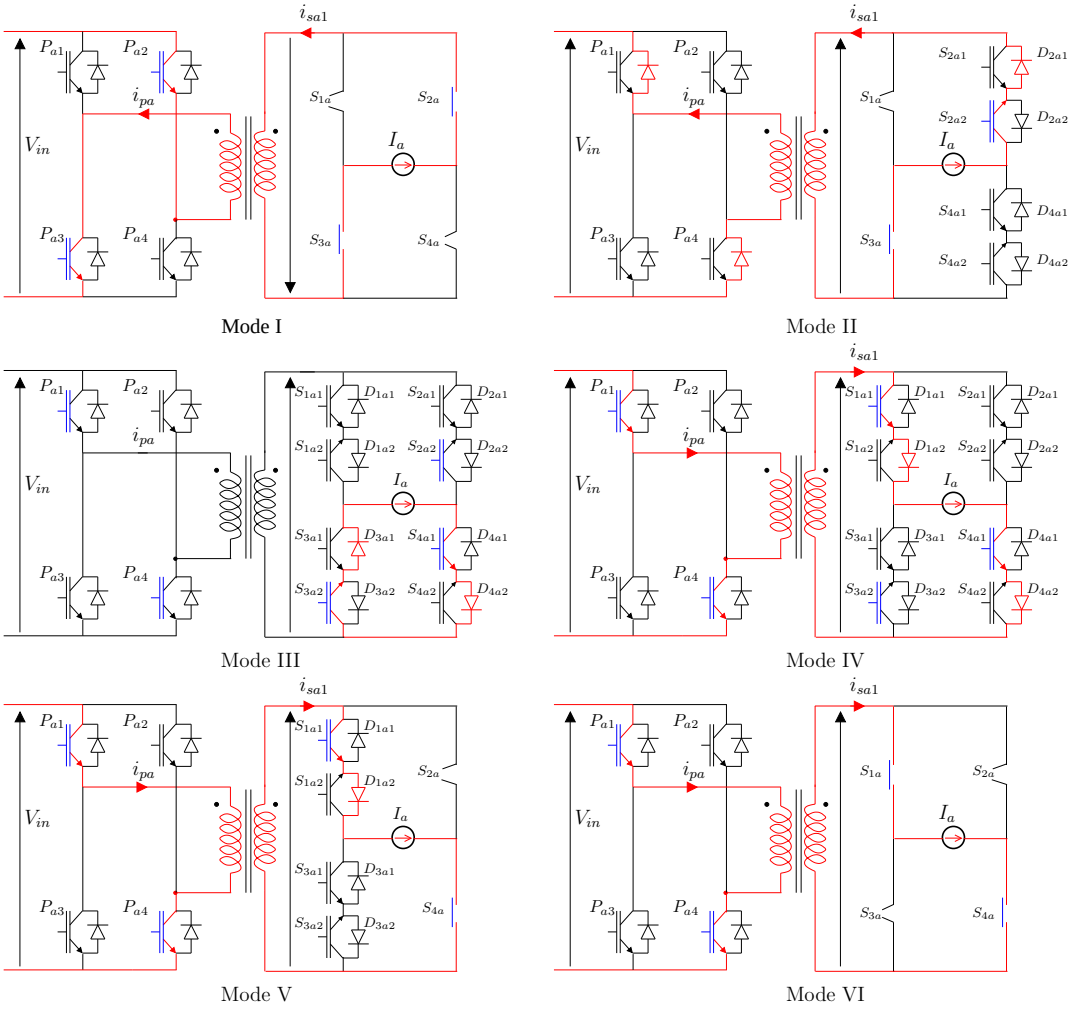


Figure 4.2: Circuit diagram for the various modes of opearation for the case 4.1a for 1 pu input voltage, V_{in} and n= 1

(1) *Mode I*: In this mode, as shown in Fig. 4.1a, b is high and a is low. Mode I of Fig. 4.2 shows the circuit representation in which the switches P_{a2} and P_{a3} are ON. This will result in a negative voltage $-4nV_{in}$ across the link, on the transformer secondary side, as indicated by the arrow pointing downwards. As shown in Fig. 4.1a signals q_{2a1} and q_{2a2}; q_{3a1} and q_{3a2} are high. This corresponds to the bi-directional switches S_{2a} and S_{3a} being ON, as shown in mode I of Fig. 4.2 resulting in a positive module output voltage, v_{a1}= $4nV_{in}$. Similarly, corresponding switches in Modules II and III will also conduct such that, v_{a2}= $2nV_{in}$; v_{a3}= nV_{in} and the total phase-neutral output voltage, v_a is $7nV_{in}$ as shown in 4.1a.

2) *Mode II*: At the beginning of mode *II*, as shown in Fig. 4.1a, signal b is gated low. Corresponding to that, as explained in ideal modulation section, signal q_{2a} goes low.

Hence, the top bi-directional switch of the right leg undergoes the first step of four-step commutation (FSC): the non-conducting switch (S_{2a1}) of the outgoing switch pair (S_{2a}) is gated low (q_{2a1}). Also, in this mode, signal a and hence, the ideal signal, q_{1a} of left leg, does not undergo any switching transition. As shown in mode *II* of Fig. 4.2, the link current, i_{sa1} is negative. On the transformer primary side, as the link current is negative and all switches are turned OFF, as shown in mode *II* of Fig. 4.2 diodes of the switches P_{a1} and P_{a4} conduct, and this results in positive link voltage $+4nV_{in}$, shown by the arrow pointing upwards. For the positive link voltage, as the switch-diode pair explained above on the secondary side conduct, v_a voltage of, $-7nV_{in}$, as shown in mode *II* of Fig. 4.1a is generated.

3) *Mode III*: Mode *III* of Fig. 4.2 shows the circuit representation in which the switches P_{a1} and P_{a4} are ON, as signal a goes high. This will result in $+4nV_{in}$ across the link on the secondary side, as shown by the arrow pointing upwards. On the secondary side, as signal a undergoes transition hence, the ideal signal, q_{3a} goes low. Hence, in the left leg the first step of FSC occurs: the non-conducting switch (S_{3a1}) of the outgoing switch pair (S_{3a}) is gated OFF (q_{3a1}). The current continues to flow through S_{3a2} and D_{3a1} pair. In case of the right leg switch pair, the second step of FSC occurs: conducting switch (S_{4a1}) of the incoming switch pair (S_{4a}) is gated ON (q_{4a1}). In the right leg, even though S_{2a2} is still ON, as the link voltage is positive, the diode D_{2a1} is reverse biased. Hence, the current starts to flow through the S_{4a1} and D_{4a2} pair. This results in a zero voltage, v_a as shown in mode *III* of Fig. 4.1a.

4) *Mode IV*: In this mode, $+4nV_{in}$ voltage across the link on the secondary side is maintained. As shown in mode *IV* of Fig. 4.2, in the left leg of the secondary side module, second step of FSC occurs: the conducting switch (S_{1a1}) of the incoming switch pair (S_{1a}) is gated ON (q_{1a1}). In the left leg, even though S_{3a2} is still ON, as the link voltage is positive, the diode D_{3a1} is reverse biased. Hence, the current flows through the S_{1a1} and D_{1a2} pair, as D_{1a2} is forward biased. In case of the right leg switch pair, the third step of FSC occurs: the conducting switch (S_{2a2}) of the outgoing switch pair (S_{2a}) is gated OFF (q_{2a2}) and the current continues to flow through S_{4a1} and D_{4a2} pair as in mode *III*. $7nV_{in}$ output voltage, is generated as shown in mode *IV* of Fig. 4.1a.

5) *Mode V*: For $+4nV_{in}$ across the link on the secondary side, as shown in Fig. 4.1a, in the left leg, the third step of FSC occurs: the conducting switch (S_{3a2}) of the outgoing switch pair (S_{3a}) in the left leg is gated OFF (q_{3a2}). The current continues to flow through the S_{1a1} and D_{1a2} pair. In case of the right leg switch pair, the last step of

the FSC takes place. The non-conducting switch (S_{4a2}) of the incoming switch pair (S_{4a}) is gated ON (q_{4a2}). This is represented as the bi-directional switch S_{4a} being turned ON as shown in mode *V* of Fig4.2. $7nV_{in}$ output voltage is maintained, as shown in mode *V* of Fig. 4.1a.

6) *Mode VI*: In this mode, for $+4nV_{in}$ across the link on the secondary side, as shown in Fig. 4.1a, in the left leg the last step of FSC occurs: the non-conducting switch (S_{1a2}) of the incoming switch pair (S_{1a}) is gated ON (q_{1a2}). This is represented as the bi-directional switch S_{1a} is turned ON.

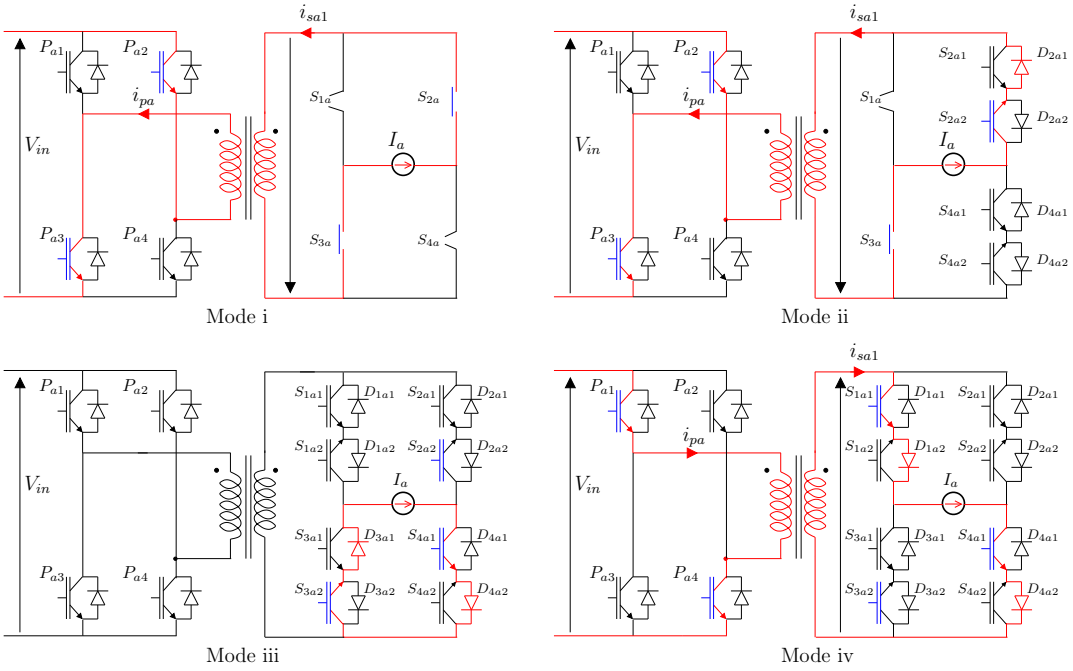


Figure 4.3: Circuit diagram for the various modes of operation for the case 4.1b

The different modes of operation as explained above show that, contrary to the ideal case wherein the output voltage, v_a is always positive $7nV_{in}$ as shown in Fig. 3.2, the output voltage is $-7nV_{in}$ in mode *II* and zero in mode *III* as shown in Fig. 4.1a. Fig. 4.4 shows the output voltage across Modules I, II and III followed by, v_a with switch non-idealities. The generated output voltage has a voltage profile different as compared to the ideal modulation strategy as highlighted by the pink and blue patches in the output voltage, v_a.

4.1.2 Glitch Compensation-I

In this section, a compensation technique is proposed to negate the negative voltage glitch which occurs in mode *II* of Fig. 4.1a. Fig. 4.3 shows the different modes of circuit operation for the exact same transition as in the previous section but with glitch compensation. Modes

v and *vi* of Glitch Compensation-I are same as modes *V* and *VI*, and hence, not shown in Fig. 4.3. A detailed description of different modes of operation is explained below:

1) *Mode i*: In this mode, as shown in Fig. 4.1b and Fig. 4.3, the switching signals and the circuit operation is exactly the same as mode *I*.

2) *Mode ii*: In this mode, as shown in Fig. 4.1b, b^* is still ON. This mode of operation is different from mode *II* of Fig. 4.1a and Fig. 4.2 where *b* was gated OFF. The secondary side switching is still determined by signals *a* and *b*. Hence, it remains the same as that of mode *II*. As shown in mode *ii* of Fig. 4.3, as the switches P_{a2} and P_{a3} still conduct, this maintains the link voltage on the secondary side as $-4nV_{in}$, as shown by the arrow pointing downwards. For the negative link voltage, the switch-diode pair as explained above on the secondary side conduct, resulting in $7nV_{in}$ voltage, v_a as shown in mode *ii* of Fig. 4.1b, hence, negating the negative voltage $-7nV_{in}$ as shown in mode *II* of Fig. 4.1a.

3) *Mode iii*: In this mode, as shown in Fig. 4.1b, b^* is gated OFF. All the switches of the primary side are gated OFF. On the secondary side, as explained in mode *III*, output current freewheels through the bottom two switch-diode pair resulting in zero voltage across the link and the output as shown in mode *III* of Fig. 4.1b.

4) *Mode iv*: In this mode, as shown in Fig. 4.1b, a^* is gated ON. As shown in mode *iv* of Fig. 4.3 this results in a positive voltage $+4nV_{in}$ across the link. For the positive link voltage as explained above in mode *IV*, the corresponding switch-diode pair on the secondary side conduct, resulting in $7nV_{in}$ voltage, v_a as shown in mode *iv* of Fig. 4.1b.

5) *Mode v* and *vi*: The modes of operation are the same as in modes *V* and *VI*.

The different modes of operation as explained above, show that the glitch compensation allows to negate the $-7nV_{in}$ voltage occurring in mode *II* of Fig. 4.1a, as shown in mode *ii* of Fig. 4.1b. Fig. 4.5 shows the output voltage across Modules I, II and III followed by, v_a with switch non-idealities. The output voltage does not go to $-7nV_{in}$ but still goes to zero in each switching cycle. Along with the distortion caused during the link voltage transition, the output voltage v_a, also has distortion during the generation of certain voltage levels when the link is constant as shown in Fig. 4.4 (highlighted by blue patches) which are not negated by glitch compensation-I as shown in Fig. 4.5.

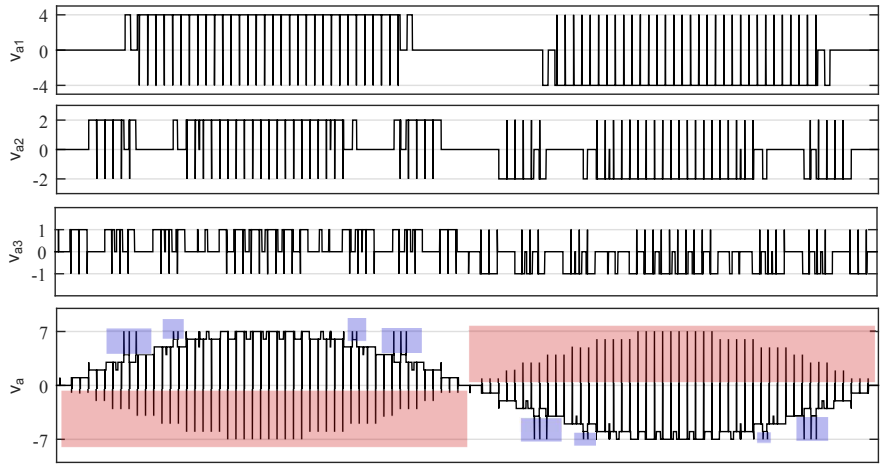


Figure 4.4: Voltage waveforms of series connected converter modules followed by phase-neutral voltage for a fundamental cycle for 1 pu input voltage, V_{in} and n= 1: for case Fig. 4.1a without any compensation.

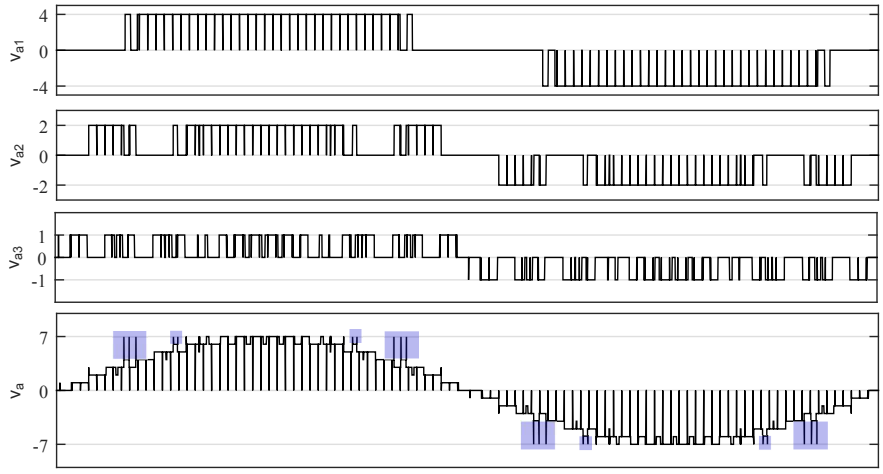


Figure 4.5: Voltage waveforms of series connected converter modules followed by phase-neutral voltage for a fundamental cycle for 1 pu input voltage, V_{in} and n= 1: for Fig. 4.1b with Glitch Compensation-I.

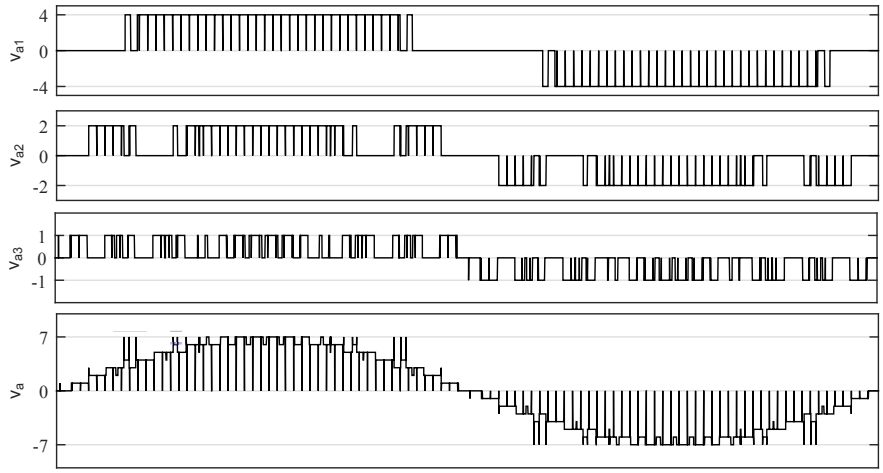


Figure 4.6: Voltage waveforms of series connected converter modules followed by phase-neutral voltage for a fundamental cycle for 1 pu input voltage, V_{in} and n= 1: for case 4.1c with glitch compensation-I and reverse power flow.

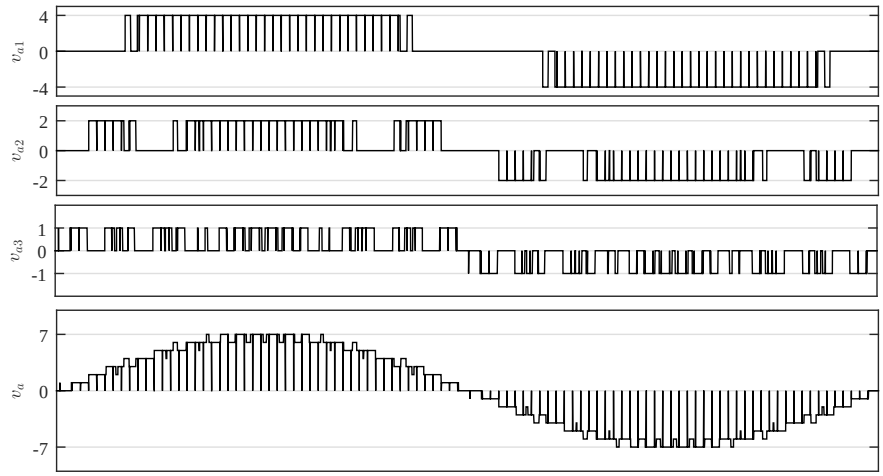


Figure 4.7: Voltage waveforms of series connected converter modules followed by phase-neutral voltage for a fundamental cycle for 1 pu input voltage, V_{in} and n= 1: with Glitch Compensation I and II.

4.1.3 Glitch Compensation-I (during reverse power flow)

The modulation and commutation pertaining to the power flow in the reverse direction that is from the three-phase grid to the DC supply is shown in Fig. 4.1c. It is to be noted that the primary side signals and the secondary side ideal switch signals will remain the same but

the commutation will change as the current direction is reversed. Fig. 4.1c and 4.8 show the switching signals and the modes of circuit operation respectively for the exact same transition but with the current direction reversed. Based on the current direction, as shown in Fig. 4.1c, the corresponding switches conduct on the secondary side converter during the various modes of operation. The resulting output voltage after glitch compensation-I is $7nV_{in}$ in modes a, b, e and f and zero in c. This is similar to Fig. 4.1b for positive current. However, in mode d, the operation is different as shown below:

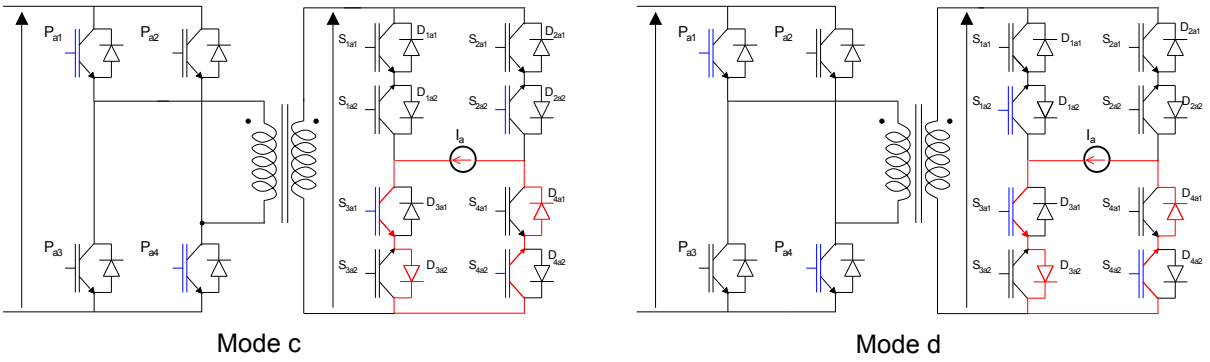


Figure 4.8: Circuit diagram for the various modes of opearation for the case 4.1c for 1 pu input voltage, V_{in} and n= 1

4) *Mode d*: On the secondary side, as shown in mode d of Fig. 4.8, in the left leg, second step of FSC occurs: the conducting switch (S_{1a2}) of the incoming switch pair (S_{1a}) is gated ON (q_{1a2}). In the left leg, even though S_{1a2} is gated ON, as the link voltage is positive, the diode D_{1a1} is reverse biased. Hence, the current continues to flow through the S_{3a1} and D_{3a2} pair, as D_{3a2} is forward biased. This mode of operation is different as compared to mode *iv* of Fig. 4.1b where the transition in the left leg was natural, unlike the forced commutation in this case. In case of the right leg switch pair, the third step of FSC occurs: the conducting switch (S_{2a1}) of the outgoing switch pair (S_{2a}) is gated OFF (q_{2a1}) and the current continues to flow through S_{4a2} and D_{4a1} pair as in mode c. Switches as shown in mode d of Fig. 4.8 conduct, resulting in an additional zero voltage, v_a interval as shown in mode d of Fig. 4.1c, different from mode *iv* of Fig. 4.1b. Fig. 4.6 shows the output voltage across Modules I, II and III followed by, v_a with switch non-idealities. The output voltage profile is similar to Fig. 4.5, except that it has an additional zero voltage interval.

The top plot of Fig. 4.9a, is the output voltage considering both the four-step commutation of the bi-directional switches and the dead-time of the primary side switches. This results in a large input current ripple as shown in the middle plot of Fig. 4.9a of one phase and bottom plot of Fig. 4.9a of all three phases. The high input ripple current will require

large passive components on the input side. However, as explained earlier, by incorporating glitch compensation-I the output voltage improves as shown in top plot of Fig. 4.9b, which results in the reduction of the input current ripple as shown in the middle and the bottom plots of Fig. 4.9b of the single and three phases respectively. Hence, the modifications in the switching signals allow to improve the power quality.

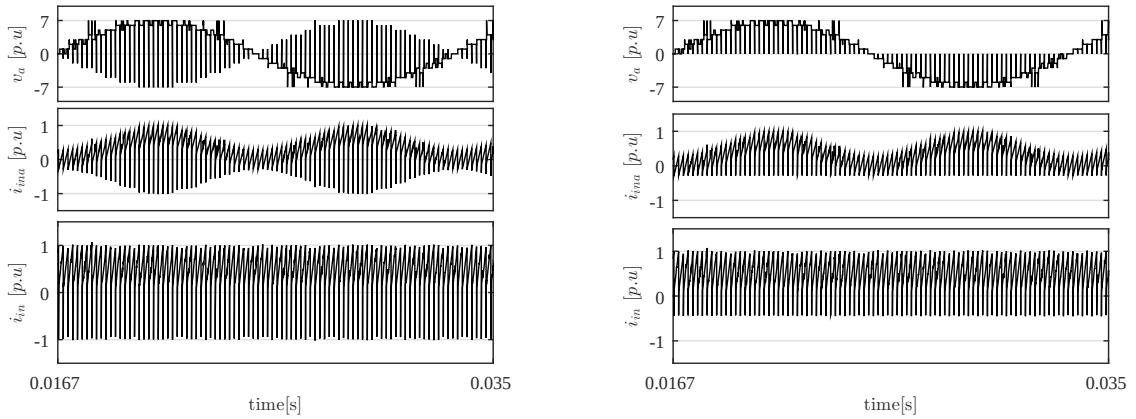


Figure 4.9: (Top) Output phase voltage, v_a (a) without any glitch compensation, (b) with glitch compensation-I; (Middle) Input current of single H-bridge (a) without any glitch compensation, (b) with glitch compensation-I; (Bottom) Total input current of all three H-bridges (a) without any glitch compensation, (b) with glitch compensation-I

4.1.4 Glitch Compensation-II

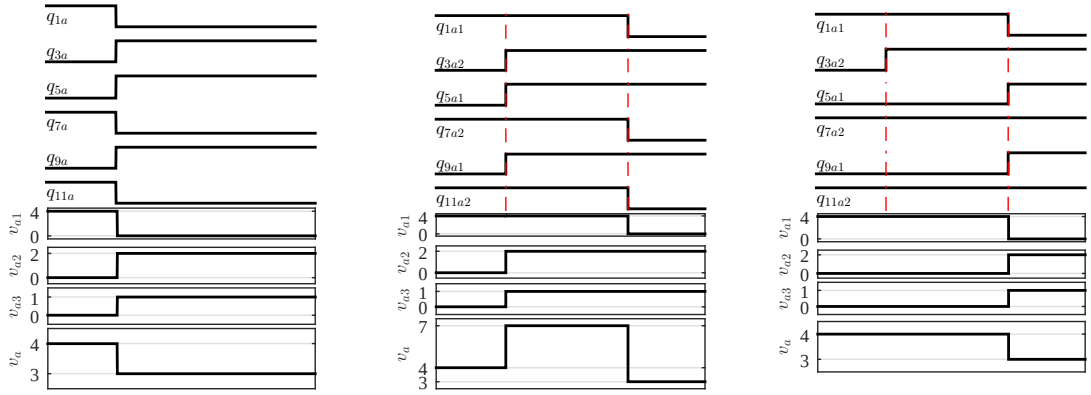


Figure 4.10: Switching signals of left leg bi-directional switches of all three AC-AC converter modules followed by the module and the phase-neutral output voltage: (a) ideal signals without four-step commutation; (b) with four-step commutation of secondary side bi-directional switches; (c) with four-step commutation of secondary side bi-directional switches and glitch compensation-II

As shown in Fig. 4.3 and 4.5 the glitches (highlighted by blue patches) in v_a are caused due to the interdependence of the three AC-AC converter modules in each phase. The section explains the cause and the compensation done to avoid the glitch. In Fig. 2.4 at a specific instant of time, consider the link voltages v_{sa1}, v_{sa2} and v_{sa3} and the output current, i_a to be positive. The output voltage level to be synthesized is $4nV_{in} \rightarrow 3nV_{in}$. As shown in Table 8.1, all the modules have to generate a pulsating voltage and hence, all three modules will undergo switching even though the link voltage is constant, as explained in the ideal modulation section. Fig. 4.10a shows the ideal switching signals of the bi-directional switches of the left leg of all the three modules in phase a as throughout the transition, in the right leg, the bottom bi-directional switch will be ON in all three modules. Also, the figure shows the output voltage waveform of the series connected converter modules followed by, v_a for the above described case. As shown in the Fig. 4.10a, when $q_{1a} = 1$; $q_{5a} = q_{9a} = 0$, v_a is $4nV_{in}$ and when $q_{1a} = 0$; $q_{2a} = q_{3a} = 1$, v_a is $3nV_{in}$. In case of ideal modulation, there is no delay during the switch transition and hence, there is no glitch in the output voltage.

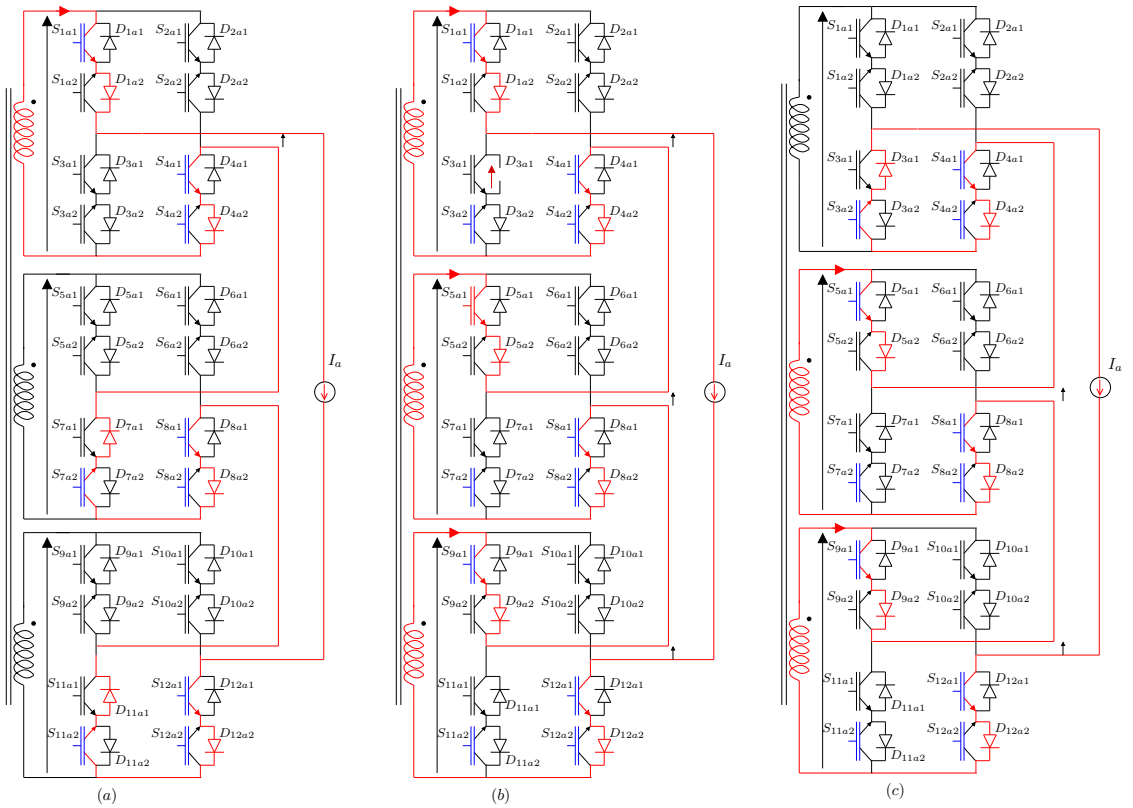


Figure 4.11: Circuit diagram for the various modes of operation (left) after first step of FSC resulting in $4nV_{in}$ (center) after second step of FSC resulting in $7nV_{in}$ output voltage instead of $3nV_{in}$ (right) after second step of FSC with compensation resulting in $3nV_{in}$

Fig. 4.10b shows the switching signals for non-ideal bi-directional switches; that is, with FSC. In Module I, the transition is from the top two uni-directional switch set to the bottom, whereas for Module II and III the transition is vice-versa. Fig 4.11a shows the circuit diagram for all three modules when the output voltage, v_a is $4nV_{in}$ and the first step (turn OFF non-conducting switch of the outgoing switch pair) of FSC has already occurred. To illustrate, the non-conducting switches (S_{1a2}, S_{7a1} and S_{11a1}) of the outgoing switch pair (S_{1a}, S_{7a} and S_{11a}) respectively are gated OFF (q_{1a2}, q_{7a1} and q_{11a1}). Fig. 4.11b shows the circuit diagram wherein, the conducting switches (S_{3a2}, S_{5a1} and S_{9a1}) of the incoming switch pair (S_{3a}, S_{5a} and S_{9a}) are gated ON (q_{3a2}, q_{5a1} and q_{9a1}) simultaneously as shown in Fig. 4.10b. As the link voltage is positive, diode D_{3a1} is reverse biased, but (D_{5a2} and D_{9a2}) are forward biased. Hence, in Module I no transition occurs. However, in Modules II and III the switching transition takes place. Hence, the output voltage is $7nV_{in}$ instead of $3nV_{in}$ as shown in Fig. 4.10b. When q_{1a1} is gated OFF, the output voltage v_{a1} across Module I is zero and the total output voltage v_a, is $3nV_{in}$. To summarize, Module I undergoes forced commutation whereas, Modules II and III undergo natural commutation resulting in a glitch in the output voltage.

The glitch in the output voltage can be avoided by delaying the signals of the modules undergoing natural commutation to match them with the signal of the module undergoing forced commutation. In this case, as shown in Fig. 4.11c, the conducting switch (S_{1a1}) of the outgoing switch pair (S_{1a}) is gated OFF (q_{1a1}) and the conducting switches (S_{5a1} and S_{9a1}) of the incoming switch pair (S_{5a} and S_{9a}) are gated ON (q_{5a1} and q_{9a1}) simultaneously as shown in Fig. 4.10c. This causes Modules II and III to generate $2nV_{in}$ and nV_{in} respectively only when, v_{a1} is zero. Hence, the output voltage is $3nV_{in}$. However, as shown in Fig. 4.10c, the third and fourth step of FSC of modules undergoing natural commutation need to be further delayed.

From Table 8.1 and Fig. 4.5 it can be seen that, glitch in the phase-neutral output voltage occurs, whenever two or more secondary side modules change state simultaneously and the primary side remains fixed. Table 4.1, shows the switch which undergoes natural commutation (this switching is to be delayed to match with the switch undergoing forced commutation) for a particular output voltage level to be synthesized for a positive link voltage. Fig. 4.7 shows the output voltage across Modules I, II and III followed by the total phase-neutral output voltage, v_a with switch non-idealities after both compensation. The output voltage still goes to zero in each switching cycle caused because of the dead-time of primary side switches. The zero interval cannot be avoided but can be minimized by using devices with extremely fast turn on and turn off times.

Table 4.1: Various instances of Glitch Compensation-II for a constant positive link voltage, for generating different positive levels in phase-neutral output voltage

Case	Output Voltage	Switch OFF (Forced)	Switch ON(Natural)
I	$6nV_{in} \rightarrow 5nV_{in}$ $2nV_{in} \rightarrow nV_{in}$	S_{5a1}	S_{9a1}
II	$5nV_{in} \rightarrow 6nV_{in}$ $nV_{in} \rightarrow 2nV_{in}$	S_{9a1}	S_{5a1}
III	$4nV_{in} \rightarrow 3nV_{in}$	S_{1a1}	S_{5a1}, S_{9a1}
IV	$3nV_{in} \rightarrow 4nV_{in}$	S_{5a1}, S_{9a1}	S_{1a1}

4.2 Modulation-II: Incorporation of switch non-idealities

The previous chapter described the ideal modified hybrid modulation technique wherein, all the switches (that is no turn-on and turn-off times) are considered to be ideal and the output voltage profile is shown in Fig. 4.2 for a fundamental cycle. This section explains

the distortions in the phase-to-neutral output voltage because of the modifications in the switching signals:

i. considering only the switches of primary side H-bridge non-ideal.

ii. to incorporate the four-step commutation strategy.

iii. both (i) and (ii).

4.2.1 Dead-time in the switches of primary side H-bridge

As shown in Fig. 4.12b, a dead-time is incorporated in the primary side H-bridge switch signals. The switches of the AC-AC converter module are still considered ideal. For the case considered in the ideal modulation section, as shown in Fig. 4.12b, for the reason explained earlier, signals s_{1a}, s_{5a} and s_{10a} follow s_1 (same as p_1) and hence the switching signals are similar to the ideal modulation as shown in Fig. 4.12a. However, the switching signal p_2 (in this case s_2) is high after a dead-time interval. This implies, that the signals s_{2a}, s_{6a} and s_{11a} are also delayed as compared to the ideal modulation in Fig. 4.12a as these signals follow s_2. But this will require the two bi-directional switches in each leg to switch simultaneously (S_{1a} turns OFF and S_{3a} turns ON). Due to the switch non-ideality a four-step commutation strategy is required.

4.2.2 Four-step commutation for switches of AC-AC Module

Each leg of the AC-AC converter module has to undergo a commutation process to satisfy two conditions:

- The isolated secondary winding connected to the AC-AC converter module is not short-circuited.
- The output current is not interrupted.

Implementation of the conventional four-step commutation strategy satisfies both the above conditions. As an example, when the link voltage is negative, if Module III is required to pulsate from $0 \rightarrow -nV_{dc}$, as explained in ideal modulation above, the output current, I_a which is assumed as shown in Fig. 4.13, has to switch from S_{11a} to S_{9a}. At a particular instant of time, the link voltage is negative and uni-directional switch pair, S_{11a1} and S_{11a2} are ON. A four-step commutation procedure is to be carried out to switch the currents from bi-directional switch S_{11a} to switch S_{9a}. The steps to do the same are described below:

In the first step, turn OFF S_{11a1} (outgoing non-conducting switch), as (S_{11a2}, D_{11a1}) pair is carrying the current.

Turn ON the IGBT, S_{9a1} (incoming conducting switch) after a commutation delay interval. As the link voltage is negative, diode D_{9a2} is reverse biased. Hence, the current will not commutate when S_{9a1} is turned ON but will continue to flow through (S_{11a2}, D_{11a1}) pair. Mode 4 of Fig. 4.13b shows the circuit diagram where D_{9a2} is reverse biased.

Turn OFF the IGBT, S_{11a2} (outgoing conducting switch), which was carrying the current after an additional commutation delay interval. At this instant, the current will commutate to (S_{9a1}, D_{9a2}) pair. This is forced commutation.

Turn ON the IGBT switch, S_{9a2} (incoming non-conducting switch) in which the diode D_{9a2} is carrying the current after one more commutation delay interval. In this manner, t]

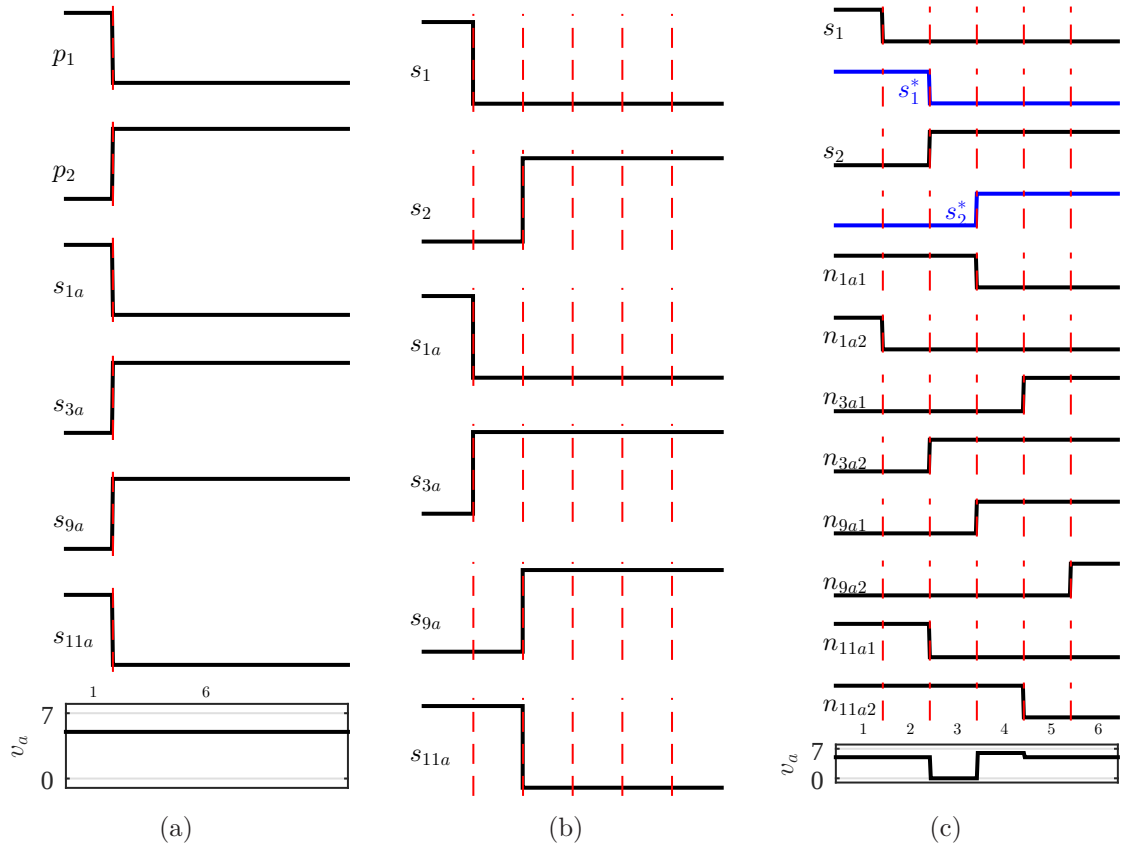
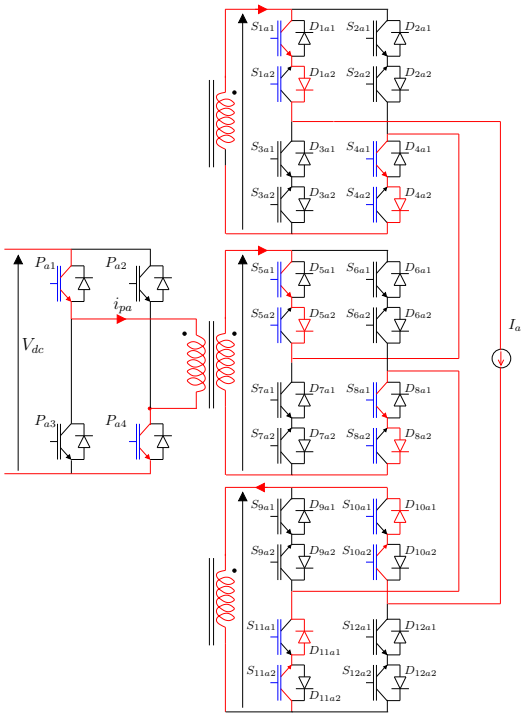


Figure 4.12: (a) Ideal signals without dead-time of primary side H-bridge switches and without four-step commutation of secondary side bi-directional switches and ideal output voltage, v_a.(b) Signals with dead-time of primary side H-bridge switches and without four-step commutation of secondary side bi-directional switches. (c) Signals with dead-time of primary side H-bridge switches and with four-step commutation of secondary side bi-directional switches and the distortion in the output voltage, v_a.

4.2.3 Effect on output voltage profile-Switching Cycle Transition

In the above case the link voltage was constant and only the left leg of Module III went through the transition. But if the link voltage is also changing then the transition will occur in six modes of operation as depicted in Fig. 4.13.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P_{a2}
i_{pa}
V_{dc}
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P_{a4}
I_a
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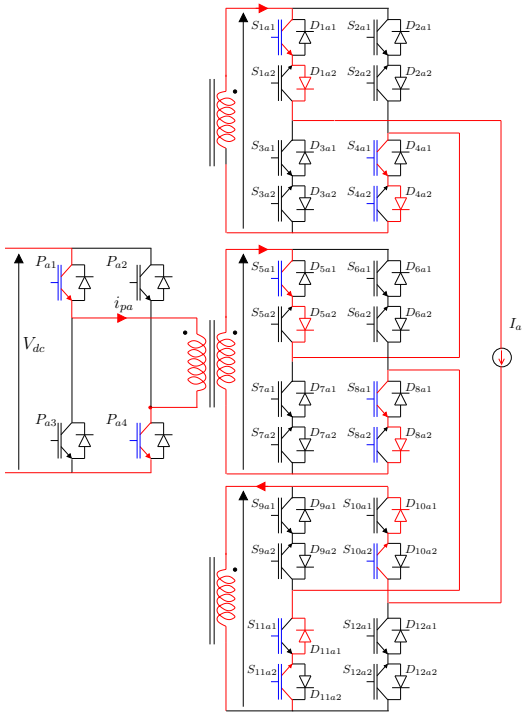
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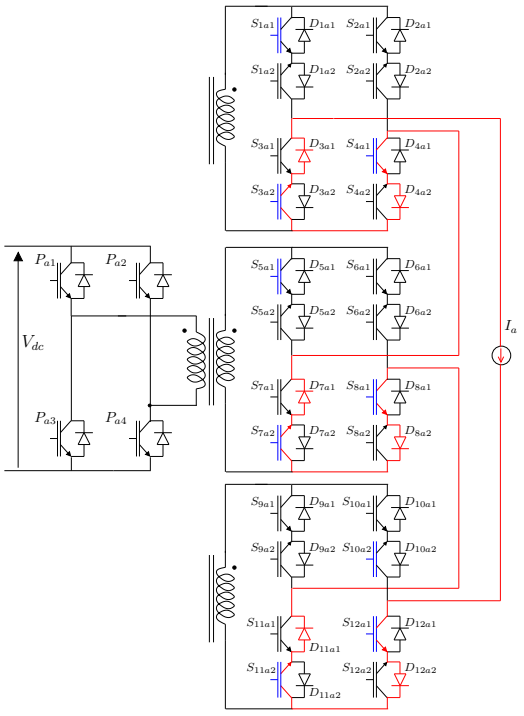
2

(a)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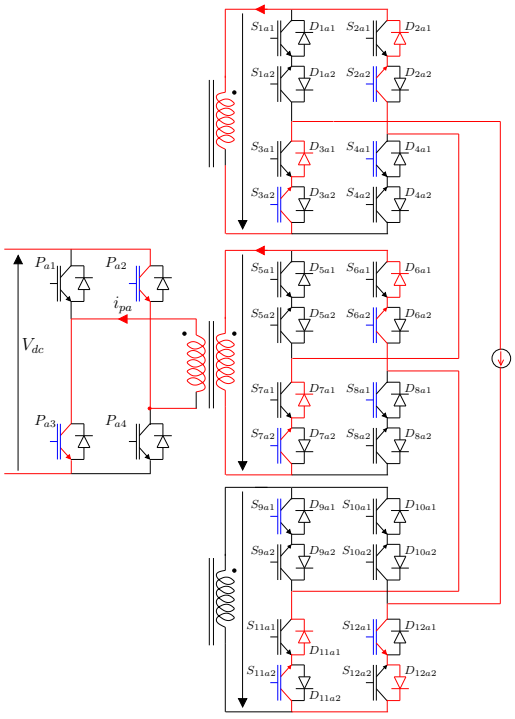
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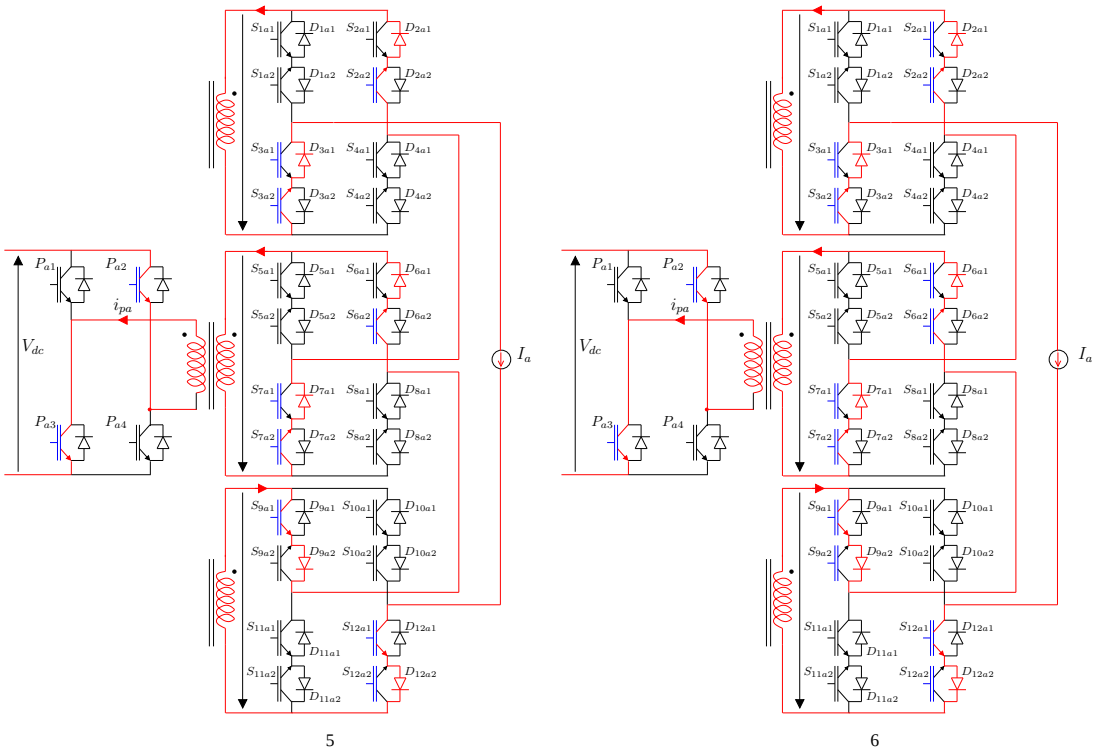
S_{7a2} D_{7a2} S_{8a2} D_{8a2}
S_{9a1} D_{9a1} S_{10a1} D_{10a1}
S_{9a2} D_{9a2} S_{10a2} D_{10a2}
S_{11a1} D_{11a1} S_{12a1} D_{12a1}
S_{11a2} D_{11a2} S_{12a2} D_{12a2}

4

(b)



(c)

Figure 4.13: Circuit diagram for the various modes of operation for the case Fig. 4.12c. Blue indicates the gate signals and red indicates the current path.

The modes are explained by considering a case in which the desired output voltage to be generated is positive, $5nV_{dc}$ and the current direction is as shown in Fig. 4.13, and assumed to be positive while the link voltage pulsates from $+V_{dc}$ to $-V_{dc}$. Fig. 4.12c shows the switching signals of the primary side H-bridge switches (s_1^* and s_2^*) which are delayed by one commutation time to improve the output voltage profile and the two bi-directional switches of left leg of Module I (S_{1a} and S_{3a}) and Module III (S_{10a} and S_{11a}) followed by the phase-to-neutral output voltage for the above transition. As the bi-directional switch is not considered ideal, hence each uni-directional switch is controlled by one switching signal. As shown in Fig. 4.12c, n_{1a1} and n_{1a2} are the signals for uni-directional switch pair S_{1a1} and S_{1a2} respectively. The switching signals of the right leg bi-directional switches are not shown and can be interpreted from Fig.4.13 (Blue color indicates the switch turned ON and red indicates the current path). For the transition considered, as shown in Table 3.2, Module I and Module II will behave exactly the same and hence, the switching signals of Module II are not shown in Fig. 4.12c. A detailed description of the different modes of circuit operation is explained below:

Mode 1: This mode corresponds to the initial state as described above, wherein the link voltage is $+V_{dc}$ and the phase-to-neutral output voltage to be generated is $5nV_{dc}$ as

shown in Mode 1 of Fig. 4.12c. Mode 1 of Fig. 4.13a shows the circuit representation, which depicts the switches ON/OFF in each of the converter module to generate the above output voltage.

Mode 2: In this mode, s_1 goes low but as the actual primary side H-bridge signals are delayed by one commutation time, hence, the link voltage is still $+V_{dc}$. As mentioned earlier in ideal modulation, as the module output voltage to be generated in Modules I and II are positive and in Module III is negative, in Modules I and II the left leg top bi-directional switch signals and in Module III the right leg top bi-directional switch signal follow s_1 as shown in Fig. 4.12c. As s_1 goes low, the first step of the four-step commutation process (turn OFF the outgoing non-conducting switch) starts in left leg of Module I and II and in right leg of Module III. Whereas in the adjacent leg of each module there is no change in the switch state. As shown in Mode 2 of Fig. 4.13a, the current path in each of the three modules show that the phase-to-neutral output voltage will be maintained as in Mode 1 at $5nV_{dc}$.

Mode 3: As shown in Fig. 4.12c, on the primary side s_1^* goes low. This means none of the switches on the primary side H-bridge are ON. On the secondary side, the switches of the left leg of Modules I and II and right leg of Module III undergo second step of four-step commutation (turn ON the incoming conducting switch). At this instant, s_2 goes high and hence, the adjacent leg in each module undergo first step of the commutation process. As shown in Mode 3 of Fig. 4.12c, the phase-to-neutral output voltage will be zero instead of being maintained as in Mode 1. This is because as seen in Mode 3 of Fig. 4.13b, the switches of the left leg of Modules I and II and right leg of Module III undergo natural commutation. Also, in the adjacent leg of all the three modules, the bottom switch and the anti-parallel diode pair are still conducting. Hence, all the three modules freewheel the output current and hence, the output voltage is zero. Moreover, in the primary side H-bridge none of the switches/diodes conduct, and as the link current is zero, even the link voltage is zero.

Mode 4: At the beginning of the mode, as shown in Fig. 4.12c, on the primary side H-bridge s_2^* goes high. On the secondary side, as shown in Fig. 4.12c, left leg of Modules I and II and right leg of Module III undergo third step of four-step commutation (turn OFF the outgoing conducting switch) whereas, the adjacent leg in each module undergo second step of the commutation process. The phase-to-neutral output voltage will be positive but instead of being at $5nV_{dc}$, it will be at $6nV_{dc}$. This is because, the left leg bi-directional switches of Module I and II and the right leg bi-directional switch of Module III have already undergone commutation. In the right leg of Module I and II the bi-directional switches undergo natural commutation and hence, the module output voltage of Modules I and II are $4nV_{dc}$ and $2nV_{dc}$ respectively. But in Module III, as the link voltage is negative,

the diode of the incoming bi-directional switch pair, D_{9a2} is reverse biased as explained in the four-step commutation section above, and Module III continues to generate zero voltage, whereas, the required voltage to be generated by Module III is $-nV_{dc}$.

Mode 5: In this mode, as shown in Fig. 4.12c, the last step of four-step commutation occurs in the left leg of Modules I and II and right leg of Module III (turn ON the incoming non-conducting switch), whereas, in the adjacent leg, third step of four-step commutation takes place. This is shown in Mode 5 of Fig. 4.13c. The phase-to-neutral output voltage will be $5nV_{dc}$ as shown in Fig. 4.12c, as all the modules generate the voltage as shown in Table 3.2 with the link voltage negative.

Mode 6: This mode corresponds to the final step of the switching transition. In this mode in the right leg of Modules I and II and in the left leg of Module III the last step of four-step commutation occurs. Mode 6 of Fig. 4.12c shows the switching signals that are high/low; and Mode 6 of Fig. 4.13c shows the circuit representation, which depicts the switches ON/OFF in each of the converter module so that the phase-to-neutral output voltage to be generated is $5nV_{dc}$ with the link voltage, $-V_{dc}$.

Hence, as shown in Fig. 4.12c the output voltage, v_a in comparison to the ideal case Fig. 4.12a, is distorted because of the switch non-idealities as explained in the six modes of operation.

Chapter 5

Design of High-Frequency Four Winding Transformer

5.1 Transformer design

For the converter topology shown in Fig. 2.4 the HFT requires a single primary winding and three secondary windings for each phase. The three secondary windings of the transformer should have an asymmetrical turns ratio as explained in the previous section along with low leakage inductance and ac resistance. Multi-winding HFTs using advanced soft magnetic materials, like amorphous and nanocrystalline have been designed for converter topologies to interface renewables to three-phase grid [85, 86]. Although difficult to manufacture, several prototypes of multi-winding HFTs [83, 85–88] and in [87] a 35kVA, 10kHz, 22kV/800V five-winding transformer has been designed and tested.

Table 5.1: Transformer specifications

Parameter	Real Power, P	Primary Voltage, V_p	Frequency, f	B_{max}	J	k_w
Value	2 kW	100 V	15 kHz	0.38 T	3.5A/mm^2	0.35

5.1.1 Transformer specifications and core material

Table 5.1 outlines the high-frequency transformer specifications. Area product method is used to design the transformer. The maximum flux density, B_{max} and current density J, are chosen to be 0.38 T and 3.5 A/mm^2 respectively [89]. Area product, A_p can be computed using (5.1) as all the other parameters like (V_{in}, I_{in}, f_{sw}) are known from the converter specifications. As shown in Fig. 5.2b, the volumes of the transformer core for different materials and high frequency have been compared. The soft magnetic materials

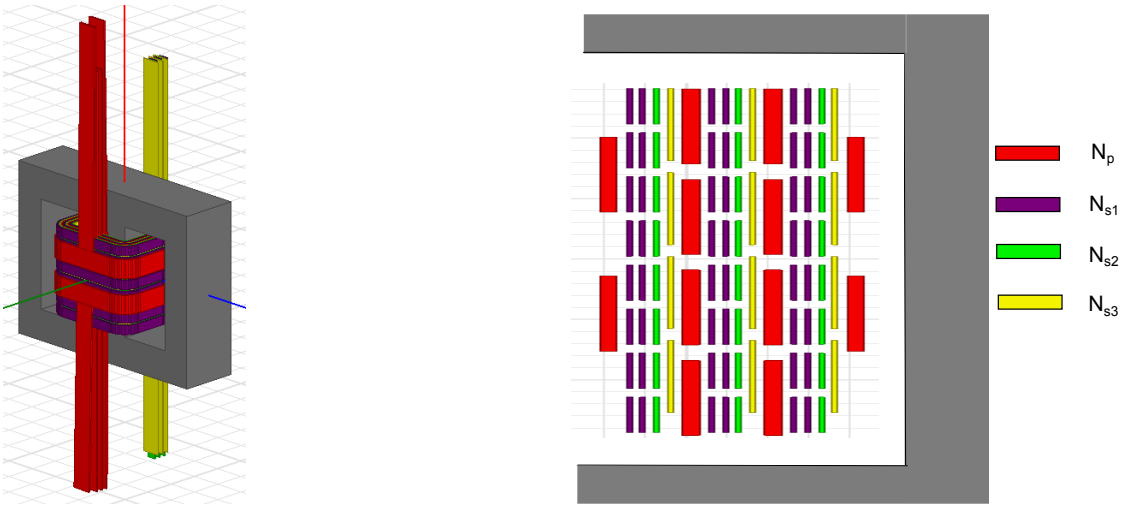
allow to achieve lower volume for the same switching frequency. However, the transformer for the proposed converter prototype is designed with ferrite core 0P47228EC owing to the ease of availability. As the core dimensions are known, the core cross-sectional area can be computed. In the proposed converter topology the link voltages are square in nature. Hence, the required number of primary turns N_p, on a core with cross-sectional area A_c, and excited with a voltage, V_{in} at a link frequency f_{sw} so that the maximum flux density B_{max} is not exceeded can be determined.

5.1.2 Winding design

The winding design of a high-frequency transformer is a critical part of the design as the proper selection of windings ensure lower losses due to low ac resistance [90–93]. Also, proper winding arrangement will be essential to attain low leakage inductance. The skin-depth at f_{sw}= $15kHz$ is 0.532 mm. The primary and secondary windings were designed with foil conductors having dimensions 0.5588 mm X 6.35 mm and 0.2286 mm X 3.048 mm respectively. The bare copper wires were wound with 3M-44 tapes having an insulation thickness of 0.139 mm. The converter topology requires that the transformer should be designed such that the leakage inductances of the secondary side windings are low. For this, the 12 primary and 12, 24 and 48 secondary turns respectively of the four winding transformer are interleaved as shown in the winding arrangement diagram in Fig. 5.1b. The interleaving consists of four sections of primary and secondary turns.

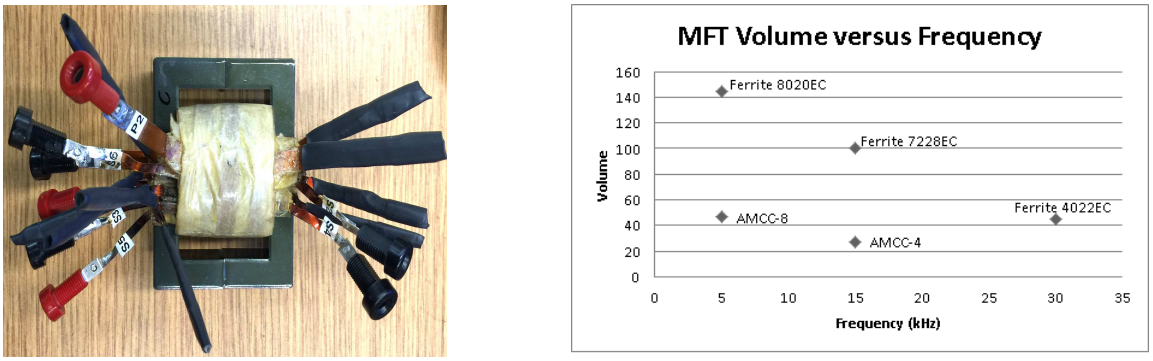
$$A_p = \frac{2V_{in}I_{in}}{4f_{sw}B_{max}Jk_w} \tag{5.1}$$

Once, N_p is computed, the number of turns in the three secondary windings are N_{s1}= $4nN_p$; N_{s2}= $2nN_p$ and N_{s3}= nN_p respectively; where $n = 1$ is considered for this design.



(a) (b)

Figure 5.1: (a) 3-D model of the four winding transformer; (b) Interleaved winding technique of the transformer for low leakage inductance



(a) (b)

Figure 5.2: (a) Prototype of the four winding transformer (b) HFT volume variation with core material and switching frequency

5.1.3 Inductance computation

Considering a pi-model of a four-winding transformer as shown in Fig. 5.3, the voltages across the four windings can be written as shown in (5.2), (5.3), (5.4) and (5.5) respectively.

$$v_1 = (L_{pa} + L_m)\dot{i_1} + L_m(n_{s1}\dot{i_2}) + L_m(n_{s2}\dot{i_3}) + L_m(n_{s3}\dot{i_4}) \tag{5.2}$$

$$\begin{aligned} v_2 = {} & L_m n_{s1}^2 \left(\frac{\dot{i_1}}{n_{s1}}\right) + (L_{la1} + L_m n_{s1}^2)\dot{i_2} \\ & + L_m n_{s1}^2 \left(\frac{n_{s2}}{n_{s1}}\dot{i_3}\right) + L_m n_{s1}^2 \left(\frac{n_{s3}}{n_{s1}}\dot{i_4}\right) \end{aligned} \tag{5.3}$$

$$v_3 = L_m n_{s2}^2 \left(\frac{\dot{i_1}}{n_{s2}}\right) + L_m n_{s2}^2 \left(\frac{n_{s1}}{n_{s2}}\dot{i_2}\right)$$
$$+(L_{la2} + L_m n_{s2}^2)\dot{i_3} + L_m n_{s2}^2 \left(\frac{n_{s3}}{n_{s2}}\dot{i_4}\right) \quad (5.4)$$

$$v_4 = L_m n_{s3}^2 \left(\frac{\dot{i_1}}{n_{s3}}\right) + L_m n_{s3}^2 \left(\frac{n_{s1}}{n_{s3}}\dot{i_2}\right)$$
$$+L_m n_{s3}^2 \left(\frac{n_{s2}}{n_{s3}}\dot{i_3}\right) + (L_{la3} + L_m n_{s3}^2)\dot{i_4} \quad (5.5)$$

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} L_{pa} + L_m & n_{s1}L_m & n_{s2}L_m & n_{s3}L_m \\ n_{s1}L_m & L_{la1} + n_{s1}^2 L_m & n_{s1}n_{s2}L_m & n_{s1}n_{s3}L_m \\ n_{s2}L_m & n_{s1}n_{s2}L_m & L_{la2} + n_{s2}^2 L_m & n_{s2}n_{s3}L_m \\ n_{s3}L_m & n_{s1}n_{s3}L_m & n_{s2}n_{s3}L_m & L_{la3} + n_{s3}^2 L_m \end{bmatrix} \begin{bmatrix} \dot{i_1} \\ \dot{i_2} \\ \dot{i_3} \\ \dot{i_4} \end{bmatrix}$$

The leakage inductances of the transformer can be derived from the inductance matrix using the approximate pi-model of the transformer. Here, n_{sk} is $\frac{N_{sk}}{N_p}$, where, k is $\{1, 2, 3\}$. The designed transformer is characterized using AP Instruments Network Analyzer 102B. The bode plots with the secondary winding terminals open-circuited and short-circuited are shown in Fig. 5.4. The open circuit measurement is done across the terminals x_1 and x_2 with all the secondary winding terminals open. The short circuit measurement is done by shorting the terminals y_1 and y_2. The inductance seen from x_1 and x_2 are $L_{pa} + L_{la1}/n_{s1}^2$. Six more measurements (shorting a terminal and recording the bode plot across another set of terminals) are done and from that the leakage inductance of all the four windings are computed. The leakage inductance values are: $L_{p1} = 0.312uH$; $L_{la1} = 0.41uH$; $L_{la2} = 0.662uH$; $L_{la3} = 1.086uH$ and the ac resistances are $R_{p1} = 22m\Omega$; $R_{la1} = 33m\Omega$; $R_{la2} = 112m\Omega$; $R_{la3} = 223m\Omega$.

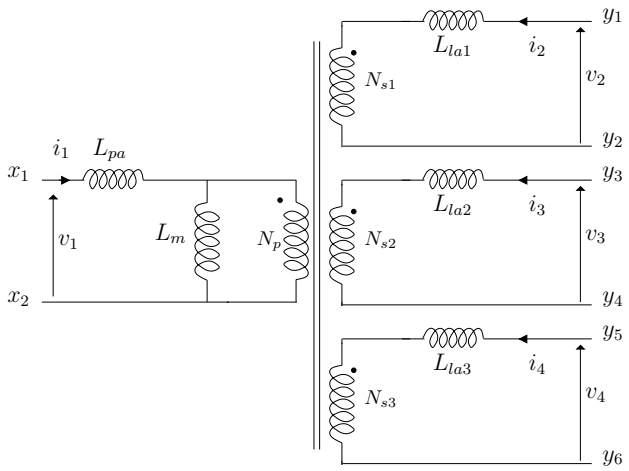


Figure 5.3: Transformer pi-model considered for extracting the various transformer parameters [94]

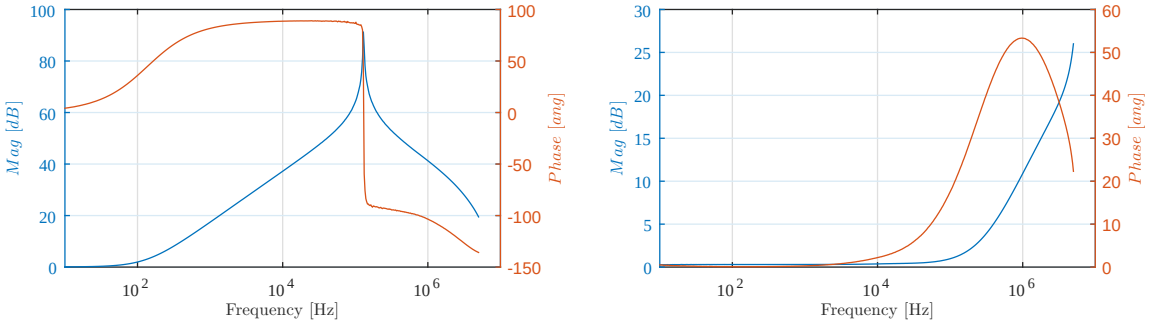


Figure 5.4: Transformer characterization using network analyzer (a) open circuit measurement as seen across x_1 x_2 terminals with all secondary terminals open; (b) measurement across primary terminals x_1 x_2 with y_1 y_2 terminals short circuited in Fig. 5.3 and y_3 y_4, y_5 y_6 terminals open.

Chapter 6

System Level Analysis of Proposed Converter Topology

6.1 Closed loop control

In this chapter, the following system level analysis of the proposed converter topology will be demonstrated.

- Closed Loop Analysis in Simulation
- Operation under Module Failure
- Filter Inductor Design

Fig. 6.1 shows a simple closed-loop controller, implemented in simulation for the power flow control. As shown in Fig. 6.2, the input voltage and the power reference change at 0.1s and 0.2s respectively. The behavior of the converter to these changes is shown in the current magnitude which increases at 0.1s to maintain the same output power and reduce at 0.2s with the reduction in active power, P. Fig. 6.3 shows the dynamic response of the converter with the change in the input voltage at 0.1s. After a short transient, the system settles at the required operating point.

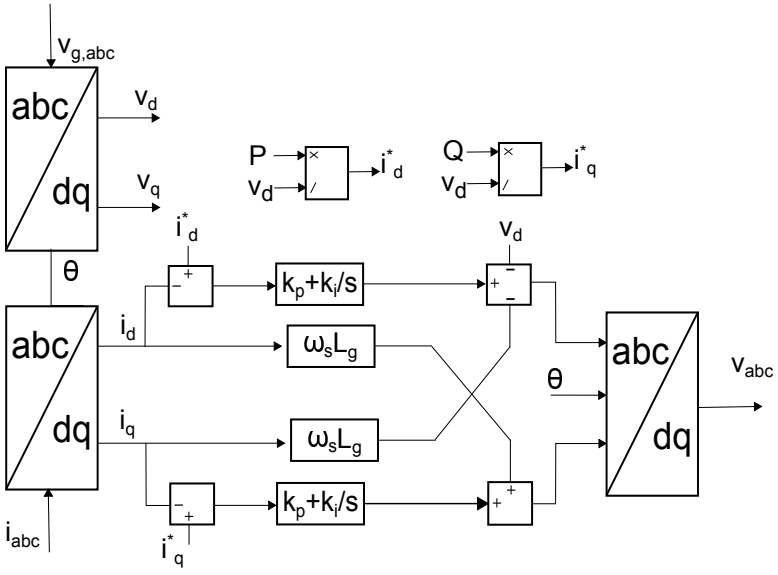


Figure 6.1: Control Model

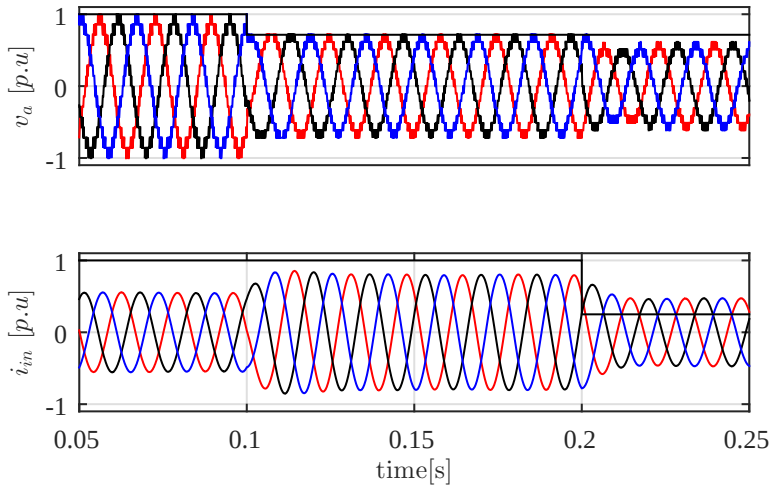


Figure 6.2: (Top) Three phase-neutral voltages and input voltage which changes at 0.1 sec, (Bottom) Three line currents along with output power command which changes at 0.2 sec

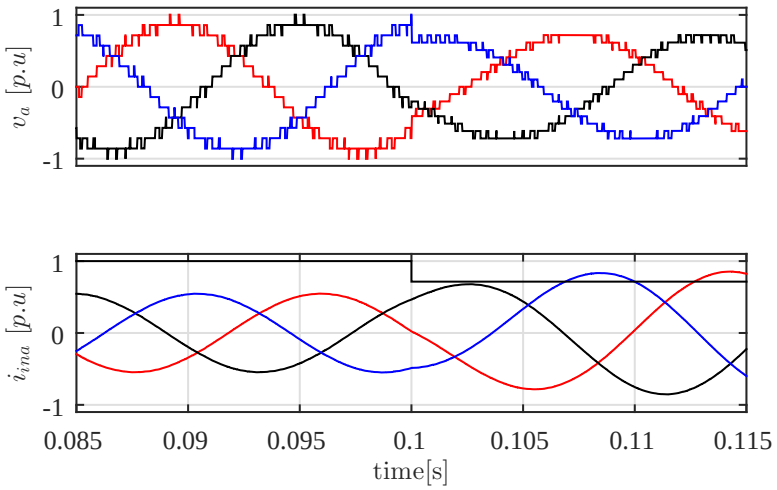


Figure 6.3: Zoomed in phase-neutral voltages and line currents at 0.1 sec which shows the dynamic behavior of the converter.

6.2 Operation under module failure

In case of a symmetrical multilevel converter, various fault-tolerant techniques have been investigated in the literature [95]. If any of the modules are faulted then a fundamental phase-shift compensation technique is used to restore balanced line currents for all three phases with reduced magnitude [96]. A set of non-linear equations as given in (6.1) are solved to generate the compensated angles between all three phases for balanced line currents. The Table in [96] outlines the angles for a eleven level inverter with five symmetrical modules in each phase. The fundamental phase-shift compensation (FPSC) technique is often used because of the easy implementation. However, the technique has some disadvantages as shown in [96]. For an asymmetrical converter, [97] shows a reconfiguration technique by using additional bi-directional switches in case of faults.

$$V_a^2 + V_b^2 - 2V_aV_bcos\alpha = V_b^2 + V_c^2 - 2V_bV_ccos\beta = V_c^2 + V_a^2 - 2V_cV_acos\gamma \tag{6.1}$$

$$\alpha + \beta + \gamma = 2\pi \tag{6.2}$$

The above FPSC technique has been investigated on the proposed topology. The angles can be computed using (6.1) for all cases. Fig. 6.4, 6.5 and 6.6 respectively show the phase, line voltages and the line currents for an unfaulted case.

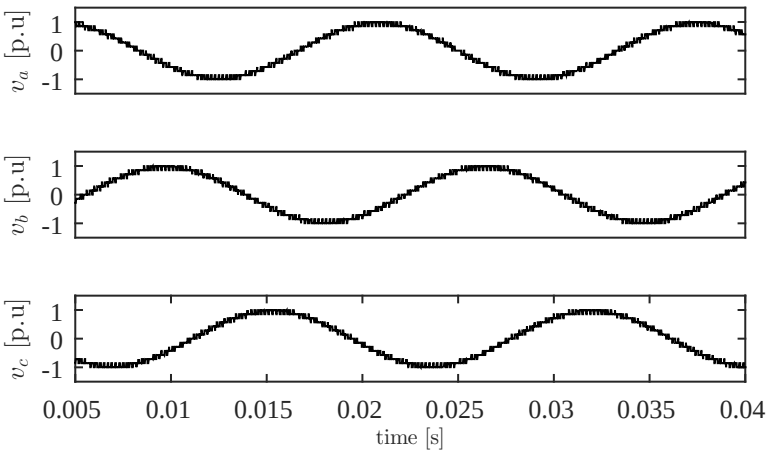


Figure 6.4: Three phase voltages for unfaulted case

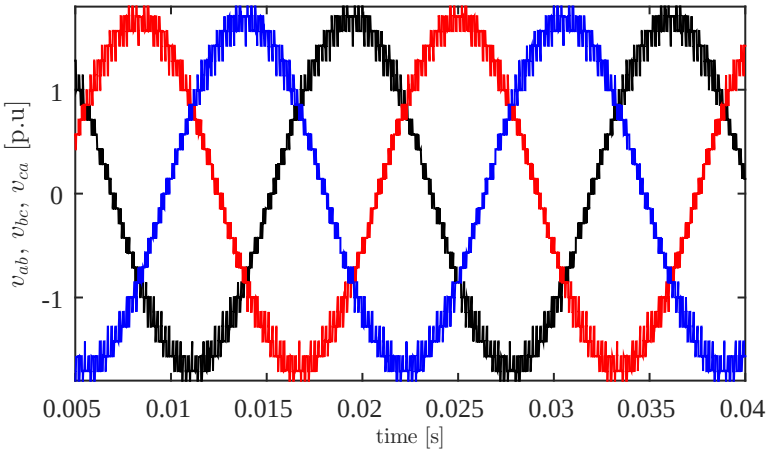


Figure 6.5: Three line-line voltages for unfaulted case

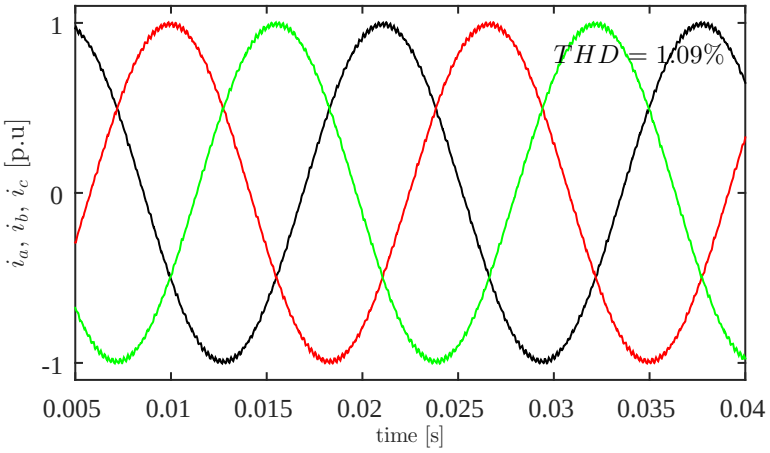


Figure 6.6: Three line currents for unfaulted case

Fig. 6.7, 6.8 and 6.9 show the same for two modules, $4nV_{in}$ and $2nV_{in}$ failed for phase- c

and all modules healthy in the remaining phases. It can be seen from Fig. 6.7 that although v_c has only three levels due to only one module being healthy, using (6.1), as the angles are different from $\frac{2\pi}{3}$, the line voltages and currents as shown in Fig. 6.8 and 6.9 respectively are balanced with reduced magnitude.

Table 6.1: Solution with reduced balanced currents for some fault cases

Phase- a	Phase- b	Phase- c	Possible Solution (in degrees)
4, 2, 1	4, 2, 1	4, ~~2~~, ~~1~~	✓$\{7, 7, 4\}$ $(\alpha = 93.5; \beta = 133; \gamma = 133.5)$
4, 2, 1	4, 2, 1	~~4~~, 2, 1	✓$\{7, 7, 3\}$ $(\alpha = 85; \beta = 137; \gamma = 138)$
4, 2, 1	4, 2, 1	~~4~~, ~~2~~, 1	✓$\{7, 7, 1\}$ $(\alpha = 68.5; \beta = 145; \gamma = 146.5)$
~~4~~, 2, 1	~~4~~, 2, 1	~~4~~, ~~2~~, 1	✓$\{3, 3, 1\}$ $(\alpha = 79.5; \beta = 140; \gamma = 140.5)$

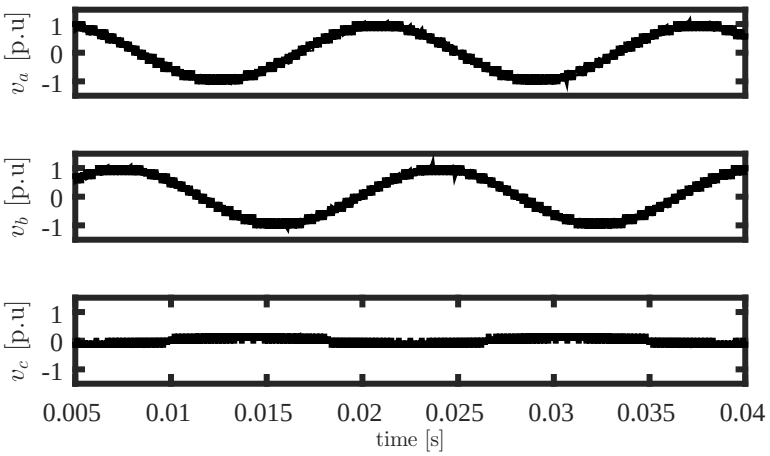


Figure 6.7: Modules $4nV_{in}$ and $2nV_{in}$ faulted in phase- c and all modules healthy in the remaining phases: Three phase voltages

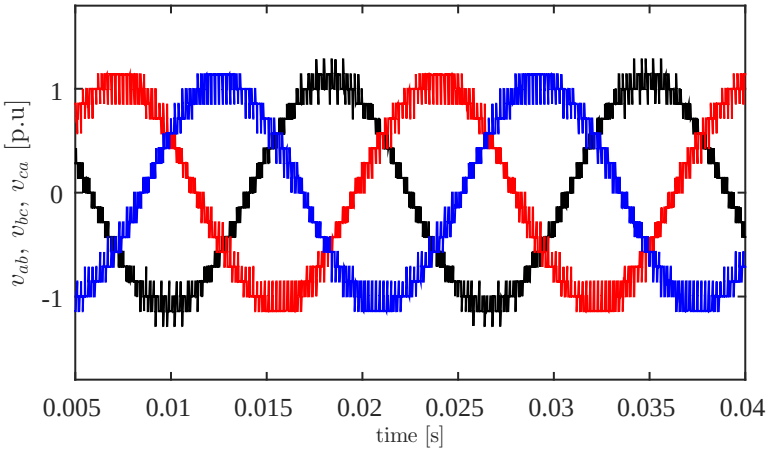


Figure 6.8: Modules $4nV_{in}$ and $2nV_{in}$ faulted in phase- c and all modules healthy in the remaining phases: Three line-line voltages

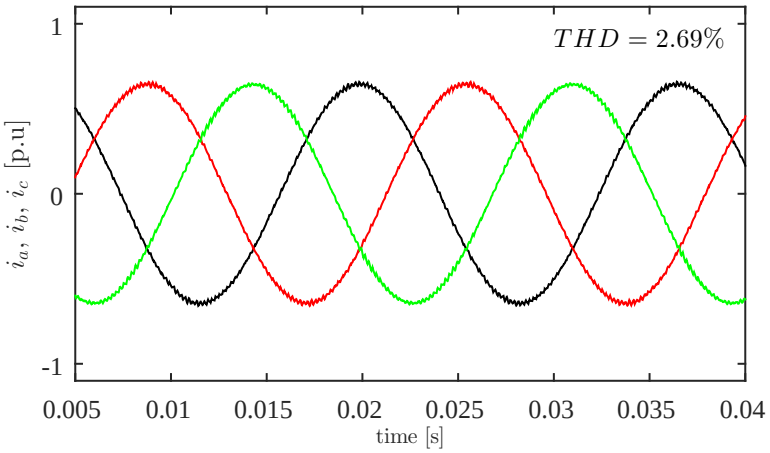


Figure 6.9: Modules $4nV_{in}$ and $2nV_{in}$ faulted in phase- c and all modules healthy in the remaining phases: Three line currents

It is to be noted that, for a fault in $2nV_{in}$ and nV_{in} modules in phase-c and all modules healthy in remaining two phases, the angles computed using (6.1), will restore balanced currents with a higher per unit value in comparison to the above case even though phase-c has three voltage levels similar to Fig. 6.7. This is because, on this occasion, module $4nV_{in}$ is healthy and hence, the average voltage generated is higher. The per unit value of line current increases as shown in Fig. 6.12 in comparison to Fig. 6.9.

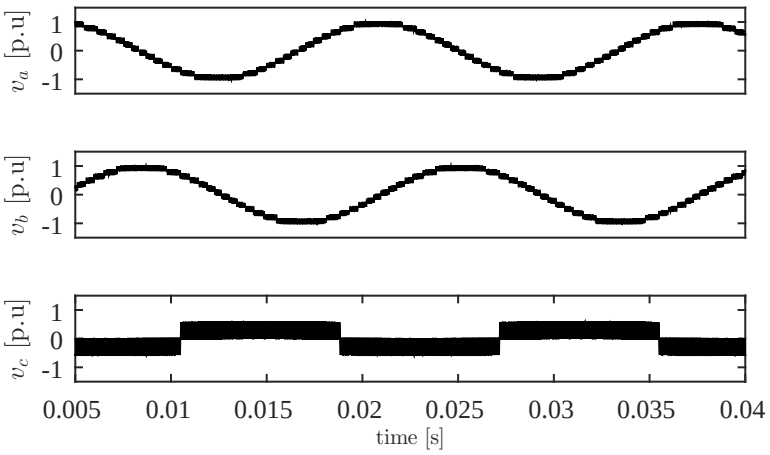


Figure 6.10: Modules $2nV_{in}$ and nV_{in} faulted in phase- c and all modules healthy in the remaining phases: Three phase voltages

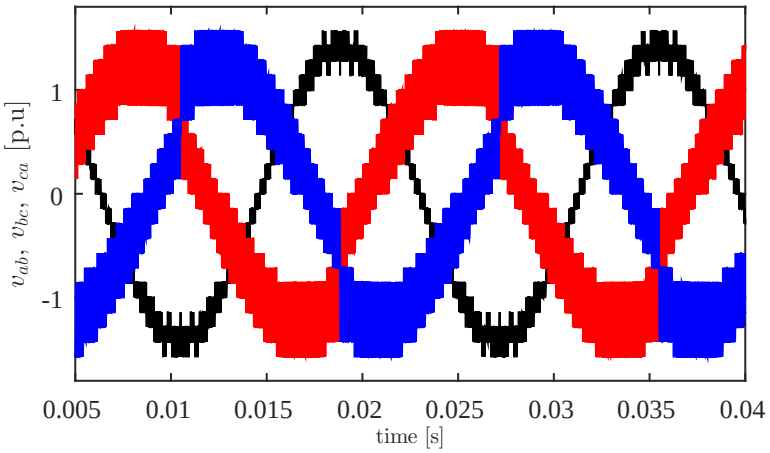


Figure 6.11: Modules $2nV_{in}$ and nV_{in} faulted in phase- c and all modules healthy in the remaining phases: Three line-line voltages

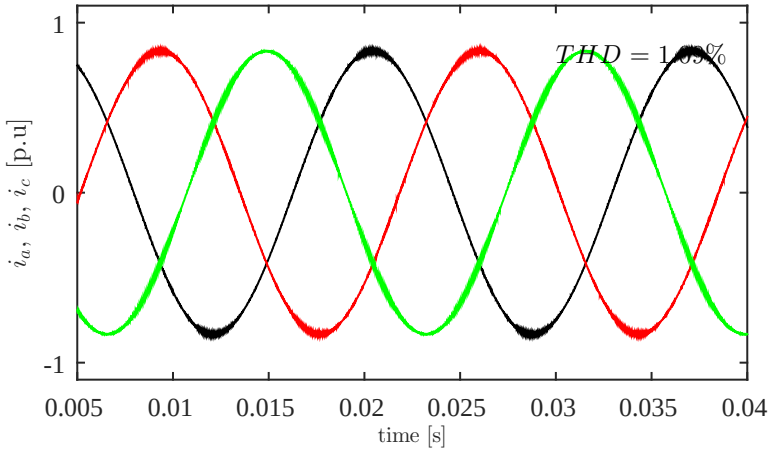


Figure 6.12: Modules $2nV_{in}$ and nV_{in} faulted in phase- c and all modules healthy in the remaining phases: Three line currents

Table 6.1, provides a manner to restore balanced currents in all three phases in case of faulted modules for some cases. For the other cases, by solving (6.1) the appropriate angles can be computed. $4, 2, 1$ indicates the three asymmetrical modules in phase- a. $\{7, 7, 3\}$ indicates the number of positive levels that can be achieved. The tick mark indicates that the fundamental phase shift compensation technique applied to symmetrical configuration is valid and the corresponding angles are computed using (6.1) and provided in the Table 6.1. For other cases, not shown in Table 6.1, but shown in [96], healthy modules of certain phases are either connected to a lower healthy module or are disconnected to restore balanced currents.

6.3 Filter inductor design

6.3.1 Design procedure

Consider a three phase system with power P, the phase-to-neutral output voltage is v_a, and the switching frequency is f_s. The ripple current is 5% of the load current, I_a. The ripple current is inversely proportional to the filter inductance, L and the switching frequency, f_s. For the same ripple current, increasing the switching frequency will reduce the filter inductance, L.

In case of an ungapped core, the relative permeability of the material will reduce with increase in the output current, I_a and hence, the design of the inductor should be such that at the rated output current, I_a, the inductance is equal to L. To design a filter inductor with inductance, L the following procedure is followed:

- From a set of available cores (toroidal, U-core, EE-core) having different relative permeability, μ_r, determine the cross-sectional area, A_c and the magnetic path length,

l_m of the core.

- Compute the number of turns, N using the relation,

$$N = \sqrt{\frac{L_{start} l_m}{\mu_0 \mu_r A_c}} \tag{6.3}$$

where, L_{start} is an initial inductance value chosen.

- Compute the magnetomotive force, H_{pk} at the maximum load current, $\hat{I}_a$ using,

$$H_{pk} = \frac{N \hat{I}_a}{l_m} \tag{6.4}$$

where, $\hat{I}_a = \sqrt{2} I_a$.

- Compute the relative permeability, $\mu_{r_{pk}}$ at this value of H_{pk}. Depending on the core manufacturer, either the variation of $\mu_{r_{pk}}$ versus H_{pk} will have a curve fitting relation [98, 99] or the value should be estimated from the permeability versus DC bias curve itself [100].

- Estimate the inductance from the computed $\mu_{r_{pk}}$, using the relation below:

$$L_{comp} = \frac{N^2 \mu_0 \mu_{r_{pk}} A_c}{l_m} \tag{6.5}$$

The computed inductance, L_{comp} will be the inductance at the rated current. If this inductance, $L_{comp} < L$, chose a larger core and increase L_{start} until L_{comp}=L.

6.3.2 Comparison of filter size for two modulation strategies

The converter has the dominant voltage harmonic at the sidebands of the switching frequency if modulated using modified uni-polar technique.

However, using the modified hybrid modulation technique shifts the dominant voltage harmonic to the sidebands of multiples of twice the switching frequency, hence the size of grid filter inductance reduces. As mentioned earlier, in case of this modulation technique, even though the switching frequency is f_s, the first dominant harmonic is at $2f_s$. Hence, for the same ripple current the frequency is double resulting in $L_{new} = L/2$. If the above procedure is followed, L_{comp}=$L/2$ which will result in a smaller core and hence a more compact grid filter inductor.

Chapter 7

Hardware Setup and Experimental Results

7.1 Hardware setup

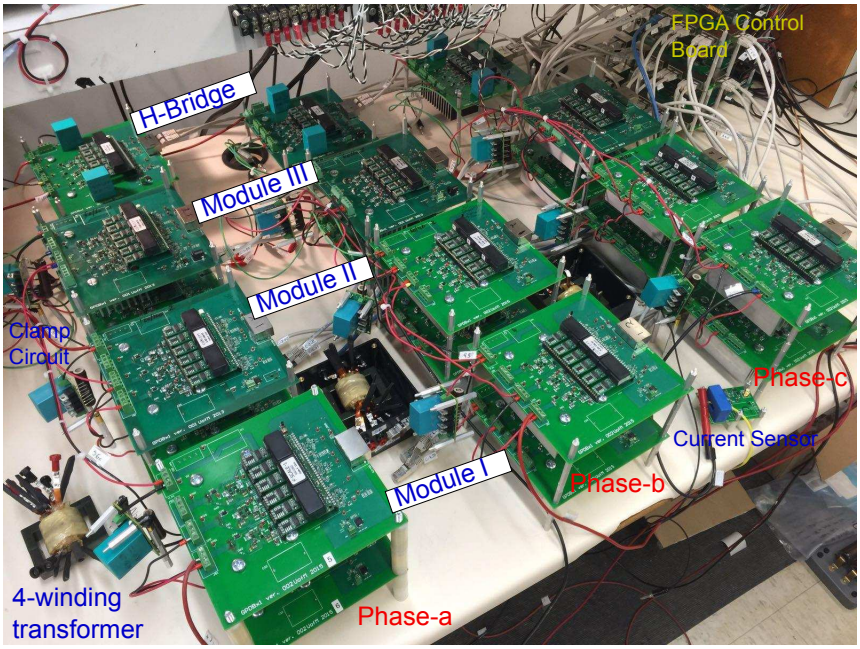


Figure 7.1: Hardware prototype of three-phase isolated asymmetrical multilevel converter

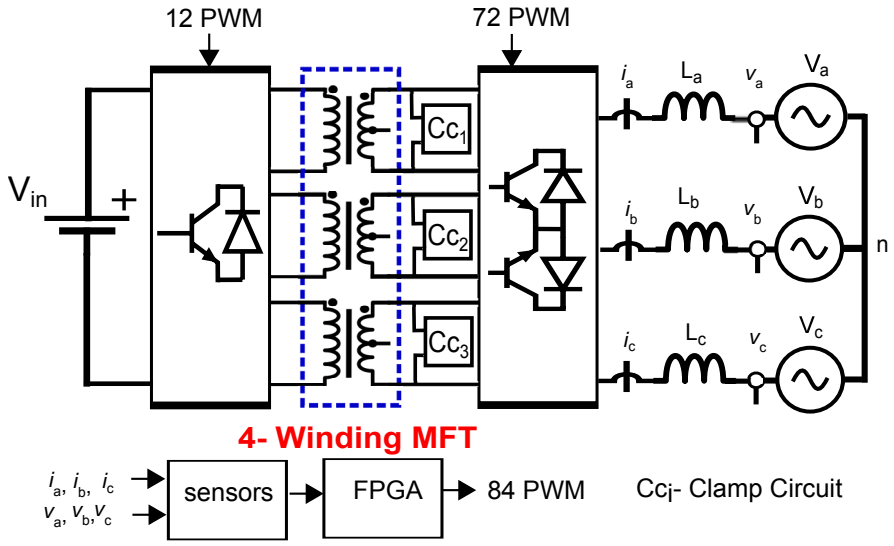


Figure 7.2: Experimental Setup of proposed multilevel converter topology to Interface low voltage DC with three-phase grid

The proposed topology is simulated using MATLAB/Simulink and experimentally verified on a scaled down fifteen level three-phase laboratory prototype as shown in Fig. 7.1. Fig. 7.2 shows the hardware setup used to validate the proposed topology experimentally. Agilent 6575A is used as the input dc supply, V_{in}. The power modules from Microsemi (APTGL120TA120TPG) are used to design each of the three full-bridges for the three-phases connected in parallel on the primary side. A total of 12 PWM signals are required for the three full-bridge modules. Three high-frequency transformers, one for each phase are designed as explained in the previous section. The power modules from Microsemi (APTGT50TDU60PG and APTGF50TDU120PG) are used to design the secondary side AC-AC converter module with bi-directional switches (two anti-parallel IGBTs connected in a common emitter configuration). Two power modules are used to design one AC-AC converter module. One module is for the two bi-directional switches in the top leg, (for example in Fig. 2.4, S_{1a} and S_{2a} in Module I are designed using one Microsemi module) and the other module is for the bottom leg switches (S_{3a} and S_{4a}). The Module III with the lowest voltage (nV_{in}) in Fig. 7.1 is designed using two APTGT50TDU60PG power modules, whereas, Modules I and II ($4nV_{in}$ and $2nV_{in}$ respectively) are designed using two APTGF50TDU120PG for each AC-AC converter module. All the three modules are connected in series on the output side. Similarly for phase, b and c, one full-bridge and three AC-AC converter modules are designed as shown in Fig. 7.1. 72 PWM signals are required for the secondary side switches forming the three-phase system. An FPGA-based control platform (Xilinx, XC3S500E) has been used to generate the PWM signals. For leakage commutation, a clamp circuit for each converter module was designed using four SiC schottky

diodes (C4D05120A) in a full-bridge configuration having zero reverse recovery current and faster switching. Three LEM current sensors, one for each phase is used to aid in four-step commutation. Three LEM voltage sensors are used to sense the AC grid voltage so that the converter output voltages are generated at a phase shift angle, δ with respect to the source voltage.

7.2 Modulation-I: Simulation and experimental results

7.2.1 Results of Glitch Compensation

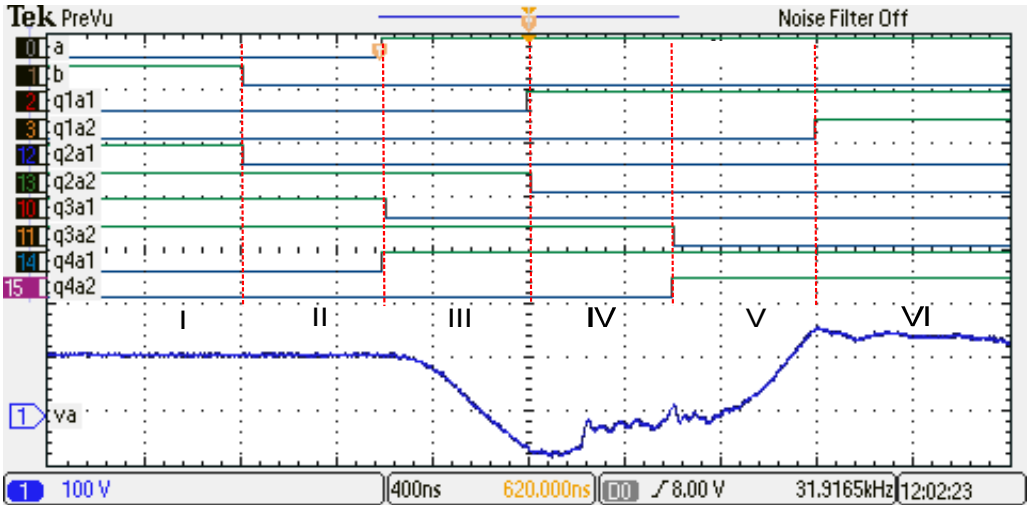


Figure 7.3: Digital signals corresponding to the six modes of operation without any compensation followed by the phase-neutral output voltage, v_a in (CH-1) [100 V/div] in 400 ns/div time scale using the experimental setup similar to the simulation results as shown in Fig. 4.1a. Each commutation interval is 600 ns

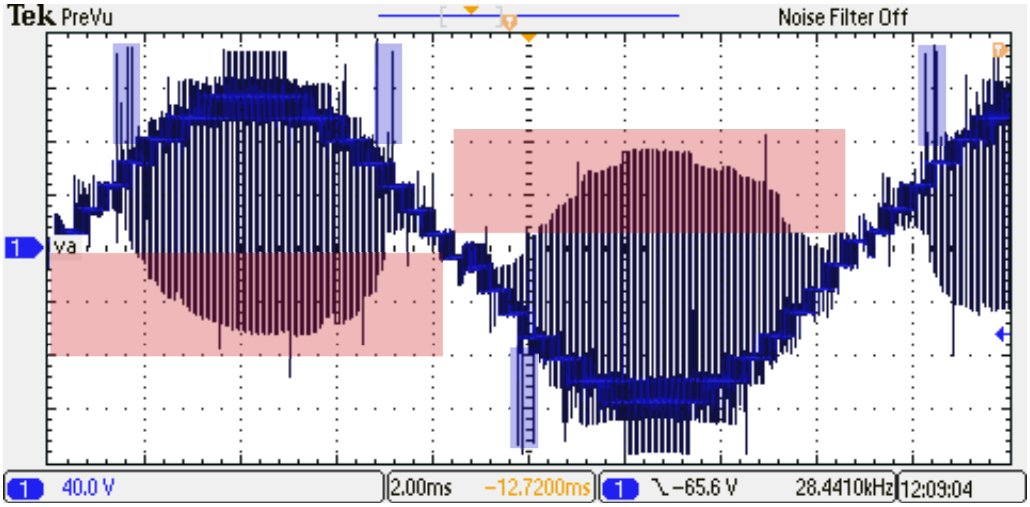


Figure 7.4: Experimental results of the fundamental cycle of phase-neutral output voltage, v_a in (CH-1) [40 V/div] in 2 ms/div time scale similar to the simulation result as shown in Fig. 4.4

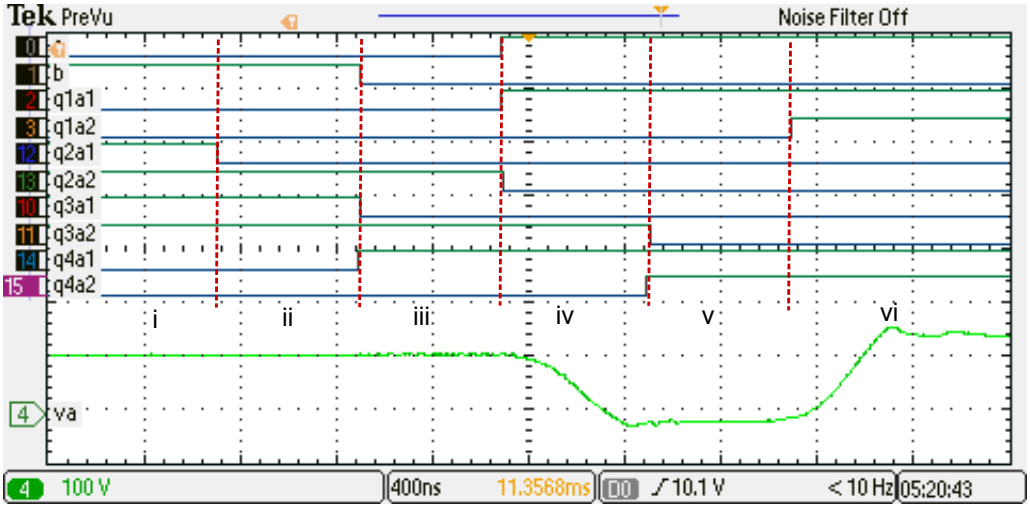


Figure 7.5: Digital signals corresponding to the six modes of operation with glitch compensation-I followed by the phase-neutral output voltage, v_a in (CH-4) [100 V/div] in 400 ns/div time scale using the experimental setup similar to the simulation results as shown in Fig. 4.1b

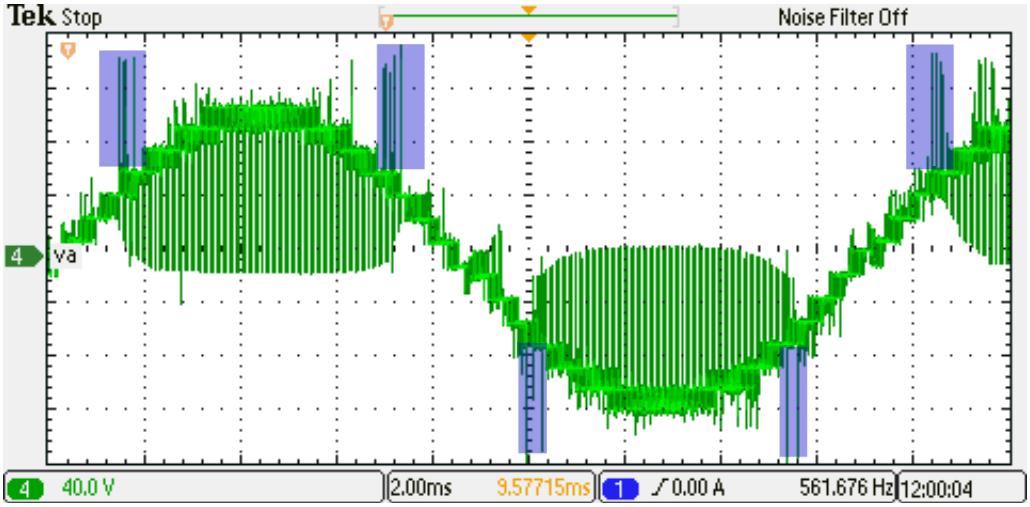


Figure 7.6: Experimental results of the fundamental cycle of phase-neutral output voltage, v_a in (CH-4) [40 V/div] in 2 ms/div time scale similar to the simulation result as shown in Fig. 4.5

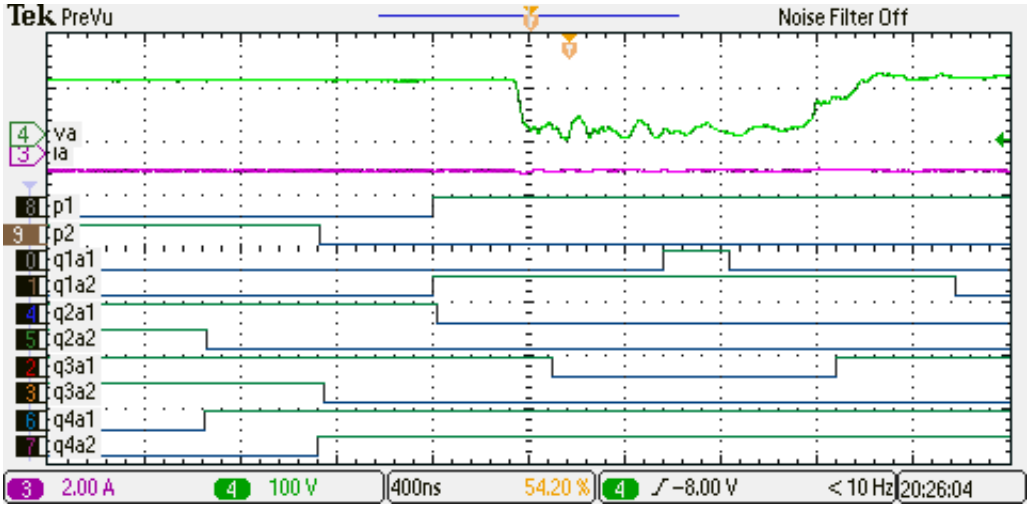


Figure 7.7: Digital signals corresponding to the six modes of operation with glitch compensation-I followed by the phase-neutral output voltage, v_a in (CH-4) [100 V/div] and i_a in (CH-3) to show the reverse power flow in 400 ns/div time scale using the experimental setup similar to the simulation results as shown in Fig. 4.1c

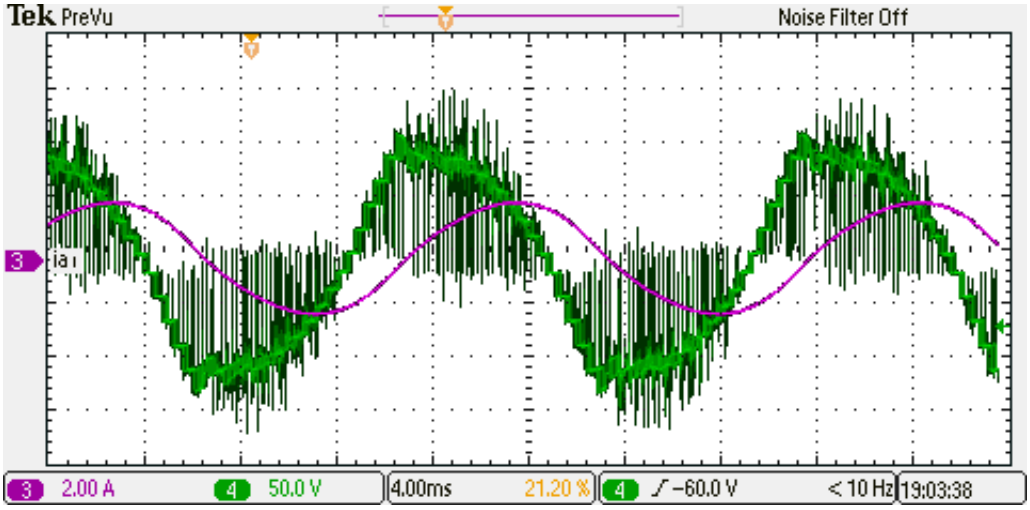


Figure 7.8: Experimental results of the fundamental cycle of phase-neutral output voltage, v_a in (CH-2) [200 V/div], current, i_a (CH-4) [1 A/div], the source voltage, v_{ga} (CH-2) [200 V/div] in 4 ms/div time scale.

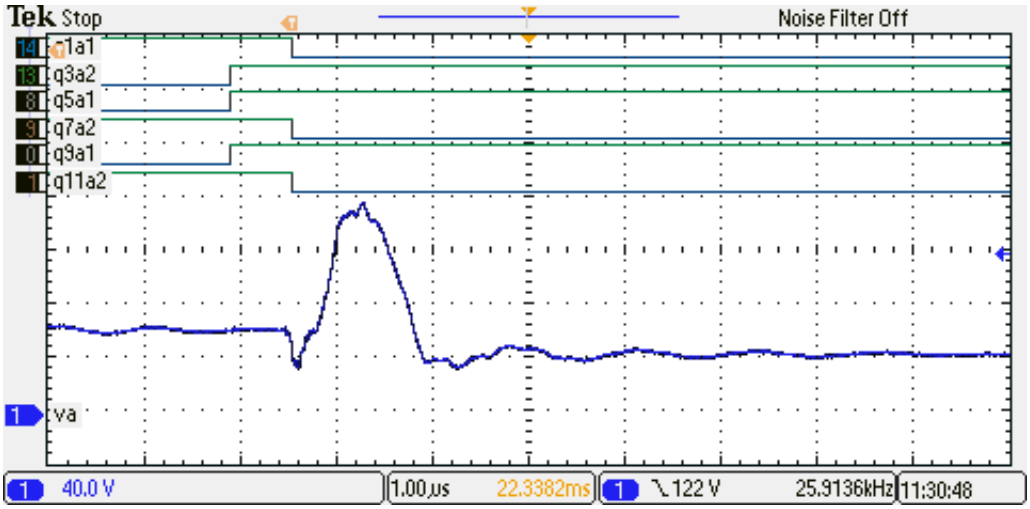


Figure 7.9: Digital signals corresponding to the left leg bi-directional switches of all three AC-AC converter modules followed by the phase-neutral output voltage, v_a in (CH-1) [40 V/div] in 1 μs/div time scale using the experimental setup: without glitch compensation-II similar to the simulation results as shown in Fig. 4.10b

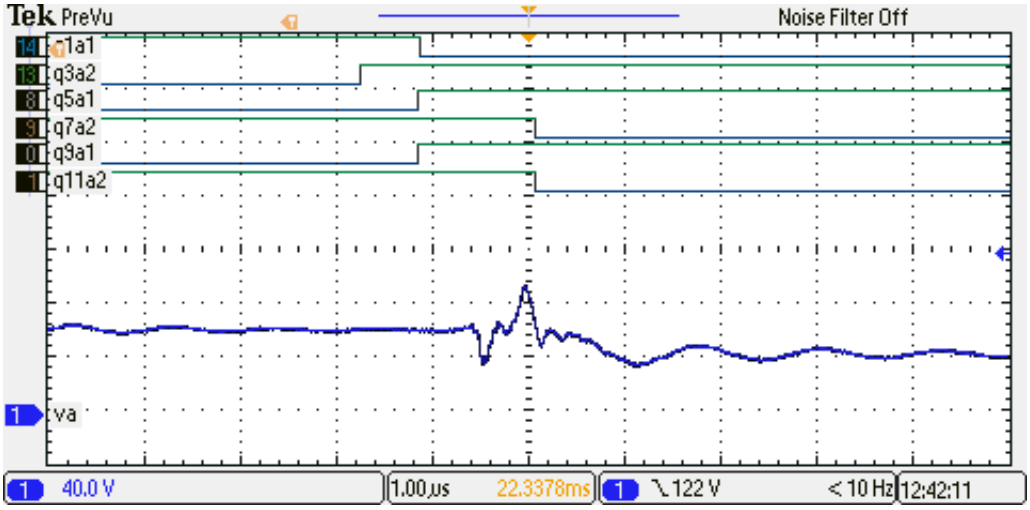


Figure 7.10: Digital signals corresponding to the left leg bi-directional switches of all three AC-AC converter modules followed by the phase-neutral output voltage, v_a in (CH-1) [40 V/div] in 1 μs/div time scale using the experimental setup: with glitch compensation-II similar to the simulation results as shown in Fig. 4.10c

The first set of experimental results correspond to the output voltage profile with and without the various glitch compensation techniques as proposed in the modulation and commutation section. Fig. 7.3 shows the digital signals of the primary side switches and all the bi-directional switches of Module I corresponding to the six modes of operation as explained using Fig. 4.2 and Fig. 4.1a. As shown in Fig. 7.3, a voltage reversal is generated in mode *II* and zero voltage in mode *III* similar to the description in the non-ideal modulation section. Fig. 7.4 shows the output voltage, which is similar to the fundamental cycle of output voltage as shown in Fig. 4.4. Fig. 7.5 shows the digital signals of the primary side switches which are delayed by a commutation interval and all the bi-directional switches of Module I corresponding to the six modes of operation as explained using Fig. 4.3 and Fig. 4.1b. As shown in Fig. 7.5 the output voltage generates zero voltage in mode *iii* similar to the description in the glitch compensation- *I* section and does not generate a voltage reversal in mode *ii*. Fig. 7.6 shows the output voltage, which is similar to the fundamental cycle of output voltage as shown in Fig. 4.5. Fig. 7.7 shows the digital signals of the primary side switches which are delayed by a commutation interval and the bi-directional switches of left lef of Module I corresponding to the six modes of operation as explained using Fig. 4.8 and Fig. 4.1c. As shown in Fig. 7.7 the output voltage generates zero voltage in two modes similar to the description above rather than only in mode *iii* for the case of postive power flow from DC to three-phase grid. The reverse power flow, even though it has the same ideal signal generation due to the forced commutation generates a zero voltage for two commutation intervals as shown in Fig. 4.1c. However, the glitches

due to the interdependence of the three AC-AC converter modules are still not resolved (highlighted by the blue patches in Fig. 7.6) as explained in non-ideal modulation section. Fig. 7.9 shows the digital signals corresponding to the bi-directional switches in the left leg of all the three AC-AC converter modules in phase-a, followed by the output voltage, v_a. As shown in the Fig. 7.9, the output voltage, v_a has a glitch similar to Fig. 4.10b. With the glitch compensation- *II* implemented, as shown in Fig. 7.10, the rising edge of the signals, q_{5a1} and q_{9a1} are delayed to match with the falling edge of the signal, q_{1a1}. Also, the corresponding switch signals, q_{7a2} and q_{11a2} of Modules II and III are also delayed. This modification results in the mitigation of the glitch in the output voltage, v_a, similar to the simulation results as shown in Fig. 4.10c.

7.2.2 Results for a three-phase system

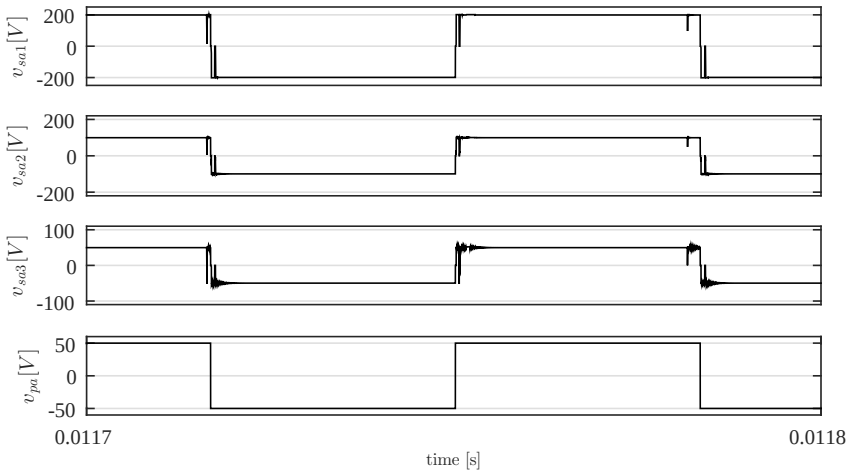


Figure 7.11: Simulated transformer link voltage across the three series connected modules, v_{sa1} in (CH-2) [200 V/div], v_{sa2} in (CH-3) [200 V/div] and v_{sa3} in (CH-4) [100 V/div] followed by the primary side link voltage, v_{pa} in (CH-1) [50 V/div] in 10 μs/div time scale.

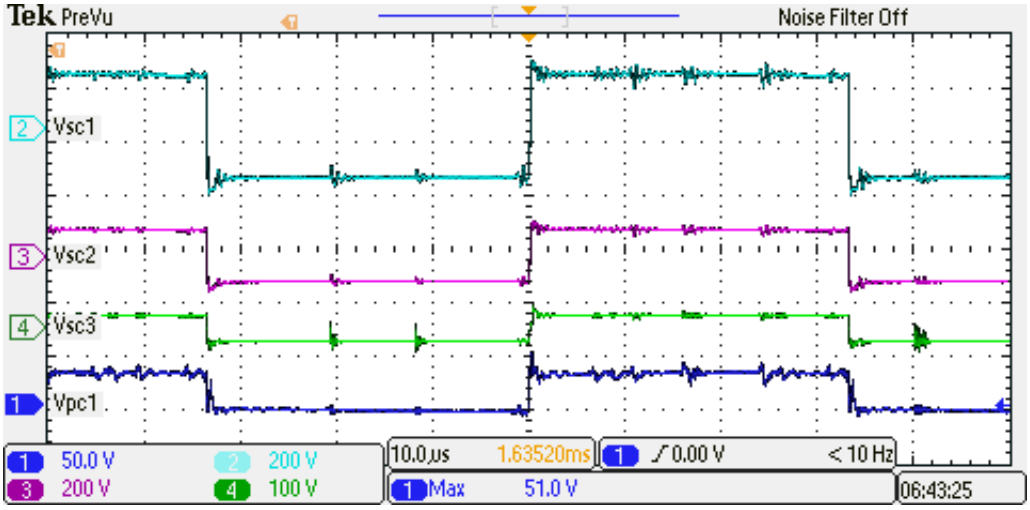


Figure 7.12: Experimental transformer link voltage across the three series connected modules, v_{sa1} in (CH-2) [200 V/div], v_{sa2} in (CH-3) [200 V/div] and v_{sa3} in (CH-4) [100 V/div] followed by the primary side link voltage, v_{pa} in (CH-1) [50 V/div] in 10 μs/div time scale.

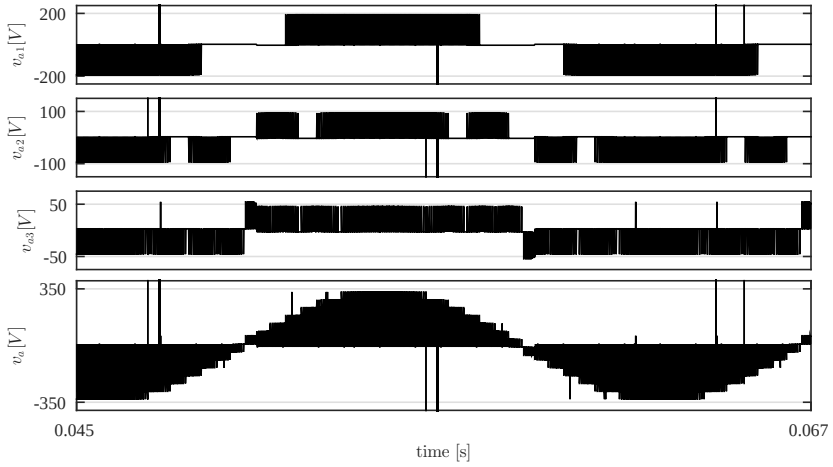


Figure 7.13: Simulated module output voltage of the three series connected modules, v_{a1} in (CH-1) [200 V/div], v_{a2} in (CH-2) [100 V/div] and v_{a3} in (CH-3) [1000 V/div] followed by the phase-neutral output voltage, v_a (CH-4) [200 V/div] in 2 ms/div time scale.

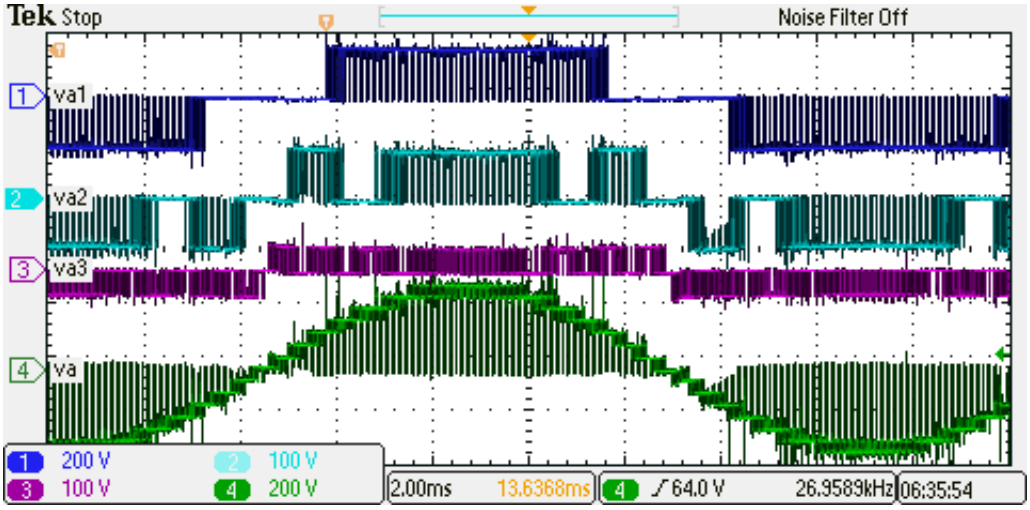


Figure 7.14: Experimental module output voltage of the three series connected modules, v_{a1} in (CH-1) [200 V/div], v_{a2} in (CH-2) [100 V/div] and v_{a3} in (CH-3) [1000 V/div] followed by the phase-neutral output voltage, v_a (CH-4) [200 V/div] in 2 ms/div time scale.

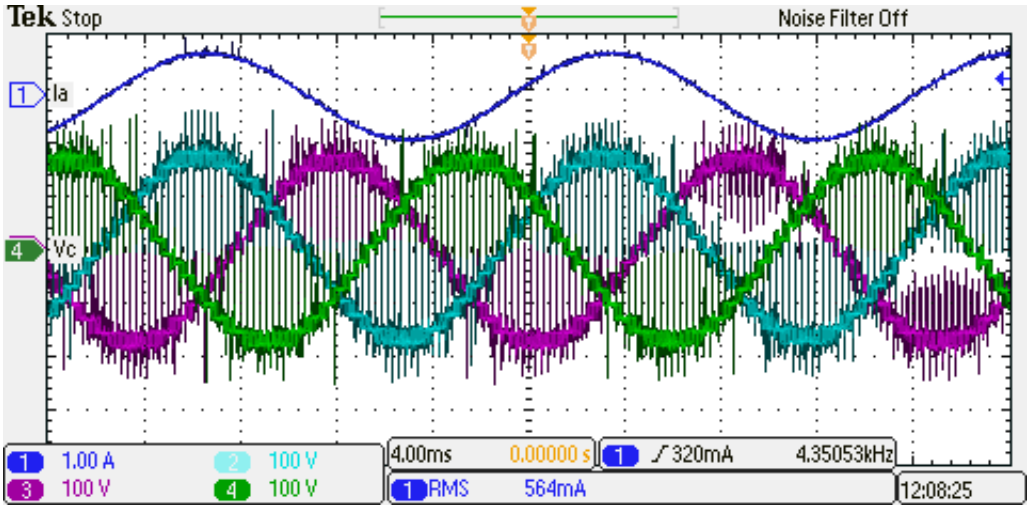


Figure 7.15: Experimental line current (CH-1) [1 A/div] along with the phase-neutral output voltage of all three-phases, v_a (CH-2), v_b (CH-3) and v_c (CH-4) [100 V/div] in 4 ms/div time scale.

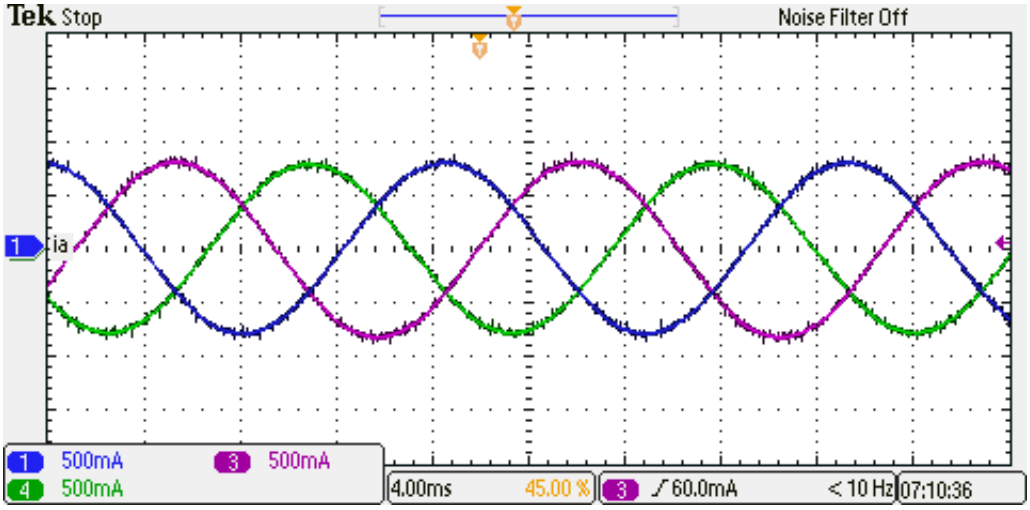


Figure 7.16: Experimental currents of all three-phases, i_a (CH-1), i_b (CH-3) and i_c (CH-4) [0.5 A/div] in 4 ms/div time scale.

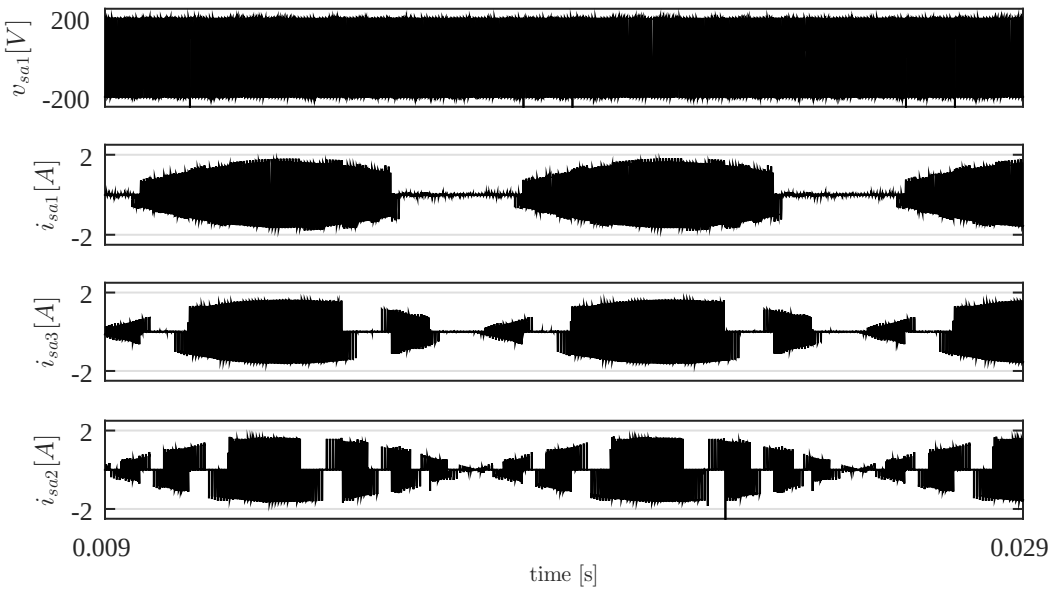


Figure 7.17: Simulated transformer link voltage, v_{sa1} in (CH-1) [400 V/div] followed by the transformer link currents through the three secondary windings, i_{sa1} in (CH-2) [2 A/div], i_{sa2} in (CH-3) [2 A/div] and i_{sa3} in (CH-4) [2 A/div] in 2 ms/div time scale.

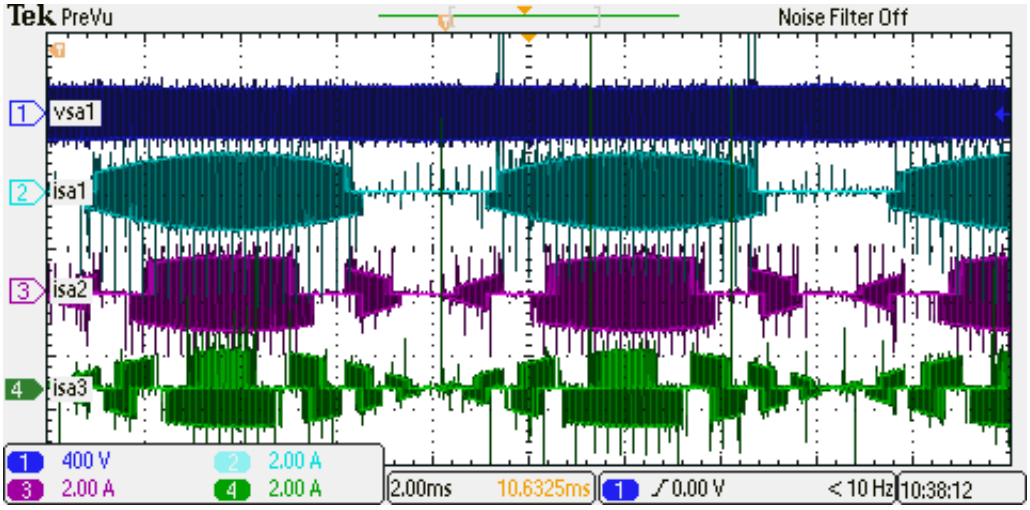


Figure 7.18: Experimental transformer link voltage, v_{sa1} in (CH-1) [400 V/div] followed by the transformer link currents through the three secondary windings, i_{sa1} in (CH-2) [2 A/div], i_{sa2} in (CH-3) [2 A/div] and i_{sa3} in (CH-4) [2 A/div] in 2 ms/div time scale.

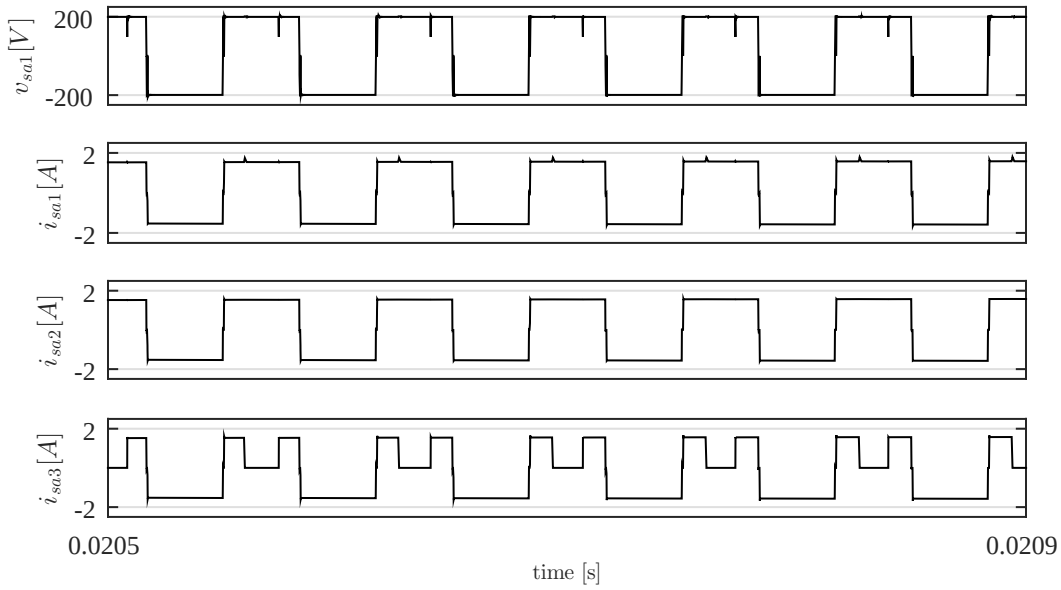


Figure 7.19: Simulated transformer link voltage, v_{sa1} in (CH-1) [400 V/div] followed by the transformer link currents through the three secondary windings, i_{sa1} in (CH-2) [2 A/div], i_{sa2} in (CH-3) [2 A/div] and i_{sa3} in (CH-4) [2 A/div] in 40 μs/div time scale.

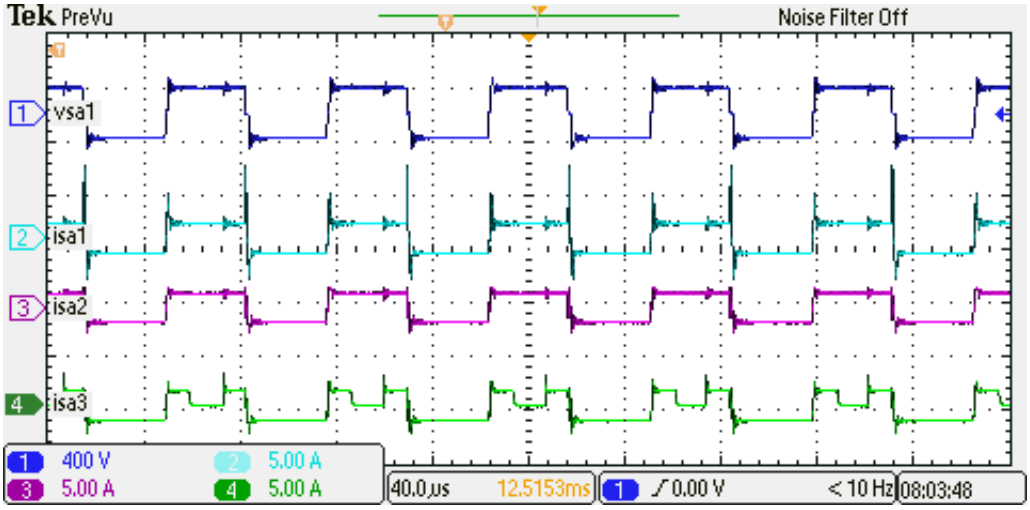


Figure 7.20: Experimental transformer link voltage, v_{sa1} in (CH-1) [400 V/div] followed by the transformer link currents through the three secondary windings, i_{sa1} in (CH-2) [2 A/div], i_{sa2} in (CH-3) [2 A/div] and i_{sa3} in (CH-4) [2 A/div] in 40 μs/div time scale.

The simulation and experimental results of the transformer link voltages across the primary and three secondary windings are shown in Fig. 7.11 and Fig. 7.12 respectively. The complimentary switching of the input side full-bridge at 15kHz with a dead-time of 600ns generates the primary side link voltage, v_{pa}. As shown in those figures, for an input voltage, V_{in} of 50V; the transformer secondary side link voltages (v_{sa1}: v_{sa2}: v_{sa3}) are 200V, 100V and 50V in a ratio of (4:2:1). Fig. 7.13 and Fig. 7.14 show the simulation and experimental results of the output voltages across each module, v_{sa1}, v_{sa2} and v_{sa3} followed by the total phase-neutral output voltage, v_a. The differences in the magnitude of the output voltage between simulation and experimental results, is primarily due to the device drop across each switch which is not considered in the simulation model. As shown in the figures, all the modules generate a zero voltage during the dead-time of primary side full-bridge. Also, the top module is used to generate the top four output voltage levels and freewheels the output current for the remaining three levels. Fig. 7.15 shows the line current, i_a followed by the phase-neutral output voltage of all three-phases, v_a, v_b and v_c. As explained earlier, in all three-phases, the output voltage goes to zero when the link voltage switches. Fig. 7.16 shows the line currents of the three-phase system.

Fig. 7.17 and Fig. 7.18 shows the link voltage and three link currents through the transformer secondary windings. The link current, i_{sa1} is zero at some intervals in a fundamental cycle. This is because as explained above, for generating the lower output voltage levels, Module I will freewheel the output current and hence, the link current, i_{sa1} through the transformer winding is zero. Similarly, the current through the other secondary winding will be zero whenever Module II freewheels the current. Figs. 7.19 and 7.20 shows the

same above plots on a 40 μs/div timescale. The link currents, i_{sa1} and i_{sa2} follow the link voltage, v_{sa1}, but, as Module I switches even though the link voltage is constant, the link current, i_{sa3} also switches.

7.2.3 Results for bi-directional power flow

$$P = 3\frac{v_{a1}v_{ga}}{X_l}sin\delta \tag{7.1}$$

$$m_a = \frac{\hat{V}_{a,1}}{7nV_{in}} \tag{7.2}$$

The mathematical relation for the power transmission and the voltage conversion are given in (7.1) and (7.2) respectively. Here, X_l=2πfsL and $\hat{V}_{a,1}$ is the peak value of the fundamental output voltage.

The line-line rms voltage of the supply is 130V, and v_a, the converter output voltage is generated at a specific angle of, δ $\pm$0.25rad with respect to the source voltage, v_{ga}. The series inductor, L_a, of approximate value is used to limit the power flow. The resulting output current i_a, output voltage, v_a for the power flow in either direction are shown in Figs. 7.21 and 7.22. The harmonic spectrum of the multilevel output voltage, v_a is shown in Fig. 7.23. The high number of levels results in a THD of 18% and the dominant harmonics are at the multiples of switching frequency. This allows to achieve low output current THD of less than 5%, with the harmonic spectrum as shown in Fig. 7.24 and hence a high power quality.

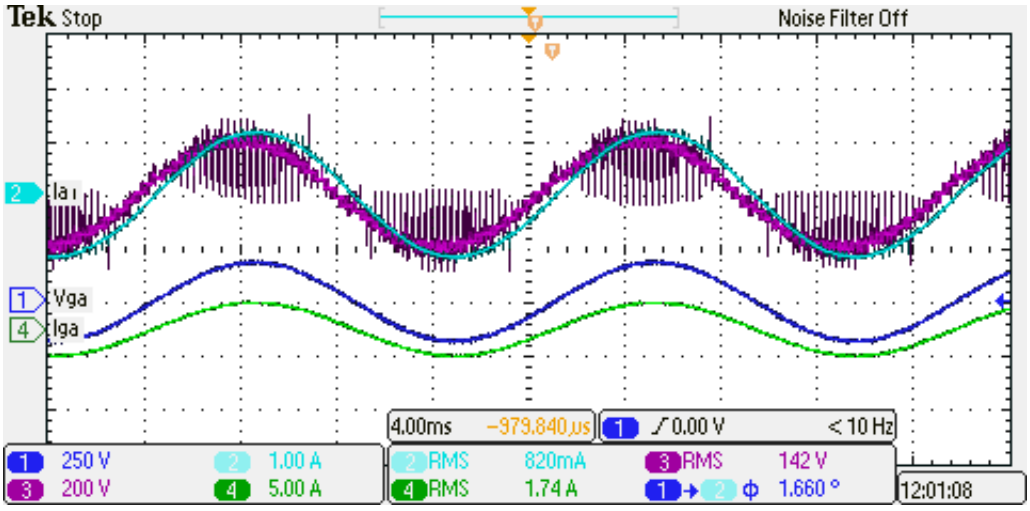


Figure 7.21: Experimental result of the converter output voltage, v_a, (CH-3) [200 V/div], current, i_a (CH-2) [1 A/div], the source voltage, v_{ga} (CH-1) [250 V/div] and source current [5 A/div] in 4 ms/div time scale

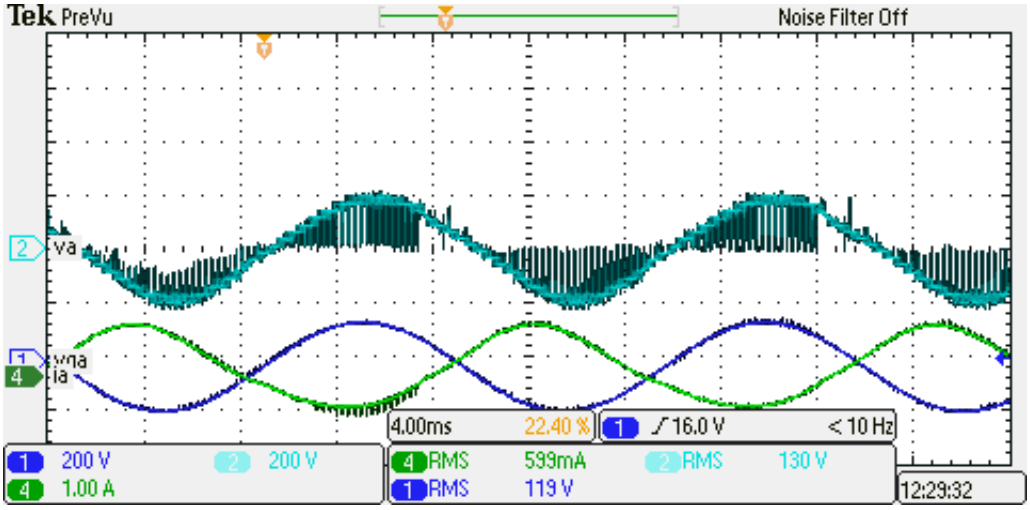


Figure 7.22: Experimental result of the converter output voltage, v_a, (CH-3) [200 V/div], current, i_a (CH-2) [1 A/div], the source voltage, v_{ga} (CH-1) [250 V/div] and source current [5 A/div] in 4 ms/div time scale.

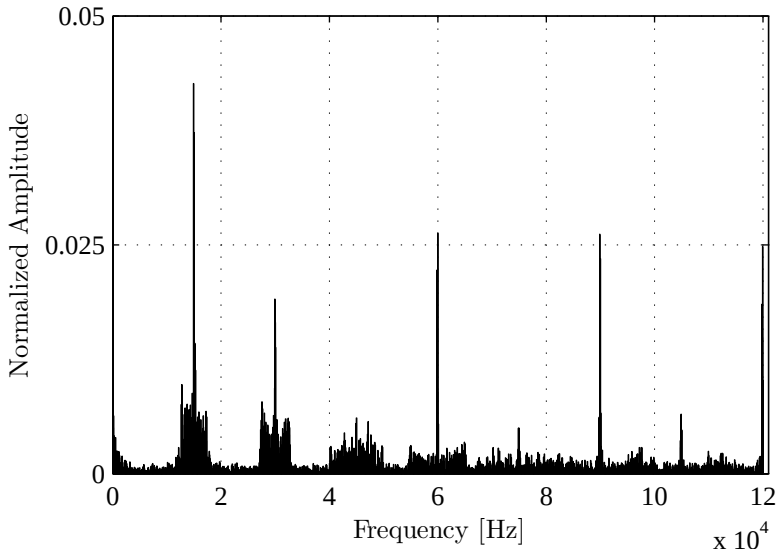


Figure 7.23: Harmonic spectrum of output phase voltage, v_a: Modulation-I

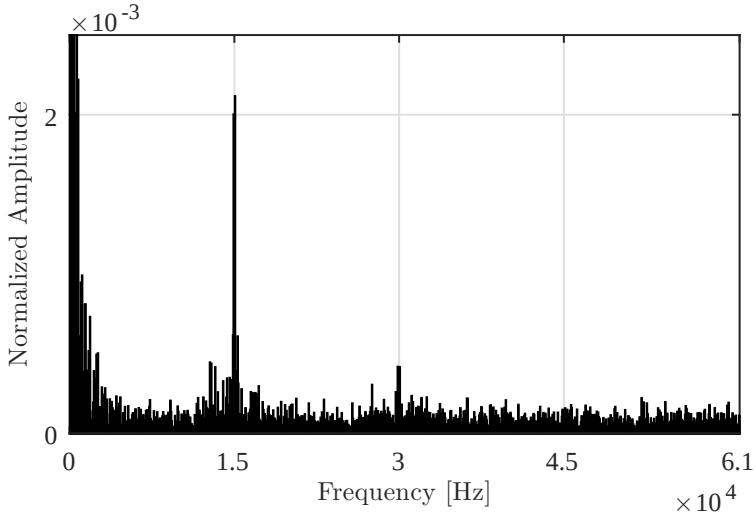


Figure 7.24: Harmonic spectrum of the output current, i_a with a THD of 2.5%.

7.2.4 Results for operation under module failure

A particular scenario is considered in which in phase-a and b, $4nV_{in}$ modules are faulted and in phase- c, nV_{in} module is faulted. Fig. 7.25 shows the output voltage and current for both the unfaulted phase- b and faulted phase- c respectively. The maximum modulation index that can be achieved in this case is 0.42. In phase- a and b, the output voltage is generated using modules II and III. In case of phase- c wherein, module-III is faulted, in order to generate balanced sinusoidal output currents modules-I and II are operated at a reduced modulation index of 0.2 to generate the same rms voltage resulting in balanced currents. The THD of the output voltage, v_c of the faulted phase- c is 48.9 % as shown in Fig. 7.26 which is much higher than that of phase- b output voltage of 26.6 %. Although the THD of output voltage of the faulted phase- c is high, the technique results in balanced output currents for both the phases as shown in Fig. 7.25. For an input dc voltage of 50V, the peak of the fundamental output voltage of the unfaulted phase is 110.2V, and 20.76V ripple rms voltage; whereas for the faulted phase it is 116.6V and 40.4V respectively. This results in a THD of 26.6% and 48.9% respectively of phase b and c. However, both the phases have a fundamental peak current of 0.55A.

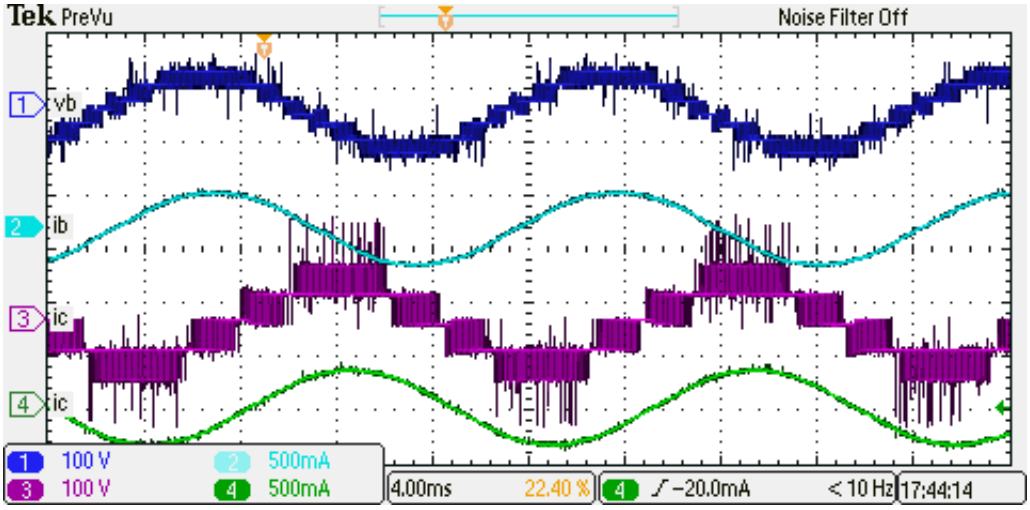


Figure 7.25: Experimental result of the output voltage, v_b in (CH-1) [100 V/div] and output current, i_b in (CH-2) [0.5A/div] of phase-b with $4nV_{in}$ module faulted and of v_c in (CH-3) [100V/div], current, i_c in (CH-4) [0.5 A/div] of phase- c with n_{in} module faulted, in 4 ms/div time scale for a modulation index of 0.4

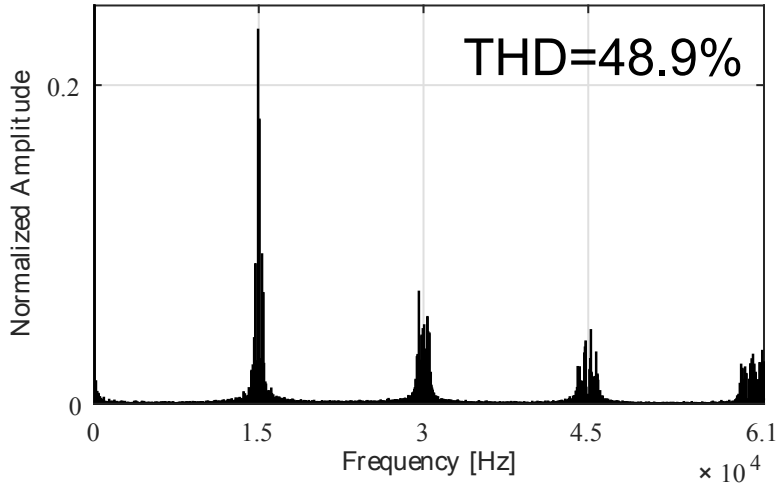


Figure 7.26: Harmonic spectrum of the output voltage, v_c of the faulted phase- c

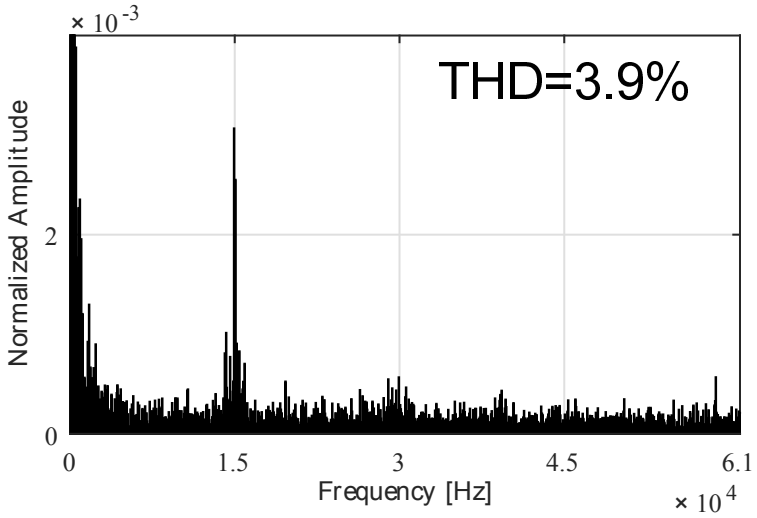


Figure 7.27: Harmonic spectrum of the output current, i_c of the faulted phase- c

7.3 Modulation-II: Simulation and experimental results

The modulation technique is verified on a scaled down fifteen level three-phase laboratory prototype as shown in Fig. 7.1. This section presents a detailed description of the hardware prototype along with key experimental and simulation results.

Table 7.1: Specifications

V_{in}	I_a	I_{in}	$\widehat{V_{ll1}}$	f_{sw}	f_o	R_{load}	L_{load}
45 V	0.96 A	15.4 A	471.1 V	15 kHz	60 Hz	200 Ω	46.6 mH

The proposed modulation technique on the converter topology was simulated using MATLAB/Simulink. The simulation parameters are same as the hardware prototype and the results are presented together. In the commutation section, it was mentioned that, due to the dead-time of the primary side H-bridge switches the output voltage will be zero whenever, the link voltage changes polarity. Fig. 7.29 provides the experimental validation of this concept described in the commutation section. The simulation and experimental results of the output current, i_a; phase-to-neutral output voltage, v_a and transformer link voltage v_{sa1}, at the instants when v_{sa1} goes to zero are shown in Fig. 7.28 and Fig. 7.29 respectively. As shown in the figures, the output load current, i_a varying at 60Hz is constant on a 10μs timescale. The secondary side link voltage, v_{sa1} will not transition instantly from +172V to −172V because of the dead-time of the primary side H-bridge switches. As shown in Mode 3 of Fig. 4.13b in the commutation section, during the dead-time all the switches of

the primary side H-bridge are gated OFF. At this instant, the continuous inductive output current, i_a freewheels through the AC-AC converter modules resulting in the output voltage, v_a to be zero as shown in Fig. 7.29.

In the ideal modulation section, it was mentioned that the modules which generate a constant output voltage switch only when the link voltage switches. But, the module which has to generate a pulsating output voltage undergoes switching transition even though the link voltage is constant. The next result demonstrates the above description using the experimental setup. Figs. 7.30 and 7.31 show the output line current, i_a, Module I output voltage, v_{a1}, Module III output voltage, v_{a3} and Module I link voltage, v_{sa1}=±172V using simulation and experimental setup respectively. As explained in the ideal modulation section, in order to generate $7nV_{in} \leftrightarrow 6nV_{in}$, that is 315V ↔ 270V output voltage, Module I which generates a constant voltage of, $4nV_{in}$, that is 164V (after the device drops); switches only when the link voltage changes polarity. Ideally, v_{a1} should be constant at 164V as shown in Fig. 4.2, but due to switch non-idealities as explained using Fig. 7.29 and Mode 3 of Fig. 4.13b, v_{a1} will momentarily generate zero voltage during the dead-time of primary side H-bridge switches. Module III in order to generate a pulsating voltage $nV_{in} \leftrightarrow 0$, that is, 36V ↔ 0, undergoes switching even though the link voltage, v_{sa1} is constant as shown in Fig. 7.31

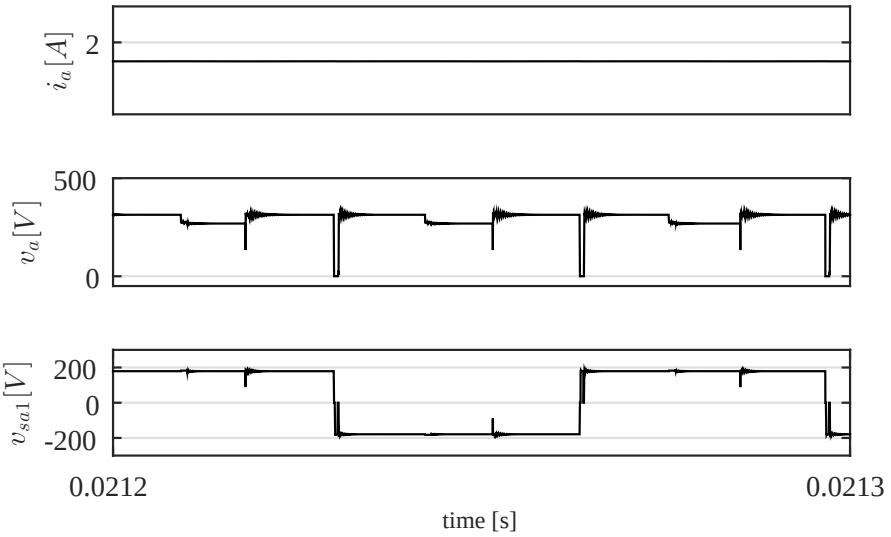


Figure 7.28: Simulation results of line current, i_a; Phase-to-neutral output voltage, v_a and transformer link voltage v_{sa1}

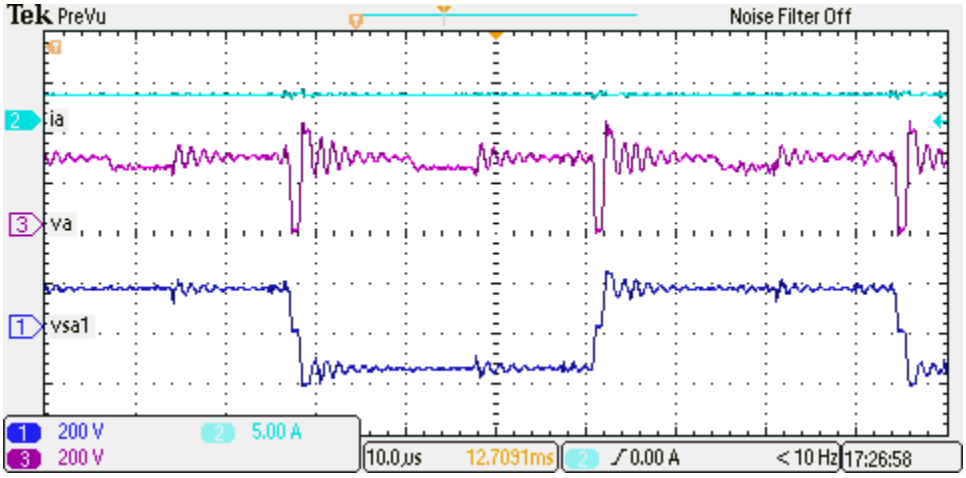


Figure 7.29: Experimental results of line current, i_a (CH-2), with 0.5 multiplication factor [5 A/div]; Phase-to-neutral output voltage, v_a (CH-3) [200 V/div] and Transformer link voltage v_{sa1} (CH-2) [200 V/div],in 10 μs/div time scale

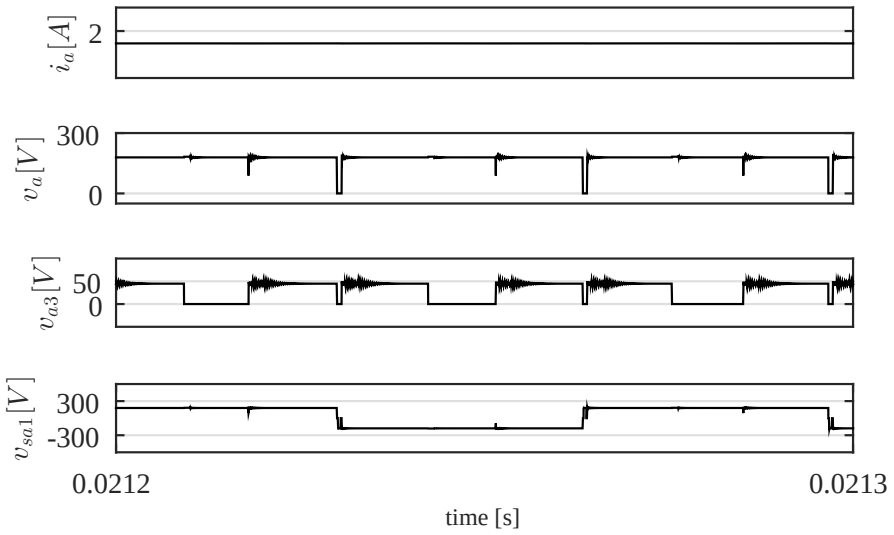


Figure 7.30: Simulation results of line current, i_a; module output voltages, v_{a1} and v_{a3} in modules I and III respectively and transformer link voltage v_{sa1}

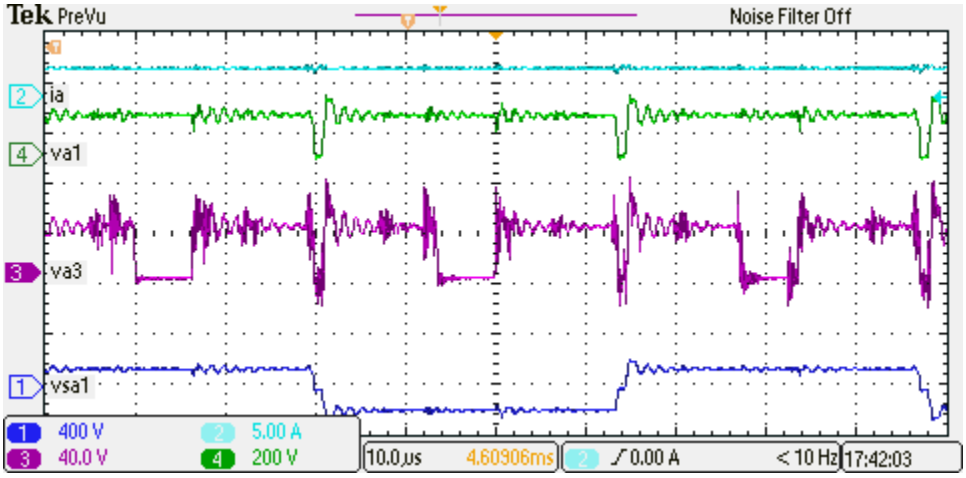


Figure 7.31: Experimental results of line current, i_a (CH-2), with 0.5 multiplication factor [5 A/div]; module output voltages, v_{a1} (CH-4) [200 V/div] and v_{a3} (CH-3) [40 V/div] in modules I and III respectively and transformer link voltage v_{sa1} (CH-2) [400 V/div] in 10 μs/div time scale

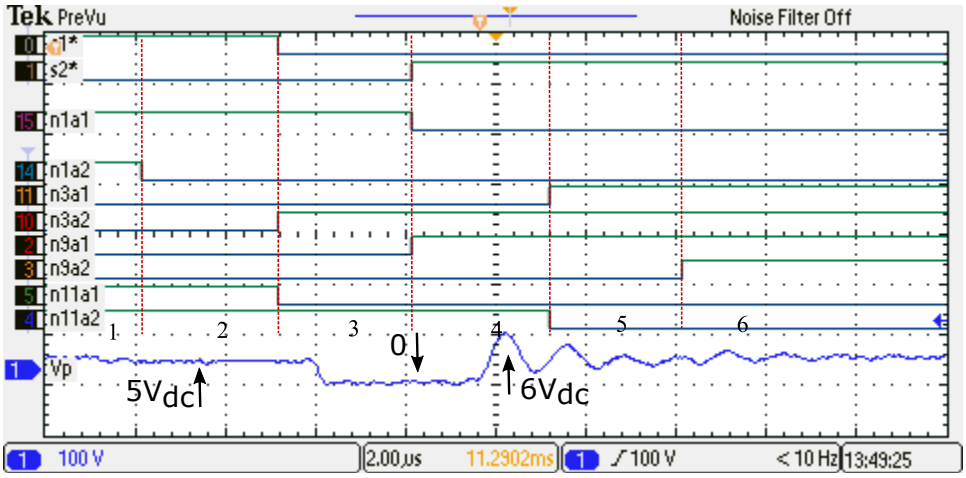


Figure 7.32: Digital signals corresponding to the six modes of operation as shown in Fig. 4.12c followed by the phase-to-neutral output voltage.

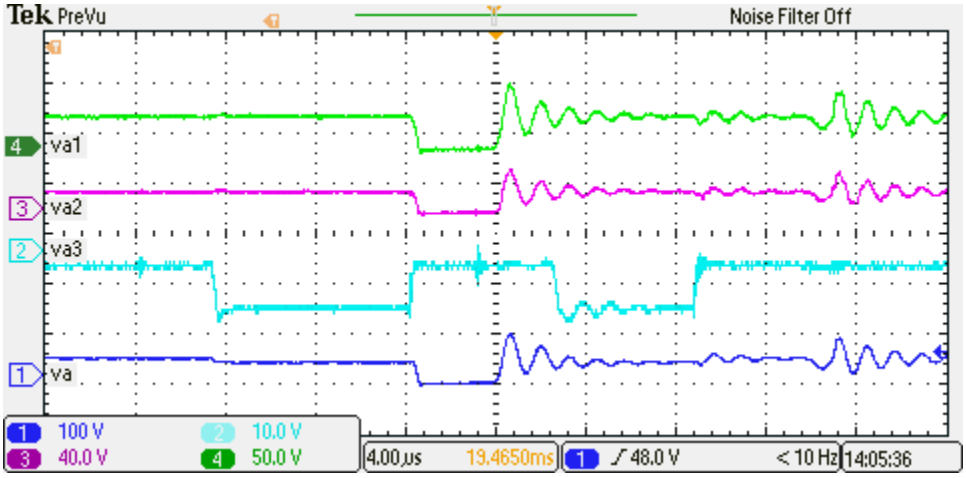


Figure 7.33: Output voltage of the three series connected modules, v_{a1} in (CH-4) [50 V/div], v_{a2} in (CH-3) [40 V/div] and v_{a3} in (CH-2) [10 V/div] followed by the phase-to-neutral output voltage, v_a in (CH-1) [100 V/div] in 4 μs/div time scale.

Fig. 7.32 shows the digital signals corresponding to the six modes of operation as described in commutation section using Fig. 4.12c. Fig. 7.33 shows the output voltage across each module followed by the total output voltage, v_a. As shown in Fig. 7.33, in order to generate v_a of $5nV_{in}$; v_{a1}=$4nV_{in}$, v_{a2}=$2nV_{in}$ and v_{a3}=$-nV_{in}$ even though the link voltage transitions from $+V_{in}$ to $-V_{in}$. The output voltage, v_a in Fig. 7.32 is delayed in comparison to the ten digital signals. As explained in the six modes of operation in the commutation section, the voltage, v_a will be $5nV_{in}$ in modes 1 and 2 and then it will generate a zero voltage in mode 3 for the aforementioned reason explained using Fig. 7.29. However, after a zero voltage, instead of generating $5nV_{in}$, output voltage is $6nV_{in}$ in mode 4. This is because, the switching of module output voltage, v_{a3} as compared to v_{a2} and v_{a1} is delayed as explained in mode 4 of Fig. 4.13b. The module output voltages v_{a1} and v_{a2} of Modules I and II respectively undergo natural commutation however, the module output voltage, v_{a3} will undergo forced commutation that is, switch from $0 \rightarrow -nV_{in}$ in the third step of the four-step commutation strategy. Hence, the resulting voltage v_a will be $6nV_{in}$ for one commutation step as shown in Fig. 7.32. Finally in mode 5 and 6 the output voltage, v_a is again $5nV_{in}$.

Figs. 7.34 and 7.35 respectively show the simulation and experimental results of the output voltage, v_a, output line current, i_a and two module output voltages, v_{a1} and v_{a2} when an R-L load is connected to the system. As shown in the figures, each module output voltage is zero during the time the link voltage changes polarity as shown in Fig. 7.29. For a particular output voltage level generation, switches in each module will undergo natural/forced commutation depending on the output current, i_a as explained using different modes of circuit operation in the commutation section and shown experimentally in Fig.

7.32. Hence, the output voltage, v_a in Fig. 7.35 has a profile different as compared to Fig. 4.2 generated using ideal switching signals. The simulation and experimental results along with the switch non-ideality also have the transformer leakage inductance. This will require a clamp circuit for leakage commutation. The modulation index considered was 0.97 and the input dc voltage was 45V. The link voltages of the three secondary windings after the device drops are 172V, 86V and 43V respectively as shown in Fig. 7.12. The module output voltages after the device drop of the AC-AC converter module switches are 164V, 80V and 36V respectively. This results in a peak output voltage of 280V. The experimental peak value of the fundamental output voltage, $\hat{V}_{a,1}$ was computed as 272V. This results in a load current of 0.96A as shown in Fig. 7.35. According to the mathematical relation in (7.2), $\hat{V}_{a,1}$ is 305.5V, which should have corresponded to a current of 1.07A. The reason for the mismatch of 0.11A between the analytical and the experimental result is due to the device voltage drop across the switches as explained above. Due to the switch non-ideality and the transformer leakage inductance the THD in the phase-to-neutral output voltage, v_a is 15.84 %.

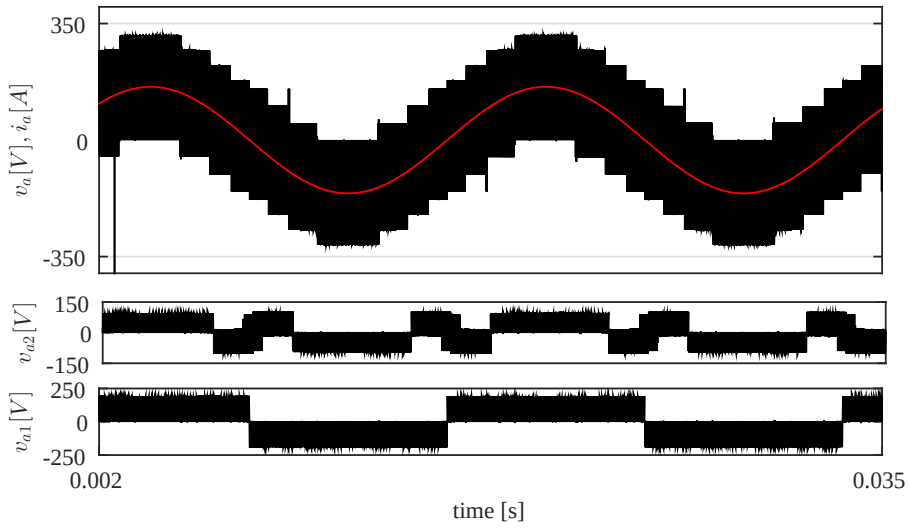


Figure 7.34: Simulation results of phase-to-neutral output voltage, v_a along with the line current followed by v_{a1} and v_{a2}

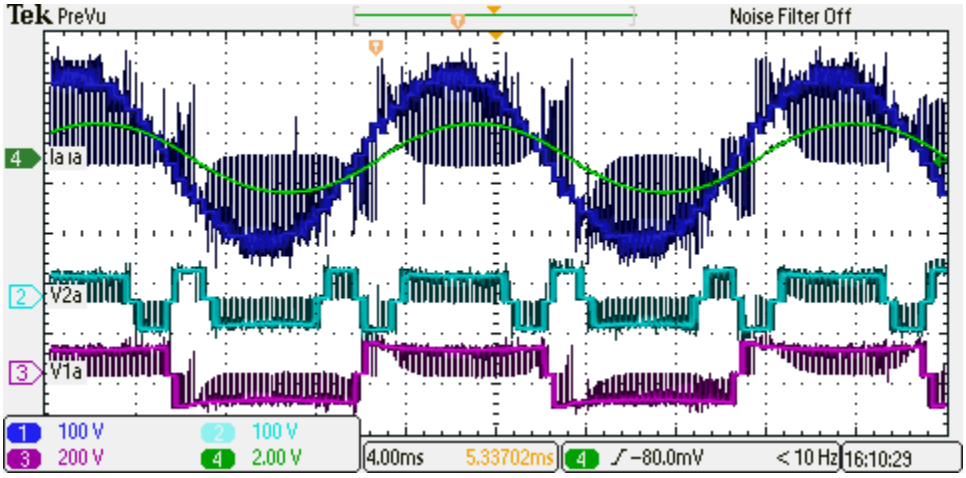


Figure 7.35: Experimental results of phase-to-neutral output voltage, v_a (CH-1) [100 V/div] along with the line current (CH-4) [2 A/div] followed by v_{a1} in (CH-3) [200 V/div] and v_{a2} in (CH-2) [100 V/div] in 4 ms/div time scale.

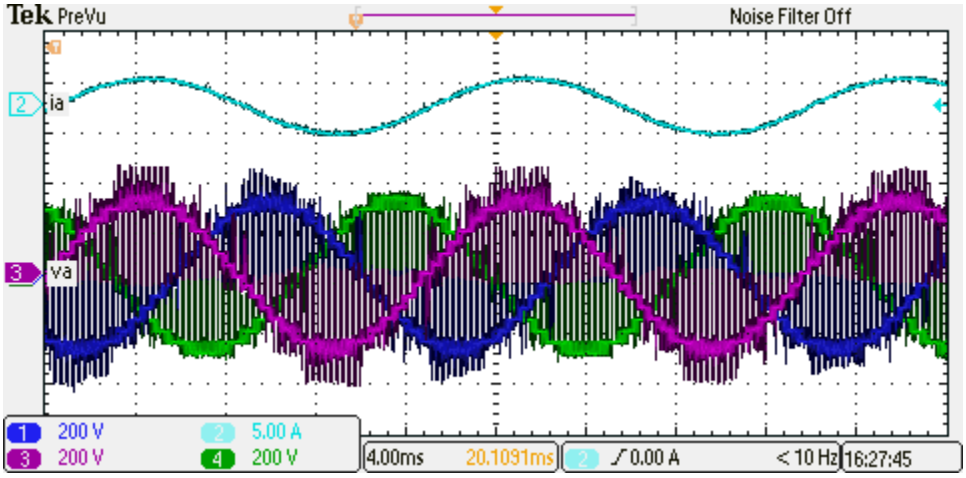


Figure 7.36: Phase-to-neutral voltages, v_a (CH-3), v_b (CH-1) and v_c (CH-4) [200 V/div]; along with the line current (CH-2), with 0.5 multiplication factor [5 A/div] in 4 ms/div time scale.

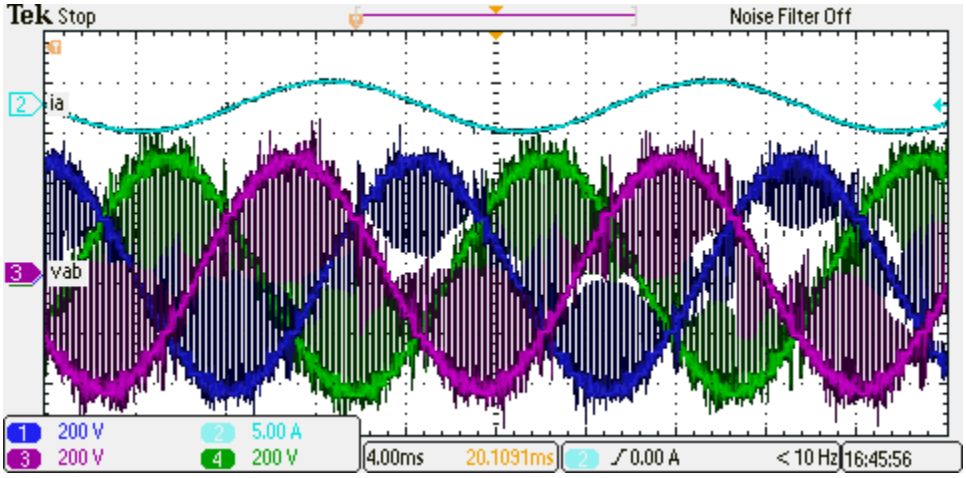


Figure 7.37: Line-to-Line output voltage of all three phases, v_{ab} (CH-3), v_{bc} (CH-1) and v_{ca} (CH-4) [200 V/div]; along with the line current (CH-2), with 0.5 multiplication factor [5 A/div] in 4 ms/div time scale.

Fig. 7.36 shows the experimental results of the line current, i_a followed by the phase-to-neutral output voltage of all three phases, v_a, v_b and v_c. Fig. 7.37 shows the line-to-line output voltage of the three-phase system.

Fig. 7.38 shows the experimental results of the leg voltages, v_{l1} and v_{l2} of left and right leg respectively of Module I followed by the module output voltage, v_{a1} for an input voltage of 45V. As shown in the figure, both the leg voltages switch at the link frequency to generate the module output voltage, v_{a1} as shown in Table 3.2. The module output voltage, v_{a1} in Fig. 7.38 generates a zero voltage which is not the case in the ideal output voltage generated using ideal signals. However, the harmonic spectrum as shown in Fig. 7.39 is similar to the harmonic spectrum using ideal signals and the module output voltage has dominant harmonics at the sidebands of twice the switching frequency which is 30kHz. Fig. 7.43 shows the experimental output voltage, v_a generated using the proposed modulation. The output generates a zero voltage whenever the primary side H-bridge switches, due to the switch non-idealities. The harmonic spectrum of v_a in Fig. 7.45 shows that the dominant harmonics are shifted to the sidebands of multiples of twice the switching frequency. The results are consistent with the literature [69, 71]. Fig. 7.39 shows the harmonic spectrum of the leg voltages and the module output voltage, v_{a1}. As shown in the figure, similar to the harmonic spectrum using ideal signals, both the leg voltages have dominant harmonics at the switching frequency of 15kHz and its sidebands. However, the differential voltage, v_{a1} has the dominant harmonic at the sidebands of twice the switching frequency which is 30kHz. Fig. 7.40 shows the nature of the leg voltages and the module output voltage, during the PWM operation; $4nV_{in} \leftrightarrow 0$. As shown in the figure, the module output voltage,v_{a1} because of the differential voltage across the two legs of Module I switches twice in a 15kHz interval.

Fig. 7.41, shows the harmonic spectrum of these voltages at 15kHz and its sidebands. In the figure, the normalized amplitude at each harmonic frequency from 14.8kHz-15.2kHz is shown on the left axis(in blue) and the phase angle in radians (in red) is shown on the right axis. Both the leg voltages, v_{l1} and v_{l2} have almost the same normalized amplitude at 15kHz and the sidebands. However, as the module output voltage is a difference of the two leg voltages, the same is not reflected in the harmonic spectrum of v_{a1} as shown in Fig. 7.41.

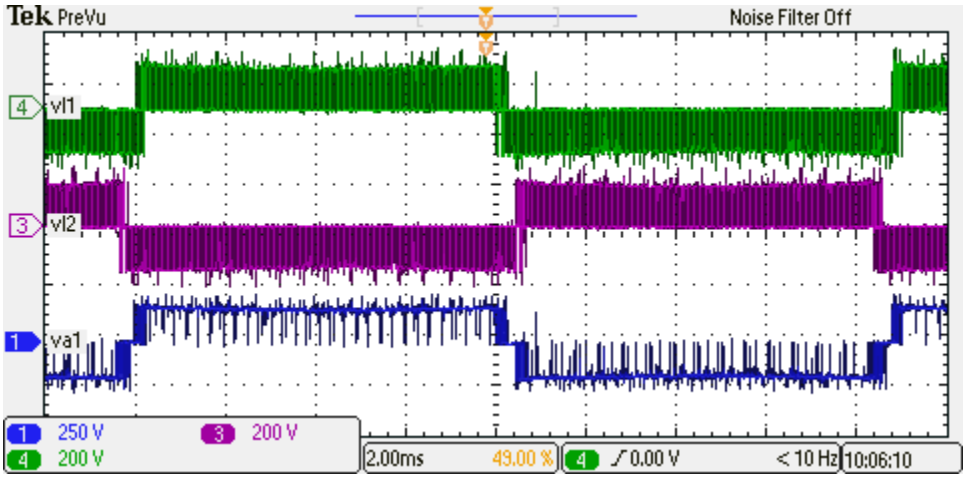


Figure 7.38: Fundamental cycle of leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1}

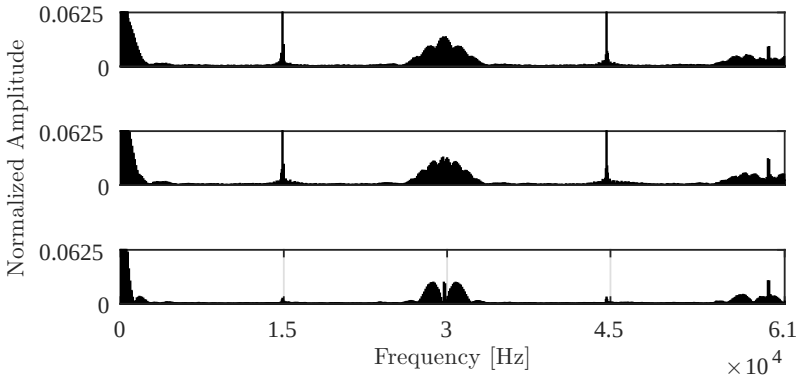


Figure 7.39: Harmonic spectrum of leg voltages, v_{l1}, v_{l2} of Module I followed by the module output voltage, v_{a1}

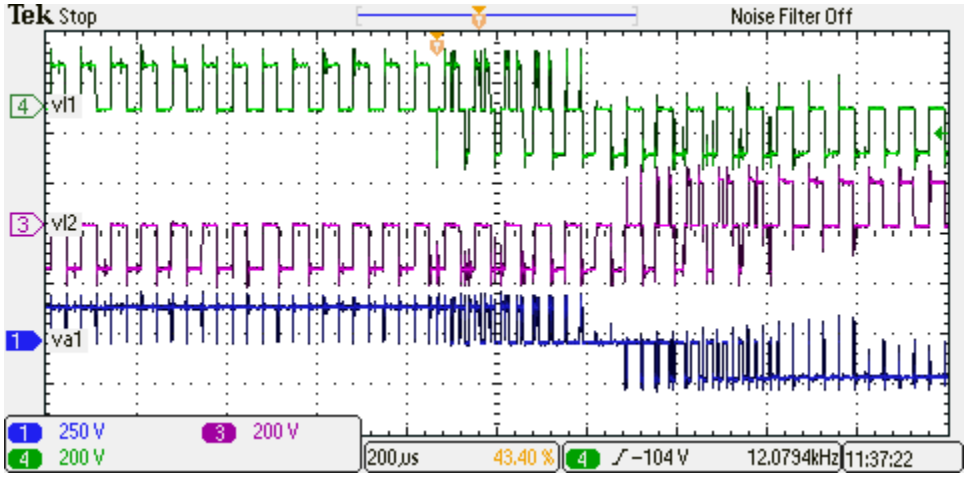


Figure 7.40: Zoomed in module voltage to show the profile during PWM operation

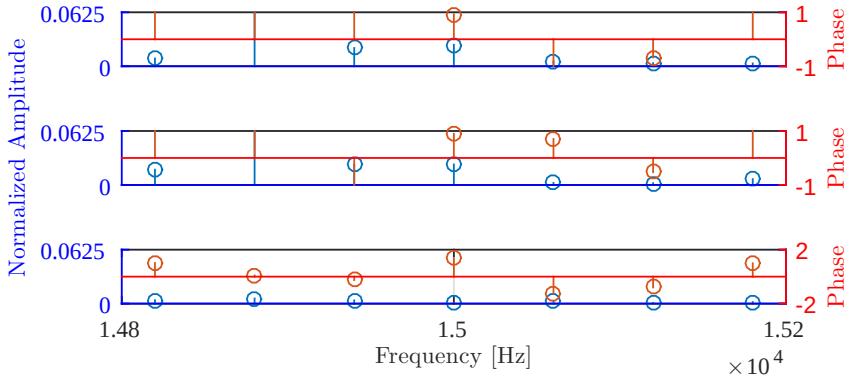


Figure 7.41: Harmonic spectrum at 15kHz to show the cancellation of the switching frequency harmonic component in the module output voltage, v_{a1}.

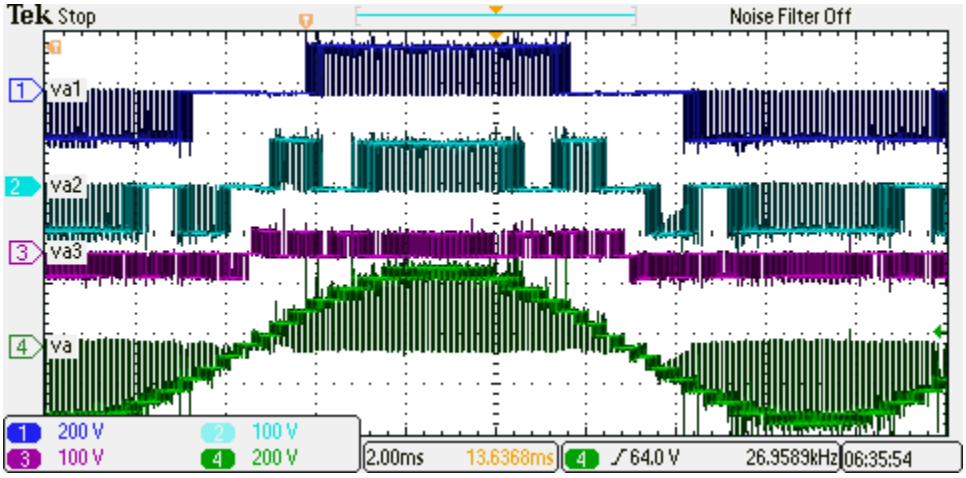


Figure 7.42: Modulation I: Module output voltage of the three series connected modules, v_{a1} in (CH-1) [200 V/div], v_{a2} in (CH-2) [100 V/div] and v_{a3} in (CH-3) [1000 V/div] followed by the phase-neutral output voltage, v_a (CH-4) [200 V/div] in 2 ms/div time scale, with a switching frequency of 15 kHz.

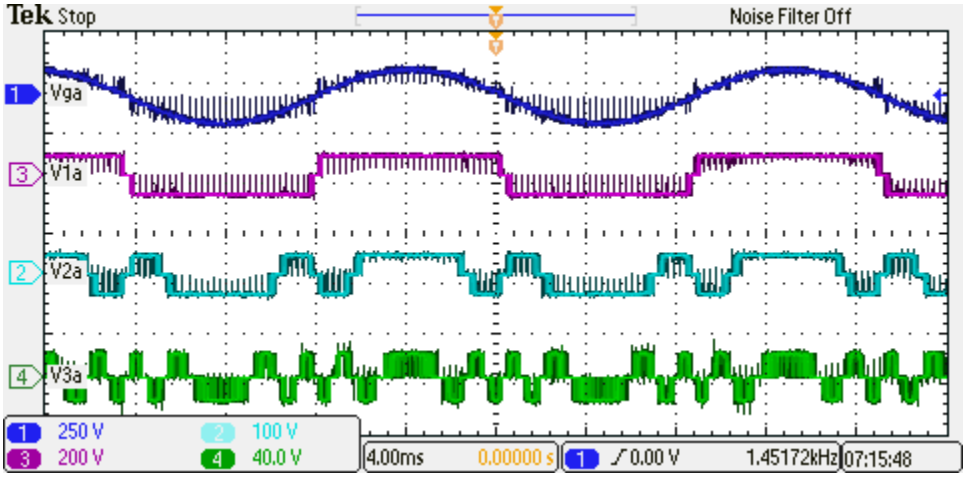


Figure 7.43: Modulation I: Module output voltage of the three series connected modules, v_{a1} in (CH-1) [200 V/div], v_{a2} in (CH-2) [100 V/div] and v_{a3} in (CH-3) [1000 V/div] followed by the phase-neutral output voltage, v_a (CH-4) [200 V/div] in 2 ms/div time scale, with a switching frequency of 15 kHz.

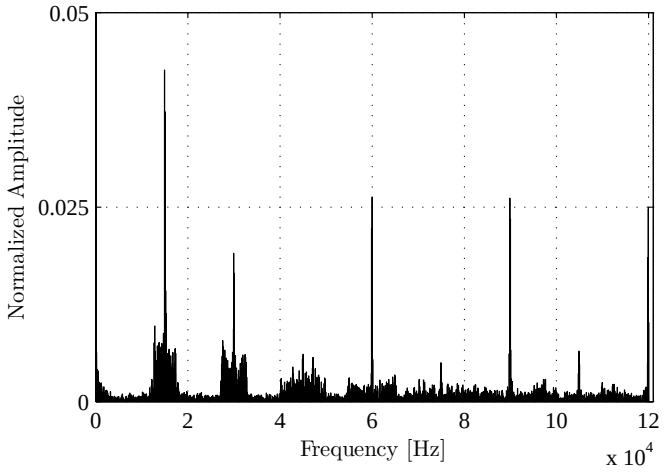


Figure 7.44: Modulation I: Harmonic spectrum of the experimental phase-neutral output voltage, v_a with a switching frequency of 15 kHz.

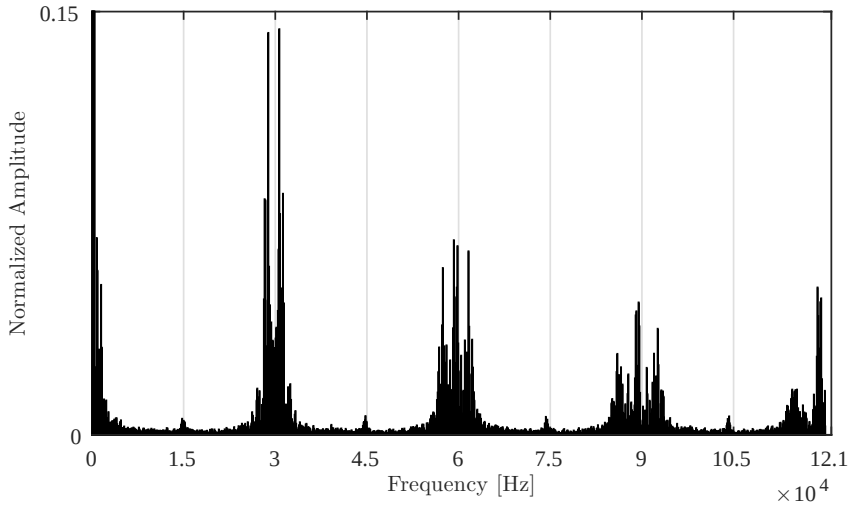


Figure 7.45: Modulation II: Harmonic spectrum of the experimental phase-neutral output voltage, v_a with a switching frequency of 15 kHz.

Chapter 8

High-Frequency Link Asymmetrical Converter

8.1 Converter topology

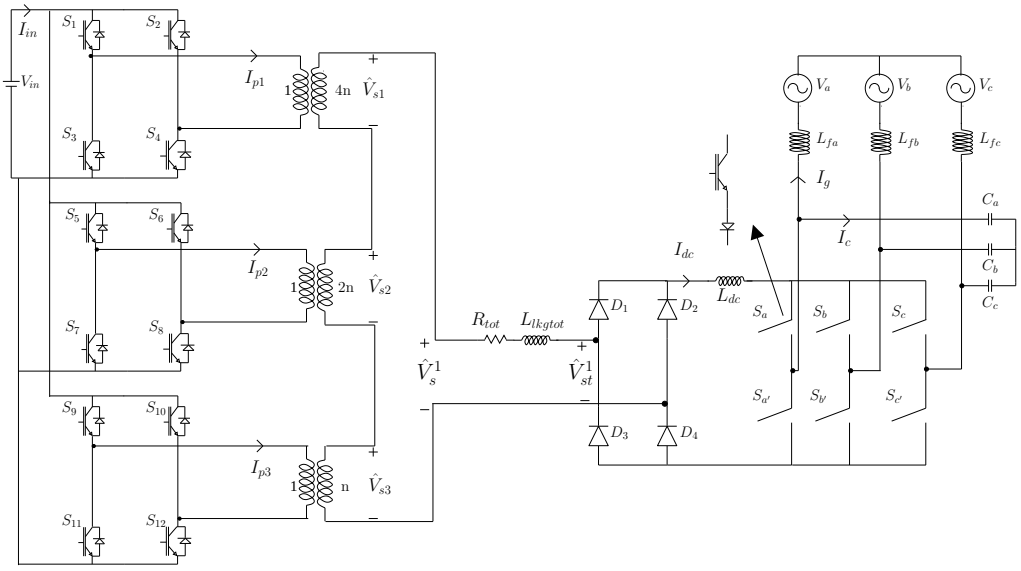


Figure 8.1: Converter Topology to Interface low voltage DC with three-phase Grid.

8.1.1 Circuit description

The converter topology with high-frequency transformer isolation is shown in Fig. 8.1. The asymmetrical converters comprising of switches S_1-S_{12} are connected in parallel on the input side in order to share the high input currents. I_{in} is the total input current from the parallel connection of all three converter modules. Each of the three asymmetrical converters are connected to three high-frequency transformers which have asymmetrical turns ratio of 1:4n,

1:2n and 1:n respectively. I_{p1}, I_{p2} and I_{p3} are the primary currents of the three HFTs. V_{s1}, V_{s2} and V_{s3} are the transformer voltages across each of the three secondary windings of the HFT and V_s is the summation of these voltages which is applied across the diode bridge. The converter modules are switched so as to generate a high-frequency stepped voltage across the output of each of the transformer secondary resulting in a multi-level stepped waveform across the diode bridge. Power flow of PV being unidirectional, secondary side of the HFT is connected to a diode bridge rectifier D_1-D_4 and a CSI made of switches S_a-S'_c via a dc link inductor, L_{dc}. The diode bridge and PWM CSI interface a three phase medium voltage grid. I_{dc} is the dc link inductor current. The CSI is connected to the grid via a capacitor bank, which is required for the current commutation, because of the presence of the grid source inductance. I_c is the current through the capacitor and I_g is the grid current.

8.1.2 Modulation strategy of input side converter

The primary side asymmetrical converters are switched so as to generate multi-level stepped voltage across the transformer secondary winding. With only three modules, 15 levels in the transformer secondary voltage can be generated; that is 7 positive levels, 7 negative levels and one zero level.

Table 8.1: Modulation Strategy for Different Positive Levels for V_s

Zone	Modulation Index	Module I	Module II	Module III
Zone I	1-0.8571	1	1	1
Zone II	0.8571-0.7143	1	1	0
Zone III	0.7143-0.5714	1	0	1
Zone IV	0.5714-0.4286	1	0	0
Zone V	0.4286-0.2857	0	1	1
Zone VI	0.2857-0.1428	0	1	0
Zone VII	0.1428-0	0	0	1

Generating the output voltage in zone I: For zone I operation the modulation index is from 1-0.8571. The switches S_1, S_4, S_5, S_8, S_9 and S_{12} are switched ON throughout the zone I operation to generate a constant voltage denoted by '1' in Table 8.1. Table 8.1 shows the modulation strategy for all the 7 zones of operation. In Table 8.1, '0' refers to the state in which the switches are switched so as to generate 0 voltage. If for all of the 7 zones of operation as shown in Table 8.1, switching the complimentary switches will generate the 7

negative levels.

The pulses can be generated using 7 level shifted carrier signals and comparing them with a reference sinusoidal signal. The seven carrier pulses hence obtained are XOR-ed accordingly to generate the pulses for the three converter modules. Fig. 8.3a shows the output voltage across the three secondaries followed by the total voltage depicting the 15 levels.

8.1.3 HFT voltage rating analysis based on DC link current of CSI

Under a unity power factor operation at the three phase grid, the capacitor current has to be supplied by the CSI [101]. Hence, the minimum DC link current I_{dc} can be expressed as in (8.1). Also, the dc link voltage across the output of the diode bridge, V_{dc} can be expressed in terms of the fundamental peak value of the total output secondary terminal voltage, $\hat{V}_{st}^1$ as given in (8.2). Assuming the CSI to be made of ideal switches, $V_{dc}I_{dc}$=P_g. Hence, from this P_g can be written as in (8.3):

$$I_{dc} = \frac{\sqrt{\left(\frac{2P_g}{3\hat{V}_g}\right)^2 + (2\pi f_s C_i \hat{v}_c)^2}}{m_i} \tag{8.1}$$

$$V_{dc} = \frac{2}{\pi}\hat{V}_{st}^1 \tag{8.2}$$

$$P_g = \frac{2}{\pi} I_{dc}\hat{V}_{st}^1 \tag{8.3}$$

In case of an ideal transformer, $\hat{V}_{st}^1$ is the same as $\hat{V}_s^1$ and can be expressed as in (8.4):

$$\hat{V}_{st}^1 = \hat{V}_s^1 = \hat{V}_{s1}^1 + \hat{V}_{s2}^1 + \hat{V}_{s3}^1 \tag{8.4}$$

where, $\hat{V}_{si}^1$, i=$\{1, 2, 3\}$ are the peak values of the fundamental component of each of the three transformer secondaries. Hence, (8.2) can be written as in (8.5)

$$\hat{V}_s^1 = \frac{\pi}{2} V_{dc} \tag{8.5}$$

As $\hat{V}_s^1$ is known, the transformer secondary voltages can be obtained from the following relation:

$$\hat{V}_{s1} = 0.57143(= 4/7)\hat{V}_s^1$$

$$\hat{V}_{s2} = 0.28571(= 2/7)\hat{V}_s^1$$

$\hat{V}_{s3} = 0.14286(= 1/7)\hat{V}_s^1$

where, $\hat{V}_{s1} = 2\hat{V}_{s2} = 4\hat{V}_{s3} = 4n\hat{V}_p$. The transformer turns ratio are n:$2n$:$4n$, and hence, the transformer secondary winding with $4n$ turns ratio will need to generate a voltage 4/7 times $\hat{V}_s^1$. As the transformer secondary voltages are known, from simulation the rms values: V_{s1}^{rms}, V_{s2}^{rms} and V_{s3}^{rms} are determined and can be used to determine the apparent power rating of the three high power high-frequency transformers using (8.6).

$$S_{link} = I_s^{rms}[V_{s1}^{rms} + V_{s2}^{rms} + V_{s3}^{rms}] \tag{8.6}$$

8.1.4 Effect of transformer leakage inductance

For a non-ideal transformer, where $L_{lkgtot} = \sum_{i=1}^{3} L_{si} + {n_i}^2 L_{pi}$ and $R_{tot} = \sum_{i=1}^{3} R_{si} + {n_i}^2 R_{pi}$, $n_i = \frac{N_{si}}{N_p}$ wherein, L_{pi}, L_{si}, R_{pi}, and R_{si}, $i = \{1, 2, 3\}$ are the primary and secondary leakage inductances and ac resistances respectively of the three HFTs:

$$\hat{V}_{st}^1 \neq \hat{V}_s^1 \tag{8.7}$$

and,

$$\hat{V}_s^1 = \frac{\pi}{2}\left[V_{dc} + \frac{2}{\pi} I_{dc}(2\pi f_{link} L_{lkgtot} + R_{tot})\right] \tag{8.8}$$

Hence, P_g can be written as in (8.9) and from this the fundamental peak value of the total transformer secondary voltage, $\hat{V}_s^1$ can be computed in terms of the dc link current, I_{dc} and grid power, P_g as given in (8.10).

$$P_g = I_{dc}\left[\frac{2}{\pi}\hat{V}_s^1 - \frac{2I_{dc}}{\pi}(2\pi f_{link} L_{lkgtot} + R_{tot})\right] \tag{8.9}$$

$$\hat{V_s^1} = \frac{2{I_{dc}}^2(2\pi f_{link} L_{lkgtot} + R_{tot}) + \pi P_g}{2I_{dc}} \tag{8.10}$$

In case of a non-ideal transformer, according to (8.7), the terminal voltage is not the same as $\hat{V}_s^1$. For the same $\hat{V}_s^1$ as in the case of an ideal transformer, the presence of transformer leakage inductance and ac winding resistance will result in a reduction of the terminal voltage, $\hat{V}_{st}^1$. Hence, according to (8.2) the dc link voltage, V_{dc} and dc link power P_{dc} will also be affected.

Table 8.2: Transformer Power Rating variation with the Leakage Inductance

Parameters	L_{lkgtot}=0		L_{lkgtot}=50μH		L_{lkgtot}=100μH	
-	Analytical	Simulation	Analytical	Simulation	Analytical	Simulation
$\hat{V}_s^1$	5814.2 V	5813.7 V	6238.6 V	6237.8 V	6663 V	6667.9 V
V_{dc}	3701.5 V	3697 V	3701.5 V	3700 V	3701.5 V	3620 V
I_s^{rms}	-	130.15 A	-	127.16 A	-	124.36 A
P_{dc}	500 kW	499.1 kW	500 kW	498.5 kW	500 kW	489 kW
S_{link}	-	603.9 kVA	-	633.04 kVA	-	661.33 kVA

So to ensure that the dc link power, P_{dc} is same as in the case of an ideal transformer, the transformer voltage rating has to be increased. The increased total transformer secondary voltage can be computed using (8.10). With the value of $\hat{V}_s^1$ known, as explained in the previous section the rms voltages of individual transformer secondary windings can be determined.

The presence of the transformer leakage inductance, causes a phase shift between the fundamental current component and the fundamental voltage component, resulting in reactive losses. The resultant lagging power factor increases the overall transformer power rating. Table 8.2 summarizes the increase in the transformer power rating caused due to the presence of leakage inductance in comparison to an ideal transformer. Three different values of leakage inductance are chosen: 0 (assuming an ideal transformer) 50 μH and 100 μH. For all the cases, values of the parameters like $\hat{V}_s^1$, V_{dc}, I_s^{rms}, P_{dc} and P_{link} which are affected as a result of the transformer leakage inductance are computed.

In case of an ideal transformer, all the parameters can be computed analytically and $\hat{V}_s^1 = \hat{V}_{st}^1$ as the transformer is ideal. For an ideal transformer, there is no phase shift between the fundamental component of link current and link voltage and hence the displacement power factor is 1. The apparent power can be computed using (8.6) and it is 603.9 kVA even though the active power is 500 kW. As the output voltage of the transformer is a multi-step voltage (close to sinusoidal), for a constant average voltage of V_{dc}, $\hat{V}_s^1 = \frac{\pi}{2}\ V_{dc}$, which increases the voltage rating of individual transformers.

For the second case when the transformer leakage inductance is present, $\hat{V}_s^1$ is determined analytically from (8.10) and compared with the simulation result. The analytical value of $\hat{V}_s^1$ for 50 μH is 6238.6 V and for 100 μH is 6667.9 V close to that obtained from simulation. The values for the other parameters are extracted directly from the simulation done in MATLAB environment.

The Table 8.2 clearly shows that due to the leakage inductance the link current smoothens,

resulting in a reduction of the current % THD. But the displacement power factor between $\hat{I}_s^1$ and $\hat{V}_s^1$ increases, resulting in increased reactive power losses. Hence, with the presence of transformer leakage inductance the apparent power increases to 633.04 kVA and 666.33 kVA for a transformer with 50 μH and 100 μH of total leakage inductance as compared to 603.9 kVA for an ideal transformer.

It is important to design the transformers with low leakage inductance but as the secondary side contains a diode bridge the proposed topology does not require any clamp circuit or any complex leakage commutation strategy.

8.1.5 Control of CSI

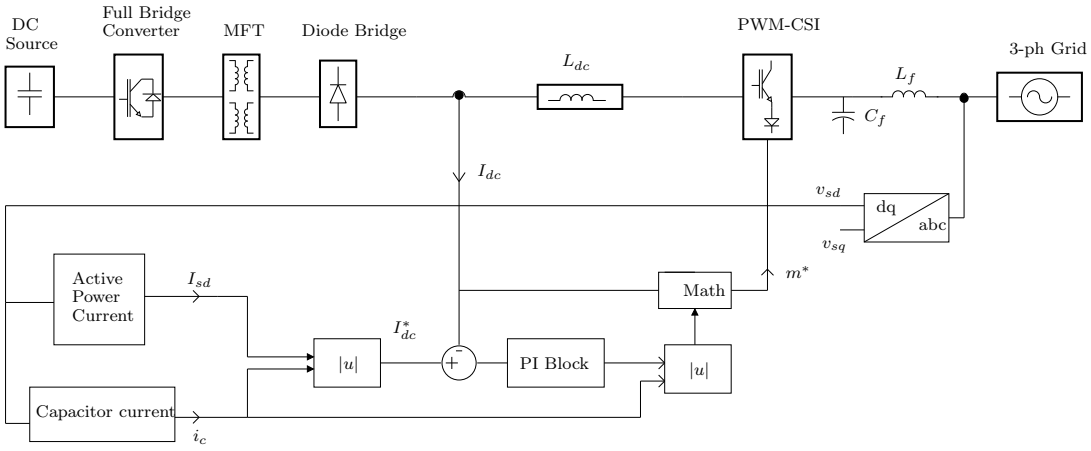


Figure 8.2: Control Diagram for a PWM-CSI

The dc link current I_{dc} in a PWM CSI supplies the active current component to the grid and also supplies the filter capacitor reactive current in case of a unity power factor operation. A closed loop control using a PI controller is implemented to maintain a constant current, I_{dc} in the steady state as shown in Fig. 8.2. Simple carrier based modulation approach is used for modulating the CSI [102]. The control scheme is employed by changing the modulation index supplied to the PWM CSI.

The d-axis is aligned with the phase a axis. Hence, the d-axis voltage, v_{sd} is same as the phase-to-neutral peak voltage, $\hat{v}_g$ and q-axis voltage, v_{sq} is 0.

The active power in dq reference frame is:

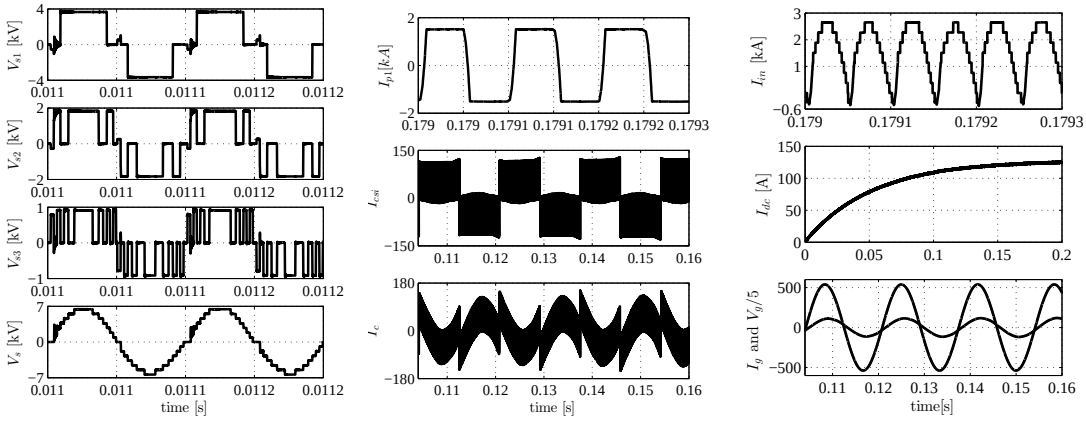
$$P_g = 1.5 v_{sd} i_{sd} \tag{8.11}$$

The active current component can be obtained from (8.11) and the reactive current can be computed using $(2\pi f_s C_i \hat{v}_g)$ assuming that the drop across the output filter inductor is

negligible so that $\hat{v}_c = \hat{v}_g$. The reference current is computed using (8.1). The modulation index m_i is considered to be 1, its maximum value.

The error signal to the PI controller is the difference of the reference dc link current, I^*_{dc} and the actual sensed current, I_{dc}. The controller ensures that the active current component of the dc link current varies according to the required active power. The output of the controller is the modulation index given to the PWM-CSI.

8.2 Simulation results



(a) (b) (c)

Figure 8.3: (a) Top to Bottom: Transformer secondary voltages across each of the three transformers followed by the total secondary voltage (b) Top to Bottom: Transformer primary current, Two level current at the output of the CSI I_{csi}, Capacitor Filter current, I_c, (c) Top to Bottom: Input dc current, I_{in}, DC link current, I_{dc}, Grid voltage, V_g and Grid Current, I_g

The proposed topology was simulated using MATLAB/Simulink. The dc voltage source of $V_{in} = 300\ V$ is to be integrated to a three-phase 3.3 $kV/500\ kW$ grid at 60 Hz. The high-frequency transformer to step up the low input voltage to three-phase medium voltage is to be designed at 10 kHz. The transformer leakage inductances are considered to be 0.04 pu.

The top plot in Fig. 8.3b shows the primary current of one HFT. The diode bridge connected to the transformer secondary causes a trapezoidal current through the transformer windings, hence eliminating the problem of transformer leakage commutation. The primary current waveform nature is the same in all three primary windings but the magnitude of the primary currents vary depending on the transformer turns ratio. The second plot in Fig. 8.3b is of the two level current waveform of the CSI for phase a and the third plot is of the filter capacitor current of phase a. The fundamental peak component of this capacitor

current is equal to $2\pi f_s C_i\ \hat{v}_c$ as given in (8.1).

Fig. 8.3c shows a plot of I_{in}, I_{dc} and the grid side voltage and current. The mean value of input current, I_{in} is close to 1666.67 A, according to $I_{in} = \frac{P_g}{V_{in}}$, but the input current goes negative on an instantaneous basis as shown in the first plot of Fig. 8.3c. This will require a capacitor in the input to avoid the flow of negative current into the dc source. I_{dc} reaches a constant value of 123.71 A in steady state as the error signal to the PI control block goes to 0. In order to achieve acceptable grid current THD ($< 5\%$) and a close to unity power factor, the grid side filter inductance is computed to be L_{filter}= 5 mH and the filter capacitor is chosen to be C_{filter}= 50 uF.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

An asymmetrical single-stage multilevel converter with HFT isolation has been proposed in this thesis for interfacing low voltage DC to high voltage AC grid. The topology combines the advantages of single-stage power conversion, galvanic isolation in a small footprint using HFT and lower voltage THD by generating multilevel voltages. The ideal modulation along with the four-step commutation algorithm for the bi-directional switches was implemented. This resulted in an output voltage profile having glitches, arising due to switch non-idealities. The cause and effect of the glitches was described in detail and a compensation technique was implemented to negate the voltage reversal. The compensation allows to improve the input current ripple profile and hence, enhances the system power quality. Another set of glitches, in the output voltage due to the interdependence of the three AC-AC converter modules were investigated and a compensation technique was proposed and demonstrated.

Another modulation technique has been investigated for the isolated asymmetrical converter using conventional level shifted carriers. Considering ideal switches, the generation of fifteen levels in the phase-to-neutral output voltage using three AC-AC converter modules is explained. However, because of the non-idealistic nature of the switch, the switching signals have to be modified. The modifications in the ideal signals to incorporate the dead-time of primary side H-bridge switches and four-step commutation of bi-directional switches is explained in detail by showing six different modes of circuit operation for one particular switching transition. The modified signals based on the high-frequency link shift the harmonic frequencies in the phase-to-neutral output voltage to the sidebands of multiples of twice the switching frequency, hence, reducing the size of the grid filter. The analysis in general can be used for any isolated single-stage converter and will also aid in the real-time implementation of the converter.

The design and characterization of the multi-winding transformer to achieve low leakage inductance was explained. Simulations and experimental results on a laboratory prototype were given to demonstrate the proposed topology and validate the compensation techniques.

The topology has certain challenges in terms of: 1) higher control complexity in comparison to two-stage conversion; 2) unlike the dual active bridge, control of the proposed topology does not allow complete soft-switching; 3) the asymmetrical configuration although enables to achieve more levels with lesser device count, however, the absence of any redundant modules affects the system in case of a module failure; 4) the proposed topology requires a multi-winding transformer design which is difficult to manufacture.

The following has been done in this thesis to address those challenges: i) A normalized index value similar to [26] has been computed to determine the optimum number of levels for asymmetrical single-stage conversion in terms of voltage THD, control complexity, switch count and number of multi-winding transformer terminals. Based on the data, 1:2:4 asymmetrical configuration allows to achieve the lowest normalized index; ii) implementation of four-step commutation, results in 3/4th transitions to be soft-switched even at low currents. iii) converter operation in case of module failure is outlined by a combination of modification in control and hardware reconfiguration [95, 97]. The other single-stage HFT isolated topologies face similar challenges [45, 68], whereas the two stage topologies require reliability critical DC-link electrolytic capacitor [103] and have issues caused due to multi-stage conversion. Reliability of a single-stage converter is more in comparison to a multi-stage converter. However, a quantitative analysis of the reliability of the proposed converter needs to be done similar to [104], [105] but is a part of future work.

9.2 Study of several isolated multilevel converter topologies

Table 9.1 presents a case study of several isolated multilevel converter topologies in the literature. It is to be noted that for an equivalent comparison with all the topologies, a three phase system is considered. For a power level, P, phase-to-neutral voltage, v_{pn}, input voltage, V_{in} and input current, I_{in}, a comparison of several topologies is outlined based on the voltage and the current rating of the devices and the control algorithm used.

Table 9.1: Case Study of Several Isolated Multilevel Converter Topologies

Topology*	Modules		Device Rating		Levels	Capacitor	Switches		Control†
	N_{pm}	N_{sm}	V_{rs}[V]	I_{ps}[A]			S_p	S_s	
ISTSC [27]	9	9	$\frac{\hat{v}_{pn}}{3}$	$\frac{I_{in}}{9}$	7	Identical	36	72	PWM
ISSSC1 [80]	3	6	$\frac{\hat{v}_{pn}}{2}$	$\frac{I_{in}}{3}$	5	-	12	24	SVM
ISSSC2 [68]	8	24	$\frac{\hat{v}_{pn}}{8}$	$\frac{I_{in}}{8}$	17	-	32	192	PWM
IATSC [61]	3 1	 3 3	V_{in} $\frac{3\hat{v}_{pn}}{13}$ $\frac{\hat{v}_{pn}}{13}$	$\frac{0.8I_{in}}{3}$ $0.2I_{in}$	27	Unidentical	12 4	 24 24	NLM
IASSC1 [63]	1	3 3 3	$\frac{4\hat{v}_{pn}}{7}$ $\frac{2\hat{v}_{pn}}{7}$ $\frac{\hat{v}_{pn}}{7}$	I_{in}	15	-	4	24 24 24	Uni- Polar PWM
IASSC2	3	3 3 3	$\frac{4\hat{v}_{pn}}{7}$ $\frac{2\hat{v}_{pn}}{7}$ $\frac{\hat{v}_{pn}}{7}$	$\frac{I_{in}}{3}$	15	-	12	24 24 24	PWM

*ISTSC- Isolated Symmetrical Two Stage Converter; ISSSC1- Isolated Symmetrical Single Stage Converter 1
ISSSC2- Isolated Symmetrical Single Stage Converter 2; IATSC- Isolated Asymmetrical Two Stage Converter
IASSC1- Isolated Asymmetrical Single Stage Converter 1; IASSC1- Isolated Asymmetrical Single Stage Converter 2
†PWM- Pulse Width Modulation; SVM- Space Vector Modulation; NLM- Nearest Level Modulation

ISTSC uses a two stage conversion from high-frequency AC-DC-line frequency AC and hence requires a large number of reliability critical DC-link capacitors. However, the high frequency dual active bridge configuration allows the devices to be soft-switched. ISSSC2 on the other hand, due to single stage conversion remove the DC-link capacitors. Such symmetrical multilevel converter topologies, require many modules to be connected in series to generate a multilevel voltage resulting in a large system. However, the reliability of the system can be increased by having a specific number of redundant modules.

Isolated asymmetrical converters can generate a large number of levels using less number

of devices. The switch count in Table 9.1 shows the difference in the number of devices in an asymmetrical converter in comparison to a symmetrical case. IATSC can achieve the lowest THD with the least number of devices. The diode bridges are replaced with H-bridges for bi-directional power flow and an equivalent device count. However, the absence of a transformer winding for the main converter requires a high voltage DC input and high voltage rating devices. Nearest level modulation is used to generate the 27-level output voltage. IASSC2 uses asymmetrical single stage modules to generate a multilevel output voltage using modified PWM. The topology allows to achieve fifteen levels in the output voltage with less number of switches and the single stage conversion allows to get rid of the DC-link capacitor. The modulation results in the dominant harmonics at the sidebands of multiples of twice the switching frequency resulting in a smaller grid filter. Also, by the virtue of four-step commutation in every transition 3/4th of the transitions are soft-switched [106]. However, due to asymmetrical configuration the reliability of the system is a concern due to the absence of redundant modules.

9.3 Future work

- Investigation of system efficiency and loss breakdown.
- Determination of optimal switching frequency based on the loss model.
- Quantitative analysis of system reliability.
- Investigate techniques to retrieve the energy lost in the leakage inductance for gate drive power supplies etc.
- Comparison of transformer design using planar, non-planar geometry and using ferrite or amorphous/nanocrystalline material in terms of leakage inductance.
- Detailed investigation of a proposed topology consisting of full-bridge modules in parallel on the low voltage input side and Modular Multi-level Converter(MMCs) on the high voltage output side with a series of asymmetrical two-winding transformers.

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