Digital Intensive Circuit Design Techniques for Enhancing Performance of Clock Generators and Data Converters

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Abstract

Over the last few decades, the semiconductor industry have been developed along with the scaling of CMOS transistors. The reduced feature size makes it easy to integrate as many as digital logic and memory circuits within a limited die area. However, analog and mixed-signal circuit systems including clock generators (i.e. PLL, DLL and etc.) and data converters (i.e. ADC, TDC and etc.) have not fully utilized the beneficial transistor scaling since they have been mainly designed with critical analog circuit blocks such as amplifiers which require the use of large transistors to meet their analog performance criteria (i.e. gain, bandwidth and etc.).

This thesis makes several contributions to the mixed-signal clock generators and data converters by proposing digital-intensive or all-digital circuit design techniques which facilitate the utilization of highly-digital mixed-signal circuit systems in a variety of applications ranging from high-performance microprocessors to compact and low-power biomedical and healthcare systems. Firstly, we present an adaptive PLL which can optimize microprocessor power and performance by automatically tracking supply noise sensitivity with the proposed closed-loop circuit including a digital bit-error monitor in Chapter 2. In Chapter 3 and 4, we propose novel quantization schemes of analog-to-digital conversion for the direct acquisition of extremely small physiological signals with sub-mV input range. By measuring the beat frequency (i.e. frequency difference) between the two VCO output clock frequencies driven by an input signal and a reference, we can detect sub-mV input signals with the ADC resolution of 6-to-7ENOB.

Novel time amplifier concepts for digital PLL based clock generator circuits are presented in Chapter 5 and 6. In Chapter 5, a switched ring-oscillator based time amplifier with precise gain control and wide input range is presented. The proposed time amplifier has been implemented in a time amplifier based three-step TDC and used for achieving high time resolution and wide input range along with a fine Vernier delay line based TDC. In Chapter 6, a noise-shaping TDC has been implemented with an adaptive pulse train time amplifier. The high TDC resolution has been achieved by combining a noise-shaping gated-ring oscillator based TDC techniques and a pulse-train based time amplifier. The adaptive time amplifier has been used for achieving wide input range by adaptively controlling the time amplifier gain (i.e. high time amplifier gain with narrow input range and low gain with wide input range).

Another type of digital PLL (i.e. bang-bang digital PLL) with a proposed noise-shaping fractional sub-sampler is described in Chapter 7. Digital PLL in-band noise is reduced with the sub-sampling operation and the spurs due to limit cycle of digital PLL are suppressed from the noise-shaping behavior of the proposed sub-sampler circuit. In the last topic of this thesis (Chapter 8), we propose an aging-tolerant digital PLL based on a dynamic element matched ring-oscillator DCO circuit. In-situ DCO aging monitor has been also included in the test-chip for the first time to evaluate the impact of different stress mechanisms on the digital PLL operation.

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Chapter 1 Introduction

Integrated circuit systems such as microprocessors and system-on-chips with billions of transistors are now being developed and used in a broad range of applications ranging from personal and mobile computers to emerging healthcare and biomedical applications. While the digital logic circuits have been benefited from the scaling of CMOS process, many analog and mixed-signal circuits including clock generators (e.g. PLL, DLL, etc.) and data converters (e.g. ADC, TDC, etc.) have been suffering from the difficulties in scalability due to the limited minimum device sizing to meet their design specifications (e.g. gain, bandwidth, etc.). While the few nanometer scale devices are being developed for the use of them in the highly-integrated systems, most of the analog and mixed-signal systems are still utilizing the old processes (e.g. 0.18μm, 0.13μm, etc.). Therefore, the conventional clock generators and data converters have not fully utilized all the benefits from using digital circuitry such as scalability, supply noise insensitivity, low area consumption and easy portability and re-configurability. In this thesis, we propose several digital-intensive circuit design techniques for enhancing the conventional mixed-signal clock generators and data converters. By enhancing the mixed-signal system performance criteria (e.g. PLL output clock noise performance, ADC output resolution, etc.) with the proposed digital-intensive circuit techniques, the overall system can be improved since the mixed-signal systems typically determines the overall system performance by generating system clocks or converting the incoming analog signals to the digital outputs for the post-processing in the digital core. The test-

chip circuits were designed and verified using the state-of-the-art silicon CMOS process technology (e.g. 65nm LP, 32nm high-k metal gate SOI).

1.1 Processor Clocking under Resonant Supply Noise

Power supply noise has been considered as one of the most important performance limiting factors of modern low-voltage and high-performance microprocessors. Many on-chip and off-chip decoupling capacitors have been used for regulating the noise. In addition, more sophisticated circuit techniques including supply grid optimization, noise-tolerant clock network designs, active and switched capacitor based decoupling capacitors have been also developed. However, the magnitude of the supply noise and their impact on the processor performance could not be removed. Supply noise caused by the resonance between the package/bonding inductance and on-die decoupling capacitors (i.e. first-droop noise) is typically believed to be the dominant supply noise source in modern high performance systems and has the largest voltage droop magnitude (i.e. 10-15% of nominal supply voltage).

Recently, circuit researchers have revealed an intrinsic timing compensation phenomenon between the clock and the data signals which is commonly referred to as the Clock-Data Compensation or CDC. The beneficial CDC effect could alleviate the negative impact of the resonant supply noise on processor operating speed. Adaptive clocking schemes have been proposed to maximize the CDC effect. However, previous techniques rely on a significant modification of the conventional clock-paths or an exhaustive search algorithm to find the optimal CDC parameters (i.e. supply noise sensitivity and phase shift). In addition, the parameters could not be adjusted once they

are programmed and therefore, they were susceptible to the operating condition changes and PVT variations. In this thesis, we propose an adaptive supply noise sensitivity tracking PLL that addresses these issues. The adaptive PLL has been implemented in 32nm SOI process for the verification of its function and performance.

1.2 Analog-to-Digital Converters for Biomedical Systems

With the increasing interests and the needs for a variety of biomedical and health-care systems, there has been a great amount of research for the development of compact and energy-efficient analog-to-digital converters (ADCs). Significant progress has been made in the design of energy efficient Successive approximation register (SAR) ADCs and they achieved microwatt level power consumption while offering a reconfigurable resolution and sampling rate. However, the advancements in the ADC designs do not always result in the significant overall system power and performance improvements due to the signal preconditioning amplifiers which have been considered as essential building blocks in the conventional sub-mV signal acquisition systems. The amplifiers typically dominates the entire power and area consumption of the system. In this thesis, we propose highly-digital VCO-based ADC designs employing beat frequency (BF) based quantizers for the direct acquisition of sub-mV input signals without the use of any signal amplifier. Using the proposed ADC, the overall power and area consumption of multi-channel sub-mV signal acquisition systems can be significantly reduced since the channel amplifiers can be completely eliminated from the system. The proposed ADCs have been demonstrated in 65nm process to verify the concept and the performance of the proposed ADC.

1.3 Time Amplifier Based Time-to-Digital Converters

Time-to-digital converters (TDCs) have been utilized in a variety of applications such as digital phase locked loops (DPLLs), time-of-flight imagers, on-chip skew and jitter measurements and nuclear experiments. Recently, the TDCs have become increasingly important with the ever-increasing uses of DPLLs in many applications. While having the main advantage of lowered PLL area by using a digital loop filter (DLF) instead of the traditional passive loop filter with area-consuming large integrating and proportional capacitors, it also has many other advantages. The advantages include supply noise insensitivity, tolerance to PVT variations, easy scalability and portability.

While having the advantages of using DPLL in lieu of analog PLL, the degraded output clock phase noise performance due to the quantization error of TDC and digitally-controlled oscillator (DCO) is the key drawback. Since it is relatively easy to achieve a fine DCO output frequency resolution (e.g. lowering DCO gain while having the same number of control bits), the design of high resolution TDC is rather involved and typically requires the intensive use of analog circuitry or the large power consumption.

Delay line (DL) and Vernier delay line (VDL) based TDC have been most widely used due to their simple circuitry. However, both TDCs are suffering from trade-offs between the time resolution and the input range. While having a wide input range, the DL based TDC suffers from a low resolution since it cannot resolve a time difference shorter than a single inverter delay. On the other hand, the VDL based TDC suffers from a narrow input range while having a relatively high resolution by introducing a small delay difference between the two delay lines. To achieve both high resolution and wide

input range, time amplifier based TDC circuits are recently gain tractions. However, the existing time amplifier circuits suffer from several limitations such as the unpredictable gain, narrow input range (while having a small gain error), large gain error (while having a wide input range) and the need for complicated gain calibration techniques. To deal with such limitations, we proposes a switched ring-oscillator based time amplifier with a precise gain control over a wide input range. A three-step TDC incorporating the switched ring-oscillator based time amplifier has been implemented in 65nm. An adaptive pulse-train time amplifier based TDC has been also proposed for achieving both high resolution and wide input range. A digital PLL using the proposed adaptive time amplifier based TDC has been also demonstrated using 65nm process.

1.4 Integer-N Bang-Bang PLL Noise Performance

The design of high-resolution TDC typically requires sophisticated circuit design techniques such as Vernier delay line, time amplifier and noise-shaping TDC. While consuming a significant amount of power, they also suffer from PVT variations. Instead of using TDC, a bang-bang (i.e. binary) phase detector (BBPD) based PLLs (BBPLLs) have been recently utilized due to its simple circuitry and the phase noise performance comparable to that of the DPLLs with a high resolution TDC. The BBPD has been also utilized as a sub-sampling phase detector in a sub-sampling PLL which has been introduced as a divider-less PLL for achieving the low in-band phase noise by replacing the conventional phase detector and feedback divider with the sub-sampling phase detector.

While the existing DPLLs based on the BBPD (i.e. a conventional BBPLL and a sub-sampling digital PLL) are capable of generating output clocks with competitive in-band phase noise performance which is comparable to that of the DPLLs with high resolution TDCs, they are still suffering from the other major clock noise source. The additional noise comes from the large magnitude of spurious tones which are generated due to the limit cycle regime of bang-bang digital PLL. In this thesis, we propose a fractional sub-sampling concept which is good for both suppressing the spur noise and improving the in-band phase noise. A BBPLL based on the proposed fractional sub-sampling phase detector has been implemented in 65nm.

1.5 Reliability of Digital PLL

With the recent of scaling of CMOS process, the negative impacts such as circuit failures and parametric shifts due to the device aging have become severe. While the aging impacts on the digital logic or memory circuits with different stress mechanisms (e.g. hot carrier injection (HCI) and bias temperature instability (BTI)) have been actively researched, circuit researchers typically have ignored the aging impacts on the analog and mixed-signal circuits. However, the most of the recent analog and mixed-signal circuit systems consist of many digital intensive or all-digital circuit building blocks. In fact, many of the existing analog and mixed-signal systems are now being replaced by their digital implementations as the performance of those circuits have become comparable to that of the analog counterparts. Therefore, the aging impacts on the digital circuitry are not any more confined to the traditional digital logic applications. In this thesis, we analyze the device aging impacts on the ring-oscillator based DCO

circuits which is the main building block of the digital PLL. Based on the analysis, we implemented an aging-tolerant digital PLL employing the proposed dynamic element matched DCO circuit with longer life time.

1.6 Summary of Thesis Contributions

This thesis makes several contributions that enhance the performance of mixed-signal clock generators and data converters. First, an adaptive PLL for optimizing microprocessor power and performance by automatically tracking the supply noise sensitivity with the developed closed loop operation. The mechanism of the supply noise sensitivity tracking for achieving the optimal clock data compensation effect is theoretically analyzed and applied to the PLL design. Second, novel VCO-based ADCs employing a beat frequency quantization concept have been invented for the direct acquisition of sub-mV input signals. A variety of physiological signals (e.g. ECG, EEG and EOG) can be acquired without the use of any signal pre-conditioning amplifier.

The third contribution of this thesis is the invention of novel digital-intensive time amplifiers for achieving TDCs with high time resolution and wide input range. Two different TDCs based on the time amplifier techniques have been implemented for generating low in-band phase noise by utilizing them in digital PLL. A TDC-less digital PLL has been also proposed as the fourth contribution of this thesis. The fractional sub-sampling circuit improves the PLL in-band noise and suppresses the spur noise due to the limit cycle behavior of bang-bang digital PLL.

As the final contribution, a reliability issue of digital PLL has been analyzed and a novel aging-tolerant DCO based digital PLL has been implemented. The proposed

dynamic element matched DCO circuit improves the DCO life time by effectively reducing the impact of hot carrier injection (HCI) stress on the DCO circuit.

The organization of this thesis is as follows. Chapter 2 describes the design of supply noise sensitivity tracking PLL for optimizing processor power and performance. Chapter 3 and 4 presents VCO-based ADC circuit design techniques utilizing BF-based quantizers for biomedical frontends. Chapter 5 discusses the design of TDC circuits with switched-ROSC based TA. An adaptive pulse-train time amplifier based noise-shaping TDC and the use of the TDC circuit in a digital PLL is described in Chapter 6. Chapter 7 presents a spur-free bang-bang digital PLL based on the fractional sub-sampler phase detector. Chapter 8 describes an aging-tolerant digital PLL by utilizing the proposed dynamic element matched DCO circuit. Chapter 9 concludes this thesis.

Chapter 2. Adaptive PLL for Optimal Processor Power and Performance

An adaptive PLL that maximize the timing compensation between clock and data, commonly referred to as the clock data compensation effect, is demonstrated in 32nm SOI CMOS. We achieved optimal clock data compensation across a wide range of PVT and operating conditions by implementing an automated supply-noise sensitivity tracking loop.

2.1 Introduction

Power supply noise is considered as one of the major performance limiting factors of modern low-voltage and high-performance microprocessors [1]. Traditionally, off-chip and on-chip decoupling capacitors have been used to regulate the supply noise across a wide range of frequencies [2]. Supply grid optimization and noise tolerant clock network designs [3]-[8] have also been widely used to minimize the impact of power supply noise on processor performance. Recently, circuit based supply noise cancellation techniques such as active decoupling capacitors [9], active damping resistors [10], and switched capacitor circuits [11] have been proposed for minimizing the supply noise and thereby reducing the processor power consumption.

Supply noise caused by the resonance between the package/bonding inductance and on-die decoupling capacitance, which is also referred to as first-droop noise [2], is generally believed to be the dominant supply noise source in modern high performance systems [8][11] and has the largest voltage droop magnitude as shown in Fig. 2.1(a). The magnitude of the resonant noise can reach up to 10-15% of the nominal supply

voltage while its fundamental frequency typically resides between 40MHz and 300MHz [12] as shown in the supply network impedance of Intel's Nehalem microprocessor in Fig. 2.1(b). Recently, researchers have revealed an intrinsic timing compensation phenomenon between the clock and the data signals (commonly referred to as the Clock-Data Compensation or CDC), which could alleviate the impact of resonant supply noise on processor speed [2][13]. Adaptive clocking schemes have been proposed to maximize the CDC effect including a new clock tree design in [2] where the amplitude and phase of the resonant noise seen by the clock buffers are modified using RC filtered clock buffers. Another promising approach to enhance the CDC effect is to systematically couple the supply noise into the PLL output clock using programmable resistor [13] or capacitor banks [14]. However, previous adaptive PLLs rely on an exhaustive search algorithm to find the optimal CDC parameters, which involves a cumbersome and time-consuming calibration process. Moreover, once programmed, these parameters cannot be adjusted making the design susceptible to the operating condition changes and other PVT variations and aging effects. In addition, the extra passive devices and analog circuitry in the CDC modulator increases the PLL area and worsens the loop stability.

In this paper, we propose an Automatic Supply-noise Sensitivity Tracking (ASST) PLL that addresses all the above-mentioned issues. The proposed PLL aligns the local clock edge with the datapath signal using an on-the-fly supply-noise sensitivity tracking loop based on a tunable critical path monitor circuit that detects timing errors. In addition to the optimized performance and power consumption by using the automatic

tracking loop, the PLL area is significantly reduced by utilizing, for the first time, an ultra-dense deep trench capacitor in the loop filter.

The remainder of this paper is organized as follows. Section II describes the impact of resonant supply noise on the processor performance and provides a brief introduction to the CDC effect. A mathematical derivation of the optimization of the CDC effect based on the proposed supply-noise sensitivity tracking scheme is presented in Section III. Section IV shows the implementation details of the 32nm adaptive PLL test chip including the supply noise sensitivity tracking loop and the dense deep trench capacitor based low area PLL loop filter. The test chip measurement results are given in Section V and a summary is provided in Section VI.

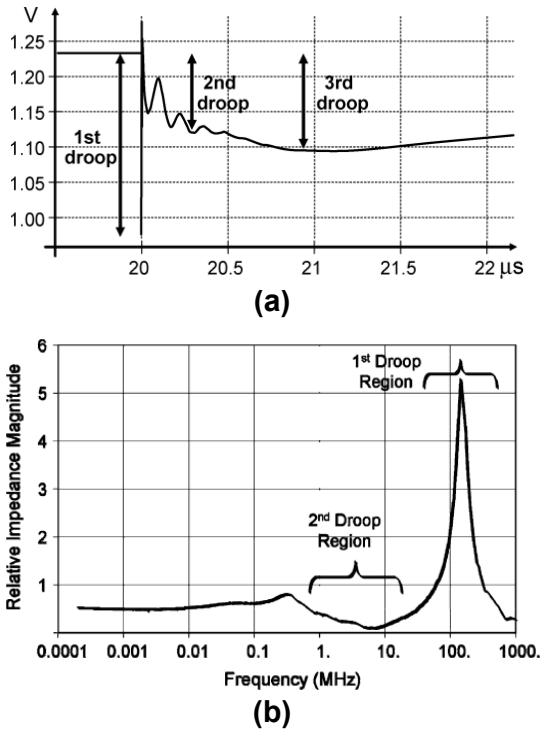


Fig. 2.1. (a) Supply noise waveform of a typical high performance processor. It contains multiple droop components owing to the different resonance frequencies of a power supply network [2]. (b) Power supply network impedance response for Intel's Nehalem^{TM} processor [13].

2.2 Resonant Supply Noise and Clock Data Compensation

Resonant supply noise has significant implications for improving chip performance and power consumption. Reducing the resonant supply noise allows processors to operate at a higher frequency for a given supply voltage as shown in Fig. 2.2 (left). Similarly, power consumption of a processor can be reduced since the same performance can be met using a lower supply voltage (Fig. 2.2, right). To minimize the resonant supply noise, the power supply network in modern processors must have extremely low impedance values (e.g. few milli-ohms) by employing large amounts of on-chip decoupling capacitors, but this incurs a significant area and leakage overhead. Furthermore, integrating more on-chip decoupling capacitors provides diminishing returns in terms of processor performance as experimentally shown in [15].

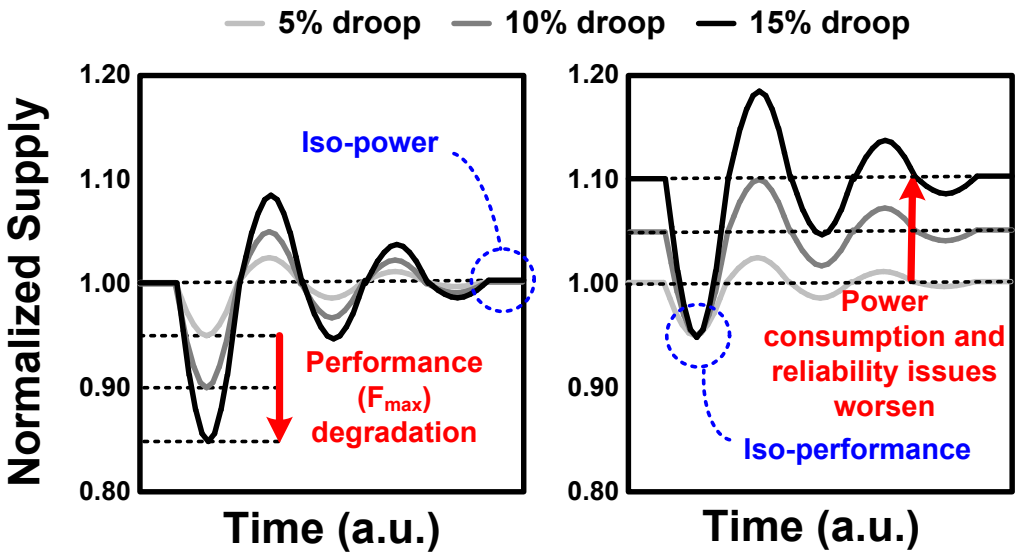


Fig. 2.2. Impact of resonant supply noise on processor F_{max} (left) and power consumption (right) for different first droop noise amplitudes.

The timing compensation between the clock period and the datapath delay can be utilized to overcome the resonant noise issue at a much lower overhead. Fig. 2.3 illustrates this in the context of a conventional and adaptive PLL [13][14]. Unlike the conventional view depicted in Fig. 2.3 (left) where the clock period is constant irrespective of the supply noise, processor performance may not suffer as much with the beneficial timing compensation effect between the datapath delay and the clock period as shown in Fig. 2.3, center. The clock delivered to the local datapath is affected by the resonant supply noise while it is travelling through the clock distribution network and therefore, the clock period is modulated. The clock period modulation is a result of two consecutive clock edges travelling through the clockpath experiencing different delays under resonant supply noise. For example, during the supply noise upswings, the second clock edge travels faster than the first resulting in a compressed clock period. Similarly, the clock period stretches out during supply noise downswings. The net effect is the modulated clock partially compensating for the datapath delay variation, alleviating the impact of resonant supply noise (Fig. 2.3, center). However, the dependence of the clockpath and datapath delays on supply noise are different and therefore, the intrinsic CDC can offer only limited timing relief.

In this paper, we propose a closed loop system that can track the optimal supply sensitivity parameter using the bit error information from a critical path replica circuit. The closed-loop tracking technique allows the processor to operate at its peak energy-efficiency point by aligning the local clock period with the datapath delay as shown in Fig. 2.3, right. By modulating the PLL output clock period while carefully accounting for the clock period modulation in the clockpath, timing failures in the datapath can be

avoided as shown in Fig. 2.4. Eventually, this leads to a lower power consumption under iso-operating frequency or a higher operating frequency under iso-power consumption.

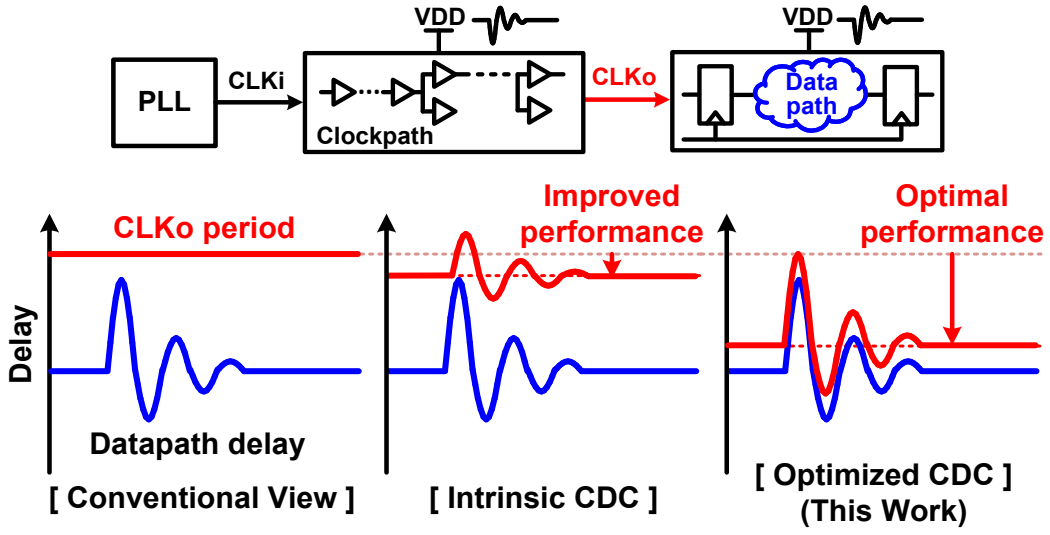


Fig. 2.3. Intrinsic and enhanced CDC effects and their impact on processor performance.

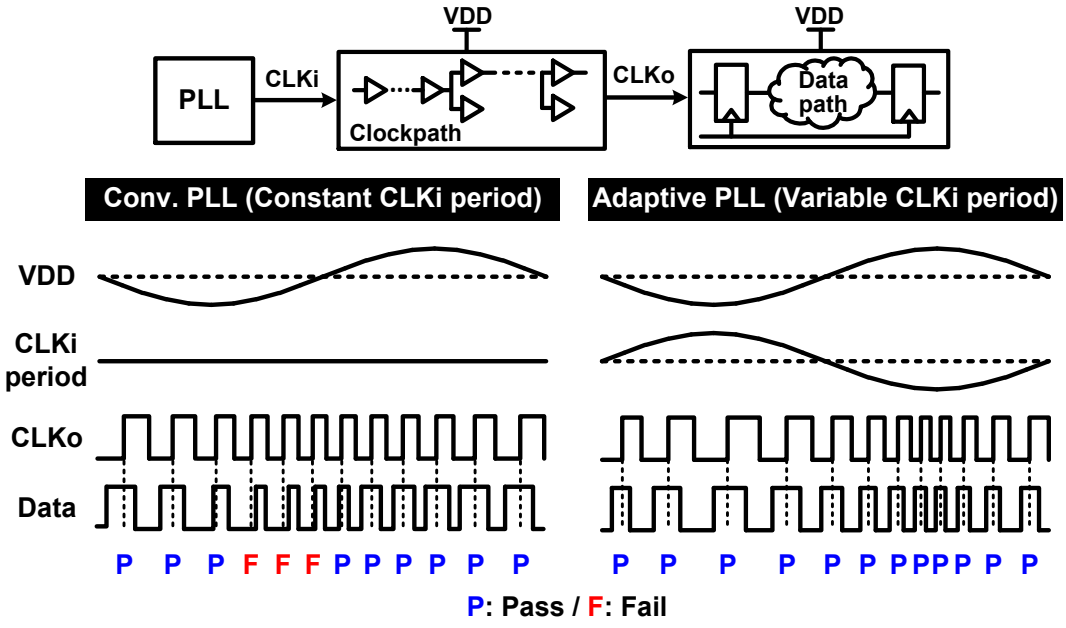


Fig. 2.4. Intrinsic CDC effect when using a conventional PLL (left). Enhancing CDC effect by employing an adaptive PLL (right).

2.3 PLL Supply-Noise Sensitivity Tracking for Optimizing CDC Effect

In previous adaptive PLL designs, CDC parameters such as phase shift and sensitivity were determined through an exhaustive search which can be cumbersome and time-consuming [14]. Another shortcoming of previous designs is that the CDC parameters could not be updated after the one-time calibration has been performed. This would make the CDC efficiency vary depending on the chip operating mode and PVT parameters. In this work, a single parameter (i.e. PLL supply-noise sensitivity) based CDC optimization is proposed to address these issues.

2.3.1 Mathematical Derivation of Optimal CDC Effect

Adaptive PLL designs in [14] and [16] enhance the CDC effect by adjusting the supply sensitivity (i.e. change in PLL output frequency or delay with respect to the resonant noise amplitude) and the phase-shift (i.e. phase difference between PLL output and resonant noise). This was achieved by systematically coupling the resonant supply noise to the PLL output clock. Before we cover the circuit design details, we first show the mathematical derivation of optimal CDC parameters. It's worth pointing out that the exact mathematical proof for optimal timing compensation is complicated and provides limited insight, so instead a simplified version based on inference is provided here to help the readers understand the basic operation of the proposed adaptive PLL.

For the mathematical modeling of the CDC effect, let's first consider a reference delay line with a nominal delay of T_{NOM} and a supply sensitivity of S_{REF}. Here, supply sensitivity is defined as the change in the reference delay under an AC supply noise,

normalized to the amplitude of the supply noise. For example, if the supply voltage has an AC noise of $V_{NOM} - 0.1V*\sin(2\pi ft)$ and the resulting delay change is $T_{NOM} + 1ns*\sin(2\pi ft+\theta)$, the supply sensitivity is 1ns/0.1V = 10 ns/V. Using the concept of a reference delay line and assuming that its delay is short enough that the phase difference between the supply noise and delay is negligible, we can model the delay of an arbitrary signal traveling through a clock path or data path. To simplify the modeling, the resonant supply noise in our analysis is assumed to be a single-tone sinusoidal function $V_{SUPPLY} = V_{NOM} - V_{NOISE}\cdot\sin(2\pi ft)$ where V_{NOM} is the nominal supply voltage and V_{NOISE} is the amplitude of the resonant noise having a frequency of f. Then, the time-varying delay of the reference delay line under resonant supply can be modeled as

$$T_{REF} = T_{NOM} + S_{REF}\cdot V_{NOISE}\cdot\sin(2\pi ft). \quad (1)$$

where T_{NOM} is the nominal delay of a reference delay line at V_{NOM} and S_{REF} is the supply sensitivity of the reference delay line.

In order to calculate the period of the local clock under resonant noise, we need to know the period of the clock generated by the adaptive PLL as well as the change in the clock period due to the resonant noise in the clock path. The later component can be calculated by taking the difference in the clock path delays of two consecutive clock edges, i.e. the preceding 1st edge and the subsequent 2nd edge. That is, the local clock period can be derived using the following expression.

$$T_{LOCAL} = T_{PLL} + (T_{CP\text{-}2nd} - T_{CP\text{-}1st}) \quad (2)$$

Now, let us define the time instances pertaining to the clock path and delay path delays needed for the rest of the derivation:

t time when the 2nd clock edge arrives at the datapath

(or time when the datapath signal arrives at the sampling flip-flop)

$t - T_{DP}$ time when the datapath signal was launched and entered the datapath

$t - T_{LOCAL}$ time when the 1st clock edge arrives at the datapath

$t - T_{CP\text{-}2nd}$ time when the 2nd clock edge enters the clockpath

$t - T_{CP\text{-}2nd} - T_{PLL}$ time when the 1st clock edge enters the clockpath

Using the general delay expression given in (1) and the timing points defined above, we derive the period of an adaptive PLL's output clock (i.e. T_{PLL}) under resonant supply noise by integrating (1) from $t - T_{CP\text{-}2nd} - T_{PLL}$ to $t - T_{CP\text{-}2nd}$:

$$T_{PLL} = T_{PLL\text{-}NOM} + (S_{PLL} \cdot V_{NOISE}/2\pi f) \cdot [\cos\{2\pi f(t - T_{CP\text{-}2nd} - T_{PLL})\} - \cos\{2\pi f(t - T_{CP\text{-}2nd})\}]. \quad (3)$$

Here, $T_{PLL\text{-}NOM}$ is the PLL clock period at a nominal supply voltage of V_{NOM} and S_{PLL} is the supply noise sensitivity of the adaptive PLL. To derive the local clock period T_{LOCAL} in (2), now we need to calculate the clockpath delay of the 1st and 2nd clock edges, namely $T_{CP\text{-}1st}$ and $T_{CP\text{-}2nd}$. The delay of the 1st clock edge travelling through the clockpath is the time integration of (1) from $t - T_{CP\text{-}2nd} - T_{PLL}$ to $t - T_{LOCAL}$ and expressed as

$$T_{CP\text{-}1st} = T_{CP\text{-}NOM} + (S_{CP} \cdot V_{NOISE}/2\pi f) \cdot [\cos\{2\pi f(t - T_{CP\text{-}2nd} - T_{PLL})\} - \cos\{2\pi f(t - T_{LOCAL})\}]. \quad (4)$$

Here, S_{CP} is the supply sensitivity of clockpath and $T_{CP\text{-}NOM}$ is the nominal clockpath delay at a supply voltage of V_{NOM}. Likewise, the clock path delay of the 2nd clock edge is the time integration of (1) from $t - T_{CP\text{-}2nd}$ to t

$$T_{CP\text{-}2nd} = T_{CP\text{-}NOM} + (S_{CP} \cdot V_{NOISE}/2\pi f) \cdot [\cos\{2\pi f(t - T_{CP\text{-}2nd})\} - \cos\{2\pi ft\}]. \quad (5)$$

Since deriving an analytical expression for optimal CDC is quite involved, we will use the inference method to find the optimal solution by first assuming that supply sensitivities of the PLL and clockpath are identical (i.e. $S_{PLL} = S_{CP}$). Using (2)-(5), we are now able to express the local clock period as

$$T_{LOCAL} = T_{PLL\text{-}NOM} + (S_{CP} \cdot V_{NOISE}/2\pi f) \cdot [\cos\{2\pi f(t - T_{LOCAL})\} - \cos(2\pi ft)] \quad (6)$$

which shows that the local clock period under the optimal CDC effect is simply the time-varying delay of the 2nd clock edge travelling from $t - T_{LOCAL}$ to t.

Similar to the derivation of the clock period, we can calculate the time-varying delay of the local datapath by integrating (1) in time from $t\text{-}T_{DP}$ to t:

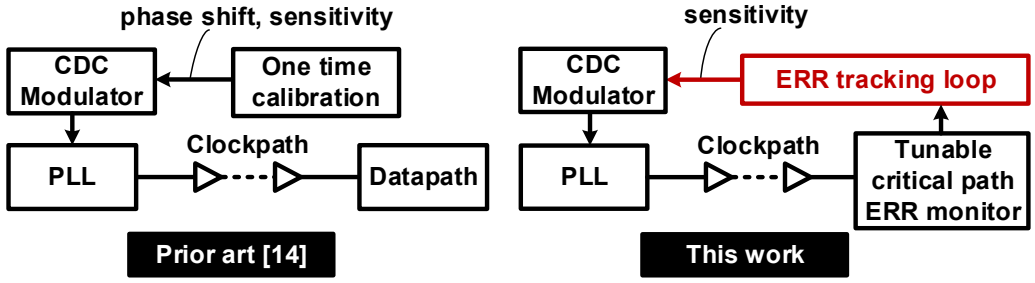
$$T_{DP} = T_{DP\text{-}NOM} + (S_{DP} \cdot V_{NOISE}/2\pi f) \cdot [\cos\{2\pi f(t - T_{DP})\} - \cos(2\pi ft)]. \quad (7)$$

Similarity between equations (6) and (7) suggests that the local clock period and datapath delay react in similar ways in the presence of resonant supply noise. The main discrepancy arises from the fact that the supply sensitivity parameters appearing in the two equations are different. That is, S_{CP} is used in (6) while S_{DP} is used in (7). Both numerical and circuit simulations show that the impact on timing compensation effect is negligibly small (see section III-C) and hence, we can conclude that the two time-varying equations can be aligned closely by simply making the supply sensitivity of the PLL the same as that of the clockpath.

2.3.2 Proposed PLL Supply-Noise Sensitivity Tracking Loop

Based on the mathematical derivation described in the previous section, we propose a scheme in which the optimal CDC effect is achieved using a single parameter (i.e. PLL supply-noise sensitivity) control. The key benefit of a single parameter control over

a multi-parameter one [14] is that it enables a simpler closed-loop system for tracking the optimal configuration (Fig. 2.5). By employing a tracking based calibration scheme and periodically updating the supply-sensitivity parameter, we can achieve the optimal performance improvement irrespective of the processor operating condition. Simulated results in Fig. 2.6 show a 7.8% higher processor F_{max} across a wide range of PVT parameters for the proposed ASST PLL as compared to the previous adaptive PLL design which has a fixed supply-sensitivity. The detailed circuits and an analysis on the proposed closed-loop system will be described in section IV.



	# of control parameters	Parameter setting	Passive area
Conv.	None	None	Large
[13]	One (sensitivity)	1D sweep, one time	Small
[14]	Two (phase, sensitivity)	2D sweep, one time	Large
This work	*One (sensitivity)	Closed-loop tracking	Small (C_{trench})

*Key requirement for stable closed-loop tracking

Fig. 2.5. Comparison with prior art. The proposed adaptive PLL employs an error tracking loop that adjusts the amount of supply noise coupled to the PLL output clock period according to the timing error information. Additionally, the PLL area is reduced by utilizing deep trench capacitors in the loop filter.

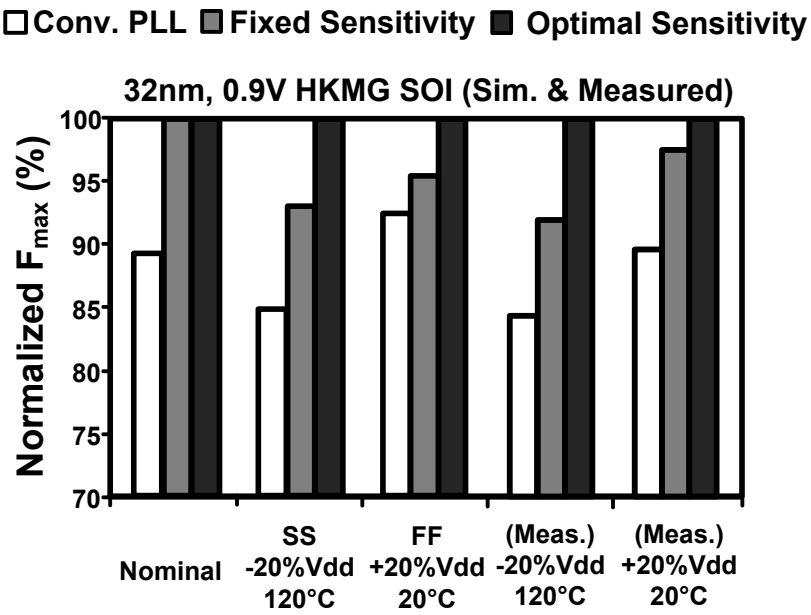


Fig. 2.6. Effectiveness of the proposed PVT tracking loop. The proposed scheme (black bars) can achieve up to a 7.8% higher processor F_{max} compared to a previous one-time calibration scheme (gray bars) under extreme PVT conditions.

2.4 Circuit Implementation In 32nm SOI

2.4.1 Automatic Supply-Noise Sensitivity Tracking Loop

A test chip was fabricated in a 0.9V, 32nm SOI process to verify the ASST PLL operation and the details are given in Fig. 2.7. The PLL consists of building blocks for a typical charge-pump PLL such as a phase frequency detector (PFD), a charge-pump (CP), a loop filter and a VCO, along with special circuits that are part of the supply noise tracking loop. In order to AC-couple the resonant supply noise to the PLL control voltage with constant sensitivity steps, a CDC modulator consisting of two capacitor banks (Cu, Cd) was implemented with each having 63 unit capacitors. Prior to the tracking operation, the delay of the critical path replica was set to its target value using tunable delay stages (Fig. 2.9(b)).

The PLL operation starts by enabling the sensitivity tracking loop in Fig. 2.7 after the PLL is locked. To adaptively control the PLL supply-noise sensitivity, an on-chip error monitor circuit is needed. For this purpose, a replica critical path monitor circuit with a tunable delay (Fig. 2.7) was designed [17]. A bit error monitor enables the error output ERR whenever a timing violation occurs in the critical path replica circuit. This is achieved by comparing the output of the replica path with the correct value (i.e. input of the replica path) using an XOR gate. We have the flexibility to choose between a single error event (=fast but potentially unstable tracking response) or until a certain number of errors has been reached (=slow but smooth tracking response) for updating the supply noise sensitivity. An up/down counter with a binary-to-thermometer code decoder is used to convert bit errors into a sensitivity code. Once the tracking loop is

locked, a digital filter determines the up/down counting direction according to the current bit error information.

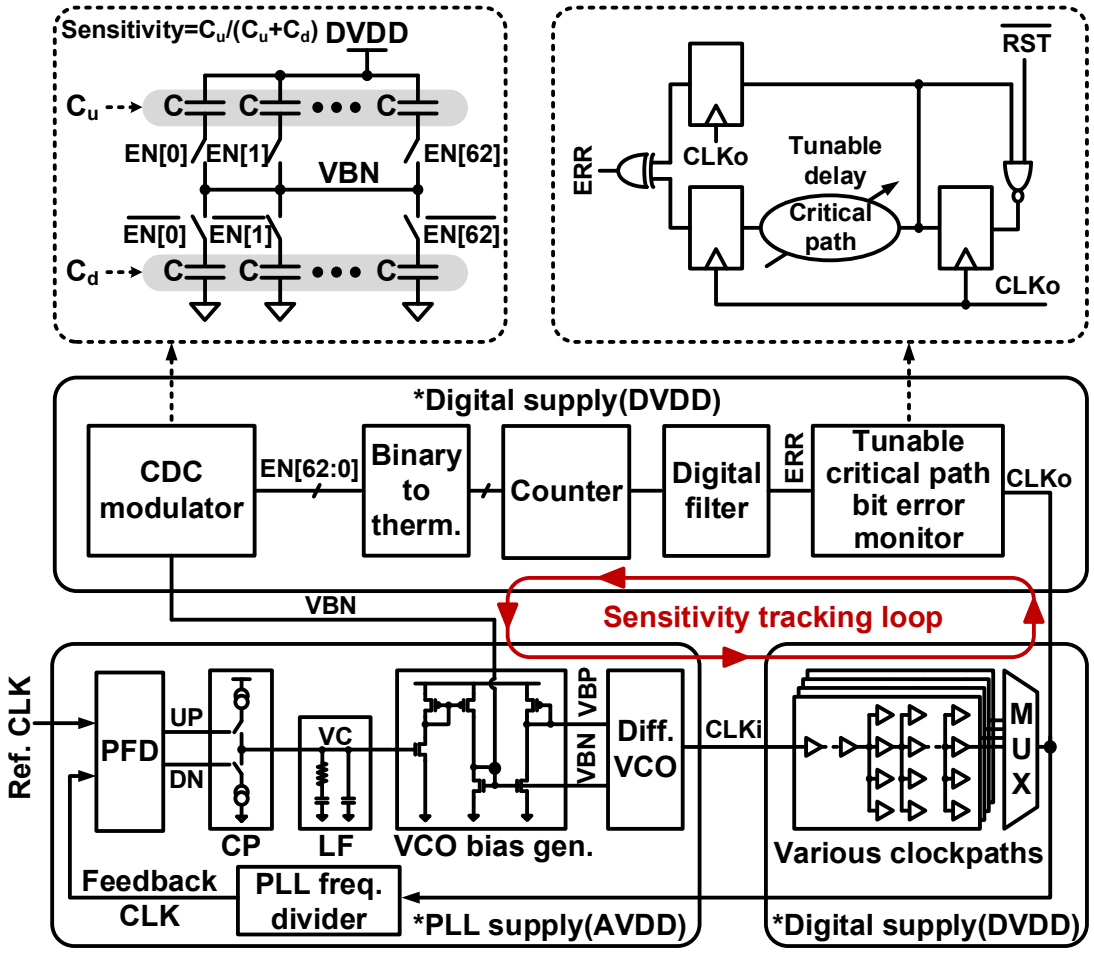


Fig. 2.7. Overall diagram of ASST PLL test chip.

To analyze the stability of the tracking loop, we need to compare the loop latency (or response time) with the sensitivity tracking time (i.e. the time it takes for the loop to reach a steady state). The loop latency consists of three delay components. The first is the delay from the thermometer code to update of the PLL supply-noise sensitivity. The corresponding signal path includes a high-pass filter and a single-stage current mirror in the differential VCO. The second delay is the clockpath delay which is around 1ns. The final delay component comes from the bit error monitor. The sum of the three delay components is approximately 1ns and does not exceed a few nanoseconds even in the worst case when the digital filter is set to accumulate the bit errors. Although the short loop latency opens the possibility of a continuous/instantaneous tracking loop, we feel that the proposed circuit is better suited for periodically calibrating the CDC parameters in real designs. For example, whenever a processor undergoes a change in the supply voltage (e.g. DVFS) or operating mode, we can first activate the tracking loop to update the supply sensitivity and then switch back to a normal mode where the processor operates at its peak F_{max} point. The sensitivity tracking time would be equivalent to many resonant noise periods as shown in the typical response behavior in Fig. 2.15. Considering the negligibly small loop latency (~few nanoseconds) compared to the sensitivity tracking delay (~hundreds of nanoseconds), the loop is considered stable.

2.4.2 Built-in Test Circuitry

A dedicated on-chip resonant noise generation circuit shown in Fig. 2.8 was implemented to test the PLL performance. First, a VCO with an external voltage bias generates the main clock. Various clock patterns such as a continuous clock, pulsed clock, or random clock can be created using a frequency divider and a clock synthesis block. The noise amplitude can also be conveniently controlled using the numerous noise injection NMOS devices that can be individually activated using a 5 bit binary code. Each NMOS device induces a fixed current spike and by activating a number of them, we can achieve a realistic resonant noise amplitude. The flexibility of this design allows us to test the PLL for a wide range of resonant noise patterns and amplitudes. Traditionally, PLL performance is characterized by directly connecting the output signal to a high speed sampling oscilloscope or to a BER measurement equipment. In this work, a simple BER measurement circuit was included in the test chip that allows us to monitor the BER in the critical path replica block using a simpler setup. It consists of a 10-bit counter and a 10-to-1 digital multiplexer (Fig. 2.9(a)). We measure the average period of the error output and compare that against the PLL clock frequency to calculate the BER without an extensive test setup [14].

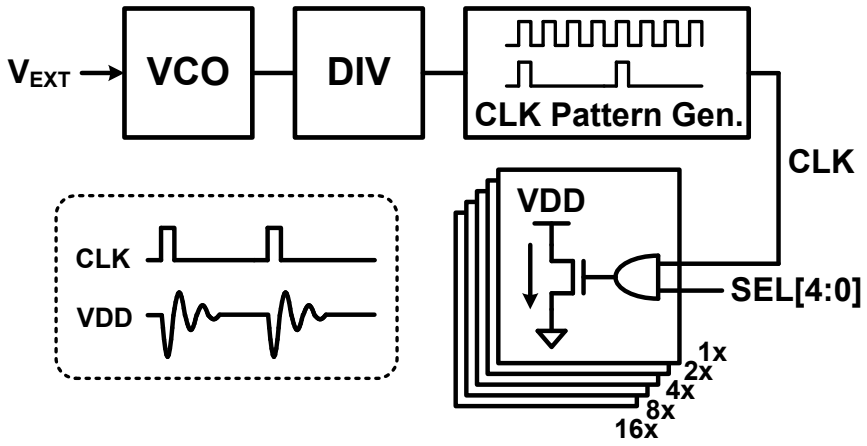


Fig. 2.8. On-chip resonant noise generation circuit.

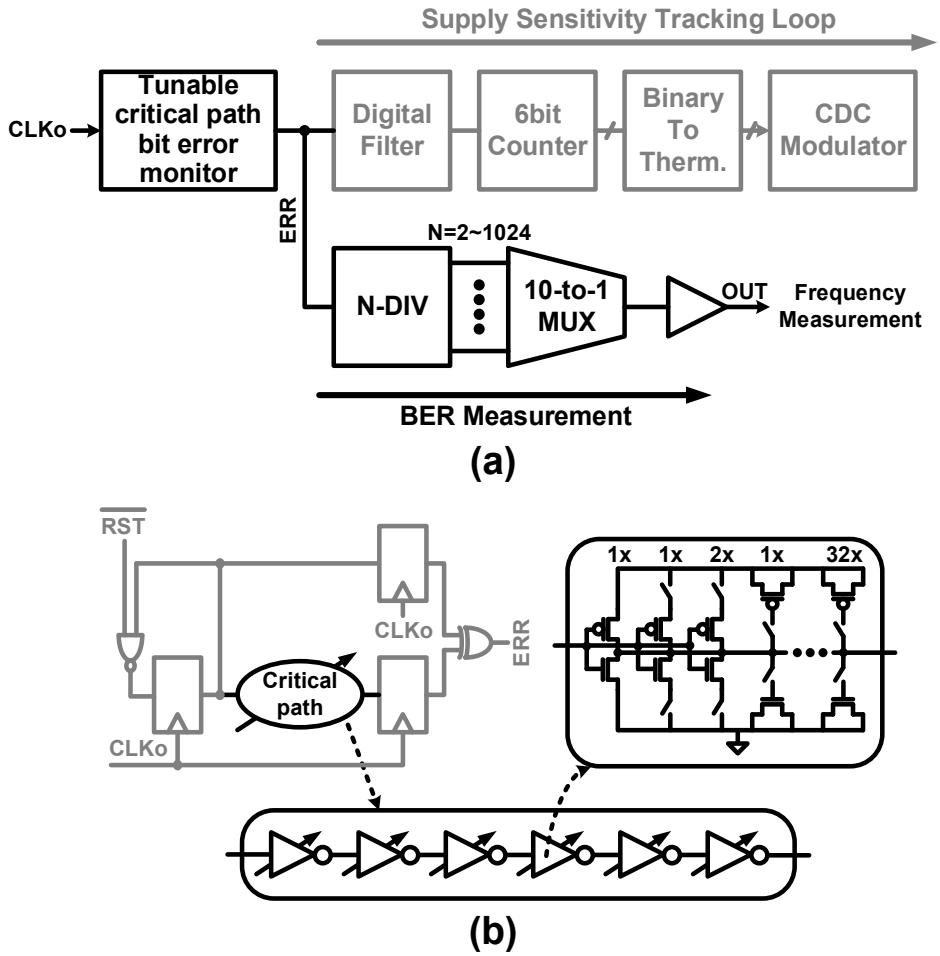
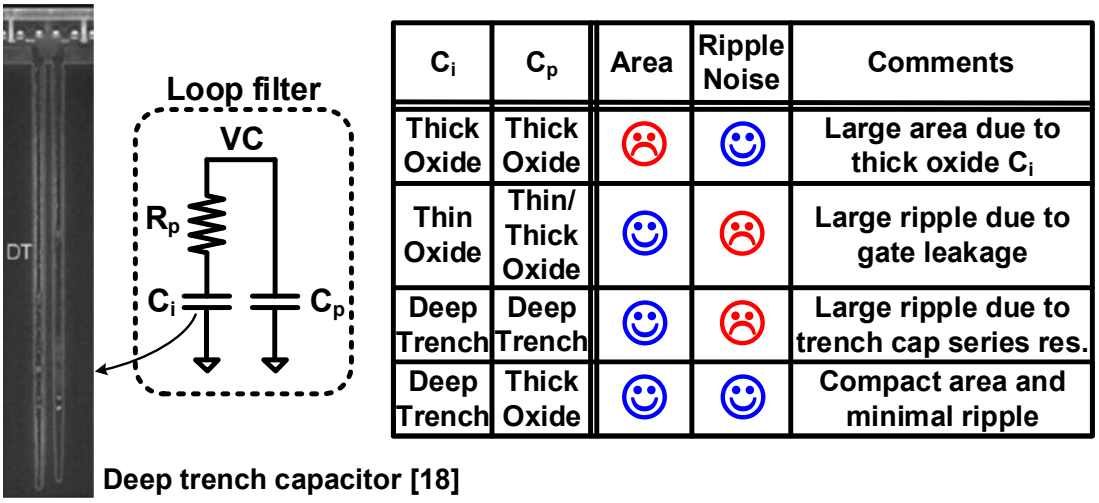


Fig. 2.9. (a) On-chip BER measurement circuit. (b) Critical path circuit with tunable delay.

2.4.3 Deep Trench Capacitor Based Loop Filter

The proposed ASST PLL effectively utilizes deep trench capacitor technology, originally developed for embedded DRAM cells [18]. The capacitance density is approximately two orders of magnitude higher compared to that of a thick oxide MOS capacitor (i.e. default option for most traditional PLLs) while the tunneling leakage is negligible due to the thick dielectric layer. Note that only the area-dominating integrating capacitor (C_i in Fig. 2.10) was implemented using a deep trench capacitor because the relatively high series resistance of trench capacitors limits their ripple rejection capability when used as a third-pole capacitor (C_p in Fig. 2.10). This was confirmed through AC and transient simulations. As is shown in Fig. 2.11, the deep trench capacitor has 23dB lower high frequency noise rejection capability and the transient PLL locking simulation result shows a 15x larger ripple voltage when it is used as a ripple rejection capacitor for the PLL. Measured results in Fig. 2.12 show no noticeable difference in PLL performance between a deep trench C_i and a thick oxide C_i based loop filter while the former provides a significant reduction in PLL area. Fig. 2.13 compares the area between a thick oxide and deep trench capacitor implementation, showing a 56x reduction in the integrating capacitor area. This translates into a 12.5x reduction in overall PLL area as shown in Fig. 2.19.



C_i	C_p	Area	Ripple Noise	Comments
Thick Oxide	Thick Oxide	☹	☺	Large area due to thick oxide C_i
Thin Oxide	Thin/ Thick Oxide	☺	☹	Large ripple due to gate leakage
Deep Trench	Deep Trench	☺	☹	Large ripple due to trench cap series res.
Deep Trench	Thick Oxide	☺	☺	Compact area and minimal ripple

Fig. 2.10. Loop filter capacitor options and trade-offs.

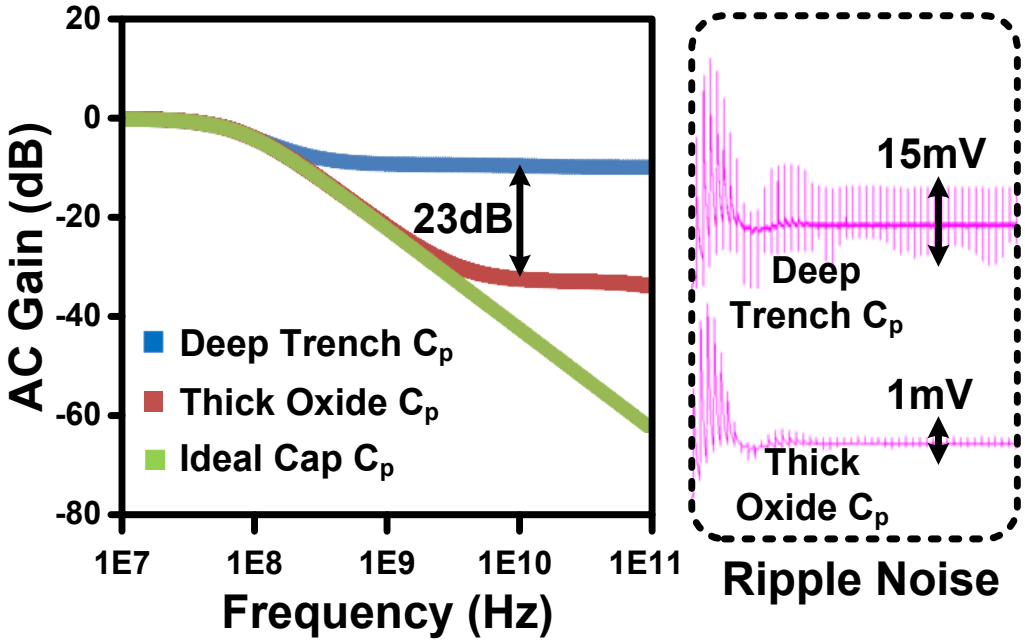


Fig. 2.11. Simulated PLL third-pole AC response and transient ripple noise for deep trench Cp and thick oxide Cp.

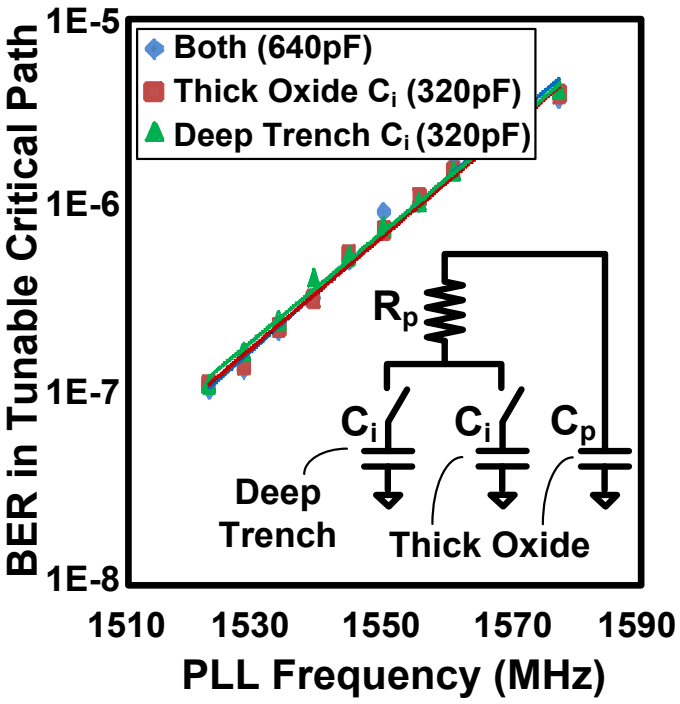


Fig. 2.12. Measured PLL performance for deep trench Ci and thick oxide Ci.

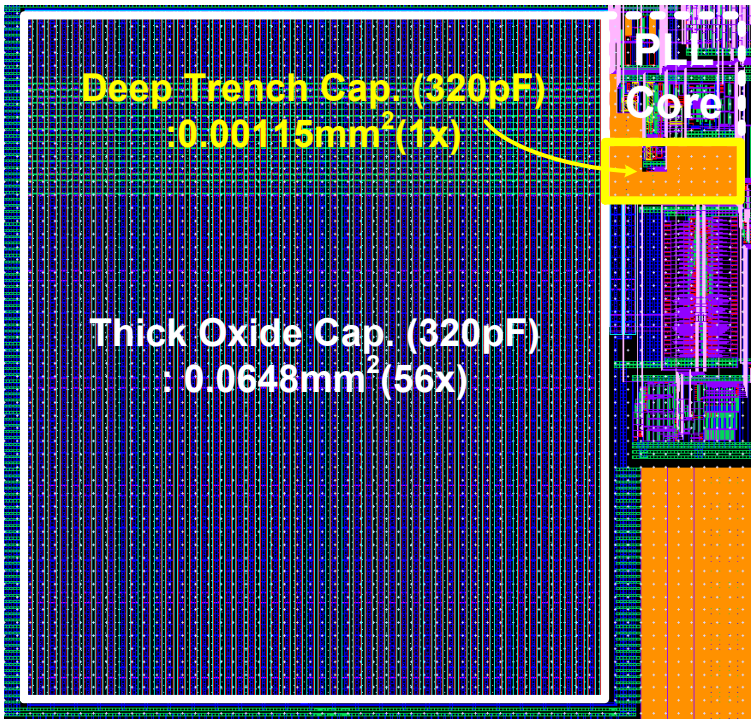


Fig. 2.13. Integrating capacitor area comparison between deep trench and thick oxide capacitor.

2.4.4 Practical Design Considerations

A first-order high-pass filter with a finite capacitance was used in our design to couple the supply noise to the PLL clock [12]. Although the actual phase shift induced by this circuit cannot be completely eliminated, it can be made negligibly small compared to the period of resonant noise frequency (e.g. 40-300 MHz) by choosing proper R and C values. Another potential concern is the discrepancy between the supply sensitivities of the clockpath and the datapath which may have a negative impact on the CDC effect. It is well known that an interconnect-dominated signal path has a lower supply sensitivity compared to a logic-dominated one. To quantify this issue, we simulated the CDC effect for datapaths with different interconnect lengths. Minimum sized inverters were used for this test while the interconnect length was varied from 10μm to 160μm. The results in Fig. 2.14 show an F_{max} improvement from 15.6% to 16.7% using the optimal CDC configuration for interconnect lengths shorter than 40μm. The F_{max} improvement drops for longer wire lengths due to the lower supply sensitivity of the datapath delay. However, the simulation results prove that for practical driver and interconnect configurations, optimizing the CDC effect can provide a significant improvement in processor performance. Finally, mismatch between the supply noise seen by the actual critical path and the replica circuit will affect the efficacy of any CDC enhancement technique including ours. Although local noise does exist, it has been shown that resonant noise is more dominant and affects the entire chip globally. These unique properties make circuit techniques enhancing clock-data compensation (e.g. adaptive PLL in [12][13][15]) highly effective in modern processor designs.

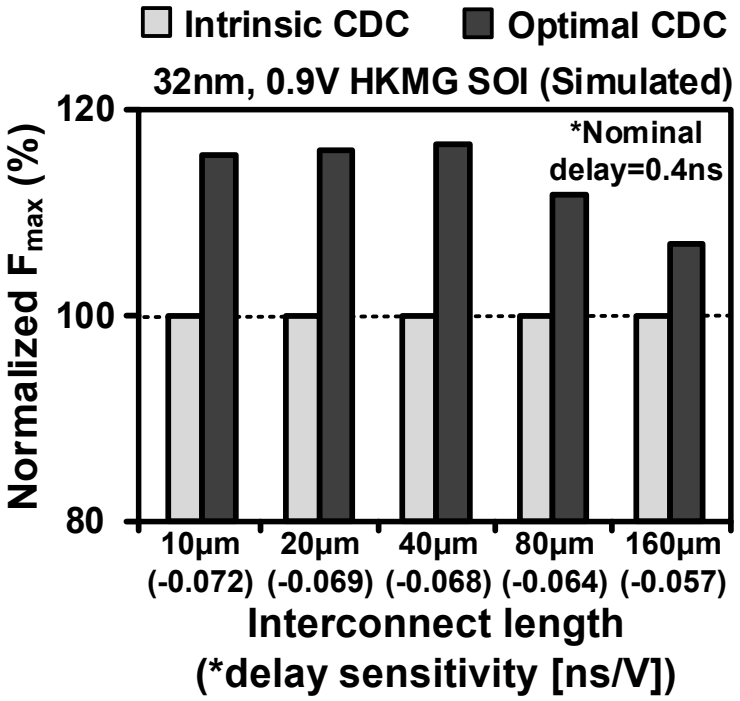


Fig. 2.14. F_{max} simulation results for intrinsic CDC and optimal CDC. For this test, we used minimum sized inverters driving wire interconnects with different lengths.

2.5 Test Chip Measurement Results

For better testability, the PLL reference clock frequency that can be varied from 50MHz to 200MHz while the frequency divider can support different programmable ratios (8, 16, 32 and 64). The VCO output frequency was designed to have a wide frequency range of 1GHz to 3GHz for the same reason. The nominal PLL loop bandwidth was chosen to be 5MHz based on the following design parameters: a charge pump current of 50μA, a K_{vco} of 10GHz/V, an integrating cap of 320pF, a 3^{rd} pole capacitance and resistance of 20pF and 1k-ohm, and a dividing ratio of 16.

Several ASST waveforms along with the measured PLL control voltage are shown in Fig. 2.15 for a typical tracking operation. The ASST PLL starts an initial timing error tracking with a monotonically increasing counter output while bit errors are being generated on-the-fly. The increased counter outputs are decoded to the thermometer code and then the CDC modulator starts to AC-couple the resonant noise to the PLL control voltage. After the initial locking, the tracking loop responds to any changes in the clockpath sensitivity due to voltage/temperature shifts by modifying the sensitivity code (i.e. EN[62:0] in Fig. 2.7).

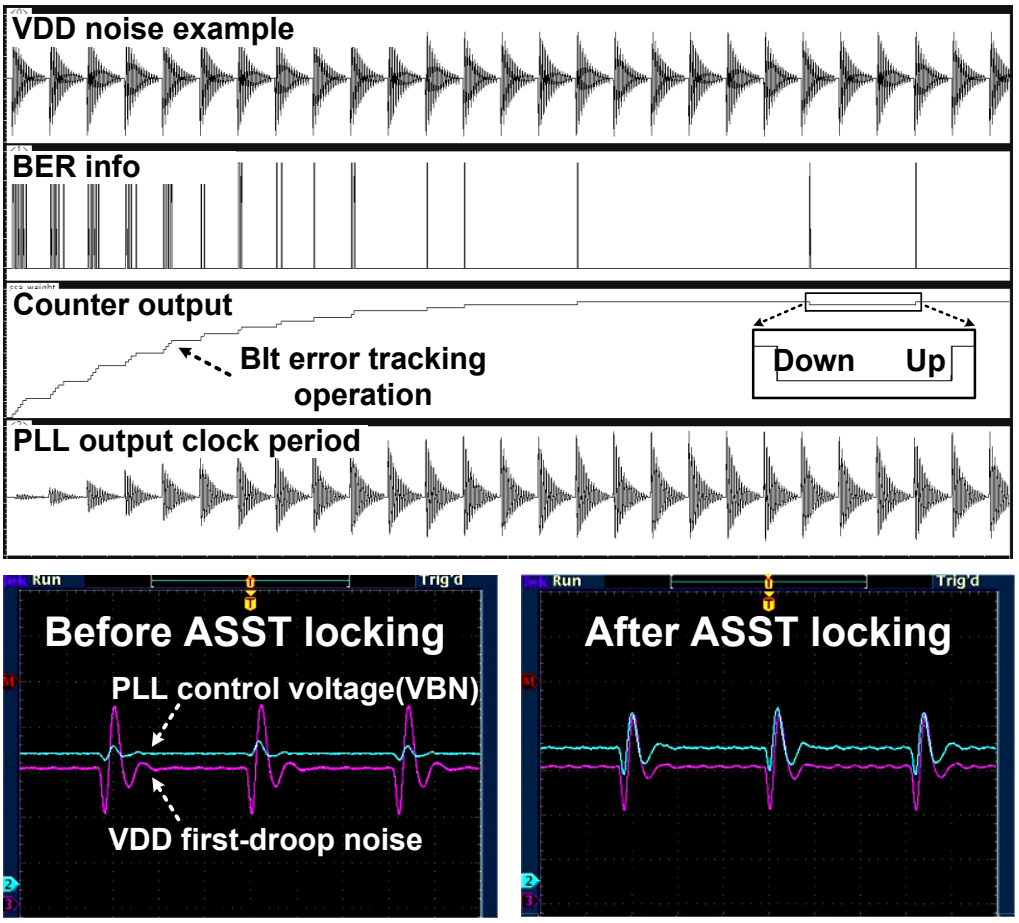


Fig. 2.15. Simulated waveforms (above) and measured VDD and PLL control voltage VBN (below) of the proposed ASST PLL.

To compare the performance between the conventional and ASST PLLs, F_{max} was extracted from the measured BER vs. frequency data [14]. Without loss of generality, we define the maximum operating frequency F_{max} as the frequency when the BER is 10^{-6} [14]. PLL phase noise along with the actual datapath delay fluctuation under supply noise is accounted for in the BER measurements. As shown in Fig. 2.16, a 15% F_{max} improvement was measured with the proposed ASST PLL compared to the conventional PLL when the resonant noise has 100MHz frequency and 90mV amplitude (i.e. 10% of supply voltage). Note that a stronger CDC effect would shift the BER curve to the right

while a lower jitter manifests as a steeper slope. The measured BER curve of the ASST PLL shows a considerable shift compared to the conventional design for a marginal decrease in the slope (i.e. from 7.8E-8/MHz to 6.4E-8/MHz) confirming the effectiveness of the proposed circuits.

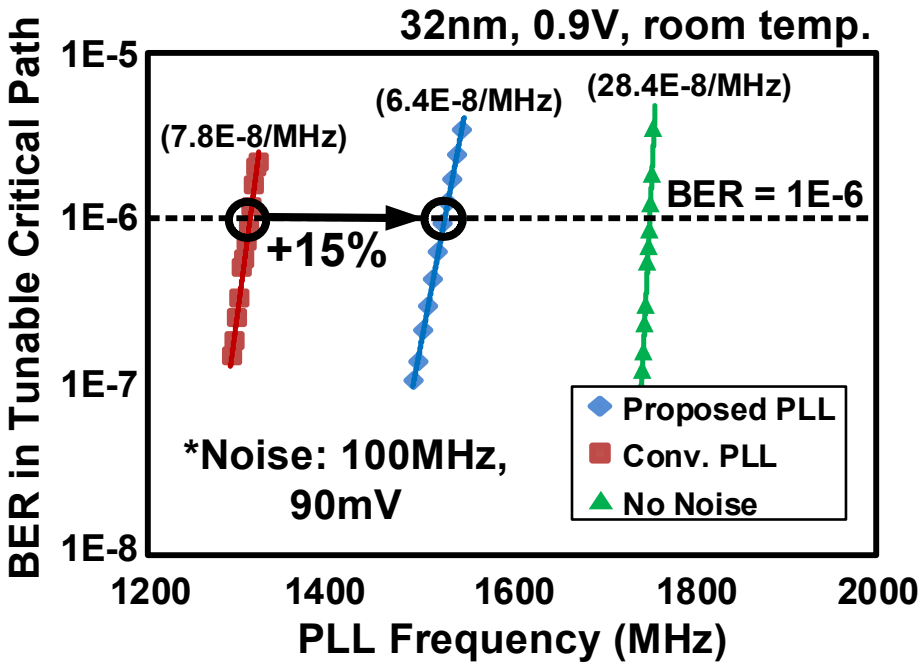


Fig. 2.16. Measured BER versus operating frequency.

The proposed ASST PLL achieves 14.5% to 15.6% higher processor F_{max} compared to a conventional PLL with a constant output clock period under 90mV supply noise amplitude (Fig. 2.17). PLL performance at different noise amplitudes, noise frequencies and clockpath designs has been measured to verify the effectiveness under a wide range of usage scenarios. From the measured results, it is proven that the ASST PLL improves the processor performance proportional to the noise amplitude throughout the resonant noise frequency band regardless of the interconnect types.

Fig. 2.18 shows the measured F_{max} for different supply voltages and PLL types. The proposed PLL achieves an F_{max} of 1.417GHz at a lower supply (0.855V) compared to the conventional PLL (0.9V). This translates into a CV^2f power reduction of 9.8% under iso-performance condition. Finally, the chip microphotograph and feature summary table are given in Fig. 2.19.

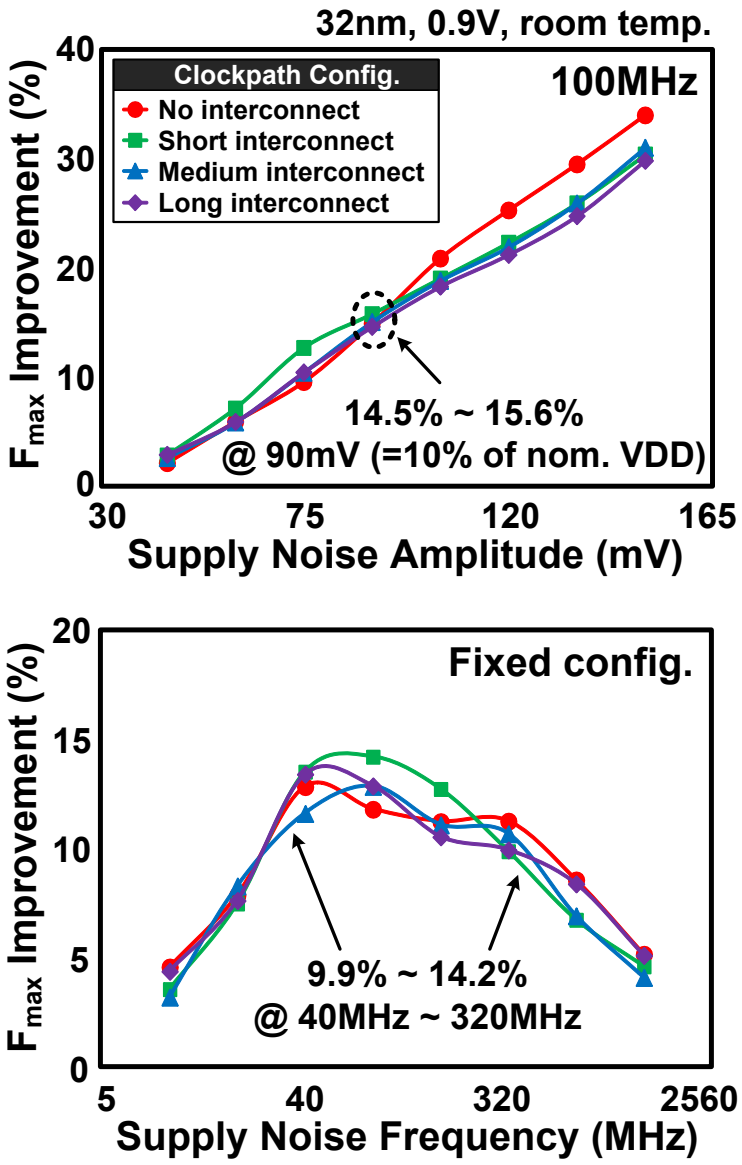


Fig. 2.17. Measured F_{max} vs. noise amplitude and frequency.

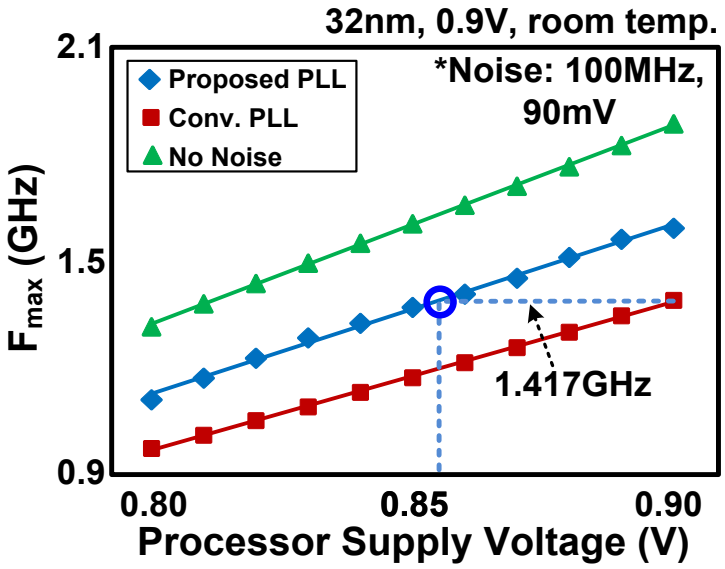
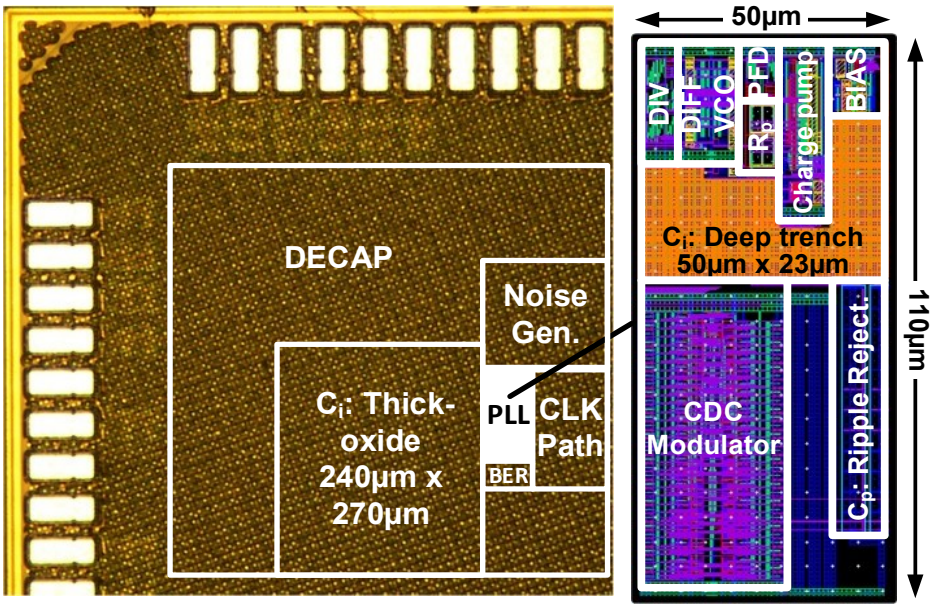


Fig. 2.18. Measured F_{max} vs. processor supply voltage.



Process	32nm HKMG SOI	Deep trench PLL area	0.0055mm²
Supply voltage	0.9V	Conv. PLL area	0.0692mm²
F_{max} improvement (w/ 90mV noise)	14.5%~15.6%	PLL area reduction	*-92.1% **-43.6%
PLL power	3.51mW@2GHz (CP-PLL: 3.15mW, ASST logic: 0.36mW)		

Compared to *single-path PLL and **dual-path PLL with 12:1 ratio [19]

Fig. 2.19. Die photo and feature summary table.

2.6 Conclusion

An adaptive PLL featuring an automated supply-noise sensitivity tracking loop for mitigating the impact of resonant supply noise on processor performance across the wide range of PVT condition was demonstrate in 32nm. The proposed design is based on a single parameter (i.e. supply-noise sensitivity) tracking loop which maintains the optimal CDC configuration by monitoring timing errors from a critical path replica. A test chip was designed in 32nm CMOS to evaluate the proposed circuits. A 14.5% to 15.6% processor F_{max} improvement was achieved for a resonant supply noise amplitude of 10%·VDD. The improved F_{max} can be translated into a 9.8% reduction in power consumption for iso-performance as the proposed PLL allows the system to operate at a lower voltage while meeting the same F_{max} requirement. In addition, the use of dense deep trench integrating capacitors enabled a 92.1% reduction in PLL area compared to a conventional PLL based on a thick-oxide capacitor implementation.

Chapter 3. VCO-Based ADC Employing Beat Frequency Quantizer for Direct Acquisition of Sub-mV Input Signals

This chapter proposes a highly-digital VCO-based ADC employing a beat frequency quantizer for the direct acquisition of sub-mV physiological input signals without the use of signal preconditioning amplifiers.

3.1 Introduction

With the ever-increasing interests and the demands of biomedical systems, there has been a great amount of research for developing compact and energy-efficient analog-to-digital converters (ADCs). For example, the state-of-the-art SAR (i.e. Successive Approximation Register) ADCs have achieved microwatt level power consumption while offering a reconfigurable sampling rate and resolution [20, 21]. While ADC remains a key building block of most of the mixed-signal signal acquisition systems, we do not always benefit from the recent advancements in the ADC designs because of the signal preconditioning amplifiers which have been considered as the essential building blocks in the conventional sub-mV signal acquisition systems which typically dominates the entire power and area consumption of the system.

Fig. 3.1 describes the simplified block diagrams of the conventional and proposed sub-mV signal acquisition system. Multiple stages of signal pre-conditioning amplifiers (e.g. low-noise amplifier (LNA), variable gain amplifier (VGA) in Fig. 3.1) have been used to acquire sub-mV physiological signals such as ECG (electrocardiogram), EEG

(electroencephalogram) and EOG (electrooculogram). They convert the extremely small (i.e. sub-mV) input signals to the outputs with a rail-to-rail voltage swing (Fig. 3.1, upper left). The amplified rail-to-rail analog signals are then converted to multi-bit resolution digital outputs by using conventional ADCs. Typically, multi-channel systems [22, 23] require many amplifiers and the number of those amplifiers increases in proportion to the number of channels while only a single (or few) time-multiplexed signal from those channels is used for the A-to-D conversion (Fig. 3.1, lower). In this work, we present a highly-digital voltage-controlled oscillator (VCO) based ADC employing a beat frequency (BF) quantizer for the direct acquisition of sub-mV input signals with no signal amplifier (Fig. 3.1, upper right). Using the proposed ADC, the overall power and area consumption of the multi-channel systems is kept nearly constant although the number of signal acquisition channels increases.

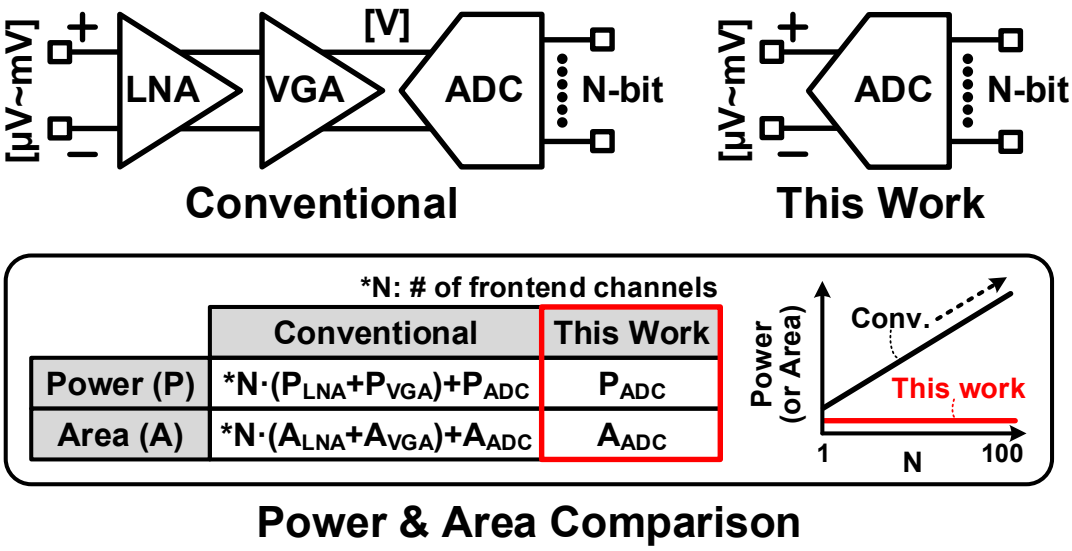


Fig. 3.1. Comparison between the conventional and proposed sub-mV signal acquisition system. Proposed direct (i.e. amplifier-less) signal acquisition system consumes a fixed power and area while that of the conventional system increases in proportion to the number of channels.

The remainder of this chapter is organized as follows. Section 3.2 describes the proposed VCO-based ADC as a candidate for the direct acquisition of sub-mV input physiological signals. Section 3.3 presents the concept of the proposed BF quantization and its high-resolution signal acquisition capability for sub-mV input signals. The implementation details of the 65nm VCO-based ADC test chip is shown in Section 3.4. A prototype multi-channel (i.e. 8-channel) frontend implementation is described with a measurement result in Section 3.5 and Section 3.6 concludes the chapter.

3.2 VCO-Based ADC for Physiological Signal Acquisition

Fig. 3.2 shows different types of common physiological signals from human body with respect to the input voltage range and bandwidth specifications. In this work, we are interested in the acquisition of three representative physiological signals in Fig. 3.2 including ECG, EEG and EOG with the input amplitude ranging from tens of microvolts to several millivolts and the hundreds of hertz maximum bandwidth. To cover the narrow input bandwidth specification of those three signals while consuming a low power, reconfigurable ADCs (e.g. SAR-ADC) have been typically used for biomedical applications. Under the fixed ADC power consumption, the maximum output resolution can be achieved by reconfiguring the sampling rate as low as possible while satisfying the input bandwidth specification.

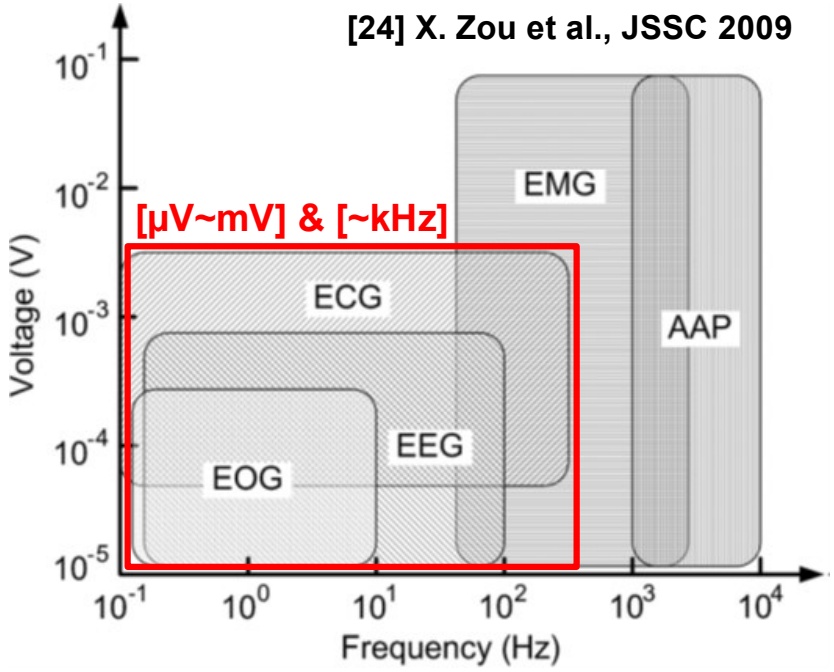


Fig. 3.2. Input range (voltage) and bandwidth (frequency) specifications for common physiological signals [24].

While the reconfigurable and energy-efficient SAR ADCs have been widely adopted to a variety of biomedical applications, VCO-based ADCs have been typically used as a multi-bit VCO-based quantizer for the high resolution continuous-time delta-sigma modulator for wireless applications [25, 26]. However, it also has been recently used as a data converter for the acquisition of neural signal [27]. In addition to the benefits such as the low area and the simple and easily scalable highly digital circuitry, the inherently reconfigurable resolution and sampling rate is another key advantage of using it as a data converter for biomedical systems. While consuming the fixed power consumption (i.e. the fixed VCO frequency), a low resolution ADC with high sampling rate is easily reconfigured to a high resolution ADC with low sampling rate.

Fig. 3.3 highlights the flexibility between the resolution and sampling rate of VCO-based ADC. For instance, a VCO with a voltage-to-frequency transfer characteristic (K_{VCO}) of 1MHz/V (e.g. 0Hz at 0V and 1MHz at 1V) followed by a linear reset counter can only achieve 1bit resolution when it is working at the sampling rate (i.e. the frequency of CK_S in Fig. 3.3) of 1MS/s with 1V input range. However, the 1bit ADC at 1MS/s can be easily reconfigured to a 10bit ADC by lowering the sampling rate to 1kS/s. Note that the ADC resolution is typically degraded in practice due to the nonlinear VCO transfer characteristic. There have been several researches [28, 29] to minimize the impact of the nonlinearity. However, these techniques are only applicable when it is used in conjunction with a complicated and large power consuming (i.e. not desirable for biomedical applications) analog integrators.

Instead of using the rail-to-rail input signal, we can directly apply the original sub-mV input signals to the VCO-based ADC. By doing so, the ADC will not suffer from

the nonlinear VCO transfer characteristic any more due to the improved VCO linearity with the lowered input voltage range. However, the ADC resolution is degraded as much as the amount of input range reduction. The resolution of the 10bit VCO-based ADC at 1kS/s and 1V input range is lowered to 1bit when the input range is reduced to 1mV.

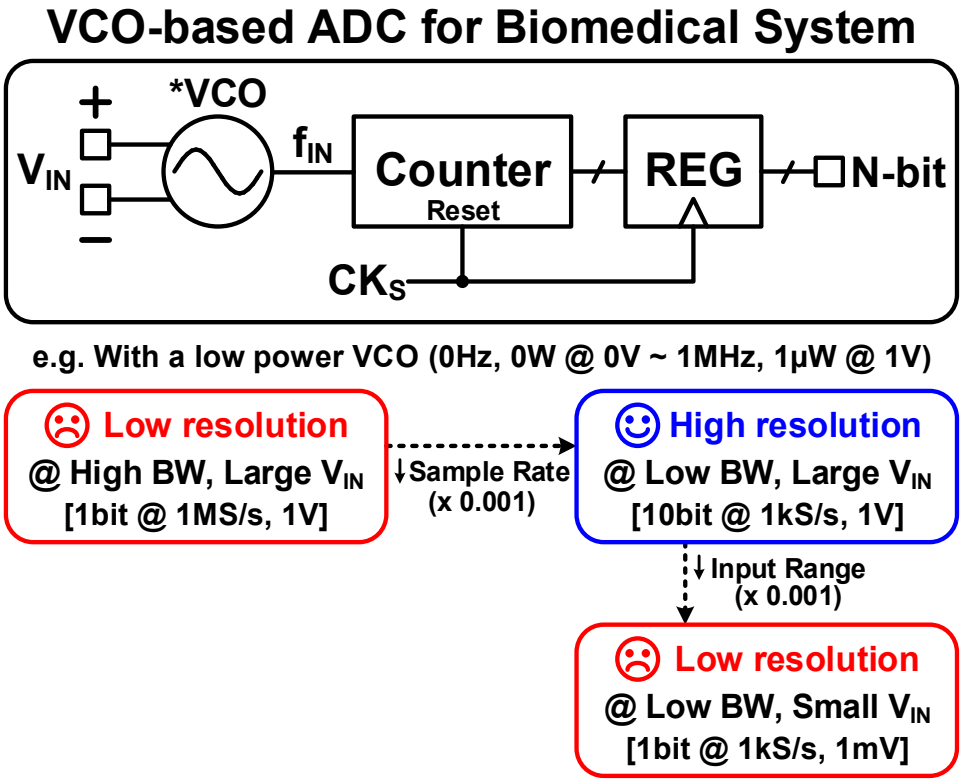


Fig. 3.3. A simple and highly digital VCO-based ADC can be used for conventional biomedical systems with low sample rate due to its flexibility between resolution and sample rate. However, the resolution is still not good enough for the direct acquisition of sub-mV input signal.

To improve the VCO-based ADC resolution at sub-mV input range, we propose a BF quantizer as shown in Fig. 3.4. To achieve a multi-bit resolution (i.e. 6-7 ENOB) VCO-based ADC at low sampling rate (e.g. 1kS/s) and low input range (e.g. 1mV), we first AC-couple the original sub-mV input signals and DC-bias them with a slight bias offset (e.g. 10mV). And then, the voltage signals with the DC-bias offset is applied to the inputs of two VCOs in Fig. 3.4 so that the VCO frequency outputs (f_{IN+} and f_{IN-}) have a slight frequency offset (e.g. 1%) and then measure the change in the frequency difference of them. This way, the detecting resolution becomes much higher than the conventional VCO-based ADC when the input signal change is extremely small (e.g. 0.01%). The detailed explanation on the proposed BF quantization scheme is described in Section 3.3.

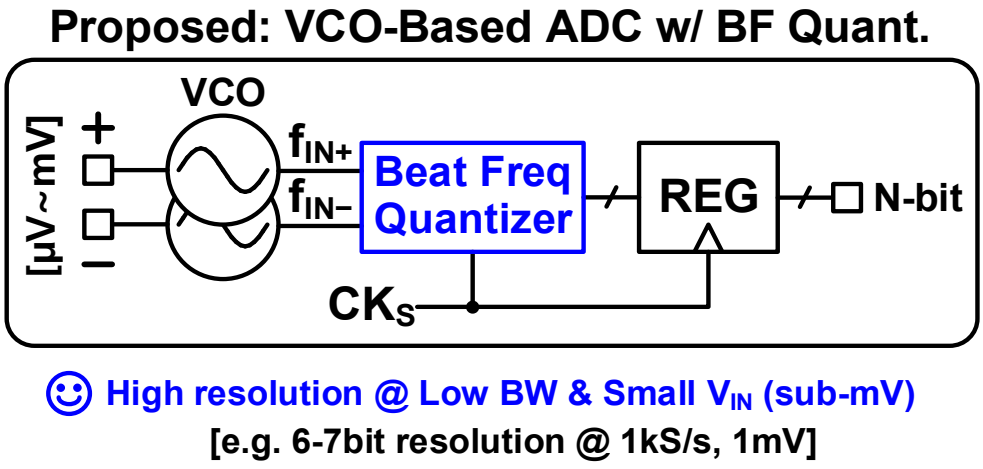


Fig. 3.4. Proposed VCO-based ADC with a BF quantizer for achieving high-resolution with sub-mV input range.

3.3 Beat Frequency Quantization for Direct Acquisition of Sub-mV Input Signals

3.3.1 High Resolution Beat Frequency Quantization

Fig. 3.5 illustrates the operating principle of the BF quantization scheme. Two voltage-controlled ring-oscillators (VCOs) are controlled by input voltage signals (V_{IN+} and V_{IN-}) and the output clocks with the corresponding frequency (f_{IN+} and f_{IN-}) are connected to a BF quantizer. The BF quantizer is consist of a phase detector (D flip flop) and a BF counter which is used for counting the frequency difference between the two input clocks. Note that the two (differential) AC-coupled input signals are DC-biased (Fig. 3.10) so that the input voltage ranges are not overlapped and the minimum difference between the two is being kept larger than the noise floor.

The proposed scheme can achieve a high resolution compared to a simple linear frequency counting method in case where the frequency difference is extremely small. This is possible by measuring a period of the beat frequency clock (D flip-flop output in Fig. 3.5) which is equivalent to the time it takes for the faster signal to pass, catch up and overtake the slower signal again [30]. To understand better how the BF quantizer works, let's consider a scenario in which the initial difference between the two VCO frequencies is 1%. This gives an output count of 100 as it takes 100 VCO periods for the slow and fast signal edges to overlap again. Now, suppose the frequency difference becomes 1.01% due to a small change in the input signal. This translates into an output count of 99 as it takes one less period for the fast signal to catch up with the slower one [30]. The same count change from 100 to 99 would have required a larger frequency change of 1% using the linear counting method implying a significantly lower sensing

resolution. Note that for the beat frequency quantization scheme, the frequency detecting resolution increases exponentially as the two VCO frequencies become closer to each other.

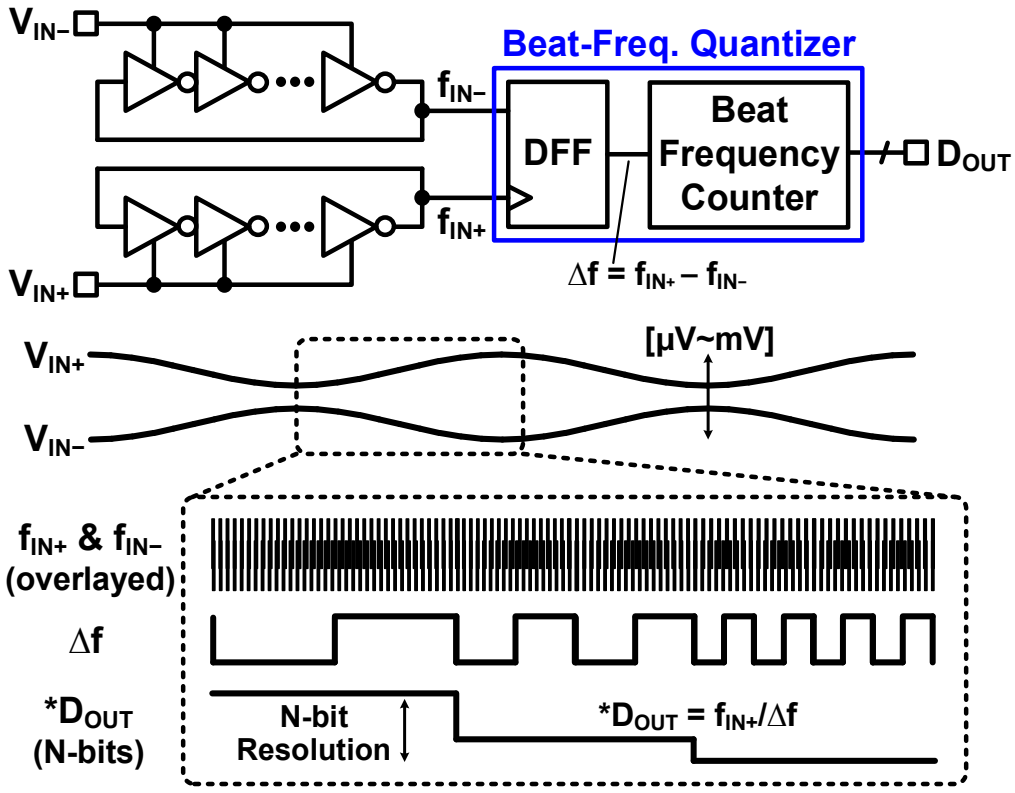


Fig. 3.5. Concept of the proposed beat frequency (BF) quantizer for achieving multi-bit (i.e. 6-7bit) resolution with a sub-mV input signal.

Fig. 3.6 shows input-to-output transfer characteristics of the conventional VCO-based and the proposed BF quantizer. For the same 1% VCO output frequency range (e.g. 0.98 to 0.99 in Fig. 3.6) with respect to the normalized VCO frequency when the counter output is 100, the BF quantizer has the counter output change of 50 (i.e. output varies from 50 to 100) while the conventional one has only 1 count difference at the output (i.e. output varies from 98 to 99). This clearly shows the high resolution frequency sensing capability of the BF quantizer. However, the large output range comes with a nonlinear transfer curve as shown in Fig. 3.6. To fully utilize the beneficial high resolution sensing capability, the nonlinear transfer curve needs to be linearized by using an explicit decoding procedure after the BF quantization.

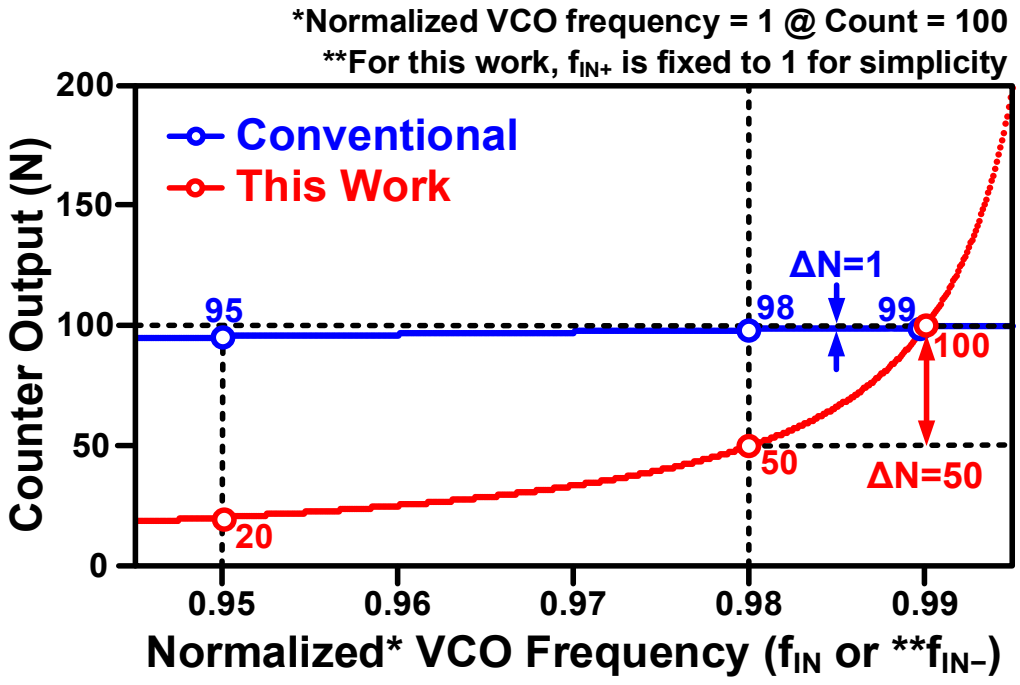


Fig. 3.6. BF quantizer input-to-output transfer characteristic.

3.3.2 Linearization of Beat Frequency Quantizer Output Code

As the simulated transfer curve shows in Fig. 3.6, the BF quantizer has a nonlinear transfer characteristic while having a wide output range. Without the output code linearization, the actual ADC resolution improvement with the BF quantizer will become insignificant compared to the conventional quantizers. To linearize the nonlinear BF quantizer output code and achieve the desirable resolution improvement, we need to decode the nonlinear code to the corresponding linear code based on the BF quantization equation shown in Fig. 3.5 (i.e. $D_{OUT} = f_{IN+}/\Delta f$ where $\Delta f = f_{IN+} - f_{IN-}$). The impact of the BF decoding operation (i.e. a post-processing of the BF-quantizer based ADC output) based on the simple BF quantization equation is illustrated in Fig. 3.7. After the post-processing, the raw ADC output with a low resolution (e.g. 3-4ENOB) due to the nonlinear ADC transfer characteristic is converted to the higher resolution (e.g. 6-7ENOB).

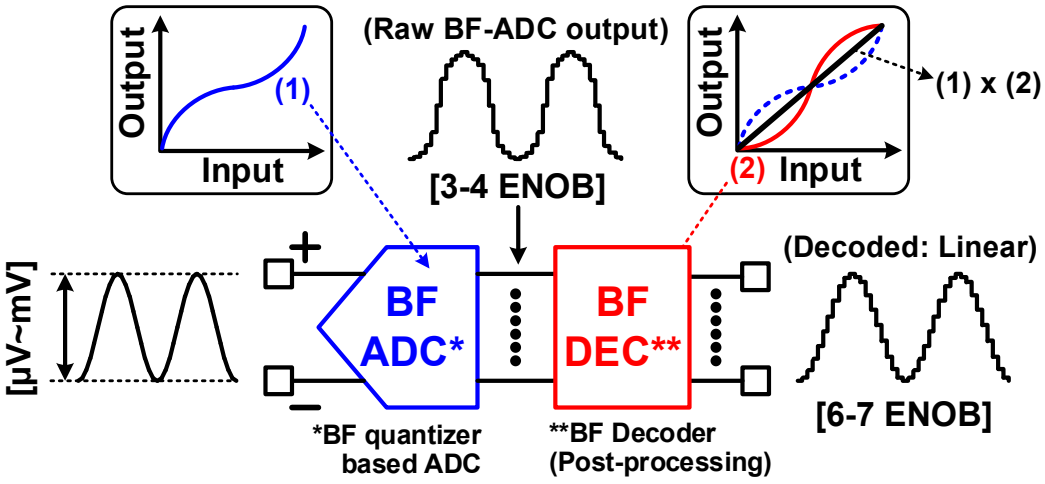


Fig. 3.7. Beat frequency decoding for linearizing the nonlinear BF quantizer input-to-output transfer characteristic.

Fig. 3.8 shows the simulated BF quantizer input-to-output transfer characteristic and the corresponding quantization error after decoding. The transfer curve is linearized while having the same resolution distribution throughout the input range. The quantizer resolution becomes lower (or higher) when the difference between the two frequencies (f_{IN+} and f_{IN-}) is larger (or smaller). As a consequence, the BF quantization error decreases as the frequency difference become smaller (i.e. toward the right on the x-axis).

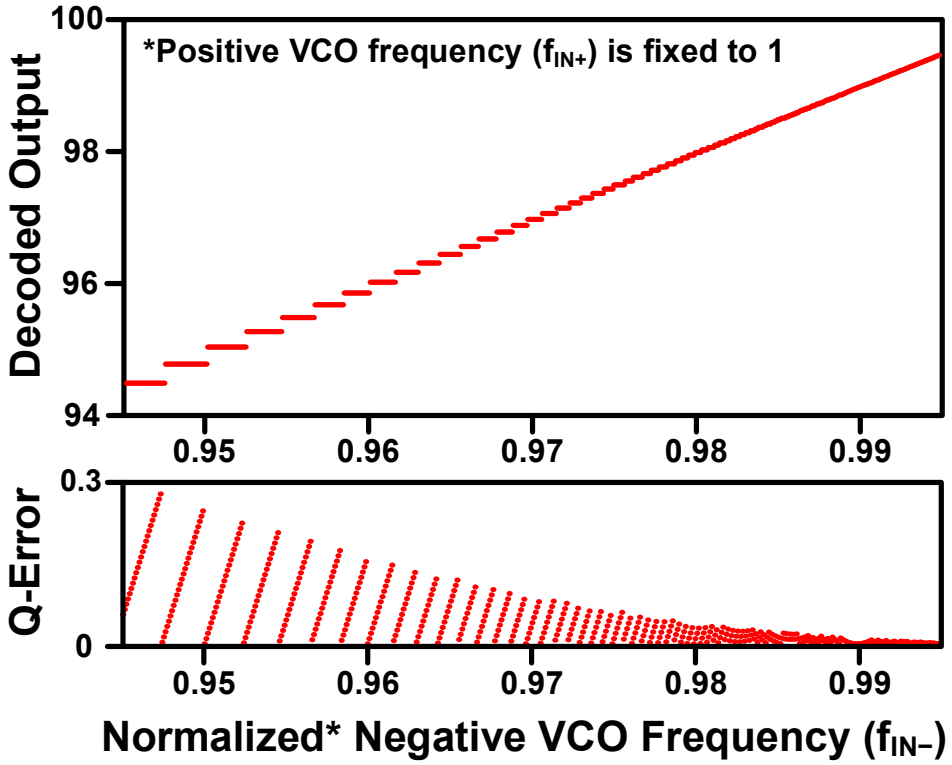


Fig. 3.8. Transfer characteristic of the decoded (i.e. linearized) BF quantizer and the corresponding quantization error.

3.3.3 Comparison with Conventional VCO-Based ADC.

VCO-based ADCs have been drawing attention lately owing to their digital-friendly implementation and inherent first order noise-shaping property. Recent publications have reported high-order continuous-time delta sigma modulator loops utilizing the VCO-based ADC as a multi-bit quantizer achieving very high SNDR (e.g. 78dB [28]). The proposed VCO-based ADC with BF quantizer has the unique property of being able to achieve high resolution for very small input signals when used as a Nyquist rate ADC. Conventional VCO-based ADCs on the other hand take advantage of the noise-shaping property to improve resolution while sampling rail-to-rail input signals.

Another noteworthy difference is that existing VCO-based ADCs have a fixed sampling period while the proposed ADC has a sampling period that is a function of the beat frequency (i.e. difference between the main and reference frequencies) period. Finally, as far as the VCO linearity is concerned, conventional designs are more susceptible to the VCO's inherent voltage-to-frequency nonlinearity and difficult to achieve high performance unless sophisticated techniques such as the phase-feedback closed-loop [28] or digital calibration [31] are employed. This stems from the rail-to-rail input signal swing requirement of conventional ADCs. In contrast, the proposed ADC has a better linearity as it can work for smaller input signals. Simulation results in 65nm show that the variation in K_{VCO} is reduced from ±14% to ±0.1% as the input signal amplitude is reduced from 400mV to 1mV. Fig. 3.9 compares various features of the conventional and proposed VCO-based ADC.

	Conv. VCO-based ADC	This Work
ADC Type	Delta-sigma	Nyquist rate
Main Feature	1^{st}-order noise-shaping	Beat frequency quantization
Input Range	Large [V]	Small [μV~mV]
VCO Linearity	Nonlinear K_{VCO} (large range)	Linear K_{VCO} (small range)
Key Circuit Block	VCO + linear counter	VCO + beat freq. quantizer
Counting Period	Fixed sample period	Variable beat freq. period
Sampling Rate	High speed [MS/s]	Low speed [kS/s]
Applications	Wireless receiver [25, 26]	Biomedical systems

Fig. 3.9. A comparison table with conventional VCO-based quantizer.

3.4 Circuit Implementations in 65nm CMOS

One limitation of the simple BF quantization scheme described above is that the sensing resolution quickly degrades as the difference between the positive and negative input voltages becomes larger. To overcome this limitation, we propose a dual reference BF quantizer circuit shown in Fig. 3.10 where the negative input signal is AC-coupled to the supply voltage of not one but two VCOs with different DC bias levels. Using the two AC-coupled negative input signals as the upper bound and lower bound, we can obtain a high sensing resolution for both positive and negative phases of the differential input signal. The DC bias levels for the two reference VCOs (V_{NH} and V_{NL}) and the main VCO (V_P) in Fig. 3.10 are set using a simple on-chip voltage bias generator. Each VCO is implemented using 5 static NAND gates with programmable capacitor banks attached to each stage for fine grain frequency trimming. A static D flip-flop and a 5 bit majority voter circuit are used in both the upper and lower paths to generate the beat frequency signal while eliminating any logic bubbles (e.g. lone 1 in a stream of 0's) that may cause logic errors. A 12 bit counter is used to record the number of reference periods corresponding to the period of the beat frequency signal. The output count is then sampled by the main sampling clock CLK_S. The 12 bit positive and negative BF quantizer outputs (D_P and D_N) are used to compute the actual input differential voltage. Fig. 3.11 shows the timing diagram for a single sampling period of the BF quantizer circuit. To reduce unnecessary switching power, all VCOs are automatically shut off once the sampling is complete. Fig. 3.12 shows the measured waveforms from the 65nm test chip.

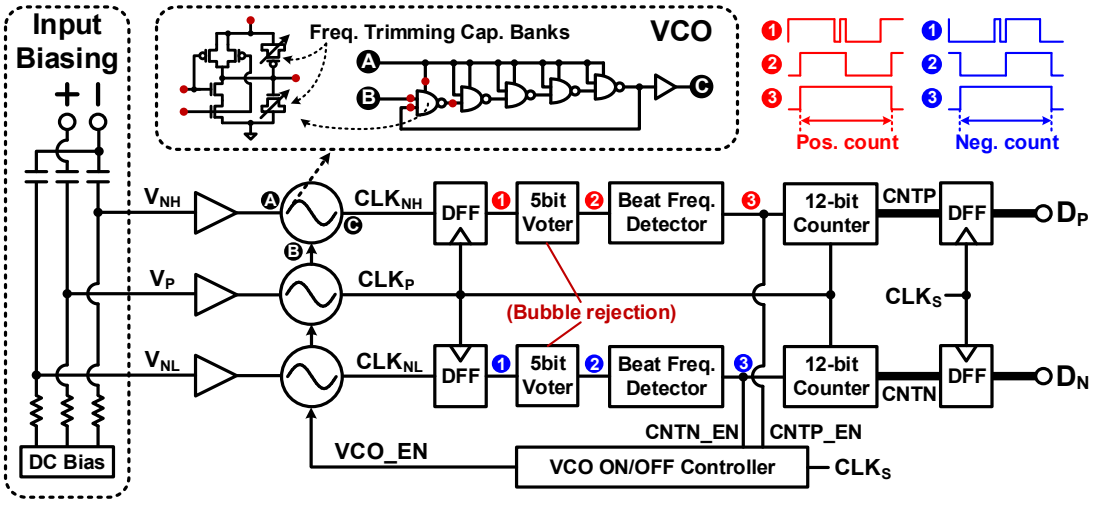


Fig. 3.10. Proposed VCO-based ADC with a dual-reference BF quantizer for improved resolution.

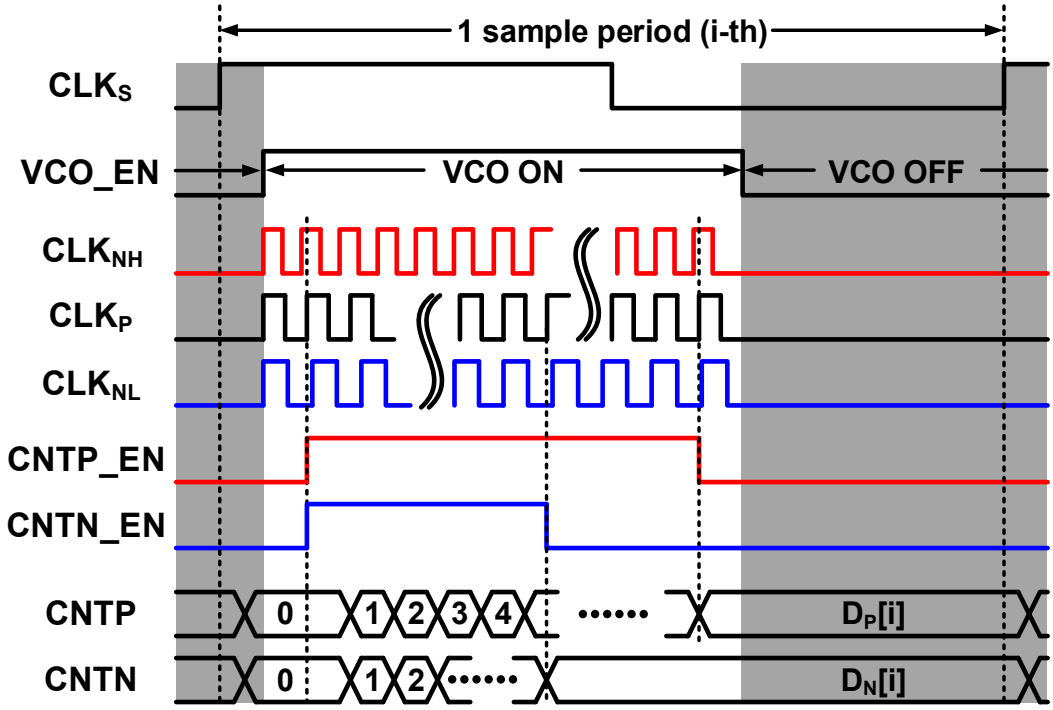


Fig. 3.11. Timing diagram of the proposed BF quantizer for a sampling cycle.

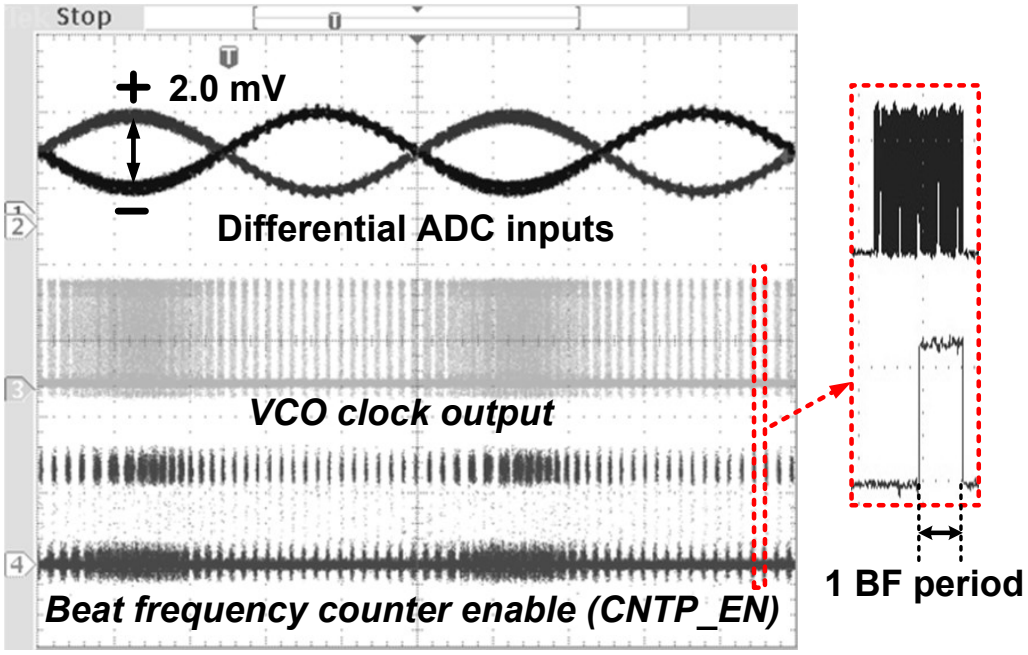


Fig. 3.12. Measured waveforms from the test chip for a 4mVpp differential input.

One interesting feature of the proposed VCO-based ADC is that we can obtain a uniformly high ADC resolution for a range of input signal amplitudes by simply adjusting the reference voltage levels. This eliminates the need for a separate variable gain amplifier reducing the power consumption, area, and complexity of the overall system. This would be particularly attractive for physiological signal acquisition systems which may have to operate across a wide range of input signals with different amplitudes. Simulation results in Fig. 3.13 show the ADC output range as a function of the signal input range and the difference between the upper bound and lower bound reference signals. The resolution increases exponentially as the reference difference approaches the input range, although in practice, the ENOB is limited by the noise floor of the input and reference signals as well as the VCO phase noise.

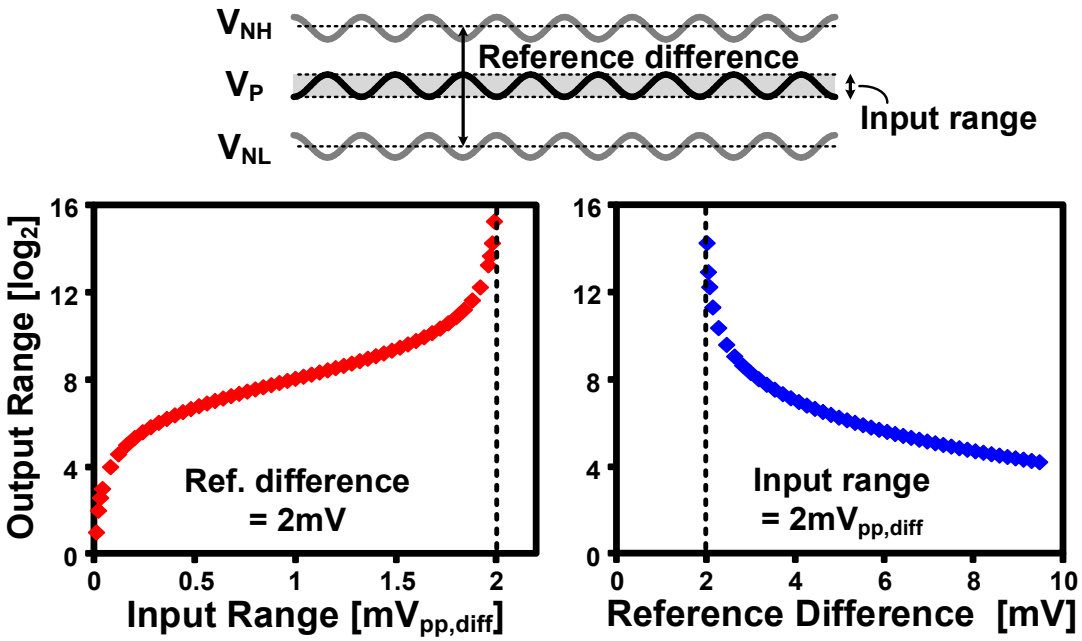


Fig. 3.13. Simulated ADC output range as a function of the input range and the voltage difference of dual references.

3.5 ADC Test Chip Measurement Results

A VCO-based ADC with the proposed BF quantizer was implemented in a 65nm LP CMOS process as a proof of concept. The measured DNL and INL were -0.71/+0.86 LSB and -1.05/+1.12 LSB, respectively as shown in Fig. 3.14. For a sampling rate of 2.083kS/s and an input signal of 1.6mV, a 39.1dB SNDR (6.2bit ENOB) and a 41.9dB SFDR were achieved (Fig. 3.15). Fig. 3.16 also shows the measured ENOB as a function of the input signal frequency, showing a 5.0 to 5.8 ENOB range for a 0.8mV input signal. Here, the Nyquist rate frequency is 1.0415kHz.

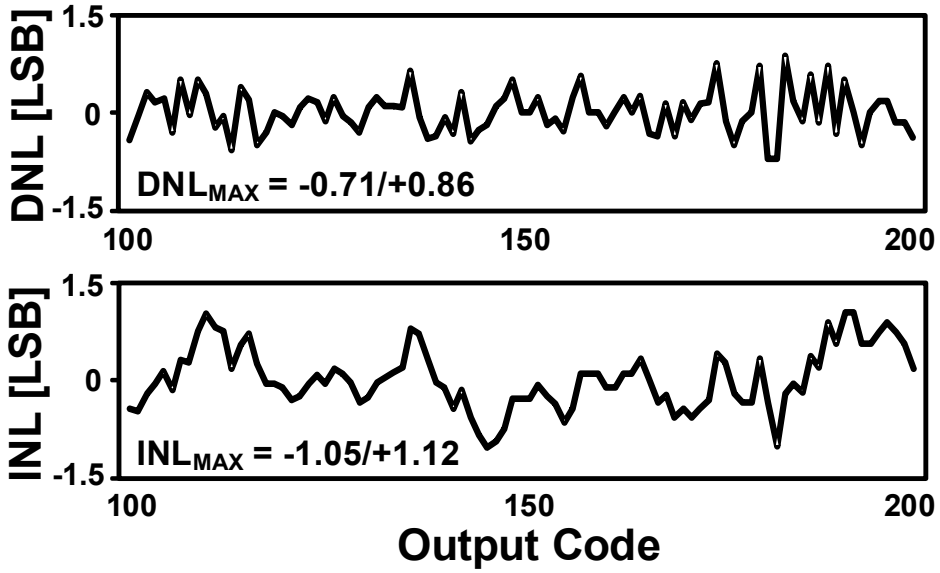


Fig. 3.14. Normalized DNL and INL from the measured ADC output codes.

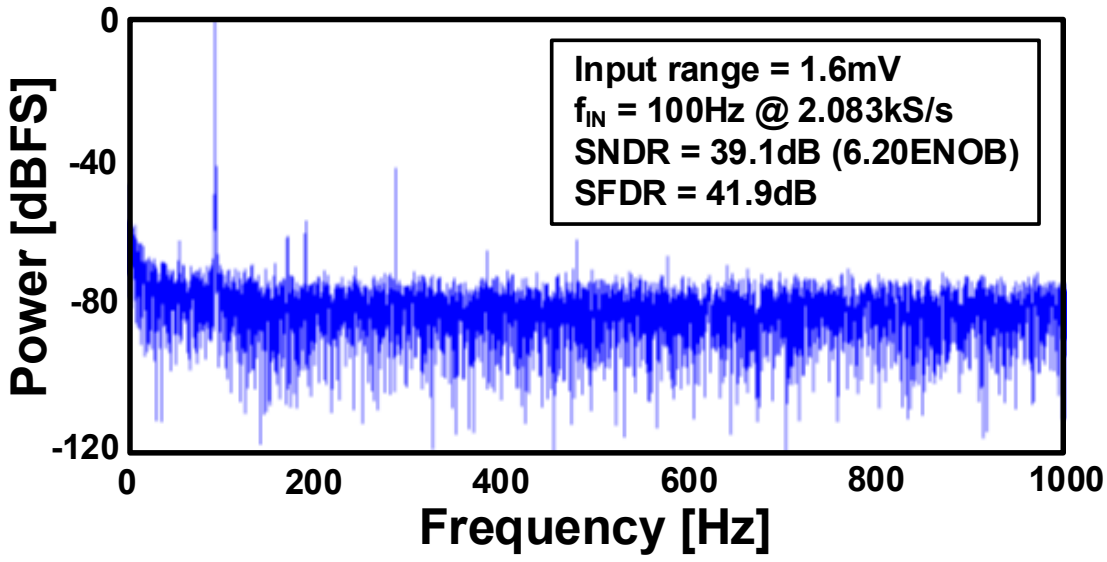


Fig. 3.15. Measured FFT for a 1.6mV input AC signal with key ADC specifications.

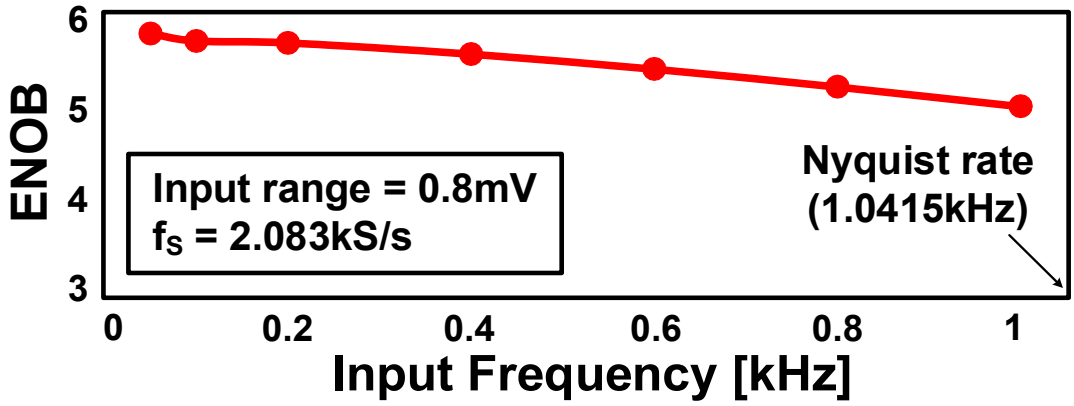


Fig. 3.16. ENOB versus input frequency.

Fig. 3.17 shows the measured ADC output code (Fig. 3.18, upper) and the decoded signal (Fig. 3.17, lower) with a 2.5mV, 60bpm ECG input signal generated by an external signal generator. The decoded output in Fig. 3.17 clearly shows the PQRST complex (i.e. each sequential letter P, Q, R, S and T represents a different portion of the cardiac cycle) of ECG signal.

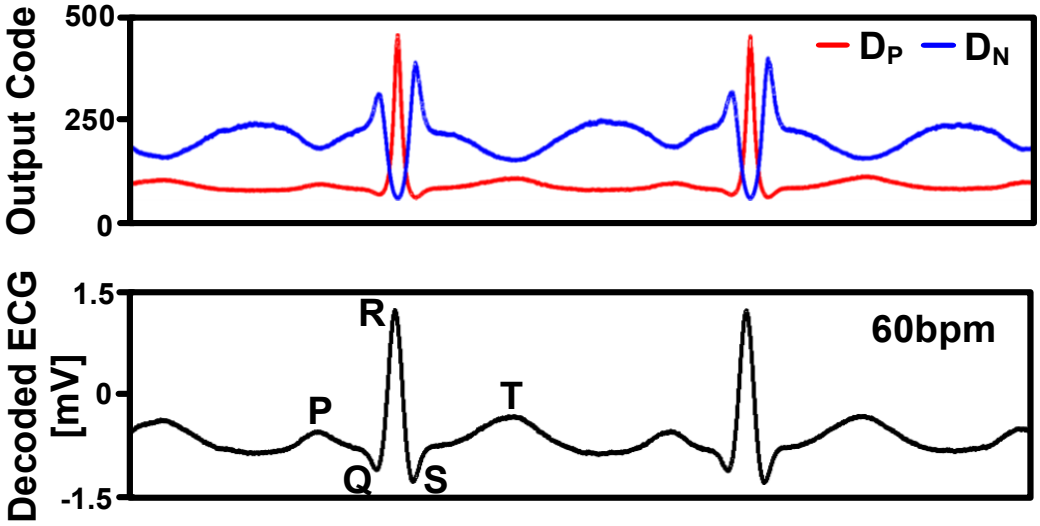


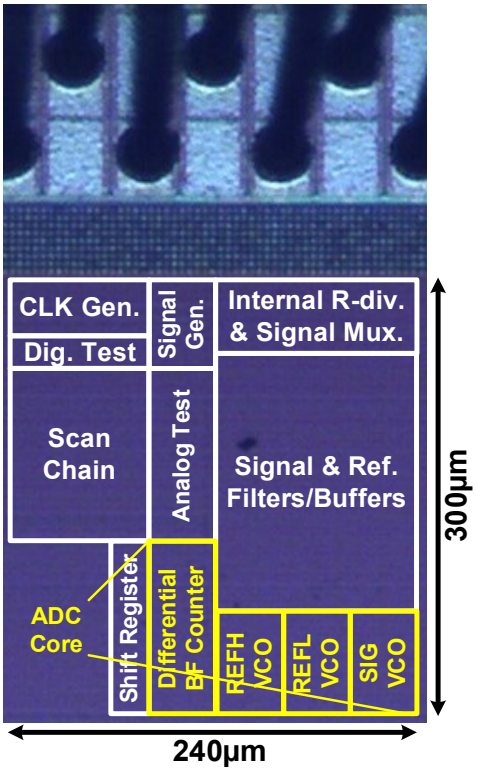
Fig. 3.17. Measured single-channel ADC output code (upper) and the decoded signal (lower) with a 2.5mV amplitude input ECG signal.

Fig. 3.18 compares the performance of the proposed ADC versus prior ADCs including a nonlinear pipeline ADC [32], a VCO-based ADC [26], a linear pipelined ADC [33], and two state-of-the-art SAR-ADCs [20, 21]. The proposed ADC shows a FOM (normalized to 1mV) of 4.80pJ/conv-step, a dynamic range (normalized to 1.2V) of 89dB, and an area of 0.013mm^2 which is much smaller than the other ADCs. The compact nature and simplicity of the proposed VCO-based ADC makes it ideally suited for multi-channel sub-mV physiological signal sensors which typically require large and power hungry multi-stage amplifiers and signal filters per channel. In contrast, the proposed ADC only requires passive signal filters which have a smaller footprint compared to having dedicated amplifier circuits. The feature summary table and the test chip microphotograph of the proposed ADC are given in Fig. 3.19.

	[32] VLSI'07	[26] ISSCC'09	[33] VLSI'12	[20] ISSCC'11	[21] ISSCC'12	This work
ADC Type	Nonlinear Pipelined	VCO-based Delta-Sigma	Pipelined	SAR	SAR	Nonlinear Beat-Freq.
Input Range	Large[V]	Large[V]	Large[V]	Large[V]	Large[V]	Small[mV]
Process / Supply Voltage	0.18μm /1.62V	0.13μm /1.5V	0.18μm /1.3V	65nm /0.4V~1.0V	90nm /1.1V	65nm /0.5V~1.2V
Sampling Rate(f_S) / Power(P)	22MS/s /2.54mW	900MS/s /87mW	30MS/s /2.6mW	20kS/s /206nW	4MS/s /17.44μW	4.17kS/s /0.92μW
Energy Efficiency (P/f_S or $P/(2 \cdot f_{BW})$ for ΔΣ)	115.5pJ	2175pJ	86.7pJ	10.3pJ	4.36pJ	220.6pJ
SNDR [dB] @ Input Range	35.6@1V	78.1@2.28V	61.5@2.2V	55.0@1.1V	58.3@1.36V	39.1@1.6mV
ENOB [bit] @ Input Range	2.8@1mV	12.7@2.28V	9.9@2.2V	8.84@1.1V	9.4@1.36V	6.2@1.6mV
Conversion-steps per mV	6.96	2.92	0.43	0.42	0.50	45.95
*FOM_{1mV} [pJ/conv-step]	16.59	744.86	199.64	24.72	8.78	4.80
**Min. Input Amplitude [mV] (Dynamic Range)	0.10 (80dB)	0.28 (78dB)	1.85 (57dB)	1.96 (54dB)	1.65 (58dB)	***0.03 (89dB)
Area [mm^2]	0.560	0.450	0.500	0.212	0.047	0.013

*FOM normalized to 1mV (=-60dB), ** Input amplitude at SNDR = 0dB
*** based on measured SNDR of 10dB @0.12mV

Fig. 3.18. A table summarizing performance comparison with the state-of-the-art ADCs.



Process		65nm LP CMOS
Operating Voltage		0.5V ~ 1.2V
Area	Test chip	0.072mm²
	BF-ADC core	0.013mm²
Input Range		120μV ~ 6mV
Max. Sampling Rate		20.83kS/s
DNL		-0.71/+0.86 [LSB]
INL		-1.05/+1.12 [LSB]
Dynamic Range		89dB
SNDR @ 1.6mV		39.1dB (ENOB=6.20)
SFDR @ 1.6mV		41.9dB
Power	VCO@2MHz	0.86μW
	Digital Power	0.06μW

Fig. 3.19. Die micrograph and a feature summary table of the proposed ADC.

3.6 Multi-Channel Frontend Implementation

A multi-channel (8-channel) sub-mV signal frontend circuit based on the proposed VCO-based ADC is also implemented in 65nm CMOS as shown in Fig. 3.20. The frontend is integrated with separated multi-channel active electrodes for verifying its functionality. The active electrode instead of the passive one has been chosen here for re-utilizing the already existing analog buffers in the VCO-based ADC shown in Fig. 3.10. The analog buffers in the active electrodes drive multi-channel input VCOs in the frontend circuit. Recently, dry active electrodes (i.e. a combination of dry electrodes with in situ amplification) are increasingly used for the measurements of common physiological signals in many emerging healthcare systems.

Each channel electrode in Fig. 3.20 is consist of a simple passive band-pass filter (i.e. a CR high pass filter followed by a RC low-pass filter) to filter-out both DC offset and high-frequency noise before driving the channel VCOs in the frontend circuit with the analog buffers in the electrodes. A single VCO from the 8 channel input VCOs is selected at a time (i.e. 8-to-1 time multiplexing) and the clock output from the selected VCO is used for the BF quantization with the other two VCO clock outputs from the positive and negative reference channels. When the 8-to-1 time multiplexing VCO-based ADC is operating, the selected input VCO is enabled (i.e. power on) while the others are disabled (i.e. power off) to minimize the multi-channel frontend power consumption.

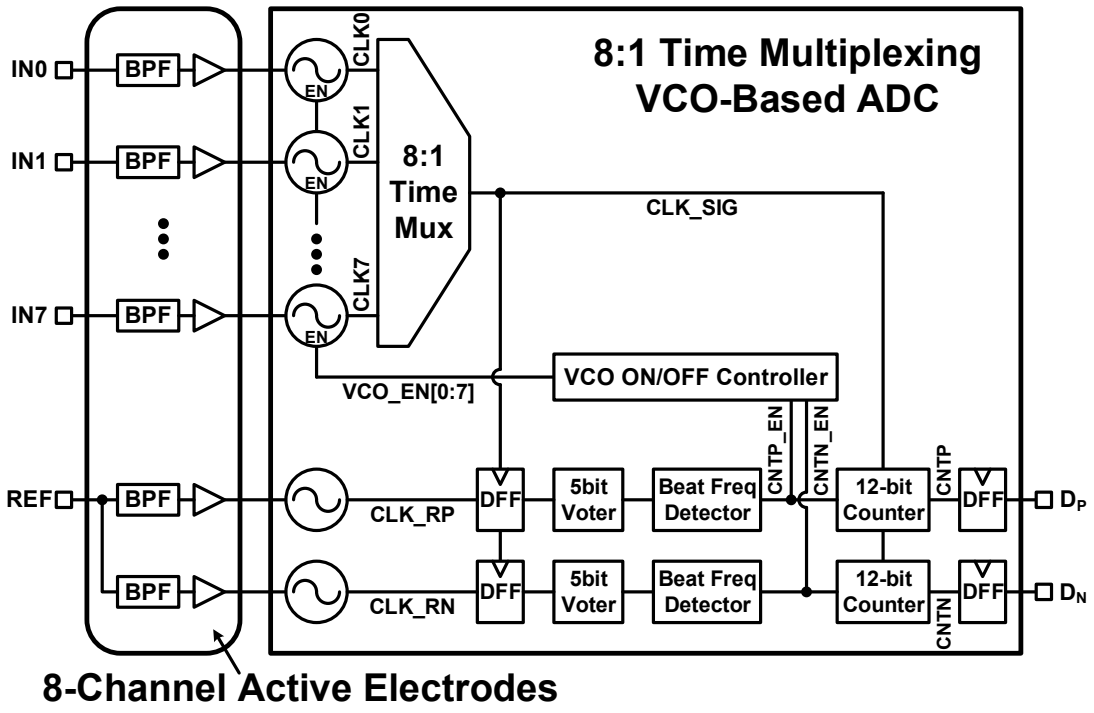


Fig. 3.20. A prototype 8-channel sub-mV signal frontend circuit with active electrodes and the proposed 8:1 time multiplexing VCO-based ADC.

Fig. 3.21 shows the measured (and decoded) 8-channel signals. Even (i.e. 0, 2, 4, 6) and odd (i.e. 1, 3, 5, 7) channels are assigned with different input signals for verifying the function of the proposed 8-to-1 time multiplexing signal acquisition frontend circuit with no channel amplifier. A common 40Hz input sine wave is applied to the even channels while the odd channels are assigned with a 240bpm ECG signal generated by an external signal generator. The test chip micrograph of the 8-channel frontend and the active electrodes is shown in Fig. 3.22.

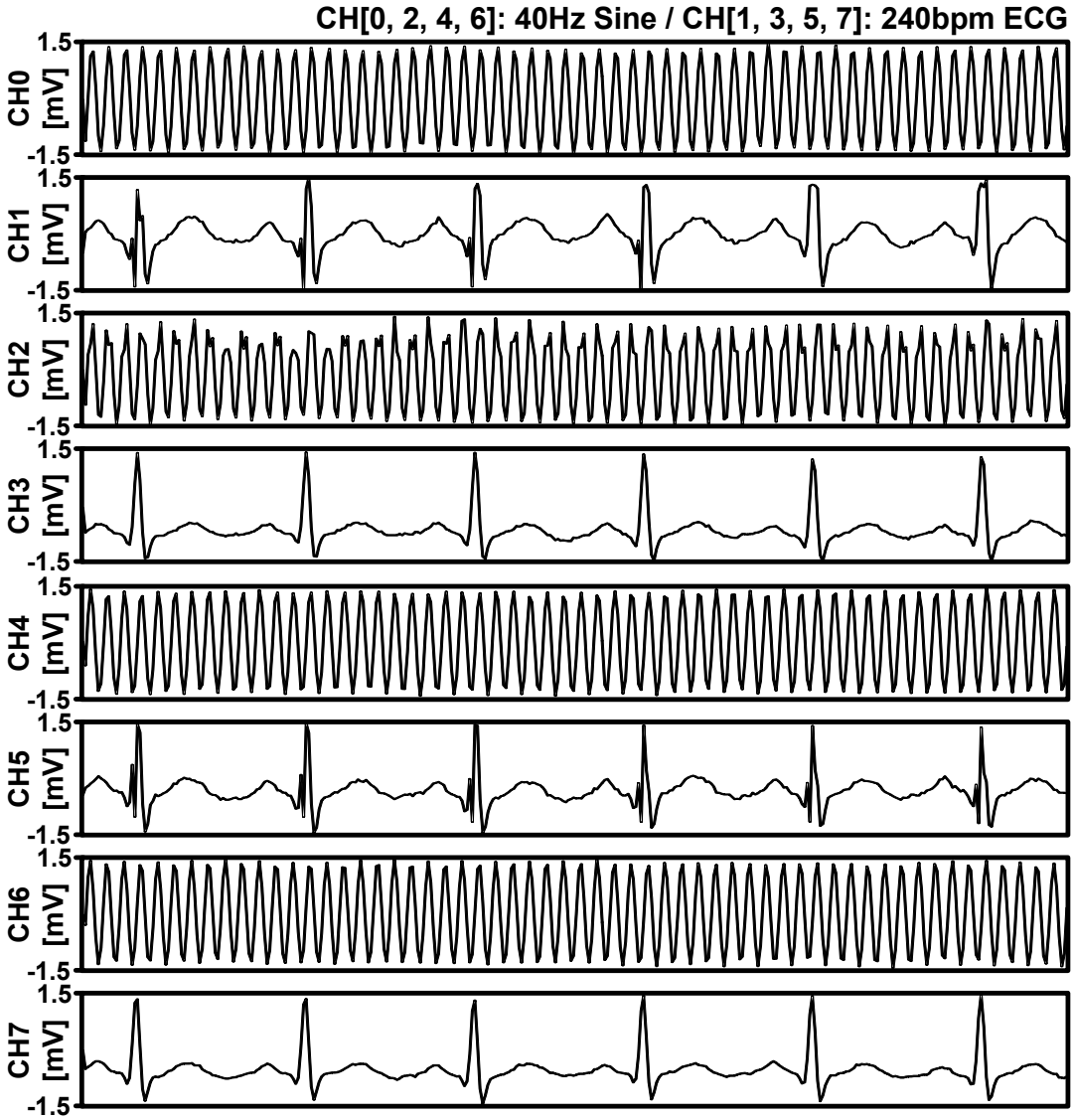


Fig. 3.21. Measured (decoded) 8-channel signals. A 40Hz sine wave is assigned to even (0, 2, 4, 6) channels and a 240bpm ECG signal is assigned to odd (1, 3, 5, 7) channels.

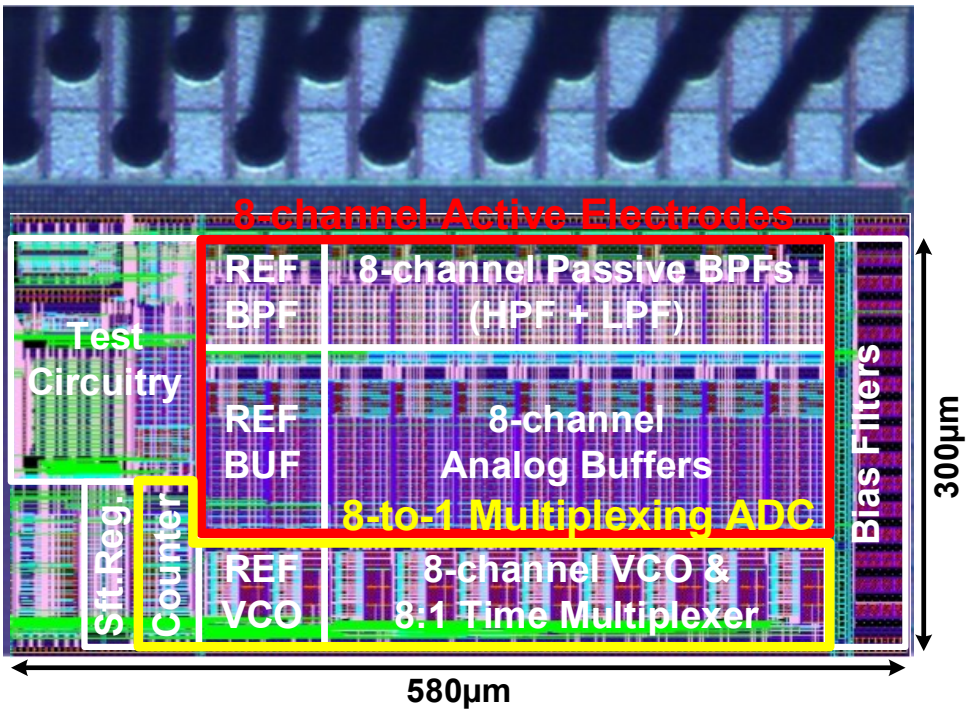


Fig. 3.22. Die micrograph of the 8-channel bio-potential frontend with active electrodes.

3.7 Conclusion

In this paper, we have presented a highly digital VCO-based ADC utilizing the beat-frequency (BF) quantization scheme for directly sampling signals with sub-mV input range. To improve the ADC resolution, we proposed a dual reference BF quantizer scheme which employs two reference VCOs. The dual reference based circuit helps maintain a consistently high sensing resolution for both positive and negative phases of the input signal. A 65nm test chip demonstrates 6.2 ENOB for a 1.6mVpp input differential signal without any external signal amplification or conditioning circuitry. A prototype 8-channel time-multiplexing signal acquisition system based on the proposed VCO-based ADC is also implemented in the same test chip and the multi-channel signal acquisition function has been verified.

Chapter 4. VCO-Based ADC Employing Multi-Phase Noise-Shaping Beat Frequency Quantizer for Direct Sub-mV Signal Acquisition

This chapter proposes an oversampling VCO-based ADC employing a novel beat frequency quantizer for the direct A-to-D conversion of sub-mV input signals without the use of signal pre-conditioning amplifiers. Compared to the prior work, the ADC resolution is improved by using the proposed multi-phase and noise-shaping beat frequency quantization.

4.1 Introduction

As one of the most critical building blocks for ultra-low power systems such as wireless sensor nodes and bio-potential signal (e.g. ECG, EEG and neural recording) acquisition systems, analog-to-digital converter (ADC) plays an important role in determining the overall system performance. Significant progress has been made recently in the energy-efficient ADC designs including the successive approximation register (SAR) ADCs for sensor and medical applications. Depending on the system level specifications, microwatt level power consumption can be achieved by adaptively reconfiguring the sampling rate and the resolution of the recently published SAR ADCs [20, 21]. However, despite these advances, the actual system performance improvement experienced by the end-user may be rather limited due to the power and area overhead of auxiliary circuits such as multiple stages of amplifiers required for signal pre-conditioning (i.e. the amplification of sub-mV input signal to a rail-to-rail output swing

for the A-to-D conversion with a multi-bit output resolution, Fig. 4.1, left top). Most prior ADC designs ignore the design complexity and the power and area overhead of various amplifiers by taking a rail-to-rail input signal range for granted. Not only does this situation obscure the true benefits of the advanced improvements on the state-of-the-art ADC designs, the additional device noise from the amplifiers or any non-ideality due to the multiple stages of cascaded signal conditioning could degrade the overall system performance.

Recently, a high resolution beat frequency (BF) quantization scheme [34] has been proposed for the direct analog-to-digital conversion of small input signals which can eliminate amplifier circuits all together from the system (Fig. 4.1, left bottom). By removing all the amplifiers from the sub-mV signal acquisition system, the overall power and area consumptions are saved and the amount of those savings could be enormous as the number of channels increases. In practice, there are increasing demands of low power and low area multi-channel neural recording systems which require more than 100 channels in a single system [22, 23]. In this chapter, we present details of the proposed VCO-based ADC based on a novel beat frequency quantizer with the improved SNDR and the higher sampling rate than the prior work [34] by employing the multi-phase and noise-shaping beat frequency (BF) quantization scheme. Experimental data from a 65nm test chip shows a 43dB SNDR when directly converting a 1mV input signal to the output digital code. The measured SFDR is 57dB.

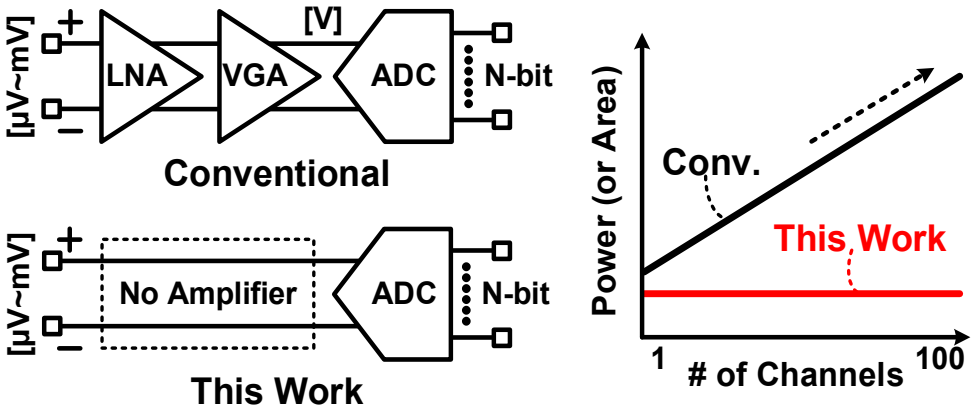


Fig. 4.1. Sub-mV signal acquisition systems with conventional and proposed ADC. Power (or area) consumption of conventional multi-channel signal acquisition system is proportional to the number of channels while it is independent of that in this work.

The remainder of this chapter is organized as follows. Section 4.2 describes the existing and the proposed VCO-based ADC design techniques for achieving high resolution. Section 4.3 reviews the concept of the beat frequency quantization. The proposed multi-phase noise-shaping beat frequency quantization scheme for sub-mV signal acquisition with the improved performance is explained in Section 4.4. Section 4.5 explains a prototype third-order continuous-time delta-sigma modulator based on the proposed BF quantizer for improving the resolution even further. The details on the implementation of the 65nm test chip is shown in Section 4.6. The chip measurement results are given in Section 4.7 and Section 4.8 concludes the chapter.

4.2 VCO-Based ADC Designs for Achieving High Resolution

Fig. 4.2 shows the existing VCO-based ADC designs [35, 36] with their key features for achieving high resolution A-to-D conversion. Typically, existing VCO-based ADCs with a chain of multiple inverter stages (Fig. 4.2, left) have been utilized all the multi-phase VCO clock outputs as counting references of their multiple reset counters. Then, the output counts from the counters are summed up and sampled to the output at every ADC sampling cycle (i.e. CK_S in Fig. 4.2). Hence, the output range of the conventional VCO-based ADC is proportional to the number of VCO output clock phases and accordingly, the resolution is improved as much as $\log_2$N-bit where N is the number of phases. For instance, let's assume there is a VCO-based ADC with 16-phase clock outputs and we have 4 counts per each sampling cycle for a single phase output clock. A 2bit resolution (i.e. $\log_2 4 = 2$) VCO-based ADC with only a single-phase clock counter becomes a 6bit ADC (i.e. $2 + \log_2 16 = 6$) by utilizing all the 16-phase VCO clock outputs as counting references.

In addition to the multi-phase clock counting, an inherent first-order noise-shaping property is another key feature for achieving the high resolution VCO-based ADC when it is used as an oversampling ADC. The input voltage signal of the VCO is integrated to the VCO output phase and it is quantized and differentiated by a reset counter. While the input signal is converted to the digital output bits, the quantization error is generated and added in-between the VCO and the reset counter. Note that the VCO-based ADC output is the combination of the quantized digital output bits and the noise-shaped quantization error (i.e. quantization error which is differentiated at the reset counter).

A non-conventional VCO-based ADC with the beat frequency quantization scheme [34] (Fig. 4.2, right) achieved a multi-bit ADC resolution when the input signal amplitude is extremely small (i.e. sub-mV). The small input signals are AC-coupled to the VCO control voltages while having a slight DC-bias offset between them. By having the slight DC-bias difference between the two VCO control voltage signals (i.e. V_{IN+} and V_{IN-}) and counting the small frequency difference (i.e. beat frequency) between the output clocks, we could achieve the large output code range with respect to the minute sub-mV input signal change.

In this work, we improve the resolution, linearity and sampling rate of the VCO-based ADC with the novel BF quantizer for the direct acquisition of sub-mV input signals by incorporating the benefits from both the conventional VCO-based ADCs (Fig. 4.3) and the prior work [34]. Instead of using only single phase outputs from the two VCOs, the proposed VCO-based ADC utilize all the multi-phase VCO outputs for measuring the beat frequencies with multiple BF quantizers (i.e. as many as the number of VCO phases). Like the conventional VCO-based ADC, the quantizer outputs are summed up and sampled to the output at every ADC sampling cycle. We also propose a first-order noise-shaping BF quantization scheme by implementing a seamless BF clock period counting method. The quantization error which is a residue from the previous BF clock period quantization (i.e. counting) is saved as a VCO phase information (i.e. input to the phase detector of BF quantizer) and utilized at the next cycle of BF quantization. This is possible due to the seamless BF clock period quantization in the proposed work. Since the prior work [34] resets VCOs after each BF clock period quantization, the quantization error is not noise-shaped.

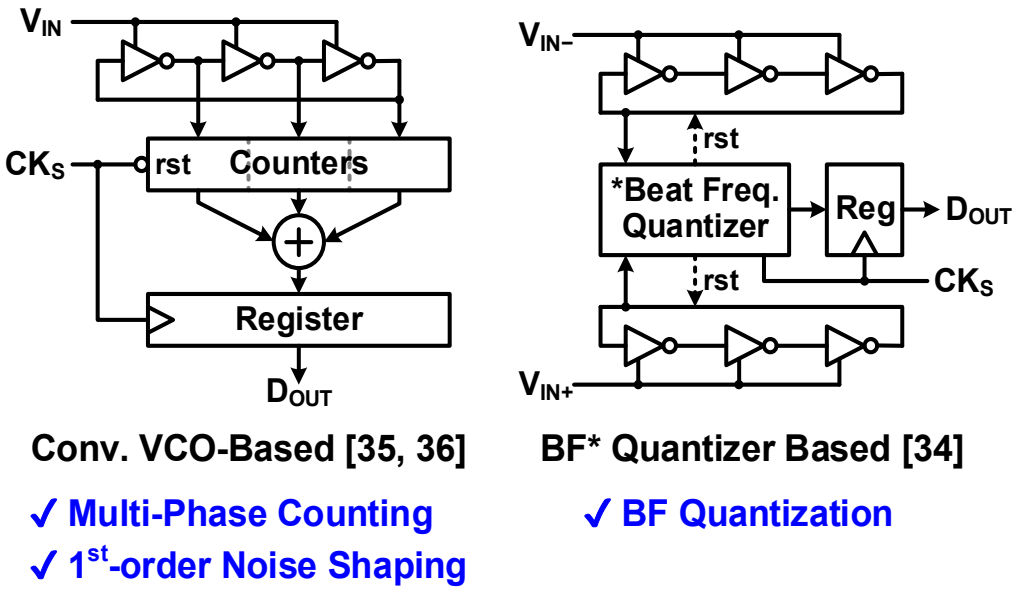


Fig. 4.2. Existing VCO-based ADCs and the key features used for achieving high resolution.

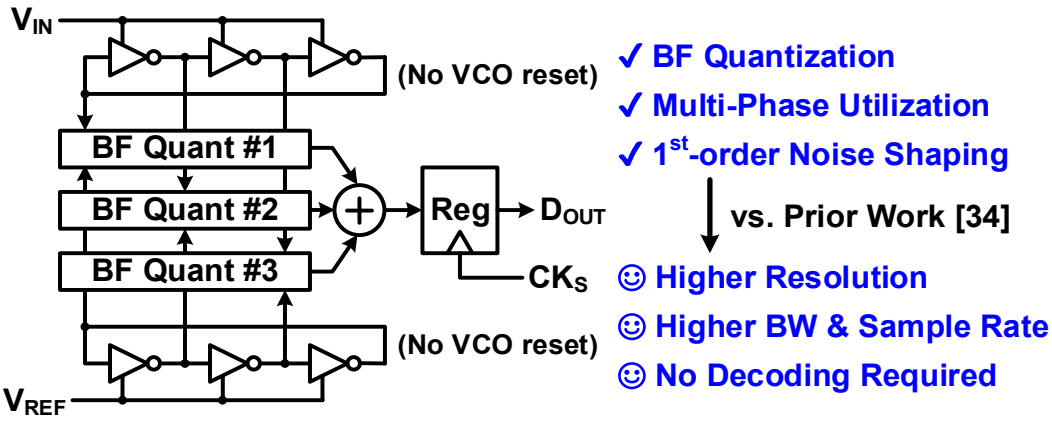


Fig. 4.3. Proposed multi-phase noise-shaping BF quantizer.

4.3 Beat Frequency Quantization for Multi-Bit Resolution Sub-mV Input Signal Acquisition

Fig. 4.4 describes the circuit and timing diagram of a single-ended BF quantizer which is consist of two D flip/flops (DFFs) and an asynchronous reset counter. The first DFF on the left is used for detecting the phase difference between the input clock (CK_{IN}) and the reference clock (CK_{REF}). The reset counter is used for counting a period of BF clock (CK_{BF}) which is the output of the first DFF. As shown in Fig. 4.4, the frequency of CK_{BF} (i.e. f_{BF}) is equal to the (quantized) frequency difference between the input and reference clock [34]. Since the BF clock is sampled by the input clock, the counter output is simply the frequency ratio between CK_{IN} and CK_{BF}. Finally, the second DFF on the right is used for sampling the counter output for each BF clock cycle. Right after this sampling, the counter is reset for counting the next BF clock cycle.

The proposed BF quantizer measures the beat frequency between the two similar VCO clock frequencies (i.e. $f_{BF}=f_{REF}-f_{IN}$) to amplify a small change in the input frequency (or the VCO input voltage) into a large measurable count output (i.e. D_{OUT}). This allows us to eliminate frontend amplifiers (e.g. LNA and VGA) from the signal acquisition system with extremely small (e.g. 1mV) input signals and as a result it reduces the power and area overhead and simplifies the overall design complexity [34]. To illustrate this point better, let's consider an example in which the initial frequency difference between CK_{REF} and CK_{IN} is 1%. This gives the initial counter output of 100 as it takes 100 clock cycles for the fast clock to pass, catch up, and overtake the slow clock. Now, suppose the frequency difference becomes 1.01% due to a miniscule change in the input signal. This translates into an output count of 99 since it takes one

less cycle for the fast clock to catch up with the slow one. In contrast, to obtain the same output count change (i.e. 100 to 99), the conventional VCO-based quantizer (see Fig. 4.2, left) would have required a much larger change in frequency (1% rather than 0.01%) which translates into a 100x lower sensitivity. Note that the CK_{REF} frequency in the BF quantizer must be configured to be close to the CK_{IN} frequency (typically within 1%) for sufficiently high resolution. This can be readily achieved using an identical VCO with a slightly different (e.g. 10mV) common-mode DC bias.

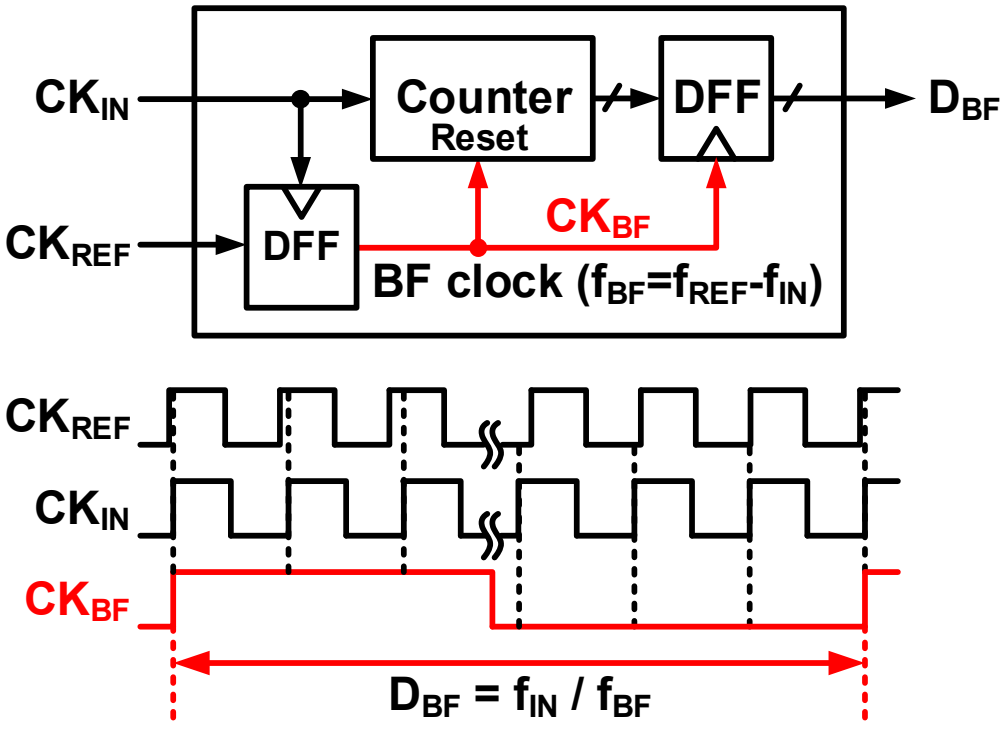


Fig. 4.4. A single-ended BF quantizer circuit and its timing diagram.

Fig. 4.5 shows the simulated range of single-ended BF quantizer output codes with two input voltages (i.e. V_{IN1}, V_{IN2}) with the same input range and the different common-mode DC biases. While the two inputs, V_{IN1} and V_{IN2} are having the same 1mV input range, the common mode DC bias offset between the inputs and the reference (i.e. V_{REF}) are different (i.e. 9.5mV between V_{IN1} and V_{REF}, 4.5mV between V_{IN2} and V_{REF}) as shown in Fig. 4.5, upper left. The input and reference voltages are then converted to the VCO frequency with the VCO gain (i.e. K_{VCO}) of 10MHz/V as shown in the equation of Fig. 4.5. For simplicity, we assumed that the VCO gain is perfectly linear throughout its input range from 0V to 1V. As a result, the VCO output frequency ranges are calculated as shown in Fig. 4.5, upper right.

Under the given simulation conditions, the single-ended BF quantizer output range is 10 when the common-mode DC bias offset is 9.5mV. However, this output range is improved by 5-times (i.e. 50) when the bias offset is reduced to 4.5mV. This is an expected result since the BF quantizer resolution increases as the input (i.e. VCO output) frequency difference becomes smaller. Note that there will be a certain limit that we can achieve the higher output resolution since the noise floor will deteriorate the overall BF quantizer signal-to-noise performance and that impact will become even larger than the improved signal resolution as the bias offset becomes too small. In practice, 10mV (i.e. 1% frequency difference in this example) is the achievable minimum bias difference for the optimal BF quantizer output resolution. Fig. 4.6 shows the simulated BF quantizer output range when the differential BF quantizer is used instead of the single-ended one under the exactly same simulation conditions. As expected, the output range becomes double compared to the results shown in Fig. 4.5.

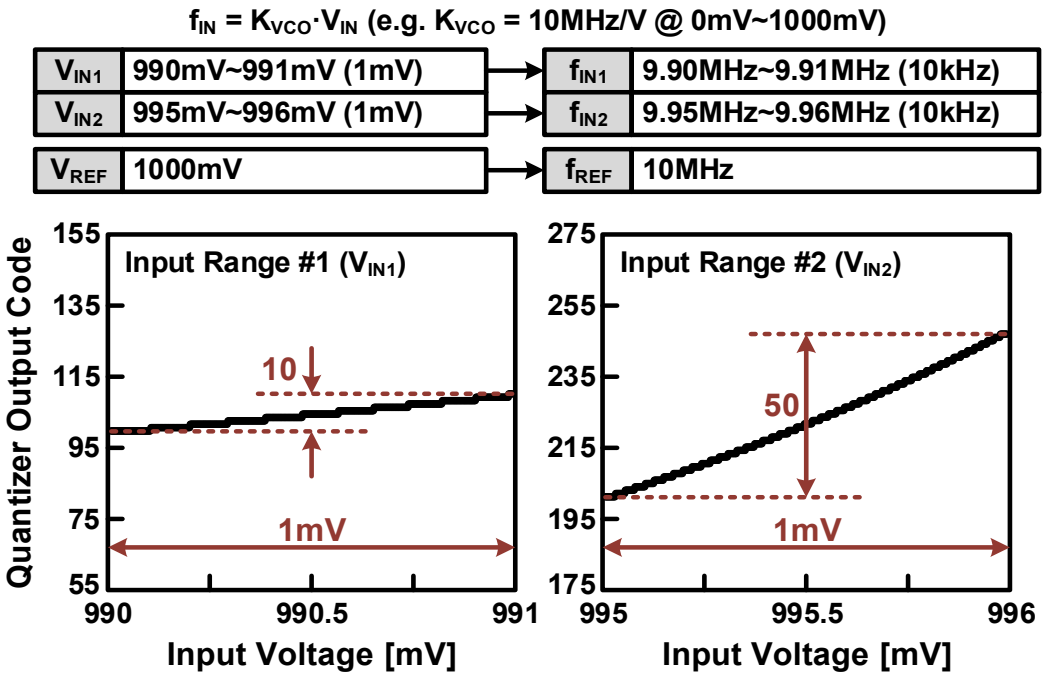


Fig. 4.5. A single-ended BF quantizer transfer characteristic (i.e. output vs. input range).

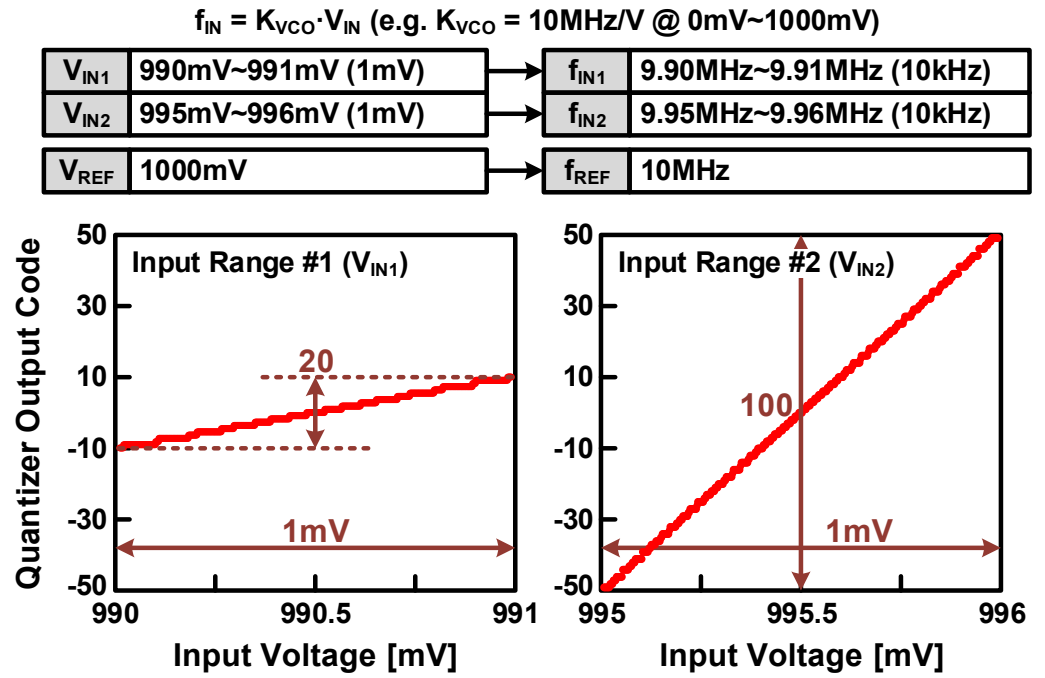


Fig. 4.6. A differential BF quantizer transfer characteristic (i.e. output vs. input range).

4.4 Multi-Phase Noise-Shaping Beat Frequency Quantizer

4.4.1 First-Order Noise-Shaping BF Quantization

In addition to the unique high resolution sensing capability of the BF quantizer, the proposed work further improves the VCO-based ADC performance by oversampling the input voltage with a noise-shaping BF quantizer as described in Fig. 4.7. The previous design in [34] resets the VCO after each BF clock period and as a result, the quantization error at the end of each BF cycle is lost (Fig. 4.7, left). By contrast, the proposed quantizer measures each BF clock cycle without resetting the VCO. By doing so, the quantization error is passed on to the next cycle and hence accounted for (Fig. 4.7, right). In addition to accomplishing first-order noise-shaping, the sampling rate is maximized since there is no dead period between samples.

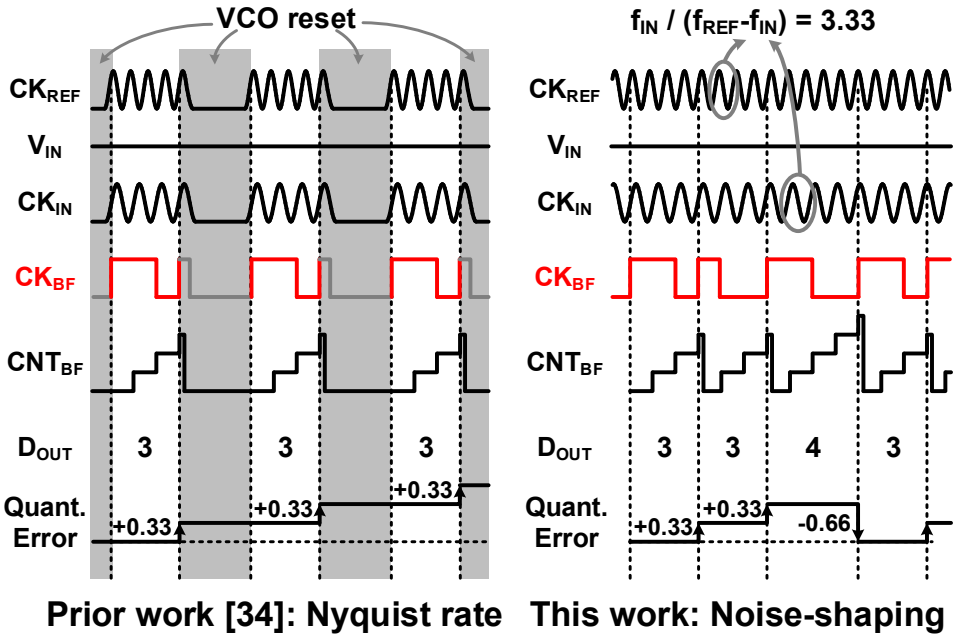


Fig. 4.7. First-order noise-shaping is achieved by counting the input clock periods in each BF cycle without any interruption. The simplified example shown here is for a small BF count number of 3 or 4.

Fig. 4.8 contrasts the simulated differential BF quantizer resolutions with the prior Nyquist rate and the proposed first-order noise shaping BF quantizer. In this simulation, the noise-shaping comes with 4x oversampling (i.e. OSR=4, sampling frequency is equal to the 8-times of input bandwidth). For a fair comparison, input sine waves with the same parameters (i.e. 1.085kHz frequency, 1mV amplitude and 10kHz bandwidth) are used for each simulation. The sampling rate for the Nyquist rate BF quantizer is 20kHz while that of the noise-shaping quantizer with 4x oversampling is 80kHz. The common-mode DC bias offset is set to 9.5mV and the VCO parameters are the same with the ones used for the simulation results shown in Fig. 4.5 and Fig. 4.6. The simulated results show that the first-order noise-shaping BF quantizer performs 38dB SNDR which is 12.1dB higher than that of the prior work with Nyquist rate BF quantization (i.e. 25.9dB SNDR).

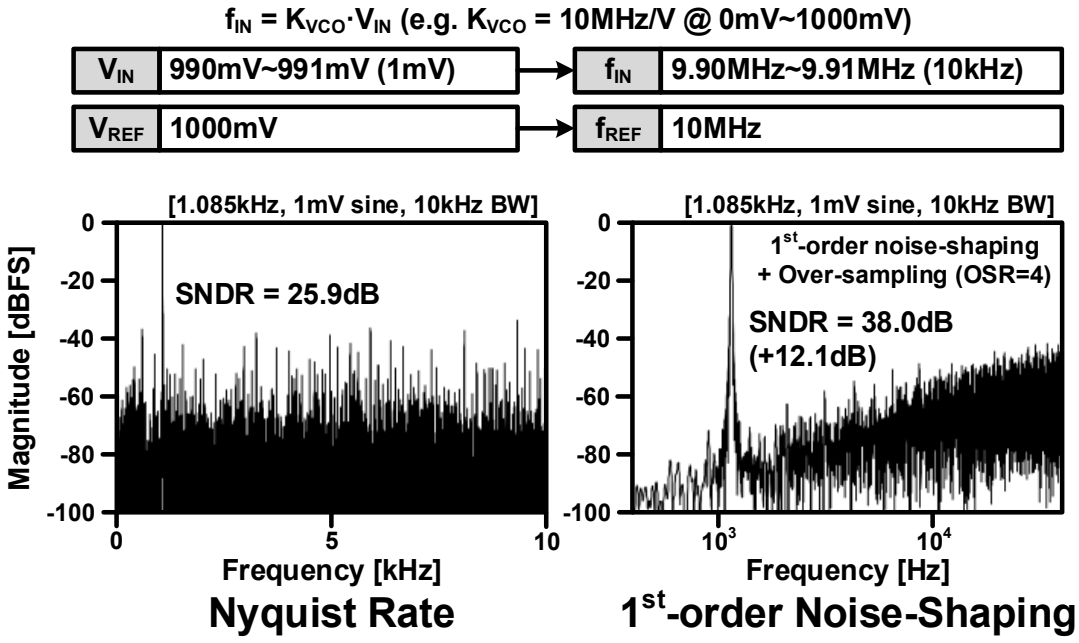


Fig. 4.8. Simulated differential BF quantizer resolution improvement with the first-order noise-shaping and 4x oversampling.

4.4.2 Multi-Phase BF Quantization

In addition to the noise-shaping, we also propose a multi-phase BF quantization scheme for improving the ADC resolution and linearity. Fig. 4.9 shows the basic idea using a simplified 7-phase ring oscillator as an example circuit. Here, the output of each VCO inverter stage is utilized for reducing the phase offset and thus achieves a finer timing resolution. The previous design used a single-phase clock which limits the timing resolution to one oscillation period of the VCO.

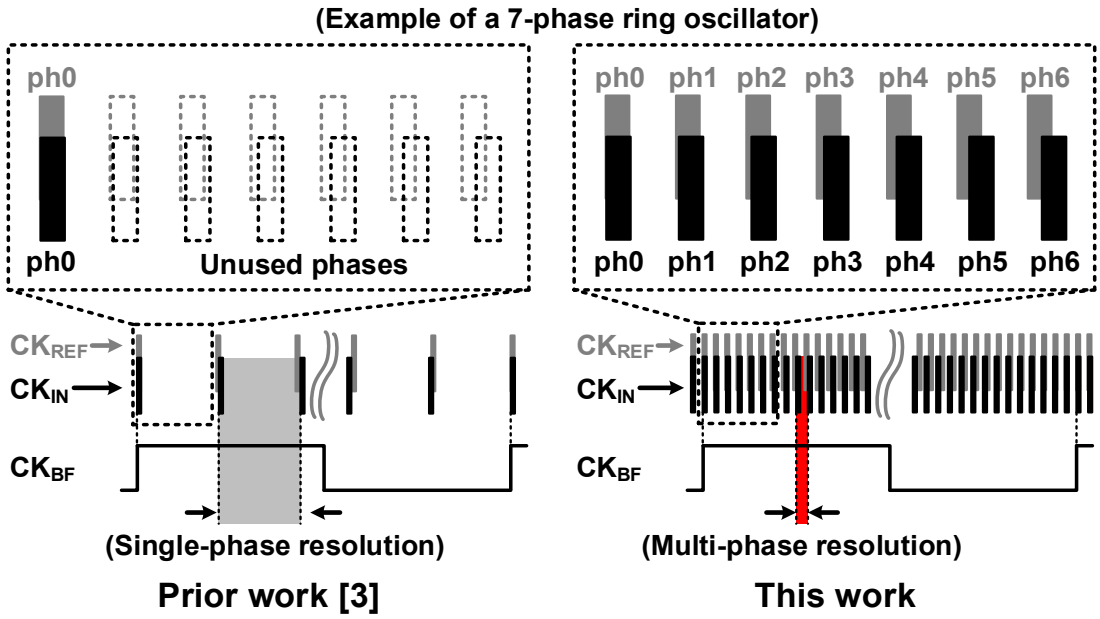


Fig. 4.9. Multi-phase BF quantization improves the timing resolution by a factor of N where N is the number of phases in the ring oscillator.

Fig. 4.10 contrasts the simulated BF quantizer resolutions with and without the use of multi-phase in addition to the 4x oversampling and the first-order noise shaping used for the simulation results in Fig. 4.8. All the other simulation conditions are the same with the conditions used for the noise-shaping BF quantizer simulation in Fig. 4.8. The

BF quantizer with 31-phases performs 65.6dB SNDR which is 27.6dB higher than 38dB SNDR with the BF quantization with a single phase. Note that the practical SNDR improvement with the use of multi-phase will be limited due to the fundamental noise floor induced by other components such as the device noise used for building the ADC circuit (see the measured results in Fig. 4.22).

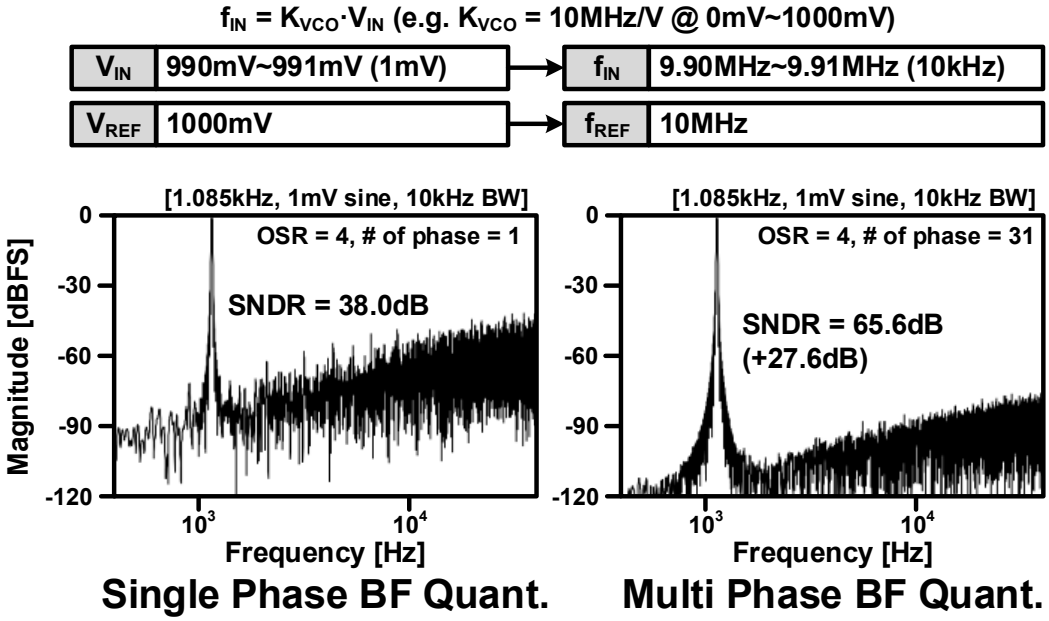


Fig. 4.10. Simulated resolution improvement with the use of multi-phase (i.e. 1-phase vs. 31-phase).

4.4.3 Pseudo-Linear BF Quantization

Fig. 4.11 shows how the BF code is utilized in the previous and the new VCO-based ADC designs. The previous single-phase implementation requires a decoder (denoted as BF DEC in Fig. 4.11) for converting the non-linear BF quantizer output code to a linear code. In contrast, the output code of the new multi-phase design can be directly used by the subsequent blocks due to the higher resolution and superior linearity. This is possible due to the fact that the proposed multi-phase design increases the number of conversion steps by a factor of N where N is the number of phase outputs available. This can be seen in Fig. 4.12, where a single conversion step in the previous single-phase BF-ADC is further divided into 31 levels, offering a 4.95-bit resolution for each conversion step of the single-phase BF-ADC.

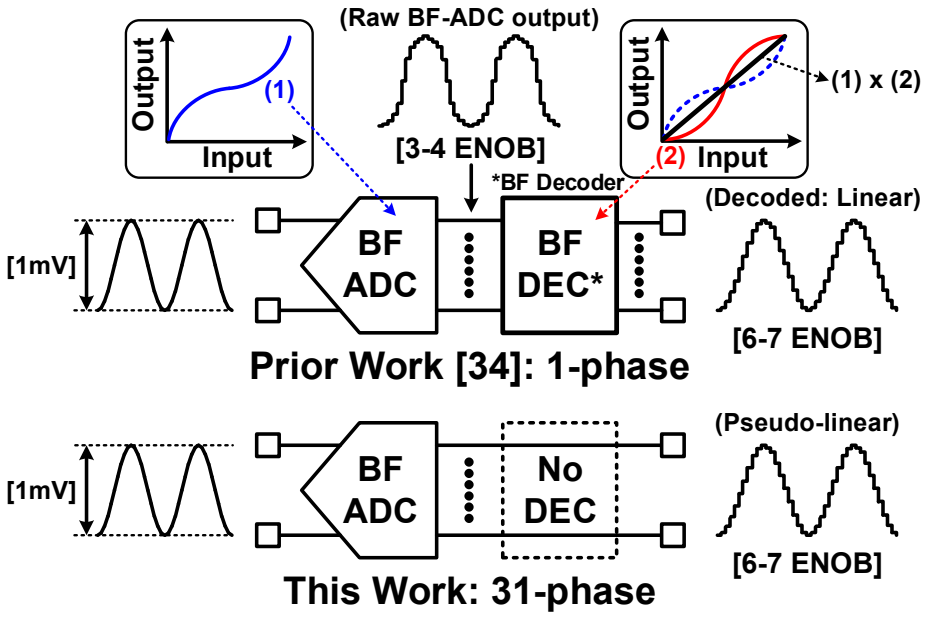


Fig. 4.11. Conversion of non-linear BF output code to a linear code. The proposed multi-phase design does not require BF decoding by incorporating a multi-phase BF quantization scheme which could result in a high resolution (6-7 ENOB) for a narrow (i.e. pseudo-linear) BF output code range.

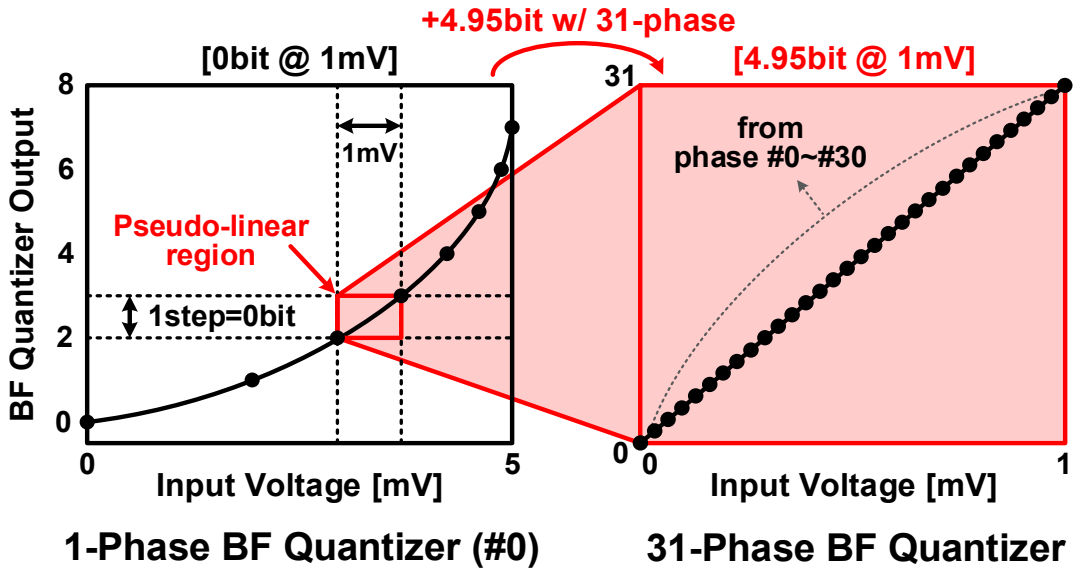


Fig. 4.12. Input voltage versus BF output code showing that a 31-phase design can improve the ADC resolution by 4.95bits compared to a single-phase design. For illustration purpose, a single-ended (i.e. not differential) BF quantizer is assumed here.

Fig. 4.13 shows the simulated ADC linearity (DNL an INL) when no decoding is applied to a 6-bit BF quantizer. For producing the same 6 bit outputs, we assumed the output range is [100, 163] for the single-phase design and [3100, 3163] for the 31-phase design. As a result, BF quantization with 31 additional levels shows a significantly lower DNL and INL (i.e. [-0.02, 0.02], [0, +0.32]) as compared to the values from its single-phase counterpart (i.e. [-0.38, +0.62], [0, +7.82]).

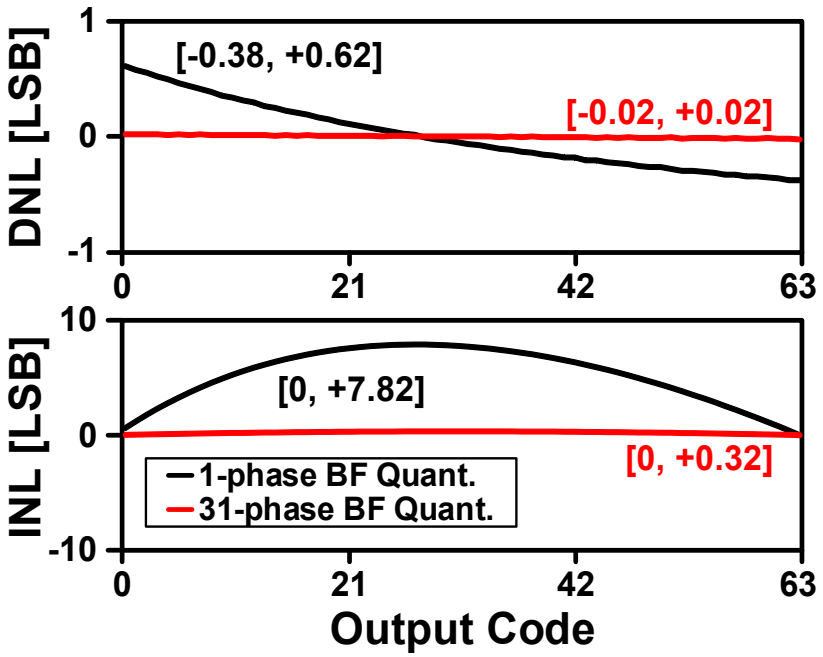


Fig. 4.13. DNL/INL for a 6bit BF quantizer output before BF decoding. Output BF code for a single-phase VCO ranges from 100 to 163, while the 31-phase VCO has a wider output range of 3100~3163. Output code range shown in the plots is from min. code (i.e. 0) to max. code (i.e. 63) for each case.

When dealing with circuit elements such as flip-flops or voltage comparators used to discern small differences in signal timing or voltage levels, metastability becomes a common concern. Although rare, metastability could cause logic failures and negatively impact the ADC linearity. The topic of metastability in VCO-based quantizers deserves a separate in-depth treatment. However, previous work [35] on VCO-based ADCs have shown that this new class of ADC has a lower probability of a metastable event compared to conventional voltage comparator-based quantizers.

Fig. 4.14 provides a comparison between various VCO-based ADCs including the proposed one with the noise-shaping multi-phase BF quantizer. While having the unique high resolution sensing capability for sub-mV input signals like the prior work [34], the

key features from the conventional VCO-based ADC including the noise-shaping and multi-phase properties have been also implemented in this work for achieving the higher resolution. In addition, the BF decoding is not required in this work due to the improved linearity with the use of multi-phase. Since we don't need the post-processing (i.e. decoding) for linearizing the quantizer outputs, the proposed BF quantizer also can be used as a quantizer for a higher-order continuous-time delta-sigma modulator (CT-DSM) to achieve even higher resolution. As an example, a prototype 3rd-order CT-DSM with the proposed BF quantizer is introduced with its SNDR simulation results in section 4.5.

	Conventional VCO-based	Prior work [34]	This work
Quantization Scheme	Linear Counting	Beat Freq. Counting	Beat Freq. Counting
Freq. Detection Sensitivity* (@ 100 counts)	Low (1%)	High (0.01%)	High (0.01%)
Noise-Shaping	Yes	No	Yes
Multi-Phase	Yes	No	Yes
BF Code Utilization	-	Wide (Nonlinear)	Narrow (Pseudo-linear)
BF Decoding	-	Required	Not Required

*Freq. step required for a count change of one

Fig. 4.14. Comparison between conventional VCO-based, prior work [34] and this work.

4.5 Higher-Order Continuous-Time ΔΣ Implementation

An advanced high-resolution ADC architecture such as a higher-order continuous-time delta-sigma modulator (CT-DSM) is another ADC candidate for the direct acquisition of sub-mV input signals. By employing the proposed BF quantizer as a multi-bit comparator of the CT-DSM, we can achieve the higher order of noise-shaping in addition to the inherent first-order noise shaping property from the quantizer itself. Since we do not require the BF decoding procedure due to the improved linearity by using the multi-phase VCO outputs as explained in Section 4.4.3, the BF quantizer output is directly used as the digital input code at the resistor digital-to-analog (RDAC) block. The cascaded 2^{nd} order delta-sigma operation is done via two conventional integrating amplifier circuits shown in Fig. 4.15.

The benefits of using the existing first-order noise-shaping VCO-based quantizers in the higher-order CT-DSM has been already proved with its high resolution ADC performance while using the simpler circuitry than the conventional CT-DSM with voltage comparators [29, 35, 37]. Fig. 4.15 shows a prototype third-order CT-DSM with N-bit differential BF quantizer. The N-bit BF quantizer output is converted to a 2^N-bit dynamic element matched (DEM) thermometer code to control 2^N unit resistor digital-to-analog converters (RDACs). Fig. 4.16 shows the simulated BF quantizer resolution with and without the use of the additional two orders of noise-shaping based on the proposed CT-DSM loop architecture. All the other simulation conditions are the same with that used for the noise-shaping BF quantizer simulation in Fig. 4.8. The prototype third order CT-DSM with the first-order BF quantizer performs 47.2dB SNDR which is 9.2dB higher than 38dB SNDR with the first-order noise shaping BF quantizer.

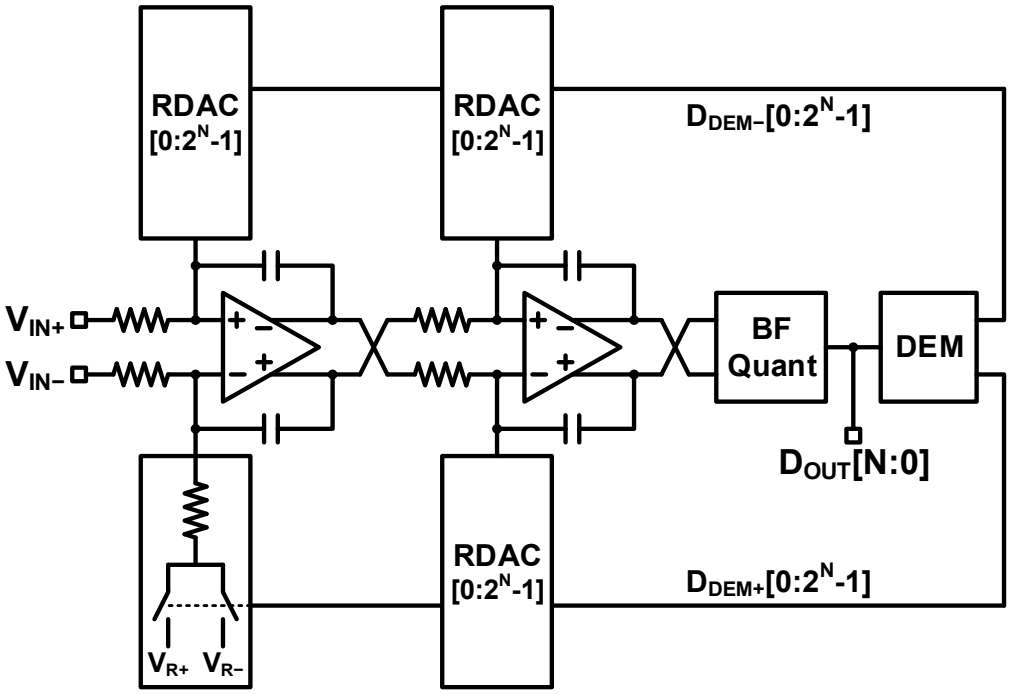


Fig. 4.15. The use of proposed circuit as a quantizer of higher-order continuous-time ΔΣ modulator.

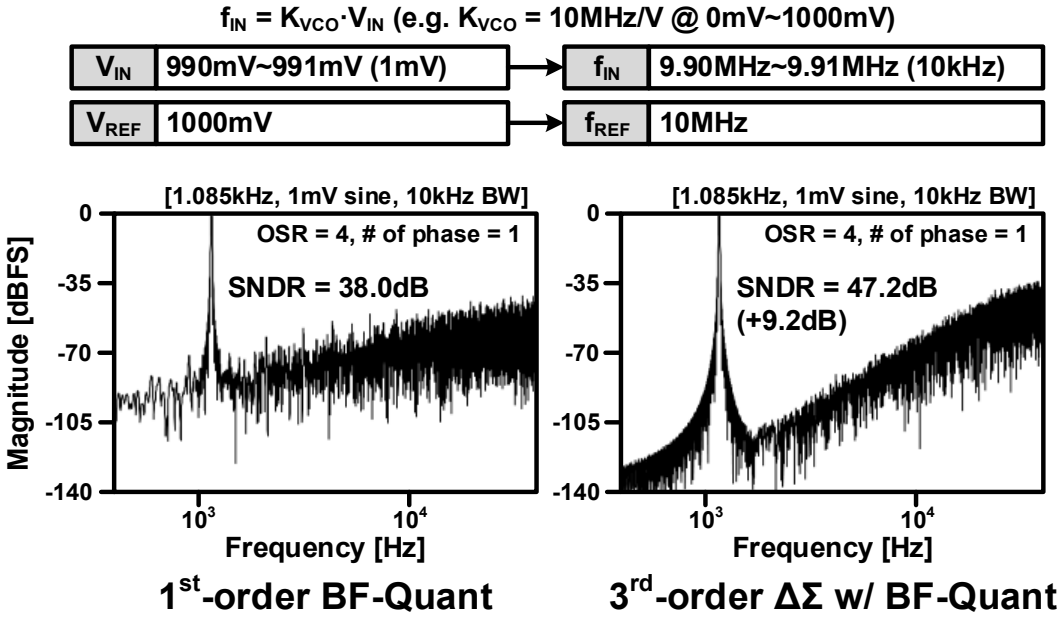


Fig. 4.16. Simulated resolution improvement with different orders of continuous-time ΔΣ modulator.

4.6 ADC Circuit Implementation in 65nm CMOS

Fig. 4.17 shows the implementation details of the proposed VCO-based ADC. Differential input signals V_{IN+} and V_{IN-} individually control the frequencies of the two 31-stage ring-oscillators. Each delay stage output is connected to a dedicated BF quantizer block. Each quantizer contains a positive and negative BF circuit for measuring frequencies (f_{REF}–f_{IN+}) and (f_{REF}–f_{IN-}), respectively. A separate 31-phase VCO is used to generate the reference clocks for the positive and negative BF quantizers. After the BF signal has been detected, sample/reset pulses are automatically generated by the self-timed short pulse generator block in Fig. 4.18. These pulses are then used to sample the current BF count and reset the counter for the next cycle. To ensure uninterrupted noise-shaping operation without missing a count, the pulse width is kept short enough to fit within a single input clock cycle. Finally, the digital output codes from all 31 BF quantizers are summed up and sampled by the system clock (i.e. CLK_S) to produce the final ADC output. The detailed ADC timing diagram is described in Fig. 4.19. By summing up the BF quantizer outputs from each VCO stage, the number of conversion steps we can obtain increases by 31x resulting in a higher ADC resolution. Alternatively, we can read out the individual BF counts of each stage without summing them up, in which case we can achieve a higher sampling rate while maintaining the same resolution.

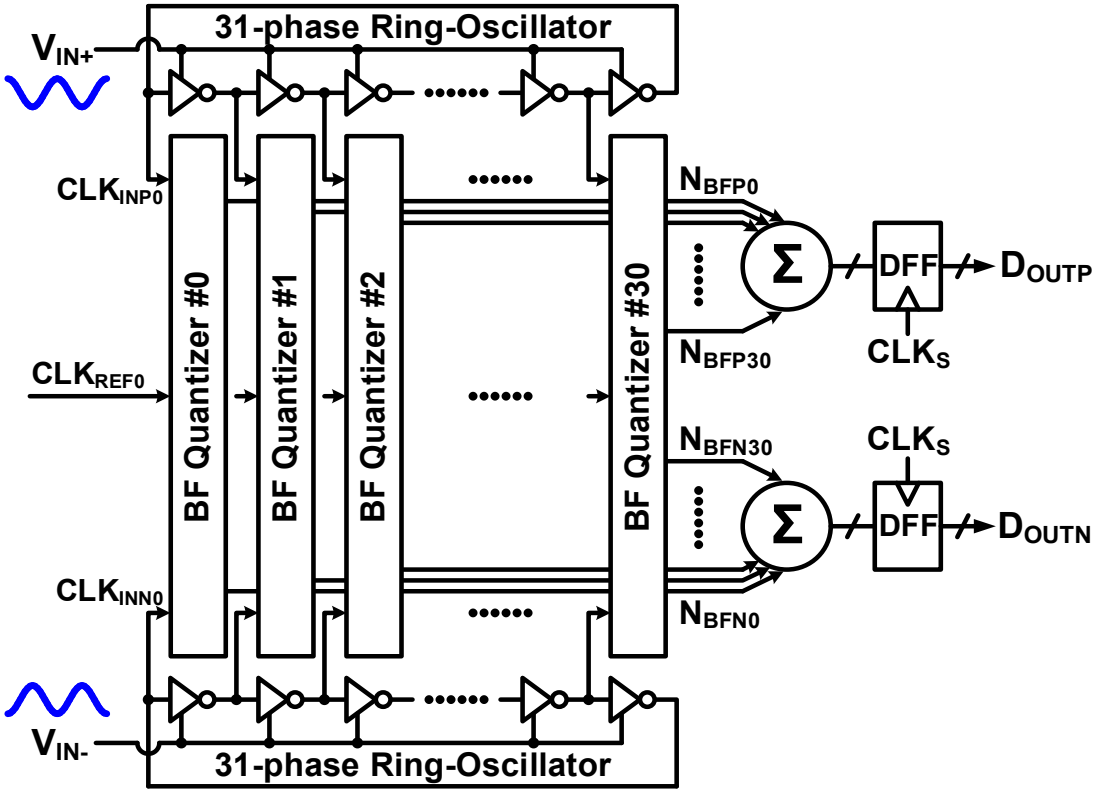


Fig. 4.17. Proposed multi-phase VCO-based ADC with an array of differential noise-shaping BF quantizers.

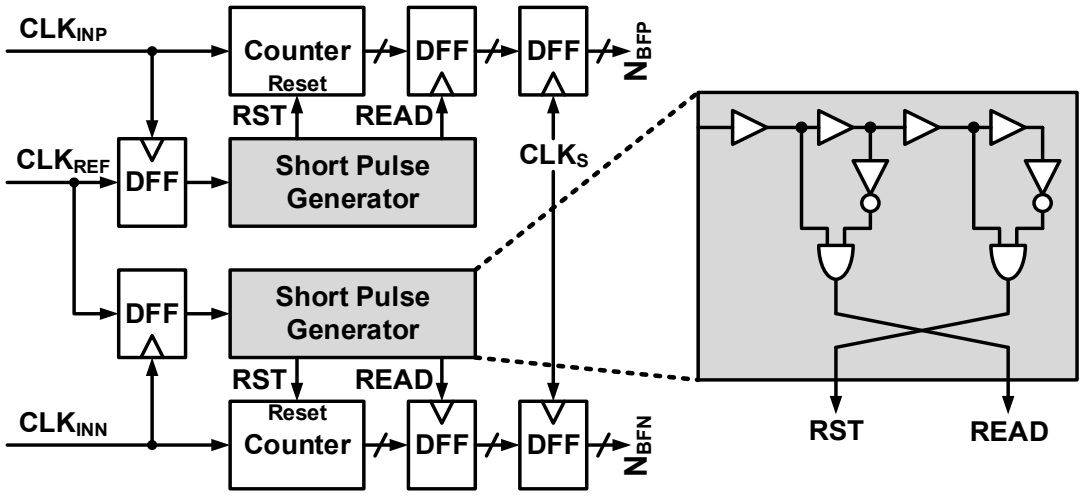


Fig. 4.18. Differential beat frequency (BF) quantizer circuit.

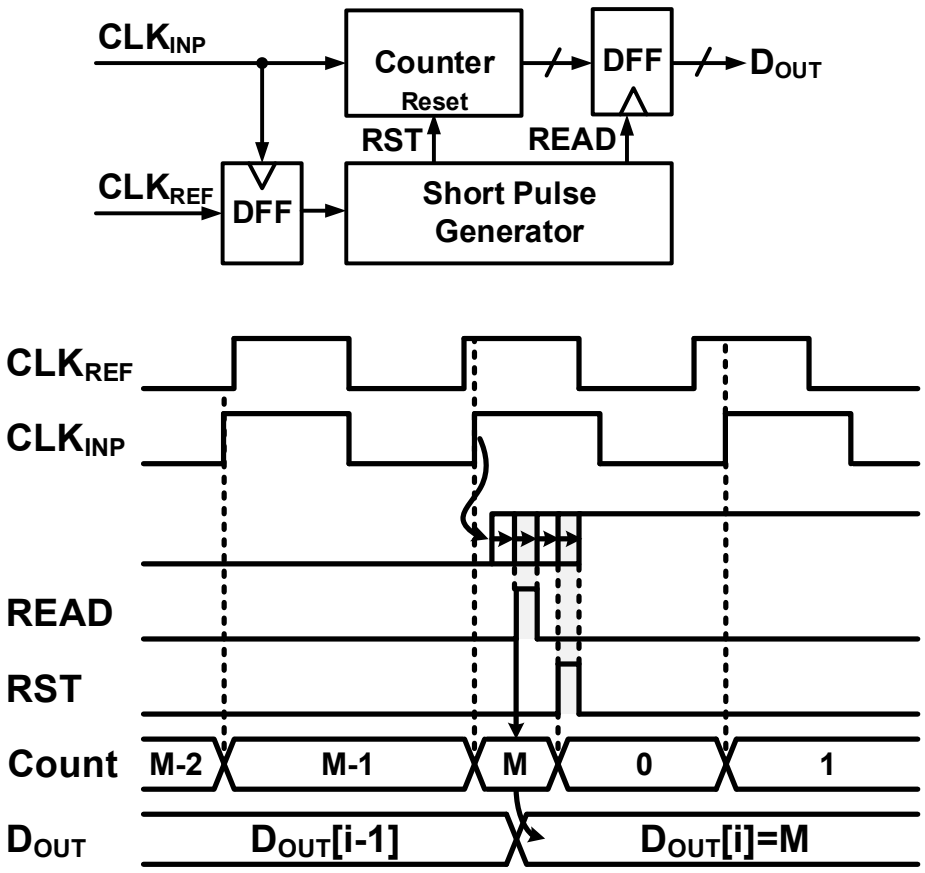


Fig. 4.19. BF quantizer timing diagram.

4.7 Test Chip Measurement Results

A test chip was fabricated in a 65nm LP CMOS process to demonstrate the proposed VCO-based ADC circuit concept and its performance. Fig. 4.20 shows the noise-shaping behavior of the proposed ADC when a small ramp input is provided. Note that the proposed multi-phase BF quantizer based ADC has a linear input-output relationship and a 31x wider output range compared to the single-phase implementation under the same test condition.

Fig. 4.21 depicts the measured SNDR as a function of input amplitude for a 1.85kHz sinusoidal input sampled at 300kHz per BF count, assuming a bandwidth of 10kHz. The results show a 43dB SNDR at -60dBFS (i.e. 1mV) for the multi-phase design which is 10dB higher than its single-phase counterpart. Fig. 4.22 shows the measured ADC output spectrum for a 1.85kHz 1mV sinusoidal input signal using a 65536-point FFT. Fig. 4.23 compares the proposed ADC with previous VCO-based ADCs in terms of various performance metrics. The die photo of the test chip is shown in Fig. 4.24 indicating an active area of 0.258mm^2.

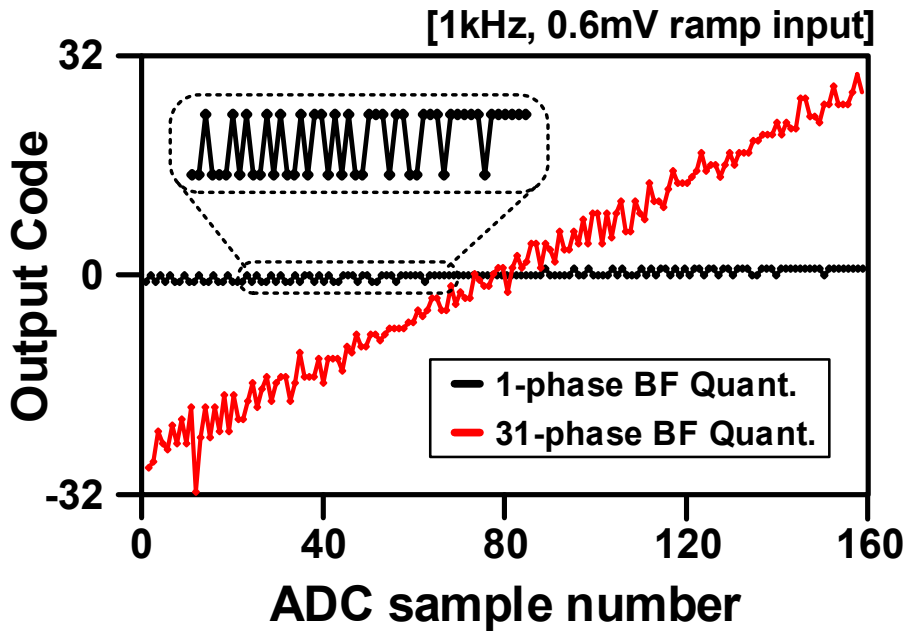


Fig. 4.20. Measured ADC output code for a 0.6mV ramp input.

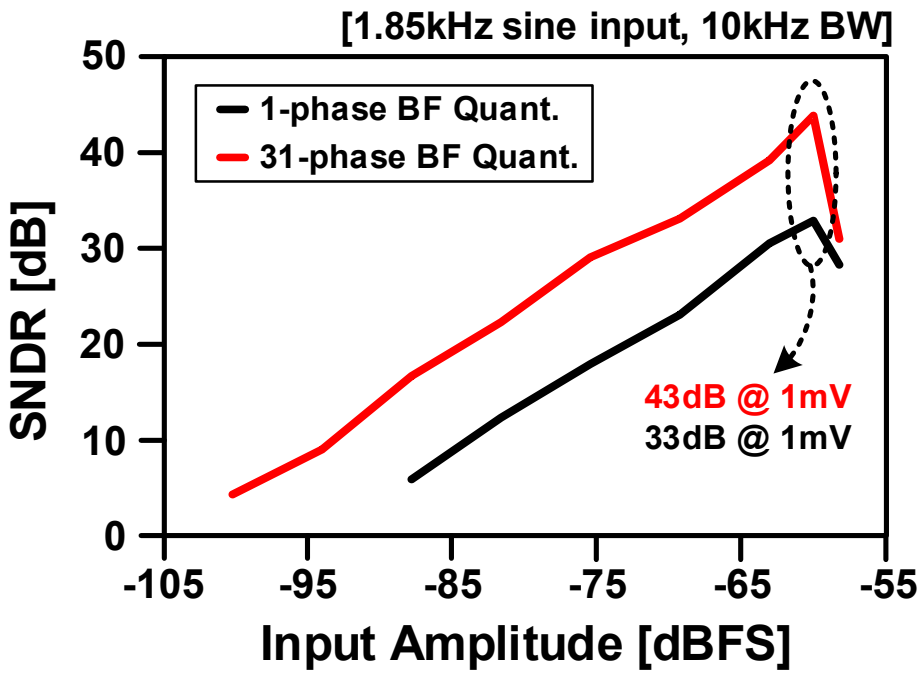


Fig. 4.21. Measured SNDR vs. ADC input amplitude for a 10kHz signal bandwidth. Here, the full-scale is assumed to be 1V, although the input range of interest is 1mV (i.e. -60dBFS).

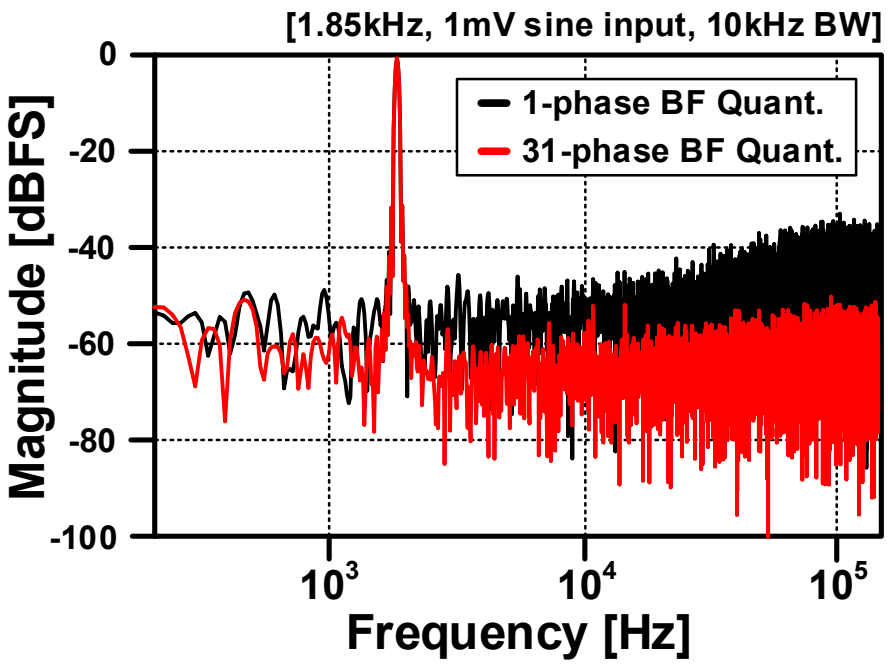


Fig. 4.22. Measured FFT of a 1.85kHz, 1mV sine input under a bandwidth of 10kHz and a sampling rate of 300kS/s. SNDR is 43dB (i.e. ENOB = 6.85) and SFDR is 56.7dB for the 31-phase BF-ADC.

	[38] VLSI'07	[36] VLSI'11	[34] CICC'13	This work
Process	0.13μm	90nm	65nm	65nm
Supply	1.2V	N/A	1.2V	1.2V
Sample Rate	950MHz	640MHz	4.17kHz	300kHz
Input BW	20MHz	8MHz	2kHz	10kHz
$SNDR_{1mV}$*	12dB	3dB	35dB	43dB
$ENOB_{1mV}$*	1.70	0.21	5.52	6.85
SFDR[dB]	N/A	71.4	41.9	56.7
IN_{0dB}[dBFS]**	-70	-63	-89	-105
Power	38mW	4.3mW	0.92μW	36μW
Area[mm^2]	0.185	0.10	0.013	0.258

* Peak SNDR/ENOB for a 1mV input amplitude.
** Input amplitude at SNDR = 0dB (dBFS @ full-scale = 1V)

Fig. 4.23. Performance comparison table.

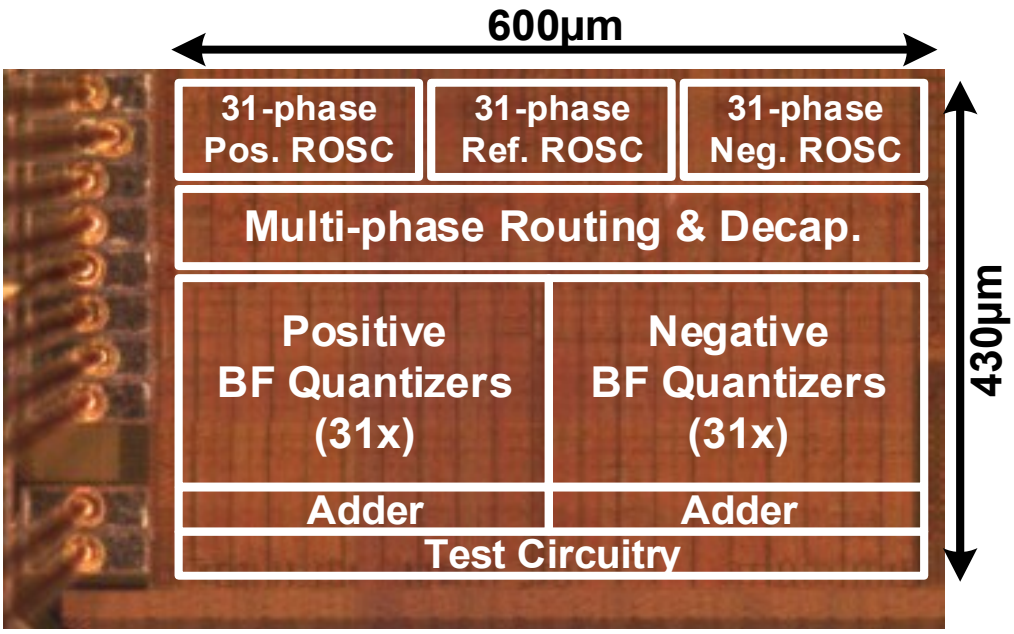


Fig. 4.24. 65nm test-chip die photo.

4.8 Conclusion

In this paper, we present the operating principle, circuit design, and experimental data of a VCO-based ADC featuring a multi-phase noise-shaping beat frequency (BF) quantization scheme. The simulated SNDR results with different VCO-based ADC circuit configurations are provided for verifying the usefulness of the proposed circuit techniques. Measured data from a 65nm test chip shows a 43dB SNDR (or 6.85 ENOB) for a 1mV input signal with 10kHz signal bandwidth when sampled at a frequency of 300kHz. The ADC consumes 36μW when operating under a 1.2V supply and occupies an active area of 0.258mm^2. In addition, we also introduce the possible utilization of the proposed VCO-based ADC as a multi-bit quantizer in the closed-loop CT-DSM for achieving even higher resolution.

Chapter 5. Three-Step TDC with a Switched Ring Oscillator Based Time Amplifier

This chapter proposes a TDC based on a novel time amplifier. The switched ring oscillator based time amplifier (TA) with scalable all-digital circuitry guarantees the precise gain control without calibration. Three stages of TDC circuits with a single TA are used for achieving 9bit digital outputs with a 1.8ps time resolution.

5.1 Introduction

Time-to-digital converters (TDCs) have been used in various applications including digital phase-locked loops (DPLL), time-of-flight imagers, on-chip skew and jitter measurements, and nuclear experiments. Recently, the TDCs have become increasingly important as the wide variety of applications utilize DPLLs [39-43] as the clock generators in lieu of the conventional type-II (i.e. charge pump based) analog PLL. Just like all the other digital circuits replacing their analog counterpart, DPLL has several advantages such as the supply noise insensitivity, tolerance on PVT variations, easy scalability and the lowered power and area consumption with respect to the process scaling.

Fig. 5.1 contrasts the basic circuit building blocks for both analog and digital PLL. While the charge pump (CP) in analog PLL converts the input phase difference between reference and feedback clocks to the output charge (or current), the TDC outputs the digital code corresponding to the phase difference. Therefore, the passive loop filter (LF) with large charge storing capacitors which occupy a significant area of analog PLL is replaced by a compact digital loop filter (DLF) in DPLL. By doing so, DPLL could

achieve a significantly lower area consumption than analog PLL. The simple and easy re-configurability is another advantage of using the TDC and DLF in DPLL instead of CP and LF in analog PLL.

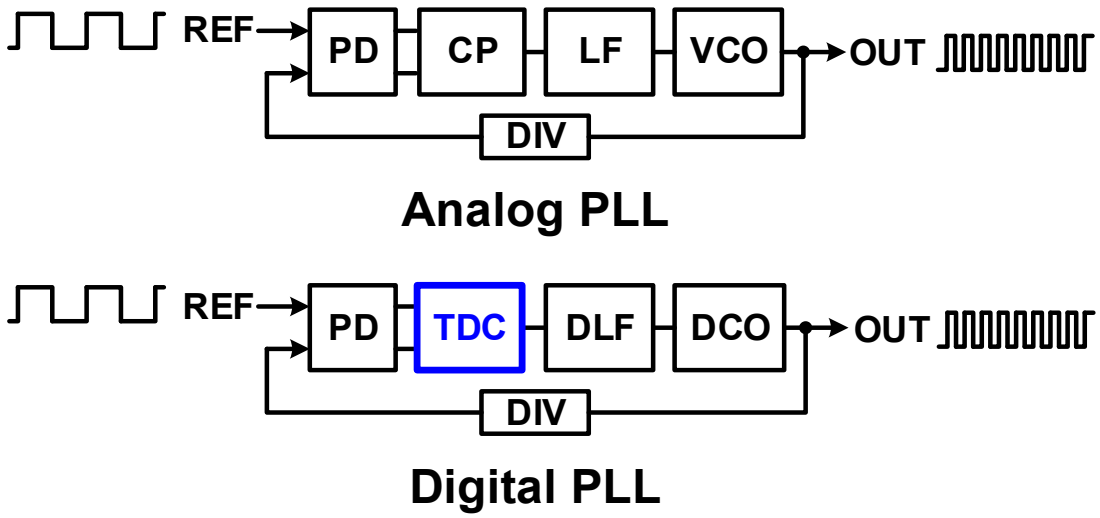


Fig. 5.1. Analog and digital PLL block diagrams.

While having the low area consumption and the benefits from using digital circuitry, the degraded output noise performance due to the quantization error is the key drawback of DPLL. The noise due to the DPLL quantization error is created at the two circuit blocks located at the boundary between the analog (i.e. clock) and the digital (i.e. binary code) domains of DPLL as shown in Fig. 5.2. The two circuit blocks include the TDC which converts the input clock phase difference to the output digital code and the digitally-controlled oscillator (DCO) which converts the input digital code to the output clock frequency (or phase). Therefore, DCO and TDC are the two major building blocks in DPLL which typically determines the overall DPLL noise performance.

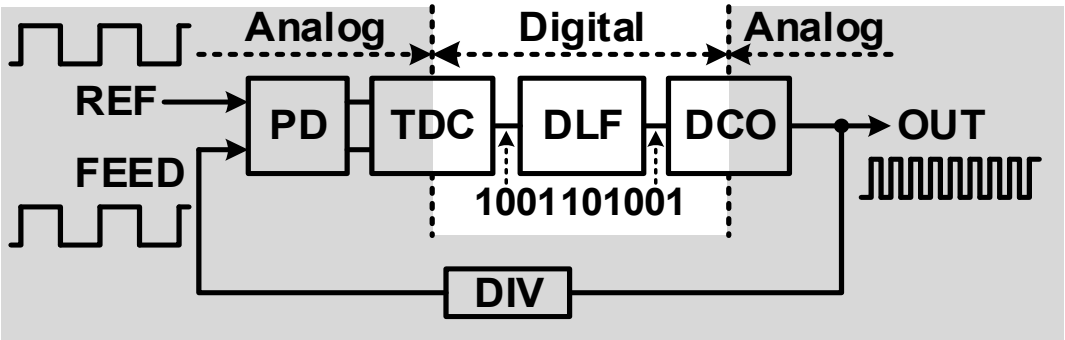


Fig. 5.2. Analog (i.e. clock) and digital (i.e. binary code) domain in DPLL.

While DCO is remained as one of the key DPLL building blocks which affects the PLL noise performance, it is relatively easier to achieve a fine DCO output frequency resolution using the proven techniques. For instance, the DCO gain can be reduced as much as possible to lower the output frequency step (i.e. lower the DCO quantization error) while having the same number of control bits. On the other hand, the design of high resolution TDC is rather involved and it typically requires the intensive use of analog circuitry or the large power consumption for achieving the high resolution.

Delay line (DL) based TDC has been the most widely used TDC due to its simplest circuitry and the fastest conversion time. The DL based TDC shown in Fig. 5.3(a) has a wide input range (i.e. input range = time resolution x 2^{bits}), but it suffers from a poor resolution since it cannot resolve a time difference shorter than a single inverter delay. Therefore, the resolution of DL based TDC depends on the process technology used for the TDC design. In addition, the vulnerability to the PVT variation is another drawback of using the DL based TDC. Vernier Delay line (VDL) is another frequently used TDC circuit technique. The VDL based TDC shown in Fig. 5.3(b) can achieve the higher time resolution than the DL based one by introducing a small delay difference (i.e. ts–tf

where ts is a slow delay and tf is a fast delay) between the two delay lines driven by the Start and Stop signals shown in Fig. 5.3(b). However, it also has limitations such as the narrow input range, long conversion time, and tight device matching requirement.

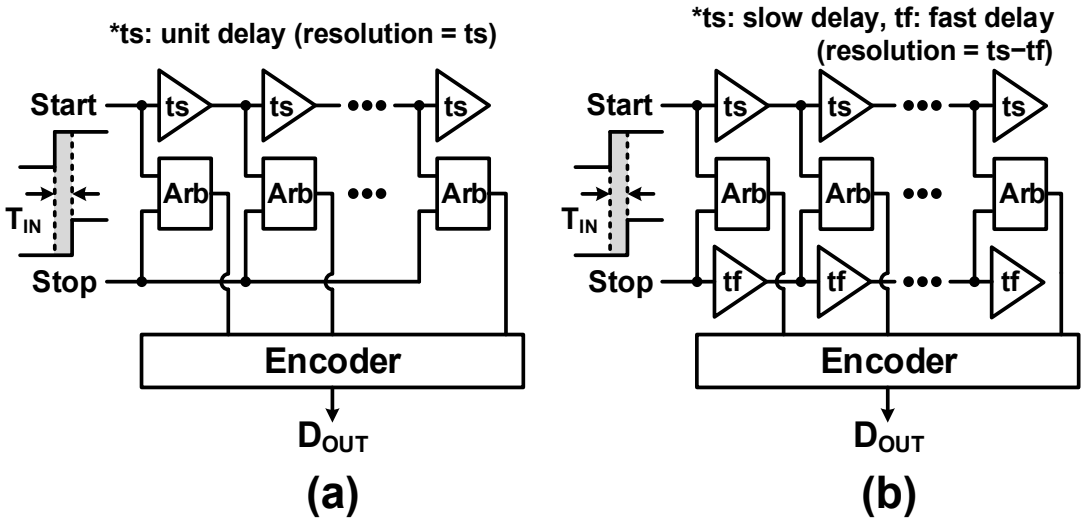


Fig. 5.3. TDC block diagrams based on (a) delay line and (b) Vernier delay line.

Fig. 5.4 contrasts different TDC categories with respect to the two TDC key features (i.e. time resolution on y-axis and input range on x-axis). Time amplifier based TDCs (e.g. two-step, pipeline and cyclic TDC) with multiple TDC stages have been recently gaining traction as a promising approach for achieving both wide input range and high resolution by amplifying the time residue which is typically discarded in the conventional single-stage TDCs. The amplified time residue is re-utilized at the subsequent TDC stages (e.g. fine TDC in two-step TDC) and therefore it can resolve higher time resolution than the conventional TDCs with a single conversion step.

There have been several researches on the time amplifier based TDC designs including two-step [44, 45], pipeline [46, 47] and cyclic [48] TDC utilizing the existing

time amplifier circuits based on the SR-latch metastability [44] and the discharging time control method [46-49]. However, previous time amplification techniques have several limitations including the narrow input range and unreliable gain that is susceptible to die-to-die and within-die variation. In this work, we propose a novel time amplifier based on all-digital switched ring oscillator circuit which guarantees a precise gain control throughout the wide input range without calibration.

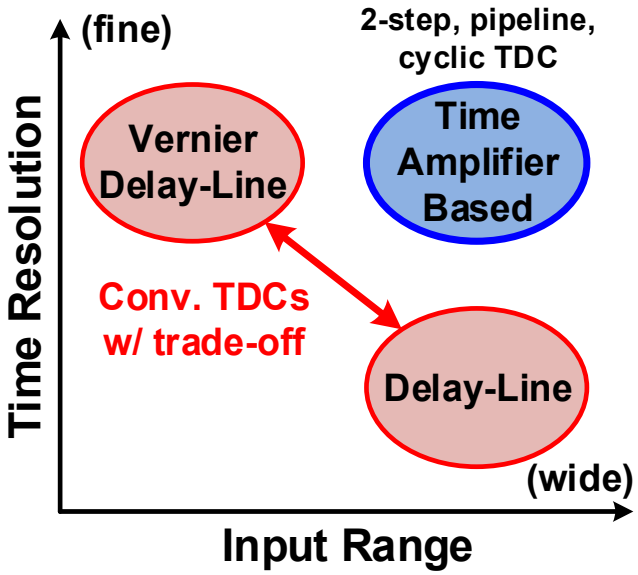


Fig. 5.4. TDC categories with resolution and input range.

The remainder of this chapter is organized as follows. Section 5.2 reviews the existing time amplifier circuit techniques used for TDCs with high resolution and wide input range. Section 5.3 describes the concept of the proposed switched ring oscillator based time amplifier. The implementation details of the 65nm TDC test chip is shown in Section 5.4. The test chip measurement results are given in Section 5.5 and Section 5.6 concludes the chapter.

5.2 Time Amplifier Based Time-to-Digital Converters

Fig. 5.5 shows the existing time amplifier based TDC circuits. The two-step TDC (or coarse-fine TDC) circuit in Fig. 5.5, upper is consist of a pair of coarse and fine TDC and a time amplifier (TA) in between the two TDCs which amplifies the time residue from the coarse TDC. After the coarse TDC is done with the conversion of time input (i.e. time difference between the rising edges of Start and Stop signals in Fig. 5.5) to the MSB digital output code, TA circuit amplifies the time residue which was supposed to be a quantization error from the coarse TDC. Then, the fine TDC re-quantize the amplified time residue and generates the LSB digital output code.

The pipeline TDC shown in Fig. 5.5, lower is another TDC circuit which utilizes TA. Each pipeline TDC stage is consist of a 1-to-3bit TDC and a time residue generation and amplification circuit which is consist of a 1-to-3bit digital-to-time converter (DTC), a time subtractor and a TA. The output bits from each pipeline stages are encoded to the final TDC output while the amplified time residue is delivered the next stage for the LSB time-to-digital conversions. By pipelining the each TDC stage operations, it could achieve both high resolution and the optimized TDC sampling speed. Note that the pipeline TDC circuit and its operation is analogous to its popular analog-to-digital converter (ADC) counterpart (i.e. pipeline ADC). Likewise, we can build other TA-based high-resolution TDC circuits (e.g. cyclic TDC, delta-sigma TDC, etc.) which are also originated from the existing ADC architectures.

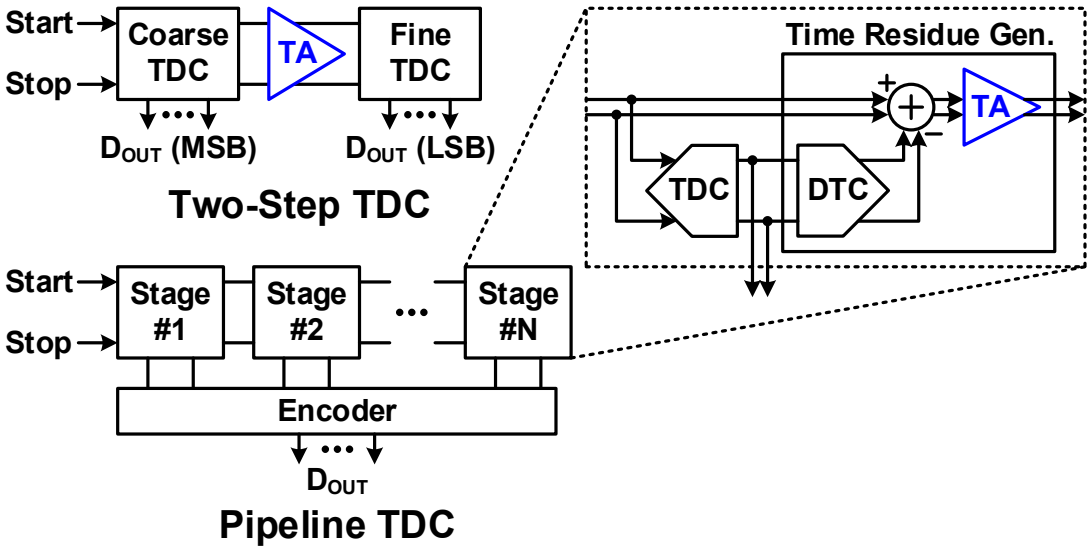


Fig. 5.5. Time amplifier based TDCs: (a) two-step TDC (b) pipeline TDC.

Fig. 5.6 shows three different TAs proposed in the recent literature. The SR latch metastability based TA [44] utilizes the intrinsic dependency between the input time difference and latch resolving time for high gain. This architecture has a relatively narrow input range which may be acceptable for certain applications, but the gain is sensitive to various process parameters and thus this type of TA requires frequent calibration. The gain of TA based on discharging time control method [46-49] shown in Fig. 5.6, upper right quickly degrades for larger time inputs and therefore a dynamic calibration is required to have a constant gain throughout the entire input range. Note that both metastability and discharging time control based TAs inherently work with nearly overlapping input edges due to their high gain and narrow range properties. The pulse train time amplifier [45] has been recently proposed to cope with the shortcomings of prior techniques. However, this design is a pseudo time amplifier in the sense that it does not amplify the time, but integrates repetitive time pulses utilizing a specialized

gated delay line based TDC to mimic time amplification. In addition, non-idealities in the requisite time-to-pulse conversion and gated delay line based TDC may even result in worse TDC performance. This chapter presents the first true time amplifier (TA) with a wide input range and precise gain control by utilizing a ring oscillator circuit that can switch between high frequency and low frequency modes. To verify the new circuit concept, we demonstrated a 9bit three-step TDC employing the proposed switched ring oscillator based TA in 65nm CMOS.

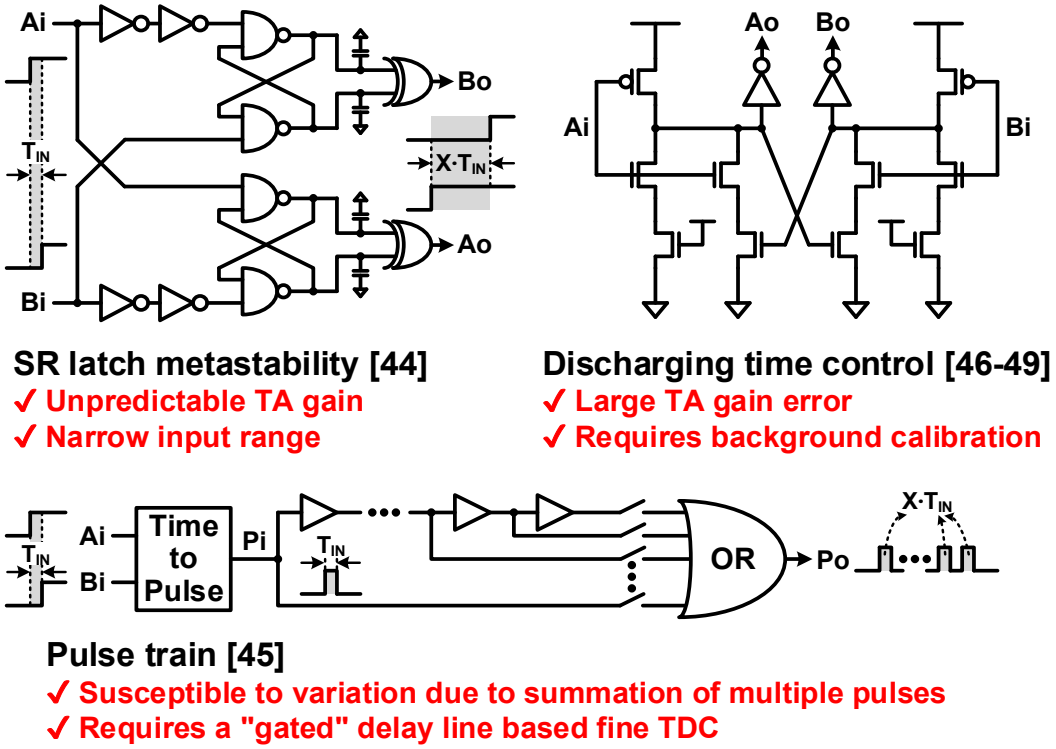


Fig. 5.6. Operating principle and limitations of three existing time amplifiers (TA). Proposed switched ring oscillator (ROSC) based TA can achieve a constant and predictable gain for a wide input range without any real-time calibration.

5.3 Switched Ring Oscillator Based Time Amplifier

Fig. 5.7 and Fig. 5.8 shows the proposed TA circuit and its timing diagram. The TA consists of two identical switched ring oscillators (ROSC) with NAND-based ROSC stages. Each ROSC stage has N+1 unit NAND gates connected in parallel and they are divided into two groups, ND1 and ND2. 1 out of N+1 unit NAND gates is assigned to group ND1 which is always turned on during the TA operation while the other N unit gates are assigned to group ND2 and can be either enabled or disabled. The incoming early (Ai) and late (Bi) input signals are directly connected to the left-most ND2 gates of both ROSCs. Activation of RO1 and RO2 are staggered based on the rising edges of Ai and Bi. Since both ND1 and ND2 groups are enabled initially, both ROSCs are operating at their maximum oscillation frequency. The time input T_{IN} (i.e. the time difference between the rising edges of input signals) is converted to the corresponding phase difference (i.e. Φ_{IN}) between the two ROSC clocks, CK_{RO1} and CK_{RO2}. Then, a self-timed signal EN_{ND2} generated after a CK_{RO2}-to-Q and an inverter delay by the edge detector circuit disables all the ND2 gates. This causes the clock period of both ROSCs to be stretched out by a factor of N+1. Finally, the rising edges of the two ROSC clocks are captured by the edge detectors once the ROSC frequencies are settled. Since the ROSC phase difference is preserved when the ROSCs are switched to a low frequency mode, the equivalent time difference between the rising edges of the two ROSC clocks is now N+1 times longer (i.e. amplified by N+1 times) than the initial difference. Fig.

5.9 is the simulated waveforms which show an example TA operation when the time input is 100ps and the TA gain is set to 8x.

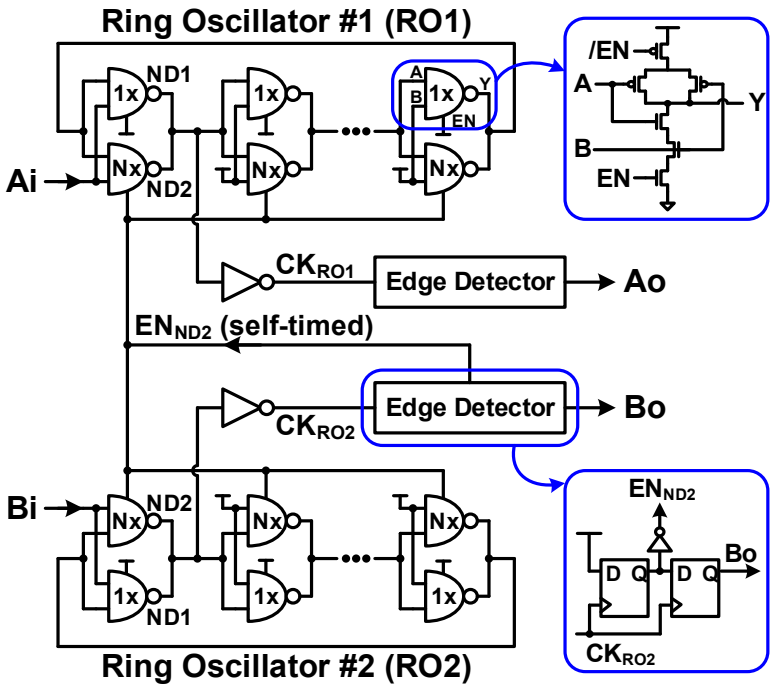


Fig. 5.7. Proposed switched ROSC based TA circuit. TA gain is determined by the sizing ratio between the 1x and Nx NAND gates. For instance, an 8-times TA can be implemented using a sizing ratio N=7.

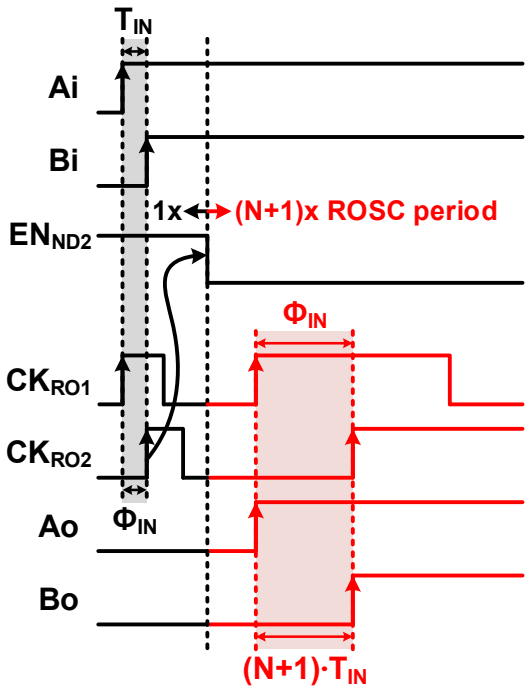


Fig. 5.8. Timing diagram of the proposed TA.

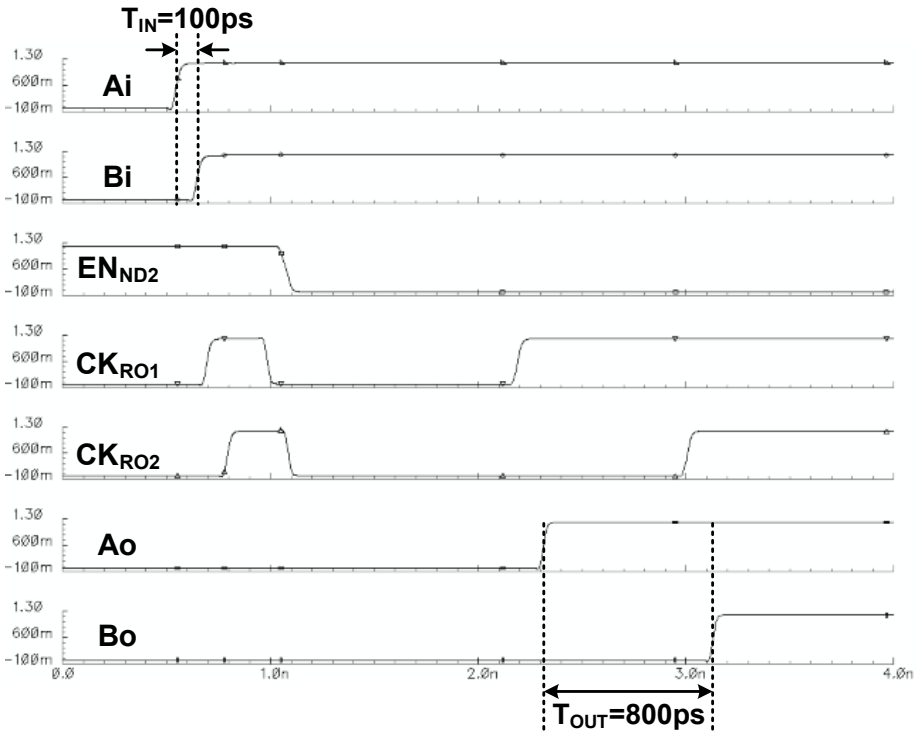


Fig. 5.9. Simulated TA waveforms for N=7 (i.e. 8x TA gain).

Fig. 5.10 describes the transfer characteristics of the proposed switched ROSC-based TA. Before the ROSC clock periods are stretched out, time input (T_{IN}) is converted to ROSC phase difference (Φ_{IN}) with respect to the ROSC frequency (f_{ROSC}) in high frequency mode. As shown in the equations in Fig. 5.10, the slope of the transfer curve is proportional to the ROSC frequency. Therefore, the slope is reduced by a factor of N+1 when the ROSC is switched to an N+1 times lower frequency mode. Since the ROSC phase difference is unchanged after the switch, the corresponding time output becomes N+1 times longer than the time input as the slope has been reduced by N+1 times. The proposed time amplification technique can be implemented for an arbitrary integer gain by simply sizing the NAND gates accordingly.

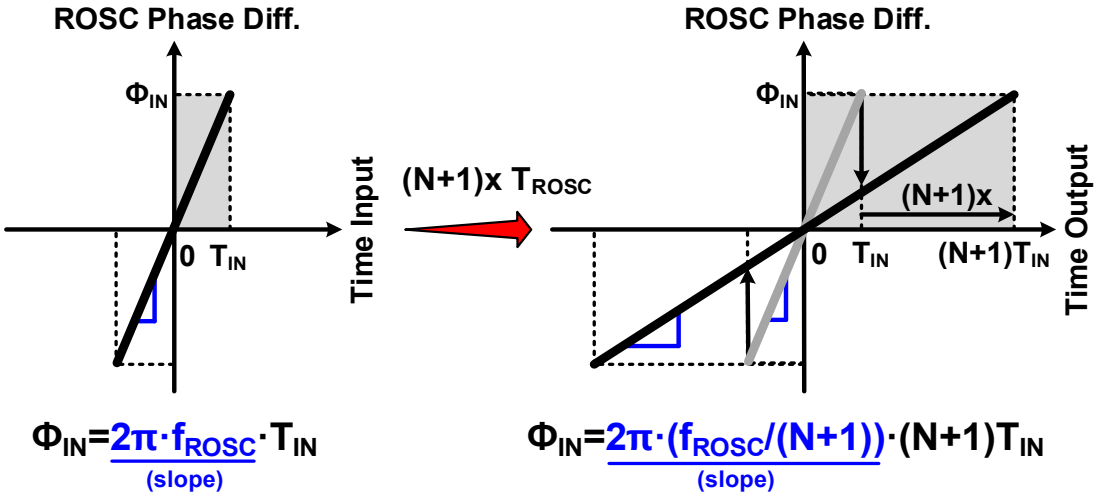


Fig. 5.10. TA transfer characteristics. Using the proposed switched ROSC based TA, the time input TIN is amplified to a time output of $(N+1)\cdot T_{IN}$ by switching to an N+1 times lower ROSC frequency.

Fig. 5.11 shows the simulated 8x (i.e. N=7) TA transfer characteristics and the gain variation with respect to the input range. For a fair comparison, the three different TAs are built and simulated in the same 65nm CMOS process using minimum device sizes. In addition, they are only calibrated at one-point (i.e. 1ps, the minimum time input) to ensure all TAs have a gain of 8x initially. Compared to the existing techniques [39-42] with fluctuating or exponentially decaying gains, the proposed TA shows an almost ideal time amplification gain as indicated by the dotted lines. The simulated ROSC-based TA gain with a 100ps input range varies from -4% to 5% while the gains of the existing techniques vary from either -71% to 15% (for metastability based) or -83% to 3% (for dependent discharging based).

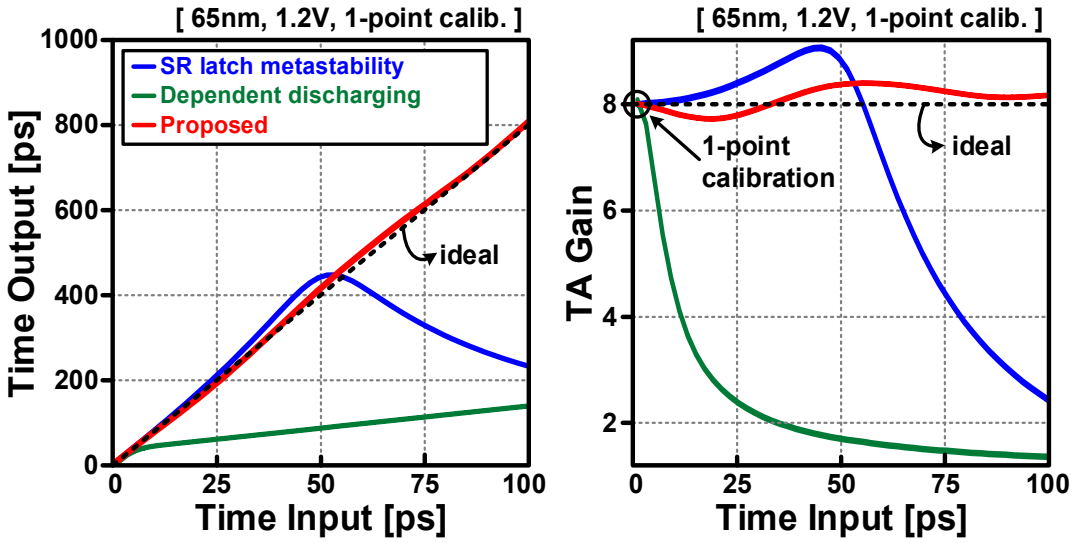


Fig. 5.11. Simulated TA output and gain plots for N=7 (i.e. 8x TA gain) after 1-point gain calibration.

5.4 TDC Circuit Implementation in 65nm CMOS

5.4.1 Three-Step TDC circuit

Fig. 5.12 shows a 3-step TDC circuit to demonstrate the proposed TA technique. The TA is inserted after a 4bit coarse resolution delay line TDC to amplify the time residue. The 8x time amplification combined with a 3bit medium resolution delay line TDC improves the TDC resolution by 8-times compared to that of a single stage delay line TDC. The medium resolution TDC is followed by an additional TDC stage to achieve an extra 2bit resolution. A 2bit Vernier delay line TDC has been used as the fine TDC to resolve a 4x higher time resolution with only an additional conversion time of 4 buffer delays. The fast buffer delay (tf) of the fine TDC is controllable using 6bit capacitor banks located at each inverter stage. The delay is tuned so that it ensures high linearity of the 2bit fine resolution. Overall, a total of 32-times higher resolution than a single buffer delay has been achieved by means of a 8x ROSC-based TA and a 2bit Vernier delay line based fine TDC. Fig. 5.13 shows the timing diagram which includes the essential internal signals in the three-step TDC operation.

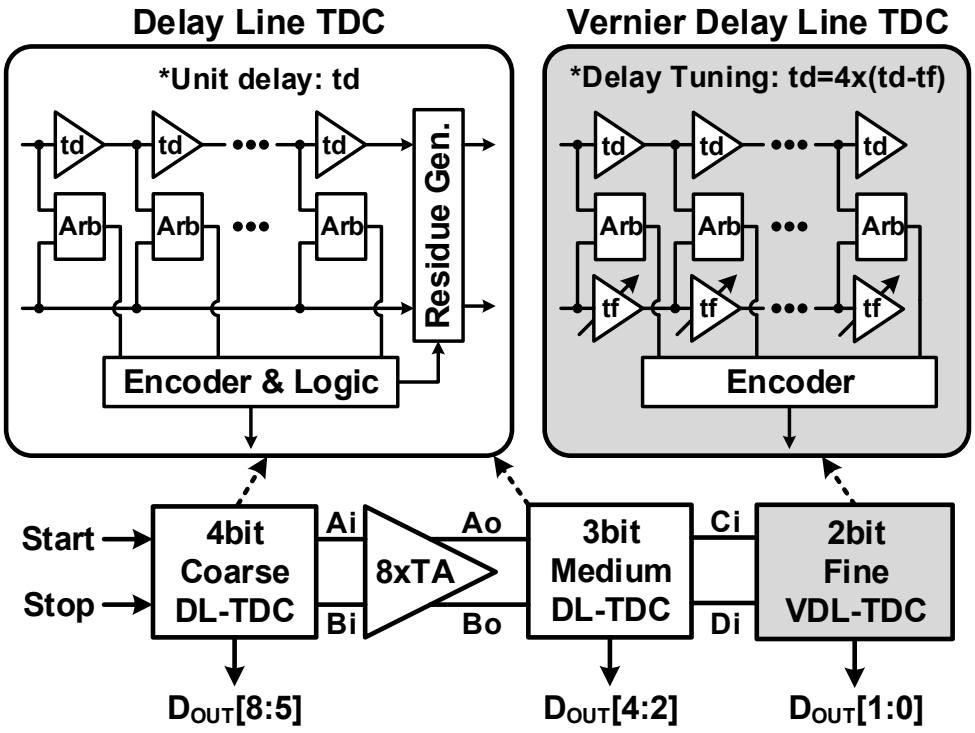


Fig. 5.12. Block diagram of a three-step TDC utilizing the proposed switched ROSC based TA. A two-step 7 bit TDC with the proposed 8x TA is followed by a 2bit VDL based TDC to achieve extra fine time resolution.

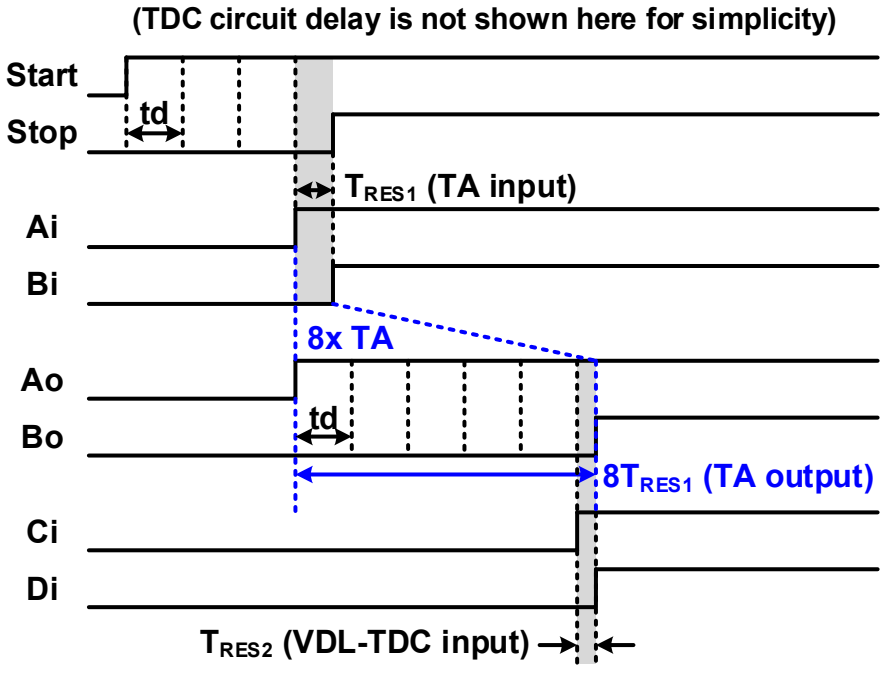


Fig. 5.13. 3-step TDC timing diagram.

5.4.2 TDC Circuit Building Blocks

Fig. 5.14 shows a 4bit Delay line (DL) based TDC circuit which is a coarse TDC of the proposed three-step TDC. 16x unit DL stages required for 4bit TDC output are grouped into 4 cascaded 4x DL stages. Each group of 4x DL stages is consist of a pair of buffer and 4 stages of unit delay and an arbiter circuit [48]. The number of DL stages per group (i.e. 4) has been chosen based on the drivability of the buffers in each group. Dummy arbiter circuits are also added in the Start signal delay path to minimize the nonlinearity effects while DL-based TDC is operating. Once the arbiter outputs are settled for each sampling cycle, the 16bit thermometer code outputs from the 16x DL stages are converted to a 4bit binary code output of DL-TDC. The 4bit binary output is also used for generating the time residue output (i.e. the time difference between the rising edges of $Start_{RES}$ and $Stop_{RES}$). A 3bit medium resolution TDC also has the same DL-based TDC circuit configuration while having the different number of unit DL stages (i.e. 8x DL stages for 3bit TDC output).

Fig. 5.15 describes a 2bit Vernier delay line (VDL) TDC circuit which works as a fine TDC of the proposed TDC. In addition to the delay stages of the DL-based TDC circuit, additional delay stages for Stop signal propagation with the faster delay are implemented for the VDL-based TDC operation. The delay difference between the slower unit delay which has been already used for the DL-based TDC and the added faster delay determines the resolution of the fine VDL-based TDC. While the conventional VDL-based TDC consumes a large conversion time, the additional conversion time due to the implemented 2bit fine VDL-based TDC is negligible compared to the entire conversion time while providing 2 more output bits for achieving

the higher TDC resolution compared to the conventional two-step TDC. Fig. 5.16 shows the arbiter circuit [48] and the unit delay circuit consisting of a pair of inverter and 6bit binary weighted capacitor banks in between them. By controlling the capacitor banks in the faster delay cells in VDL-based TDC, we can program the faster delay to be 3/4 delay of the slower delay (or unit delay of DL-based TDC). By doing so, the VDL-based TDC time resolution becomes td/4 and therefore, the VDL-TDC works as a 2bit fine TDC.

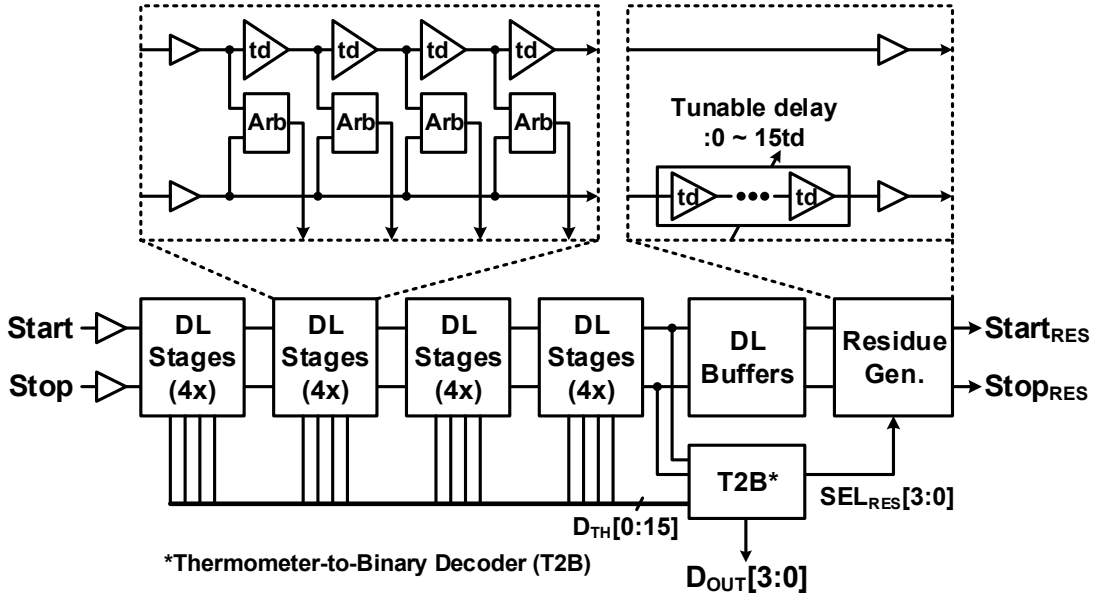


Fig. 5.14. Delay line based TDC circuit (4bit coarse TDC).

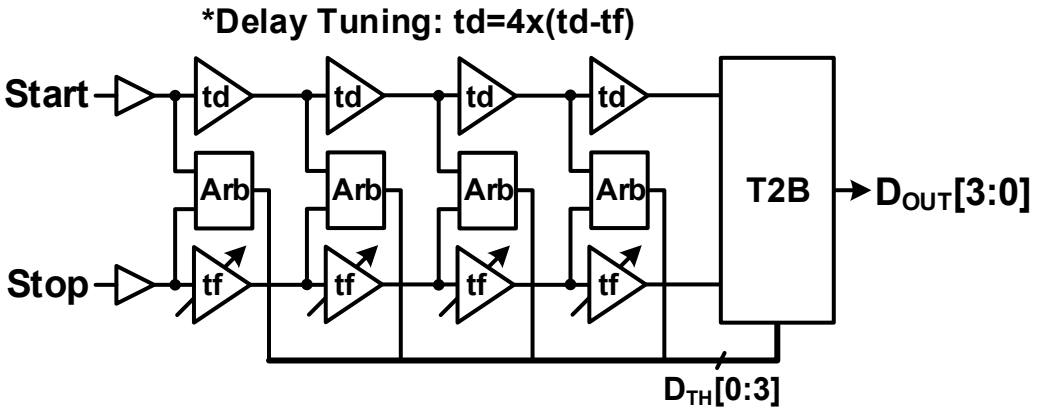


Fig. 5.15. Vernier delay line TDC circuit.

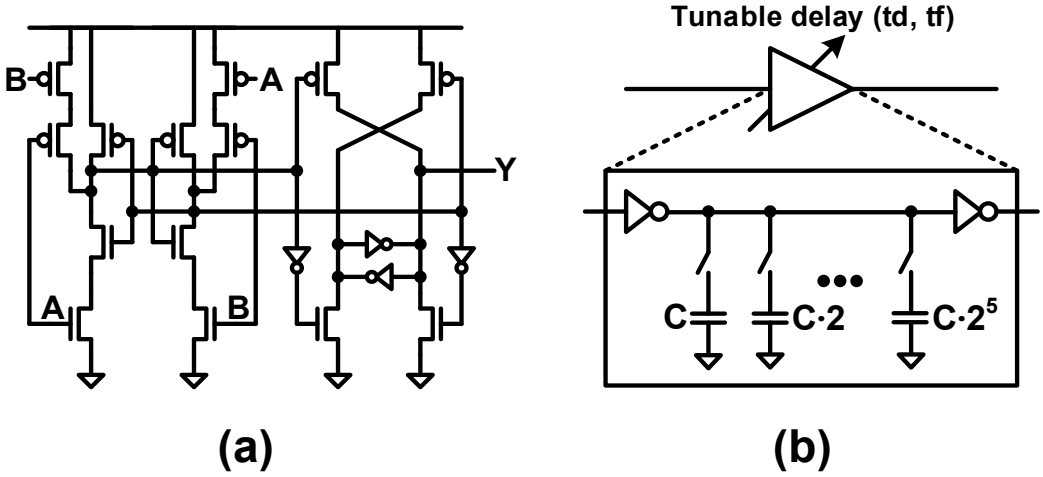


Fig. 5.16. TDC sub circuits: (a) Arbiter [48] and (b) A tunable delay (td and tf in Fig. 5.12) with 6bit binary weighted capacitor banks.

5.5 Test Chip Measurement Results

Fig. 5.17 and Fig. 5.18 shows the measurement results of the test chip implemented in a 65nm CMOS process. For the linearity test of the proposed TDC, a ramp time input is generated by taking two clock signals with a slight frequency difference from an external waveform generator (Agilent 81160A). The TDC transfer curve is obtained by collecting code counts and it is compared with the ideal transfer curve to show the differential errors (DNL) and absolute errors (INL). With no calibration, the TDC achieves a maximum DNL of 0.9/1.9LSB and the maximum INL of 3.7/10LSB for 2-step/3-step operating modes, respectively. Variation in the output codes for three different external delays was also measured and the results show a standard deviation ranging from 0.62LSB to 2.86LSB. The performance summary including comparisons with prior designs are shown in Fig. 5.19. The TDC consumes 2.2mW when operating at 1.0V and it occupies an active area of 0.068mm^2. The chip microphotograph is shown in Fig. 5.20.

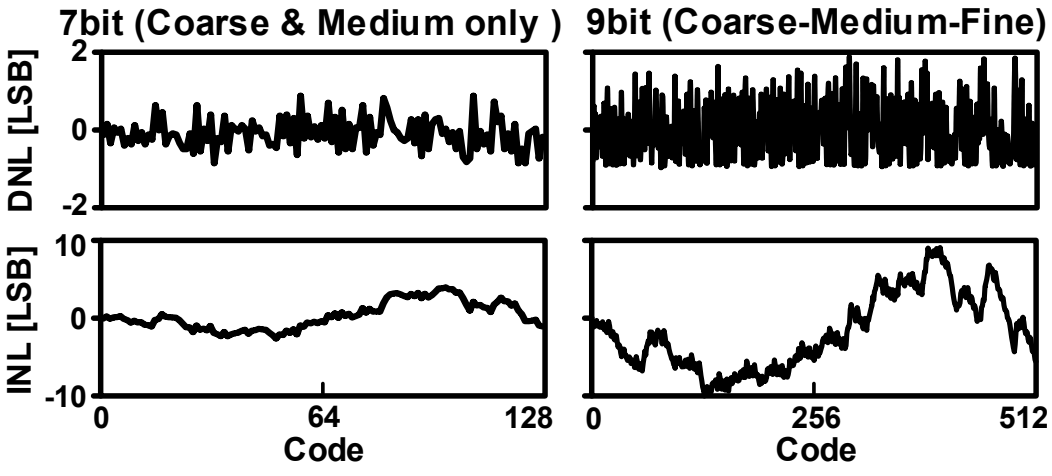


Fig. 5.17. TDC linearity (DNL/INL) measurement results.

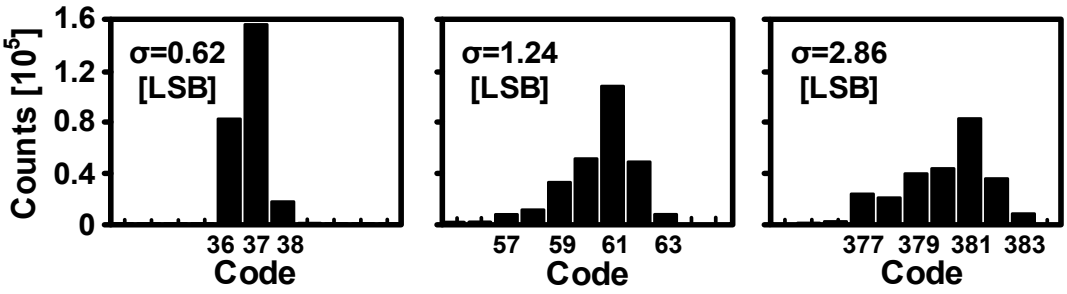


Fig. 5.18. TDC one-shot measurement results.

		[44]	[46]	**This Work**	
Process		90nm	130nm	**65nm**	
TA	Scheme	Metastability	Disch. Ctrl	**ROSC-based**	
	In. Range*	21ps	3ps	**100ps**	
	Gain Error**	-71%~+15%	-83%~+3%	**-4%~+5%**	
	Calibration	Required	Required	**Not Required**	
TDC	Conv. rate	10MS/s	65MS/s	**80MS/s**	
	Scheme	2-Step	Pipeline	**2-Step**	**3-Step**
	Resolution	1.25ps	0.63ps	**7.2ps**	**1.8ps**
	Bits	9bit	11bit	**7bit**	**9bit**
	DNL_{MAX}	0.8LSB	0.5LSB	**0.9LSB**	**1.9LSB**
	INL_{MAX}	3LSB	9LSB	**3.7LSB**	**10LSB**
	Power	3mW	10.5mW	**2mW**	**2.2mW**
	Area [mm^2]	0.6	0.32	**0.053**	**0.068**

*Input range for 5% max. gain error **Gain error w/o calib. (8x TA @ Fig. 4)

Fig. 5.19. TDC performance comparison.

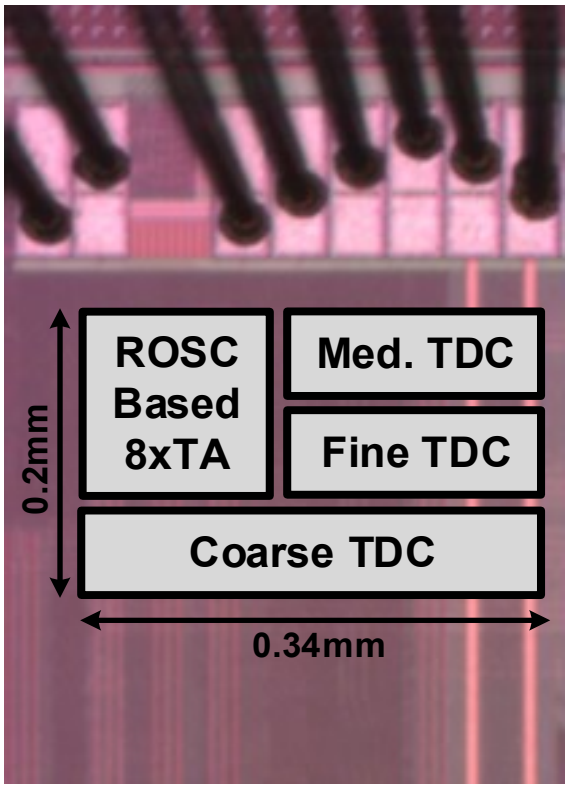


Fig. 5.20. Die micrograph.

5.6 Conclusion

A 9bit, 1.8ps resolution 3-step TDC employing a switched ring oscillator based time amplifier is demonstrated in 65nm CMOS process. The proposed time amplifier gain with a 100ps input range varies from -4% to 5% while the gains of the existing techniques vary from -71% to 15% or -83% to 3%. A total of 32-times higher resolution than a single buffer delay has been achieved by means of a 8x switched ring oscillator based TA and a 2bit Vernier delay line based fine TDC. Without calibration, the 3-step TDC achieves a maximum DNL of 0.9/1.9LSB and the maximum INL of 3.7/10LSB for 2-step/3-step modes.

Chapter 6. Digital PLL with Noise-Shaping Time-to-Digital Converter Featuring Adaptive Pulse-Train Time Amplification

This chapter proposes a digital PLL with a noise-shaping gated ring oscillator TDC featuring an adaptive pulse-train time amplification. The proposed TDC achieves both high resolution and wide input range by adaptively controlling the time amplifier gain with respect to the length of time input.

6.1 Introduction

Recently, digital PLL (DPLL) is widely being utilized in a variety of applications. State-of-the-art DPLL publications [39-43, 50] show their improved noise performance achievements comparable to that of the analog PLL. DPLL has several advantages including the significantly reduced loop filter (LF) area consumption and the easily reconfigurable and scalable digital circuitry over its analog counterpart. In addition, it also has other advantages including the supply noise insensitivity and the tolerance to the PVT variations.

Fig. 6.1 shows the basic DPLL block diagram. Time-to-digital converter (TDC) is one of the critical building blocks in DPLL which determines the PLL noise performance due to its quantization error. After a decision whether the reference (or feedback) clock phase is earlier or later than the other via a phase detector (PD), the time difference between the rising edges of the detected early (Start) and late (Stop) signals is converted to the digital output code (D_{OUT}). The noise due to the quantization

error (i.e. difference between the ideal and quantized D_{OUT} in Fig. 6.2) while converting the time difference to the digital output degrades the DPLL in-band phase noise performance.

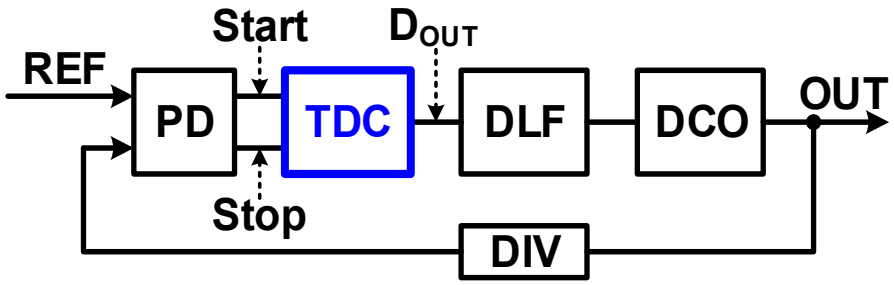


Fig. 6.1. Digital PLL block diagram.

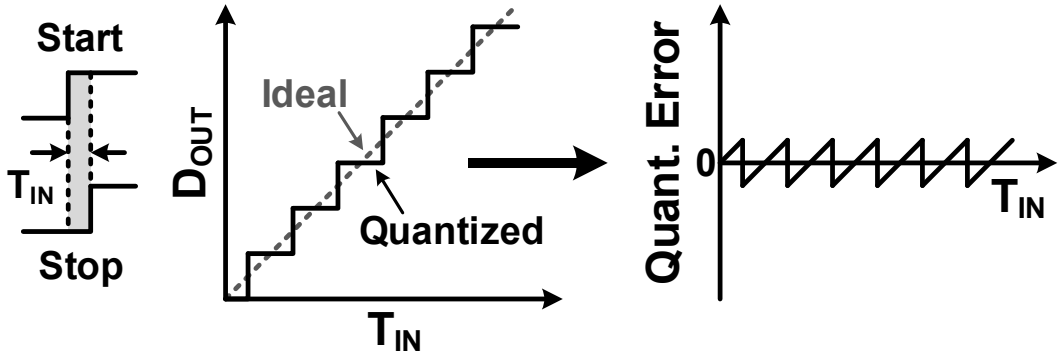
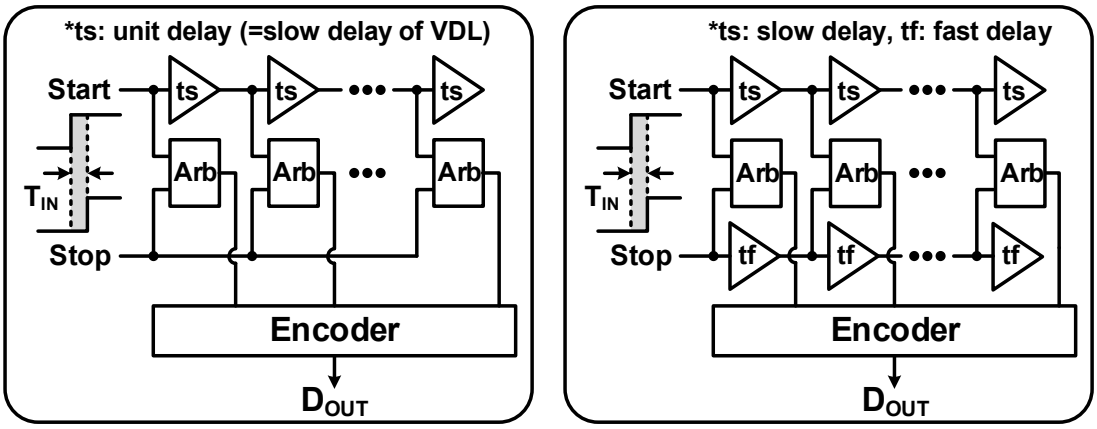


Fig. 6.2. TDC quantization error.

Fig. 6.3 describes the two most frequently used TDC types based on delay line (Fig. 6.3, upper left) and Vernier delay line (Fig. 6.3, upper right). While having a relatively low time resolution which is equal to a unit delay, the delay line (DL) based TDC has a wide input range (i.e. input range = conversion time). On the other hand, Vernier delay line (VDL) based TDC could achieve the higher time resolution (than the DL based TDC) by utilizing the delay difference between a slow and a fast delay while having the

narrow input range (i.e. much smaller than the conversion time). The performance comparison between the DL and VDL based TDC is shown in Fig. 6.3, lower. Under a fixed TDC conversion time of 10.24ns, DL based TDC has the low time resolution of 40ps which is equal to a unit delay (ts) of the TDC while having the wide input range (10.24ns). On the other hand, VDL based TDC operates with the higher time resolutions (e.g. 10ps and 2ps) while having the narrower input ranges (e.g. 2.56ns and 0.512ns) when we have different fast delays (e.g. tf = 30ps and 38ps).



	DL-TDC	*ts=40ps	VDL-TDC	*tf=30ps	*tf=38ps
Resolution	ts	40ps	ts−tf	10ps	2ps
Input Range	$2^N \cdot ts$	10.24ns	$2^N \cdot (ts-tf)$	2.56ns	0.512ns
Conv. Time	$2^N \cdot ts$	10.24ns	$2^N \cdot ts$	10.24ns	10.24ns

*e.g. 8bit TDC w/ a fixed slow delay (ts=40ps) & 2 fast delays (tf=30ps/38ps)

Fig. 6.3. Block diagrams of TDCs based on (a) delay line and (b) Vernier delay line and the comparison of resolution, input range and conversion time.

Time amplifier (TA) based TDC techniques [44-49] have been recently gaining traction as a promising approach for achieving both wide input range and high resolution. Time residue generated by the preceding TDC stage is amplified by TA and utilized by

the subsequent TDC stage for achieving higher resolution than the conventional single stage TDC. There have been several prior publications on the time amplifier based TDC designs including two-step [44, 45], pipeline [46, 47], cyclic [48] and sub-exponent [49] TDC. Fig. 6.4 shows the two representative types of TDC based on TA. In the two-step TDC, TA is used for amplifying the time residue generated at the coarse TDC after the conversion of coarse MSB digital output. The amplified time residue is used for producing the fine LSB digital output at the following fine TDC. While the two-step TDC is only employing a single TA for the coarse-fine TDC operation, the pipeline TDC has multiple of them to form multiple pipeline stages. Each pipeline stage is consist of a pair of TDC and DTC and a TA. Note that both two-step and pipeline TDC are analogous to their analog-to-digital converter (ADC) counterparts. Likewise, we can also build other TDC architectures (e.g. cyclic TDC, delta-sigma TDC and etc.) by referring to the existing ADC architectures.

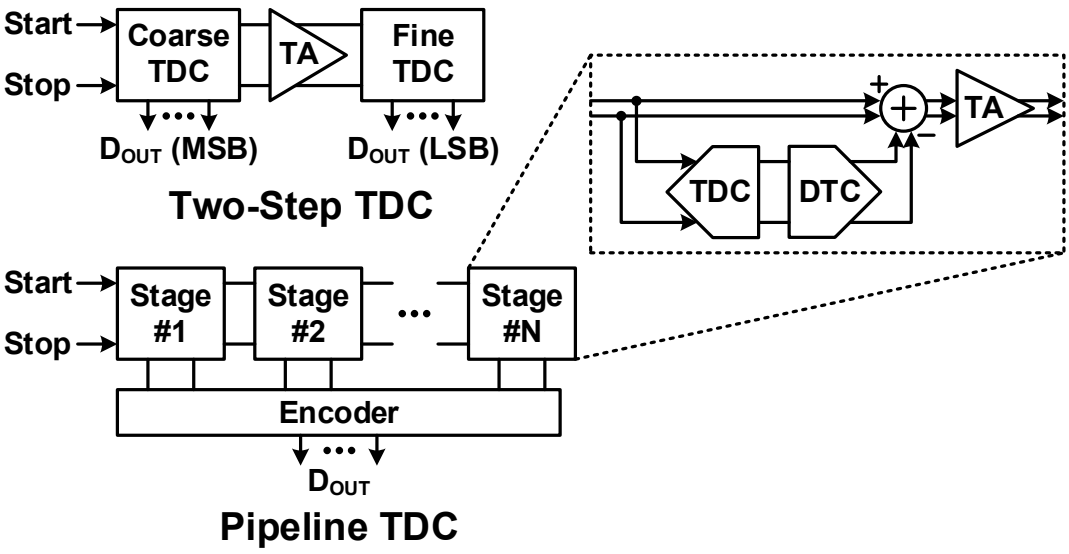


Fig. 6.4. Time amplifier based TDCs: (a) two-step TDC (b) pipeline TDC.

Noise-shaping is another circuit technique which can improve the time resolution of TDCs. By shaping the TDC quantization noise to the frequency much higher than the DPLL bandwidth, the in-band phase noise due to the TDC is reduced (i.e. shaped to the high frequency) while the increased high frequency noise is low-pass filtered by digital loop filter. Recent publications show different noise-shaping TDC circuit techniques including the gated ring oscillator (GRO) based TDC [52] and the analog intensive 1bit noise-shaping delta-sigma TDC [53] shown in Fig. 6.5. Both achieved the first-order noise-shaping effect which results in the lowered in-band phase noise.

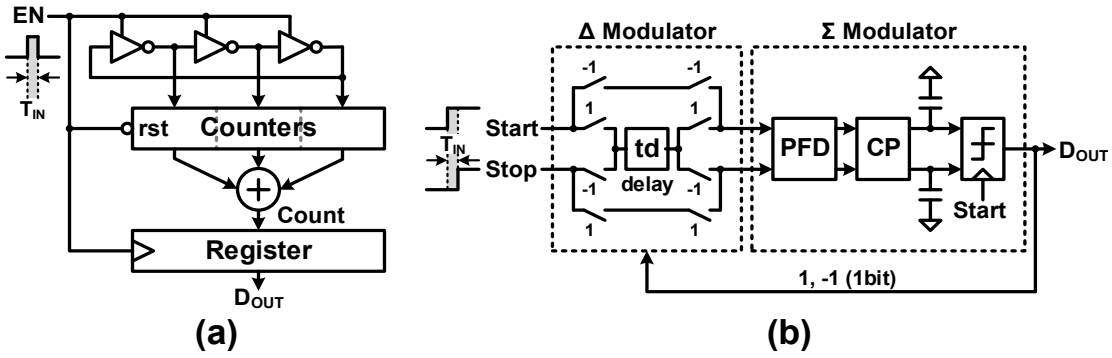


Fig. 6.5. Prior noise-shaping TDCs (a) gated ring oscillator (GRO) TDC [52] and (b) 1bit noise-shaping delta-sigma TDC [53].

In this work, we propose a noise-shaping TDC based on adaptive pulse-train time amplifier for achieving the improved DPLL in-band phase noise. The proposed TDC achieves both high resolution and wide input range by adaptively controlling the pulse-train TA gain with respect to the length of time input. Both first-order noise-shaping and time amplification functions are implemented in a single TDC by utilizing the same operating mechanism (i.e. noise-shaping between pulses) of the existing pulse-train TA [45] and gated ring oscillator based TDC [52].

The remainder of this chapter is organized as follows. Section 6.2 reviews the noise-shaping based TDC circuit techniques (i.e. pulse train TA and GRO based TDC) for improving the TDC time resolution. Section 6.3 describes the concept of the proposed noise-shaping TDC featuring the adaptive pulse-train TA. The implementation details of the 65nm test chip is shown in Section 6.4. The test chip measurement results are given in Section 6.5 and Section 6.6 concludes the chapter.

6.2 Noise-Shaping Based TDC Techniques

6.2.1 Pulse-Train Time Amplification

Fig. 6.6 shows existing TA circuits based on the SR-latch metastability and the discharging time control method. The metastability based TA [41, 44] utilizes the intrinsic dependence between the input time difference and the SR-latch resolving time. While having a stable gain within a narrow input range which is acceptable for certain applications, it suffers from the inherently unpredictable gain and the limited input range. The TA gain of the discharging time control method [46-49, 51] quickly degrades as the time input increases and therefore a background calibration is required to have a constant gain throughout the entire input range.

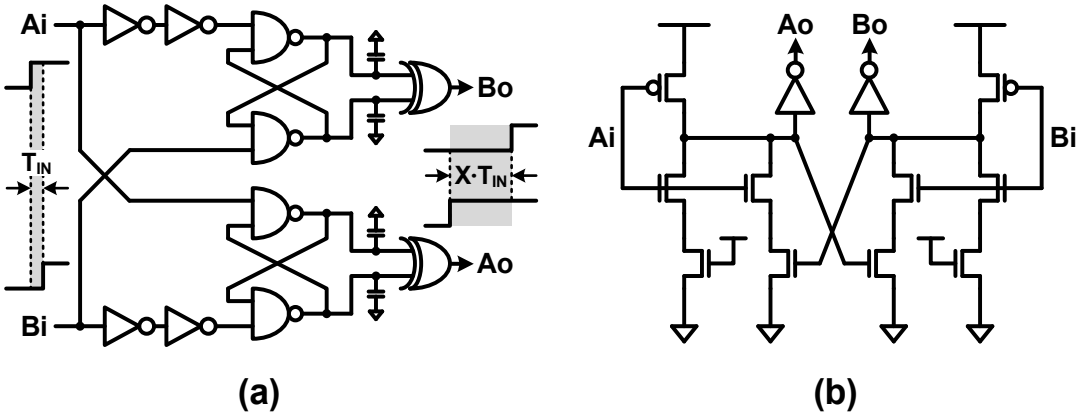


Fig. 6.6. Existing TA circuits: (a) SR-latch metastability based [41, 44] and (b) Discharging time control method [46-49, 51].

Recently, pulse-train TA [45] (Fig. 6.7) has been proposed to deal with the shortcomings of the prior techniques. In addition to the precise gain control and the wide input range, the simple and scalable highly digital circuitry makes it an attractive form of time amplifier. Note that the pulse-train TA concept is based on the noise-shaping effect between each pulses (not the samples) with gated delay line based TDC technique. Since the quantization error from the previous pulse (under the same sampling cycle) is saved and utilized for the quantization of the next pulse, the sampled digital output for the multiple time pulses is equivalent to the TDC output with a single amplified (i.e. as much as the number of pulses) time pulse as shown in Fig. 6.8.

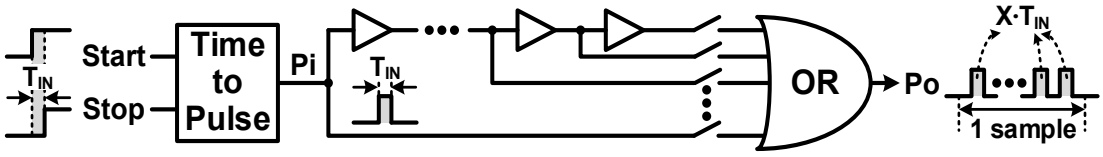


Fig. 6.7. Pulse train TA circuit.

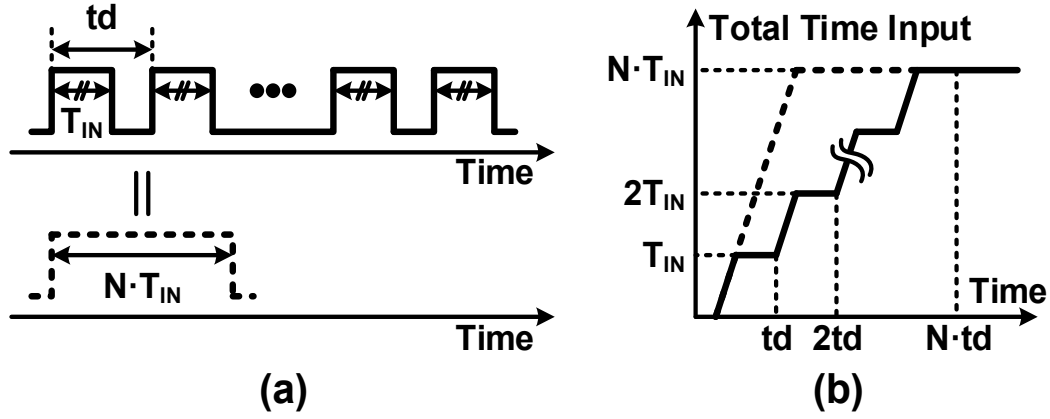


Fig. 6.8. Concept of the pulse train TA [8]: (a) Time amplified signals with pulse train (upper) and a single amplified time (b) Equivalent total time input.

6.2.2 Gated Ring-Oscillator Based TDC

A gated ring-oscillator (GRO) based TDC [52] (Fig. 6.9) improves the DPLL in-band phase noise due to its unique first-order noise shaping property by gating on and off the ring-oscillator. As shown in Fig. 6.9, right, the phase information from the multi-phase GRO output clocks are saved after each sampling cycle, and the saved phase information is used at the next sampling cycle. This in effect is a first-order noise shaping property and therefore, the low frequency quantization noise is shaped to the high frequency (i.e. much higher than the PLL bandwidth). Since the shaped high-frequency quantization noise is filtered out by a low-pass loop filter, it does not degrade the PLL phase noise performance.

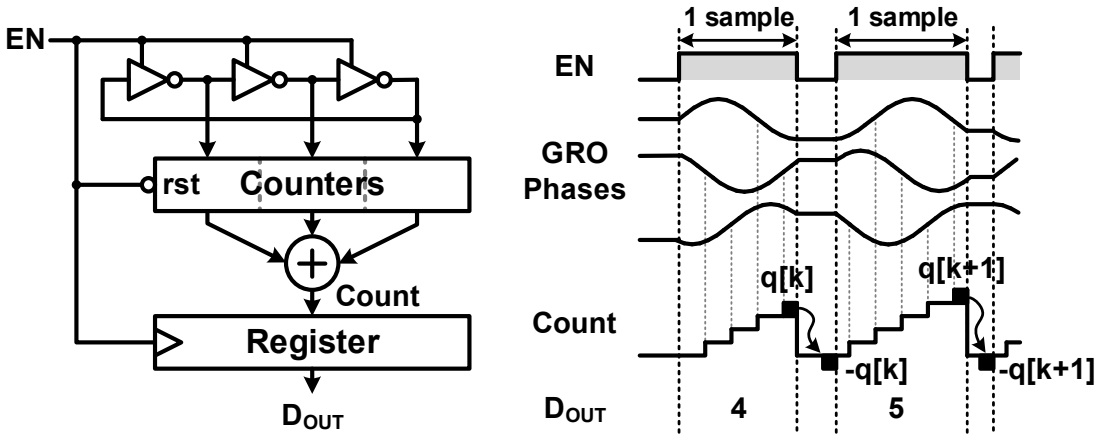


Fig. 6.9. Gated ring-oscillator (GRO) based TDC circuit and its timing diagram.

6.3 Noise Shaping TDC Based-On Adaptive Time Amplifier

6.3.1 Noise-Shaping TDC with a Cascaded Pulse-Train TA and GRO- TDC

Fig. 6.10 shows the block diagram of the proposed TDC circuit with a cascaded pulse-train time amplifier and a noise-shaping gated-ring oscillator (GRO) based TDC for achieving high time resolution. Time input (i.e. the time difference between the rising edges of the two input signals, Start and Stop) is first converted to multiple time pulses with the same pulse width (i.e. a pulse width = time input). The generated time pulses enable the GRO and the total time input which is equivalent to the sum of multiple time pulses are then counted with the GRO multi-phase clock outputs. The resulting counter output is sampled per each TDC sampling cycle. Since the GRO is not reset after each sampling cycle, the quantization error is saved and utilized at the next sampling cycle. Therefore, the additional first-order noise shaping effect improves the time resolution of the previous pulse-train TA even further.

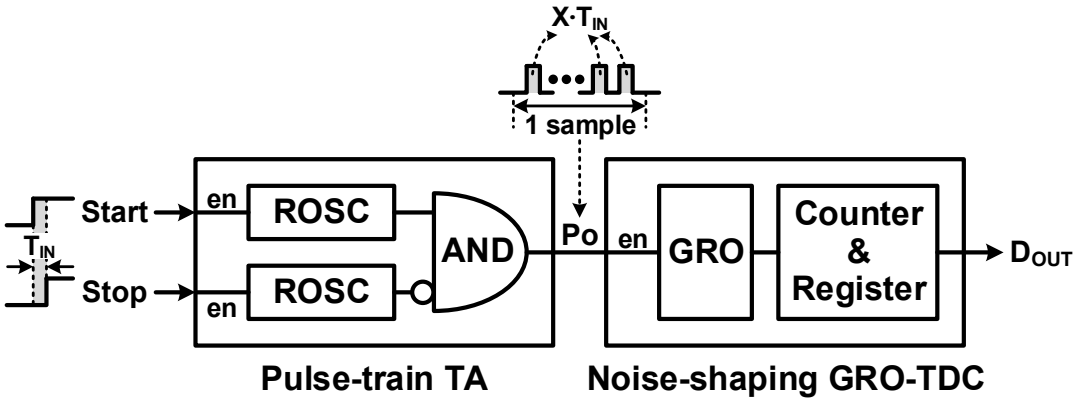


Fig. 6.10. Block diagram of the proposed noise-shaping TDC with a cascaded pulse-train time amplifier and the gated-ring oscillator (GRO) based TDC.

The operating concept of the proposed TDC integrating both noise-shaping and time amplifier properties in it is described with a timing diagram in Fig. 6.11. The noise shaping between each time pulses in a TDC sampling cycle is equivalent to the pulse train TA and therefore a 4x time amplification is achieved in the example shown in Fig. 6.8. After the fourth time pulse in a sample, the GRO counter is reset while the GRO is gated-off to keep the phase information so that the quantized error from the previous cycle (i.e. q[k] in Fig. 6.11) is saved as a GRO phase information and utilized at the next sampling cycle by gating-on the GRO again.

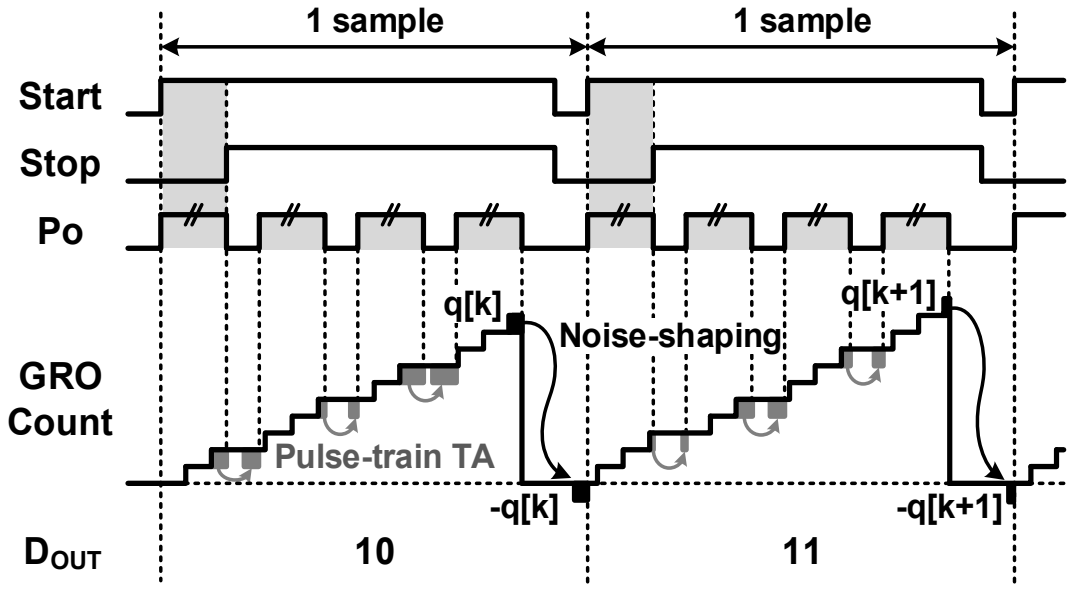


Fig. 6.11. Concept of the TDC featuring both time amplification and noise-shaping. For illustration purpose, an example of 4x pulse-train TA is shown here.

6.3.2 Adaptive Time Amplification

Using the proposed circuit, we could achieve the high TDC resolution due to the combined effect of noise-shaping and time amplification. However, the input range is supposed to be reduced as a trade-off since the pulse-train TA in the proposed TDC amplifies the time input instead of the time residue. We also observed that the conventional (single-stage) TDC including the GRO-based TDC does not utilize the full sampling cycle especially when the time input is extremely small (Fig. 6.12, left). Note that the time input of the TDC for DPLL is kept minimum once the PLL is locked (i.e. steady-state).

In this work, we propose an adaptive time amplification scheme which makes TDC fully utilize its sampling cycle by adaptive controlling the TA gain with respect to the length of time input (Fig. 6.12, right). For instance, we can achieve the highest TA gain of 16x for the smallest time input range while the gain is decreasing from 16x to 1x as the time input increases (Fig. 6.13). Since the TDC input of DPLL is always being extremely small (i.e. tens of picoseconds) while it is in a steady-state (i.e. locked), the reduced gain when the time input is large does not degrade the overall PLL in-band phase noise performance.

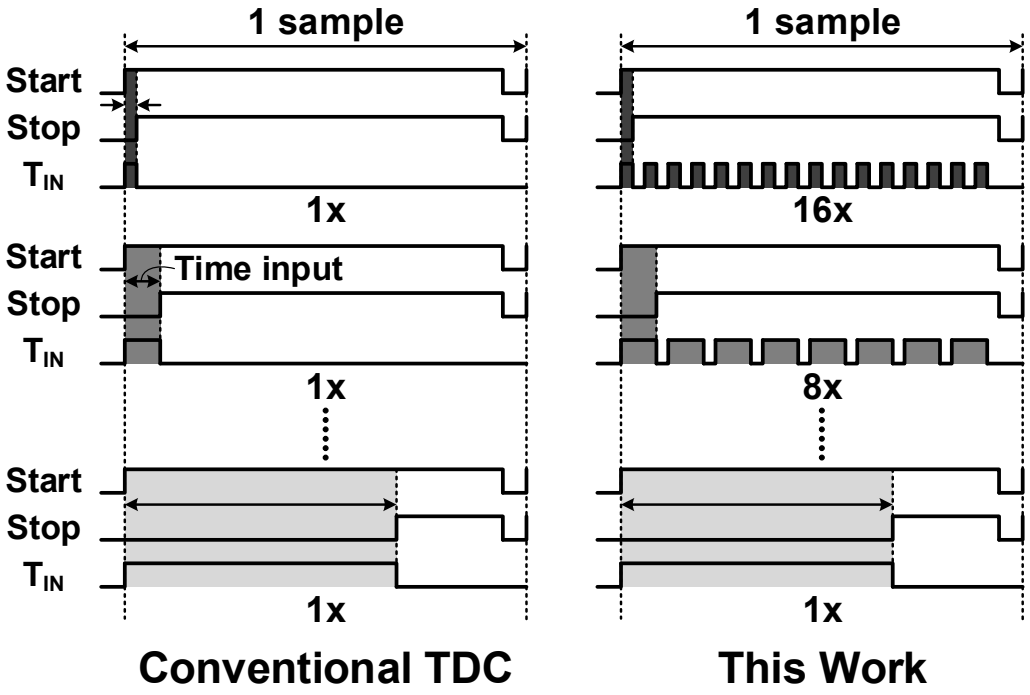


Fig. 6.12. Proposed adaptive time amplification scheme based on pulse train TA [45].

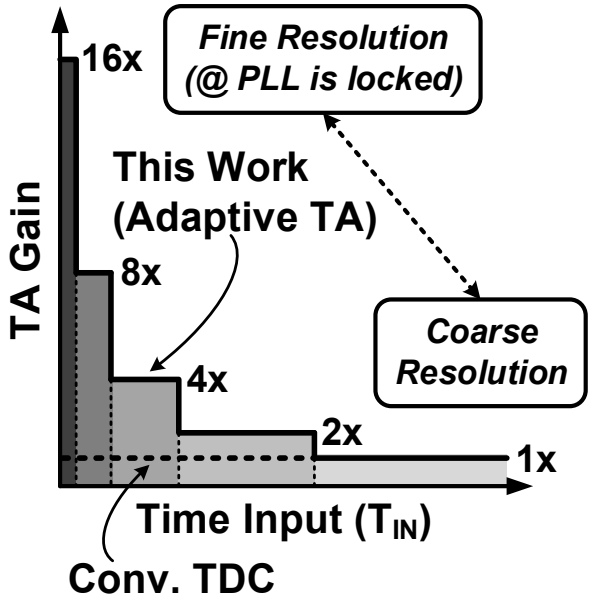


Fig. 6.13. Adaptive TA gain with respect to time input.

6.4 Circuit Implementation in 65nm CMOS

6.4.1 Noise-Shaping TDC Circuit

Fig. 6.14 shows a prototype noise-shaping TDC circuit implemented in a 65nm test chip. An adaptive pulse-train TA circuit is followed by a GRO-based TDC. A pair of 5-stage ring oscillator (ROSC) is used for generating multiple time pulses by turning on each ROSCs sequentially with the incoming rising edges of Ai (early) and Bi (late) signals. A self-timed ROSC enable signal (EN_{RO}) is generated and used for turning-off the ROSCs for minimizing the power consumption while they are not required. A time comparator is designed using the arbiter (i.e. phase comparator) circuits in [48] and the outputs are used for selecting the TA gain. Depending on the selected TA gain, the ROSC clock outputs are divided with synchronous dividers and the outputs are connected to an AND gate to generate the time pulses. The GRO-based TDC is consist of a gated 5-stage ROSC circuit, a ripple counter and D flip/flops (DFFs) for sampling GRO counter outputs per each TDC sample. Like the prior GRO-based TDC [52], the GRO is gated on and off based on the input enable signal (Po in Fig. 6.14). The counter output is sampled to the output by the DFFs which is driven by a triggering signal (read in Fig. 6.14). Right after the sampling, the counter is reset for the next sampling cycle. Both the read and reset signals are generated by a control signal generator in the adaptive time amplifier circuit.

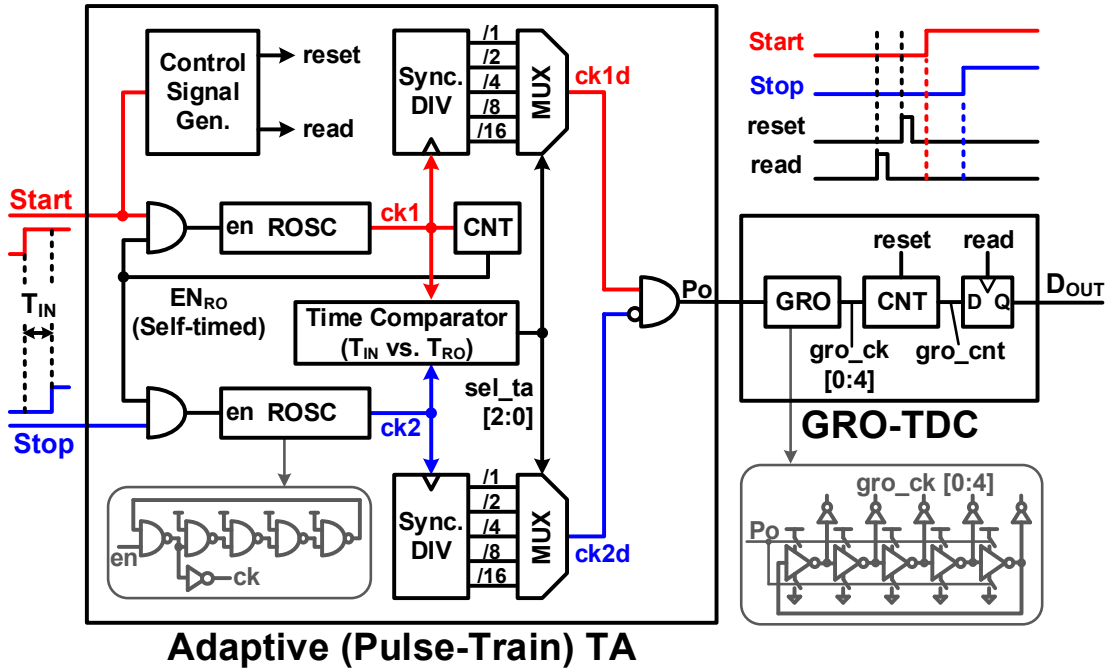


Fig. 6.14. Proposed TDC circuit with an adaptive pulse-train TA and a GRO-based TDC.

Fig. 6.15 shows the TDC timing diagram within a TDC sampling cycle. As an example, 4x TA is shown here. Once the length of time input is compared with the time references, the TA gain is selected (e.g. 16x @ $T_{IN} < 0.5T_{RO}$, 8x @ $0.5T_{RO} < T_{IN} < T_{RO}$, 4x @ $T_{RO} < T_{IN} < 2T_{RO}$, 2x @ $2T_{RO} < T_{IN} < 4T_{RO}$, 1x @ $4T_{RO} < T_{IN}$). As a result, the ROSC clocks are divided (e.g. divide-by-4 @ 4x TA in Fig. 6.15) and used for generating the pulses for GRO enable signaling. Then, a sequence of four pulses (i.e. pulse train) is generated by the AND operation of ck1d (i.e. a divided clock of ck1) and ck2d (i.e. a divided clock of ck2) and the GRO is gated on and off based on this sequence. Then, GRO output clock phases (gro_ck) are used for counting the multiple time pulses (Po) and the resulting count output is sampled by the read signal and the counter is reset right after that.

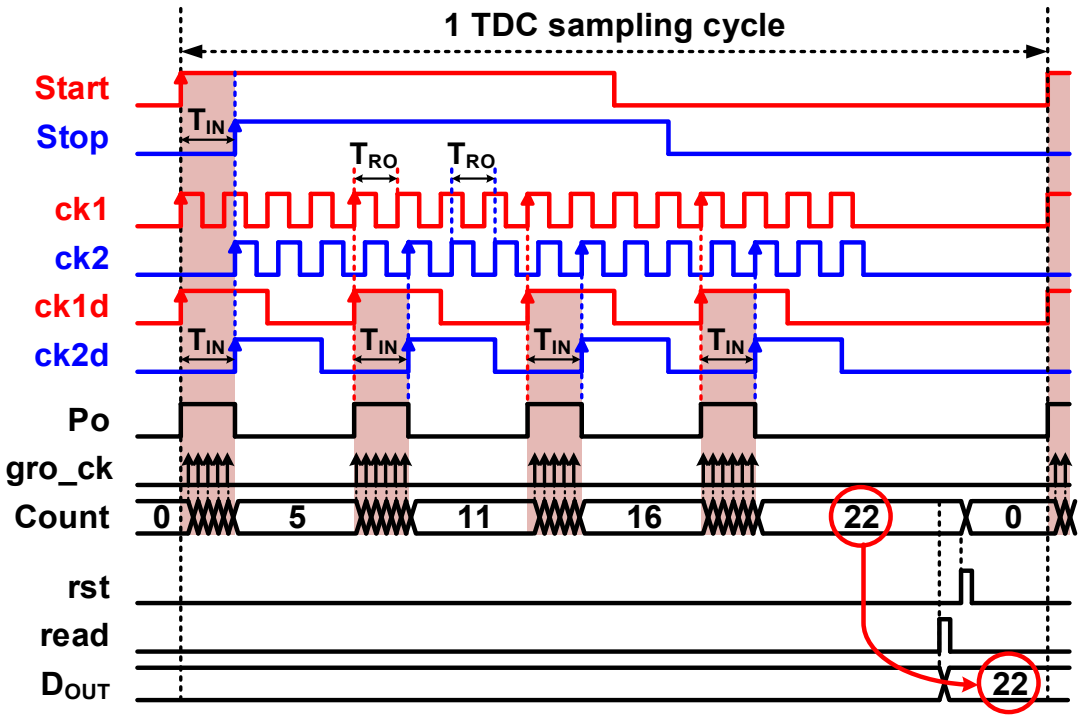


Fig. 6.15. Timing diagram of the proposed TDC (e.g. 4x TA).

6.4.2 All-Digital PLL Circuit with the Proposed TDC.

A 0.3-to-1.8GHz all-digital PLL circuit is implemented as shown in Fig. 6.16 to verify the function and evaluate the phase noise performance improvement with the proposed TDC circuit. A simple binary phase detector (PD) is used for de-multiplexing the reference and feedback clocks to TDC and multiplexing the TDC digital outputs to digital loop-filter (DLF) input. A replica TDC circuit (i.e. offset TDC in Fig. 6.16) is used for measuring the time offset which is required for maintaining the minimum pulse width to ensure the correct pulse-train TA operation. The offset TDC could also be used for improving (minimize) the PLL output spur level by dynamically measuring and cancelling-out the time-varying (i.e. voltage and temperature dependent) TDC offset while PLL is operating. The multiplexed TDC outputs are multiplied with different gain (i.e. to balance the output range with different TA gain) and it is controlled by the time comparator outputs (in Fig. 6.14). A ring-oscillator based digitally-controlled oscillator (DCO) is controlled by a fine 10bit digital code output from a digital loop-filter (DLF) and a 4bit coarse control code to select the coarse DCO frequency band with a lowered DCO gain (i.e. $K_{DCO} \approx 150MHz/2^{10}$-steps). The simulated all-digital PLL working behavior in 65nm is shown in Fig. 6.17. It is clearly shown in the simulation results that the TA gain starts with the lowest gain (i.e. 1x) to the largest gain (i.e. 16x) when the PLL is locked in a steady-state.

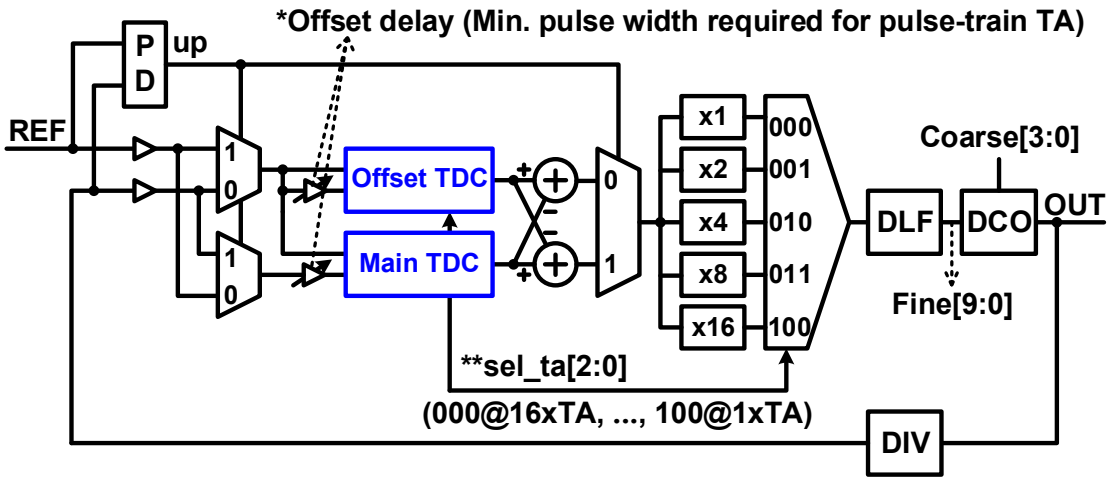


Fig. 6.16. ADPLL circuit with the proposed TDC. An offset TDC is added to digitize and subtract the required offset delay from the main TDC.

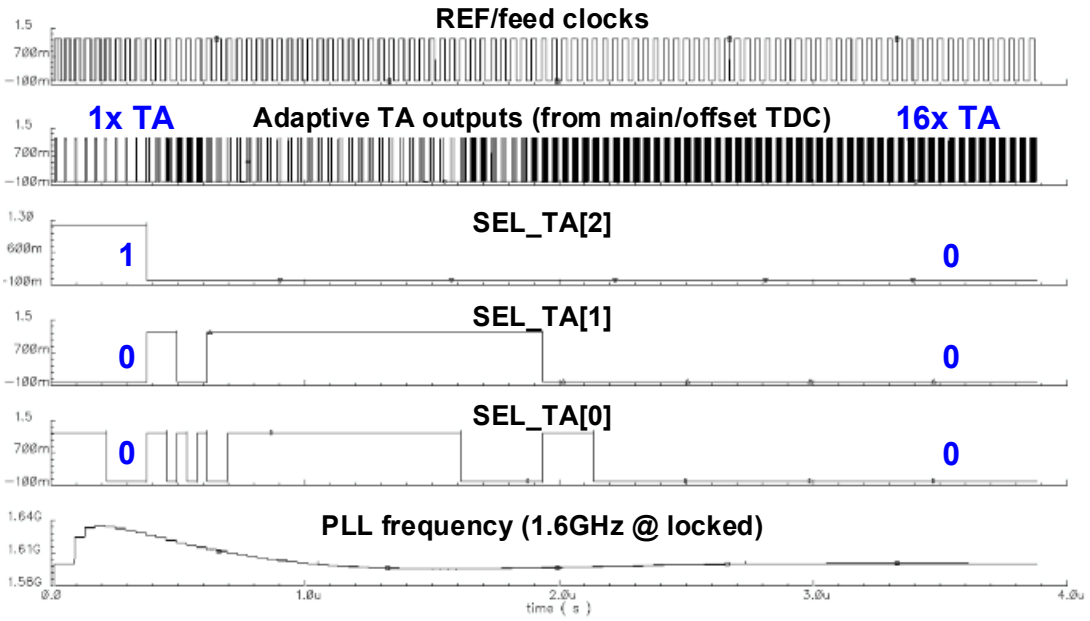


Fig. 6.17. Simulated PLL locking behavior with adaptive TA operation.

6.5 Test Chip Measurement Results

Fig. 6.18 shows the measured PLL phase noise at 0.4GHz from the PLL test chip implemented in a 65nm CMOS process. The in-band phase noise measured at 100kHz frequency offset is -91dBc/Hz with the noise-shaping TA circuit with 1x TA gain. The phase noise becomes -98dBc/Hz (i.e. 7dB lower than that of 1x TA gain) with the improved TA gain of 4x. The integrated phase jitter (from 10kHz to 1MHz) is 8.4ps with 4x TA gain while it is 12.8ps with 1x gain. Fig. 6.19 shows measured spur levels at 0.8GHz with and without the use of offset TDC. The spur level is lowered as much as 10dB and 20dB with offset TDC compared to that of the TDC without offset TDC, but with fixed external offset codes. The die micrograph and performance summary are shown in Fig. 6.20 and Fig. 6.21.

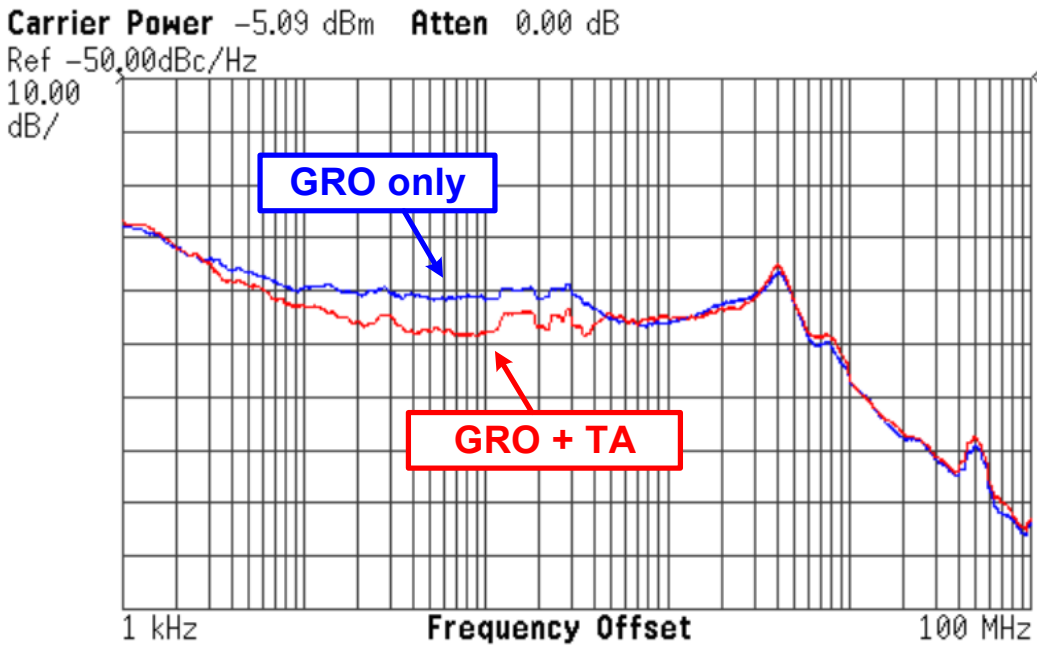


Fig. 6.18. Measured phase noise at 0.4GHz.

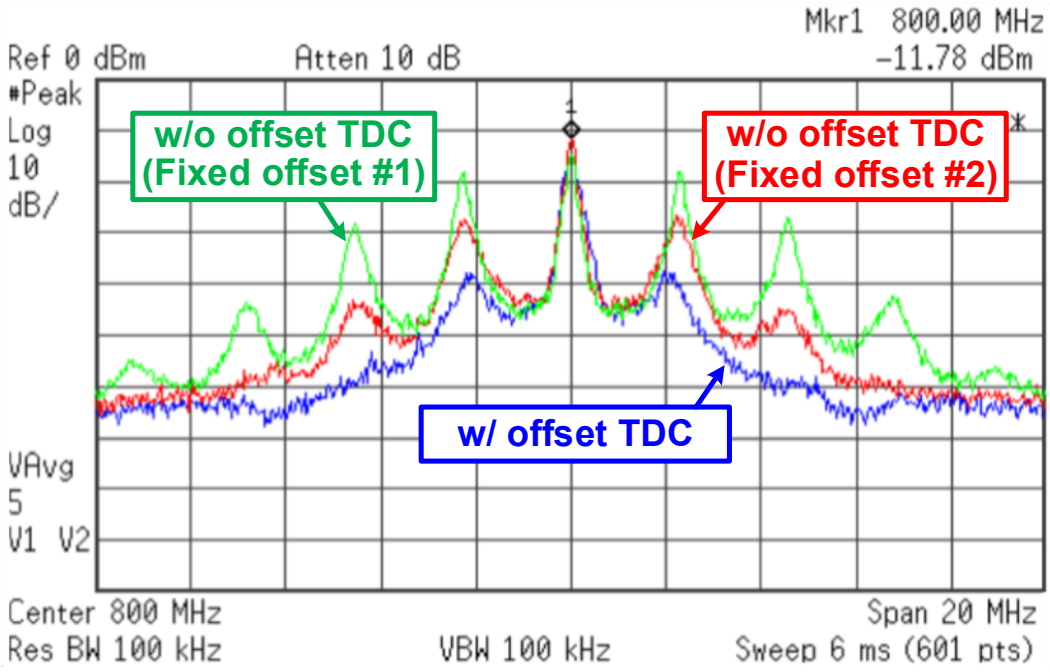


Fig. 6.19. Measured ADPLL output spectra with and without offset TDC.

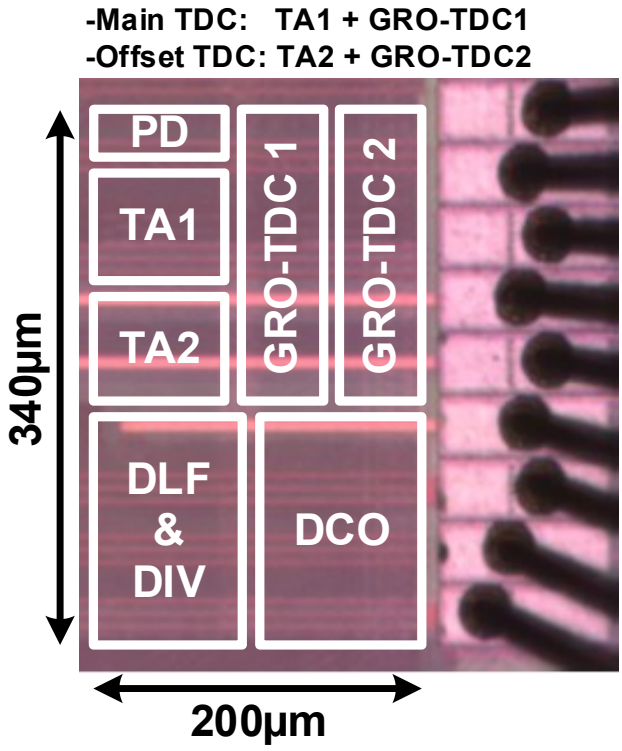


Fig. 6.20. Chip micrograph.

	GRO	GRO+TA
Tech/Supply	65nm / 1.2V	
PLL Type	Integer-N	
DCO Type	5-stage Ring-OSC	
DCO Control	10bit capacitor bank	
Frequency	0.3 - 1.8GHz	
PN@0.4GHz [dBc/Hz]	-91@100k -96@1M	-98@100k -96@1M
*Integrated Phase Jitter	12.8ps (0.51%)	8.4ps (0.34%)
PLL Power	2.5mW @ 0.8GHz	
PLL Area	0.068mm^2	

*Integrated PN from 10kHz to 1MHz offset
(Percentage from 1 clock period)

Fig. 6.21. Performance summary.

6.6 Conclusion

A 0.3-to-1.8GHz all-digital PLL employing a noise-shaping TDC based-on adaptive pulse-train time amplifier is demonstrated in 65nm CMOS process. The time resolution is improved with both noise-shaping and the time amplification integrated in a single TDC. To achieve both high resolution and the wide input range with the proposed noise-shaping time amplifier, an adaptive time amplification scheme is also proposed. The maximum TA gain of 16x is achieved when the time input is minimum while the lowest gain of 1x ensures the wide input range. The measured in-band phase noise at 100kHz and the integrated phase jitter (from 10kHz to 1MHz offset) at 0.4GHz PLL output frequency is -98dBc/Hz and 8.4ps with 4x TA gain with noise-shaping.

Chapter 7. Spurious-Free Bang-Bang Digital PLL with Fractional Sub-Sampling Phase Detector

This chapter presents a spurious-free integer-N bang-bang PLL (BBPLL) based-on the proposed fractional sub-sampling (FSS) phase detector. The spurious noise due to the limit cycle regime of bang-bang digital PLL is suppressed and the in-band phase noise is reduced compared to that of the conventional integer-N bang-bang PLL.

7.1 Introduction

Time-to-digital converters (TDCs) and digitally-controlled oscillators (DCOs) have been considered as crucial building blocks in the digital PLL (DPLL) designs since they determine the overall phase noise performance. While it is relatively simpler to achieve a high frequency resolution by having a low DCO gain or inserting a simple digital delta-sigma modulator in-between the digital loop-filter (DLF) and DCO, the design of high time resolution TDC requires sophisticated circuit techniques such as Vernier delay line [54-56], time amplifier [44, 46, 49] and noise-shaping [52, 53]. While consuming a significant amount of power consumption, they also suffer from PVT variations. Recently, bang-bang phase detector (BBPD) based PLLs (BBPLLs) [57-61] have been widely utilized due to its simple circuitry and the phase noise performance comparable to that of the DPLL with a high resolution (i.e. few picoseconds time resolution) TDC [57]. Fig. 7.1 shows the basic block diagram and the TDC/BBPD transfer characteristics (i.e. output digital code vs. input phase difference) of DPLL with and without the use of a multi-bit time resolution TDC.

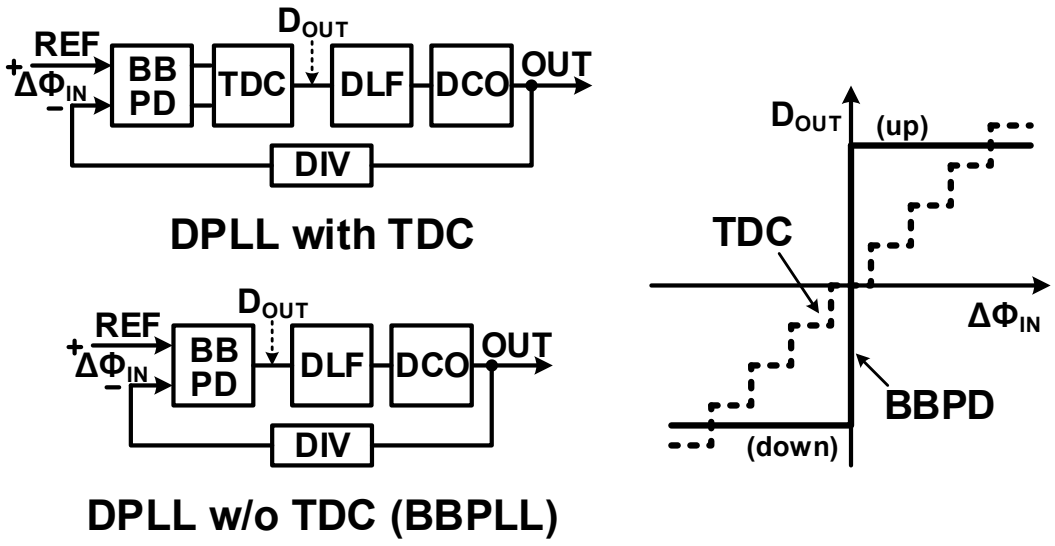


Fig. 7.1. Digital PLL block diagrams with/without TDC and the transfer characteristics of TDC and BBPD.

Recently, sub-sampling PLL has been introduced as a feedback divider-less PLL for achieving the low PLL in-band phase noise by replacing the conventional phase detector and feedback divider with its sub-sampling phase detector. By doing so, the in-band phase noise due to the PLL divider noise is completely removed while the noise due to the phase noise (PD) and charge pump (CP) is reduced as much as the square of the reduced dividing ratio. Based on the conventional PLL noise transfer functions in [62], the PD/CP noise is amplified by N^2 where N is the PLL (feedback) divider ratio and added to the in-band phase noise with the divider noise. An analog sub-sampling PLL [62-64] based on the sub-sampling phase detector (SSPD) circuit was first proposed as shown in Fig. 7.2, left. A capacitor in series with a sampling switch was used as an analog SSPD. The SSPD directly samples (i.e. sub-sampling) the high frequency voltage-controlled oscillator (VCO) clock using a reference clock with 1/N clock frequency compared to the target PLL output frequency when it is locked. While the

phase is locked with the sub-sampling operation, a separated frequency locked loop (FLL) is typically required for the frequency locking. A digital implementation of the sub-sampling PLL has been also published [65], recently. The digital sub-sampling PLL with its BBPD based sub-sampling phase detector is shown in Fig. 7.2, right. A typical D flip/flop (DFF) was used for sub-sampling the high frequency digitally-controlled oscillator (DCO) clock output using a low frequency reference clock. Note that the digital sub-sampling PLL based on BBPD sub-sampler has almost the same circuitry with the digital BBPLL except for the separated FLL circuit.

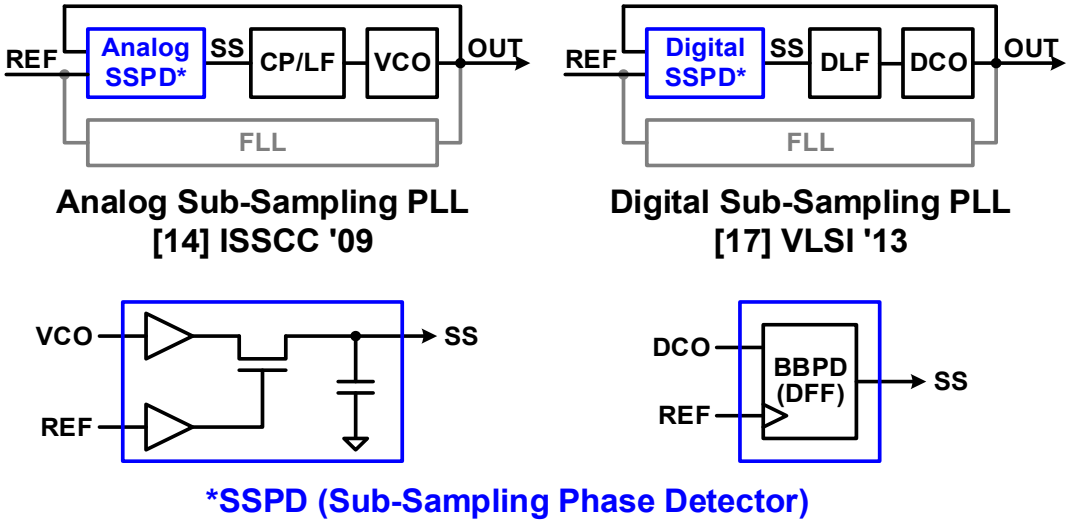


Fig. 7.2. Existing sub-sampling PLLs [62-65] with analog/digital sub-sampling phase detectors.

While the existing DPLLs based on BBPD (i.e. conventional or sub-sampling BBPD) are capable of generating output clocks with competitive in-band phase noise performances which is comparable to that of the other DPLLs with high resolution TDCs, they are suffering from the other clock noise source. The additional noise comes from the large magnitude of spurious tones which are generated due to the limit cycle regime of DPLL. The magnitude of spurs due to the limit cycle of BBPLL is especially large compared to that of the other DPLLs due to the intrinsic nonlinear transfer characteristics of BBPD. In this work, a fractional sub-sampling concept is proposed to suppress the problematic large spur noise of the existing BBPLLs. In addition to the beneficial noise-shaping clock dividing function which suppresses the spurs, the (fractional) sub-sampling operation itself improves the BBPLL in-band phase noise performance as much as the reduced division ratio. To verify the function and evaluate the PLL performances (i.e. magnitudes of phase noise and spurious tones), all-digital BBPLLs are demonstrated in 65nm CMOS.

The remainder of this chapter is organized as follows. Section 7.2 reviews the existing DPLL circuit techniques for suppressing the spurious tones. Section 7.3 describes the concept of the proposed noise-shaping fractional sub-sampling and its use in the implemented integer-N BBPLL. The details of the fabricated 65nm test chip is shown in Section 7.4. The test chip measurement results are given in Section 7.5 and Section 7.6 concludes the chapter.

7.2 Digital PLLs with Spur Suppression Techniques

Existing DPLLs (Fig. 7.3) including the noise-shaping TDC based integer-N PLLs and fractional-N DPLLs with a dual modulus feedback divider and a delta-sigma modulator do not suffer from the DPLL spur noise due to the noise-shaping functions which are integrated for the other purposes. The noise-shaping TDCs [52, 53] have been designed for improving the in-band phase noise by shaping the TDC quantization noise to the frequency much higher than the PLL bandwidth. While doing this, the low frequency spur and TDC quantization noise are shaped to the high frequency and low-pass filtered out via DLF. The delta-sigma modulator integrated in the fractional-N DPLLs is intended for shaping the low-frequency spurious noise due to the periodic dual-modulus dividing operation for generating fractional-N frequency. At the same time, the spurious tones due to the limit cycle is also shaped to the high frequency while the fractional-N PLL is operating.

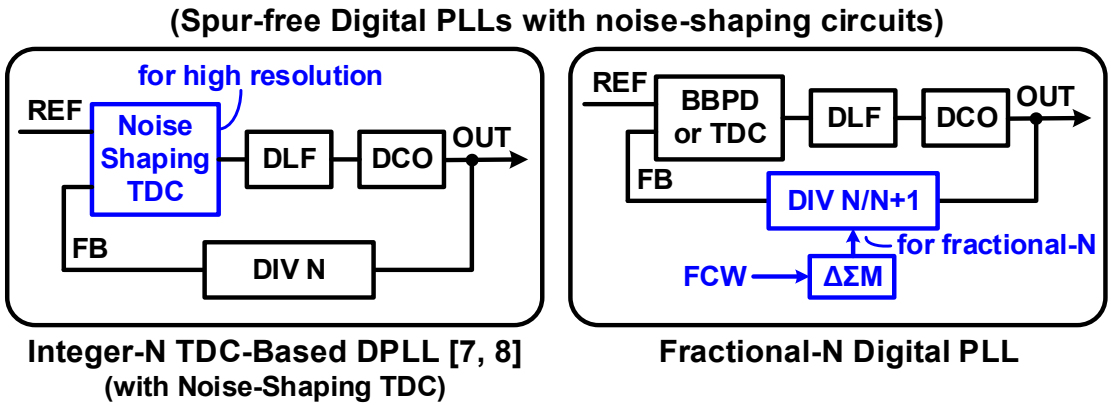


Fig. 7.3. Spur-free digital PLL circuits with no explicit spur reduction techniques. Integer-N digital PLL with BBPD or TDC (w/o noise-shaping) requires explicit spur reduction techniques.

While the specific types of DPLLs (i.e. integer-N DPLL based on noise-shaping TDC and fractional-N DPLL) shown in Fig. 7.3 are free from spurs due to the noise-shaping circuits integrated for other purposes, the integer-N DPLLs based on BBPD (or TDC with no noise-shaping property) are suffering from the problematic spurious tones without the use of special circuitry for suppressing them. To mitigate the impact of the periodic limit cycle behavior on the spurs, prior BBPLL publications introduced circuit techniques which generate intentional dithering. As shown in Fig. 7.4, a stochastic TDC [66] or a reference clock delay dithering method [57] have been used for suppressing the spurious tones from the integer-N BBPLL. Fig. 7.4, bottom shows an example of the suppressed spurs by utilizing the technique in [66]. Note that the complexity of the existing spur-suppression techniques are rather complicated when it is compared with the conventional BBPD. It also increases the overall power and area consumption.

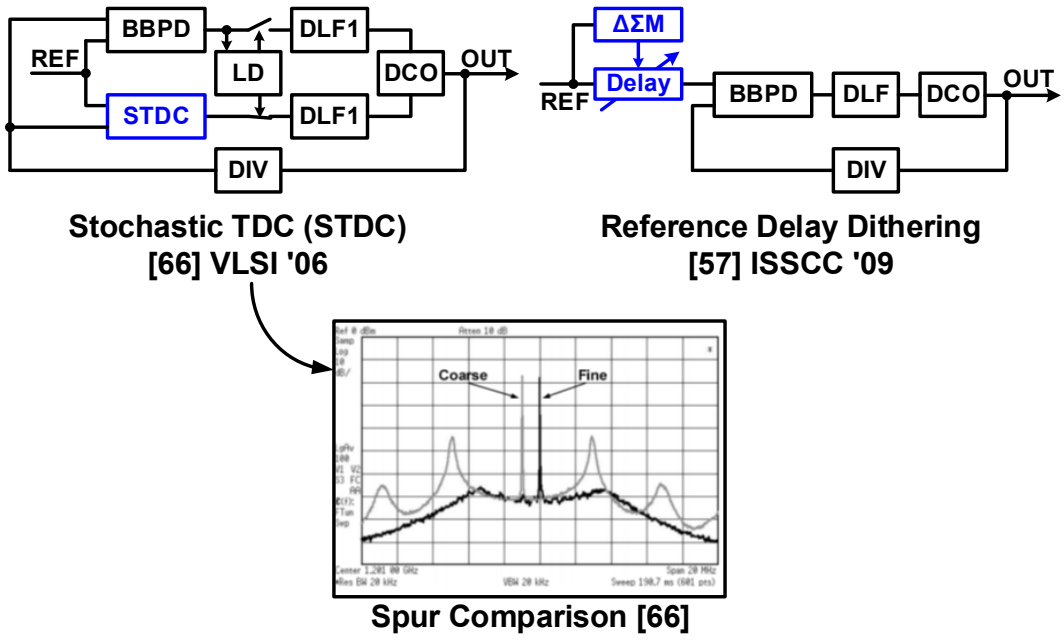


Fig. 7.4. Existing techniques [57, 66] to suppress spurious noise due to the limit cycle behavior from the integer-N BBPLL.

7.3 Fractional Sub-Sampling Digital PLL

To suppress the spurious noise due to the limit cycle behavior of integer-N bang-bang digital PLL, a simple DFF-based fractional sub-sampler (FSS) circuit is proposed in this work. The intrinsic first-order noise-shaping and sub-sampling properties of DFF when it is used as the FSS circuit is described in this section.

7.3.1 DFF-Based Noise-Shaping Fractional Sub-Sampler

The existing BBPDs utilize DFF as a phase detector which generates up or down signals (i.e. binary phase detector outputs) by comparing the phases from the reference (CK_{REF}) and feedback clock (CK_{FB}). Ideally, the phase difference between CK_{REF} and CK_{FB} becomes zero when BBPLL is locked. However, the BBPD output is periodically alternating between up and down due to the nonlinear (i.e. binary) nature of the BBPD transfer characteristic. This is the limit cycle behavior of the BBPLL and the magnitude of spurious tones and the corresponding output clock jitter due to the limit cycle is increased when the BBPLL loop gain and the latency increases [57].

In this work, the same DFF circuit is used as a pure sampler circuit (i.e. not a phase detector). The only assumption we have for the correct operation of the proposed DFF-based sampler circuit is that we have a certain frequency difference (e.g. CK_{REF} is 20% faster than CK_{FB} or $f_{REF}-f_{FB}=(1/5)\cdot f_{FB}$ in Fig. 7.5) between CK_{REF} and CK_{FB}. While we have a so-called fractional sub-sampling operation (i.e. $f_{FB} < f_{REF} < 2\cdot f_{FB,}$ a sub-sampling ($f_{REF}<2\cdot f_{FB}$) while the sampling clock (CK_{REF}) and the input clock (CK_{FB}) has a fractional frequency difference ($f_{FB} < f_{REF}$)), the DFF output frequency becomes a quantized frequency difference between the two DFF incoming clocks (i.e. beat

frequency quantization [76]). Under the given fractional frequency difference, the DFF-based FSS circuit generates a clock output which has a quantized frequency (or period) as shown in Fig. 7.5. Note that a period of DFF output clock (T_{FSS}) is equal to an integer (e.g. 6 in Fig. 7.5) times the reference clock period (T_{REF}). This is natural since the DFF output is sampled by CK_{REF}. While it is an integer multiplication of T_{REF}, it can be also expressed as a function of T_{FB}. As it is shown in Fig. 7.5, T_{FSS} is decomposed into a quantized number of T_{FSS} and the remainder is the first-order differentiated quantization error. The FSS circuit quantization error is generated whenever there is a phase misalignment between the incoming clocks. The quantization error generated at the previous CK_{FSS} cycle is used at the current quantization cycle while the quantization error from the current cycle is to be utilized at the next cycle.

Note that the proposed DFF-based FSS circuit is equivalent to a noise-shaping beat-frequency quantizer [76] which has already proven its first-order noise-shaping property by utilizing it as a quantizer for a VCO-based ADC when we add a simple asynchronous counter at the DFF output. The counter output number is corresponding to the quantized FSS output when it is counted with CK_{REF}.

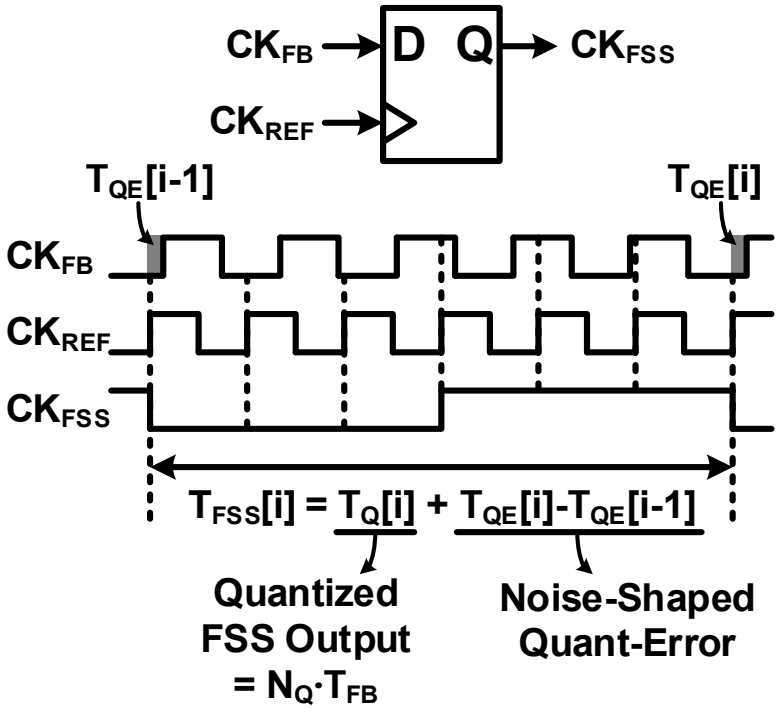


Fig. 7.5. Illustration on the noise-shaping behavior of DFF based sampler (i.e. fractional sub-sampler) when the input (CK_{FB}) and sampling clock (CK_{REF}) have a fractional frequency difference.

As illustrated in Fig. 7.5, the proposed FSS circuit has two key features. First of all, it is a sub-sampler and therefore it reduces (or eliminate) the PLL feedback division ratio. As the other sub-sampler does, it enhances (lowers) the in-band phase noise performance. In addition to the sub-sampling property, the noise-shaping behavior is another key advantage of the FSS circuit. Without the use of explicit delta-sigma circuitry, the feedback clock is dithered with the intrinsic first-order noise-shaping property. Fig. 7.6 summarizes the two key features of FSS circuit with an equivalent circuit. The DFF-based FSS circuit is equivalent to a divider (i.e. $/N_Q$ where N_Q is the quantized division ratio) combined with a first-order delta-sigma modulator updated at every cycles of CK_{FSS}.

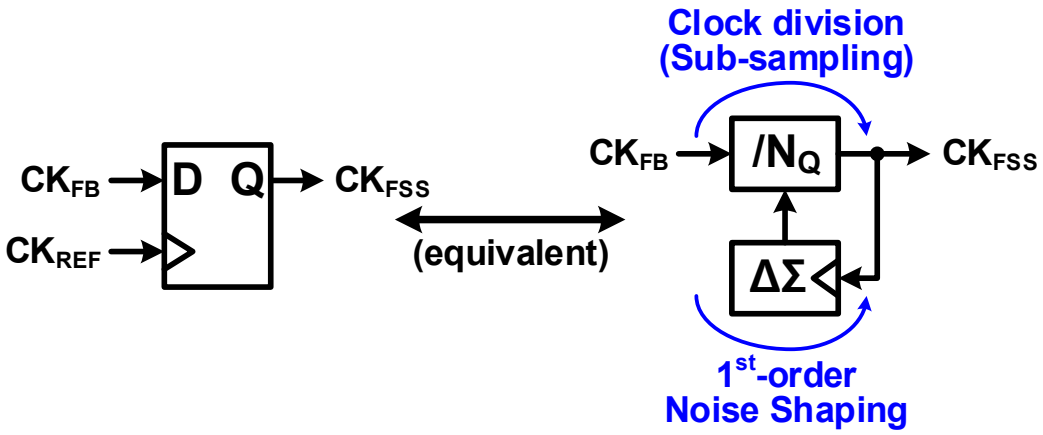


Fig. 7.6. DFF-based fractional sub-sampler is equivalent to a noise-shaped integer-N feedback clock divider. The simulated feedback division ratio can be found in Fig. 8, right.

Fig. 7.7 illustrates an example noise-shaping fractional sub-sampling operation when the frequency difference between the two incoming clocks of FSS is $f_{REF}/3.6$. Due to the fractional denominator in the frequency difference, the quantized division ratio (N_Q in Fig. 7.6) will be alternating between 3 and 4 while the occurrences of those 2 division ratio at the FSS output is controlled by the inherent first-order noise-shaping operation. As shown in Fig. 7.7, the quantization errors due to the phase misalignments between CK_{FB} and CK_{REF} in every CK_{FSS} cycle are used at the corresponding next cycles.

Fig. 7.8 shows a simulated frequency ratio between the CK_{REF} and CK_{FSS} (Fig. 7.8, left) and the CK_{FB} and CK_{FSS} (Fig. 7.8, right) when f_{REF} is fixed to 266.667MHz and f_{FB} is swept from 196MHz to 204MHz. While the frequency ratio is fixed to integer numbers (i.e. $f_{REF}/f_{FSS}=4$ and $f_{FB}/f_{FSS}=3$) when the f_{FB} is at 200MHz, the slight frequency changes from 200MHz (i.e. the phase drifts due to the slight frequency changes from 200MHz) causes the noise-shaped division ratios as shown in Fig. 7.8.

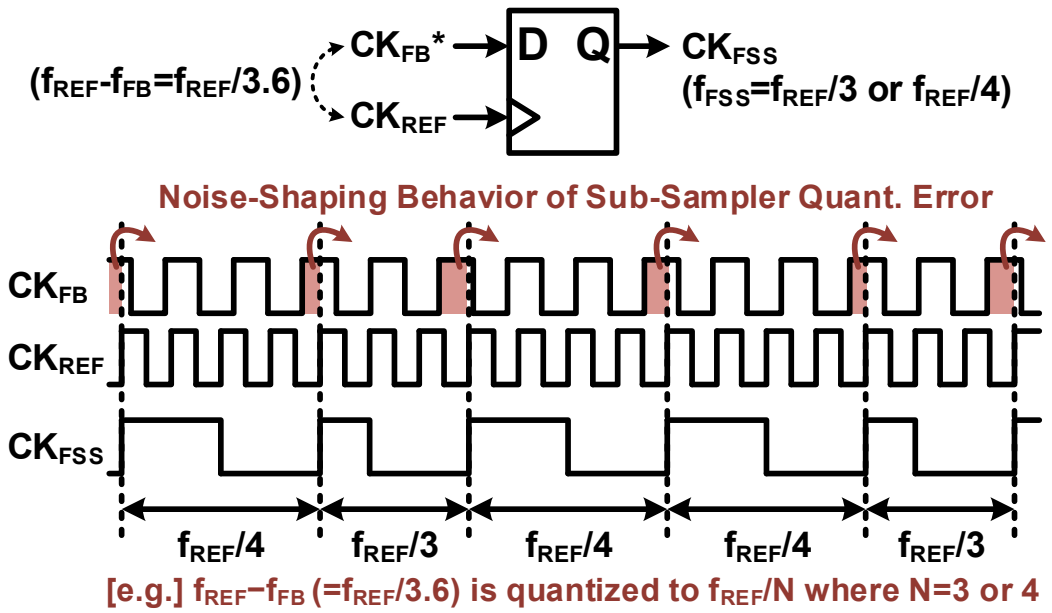


Fig. 7.7. Concept of the noise-shaping behavior in the fractional sub-sampler.

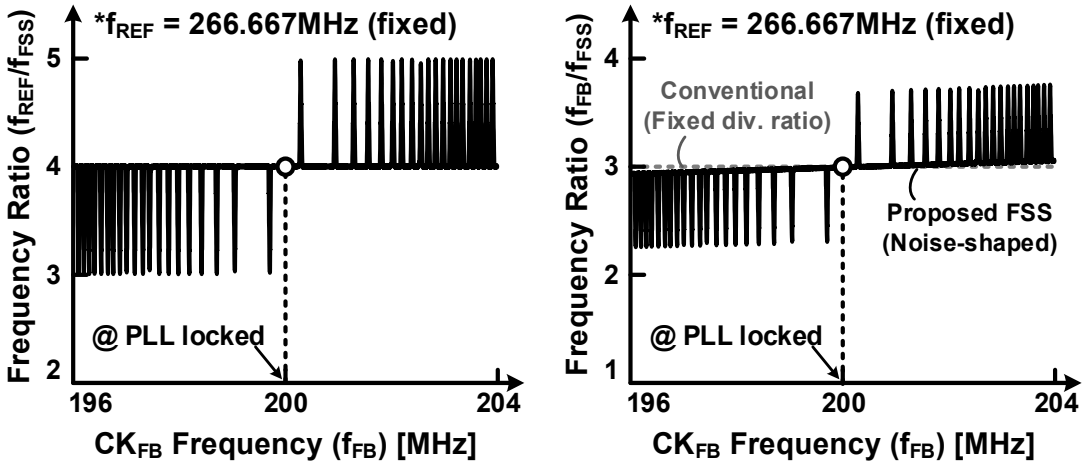


Fig. 7.8. Simulated frequency ratio between FSS output and inputs (i.e. CK_{REF} and CK_{FB}). We can clearly see the noise-shaping behavior of fractional sub-sampling operation.

7.3.2 Fractional Sub-Sampling Phase Detector

To utilize the beneficial noise-shaping and sub-sampling operation, a phase detector (i.e. FSS phase detector) including the proposed fractional sub-sampler circuit and a conventional bang-bang phase and frequency detector (i.e. BBPFD). An additional divider (i.e. PDIV) is also added in the detector circuit for generating a target FSS output clock and compare the phase of that clock with the FSS output. The PLL is locking while the feedback clock is dithered as much as the frequency difference between the transient and target feedback clock frequency as it is shown in Fig. 7.8.

Fig. 7.9 shows the proposed FSS phase detector circuit and its waveforms when the BBPLL is locked. Before the fine PLL locking operation, the coarse feedback clock frequency is set to make the frequency between the feedback and reference clock to be around 3:4 by using a frequency calibration procedure. The DFF in Fig. 7.9 is equivalent to a divider-by-3 of the conventional BBPLL while the noise-shaping behavior is added on top of that which will be suppressing the spurious noise while the BBPLL is locking.

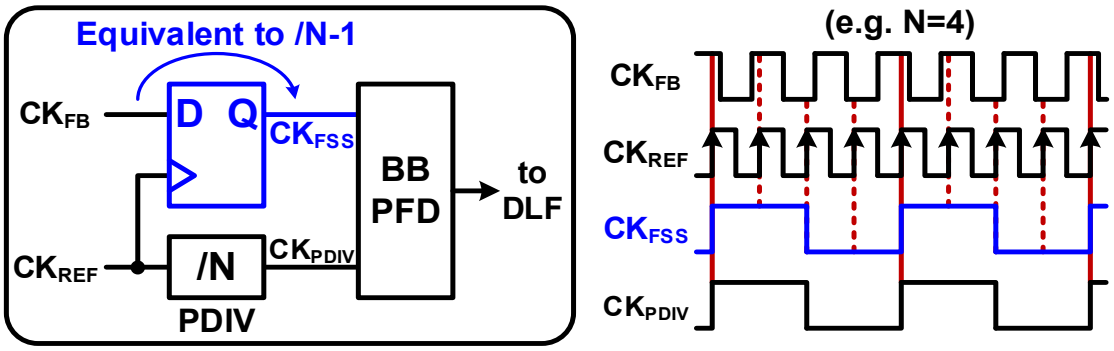


Fig. 7.9. Fractional-N sub-sampler (FSS) circuit and its waveforms when the BBPLL based on FSS phase detector is locked.

The BBPFD output of the proposed FSS phase detector is compared with that of the conventional phase detector when the feedback clock is faster (or slower) than the target frequency (when the PLL is locked) in Fig. 7.10. While having a fixed faster or slower divided feedback clock frequency (CK_{MDIV} or CK_{FSS}) than the divided reference clock frequency, the BBPFD in the proposed FSS phase detector circuit generates noise-shaped up and down signals which alternates depending on the magnitude of FB frequency variation. As a result, the spur noise of BBPLLs is suppressed. Fig. 7.11 shows the implemented BBPLL based on the proposed fractional sub-sampling phase detector circuit (Fig. 7.11, lower) and the conventional BBPLL (Fig. 7.11, upper) which has been used as a reference BBPLL design for performance comparison.

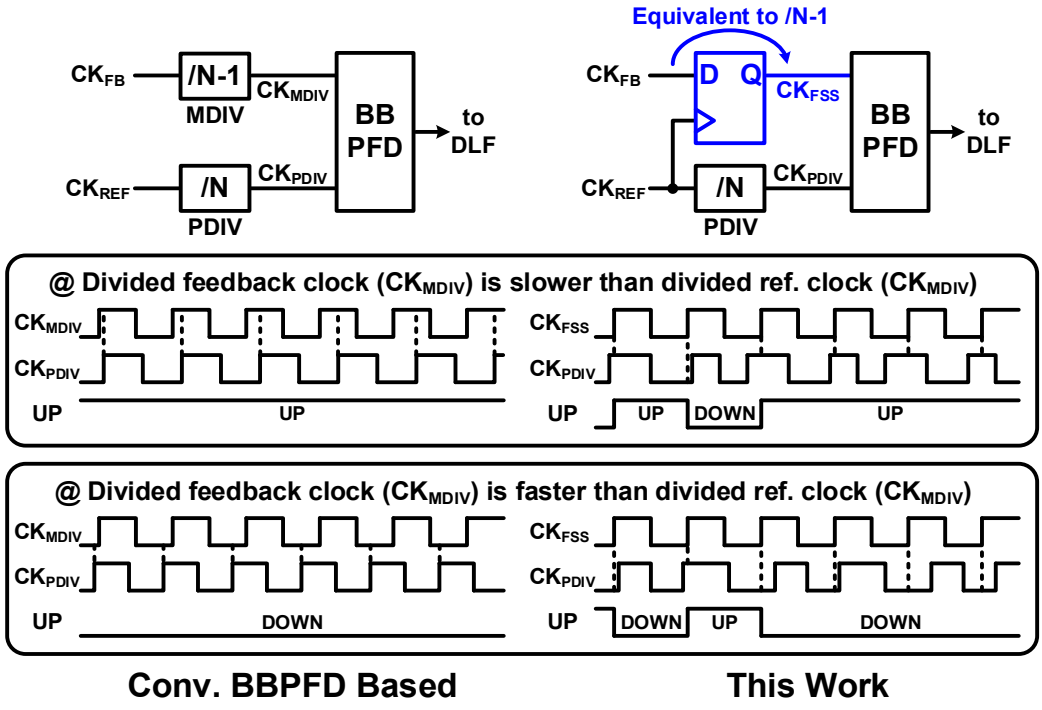


Fig. 7.10. BBPFD output comparison when the divided feedback clock is slower (or faster) than the divided reference clock.

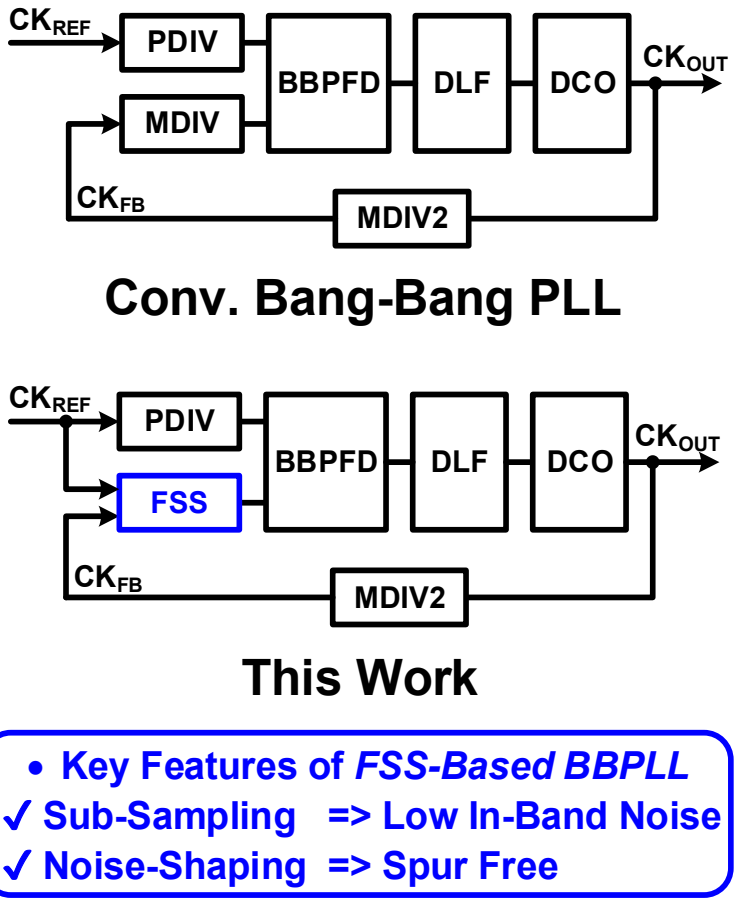


Fig. 7.11. BBPLL block diagrams with the proposed noise-shaping fractional sub-sampler (FSS). The FSS circuit (i.e. DFF) replaces MDIV in the conventional BBPLL circuit. MDIV2 is the reduced dividing ratio by the use of cascaded MDIV or FSS circuit.

7.4 Circuit Implementation in 65nm CMOS

Fig. 7.12 shows the block diagram of the proposed bang-bang digital PLL with the proposed fractional sub-sampling (FSS) phase detector circuit. The pre-dividing ratio of /4 is chosen while the equivalent division ratio of the FSS circuit is /3. When the PLL is locked, the output frequency of the FSS circuit (f_{FSS}) becomes 1/3 of f_{FB}. The PLL output frequency is programmable (i.e. 0.8GHz and 1.6GHz) with two feedback division ratios (i.e. N=12 and 24) when the reference clock frequency is set to 266.667MHz (= (4/3) x 200MHz). DLF is designed so that the loop gain can be programmed with both a coarse control with binary weights (e.g. K_{FC} = 1x, 2x, 4x…) and a fine control with an external integer input (e.g. K_{FF} = 1, 2, 3…). A ring-oscillator based DCO with 10bit distributed capacitor banks [61] has been used for achieving a fine DCO output frequency step while the coarse frequency can be controlled by enabling the number of inverter chains connected in parallel. Fig. 7.13 shows the circuit and layout of the DCO.

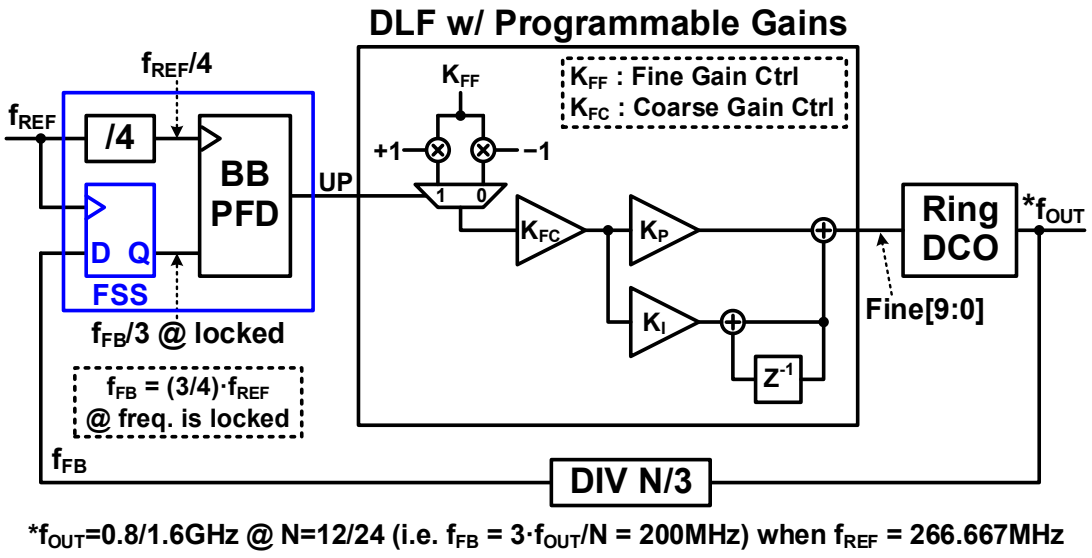


Fig. 7.12. Proposed bang-bang digital PLL block diagram.

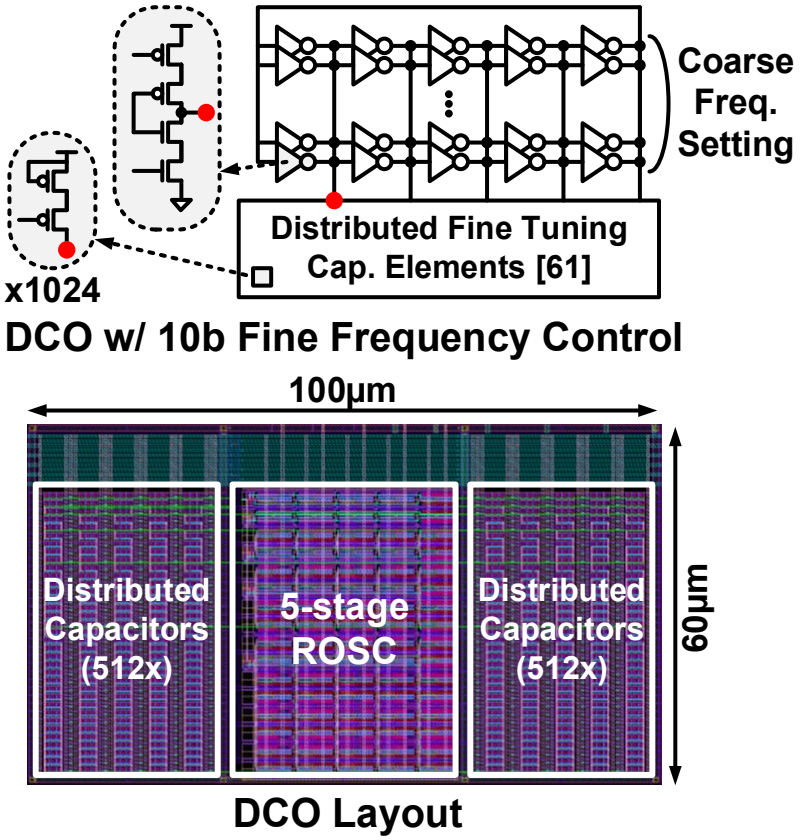


Fig. 7.13. Ring-oscillator based DCO schematic and layout.

The proposed PLL in Fig. 7.12 can be easily reconfigured to a conventional bang-bang digital PLL by replacing the sub-sampler (DFF) in the FSS circuit into a fixed divider (i.e. MDIV with the dividing ratio of /3) as shown in Fig. 7.14. While using the same PLL loop configurations, the function and the PLL noise performance have been compared.

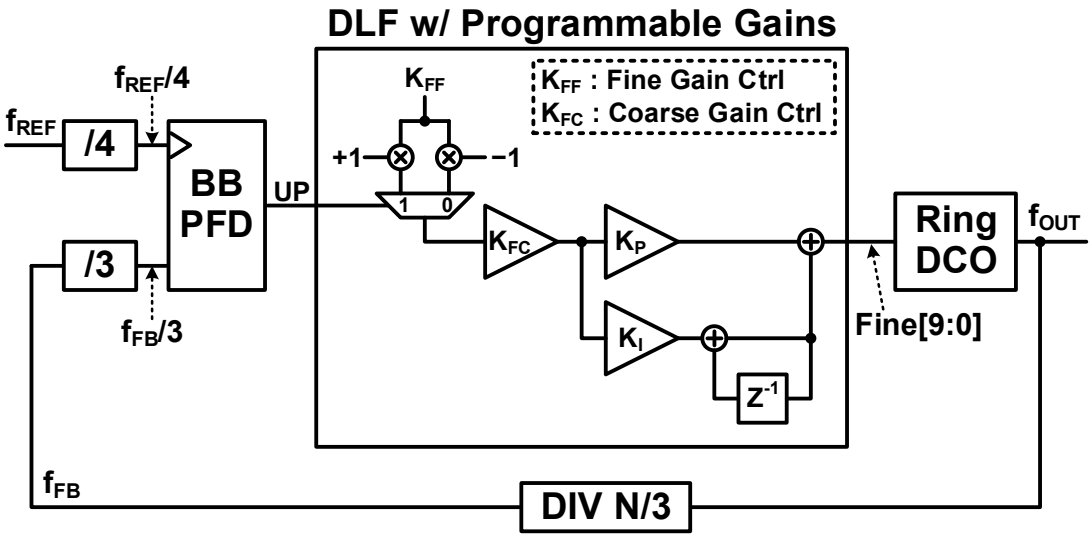


Fig. 7.14. A reference BBPFD based digital PLL with the same PLL loop configuration. All PLL parameters and circuits are shared only except for a D flip-flop in the proposed FSS circuit.

7.5 Test Chip Measurement Results

Fig. 7.15 shows the measured PLL output power spectra at 1.6GHz. The magnitude of spurious tones at the frequency offset of 6MHz from the carrier frequency is reduced by more than 20dB. The measured PLL phase noise results at 1.6GHz are shown in Fig. 7.16. The in-band noise floor of the proposed PLL is lowered by 9dB (i.e. -97dBc/Hz) compared to that of the conventional bang-bang PLL with -88dBc/Hz in-band noise floor. The integrated RMS phase jitter (from 20kHz to 2MHz) is measured to be 2.8ps while that of the conventional PLL is 7.9ps. The integrated phase jitter difference becomes much larger when we increase the maximum frequency offset for the noise integration. While the conventional BBPLL output clock at 1.6GHz is having 39.7ps phase jitter, the proposed BBPLL outputs the same frequency output clock with 8.5ps integrated phase jitter due to the smaller PLL in-band noise and the suppressed frequency spurs. The test-chip die micrograph is shown in Fig. 7.17 and the performance summaries are shown in Fig. 7.18 and Fig. 7.19.

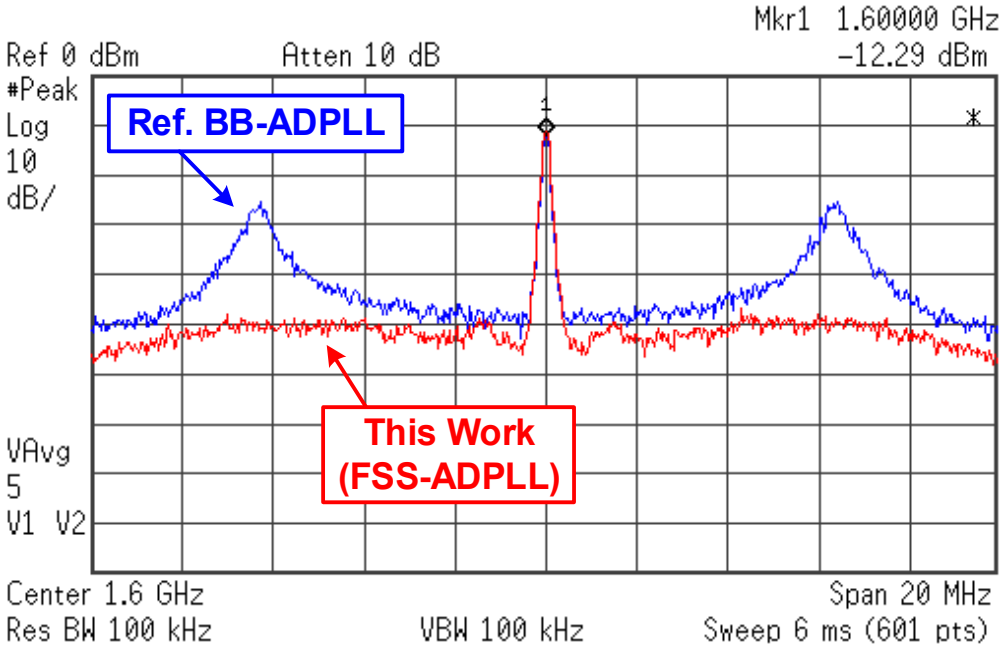


Fig. 7.15. Measured PLL output power spectra at 1.6GHz.

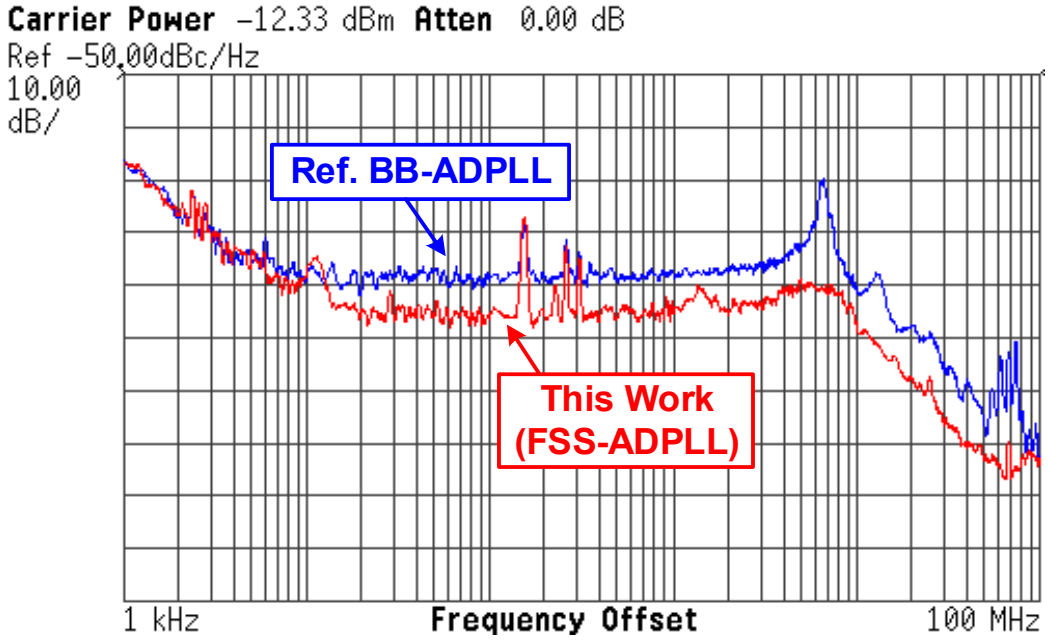


Fig. 7.16. Measured PLL output phase noise at 1.6GHz.

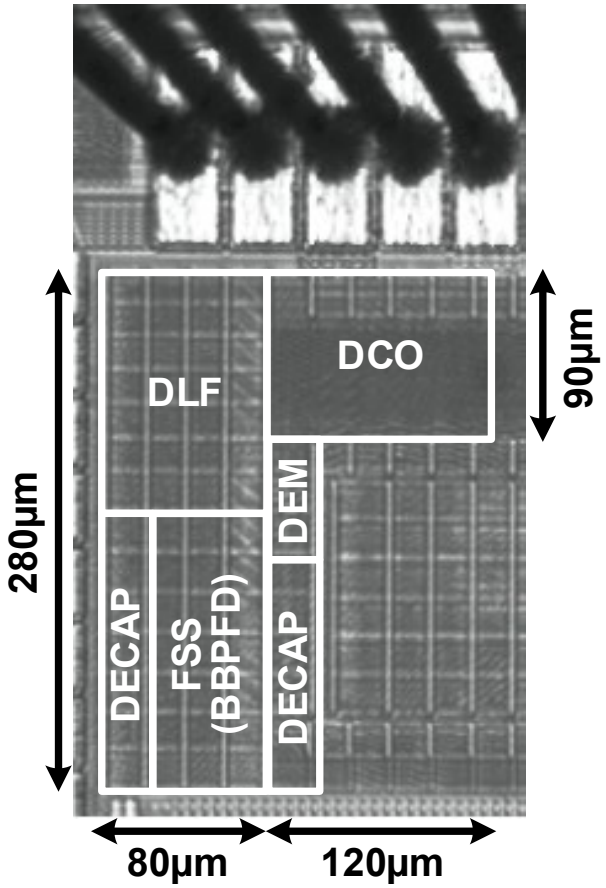


Fig. 7.17. Chip micrograph.

Process / Supply	65nm CMOS / 1.2V
PLL Type	Integer-N Bang-Bang Digital PLL
DCO Type	5-stage Ring Oscillator
PLL Frequency Setting	0.8GHz / 1.6GHz
Fine Frequency Control	10bit Capacitor Bank (i.e. 1024-steps)
In-Band Phase Noise	-101dBc/Hz@0.8GHz, -97dBc/Hz@1.6GHz
Integrated RMS Jitter	3.5ps@0.8GHz, 2.8ps@1.6GHz
Power	1.5mW@0.8GHz, 2.7mW@1.6GHz
Area	0.037mm^2

Fig. 7.18. Performance summary.

		Conv. BBPLL	This Work
In-Band Phase Noise (PN)	0.8GHz	-88dBc/Hz	-101dBc/Hz
	1.6GHz	-88dBc/Hz	-97dBc/Hz
PN Peaking (@6-7MHz offset)	0.8GHz	-55dBc/Hz	-95dBc/Hz
	1.6GHz	-70dBc/Hz	-90dBc/Hz
Integrated Jitter* (20k-2MHz)	0.8GHz	15.7ps	3.5ps
	1.6GHz	7.9ps	2.8ps
Integrated Jitter** (20k-20MHz)	0.8GHz	66.4ps	11.4ps
	1.6GHz	39.7ps	8.5ps

*Integrated jitter with 20k-2MHz offset (in-band noise)
**Integrated jitter with 20k-20MHz offset (in-band noise + spur)

Fig. 7.19. Performance comparison with conventional bang-bang digital PLL (BBPLL) built in the same test chip.

7.6 Conclusion

An integer-N bang-bang digital PLL featuring a fractional sub-sampling phase detector is demonstrated in 65nm CMOS process. The in-band noise floor has been lowered by reducing the feedback division ratio with the use of fractional sub-sampler instead of a conventional divider while the spurs due to the limit cycle of BBPLL is suppressed by the noise-shaping behavior of the same circuit. The measured results show the phase noise at 1.6GHz of -97dBc/Hz which is 9dB lower than the conventional BBPLL. The integrated phase jitter at 1.6GHz clock outputs of the proposed BBPLL from 20kHz to 2MHz frequency offset is 2.8ps while that of the conventional BBPLL is 7.9ps. When the same phase noise is integrated from 20kHz to 20MHz, the integrated jitter with the proposed BBPLL becomes 8.5ps while that of the conventional BBPLL is 39.7ps. The spur is suppressed and the phase noise peaking at 6-7MHz frequency offset is lowered by more than 20dB at 1.6GHz.

Chapter 8. Aging-Tolerant Digital PLL Featuring Dynamic Element Matched Ring-DCO with On-Chip Aging Monitor

This chapter proposes an aging-tolerant digital PLL employing a dynamic element matched ring-oscillator based DCO circuit. A compact on-chip reliability monitor is also integrated for measuring DCO frequency degradation due to the aging.

8.1 Introduction

As CMOS process scales, the negative impacts such as the circuit failures or the parametric shifts due to the device aging have become severe. While the aging impacts on digital logic or memory circuits with different stress mechanisms including hot carrier injection (HCI) and bias temperature instability (BTI) have been actively researched [67-70], circuit researchers typically have ignored the aging impacts on the analog and mixed-signal circuits. The devices used for the analog and mixed-signal circuit systems such as clock generators (e.g. PLL and DLL) and data converters (e.g. ADC and TDC) have been considered to be less affected by the aging due to their analog circuit configurations such as the amplifiers (i.e. one of the most crucial analog circuit building blocks) with multiple stacks of transistors with large device size (length and width). However, most of the recent analog and mixed-signal systems are not only consisting of the analog circuit building blocks, but they are also implemented with many digital-intensive or all-digital circuit building blocks. In reality, many of the existing analog and mixed-signal systems are now being replaced by their digital

implementations (e.g. digital PLL, digital ADC and etc.) as the performance of those circuits have become comparable to that of the analog counterparts while having all the benefits from using digital circuits such as easy scalability and supply noise insensitivity. Therefore, the negative aging impacts on the digital circuits are not any more confined to the traditional digital logic applications such as microprocessors, but they also degrade the analog and mixed-signal system performances. In this work, we analyze the device aging impacts on the ring-oscillator based digitally controlled oscillator (DCO) circuit which is the main building block of the digital PLL. Based on the analysis, we implemented an aging-tolerant digital PLL (DPLL) employing the proposed dynamic element matched (DEM) DCO circuit with the longer life time.

Fig. 8.1 illustrates the different stress mechanisms (HCI and BTI) applied to NMOS and PMOS transistors and an inverter (i.e. a representative digital logic circuit) during standard digital operating conditions. As shown in Fig. 8.1, NMOS and PMOS transistors are being stressed by the HCI phenomenon while the devices are switching on when the appropriate bias voltages are applied to NMOS and PMOS gates (i.e. supply voltage to NMOS gate and ground for PMOS gate). Once the devices are fully turned on, the NMOS and PMOS devices are now stressed by the BTI effects. Based on the gate bias voltage polarity, the BTI stress applied to NMOS is called PBTI (positive BTI) and the opposite voltage stress applied to PMOS is called NBTI (negative BTI). Both HCI and BTI stress mechanisms are characterized by positive shifts in the threshold voltages of NMOS and PMOS. While the device aging due to the BTI stress is mostly recovered when the stressed device is turned off, the aging due to the HCI stress is

permanent. Detailed explanations on the physics of the stress mechanisms can be found in [67].

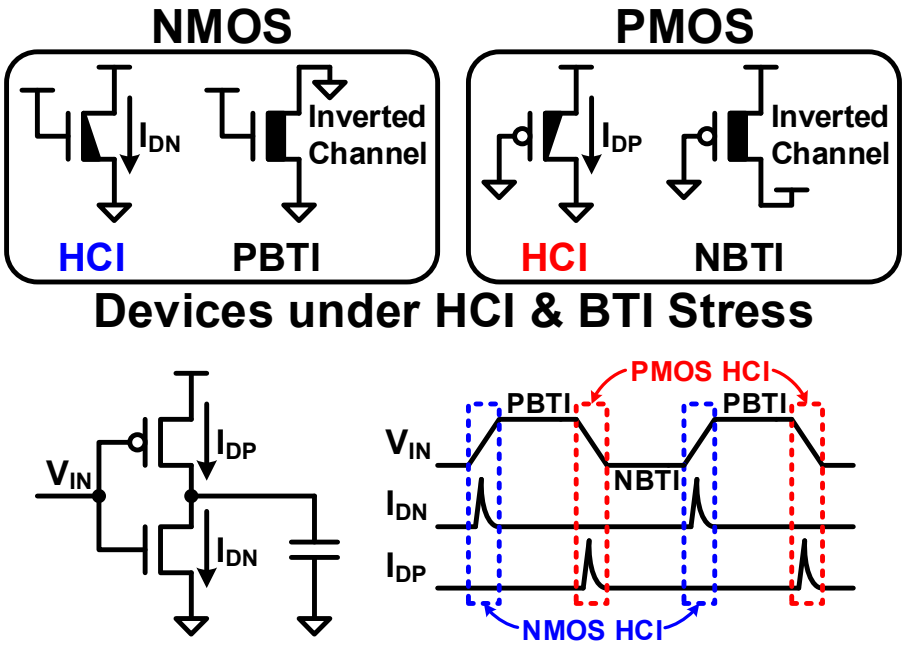


Fig. 8.1. HCI and BTI stresses applied to NMOS, PMOS and an inverter during standard operation.

As shown in Fig. 8.1, the different stress mechanisms negatively affect both NMOS and PMOS devices while the inverter is operating as a standard digital logic. Note that the ring-oscillator based DCO circuit for DPLL can be built with a chain of these inverters. As one of the most important building blocks, DCO plays a crucial role (i.e. generating a high frequency clock with low phase noise) in DPLL. DCO generates the DPLL output clock and its frequency is controlled by the input digital control code which tunes the fine frequency trimming elements such as the distributed capacitor banks [61]. While the same stress mechanisms are being applied to the ring-oscillator based DCO circuit, the impact of those stresses are reflected to the degraded DCO

output frequency (i.e. DPLL output frequency). Therefore, the DCO under aging could affect the entire DPLL operation (i.e. failure to generate the target high frequency clock due to the aging) especially when the DCO has the narrow frequency range.

While the DCO circuit is consist of standard logic inverters, the aging impact of DCO could be different from that of the standard digital logic circuitry due to its different operating frequency. For instance, let's assume that the DPLL is being used for a microprocessor. The average switching probability of the digital logic path in the processor is much lower than the operating system clock frequency. In fact, the average switching rate of the digital logic path in the processor operating at 2-3GHz frequency is typically in the range of tens of MHz to 100MHz at most depending on the operating conditions. In other words, the nominal operating frequency of DCO circuit in DPLL is 20-30x higher than that of the typical digital logic circuit.

To illustrate the impact of different switching frequencies on the device aging, Fig. 8.2 shows the inverter input voltage and NMOS and PMOS transient currents under different operating frequency. In Fig. 8.2, we have different operating frequency (i.e. 1x, 2x, 4x) under the fixed operating time period. As explained from the different device stress mechanisms shown in Fig. 8.1, the increased number of device transitions will bring the proportionally increased number of HCI occurrences. The HCI occurrences for each NMOS (i.e. dotted blue circles) and PMOS devices (i.e. dotted red circles) and a plot of those occurrences with respect to the operating frequency are shown in Fig. 8.2, right. Based on the plot, we can easily see that the impact of HCI stresses of DCO circuit (and DPLL) could become much larger than that of the conventional digital logic circuitry.

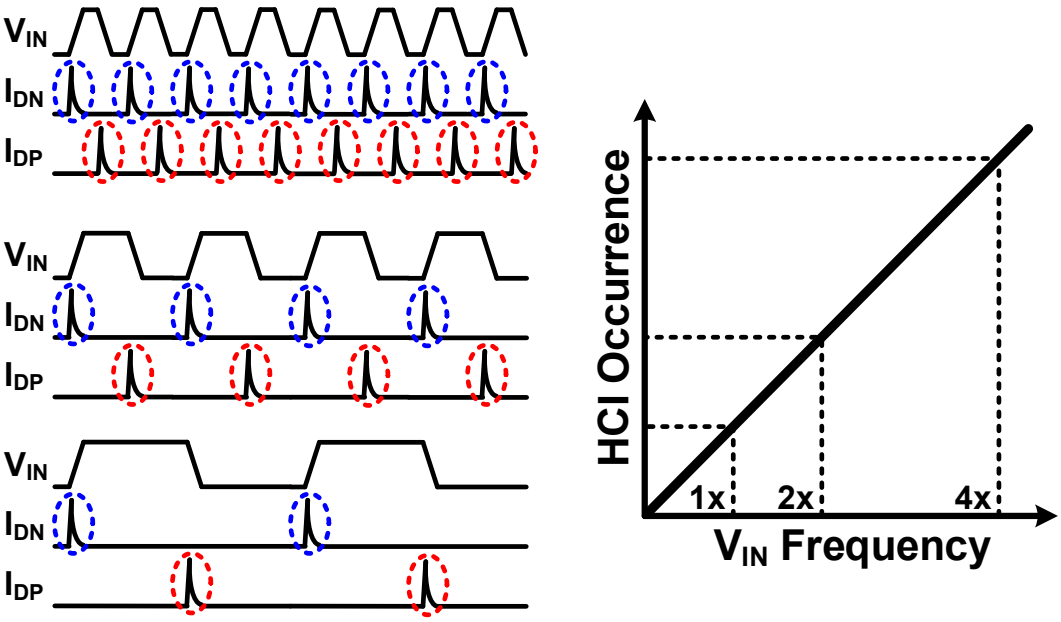


Fig. 8.2. Increasing HCI occurrence in proportion to the inverter operating frequency.

The prior aging measurement result (Fig. 8.3) with different operating (stress) frequency did already prove the dependence of HCI stress impacts on the digital circuits with respect to its operating frequency. The measured results in Fig. 8.3 shows the frequency shifts due to the different AC device stresses (with different frequency) applied to a ring oscillator circuit which consists of an all-digital inverter chain. The stressed ring oscillator frequency starts to degrade much faster as the HCI stress overtakes the entire stress impact as we can see from the crossing points for each BTI and HCI plots with different frequency. As the AC frequency increases, the crossing point moves toward the left and therefore, the corresponding life time of the digital circuit will be shortened. While the HCI occurrences are increasing in proportion to the operating frequency, we can also predict that the BTI effects on the same DCO circuits will be somehow reduced since transistors in DCO will be undergoing dynamic transitions for the major time portions while the DCO is operating. The previous

measurement results in Fig. 8.3 proves the slightly decreased BTI aging impacts on the digital logic circuits while increasing the circuit operating frequency.

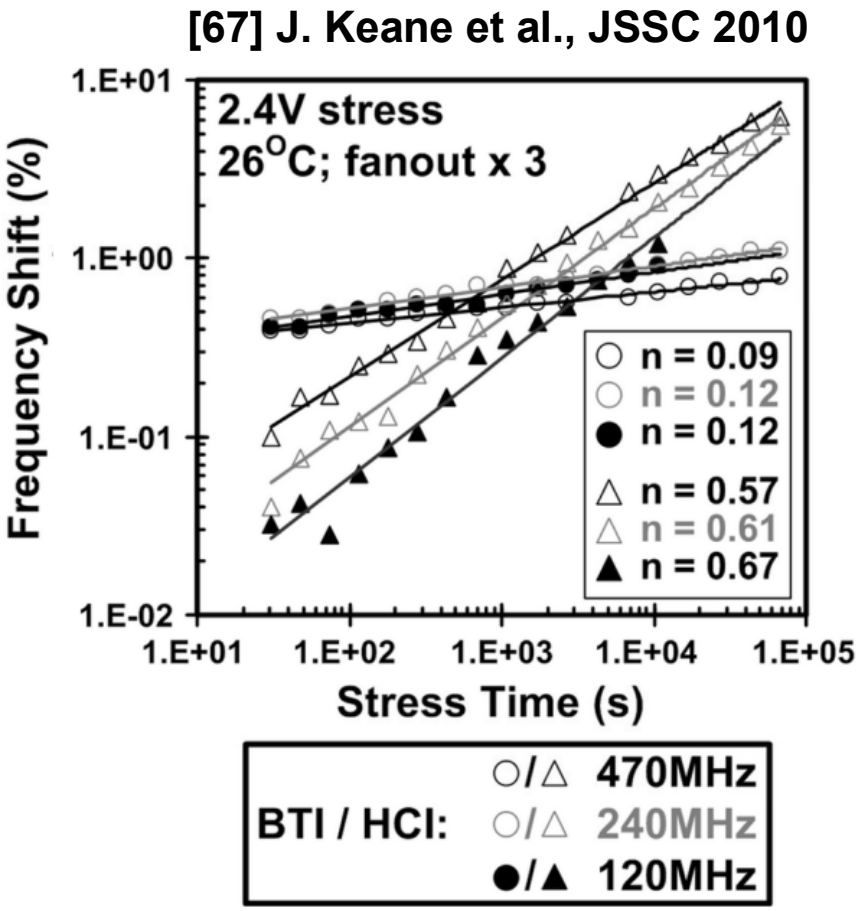


Fig. 8.3. Ring oscillator frequency shift (degradation) due to the aging. HCI quickly dominates the entire aging as frequency increases.

In this work, we propose an aging-tolerant digital PLL circuits employing a dynamic element matched (DEM) digitally-controlled oscillator (DCO) circuit. By reusing (i.e. alternating based on the DEM logic while the PLL is changing their modes) the typically unused inverter chains after an automatic frequency calibration mode of digital PLL, the HCI aging impact has been reduced. In addition, an on-chip DCO reliability monitor (for measuring DCO frequency degradation due to aging) based on the high-resolution beat frequency detection scheme [67] is integrated for the first time with PLL.

The remainder of this chapter is organized as follows. Section 8.2 introduces the impact of DCO aging on digital PLL. Section 8.3 describes the DCO frequency degradation with respect to the different aging mechanisms and the impact of conventional and the proposed DCO circuits on the aging. The proposed aging-tolerant digital PLL circuit and the 65nm test-chip implementation details are shown in Section 8.4. The test chip measurement results are given in Section 8.5 and Section 8.6 concludes the chapter.

8.2 DCO Aging Impact on Digital PLL

To achieve wide output frequency range while lowering the digitally-controlled oscillator (DCO) gain (i.e. K_{DCO}) for having the fine frequency resolution, the automatic frequency calibration (AFC) method [71-74] has been widely used for digital PLLs shown in Fig. 8.4. The DCO frequency difference due to the process variation is also calibrated by the AFC operation. Once the AFC is done, the DCO frequency variation due to the voltage and temperature variation is supposed to be covered by the DCO frequency range while the PLL is being under locked condition with its negative feedback loop operation.

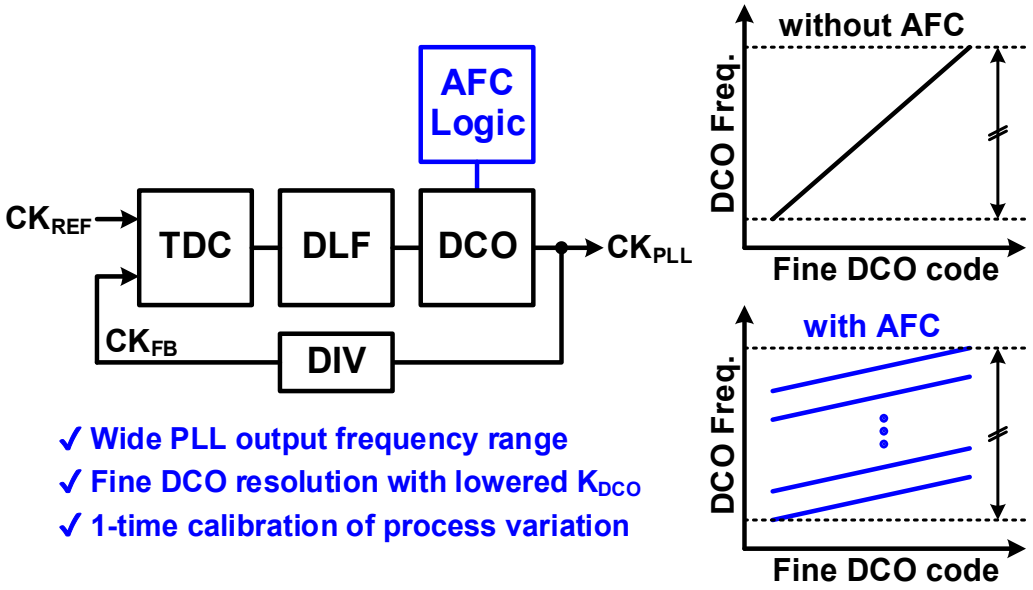


Fig. 8.4. Digital PLL with automatic frequency calibration (AFC).

As the ring-oscillator based DCO ages, the output frequency is degraded while it is working as a stand-alone free running oscillator. When it is used as a building block of digital PLL, then the digital input control code will be increasing while PLL is

generating the same output frequency. Once the digital control code hits its maximum code, PLL could not be locked any more. Note that the AFC operation can be done before the PLL fine locking operation every time when PLL is enabled. However, the increased settling time with the added AFC operation comes with the decreased energy efficiency due to the additional PLL power consumption during the AFC operation. Therefore, the AFC operation is typically used for the one-time calibration of DCO frequency difference due to the process variation.

From the prior researches on the circuit and device aging (e.g. HCI aging), we can assume that the aging impacts on CMOS digital circuitry will become significantly large when the circuit is built with minimum length devices and operated under the higher supply voltage than the nominal value. Based on these assumptions, the aging impacts on the voltage-controlled oscillator (VCO) circuit in analog PLL is relatively small since the VCO is typically controlled by the local supply voltage which is lower than the nominal PLL supply. This is also true for the DCO circuit which is internally consist of a cascaded DAC and VCO instead of a true DCO circuit. However, the DCO circuit with fine frequency tuning elements such as the capacitor banks [61] is directly controlled by the nominal supply voltage and it is typically designed with minimum length devices to generate the several GHz high frequency output clock.

In addition to the increased concerns on DCO aging with the use of minimum length devices and the nominal supply voltage, the high frequency operation of DCO circuit is another concern. While the BTI stress dominates the entire aging effects when the digital circuit operating frequency is low (i.e. tens of MHz ~ few hundreds of MHz), the HCI stress will quickly take over the overall aging impacts as the frequency increases (i.e.

hundreds of MHz ~ several GHz) [67]. Based on the prior aging measurement results, HCI was the much faster aging mechanism than BTI and therefore it will dominate the aging effects though the initial impact is much smaller than BTI. Therefore, the frequency degradation of DCO operating at several GHz frequency will be much faster than the typical digital logic circuits with tens of MHz average transition rates due to the much severe HCI stresses.

In Fig. 8.5, we describe the possible PLL locking failure with DCO aging. After the AFC (i.e. coarse frequency locking) logic and the PLL locking (i.e. fine frequency and phase locking) operation, DCO in the PLL keeps operating in the high oscillation frequency. While the DCO circuit is working properly within the PLL loop, the DCO code for the generating the same target PLL frequency is gradually increasing due to the stressed devices in the DCO circuit. As a result, the PLL could not be locked from a time point (Fig. 8.5, right) when the maximum DCO frequency becomes lower than the target frequency.

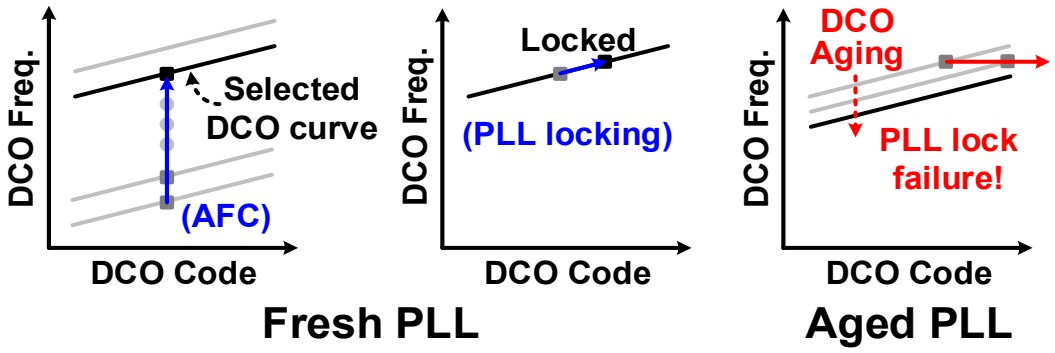


Fig. 8.5. Description on the negative impact of DCO aging on PLL (i.e. lock failure).

8.3 Dynamic Element Matched Ring-DCO Circuit

Fig. 8.6 shows the DCO circuit with enabled and disabled inverter chains after AFC operation. For N-bit AFC operation, all the multi-phase internal DCO nodes of 2^N replica inverter chains are connected in parallel. Once the AFC operation is done, the power switches of the selected M out of 2^N inverter chains are enabled while the other 2^N-M inverter chains are disabled by gating them off from the supply and ground. As a result, the enabled M chains are under BTI and HCI aging while it is operating and the disabled 2^N-M inverter chains on the other hand are under only BTI aging. Therefore, the disabled inverter chains are being kept relatively fresh compared to the enabled inverter chains.

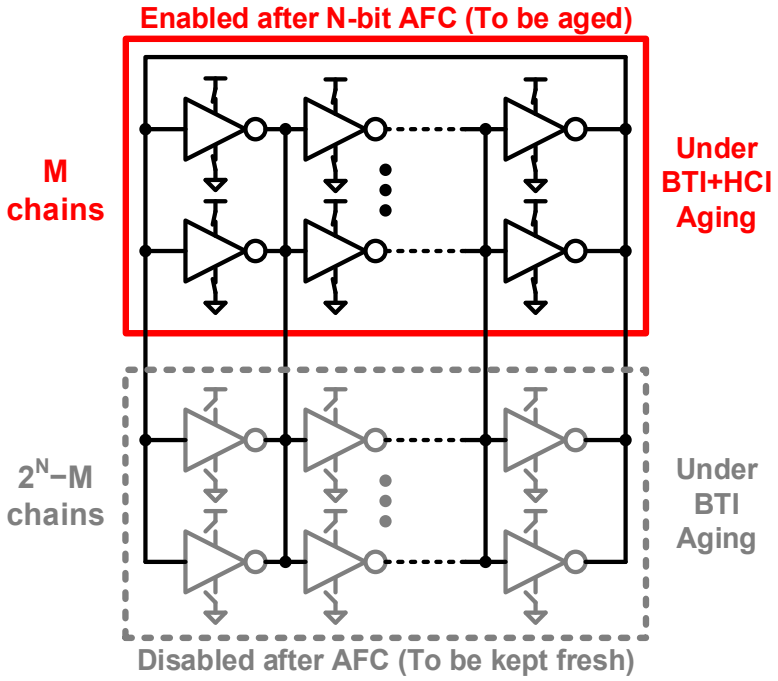


Fig. 8.6. Enabled and disabled DCO inverter chains after AFC operation. The enabled inverter chains are under both BTI and HCI aging while it is operating. On the other hand, the disabled chains are being kept relatively fresh since it is only affected by BTI aging [67].

The proposed dynamic element matched (DEM) ring-DCO circuit minimizes the HCI aging impact on the DCO frequency degradation by fully utilizing the inverter chains designed for AFC operation. As shown in Fig. 8.7, the selected inverter chains while the PLL mode is a transition (from idle to active) are sequentially switched based on the DEM logic operation while the conventional DCO is only utilizing the fixed inverter chains once the AFC operation is done. As a result, the proposed DEM based DCO circuit undergoes the effective aging impact of 37.5% (i.e. 3/8 reduced aging impact) while the conventional DCO is stressed 100% while it is operating.

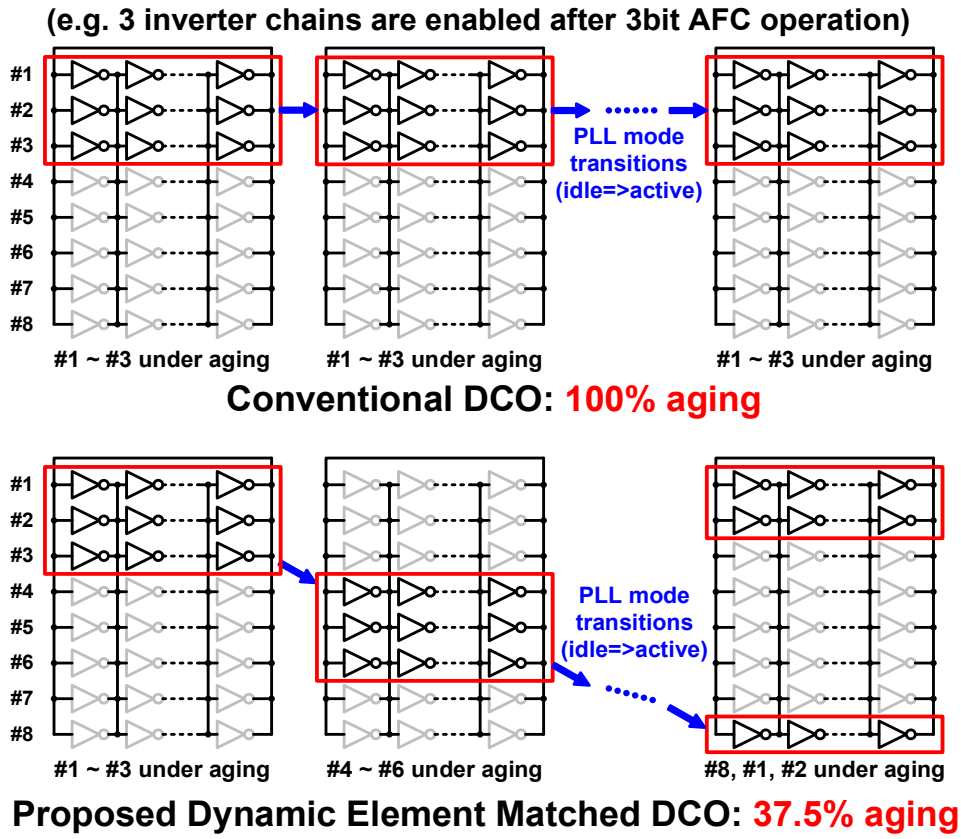


Fig. 8.7. Concept of the dynamic element matched (DEM) DCO for minimizing aging impact on ring-type DCO. The HCI aging impact will be reduced by 3/8 in this example. Note that the inverter chains are enabled and disabled sequentially while the PLL mode is changing (i.e. idle mode to active mode).

8.4 Aging-Tolerant Digital PLL Implementation in 65nm

8.4.1 Aging-tolerant digital PLL circuit

Fig. 8.8 shows the implemented bang-bang PFD based digital PLL with the proposed dynamic element matched DCO circuit (i.e. stress DCO in Fig. 8.8) and the on-chip DCO aging monitor based on the beat frequency detection scheme [75, 76]. A replica DCO circuit is also integrated as a reference DCO without stress for the on-chip aging measurement. While the PLL is operating (Fig. 8.9), a multiplexer in between digital loop-filter (DLF) and the DCO routes the DLF output (i.e. a 10bit fine DCO code, F_DCO[9:0]) to the stress DCO while the test code for aging measurement (i.e. a 10bit test code, F_TEST[9:0]) is being used for controlling the stress and reference DCO when the aging measurement is undergoing (Fig. 8.10). The stress DCO is controlled by a 16bit thermometer code (C_DEM[15:0]) which is the output of a DEM logic. The incoming 4bit binary code (C_DCO[3:0]) from AFC logic is converted to a thermometer code and the output is updated every rising edges of the DEM update clock, CK_{DEM}.

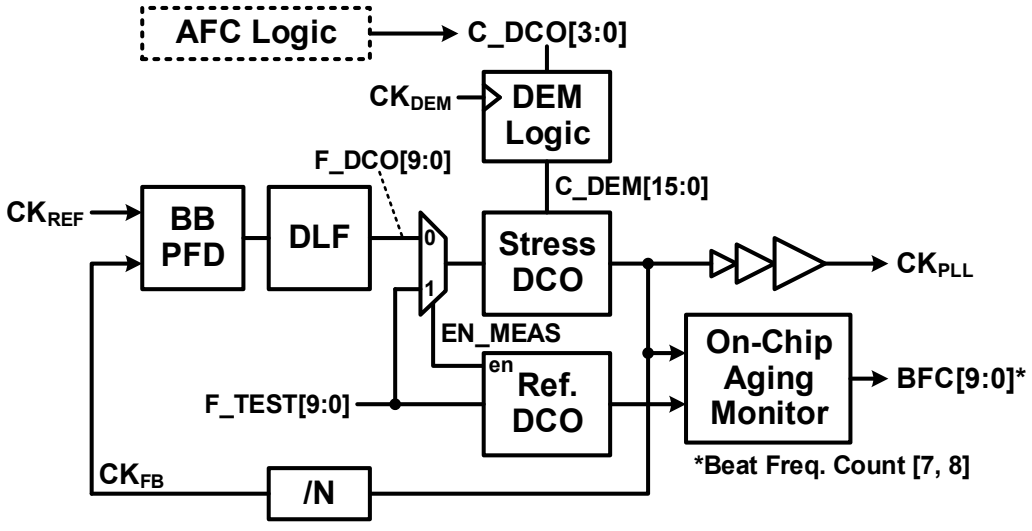


Fig. 8.8. Digital PLL circuit with the proposed dynamic element matched DCO.

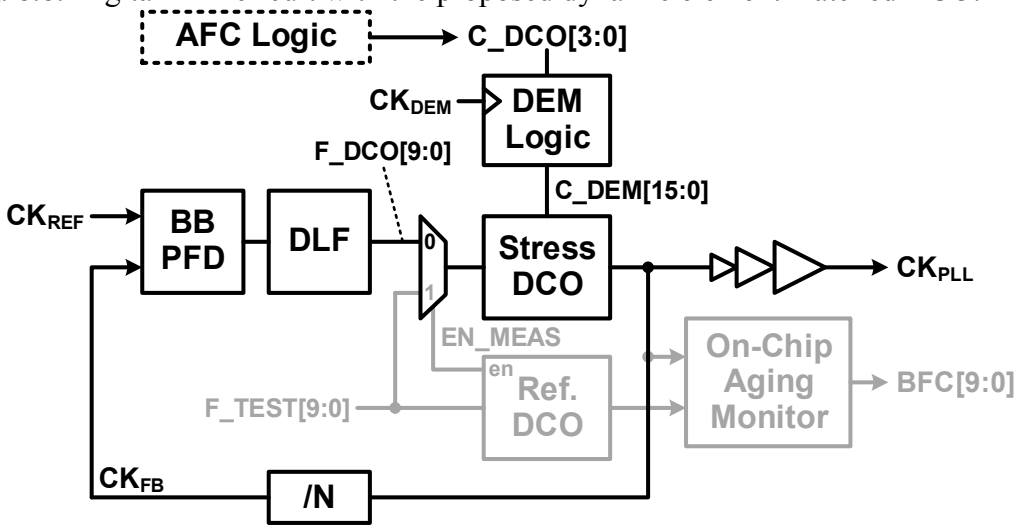


Fig. 8.9. PLL circuit in a stress mode. PLL is operating in an accelerated aging condition with a high stress voltage. A 2x nominal VDD (i.e. 2.4V) has been used.

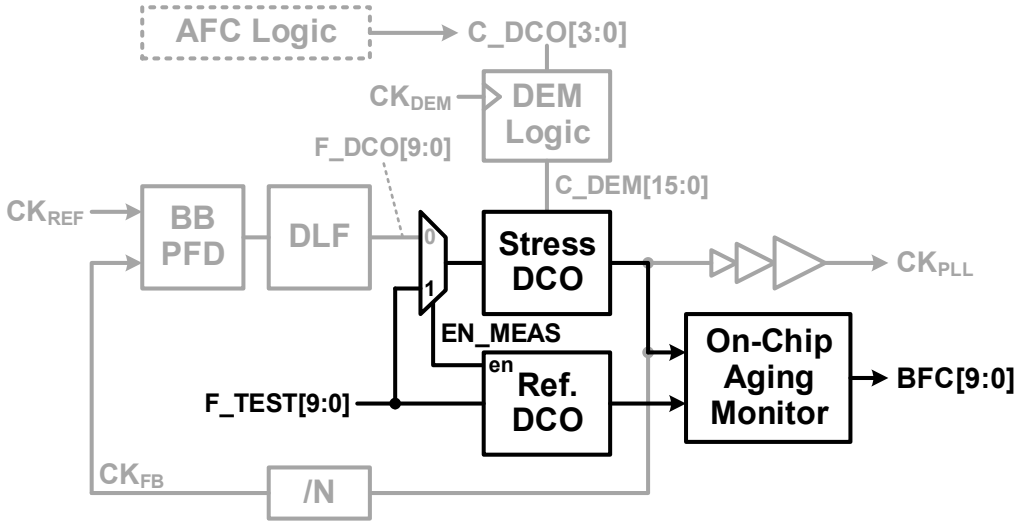


Fig. 8.10. PLL circuit in a measurement (i.e. DCO aging on-chip monitoring) mode.

Fig. 8.11 describes the timing diagrams of the DEM based DCO operation. When the PLL mode changes from idle to active mode, CK_{DEM} is enabled and the rising edge of CK_{DEM} updates the DEM logic output. For instance, Fig. 8.11 shows the DEM outputs and the resulting PLL clock output (CK_{PLL}) when the three inverter chains are selected after AFC operation. While having the same PLL output clock frequency, the selected (enabled) inverter chains are switched from the 0^{th} to 2^{nd} to the 3^{rd} to 5^{th} chains based on the DEM logic outputs (C_DEM[0:15]).

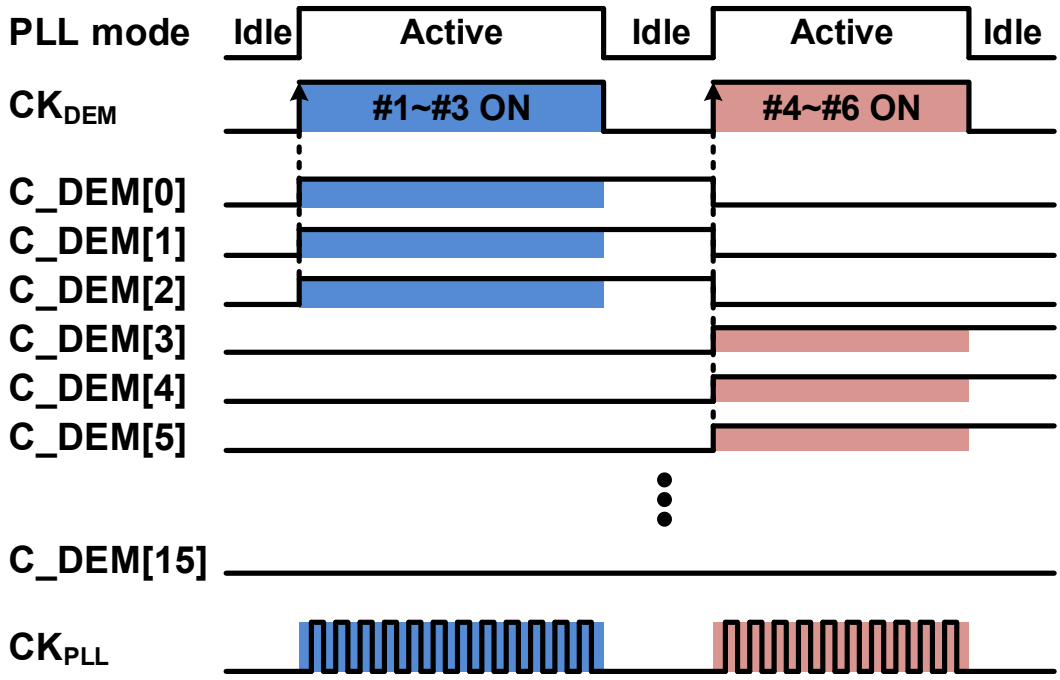


Fig. 8.11. Use of dynamic element matched DCO based digital PLL for processor cores with frequent idle/active state transitions.

8.4.2 Dynamic element matched DCO circuit

Fig. 8.12 shows the DEM logic circuit. The incoming 4bit binary inputs from AFC logic is converted to a 16bit thermometer code and shifted to the output with the barrel shifter circuit in [29]. The barrel shifter is controlled by the output of a 4bit accumulator which integrates the input binary code at every CK_{DEM} rising edges. The 16bit thermometer DEM logic outputs are connected to the DCO circuit shown in Fig. 8.13 and it controls the number of enabled inverter chains for coarse PLL frequency setting. A pair of power switches are designed for controlling the supply voltage of stress and reference DCO circuit. When the test chip is operating in the stress mode (i.e. MEAS_STR = 0), VDD_Stress which has 2x higher voltage (2.4V) than the nominal supply (1.2V) to expedite the DCO aging for testing purpose is connected to the stress DCO while the ground is connected to the reference DCO to prevent it from aging. In the measurement mode (i.e. MEAS_STR = 1), the switches for both stress and reference DCO are connected to the nominal supply so that we can measure the frequency degradation of stress DCO by comparing it with the reference DCO frequency with no aging. For the 10bit fine DCO frequency control, fine capacitor elements [61] are distributed throughout the multi-phase DCO outputs.

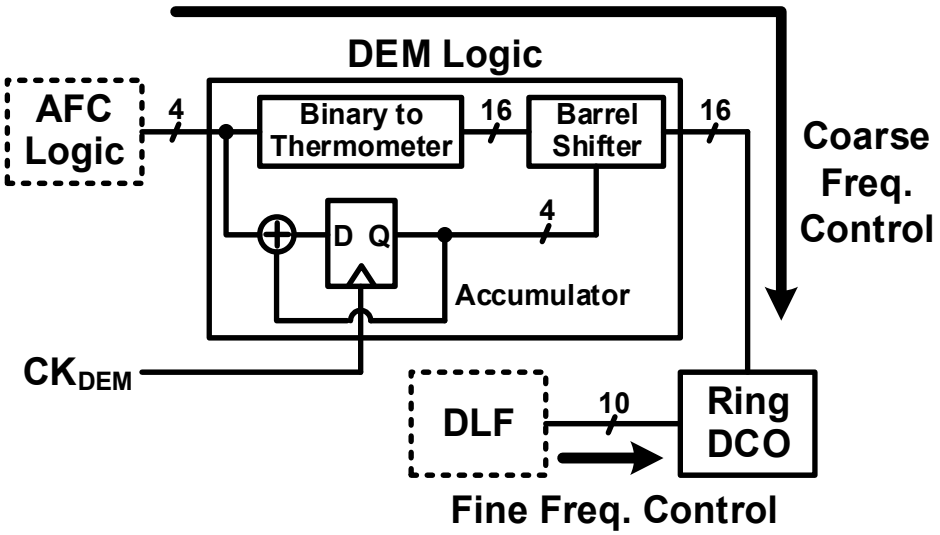


Fig. 8.12. DEM logic with an output thermometer code for DCO coarse frequency control.

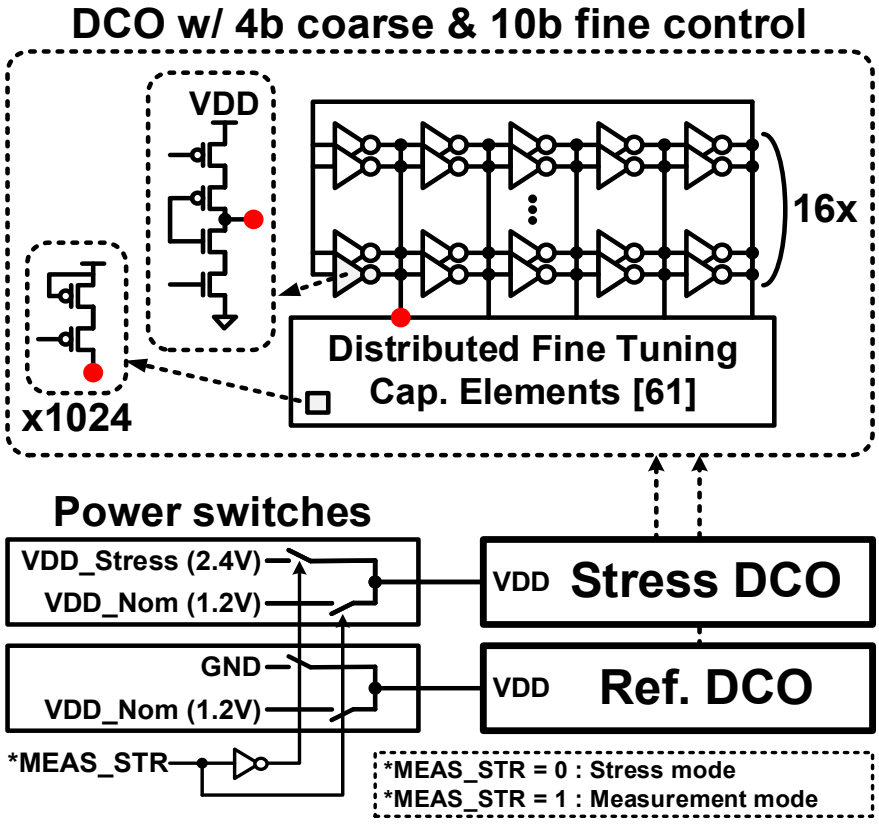


Fig. 8.13. DCO circuit with power switches for stress/measurement control.

8.4.3 On-chip DCO aging monitor circuit

Fig. 8.14 describes the on-chip aging monitor circuit for measuring the frequency degradation due to the DCO aging. The monitor circuit based on the beat frequency detection scheme [67, 75, 78-80] is capable of measuring a slight frequency degradation due to the different aging mechanisms (i.e. BTI and HCI) within a very short measurement interruption time (<1μs). Input clock phases of the incoming stressed DCO clock (CK_{STR}) and the reference DCO clock (CK_{REF}) are compared at the D flip flop (DFF) and the output (i.e. beat frequency clock) is going through a 5bit voter circuit to reject erroneous bubbles while the output is under transition (i.e. low-to-high or high-to-low). A 10bit asynchronous ripple counter is used for counting a period of the beat frequency clock by using the reference clock input as a counting reference. A short pulse generator delays the beat frequency clock and generates sequential short pulses for reading the counter outputs and resetting the counter after reading the output. Finally, an external trigger signal (READ_BF) is used for sampling of the monitor output.

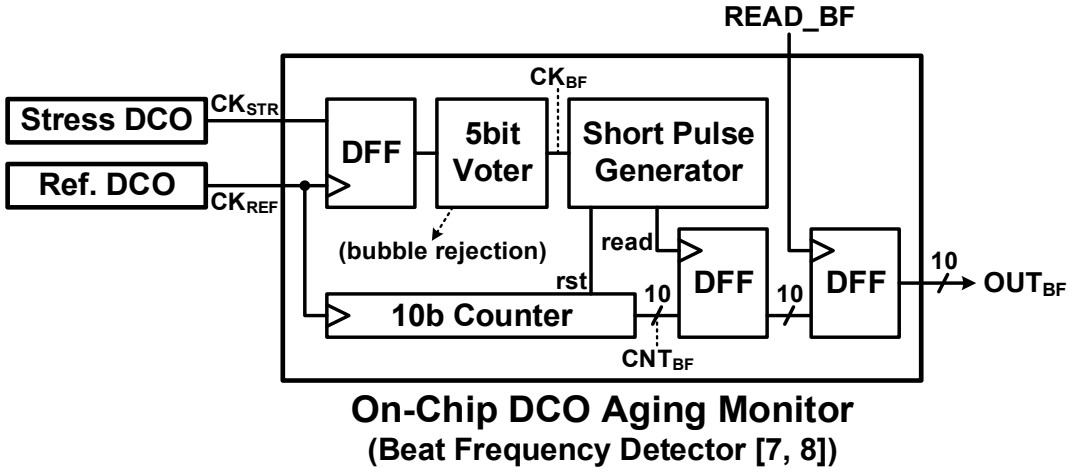


Fig. 8.14. On-chip aging monitor circuit based-on beat frequency detection scheme.

Fig. 8.15 shows the timing diagram of the on-chip aging monitor circuit operation. The stress DCO in Fig. 8.8 is operating under a 2.4V supply voltage (i.e. 2x larger than the 1.2V nominal supply) when the test-chip is operating under the stress mode and therefore, the clock output (CK_{STR}) has 2.4V swing as shown in Fig. 8.15. On the other hand, the reference DCO in Fig. 8.8 is turned off (i.e. no alternating output as shown in Fig. 8.15) so that it is kept as a fresh DCO while the stress DCO is under stressed. In the measurement mode, both stress and reference DCO are now connected to the 1.2V nominal supply voltage for measuring the frequency degradation of the stress DCO. For a period of beat frequency clock (CK_{BF}), the counter output is incremented with the reference clock (CK_{REF}) and then finally sampled to the output (OUT_{BF}) by using an external trigger signal (READ_BF) once a cycle of the BF count is done.

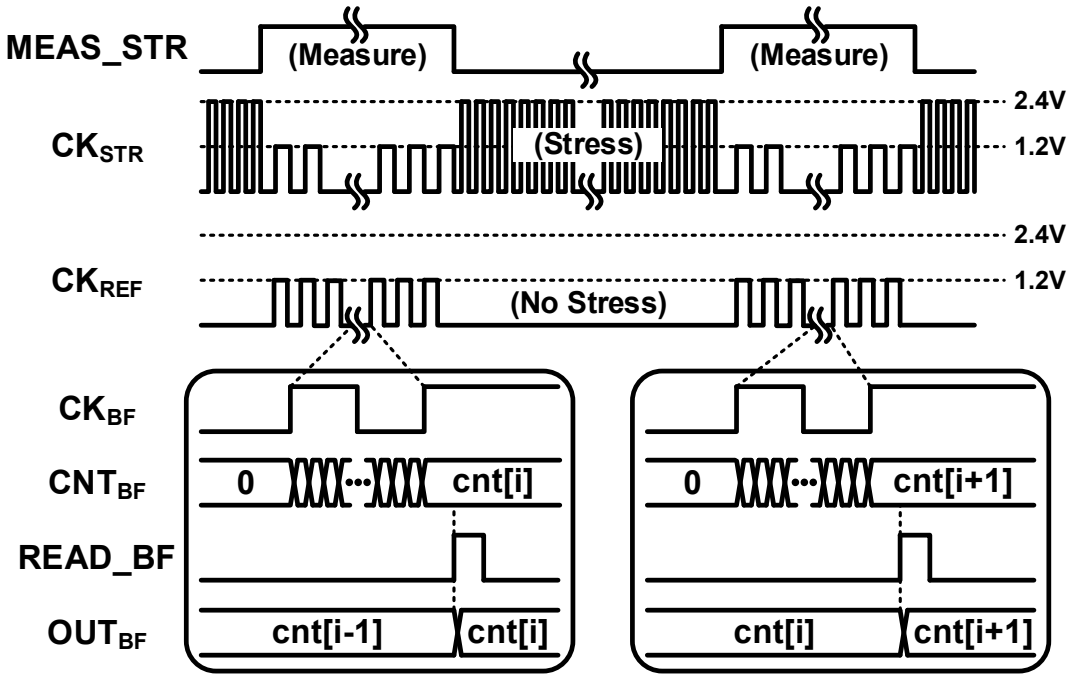


Fig. 8.15. On-chip aging monitor timing diagram.

8.5 Test-Chip Measurement Results

Fig. 8.16 shows the measured frequency degradation of the conventional and the proposed dynamic element matched DCO circuit when it is stressed with 2.4V stress supply voltage (i.e. 2x nominal 1.2V supply voltage) and 0.8GHz oscillating frequency. The slower frequency degradation (i.e. slower slopes in Fig. 8.16) at the early stress time (<100sec) is due to the BTI stress impact while the faster frequency degradation (i.e. steeper slope) after about 100sec is due to the HCI stress.

To compare the different amount of aging impacts, we define the DCO life time as the time it takes to have 5% frequency degradation. We assumed that the DCO is not able to generate the desired PLL output frequency after the 5% of frequency degradation and hence, the PLL is unable to be locked. Based on the assumption, we extract the DCO life time from the measured frequency degradation in Fig. 8.16 and the proposed DCO has the longer life time (i.e. 2.91x) than the conventional DCO as a result. This is due to the effectively lowered HCI aging impact on the inverter chains due to the sequentially enabled inverter chains with DEM logic. Fig. 8.17 highlights the HCI aging portion by plotting the DCO frequency degradation from 100sec stress time. In Fig. 8.17, the life time has improved more when the AFC code (C_DCO[3:0]) is low. In other words, it is clear that the beneficial impact of the proposed DCO circuit is maximum when the AFC code is minimum (i.e. when there are many unused inverter chains after AFC operation). Die micrograph and performance summary are shown in Fig. 8.18 and Fig. 8.19.

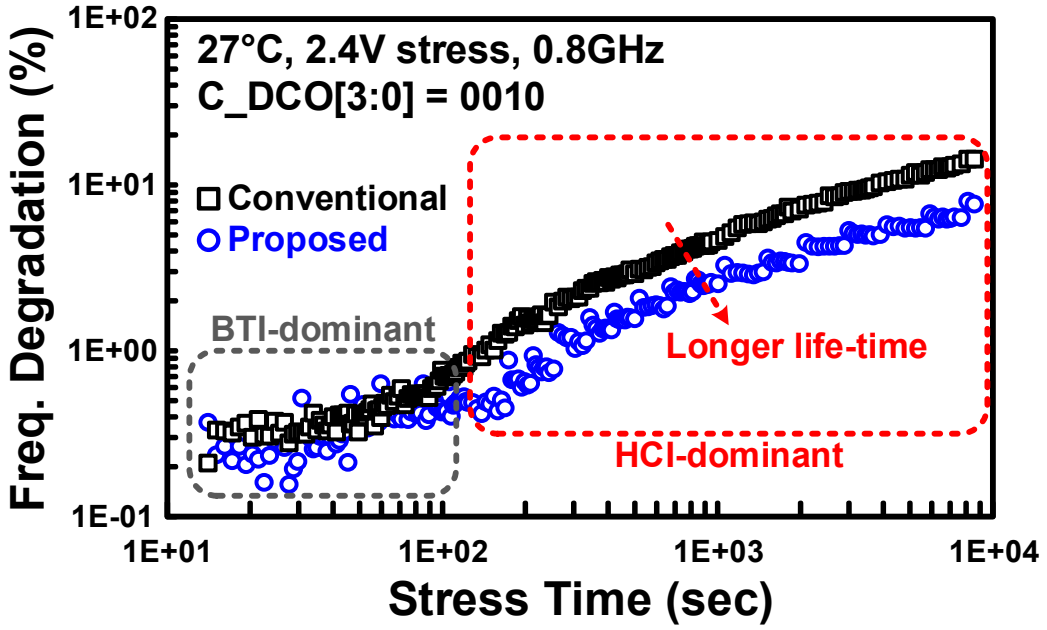


Fig. 8.16. Measured DCO frequency degradation due to aging with conventional and proposed DCO.

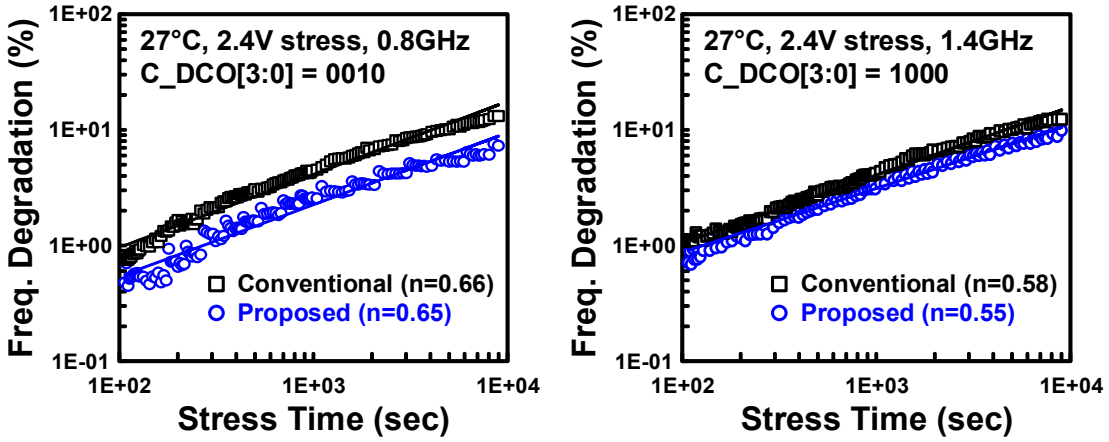


Fig. 8.17. Measured DCO frequency degradation due to HCI aging with different C_DCO [3:0].

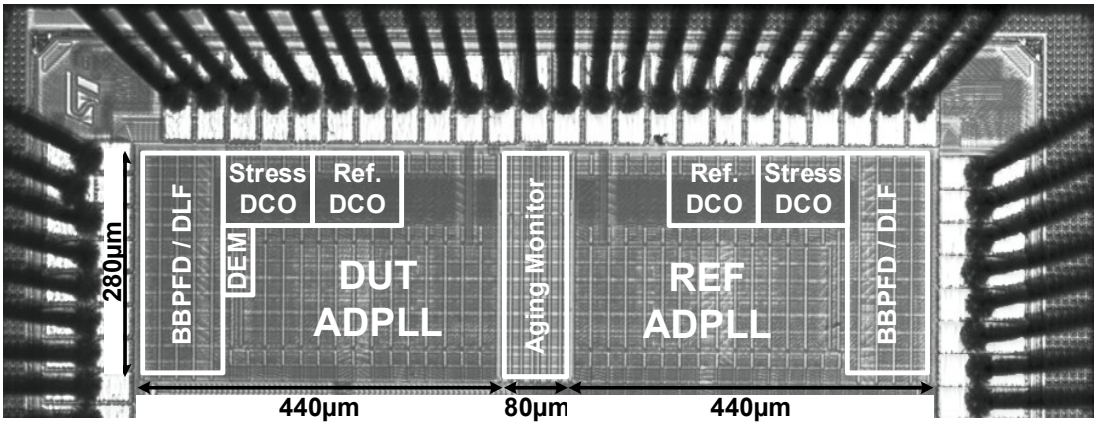


Fig. 8.18. Chip micrograph.

Process	65nm CMOS
Nominal Supply	1.2V
Stress Supply	2.4V
DCO Range @ Stress Supply	0.6GHz ~ 3.4GHz
Aging monitor resolution (ΔT)	< 1ps
Life-Time* w/ Conv. DCO [s]	1.15e3 @ C_DCO=0010
Life-Time* w/ Proposed DCO [s]	3.35e3 @ C_DCO=0010

*Stress time @ DCO freq. degradation becomes 5%

Fig. 8.19. Chip summary.

8.6 Conclusion

The impact of NMOS and PMOS device aging due to different stress mechanisms (i.e. HCI and BTI) on DCO circuits of digital PLL has been analyzed in this work. Based on the analysis, an aging-tolerant digital PLL employing a dynamic element matched ring oscillator based DCO is demonstrated in 65nm CMOS process. By dynamically utilizing the unused inverter chains after the one-time AFC operation, the average HCI impact has been reduced in the proposed DCO circuit. Both proposed and conventional DCO frequency degradations due to the DCO circuit aging is measured with an on-chip reliability monitor based on the beat-frequency detection scheme. From the measured frequency degradation data, the DCO life time has been extracted by assuming the DCO frequency degrades as much as 5% when the DCO could not be locked to the desired PLL output frequency. The measured life time with the proposed DCO circuit is 2.91x longer than the conventional DCO circuit.

Chapter 9 Summary

In this thesis, digital intensive circuit design techniques for enhancing the overall performance of mixed-signal clock generators (charge-pump PLL, all-digital PLL based on TDC or binary bang-bang phase detector) and data converters (VCO-based ADC, time amplifier based TDC) were demonstrated in 32nm SOI and 65nm CMOS process.

The first contribution of this thesis is the invention of the first adaptive PLL which optimizes the processor power and performance by adaptively tracking the supply noise sensitivity with the developed closed loop operation based on the on-chip bit error monitoring circuitry. The theoretical analysis on the mechanism of the optimal supply noise sensitivity tracking and its demonstration in a 32nm SOI processor were described in chapter 2. With the invented adaptive circuit technique, a 14.5% to 15.6% processor F_{max} improvement was achieved for a resonant supply noise amplitude of 10% VDD. The improved F_{max} can be directly translated into a 9.8% power reduction for iso-performance as the proposed PLL allows the system to operate at a lower voltage while meeting the same performance requirement. The use of deep trench capacitors in the PLL loop filter enabled a 92.1% area reduction compared to a conventional PLL with a thick-oxide capacitor implementations.

The invention of VCO-based ADCs in chapter 3 and 4 based on beat frequency quantization schemes for the direct acquisition of sub-mV input signals is the second contribution of this thesis. The power and area consuming signal preconditioning amplifiers which have been typically used for the physiological signal acquisition frontend circuits for wide variety of biomedical and health-care systems can be

completely removed by using the proposed ADCs. Two versions of the VCO-based ADCs have been demonstrated in 65nm CMOS process. The first one utilizing the beat frequency quantization scheme in a Nyquist-rate VCO-based ADC achieves 39dB SNDR (6.2 ENOB) for a 1.6mV input signal without any external signal amplification or conditioning circuitry. A prototype 8-channel time-multiplexing signal acquisition system has been also demonstrated and its function of the direct multi-channel sub-mV signal acquisition has been verified with separated 8-channel active electrode circuits. The second VCO-based ADC was developed based on the newly designed multi-phase noise-shaping beat frequency quantizer. To utilize the beneficial noise-shaping property, an oversampling VCO-based ADC was implemented in a 65nm CMOS process. The measurement data from the test chip shows a 43dB SNDR (6.9ENOB) for a 1mV input signal with 10kHz signal bandwidth when sampled at a frequency of 300kHz.

The third contribution of this thesis is the invention of novel digital-intensive time-amplifiers for time-to-digital converters (TDC) with high resolution and wide input range. Chapter 5 demonstrated the switched ring-oscillator based time amplifier (TA) and the three-step TDC circuit incorporating the proposed TA circuit. The simulated TA performs an 8x time amplification while having a 100ps input range with a gain variation ranging from -4% to 5% while the gains of the existing techniques vary from -71% to 15% or -83% to 3%. The demonstrated 9bit three-step TDC circuit in 65nm achieved a 1.8ps time resolution while having the maximum DNL of 0.9/1.9LSB and the maximum INL of 3.7/10LSB for 2-step/3-step modes. Chapter 6 presented a noise-shaping TDC circuit based on the proposed adaptive pulse train time amplifier circuit. The TDC is implemented with an all-digital PLL for verifying its functionality and PLL

in-band phase noise improvement by using it. The maximum gain of 16x is achieved when the time input is minimum while the lowest gain of 1x ensures the wide input range. The measured in-band phase noise with 0.4GHz PLL output clock at 100kHz frequency offset is -98dBc/Hz. The integrated phase jitter from 10kHz to 1MHz offset frequency is measured to be 8.4ps.

In addition to the digital PLLs with novel time amplifier based TDCs demonstrated in chapter 5 and 6, a novel TDC-less digital PLL was also proposed. A novel spur-free bang-bang digital PLL (BBPLL) with the proposed fractional sub-sampling (FSS) phase detector circuit demonstrated in chapter 7 is the fourth main contribution of this thesis. The sub-sampling operation of the proposed FSS circuit lowers the in-band phase noise and its intrinsic first-order noise-shaping behavior suppresses the spurious noise due to the limit cycle regime of BBPLL. The measured results show the proposed BBPLL in-band phase noise at 1.6GHz of -97dBc/Hz which is 9dB lower than that of the conventional BBPLL. The integrated phase jitter at 1.6GHz from 20kHz to 2MHz frequency offset is 2.8ps while that of the conventional BBPLL is 7.9ps.

The final contribution of this thesis is the development of the on-chip reliability monitor for measuring the DCO frequency degradation due to the device aging and the aging-tolerant digital PLL. The aging-tolerant BBPLL based on the dynamic element matched DCO circuit was demonstrated in chapter 8. Without the use of additional power or area consumption, the life time of DCO circuit is 2.91-times longer than that of the conventional DCO. The life time improvement was achieved by utilizing the typically unused inverter chains after the one-time automatic frequency calibration of

conventional PLL. The hot carrier injection (HCI) stress induced device aging impact has been effectively reduced by using the proposed technique.

References

[1] M. Saint-Laurent and M. Swaminathan, “Impact of power-supply noise on timing in high-frequency microprocessors,” IEEE Transactions on Advanced Packaging, vol. 27, no. 1, pp. 135–144, Feb. 2004.

[2] K. L. Wong, T. Rahal-Arabi, M. Ma, et al., “Enhancing microprocessor immunity to power supply noise with clock-data compensation,” IEEE Journal of Solid-State Circuits (JSSC), vol. 41, no. 4, pp. 749-758, Apr. 2006.

[3] X. Hu, T. Toms, R. Radojcic, et al., “Enabling power distribution network analysis flows for 3D ICs,” Proceedings of IEEE International 3D Systems Integration Conference, pp. 1–4, Sep. 2010.

[4] V. Gutnik and A. Chandrakasan, “Active GHz clock network using distributed PLLs,” IEEE Journal of Solid-State Circuits (JSSC), vol. 35, no. 11, pp. 1553–1560, Nov. 2000.

[5] T. Fischer, J. Desai, B. Doyle, et al., "A 90-nm Variable Frequency Clock System for a Power-Managed Itanium Architecture Processor," IEEE Journal of Solid-State Circuits (JSSC), vol. 41, no. 1, pp. 218-228, Jan. 2006.

[6] M. Mansuri and C. K. Yang, "A Low-Power Adaptive Bandwidth PLL and Clock Buffer with Supply-Noise Compensation," IEEE Journal of Solid-State Circuits (JSSC), vol. 38, no. 11, pp. 1804-1812, Nov. 2003.

[7] S. Yasuda and S. Fujita, "Compact Fault Recovering Flip-Flop with Adjusting Clock Timing Triggered by Error Detection," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 721-724, Sep. 2007.

[8] E. Hailu, D. Boerstler, K. Miki, et al., “A circuit for reducing large transient current effects on processor power grids,” IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 2238–2245, Feb. 2006.

[9] J. Gu, R. Harjani, and C. Kim, “Distributed active decoupling capacitors for on-chip supply noise cancellation in digital VLSI circuits,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 216–217, Jun. 2006.

[10] J. Xu, P. Hazucha, M. Huang, et al., “On-die supply-resonance suppression using band-limited active damping,” IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 286–603, Feb. 2007.

[11] J. Gu, H. Eom, and C. H. Kim, “On-chip supply noise regulation using a low power digital switched decoupling capacitor circuit,” IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 6, pp. 1765–1775, Jun. 2009.

[12] D. Jiao, B. Kim, and C. H. Kim, "Design, Modeling, and Test of a Programmable Adaptive Phase-Shifting PLL for Enhancing Clock Data Compensation," IEEE Journal of Solid-State Circuits (JSSC), vol. 47, no. 10, pp. 2505–2516, Oct. 2012.

[13] N. Kurd, P. Mosalikanti, M. Neidengard, et al., “Next generation Intel® core™ micro-architecture (Nehalem) clocking,” IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1121-1129, Apr. 2009.

[14] D. Jiao and C. H. Kim, “A Programmable Phase-Shifting PLL for Clock Data Compensation under Resonant Supply Noise,” IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 272-274, Feb. 2011.

[15] T. Rahal-Arabi, G. Taylor, M. Ma, et al., "Design and Validation of the Pentium III and Pentium 4 Processors Power Delivery," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 220-223, Jun. 2002.

[16] B. Kim, W. Xu, and C. H. Kim, "A 32nm, 0.9V Supply-Noise Sensitivity Tracking PLL for Improved Clock Data Compensation Featuring a Deep Trench Capacitor Based Loop Filter," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. C162-C163, Jun. 2013.

[17] J. Tschanz, K. Bowman, S. Walstra, M. Agostinelli, T. Karnik, V. De, "Tunable Replica Circuits and Adaptive Voltage-Frequency Techniques for Dynamic Voltage, Temperature, and Aging Variation Tolerance," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 112-113, Jun. 2009.

[18] N. Butt, K. Mcstay, A. Cestero, et al., " A 0.039um2 High Performance eDRAM Cell based on 32nm High-K/Metal SOI Technology," IEEE International Electron Devices Meeting (IEDM) Technical Digest, pp. 27.5.1-4, Dec. 2010.

[19] J. Craninckx and M. Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer," IEEE Journal of Solid-State Circuits (JSSC), vol. 33, no. 12, pp. 2054-2065, Dec. 1998.

[20] M. Yip, A. P. Chandrakasan, "A Resolution-Reconfigurable 5-to-10b 0.4-to-1V Power Scalable SAR ADC," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 190-191, February 2011.

[21] P. Harpe, Y. Zhang, G. Dolmans, K. Philips, H. D. Groot, "A 7-to-10b 0-to-40MS/s Flexible SAR ADC with 6.5-to-16fJ/conversion-step," IEEE International

Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 472-473, February 2012.

[22] R. Harrison, P. Watkins, R. Kier, R. Lovejoy, D. Black, R. Normann, F. Solzbacher, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 554-555, February 2006.

[23] M. Chae, W. Liu, Z. Yang, T. Chen, J. Kim, M. Sivaprakasam, M. Yuce, "A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 554-555, February 2006.

[24] X. Zou, X. Xu, L. Yao, Y. Lian, "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 4, pp. 1067-1077, Apr. 2009.

[25] J. Kim, W. Yu, H. Yu, S. Cho, "A Digital-Intensive Receiver Front-End Using VCO-Based ADC with an Embedded 2nd-Order Anti-Aliasing Sinc Filter in 90nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 176-177, February 2011.

[26] M. Park, M. Perrot, "A 0.13μm CMOS 78dB SNDR 87mW 20MHz BW CT ΔΣ ADC with VCO-Based Integrator and Quantizer," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 170-171, February 2009.

[27] R. Muller, S. Gambini, J. Rabaey, “A 0.013mm2 5μW DC-Coupled Neural Signal Acquisition IC with 0.5V Supply,” IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 302-303, February 2011.

[28] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, P. Hanumolu, “A 16mW 78dB-SNDR 10MHz-BW CT-ΔΣ ADC Using Residue-Cancelling VCO-Based Quantizer,” IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 152-153, February 2012.

[29] M. Park, M. Perrot, “A 78dB SNDR 87mW 20MHz Bandwidth Continuous-Time ΔΣ ADC with VCO-Based Integrator and Quantizer Implemented in 0.13μm CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 12, pp. 3344-3358, December 2009.

[30] T. Kim, R. Persaud, C. H. Kim, “Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 122-123, June 2007.

[31] J. Daniels, W. Dehaene, M. Steyaert, A. Wiesbauer, “A 0.02mm2 65nm CMOS 30MHz BW All-Digital Differential VCO-based ADC with 64dB SNDR,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 155-156, June 2010.

[32] J. Lee, S. Park, J. Kang, J. Seo, J. Anders, M. Flynn, “A 2.5mW 80dB DR 36dB SNDR 22MS/s Logarithmic Pipeline ADC,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 194-195, June 2007.

[33] B. Hershberg, S. Weaver, K. Sobue, S. Takeuchi, K. Hamashita, U. Moon, “A 61.5dB SNDR Pipelined ADC Using Simple Highly-Scalable Ring Amplifiers,”

Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 32-33, June 2012.

[34] B. Kim, W. Xu, C. H. Kim, "A Fully-Digital Beat-Frequency Based ADC Achieving 39dB SNDR for a 1.6mVpp Input Signal," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, September 2013.

[35] M. Straayer, M. Perrot, "A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 4, pp. 805-814, April 2008.

[36] S. Rao, B. Young, A. Elshazly, W. Yin, N. Sasidhar, P. Hanumolu, "A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 270-271, June 2011.

[37] K. Reddy, S. Rao, R. Inti, B. Young, A. Elshazly, M. Talegaonkar, P. Hanumolu, "A 16-mW 78-dB SNDR 10-MHz BW CT ΔΣ ADC Using Residue-Cancelling VCO-Based Quantizer," IEEE Journal of Solid-State Circuits (JSSC), vol. 47, no. 12, pp. 1-12, December 2012.

[38] M. Straayer, M. Perrot, "A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based Quantizer and DEM circuit in 0.13u CMOS," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 246-247, June 2007.

[39] R. Staszewski, K. Muhammad, D. Leipold, C. Hung, Y. Ho, J. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. Eliezer, E. de-Obaldia, P.

Balsara, “All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 39, no. 12, pp. 2278-2291, December 2004.

[40] D. Kim, H. Song, T. Kim, S. Kim, D. Jeong, “A 0.3–1.4 GHz All-Digital Fractional-N PLL With Adaptive Loop Gain Controller,” IEEE Journal of Solid-State Circuits (JSSC), vol. 45, no. 11, pp. 2300-2311, November 2010.

[41] M. Lee, M. Heidari, A. Abidi, “A Low-Noise Wideband Digital Phase-Locked Loop Based on a Coarse–Fine Time-to-Digital Converter With Subpicosecond Resolution,” IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 10, pp. 2808-2816, October 2009.

[42] J. Borremans, K. Vengattaramane, V. Giannini, B. Debaillie, W. Thillo, J. Craninckx, “A 86 MHz–12 GHz Digital-Intensive PLL for Software-Defined Radios, Using a 6 fJ/Step TDC in 40 nm Digital CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 42, no. 10, pp. 2116-2129, October 2010.

[43] L. Vercesi, L. Fanori, F. Bernardinis, A. Liscidini, R. Castello, “A Dither-Less All Digital PLL for Cellular Transmitters,” IEEE Journal of Solid-State Circuits (JSSC), vol. 47, no. 8, pp. 1908-1920, August 2012.

[44] M. Lee, A. Abidi, “A 9 b, 1.25 ps Resolution Coarse–Fine Time-to-Digital Converter in 90 nm CMOS that Amplifies a Time Residue,” IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 4, pp. 769-777, April 2008.

[45] K. Kim, Y. Kim, W. Yu, S. Cho, “A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier,” IEEE Journal of Solid-State Circuits (JSSC), vol. 48, no. 4, pp. 1009-1017, April 2013.

[46] Y. Seo, J. Kim, H. Park, J. Sim, “A 0.63ps Resolution, 11b Pipeline TDC in 0.13μm CMOS,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 152-153, June 2011.

[47] J. Kim, Y. Seo, Y. Suh, H. Park, J. Sim, “A 300-MS/s, 1.76-ps-Resolution, 10-b Asynchronous Pipelined Time-to-Digital Converter With on-Chip Digital Background Calibration in 0.13-μm CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 48, no. 2, pp. 516-526, February 2013.

[48] Y. Seo, J. Kim, H. Park, J. Sim, “A 1.25ps Resolution 8b Cyclic TDC in 0.13μm CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 47, no. 3, pp. 736-743, March 2012.

[49] S. Lee, Y. Seo, H. Park, J. Sim, “A 1 GHz ADPLLWith a 1.25 ps Minimum-Resolution Sub-Exponent TDC in 0.18μm CMOS,” IEEE Journal of Solid-State Circuits (JSSC), vol. 45, no. 12, pp. 2874-2881, December 2010.

[50] Y. Park, D. Wentzloff, “An All-Digital PLL Synthesized from a Digital Standard Cell Library in 65nm CMOS,” Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, September 2011.

[51] A. Elkholy, et al., “A 3.7mW 3MHz Bandwidth 4.5GHz Digital Fractional-N PLL with -106dBc/Hz In-band Noise using Time Amplifier Based TDC,” Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 1-2, June 2014.

[52] D. Jee, Y. Seo, H. Park, J. Sim, “A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping ΔΣ TDC,” IEEE Journal of Solid-State Circuits (JSSC), vol. 47, no. 4, pp. 875-883, April 2012.

[53] C. Hsu, M. Straayer, M. Perrot, "A Low-Noise Wide-BW 3.6-GHz Digital ΔΣ Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 12, pp. 2776-2786, December 2008.

[54] P. Dudek, S. Szczepanski, J. Hatfield, **"**A High-Resolution CMOS Time-to-Digital Converter Utilizing a Vernier Delay Line**,"** IEEE Journal of Solid-State Circuits (JSSC), vol. 35, no. 2, pp. 240-247, February 2000.

[55] J. Yu, F. Dai, R. Jaeger, "A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13µm CMOS Technology," IEEE Journal of Solid-State Circuits (JSSC), vol. 45, no. 4, pp. 830-842, April 2010.

[56] P. Lu, P. Andreani, A. Liscidini, "A 90nm CMOS Gated-Ring-Oscillator-Based Vernier Time-to-Digital Converter for DPLLs," Proceedings of IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 459-462, September 2011.

[57] A. Rylyakov, J. Tierno, H. Ainspan, J. Plouchart, J. Bulzacchelli, Z. Deniz, D. Friedman, "Bang-Bang Digital PLLs at 11 and 20GHz with sub-200fs Integrated Jitter for High-Speed Serial Communication Applications," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 94-95, February 2009.

[58] D. Tasca, M. Zanuso, G. Marzin, S. Levantino, C. Samori, A. Lacaita, "A 2.9-to-4.0GHz Fractional-N Digital PLL with Bang- Bang Phase Detector and 560fsrms Integrated Jitter at 4.5mW Power," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 88-89, February 2011.

[59] J. Tierno, A. Rylyakov, D. Friedman, "A Wide Power Supply Range, Wide Tuning Range, All Static CMOS All Digital PLL in 65 nm SOI," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 1, pp. 42-51, January 2008.

[60] J. Hong, S. Kim, J. Liu, N. Xing, T. Jang, J. Park, J. Kim, T. Kim, H. Park, "A 0.004mm2 250μW ΔΣ TDC with Time-Difference Accumulator and a 0.012mm^2 2.5mW Bang-Bang Digital PLL Using PRNG for Low-Power SoC Applications," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 240-241, February 2012.

[61] N. August, H. Lee, M. Vandepas, R. Parker, "A TDC-Less ADPLL with 200-to-3200MHz Range and 3mW Power Dissipation for Mobile SoC Clocking in 22nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 246-247, February 2012.

[62] X. Gao, E. Klumperink, M. Bohsali, B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by N^2," IEEE Journal of Solid-State Circuits (JSSC), vol. 44, no. 12, pp. 3253-3263, December 2009.

[63] X. Gao, E. Klumperink, G. Socci, M. Bohsali, B. Nauta, "A 2.2GHz Sub-Sampling PLL with 0.16psrms Jitter and -125dBc/Hz In-band Phase Noise at 700μW Loop-Components Power," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp.139-140, June 2014.

[64] P. Huang, W. Chang, T. Lee, "A 2.3GHz Fractional-N Dividerless Phase-Locked Loop with -112dBc/Hz In-Band Phase Noise," IEEE International Solid-

State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 362-363, February 2014.

[65] Z. Ru, P. Geraedts, E. Klumperink, X. He, B. Nauta, "A 12GHz 210fs 6mW Digital PLL with Sub-sampling Binary Phase Detector and Voltage-Time Modulated DCO," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. C194-C195, June 2013.

[66] V. Kratyuk, P. Hanumolu, K. Ok, K. Mayaram, U. Moon, "A Digital PLL with a Stochastic Time-to-Digital Converter," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 31-32, June 2006.

[67] J. Keane, X. Wang, D. Persaud, C. H. Kim, "An All-In-One Silicon Odometer for Separately Monitoring HCI, BTI, and TDDB," IEEE Journal of Solid-State Circuits (JSSC), vol. 45, no. 4, pp. 817-829, December 2009.

[68] J. Kim, R. Rao, J. Schaub, A. Ghosh, A. Bansal, K. Zhao, B. Linder, J. Stathis, "PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability," Symposium on VLSI Circuits (SOVC) Digest of Technical Papers, pp. 224-225, June 2011.

[69] P. Jain, A. Paul, X. Wang, C. H. Kim, "A 32nm SRAM Reliability Macro for Recovery Free Evaluation of NBTI and PBTI," IEEE International Electron Devices Meeting (IEDM) Technical Digest, pp. 9.7.1-4, Dec. 2012.

[70] X. Wang, W. Xu, C. H. Kim, "SRAM Read Performance Degradation under Asymmetric NBTI and PBTI Stress: Characterization Vehicle and Statistical Aging Data," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, September 2014.

[71] A. Rao, M. Mansour, G. Singh, C. Lim, R. Ahmed, D. Johnson, "A 4–6.4 GHz LC PLL With Adaptive Bandwidth Control for a Forwarded Clock Link," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 9, pp. 2099-2108, September 2008.

[72] C. Jeong, D. Choi, C. Yoo, "A Fast Automatic Frequency Calibration (AFC) Scheme for Phase-Locked Loop (PLL) Frequency Synthesizer," Proceedings of IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 583-586, June 2009.

[73] S. Tarng, J. Peng, T. Chueh, M. Kuo, "An Automatic Frequency Calibration Technique for Fractional-N Frequency Synthesizers," Proceedings of IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 154-157, September 2010.

[74] J. Shin, I. Seo, J. Kim, S. Yang, C. Kim, J. Park, H. Kim, M. Kwak, G. Hong, "A Low-Jitter Added SSCG with Seamless Phase Selection and Fast AFC for 3rd Generation Serial-ATA," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 409-412, September 2006.

[75] T. Kim, R. Persaud, C. H. Kim, "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," IEEE Journal of Solid-State Circuits (JSSC), vol. 43, no. 4, pp. 874-880, April 2008.

[76] B. Kim, S. Kundu, S. Ko, C. H. Kim, "A VCO-Based ADC Employing a Multi-Phase Noise-Shaping Beat Frequency Quantizer for Direct Sampling of Sub-1mV Input Signals," Proceedings of IEEE Custom Integrated Circuits Conference (CICC), pp. 1-4, September 2014.

[77] J. Liu, T. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, H. Park, "A 0.012mm2 3.1mW Bang-Bang Digital Fractional-N PLL with a Power-Supply-Noise Cancellation Technique and a Walking-One-Phase-Selection Fractional Frequency Divider," IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers, pp. 268-269, February 2014.

[78] J. Keane, W. Zhang, C. H. Kim, "An Array-Based Odometer System for Statistically Significant Circuit Aging Characterization," IEEE Journal of Solid-State Circuits (JSSC), vol. 46, no. 10, pp. 2374-2385, October 2011.

[79] X. Wang, Q. Tang, P. Jain, D. Jiao, C. H. Kim, "The Dependence of BTI and HCI-Induced Frequency Degradation on Interconnect Length and Its Circuit Level Implications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, pp. 1-12, 2014.

[80] Q. Tang, X. Wang, J. Keane, C. H. Kim, "RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit," Symposium on VLSI Technologies (SOVT) Digest of Technical Papers, pp. T188-T189, June 2013.