New Approaches for Printed Electronics Manufacturing

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Abstract

In printed electronics, electronic inks are patterned onto flexible substrates using roll-to-roll (R2R) compatible graphic printing methods. For applications where large-area, conformal electronics are necessary, printed electronics holds a competitive advantage over rigid, semiconductor circuitry, which does not scale efficiently to large areas. However, in order to fully realize the true potential of printed electronics, several manufacturing hurdles need to be overcome.

Firstly, minimum feature sizes produced by graphic printing methods are typically greater than 25 μm, which is at least an order of magnitude higher for dense, high-performing electronics. In this thesis, conductive features down to 1.5 μm are demonstrated using a novel inkjet printing-based process. Secondly, high-resolution printed conductors usually have poor current-carrying capacity, especially for longer wires in large-area applications. This thesis explores the fundamentals of aerosol-jet printing and reveals the regime for printing high-resolution lines with excellent current carrying capacity. Additionally, a novel manufacturing process is demonstrated, which can process 2.5 μm wide conductive wires with linear resistances as small as 5 $\Omega\ mm^{-1}$.

Another challenge for printed electronics manufacturing is to deal with topography produced on the substrate surface by printed features. Besides complicating the subsequent use of contact-printing methods, surface topography is a source of poor device yields as well. This thesis describes two novel methodologies of creating topography-free printed surfaces. In the first method, nanometer-level smooth, planarized

silver lines are obtained using a transfer printing approach. In the second method, open microchannels, imprinted in plastic substrates, are filled with a controlled amount of metal using liquid-based additive processes, to obtain conductive wires flush with the substrate surface.

Finally, this thesis addresses the issue of overlay alignment, which is the most significant challenge of printed electronics manufacturing. Multi-layered electronic devices require alignment of multiple layers of different materials with micron-level tolerances, which is a daunting task to accomplish on deformable, moving substrates in R2R production formats. This thesis describes a novel, self-aligned manufacturing strategy for printed electronics that relies on capillary flow of inkjet-printed inks within open micro-channels. Multi-level trench networks, pre-engineered on the substrate surface, are sequentially filled with different inks which, upon drying, form stacked layers of electronic materials. Using this approach, fully self-aligned fabrication of all the major building blocks of an integrated circuit is demonstrated. Overall, this thesis presents several new manufacturing avenues for realizing high-performing and dense electronics on plastic by R2R processing.

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Chapter 1 Introduction

1.1 Motivation

Integration of electronics into flexible and large-area formats promises to deliver novel functional capabilities in areas related to distributed-sensing, information display, identification tagging, health diagnostics and human-machine interfacing.[1-3] Envisioned applications of flexible electronics include roll-up displays,[4] wearable energy-harvesting systems,[5] electronic sensors for robots (e-skins),[6] biological sensors (bionic ears),[7] etc. For decades, silicon has played a key role in electronic device manufacturing, both as a substrate and semiconductor. However, silicon devices are rigid and brittle, and are processed by a combination of processing steps which involve masking, etching, evaporation, and deposition of materials under high vacuum and at high temperatures. This costly, time-consuming and complex manufacturing paradigm is not readily

adaptable to high-speed, large-area processing on inexpensive flexible substrates such as plastic or paper. In light of the well-recognized potential of flexible electronics, the immediate challenge is to develop robust manufacturing platforms that can truly deliver dense, high-performing circuitry on flexible substrates with the desired cost and area scaling.

Printed electronics is a disruptive technology that deals with laying down electronic circuits on large-area, flexible substrates using low-temperature, liquid-phase processes.[8]The primary goal of printed electronics is to create structures that are functionally similar to conventional electronics but at a far greater production speed, lower cost and with less manufacturing complexity. In printed electronics, electronic inks are patterned onto flexible substrates using graphic arts printing methods, such as inkjet, flexographic, gravure, and screen printing, which are traditionally used for everyday items such as books, packaging, and newspapers.[9-11] Metallic, semiconducting and insulating liquid inks are selectively applied to moving, flexible substrates, which, upon drying, form functional films. Liquid-based processing offers the potential for high-throughput roll-to-roll (R2R) manufacturing on large-area web substrates. In addition, printed electronics (like 3-D printing) is an additive technology, i.e. materials are deposited only where they are required. This eliminates material wastage associated with subtractive processes used in fabrication of silicon-based devices. It is important to note that the goal of printed electronics is not to compete with silicon technology; rather, the aim is to find applications, such as distributed sensors, where large area, conformal

electronics are necessary or provide a clear advantage, and where implementation with silicon circuits would be impossible or too costly.

Despite the promise, several manufacturing hurdles need to be overcome for realizing the true potential of printed electronics. Firstly, minimum feature sizes processed by graphic printing presses are typically limited to 25 μm, which is at least an order of magnitude higher than required for high-performance electronics applications. Secondly, aspect ratio (height/width) of printed conductors is generally low (< 0.01), which limits their current-carrying capacity over long distances. Moreover, printed conductors, owing to their inherent non-uniformities, create undesirable topological features on the substrate surface, which complicates subsequent device processing. Further, devices are built from a variety of materials and, therefore, printing processes should allow for printing of inks with a range of properties. Unlike the graphics printing industry, where precise layer to layer registration are not crucial, multi-layered electronic devices demand excellent control over the feature size and placement. A central challenge, therefore, is to align multiple layers of different materials with micron level tolerances (or better!). The precision alignment mechanisms typical of wafer-based semiconductor fabrication facilities are generally not available for web-handling equipment and it is a daunting proposition to think about how microscale devices can be fabricated on moving webs.

The central goal of this thesis is to address the major challenges of printed electronics manufacturing. This thesis describes the development of several novel strategies specifically aimed at (i) simultaneous improvement in resolution and current-carrying capacity of printed conductors, (ii) creating smooth, topography-free printed

surfaces, and (iii) finding solutions to the issue of *overlay alignment* or registration in R2R manufacturing systems.

1.2 Thesis Outline

Chapter 2 highlights some of the potential applications of printed electronics. It provides a brief overview of printing technologies, and delves into device fundamentals while elucidating specific demands on printing processes. In Chapter 3, the major challenges of printed electronics manufacturing are discussed in detail. The current state-of-the-art resolution and aspect ratio of printed conductors are described. The problem of roughness and surface topography of printed features is highlighted. Also, the critical challenge of materials registration in R2R printed electronic is discussed, and prior work in the literature aimed at addressing this issue is summarized.

Chapter 4 explores the fundamental physics that governs a recently developed printing method, called aerosol jet printing. Aerosol jet printing requires control of a number of process parameters, including the flow rate of the carrier gas that transports the aerosol mist to the substrate, the flow rate of the sheath gas that collimates the aerosol into a narrow beam, and the speed of the stage that transports the substrate beneath the beam. In this Chapter, the influence of process parameters on the geometry of aerosol-jet printed silver lines is studied with the aim of creating high resolution conductive lines of high current carrying capacity. A systematic study of process conditions revealed a key parameter: the ratio of the sheath gas flow rate to the carrier gas flow rate, defined here as the focusing ratio. Line width decreases with increasing the focusing ratio and stage

speed. Simultaneously, the thickness increases with increasing the focusing ratio but decreases with increasing stage speed. Geometry control also influences the resistance per unit length and single pass printing of low resistance silver lines is demonstrated. The results are used to develop an operability window and locate the regime for printing tall and narrow silver lines in a single pass.

Chapters 5 and 6 describe two novel methodologies of creating topography-free printed surfaces. Surface topography, courtesy of the printed electronics, is not ideal for device processing. In Chapter 5, a simple and scalable method for creating flexible substrates with embedded, printed silver lines is described. In a sequential process, aerosol-jet printed silver lines are transferred from a donor substrate to a thin reactive polymer coating on a receptor substrate. The embedded conductors are analyzed for their planarization and smoothness by scanning electron and atomic force microscopy. Results of electrical measurements quantifying the transfer yield of the conductors are described. Root mean square roughness of the embedded wires was found to be less than 10 nm; an order of magnitude lower than their as-printed form.

In Chapter 6, a novel process for fabricating high-resolution, high-aspect ratio metal wires embedded in a plastic substrate is described. In a sequential process, high-resolution channels connected to low-resolution reservoirs are first created in thermosetting polymer by imprint lithography. A reactive Ag ink is then inkjet-printed into the reservoirs and wicked into the channels by capillary forces. These features serve as a seed layer for copper deposition inside the channels via electroless plating. Fundamentals of capillary flow and drying of reactive silver inks in open microchannels

are explored. Time-resolved growth of copper inside printed microchannels is demonstrated. Highly conductive wires (> 50% bulk metal) with minimum line width and spacing of 2 and 4 μm, respectively, and an aspect ratio of 0.6 are obtained.

Chapter 7 aims to address the most significant problem of printed electronics manufacturing- alignment of multiple layers of disparate materials with micron-level tolerances on deformable, moving substrates. In this Chapter, a novel manufacturing approach, called self-aligned capillarity assisted lithography for electronics (SCALE), is introduced that that allows precision patterning of multilayered electronic devices by inkjet printing on micro-imprinted plastic substrates. Materials registration is achieved automatically by sequential deposition of liquid inks into multi-level trench networks on the substrate surface using capillary forces. A series of complex, multi-tier capillary networks are described, with the aim of fully self-aligned fabrication of all the major building blocks of an integrated circuit, including resistors, capacitors, transistors, and crossovers.

Chapter 8 discusses the ongoing and future endeavors for processing high-speed printed transistors. With the aim of reducing parasitic capacitances, ongoing efforts involve development of new transistor architectures using the SCALE process. In particular, aligned-gate transistors, and nanoscale transistors are key focus areas. Possibilities of creating single-crystal, aligned organic semiconductors using the SCALE process are also discussed.

Chapter 2 Printed Electronics

2.1 Printed Electronics Applications

RFID Tags

Item-level RFID (radio frequency identification) tags are considered as potential replacements for the ubiquitous UPC (universal product code) barcode.[12] Deployment of item-level RFID tags can automate inventory control and price updating in supermarkets, and considerably expedite the checkout process, e.g. customers can simply walk through an electronic counter instead of individually scanning all the items. However, several models have shown that in order to be economically viable, each tag must cost less than a cent.[2, 13, 14]

An RFID tag primarily consists of an antenna for receiving and transmitting the signal, and an integrated circuit for modulating RF signal, supplying DC power, and storing and processing information. Currently, the specialized functions of the integrated

circuit are achieved by attaching a silicon chip to an external antenna on a paper or plastic substrate using a pick-and-place approach. However, this manufacturing strategy is cost-intensive and low-throughput. An all-printed integrated circuit technology can potentially cut down the manufacturing cost to below 1 cent per tag.

An attractive feature of RFID tags is that no external power source is required to drive the circuit inside the tag, i.e., the tag derives energy from the readout device itself. For item level RFID tags, typical read-out requirements are less than 1 meter. The carrier frequency of the RFID system, as regulated by Federal Communications Commission (FCC), is allowed in the following four communication bands: 2.4 GHz, 900 MHz, 13.56 MHz and 135 kHz.[9] For distances in the range of one meter, low operation frequencies (135 kHz and 13.56 MHz) work well because power can be supplied to the tag using inductive coupling. However, a drawback of 135 kHz is that it requires a large antenna area, which increases the footprint of the tag. Higher frequencies (2.4 GHz and 900 MHz) produce far-field coupling as well, which can potentially cause accidental readouts at multiple checkout counters. Therefore, 13.56 MHz is the ideal frequency for item-level RFID applications. The internal circuit of an RFID tag consists of multitude of devices such as inductors, capacitors, diodes, and transistors. It is mandatory that each of these devices operate at 13.56 MHz. MHz-class printed circuitry seemed unlikely a decade ago, but recent developments in high-performance electronic inks[15-17] have opened up possibilities of all-printed RFID tags. In fact, an all-printed RFID tag has already been demonstrated, with an estimated cost of 3 cents per tag.[18]

Sensors for Internet of Things

The Internet of Things (IoT) concept is an ecosystem of connected, smart devices within the existing framework of the Internet.[19] IoT promises advanced connectivity of devices, systems, and services to bring automation to nearly every field of life. Under the IoT concept, everyday physical items are provided with local intelligence and connectivity to the cyberspace through the Internet. For example, consider a 'smart' refrigerator that keeps track of the availability and expiry date of food items and automatically places an order at the nearby grocery shop if the food supply is below a certain limit.

At the heart of IoT are sensors, which are embedded into physical objects with the ability to communicate with each other. A smart sensor, however, is an elaborate system in itself. Typically, it consists of a sensing element that responds to an external stimulus such as temperature, pressure, or light. Based on its internal configuration, the sensing element may respond to the stimulus by outputting a current or voltage change. This serves as an input for the logic circuitry, also embedded on the sensor, which performs the necessary computation and processing. The processed data is temporarily stored on a memory device or broadcasted onto an antenna. This antenna can then communicate with a cellphone by a communication protocol, e.g. NFC (Near Field Communication) or RFID. The cell phone, in turn, serves as a gateway to the Internet or the "cloud" which connects it to other devices.

The key challenge in sensor fabrication is that discrete functionalities, i.e., sensing, computation, data storage and broadcasting, need to be integrated on the same

platform. One manufacturing strategy could be to bond silicon chips to the sensing elements on flexible strips. However, given the fact that trillions of sensors are required to power tomorrow's IoT, this pick-and-place paradigm may not be a scalable approach. High-speed printing methods not only give the desired throughputs, they also offer very easy integration of different materials on the same substrate.. Therefore, from the perspective of printed electronics, IoT offers a unique opportunity; for applications requiring large-scale integration of multiple, potentially incompatible materials on the same substrate.

Flexible Displays

All display technologies have an active matrix (AM) thin film transistor (TFT) array in common, which acts as a backplane to precisely control the display media.[1] The backplane comprises of a pixel grid, where each pixel is driven by TFTs and capacitors. The gate of the TFT is connected to the horizontal scan line that turns on the TFTs row-by-row, while the drain is connected to the vertical data line that supplies the voltage to charge or discharge the capacitor. The voltage stored in the capacitor is used to control the brightness or grayscale of the pixel. Liquid crystal displays are backlit, therefore, a portion of incoming light is blocked by opaque metal layers used for scan and data lines, TFTs, and capacitors. A high aperture ratio, a ratio of the transparent area to the total area of a pixel, is required to maximize the brightness and contrast.

Currently, all display backplanes processed using high-temperature (>1000 °C) and vacuum-deposition methods on glass or silicon substrates. However, these manufacturing processes are not extendable to plastic substrates for flexible display

applications. Using high-speed, low-temperature printing processes, large-area flexible or roll-able displays can be processed on plastic substrates at lower costs. However, with the aim of maximizing aperture ratio, scaling down of the device footprint while maintaining the same current levels is essential. It is worthwhile noting that, unlike the printed RFID application, which requires MHz-class printed transistors, display applications only require an operation speed of 10-100 KHz.[9]

2.2. Review of Printing Technologies

Gravure Printing

Gravure printing is often used commercially to produce high-quality graphic materials, for example, magazines.[20] In gravure printing, an engraved metallic cylinder containing the geometrical information of the print pattern is created by laser engraving or chemical etching. As shown in Figure 2.1, the engraved cylinder is inked by dipping it into an ink tray, and excess ink is removed from the cylinder surface using a doctor blade. The cylinder is brought in contact with a moving substrate at high pressure where transfer of liquid inks from the gravure cells to the substrate occurs. The width and thickness of the printed dots depends on the fraction of the ink transferred and wetting characteristics of the ink on the substrate.[20-22] For high ink transfer, a high print pressure and low viscosity (10-100 mPa s) is preferred.[22] Merging of the individual printed dots to form continuous features can occur depending on the ratio of cell width to cell spacing on the engraved cylinder. Key benefits of gravure technique include longer lifetime of metallic cylinders, and high print resolution (~10-20 μm). However, the metal cylinders are expensive to fabricate in the first place. Also, the doctoring step leaves behind

undesirable residue on the cylinder surface which affects the print quality. Merging of individual printed dots to make continuous features can have a negative impact on line consistency, especially for very-high resolution gravure printing (< 10 μm). In addition, the high print pressures exclude the possibility of printing on substrates pre-patterned with soft materials.

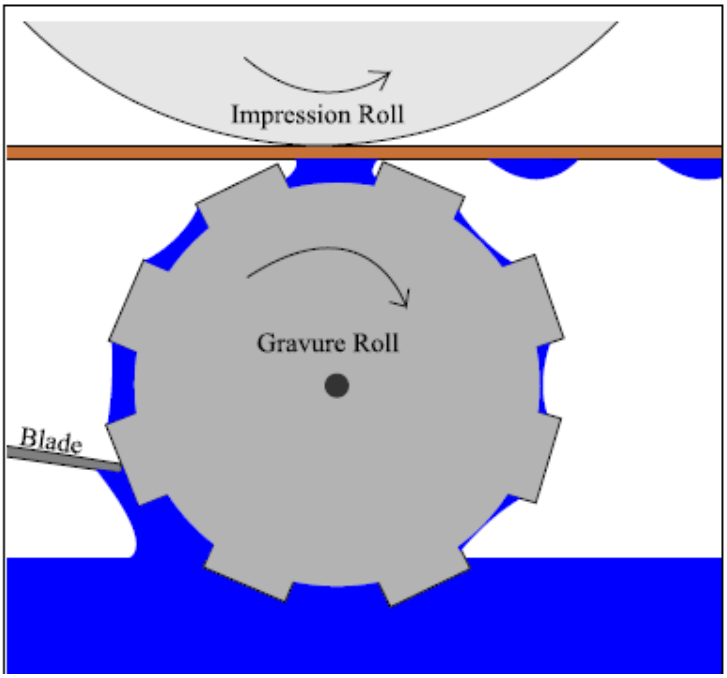

Figure 2.1 Schematic of the gravure printing process.

Flexographic Printing

In flexographic printing, printed features are produced from raised elements on a plate cylinder.[21,22] The elastic printing plates are typically patterned by photolithography, laser engraving or micromolding from a metallic plate. First, the ink is transferred from a fountain roll to an anilox cylinder, which has homogeneously distributed, small engraved cells designed to hold a specific amount of ink (Figure 2.2). The raised surface of the printing roll is inked by direct contact with the anilox cylinder

surface which evenly transfers a controlled amount of ink with uniform thickness. Images can be transferred to any kind of substrate at relatively mild print pressures, and therefore flexography is less destructive than gravure printing. The desired ink viscosity is low (<500 mPa s), which is beneficial for printing low-viscosity semiconductor inks. Importantly, continuous and arbitrarily-shaped features are directly printed onto the substrate as opposed to relying on merging of discrete dots in gravure printing. However, flexographic printing is generally low-resolution (50-75 μm)[50] due to the distortion of the elastic printing plate in contact with the substrate. Also, the ink gets squeezed between the plate and the substrate leading to thicker deposits near the edges. Furthermore, the solvent of the ink can potentially cause swelling of the printing plate which can degrade the print quality over time.

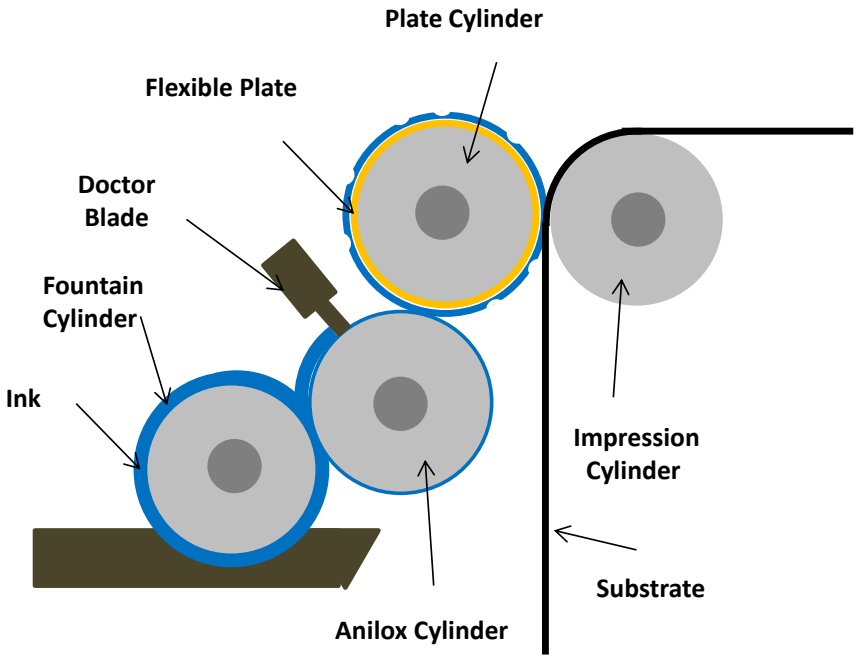

Figure 2.2 Schematic of the flexographic printing process.

Offset Printing

Offset printing is based on the difference of surface energy on the plate cylinder.[25] The surface energy contrast is typically created using photolithography. The non-image area is first wetted by water and then the ink sticks to the image area. Unlike flexography, no relief features are required in offset printing. The ink is then transferred to an intermediate offset cylinder and subsequently printed on to the final substrate at a relatively high nip pressure. High-print resolution can be obtained using this technique, but the presence of water is a limiting factor for printed electronics applications.

Screen Printing

In screen printing, a layer of ink is pushed through the openings of the screen onto the substrate. The screen is typically made of a porous mesh support, from materials like polyester or stainless steel. The screen support allows the use of areas which are not connected, which would otherwise fall through a regular stencil or mask. The mesh is coated with a light-sensitive emulsion that blocks out the individual holes in the mesh. The desired print pattern is printed on a transparent film and placed tightly between the emulsion-coated mesh and a light source. The unexposed emulsion is washed away whereas the exposed emulsion hardens and stays, completing the screen fabrication process. The screen is placed on top of the substrate and an ink is pushed along the surface of the screen using a squeegee. The mesh density and ink properties are critical in determining the print resolution and thickness. Screen printing is often used as a sheet-to-sheet process, but is also adaptable to a R2R process, as in rotary screen printing.

In rotary screen printing, a cylindrical screen is employed that rotates in a fixed position. The substrate moves at a constant speed between the screen and an impression roller. Care is taken so that the angular velocity of the screen matches with substrate speed. The squeegee is situated inside the screen with its edge making contact with the screen's inside surface precisely at the point where the screen, substrate, and impression roller come together. Ink is supplied to the center of the screen and collects underneath the squeegee and the screen's interior surface. The motion of the screen causes this bead of ink to roll, which forces the ink into stencil openings, essentially flooding the screen. The squeegee then shears the ink as the screen and substrate come into contact, allowing the ink to transfer to the substrate.

Inkjet Printing

Inkjet printing is a digital patterning technique, where the print pattern can be altered *on the fly*. Compared to the mass printing techniques discussed above, inkjet printing is non-contact and requires considerably smaller ink volumes. Digital mastering reduces processing costs and allows rapid changes to the design.

Commercial inkjet printers are mainly of two types: thermal bubble jets and piezoelectric jets. A thermal-bubble jet nozzle consists of an ink reservoir and a heating element. Current is passed through the heating element to vaporize the ink inside the reservoir. A bubble is formed and it expands to create a pressure wave to eject an ink droplet. For piezoelectric jets, a piezoelectric element is used as an actuator inside the ink nozzle. As shown in Figure 2.3, a voltage pulse is applied to the piezoelectric plate to cause a deflection, creating an acoustic wave that propagates inside the nozzle to eject the

droplet. Thermal-bubble jets, although cheaper than piezoelectric jets, are not suited for printed electronics, as most electronic inks are not compatible with the repeated thermal cycles, e.g. metal nanoparticles may undergo sintering from the heat. Majority of the work reported in the literature on inkjet-printed electronics employs piezoelectric jets.

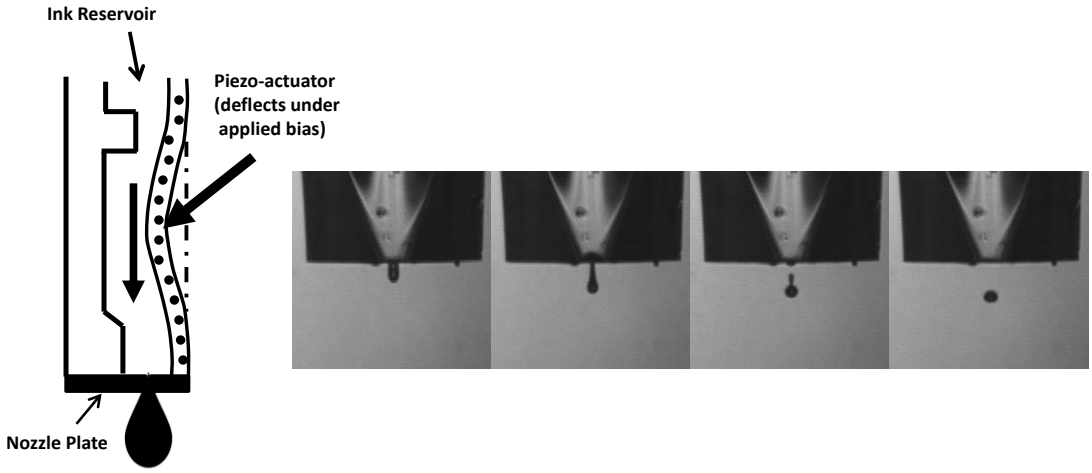

Figure 2.3 Working principle of piezoelectric jets. A voltage pulse is applied to a piezoelectric element to cause a deflection, creating an acoustic wave inside the nozzle that ejects an ink droplet (left). The drop forms from an initial liquid column that thins to form a leading droplet with an elongated tail or ligament. The ligament finally ruptures to form a single droplet (right).

The resolution of inkjet printing is primarily dictated by minimum droplet volume ejected by the nozzle. Typically, inkjet printed droplet volumes range from a few picoliters to tens of picoliters, corresponding to diameters between 10-60 μm. Upon impact with the substrate, the droplet spreads out depending on the wetting characteristics of the ink with the substrate. Line width as small as 25 μm can be achieved with inkjet printing.[23] Although Sekitani et al.[24] have demonstrated 2 μm Ag lines using sub-femtoliter inkjet-printed droplets, multiple passes were required to obtain the desired metal content in the wires.

Inkjet printing is R2R compatible, although the printing speed is slower than the mass printing methods. Also, the ink properties need to be tuned well to ensure stable printing over a long period of time. An ink with a viscosity of 10-12 cP and surface tension of 28-33 mN/m is recommended to obtain stable jetting.[25] Also, to prevent the clogging of the nozzle from the drying of the ink solvent near the nozzle tip, higher boiling point solvents are preferred.

One major problem with inkjet printing is the non-uniform drying of the printed films. Inkjet-printed patterns typically have a doughnut shaped cross-section[10] with increased height at the edges because of the coffee-stain effect.[26] During drying, rate of evaporation is faster at the edges due to curvature gradients and contact line pinning at the edge, which is compensated by the outward movement of the solute. The coffee stain effect is present in other printing methods as well, but is exceptionally pronounced in inkjet printing because of the low viscosity of the inks. One way of avoiding this problem is adding a high-boiling point, low-surface tension co-solvent to compensate the outward convective flow with inward Marangoni flow that is created by surface tension gradients. The drying history of the printed film is exceptionally critical in dictating the quality (e.g., crystal orientation) of small-molecule semiconductor films such as TIPS-pentacene.[27]

2.3 Device Fundamentals and Demands on Printing Processes

Transistors are the building blocks of flexible electronics circuitry. A transistor is a three-terminal device used to amplify and switch electronic signals. The current flow between two terminals is controlled by the magnitude of the electric field applied at the

third. A thin-film transistor (TFT) is a special kind of transistor made by depositing thin films of materials in a layered configuration.

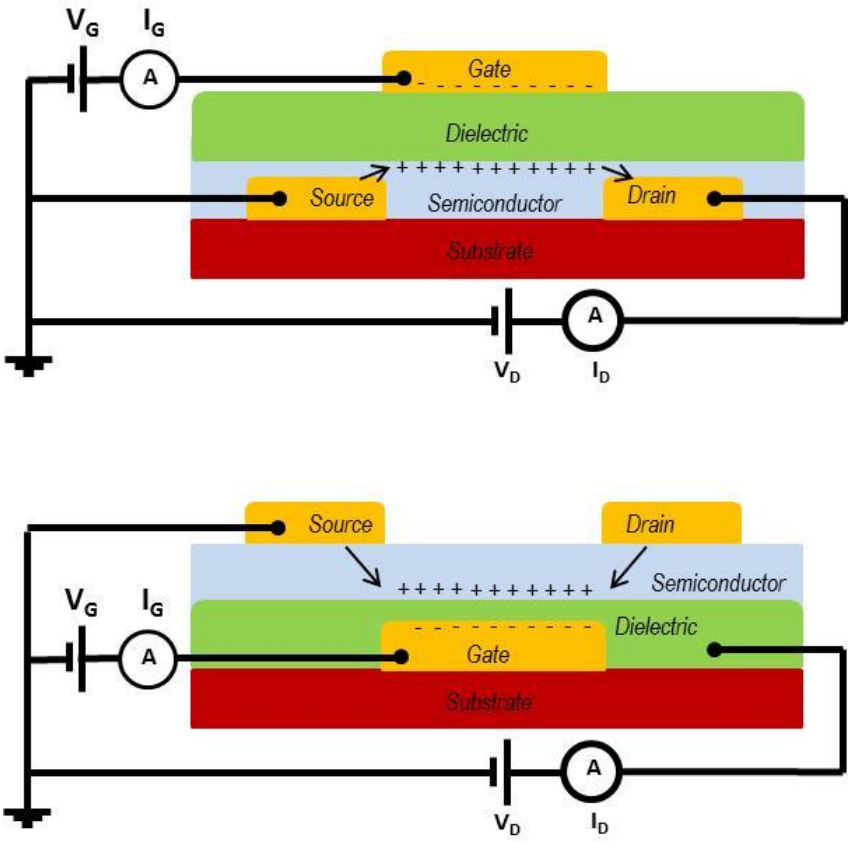

Figure 2.4 Architecture of thin film transistors: (above) bottom-contact, top gate and (below) top-contact, bottom gate.

The fundamental device components of a TFT are (i) three conducting electrodes, namely source, drain and gate contacts, (ii) the semiconductor layer, and (iii) the dielectric layer (insulators such as polymers or oxides) arranged in a certain configuration. TFTs can have several geometries; two of the most common geometries employed in printed TFTs- top contacts and bottom contacts are shown in Figure 2.4. The operation mechanisms are similar for both geometries, although the device performances may be different. All TFTs utilize a capacitively coupled gate dielectric layer to modulate

the current in the semiconductor layer. When a voltage bias is applied to the gate electrode, a conducting channel is formed by the accumulation of electrons or holes at the semiconductor-dielectric interface. This reduces the effective resistance of the path between the source and the drain, allowing the drain current to flow between the source and drain electrodes, if there is a source-drain bias applied between them. This is referred to as the ON state. In the absence of a gate voltage, the channel has high resistance and no current flows between the source and the drain. This is referred to as the OFF state. The transistor must produce enough ON current to activate or switch another part of a circuit, but it must not generate OFF currents that are large enough to cause unwanted switching. The magnitude of these ON and OFF currents and the time required to switch between these two states determine the utility of the transistor in integrated circuits.

The basic equation describing the TFT drain current (in the saturation regime) is

$$(I_{DS}) = (\frac{W}{2L})\ \mu C_i\ (V_{GS} - V_T)^2 \qquad (2.1)$$

where I_{DS} is the drain current in the saturation regime, μ is the field effect mobility of the semiconductor, W the channel width, L the channel length, C_i is the capacitance per unit area of the dielectric, V_T the threshold voltage, and V_{GS} the gate voltage. Mobility (measured in $cm^2V^{-1}s^{-1}$) is a measure of how easily charge carriers (i.e. electrons or holes) move within the semiconductor when subjected to an electric field. Threshold voltage, in simple words, is approximately the gate voltage at which there is a rapid increase in the source-drain current.

For printed transistors to be competitive with the polycrystalline or amorphous silicon transistors both in terms of cost and performance, a diverse suite of materials is

required; including high conductivity metals for electrodes and interconnects, high-capacitance/low-leakage gate dielectrics, and high-mobility n-type and p-type semiconductors. Besides, serious patterning challenges in large scale, continuous TFT fabrication need to be addressed, which makes it an intriguing problem for materials science and process engineering.

The most basic component of an integrated circuit is the wire or conductor, which acts as a conduit for current. Wires are an integral part of all devices. Moreover, interconnections between devices and other components are accomplished through wires. In light of dense, large-area applications, wires require both narrow line widths for high density circuitry, and sufficient thickness for high current carrying capacity over long distances. Therefore, a goal for printing conductive networks is to create lines with high resolution (low line width) and high aspect ratio, where aspect ratio is defined as the ratio of height to the width of the lines. Also, the ability to print two narrowly spaced lines is extremely important, especially in TFTs. The distance between the source and the drain electrodes, called the channel length (L) controls the maximum switching frequency, $f \propto \mu/L^2$, device integration density, $N \propto 1/L^2$, and is related to the drain current, $I_D \propto \mu/L$.[1] High precision is also required in printing the gate electrode; ensuring minimal overlap with the source and the drain to minimize parasitic capacitances.[28] The strict alignment requirement of the gate electrode to the source-drain channel is especially a serious manufacturing challenge for printed electronics.

The crucial parameter for a dielectric is capacitance per unit area C_i,

$$C_i = \varepsilon_o \frac{k}{d} \qquad (2.2)$$

where ε_o the permittivity of vacuum, k is the dielectric constant of the material and *d* is the thickness of the film. Thus, the capacitance value is governed not only by intrinsic material properties (*k*), but by the printing process (*d*) as well. Uniformity of the dielectric films is crucial for transistor performance. Insulating polymers, oxides or organic-inorganic hybrid materials are typically employed as dielectric films in printed TFTs.[29] Variation in film thickness is detrimental as it leads to non-uniform electric field experienced at the gate-dielectric interface. Thinner areas may also lead to dielectric breakdown. Dielectric breakdown occurs when the electric field across a dielectric layer is strong enough to force electron transfer through the material. Defects such as pinholes or cracks provide potential paths for leakage. Cracks can form due to shrinkage of the dielectric layer during curing or drying. Pinholes may form due to a bubble of entrapped gas that ruptures after the film is set. A smooth gate dielectric surface is also essential as it enhances the ordering of the organic semiconductor molecules near the interface.[30]

From Equation (2.1), it is evident that a viable approach for substantially increasing the drain current while operating at low biases would be to increase the capacitance of the gate dielectric. Therefore, thin dielectric layers are preferred as they give higher capacitance for a given material. However, too thin dielectric results in higher leakage currents or may increase the likelihood of direct shorts. Although thicker dielectrics cause an undesired rise in operating voltage, they help suppress the formation of pinholes and the problems associated with step coverage. Therefore, the printing process should provide excellent control over film thickness and uniformity.

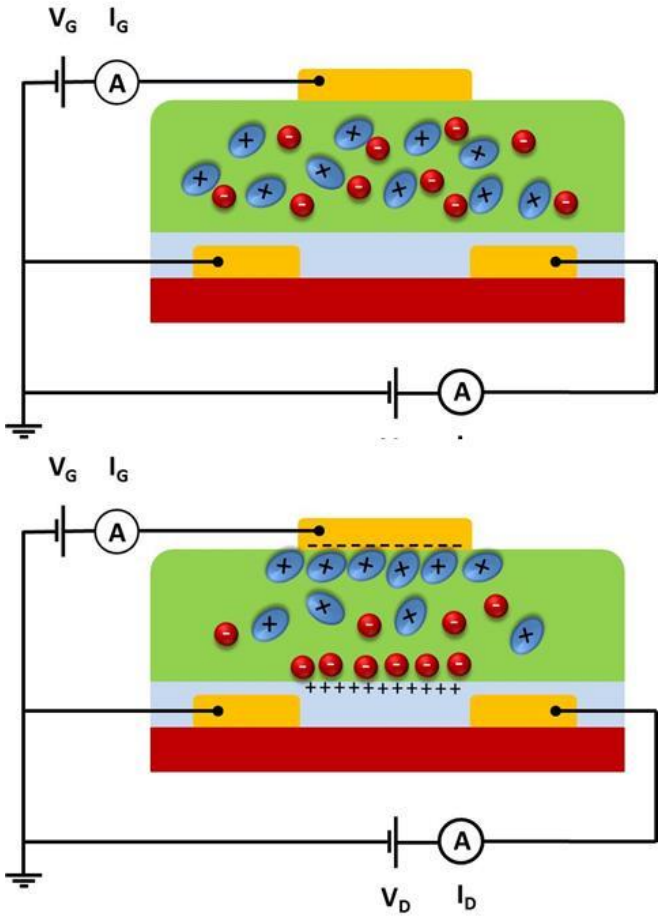

Figure 2.5 Electrolyte-gated transistors. Upon application of a gate bias, ions migrate to the two interfaces to form electrical double layers. Gate potential is dropped across the double layers and there is little potential drop in the bulk of the electrolyte.

An alternate to polymeric or oxide dielectrics are electrolytes, which are ionically conducting but electronically insulating.[31] When an electrolyte is employed as a gate dielectric layer in a TFT, and a gate bias is applied to the gate electrode, the ions in the electrolyte migrate towards the gate/electrolyte and electrolyte/semiconductor interfaces (Figure 2.5). If the semiconductor layer is ion-impermeable, a Helmholtz layer is formed by the ions on the electrolyte side of the interface, and charge carriers accumulate on the semiconductor side, together forming an electric double layer. The thickness of this

double layer is usually around 1 nm, therefore it has a much larger capacitance (on the order of 10 $\mu F/cm^2$) than traditional dielectrics. Another electrical double layer is also formed at the gate/electrolyte interface. Both the double layers contribute to the total capacitance according to the rule of capacitors in series (i.e., $1/C=1/C_1+1/C_2$). Unlike conventional dielectrics, nearly all the applied gate potential is dropped across the double layers and there is little potential drop in the bulk of the electrolyte. Therefore, the polarization of the electrolyte produces a large electric field at the semiconductor interface that in turn causes charge carrier accumulation at very low gate voltages (<2V). On the other hand, with ion permeable semiconductors, such as polymers, the ions migrate into the semiconductor layer. By chemically reacting with semiconductor, ions induce charge carriers in the semiconductor layer. Effectively, the ion penetration produces a three-dimensional channel whose current depends on the doping level, which is also controlled by the gate voltage.

Solid-state electrolytes made by dissolving inorganic salts in soft polymers, e.g. Li salt $LiClO_4$ dissolved in poly(ethylene) oxide (PEO) have been employed as high capacitance dielectrics.[32] However, the ionic conductivity of these materials is limited to only 10^{-5} to 10^{-4} S/cm at room temperature. Low ionic conductivities lead to increased polarization time, and therefore lower switching frequencies. Among the known electrolytes, ionic liquids exhibit the highest ionic conductivity reaching up to 10^{-2} S/cm. Ionic liquids are a type of organic salt which are liquid at room temperature. In order to make them compatible with practical electrical circuits, ionic liquids can be dissolved in small quantities of cross-linked polymers to form a gel-like material called ion gel.[33, 34]

For example, a common ionic liquid, [EMIM][TFSI] can be dissolved in a block-copolymer, PS-PMMA-PS at a weight fraction as low as 10%. The PS block is insoluble in the ionic liquid, whereas the PMMA block is soluble. This solubility contrast leads to the formation of a physical cross-linked network of the block-copolymer to lend mechanical integrity to the gel without compromising its ionic conductivity.

Ion gel films can be printed from an ion gel ink prepared by co-dissolving ionic liquid and block-copolymer in a common solvent. Unlike conventional dielectrics, where the operating voltage of the device scales inversely with the dielectric film thickness, operating voltages of the ion gel-gated transistors are independent of the gel thickness. Therefore, low voltage TFTs can be obtained even for fairly large thickness of the gel (1 μm or larger!). From a printing standpoint, this unique aspect of the ion gel dielectric is extremely favorable because it relaxes the requirement of strict thickness control for the dielectric film. However, polarization response time of the does depend on the gel thickness. The polarization time of electrolytes is described by the RC time constant, which is the product of the electrolyte ionic resistance (R in Ohms) and the double layer capacitance (C in Farads). With a film thickness of 1 μm, the calculated RC time constant is as small as 1 μs. This, in turn, implies that ion-gel gated TFTs can potentially operate as fast as 1 MHz; which makes them useful for many printed electronics applications.

The crucial parameter for printable semiconductors is the charge carrier mobility. Mobilities higher than 1 $cm^2V^{-1}s^{-1}$ in printed thin films have been achieved, [17, 35-37] even exceeding 10 $cm^2V^{-1}s^{-1}$ in more recent times.[38] A widely studied organic semiconductor is regioregular poly (3-hexylthiophene) (P3HT), with which field-effect mobilities of

0.1–0.3 have been achieved.[39, 40] The mobility of P3HT depends sensitively on the degree of crystallinity of the deposited film. Modifying the printing or annealing conditions strongly affects the morphology and hence the mobility.[39, 41] It is therefore certain that a successful printing method for organic semiconductors will be one that produces films with high degree of crystallinity and low density of grain boundaries.[42, 43]

Unlike the dielectric, the effect of semiconductor thickness on mobility in different device architectures and with different dielectrics is debated in literature.[44-46] It can be argued that mobility should not change much with thickness as the charge transport takes place mainly within a few nanometers at the semiconductor-dielectric interface. This is especially true in silicon-based bottom gate devices where P3HT is processed on the smooth surface of silicon dioxide. However, in top gated TFTs, where the channel is formed at the interface between the upper side of the P3HT layer and the dielectric deposited on top of it, possible changes in the P3HT surface roughness, presumably with increasing thickness, would directly affect the charge transport.[47] Therefore, for superior device performance, the printing method should yield highly smooth and uniform semiconductor films. The typically reported values of semiconductor thickness in TFTs are 30-200 nm.[48] Printing films as thin as these is a challenge for printing processes as the ink needs to cover the surface uniformly and remain continuous while drying, even in the presence of surface roughness and localized variation in surface energy.

Chapter 3 Challenges in Printed Electronics Manufacturing

3.1 High Resolution

Feature sizes smaller than 100 nm are routinely processed in modern-day semiconductor fabs. In fact, with Intel's state-of-the-art FinFET technology, gate line widths down to 22 nm have been achieved.[49] Minimum feature size not only has direct implications on device density, but is critical to device performance as well. For example, spacing between the transistor source and drain electrodes, also defined as channel length, dictates the maximum current and switching frequency of the device. Also, for display applications, smaller device footprint enables a higher aperture ratio, and therefore enhanced brightness and contrast.

Compared to CMOS processing, minimum feature sizes produced by printing techniques are much larger. Graphic printing methods are inherently designed to print feature sizes above the resolution of the naked eye (15-20 μm). For example, with

flexography, continuous conductive Ag tracks can be printed on flexible poly(ethylene terephthalate) (PET) substrate with a minimum line width of 75 μm.[50] Offset-printed features have typically a resolution in the range of 20 μm[51] and larger. The printing resolution for screen printing is limited to 50-70 μm using conventional screen printing meshes with 40 μm line openings.[52] Although stencils can be produced with finer line openings, the wire of the mesh tends to block the extremely fine openings and does not allow the ink to pass through the stencil, causing defects. A typical gravure printing press can print ~ 20 μm wide Ag lines.[53] Recently, Subramanian and co-workers have demonstrated sub-10 μm gravure printed lines [54, 55]. Francis and co-workers have also shown 2 μm wide lines using patterned silicon gravure plates. Despite these advances, line consistency is an issue for gravure printing, especially for the fine features. The minimum width of inkjet features is ~ 20 μm,[56] dictated by limits on droplet diameter and spreading on the substrate upon impact. Although Sekitani et al.[24] have demonstrated 2 μm Ag lines using sub-femtoliter inkjet-printed droplets, multiple passes were required to obtain the desired metal content in the wires.

In summary, resolution of mass printing methods is typically limited to ~ 20 μm or larger. In order to achieve the goal of high-performing and dense electronics using printing, this value needs to be decreased by at least an order of magnitude. There are several exotic laboratory-scale printing techniques, such as microcontact printing, micromolding in capillaries, and printing on pre-patterned substrates, that have been used for fabricating high-resolution electronics. Microcontact printing (μCP), pioneered by the Whitesides group[57], has been used to process metallic features as small as 0.5 μm.[57] In

μCP a flexible, elastomeric stamp (typically made of PDMS) with patterned reliefs is inked by a solution containing molecules terminated by different chemical functionalities (e.g. thiols, silanes, biomolecules etc.). After drying, the stamp is brought into conformal contact with the substrate ensuring transfer of the ink molecules to the substrate, and thereby forming a self-assembled monolayer (SAM) in the contact areas. In a subsequent step, the patterned SAM can be used as etch mask or as a seed layer for electroless deposition. In micromolding in capillaries (MIMIC)[58], closed capillary grooves are created by placing a soft elastomeric stamp, usually made of PDMS, with parallel protrusions on a smooth substrate. Upon placement of a drop of an ink at the open end of the capillary, the ink spontaneously wicks into the channel by capillary pressure. After complete curing of the ink, the stamp is removed leaving the patterns on the substrate. Lines of polyaniline, a conductive polymer, with a resolution of 350 nm have been obtained by MIMIC.[59] Centimeter-scale, 10 μm-wide reduced graphene oxide lines have also been patterned on a PET substrate using MIMIC.[60] However, while high resolution can be achieved, these techniques involve several processing steps and are typically unsuitable for large-area, high-throughput manufacturing. Therefore, a challenge for printed electronics is to produce (at least) sub-5 μm features with excellent fidelity, without compromising the primary benefit of high-throughputs. A survey of commercially available printing techniques and their comparison for resolution and throughput is shown in Fig. 3.1.[61, 62]

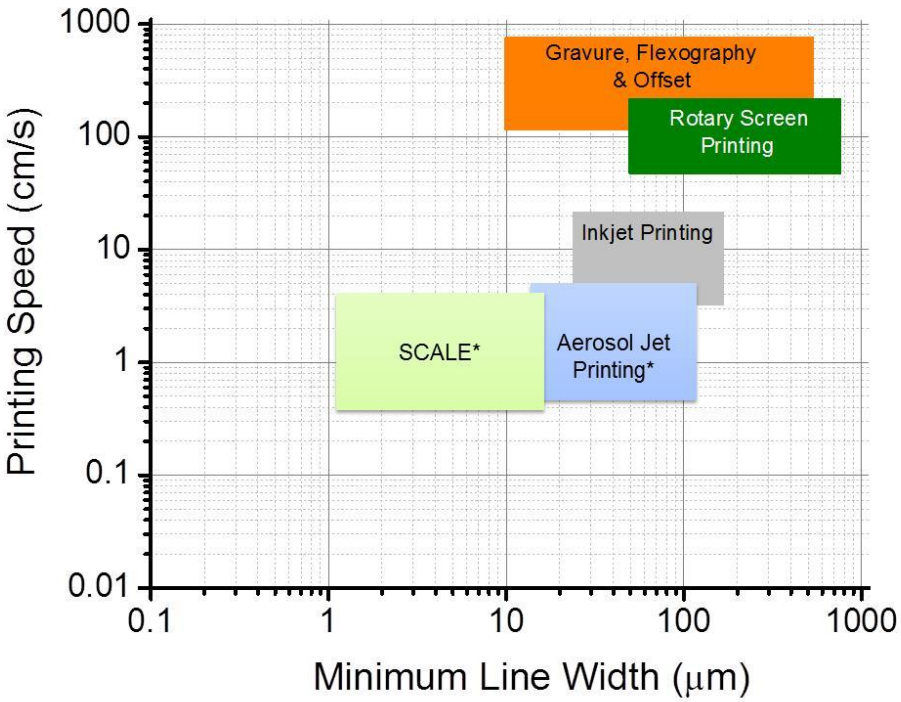

Figure 3.1 Comparison of resolution and throughput of commonly used printing techniques.

3.2 High Aspect Ratio Conductors

Conductive wires are essential elements of electronic circuitry, and high-resolution, high conductivity traces are crucial for achieving high-density, faster devices.[1] A major benefit of mass-printing methods over conventional semiconductor processing is the ability to fabricate large-area (~meters) electronics. Large-area circuitry necessitates longer conductive wires, which also translates to higher resistances in accordance with Ohm's law. In order to offset resistive losses, printed conductors can either have larger widths or increased heights to enhance the cross-sectional area. Because widths need to

be low to satisfy the condition of high-density circuitry, conductors with large heights or high aspect ratios (height/width) are required.

Features processed using mass printing methods typically have low aspect ratios. For example, flexographically-printed Ag lines by Deganello and co-workers[50], had a parabolic cross-section with a height and width of 0.75 μm and 75 μm, respectively (Figure 3.2). Despite a reasonable thickness value, this translates to an aspect ratio of only 0.01 due to the poor lateral resolution. In a modified flexographic process,[63] where printing was performed on a hydrophobic substrate from a PDMS print plate, a lateral resolution of 20 μm was achieved. However, the thickness of the printed patterns also decreased to 0.17 μm, and therefore, showing no improvement in the aspect ratio. In fact, multiple printing passes had to be employed to obtain respectable resistance values. Gravure printed lines typically exhibit an aspect ratio much smaller than 0.01 (printed height < 100 nm).[53, 54] The problem of poor aspect ratios is especially severe for highly-scaled gravure printing (sub-10 μm cells), due to challenges of adequate cell-filling and cell-emptying at these length scales. Owing to the high viscosity (due to high solids' loading) of the inks, screen printed lines can have wet thickness greater than 100 μm. However, the best reported aspect ratios are limited to 0.07-0.08 because of large line widths.[64] The possibility of printing relatively thick layers enables printing of low-resistance structures, also with conducting polymers, by compensating the high volume resistivity with a thicker layer. However, screen printing is suitable only for low-density applications. Inkjet printed lines typically have an aspect ratio between 0.01 and 0.05. Low viscosity requirements put a cap on the maximum solids' loading in the ink, which

limits the height of the printed features. In principle, for all the printing methods, thicker films can be obtained by employing multiple printing passes. However, this approach has several disadvantages. Firstly, this requires a time-consuming alignment step. Secondly, increment in thickness is generally accompanied by a slight width increase as well, which dampens the aspect ratio gain. Clearly, achieving aspect ratios greater than 0.1 is a challenge for printed electronics and requires development of innovative processing strategies.

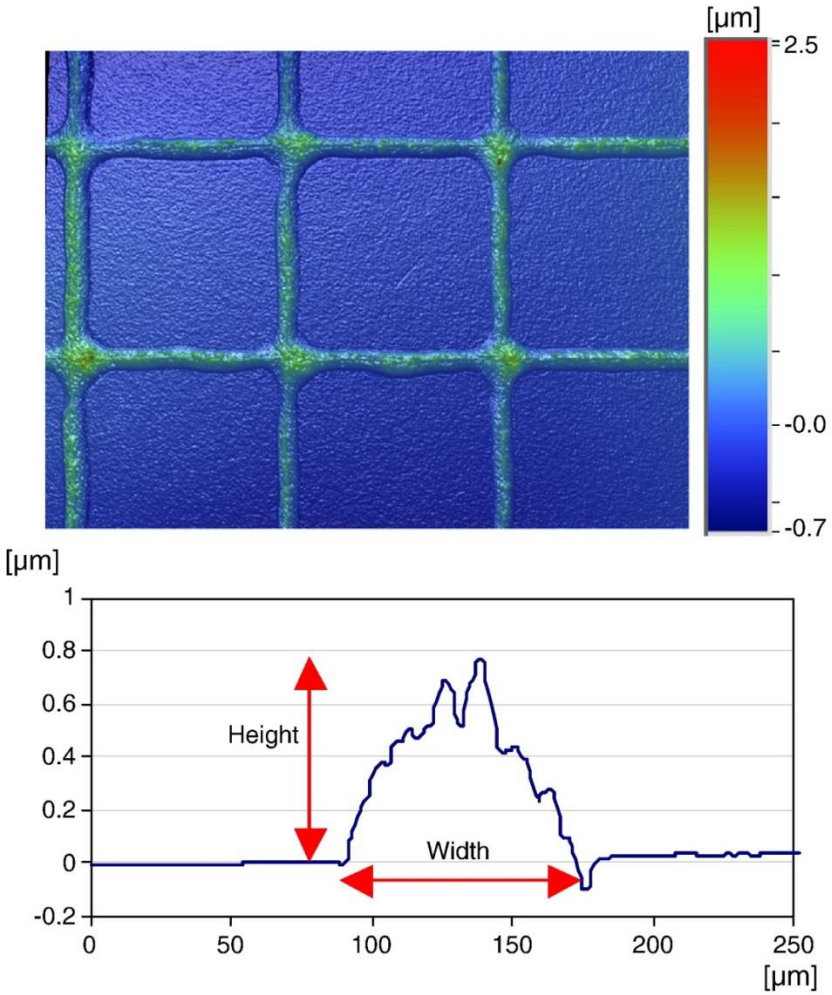

Figure 3.2 Top view of a silver grid produced by flexographic printing and cross section profile of one of its tracks.[50]

3.3 Surface Topography

Evaporated or sputtered films processed in vacuum-deposition systems typically have nm-level surface roughness, with negligible topography on the substrate. The uniformity and smoothness of conductors is important because charge carriers are conveyed either across or along conductor interfaces in electronic devices.[65] However, printed films are inherently rough due to the dynamics of drying and curing. Apart from surface roughness, printed films have non-uniform cross-sections depending upon the drying history of the film. For example, inkjet-printed lines have a characteristic doughnut-like cross-section due to the coffee-stain effect. High aspect-ratio conductive features are required for the goal of large-area electronics, as discussed in the previous section, which also contribute to creating topography on the substrate surface.

From a manufacturing standpoint, topography on the substrate complicates the use of popular mass-production printing methods such as gravure or flexography, as these involve physical contact between the printing roll and the moving web. Also, many printed devices require overlaying a thin organic film on metal wires. For example, in TFTs, high-capacitance gate dielectrics, which are critical to low operating voltages, are generally achieved by coating an ultra-thin polymer film or a self-assembled monolayer over a metal gate electrode.[29, 66-68] Also, a composite electrode formed by coating a thin layer of a conductive polymer over a metal grid appears to be a strong candidate for substituting indium tin oxide as the transparent electrode in organic solar cells and light-emitting diodes.[69-71] Achieving uniform coating on surfaces with topography is challenging and coating defects can result in shorts, i.e., device failure. The problem is

even more severe for printed conductors that have roughness of the same order as the thickness of the overlying film. For all of these reasons, developing methodologies for creating planarized flexible substrates with embedded, printed metallic tracks is essential.

3.4 Layer to Layer Registration

A major bottleneck to printed electronic manufacturing is overlay alignment or layer-to-layer registration. Most electronic devices are multi-layered. A classic example is a thin film transistor (TFT). As shown in Figure 3.3, the TFT fabrication sequence involves printing the source-drain electrodes spaced 5 μm (or less!) apart; printing the semiconductor ink between the source-drain electrodes; deposition of the dielectric ink atop the semiconductor, and printing the gate precisely on top of the source-drain channel.

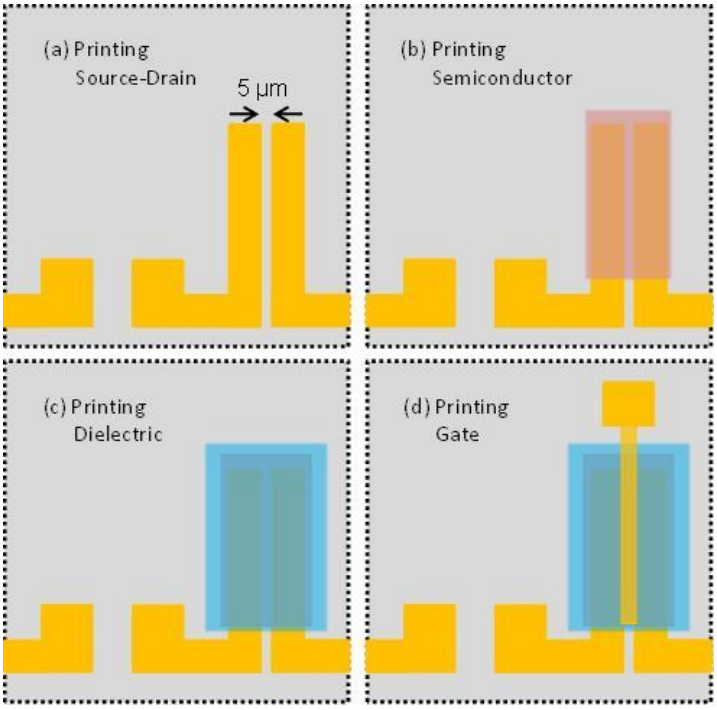

Figure 3.3 Printed transistor fabrication sequence.

It is a serious challenge to print all these layers on top of each other on moving substrates with micron-level precision. The problem is exaggerated by the use of flexible substrates which lack dimensional stability generally associated with glass or silicon substrates. Polymeric substrates may warp, expand or contact during processing, making it difficult to align features that are produced at different times in the process flow. A rule of thumb is that alignment tolerances should be 10% of the minimum feature size.[72] Therefore, if the minimum feature size is 10 μm, the alignment tolerance is approximately 1 μm. If the substrate is 1 m wide and the alignment needs to be held at 1 μm, this requires a dimensional stability of 1 ppm, greater than the thermal expansion stability of most polymeric substrates. Additionally, in any R2R setup, there is always some non-uniformity in web tension which causes substrate distortion. Furthermore, all contact printing methods such as gravure, flexographic, and offset involve mechanical stretching of the web and the print roll, leading to substrate distortion. Even in non-contact printing methods, e.g. inkjet printing, there is at least a ±10 μm variation of drop positioning arising from jetting inaccuracies or droplet deviation in-flight. All of these factors make alignment on moving, flexible substrates extremely challenging.

To overcome these challenges, self-aligning strategies are needed that enable materials registration to be achieved automatically during R2R processes. One such strategy is Self-Aligned Imprint Lithography (SAIL)[73-75], where all the all key materials are coated onto a web substrate and then a top coat resist is applied. The resist is imprinted with a stamp encoded with geometrical information such that subsequent etching steps selectively reveal specific underlayers (metal, semiconductor, and

dielectric) across the substrate (Figure 3.4). A major drawback of SAIL, however, is that it is a subtractive process, i.e., valuable materials are etched away.

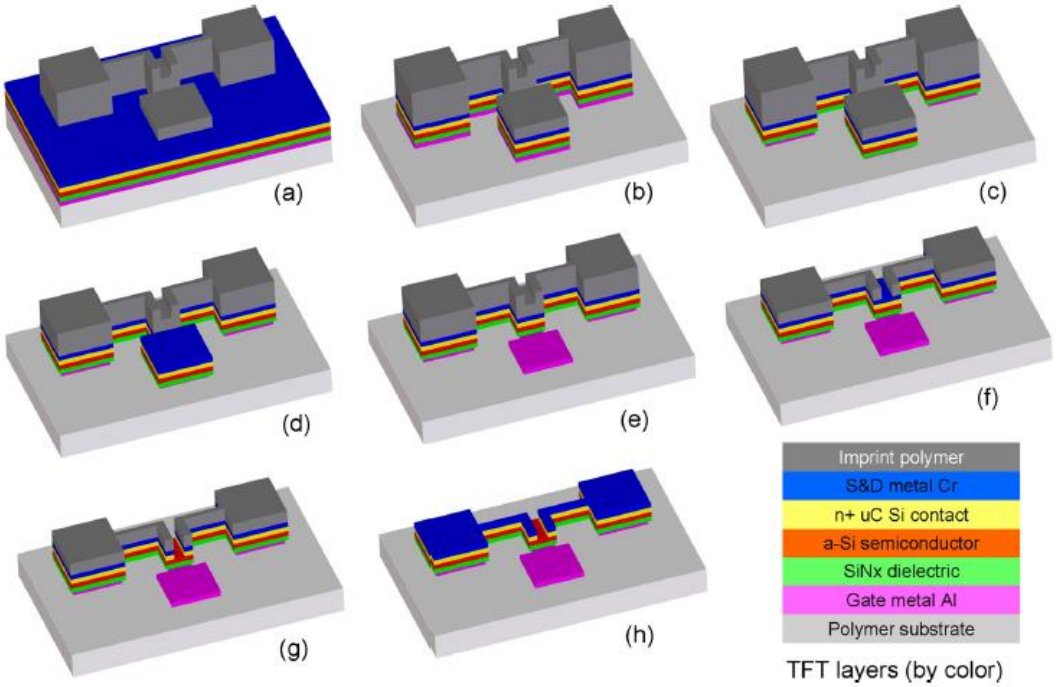

Figure 3.4 Self-aligned imprint lithography process. A multi-level three dimensional stamp is imprinted into a resist coating on the substrate, and subsequent etching steps reveal specific underlayers of metal, semiconductor and dielectric. Reproduced with permission from [73]

Self-aligned inkjet-printed patterns have also been obtained by ink de-wetting on chemically patterned surfaces.[76-79] The general concept of wetting-based self-alignment was first introduced by Sirringhaus and co-workers[80] for the formation of narrow-gap source-drain structures. In their work, the authors employed a lithographically patterned spacer as a 'mesa' structure (Figure 3.5a). A mesa is raised structure with a flat top, surrounded by steep cliffs on all sides. A conducting polymer poly-(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT:PSS) was then

inkjet printed on the hydrophobic mesa structure. The PEDOT:PSS ink then dewetted from the spacer to form self-aligned source-drain electrodes. The transistor was then completed by spin-coating of semiconductor, dielectric, and inkjet-printed top gate. Subramanian and co-workers[76] also applied the concept of wetting-based self-alignment

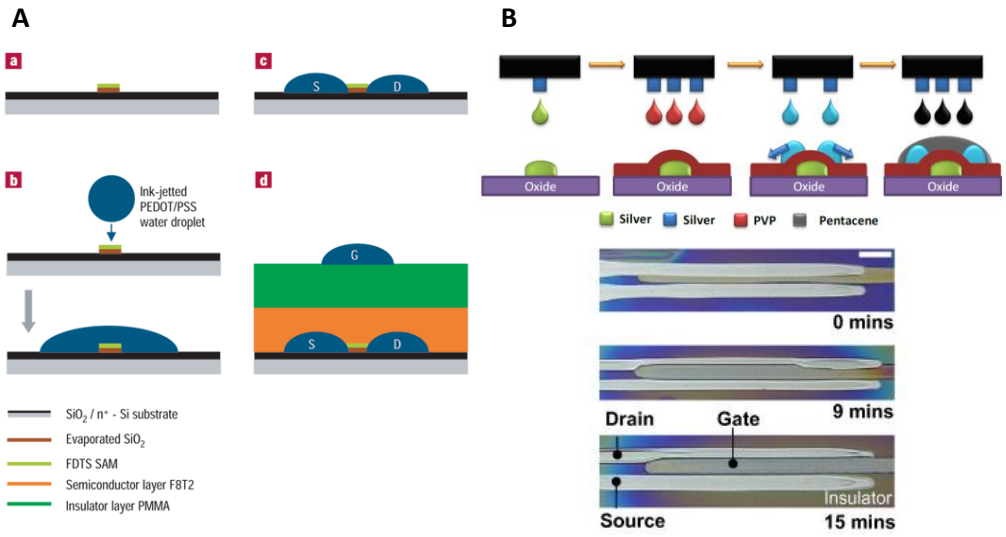

Figure 3.5 Wetting based self-alignment processes. (a) Creation of high-resolution source-drain channel by dewetting of PEDOT:PSS ink on raised hydrophobic $Si0_2$ structures.[Reproduced with permission from [80]] (b) Formation of aligned source-drain electrodes by dewetting of Ag ink on hydrophobic inkjet printed gate line.[76]

to align the gate to the source-drain channel (Figure 3.5b). A hydrophobic polymer dielectric, polyvinyl pyrrolidone was spun-coat on inkjet-printed silver gate to form a mesa structure. Upon printing a silver ink on top of the mesa structure, some portion of the printed silver dewetted and rolled off the mesa structure to give self-aligned source and drain electrodes. However, in the true sense, these processes are only partially self-aligned because they require micron-level registration of the inkjet nozzle to previously patterned features. Moreover, only a few selective layers of the device stack can be patterned using these techniques, not the entire device.

Chapter 4 Optimization of Aerosol-Jet Printing for High-Resolution, High-Aspect Ratio Conductors

4.1 Aerosol Jet Printing Process

Aerosol jet printing is a relatively new method for fabrication of printed electronics. In this method, the functional ink is aerosolized and entrained in a gas stream. There are two options for generating the aerosol: pneumatic and ultrasonic. The aerosol stream is directed to a print head where it is aerodynamically focused by a co-axial sheath gas flow, as shown in Figure 4.1. The result is a high density deposit with feature size only a fraction of the nozzle opening. The technique is suitable for printing conductors, semiconductors and dielectrics. As a consequence, there has been recent interest in using the method for a variety of applications, including printing of transistors,[33, 81-83] strain gauges,[83] interconnects,[84] and solar cells.[85]

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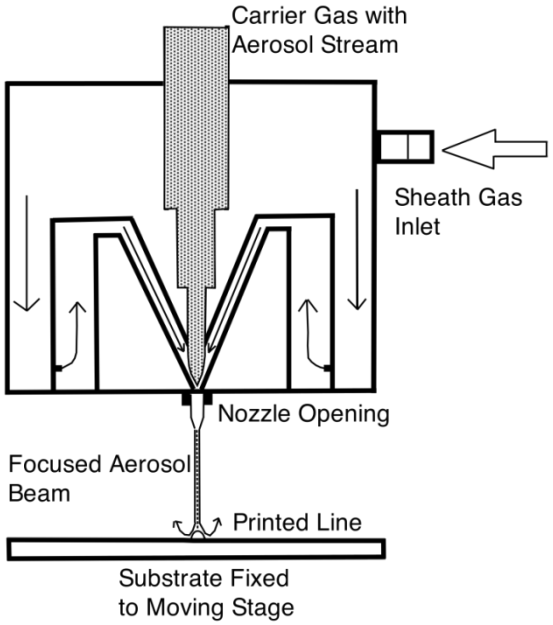

Figure 4.1 Schematic of the aerosol jet print head showing aerodynamic focusing by sheath gas inside the print head.

While most of the past reports demonstrate the technique's applicability, there are very few studies examining the factors that affect the printing quality. Goth *et al.* studied printing of silver lines with an aerosol jet printer outfitted with a pneumatic atomizer. They showed that the width of the printed lines is affected by the three adjustable flow rates on their instrument and the stage speed; however, regarding thickness control, they focused on the effect of number of layers deposited. Verheecke *et al.* also studied printing with a pneumatic atomizer and developed a process window showing the effects of the three gas flow rates on the edge definition of the printed lines. While these studies reveal some information on the printing process, they are specific to the pneumatic atomizer and cover only a portion of the process parameters. More research is needed on printing with the ultrasonic atomizer, which is well suited to lower viscosity inks and arguably has

tighter control of the aerosol mist particle size, and on the effects of full range of process variables on the characteristics of printed lines.

The aerosol jet printing process with the ultrasonic atomizer is influenced by a number of variables. The adjustable process parameters include the atomization frequency, carrier gas flow rate, sheath gas flow rate, nozzle diameter, working distance, stage speed and stage temperature. Additionally, the surface tension, solids loading and viscosity of the ink play crucial roles in obtaining a wide range of structures from tall interconnects to thin capacitor films. In this work, we systematically study the influence of process parameters on geometry and electrical properties of lines created from silver nanoparticle ink. By exploring these process parameters in combination, we identify a key parameter, the focusing ratio, which is defined as:

$$\text{Focusing Ratio (FR)} = \frac{\text{Sheath Gas Flow Rate}}{\text{Carrier Gas Flow Rate}} \tag{4.1}$$

While the role of the sheath gas in focusing the aerosol is recognized, we demonstrate here that the focusing ratio is central to controlling the line features and resistance. Additionally, the results are used to develop an operability window and process regime for printing tall and narrow silver lines in a single pass.

4.2 Experimental Methods

All printing experiments were carried out with a nanoparticle silver ink (UTDAg40X, UT Dots Inc.). This ink is compatible with the ultrasonic atomizer of the aerosol jet printer, which has a recommended ink viscosity range of 1-5 cP. The ink contains 40 percent by weight of the silver nanoparticles (8-15 nm in diameter) in a solvent mixture

of xylene and other hydrocarbons (proprietary). For each printing run, a glass vial was loaded with 1.70 ml of the ink and 0.30 ml (15% v/v) terpineol as a co-solvent. During atomization, the ink vial was maintained at a constant temperature (14°C) using a temperature stabilized water bath.

Silver lines were printed in a single pass using a commercial Aerosol Jet Printer (Optomec Inc.). Dry N_2 (HP grade, 99.998 %) was used as the carrier and sheath gas. Experiments were carried out with carrier gas and sheath gas flow rates ranging from 0-50 standard cubic centimeters per minute (sccm) and 0-200 sccm, respectively. Three different nozzle sizes (100, 150 and 200 μm) were used; each nozzle is 7.50 mm long. The atomizer current was kept constant at 0.60 mA and the printer stage heater was not used. Stage speeds were varied from 1 to 100 mm/s. Printing was done both on polyimide (3 mils Kapton, DuPont) and silicon substrates. All printed lines were sintered in an oven at 200°C for 1 hour.

The geometrical features, microstructures and electrical properties of the printed lines were characterized. Line widths were measured using the Alignment Viewer optical microscope that is incorporated into the printer. With this method, we could exclude any overspray and characterize the electrically functional part of the line. The line thicknesses were measured after sintering using a Tencor P-16 profilometer. Due to the parabolic cross section of the lines, the total thickness was taken as the average thickness of the cross section. An example profilometer trace is shown in Figure 4.2. The lines were also imaged using a Hirox microscope (Digital Microscope KH-7700) and a scanning electron microscope (JEOL-6500). To measure the electrical conductivity, silver pads and lines

were printed. The conductivity measurements were made using the two point probe method in a N_2 filled glovebox with Keithley 236 electrometers.

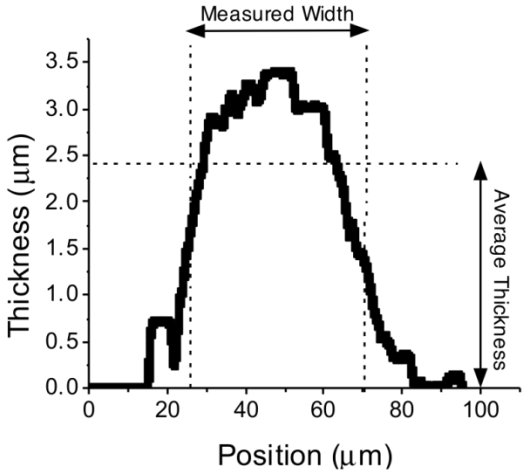

Figure 4.2 Cross sectional profile of an aerosol-jet printed silver line obtained from surface profilometry. This data provided the average thickness (2.41 μm). The width, measured in the optical microscope (45 μm), is also shown.

4.3 Effect of Process Parameters on Line Geometry

Figure 4.3 shows the versatility of aerosol jet printing. Silver lines were printed on flexible polyimide substrates (Fig. 4.3a), over surface topology (Fig. 4.3b), and in complex and high resolution patterns (Fig. 4.3c and d). The quality and features of the printed patterns are determined by several printing processing parameters as well as the properties of the ink. An important process parameter is the focusing ratio (Eq. 4.1), as demonstrated in Figure 4.3(e –g). In this paper, we explore the key adjustable printing parameters: focusing ratio, nozzle size, carrier gas flow rate and, stage speed. For simplicity, the same ink was used for printing and efforts were made to keep all other conditions the same.

The distance between the nozzle tip and the substrate, i.e., the working distance, impacts the quality of the printed lines. Figure 4.4 shows the variation of line width with working distance. The shutter below the nozzle limits the distance of closest approach to the substrate to 2.0 mm. For all focusing ratios, the aerosol beam is highly collimated up to a distance of 5 mm. The line width slightly increases with the working distance up to a distance of 5 mm. Beyond that, there is a large amount of overspray and the edge of the line is no more coherent. A working distance of 2 mm was chosen for all measurements in this work. This value produced a highly collimated aerosol beam for all focusing ratios investigated.

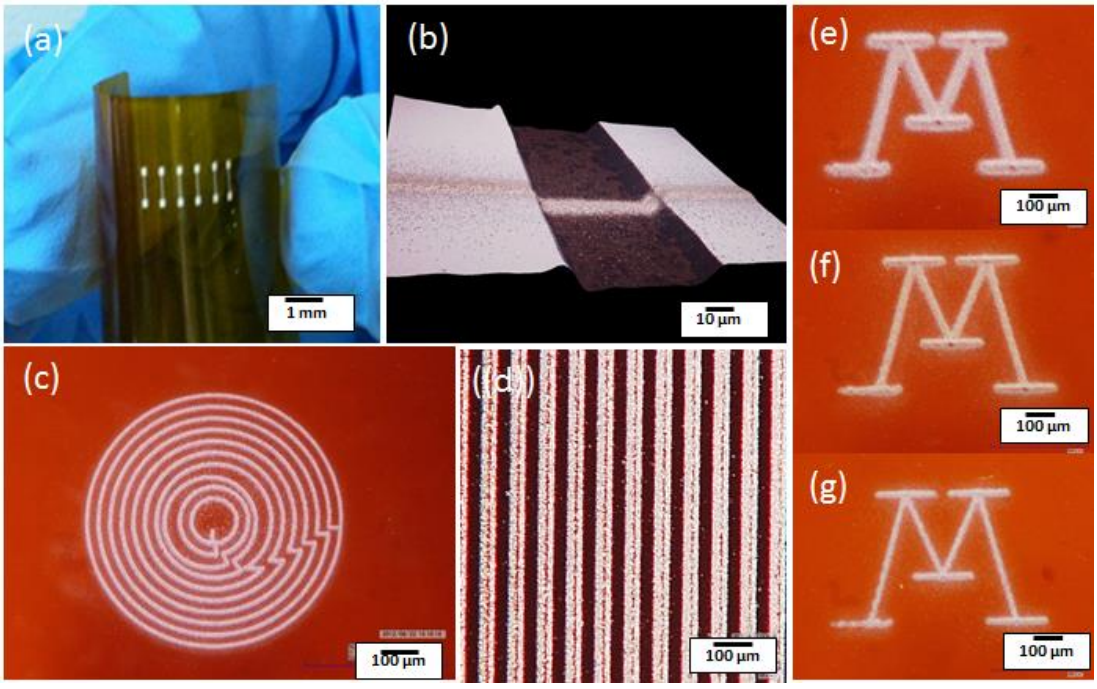

Figure 4.3 Images of different aerosol-jet printed silver patterns. : (a) printed pads and lines on flexible polyimide substrate for electrical characterization; (b) topographical image of a line printed over a 10 µm deep trench with slightly tapered walls etched in silicon; (c) printed spiral pattern on polyimide; (d) 40 µm wide lines with 30 µm spacing; and University of Minnesota logo printed at focusing ratio (e) 3, (f) 5 and (g) 7.

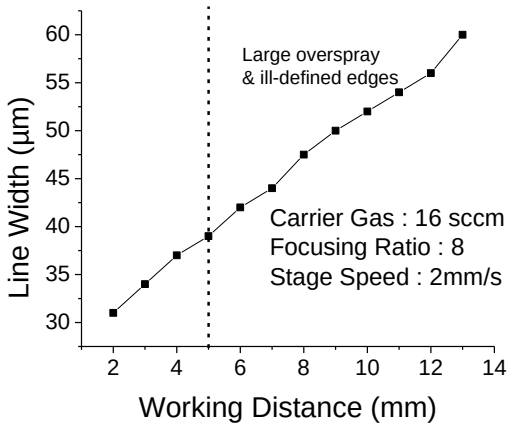

Figure 4.4 Variation of line width with working distance.

Figure 4.5(a) shows the effect of focusing ratio on the line width and thickness for a fixed nozzle diameter (200 µm), carrier gas flow rate (20 sccm) and stage speed (2 mm/s). The line width decreases as the focusing ratio increases up until a focusing ratio of about 8. Beyond this value, the width is nearly constant. Extremely wide lines, such as 120 µm, are obtained for a focusing ratio of 1 whereas lines as narrow as 25 µm are obtained for higher focusing ratios. The error bars represent the variability from run to run expressed as standard deviation. The variations in width become smaller as the focusing ratio increases. Unlike the width, the line thickness variations increase with the focusing ratio. The trend is also demonstrated in the profilometry scan results shown in Figure 4.5(b). Overall, the thickness has more variability than the line width. As described more below, the thickness is affected significantly by the carrier gas flow rate and is subject to fluctuation based on the aerosol output. Above a FR of 8, the thickness becomes more erratic, not increasing as expected. This behavior may be due to change in the aerosol flow characteristics or premature drying brought about by the high sheath gas

flow rate. These effects require more investigation, but in practice regions of high variability are avoided.

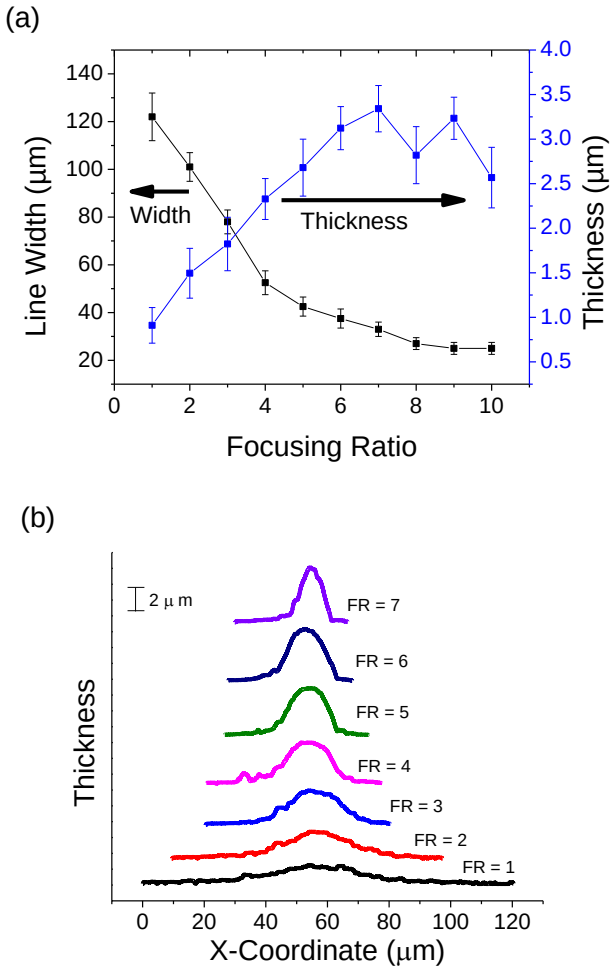

Figure 4.5 (a) Effect of focusing ratio on line width and thickness. (b) 2-D profilometry data of lines printed for focusing ratios from 1 to 7. The carrier gas flow rate and stage speed are fixed at 20 sccm and 2 mm/s, respectively.

The line width and thickness are also a function of nozzle size. Figure 4.6 shows the effect of nozzle diameter and focusing at constant carrier gas flow rate (16 sccm) and stage speed (2 mm/s). As expected, finer lines are produced from smaller nozzles. Interestingly, the drop in line width with increasing focusing ratio is more dramatic in the

smaller nozzles. However, there is a limitation; pressure builds up in the nozzle as

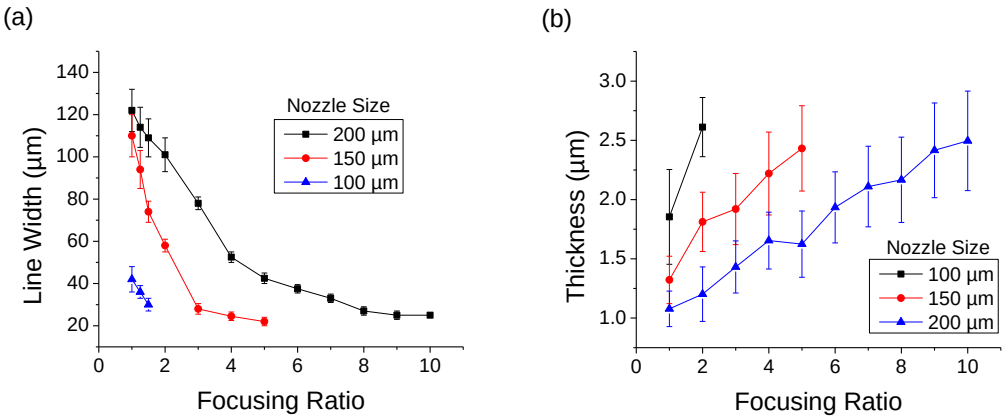

Figure 4.6 Effect of nozzle size on (a) line width and (b) thickness. The carrier gas flow rate and stage speed are kept constant at 16 sccm and 2 mm/s, respectively.

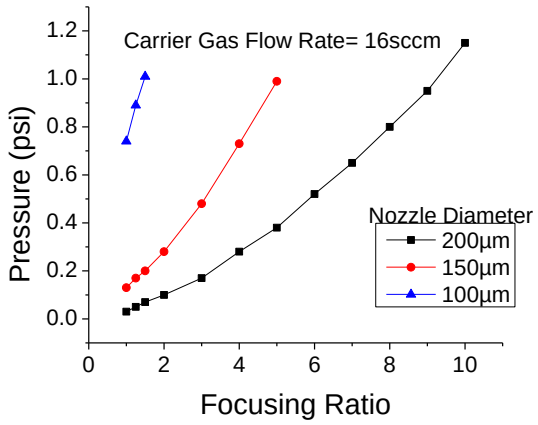

Figure 4.7 Variation of pressure on the inside walls of the nozzle with focusing ratio.

focusing ratio increases. For smaller nozzles, the pressure limitation is reached at lower focusing ratios as compared with larger nozzles. The pressure of the gases is measured by a pressure transducer in the mass flow controller (MFC). In a standard model of the aerosol-jet printer, the pressure reading of the both the carrier and the sheath gas is displayed on the MFC window on the computer monitor. Under normal working conditions, the sheath and the carrier gas show similar pressure values. Since the smallest constriction in the system is at the nozzle exit, the pressure is higher upstream of the

nozzle exit. Figure 4.7 shows the variation of pressure reading with focusing ratio in three different nozzles. For a given carrier gas flow rate, the pressure reading increases with increasing focusing ratio, finally exceeding 1 psi which prompts a warning on the MFC window. The pressure increases almost linearly, and the increase is abrupt in smaller nozzles.

Hence, the line width reaches a limiting value that is independent of the nozzle diameter. Except for the extremely wide lines, almost the entire spectrum of line widths achieved using a 200 μm nozzle can be achieved with a 150 μm nozzle at comparatively lower sheath gas flow rates. Figure 4.6(b) shows the variation in thickness of the same lines with nozzle size and focusing ratio. For a given focusing ratio, the thickness increases with a decrease in the nozzle diameter. All the three nozzle diameters yield almost the same maximum thickness but the minimum thickness is lower in the 200 μm nozzle. It is evident that the 200 μm nozzle yields a wider range of both line width and thickness and also sustains higher sheath gas flow rates. Consequently, the 200 μm nozzle was used for the rest of the work.

Figures 4.8(a) and (b) show the effect of carrier gas flow rate on the line width and thickness, respectively, at different focusing ratios and constant stage speed of 2 mm/s. For most carrier gas flow rates, the line width depends on the ratio of sheath gas flow rate to carrier gas flow rate and not the respective values. This result laid the basis for the definition of focusing ratio, which is used extensively in this work. A slight deviation in the trend is found for carrier gas flow rates greater than 30 sccm. Here, the width begins to increase, consistent with spreading after deposition. Note that the nozzle pressure

limitation restricts the carrier gas flow rates that can be used at high focusing ratios. Unlike the line width, the thickness changes considerably with the carrier gas flow rate. Thickness increases with carrier gas flow rates until at higher flow rates it falls off again due to spreading after deposition. As before, for the same carrier gas flow rate, the thickness is higher at higher focusing ratios.

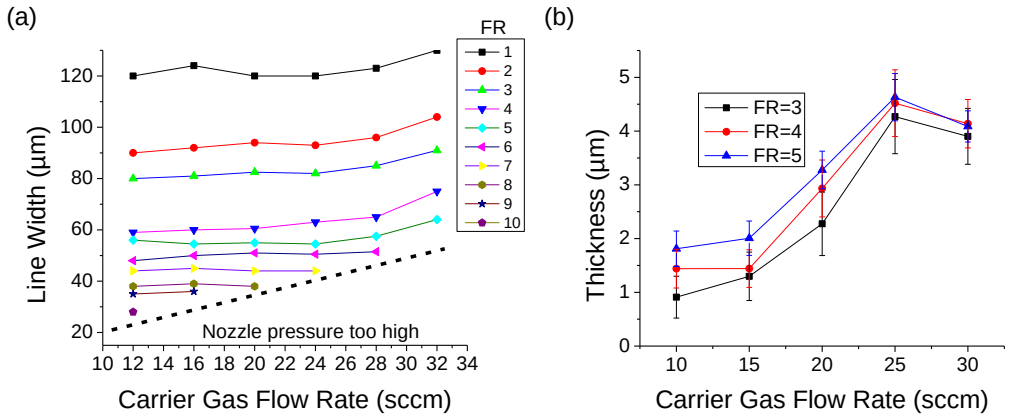

Figure 4.6 Effect of carrier gas flow rate on (a) line width and (b) thickness for different focusing ratios. The stage speed used is 2 mm/s.

Line geometry is further modified by stage speed, as demonstrated in Figure 4.9(a). The data show how stage speed affects the line width at different focusing ratios for a given carrier gas flow rate. Line width decreases steadily as stage speed increases from 1 to 4 mm/s and then saturates. As discussed later, spreading influences this trend. Thickness decreases continuously with stage speed (Fig. 4.9b). Similar trends are also observed for various focusing ratios.

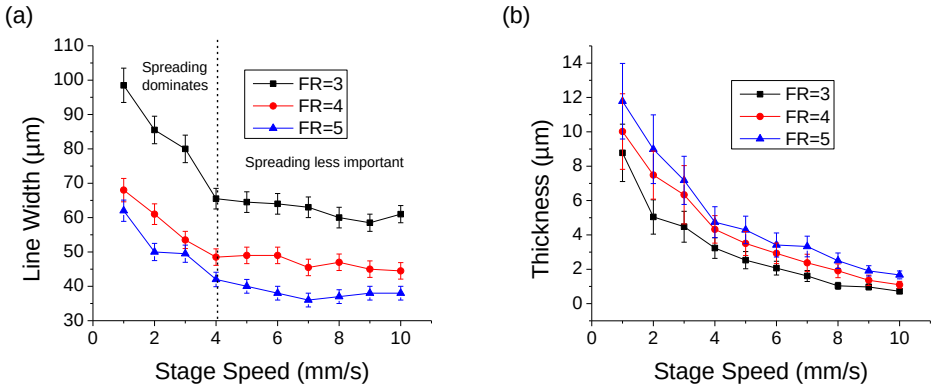

Figure 4.7 Effect of stage speed on (a) line width and (b) thickness for different focusing ratios. The carrier gas flow rate is fixed at 24 sccm.

4.4 Physical Principles of Aerosol Jet Printing

Figure 4.10 is a schematic diagram showing the physical features of the aerosol beam from nozzle to substrate and the connection to the geometry of the as-printed line. The sheath gas forms an outer layer around the aerosol stream and prevents the contact between the aerosol particles with the inside walls of the nozzle, preventing clogging. The collimation of the aerosol beam takes place in two stages.[9] Prior to the nozzle (see Fig. 4.1), the sheath gas surrounds the aerosol stream as it passes through a first orifice. Next, the combined sheath gas and aerosol stream is focused further as it passes through the narrower nozzle. The combined sheath and aerosol beam is accelerated to an exit velocity, V_e, creating an aerosol stream with cross sectional area A_e.

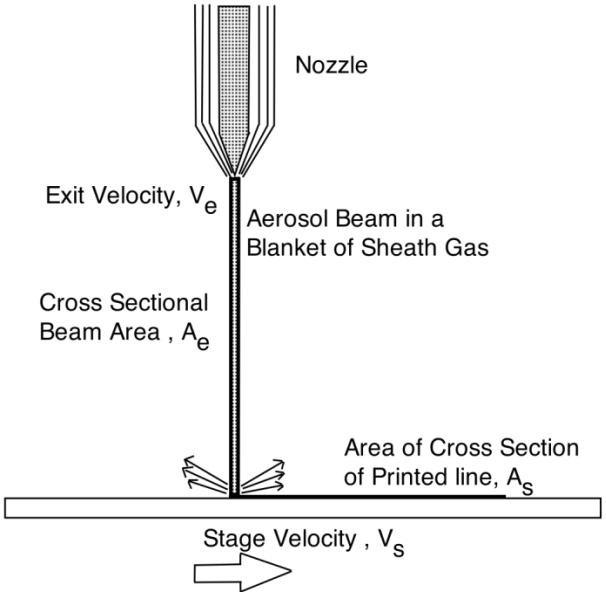

Figure 4.8 Enlarged view of the nozzle showing physical features as the aerosol jet exits the nozzle and meets the moving substrate to form a printed line. Upon impact, the aerosol beam coalesces and the gases are expelled.

If there is no loss of material, the mass flow rate at the point of exit from the nozzle and at the point where the aerosol beam hits the substrate are the same, and the continuity equation applies:

$$\rho_e A_e V_e = \rho_s A_s V_s \qquad (4.2)$$

where A_s and V_s are the cross sectional area of the printed line and stage speed, respectively, and ρ_e and ρ_S are the densities of the aerosol beam and the coalesced as-printed material, respectively. Rearranging, the factors that control the width, *w*, and thickness, *t* of the as-printed line are given by:

$$w.t \approx A_s = \left(\frac{\rho_e}{\rho_s}\right)\frac{V_e A_e}{V_s} \qquad (4.3)$$

Upon impingement, the aerosol droplets coalesce to form a liquid line. The width of the printed line is the sum of the diameter of the collimated beam and lateral spreading after deposition. It should be noted that A_s is different from the final cross sectional area owing to the decrease in thickness from evaporation and sintering. While this simple picture does not address the details of how the aerosol stream condenses into a printed line and the subsequent spreading, evaporation and sintering, it does help to explain the observed effects of process parameters on the printed line geometry.

For a fixed carrier gas flow rate and stage speed, the line width decreases and thickness increases with an increase in the sheath gas flow rate or in other words with an increase in the focusing ratio (Fig. 4.5). Increasing the sheath gas flow rate tightens the aerosol beam and reduces the cross sectional area of the beam at the exit, A_e. Assuming ρ_e is constant, the reduction in A_e also leads to an increase in V_e such that the product, $A_e V_e$ is a constant (by conservation of mass). Assuming that ρ_s does not change much for different sheath gas flow rates, it can be seen from equation (4.3) that the product of width and thickness is also a constant for a fixed stage speed. The width and the thickness of the as-printed line are therefore hyperbolically related to each other, as shown schematically in Figure 4.11. On each of the hyperbolas, increasing the focusing ratio leads to a decrease in the width and increase in the thickness but the cross-sectional area remains the same.

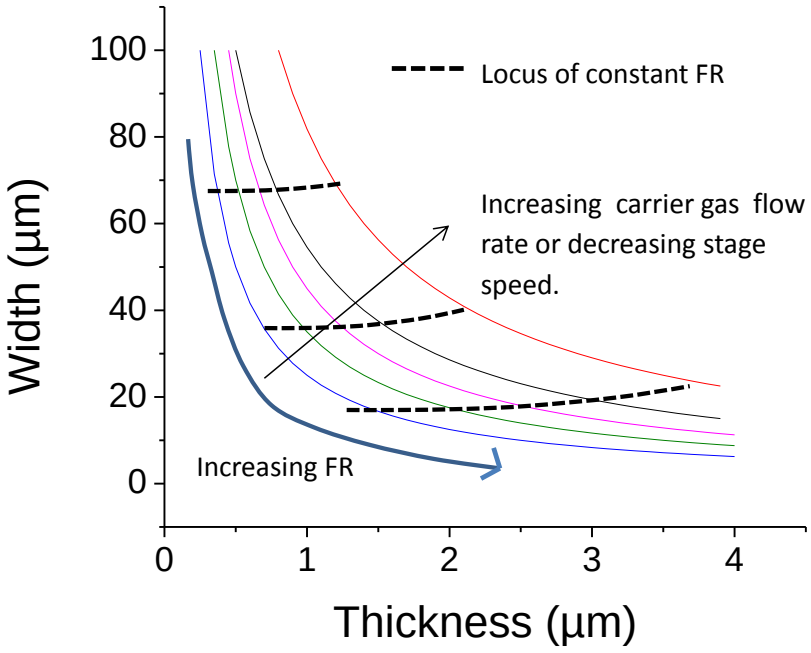

Figure 4.9 Schematic showing line width and thickness variation with focusing ratio for different carrier gas flow rates (at fixed stage speed) or different stage speeds (at fixed carrier gas flow rate) based on the conservation of mass equation. Numerical values on the axes are estimates for as-printed lines before drying and sintering.

Line width is found to be nearly the same for a fixed value of focusing ratio and stage speed irrespective of the carrier gas flow rate, as shown in Figure 4.8(a). We believe that the co-axial carrier and sheath gas flow inside the nozzle readjusts to yield similar beam diameter as long as both the flow rates remain proportionate. In terms of equation (2), increasing the carrier gas flow rate at fixed focusing ratio results in an increase in the V_e while keeping A_e constant; hence, we expect A_s to increase. This increase can also be represented by a different hyperbola for each value of carrier gas flow rate, as shown in Figure 4.11. Since the beam diameter is fixed, the increase in A_s is accommodated by an increase in thickness. Therefore, moving to the right on the constant FR lines (Fig. 4.8),

there is no change in the line width but the thickness keeps increasing, also shown in Figure 4.8(b). The effect of nozzle diameter can be likewise understood.

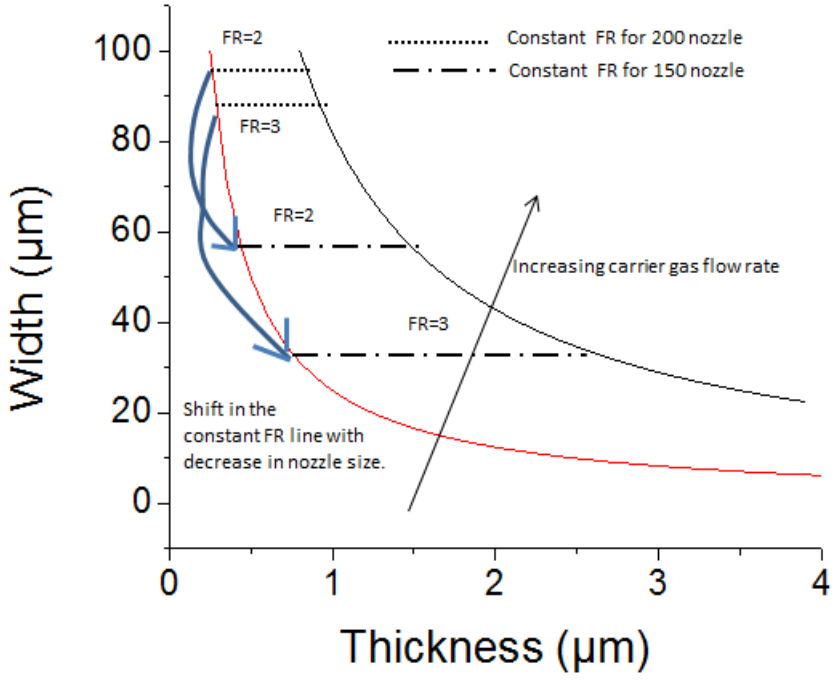

Figure 4.10 Schematic showing line width and thickness variation with nozzle diameter for different carrier gas flow rates.

Figure 4.6 demonstrates the effect of nozzle diameter on the geometry of the printed lines. A smaller nozzle is more effective in focusing an incoming aerosol stream due to geometrical considerations. Since the incoming mass does not change with nozzle size, the width and thickness still follow the same relationship and there is no separate hyperbola for a smaller nozzle in Figure 4.12. The enhanced focusing ability of the smaller nozzle can then be understood by an apparent shift of constant focusing ratio lines with the hyperbola. The point of intersection with a hyperbola shifts downwards on the same curve. Consequently, the reduction in width (Fig. 4.6a) and increase in the

thickness (Fig. 4.6b) of the printed lines is greater in a smaller nozzle for the same focusing ratio.

Increasing the stage speed at a fixed carrier and sheath gas flow rate further lowers the line width and thickness, as illustrated in Figure 4.9 (a) and (b), respectively. This effect can be directly related to equation (3). Namely, increasing V_s with all else constant requires A_s to decrease. Therefore, each hyperbola in Figure 4.11 corresponds to a certain stage speed. While the decrease in thickness with stage speed is expected, the variation of line width with stage speed is less expected. Line width varies greatly with stage speed at slower speeds and becomes more or less constant after a certain speed, as shown in Figure 4.9(a). This general trend is represented qualitatively in Figure 4.11 where for a fixed focusing ratio, line width starts to increase below a specific stage speed. Spreading becomes an important factor in determining line widths when the ink accumulates on the substrate at a rate that the amount of solvent in the printed line after coalescence is appreciable. This phenomenon is more pronounced at low stage speeds (Fig. 4.9a, stage speed < 4 mm/s) and high carrier gas flow rates (Fig. 4.8a, carrier gas > 30 sccm). Under these conditions, a large amount of liquid accumulates over a fixed width determined by the focusing ratio. This constrained build-up leads to a non-equilibrium curvature of the liquid just after coalescence. Consequently, there is fluid flow driven by surface tension and curvature gradients, causing an increase in line width. Eventually, the liquid attains its equilibrium curvature dictated by the contact angle. At high stage speeds or low carrier gas flow rates, the curvature of the coalesced liquid is close to its equilibrium value and therefore spreading is not dominant. Almost no decrease in line width is

observed at higher stage speeds (Fig. 4.9a), suggesting the reduced importance of spreading and the sole dependence of the width on the beam diameter.

Focusing is crucial in aerosol jet printing; however, several factors limit the focusing ratio. One factor is the maximum pressure limit of the nozzle. As the flow rates for the sheath and carrier gas increase, the pressure exerted on the nozzle also increases, eventually reaching a limiting value. Additionally, at higher focusing ratios there is a possibility of departure from laminar flow behavior of the combined aerosol and sheath gas jet as indicated by the unexpected thickness variation after FR of 8 in Figure 4.5(a). Focusing ratio, ultimately, is limited by the fact that the gases inside the nozzle cannot exceed the sonic velocity (the maximum velocity to which a fluid can be accelerated in a converging nozzle).

A phenomenological problem with aerosol jet printing is overspray (Fig. 4.13). Overspray is harmful not only for the loss of material but also because it renders aerosol jet printing unfit for printing narrowly spaced lines such as a source-drain channel in transistors. Overspray is a complex phenomenon and is dominant at high sheath gas flow rates, slower stage speeds, and high working distances. The physical principles behind overspray are still not completely understood. Overspray can be quantified in two ways: density and spread. One possible strategy to study overspray could be to predefine allowable values of these parameters and use image analysis to measure overspray as process variables change. Studies are underway to study the effect of process variables on overspray.

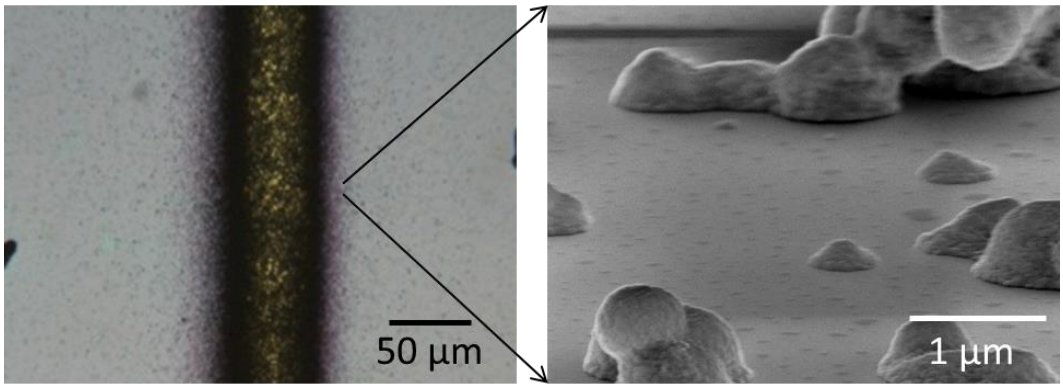

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Figure 4.11 The phenomenon of overspray. (a) Optical microscope image of overspray on either side of a printed and sintered silver line on a silicon wafer. (b) SEM image of the same region showing overspray as tiny clusters of sintered silver nanoparticles.

4.5 Effect of Process Parameters on Electrical Properties.

A fundamental property of a conductive line is the scaling of its resistance with length. The length dependence of resistance from Ohm's law is given by the following expression for the two point probe method,

$$R = R_c + \rho L/A \qquad (4.4)$$

where R is the total resistance of the line, R_c is the contact resistance, ρ is the resistivity, L and A are the length and area of cross section of the line, respectively. Using a two-point probe method, the resistance of printed wires with five different lengths was measured. Figure 4.14 shows the linear relationship between resistance and length, suggesting that the lines closely follow Ohm's law. In Figure 4.14, the contact resistance between the tungsten probe tip and the silver line is a given by the intercept of the line. The product of the slope of the line with the cross sectional area gives the resistivity. The value of contact resistance was calculated for multiple samples with different cross sectional areas each undergoing the same sintering cycle. The average value is around

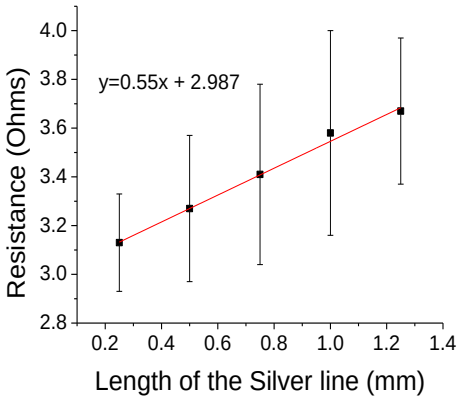

Figure 4.12 Resistance vs. length for lines printed at carrier gas flow rate = 17 sccm, focusing ratio = 7 and stage speed = 2 mm/s.

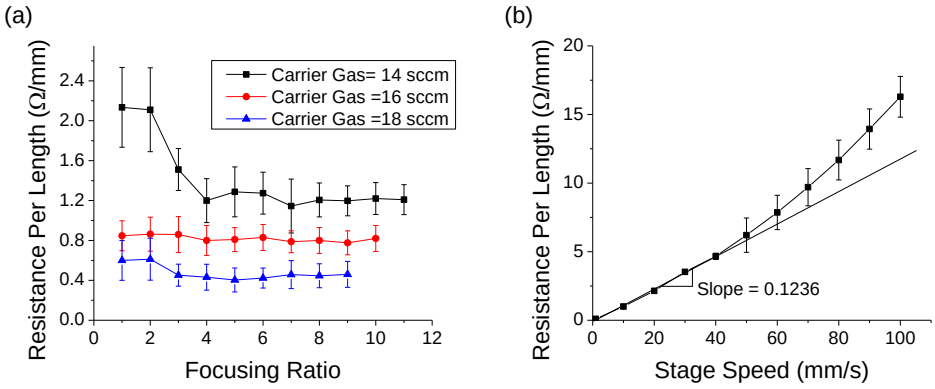

Figure 4.13 Electrical properties of printed lines. (a) Dependence of the resistance per unit length on the focusing ratio and the carrier gas flow rate (stage speed = 2 mm/s). (b) Effect of stage speed on resistance per unit length (carrier gas flow rate = 40 sccm and FR = 3)

3 Ω and is assumed to be the contact resistance for all resistance measurements. The calculated resistivity is 3.61 μΩ-cm which translates to approximately twice that of bulk silver, on par with other reported values for printed silver lines.[26, 27]

Figure 4.15 shows the effect of the process parameters on the electrical properties of the sintered silver lines. As shown in Figure 4.15(a), the resistance per unit length is

approximately independent of focusing ratio for a fixed carrier gas rate and stage speed. The resistance of lines is displayed on a per mm basis after subtracting the contact resistance. The exception is an increase in resistance that occurs at low focusing ratio and low carrier gas flow rate (14 sccm). Under these conditions, the lines were noticeably less dense than the lines printed under other conditions. Resistance per unit length also increases with the stage speed, as shown in Figure 4.15(b). The dependence is linear up to a certain stage speed. Here, conductive lines are printed at stage speeds as high as 100 mm/s. This high speed printing requires a relatively large carrier gas flow rate to ensure adequate material for deposition. It was also observed that at stage speeds above 10 mm/s, printing began with a snake-like deposition as the stationary stage accelerated to a very high speed. The wiggle from this inertial effect straightens out once the stage attains a constant velocity.

The factors influencing the line geometry as discussed above also have a direct bearing on the electrical properties. The current carrying ability of a line is directly proportional to its cross sectional area. Keeping the carrier gas flow rate and stage speed constant, the line width decreases and the thickness increases as the focusing ratio increases. To validate this argument, the resistance per length was measured for lines printed at a fixed carrier gas flow rate and stage speed for different focusing ratios. No change in resistance is seen for the same carrier gas flow rate, as shown in Figure 4.15(a). The resistance decreases with increasing the carrier gas flow rates due to an increase in the cross sectional area. At low carrier gas flow rates with comparable sheath gas flow rates, there is not enough solvent in the as printed feature for complete coalescence. Therefore, for

the carrier gas flow rate of 14 sccm at focusing ratio 1 and 2, the deposit has low density and higher resistivity leading to higher resistance per unit length. Increasing the focusing ratio above 2 results in more dense, well-formed lines having reduced resistivity that does not vary much over the remaining range. The resistance per unit length also increases with stage speed, as shown in Figure 4.15(b), following almost a linear relationship up to 40 mm/s. The linear increase of resistance with stage speed suggests a decrease in the cross sectional area but no change in the resistivity of the printed feature. Beyond a stage speed of 40 mm/s, there is inadequate coalescence of the ink upon printing and consequently the microstructure of the line becomes increasingly porous. Even though the lines are conductive, the resistivity is higher due to increased porosity and hence the resistance is higher than predicted by the linear relationship in Figure 4.15(b).

4.6 Operability Window and Process regime.

Figure 4.16 shows an operability window with varying carrier gas flow rate and stage speed, and the impact of the focusing ratio on line geometry for a given carrier gas flow rate. As shown in Figure 4.16 (a), there is a range of stage speeds that can be selected for any given carrier gas flow rate. The limits in Figure 4.16(a) were determined experimentally with error bars representing the variability in assigning the characteristic region and lines drawn to represent the boundaries. At low stage speeds, the input from the impinging aerosol jet cannot be accommodated in the printed line, but rather forms an irregular, ill-defined deposit. On the other hand, above a critical stage speed there is insufficient material in the impinging aerosol jet and the printed line becomes discontinuous. Figure 4.16(a) was gathered for a single focusing ratio, but the bounds

shown were not very sensitive to the focusing ratio and so the process window can be applied over a range of printing conditions. Focusing ratio does, however, have a dramatic impact on the line characteristics.

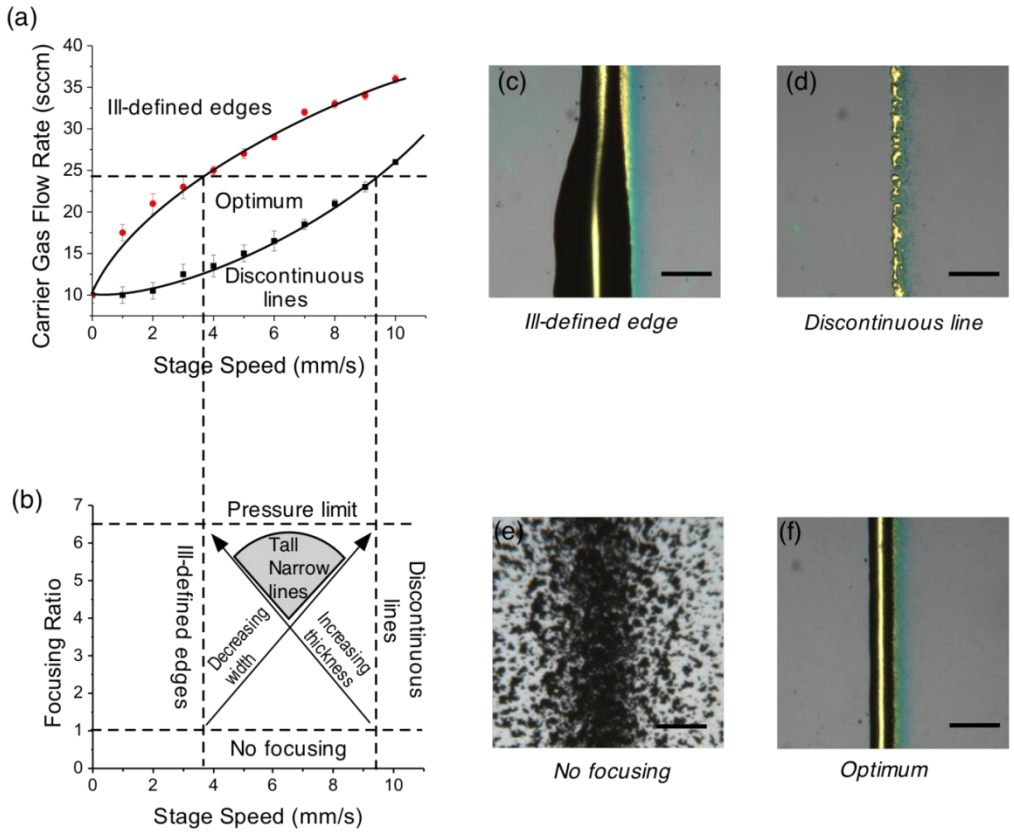

Figure 4.14 Operability window and process regime. (a) Upper and lower bounds on the carrier gas flow rate for each stage speed determined at a fixed focusing ratio (FR=3), and (b) operability window for a given carrier gas flow rate (24 sccm) with the region of tall and narrow lines highlighted. Optical microscope images showing (c) a line with an ill-defined edge printed at very low stage speed (1 mm/s), (d) a discontinuous line printed at very high stage speed (40 mm/s), (e) an incoherent line printed at focusing ratio less than 1 and (f) a line printed under optimized conditions. Each bar is 50 μm.

Figure 4.16(b) shows the effect of the focusing ratio and the stage speed at a constant carrier gas flow rate. The figure shows an example with a carrier gas flow rate of 24 sccm; the bounds on stage speeds from Figure 4.16(a) are translated to Figure 4.16(b).

The upper bound of the focusing ratio for the stated carrier gas flow rate is 6.5, limited by the maximum allowable pressure of the gases inside the nozzle. The lower bound is at FR=1, below which there are no coherent lines. The four bounds create an operability window. This process could be repeated for each of the carrier gas flow rates. The role of the focusing ratio is shown in the window. Higher focusing ratios are a key to getting both low line widths and high thicknesses. Too slow a stage speed increases the line width. However, too high a stage speed reduces both the line width and thickness. Therefore, each operability window has a domain for low line widths and high aspect ratio lines. Referring again to Figure 4.16(a), it is important to note that increasing the carrier gas flow rate has the effect of shifting the operability window to higher deposition speeds. However, the upper bound of focusing ratio (Fig. 4.16b) is also brought down simultaneously, thereby shrinking the operability window. Also, the operability window may require additional limits based on studies of the correlation between overspray and process variables.

A demonstration of lines printed in the “tall and narrow” regime of the operability window is shown in Figure 4.17. A grid of silver lines, 20 μm wide and about 2 μm tall, was printed in a single pass at a carrier gas flow rate of 24 sccm, focusing ratio of 6 and stage speed of 5 mm/s using a 200 μm nozzle.

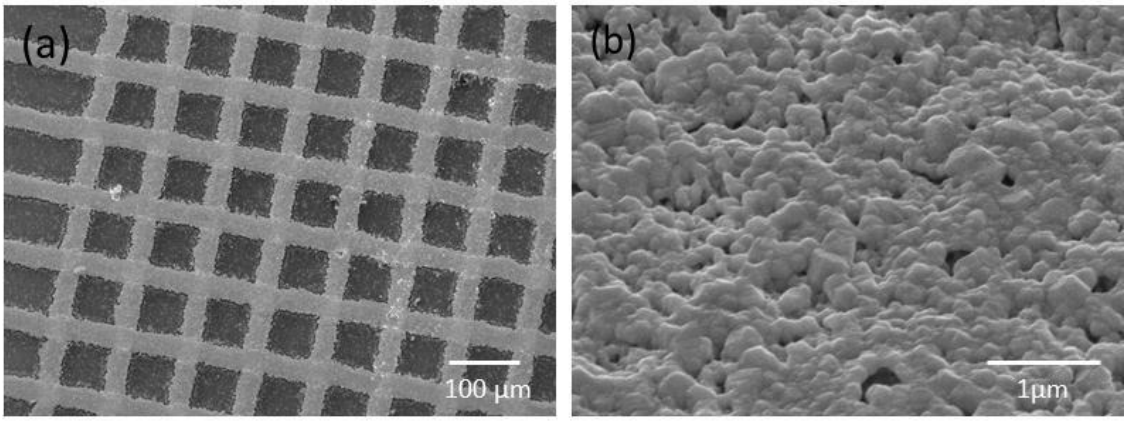

Figure 4.15 Characterization of sintered silver lines printed using optimized conditions. SEM micrographs showing (a) a grid of silver lines, 20 µm wide printed at carrier gas flow rate = 24 sccm, FR = 6 and stage speed = 5 mm/s and (b) surface topography revealing sintered silver nanoparticles.

4.7 Summary

A systematic study of aerosol jet printing process variables revealed conditions for creating tall and narrow conductive silver lines in a single pass, and a simple model based on continuity between the aerosol beam and the printed line was used to explain the impact of these adjustable parameters on the printed line geometry. The concept of focusing ratio, the ratio of the sheath gas flow rate to the carrier gas flow rate, was introduced and shown to be central to the printing process. The focusing ratio alone determines the line width so long as post-deposition spreading is minimal. Narrower lines are created at high focusing ratios. Line thickness was found to increase with focusing ratio and carrier gas flow rate, but decrease with stage speed. The decrease in thickness and hence the increase in the line resistance with increasing stage speed could be offset by increasing the carrier gas flow rate at fixed focusing ratio. To define printing conditions and optimize them for electrical function, an operability window was defined

and the regime for tall and narrow lines identified. Under the optimized conditions, lines as narrow as 20 μm with an aspect ratio of 0.1 were printed in a single pass.

Chapter 5 Planarization of High-Aspect Ratio Aerosol-Jet Printed Conductors

5.1 Background and Motivation

For both superior current carrying capacity and high-density circuitry, conductors with large cross-sectional areas and high aspect ratios (height/width) are necessary.[56] In Chapter 4, we described an optimization strategy to locate the regime for processing silver lines as narrow as 20 μm with aspect ratios greater than 0.1 using aerosol jet printing. However, high-aspect ratio printed conductors lead to topography on the substrate surface which is not ideal both for device processing. For example, in organic thin film transistors (OTFTs), high-capacitance gate dielectrics, which are critical to low operating voltages, are generally achieved by coating an ultra-thin polymer film or a self-assembled monolayer over a metal gate electrode.[29, 66-68] Also, a composite electrode formed by coating a thin layer of a conductive polymer over a metal grid appears to be a strong candidate for substituting indium tin oxide as the transparent electrode in organic solar cells and light-emitting diodes.[69-71]

An adapted version of this chapter is published as:
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Thus, many organic devices require overlaying a thin organic film on metal wires. Achieving uniform coating on surfaces with topography is challenging and coating defects can result in shorts, i.e., device failure. The problem is even more severe for printed conductors that have roughness of the same order as the thickness of the overlying film. From a manufacturing standpoint, topography on the substrate, courtesy of the printed electrodes, complicates the use of popular mass-production printing methods such as gravure or flexography, as these involve physical contact between the printing roll and the moving web. Furthermore, adhesion of printed metal tracks with plastic substrates is generally weak, necessitating an encapsulation layer for protection. For all of these reasons, developing methodologies for creating planarized flexible substrates with embedded, printed metallic tracks is essential.

There have been a few demonstrations previously to create embedded metallic tracks in flexible substrates. For example, a thermal imprinting-based strategy has been employed to create embedded silver meshes on plastic substrates.[86-88] In this technique, a flexible metallic master, wrapped around a heated roller, is pressed into a moving plastic substrate to form trenches. A silver ink is then filled into the trenches using a doctor blade. However, this method has several drawbacks. Firstly, the resolution of the embedded feature is dictated by the minimum feature size of the relief pattern on the metallic master. Engraving high resolution features on a metallic master requires specialized techniques, namely chemical etching, electromechanical or laser engraving, which are cost-intensive. Although 10 μm features or smaller have been achieved with a metallic master,[54, 86] ink filling becomes increasingly difficult at such small size scales.

Secondly, the doctor blade operation necessarily leaves behind some residue on the land, rendering it unfit for subsequent printing or coating. In principle, the residue may be minimized by creating a wettability contrast between the trench and the land but complete removal is difficult especially for large-area substrates. Finally, sintering of the ink inside the trenches leads to solvent removal and volume shrinkage, leaving behind non-flush metallic traces.

Another approach for obtaining embedded features is transfer printing, which is based on the transfer of features from a donor to a receptor substrate. For instance, Facchetti et al. used a 'hot press' based transfer printing method to embed metal lines into a polymeric film.[89] In this method, poly (methyl methacrylate) (PMMA), a thermoplastic polymer, is heated above its glass transition temperature (T_g) and pressed over metal lines, pre-patterned on a low energy donor substrate. After cooling below the T_g, the PMMA film is detached resulting in transfer of metal lines from the donor substrate to the polymer film. The authors report a high metal transfer yield (>90 %). However, the long time (~ 1 hr) required for hot pressing makes the process unsuitable for high-throughput manufacturing. Also, PMMA does not have the chemical and thermal tolerances that some of the subsequent processing steps in device manufacturing might entail. A similar technique, called template stripping, was employed to obtain a smooth, buried network of silver nanowires in a polymer, where a thick polymeric film is casted onto a silver nanowire film and subsequently peeled off from the donor substrate.[90, 91] Liu and co-workers obtained ultra-smooth silver electrodes by coating a photopolymer on top of evaporated silver electrodes on a silicon substrate, followed by a

stripping step.[92, 93] However, the thickness of the photopolymer was unusually high (~1mm) , which possibly assisted in its removal form the donor substrate.[94, 95] Galagan et al. built an organic solar cell on a substrate with a recessed grid of silver lines, but details of the embedding methodology were not revealed.[69] One main issue with template stripping is that easy delamination requires thick polymer coatings, which limits the bendability of the embedded electrodes.[6, 96]

Here, we report a simple method, called insertion, curing and delamination (ICD), for embedding high aspect ratio, printed silver lines into a thin polymer coating on a flexible substrate. ICD is based on the transfer of features from a donor to a receiving substrate, but unlike template stripping and transfer printing, consists of processing steps that are easily scalable for roll-to-roll (R2R) manufacturing. In particular, it employs low viscosity reactive liquids rather than thermoplastic melts (e.g. transfer printing), which facilitates rapid conformal contact with the donor substrate. Further, these reactive liquids are coated on high energy receiving substrates rather than low energy donor substrates (e.g. template stripping). This combination of features makes ICD compatible with thin coatings, a wide range of feature sizes, non-planar surfaces and high speed (short contact time) R2R steps. The transfer yield is 100 %, and the surface roughness of the embedded silver electrodes is less than 10 nm. The embedded electrodes exhibit excellent flexibility and robustness when subjected to mechanical stress, an essential requirement for truly flexible electronics.

5.2 Fabrication Scheme and Experimental Details

The fabrication of embedded silver electrodes via ICD involves a series of steps, schematically illustrated in Figure 5.1.

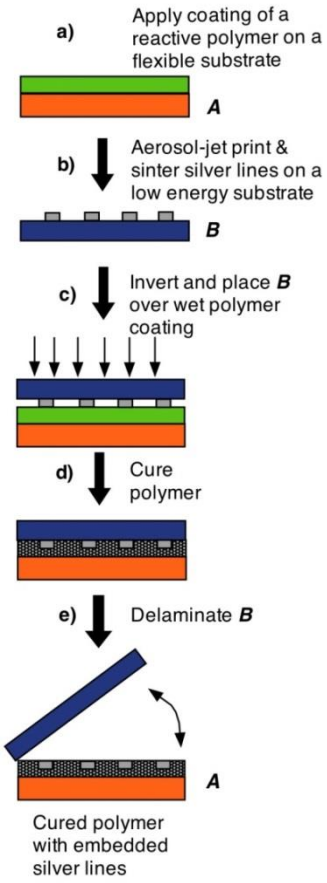

Figure 5.1 Scheme showing steps in insertion, curing and delamination (ICD). a) A liquid pre-polymer mixture of a reactive polymer is coated on a plastic substrate, **A**. b) Silver patterns are aerosol-jet printed and sintered on a low energy flexible substrate, **B**. c) **B** is inverted and lowered onto the wet polymer coating on **A**, ensuring complete insertion of the silver patterns and no air entrapment. d) The pre-polymer mixture is cured. e) **B** is delaminated, leaving the silver patterns flush with the surface of the polymer coating on **A**.

Initially, a thin (~ 10 μm) coating of a thermally cross-linkable, flexible epoxy pre-polymer mixture is applied to a polyimide substrate. Silver electrodes are aerosol-jet printed and sintered on a different low surface energy, flexible substrate. Silicone-coated

polyethylene terephthalate (s-PET) and silane-treated silicon were chosen for this work. This printed substrate is then inverted and lowered onto the pre-polymer mixture at an angle that allows the liquid pre-polymer to fill around the silver lines and air to escape. Subsequently, the pre-polymer mixture, currently sandwiched between the two substrates, is thermally cured forming a solid cross-linked film. Following complete cure, the top substrate is manually delaminated, leaving the silver patterns embedded in the epoxy coating. The experimental details are as follows:

Printing of Silver Lines. A 125 μm thick silicone-coated PET film (8310 Release Coating, Saint-Gobain Performance Plastics Ltd.) and a silane-treated silicon wafer were used as donor substrates. For silane-treatment, the wafer was placed in a dessicater with 2 mL trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl)silane (FOTS, Sigma Aldrich) solution. The dessicator was then pumped down to 1 torr pressure to allow the FOTS solution to evaporate. The sample was left overnight for complete coverage. The printed lines were sintered at 150° C for 1 hr in an atmospheric oven. s-PET was slowly cooled to room temperature and then inserted into the wet polymer coating. s-PET softened at 150°C but restored its original stiffness upon slow cooling to room temperature.

Coating Preparation. For preparing the coating solution, the epoxy monomer and its curing agent (Epotek 310-M1) were thoroughly mixed in a 1.8:1 weight ratio, respectively and vacuum degassed for 10 min. A wire wound rod was used to form a ~10 μm thick coating on a 75 μm thick polyimide film (Kapton, American Durafilm). Prior to coating, the substrate was cleaned with acetone, methanol, isopropyl alcohol and deionized water.

Insertion, Curing and Delamination. The printed substrate was inverted and slowly lowered onto the coated substrate at an angle approximately greater than 30° with the horizontal. Upon insertion of the silver features by gentle pressing, the coating was cured at 120 °C for 30 min on a hot plate. After complete cure, the top substrate was delaminated manually to obtain embedded silver lines in the epoxy coating.

5.3 Characterization of Embedded Conductors

The flushness of the silver line with the epoxy coating was verified using scanning electron microscopy (Figure 5.2).

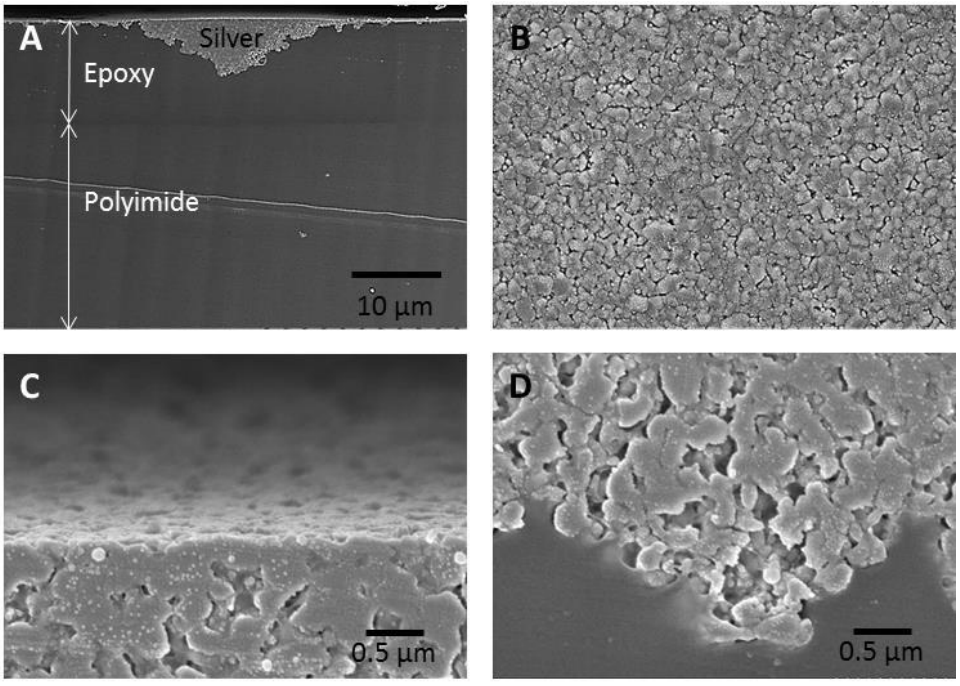

Figure 5.2 Scanning electron micrographs revealing a) a silver line flush with an epoxy coating on a polyimide substrate, b) surface topography of an embedded silver line, and extent of sintering of the silver nanoparticles near the c) top and d) bottom of the embedded line.

Figure 5.2a displays a cross-section scanning electron microscope (SEM) image of a 40 µm wide, 6 µm tall (maximum height) silver line embedded in a 10 µm thick epoxy

coating on a polyimide substrate. The flat, top surface of the silver metal flush with the polymer coating is clearly observed. Higher magnification images show uniform sintering across the cross-section of the lines (Figure 5.2c, d). The printed lines were annealed in an atmospheric oven, which provided uniform sintering conditions throughout the cross-section. Because of the low viscosity of the pre-polymer mixture (~315 mPa·s), the epoxy pre-polymer mixture could minutely track the footprint of the printed line, forming 'microscopic fingers'. As a result, the intrinsically fragile printed silver line is now firmly anchored by the polymer matrix.

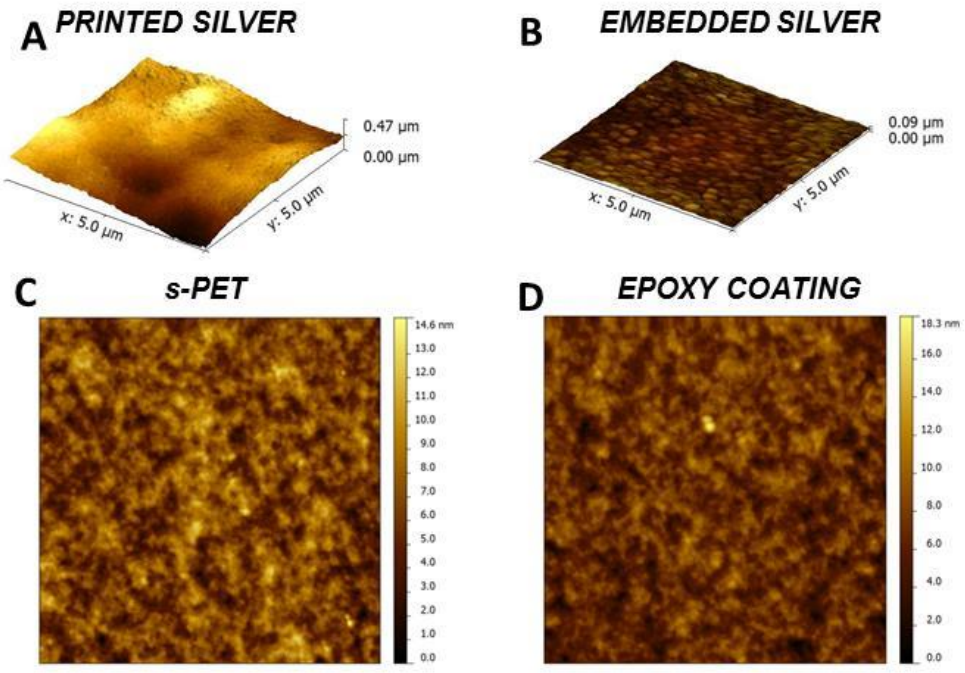

Figure 5.3 AFM tapping mode height images of a) printed (and sintered) silver (root mean square (rms) roughness 81.8 nm), b) embedded silver (rms roughness 8.3 nm), c) s-PET (rms roughness 1.80 nm) and d) epoxy coating (rms roughness 1.83 nm). Scan areas in both c and d are 25 μm^2.

An added advantage of ICD is the smoothness of the embedded features. Figure 5.2b displays the surface morphology of embedded silver, showing absence of any major topographical features. However, nanoscopic pores due to incomplete sintering of the silver nanoparticles are also apparent. The root mean square (rms) roughness characterized using atomic force microscopy was 81.8 and 8.3 nm respectively for the as-printed and embedded silver, over a 25 μm^2 area (see Figure 5.3a,b). Due to the low surface roughness, the embedded silver has a shiny, mirror-like appearance, whereas the as-printed silver appears dull.

In ICD, the structure of printed silver is inverted such that the bottom surface comes to the top. Therefore, surface roughness of embedded silver depends on the 'template' on which it is initially printed.[97] The rms roughness of our template, s-PET, over a 25 μm^2 area is found to be 1.80 nm (Figure 5.3c). The flatness and smoothness of s-PET is transferred to silver, resulting in topography-free, smooth embedded features. However, the presence of nanoscopic pores on the surface leads to a slight increase in its roughness compared to s-PET. The rms roughness of the revealed surface of the epoxy coating over a 25 μm^2 area is 1.83 nm, which matches well with the roughness of s-PET (Figure 5.3d). Also, this surface is free from any residue from the delamination process, which makes it ideal for fabrication of electronic devices.

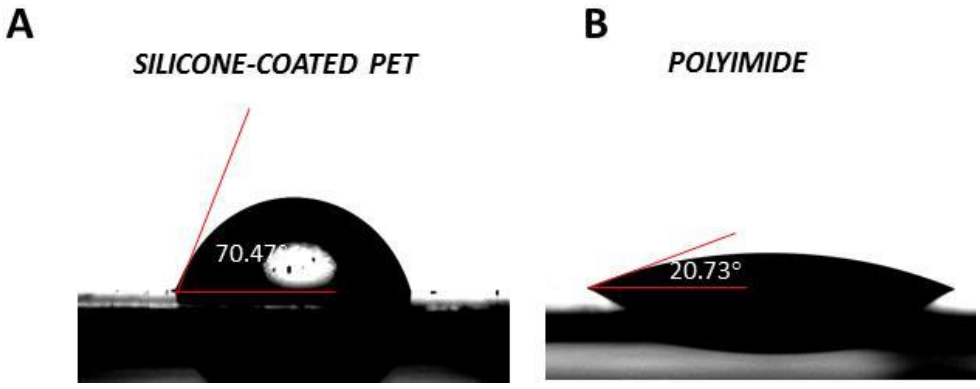

Figure 5.4 Comparison of contact angle of epoxy pre-polymer mixture on a) silicone-coated PET and b) polyimide substrates, suggesting stronger adhesion of the cured epoxy with the latter.

Central to ICD is the delamination step, where two important physical processes occur simultaneously. Firstly, the interface between the donor substrate and the epoxy coating is cleaved, generating two new surfaces. The wettability of liquid pre-polymer mixture on a substrate provides a good estimate of the interactions between the cured film and the substrate. The contact angles of the epoxy pre-polymer mixture on s-PET and polyimide substrates were found to be 70.5° and 27.4°, respectively (Figure 5.4). Quantitatively, the work of adhesion, W_A, of a liquid with a solid is expressed as

$$W_A = \sigma_L (1 + \cos\theta) \qquad (5.1)$$

where σ_L is the surface tension of the liquid and θ is the contact angle of the liquid with the solid. Because of a lower value of W_A, s-PET could be delaminated from the cured epoxy coating by gentle peeling. On the other hand, owing to its strong adhesion with the epoxy, polyimide served as a supporting film for the thin coating, forming a robust composite substrate.

The second process that occurs during delamination is transfer of silver from the donor substrate to the epoxy coating. A high transfer yield requires a weak adhesion with the donor, which is possible with a low surface energy substrate. Both s-PET and silane-treated silicon qualify as low surface energy substrates, but printing continuous features on low energy surfaces is challenging due to ink de-wetting.[98] We employed aerosol-jet printing (AJP) to overcome this problem. In AJP, a silver nanoparticle ink is atomized to generate an aerosol mist. The silver nanoparticles, entrained in the aerosol droplets, are transported by a flowing carrier gas to a print-head, where an annular sheath gas focuses the incoming stream forming a high-speed jet. When the jet impinges a moving substrate, the aerosol droplets coalesce to form a liquid line. Due to the small (1-5 μm) size of the freshly generated aerosol droplets, rapid evaporation of solvent occurs during flight, leading to a significant increase in the solids loading and therefore viscosity of the aerosol droplets in the impinging jet. The high viscosity of the coalesced liquid diminishes the role of substrate's surface energy in determining the wetting characteristics and uniquely allows printing on a low energy surface.

Figure 5.5 demonstrates the versatility of ICD. Figure 5.5a shows the word "EMBEDDED" written using a combination of multi-oriented silver lines, buried in an epoxy coating using ICD, suggesting that the silver transfer is independent of orientation of the silver lines (with respect to the delamination direction). Due to the ease of the constituting steps in ICD, we could fabricate an embedded hexagonal grid of silver lines on a large area, flexible substrate (Figure 5.5b). To demonstrate the minimum feature size attainable using ICD, an array of 25 μm wide silver lines with a line-spacing of 20 μm

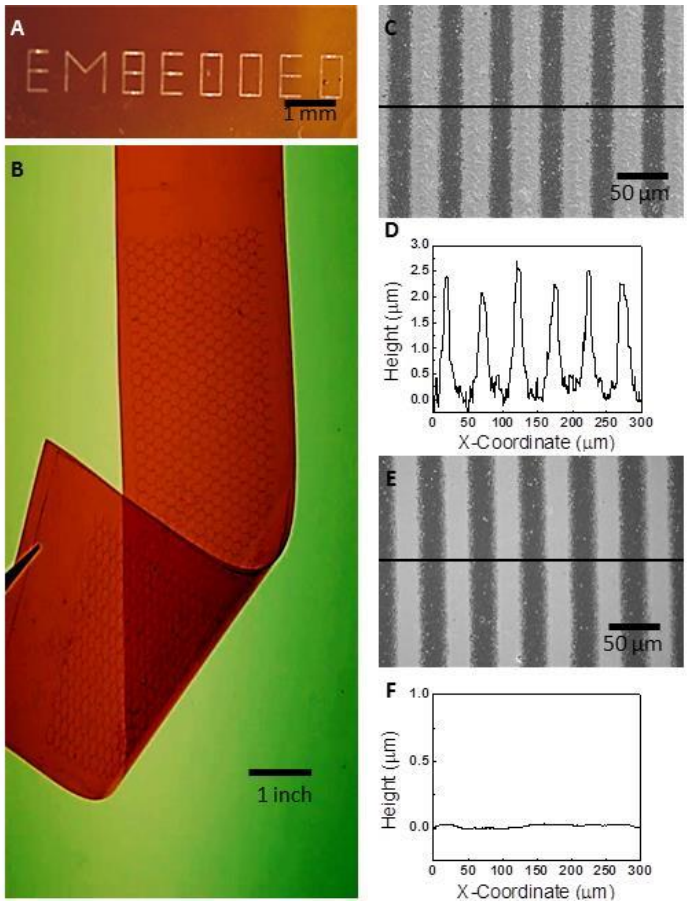

Figure 5.5 Versatility of ICD. a) The letters "EMBEDDED" written using 50 µm wide silver lines, embedded in an epoxy-coated polyimide substrate. b) An embedded hexagonal grid of 40 µm wide silver lines on a 10 in. long 3 in. wide substrate, demonstrating the scalability of ICD. c) SEM image showing an array of silver lines (width: 25 µm, line spacing: 20 µm) on a silicone-coated PET substrate and d) profilometric traces illustrating the cross section of the lines. e) SEM image displaying the same lines upon embedment and f) profilometric scan confirming the absence of topography on the substrate.

was printed on s-PET and characterized using SEM and profilometry (Figure 5.5c, d). After embedding, the same lines appeared much smoother than their initial, as-printed form (Figure 5.5e), and were also completely flush with the surface of the epoxy (Figure 5.5f). As mentioned earlier, the low viscosity pre-polymer mixture could easily fill the space between narrowly-spaced lines, yielding a flat surface. Interestingly, even the tiny

(0.1-0.5 µm) overspray clusters on either side of the lines, characteristic of AJP, were also transferred. It is worthwhile mentioning that the minimum feature size is not limited by any of the processing steps in ICD, but depends on the resolution of the printing technique. ICD was found to be equally effective for complex patterns such as a 30 ×30 grid, fabricated using 20 µm wide silver lines with a 200 µm pitch (Figure 5.6).

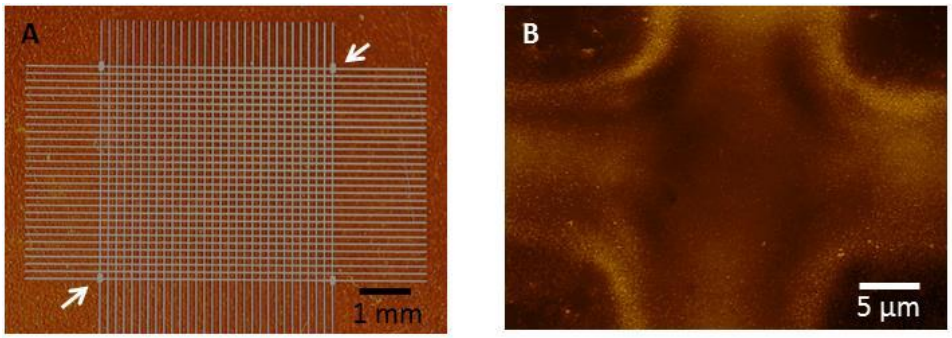

Figure 5.6 a) Optical microscope image of an embedded square grid of silver lines (width: 20 µm, line spacing: 160 µm) comprising of 900 cross-overs. The measured electrical resistance between the highlighted points of the grid was 30.01Ω, close to its as-printed value. b) AFM tapping mode height image revealing a buried cross-over in the above grid. Image height range is 100 nm.

5.4 Electrical Characterization and Bending Tests

To measure the transfer yield, we investigated the change in electrical resistance of silver lines before and after ICD. Figure 5.7a shows the distribution of electrical resistance of 25 silver lines (each 5 mm long) printed and annealed on s-PET. Within error, no change is observed in the electrical resistance after embedding (Figure 5.7b), indicating 100 % transfer. After delamination, the donor substrate was examined under an optical microscope, and was completely free from silver residue. The same substrate was used multiple times without any substantial decrease in the transfer yield. We also found

the transfer yield did not vary much with different epoxy coating thicknesses, and the minimum coating thickness is limited by the thickness of the silver features.

To investigate mechanical flexibility and durability of the embedded electrodes, we examined the change in electrical resistance of five embedded electrodes subjected to repeated bending cycles at two different radii of curvature (*r*). Mechanical bending of embedded electrodes was performed by attaching the substrate to a stationary block and a sliding stage, connected to computer-controlled positioning equipment (Aerotech Co.). The substrate was bent to a certain radius and restored to its initial state at a rate of 10 cm $s^{-1}$to complete one bending cycle. The "bending" radius was controlled by the displacement of the sliding stage. Electrical resistance of the electrodes was measured for every 2000 cycles for two different bending radii. As shown in Figure 4d, for *r* of 0.5 cm (~ 1.2 % tensile strain), silver electrodes subjected to 10,000 repeated bending cycles exhibited only a slight increase (1.2-fold) in their electrical resistance relative to the initial value. Optical microscope images revealed a few voids in these electrodes that were not seen in the initial sample (Figure 5.7d i, ii). For *r* of 0.1 cm (6.2 % strain), the electrical resistance increased gradually after many cycles, with a 2.4-fold increase after 8000 cycles. All the electrodes undergo cracking and failure after 10,000 cycles (Figure 5.7d iii). Notably, bending performance of our embedded electrodes is not too different from as-printed thin silver electrodes reported in the literature.[99]

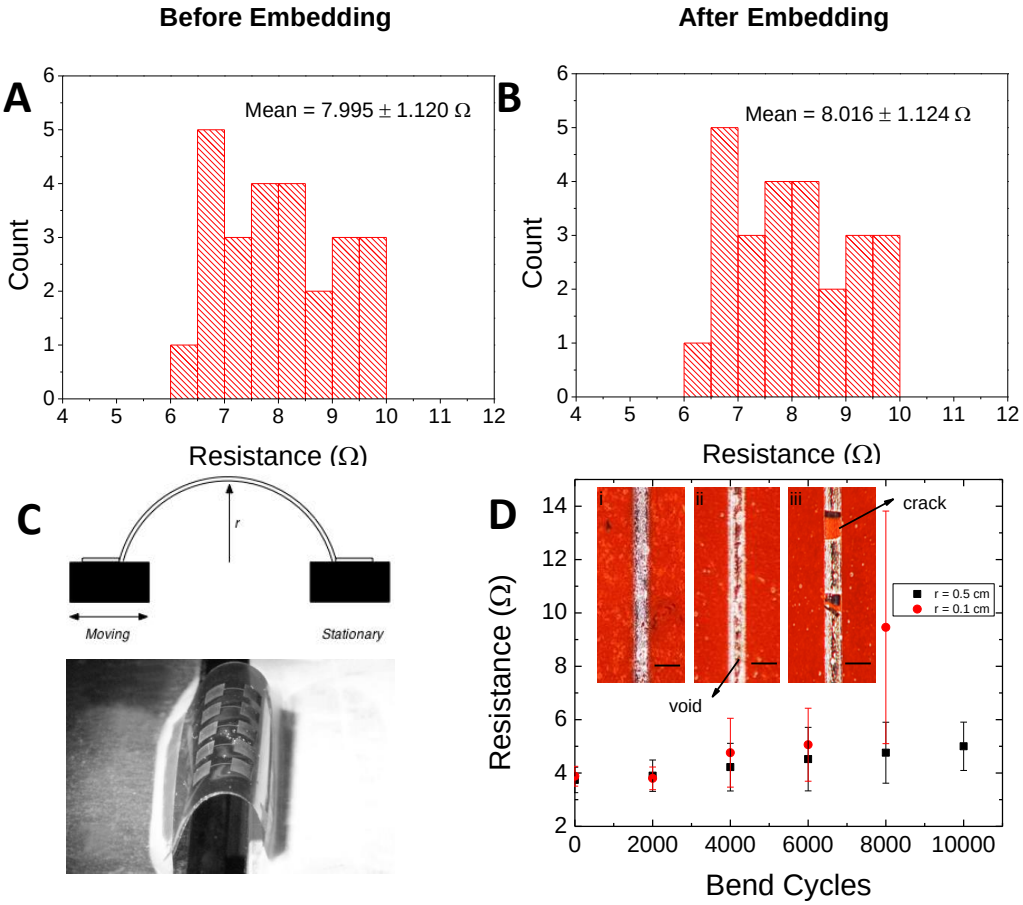

Figure 5.7 Histograms showing the distribution of electrical resistance of 25 silver lines a) before and b) after embedding. No significant change in the average resistance is observed. c) Experimental set up for the bending test. The substrate, attached to a stationary block and a sliding stage, is bent to a certain radius and restored to its initial state at a rate of 10 cm s^{-1} to complete one bending cycle. d) Electrical resistance of the embedded silver electrodes as a function of bending cycles under different bending radii (0.5 cm and 0.1 cm). Inset: Optical micrographs of embedded silver lines i) before bend cycles, and after ii) 10 000 bending cycles for r = 0.5 cm and (iii) 8000 bending cycles for r=0.1 cm. Scale bar is 50 µm.

A special feature of ICD is the ability to fabricate embedded features in non-planar surfaces. As a demonstration, we created wells with sloped sidewalls in a silicon wafer using conventional photolithography and wet-etching processes. Subsequently, the surface of this wafer was treated with a silane to make it low-energy. Silver lines were

aerosol-jet printed across a well in the wafer. The relatively large (2-5 mm) working distance in AJP enables uniform printing across the variable topography. Upon subjecting this substrate to ICD, a plateau in the epoxy coating is obtained with an embedded silver line running across it. Electrical measurements showed that the embedded silver line was conductive despite transcending an abrupt topography on the substrate. Scanning electron microscopy further confirmed a continuous transition of the embedded silver along the sloped part of the plateau (Fig. 5.8).

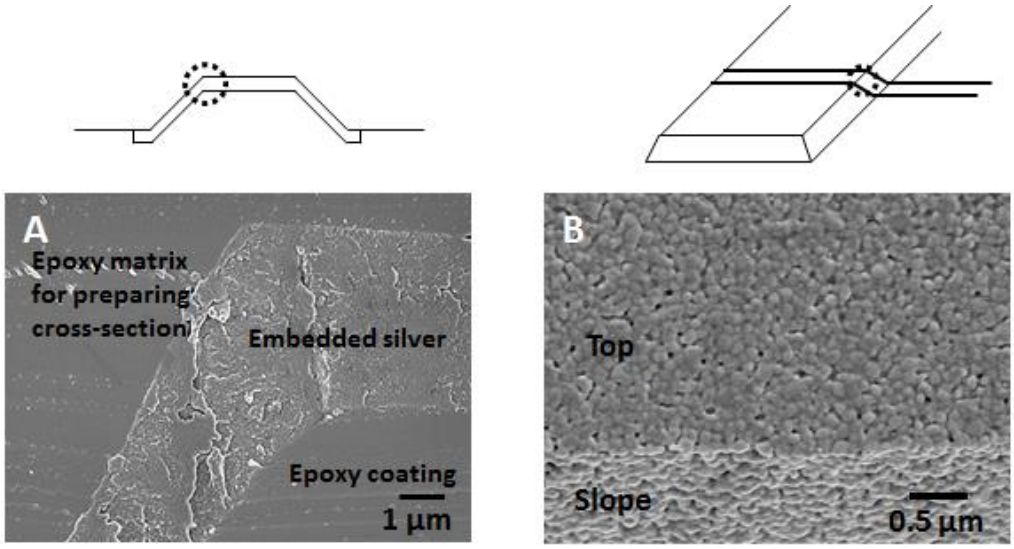

Figure 5.8 ICD on non-planar surfaces. a) Cross sectional SEM image displaying an embedded silver line over a sloped step. b) Top view SEM image showing the transition of the embedded silver line near the edge, free from cracks or other discontinuities.

ICD should be promising for implementation in a continuous process employing printing and coating techniques. For example, high aspect ratio silver lines can be printed on a donor substrate using AJP or screen printing. The printed lines can be sintered rapidly with a flash sintering method.[100] Conventional industrial coating methods such as slot-die, curtain or roll coating can be used to apply a thin coating of a reactive

polymer. In this work, we employed a thermally curable polymer, but a similar, fast-curing photo-curable polymer should be equally effective.[101] The delamination step is performed routinely in continuous industrial processes, e.g. tape casting of ceramics.[102] Because of the reusability of the donor substrate, ICD may be performed in a continuous loop, thereby maintaining the benefits of additive manufacturing.

5.5 Conclusions

In conclusion, we have demonstrated a simple method for obtaining flexible substrates with embedded, printed silver lines. The unique ability of aerosol-jet to print on low energy surfaces enables successful transfer of printed features from a low energy donor substrate to a polymeric coating on a receiving substrate. The polymer coating is strongly adhered to a supporting film, which lends mechanical robustness to the composite substrate and allows workability with thin coatings. The transfer yield is 100 %, independent of size and orientation of the printed features or thickness of the coating. Importantly, surface roughness of the embedded electrodes is an order of magnitude lower than the as-printed electrodes. The embedded electrodes exhibit tremendous flexibility and resilience, not showing a significant degradation in electrical performance after thousands of bending cycles. Another attractive feature of ICD is the ability to create continuous embedded metal lines in non-planar substrates. Because all constituting steps are additive and rapidly processable, ICD should be adaptable as an R2R manufacturing process.

Chapter 6 Low-Resistance, High-Resolution Planarized Conductors by Inkjet Printing and Electroless Deposition

6.1 Background and Motivation

Conductive wires are essential elements of electronic circuitry, and high-resolution conductive traces are crucial for achieving high-density devices.[1, 103] So far, we have explored aerosol-jet printing which can process lines as narrow as 20 μm under optimized conditions. This is a significant advancement over minimum feature sizes obtainable from other printing techniques. However, high-performing electronic devices necessitate even further improvements in resolution. Decrease in line width is concomitant with increase in resistance. The effect is even more pronounced for printed conductors which have much higher volume resistivity. Also, large-area electronic circuitry requires longer wires, which naturally have higher resistances.

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In order to offset resistive losses without sacrificing the high-resolution, printed conductors need to have increased heights or high aspect ratios (height/width) to enhance the cross-sectional area. As discussed in Chapter 3, a practical goal for printed electronics is to process conductors with an aspect ratio > 0.1 with line widths smaller than 20 μm. Furthermore, the ability to embed high-aspect ratio wires within plastic substrates to yield planarized circuitry is highly desirable for subsequent processing steps (e.g., coating a thin organic film on top of the wires).[69, 89, 104, 105]

High throughput printing methods, such as flexography, gravure, offset and screen printing, are widely used for patterning large-area electronic devices.[106] However, a general drawback of these techniques is poor-resolution, low-aspect ratio (< 0.1) and inhomogeneities in layer thickness. Recently, high-resolution (< 10 μm) gravure-printed Ag lines have been demonstrated,[54, 55] but line consistency remains a concern, particularly for these fine features. Inkjet printing of metal lines from a diverse array of inks, including, nanoparticle, metal-organic decomposition, or particle-free solutions has also been demonstrated.[65, 107-109] However, the minimum width of inkjet and aerosol-jet printed features is ~ 20 μm,[56] due to limits on droplet diameter and spreading on the substrate upon impact. Although Sekitani et al.[24] have demonstrated 2 μm Ag lines using sub-femtoliter inkjet-printed droplets, multiple passes were required to obtain the desired metal content in the wires.

Here, we present a robust, low-temperature and liquid-based patterning method for obtaining high-resolution and high-aspect ratio metal lines embedded in a plastic substrate that combines three steps: (1) imprint lithography (I),[110] (2) inkjet printing

(P),[111] and (3) electroless plating (P).[112] We refer to this method by the acronym, IPP. In IPP, firstly, microchannels connected to reservoirs are molded into a coated thermoset material using imprint lithography. Next, using a drop-on-demand inkjet printer, a reactive Ag ink is delivered into the reservoir which flows into the microchannel via capillarity resulting in a thin Ag trace upon annealing. Subsequently, the channel is filled completely with metal by immersing the substrate in a Cu electroless plating bath, where the Ag inside the microchannels serves as a catalyst for selective deposition of Cu.

6.2 Fabrication Scheme and Experimental Details

Figures 6.1 and 6.2 shows a series of steps involved in the IPP process. First, a master template was fabricated by etching reservoirs and channels in a silicon substrate (Fig. 6.1a). The width of the channels ranged from 1.5-100 μm, whereas the reservoirs are 400 μm in diameter. The master template, in turn, was used to create a polydimethylsiloxane 'daughter' stamp (Fig. 6.1b). The stamp was then pressed into a curable epoxy prepolymer liquid coated on a polyethylene terephthalate (PET) film pre-treated by plasma to enhance the adhesion between the epoxy coating and the substrate. The prepolymer was cured using UV illumination, following which the stamp is delaminated to yield imprinted reservoirs and channels on the epoxy-coated PET substrate. Next, a reactive silver ink[109] was deposited into the reservoirs using a drop-on-demand inkjet printer, where it was wicked along the channels via capillary forces. Unlike flat substrates, spreading of this low viscosity ink was confined only to the width of the channel. Upon drying and annealing of this ink, a thin deposit of Ag was left behind in the reservoir and the channel.[113]

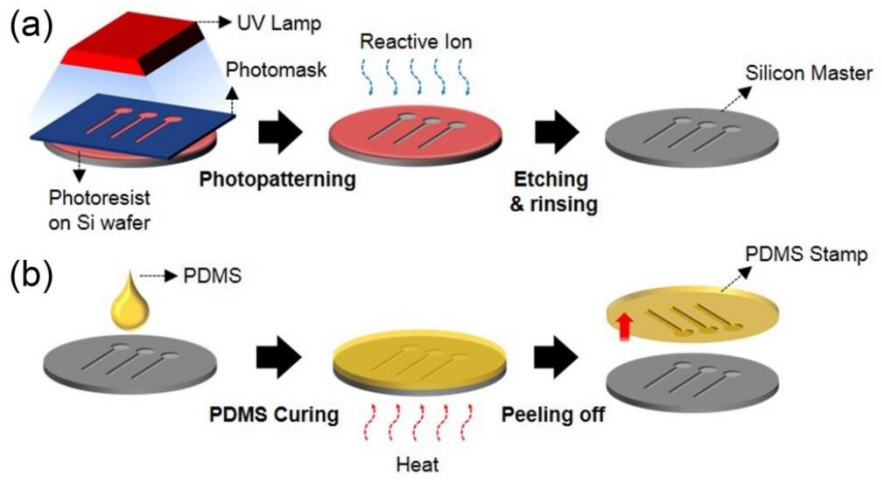

Figure 6.1 Fabrication of master template and PDMS daughter stamp**.** (a) Fabrication of a master template (containing reservoirs attached to microchannels) using reactive-ion etching on a photolithographically-patterned silicon substrate. (b) Creation of a PDMS stamp by thermally curing the PDMS pre-polymer mixture atop the master template, followed by delamination of the cured stamp.

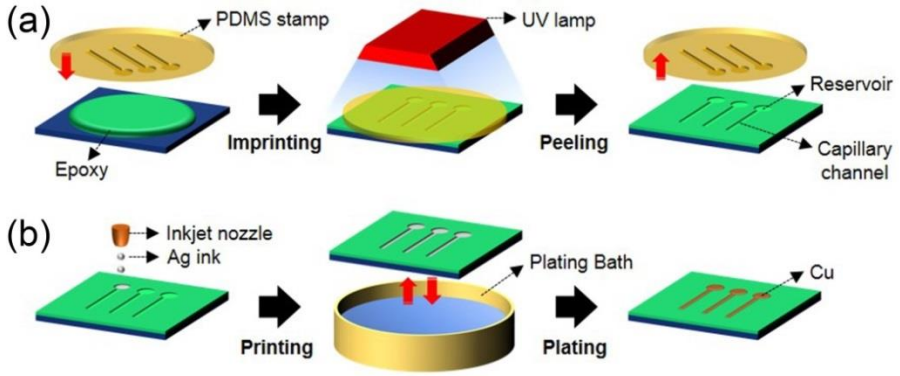

Figure 6.2 IPP process steps. (a) Fabrication of a flexible, imprinted substrate by pressing a PDMS stamp into a PET substrate coated with a curable epoxy pre-polymer, solidifying the coating by UV-illumination, and peeling the stamp after the coating is completely cured. (b) Creation of high-resolution and high-aspect ratio metal wires by first inkjet printing of a reactive Ag ink into the micro-imprinted reservoirs. Capillary flow drives the ink into and along the micro-channels. Finally, the channels are completely filled with metal by immersing the printed substrate in a Cu electroless plating bath.

Next, the printed channels are filled completely by immersing the substrate in a Cu electroless plating bath, where the Ag inside the microchannels serves as a seed layer for selective deposition of Cu. In the final configuration, the filled microchannels serve as conductive wires, whereas the reservoirs serve as contact pads (Fig. 6.3).

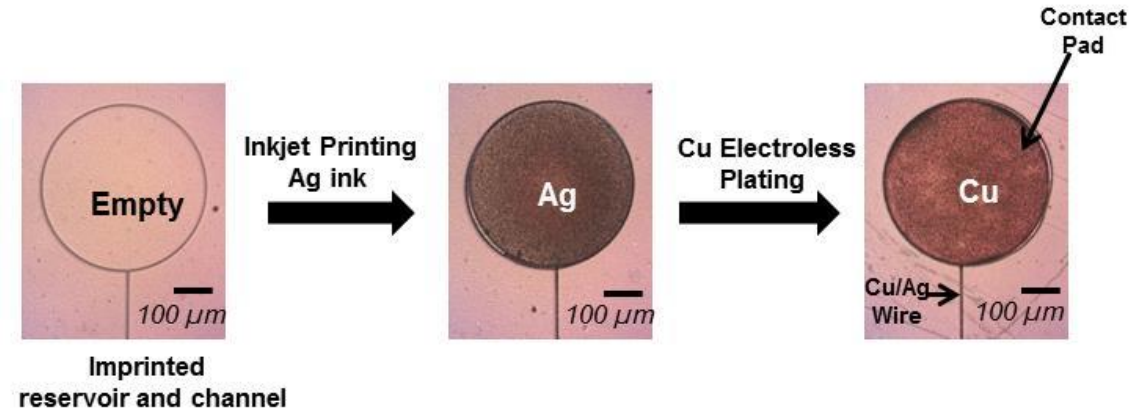

Figure 6.3 Fabrication of wires and contact pads using the IPP process. (a) A reservoir and a channel created in a plastic substrate using imprint lithography. The width of the channel is 5 µm. (b) Ag metal inside the imprinted cavity produced from inkjet-printing reactive Ag ink into the reservoir and wicking of the ink into the channel. Ag metal was obtained after drying and annealing of the ink. (c) Cu growth atop Ag metal after immersing the substrate in a Cu electroless plating bath. In a circuit, the filled reservoir serves as a contact pad, whereas the filled channel is a conductive wire.

Detailed experimental procedures are as follows.

Master Template Fabrication: Silicon wafer (100) was first cleaned by a Piranha solution (5:1 H_2SO_4 with H_2O_2) for 20 min at 120° C, and then rinsed with DI water and dried. The wafer was prebaked at 115° C for 1 min. Photoresist (Shipley 1813) was spin coated (3000 rpm) on the silicon wafer for 30 s, followed by softbake at 110°C for 1 min to drive off solvents. A pre-designed mask was placed above the photoresist-coated silicon wafer, and exposed to UV light for 5 s in an ultraviolet exposing system (Karl Suss

MABA6). The silicon wafer was immersed in the developer solution for 1 min, rinsed with DI water and dried. The patterned silicon wafer was then dry etched to a required depth by reactive ion etching (SLR 770 Deep Trench Etcher). The etch rate was 0.9 μm min^{-1}. Lastly, the patterned silicon wafer with reservoirs and channels was washed in acetone and isopropyl alcohol to remove the photoresist and rinsed with DI water. The patterned silicon wafer was placed in a hexamethyldisilazane (HMDS) vapor bath for 2 h.

Polydimethylsioxane (PDMS) Stamp Fabrication: For preparing the PDMS stamp, PDMS monomer and its curing agent (Dow Corning, Sylgard-184) were thoroughly mixed in a 10:1 weight ratio, respectively, and vacuum degassed for 30 min. The master template substrate was placed in a plastic petri dish and 30 g of the PDMS pre-polymer mixture was poured over the substrate and allowed to level out. The pre-polymer mixture was then cured in an atmospheric oven at 60°C for 12 h. After completely curing, the PDMS stamp was delaminated from the silicon master template. The stamp was then placed in an oven at 120°C for 2 h to enhance its modulus.

Imprinted Flexible Substrate Fabrication: A 25 μm thick coating of a flexible, UV-curable polymer, NOA-73 (Norland Products Inc.), was applied to a 75 μm thick PET substrate. Prior to the coating, the PET substrate was air-plasma treated for 3 min to promote the adhesion of the coating. The PDMS stamp was inserted into the liquid coating and pressed using a glass roller to drive out any entrapped air bubbles at the coating-stamp interface. The coating was cured by exposure to UV light for 20 min. Following complete cure, the stamp was delaminated, leaving behind imprinted features in the NOA/PET substrate.

Inkjet Printing of Ag Ink: An 80 µm diameter drop-on-demand inkjet nozzle was employed for printing the Ag ink. The optimized waveform consisted of a rise time of 5 µs, dwell time of 20 µs and fall time of 5 µs, drive voltage of 100 V and jetting frequency of 360 Hz. The diameter of a single ejected droplet was about 65-75 µm. The nozzle was aligned to an imprinted reservoir, and a fixed number of droplets were delivered to the reservoir. Prior to printing, the imprinted substrate was air-plasma treated for 3 min for surface energy enhancement to facilitate capillary flow. The printed substrate was annealed on a hot plate at 100°C for 5 min.

Cu Electroless Plating: The Cu electroless plating solution contained 2.704 g of $CuSO_4 \cdot 5H_2O$, 8.15 g of ethylenediaminetetraacetic acid disodium salt**,** 3.25 g of NaOH, 100 mL of DI water, and 25 mL of an aqueous solution of formaldehyde (37 % by weight). The temperature of the bath was maintained at 55°C. The printed substrate was kept in the bath for a known amount of time and taken out, rinsed with DI water, and dried using an air gun.

6.3 Capillary Flow of Silver Ink in Open Microchannels

A particle-free, reactive Ag ink was used to create the seed layer, whose rheological properties were tailored to simultaneously facilitate inkjet printing and capillary flow. This reactive silver ink was an aqueous silver-amine complex in the presence of a reducing agent (formic acid) that decomposes upon heating to leave behind a pure metallic silver trace. This complex was tuned for inkjet printing by increasing the molecular weight of the primary amine chelator compared to ammonia used in the original publication.[109] The increased steric hindrance of the complex results in an ink in

which the surface tension and viscosity can be tuned. The ink had respective values of 24-27 mN/m and 10-12 cP. This ink was devoid of any organic binder. The surface of Ag metal obtained post-annealing is free from any organic residue, hence serving as an excellent seed layer for Cu growth, as discussed later.

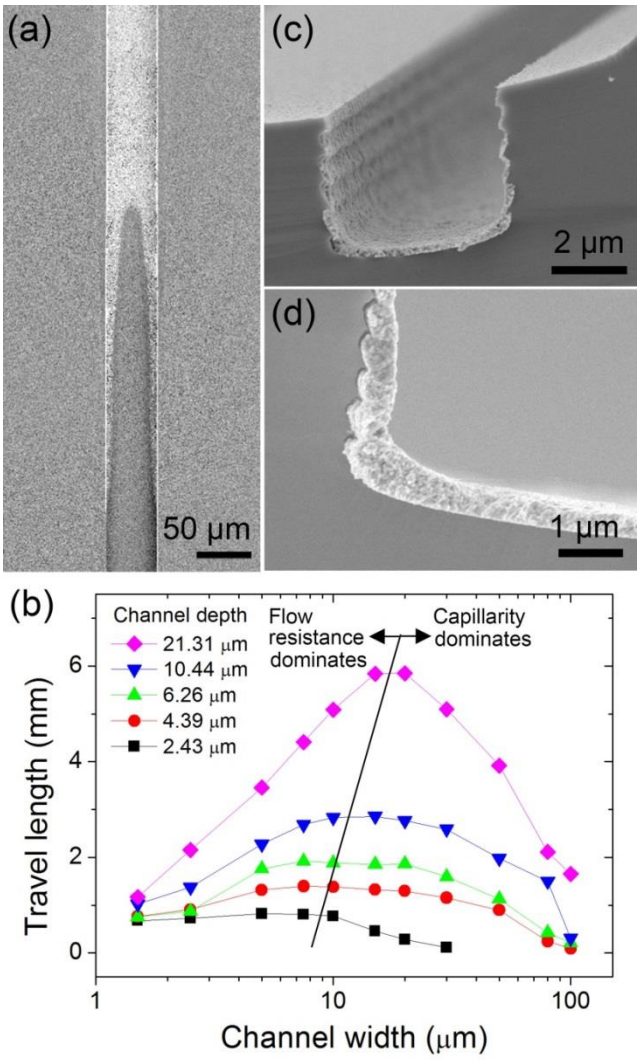

Figure 6.4 Capillary filling of Ag ink in microchannels. (a) Top-view scanning electron micrograph (SEM) showing the termination point of the Ag ink inside a 50 µm wide, 10 µm deep imprinted channel on a plastic substrate. (b) Variation of Ag ink travel length with different channel depths and widths. The total length of the channels was 5 cm. Cross-sectional SEM displaying (c) Ag metal deposited on the sidewalls and bottom of a 5 µm wide channel post drying and annealing of the ink, and (d) region of increased Ag thickness near one of the bottom corners of a channel.

Figure 6.4a shows a plan-view scanning electron micrograph (SEM) of a 50 µm wide channel filled with Ag metal. The Ag ink remained confined within the channel during the wicking process. The controlled nature of capillary flow ensured that the lands are residue-free, which is an advantage over other trench-filling methods (e.g. doctor blade filling[86, 87]). The two leading edges near the termination of flow are also distinguishable, suggesting that for the entire duration of capillary flow, the bulk liquid trailed the liquid along the sidewalls. As the Ag ink in the reservoir approached the capillary channel, the liquid was first imbibed along the two corners of the channel forming a curved meniscus, leading to a pressure gradient between the reservoir and the channel (i.e., the capillary pressure, ΔP).[114] Capillary pressure in the direction of flow in an open, rectangular channel can be described as[115]

$$\Delta P = \gamma(\cos\theta)\left(\frac{1}{d} + \frac{2}{w}\right) \qquad (6.1)$$

where γ is the surface tension of the liquid, θ is the contact angle of the liquid on the walls of the channel, and d and w are depth and width of the channel, respectively. This pressure gradient drives ink flow down the channel against the competing flow resistance arising from friction at the channel walls.[116]

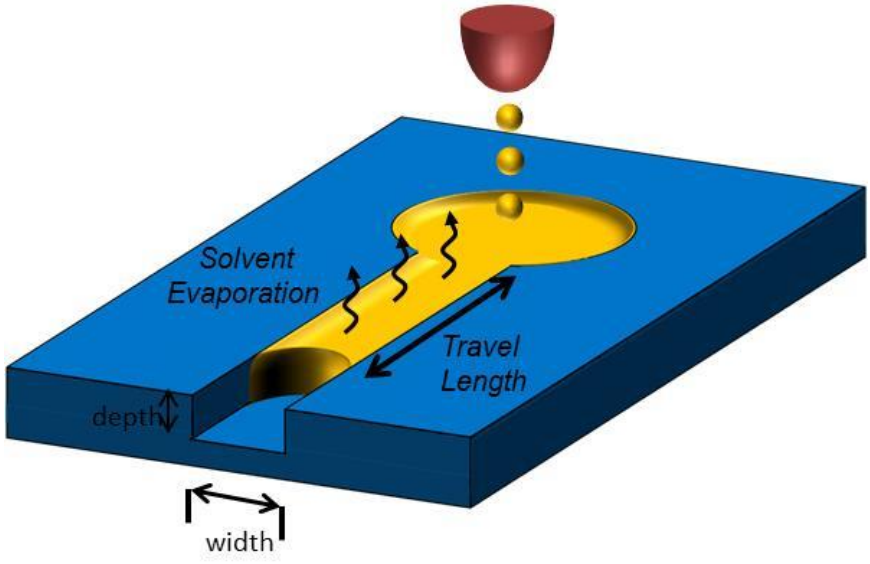

Figure 6.5 Schematic of the experimental set up for investigating the influence of channel geometry on travel length of reactive Ag ink. The ink, with a volume equivalent to reservoir volume, is flowed within 5 cm long, open channels of varying widths and depths.

To investigate the effect of channel geometry on the travel length, the reactive Ag ink, with a volume equivalent to reservoir volume, was introduced and flowed within 5 cm long channels of varying widths and depths (Fig. 6.4b and Fig. 6.5). Beginning with the widest channels, as shown on the right in Figure 6.4b, travel length initially increased upon decreasing the channel width at a constant channel depth. However, for narrow channels (<15 μm), the opposite trend occurred, as discussed below. Travel length also increased upon increasing the channel depth at any constant value of width. For a continual supply of liquid to a closed capillary channel, liquid flow never terminates, although the speed of the advancing liquid front continuously decreases along the channel length.[117] By contrast, in open channels, the movement of the ink is also accompanied by solvent evaporation, which results in a localized increase in viscosity at the advancing liquid front (the part that exists in the channel for the longest duration). Eventually, this

liquid front completely solidifies and further ink flow is inhibited. Once formed, the solidification front advances inwards towards the reservoir.

The travel length of the reactive silver ink in an open channel can be roughly estimated as the product of the average flow velocity and the time at which solidification sets in at the advancing liquid front. The onset of solidification depends upon the vapor pressure of the ink and height of the liquid inside the channel, but not on channel width (exposed surface area to volume ratio of liquid in channels with different widths but same depth is constant). The average flow velocity, on the other hand, has a strong dependence on the width of the channel. Decreasing the channel width, while maintaining a constant depth, enhances capillary pressure (from (6.1)). However, flow resistance also increases upon decreasing the width, with the effect being especially pronounced in very narrow channels. Resistance to flow in a closed microchannel of width w is inversely proportional to w^4; [116, 118] hence, a similar dependence can also be expected for open microchannels. Therefore, average flow velocity increases and subsequently decreases upon decreasing the channel width for a fixed depth, dictated by the relative dominance of either capillary pressure or flow resistance, respectively (Fig. 6.4b).

Interestingly, the travel length increased upon increasing the channel depth, for a constant width. Although increasing the channel depth decreases capillary pressure (from (6.1)), it also reduces the effect of viscous dissipation from the channel floor, besides increasing the time for solidification at the advancing liquid front Therefore, both flow velocity and travel time of the ink increase in deeper channels. It is worthwhile noting that maximum travel length observed for our experiments is close to 6 mm, which should

be adequate for most printed circuits applications. Work is underway to increase this travel length by further reducing the initial ink viscosity and suppressing evaporation during the ink migration process.

Cross-sectional SEM provides insight into the dynamics of flow and drying of the Ag ink inside a microchannel. Figure 6.4c reveals that a thin Ag deposit is present on both the sidewalls and bottom of a 5 μm wide channel. The presence of Ag on the sidewalls indicates that during the entire capillary flow, the liquid filled the channel almost to the top.[119] It is also testimony to the pinning of the contact line to the top of the walls during drying. Similar to the coffee-ring effect on flat surfaces,[26] the pinned contact line initiates liquid flow from the center towards the wall during drying, leading to a region of slightly increased Ag thickness near the walls and a region of uniform thickness away from the walls (Fig. 6.4d). This is consistent with results obtained for polymer and latex solutions dried within similar confined geometries.[120, 121]

6.4 Electroless Deposition of Cu in Printed Microchannels

Capillary filling enables patterning of the reactive Ag ink in high-resolution channels. However, the channels are only partially filled with metal after drying and annealing of the ink. To obtain high-aspect ratio conductors, complete filling of the channels with metal is required. This is accomplished by electroless deposition of Cu. Upon immersing the substrate in the plating solution, Cu ions from the solution diffuse towards the Ag metal inside the microchannels, where they are reduced to Cu metal.[112]

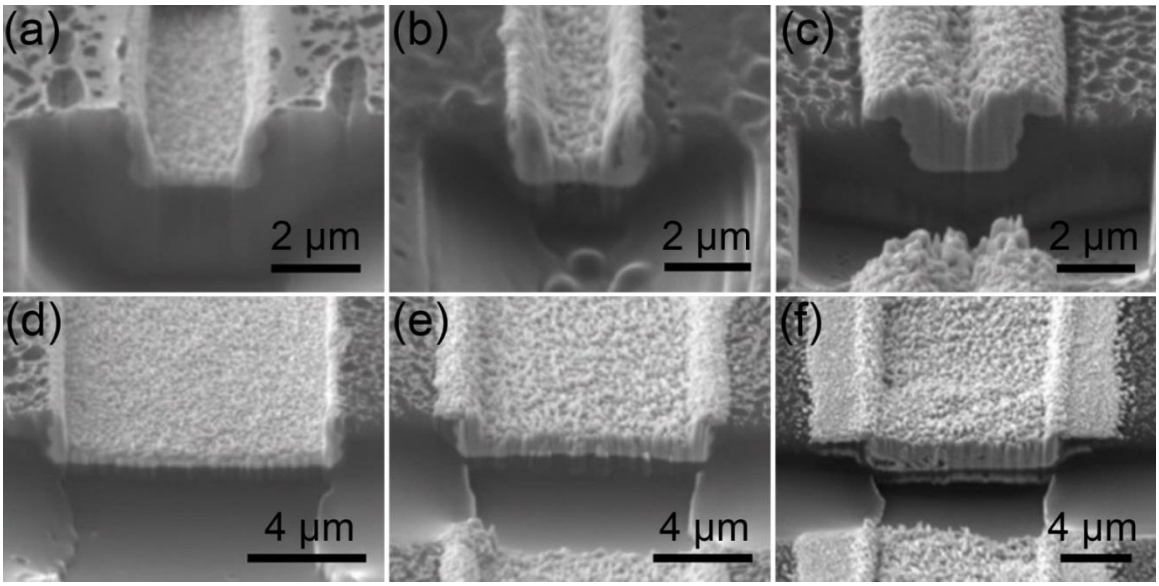

Figure 6.6 Electroless plating of Cu in printed microchannels. Focused ion beam cross-sections showing Cu growth in a 2.5 µm wide channel after (a) 3 min, (b) 6 min and (c) 9 min immersion time in the plating bath, and a 10 µm wide channel after (d) 3 min, (e) 6 min and (f) 9 min immersion time. The depth of the channel in both the cases is 2.5 µm.

Figure 6.6 displays focused ion beam (FIB) cross-sections, which illustrate time-dependent growth of Cu inside Ag-filled micro channels (widths: 2.5 and 10 µm, depth: 2.5 µm). The temperature of the bath was maintained at 55°C. After 3 min immersion time, Cu grew exclusively atop Ag present on both the sidewalls and the bottom of the channel (Fig. 6.6a, d). The thickness of Cu increased with plating time, with an average growth rate ~ 300 nm min^{-1}. Interestingly, side overgrowth near the top of the channel sidewalls was also seen after a plating time of 6 min, indicating isotropic growth of Cu around an individual Ag seed (Fig. 6.6e). Eventually, after 9 min, both the 2.5 and 10 µm channels were flush with Cu with an overgrowth of 0.8 and 3 µm, respectively on either side of the channel (Fig. 6.6c, f). Advancing Cu metal fronts from both the sidewalls and

the bottom seamlessly merged to completely fill the channels, yielding very high aspect ratios (height/width) of 0.6 and 0.1 for the 2.5 and 10 μm channels, respectively. It should be noted that the aspect ratios can be further improved by inhibiting the side-overgrowth through the addition of special additives to the electroless plating solution.[122] The surface morphology of the plated Cu was characterized using atomic force microscopy, which revealed that the root-mean-square roughness over a 25 μm^2 area was 81.8 ± 5.2 nm (Fig. 6.7).

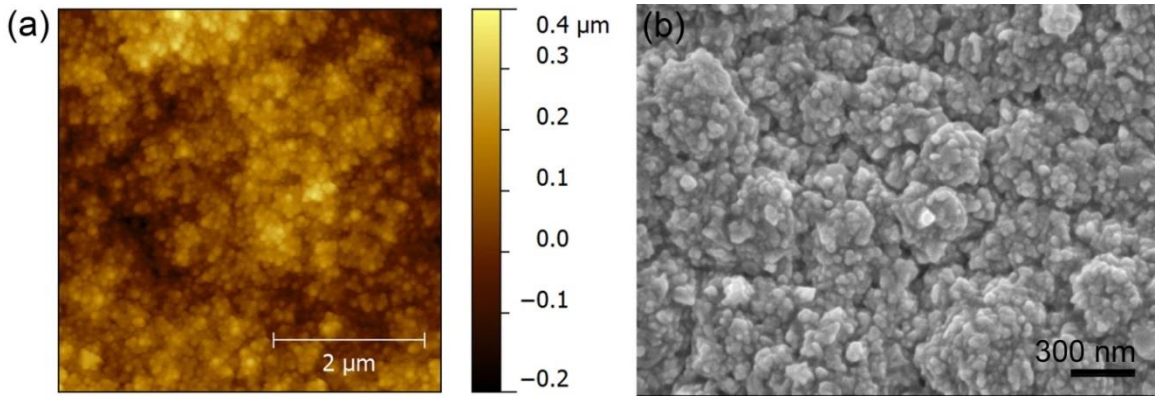

Figure 6.7 Surface characterization of electroless-plated Cu. a) Tapping-mode AFM height image of electroless-plated Cu film. The rms roughness of the film is 81.8 nm over a 25 μm^2 area. b) SEM displaying nanoscale Cu grains in the film.

6.5 Electrical Characterization and Bending Tests

To study the effect of the channel geometry on the electrical properties, we used the two-point probe method (Figure 6.8a) to measure the resistance of the Cu/Ag wires in channels with different widths (2.5 to 20 μm) at a constant depth (4 μm). Figure 6.8b illustrates the resistance of all wires, irrespective of the channel width, varied linearly with length in accordance with Ohm's law, suggesting dimensional invariance of the wires along their length. The contact resistance (between the tungsten probes and the

wires) was nearly independent of the wire width, which is also a signature of a true conductor. The calculated resistivity is similar for all wires, with an average value of 2.96 ± 0.1 μΩ-cm, which translates to a conductivity of 57 % of bulk Cu (Fig. 6.8c). This is impressive considering the maximum temperature employed during the entire process was 100°C during annealing the Ag ink. The resistance per unit length of the wire scales inversely with the channel width. For example, linear resistance almost doubles upon decreasing the channel width by a factor of 2. Despite the low line width, very low values of linear resistance (down to 1 Ω mm^{-1} for 10 μm wide channels) are achieved due to the low resistivity and high aspect ratio of the patterned wires. We also studied the effect of channel shape on resistance of the wires (Fig. 6.9). Interestingly, the resistance of wires in non-linear channels is slightly higher than those in linear channels of the same length, which may result from thinner Ag deposits around bends in the channel.

To investigate mechanical flexibility and durability of the Cu/Ag wires, we examined the change in electrical resistance of five wires (width: 15 μm, depth: 4 μm) subjected to repeated bending cycles at two different radii of curvature (r) (Fig. 6.8d). As shown in Figure 6.8e, for r of 1.2 cm (~ 0.4 % tensile strain), electrodes subjected to 1000 repeated bending cycles exhibited only a slight increase in their electrical resistance relative to the initial value. For r of 0.6 cm (0.8 % strain), the electrical resistance increased gradually, with a 1.5-fold increase after 1000 cycles. None of the patterned wires exhibited complete failure. The SEM image reveals formation of micro-cracks

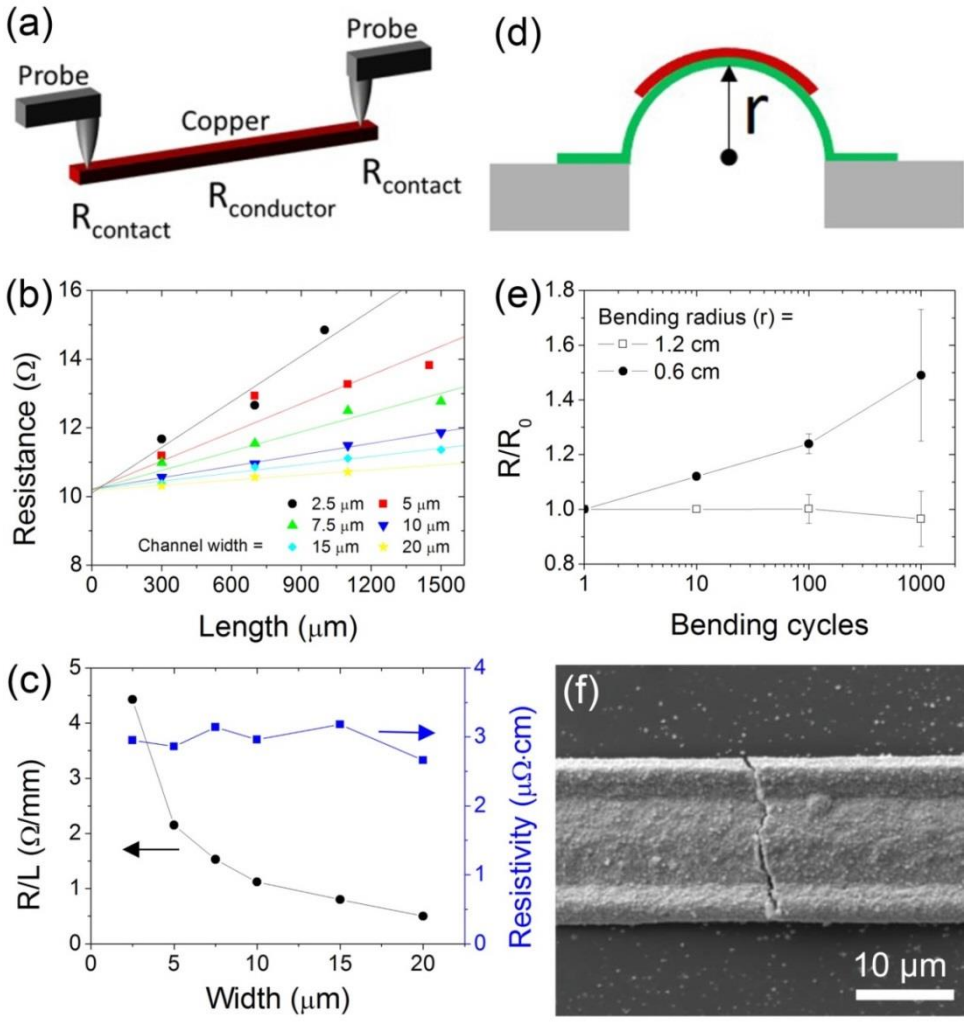

Figure 6.8 Electrical properties and bendability of Cu/Ag wires. (a) Schematic of the two-point probe method to measure electrical resistance of the wires. (b) Variation of wire resistance with length for different channel widths, but constant depth (4 μm). Both 2.5 μm and 20 μm have only three data points, because of termination of capillary flow of the Ag ink before 1.5 mm. (c) Variation of linear resistance and resistivity (derived from (b)) with channel width. The resistivity values do not show a major change over the entire range of widths. (d) Schematic depicting the experimental set up for the bending test. The substrate, attached to a stationary block and a sliding stage, is bent to a certain radius and restored to its initial state to complete one bending cycle. (e) Electrical resistance of the wires as a function of bending cycles under different bending radii (0.6 cm and 1.2 cm). (f) SEM showing a micro-crack along the width of a wire after 1000 bending cycles at r = 0.6 cm.

along the width of the wires, parallel to the axis of bending (Fig. 6.8f). Although the bending performance is acceptable for most flexible electronics applications, it may be further optimized by employing thinner wires or an encapsulating layer to shift the stress-neutralization plane during bending into the Cu layer.[123]

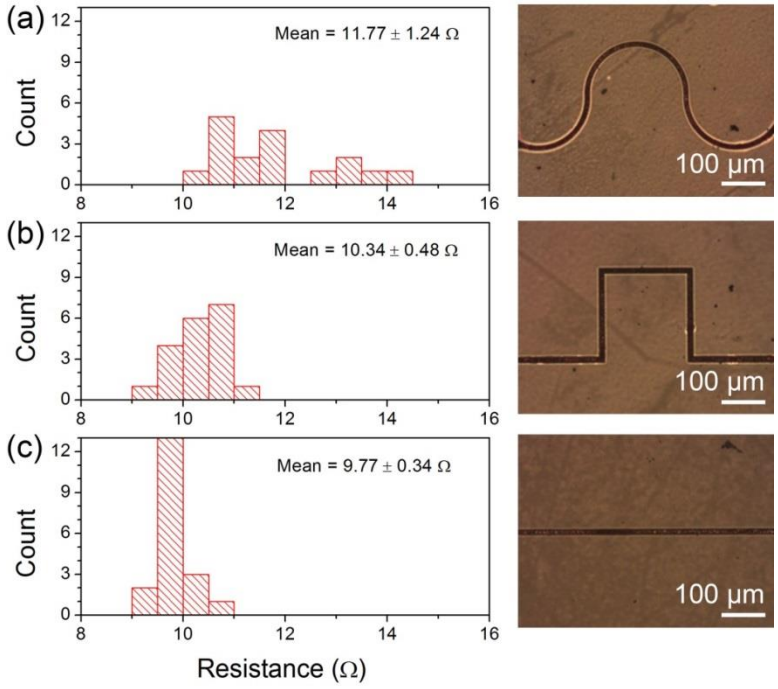

Figure 6.9 Effect of channel shape on electrical resistance. Histogram showing distribution of resistance of 18 wires fabricated in (a) curvilinear channels, (b) linear channels with four 90° bends and, (c) linear channels with no bends. The length of each wire was 1 mm.

We also investigated the adhesion of the Cu/Ag wires (widths: 2.5-100 μm, depth: 4 μm) using the scotch tape and ultrasonication tests. Although wider wires (> 30 μm) showed delamination in some locations, the narrower wires displayed exceptional adhesion to the molded epoxy substrate and remained anchored to the channels even after 3 consecutive tests.

Figure 6.10 highlights the versatility of this method to produce high-resolution conductors. Fig. 6.10a shows a top-view SEM of a 2 μm wide Cu/Ag line. Despite such high-resolution, line consistency and sharp edge definition over a length scale of tens of microns are clearly evident. Because capillary flow is impartial to the shape of the channel, complex patterns such as 'UMN' (line width: 12 μm) and crossbars (line width and spacing: 5 μm) can also be easily produced, without breaks or defects. For device applications, miniaturized line spacing is critical to performance along with line width. To determine the minimum line spacing obtainable using this approach, we fabricated an array of channels (line width and depth: 4 μm) with an initial spacing of 15, 7.5 and 5 μm. After the printing and plating steps (plating time: 15 min), the width of the individual Cu/Ag wires was 7 μm and the spacing reduced to 12, 4 and 2 μm, respectively (Fig. 6.10 d-f). No shorts were observed for lines with 4 μm spacing, but the 2 μm lines exhibited occasional shorting (Fig. 6.10f). To our knowledge, such high-resolution, high-aspect ratio metal patterning of conductive features embedded in plastic substrates using an additive, liquid-based process has not been reported previously. To test the suitability of our wires for organic devices, we employed 3 μm wide wires as source-drain contacts in organic thin film transistors (OTFT) (See Fig. 6.11). The devices displayed average values (n=16) of ON/OFF ratio higher than 10^5, field-effect mobility 0.2 $cm^2V^{-1}s^{-1}$ and threshold voltage -0.6 V. These values prove the viability of our electrodes for transistor applications.

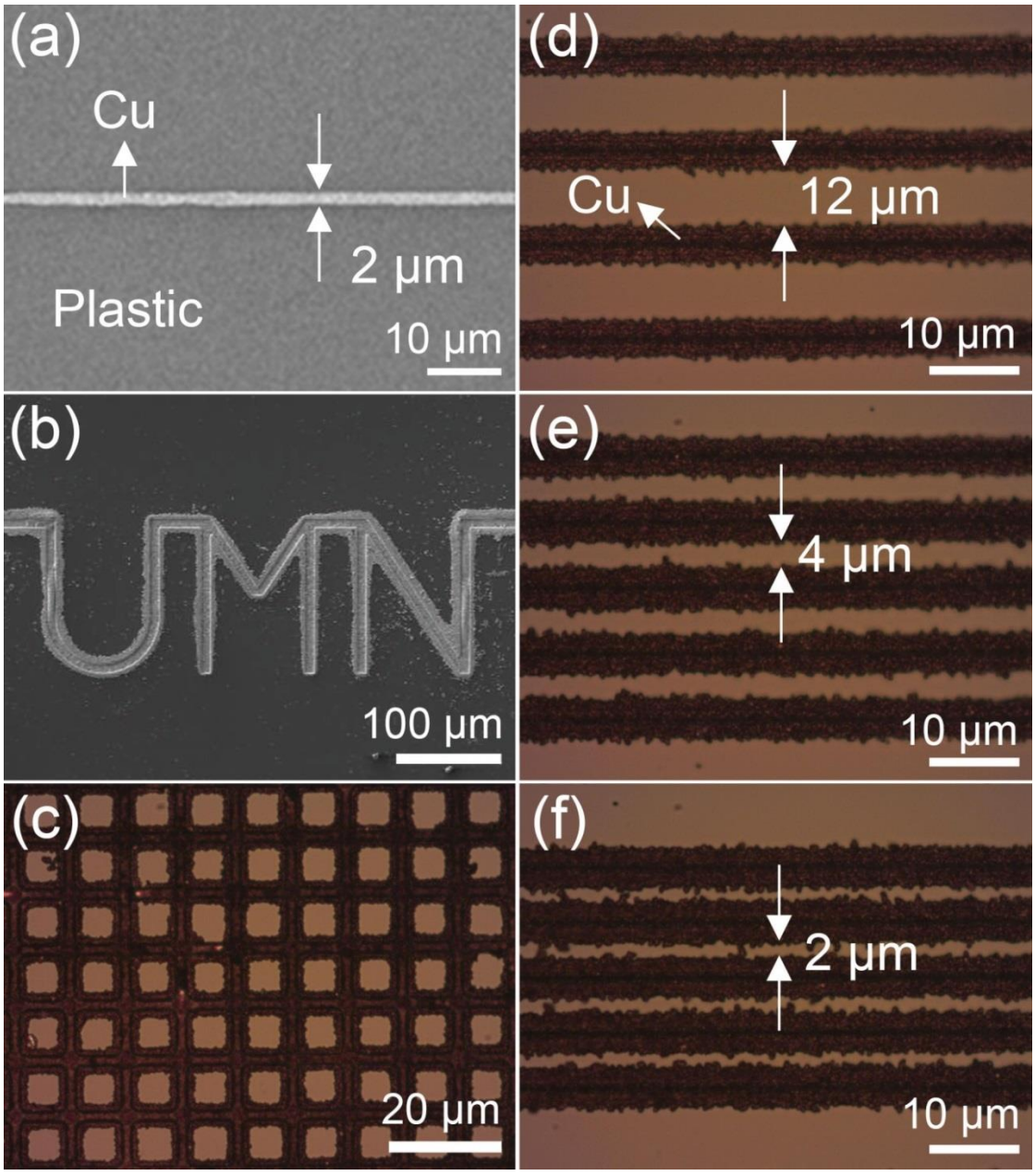

Figure 6.10 IPP patterning of high-resolution, complex features. SEM images of a patterned (a) 2 μm wide Cu/Ag wire and (b) UMN feature on a plastic substrate. The lighter region is metal. Optical micrographs showing (c) a crossbar pattern (line width and spacing: 5 μm), and an array of 4 μm wide lines with a spacing of (d) 12 μm, (e) 4 μm, and (f) 2 μm. Darker regions are metal. Occasional shorting in 2 μm wires is evident.

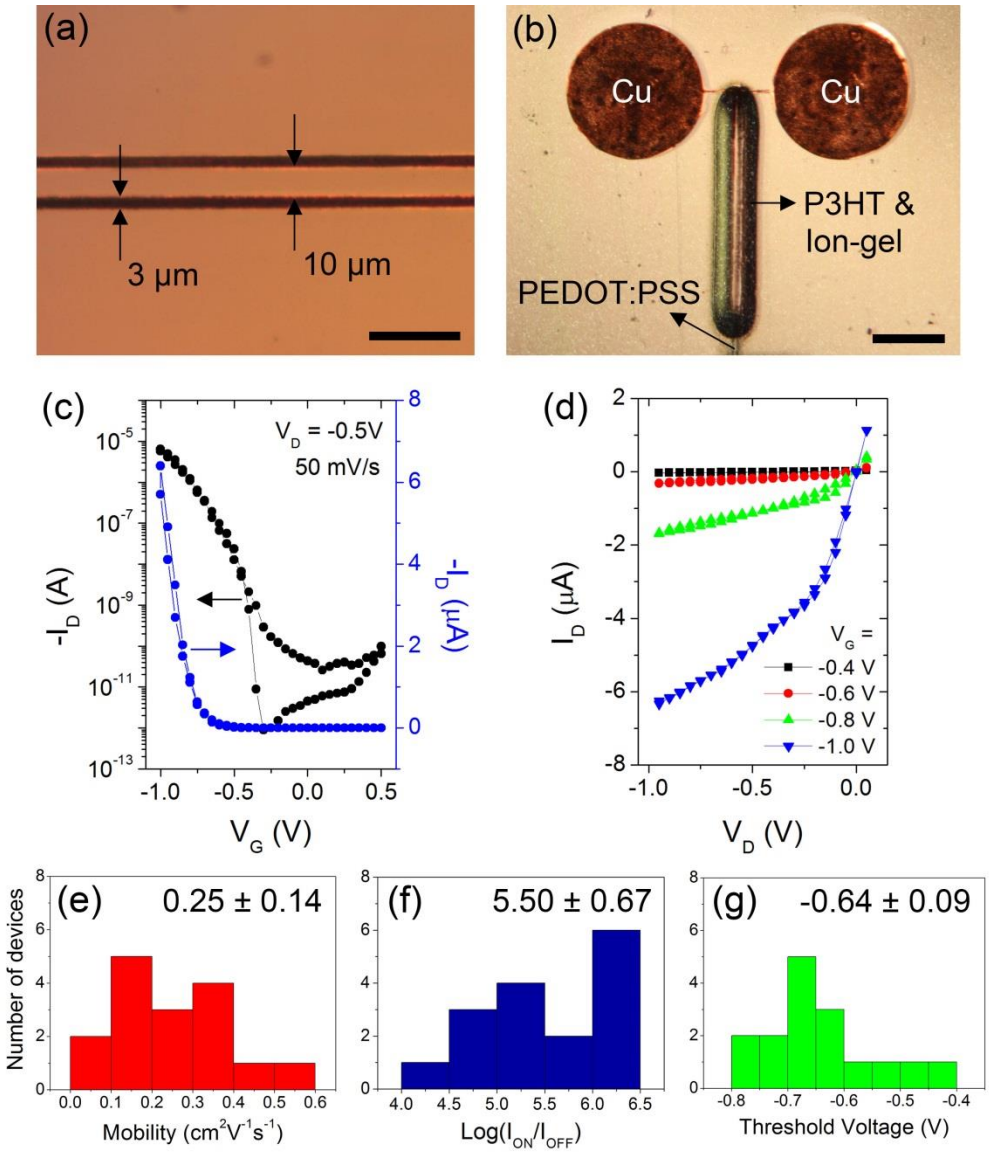

Figure 6.11 Organic thin film transistors (OTFT) using Cu/Ag wires as source-drain electrodes. Optical micrographs showing the (a) source-drain channel of the OTFT built using 3 µm wide wires with a spacing of 10 µm and b) printed device on a PET substrate. The semiconductor, dielectric, and the gate electrode were printed using aerosol jet printing. Cu-filled reservoirs act as contact pads in the device.(c) Transfer and (d) output characteristics of a TFT with the Cu/Ag electrodes at V_D -0.5 V. Histograms showing distribution of (e) field-effect mobility, (f) log (I_{ON}/I_{OFF}), and (g) threshold voltage of16 devices. Scale bar in (a) and (b) are 300 and 100 µm respectively.

6.6 Conclusions

We have demonstrated a new approach, referred to as IPP, for patterning highly conductive wires through capillarity-induced flow of inkjet-printed reactive Ag ink into micro-imprinted channels on a plastic substrate followed by a Cu electroless plating step. Specifically, high-resolution metal wires with minimum line width and spacing down to 2 and 4 μm, respectively, have been achieved using this approach. High aspect ratio features, up to 0.6, are obtained after the Cu deposition. The Cu/Ag wires display excellent conductivity (> 50% of bulk metal), which is invariant over different channel dimensions, making them suitable candidates for flexible electronic devices and circuits. Due to their high aspect ratio and electrical conductivity, wires as fine as 2.5 μm exhibit a very low linear resistance (< 5 Ω mm^{-1}). The embedded wires exhibit good flexibility and resilience, with minimal degradation in electrical performance after thousands of bending cycles. Since our patterning approach is compatible with roll-to-roll processing, it can be readily implemented in a continuous, additive manufacturing process.

Chapter 7 Self-Aligned Manufacturing Process for Printed Electronics

7.1 Background and Motivation

Printing electronically active inks on flexible substrates is attractive because it can be integrated with roll-to-roll (R2R) manufacturing resulting in high-throughput device fabrication. However, it is a challenge to create multilayered devices with the required control over ink placement and feature size. The precise alignment capabilities of photolithography-based semiconductor fabrication do not readily translate to R2R manufacturing, making alignment of multiple layers of disparate materials with micron-level tolerances quite difficult to achieve on fast moving webs.

To overcome these challenges, self-aligning strategies are needed that enable materials registration to be achieved automatically during R2R processes. One such strategy is Self-Aligned Imprint Lithography (SAIL),[73-75] where all the all key materials are coated onto a web substrate and then a top coat resist is applied. The resist is imprinted with a stamp encoded with geometrical information such that subsequent

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etching steps selectively reveal specific underlayers (metal, semiconductor, and dielectric) across the substrate. A major drawback of SAIL, however, is that it is a subtractive process, i.e., valuable materials are etched away. Self-aligned inkjet-printed patterns have also been obtained either by confinement of ink droplets in a "bank"[80] or by de-wetting on chemically patterned surfaces[76-79]. However, these processes are only partially self-aligned because they require micron-level registration of the inkjet nozzle to previously patterned features. Moreover, only a few selective layers of the device stack can be patterned using these techniques, not the entire device.

Here, we report a new approach for printing multilayered electronic devices that is simultaneously self-aligned, additive, and scalable, which relies on capillary flow of electronically active inks within microchannels carefully engineered on the substrate surface. We term this process: Self-aligned Capillarity-Assisted Lithography for Electronics (SCALE). In SCALE, multi-tier channels, each of which is connected to a separate reservoir, are molded into a coated thermoset material by imprint lithography. The dimensions of the channels range from a few microns to tens of microns and they are connected to larger reservoirs. Electronic inks are delivered to these reservoirs by "drop-on-demand" inkjet printing, from which the liquid inks are wicked into the microchannels by capillarity. The process is self-aligned, because multiple inks can be delivered sequentially to cavities engineered into a multi-level microchannel network, to form, upon drying, multilayered electronic devices. Importantly, control over the printing process is only required at the size scale of the reservoir (~ 100s of microns), rather than the size scale of the device. Specifically, we demonstrate that all the major multilayered

electronic components of an integrated circuit, i.e., resistors, capacitors, transistors, and cross-overs can be fabricated using the SCALE process.

7.2 Self-Aligned Resistors

Figure 7.1 illustrates SCALE fabrication of a single resistor. In the first step, a two-level topographical pattern is created on the surface of a plastic substrate by pressing a polydimethylsiloxane (PDMS) stamp into a liquid epoxy prepolymer coated on a polyethylene terephthalate (PET) film, with subsequent UV curing to solidify the liquid layer (see Methods). The imprinted features, both recessed and raised, with respect to the substrate surface are shown in the scanning electron microscope (SEM) image in Figure 7.1a. A schematic of the plan view of the imprinted cavity and the cross-section along the dotted line are shown in Figure 7.1b. A reactive Ag ink[109] is delivered (volume ~2 nL) to the two lower-level reservoirs by an ink jet nozzle (Figure 7.1c). Capillarity spontaneously draws this low viscosity ink (10-12 cP) into the feeder channels (width, w = 10 μm) and fills the cavities.[113, 114, 124] The Ag ink is then dried and sintered at 100°C for 5 min, leaving behind a thin trace of Ag metal on the sidewalls and bottom of the channel and the reservoir. The Ag-coated channels and reservoirs serve as electrodes and electrode pad, respectively. Next, a carbon black ink is loaded into the upper-level reservoir (Figure 7.1d). This reservoir is connected to a main channel (w = 50 μm) which, in turn, branches into two channels. Again, capillarity drives the ink down the main channel before the flow splits along the two branches, proceeding on top of the two Ag-filled channels. Upon evaporation of the ink solvent, a thin deposit of carbon black is left behind which bridges the two Ag electrodes, completing the resistor fabrication.

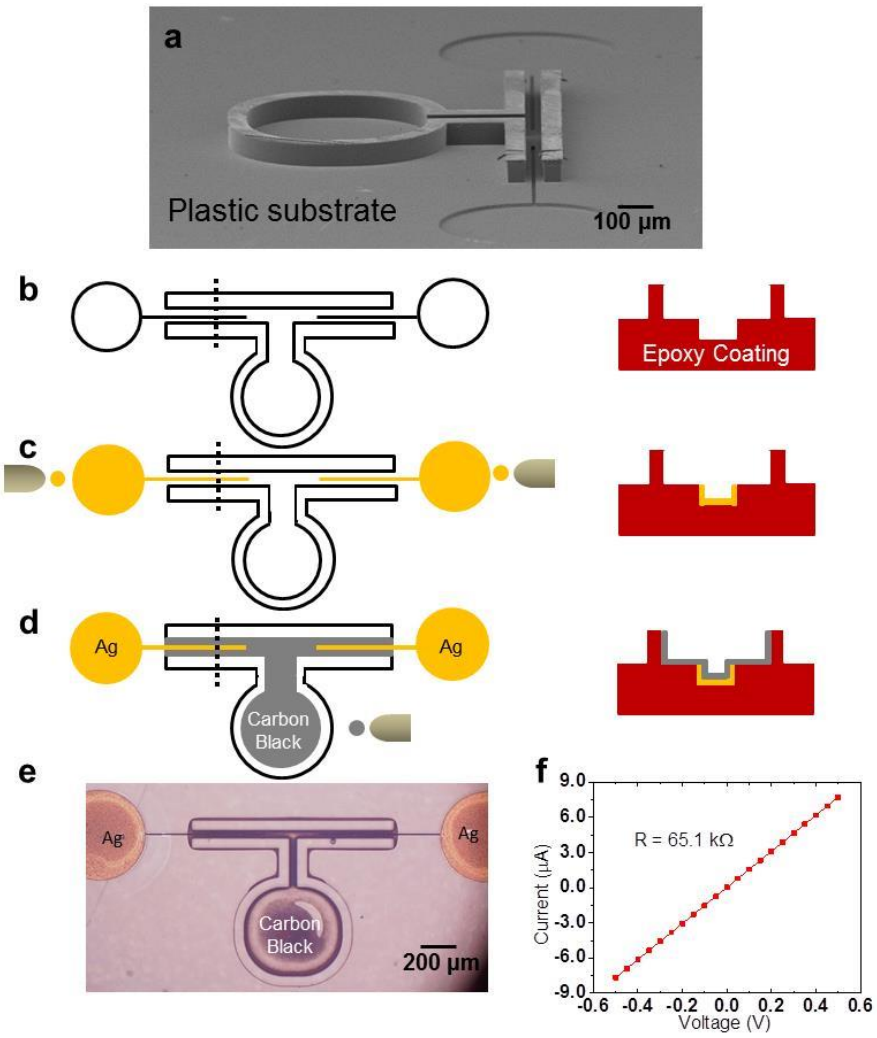


Figure 7.1 Fabrication of resistors using the SCALE process and electrical characterization. (a) SEM image displaying an imprinted device cavity on the surface of an epoxy/PET substrate for processing a resistor. (b) Schematic of plan view of the device (left) and cross section along the dotted line (right). (c) Metal electrodes are processed by inkjet printing an Ag ink into the yellow reservoirs. The ink is wicked into the channels by capillarity; a thin Ag film is left behind on the the channel walls upon annealing (right). (d) A carbon black ink is dispensed into the gray reservoir which wicks into the attached channel connecting the two metal electrodes in the process. e, Optical micrograph of a completed device. (f) Current-voltage characteristics of the printed device.

An optical microscope image of the completed device is shown in Figure 7.1e. Figure 7.1f displays the current-voltage characteristics of a typical device, and the nice

linear response suggests Ohmic contact between the printed carbon black and Ag films. We fabricated 25 resistors in a single batch and the average value of resistance is measured to be 64.0 ± 2.7 kΩ (see Figure 7.2). The yield is 100 % and the spread in the resistance values small, indicating excellent reproducibility of the printed layers in all the devices.

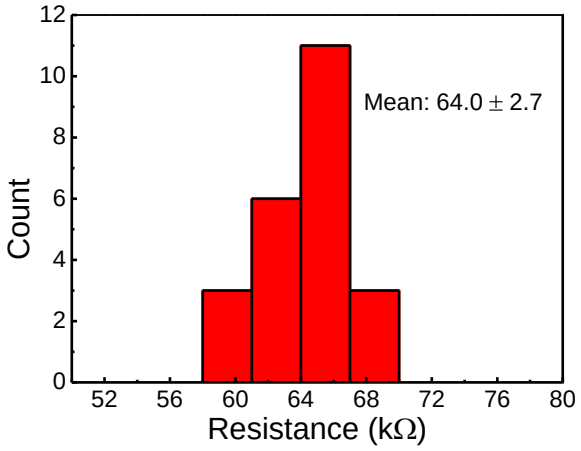


Figure 7.2 Histograms of resistance of 25 resistors fabricated using SCALE. The device yield was 100 %.

7.3 Self-Aligned Capacitors

To fabricate capacitors using the SCALE process, we adopted an interdigitated architecture, where Ag metal and an "ion gel"[34] polymer electrolyte serve as electrodes and dielectric material, respectively. Ion gels are formed by the gelation of a triblock copolymer (polystyrene-b-poly(methylmethacrylate)-b-poly(styrene) (PS-PMMA-PS) in an ionic liquid (1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide) [EMIM][TFSA]. Ion gel films exhibit very high capacitance values, courtesy of the mobile ions in the polymer matrix, which, upon application of a voltage across the two

electrodes, form nanometer-thick electrical double layer (EDL) capacitors at the electrode-electrolyte interfaces[31]. For preparing an inkjet-printable ion gel ink, (PS-PMMA-PS) and [EMIM][TFSA] (20:80 wt. ratio) are co-dissolved in n-butyl acetate, a high boiling solvent to overcome the problem of nozzle clogging during printing).

Similar to the two-tier structure for resistors, cavities at two different elevations are imprinted into the plastic substrate for fabricating capacitors (**Figure 7.3**a). The lower- and upper-level cavities consist of reservoirs and channels for patterning the Ag electrodes and the ion gel dielectric, respectively. The width and separation of the Ag channels is 10 μm each. In the first of the two printing steps, Ag ink is loaded into the two lower-level reservoirs, which then spontaneously fills the multi-branched channels by capillarity (Figure 7.3b). Upon drying and annealing of the ink, well-defined Ag interdigitated electrodes are obtained with line width comparable to the initial channel width (Figure 7.4a). In the second printing step, ion gel ink is delivered to the upper-level reservoir, and again, the ink travels down the channel via capillarity, swamping the underlying interdigitated Ag electrodes (Figure 7.3c). Upon solvent evaporation, which occurs spontaneously without requiring an additional annealing step, an ion gel film is produced between the interdigitated electrodes. An optical micrograph of a portion of the completed device is shown in Figure 7.3d. Figure 7.3e shows specific capacitance of the device as a function of frequency from 10 Hz to 1 MHz. A remarkably large capacitance value of about 25 μF cm^{-2} is obtained at 10 Hz, owing to EDL formation at the Ag-gel interfaces.

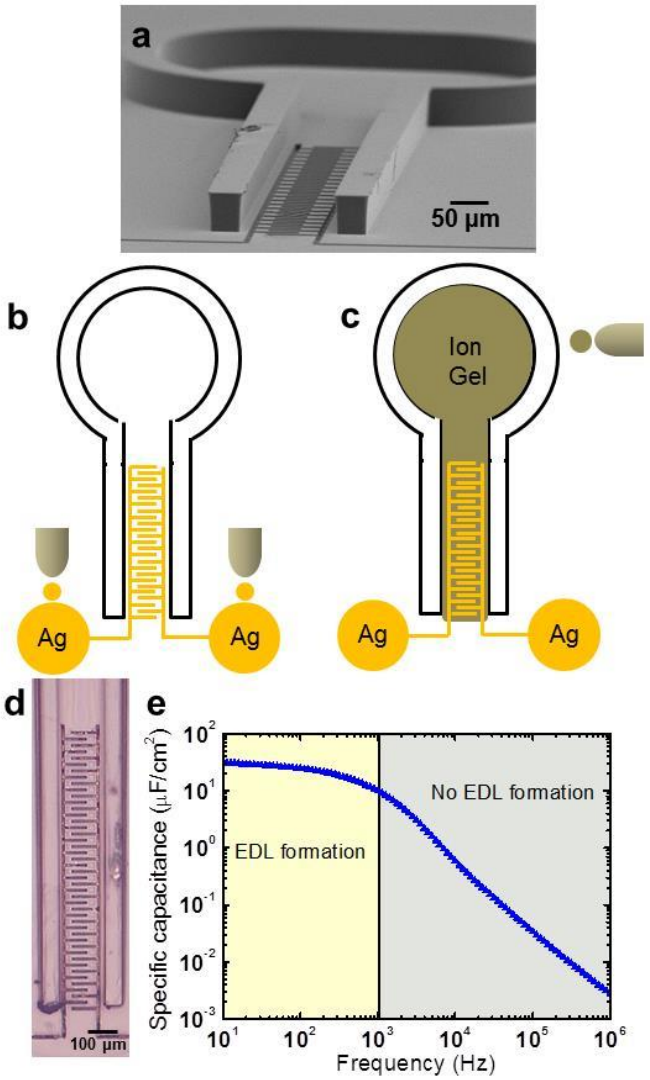


Figure 7.3 Fabrication of capacitors using the SCALE process and electrical characterization. (a) SEM image displaying an imprinted device cavity on the surface of the epoxy/PET substrate for processing a capacitor. Scheme showing fabrication of capacitors by sequential delivery of (b) Ag ink to the yellow reservoirs, and (c) ion gel ink to the gray reservoir. Both the inks are wicked into their respective channels to form, upon drying and annealing, a self-aligned interdigitated capacitor. (d) Optical micrograph of a completed device. e, Frequency dependence of the specific capacitance of the printed capacitors. The capacitance-frequency curve can be divided into two regimes: EDL formation at the Ag-gel interface, and no EDL formation.

The capacitance value decreases gradually with increasing frequency but remains above 10 μF cm^{-2} even at 1 kHz. At frequencies greater than 1 kHz, the decrease is more dramatic because EDL formation is suppressed. Frequency response of our capacitors strongly depends on the polarization response time of the gel, which may be further improved by decreasing the spacing between the Ag digits. We note that the absolute value of capacitance of the devices can be modulated solely by varying the Ag digit count, with a 1.5 nF capacitance change for every Ag digit (See Figure 7.4b).

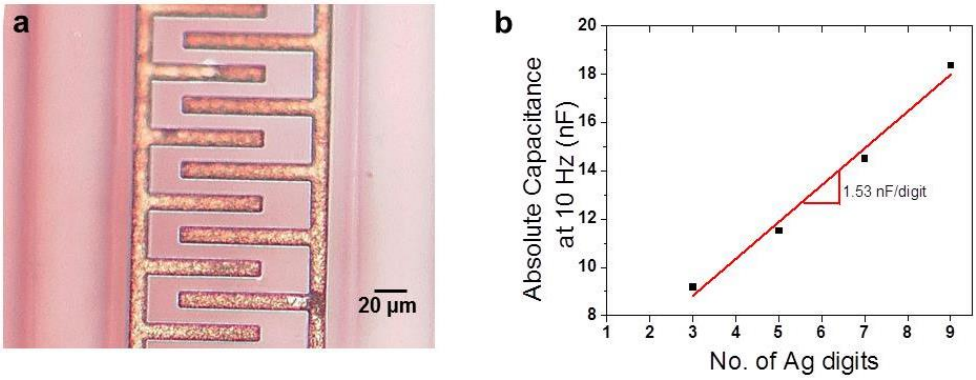


Figure 7.4 (a) Optical image of capacitor electrode digits after capillary-filling, drying and annealing of reactive Ag ink. The Ag ink flow is confined to the width of the channel and the final electrode width matches with the width of the empty channel. (b) Variation of absolute capacitance of printed capacitors with Ag digit count.

7.4 Self-Aligned Transistors

To create transistors, which are the most important and complex building blocks of an electronic circuit, by the SCALE process, we adopted electrolyte-gated transistor (EGT) technology[31], i.e., an electrolyte (ion gel in our case) is employed as the gate dielectric material in the thin film transistor (TFT) stack. EGTs have several key benefits,

including low-voltage operation despite relatively high dielectric thickness (~µm), and the option to physically offset the gate electrode from the source-drain channel.

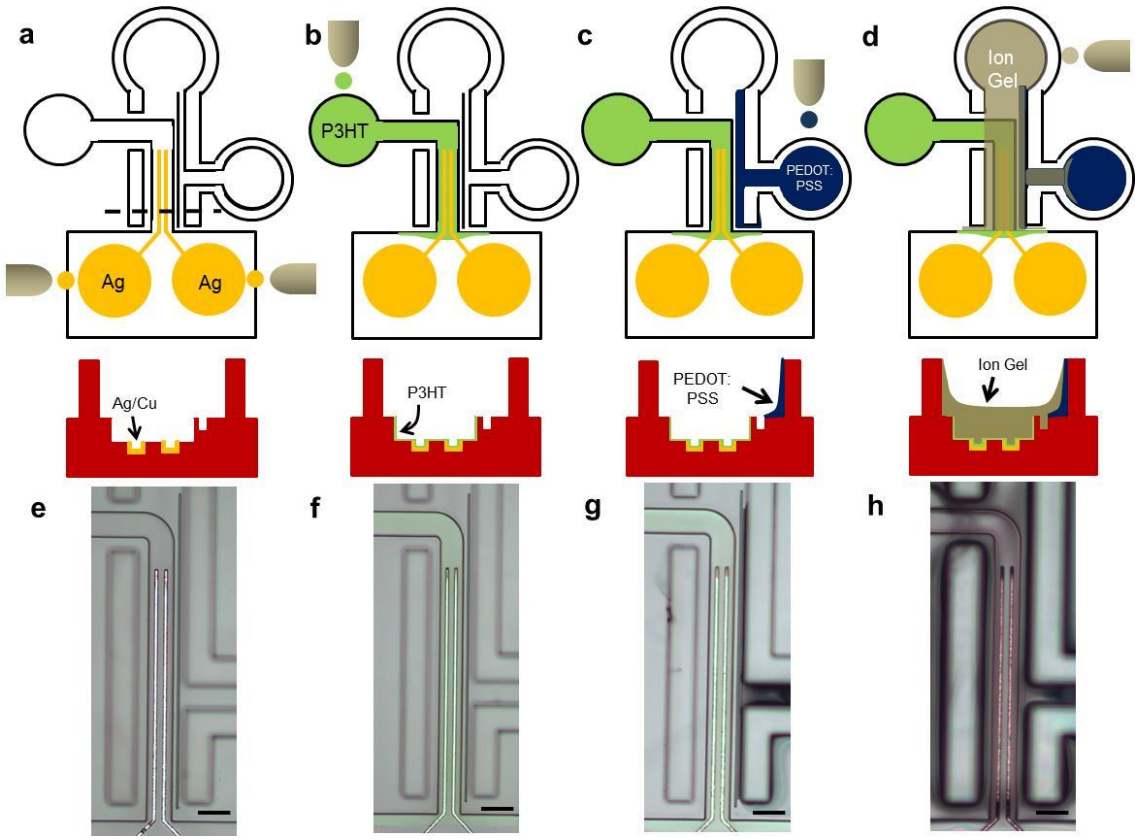


Figure 7.5 Fabrication of transistors using the SCALE process. Schematic of plan view of the device cavity (top) and cross-section along the dotted line (below) after (a) filling the source-drain cavities with Ag ink, followed by Cu electroless plating (not shown), (b) filling the transistor channel with semiconductor ink (P3HT) , (c) patterning the gate electrode (PEDOT:PSS) and (d) filling the device cavity with the dielectric ink (ion gel). Optical micrographs of the imprinted device cavity on the plastic substrate surface after sequential patterning of Cu/Ag source-drain, (f) P3HT semiconductor, (g) PEDOT:PSS gate, and h, ion gel dielectric. Scale bar in e-h is 50 µm.

Given the multiplicity of functional layers in a transistor, a four-tier imprint is created in the plastic substrate. A schematic of the plan view of the device and the cross-

section along the dotted line is shown in **Figure 7.5**a. The SEM image in **Figure 7.6**c displays the complex, high-resolution imprinted device cavity. Firstly, the source and drain electrodes are processed. Ag ink is delivered to the two lowest-lying reservoirs (colored yellow in Figure 7.5a). As before, Ag-coated channels (w = 5 μm) are obtained after capillary-filling, drying and sintering of the Ag ink. The printed Ag metal is then coated by a thin film of Cu by immersion in a Cu electroless plating solution for 3 min, followed by a rinse with deionized (DI) water. The Ag inside the microchannels acts as a seed layer for selective deposition of Cu. The Cu deposition is critical to device performance, as discussed later. As is evident in the optical micrograph in Figure 7.5e and the SEM image in Figure 7.5d, the processed source and the drain electrodes have sharp edge definitions. Focused ion beam milling along the dotted line in Figure 7.6d reveals a thin coat of Cu/Ag metal on the sidewalls and bottom of the channel (Figure 7.6e).

In the second printing step, a semiconductor ink is delivered to the green reservoir (Figure 7.5b). We selected a p-type semiconducting polymer, poly(3-hexylthiophene) (P3HT). The P3HT ink wicks into the channel (w = 40 μm); capillary pressure drives the ink on top of the source and the drain electrodes before the flow bifurcates along the perimeter of the large rectangular cavity (Figure 7.5b and f). Note that bifurcation of capillary flow along the outlet reservoir walls, as opposed to flooding of the open space, is consistent with observations in microfluidic devices[125] and holds true for other inks as well, e.g., Ag ink (Fig. 7.7).

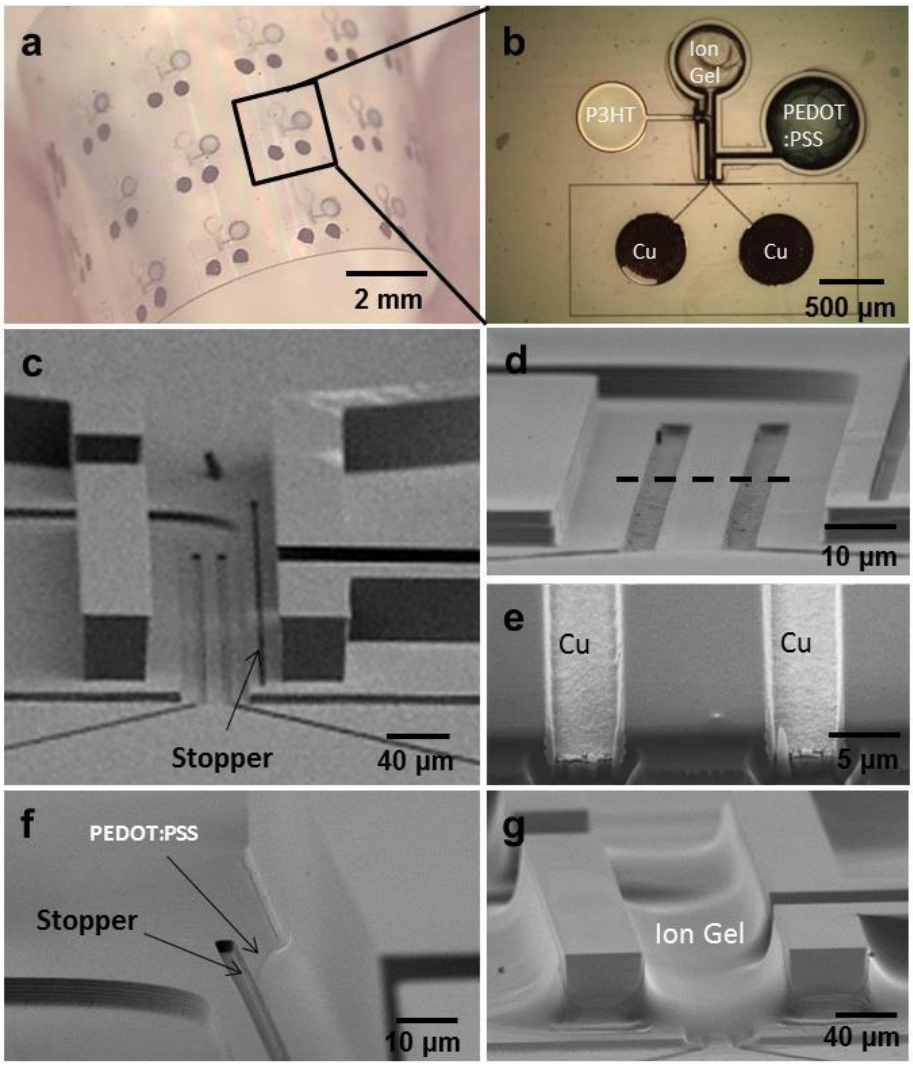


Figure 7.6 Optical and electron microscopy of printed transistors. Optical micrograph of (a) an array of printed transistors and (b) a single device on an epoxy/PET substrate fabricated using the SCALE process. (c) SEM image of the imprinted device cavity displaying all the channels employed in the fabrication process. (d) SEM image of source-drain cavities filled with Ag/Cu metal after the printing and plating step. (e) Focused ion beam cross-section along the dotted line in d illustrating a thin coat of metal on the sidewalls and bottom the channels. (f) SEM image showing the printed PEDOT:PSS film pinned to the right edge of the stopper channel, and (g) printed ion gel film in the device cavity.

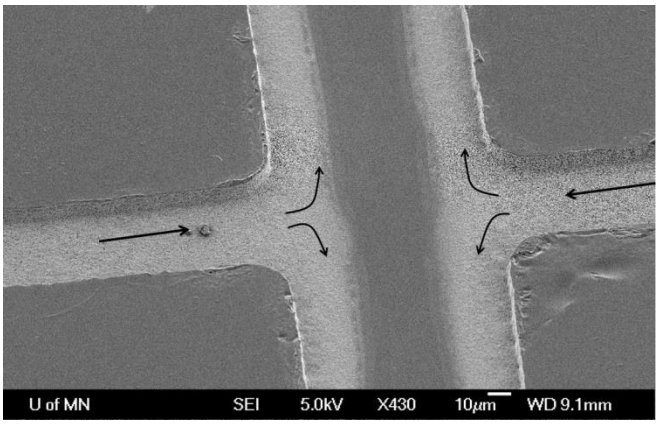


Figure 7.7 SEM image of printed Ag metal films showing bifurcation of reactive Ag ink along the sidewalls as it flows into a larger channel from the side channels.

Evaporation of the ink solvent leaves behind a thin semiconducting polymer film between the source-drain electrodes. The film at the channel floor is remarkably smooth, as revealed by atomic force microscopy, with a mean root mean squared roughness over a 25 μm^2 area of only 2.1 ± 0.2 nm (Fig. 7.8).

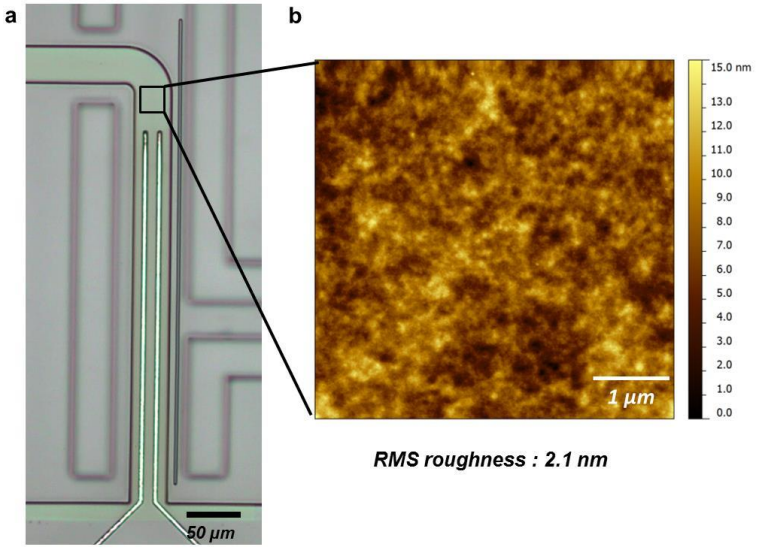


Figure 7.8 (a) Optical image of printed P3HT film in the device channel, and (b) atomic force microscopic image of printed P3HT film on the bottom of channel.

We employ a unique strategy for processing the gate electrode based on a commercially available inkjet-printable poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) ink (0.8 wt. % in H_2O). The PEDOT:PSS ink is dropped into the blue reservoir; the ink wicks into the channel and the liquid flow bifurcates at the channel outlet (Figure 7.5c). A narrow "stopper" channel (w = 3 μm), not connected to any reservoir, is strategically positioned between the P3HT channel and the PEDOT:PSS channel outlet (Figure 7.6c and f). During bifurcation of the PEDOT:PSS ink flow, the two leading edges of the capillary flow turn in opposite directions. The advancing contact line of the trailing bulk liquid is pinned to the top edge of the stopper and the ink does not trip over into the channel (Figure 7.5g and 7.6f). It has been shown that sharp micro-steps on a substrate can pin an advancing contact line[126, 127]. The pinning effect is highly reproducible and is also observed for the Ag ink (Fig. 7.10). The stopper, therefore, not only facilitates precise patterning of the gate, but also eliminates the possibility of shorting between the foot of the gate electrode and the P3HT film clung to the sidewall of its respective channel.

The final printing step involves loading the ion gel ink into the gray reservoir (Figure 7.5d). This reservoir is connected to a channel that encompasses all the other channels. The ion gel ink flows on top of all the underlying patterned channels; drying ensues and an ion gel film is left behind (Figure 7.5h). Note that the large height of the channel walls (~ 46 μm) imparts sufficient momentum to the capillary flow such that it is uninterrupted by the discontinuity in one of the channel walls. Multiple shots of the ink are delivered for a sufficient build-up of gel thickness in the channel (Figure 7.6g). The

completed device is annealed at 120°C on a hot plate in a N_2-filled glovebox. An optical micrograph of the completed EGT is shown in Figure 7.6b.

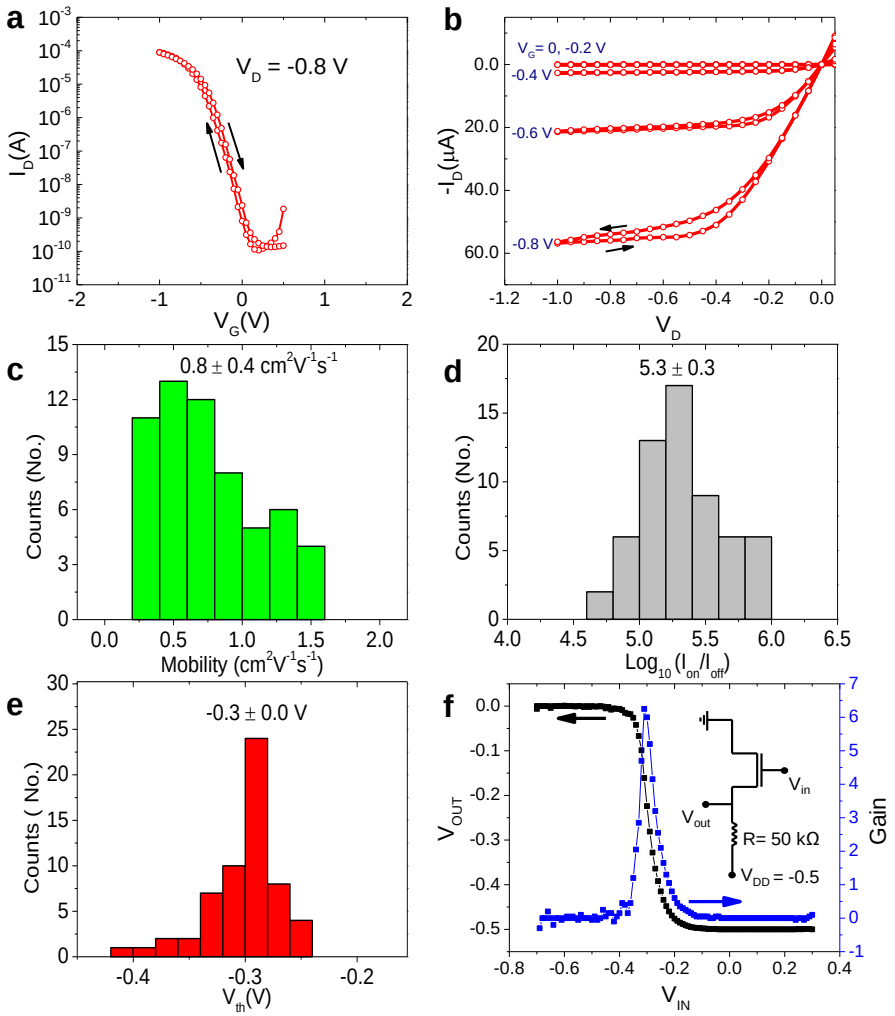


Figure 7.9 Electrical characterization of printed transistors and inverters. (a) Transfer and b, output characteristics of printed P3HT EGTs (W/L = 400 μm/ 10 μm). Gate voltage sweep rate was 50 mV s^{-1}. (c) Histograms of field effect mobility, I_{ON}/I_{OFF}, and threshold voltage of 59 printed devices, respectively. f, Quasi-static behavior of a resistor loaded inverter with P3HT EGTs. The voltage gain (dV_{out}/dV_{in}) of the device was ≈ 6.2.

Figure 7.9 a and b show the transfer and output characteristics of an individual SCALE TFT, respectively. The transfer curve in Figure 5a was acquired with the gate

voltage (V_G) swept from 0.5 to -0.9 V and back at 50 mV s^{-1} for drain voltage V_D = -0.8 V. The device turns on sharply near 0 V, with ON/OFF current ratio of ~ 10^6, and negligible current hysteresis between the forward and the reverse scans. The output curve shows the expected modulation of the drain current (I_D) with gate voltage in both the linear and saturation regimes, and the linear I_D-V_D relationship at low bias suggests nice Ohmic contacts despite the unusual electrode geometry.

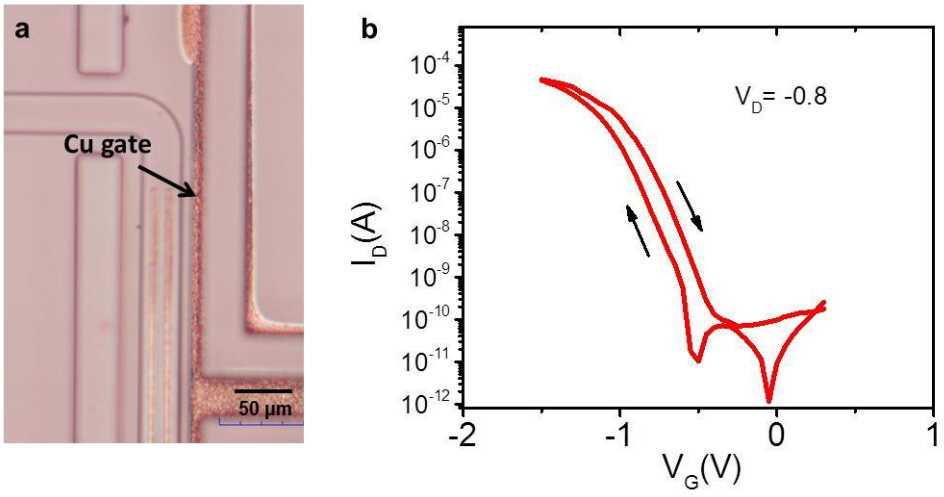


Figure 7.10 (a) Optical image showing Cu source, drain and gate electrodes processed by inkjet printing reactive Ag nk into the channel cavities, followed by an overcoat of Cu by electroless plating. Note that precise patterning of the gate electrode in the vicinity of the source-drain channel is facilitated by the pinning of the Ag ink to the stopper edge. (b) Transfer curve of a typical P3HT EGT with Cu gate obtained by sweeping the gate voltage at 50 mV/s.

A Cu overcoat on the Ag smooths the sharp channel edges, possibly facilitating a more conformal contact of the thin P3HT film with the electrodes around the edges. We also employed Cu as a gate electrode for the EGTs by patterning the source, drain and gate electrodes at the same time in the process flow. The devices showed similar

performance metrics compared to the PEDOT:PSS gated devices, although a slightly larger hysteresis was observed (Figure 7.10b).

To quantify statistical variations in device performance, we printed 75 devices in five batches. A yield of ~ 80 % (59 out of 75 devices were functional) is observed. Device failure largely arose from errors in ink delivery to the reservoirs and/or impediment to capillary flow by dust particles on the substrate surface. As a first demonstration, these yields are acceptable-especially given that these devices are printed in air on a simple, laboratory benchtop using a single inkjet nozzle with manual x-y motion control. Figure 7.9c-e display histograms of the statistical spread in key figures of merit for the 59 devices. The average saturation carrier mobility (μ) and the threshold voltage (V_{th}) are calculated to be 0.8 ± 0.4 $cm^2V^{-1}s^{-1}$ and -0.3 ± 0.0 V, respectively, from the plots of square root drain current ($I_D^{0.5}$) versus V_G, according to the standard saturation regime equation

$$I_D = \left(\frac{W}{2L}\right) \mu C_i \left(V_G - V_{th}\right)^2 \qquad (7.1)$$

The channel width (W) and channel length (L) are 400 and 10 µm, respectively. The capacitance of the gel (C_i) is measured to be 5.2 µF cm^{-2} by capacitance-voltage characteristics The average $\log_{10}(I_{ON}/I_{OFF})$ is an impressive 5.3±0.3.

To demonstrate initial device integration with SCALE, we also fabricated simple resistor-loaded inverters by connecting P3HT EGTs in series with 50 kΩ resistors, both processed using methods described above. The circuit diagram and the input-output characteristics are presented in Figure 7.9f. The device shows good inverter action; the

output voltage switches between -0.5 V (the applied drain voltage, V_{DD}) and 0 V as the input gate voltage is swept, and the voltage gain (dV_{out}/dV_{in}) is found to be ≈ 6.2.

7.5 Self-Aligned Crossovers

For building complete electronic systems, strategies for fabricating interconnect crossovers are also essential. A crossover is essentially a metal-insulator-metal stack. We fabricated crossovers using the SCALE process by employing a three-tier imprint, a schematic of which is shown in **Figure 7.11**. Firstly, Ag electrodes are fabricated by delivering Ag ink to the yellow reservoirs (Figure 6a). Next, a UV curable dielectric ink (NOA-73, Norland Products Inc.) dissolved in acetone (50:50 vol. %) is printed into the two gray reservoirs (Figure 7.11b). Acetone is added to NOA 73 (a liquid prepolymer) as a viscosity modifier for inkjet printing. The ink flows on top of the printed Ag channel, and then along the perimeter of the open cavity. The prepolymer is cured by irradiating the substrate with UV light, and the thick, cured film insulates the Ag electrode underneath. Fabrication is completed by simply delivering Ag ink to the middle, top-tier reservoir (Figure 7.11c), thereby bridging the two Ag electrodes processed in the first step. An optical micrograph of the completed device is shown in Figure 7.11d. I-V measurements across R_{11} and R_{22} yield nice linear curves (Figure 7.11e) but no current is observed across R_{12} (Figure 7.11e, and Figure 7.12), suggesting excellent insulation between the two perpendicular metal electrodes.

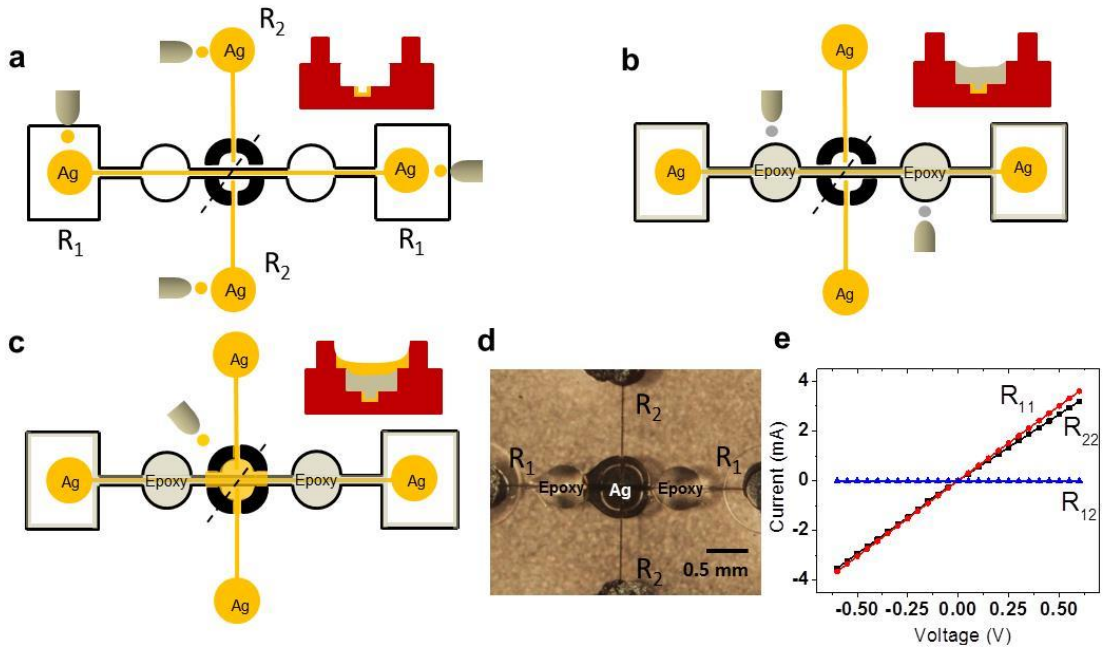


Figure 7.11 Fabrication of crossovers using the SCALE process and electrical characterization. Schematic of plan view of the device and cross-section along the dotted lines after printing (a) Ag ink in the yellow reservoirs, (b) NOA epoxy ink in the gray reservoirs, and (c) Ag ink again in the middle reservoir to connect the two Ag electrodes processed in step a. (d) Optical image of a completed device. (e) Current-voltage characteristics of the printed device. Measurements across R_{11} and R_{22} yield linear I-V curves, but no current is observed across reservoirs R_1 and R_2 suggesting excellent insulation.

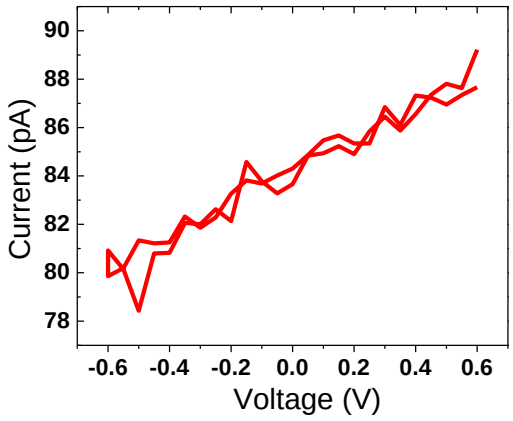


Figure 7.12 Current-voltage measurement between reservoirs R_1 and R_2 in the crossover fabrication scheme, suggesting excellent insulation between the perpendicular conductors.

A potential drawback of the SCALE process is the large footprint of the devices; e.g., the substrate area per transistor in this work is 4 mm^2. This is primarily due to the large size of the reservoirs (~0.5 mm diameter), necessitated by the limitations of our printing system. Future efforts will involve employing inkjet printheads capable of producing droplets with diameters 10 μm or smaller with automated x-y motion control.

This will allow reduction in the reservoir size by a factor of 10 enabling an estimated integration density of 2,000 devices cm^{-2}, an excellent figure of merit for printed electronics.

7.6 Experimental Details

Master Mold Fabrication

(i) Resistors and Capacitors: The master mold fabrication involved two photolithography cycles: Cycle (a) - A 4 in. silicon wafer (100) was prebaked at 200 °C for 5 min. Photoresist (NR71-1500P, Futurrex, Inc.) was spin-coated (300 rpm for 5s followed by 3000 rpm for 45 s) on the silicon wafer, followed by softbake at 150 °C for 1 min. A predesigned mask was placed above the photoresist-coated silicon wafer and exposed to UV light for 28 s in an ultraviolet exposing system (Karl Suss MA6). The exposed wafer was baked at 110 °C for 1 min. The silicon wafer was immersed in the developer solution (RD6, Futurrex, Inc.) for 18 s, rinsed with DI water, and dried. The patterned silicon wafer was then dry-etched to 5 μm depth by reactive ion etching (SLR 770 Deep Trench Etcher). The etch rate was 0.9 μm min^{-1}. After etching, the photoresist is completely removed by sonicating the wafer in 1165 resist remover for 10 min. Cycle (b) - The wafer was cleaned by a Piranha solution (1:1 H_2SO_4 with H_2O_2) for 20 min at 120 °C and then

rinsed with deionized (DI) water and dried. SU-8 2050 photoresist (MicroChem Corp.) was spin-coated on the silicon wafer (500 rpm for 5s followed by 3000 rpm for 30 s), followed by softbake at 65 °C for 3 min and 95 °C for 7 min. The photoresist-coated silicon wafer was exposed to UV light through a pre-designed mask for 24 s. The exposed wafer was baked at 65 °C for 1 min and 95 °C for 7 min. The silicon wafer was immersed in the SU-8 developer solution for 5 min, rinsed with isopropanol alcohol, and dried. The height of the SU-8 features was about 46 μm. The completed wafer was hard-baked at 180 °C for 10 min.

(ii) Transistors: The master mold fabrication involved three parts: (a) All steps in cycle (a) from (i) were performed to create 6 μm deep reservoirs and channels in a silicon wafer. (b) Again, cycle (a) from (i) is repeated, but the spin coating speed was 1800 rpm instead of 3000. The features were etched down to 3 μm. (c) All steps in cycle (b) from (i) were performed to obtain 46 μm high SU-8 features on the wafer surface.

(iii) Crossovers: The master mold fabrication involved three parts: (a) All steps in cycle (a) from (i) were performed to create 10 μm deep reservoirs and channels in a silicon wafer. (b) Again, cycle (a) from (i) is repeated, but the spin coating speed is kept 1800 rpm instead of 3000. The features were etched down to 5 μm. (c) All steps in cycle (b) from (i) were performed to obtain 46 μm high SU-8 features on the wafer surface.

Silanization: The patterened silicon master molds are silane-treated using the following procedure. The wafer was placed in a desiccator with 0.2 mL of trichloro(1*H*,1*H*,2*H*,2*H*-perfluorooctyl)silane (FOTS, Sigma Aldrich) solution. The desiccator was then pumped

down to 1 Torr of pressure to allow the FOTS solution to evaporate. The sample was left overnight for complete coverage.

PDMS Stamp Fabrication

For preparing the PDMS stamp, PDMS monomer and its curing agent (Dow Corning, Sylgard-184) were thoroughly mixed in a 10:1 weight ratio, respectively, and vacuum-degassed for 30 min. The Si master mold was placed in a plastic Petri dish, and 30 g of the PDMS prepolymer mixture was poured over the master mold and allowed to level out. The prepolymer mixture was then cured in an atmospheric oven at 60 °C for 12 h. After completely curing, the PDMS stamp was delaminated from the master mold. The stamp was then placed in an oven at 120 °C for 2 h.

Imprinted Flexible Substrate Fabrication

A flexible, UV-curable polymer, NOA-73 (Norland Products Inc.), was coated onto a 75 μm thick PET substrate. Prior to the coating, the PET substrate was air–plasma treated for 3 min to promote the adhesion of the coating. The PDMS stamp was inserted into the liquid coating and pressed using a glass roller to drive out any entrapped air bubbles at the coating–stamp interface. The coating was cured by exposure to UV light for 20 min. Following complete cure, the stamp was delaminated, leaving behind imprinted features in the NOA/PET substrate.

Inks Preparation

Reactive Ag ink was obtained from Electroninks, Inc. Carbon black ink was purchased from Methode Electronics, Inc. P3HT was purchased from Rieke Metals, Inc. and the ink was prepared by dissolving the polymer in 1,2-dichlorobenzene (5 mg mL^{-1}). An inkjet

printable version of PEDOT:PSS ink (0.8 wt% in H_2O) was purchased from Sigma Aldrich. The ink was sonicated for 10 min just before printing. Ion gel ink was prepared by co-dissolving (PS-PMMA-PS) and [EMIM][TFSA] in n-butyl acetate in the following proportions: 2 wt % polymer, 8 wt % ionic liquid, and 90 wt % solvent. All the inks were filtered through 0.45 μm filter prior to printing.

Ink Jet printing

A custom-built drop-on-demand inkjet printer was employed, consisting of a MicroFab nozzle (MJ-AT-01), a charge-coupled device (CCD) camera, a strobe and strobe driver, a jetting driver, and a system computer, which controlled the pulse waveform. A reservoir filled with ink (1 mL) was attached to the nozzle. The nozzle was moved in the x-y direction manually using micrometers. A unipolar waveform for all the inks was employed consisting of rise time of 5 μs, fall time of 5 μs, and drive voltage of 100 V. The dwell time for the Ag, P3HT, PEDOT:PSS and ion gel inks was 20, 25, 15 and 30 μs, respectively. All the inks were jetted at a frequency of 1 kHz. The nozzle's orifice diameter was 80 μm and diameters of a single ejected droplet for all the inks ranged between 60-70 μm. Prior to the printing, the substrate was air-plasma treated for 3 min to enhance its surface-energy to augment capillary flow. All printing was performed in ambient atmosphere.

Cu Electroless Plating

The Cu electroless plating solution contained 2.704 g of $CuSO_4 \cdot 5H_2O$, 10.25 g of ethylenediaminetetraacetic acid disodium salt, 3.25 g of NaOH, 100 mL of DI water, and 25 mL of an aqueous solution of formaldehyde (37% by weight). The temperature of the

bath was maintained at 55 °C. The printed substrate was kept in the bath for 3 min and taken out, rinsed with DI water, and dried using an air gun.

Electrical Characterization of Devices

The capacitance measurements were performed using a HP4192A LF impedance analyzer. Current-voltage characteristics for resistors and conductors were measured using two Keithley 236 source measurement units. Transistor current-voltage characteristics were measured using two Keithley 236 source measurement units and a Keithley 6517 electrometer. All measurements were performed in N_2 atmosphere.

7.7. Conclusions

In summary, we have developed a novel self-aligned process, referred to as SCALE, for producing multi-layered electronic devices on plastic substrates. Given the deformable nature of web substrates in continuous manufacturing systems, self-alignment of all the functional layers of electronic devices is of paramount importance. We have demonstrated that a wide variety of electronic devices including resistors, capacitors, transistors, and crossovers can be patterned using SCALE with excellent control over feature size, placement, and performance. The SCALE process essentially combines imprint lithography and inkjet printing, each of which can be implemented in R2R production formats[101, 128]. By guiding inkjet-printed liquid drops into pre-defined device cavities on the substrate surface via capillarity, valuable materials are deposited precisely where they are required, thereby maintaining the benefits of additive manufacturing. Currently, patterns smaller than 100 nm can be achieved using imprint lithography, and therefore, devices much smaller than those presented in this work are accessible by

SCALE. We anticipate that by employing state-of-the-art, low-volume (~1 pL) inkjet printers and optimized liquid distribution capillary networks, unprecedented device integration densities on plastic are possible with SCALE, opening up new avenues for R2R printed electronics.

Chapter 8 Ongoing and Future Research

8.1 Nanoscale Printed Conductors

To date, all work performed with SCALE has been with micron-scale channels. A future goal is to pattern nano-scale features using SCALE. Nano-scale printed conductive lines not only increase the device density but are of special interest for processing source-drain electrodes in high-speed thin film transistors. Several research groups have studied capillary flow in nanoscale, closed capillaries with low aspect ratios (w>>d).[129] Capillary channels as narrow as 5 nm have been explored to-date and the general fundamentals of capillary flow hold for simple liquids. Hence, it is expected that the size scale of the nanocapillaries should not be a limiting factor. From a fabrication standpoint, nanochannels can be created in the master mold either using either electron beam lithography or focused ion beam milling technique.

Based on the discussion of effect of channel geometry on ink travel length in microchannels in Chapter 6, it is expected that the flow velocity of the inks in nanochannels will be much slower (on the order of 10-100 μm /s) due to enhanced hydrostatic friction from the sidewalls. Because the exposed surface area to volume ratio of the inks remains constant for channels of any width but same height, the drying time of

the inks should largely remain unchanged in the nanochannels. Therefore, owing to the lower flow velocity, the total travel length in nanochannels may not be large enough for practical applications. Of course, travel length can be boosted by increasing channel height, but deeper channels require longer plating times to fill up. One way of increasing travel length is by employing a 'dual-channel' strategy as shown in Figure 8.1. A short microchannel (with optimized aspect ratio) can be directly connected to a reservoir, which, in turn, is connected to a nanochannel. Upon wicking into the microchannel, the ink is imparted a certain amount of momentum before entering the nanochannel. This built-in momentum should help the advancing liquid front to overcome the frictional losses from the walls of the nanochannel, pushing the ink much further down the channel. The transition to the nanochannel can be made more gradual by introducing a mild taper near the entrance.

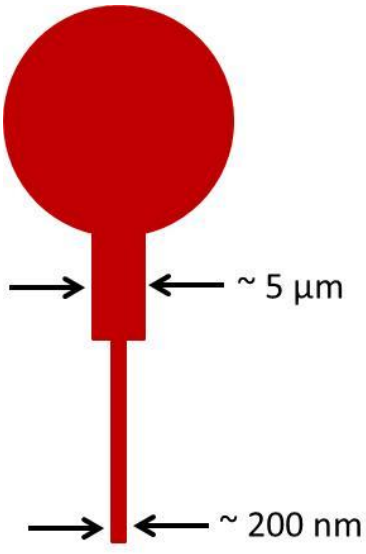


Figure 8.1 Dual-channel strategy for enhanced flow in nanochannels.

Interdigitated ion-gel capacitors with reasonable performance metrics were fabricated using SCALE. In our current demonstration, the line width and spacing of the Ag digits was 10 μm. Frequency response of these capacitors was limited to 1 kHz, owing to the large separation between the Ag digits. Using the above strategy, nanoscale conductors can be employed as the electrodes for the capacitors. Because of the excellent confinement of the Ag ink in the channels throughout the duration of capillary flow, it is conceivable that the minimum spacing between two electrodes can be brought down to below 1 μm. This value is comparable or smaller than the electrode separation in the previously demonstrated sandwich-type ion-gel capacitors, which show excellent capacitive behavior at frequencies as high as 100 KHz.[130] Alternatively, sandwich type ion-gel capacitors can also be fabricated using a three-tier structure, using strategies discussed in the following sections.

8.2 Novel Architectures for High-Speed Transistors

To date, we have demonstrated side-gated EGTs using the SCALE process. The side-gated geometry relaxes the strict alignment requirement of patterning the gate electrode on top the source-drain channel. However, physically offsetting the gate electrode to the side often leads to an increased separation from the transistor channel. This increases the polarization response time of the gel, thereby decreasing transistor speed. Also, current SCALE EGTs have a large overlap between the electrolyte and the semiconductor layers. A considerable overlap area (~ 50 %) lies outside of the transistor

channel area caused by the uninhibited flow of the inks in open-ended capillary channels, leading to parasitic capacitances.

In order to address these issues, we have devised novel structures for creating aligned-gate EGTs, wherein the gate electrode is patterned directly either on top or beneath the transistor channel. Also, efforts have been made to minimize the electrolyte-semiconductor interfacial area. An example structure is shown in Figure 8.2. In this top-gated structure, Cu/Ag source-drain electrodes and P3HT film were patterned similarly to the side gated EGTs (see Section 7.3). To pattern the dielectric, the ion gel ink is dispensed into the gray reservoir. The tall channel walls drive the ink on top of the partially enclosed P3HT-coated channel, all the way down to the open-end of the channel. As shown in Figure 8.3a, the ink comes to a dramatic halt at the open-end, i.e., no capillary flow is observed in the P3HT-coated channel.

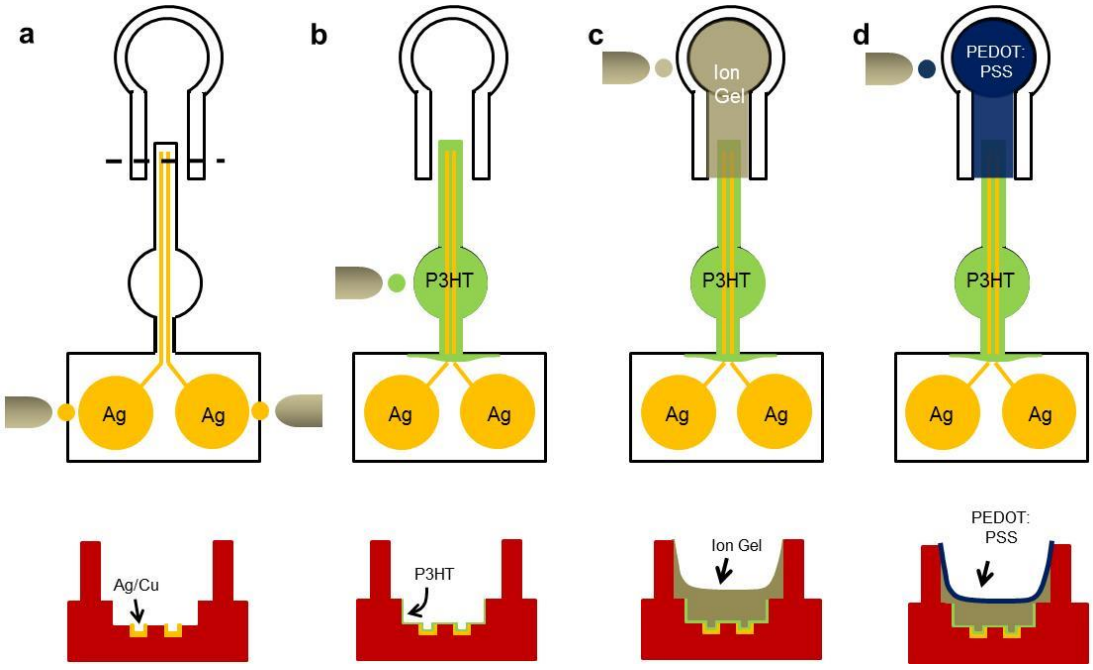


Figure 8.2 Top-gated EGTs using SCALE.

The rheological property of the ion-gel ink plays an important role in determining the travel length of the ink. The optimized ion gel ink consisted of (PS-PMMA-PS) and [EMIM][TFSA] co-dissolved in a solvent mixture of n-butyl acetate (BA) and dimethylformamide (DMF) in the following proportions (wt.%): 2:8:45:45, respectively. Absence of DMF in the ink led to an exaggerated flow into the P3HT-coated channel, whereas an ion gel ink, devoid of BA, did not enter into the P3HT-coated channel at all. Due to the presence of the hydrophobic side chains, the surface of a P3HT film is also hydrophobic. DMF is a high-surface tension liquid (37.10 mN/m) which does not wet the surface of P3HT, whereas BA (surface tension: 25.30 mN/m) spreads nicely on P3HT. Evidently, a 1:1 solvent mixing ratio of the solvents keeps the surface tension of the ink low enough to ensure its descent into the P3HT-coated channel, but high enough that there is no subsequent capillary flow inside the P3HT-coated channel. Therefore, P3HT-gel overlap is dictated solely by the length of the hydrophilic walls of outermost channel (Figure 8.3a).

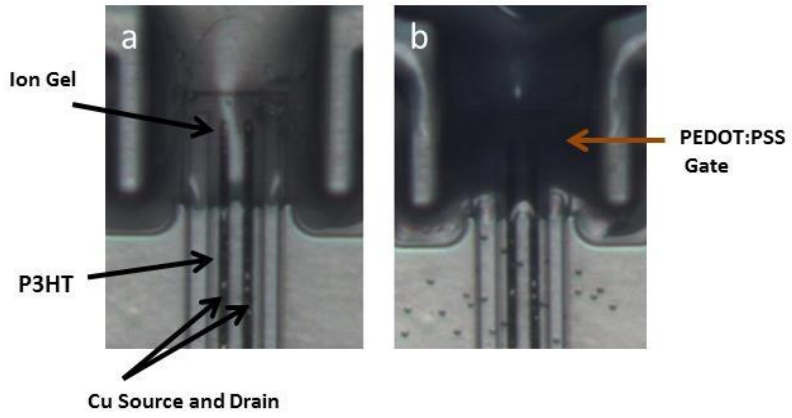


Figure 8.3 Optical micrographs of top-gated EGTs using SCALE. Both (a) ion gel and (b) PEDOT:PSS are precisely patterned on top of a portion of the transistor channel.

The gate ink (PEDOT:PSS) was also dispensed into the ion gel reservoir. Owing to the large height of the channel walls, PEDOT:PSS ink is able to flow on top of the pre-deposited ion gel film. The ink also comes to an automatic halt near the open-end of the channel (Figure 8.3b). This time, the termination is produced by the thicker ion gel film near the open-end channel. The thickness gradient is a direct result of solute migration to the outer rim during the drying process, as also observed in the coffee ring effect on flat surfaces.

The top-gated devices displayed the usual switching behavior in the quasi-static electrical measurements. The hysteresis between the forward and reverse scans was almost completely eliminated, indicating complete oxidation and reduction of the P3HT film. The reduced separation between the gate and the P3HT film allows enough time for the ions to diffuse in and out of the permeable P3HT film for gate voltage sweep-rates as high as 0.1 V s^{-1}. The devices were also assessed for their speed via dynamic inverter measurements. The EGTs were connected in series with 1 MΩ resistors, and an input

square wave signal, switching between 0.5 V and -0.5 V, was applied at a fixed V_{DD} = -0.8 V. The output signal was recorded for different frequencies of the input signal. As demonstrated in Figure 8.4, the device showed a clear inverter response for 10 Hz input signal, switching ideally between 0 and V_{DD} without any delay or shape distortion. Near-ideal switching was obtained even for 200 Hz input signal, although spikes in the switching characteristics were also evident. These spikes can be attributed to parasitic capacitances, as discussed later. For frequencies higher than 200 Hz, the width of the parasitic spikes became more pronounced and the amplitude of the output signal decreased progressively. No inverter action was seen for frequencies higher than 1 kHz.

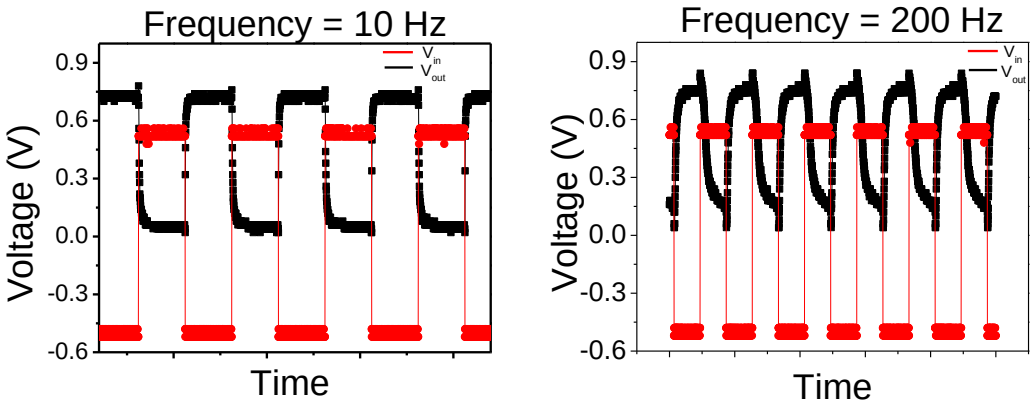


Figure 8.4 Inverter measurements of top-gated EGTs at 10 Hz and 200 Hz.

Quasi-static transfer curve measurements taken after continuous inverter operation at 100 Hz (≈ 60000 switching cycles) for 10 min revealed a significant amount of device degradation, as shown in Figure 8.5. The on-current decreased by an order of magnitude and the threshold voltage shifted by – 300 mV. This is possibly due to oxidation of the Cu contacts at positive biases in the presence of the electrolyte.[82] Using electrochemically stable carbon-based conductors as the source-drain contacts can be one

way of circumventing this problem. A thin coat of graphene or carbon black over the Cu electrodes can provide the necessary electrochemical stability to the contacts without compromising the electrical conductivity.

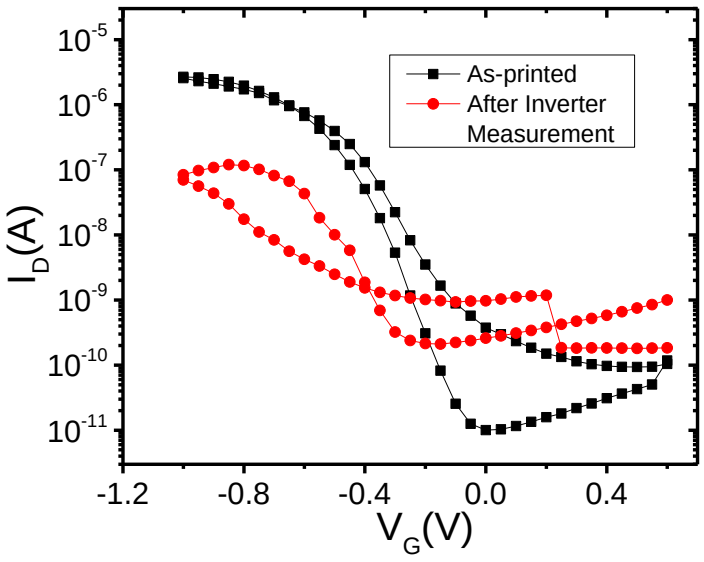


Figure 8.5 Transfer characteristics of top-gated EGTs before and after inverter measurements.

Because of the exceptionally high capacitance of the ion-gel dielectric, parasitic capacitances play a dominant role in during the dynamic operation of EGTs. As shown in Fig. 8.4a, dynamic inverter measurements at 200 Hz display voltage spikes in the output characteristics for each input voltage flip. The width of the spikes increases with increasing frequency (not shown), distorting the shape of the output signal to the effect that no inversion is observed after a certain frequency. In our SCALE devices, the gate forms a capacitor each with the source, the drain and the semiconductor. The parasitic spikes in inverter measurements are caused by instantaneous charging and discharging of the gate-drain capacitor at every input voltage inversion. It can be mathematically shown

that the width of the parasitic spike or, in other words, the degree of non-ideality in the output characteristics is directly proportional to the frequency. Therefore, to enhance the dynamic performance of our devices, it is critical that gate-to-drain capacitance be minimized. This can be achieved by minimizing or eliminating contact between the ion gel and the drain electrode. In our current top-gated device architecture, this can be accomplished by sealing the source-drain contacts by depositing an insulating polymer such as PMMA into their respective channels via capillary flow. In that case, according to the rule of capacitors in series, the PMMA/ion gel bilayer capacitance will be primarily determined by the PMMA capacitance which is three orders of magnitude lower than the ion gel capacitance. Alternatively, a SCALE architecture can be conceived where the ion gel film is patterned in close proximity to the contacts while avoiding any kind of overlap.

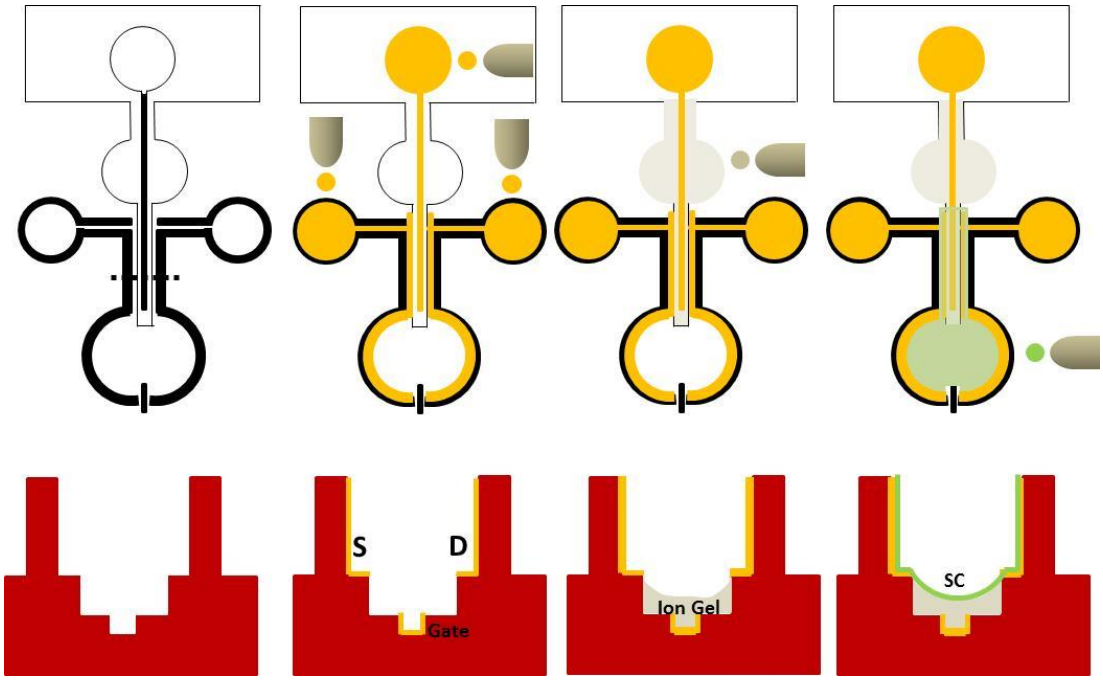


Figure 8.6 Bottom-gated EGTs using SCALE

We devised a bottom-gated architecture that could eliminate direct contact between the ion-gel and the contacts. As depicted in Figure 8.6, this three-tier device architecture necessitated only three printing steps. Firstly, the Ag/Cu gate (at tier I), source and drain (at tier III) electrodes were patterned simultaneously via the printing and plating approach. Secondly, the gate electrode was insulated by depositing the ion-gel ink in the tier II channel. Importantly, as can be seen in Figure 8.7a, the ion gel film makes contact with the source-drain electrodes only at the edges. The device was completed by delivering P3HT ink (0.5 mg/mL in dichlorobenzene) in the tier III channel which flowed atop the ion gel film. It is important to note that the solvent of the P3HT ink attacks the ion-gel film. However, the evaporation of the ink solvent inside the channel is fast enough to prevent damage to the underlying ion-gel film. Nonetheless, a thick ion gel film is essential to avoid shorting.

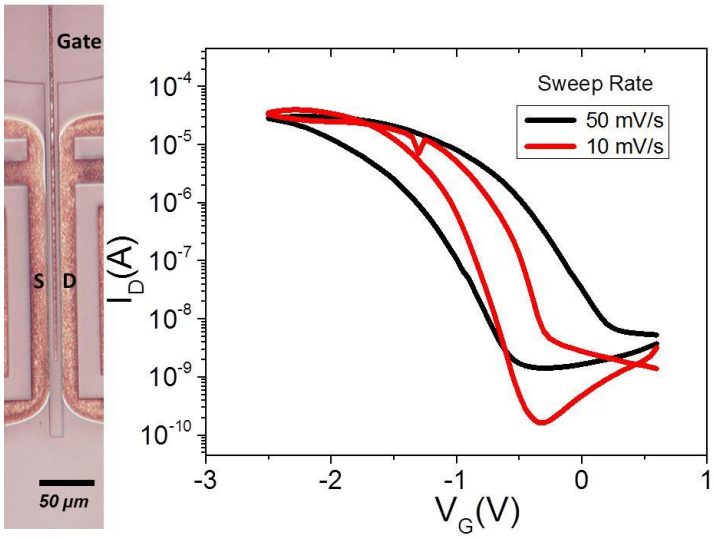


Figure 8.7 Transfer characteristics of bottom-gated EGTs.

Quasi-static I_D-V_G measurements revealed that the device turned on around -0.5 V (compared to 0 V for the top and side gated devices) with a current amplification ratio greater than 10^4. However, a significant current hysteresis was also observed between the forward and reverse scans. Device turn-on at -0.5 V as opposed to 0 V is consistent with the work function difference of the Cu and PEDOT:PSS gate electrodes.

Hysteresis is directly related to the choice of the gate electrode and electrolyte-gate interfacial area. Because of the diffusion of the ions into the P3HT film, a very large three dimensional capacitor is formed at the P3HT-ion gel interface during the forward scan. The condition of no hysteresis is obtained when this capacitor is able to discharge itself fully while simultaneously charging the capacitor at the gate-electrolyte interface. Since capacitance scales with area, a large gate-electrolyte interface is, therefore, important to balance the two capacitors and eliminate hysteresis.

In our bottom-gate devices, the Cu gate is impermeable to the ions and the Cu-ion gel interface is considerably smaller than P3HT-ion gel interface. Hence, there is a significant mismatch between the capacitances at the two interfaces which leads to hysteresis. An effective way of reducing hysteresis would be to deposit a thin film of PEDOT:PSS atop the Cu gate electrode by capillary flow. This Cu/PEDOT:PSS bilayer gate electrode retains the high conductivity of the metal while providing a large interfacial gate capacitance during EGT operation because of ion-permeability into the PEDOT:PSS film. However, we find that flowing PEDOT:PSS ink in a Cu-filled channel is not trivial. Due to the hydrophobicity of the Cu-filled channel, the ink tends to de-wet from the channel area.

One possible solution is to make the Cu-filled channel extremely hydrophilic by using suitable self-assembled monolayers (SAMs). Hydrophilic phosphonic acid SAMs are known to adhere quite well to the native oxide on the Cu surface,[131] rendering a water contact angle smaller than 20°. The SAM treatment step is not too intensive from a manufacturing standpoint as well, as the printed Cu web substrates can be simply fed through an alcohol-based SAM bath for a few minutes to get sufficient coverage on the Cu surface.

Preliminary experiments were also performed to fabricate SCALE TFTs with more conventional, polymeric dielectrics such as cross-linked poly (methyl methacrylate) (PMMA), and SU-8. Employing these materials as gate dielectrics increases the operational voltages of the devices considerably. However, when patterned efficiently, these are known to be faster than EGTs, with the best reported switching time around 1 μs.[132] Short channel length, a high mobility semiconductor and an aligned gate, i.e. gate electrode patterned with minimum overlap with source-drain electrodes, are some of the crucial requirements for high-speed operation of these TFTs. However, the strict alignment requirement is difficult to achieve in continuous manufacturing systems. Our goal is to assess the suitability of the SCALE process in fabricating aligned, top-and bottom-gated TFTs based on conventional dielectrics.

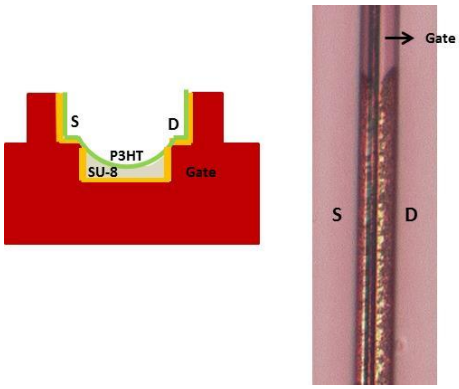


Figure 8.8 Bottom-gate aligned transistors using SCALE employing SU-8 gate dielectric.

For our bottom-gated device architecture (Figure 8.8), we used a two- tier structure where the gate was patterned in the lower tier by filling an Ag ink. An SU-8 dielectric ink was then deposited in the same channel on top of the Ag electrode. The ink was annealed for complete solvent removal and then physically cross-linked by UV irradiation. The cross-linking step not only enhances the dielectric constant of the film, but also tolerance to ink solvents in the subsequent printing steps. The device is completed by sequentially depositing the source, drain and the semiconductor inks in the upper tier cavities. Upon TFT measurements, we found that gate leakage current (of the order of µAs) was always equal to the channel current, indicating that the devices were short. This was true even for thicker dielectric films. The origin of shorting can be understood from the drying profiles of the gate and dielectric inks inside the channel. As discussed earlier, during the drying process, the ink is pinned to the top two corners of a channel. The pinning effect produces a thin film of the solute not only on the channel floor but also on the sidewalls. Moving upwards along a sidewall face, the film thickness decreases progressively due to solute redistribution. Therefore, despite a thick dielectric

film in the middle of the channel, there is still a possibility of incomplete insulation of the gate near the channel edges.

A flat gate profile would be ideal to address the issue of shorting. However, it is difficult to obtain a flat film from drying of liquid solutions in confined, rectangular geometries. A more convenient approach would be to start with a commercially-available, metal-patterned plastic web substrate. For instance, a PET substrate, patterned with an array of 100 × 100 μm^2 gold patches on it, which serve as the gate electrodes. A thin coating of an imprint resist can be applied to the web substrate using a large-area coating technique, e.g., slot-die coating. High-resolution features, encoded with the geometrical information to process the source, drain and semiconductor layers, can be imprinted into the resist coating coarsely aligned to the underlying low-resolution gates. The ultra-thin (< 100 nm) residual resist from the imprinting process can serve as the gate dielectric itself. Access to the gate, essential for wiring up individual devices, can be gained through electrical vias created by inkjet printing a resist etchant in selected areas. However, this approach cannot be claimed to be fully self-aligned because of the large gate footprint, which is an unavoidable source for parasitic capacitances. Because the gate electrode is much wider, the effective capacitance value will be determined by the width of the source-drain electrodes and interconnects. Therefore, the key to processing high-speed devices using this approach hinges on the ability to process nanoscale source and drain. In principle, features down to 50 nm can be achieved using nanoimprint lithography. Filling these nanochannels with conductive inks remains an open challenge and is a subject of ongoing research. Also, metal-filled reservoirs, a natural artefact of the

SCALE process, would also contribute significantly to the parasitics. An alternative method to fill nanotrenches with conductive inks, without utilizing low-resolution reservoirs, will be required. We have recently developed one such method, which is discussed later.

We have also fabricated top-gated devices using conventional dielectric materials. The source, drain, semiconductor and the dielectric layers were fabricated sequentially using the SCALE process, using methods described earlier. A unique strategy was employed to process an aligned-gate without producing shorts (Figure 8.9). Firstly, a 6 μm-thick coating of positive photoresist (AZ-9260, MicroChemicals GmbH) was applied on the printed substrate. The substrate was illuminated with UV-light for 56 s through the backside. The printed Ag metal traces block the UV light, acting as a photomask for the overlying photoresist. The substrate is then immersed in a developer solution and the exposed regions of the photoresist are removed. The remaining photoresist on the substrate forms a channel directly on top of the semiconductor channel. Using capillarity, the channel is then filled with PEDOT:PSS ink to create an aligned gate.

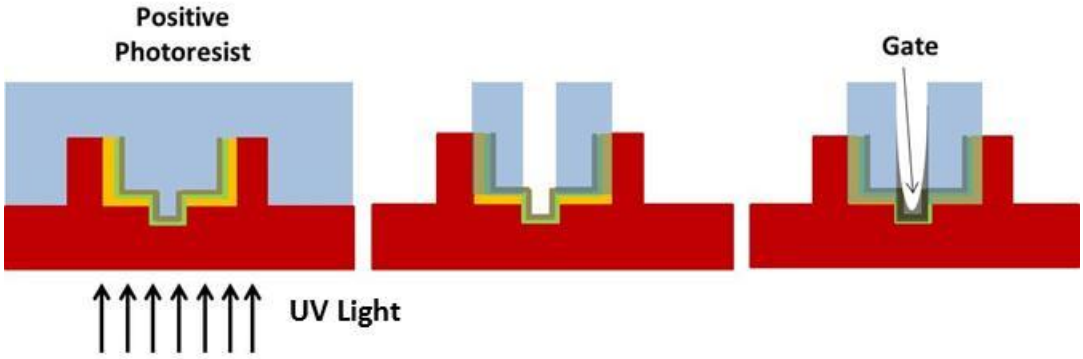


Figure 8.9 Top-gate aligned transistors by a combination of SCALE and backside exposure.

Electrical measurements confirmed that, unlike the bottom-gated devices, the top-gated devices did not short. The devices, however, did not turn on. One possible reason could be the degradation of the organic semiconductor from the UV radiation. UV illumination in air can cause scission of the polymer backbone or conjugation disruption in the polythiophene films. Although degradation of the organic semiconductor film can be suppressed by performing UV exposure in an inert atmosphere, this strategy is not suitable for continuous manufacturing systems. A more practical way would be to employ transparent metal oxides as the semiconductor layers, which are not degraded by UV radiation. Zinc oxide and indium-gallium-zinc oxide can be potential candidates.[34, 133]

Side-gated EGTs display the usual TFT metrics, but are slow due to the increased distance the ions need to travel between the source-drain channel and the gate electrode. In order to achieve the MHz switching speed goal, this offset needs be minimized by at least an order of magnitude and potentially brought down to the sub-micron regime. Also, as discussed earlier, to minimize the parasitic capacitance at the gel-electrode interface, the source, drain and gate electrode widths should also be in the nanoscale regime. In an example device layout of a side-gated nano-EGT, the source and the drain electrodes are flanked by a split gate on either side. The ratio of the device channel width to channel length is 10 μm/500 nm, the gate electrode offset is 500 nm, and the line widths of each of the electrodes are also 500 nm. However, a daunting challenge is to print the semiconductor ink precisely in the nanoscale gap between the source-drain electrodes, without shorting the gate electrode (an alignment tolerance of a few 100 nanometers). In

principle, this device can be processed completely by SCALE itself. However, a major drawback of the SCALE process is the large footprint of the devices because of the presence of low-resolution reservoirs. For instance, patterning nano-EGTs by SCALE requires a total substrate area of around 10000 μm^2 whereas the active area of the device is only 50 μm^2. Therefore, device integration densities with the SCALE process, although advanced over other printing methods, still have room for improvement.

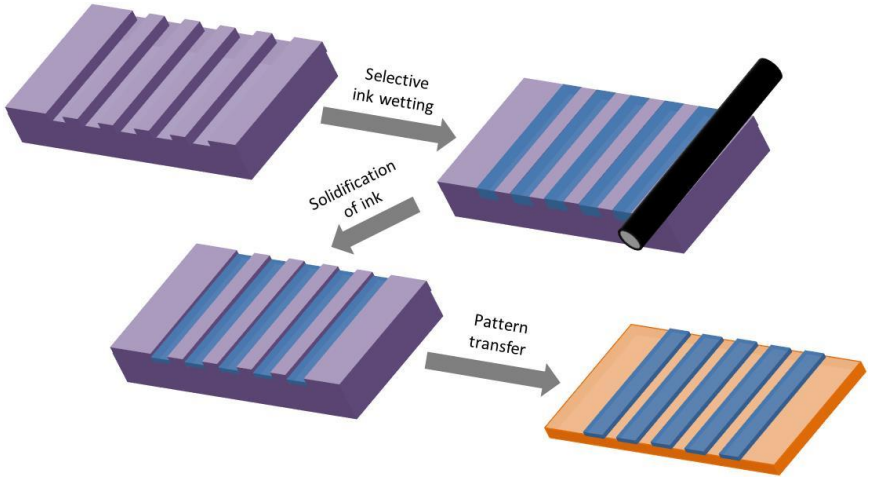


Figure 8.10 Discontinuous dewetting-based transfer printing method for nanoscale conductive lines.

With the aim of patterning nanoscale traces, we have developed a new transfer printing method. This transfer printing method is high-resolution, scalable, and highly parallel. Figure 8.10 illustrates the series of steps for patterning functional materials using this method. Firstly, cytop-coated Si molds were fabricated using standard photolithography procedures. Cytop has very low surface energy (19 mJ m^{-2}). We employed a hard mold in this work, but a soft, flexible mold made from low surface energy materials such as polyurethane acrylate (PUA) and polydimethylsiloxane (PDMS) should be equally effective. The patterned mold was then filled with an ink solution using

selective inking. Discontinuous dewetting was used to fill only the recessed areas of the mold with the ink solution. By dragging a deposited ink solution over the patterned mold, the ink solution moves over the surface of the mold, filling the trenches without leaving any residues on the raised surface (Fig. 1b). Discontinuous dewetting takes advantage of the interfacial free energy difference between the mold and the ink solution, and the ink solution must have a surface free energy appropriate to the mold. The rate of dragging the solution, the aspect ratio of the features in the mold, and the viscosity of the ink solution also determine the success of the discontinuous dewetting process. Unlike gravure printing, this method does not require an aggressive doctoring step which can potentially damage the mold. Also, it is compatible with a broad range of ink properties, and is free from the problem of printhead clogging.

The filled ink is next solidified by curing it. Almost no residue remains on the protruding surfaces of the mold as a result of the selective inking. Next, a PET substrate, coated with a thin film of liquid epoxy, is brought into conformal contact with the mold. The epoxy is cured via UV illumination through the PET substrate. Upon complete solidification of the epoxy layer, the PET substrate is delaminated from the mold. The printed traces inside the mold trenches are transferred to the epoxy/PET substrate.

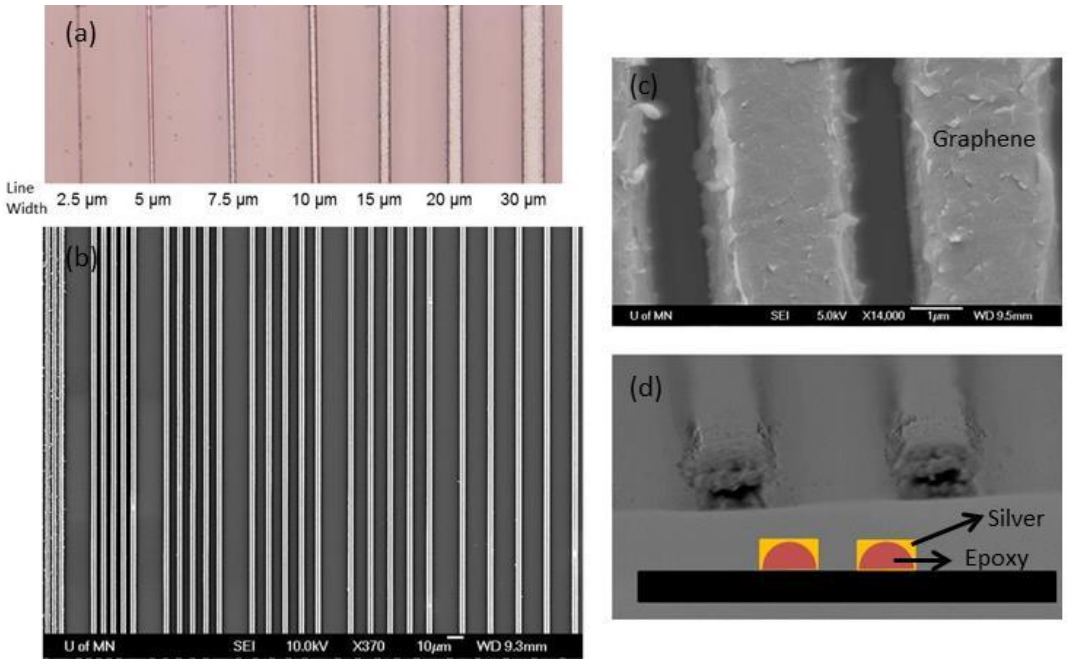


Figure 8.11 Examples of transfer printed (a, b and d) Ag, and (c) graphene lines.

Examples of transfer printed lines are shown in Figure 8.11. Silver features with line widths all the way from 30 µm to 2.5 µm could be patterned using this approach. The upper limit is set by the aspect ratio (height/width) of the trench. Depending on the channel height, the width should be low enough for liquid confinement in the channels. The lower limit is defined by the resolution of the mold in our case, but we believe features much smaller than 2.5 µm are accessible using this method. The minimum line spacing of about 1 µm was achieved, as shown in the SEM image in Figure 8.11b. Also, the edge definition of the printed lines is extremely sharp, which is a major advantage over other printing methods. The region between the lines is remarkably clean for all spacings investigated between 1 and 20 µm. It is conceivable that these characteristics would also be consistent in the sub-micron regime. The cross-section of the printed Ag

lines is displayed in Figure 8. 11d. A thin film of Ag covers the surface of raised epoxy structure on all the three sides. Also, we find that the transfer printing method is compatible with graphene inks as well. As shown in Fig. 8.11 c, we could obtain graphene lines with line width and spacing down to 2.5 and 1 μm, respectively.

This transfer printed method, combined with SCALE and aerosol-jet printing, can be a potential route to printed nano-EGTs, as shown in Figure 8.12. In the first step, the source, drain and the gate electrodes can be patterned simultaneously by the transfer printing method, each with line width and spacing of 500 nm. Due to the raised structure of the transfer printed lines, two adjacent printed lines form a channel by themselves. Now, using the SCALE process, this nanochannel between the source and the drain electrodes can be filled with a semiconductor ink. Although flow of liquids in open capillary channels is yet to be explored, a total travel length of 10 μm would suffice for nano-EGTs. The uniqueness of the SCALE process is that the semiconductor ink flows strictly inside the channel without spilling over. Therefore, a possibility of shorting with the gate electrode is eliminated despite a separation of only 500 nm. In this way, the source, drain, gate and semiconductor are patterned over a lateral width of only 2.5 μm. To our knowledge, none of the existing printing methods can provide this level of registration accuracy. Finally using aerosol jet printing, an ion gel film (width= 50 μm) can be printed across the transistor channel and the gate. Because the lateral dimensions of the underlying features is only a couple of microns, an alignment tolerance larger than 40 μm is available to aerosol jet printing.

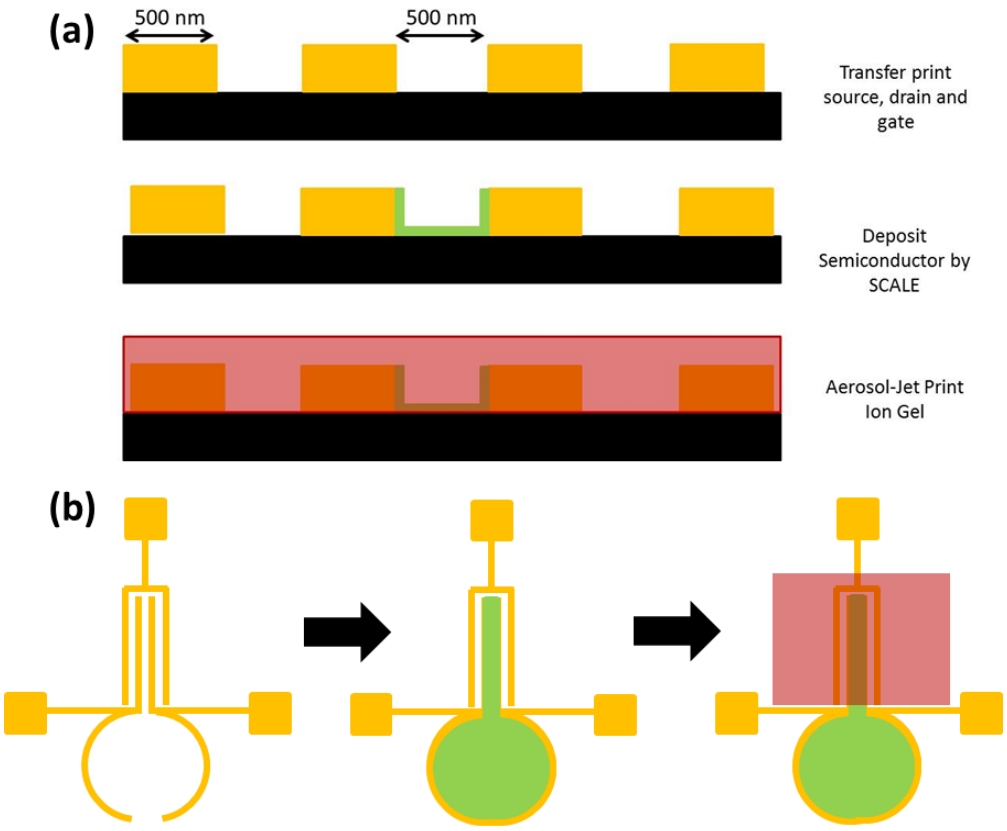


Figure 8.12 Strategy for fabrication of misalignment-tolerant nanoscale EGTs by a combination of transfer printing, SCALE, and aerosol-jet printing.

It is important to estimate the integration densities that can be achieved using this strategy. The total device footprint is only 50 x 50 μm^2. It is worthwhile noting that, unlike the SCALE process, no low-resolution reservoirs are required for ink delivery. The semiconductor ink can also be inkjet printed into a reservoir-like cavity created using the tail-ends of the printed source-drain electrodes, making use of device layout and wiring schemes. A preliminary analysis shows that we can easily produce a complementary inverter in a 200 x 200 μm^2 area. This translates to 1250 inverters/cm^2 (or 2500 TFTs/cm^2), an unprecedented number for printed electronics.

8.3 Aligned Single-Crystal Organic Semiconductors

Lateral confinement and directed flow of liquid semiconductor inks in capillary channels can assist alignment of crystalline domains in semiconductor films. In particular, small molecule organic semiconductors (OSCs), such as 6,13(bis-triisopropylsilylethynyl) pentacene (TIPS-pentacene) are good candidates to study this phenomenon.[134] Small molecule OSCs typically show poor film morphology with traditional printing techniques. For instance, an inkjet printed TIPS-pentacene droplet on a flat substrate leaves behind a polycrystalline film with randomly oriented crystallites (Figure 8.13a). In contrast, TIPS-pentacene ink flowed in an open microchannel (w = 10 μm) leaves a higher-quality film upon solvent evaporation, as confirmed by cross-polarized optical microscopy. In Figure 8.13b, the left and the right images show the same area under different sample rotation angles. The crystalline domains extinguished polarized light almost completely in the left images, while the maxima in intensity occurred when the substrate was rotated ≈ 45° as shown in the right images. The change in intensity of the crystalline domains indicates that the thin films formed in the capillary channel are more aligned compared to the flat substrate.

When a nucleation event occurs, the crystal growth takes place in all directions if the substrate is not patterned. However, in narrow channels, TIPS-pentacene crystals that grow misoriented relative to the channel terminate at the channel walls. As a result, only crystalline domains that are aligned parallel to the channel grow continuously and form long, aligned domains. Effect of other factors such as channel geometry and ink concentration in dictating growth dynamics is a subject of ongoing research.

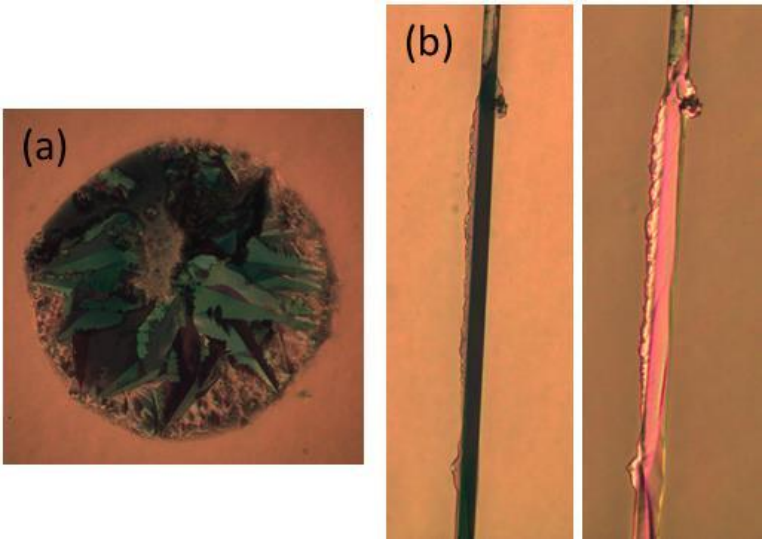


Figure 8.13 (a) Inkjet–printed TIPS-pentacene film on flat epoxy substrate, and (b) Cross-polarized optical microscope image of TIPS-pentacene film in a capillary channel.

8.4 Exploring Fundamentals of New Printing Processes

Visualization of Aerosol Jet Printing

This thesis thoroughly investigates the process space for aerosol jet printing, with the aim of understanding the physical principles that govern this new printing method. However, these results are ex post facto, i.e., derived from measuring the properties of the printed lines. High-speed imaging of the aerosol jet would be an excellent dynamic tool to provide great insights for strengthening our current understanding of the process. Visualization of the variation of jet diameter and speed upon changing the focusing ratio would further authenticate the arguments on line width and thickness. In particular, physical limits on the minimum jet diameter and maximum jet velocity will be revealed. These results will be crucial in achieving the goal of sub-10 μm resolution with aerosol-

jet printing. High-speed visualization can also be an effective tool to understand overspray. Overspray is a phenomenological problem with aerosol jet printing, which is especially detrimental for processing closely-spaced, high -resolution lines. The origins of overspray are not clearly understood. One possible source of overspray is a wide particle size distribution of the aerosol at the time of ejection from the jet. The smaller particles have lesser inertial momentum and are, therefore, more likely to be thrown off the jet axis at the time of ejection. Using a carrier gas pre-saturated with the solvent of the aerosol can suppress evaporation of the aerosol solvent in flight, and help maintain the tight particle size distribution. Another source of overspray can be from the bouncing of the aerosol particles upon impact with the substrate surface. This is a known phenomenon in other spray-based coating methods. High-speed imaging of jet-ejection and jet-substrate interaction can provide more insights into the origin of overspray. Systematic experiments can be performed with variety of inks having different surface tension, viscosity and vapor pressure values to pin down the rheological properties for minimal overspray. Once the appropriate ink is identified, the entire process space can be analyzed to determine regions of high overspray. Preliminary investigations have shown that overspray is maximum for high sheath gas flow rates, low carrier gas flow rates and high working distances.

Fundamentals of Liquid Flow in Open Microchannels

Capillary flow of liquid inks on microstructured plastic surfaces is central to both the IPP and SCALE process. In both the processes, liquid inks are flowed in open

microchannels via capillarity. The total travel length of the inks in the channels dictates the patterning of functional materials.

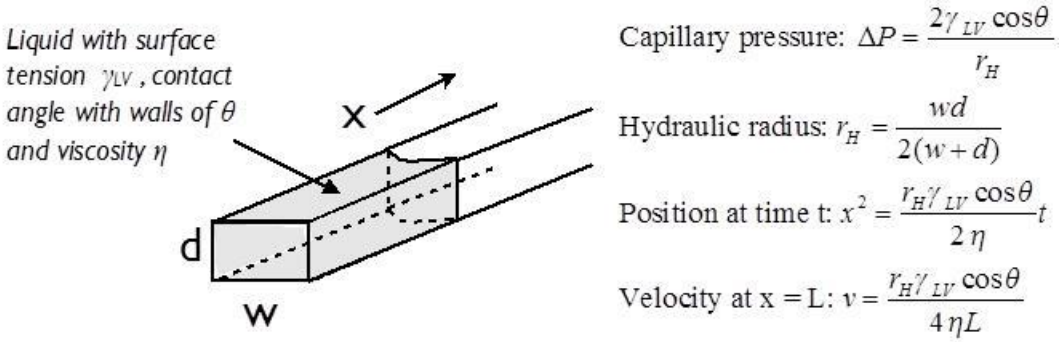


Figure 8.14 Fundamentals of capillary driven flow into a closed rectangular cavity connected on the left to a filled reservoir (not shown).

The well-established fundamentals of capillary-driven flow have been shown to describe flow in small channels, even down the μm and nm scale. For example, consider the flow of liquid from a large reservoir into a closed, rectangular capillary channel. See Figure 8.14. For the liquid to enter into the capillary, good wetting of the capillary walls (low contact angle) is necessary so that the flow is thermodynamically favorable. Once the liquid wets the capillary walls, a curved meniscus forms, leading to a pressure gradient between the reservoir and the capillary (i.e., the capillary pressure, ΔP). This pressure difference drives flow down the capillary with viscous resistance provided by friction at the capillary walls. The classic Washburn equation describing the liquid front position, x, and the related expression for velocity are shown in Figure 8.14. From these expressions, it is clear that the capillary filling speed for a given length of channel increases as the wettability of the walls increases (i.e., θ decreases), the viscosity of the

liquid decreases and the surface tension of the liquid increases. More complex equations are available in the literature for flow in open capillary channels. Here, the surface tension of the liquid plays an additional role in the thermodynamic condition for liquid entry into the channel and in the flow process itself. However, again the general trend offered by the Washburn equation holds and provides guidance.

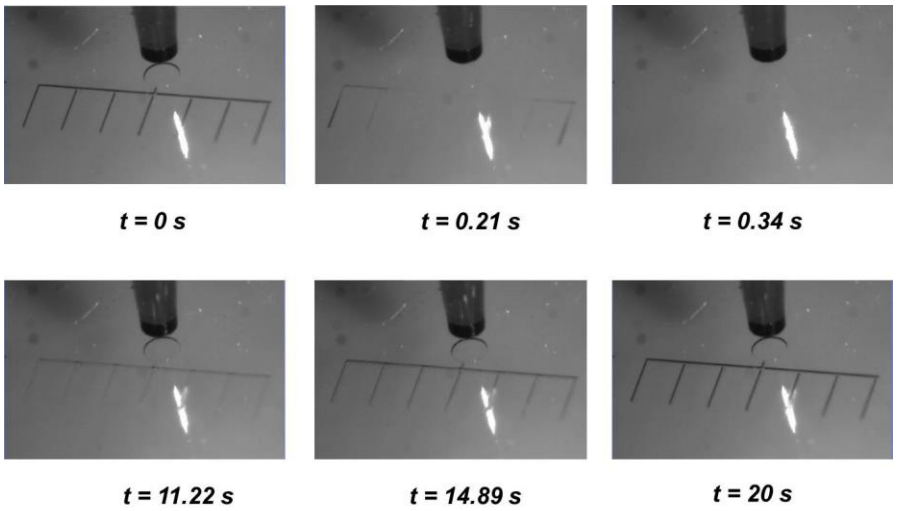


Figure 8.15 A drop-on-demand ink dispenser located above an imprinted reservoir and imprinted 50 μm wide microchannels. Sequential photos show liquid P3HT ink filling channels by capillarity (0.21 s), complete filling (0.34 s), and drying (11-20 s). Loss of contrast at 0.21 s and 0.34 s is due to refractive index matching of liquid ink with substrate.

Whereas travel length studies of reactive silver ink were performed in Chapter 6, more investigation on ink flow fundamentals is required to completely map out the process. Using model fluids and top-view optical microscopy, travel velocity of the advancing liquid front inside the microchannel can be measured for different channel widths and depths. In our experiments with P3HT ink flowed in 50 μm wide, 10 μm

deep microchannels (see Figure 8.15), the advancing liquid front travelled a distance of 3 mm in about 0.5 seconds, yielding an average flow velocity of 6 mm s^{-1}. This is roughly consistent with the estimated travel velocities using the Washburn equation. However, solvent evaporation during fluid flow complicates the precise mapping of the kinetics of process. Therefore, a good starting point would be to work with model liquids with negligible vapor pressure such as glycerol-water mixtures or NOA-73.

Glycerol-water mixtures can be prepared with a range of surface tension and viscosity values. It is obvious that lower viscosity fluids will have higher travel velocities. However, role of surface tension on travel velocities is not clearly understood. Equation 6.1 suggests that capillary pressure increases with increasing surface tension, therefore, it is expected that high surface tension fluids should have higher travel velocities. Experimentally, we find that low-surface tension fluids (e.g. reactive silver ink) show much greater travel lengths than high surface tension fluids (e.g. PEDOT:PSS ink). Systematic experiments based on water-glycerol mixtures can help explain this anomalous observation.

In Figure 6.4, we observed an optimal channel aspect ratio, roughly close to 1 for, maximum travel length. It is argued that capillary pressure and flow resistance balance themselves for this aspect ratio. However, mathematical origins of this phenomenon are not fully understood. Fundamental studies of travel velocity with channel geometry using model fluids can equip us with the necessary mathematical arsenal to unravel the mystery of this special aspect ratio. More importantly, these results can help us design the

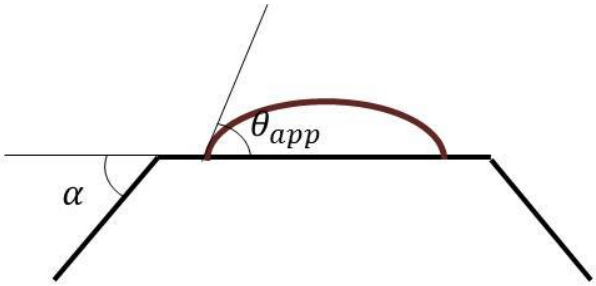
appropriate geometry of nanochannels, which are expensive to fabricate and where an extensive trial-and-error approach cannot be afforded.

After establishing concrete relationships with model inks, similar experiments can be performed with real inks. Solvent evaporation during the migration of the inks would have to be accounted for. An important variable is the travel time of the ink in the channels, which is set by the onset of solidification at the advancing liquid front. Theoretically speaking, solvent evaporation is dependent only on the ratio of exposed surface area and volume of the ink in the channel; therefore, total travel time should not be a function of width, for channels of the same depth. By the same argument, travel time is expected to be longer in deeper channels. Similarly, high vapor pressure inks should have longer travel times due to slower evaporation rates. However, these arguments need to be authenticated via systematic fundamental studies. Reactive silver inks are good candidate materials for these tests as they show a distinct color change upon solvent evaporation.

Pinning of Liquids on Sharp Micro-steps

Several SCALE devices employ a ‘stopper’ channel to halt liquid flow in open ended channels. This is important for discrete patterning of materials. The stopper channel serves as a sharp micro-step on the substrate surface that pins an advancing liquid contact line. We have observed that pinning effect is observed for PEDOT:PSS, ion gel and reactive silver inks. However, the ion gel ink, after multiple printing attempts, tripped into and across a stopper channel. Intuitively, one would expect that an advancing liquid front should always trip over into the stopper channel. However, the pinning of an

advancing liquid front to a sharp microedge on the substrate surface is dictated by the Gibbs criterion, as explained in Figure 8.16.



$$\theta_{app} = \theta_{cr} = \theta_{eq} + \alpha$$

Figure 8.16 Gibbs criterion for liquid pinning on sharp microsteps.

Pinning is primarily dictated by the dynamic contact angle of the advancing liquid front (θ_{app}), equilibrium contact angle of the ink with the substrate (θ_{eq}), and edge sharpness ($\propto$). We believe that, for the majority of the inks employed in the SCALE process, the dynamic contact angle of the ink is always smaller than the sum of the equilibrium contact angle and edge sharpness. However, for multiple deposits of the same material at the edge, the sharpness of the edge gets blunted with every printing step, which ultimately leads to the descent of the incoming ink into the stopper channel. The dynamic contact angle is also dependent on the volume of the incoming liquid front. Using model inks and cross-sectional microscopy, factors governing the pinning behavior can be systematically investigated.

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