SVPWM Technique with Varying DC-Link Voltage for Common Mode Voltage Reduction in a Matrix Converter and Analytical Estimation of its Output Voltage Distortion

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Dedication

To my parents and all those who believed in me and stood by me.

Abstract

Common Mode Voltage (CMV) in any power converter has been the major contributor to premature motor failures, bearing deterioration, shaft voltage build up and electromagnetic interference. Intelligent control methods like Space Vector Pulse Width Modulation (SVPWM) techniques provide immense potential and flexibility to reduce CMV, thereby targeting all the afore mentioned problems. Other solutions like passive filters, shielded cables and EMI filters add to the volume and cost metrics of the entire system. Smart SVPWM techniques therefore, come with a very important advantage of being an economical solution.

This thesis discusses a modified space vector technique applied to an Indirect Matrix Converter (IMC) which results in the reduction of common mode voltages and other advanced features. The conventional indirect space vector pulse-width modulation (SVPWM) method of controlling matrix converters involves the usage of two adjacent active vectors and one zero vector for both rectifying and inverting stages of the converter. By suitable selection of space vectors, the rectifying stage of the matrix converter can generate different levels of virtual DC-link voltage. This capability can be exploited for operation of the converter in different ranges of modulation indices for varying machine speeds. This results in lower common mode voltage and improves the harmonic spectrum of the output voltage, without increasing the number of switching transitions as compared to conventional modulation. To summarize it can be said that the responsibility of formulating output voltages with a particular magnitude and frequency has been transferred solely to the rectifying stage of the IMC.

Estimation of degree of distortion in the three phase output voltage is another facet discussed in this thesis. An understanding of the SVPWM technique and the switching sequence of the space vectors in detail gives the potential to estimate the RMS value of the switched output voltage of any converter. This conceivably aids the sizing and design of output passive filters. An analytical estimation method has been presented to achieve this purpose for am IMC. Knowledge of the fundamental component in output voltage can be utilized to calculate its Total Harmonic Distortion (THD).

The effectiveness of the proposed SVPWM algorithms and the analytical estimation technique is substantiated by simulations in MATLAB/Simulink and experiments on a laboratory prototype of the IMC. Proper comparison plots have been provided to contrast the performance of the proposed methods with the conventional SVPWM method. The behavior of output voltage distortion and CMV with variation in operating parameters like modulation index and output frequency has also been analyzed.

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Chapter 1

Introduction

1.1 The Indirect Matrix Converter Topology

Matrix converters (MC) [1] have been discussed over the past two decades as an all-silicon solution compared to the conventional back-to-back connected voltage source converters for industrial adjustable speed drives. They are a modern AC-AC power converter which can formulate sinusoidal voltages/currents of a particular magnitude and frequency. Its unique features like single stage power conversion, elimination of the bulky DC-link capacitor, high power density, open loop input power factor correction, regenerative capability, etc. give it an upper hand [2]. This can directly translate to improved life-time, reliability and compactness of the system. Matrix converters can be implemented via two different topologies [3]

- Direct Matrix Converter (DMC)
- Indirect Matrix Converter (IMC)

The IMC consists of two stages of operation. The first stage is the rectifier stage which consists of six bidirectional switches and the second stage is the inverter stage which consists of six unidirectional switches. The performance of the IMC is similar to the DMC in terms of output and input waveforms. But as proposed by [4], the IMC has lesser commutation problems as compared to the DMC.

Although the matrix converters offer many advantages, it has two major disadvantages. Its maximum voltage transfer ratio is limited to 0.866 and the converter is

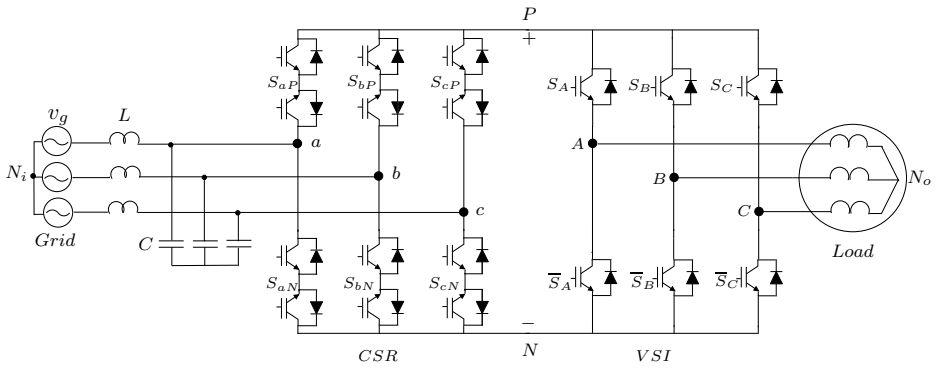


Figure 1.1: Indirect matrix converter (IMC) topology

unstable to momentary power source interruptions due to the absence of an intermediate power storage element. There have been many studies addressing these issues [5–7].

1.2 State of the Art

A major problem in these electric drives is the generation of switching common-mode voltages (CMV) at the machine terminals. Coupled with parasitic capacitances, this results in electromagnetic interference (EMI), shaft voltage buildup and high frequency bearing and ground currents which reduce the machines lifetime [8–10]. Common mode chokes and increased filter requirements can reduce the peak values of these common mode voltages. But this would translate to additional hardware components and would make the entire system bulkier and expensive. Few of these methods have been discussed in [11–13]. Therefore converter control strategies are explored to reduce the peak CMV. This eliminates the aforementioned disadvantages of volume and cost. A few model predictive control technique based strategies are discussed in [14–16]. Analysis and comparison of common mode voltage characteristics between a matrix converter and a Voltage Source Inverter (VSI) is presented in [17].

Space Vector Pulse Width Modulation is another very effective and flexible IMC control strategy. In this strategy, every vector of the rectifying stage formed by a current source rectifier (CSR) and the inverting stage formed by a voltage source inverter (VSI) corresponds to a particular switching state. An intelligent choice of these switching vectors can reduce the value of peak CMV. The control strategies of the CSR and the

VSI are independent in nature. A few advantages of this technique over other control techniques are

- Wide linear modulation range
- Greater flexibility to reduce switching losses or common mode voltage
- Improved Total Harmonic Distortion

Different SVM techniques to reduce CMV by controlling the VSI is discussed in [18], [19]. This is applied to an IMC while employing the conventional SVM on the CSR in [20, 21]. Their methods involve the usage of multiple active voltage vectors while eliminating the usage of zero vectors, but it translates to additional switching losses. Another method to eliminate the CMV in the DMC topology has been proposed by [22]. But this method comes with a disadvantage of limiting the voltage transfer ratio to 0.5. A method to appropriately choose zero vectors on the CSR to reduce the harmonic distortion in the output voltage is proposed in [23]. SVM techniques to reduce CMV in current source based drives is dealt with in [24, 25] . Extending the similar concept to the rectifying stage of an IMC, [21] and [26] suggest using different active current vectors on the CSR to generate two levels of virtual DC-link voltage. Adjustable output voltage of the IMC is synthesized by appropriate usage of zero vectors for the VSI control. This is particularly advantageous for operation of the IMC at lower modulation index range because the THD of output voltage is greatly reduced.

1.3 Contribution of the thesis

Making use of the CSR's capability to produce different levels of DC-link voltage, the proposed modulation strategies discussed in this thesis transfer control of generating the required output voltage to the rectifying stage entirely. The VSI is controlled to operate at the maximum modulation index, without usage of any zero vectors. There is another region of DC-link voltage for the higher modulation range of operation, which has not been addressed in literature as applied to an IMC. This is targeted in Method I where three adjacent active current vectors are used for forming the higher region of DC-link voltage. Usage of alternate active current vectors and an appropriate zero

vector produces the lower region of DC-link voltage and is the basis behind Method II. The choice of zero vectors in Method II is in accordance with [23], thereby improving its performance as compared to [26]. The proposed method results in reducing the peak CMV by 42.3% compared to conventional modulation. Apart from the improvement in peak values of CMV, the lower order harmonics (third) are also reduced in the proposed method. This reduction aids the design of common mode chokes according to the paper [27] by reducing its size and width. Added benefits are reduced distortion in the output voltage, reduction in the switching losses in the inverter stage and lower core losses in the rotating machine.

The thesis also presents an analytical estimation method to predict the amount of distortion in output voltage. The method is inspired from [28–31]. Knowledge of the SVPWM strategy implemented for the operation of the IMC, gives us the potential to exactly estimate the voltage levels and corresponding dwell times of the switched output voltage of the matrix converter. This information is sufficient to compute its RMS value. Its fundamental component and its THD can be subsequently evaluated.

The thesis is organized in the following manner -

- Chapter 1 provides an introduction.
- Chapter 2 describes the conventional Space Vector Modulation Technique implemented for the control of an Indirect Matrix Converter.
- Chapter 3 details the proposed Space Vector Modulation Technique for the control of an Indirect Matrix Converter. The technique is validated with simulation and hardware results.
- Chapter 4 proposes a procedure for the analytical estimation of distortion in output voltage.
- Chapter 5 discusses performance comparison of the proposed and conventional SVM techniques. It also substantiates the analytical estimation method.
- Chapter 6 presents the conclusion and the future work.

Chapter 2

Conventional Space Vector Modulation Technique

The IMC topology consists of a rectifying stage (CSR) and an inverting stage (VSI) as shown in Fig. 1.1. The CSR is controlled appropriately to produce a virtual DC-link voltage as well as to maintain sinusoidal input currents. Similarly, the function of the VSI is to generate balanced output three-phase voltages of desired magnitude and frequency. This fact translates to operation of the converter at different modulation indices. This can be achieved through control on the CSR and the VSI. The thesis focuses on a Pulse Width Modulation (PWM) technique called SVPWM. In SVPWM, for a sufficiently small time interval, the reference voltage or current vector can be formulated by the usage of stationary vectors. As the time instant changes a new set of stationary vectors may be used for formulating the reference. This time interval for a converter depends on its switching frequency.

The space vector X corresponding to any three phase quantities x_a, x_b and x_c can be expressed as (2.1). The two major aspects of this modulation strategy are selection of switching vectors and computation of corresponding time intervals. This section discusses these aspects for the conventional SVPWM method.

$$X = x_a + x_b e^{j2\pi/3} + x_c e^{j4\pi/3} \tag{2.1}$$

2.1 SVM OF Rectifying Stage

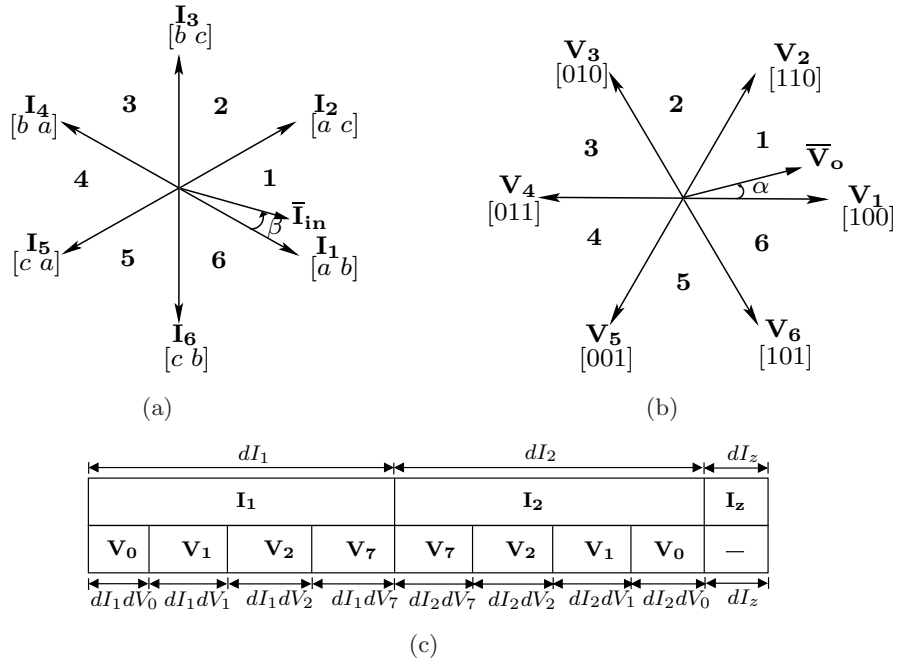


Figure 2.1: Conventional SVM: (a) Space vectors of CSR, (b) Space vectors of VSI and (c) Switching sequence

The space vector diagram of the rectifier stage comprises of six active current vectors (I_1-I_6) and three zero current vectors as shown in Fig. 2.1(a). Each vector represents a distinct state of the CSR. For every phase $x \epsilon a, b, c$, switches S_{xP} and S_{xN} can take values of 0 or 1. "$S_{xP} = 1$" or "$S_{xN} = 1$" implies that the input phase x is connected to the positive pole "P" or negative pole "N" of the DC-link respectively. Out of the three switches S_{aP},S_{bP} and S_{cP}, connected to "P", only one switch can be on at any instant. This applies to the corresponding three switches connected to "N". The purpose of the CSR is to ensure the formulation of three phase balanced input sinusoidal currents. According to the SVPWM method, the reference input current vector $\overline{\mathbf{I}}_{\mathbf{in}}$ is generated by the usage of two adjacent active vectors and one zero vector. The time instants for application of each vector is decided by its duty ratio. Duty ratio can be expressed as $= T/T_s$, where T_s is the sample time and T is the time for which a particular vector is applied. Table 2.1 maps the current space vectors with the state of switches, where 1

refers to the switch being ON and 0 refers to the switch being OFF.

Table 2.1: Switching States for the Rectifying Stage of IMC

Switching Function	I_{ab}	I_{ac}	I_{bc}	I_{ba}	I_{ca}	I_{cb}	I_{aa}	I_{bb}	I_{cc}
S_{aP}	1	1	0	0	0	0	1	0	0
S_{bP}	0	0	1	1	0	0	0	1	0
S_{cP}	0	0	0	0	1	1	0	0	1
S_{aN}	0	0	0	1	1	0	1	0	0
S_{bN}	1	0	0	0	0	1	0	1	0
S_{cN}	0	1	1	0	0	0	0	0	1

The duty ratios of current vectors I_1, I_2 and I_z are given by dI_1, dI_2 and dI_z respectively. We consider an instant of time when the reference vector, $\overline{\mathbf{I}}_{\mathbf{in}}$ lies in Sector 1, as seen in Fig. 2.1(a). Solutions to the above duty ratios given by (2.3) can be obtained by solving (2.2). Here m_I $(= I_{in}/I_{DC})$ is the modulation index of the CSR, β is angle between the first vector and reference vector, I_{in} is the peak input current to be synthesized and I_{DC} is the average DC-link current.

$$\begin{aligned} dI_1\overline{I}_1 + dI_2\overline{I}_2 + dI_z \times 0 &= \overline{I}_{in} \\ dI_1 + dI_2 + dI_z &= 1 \end{aligned} \tag{2.2}$$

$$\begin{aligned} dI_1 &= m_I \sin\left(\frac{\pi}{3} - \beta\right) \\ dI_2 &= m_I \sin\beta \\ dI_z &= 1 - dI_1 - dI_2 \end{aligned} \tag{2.3}$$

Usage of two adjacent active vectors and one zero vector to form the current reference results in the the DC-Link voltage as seen in Fig. 2.2. For example in Sector 1, the current reference is formed using the vectors I_{ab}, I_{ac} and an appropriate zero vector

resulting in voltage levels v_{ab}, v_{ac} and a zero voltage.

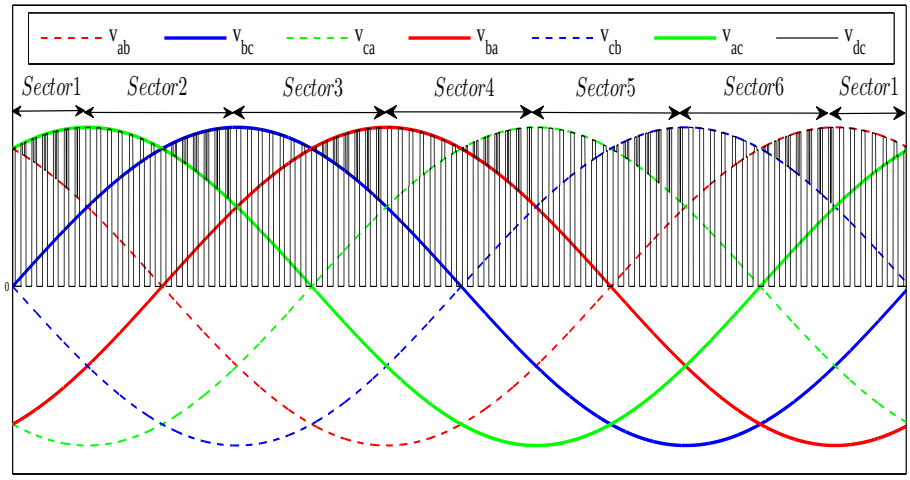


Figure 2.2: DC-Link voltage for Conventional SVPWM

2.2 SVM of Inverting Stage

The space vector diagram of the inverting stage comprises of six active voltage vectors (V_1-V_6) and two zero voltage vectors (V_0,V_7) as shown in Fig. 2.1(b). The switching function of this stage is defined as $S_y = 1(y = A, B, C)$ when the switch is ON or $S_y = 0$ when that switch is OFF. The corresponding switches on the lower leg have complimentary switching signals $\overline{S}_y$. The states of the switches corresponding to each vector is summarized in Table. 2.2. In this converter at any instant of time, only one switch in a leg can be switched on.

Table 2.2: Switching States for the Inverting Stage

Switching Function	V_1	V_2	V_3	V_4	V_5	V_6	V_0	V_7
S_A	1	1	0	0	0	1	0	1
S_B	0	1	1	1	0	0	0	1
S_C	0	0	0	1	1	1	0	1
$\overline{S}_A$	0	0	1	1	1	0	1	0
$\overline{S}_B$	1	0	0	0	1	1	1	0
$\overline{S}_C$	1	1	1	0	0	0	1	0

Like the CSR, in the VSI the reference output voltage vector is generated by using two adjacent active vectors and one zero vector. If the duty ratios for the voltage vectors V_1, V_2 and V_z are given by dV_1, dV_2 and dV_z, solutions to these duty rations given in (2.5) can be obtained by solving (2.4). Here m_V $(= V_o/V_{DC})$ is the modulation index of the VSI, α is angle between the first vector and reference vector, V_o is the peak output voltage to be synthesized and I_{DC} is the average DC-link voltage.

$$\begin{aligned} dV_1\overline{V}_1 + dV_2\overline{V}_2 + dV_z \times 0 &= \overline{V}_o \\ dV_1 + dV_2 + dV_z &= 1 \end{aligned} \tag{2.4}$$

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha \\ dV_z &= 1 - dV_1 - dV_2 \end{aligned} \tag{2.5}$$

In order to minimize the switching losses in the converter, the total number of switching transitions are minimized at the inverting and the rectifying stage of the converter. The switching sequence of the various voltage and current vectors is provided in Fig. 2.1(c). It can further be noticed that during the instant when the current vector transitions, a zero voltage vector is applied. This makes the rectifying stage of the

converter soft switched. In order to generate the pulses that control the operation of various switches in the IMC, the duty ratios are compared with a high frequency symmetrical triangular carrier with a upward ramp and a subsequent downward ramp. The switching frequency for various simulations and experimental results in this thesis is 5 kHz.

2.3 Common Mode Voltage Analysis for CSR and VSI

The common mode voltage (CMV) in an IMC can be defined as the voltage between the load neutral point N_o and the neutral of the input three phase power supply N_i. The expressions for individual CMV of the rectifier and inverter can be expressed as in (2.8) and (2.11) respectively. The switching states of the switches of the rectifying stage decides the DC-Link voltage waveform. Similarly appropriate modulation of the switches of the inverting stage generates the output three phase balanced voltage waveforms from the DC-Link voltage. It can therefore be concluded that the common mode voltage of the IMC depends on the switching states of the CSR, the VSI and the input instantaneous three phase voltages given by (2.6). At any instant of time the input voltages are balanced thereby resulting in equation (2.7)

$$\begin{aligned} v_a &= V_i \cos(\omega_i t) \\ v_b &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c &= V_i \cos\left(\omega_i t - \frac{4\pi}{3}\right) \end{aligned} \tag{2.6}$$

$$v_a + v_b + v_c = 0 \tag{2.7}$$

2.3.1 CMV for CSR

The CMV of a CSR is given by (2.8). Every current vector corresponds to a particular state of switches which there by translates to a particular value $V_{CM(CSR)}$. This can be deduced based on the switches that are ON and the instantaneous values of input

voltage v_a, v_b and v_c. Let us for example consider the current vector I_{ab}. The positive pole P of the DC-Link is connected to v_a through the switch upper switch of the a phase ($S_{aP} = 1$) while the negative pole N is connected to v_b through the lower switch of the b phase ($S_{bN} = 1$). Table. 2.3 summarizes the $V_{CM(CSR)}$ values corresponding to every current vector.

$$V_{CM(CSR)} = \frac{1}{2}\left(v_{PN_i} + v_{NN_i}\right) \tag{2.8}$$

for an active current vector I_{ab},

$$\begin{aligned} V_{CM(CSR)} &= \frac{1}{2}\left(v_a + v_b\right) \\ &= \frac{-v_c}{2}\left(from\,(2.7)\right) \end{aligned} \tag{2.9}$$

Similarly for a zero current vector I_{aa},

$$\begin{aligned} V_{CM(CSR)} &= \frac{1}{2}\left(v_a + v_a\right) \\ &= v_a \end{aligned} \tag{2.10}$$

2.3.2 CMV for VSI

The CMV of a VSI is given by (2.11). Like a CSR, the CMV of a VSI is dependent on its switching states and instantaneous DC-Link voltage v_{dc}. Let us for example consider the voltage vector V_1. The switching states corresponding to this vector are $(S_A, S_B, S_C) = (1, 0, 0)$. Therefore the output phase A, through the upper switch ($S_A = 1$) is connected to the positive pole P of the DC-Link while output phases B and C are connected to the negative pole N of the DC-Link through the corresponding bottom switches ($\overline{S}_B = 1$ and $\overline{S}_C = 1$). Thus, for I_{ab} the output phase voltages v_{AN}, v_{BN} and v_{CN} can be expressed as (2.14). The $V_{CM(VSI)}$ values corresponding to every voltage vector is summarized in Table. 2.4.

$$V_{CM(VSI)} = \frac{1}{3}\left(v_{AN} + v_{BN} + v_{CN}\right) \tag{2.11}$$

Table 2.3: Instantaneous CMV of the Rectifying Stage

Current Vector	Switches ON	$V_{CM(CSR)}$
I_{ab}	S_{aP}, S_{bN}	$-v_c/2$
I_{ac}	S_{aP}, S_{cN}	$-v_b/2$
I_{bc}	S_{bP}, S_{cN}	$-v_a/2$
I_{ba}	S_{bP}, S_{aN}	$-v_c/2$
I_{ca}	S_{cP}, S_{aN}	$-v_b/2$
I_{cb}	S_{cP}, S_{bN}	$-v_a/2$
I_{aa}	S_{aP}, S_{aN}	v_a
I_{bb}	S_{bP}, S_{bN}	v_b
I_{cc}	S_{cP}, S_{cN}	v_c

For active voltage vector V_1,

$$\begin{aligned} V_{AN} &= S_A \times v_{dc} = v_{dc} \\ V_{BN} &= S_B \times v_{dc} = 0 \\ V_{CN} &= S_C \times v_{dc} = 0 \end{aligned} \tag{2.12}$$

the corresponding $V_{CM(VSI)}$ can be expressed as,

$$\begin{aligned} V_{CM(VSI)} &= \frac{1}{3}\left(S_A v_{dc} + S_B v_{dc} + S_C v_{dc}\right) \\ &= \frac{1}{3}\left(v_{dc} + 0 + 0\right) \\ &= \frac{1}{3}\left(v_{dc}\right) \end{aligned} \tag{2.13}$$

Similarly for a zero voltage vector V_7,

$$\begin{aligned} V_{AN} &= S_A \times v_{dc} = v_{dc} \\ V_{BN} &= S_B \times v_{dc} = v_{dc} \\ V_{CN} &= S_C \times v_{dc} = v_{dc} \end{aligned} \tag{2.14}$$

the corresponding $V_{CM(VSI)}$ can be expressed as,

$$\begin{aligned} V_{CM(VSI)} &= \frac{1}{3}\left(S_A v_{dc} + S_B v_{dc} + S_C v_{dc}\right) \\ &= \frac{1}{3}\left(v_{dc} + v_{dc} + v_{dc}\right) \\ &= v_{dc} \end{aligned} \tag{2.15}$$

Table 2.4: Instantaneous CMV of the Inverting Stage

Voltage Vector	S_A, S_B, S_C	$V_{CM(VSI)}$
V_1	$1, 0, 0$	$v_{dc}/3$
V_2	$1, 1, 0$	$2v_{dc}/3$
V_3	$0, 1, 0$	$v_{dc}/3$
V_4	$0, 1, 1$	$2v_{dc}/3$
V_5	$0, 0, 1$	$v_{dc}/3$
V_6	$1, 0, 1$	$2v_{dc}/3$
V_0	$0, 0, 0$	0
V_7	$1, 1, 1$	v_{dc}

This conventional SVPWM method thereby results in the proper control on the IMC in any modulation index range ($0 < m < 0.866$), to generate voltage with variable frequency and magnitude. Fig. 2.3 summarizes the different waveforms in an IMC. The output voltage of the IMC is switched with a fundamental sinusoidal component. The modulation technique achieves the purpose of formulating this of a particular magnitude

and frequency. The DC-Link voltage is used to synthesize the output phase voltages. Output currents are balanced and sinusoidal in nature. The bottom most waveform is the net CMV of the IMC, whose peak values lie between V_i and $-V_i$.

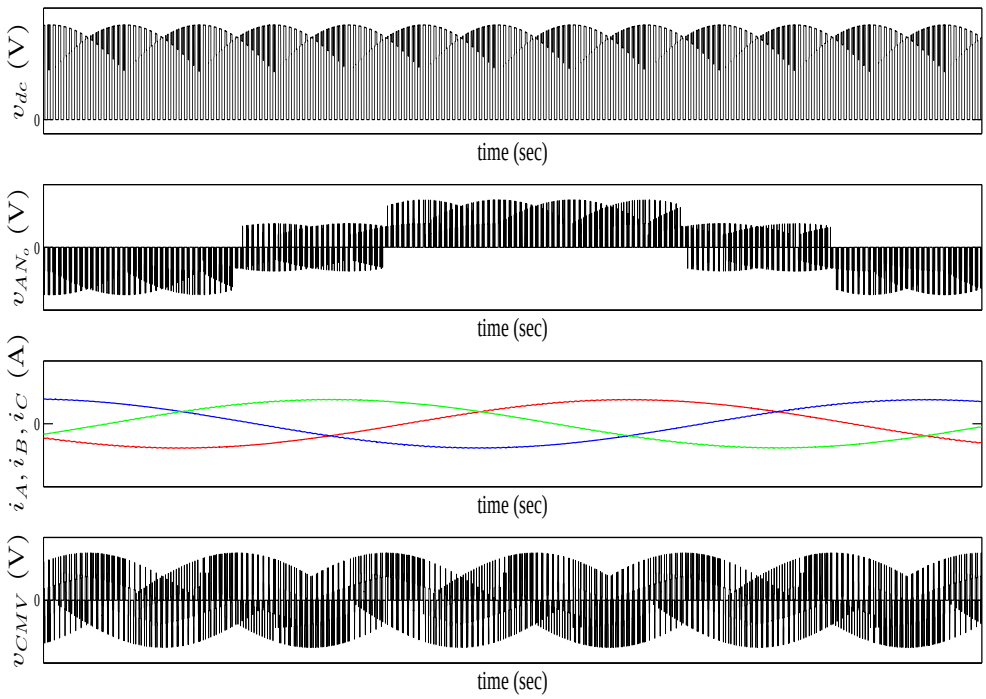


Figure 2.3: From top to bottom - DC-Link voltage, Output voltage referenced to load neutral, Output currents and CMV

Chapter 3

Proposed Space Vector Modulation Technique

The main motive of the proposed SVPWM method is to target the ill effects of CMV and output voltage distortion. The basic concept of this method lies in the simple fact that both CMV and output voltage distortion are dependent upon switching states and switching sequence of the switches in an IMC and SVPWM offers immense flexibility and potential to reduce them. An intelligent choice of switching states, which translates back to a smart choice of current or voltage space vectors can improve the harmonic profile of output voltage and reduce peak values of CMV. This section describes in detail the novel space vector modulation (SVM) technique and the corresponding switching sequence. The technique is substantiated through simulation and hardware results.

The solution which this thesis offers to the above mentioned problems requires us to study the operation of the IMC in two ranges of operation -

- High Modulation Index Range (HMIR)
- Low Modulation Index Range (LMIR)

Two different and independent strategies of SVPWM targets each of these ranges of operation. Both these methods transfer control of generating appropriate output voltages to the CSR. The usage of zero vectors in the VSI for the generation of balanced three phase output voltages as discussed in the previous chapter results in a higher peak

value of CMV. In order to eliminate the application of zero vectors the duty ratios of the active voltage vectors can be normalized to get dV_1' and dV_2' as per (3.1), where dV_1 and dV_2 are obtained from (2.5). This is a good assumption to make because the contribution of zero vectors to the formation of output voltage is very less when the inverting stage is operated at its full modulation index. For computational simplicity, elimination of zero vectors can be achieved by another method where the duty ratios of the active vectors are given by (3.2).

$$\begin{aligned} dV_1' &= \frac{dV_1}{dV_1 + dV_2} \\ dV_2' &= \frac{dV_2}{dV_1 + dV_2} \end{aligned} \tag{3.1}$$

$$\begin{aligned} dV_1' &= dV_1 \\ dV_2' &= 1 - dV_1 \end{aligned} \tag{3.2}$$

Any variation in modulation of the rectifying stage affects the DC-Link voltage waveform. For instance, elimination of zero current vectors in the modulation of the CSR removes all instances of zero voltage on the DC-Link. The proposed method targets the usage of different combinations of active vectors in the rectifying stage thereby making use of the different levels of average virtual DC-link voltage. The inverting stage of the IMC generates three phase balanced output voltages from the DC-Link voltage. Therefore, the harmonic spectrum of the output voltages is a reflection of the nature of DC-link voltage. This capability of the CSR is utilized for operation of the IMC in different ranges of modulation index.

3.1 Method I for HMIR

The Method I discusses the operation of the IMC at the higher modulation index range which is defined by $0.577 < m < 0.866$, where m $(= 1.5 m_I m_V)$ is the total modulation index of the IMC. In this range of operation of the converter, the zero current vectors of the CSR have lesser contribution than the active current vectors towards the generation of the required fundamental component of input current. Therefore, the proposed method of modulation eliminates the usage of zero current vectors and uses only active current vectors. Unlike the conventional SVPWM which uses two active vectors, the proposed method makes use of three active current vectors for generating the reference input current.

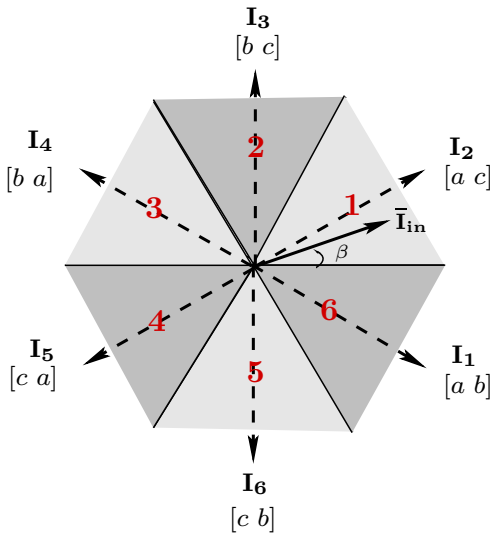


Figure 3.1: Modified space vectors of CSR in proposed SVM technique

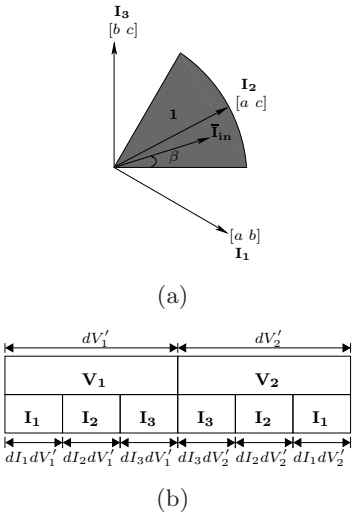


Figure 3.2: Proposed SVM: (a) Formation of reference in Sector 1, (b) Switching Sequence

For operation of the IMC in HMIR, the reference current vector $\overline{\mathbf{I}}_{\mathbf{in}}$ follows the modified space vector diagram of Fig. 3.4. Here the position of sectors is shifted by an angle of $\frac{\pi}{6}$ as compared to the conventional space vector of 2.1(a). For generality, let us assume $\overline{\mathbf{I}}_{\mathbf{in}}$ lies in Sector 1 as represented by the shaded portion of 3.2(a). Three nearest active vectors I_1, I_2 and I_3 are used to generate this current reference whose

dwell times, dI_1, dI_2 and dI_3 are obtained by solving (3.3). The solutions are provided by equation (3.4).

$$\begin{aligned} dI_1\overline{I}_1 + dI_2\overline{I}_2 + dI_3\overline{I}_3 &= \overline{I}_{in} \\ dI_1 + dI_2 + dI_3 &= 1 \end{aligned} \tag{3.3}$$

$$\begin{aligned} dI_1 &= 1 - m_I \sin\left(\frac{\pi}{6} + \beta\right) \\ dI_2 &= \sqrt{3} m_I \sin\left(\frac{\pi}{3} + \beta\right) - 1 \\ dI_3 &= 1 - m_I \cos\beta \end{aligned} \tag{3.4}$$

where β is the angle of $\overline{\mathbf{I}}_{\mathbf{in}}$ with respect to the leading edge of the sector and m_I is the modulation index of the CSR which lies between $0.666 < m_I < 1$. This range is defined in order to ensure that the duty cycles in 3.4 stay positive.

Usage of three adjacent active vectors for formation of the current reference results in three voltage levels at the DC-Link. For example in sector 1, vectors used are I_{ab}, I_{ac} and I_{bc} which translates to the DC-Link voltage having three levels of v_{ab}, v_{ac} and v_{bc} respectively. The DC-Link voltage for this method is as shown in Fig. 3.3.

Overall, by studying the optimized switching sequence of the space vectors as shown in Fig. 3.2(b), the duty cycles for the current vectors are obtained by multiplying dV_1' and dV_2' with dI_1, dI_2 and dI_3 respectively. Table 3.1 summarizes the current vectors used corresponding to each sector of the space vector diagram of Fig 3.4 while Fig. 3.7 summarizes the various waveforms in the IMC using the modulation strategy proposed in Method I.

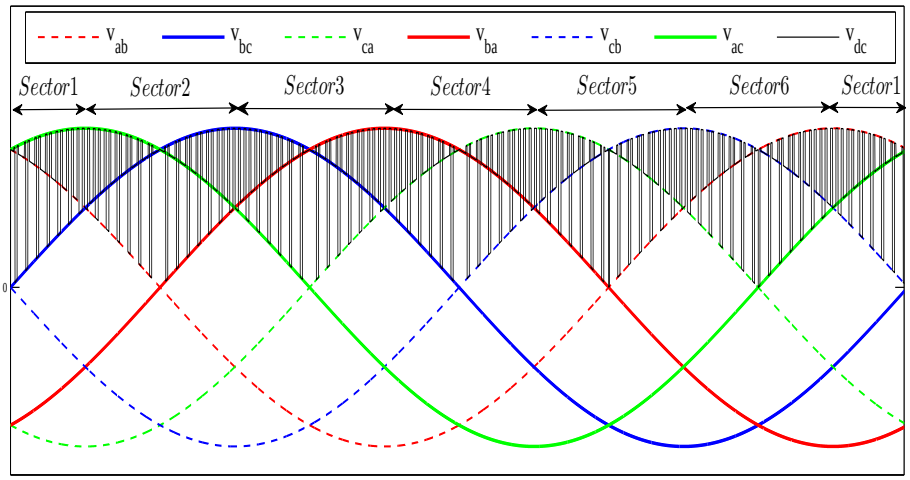


Figure 3.3: DC-Link voltage for Proposed Method I for HMIR

Table 3.1: Method I - Summary of current vectors for corresponding sectors

Sector	$\omega_i t$	Vectors applied
1	0 - $\frac{\pi}{3}$	I_{ab},I_{ac},I_{bc}
2	$\frac{\pi}{3}$ - $\frac{2\pi}{3}$	I_{ac},I_{bc},I_{ba}
3	$\frac{2\pi}{3}$ - π	I_{bc},I_{ba},I_{ca}
4	π - $\frac{4\pi}{3}$	I_{ba},I_{ca},I_{cb}
5	$\frac{4\pi}{3}$ - $\frac{5\pi}{3}$	I_{ca},I_{cb},I_{ab}
6	$\frac{5\pi}{3}$ - 2π	I_{cb},I_{ab},I_{ac}

3.2 Method II for LMIR

Method II discusses the operation of the IMC at the lower modulation index range which is defined by $0 < m < 0.5$. For this range of operation, two alternate active vectors along with an appropriate zero vector are used for formation of the reference input current. Unlike Method I, it is obvious that there is a significant contribution of zero current vectors towards the formation of the fundamental sinusoidal input current in LMIR and hence its usage cannot be eliminated. It effectively allows us to access further lower values of modulation indices. The proper choice of the zero current vector is very critical to reducing the peak value of CMV in this method. The three available zero vectors I_{aa}, I_{bb} and I_{cc} correspond to $V_{CM(CSR)}$ values of v_a, v_b and v_c respectively. The zero vector chosen should correspond to the phase with the least instantaneous value of input grid voltage. This is accordance with the concept proposed in [23]. Table. summarizes the current vectors used for each sector of the space vector diagram of Fig. 3.4.

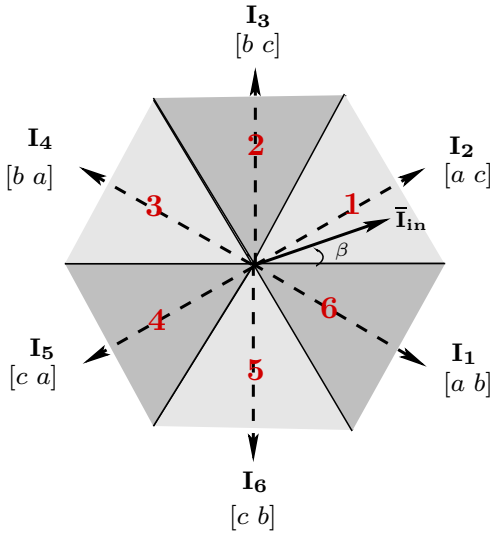


Figure 3.4: Modified space vectors of CSR in proposed SVM technique

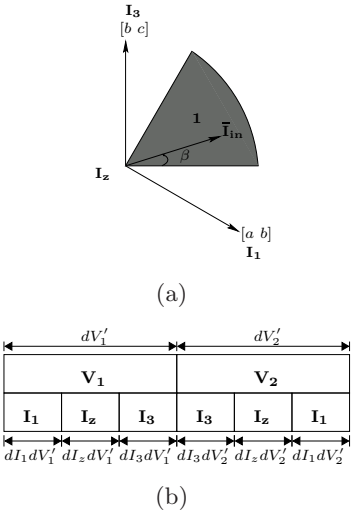


Figure 3.5: Proposed SVM: (a) Formation of reference in Sector 1, (b) Switching Sequence

The space vector diagram for operation of the IMC in LMIR is similar to the one

proposed in Method I. Here, for generating a reference current $\overline{I}_{in}$ in Sector 1 as represented by the shaded portion of Fig. 3.5(a), two alternate active vectors I_1 and I_3 and a zero vector I_z are used. The duty cycles dI_1, dI_3 and dI_z corresponding to these vectors are obtained by solving the set of equations given by (3.5). The solutions are consecutively provided in (3.4).

$$\begin{aligned} dI_1\overline{I}_1 + dI_3\overline{I}_3 + dI_z \times 0 &= \overline{I}_{in} \\ dI_1 + dI_3 + dI_z &= 1 \end{aligned} \tag{3.5}$$

$$\begin{aligned} dI_1 &= m_I \cos\beta \\ dI_3 &= m_I \sin\left(\frac{\pi}{6} + \beta\right) \\ dI_z &= 1 - dI_1 - dI_3 \end{aligned} \tag{3.6}$$

where β follows the same definition as Method I. Here m_I, the modulation index of the CSR lies between $0.666 < m_I < 1$. This range is defined in order to ensure that the duty cycles in 3.6 stay positive.

This method makes use of two alternate active vectors and an appropriate zero vector for the formation of the current reference in the LMIR. For example in sector 1, active vectors used are I_{ab} and I_{bc} resulting in two voltage levels of v_{ab} and v_{bc} in thr DC-Link voltage respectively as shown in Fig. 3.6.

The optimized switching sequence of the space vectors for reducing the number of switching transitions is demonstrated in Fig. 3.5(b). Overall, the duty cycle of the current vectors can be obtained in a similar manner as proposed in Method I. It should be noted that for operation of the IMC in the range $0.5 < m < 0.577$, the method described in [23] can be used. Table. 3.2 summarizes the current vectors to be used in each sector which Fig. 3.8 summarizes the waveforms obtained by implementation of poposed Method II to control an IMC.

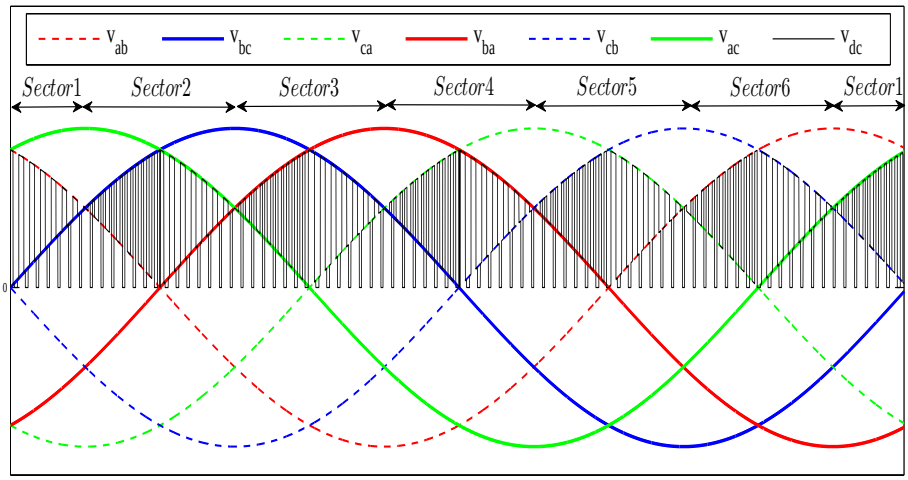


Figure 3.6: DC-link voltage for Proposed Method II for LMIR

Table 3.2: Method II - Summary of current vectors for corresponding sectors

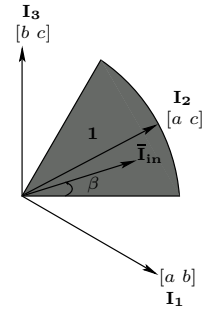
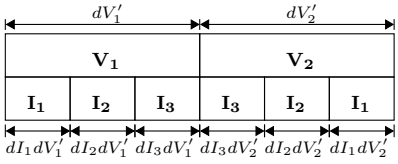
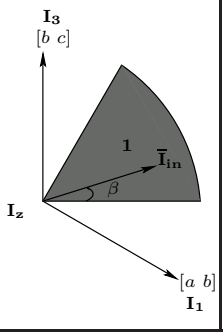
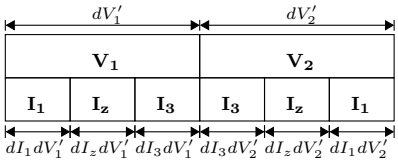
Sector	$\omega_i t$	Active Vectors	Zero Vector
1	0 - $\frac{\pi}{3}$	I_{ab},I_{bc}	I_{bb}
2	$\frac{\pi}{3}$ - $\frac{2\pi}{3}$	I_{ac},I_{ba}	I_{aa}
3	$\frac{2\pi}{3}$ - π	I_{bc},I_{ca}	I_{cc}
4	π - $\frac{4\pi}{3}$	I_{ba},I_{cb}	I_{bb}
5	$\frac{4\pi}{3}$ - $\frac{5\pi}{3}$	I_{ca},I_{ab}	I_{aa}
6	$\frac{5\pi}{3}$ - 2π	I_{cb},I_{ac}	I_{cc}

3.3 Summary

Fig. 3.7 and Fig. 3.8 summarizes the various waveforms obtained through simulations of an IMC model designed in MATLAB/Simulink for Method I and Method II respectively. We notice that the shape of DC-Link voltages obtained in both are different from the conventional DC-Link voltage. The shape of the output switched phase voltages is in correspondence with the shape of the DC-Link voltage. Three phase sinusoidal balanced currents are formulated by both the proposed modulation techniques. It can be noticed that the peak of CMV of the IMC has been reduced to lie between $\frac{V_i}{\sqrt{3}}$ and $-\frac{V_i}{\sqrt{3}}$.

The basic concept of the two proposed methods - Method I and II has been summarized in Table. 3.3. This involves a condensed portrayal of modulation index range of operation, Vector diagrams and the switching sequence of the vectors for both the methods. In order to maintain generality it is assumed that the current reference at a particular instant lies in Sector 1.

Table 3.3: Summary of proposed SVM Techniques

Method	m Index Range	Vector Diagram	Switching Sequence
I	$0.577 < m < 0.866$		
II	$0 < m < 0.5$		

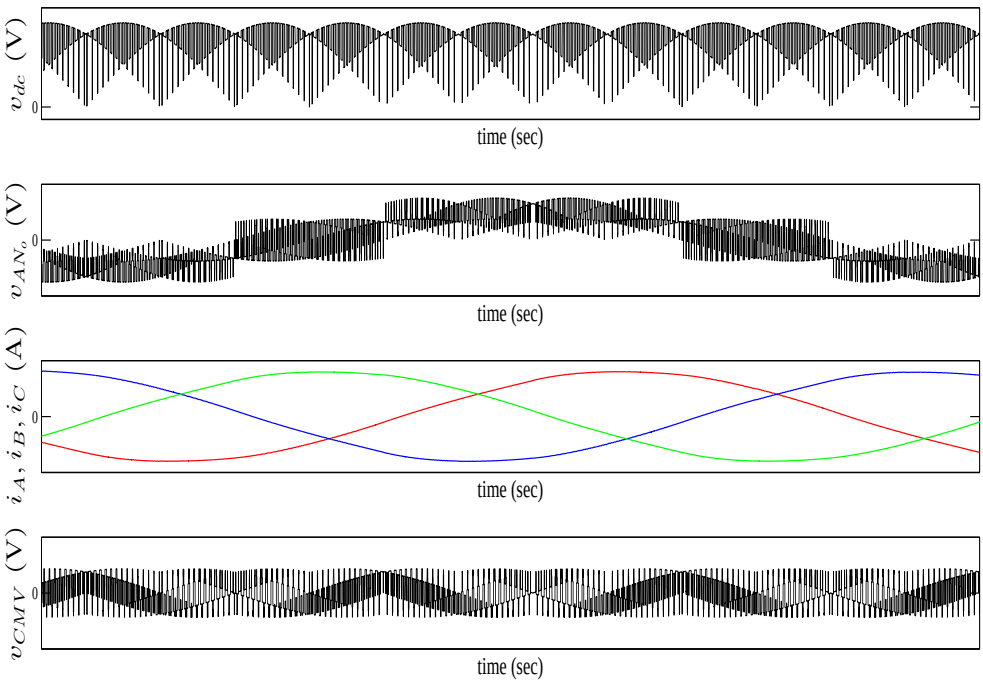


Figure 3.7: From top to bottom - DC-link voltage, Output voltage referenced to load neutral, Output currents and CMV

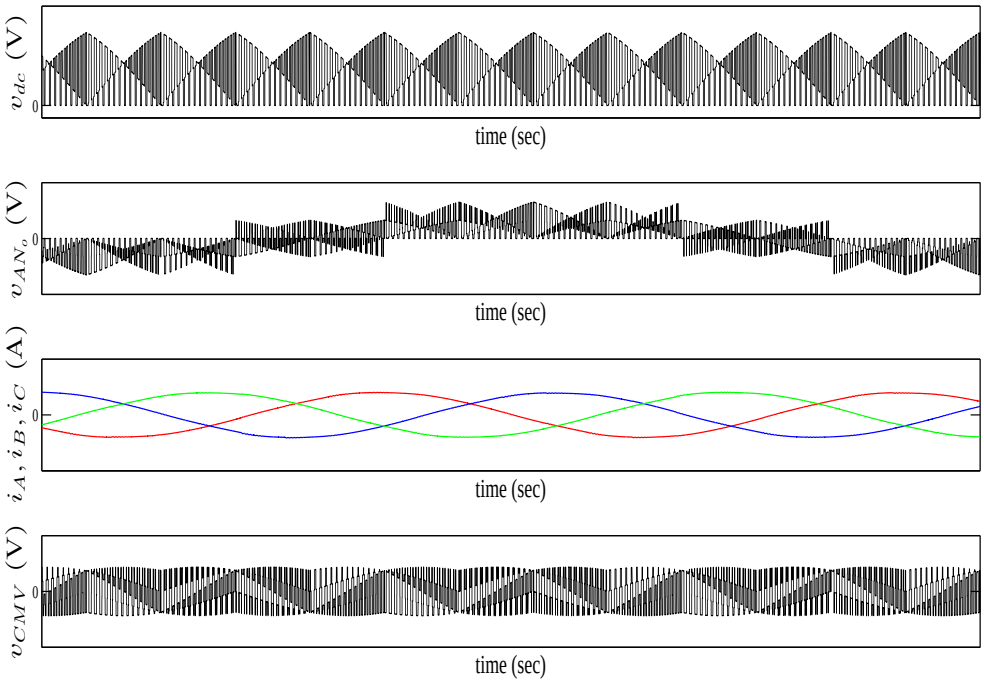


Figure 3.8: From top to bottom - DC-link voltage, Output voltage referenced to load neutral, Output currents and CMV

Chapter 4

Analytical Estimation of Output Voltage Distortion

Knowledge of the exact SVPWM strategy implemented on the rectifying and inverting stage of an IMC gives us the potential to accurately estimate the different levels of the three phase output voltage $v_{AN_\circ}$, referred to the neutral of the output load. The main motivation behind the estimation of the content of distortion in output voltage lies in the design on EMI filters for motor loads.

The output voltage $v_{AN_\circ}$ can be expressed in terms of the instantaneous output phase voltages referred to the negative pole N of the DC-Link as given by the equation (4.1). Moreover v_{AN}, v_{BN} and v_{CN} can be further written in terms of their respective switching functions (S_A, S_B and S_C) and the instantaneous value of DC-Link voltgae v_{dc} as per the equation (4.2). The following section describes a step-by-step process to analytically determine the content of distortion in v_{AN_o} for conventional SVPWM and proposed SVPWM techniques - Method I and Method II. The derivation of expressions for the above methods is executed by taking into consideration an input current reference I_{in} and an output voltage reference V_o both in Sector 1 of their respective space vector diagrams. For a start two assumptions are made,

- Output frequency f_o is equal to the grid frequency.
- I_{in} and V_o are aligned along the leading edge of a sector.

In Chapter 4., it will be shown that the estimation process holds true for 1) f_o values other than the grid frequency 2) f_o equal to the grid frequency but with dissimilar alignment of I_{in} and V_o.

$$v_{AN_\circ} = \frac{1}{3}(2v_{AN} - v_{BN} - v_{CN}) \tag{4.1}$$

$$= \frac{1}{3}(2S_A v_{dc} - S_B v_{dc} - S_C v_{dc}) \tag{4.2}$$

4.1 Analysis for Conventional SVPWM

According to the Conventional SVPWM method discussed in Chapter 2., for references lying in Sector 1, I_{in} is generated using active current vectors I_1 and I_2 while V_{in} is generated using active voltage vectors V_1 and V_2. The zero vectors are not taken into consideration in this estimation process. This is because the application of zero current vectors results in $v_{dc} = 0$ while application of zero voltage vectors results in $v_{AN_O} = 0$. They therefore have no contribution to output voltage distortion.

Table 4.1: Voltage Levels in V_{AN_o} and v_{dc} for Conventional SVPWM

Sector	I_1	I_2	Levels in v_{dc}		dV_1	dV_2	Levels in v_{AN_o}			
(CSR,VSI)			dI_1	dI_2			dI_1dV_1	dI_1dV_2	dI_2dV_2	dI_2dV_1
(1,1)	I_{ab}	I_{ac}	v_{ab}	v_{ac}	$V_{[100]}$	$V_{[110]}$	$\frac{2}{3}v_{ab}$	$\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{ac}$	$\frac{2}{3}v_{ac}$
(2,2)	I_{ac}	I_{bc}	v_{ac}	v_{bc}	$V_{[110]}$	$V_{[010]}$	$\frac{1}{3}v_{ac}$	$-\frac{1}{3}v_{ac}$	$-\frac{1}{3}v_{bc}$	$\frac{1}{3}v_{bc}$
(3,3)	I_{bc}	I_{ba}	v_{bc}	v_{ba}	$V_{[010]}$	$V_{[011]}$	$-\frac{1}{3}v_{bc}$	$-\frac{2}{3}v_{bc}$	$-\frac{2}{3}v_{ba}$	$-\frac{1}{3}v_{ba}$
(4,4)	I_{ba}	I_{ca}	v_{ba}	v_{ca}	$V_{[011]}$	$V_{[001]}$	$-\frac{2}{3}v_{ba}$	$-\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{ca}$	$-\frac{2}{3}v_{ca}$
(5,5)	I_{ca}	I_{cb}	v_{ca}	v_{cb}	$V_{[001]}$	$V_{[101]}$	$-\frac{1}{3}v_{ca}$	$\frac{1}{3}v_{ca}$	$\frac{1}{3}v_{cb}$	$-\frac{1}{3}v_{cb}$
(6,6)	I_{cb}	I_{ab}	v_{cb}	v_{ab}	$V_{[101]}$	$V_{[100]}$	$\frac{1}{3}v_{cb}$	$\frac{2}{3}v_{cb}$	$\frac{2}{3}v_{ab}$	$\frac{1}{3}v_{ab}$

Application of I_1 and I_2 in Sector 1 of the rectifying stage corresponds to switching states $[a, b]$ and $[a, c]$ respectively. Apart from the zero voltage level due to the zero current vector, this results in two instantaneous voltage levels of v_{dc}, v_{ab} and v_{ac} for dwell times, dI_1 and dI_2 respectively. Shifting focus to the inverting stage, application of V_1 and V_2 corresponding to switching states $[1, 0, 0]$ and $[1, 1, 0]$ in Sector 1 results in four instantaneous voltage levels of V_{AN_o}, $\frac{2}{3}v_{ab}$, $\frac{1}{3}v_{ab}$, $\frac{1}{3}v_{ac}$ and $\frac{2}{3}v_{ac}$ with dwell times of dI_1dV_1, dI_1dV_2, dI_2dV_2 and dI_2dV_1 respectively. This is in accordance with the switching sequence of space vectors as shown in Fig. ??. The voltage levels of V_{AN_o} are obtained using equations (4.1) and (4.2). Table. 4.1 summarizes the v_{dc} and v_{AN_o} levels for different sectors of the CSR and VSI.

The RMS square of output voltage of the inverting stage of the IMC ($=v_{AN_o}$) over one sampling cycle in the first sector is computed by the equation given in (4.3). This concept is extended and the RMS square expressions of v_{AN_o} in a sampling cycle are obtained for the second sector in (4.4) and third sector in (4.5). The equations (4.3),(4.4) and (4.5) repeats for the remaining three sectors. The RMS square of the inverting stage's output voltage over one sector can be found by (4.6) where ω_o is the output frequency of the IMC. Taking into consideration the contribution from each sector, the net RMS square of v_{AN_o} over a fundamental cycle is found from (4.7) as a function of modulation indices m_I and m_V in (4.8). We further notice that this expression is independent of grid frequency and output frequency, thereby validating the assumptions made at the beginning of this chapter. The RMS square of the switching frequency component which can be translated to distortion in output voltage is given by (4.9) where fundamental component of output voltage, V_o is expressed in terms of fundamental component of grid voltage V_i as $\frac{3}{2}m_I m_V V_i$.

$$
\begin{aligned}
v^2_{AN_o,S-1}(rms) &= dI_1dV_1\left(\frac{2}{3}v_{ab}\right)^2 + dI_1dV_2\left(\frac{1}{3}v_{ab}\right)^2 + dI_2dV_2\left(\frac{1}{3}v_{ac}\right)^2 \\
&\quad + dI_2dV_1\left(\frac{2}{3}v_{ac}\right)^2 \qquad (4.3)\\
v^2_{AN_o,S-2}(rms) &= dI_1dV_1\left(\frac{1}{3}v_{ac}\right)^2 + dI_1dV_2\left(-\frac{1}{3}v_{ac}\right)^2 + dI_2dV_2\left(-\frac{1}{3}v_{bc}\right)^2 \\
&\quad + dI_2dV_1\left(\frac{1}{3}v_{bc}\right)^2 \qquad (4.4)\\
v^2_{AN_o,S-3}(rms) &= dI_1dV_1\left(-\frac{1}{3}v_{bc}\right)^2 + dI_1dV_2\left(-\frac{2}{3}v_{bc}\right)^2 + dI_2dV_2\left(-\frac{2}{3}v_{ba}\right)^2 \\
&\quad + dI_2dV_1\left(-\frac{1}{3}v_{ba}\right)^2 \qquad (4.5)
\end{aligned}
$$

$$
v^2_{AN_o,i}(rms) = \frac{1}{3}\int_{SECTOR_i} v^2_{AN_o,S-i}(rms)\, d\left(\omega_o t\right), i = 1,2,3 \qquad (4.6)
$$

$$
v^2_{AN_o}(rms) = \frac{1}{3}\sum_{i=1,2,3} v^2_{AN_o,i}(rms) \qquad (4.7)
$$

$$
v^2_{AN_o}(rms) = \frac{m_I m_V V_i^2\left(2\pi + 3\sqrt{3}\right)}{4\pi} \qquad (4.8)
$$

$$
v^2_{AN_o sw}(rms) = \frac{m_I m_V V_i^2\left(2\pi + 3\sqrt{3}\right)}{4\pi} - V_o^2(rms) \qquad (4.9)
$$

4.2 Analysis for Proposed Method I

According to the modulation strategy for Method I, a current reference I_{in} in Sector 1 of Fig. 3.4 is obtained by using three active current vectors I_1, I_2 and I_3 while a reference voltage V_o is obtained using two active voltage vectors V_1 and V_2. For the first sector, I_1, I_2 and I_3 in the rectifying stage of the IMC correspond to switching states of $[a,b]$, $[a,c]$ and $[b,c]$. Application of these vectors results in three different voltage levels at the DC-Link, which correspond to v_{ab}, v_{ac} and v_{bc} with dwell times of dI_1, dI_2 and dI_3 respectively. This DC-Link voltage is used by the inverting stage to formulate

three phase balanced output voltages. In this stage vectors V_1 and V_2 correspond to switching states $[1,0,0]$ and $[1,1,0]$. Using equations (4.1) and (4.2), we can accurately predict that here V_{AN_o} will have six different instantaneous voltage levels, $\frac{2}{3}v_{ab}$, $\frac{2}{3}v_{ac}$, $\frac{2}{3}v_{bc}$, $\frac{1}{3}v_{bc}$, $\frac{1}{3}v_{ac}$ and $\frac{1}{3}v_{ab}$ with dwell times of dI_1dV_1', dI_2dV_1', dI_3dV_1', dI_3dV_2', dI_2dV_2' and dI_1dV_2'. This is in accordance with the switching sequence in Fig. 3.2(b). Table. 4.2 summarizes the voltage levels in v_{dc} and v_{AN_o} for different sectors of the CSR and VSI.

Table 4.2: Voltage Levels in V_{AN_o} and v_{dc} for Proposed Method I

Sector	Levels in v_{dc}			Levels in v_{AN_o}					
(CSR,VSI)	dI_1	dI_2	dI_3	dI_1dV_1'	dI_2dV_1'	dI_3dV_1'	dI_3dV_2'	dI_2dV_2'	dI_1dV_2'
(1,1)	v_{ab}	v_{ac}	v_{bc}	$\frac{2}{3}v_{ab}$	$\frac{2}{3}v_{ac}$	$\frac{2}{3}v_{bc}$	$\frac{1}{3}v_{bc}$	$\frac{1}{3}v_{ac}$	$\frac{1}{3}v_{ab}$
(2,2)	v_{ac}	v_{bc}	v_{ba}	$\frac{1}{3}v_{ac}$	$\frac{1}{3}v_{bc}$	$\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{bc}$	$-\frac{1}{3}v_{ac}$
(3,3)	v_{bc}	v_{ba}	v_{ca}	$-\frac{1}{3}v_{bc}$	$-\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{ca}$	$-\frac{2}{3}v_{ca}$	$-\frac{2}{3}v_{ba}$	$-\frac{2}{3}v_{bc}$
(4,4)	v_{ba}	v_{ca}	v_{cb}	$-\frac{2}{3}v_{ba}$	$-\frac{2}{3}v_{ca}$	$-\frac{2}{3}v_{cb}$	$-\frac{1}{3}v_{cb}$	$-\frac{1}{3}v_{ca}$	$-\frac{1}{3}v_{ba}$
(5,5)	v_{ca}	v_{cb}	v_{ab}	$-\frac{1}{3}v_{ca}$	$-\frac{1}{3}v_{cb}$	$-\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{cb}$	$\frac{1}{3}v_{ca}$
(6,6)	v_{cb}	v_{ab}	v_{ac}	$\frac{1}{3}v_{cb}$	$\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{ac}$	$\frac{2}{3}v_{ac}$	$\frac{2}{3}v_{ab}$	$\frac{2}{3}v_{cb}$

The RMS square of the output voltage ($= v_{AN_o}$) for this method is obtained in a similar manner as discussed previously. Expressions for v_{AN_o} over a sampling cycle in sector 1, 2 and 3 of the inverting stage are provided by equations (4.10), (4.11)

and (4.12) respectively. These expressions repeat for the remaining three sectors. The final expression of the RMS square value of v_{AN_o} over a fundamental cycle, in terms of modulation indices if provided by (4.13). We do notice here that this expression is not only independent of grid frequency and ouput frequency but is also independent of m_V. This is because the inverting stage of the IMC is operated at its full modulation index. The distortion in v_{AN_o} is given in (4.14), where the definition of V_o remains the same.

$$\begin{aligned} v^2_{AN_o,S-1}\,(rms) &= dI_1dV_1'\left(\frac{2}{3}v_{ab}\right)^2 + dI_2dV_1'\left(\frac{2}{3}v_{ac}\right)^2 + dI_3dV_1'\left(\frac{2}{3}v_{bc}\right)^2 \\ &\quad + dI_3dV_2'\left(\frac{1}{3}v_{bc}\right)^2 + dI_2dV_2'\left(\frac{1}{3}v_{ac}\right)^2 + dI_1dV_2'\left(\frac{1}{3}v_{ab}\right)^2 \end{aligned} \tag{4.10}$$

$$\begin{aligned} v^2_{AN_o,S-2}\,(rms) &= dI_1dV_1'\left(\frac{1}{3}v_{ac}\right)^2 + dI_2dV_1'\left(\frac{1}{3}v_{bc}\right)^2 + dI_3dV_1'\left(\frac{1}{3}v_{ba}\right)^2 \\ &\quad + dI_3dV_2'\left(-\frac{1}{3}v_{ba}\right)^2 + dI_2dV_2'\left(-\frac{1}{3}v_{bc}\right)^2 \\ &\quad + dI_1dV_2'\left(-\frac{1}{3}v_{ac}\right)^2 \end{aligned} \tag{4.11}$$

$$\begin{aligned} v^2_{AN_o,S-3}\,(rms) &= dI_1dV_1'\left(-\frac{1}{3}v_{bc}\right)^2 + dI_2dV_1'\left(-\frac{1}{3}v_{ba}\right)^2 + dI_3dV_1'\left(-\frac{1}{3}v_{ca}\right)^2 \\ &\quad + dI_3dV_2'\left(-\frac{2}{3}v_{ca}\right)^2 + dI_2dV_2'\left(-\frac{2}{3}v_{ba}\right)^2 \\ &\quad + dI_2dV_2'\left(-\frac{2}{3}v_{bc}\right)^2 \end{aligned} \tag{4.12}$$

$$v^2_{AN_o}(rms) = \frac{V_i^2\left(\pi + 4\sqrt{3}m_I - 3\sqrt{3}\right)}{3\pi} \tag{4.13}$$

$$v^2_{AN_osw}(rms) = \frac{V_i^2\left(\pi + 4\sqrt{3}m_I - 3\sqrt{3}\right)}{3\pi} - V_o^2(rms) \tag{4.14}$$

4.3 Analysis for Proposed Method II

The previous chapter talks about this method in detail. This method targets the operation of the IMC at the lower modulation indices. A current reference I_{in} is formed by active current vectors I_1 and I_3 and an appropriate zero vector I_z. In sector 1 of Fig. 3.4, I_1,I_3 and I_z correspond to switching states of $[a, b]$, $[b, c]$ and $[b, b]$ respectively. The DC-Link voltage therefore has two voltage levels of v_{ab} and v_{bc}. The zero vector is neglected in this estimation process for the same reasons as cited in the conventional method. The inverting stage of the IMC follows the same set of voltage vectors and dwell times as discussed in the previous section. Equations (4.1) and (4.2) are used as a reference to predict four different voltage levels of V_{AN_o}. In accordance with the switching sequence in Fig. 3.5(b) these levels are $\frac{2}{3}v_{ab}$, $\frac{2}{3}v_{bc}$, $\frac{1}{3}v_{bc}$ and $\frac{1}{3}v_{ab}$ with dwell times of dI_1dV_1', dI_3dV_1', dI_3dV_2' and dI_1dV_2'. Table. 4.3 summarizes the different voltage levels in v_{dc} and v_{AN_o} for different sectors of the CSR and VSI.

The process of deriving the expression of RMS square of output voltage is similar to the one described in the previous section. v_{AN_o} over a sampling cycle in sector 1,2 and 3 of the inverting stage can be written as (4.15), (4.15) and (4.15) respectively. The final expression, independent of m_V, grid frequency and output frequency for the RMS square of v_{AN_o} is given by (4.18) while the distortion in it is given by (4.19).

$$\begin{aligned} v^2_{AN_o,S-1}(rms) &= dI_1dV_1'\left(\frac{2}{3}v_{ab}\right)^2 + dI_3dV_1'\left(\frac{2}{3}v_{bc}\right)^2 + dI_3dV_2'\left(\frac{1}{3}v_{bc}\right)^2 \\ &\quad + dI_1dV_2'\left(\frac{1}{3}v_{ab}\right)^2 \qquad (4.15) \\ v^2_{AN_o,S-2}(rms) &= dI_1dV_1'\left(\frac{1}{3}v_{ac}\right)^2 + dI_3dV_1'\left(\frac{1}{3}v_{ba}\right)^2 + dI_3dV_2'\left(-\frac{1}{3}v_{ba}\right)^2 \\ &\quad + dI_1dV_2'\left(-\frac{1}{3}v_{ac}\right)^2 \qquad (4.16) \\ v^2_{AN_o,S-3}(rms) &= dI_1dV_1'\left(-\frac{1}{3}v_{bc}\right)^2 + dI_3dV_1'\left(-\frac{1}{3}v_{ca}\right)^2 + dI_3dV_2'\left(-\frac{2}{3}v_{ca}\right)^2 \\ &\quad + dI_1dV_2'\left(-\frac{2}{3}v_{bc}\right)^2 \qquad (4.17) \end{aligned}$$

Table 4.3: Voltage Levels in V_{AN_o} and v_{dc} for Proposed Method II

Sector	Levels in v_{dc}		Levels in v_{AN_o}			
(CSR,VSI)	dI_1	dI_2	dI_1dV_1'	dI_3dV_1'	dI_3dV_2'	dI_1dV_2'
(1,1)	v_{ab}	v_{bc}	$\frac{2}{3}v_{ab}$	$\frac{2}{3}v_{bc}$	$\frac{1}{3}v_{bc}$	$\frac{1}{3}v_{ab}$
(2,2)	v_{ac}	v_{ba}	$\frac{1}{3}v_{ac}$	$\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{ba}$	$-\frac{1}{3}v_{ac}$
(3,3)	v_{bc}	v_{ca}	$-\frac{1}{3}v_{bc}$	$-\frac{1}{3}v_{ca}$	$-\frac{2}{3}v_{ca}$	$-\frac{2}{3}v_{bc}$
(4,4)	v_{ba}	v_{cb}	$-\frac{2}{3}v_{ba}$	$-\frac{2}{3}v_{cb}$	$-\frac{1}{3}v_{cb}$	$-\frac{1}{3}v_{ba}$
(5,5)	v_{ca}	v_{ab}	$-\frac{1}{3}v_{ca}$	$-\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{ab}$	$\frac{1}{3}v_{ca}$
(6,6)	v_{cb}	v_{ac}	$\frac{1}{3}v_{cb}$	$\frac{1}{3}v_{ac}$	$\frac{2}{3}v_{ac}$	$\frac{2}{3}v_{cb}$

$$v_{AN_o}^2(rms) = \frac{2\sqrt{3}m_I V_i^2}{3\pi} \tag{4.18}$$

$$v_{AN_osw}^2(rms) = \frac{2\sqrt{3}m_I V_i^2}{3\pi} - V_o^2(rms) \tag{4.19}$$

4.4 Summary

To conclude, the analytical expressions of output voltage of the IMC referred to the load neutral N_o, for the conventional method and proposed methods, I and II are summarized in Table. 4.4. It can be seen that none of these expressions depend on grid frequency

(ω_i) or output frequency (ω_o). Moreover, it can also be noticed that the expressions for Method I and Method II are independent of m_V unlike the conventional method. This is because for both the proposed method, the inverting stage of the IMC is operated at its full modulation index and the entire control of generating variable frequency and variable magnitude output voltage is transferred to the rectifying stage.

Table 4.4: Analytical Expressions for different SVPWM Methods

SVPWM Method	Analytical Expressions for $v^2_{AN_o}(rms)$
Conventional	$\frac{m_I m_V V_i^2 \left(2\pi + 3\sqrt{3}\right)}{4\pi}$
Proposed Method I	$\frac{V_i^2 \left(\pi + 4\sqrt{3} m_I - 3\sqrt{3}\right)}{3\pi}$
Proposed Method II	$\frac{2\sqrt{3} m_I V_i^2}{3\pi}$

Chapter 5

Results and Performance Analysis

This chapter presents the results in the form of various waveforms obtained through model-based simulation and on a laboratory prototype of the IMC. Proposed methods I and II are validated by operation of the IMC at two different points - 1) in HMIR and 2) in LMIR. The proposed analytical estimation method of output voltage distortion is also substantiated with appropriate results. The different sections to follow are -

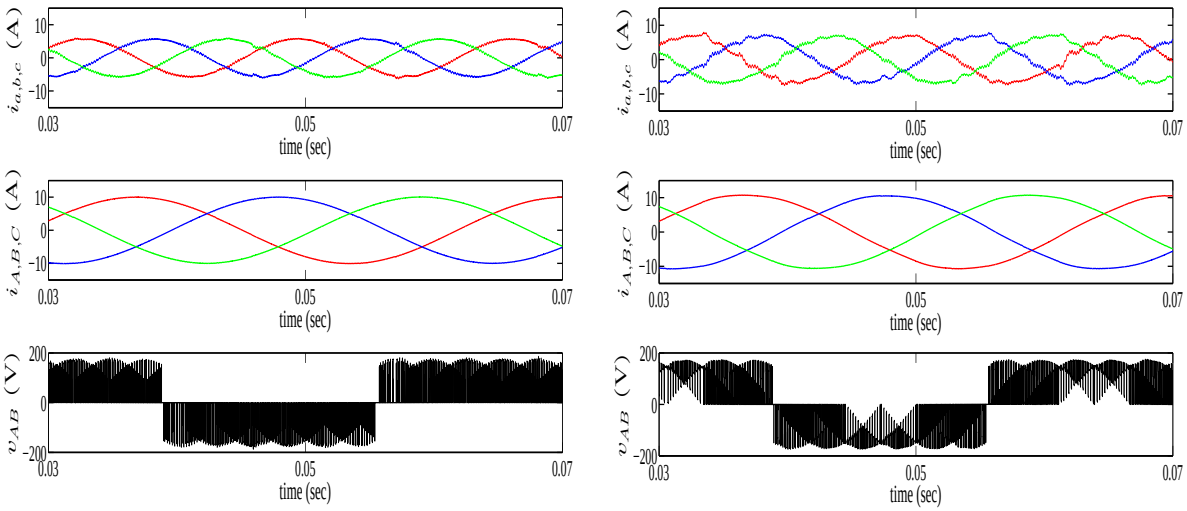
- Simulation Results
- Experimental Results
- Comparison and Performance Analysis

5.1 Simulation Results

The proposed SVPWM techniques discussed in Chapter. 3 are validated through simulations performed on an IMC, modeled in MATLAB/Simulink. For the purpose of proper comparison, the conventional SVPWM technique, discussed in Chapter. 2 is also simulated on the same model. The model is simulated using ideal switches for the IMC with supply grid at $120V_{LL_{RMS}}$ and a switching frequency of $5kHz$. The output frequency is maintained at 30 Hz and the load is $R = 5.4\ \Omega$ and $L = 22\ mH$ per phase. This section

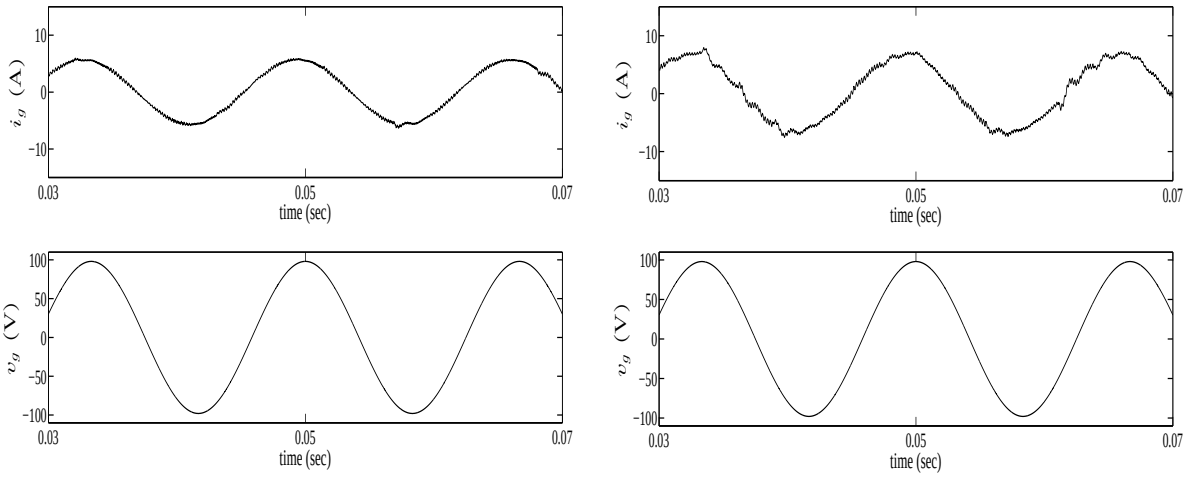
presents the simulation results of various waveforms during the operation of the IMC at $m = 0.7$ (HMIR) and $m = 0.4$ (LMIR). Results for conventional and proposed methods are displayed alongside each other for easy comparison. All figures on the left hand side of this section correspond to operation of the IMC using the conventional SVPWM method. Similarly figures on the right hand side correspond to operation of the IMC employing the proposed SVPWM methods. These set of waveforms are substantiated by experimental results discussed in the next section.

Fig. 5.1 and Fig. 5.5 ensures that both grid currents and output currents are balanced and sinusoidal in nature for conventional and proposed SVPWM methods. The quality of grid currents can be improved by proper design of an input filter, which is beyond the scope of this thesis work. A single phase grid current and corresponding phase voltage of the IMC are presented in Fig. 5.3 and Fig. 5.7. We observe that for both modulation methods at both the points of operation, the grid grid voltage and current are nearly in phase with the each other, thereby maintaining unity power factor. The DC-link voltage, output line-neutral voltage and CMV are presented in Fig. 5.2 and Fig. 5.6. It can be inferred from Fig. 5.3(b) that the higher region of DC-Link voltage is utilized in Method I, for formulation of balanced output voltages at $m = 0.7$. A similar conclusion can be drawn from Fig. 5.7(b) where the lower region of DC-Link is utilized to meet the same purpose at $m = 0.4$. Utilization of this capability of the rectifying stage to formulate different DC-Link voltage levels is the primary concept behind the proposed SVPWM methods. The shape of the output line-neutral voltages follows the shape of the corresponding DC-Link voltage. This results in an improved harmonic spectrum of output voltages. Both the proposed methods of modulation, also come with another major advantage of reducing the peak value of CMV by a factor of $\sqrt{3}$ in comparison to the conventional method. The harmonic spectrum of output switched voltage and CMV is presented in Fig. 5.4and Fig. 5.8. There is an obvious improvement in the harmonic spectrum of CMV for the proposed methods. The reduction in the magnitude of third harmonic content results in a decrease in the RMS values of CMV - 18.25% in Method I and 34.6% in Method II. Even though there is not an obvious improvement in the harmonic spectrum of output voltage, the improved impacts can be judged from comparison curves of Fig. 5.16(a) and Fig. 5.16(b).



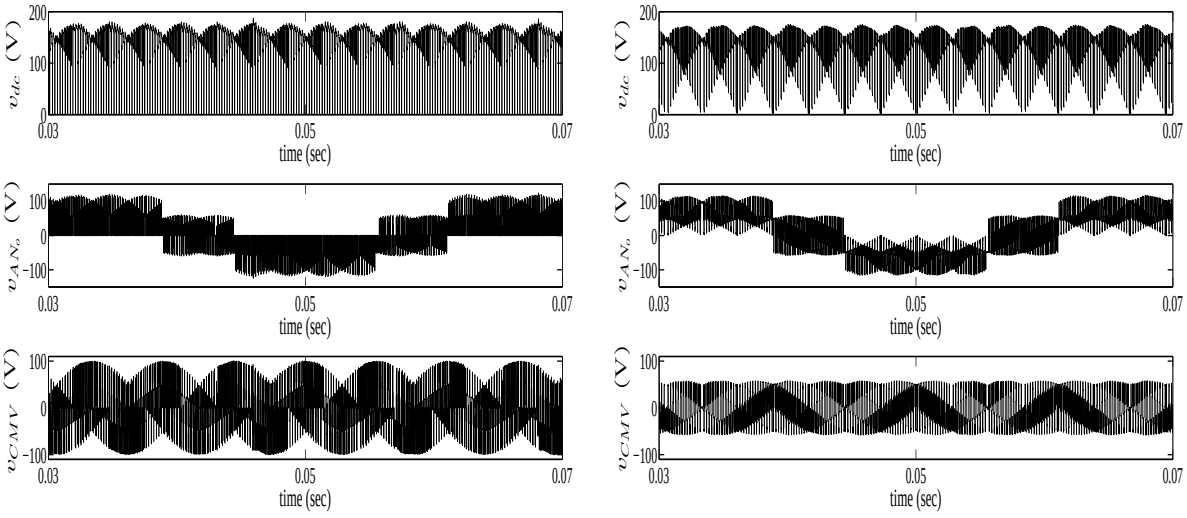
(a) (b)

Figure 5.1: Simulation Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - Grid currents, Output currents and Output line-line voltage



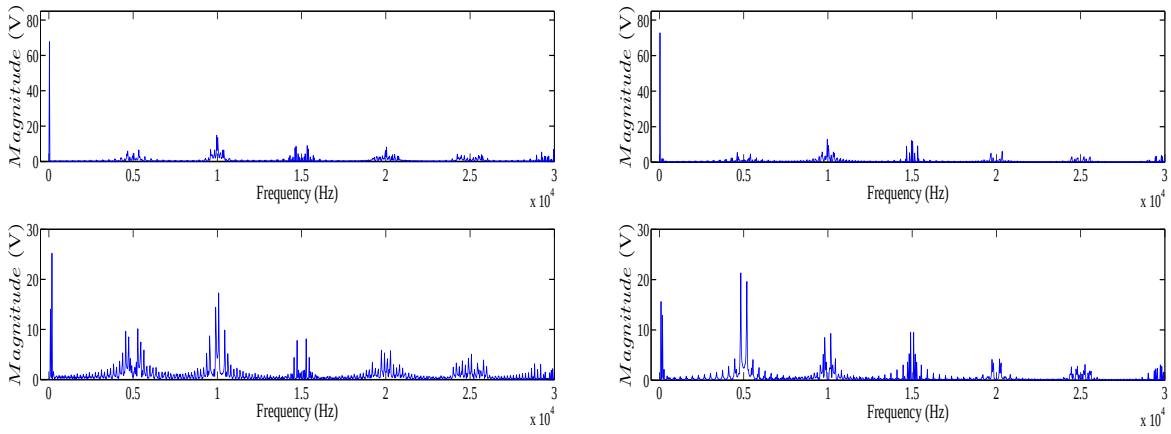
(a) (b)

Figure 5.2: Simulation Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - Grid current and Grid voltage



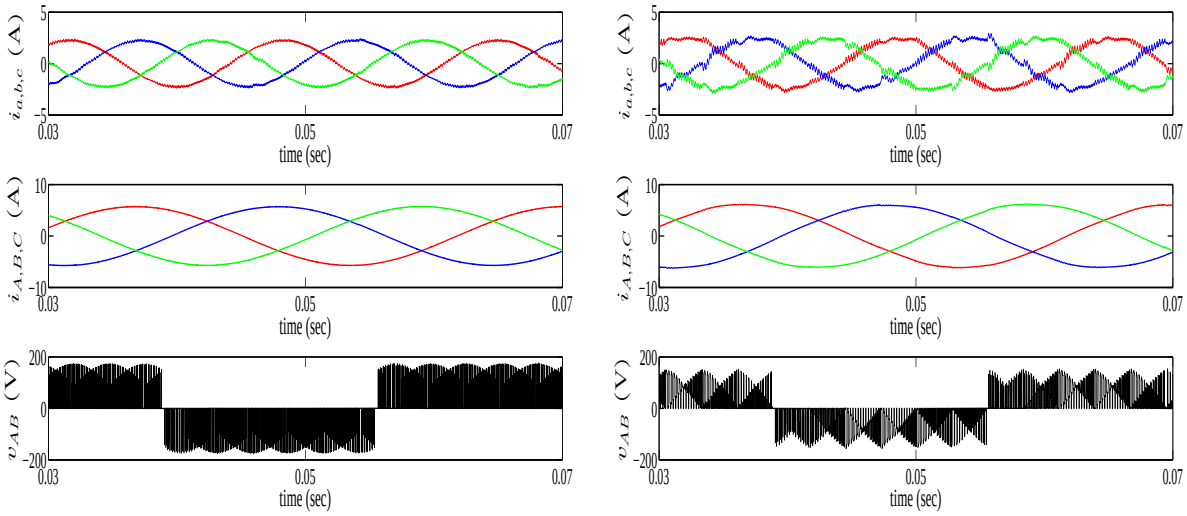
(a) (b)

Figure 5.3: Simulation Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - DC-Link voltage, Output line-neutral voltage and CMV



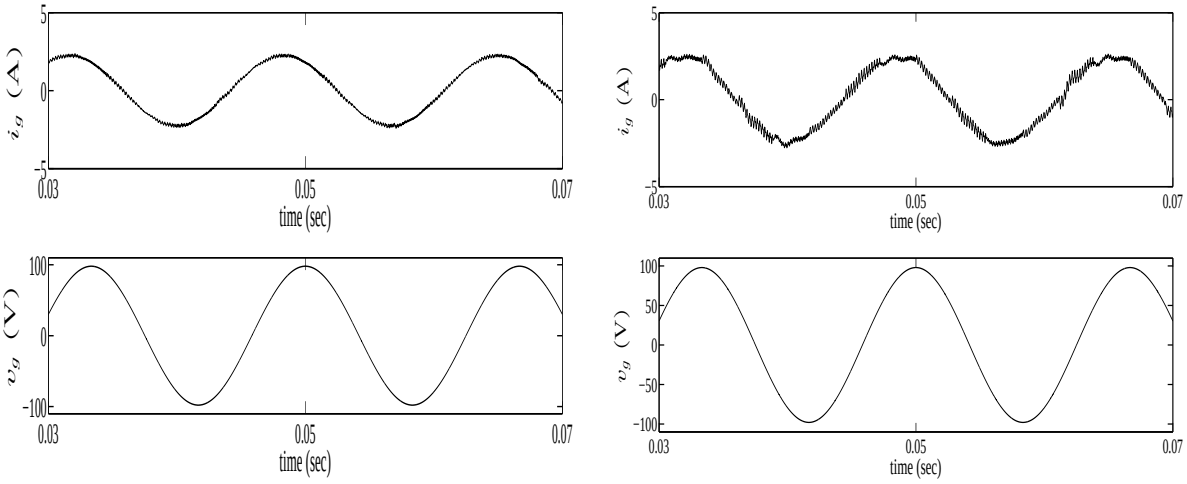
(a) (b)

Figure 5.4: Simulation Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - FFT of Output line-neutral voltage and FFT of CMV



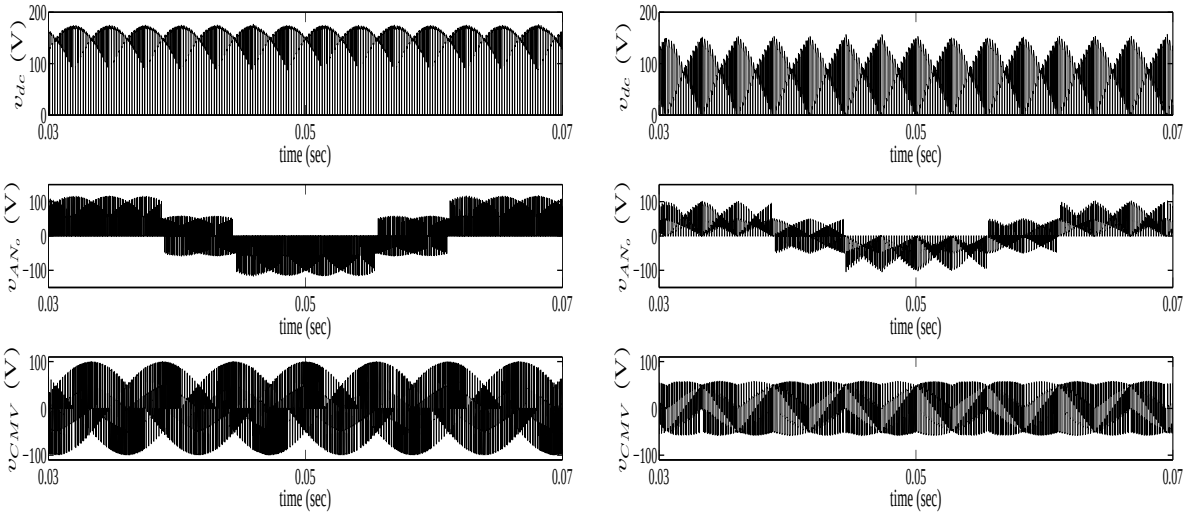
(a) (b)

Figure 5.5: Simulation Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - Grid currents, Output currents and Output line-line voltage



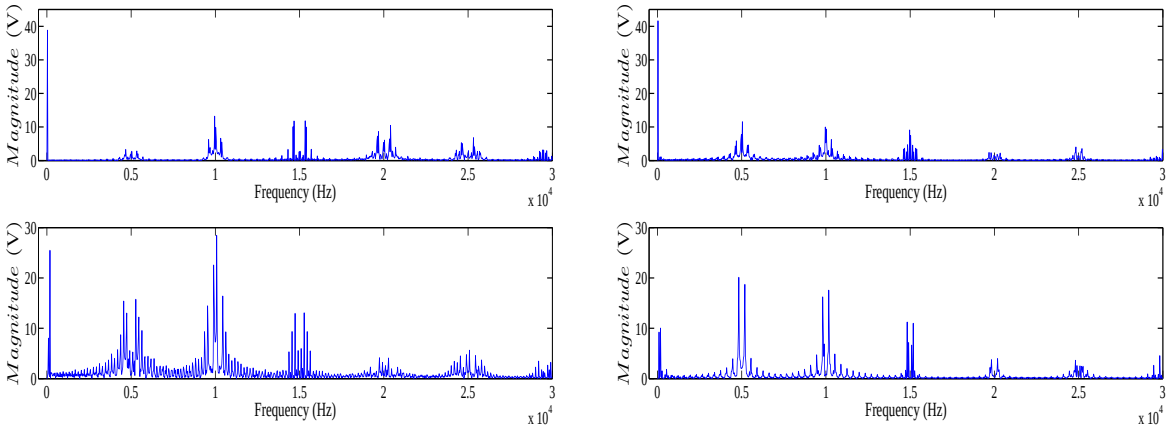
(a) (b)

Figure 5.6: Simulation Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - Grid current and Grid Voltage



(a) (b)

Figure 5.7: Simulation Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - DC-Link voltage, Output line-neutral voltage and CMV



(a) (b)

Figure 5.8: Simulation Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - FFT of Output line-neutral voltage and FFT of CMV

5.2 Experimental Results

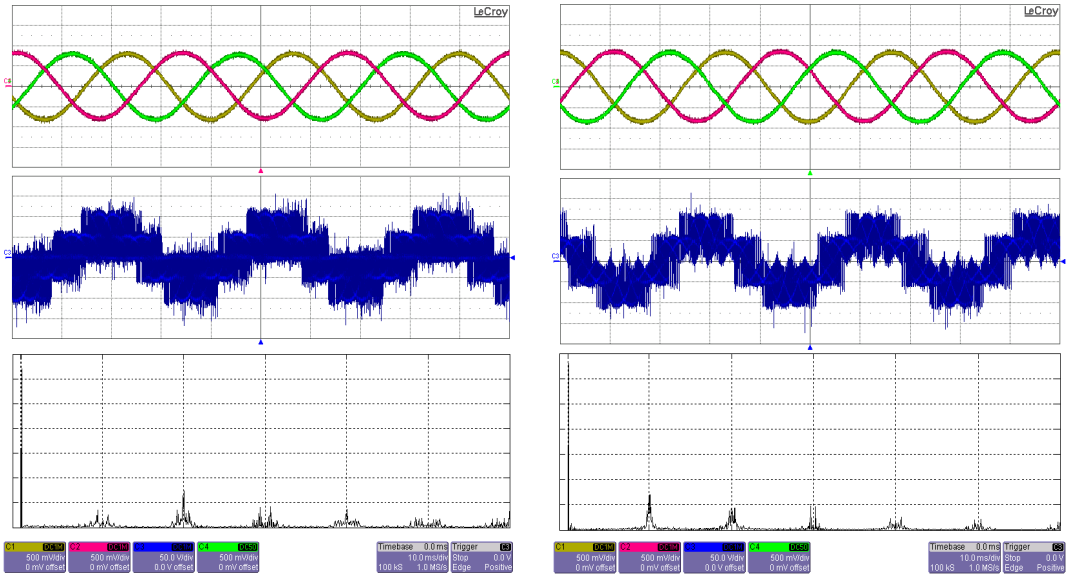
This segment discusses the experimental results for proposed modulation methods I at $m = 0.7$ and II at $m = 0.4$ that are obtained on a scaled down laboratory prototype of the IMC as shown in Fig. 5.15. The corresponding results for operation of the IMC using the conventional method is also discussed for the purpose of performance comparison. Integrated power IGBT module APTGF90TA60PG from Microsemi and gate driver 6SD106EI from CONCEPT are used. Control signals for SVM are generated from a FPGA (Xilinx XC3S500E). The experiments are run with a grid voltage of $120V_{LL_{RMS}}$ with a modulation index of $m = 0.7$ for Method I and $m = 0.4$ for Method II at a switching frequency of $5kHz$. Output at $30Hz$ is generated across a balanced three phase load of $R = 5.4\ \Omega$ and $L = 22\ mH$ per phase. An appropriate input filter was used to ensure unity power factor at the grid.

Fig. 5.9 for $m = 0.7$ and Fig. 5.12 for $m = 0.4$ presents the three phase output currents, output line-neutral voltage and FFT of output line to neutral voltage for conventional and proposed SVPWM methods. It can be observed that even though the magnitude of output current is the same, the shape of the output line to neutral voltage waveform is different. The RMS values of output voltage are as follows

- At $m = 0.7$ - $60V$ for Conventional SVPWM in Fig. 5.9(a) and $56.7V$ for Proposed Method I in Fig. 5.9(b).
- At $m = 0.4$ - $47.4V$ for Conventional SVPWM in Fig. 5.12(a) and $39.6V$ for Proposed Method II in Fig. 5.12(b).

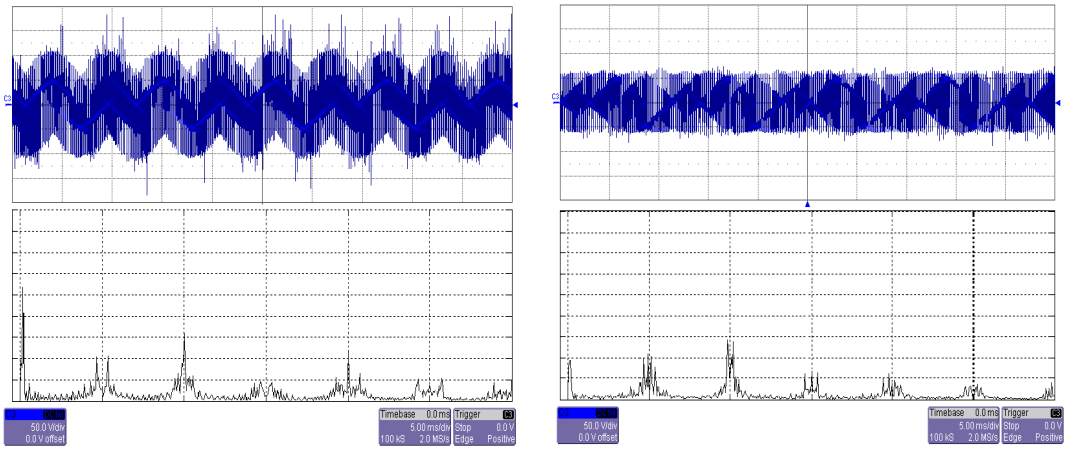
Similarly Fig. 5.10for $m = 0.7$ and Fig. 5.12 for $m = 0.4$ presents the CMV for conventional and proposed SVPWM methods. The peak of the CMV in both the proposed methods has been reduced by a factor of $\sqrt{3}$ in comparison to the conventional method. The FFT of the CMV shows that the third harmonic component's ($=180Hz$) peak value has been reduced by 64.5% in Method I and by 62.4% in Method II. The RMS values of CMV are as follows

- At $m = 0.7$ - $50.2V$ for Conventional SVPWM in Fig. 5.10(a) and $37.7V$ for Proposed Method I in Fig. 5.10(b).



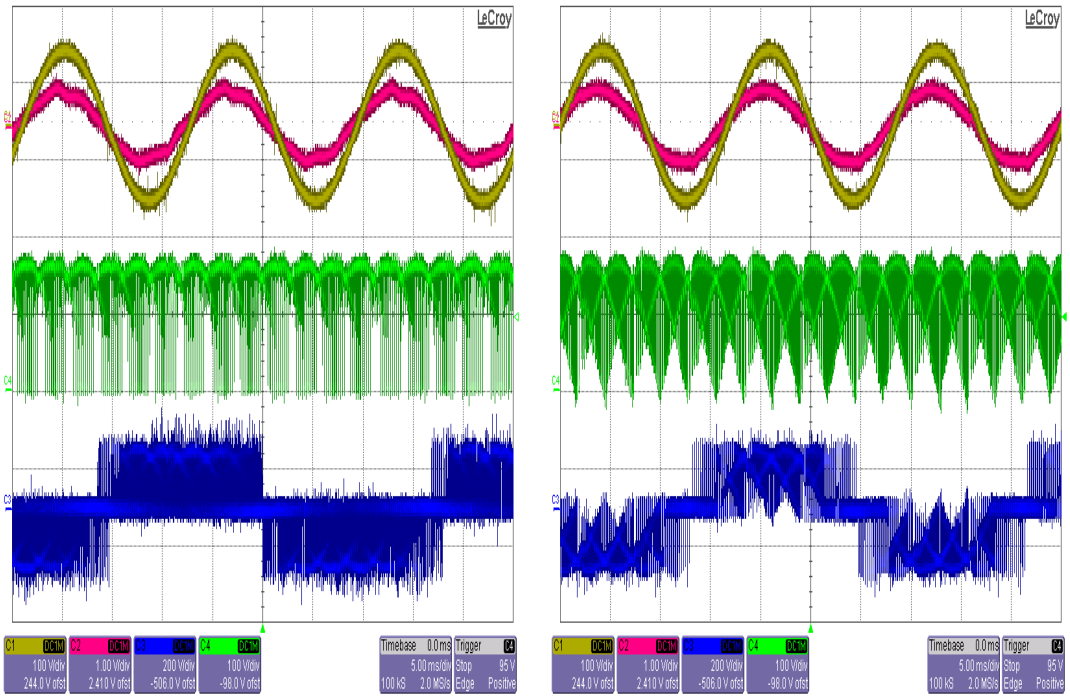
(a) (b)

Figure 5.9: Experimental Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - Output currents (X-Axis : 10ms/div, Y-Axis : 5A/div), output line-neutral voltage (X-Axis : 10ms/div, Y-Axis : 50V/div) and FFT of output line-neutral voltage (X-Axis : 5kHz/div, Y-Axis : 10V/div)



(a) (b)

Figure 5.10: Experimental Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - CMV (X-Axis : 5ms/div, Y-Axis : 50V/div) and FFT of CMV (X-Axis : 5kHz/div, Y-Axis : 5V/div)

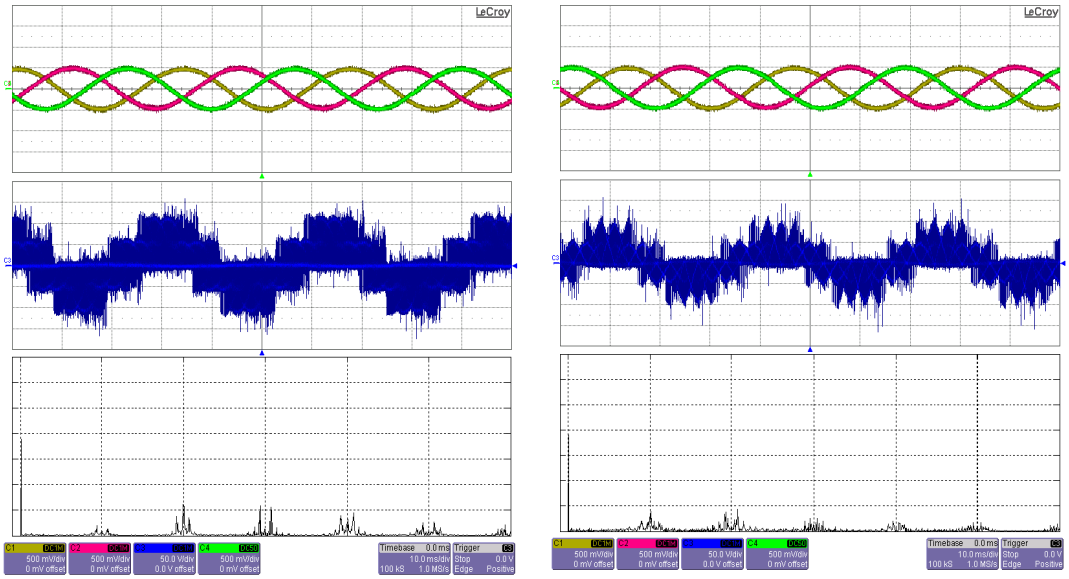


(a) (b)

Figure 5.11: Experimental Results at $m = 0.7$ for (a) Conventional SVPWM (b) Proposed Method I. From top to bottom - Grid voltage and current (X-Axis : 5ms/div, Y-Axis : 100V/div, 10A/div), DC-Link voltage (X-Axis : 5ms/div, Y-Axis : 100V/div) and output line-line voltage (X-Axis : 5ms/div, Y-Axis : 200V/div)

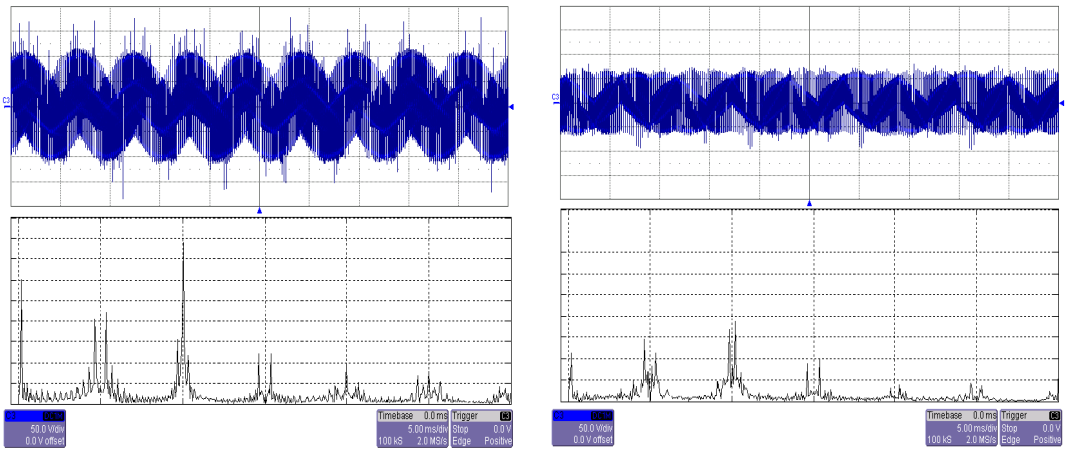
- At $m = 0.4$ - $66V$ for Conventional SVPWM in Fig. 5.13(a) and $41.5V$ for Proposed Method II in Fig. 5.13(b).

The grid voltage, grid current, DC-Link voltage and output line-line voltage waveforms for the conventional and proposed methods are given in Fig. 5.11 for $m = 0.7$ and Fig. 5.14 for $m = 0.4$. The shape of the output line-line voltage waveform is in accordance with its respective DC-Link voltage. As observed, the lower region of DC-link voltage is used for operation of the IMC at a lower modulation index and vice versa. This improves the harmonic spectrum of the output switched voltage of the IMC. It can also be noticed that the DC-Link voltage in Fig. 5.11(b) has no instant of zero voltage unlike Fig. 5.14(b). This is because Method I only uses active current vectors at the rectifying stage Method II uses both active and zero current vectors.



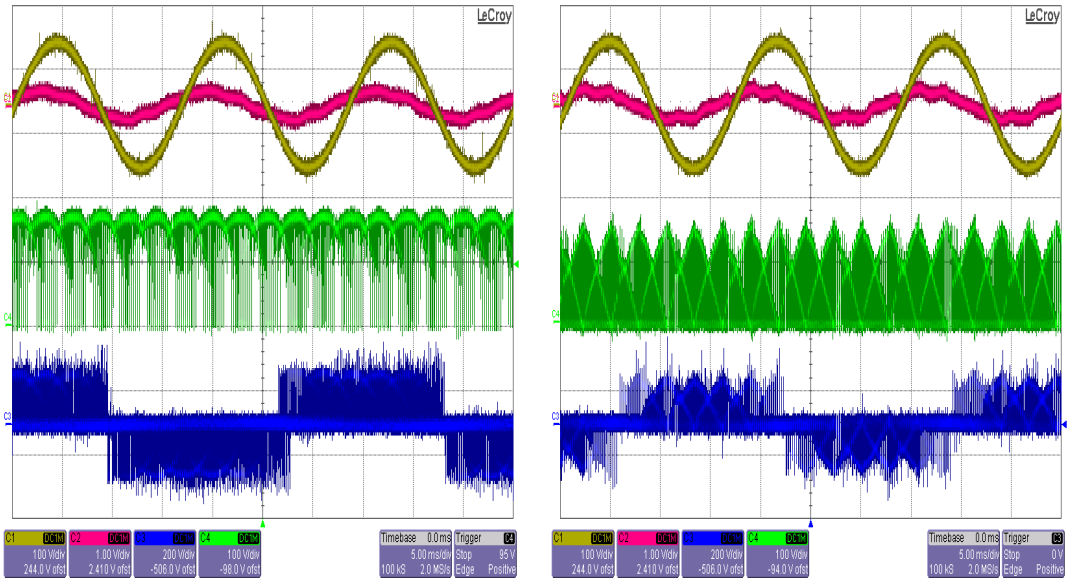
(a) (b)

Figure 5.12: Experimental Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - Output currents (X-Axis : 10ms/div, Y-Axis : 5A/div), output line-neutral voltage (X-Axis : 10ms/div, Y-Axis : 50V/div) and FFT of output line-neutral voltage (X-Axis : 5kHz/div, Y-Axis : 70V/div)



(a) (b)

Figure 5.13: Experimental Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - CMV (X-Axis : 5ms/div, Y-Axis : 50V/div) and FFT of CMV (X-Axis : 5kHz/div, Y-Axis : 5V/div)



(a) (b)

Figure 5.14: Experimental Results at $m = 0.4$ for (a) Conventional SVPWM (b) Proposed Method II. From top to bottom - Grid voltage and current (X-Axis : 5ms/div, Y-Axis : 100V/div, 10A/div), DC-Link voltage (X-Axis : 5ms/div, Y-Axis : 100V/div) and output line-line voltage (X-Axis : 5ms/div, Y-Axis : 200V/div)

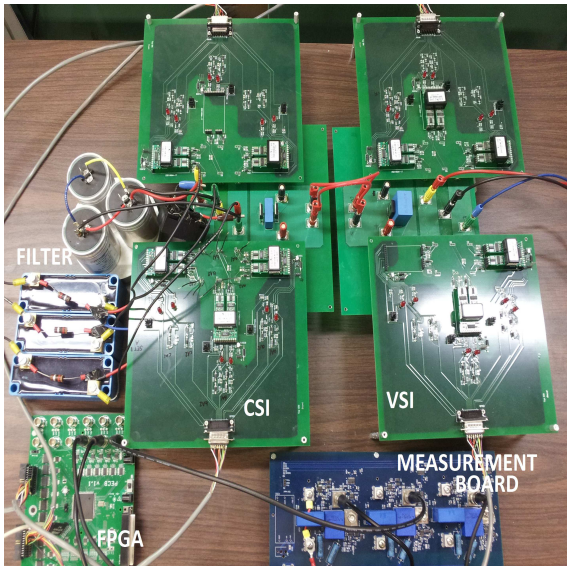


Figure 5.15: Laboratory prototype of the IMC

5.3 Comparison and Performance Analysis

Now that the experimental and simulation results have been presented that confirm and validate the operation of the IMC with the proposed methods of modulation, we shift our focus to compare its performance with the conventional SVPWM method, based on a few parameters like

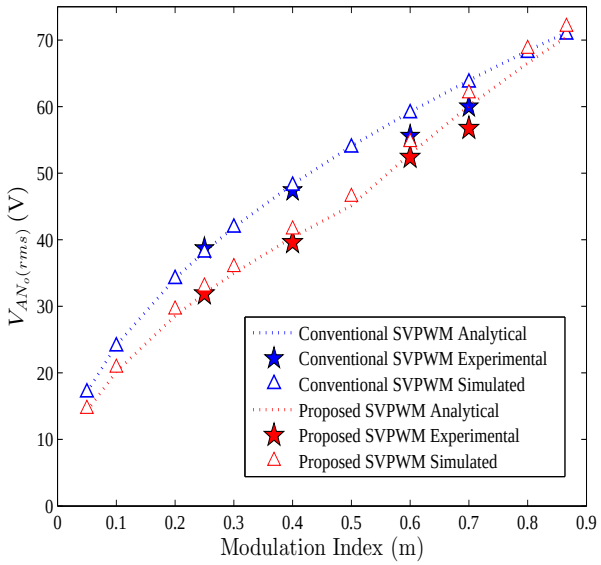
- Output Voltage Distortion
- Common Mode Voltage (CMV)
- Switching Transitions

5.3.1 Output Voltage Distortion

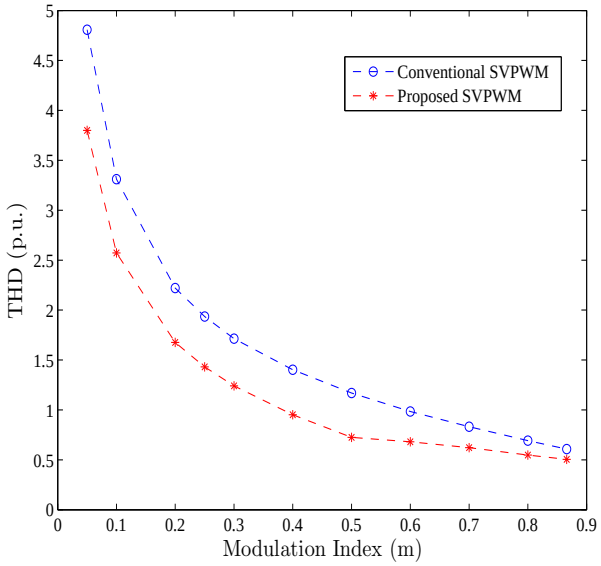
The IMC produces switched voltage at its output with a fundamental sinusoidal component. The distortion in this voltage is due to the presence of switching and higher order harmonic components. The machine terminals are subjected to this voltage. A higher degree of distortion in output voltage would compromise its quality and increase the core losses in the machine.

With change in Modulation Index - Fig. 5.16(a) compares the RMS value of output voltage for the proposed SVPWM with the conventional method for different values of modulation indices. Assuming that the fundamental component is nearly the same in both the methods, the amount of distortion in output voltage follows the same trend as shown. This comparison plot also validates the effectiveness of the proposed analytical estimation method and the expressions provided in Table. 4.4, for the three SVPWM methods. Fig. 5.16(b) compares the THD in output voltage for the simulated model.

With change in Output Frequency (f_o) - Fig. 5.17(a) and Fig. 5.17(b) presents the comparison of RMS value of output voltage with change in output frequency for $m = 0.7$ and $m = 0.4$ respectively. It can be observed from the experimental data points that the RMS values do not change with change in output frequency. This observation can also be concluded from the expressions summarized in Table. 4.4 which are independent of output frequency.

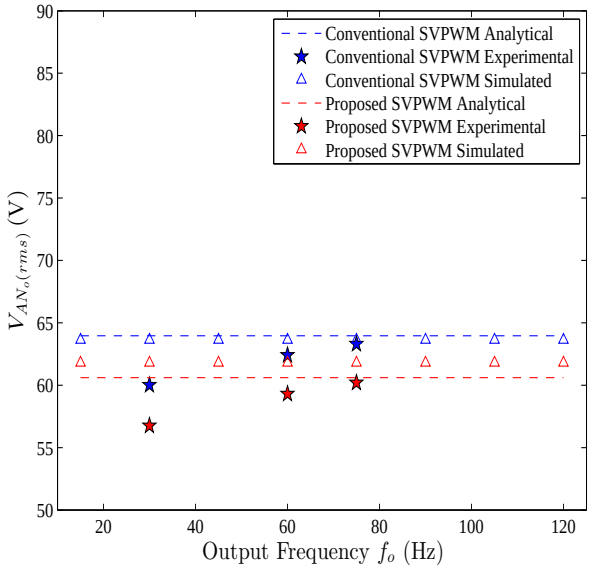


(a)

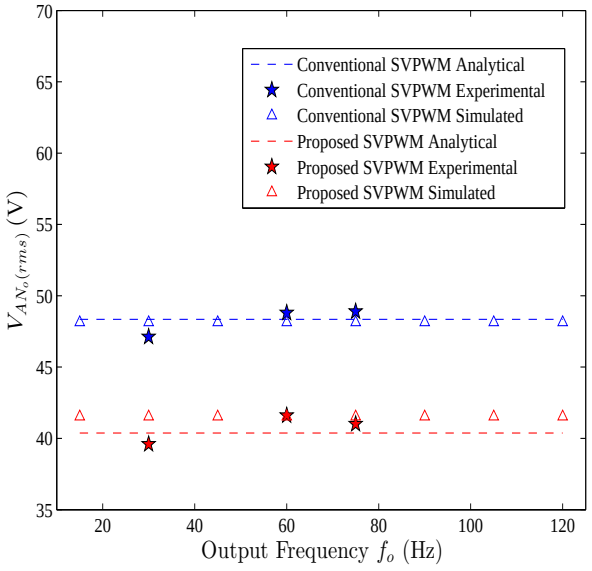


(b)

Figure 5.16: With change in Modulation Index : (a) Comparison of RMS value of output voltage (b) Comparison of THD in output voltage



(a)



(b)

Figure 5.17: With change in Output Frequency : (a) Comparison of RMS value of output voltage at $m = 0.7$ (b) Comparison of RMS value of output voltage at $m = 0.4$

5.3.2 Common Mode Voltage

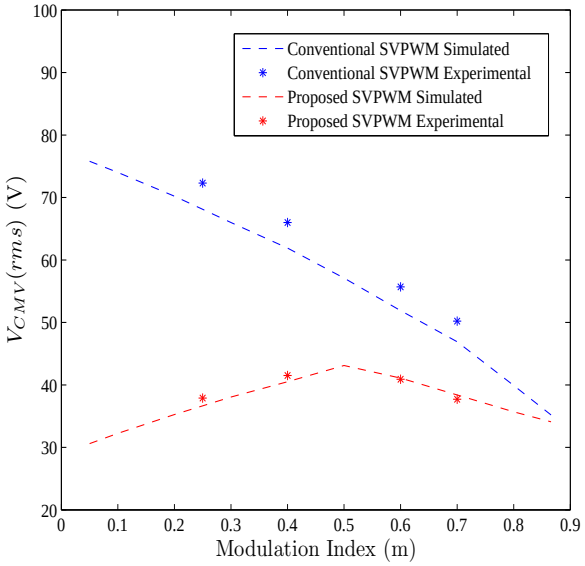
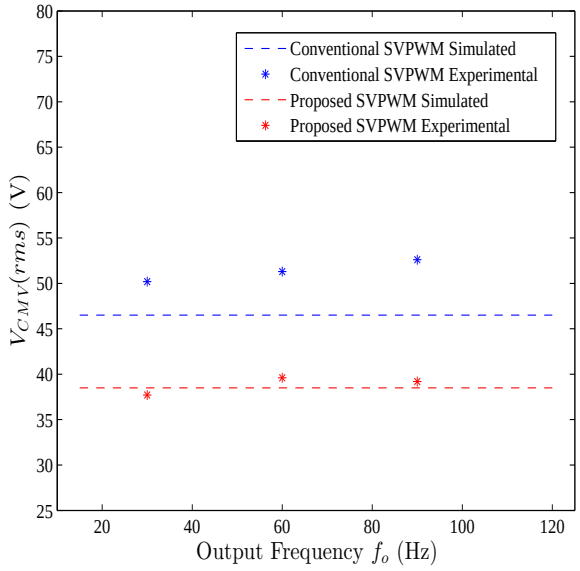


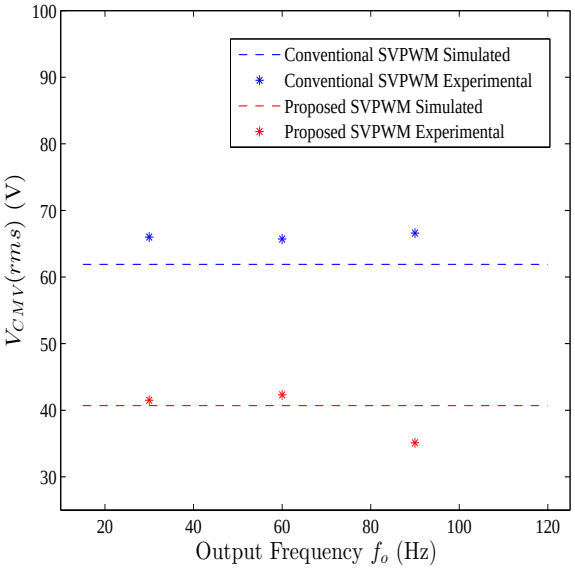
Figure 5.18: Comparison of CMV with modulation index

As proven in the previous sections dealing with experimental and simulation results, in both the proposed methods of modulation, the peak of the CMV is reduced by a factor of $\sqrt{(}3)$ as compared to its corresponding value with the conventional method of modulation. These peak values of CMV remains a constant with change in modulation index or output frequency. The proposed SVPWM method also reduces the peak of the third harmonic component (=$180Hz$), which is the major contributor towards the net RMS value of CMV.

With change in Modulation Index - Here Fig. 5.18 provides a comparison of the RMS values of CMV for the different modulation techniques over a range of modulation indices. We observe that the percentage of improvement in $V_{CMV}(rms)$ for the LMIR is higher than the HMIR. The decreasing trend in the RMS values of CMV with the increase in the value of modulation index, in the conventional SVPWM method can be attributed to the decrease in the usage of zero voltage vectors for the formation of output reference voltage at higher ranges of operation. On the other hand, the proposed methods do not use zero voltage vectors for modulation. The inverting stage of the IMC



(a)



(b)

Figure 5.19: With change in Output Frequency : (a) Comparison of RMS value of CMV at $m = 0.7$ (b) Comparison of RMS value of CMV at $m = 0.4$

is thus operated at its full modulation index for both the methods - I and II. We observe that for Method I (HMIR), RMS values of CMV increase with increase in modulation index while for Method II (LMIR), the RMS values of CMV decrease with increase in modulation index. This trend can be attributed to the usage of different set of current vectors for each method.

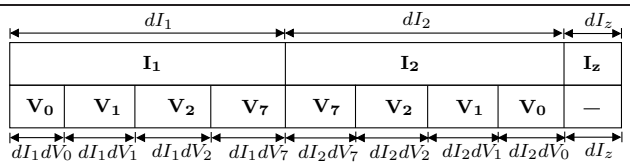
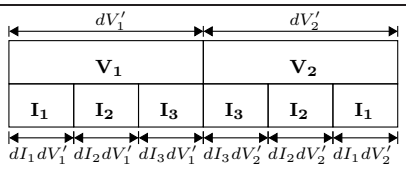
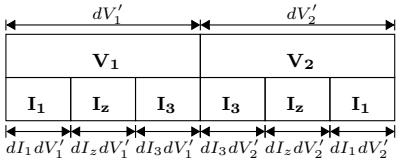
With change in Output Frequency - Fig. 5.19(a) at $m = 0.7$ and Fig. 5.19(b) at $m = 0.4$ presents the comparison of RMS values of CMV for both SVPWM techniques with change in output frequency. It should be observed that the values remain a constant for $f_o < f_i$ and $f_o > f_i$, where f_o is the output frequency and f_i is the grid frequency.

5.3.3 Switching Transitions

A higher number of switching transitions over one time sample will translate to increased switching losses in the converter. Table. 5.1 summarizes the switching sequence of each of the SVPWM methods. The switching sequence represents the current and voltage space vectors used over one sample time and their corresponding dwell times. Here the number of transitions correspond to the changeover from one vector to the other and not the actual transition of switches.

For the conventional method, the rectifying stage of the IMC is soft switched because a transition in the current space vector is simultaneously accompanied with the application of a zero voltage vector. So the number switching transitions in this case correspond to the ones on inverting stage of the IMC. If we consider the switching sequences of the two proposed methods, neither the rectifying stage nor the inverting stage is soft switched. So the total number of switching transitions takes into account both the stages of the IMC. We also observe from the table that the performance of the converter in terms of switching losses will follow a similar trend due to an equal number of switching transitions in all the three SVPWM methods.

Table 5.1: Summary of Switching Sequence and Switching Transitions

SVPWM Method	Switching Sequence	Transitions
Conventional		6
Method I		6
Method II		6

Chapter 6

Conclusion and Future Work

Common Mode Voltage is a very significant practical issue with electric drive systems. Higher values of CMV results in high frequency bearing currents and EMI problems. The bearing currents in particular results in premature failure of motors. Additional hardware solutions addressing CMV, like passive filters and shielded cables have the disadvantage of adding to the volume and cost metrics of the system. This thesis shifts the focus to intelligent control techniques which can reap similar benefits at no additional cost or space requirements. The technical novelty of this work lies in the proposition of a new SVPWM control technique which not only targets at reducing the CMV but also improves the harmonic spectrum of the output switched voltage of the IMC. Considering the fact that the IMC topology finds its use in variable speed drive applications, two independent modulation techniques have been proposed, each targeting a different range of operation of the IMC. These two modes are summarized as 1) HMIR - $0.577 < m < 0.866$ and 2) LMIR - $0 < m < 0.5$.

The switching states of the rectifying stage of the converter control the shape of the DC-Link voltage waveform. Intelligent control (in the form on an SVPWM technique) of these switches provides the flexibility and potential to attain different voltage levels at the DC-Link which further translates to an improved harmonic spectrum of output voltage. Therefore, the objective and control to generate output voltages of a certain magnitude and frequency is transferred to the rectifying stage of the converter. The inverting stage of the IMC is always operated at its full modulation index.

This thesis also proposes a methodical analytical estimation method to accurately

predict the degree of distortion in output voltage. This process has been explained in detail for both the conventional and proposed SVPWM techniques. Simple mathematical expressions have been obtained to estimate the RMS square value of output phase voltages. The expressions only depend on values of input grid voltage and modulation index (operating parameter). It is independent of switching, grid or output frequencies. With a proper knowledge of the fundamental component in output voltage, the THD can be easily calculated. Proper comparison plots have been provided to prove the effectiveness and accuracy of this estimation method.

The working of the proposed modulation techniques have been explained and validated through both simulation results on an IMC model in MATLAB/Simulink and experimental results on a laboratory prototype. The peak values of CMV has been reduced by a factor of $\sqrt{3}$ compared to the conventional technique. The methods also comes with other advanced features like reduction reduction in THD of the output phase voltage, reduced switching losses in the VSI and lower machine losses. Plots comparing the conventional and proposed algorithm based on harmonic content and CMV have been provided. Variations of these parameters with output frequency and modulation index has also been analyzed.

6.1 Future Work

- Implement the proposed algorithm with appropriate V/f control on a motor to analyze the nature of shaft voltage and bearing currents, and compare it with the conventional SVPWM algorithm.
- Usage of active voltage vectors on the inverting stage with normalized dwell times demands an equal compensation on the rectifying stage. Inclusion of this feature can potentially improve the performance of the proposed methods.
- The estimation of RMS square of output voltage and thereby distortion, can be used for the design of output passive filters at the motor terminals.
- The estimation procedure proposed in this thesis can be extended to estimation of CMV and switching losses.

- Proposing another SVPWM algorithm targeting the operation of the IMC at $0.5 < m < 0.577$.
- Comparison of the proposed SVPWM technique with other similar techniques targeting improvement in THD and reduction of CMV.

Chapter 7

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