Parasitic Component Analysis and Acoustic noise evaluation in Voltage Regulator Modules (VRMs)

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Finally, I express my gratitude to my parents for their emotional support and encouragement.

Abstract

Stable and regulated supply voltage has been an important topic of discussion in a consumer electronic products. Every chip and device requires specified voltages with small margins. Voltage regulated modulators (VRMs) have always been proven to provide a solution to this problem. Building a power stage using point of load method helps overcome variability issue in the signal but introduces a converter with lot of supporting components. Multiple combination of capacitors and resistors of different material composition are required to obtain an optimal design for the product. PCB parasitic comes into play and due to high current slew rate physical stress builds up in the caps which tend to come out in form of acoustic noise. This thesis deals with such issues which can improve the product quality but keeping the cost low by utilizing and analyzing components the proper way.

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1. Introduction

In today's world of rapidly evolving consumer electronic industry, there is a constant demand of low voltage, small form factor and high efficiency power supply units (PSUs) which supply power at required specifications to millions of devices across the globe. Including small gadgets like smartphones which consume few watts to power hungry enterprise servers which require few kilo-watts, everything needs their own customized DC/DC power supply units.

With changing technology and miniaturization of devices, different components on the same platform require different power levels. This can be achieved by stepping down voltage at different levels so that every components has its desired voltage. For example inside a computer, microprocessor and DIMMs requires different voltages and same is the case with PCIe module and USB ports. In the past, this was done using a single power cabinet at one place and wires were used to connect individual components. This method did work when voltage levels were in few volts like ±12, ±5 etc. But now, when microprocessor takes 0.85V and other ICs on board need 1.8V, long wires can no longer be used as they introduce parasitic inductance and resistance which causes lot of noise and stability issues.

1.1 Concept of VRMs

To address this problem, Point of Load (POL) the concept was introduced which requires the conversion of power to a different level as close as possible to the load. This helps in supplying high peak current demand, low noise margins and high power densities

resulting in highly efficient converters. These DC/DC converters are called Voltage Regulator Modules or VRMs.

A Voltage Regulator Module (VRM) is a circuit that is soldered or connected to the baseboard which is designed to supply required power and voltage to different ICs and microprocessors. Every VRM on the board is custom designed for the specification mentioned by the vendor. It is a power electronics circuit, essentially a synchronous buck converter which regulates the voltage with very tight precision.

A VRM is a closed loop amplifier, it converts one level of electrical energy to a different level with a regulated current or voltage specifications. Regulation is performed by tapping the output voltage and comparing it to a reference voltage which is then amplifies error signal and used to control a PWM that helps to maintain a voltage level desired by the load.

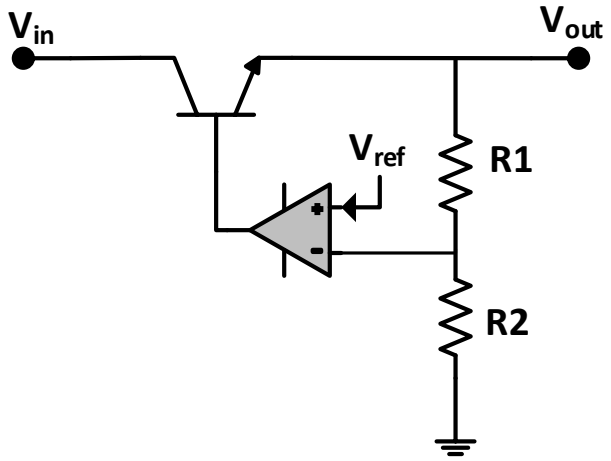

Figure 1. Basic linear regulator

There are basically two types of VRMs: Linear Regulators and Switching Regulators. [1] Former employs an active switch like a BJT or MOSFET controlled by a

high gain differential amplifier. It compares the output voltage with a precise reference voltage and adjusts the switch to maintain a constant voltage.

The latter converts dc input voltage to switched voltage applied to a switch. The output voltage is fed back to a circuit that controls the duty cycle which maintains the output voltage regardless of load variations and supply voltage.

Linear regulators are normally used where converter efficiency is not a concern. It is easy to design, has small form factor, cheap, less noisy but high in heat dissipation. On the other hand when high efficiency converters are required switching regulators are preferred. Although it has high noise, difficult to design and has number of parts, its low heat dissipation and more control on regulation gives it an upper hand to be used in number of applications.

1.2 Problem statement

The line of regulators that is discussed in this thesis is IC based DC/DC buck converter which finds its application in almost every consumer electronic device. TVs, gaming consoles, graphic cards, motherboards, tablets etc. every gadget available around today has one of these converters which helps them to perform better. Small size, affordable, durable and highly efficient which gives means longer battery life. This converter gets attention from CPU and GPU design as they require low voltage, high current with very low ripple output voltage for their low power configuration which takes up around 35-45 Watts or enterprise server CPU and GPU which demands 150-170 Watts. The closer one gets to the load, the sensitive the circuit becomes which includes effect from parasitic impedance such as stability and bandwidth issues. During transients, these

impedances like on board capacitance and interconnects play an important role in determining output waveform of the converter. Along with this issue there is a problem of audible noise from the components itself. Because of piezoelectric effects of MLCCs and inductor coils, the component expands and contracts in its own space and vibrates in multiple frequencies. The one which falls under 20Hz-20 KHz becomes significantly audible and becomes a consumer product problem. This thesis addresses some of such issues and finds ways to minimize its effect.

1.3 Organization of thesis

With the introduction of the concept in chapter 1, and describing the functioning of VRMs in chapter 2, chapter 3 deals with the literature review that introduces new concepts in VR design. Chapter 4 contains the hardware implementation of the tests and experiments suggested. Chapter 5 sums up the results that have been obtained along with explanation and graphs. Finally, Chapter 6 summarizes the work and describes future work that can be done.

2. Functioning of VRM

IC based VRMs gained popularity with the evolution of smaller microprocessor and other ICs on the PCB. Every generation of chip design scales down by half the node size which calls for low voltage operation that leads to demand of converters that supply required power at recommended low voltage and many other constrained parameters. Size of converter became an important factor in deciding the total size of the PCB and the device itself. Since the real estate on the board is expensive, these on board converters have high power densities and have to operate at high efficiencies [2]. Also they have to be very fast, because as IC behavior changes with respect to speed, the converter has to catch up to maintain the smooth working. Slew rates can be up to 20A/us or higher during transients and especially when dealing with microprocessors and GPUs where current is high, slew rate makes a lot of difference [15].

2.1 Power modes

Unlike other power electronic circuits where the load is essentially a motor or drive, where the load changes are gradual and not too spiky, semiconductor devices (load) try to work at two extreme states. These states are defined to save power consumption in a chip during its peak operation. On a typical base board, there are kind of IC chips. One which are always powered ON that do not consume a lot of power like PCIe module, Ethernet ports controller, wireless communication ICs, etc. and on the other hand there are power hungry chips like CPU and GPUs which switch between specified power states to save power efficiently. Most modern chips have mainly two power states: active mode and sleep mode.

Active mode is defined as the time when IC is utilizing its maximum potential consuming high power. They are designed to operate at high frequency such that work can be done in small time frame and then switch immediately to a low power state defined as sleep mode where it consumes minimal current just to keep alive and maintain standby power such that, as and when demand increases it can switch back to active mode easily.

2.2 Types of IC controllers

Depending upon the size and functionality of the device, these controllers are available at different vendor with customized specification. Usually they are characterized as general, automobile, military, communication etc. such that their parameters can be set according to their working environment. Harsh conditions require more relaxed parameters. Components used in military devices are design to be functioning at extreme temperature and their casing is more rigid.

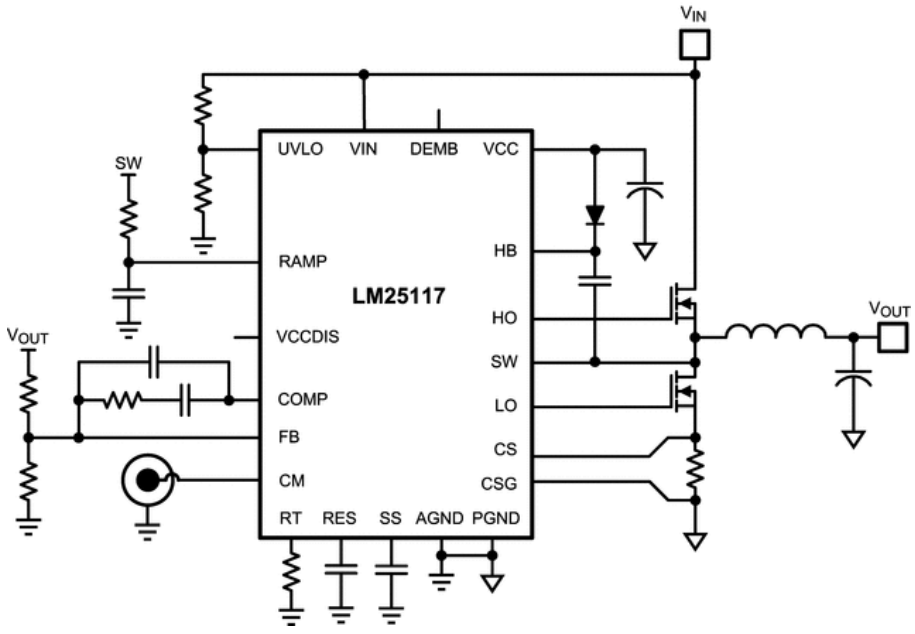

Figure 2. Example of discrete converter [24]

These converters are design to work at a specific configuration or they can be modified as per requirements. Broadly they are classified as: Discrete and Integrated converters.

Discrete converters are the ones which are completely configurable and design can tweak most of its parameters using external components like its switching frequency, feedback loop, compensation loop, ramp up signal, soft start time, etc. The figure 3 below shows an example of discrete converter that uses many resistor and capacitor to set the parameters. In some of the converters, MOSFETS are also configurable. Therefore it takes more space on the board, more time to design but it gives designer an upper hand in maintaining the desired output waveform. At the same time it arises issues regarding picking up noise because of its so many discrete components.

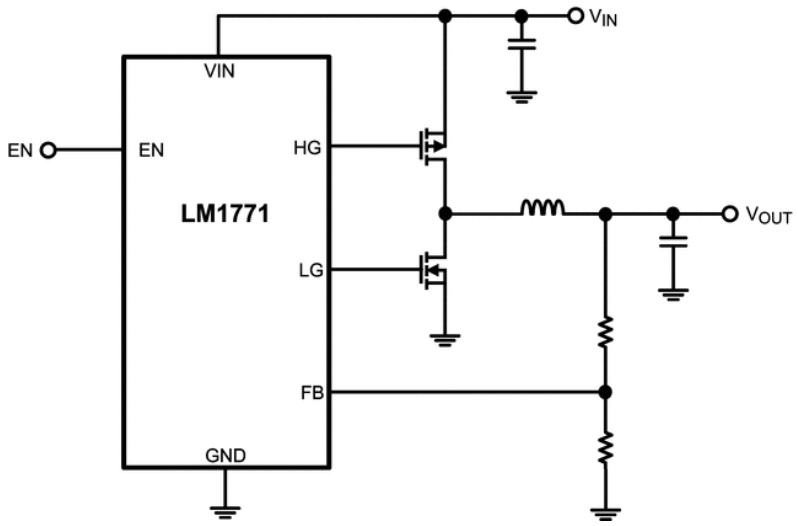

Figure 3. Example of Fully Integrated converter [3]

On the other hand, fully integrated converters are available which are not that flexible with its parameters. There is no control over compensation loop parameters. Switching frequency and soft switching time is fixed. Because of less number of external components, the size on board is relatively small and easy to design. The figure 3 shows

an integrated converter which is hardly customizable. This minimizes all the hassle of component selection, buying, testing and characterization which can save money and important time in the design process.

2.3 Voltage feedback and compensation loop

VRM can be divided into three blocks that control the functioning of the system. From the figure 4, Modulator block has switches and its PWM circuitry to control duty cycle. Output filter generally consists of inductor and output capacitor which controls the charge and discharge cycles on the output waveform. Also its compensation loop which takes input from voltage divider circuit, processes it through an error amplifier and decides the stability of the converter.

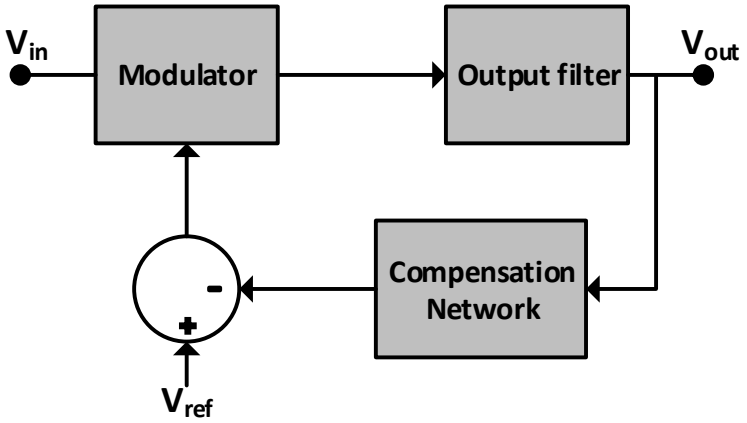

Figure 4. Block diagram of closed loop converter

A more detailed diagram of the system can be seen below where it can be broadly divided into plant and feedback loop. The feedback loop starts from output voltage getting evaluated by voltage divider circuit which is set to the desired output value. The lower resistor value is fixed first and then upper resistor is adjusted. The lower resistor R2 is out of the AC analysis of the circuit and does not affect the bandwidth of the circuit directly. It plays no part in determining the poles and zeros of the converter. [6]

$$\frac{R1}{R2} = \frac{V_{out}}{V_{ref}} - 1 \qquad \text{... (1)}$$

This is fed to the error amplifier which is then compared with a reference voltage to generate an error signal used to rectify the duty cycle. In many modern chips output of the error amplifier is termed as COMP. This is applied to one of the inputs of PWM comparator and saw-tooth voltage ramp is applied to other input which is either internally generated or derived from current ramp. This results in pulses of desired width which is used to drive the switch.

One very different approach to control in modern converter is a technique called feed-forward correction. When there is a disturbance the controller does not know beforehand how much correction is required to stabilize the system. It works through the process and finally reaches to a stable point.

This technique requires input voltage to be sensed and slope of the comparator saw-tooth ramp increased if input goes up. In buck converter the governing equation is $D=V_{out}/V_{in}$. Therefore if input increases, duty cycle should go down. So rather than wait for control voltage to decrease duty cycle, one can also change the ramp itself, this helps with the change almost instantaneously.

Pulses obtained from the PWM comparator now controls the gates of the switches which works alternately in charge and discharge cycles. To increase the efficiency of the converter, Schottky diode is placed across lower switch, to carry some high circulating current during short circuit conditions.

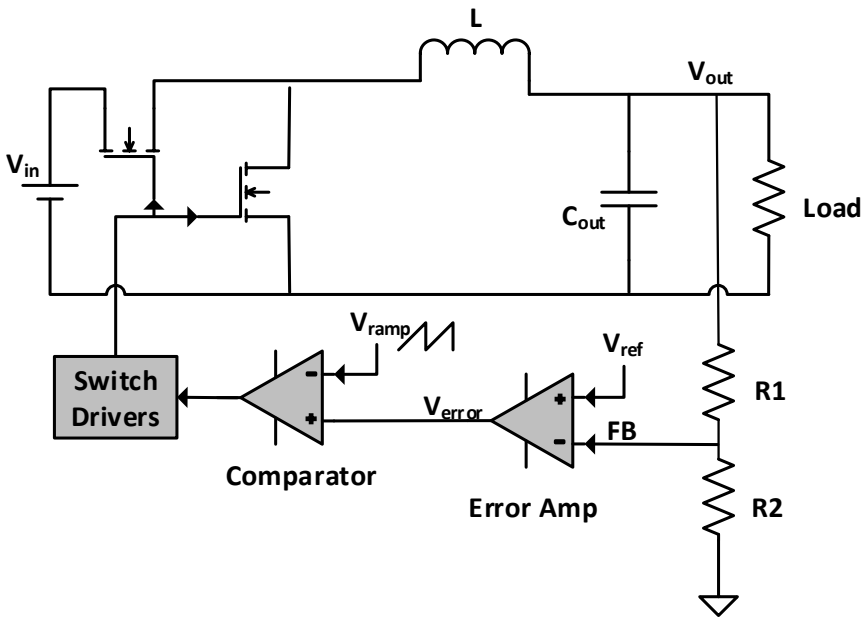

Figure 5. Closed loop system of a synchronous buck converter

Compensation loop plays an important role in stabilizing the system. There are three types of error amplifier schemes which are used depending on their usage, complexity and flexibility. This thesis will emphasis only on type III loop as that will be used in simulation and hardware setup. The transfer function of type III error amplifier shown in the figure 5 can be written as:

$$\frac{wp0}{s} \cdot \frac{\left(\frac{s}{wz1}\right)+\left(\frac{s}{wz2}\right)+1}{\left(\frac{s}{wp1}\right)+\left(\frac{s}{wp2}\right)+1} \quad \ldots (2)$$

Ignoring the minus sign because of negative feedback system, there is one pole at origin, two poles and two zeros to work with. This gives more control over parameters and obtaining desired bode plots. The loop is stable for any phase shift less than 360 degrees, a critically damped system with last loop response and minimal overshoot will have a phase margin of about 60 degrees. Usually any phase margin above zero degrees is stable, but

lower values of phase margin involves a lot of ringing in the loop during transients or any slight change in load

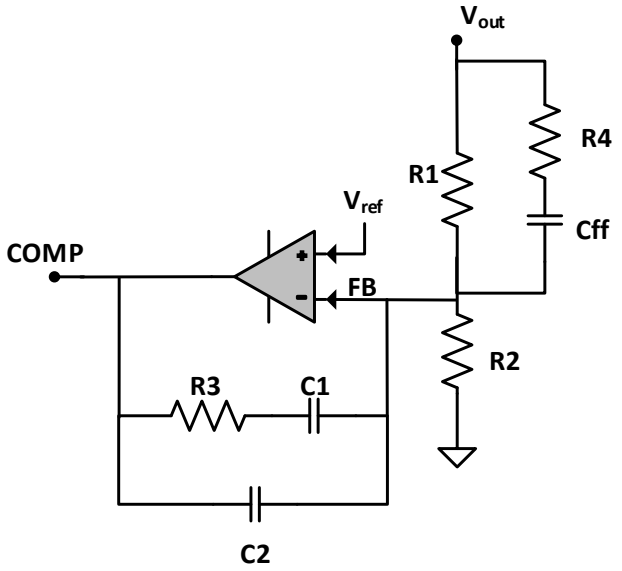

Figure 6. Type 3 compensation network

Another point to be noted here is the capacitor connected in parallel to the higher side resistor in the feedback voltage divider circuit. This is called feed forward capacitor used to correct disturbances in gain and phase margin plot because of parasitic impedances on board. A more detailed explanation will be given in further topics in the thesis.

3. Literature Review

This part deals with the studies and research findings related to problems with parasitic impedances and stability issues with DC-DC converters. PCB design and layout play utmost important part in a converter design which is limited by tight rules. Performance of a converter is solely based on how components are placed on the board. That is why datasheets give general design rules to emphasis placement of parts at proper location. A more detailed information on design and layout of board with tips and tricks to place components can be found in literature published by the vendor of that specific product [7]. It provides in depth information on EMI issues, crosstalk, ground planes, decoupling capacitors, traces, vias and board stack-up. These are few of the design consideration which help in building a more stable converter free from voltage spikes and capable of carrying large currents without glitches. Transients prevailing the system has to be studied which are closely related to parasitic impedances on the board.

Although there are few basic rules that everyone follow while designing a layout e.g. output decoupling capacitor should be placed as close as possible to the load so that the capacitor is able to provide the required transient current [15]. Those rules are for minimum consideration of the design and will not be sufficient for this thesis. There has to be more detailed values of the traces on board because that is something which makes all the difference when designers talk about a power supply DC-DC converter for a microprocessor. There has been a lot of effort put into calculating stray impedances from PCB layout such as package leads, pad to ground, pad to trace caps and similar parameters.

3.1 Impedance Measurement

There are different methods proposed in literature to find stray impedance values. Most reliable method suggests to use physical dimensions of a trace or pad to find its impedance which is based on the assumption that all the dimension are rectangular [8] [9]. With more powerful simulation packages one can also find those values using softwares like Maxwell etc. This thesis shows some easy lab techniques to find those values which can executed using simple lab equipment.

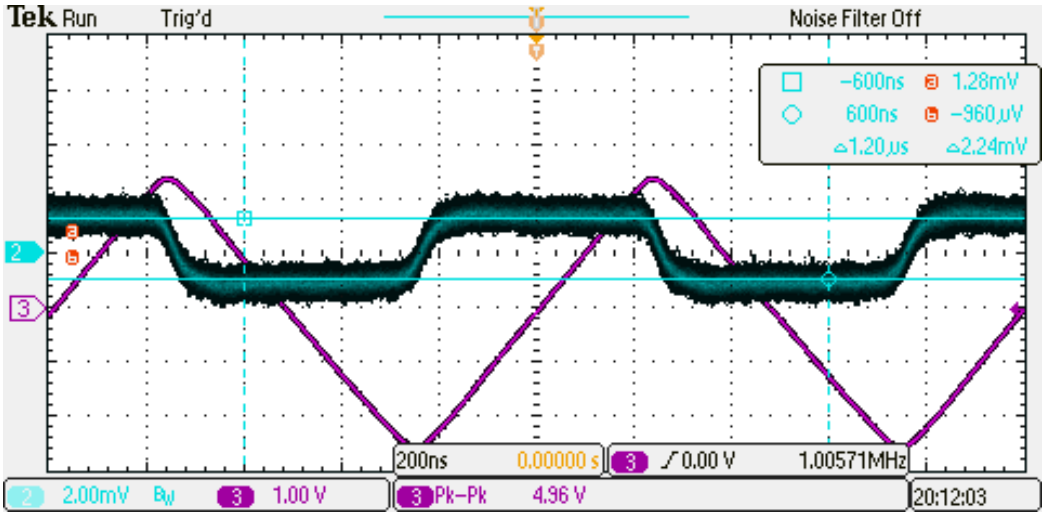

Figure 7. Input and output signals through the coaxial cable

As mentioned in [10], capacitance and inductance can be found by passing triangular wave through a trace using a frequency generator and observing at the waveform at both ends. The technique involves calculation of current passing through the trace with known values of termination resistor (R) involved.

When a triangular waveform (V_{1pp}) is passed at a known frequency (F) through an isolated trace on board as shown in the figure 7. The waveform on the other end looks like a distorted square wave (V_{2pp}). Pk-pk voltage waveform values are taken as input for the

calculation which gives a value of 2.2pF. This technique can be used to calculate trace and pad capacitance to model a converter in simulation which can be more realistic.

$$C_P = \frac{V_{2pp}}{V_{1pp}} . \frac{1}{4.R.F} \quad \text{... (3)}$$

3.2 Voltage Injection Method

Another challenge in this process was to measure bode plot using network analyzer and on board components. This was very crucial as every change made to the component as an improvement to DC analysis should also be verified at AC level. Very small variation in components can make huge difference when it is a part of feedback loop because of amplifiers.

Bandwidth of controls loop describes the response time of the system; with respect to switching regulators, it is indicative of the time it takes for output voltage to recover after a transient or load change, for example a processor transition from sleep to active state. Also control loop margin is sign of stability of system and dc gain provides information about steady state error of DC output voltage. To obtain so many parameters, it becomes very necessary to obtain a bode plot of the system.

When it comes to DC-DC converter, the best way to calculate bode plots is using voltage injection method [13]. A given integrated converter could be stable at a given specifications and conditions but it becomes important to measure its stability in conditions when these given parameters changes, for instance, input voltage, load, temperature, behavior of the load etc. Converter loop stability has to be measured at worst case scenarios.

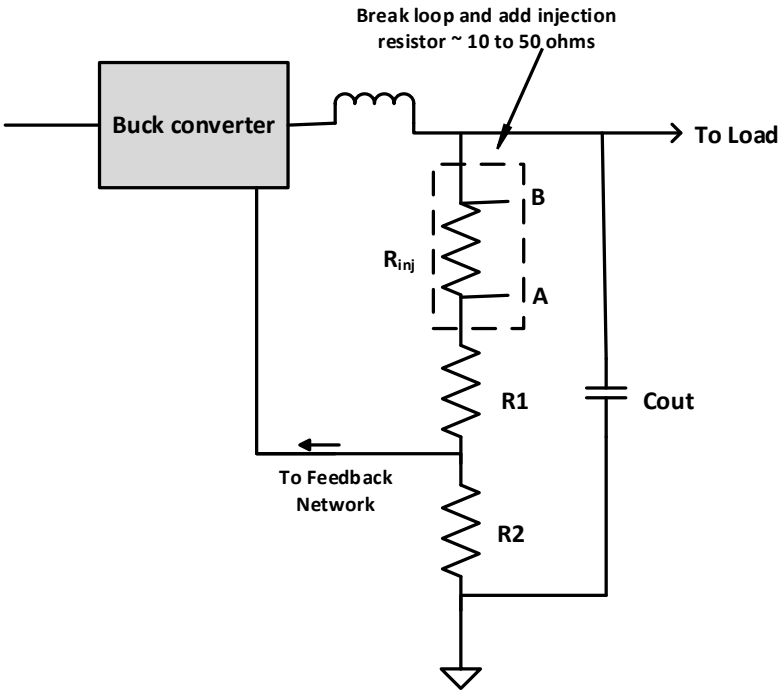

Figure 8. Modification to circuit for voltage injection method

The best way to do this is to inject an error signal in the loop and observe how it reacts to it. Sweep the frequency of the error signal within the desired frequency range and plot gain and phase response as bode plot. To start with this measurement a small resistor is required to be added in the circuit by breaking the feedback loop as shown in the figure 8 [14]. The injection resistor R_{inj} is added close to the top feedback resistor R1 and output with test points A and B on both sides for the probes or connectors. The value of this resistor can vary between 10-50ohms as it will not affect the feedback loop causing any error. The actual loop gain $T_v(s)$ and measured gain T(s) can be formulated as below. $Z_1(s)$ being the source impedance and $Z_2(s)$ as load impedance [11].

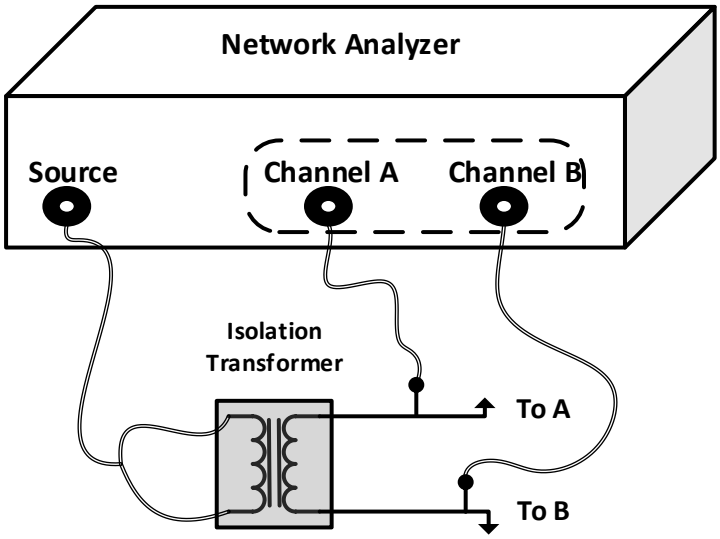

Figure 9. Hardware setup for voltage injection method

$$T_v(\mathrm{s}) = \mathrm{T}(\mathrm{s})\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) + \frac{Z_1(s)}{Z_2(s)} \quad \ldots (4)$$

As far as the hardware test setup is concerned a network analyzer and an isolation transformer is used. The source signal is isolated from the power supply using an isolation transformer so that it would not affect test circuit also it will not inject any signal back to the network analyzer that could spoil it [12]. Channel probes are connected to respective test points as shown in the figure 9 and bode plots are obtained using a computer. Gain margins and phase margins can be easily calculated using markers.

3.3 Feed forward Capacitor

A lot of effort is put into different ways to keep unwanted fluctuations in waveforms out of the way because of parasitic impedances. This adds extra space and cost on the board. But the question which persists is how to overcome that problem in an inexpensive and compact ways. According to [16] [17], a feed-forward capacitor comes handy in solving this problem. This is a method to improve stability and bandwidth using a capacitor

placed across the high side feedback resistor. This capacitor adds a pole and zero ($f_z<f_p$) to the control loop. This improves both transient response and bandwidth of the system which is shown in the result section.

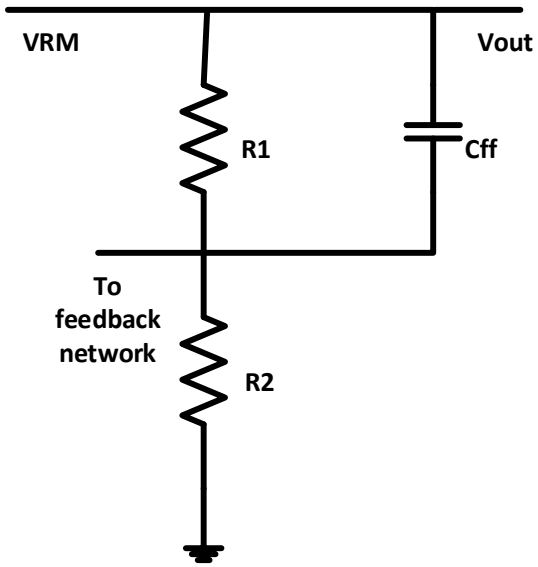

Figure 10. Placement for feed-forward capacitor

Cff value is chosen such that the gain and phase boost of the feedback increases the bandwidth of the converter which is disturbed by the parasitic effect while still maintains an acceptable phase margin. Very careful observation has to be done, because there could be a chance of causing loop gain to crossover too high in frequency and Cff phase boost insufficiency to make system unstable. To determine its value to crossover frequency of the system is found without the Cff and using network analyzer. Once this is known use equation (5) to find appropriate Cff value which gives bandwidth improvement and phase boost [17].

$$f_{nocff} = \sqrt{f_z \cdot f_p} \quad \text{... (5)}$$

Geometric mean of frequency gives us crossover frequency with no Cff. Where f_z and f_p are:

$$f_z = \frac{1}{2\pi.R1.Cff} \quad \text{... (6)}$$

$$f_p = \frac{1}{2\pi.Cff}.\left(\frac{1}{R2} + \frac{1}{R1}\right) \quad \text{... (7)}$$

Combining the above equations, and solving for Cff:

$$f_{nocff} = \sqrt{\frac{1}{2\pi.R1.Cff}.\frac{1}{2\pi.Cff}.\left(\frac{1}{R2} + \frac{1}{R1}\right)} \quad \text{... (8)}$$

Cff takes the form of optimal value as Cff_op

$$Cff\_op = \frac{1}{2\pi.f_{nocff}}\sqrt{\frac{1}{R1}.\left(\frac{1}{R2} + \frac{1}{R1}\right)} \quad \text{... (9)}$$

This method will be used in next chapter to find optimum numerical value for my hardware.

3.4 Output capacitor selection

For a VRM, output capacitor serves two purposes, one to reduce voltage ripple and second to provide high currents when load changes very rapidly. Usually it is selected as a combination of electrolytic and ceramic capacitor to be cost and area effective and to reduce ERS and ESL. Electrolytic caps are usually bulky poscaps which can store large amount of charges and MLCCs helps in maintaining ripple content in the output signal.

And as the name suggests, MLCC is made up of multiple layers of solid electrodes and dielectric which expand and contract at atomic level and changes it shape. But because of its small size it starts vibrating. These vibrations can fall under audible frequency range (20Hz-20 KHz) and makes unpleasant sounds. These sounds can be from the MLCC itself or can be from the MLCC hitting the PCB which makes even more noise.

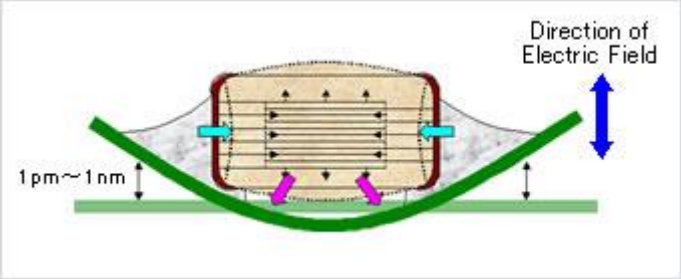

Figure 11. Dynamics inside MLCC [24]

After doing many different tests and trying different samples of MLCCs, this thesis presents some results which can bring down the cost of the project.

4. Simulation and Hardware setup

The simulations were done on Cadence PSPICE because it gives more realistic waveforms as it uses dynamic simulation. Also PSPICE models of most of the components are easily available which can be imported to design files. These models are close approximation of the device in production.

For hardware module, a high current low voltage converter was selected which had type III compensation loop e.g. Texas Instrument part TPS40055 which is a discrete type synchronous buck converter with a regulated output of 1.8V and can carry up to 15A.

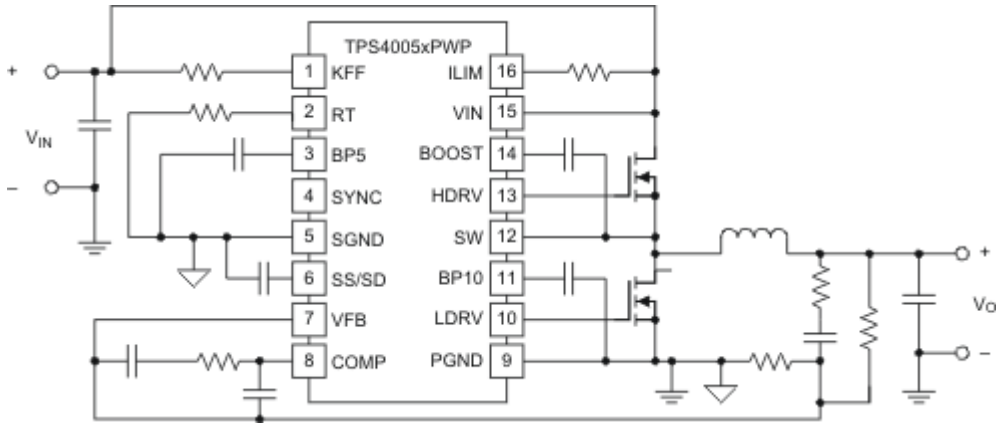

Figure 12. Circuit diagram for TPS40055 [4]

Most of its parameters are configurable like switching frequency, soft start time, MOSFETs, etc. Its PSPICE model is also available which made simulations more efficient. This part can be used in server application where it can power the microprocessor and ICs on-board. For this reference design an evaluation board was used by Texas instruments for better comparison of results. It was configured to run with switching frequency of 300 KHz, this required a capacitor calculation. Similarly there were other parameters which were designed using the datasheet provided. For LC filter design minimum values were calculated using classic formulae but to examine the effect of overshoot and undershoot of

voltage during transient additional consideration of inductive and capacitive energy was done [5].

$$L_{min} = \frac{(V_{in} - V_{out}).D}{I_{ripple}.F_{sw}} \quad \text{... (10)}$$

$$C_{min} = \frac{I_{ripple}}{8.V_{(out)ripple}.F_{sw}} \quad \text{... (11)}$$

The above given equations can be used to calculate a LC filter which considers the effect of output voltage ripple and inductor current ripple but to account for transients lode response especially during mode change, one has to accommodate this effect because as load changes from high to low, the converter increases the output voltage temporarily to adjust the duty cycle. This increase in output voltage is known as overshoot (V_{ov}) and output capacitor should be designed to handle this condition. This can be done by equating total energy before and after the load transient.

$$\frac{1}{2}.C.{V_{out}}^2 + \frac{1}{2}.L.{I_{pk}}^2 = \frac{1}{2}.C.(V_{ov} + V_{out})^2 \quad \text{... (12)}$$

I_{pk} is the change of load from maximum to minimum value. Solving for C in this equation gives:

$$C_{min} = \frac{L.{I_{pk}}^2}{(V_{ov} + V_{out})^2 - {V_{out}}^2} \quad \text{... (13)}$$

There is a tradeoff between output voltage response and output voltage ripple. These above equations can be used to balance those two parameters. To simulate the

different loads, DC electronic load was used by BK precision which allows to go up to 30 A of current.

Figure 13. Tps40055 evaluation module

5. Results

Below is the schematic for the test circuit which has model from Texas Instruments and it has MOSFETs and Schottky model too. It is supplied with 12V DC and a pulse current load is connected. Also feedback and compensation loops are modelled.

5.1 Parasitic Impedance

LC filter has 4 capacitors: 2x470uF, 1x47uF and 1x0.1uF which plays important role in filtering out undesired oscillation. To damp more oscillation one can use big L and C values but in industry specific commercial models designers tend to keep components in budget because of cost and area.

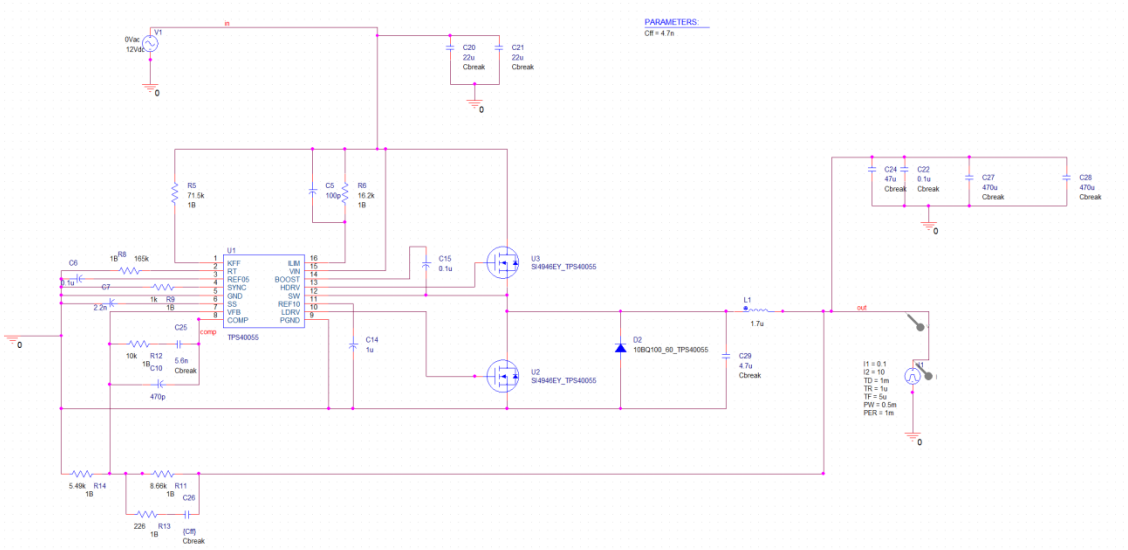

Figure 14. PSpice circuit simulation for TPS40055

According to paper [18], for better response of a DC-DC buck converter, it is suggested to use high switching frequency. This leads to a higher bandwidth for the feedback loop which in turns increases crossover frequency. Doing this helps with obtaining high slew rate in output voltage as inductor tracks the change of load current up

to the bandwidth. Therefore helps in reacting to the change in loads and transients rapidly which finally increases VRM response.

But the question arises how high the switching frequency can be. Although it can help in reducing the size of our LC filter because the charging discharging cycle decreases. It tend to create more problems than solutions like high switching losses, EMI problems and the one which designers are concerned about, the parasitic impedances comes into picture at high frequency. It becomes utmost important to fix this issue as the CPU or IC connected as load require such a high precision in supply voltage. It can also cause instability which may even turn off or damage a vital and expensive piece of component in a system.

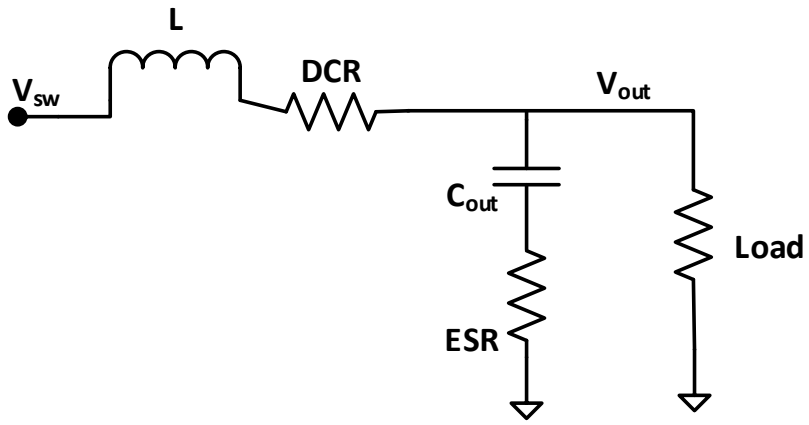

Figure 15. Standard model for output LC filter

To understand this one has to calculate all the values in the standard model for filters in a converter using the techniques explained in previous chapters [19]. This step becomes utmost crucial as the values obtained are extremely small and one tends to ignore such small values in many other cases but here high frequency can make significant changes.

The figure 16 shows a standard model of a filter which only takes into account of DCR from inductor and ESR from capacitor which makes an ideal situation in this case as no effect of parasitic impedance can be seen. Its frequency response using the test circuit over a wide band frequency to observe any deviations and shown in figure 16.

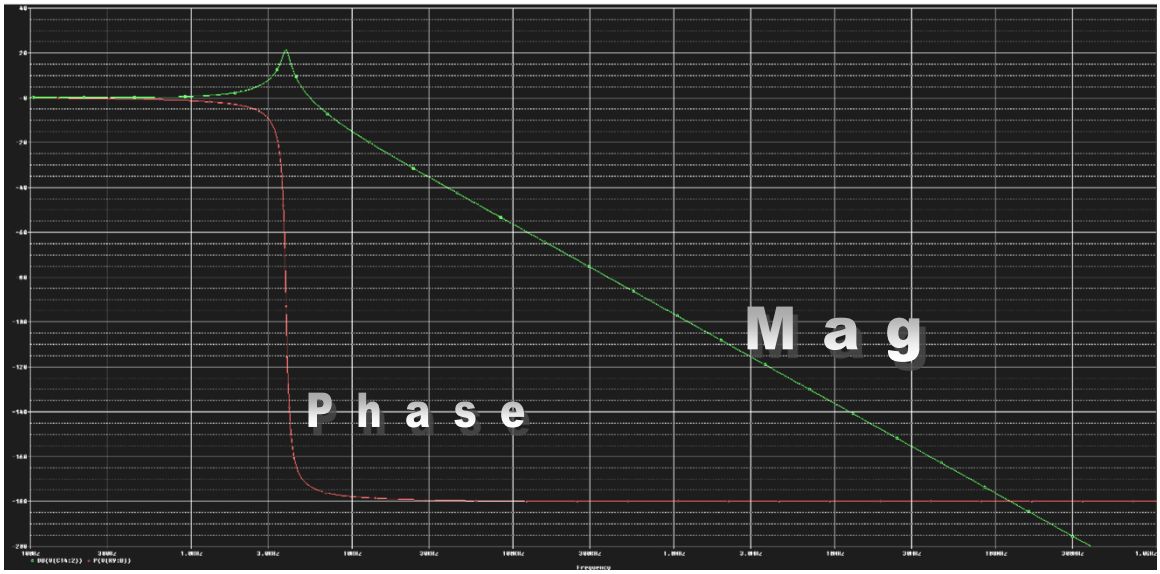

Figure 16. Bode plot of output filter of standard model

The graph looks like an ideal frequency response plots with no abnormalities at high frequency. In real world situation this is not the case because the board parasitic impedances comes into picture. Pad capacitances, trace impedance etc. comes together to create some variation in the response which is undesired and it rectification methods will be discuss in further topics.

Below is a model of output filter but with all the parasitic impedance represented as the standard model [19] for VRMs. It takes into account of all the components from inductor pad, output bulk capacitors all the way through the point connected to the load. All these components are on board and processor package impedance components are not included which is out of the scope of this thesis.

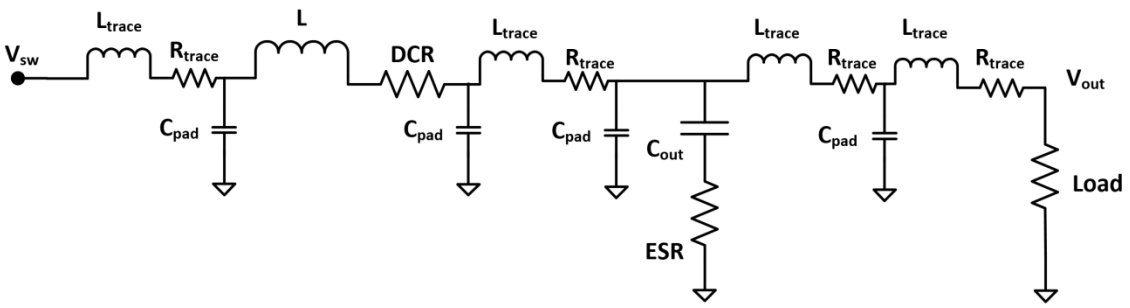

Figure 17. Practical model for output LC filter

It consists of all the hidden components of the board and makes our model more legit to analyze in computer simulations. All the values are calculated by the methods explained in previous chapters. A FR4 board is used, electrical properties and geometry help us to find PCB parasitic values. A bar of 1 square inch cross section and 1 foot long has about 8.3 micro ohms of resistance [20]. With the help of support engineers at Texas Instruments all the desired impedance values were obtained. Average trace resistance given by R_{Trace} which is 0.025ohms/foot on our 0.062 inch 4 layer 2 oz. annealed copper board with layer to layer spacing of 0.02 inch [21]. Similarly C_{Trace} and L_{Trace} have been calculated using the given physical and electrical properties which is 3.1pF/inch and 100pH/inch.

Once all the required parameters are ready, they are substituted in the model using PSPICE tool and simulated for frequency response graph with a wide band frequency as shown in the figure 18. At very high frequencies, a drastic deviation in the response is noticed because of the parasitic impedance involved in the circuit on board. This is because the small values of impedance forms different loops which reacts to high frequency components in the signal. This changes gain and phase margin of the system which is undesired and may affect the system stability. It changes the crossover frequency of the system if it lies in the affected frequency band.

One has to take special attention in designing converters which has crossover frequency in this range. With developing technologies of converter design, DC-DC converters can operate in GHz range and these are the ones which will be affected the most. Such converters demands are increasing [22] and this thesis deals with ways to rectify and optimize this problem. These are used in high precision military and aerospace designs where scope of deviation is next to zero as high stakes are involved.

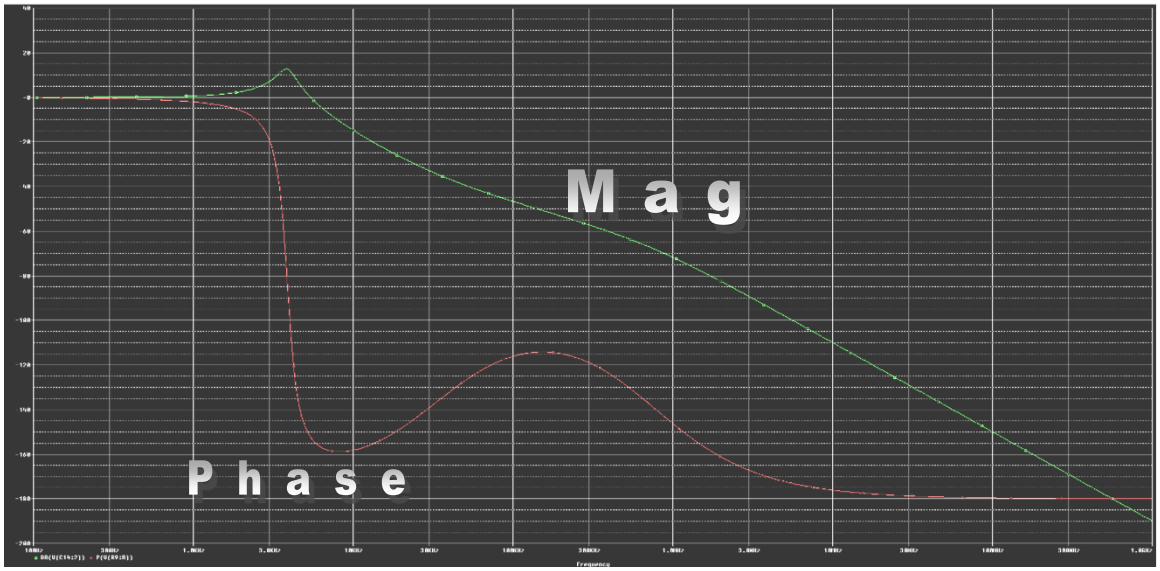

Figure 18. Bode plot of output filter of practical model

This plot shows that a converter designed for a particular set of parameters can deviate because of parasitic impedances. The solution proposed for this problem is to use feed-forward capacitor as mentioned in previous chapters. As this is a type III compensation loop the value for feed-forward capacitor is calculated but it needs to be optimized to account for the above described disturbances.

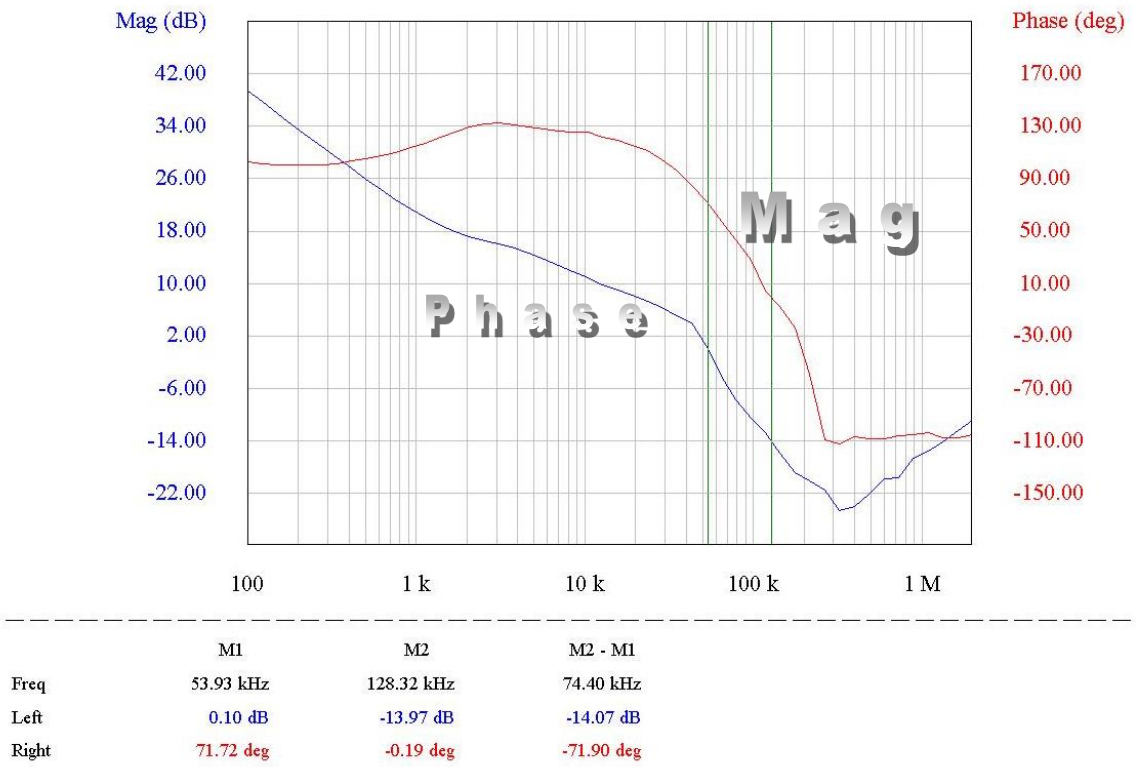

Figure 19. Network analyzer output for un-optimized Cff

Consider the components which matters in this analysis:

- L = 1.7uH
- C_{out} = 2x470uF, 1x47uF, 1x0.01uF
- C_{ff} = 4.7uF

This value for C_{ff} comes from the initial calculations of optimum location of poles and zeros for the loop. Bode plots can be used here to understand clearly the improvement with this technique. As mentioned in previous chapters, direct voltage injection method is used to calculate the bode plots using a network analyzer.

The figure 20 shows a plot without any changes with components configuration as specified above. The first green marker from left shows the crossover frequency of my converter which is around 54 kHz with a phase margin of 71 degrees.

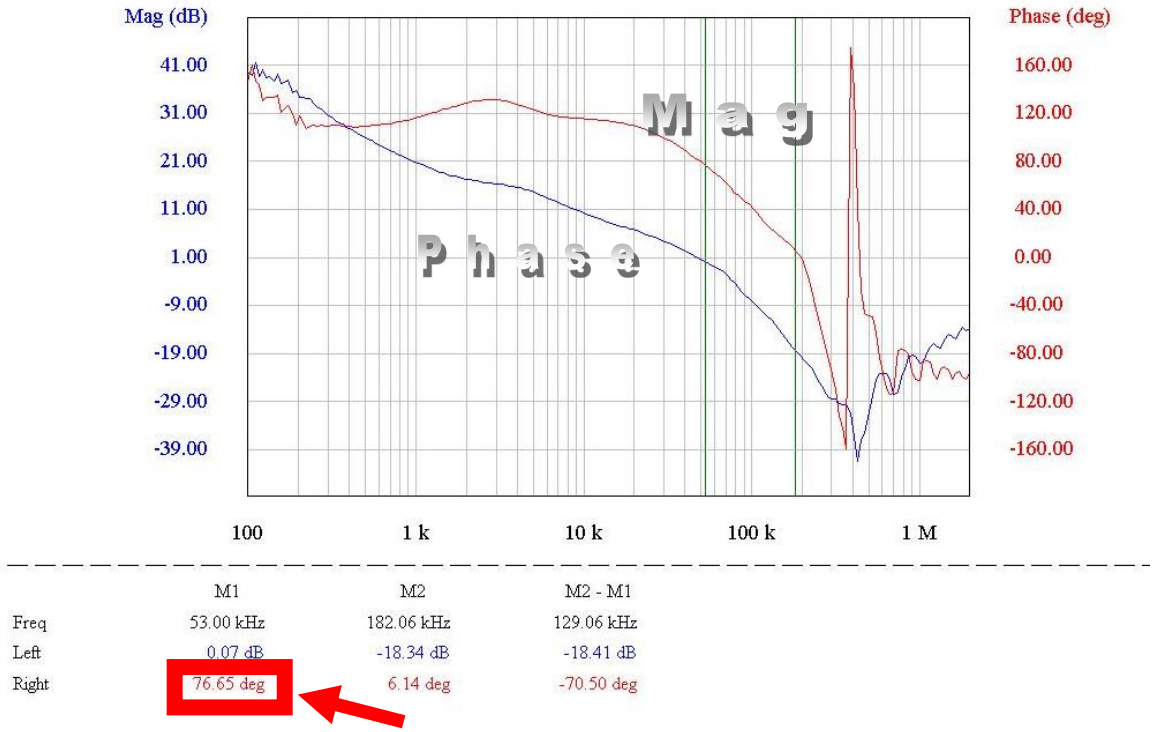

Figure 20. Network analyzer output for optimized Cff

Now because of parasitic impedances these values changes when switching frequency goes beyond 1 GHz. By calculating optimized value of Cff one can adjust the phase and gain margin along with crossover frequency. For this find crossover frequency of the same converter without any feed forward capacitor. Using the formulae in previous chapters these values are obtained:

- L = 1.7uH
- C_{out} = 2x470uF, 1x47uF,1x0.01uF
- C_{ff} = 2.4uF

This optimum value of feed forward capacitor can help to obtain bode plot to observe potential benefits for a closed loop system. Notice that there is a change in phase margin exactly at the frequency required. It has increased at the cut off frequency which now

increases the band width of the system. This improves the stability of the system which can be seen well on the time domain graphs.

In the figure (21), output voltage rail of the converter hardware is displayed. It is taken at an instance of a large change in load (0.5 A to 15 A). On the x axis shows time (ms) and y axis has output voltage (V). Two cases are considered here, one with the Cff (red plot) and other without it (green plot). And it is clearly shown that feed forward cap helps in reducing undershoot, which makes faster transient. Also observe that the green plot has less ripples in the output waveform which in turn helps in reducing the output capacitor values.

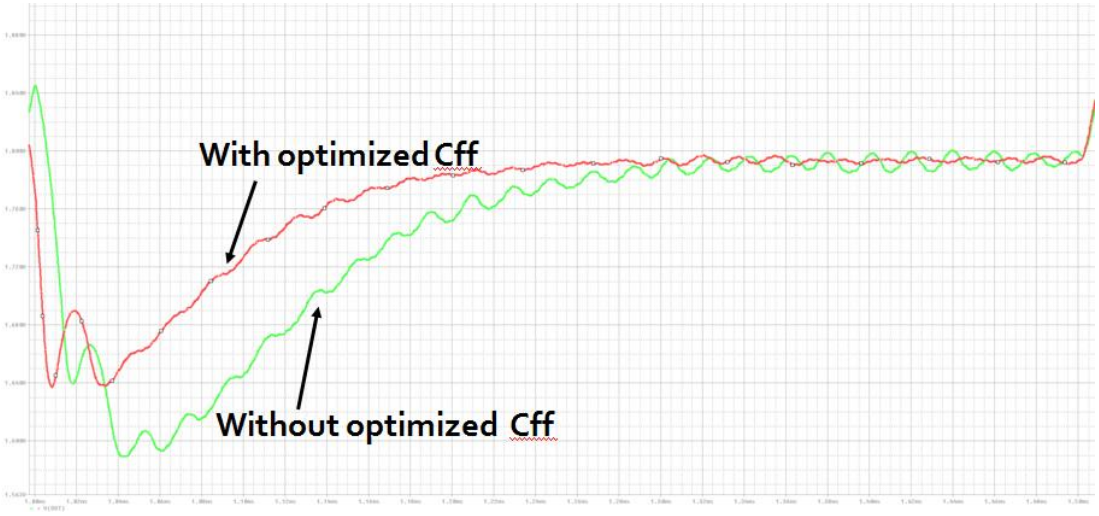

Figure 21. Improvement by using optimized Cff

5.2 MLCC audible noise issue

These kind of tests are done in anechoic chamber with microphones. First the circuit is excited as required and then proper load is provided. At high loads capacitors tend to make noises called as "capacitor sing". Noise is measured in dBA level, usually baseline noise in a quiet room is around 18-20 dBA. Any audible noise in range of 30 dBA from a handheld device or a phone can be disturbing, leading to very bad user experience.

There are few main reasons that contribute to these noises:

1. Amount of solder used
2. Orientation of capacitor

All tests are done in isolation so they do not interfere keeping all other parameters constant. Here is the result for amount of solder used:

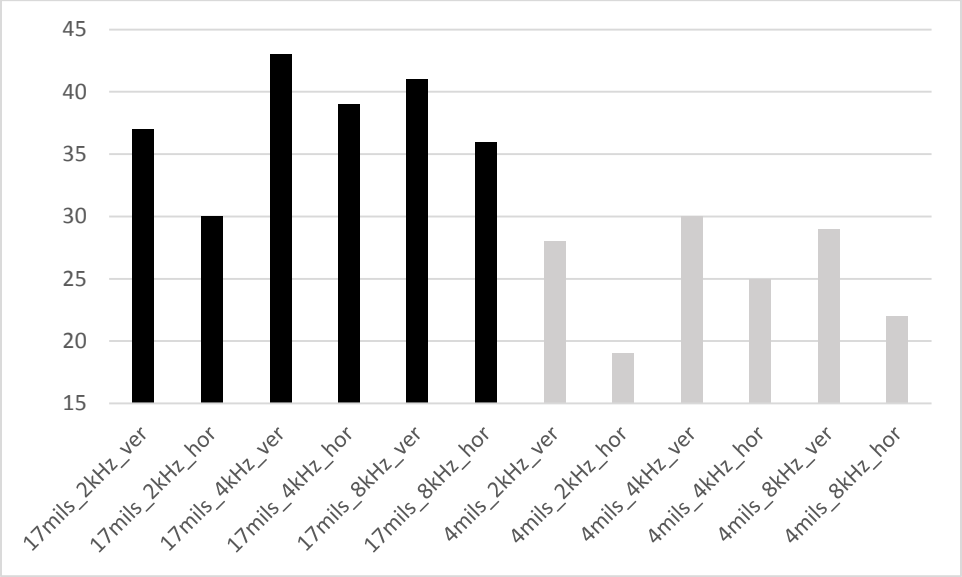

Figure 22. Capacitor acoustic noise w.r.t. solder amount

In figure 22 above the bars marked black represents acoustic noise with more solder (17 mils) used to place down the PCB whereas grey shade represents noise with less solder. Because of less solder and low solder fillet height the cap is not tightly attached to the board which suppresses vibrations to transfer from cap to board, hence reducing very evident audible noise. More the solder, more the vibrations move from cap to board. This leads to an important design specification of choosing the solder stencil thickness for the factory without disturbing the reliability of the product.

Orientation of capacitor is something that is usually ignored in manufacturing process but it decides the alignment of plates of the capacitor. There are about 100 layers

in a MLCC cap package which is closely separated by thin layers of dielectric. Because of ferroelectric material they have piezoelectric behavior and will expand and contract. Now caps can be placed horizontally or vertically with respect to PCB as shown in figure 23. These are the high magnified images from an electron microscope. The capacitor is sliced right through the middle along the length. Point to note is the lateral expansion of layers dominates its orthogonal counterpart which makes vertical plate orientation to hit the PCB board, thus making more noise.

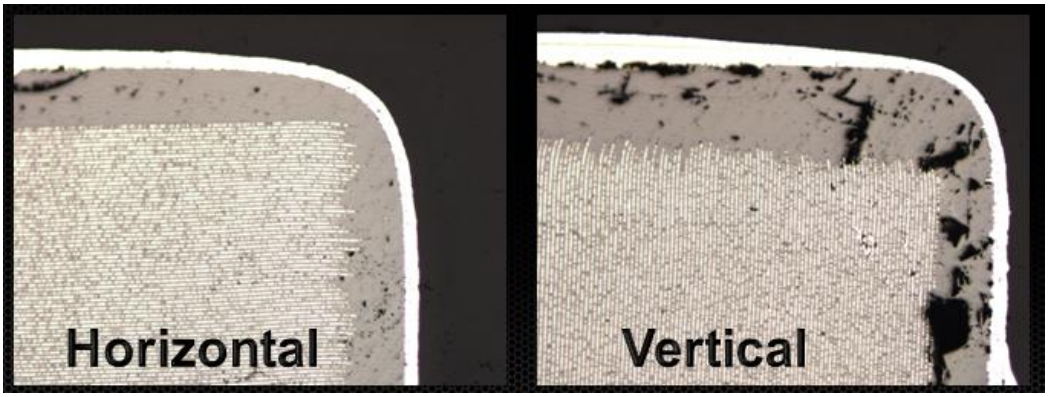

Figure 23. High magnified picture of cross section of capacitor plates [23]

In the figure 24, the bars in black represents horizontal orientation and grey represents vertical. And for each frequency, irrespective of the solder fillet height, the value on y-axis is less for horizontal than vertical. Plates aligned horizontally expands together sideways which is parallel to the board making way less noise than vertical plates where it bulges out and pushes the PCB board at the rate of switching frequency.

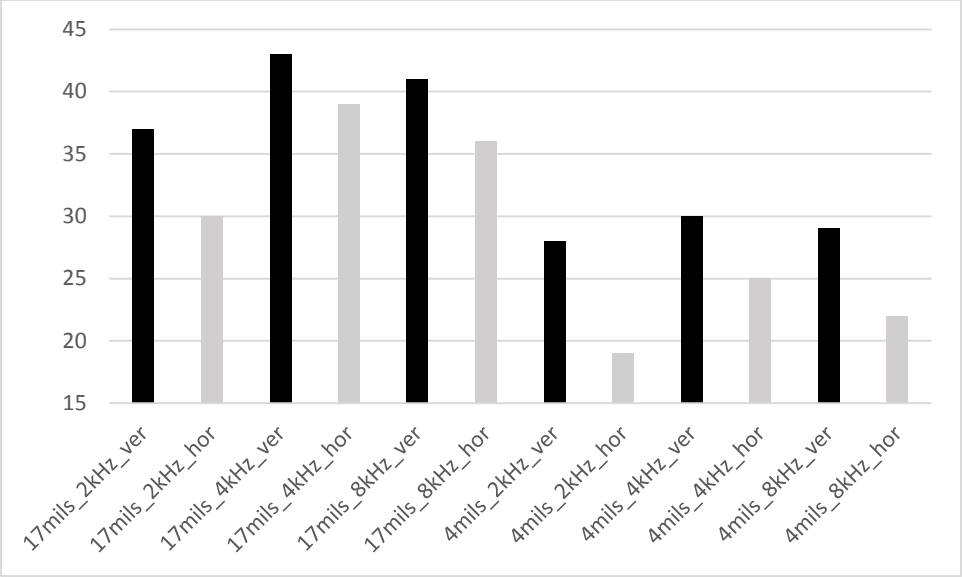

Figure 24. Capacitor acoustic noise w.r.t. orientation of plates

6. Conclusion and Future Work

This thesis addresses some of the problems which concern engineers and designers in the very end of a product design. Both the issues arise after the component selection. It decides the quality of the product and the profit margins for the company. Acoustic noise issue which arises after half of the design cycle is finished that can add up extra validation cost and could increase time to market (TTM). This analysis on capacitor acoustic ensures the designers to use same old and cheap parts and getting better performance without spending more time on validation. On the other hand the analysis on the feed forward capacitor makes converter faster, increases bandwidth and stable to variations in load.

In future, one can plan to conduct more tests on modeling output filter capacitors of different material in a converter and analyzing their effect on output ripple, with a possibility of reducing the number of MLCCs which saves manufacturing costs. Candidates can create PSpice models based on coefficients of materials like tantalum and aluminum etc. and simulate in a practical test environment. Similar analysis can be done for inductors too.

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8. Appendix

List of few industry oriented definitions:

- Point of load (POL) - Unlike SMPS in a cabinet which supplies power to PC components using long and bulky wires, POL system are placed close to their place of usage. It is capable of supplying high peak current and low noise margins.
- Time To Market (TTM) – It is the time required for a complete product cycle from initial design till it is available for sale. Commercial term used by marketing team to plan out the time line for the company.
- Mean time to failure (MTTF) – Time it takes for a product to perform as expected under some defined specification before it stops working. Use to calculate manufacturing efficiency and yield for the company.