Design and Comparison of Passive Component Requirements of a Matrix Converter and Voltage-Source based Back-to-Back Converter

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Dedication

To Mom and Dad for always believing in me

Abstract

A filter is required to eliminate the high frequency switching ripple present in the input current of AC/AC pulse-width modulated (PWM) converters. Design of such filters requires an estimation of the higher harmonic components present in various voltages and currents. Due to pulse-width modulation (PWM), the matrix converter generates switched currents at its input and the back-to-back converter generates switched input voltages which flows distorted currents. This dissertation presents simple closed form analytical expressions for the RMS input current ripple of the matrix converter and RMS input voltage ripple of a DC-link based back-to-back converter. The design of DC-link capacitor in a back-to-back converter requires the estimation of ripple current flowing through it which is also analytically computed. The expressions evaluated are independent of variation of load frequency, output alignment angle, switching frequency, etc. and is a function of known parameters like the modulation indices of the converters, the load and its power factor, DC-link voltage, etc. A systematic step-by-step procedure is presented to design various input filter components from the specifications of allowable THD in the grid current, permissible distortion in the input voltage, allowable inverter current ripple and reactive current drawn by filter capacitor. The converters are modeled for the grid frequency component in order to evaluate the design for input power factor, voltage drop across the filter, maximum possible real power transfer, etc. A damping resistance has been designed ensuring minimum ohmic loss. The analytical estimation of the ripple quantities and the proposed design procedure have been validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.

A comprehensive comparison between the passive filter component requirements of a matrix converter and a DC-link based back-to-back converter is studied under different operating conditions. An input L-C filter of matrix converter is compared with an LCL filter and DC-link capacitor of a back-to-back converter. To compare size, volume and lifetime of passive components, the analysis with a quantitative and qualitative comparison of the passive component values along with their current and voltage ratings is also presented under different load power rating and variation of switching frequency.

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Chapter 1

Introduction

Pulse width modulated (PWM) AC-AC converter systems have become widely used in industry for high power conversion applications. Different converter topologies with and without a DC-link structure have been proposed in literature [1]. Lately the matrix converter (MC) has emerged as a viable solution for direct power conversion, compared to the conventional voltage source based back-to-back connected converter (B-BC). The matrix converter converts three phase AC to three phase PWM AC of desired magnitude and frequency. It uses an array of controlled bidirectional switches to couple a 3-phase grid with a 3-phase load without the need of any intermediate energy storage. This kind of converter can find use in large energy conversion systems like motor drives, variable frequency wind generators, aircraft applications, etc. Its unique properties like bidirectional power flow, single stage power conversion, open loop input power factor correction, regenerative capability and most importantly minimum energy storage requirements which eliminates the bulky DC-link capacitor, give it an upper hand [2] [3] [4]. However currently most of the applications primarily still use the conventional voltage source based back-to-back connected converters for some of their added benefits like voltage boosting capability and ease of use. The matrix converters are still to have a deeper market penetration in the future.

Over the past decade, researchers have been comparing these two converters on various scales like performance, reliability issues, power losses, semiconductor area, passive component requirements, size and volume for different applications. Comparison based on the reliability issues due to voltage stress of the switches is presented in [5]

for aerospace applications. A performance comparison of the two converters shows that matrix converters could be more tangible at high power, high voltage applications [6]. A comparative study of the two was done under open-circuit faults in the power switches [7] looking at the input/output currents THD and motor torque oscillations. A comparison to determine the highest output power based on the thermal stress of the switches is conducted, where it is shown that matrix converters perform better at low output frequencies [8]. A more detailed comparison based on semiconductor power losses is done in [9, 10, 11]. However with advancing technology and emerging power semiconductor devices, device stress and losses might not be the dominating factor. A very important aspect is the volume of the passive components [12]. The passive components affects the weight and volume of the overall converter thus decreasing/increasing cost of equipment.

The matrix converter when invented claimed itself to be an all-silicon solution to AC/AC power conversion because of the absence of a bulky DC-link capacitor. However the modulation of these AC/AC converters injects higher order harmonics into the grid current and input voltage which is harmful. The MC injects harmonic currents and a B-BC produces switched voltages at its input. Extra passive filter components are required to mitigate these harmonic components for safe operation. The MC requires input filters to ensure sinusoidal currents at the grid. An LC filter is generally used to attenuate higher order harmonics in the grid current of the MC. In the B-BC, due to pulse width modulation (PWM) of the VSI (Voltage Source Converter), high frequency switched voltages are generated resulting in distortion of the grid currents. Hence an inductive L filter is generally used to couple it with the grid. However to reduce cost of copper and magnetic material of L, an LCL filter is more often used. The LCL filter results in relaxing the size of the boost inductor (inverter side) and provides better attenuation of the ripple current. The B-BC also has an additional bulky DC-link capacitor to maintain a stable DC-link voltage.

Design of these passive components requires an accurate estimation of different ripple quantities present in different voltages and currents. Along with attenuating the ripple components in the grid current, a properly designed filter must also ensure :

- minimum voltage drop across filter,
- high quality voltage at the converter input in the case of MC, and

- high grid power factor,
- minimum loss in damping resistor,
- low electromagnetic interference

In this dissertation , simple closed form analytical expressions are derived for the RMS ripple quantities in different voltages and currents. A systematic step-by-step design procedure is then presented to calculate the filter components based on certain design specifications. The dissertation then compares the filter requirements of the matrix converter with a back-to-back converter based on analytical estimation of the ripple quantities. An input L-C filter of the matrix converter is designed and compared with an LCL filter and DC-link capacitor of the back-to-back converter. The next section of this chapter presents the current state of the art filter design methods of matrix converter and voltage source inverters. This is followed by the outline and important contributions of this thesis.

1.1 Current state of the art

1.1.1 Filter design of Matrix Converter

A suitable design of the input filter requires an estimation of the input current ripple. Analytical expression for the input current based on the modulation scheme is derived in[13] [14]. However computation of RMS ripple using these methods requires computation with complicated Bessel functions. These expressions also do not clearly show dependence of the input current spectrum on output/load power factor angle. In [15] input current harmonics due to unbalanced grid voltages are analytically evaluated using complex Fourier transforms and approximated by linearizing the input/output equations. In [16] [17] ripple estimation of the input current is done based on a simulation model to design the input filter. In [18] the switching ripple in the input current is approximated to be equal in magnitude to the fundamental component. Thus, no simple analytical expression for the input current ripple exists for a matrix converter.

Different procedures have been proposed to design the passive components of the input filter. In [19], a design for multistage $L-C$ filter based on cost function optimization has been provided using genetic algorithms with different constraints like maximum

amplitude of input current ripple, minimum power factor, maximum losses in damping resistor, maximum distortion in input voltage and stability. In [12] the input filter is designed using a custom developed automated filter design software. In [21] the proposed design is based on fundamental components. Input filter design for other configurations of matrix converter can be found in [22] [23] [24]. Input filter is designed by analyzing the input currents under unbalanced and non-linear loads for an indirect 4-leg matrix converter [22]. Design of a differential mode EMC input filter [23] and a new filter topology aided by a small DC-link second order filter [24] is done for a sparse matrix converter.

A resistance is needed to mitigate oscillations at and around the LC resonance frequency and to improve stability [25] [26] [27]. Modulation based virtual damping techniques, though energy efficient are usually complex and require additional control and cost of sensors [28] [29] [30]. Effective damping by use of a virtual resistor connected in parallel with the capacitor is shown in [28]. Predictive control with an active damping method based on virtual harmonic resistor to mitigate the resonance effect is done for an indirect matrix converter [29] and direct matrix converter [30].

1.1.2 Filter design of Voltage Source Inverters

A proper design of the LCL filter requires an accurate estimation of the inverter's PWM voltage ripple. In [32] [33], the PWM voltage RMS is derived using special Bessel functions. In [34], the inverter voltage ripple is calculated using an approximate harmonic analysis. However above methods require complicated computations using special functions. In [35], the maximum amplitude of inverter ripple current is given through analysis of the current transient process and [36] computes the actual ripple current based on the PWM pattern. However the ripple current derived to use in filter design is itself a function of the filter component L. A simulation model is used to derive the ripple quantities in [17]. Analytical calculation of current stress on the DC-link considering the front end to be a diode bridge is given in [37].

Different design procedures have been proposed in literature for LCL filter based on frequency domain approach [38, 39, 40, 41, 42, 43]. Filter design using generic optimization with different constraints like ripple current in input and grid side, maximum

temperature, maximum filter volume, etc. is done in [44]. To mitigate resonance effects of filter components, active and passive damping schemes have been proposed. Active damping schemes, though energy efficient require additional control complexity [31, 45, 46, 47, 48, 49]. A simpler and more cost effective solution is to use a passive damping technique. Different filter topologies for proper passive damping have been proposed in [50, 51, 52, 53].

1.2 Outline and contributions of the thesis

1.2.1 Input L-C filter design of Matrix Converter

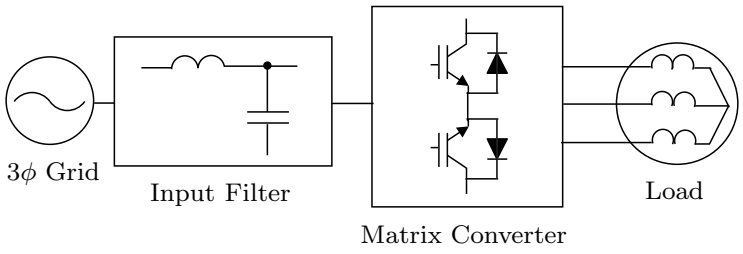


Figure 1.1: Matrix converter based drive with input L-C filter

The matrix converter system with the input L-C filter is shown in Fig. 1.1. The input L-C filter design based on analytical estimation of input RMS current ripple is presented in Chapter 2 [54] [55]. A simple closed form analytical expression for the RMS input current ripple has been derived for the space vector modulation of matrix converters. This expression, by means of basic trigonometric functions includes the effects of the modulation index, the load and its power factor. This eliminates the need for complex calculations using special functions and for using a simulation model to estimate the input current ripple. A step by step design procedure for a single stage L-C filter of matrix converter is presented next. From the analytical estimation of the RMS input ripple current, the MC is modeled for switching frequency component. Analyzing this model the design equations are derived to get the values of the filter components from the specifications of the THD of the grid current and acceptable distortion in the input voltage. A model at the grid frequency is used to evaluate the design for the input power factor, voltage drop across the filter, etc. A passive damping resistor in

parallel with the filter inductor is designed for minimizing LC resonance. The parallel placement is done to minimize power loss, and the resistor value is designed depending on this minimum allowable power loss.

1.2.2 LCL Filter and DC-link Capacitor design of Back-to-Back Converter

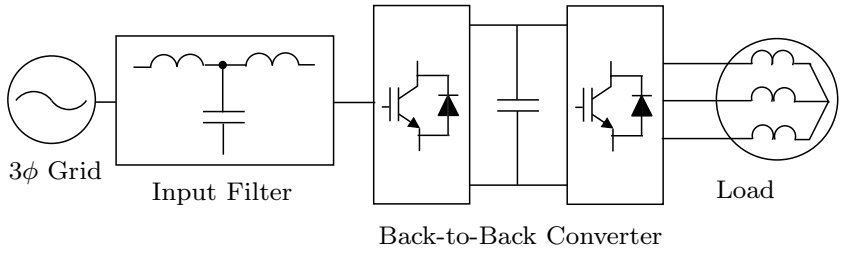


Figure 1.2: Back-to-Back converter based drive with input LCL filter

The back-to-back converter system with the input LCL filter is shown in Fig. 1.2. An LCL filter and DC-link capacitor are designed for the back-to-back converter in Chapter 3 [56] [57]. Simple closed form analytical expression is derived for the input inverter voltage ripple as a function of just the modulation index and DC-link voltage. This is used in a systematic step-by-step design procedure to calculate different filter components. The voltage source based back-to-back converter is modeled for both the fundamental and switching frequency components. Both the components are analyzed independently by the principle of superposition. From this, simultaneous design equations are derived to calculate the filter values based on allowable specifications in inverter current ripple, grid current ripple and reactive current through filter capacitor. A passive damping resistor in series with C is designed for minimum ohmic loss. The DC-link capacitor design needs an accurate estimation of the current stress through it. This is also analytically computed from the modulation theory as a function of the load, its power factor, grid current and modulation indices of the front end and load end converters.

1.2.3 Comparison of Passive Components in MC and B-BC

The designed passive components are compared on various factors in Chapter 4 [57]. The values of passive components obtained from the Chapter 2 and 3 is used in determining the passive component requirements of the two AC/AC converters. The size, volume and lifetime of these passive components depends upon the current and voltage ratings, which is analytically computed. With these data, a comprehensive quantitative and qualitative comparison is presented.

1.3 Summary

In summary, this dissertation presents the passive components design for a matrix converter and voltage source based back-to-back converter by analytical estimation of ripple quantities. Ripple quantities in different voltages and current are analytically derived from the modulation strategy. This is used in a systematic step-by-step design procedure to determine the values of passive components. A comprehensive comparison of the passive component requirements is presented for different operating conditions. The analytical estimation of ripple quantities with filter design is validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.

Note: Part of this chapter is reproduced from my previous publications [54] [55] [56] [57]

Chapter 2

Input L-C filter design of Matrix Converter

2.1 Introduction

The input currents drawn from the 3-phase grid of a MC contain higher frequency components along with the desired line frequency component. A passive L-C filter is used to eliminate these higher order harmonics and to draw high quality currents from the grid [58]. Unlike matrix converters the input filter design of DC-link based AC/AC converters has been extensively studied in the literature [33] [50] [59]. Input filter design for current source inverters can be found in [60] [61]. This chapter describes the systematic filter design for a matrix converter. The designed filter results in high quality grid current, near unity power factor, negligible drop across filter and minimum loss in damping resistor. A suitably designed input filter also ensures 1) negligible drop across filter, 2) high quality voltage at the converter input, 3) near unity power factor [62], 4) significantly reduced electromagnetic interference (EMI) [63], and 5) minimum loss in damping resistor.

The filter design described in this chapter is applicable to both the Direct matrix converter (DMC) and Indirect matrix converter (IMC) topologies as shown in Fig. 2.1. The input filter design described requires modeling of the matrix converter for different frequency components. Modeling of the converter including estimation of the RMS input current ripple depends on the modulation technique. Space vector modulation

(SVM) is the most widely used modulation strategy to achieve highest voltage transfer ratio and optimized switching pattern in a matrix converter [64]. Indirect modulation technique [65] is the commonly used SVM for matrix converters and is considered in this chapter. The following sections describe the basic modulation of matrix converter and its modeling for filter design. Using the models, a step-by-step design procedure for calculating different filter components is presented. The design is validated by simulations in MATLAB/Simulink and experiments on a laboratory prototype.

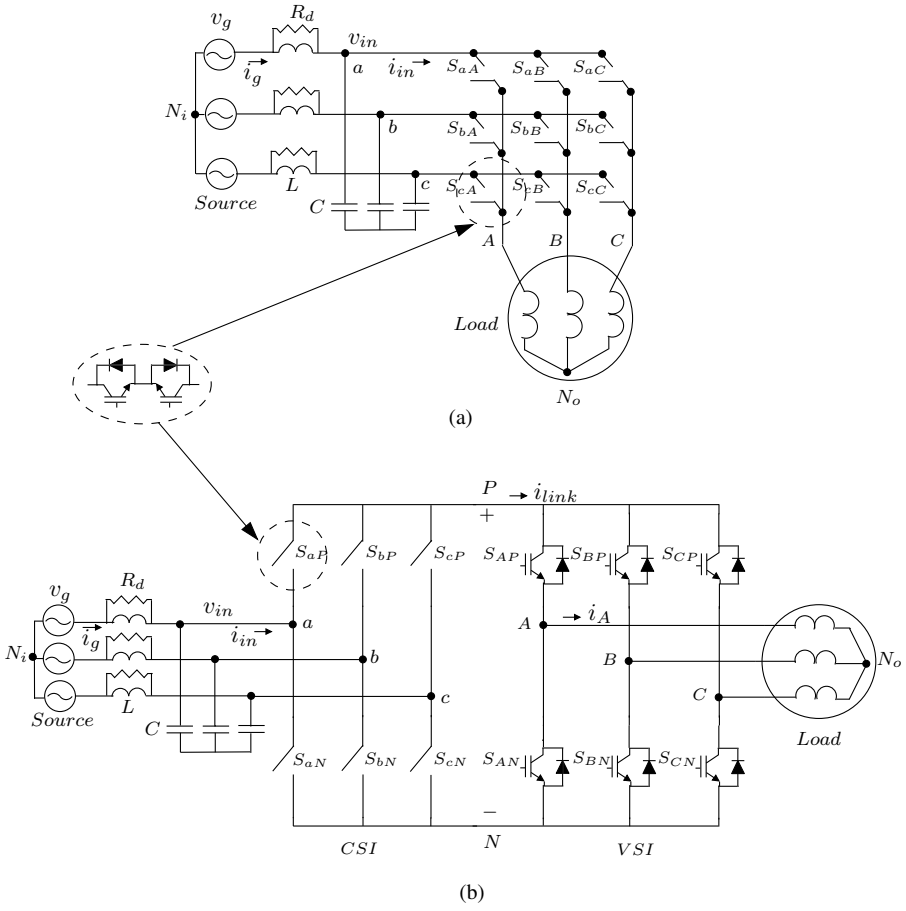


Figure 2.1: (a) Conventional Direct Matrix converter topology (b) Circuit diagram for the Indirect Matrix converter

2.2 Indirect Modulation of Matrix Converter

The indirect modulation technique was first proposed for the indirect MC topology, but is also applicable to the direct MC topology. In indirect modulation, the matrix converter is replaced by two converters as shown in Fig. 2.1(b). The grid side converter acts as a Current Source Inverter (CSI), and the load side converter is modulated as a Voltage Source Inverter (VSI). These two converters are connected through a virtual DC link. The front end converter rectifies input 3-phase utility to a virtual DC, from which the output converter generates balanced 3-phase voltages of desired magnitude and frequency. The CSI stage conducts power in both directions and is made up of four quadrant bidirectional switches in the common emitter configuration. These switches can conduct and block current in both directions which gives the matrix converter the unique feature of bidirectional power flow. The VSI is made up of regular IGBT's with an anti-parallel diode.

The CSI has nine allowable switching states. Each of these states corresponds to one current space vector. In this analysis, space vector corresponding to a set of 3-phase quantities x_a, x_b, x_c is a complex vector X as given in (2.1). The six active and three zero vectors of CSI are shown in Fig. 2.2(a). Here $[a\ b]$ refers to the switching state when switch S_{aP} and S_{bN} are ON. The zero vectors occur when we have $[a\ a]$, $[b\ b]$ or $[c\ c]$ as switching states. Similarly Fig. 2.2(b) shows the six active voltage space vectors of the VSI. [1 0 0] refers to a switching state when the switches S_{AP}, S_{BN} and S_{CN} are ON. The VSI can apply two zero states given by [0 0 0] and [1 1 1]. Both of these hypothetical converters together can produce 18 active switching states of matrix converter. For example, state $[a\ b\ b]$ where a is connected to output phase A, b is connected to output phase B and C respectively can be implemented by simultaneously applying $[a\ b]$ and [1 0 0] in the hypothetical converters.

$$X = x_a + x_b e^{j2\pi/3} + x_c e^{-j2\pi/3} \tag{2.1}$$

In one sampling cycle T_s (carrier frequency of $1/T_s$) the input reference current vector $\overline{\mathbf{I}}_{\mathbf{in}}$ in Fig. 2.2(a) is generated from two adjacent active vectors and one zero vector, whose duty ratios are given by (2.2), where m_I is the ratio of peak of the fundamental component of the input current to the average virtual DC-link current. A rising edge

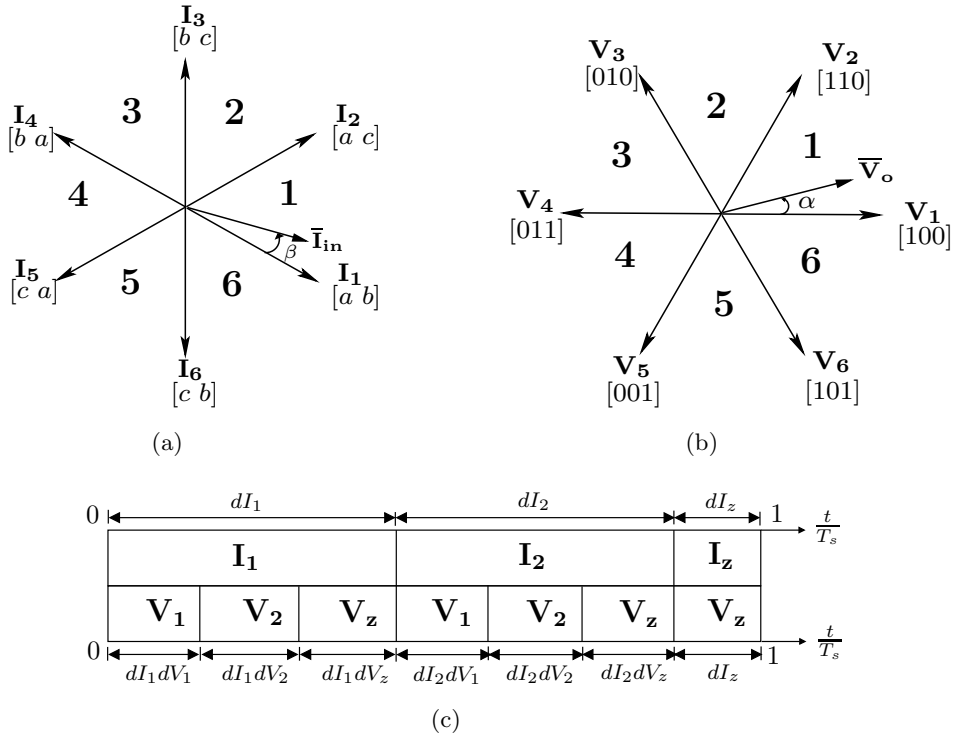


Figure 2.2: (a) Current space vectors produced by CSI (b) Voltage space vectors produced by VSI (c) Switching sequence of Matrix converter

and falling edge saw tooth carrier C1 and C2 is used to determine the time duration's dI_1T_s and dI_2T_s for which the two active current vectors must be applied. The use of two different carriers is made use of to generate non-overlapping pulses.

The output reference voltage space vector $\overline{\mathbf{V_o}}$ in Fig. 2.2(b) is generated by applying two nearest active vectors and a zero vector and their duty ratios are given by (3.1), where m_V is the ratio of peak of the fundamental component of the output voltage to the average virtual DC link voltage. Variable slope carriers C3, C4, C5, C6 are generated depending on the time duration's dI_1T_s and dI_2T_s. Output voltage vectors dV_1T_s and dV_2T_s are compared with these carriers to generate the actual pulses for the matrix converter. The entire modulation scheme and generation of pulses is shown in

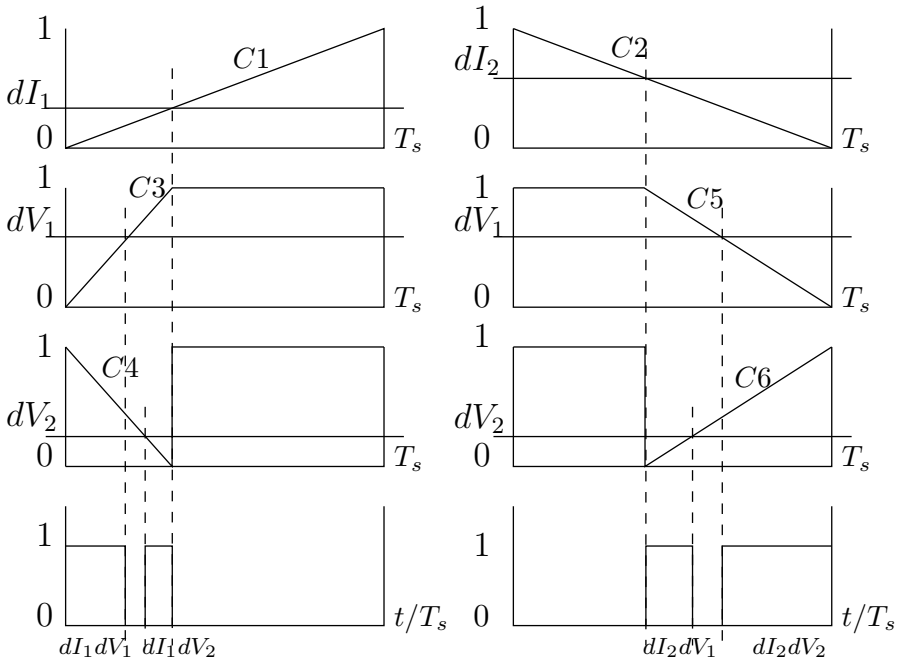


Figure 2.3: Different carriers and generation of gate pulses in indirect modulation of matrix converter

Fig. 2.3. The switching sequence applied over a sampling cycle is given in Fig. 2.2(c).

$$\begin{aligned} dI_1 &= m_I \sin\left(\frac{\pi}{3} - \beta\right) \\ dI_2 &= m_I \sin\beta \\ dI_z &= 1 - dI_1 - dI_2 \end{aligned} \tag{2.2}$$

$$\begin{aligned} dV_1 &= \sqrt{3} m_V \sin\left(\frac{\pi}{3} - \alpha\right) \\ dV_2 &= \sqrt{3} m_V \sin\alpha \\ dV_z &= 1 - dV_1 - dV_2 \end{aligned} \tag{2.3}$$

2.3 Modeling of Matrix Converter for Filter design

To the input filter, the matrix converter appears to be a voltage dependent current source. In this section, the matrix converter is modeled as a current source both for the fundamental and the higher harmonic components (multiples of switching frequency).

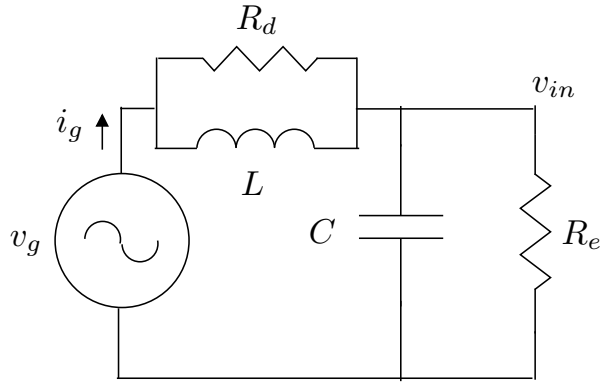


Figure 2.4: Per-phase model at fundamental frequency

The average input current vector is aligned along the input voltage vector in order to get unity power factor. So for the input or source frequency, the matrix converter can be modeled as a resistive load R_e. The peak of the average output voltage V_o can be written in terms of the peak of the input line to neutral voltage V_{in} as in (2.4). Similarly the peak of average input current I_{in} can be written in terms of the peak of output load current I_o as in (2.5) where ϕ_o is the load power factor angle. Using these two equations, the effective resistance of the matrix converter as seen by the input filter can be expressed in terms of the output load impedance ($|Z_L| = \frac{V_o}{I_o}$) as in (2.6), Fig. 2.4.

$$V_o = \frac{3}{2} m_I m_V V_{in} \tag{2.4}$$

$$I_{in} = \frac{3}{2} m_I m_V I_o \cos\phi_o \tag{2.5}$$

$$R_e = \frac{V_{in}}{I_{in}} = \frac{|Z_L|}{(\frac{3}{2})^2 (m_I m_V)^2 \cos\phi_o} \tag{2.6}$$

In order to model the matrix converter for higher order harmonics, the total RMS of the input current is analytically computed. As a first step, it is assumed that the output frequency is same as the input frequency. In order to simplify the computation, it is also assumed that the average output voltage vector was aligned along vector $\mathbf{V_1}$ when

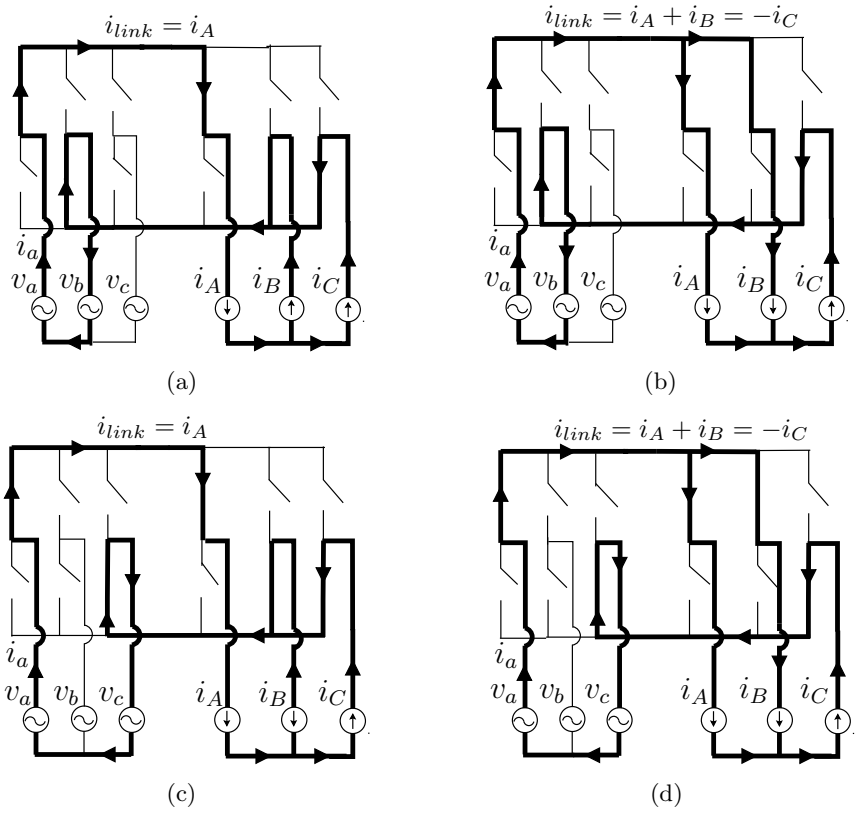


Figure 2.5: Current flow paths for time periods (a) $dI_1dV_1T_s$, (b) $dI_1dV_2T_s$, (c) $dI_2dV_1T_s$, (d) $dI_2dV_2T_s$ in Sector 1

the average input current vector was aligned along vector $\mathbf{I_1}$. Later it is shown from simulation and experimental results that the RMS of the input current computed with the two previous assumptions holds even when (i) the input and output frequencies are different, and (ii) in case of same input and output frequency with a different alignment of average input current and output voltage vectors.

The average (over T_s) output phase A line to neutral voltage and line current are given by (2.7) and (2.8) respectively where V_o and I_o are amplitudes, ω_o is the output frequency and ϕ_o is the load power factor angle. As shown in Fig. 2.2(c), one sampling cycle T_s is composed of time periods $dI_1dV_1T_s$, $dI_1dV_2T_s$, $dI_2dV_1T_s$ and $dI_2dV_2T_s$ when only active vectors are applied. In the following analysis it is assumed that both $\overline{\mathbf{I}}_{\mathbf{in}}$ and $\overline{\mathbf{V}}_{\mathbf{o}}$ are in Sector 1. During time period $dI_1dV_1T_s$, vector $\mathbf{V_1}$ [1 0 0] is applied

by output converter. So the virtual DC-link current i_{link} is same as the output phase A current. The switching state of the input converter during the same period is [a b] corresponding to $\mathbf{I_1}$. So the input phase a is connected to the output phase A through the virtual DC link, Fig. 2.5(a). Similarly during $dI_1dV_2T_s$ period with vectors [a b] and [1 1 0] applied, input line current $i_a = i_A + i_B = -i_C$ as seen from Fig. 2.5(b). Similarly, during $dI_2dV_1T_S$ period $i_a = i_A$ and during $dI_2dV_2T_s$ period $i_a = -i_C$ as shown in Fig. 2.5(c) and Fig. 2.5(d) respectively. Here we assume the output frequency f_o is much smaller compared to the switching or the sampling frequency (f_s=$1/T_s$) of the converter, such that the output currents over a sampling cycle T_s remains constant and can be modeled as current sources.

The square RMS of the input line current i_a over one sampling cycle T_s when both $\overline{\mathbf{I}}_{\mathbf{in}}$ and $\overline{\mathbf{V}}_{\mathbf{o}}$ are in their respective first sectors is given by (2.9). Note due to assumptions made at the beginning of this analysis at any instant both vectors $\overline{\mathbf{I}}_{\mathbf{in}}$ and $\overline{\mathbf{V}}_{\mathbf{o}}$ will be in same respective sectors i.e. when $\overline{\mathbf{I}}_{\mathbf{in}}$ is in sector 2 of Fig. 2.2(a), $\overline{\mathbf{V}}_{\mathbf{o}}$ will be in sector 2 of Fig. 2.2(b). Similarly it is possible to obtain the expressions for the square RMS of the input line current i_a over a sampling cycle when both the input current and output voltage space vector are in their respective second sectors (2.10) and third sectors (2.11). These expressions repeat for other three sectors. (3.7) shows how to relate RMS over one sampling cycle to the RMS over one sector. Assuming the output line currents are balanced and sinusoidal (2.8) and using (2.2), (3.1) and (3.7), it is possible to obtain the RMS of the input line current i_a over one sector. Finally the RMS of i_a over one cycle of the fundamental component of input current can be obtained from the RMS of each sector using (3.8).

Hence the input RMS current is obtained as a function of load power factor and modulation index as in (2.14). The RMS of switching ripple current is obtained by subtracting the RMS of the fundamental component from total input RMS current (2.15). (2.14) and (2.15) provides simple analytical expression for the input RMS current ripple in terms of modulation index, load current amplitude and load power factor angle. Note (2.14) has been derived based on two assumptions mentioned at the beginning of this subsection. It has been shown in the following sections from simulations and experiments that expressions in (2.14), (2.15) are completely general and remain true even when those assumptions do not hold. Fig. 2.6 shows the variation of input RMS

current with change in modulation index and load power factor.

$$\begin{aligned}\overline{v_A} &= V_o \cos(\omega_o t)\\ \overline{v_B} &= V_o \cos\left(\omega_o t - \frac{2\pi}{3}\right)\\ \overline{v_C} &= V_o \cos\left(\omega_o t + \frac{2\pi}{3}\right)\end{aligned} \tag{2.7}$$

$$\begin{aligned}\overline{i_A} &= I_o \cos(\omega_o t - \phi_o)\\ \overline{i_B} &= I_o \cos\left(\omega_o t - \frac{2\pi}{3} - \phi_o\right)\\ \overline{i_C} &= I_o \cos\left(\omega_o t + \frac{2\pi}{3} - \phi_o\right)\end{aligned} \tag{2.8}$$

$$i^2_{a_{RMS,Ts_{SECTOR1}}} = (dV_1 dI_1 + dV_1 dI_2)(i_A)^2 + (dV_2 dI_1 + dV_2 dI_2)(-i_C)^2 \tag{2.9}$$

$$i^2_{a_{RMS,Ts_{SECTOR2}}} = dV_1 dI_1 (-i_C)^2 + dV_2 dI_1 (i_B)^2 \tag{2.10}$$

$$i^2_{a_{RMS,Ts_{SECTOR3}}} = dV_1 dI_2 (i_B)^2 + dV_2 dI_2 (-i_A)^2 \tag{2.11}$$

$$I^2_{a_{RMS_{SECTOR}}} = \frac{1}{\pi/3} \int_{SECTOR} i^2_{a_{RMS,Ts}} d(\omega_o t) \tag{2.12}$$

$$I^2_{a_{RMS}} = \frac{1}{3} \sum_{i=1,2,3} I^2_{a_{RMS_{SECTORi}}} \tag{2.13}$$

$$I^2_{a_{RMS}} = \frac{3\sqrt{3} m_I m_V I_o^2}{\pi^2} \left\{ \left(\frac{\pi\sqrt{3}}{12} + \frac{3}{8} \right) (1 + \cos 2\phi_o) + \left(\frac{\pi}{12} - \frac{\sqrt{3}}{16} \right) \sin 2\phi_o \right\} \tag{2.14}$$

$$I^2_{a_{SWRMS}} = I^2_{a_{RMS}} - \left(\frac{3}{2\sqrt{2}} m_I m_V I_o \cos\phi_o \right)^2 \tag{2.15}$$

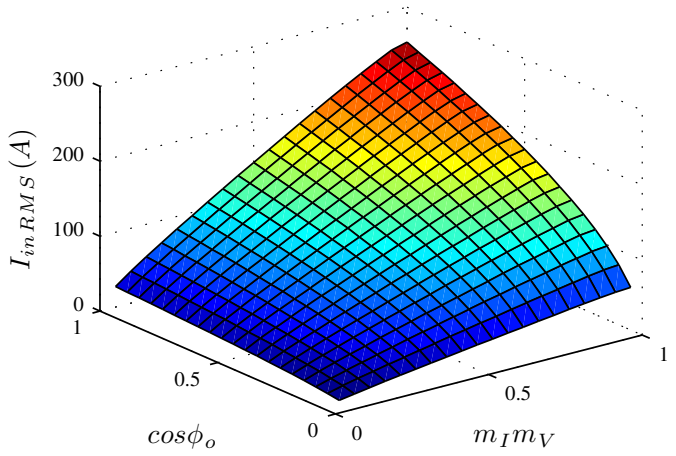


Figure 2.6: Input RMS current with variation in load power factor and modulation index

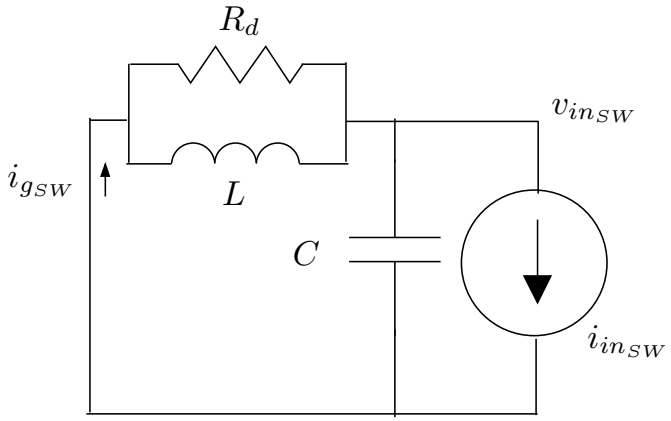


Figure 2.7: Per-phase model at switching frequency

For the ripple component, the matrix converter is modeled as a sinusoidal current source at frequency $1/T_s$ as shown in Fig. 2.7. The RMS of this current source is assumed to be given by (2.15). Due to pulse width modulation the first group of dominant harmonic components in the input current waveform appears to be at and around the sampling frequency f_s. The other harmonic components with appreciable magnitude occurs at and around multiples of sampling frequency. In this model we assume that the entire energy in the input current other than the fundamental is concentrated at

the switching frequency. This results in a slight over design of the filter components.

2.4 Input L-C filter design of Matrix Converter

The matrix converter generates switched discontinuous currents at its input. To obtain smooth continuous sinusoidal currents a passive L-C filter is used. This section presents a step by step design of this filter. In this design, the MC is modeled using the analysis given in the previous section.

In order to mitigate oscillations near the resonance frequency of the L-C network, a damping resistor is introduced in parallel with L. The parallel damping resistor is designed to restrict the power loss to a minimum. As discussed in the previous section, the input current is composed of a fundamental and a ripple component. In what follows, each of these components are considered separately and superposition is applied.

The L-C filter is designed such that the RMS of the ripple component of the grid current, $I_{g_{SWRMS}}$ must be within a limit in order to maintain a particular THD. According to IEEE 519 [66], THD in the grid current must be less than 5%. For the proper operation of the matrix converter, the input voltage of the matrix converter must have a limited amount of higher harmonic ripple, $V_{in_{SWRMS}}$. Analyzing the circuit as shown in Fig. 2.7, it is possible to express both of these ripple components in terms of $I_{in_{SWRMS}}$ (2.16), (2.17). These equations are used to obtain the Bode plots of the transfer functions between different input and output variables of the L-C filter. As can be seen from Fig. 2.8 the magnitude plot of the transfer function between the grid current and the input current of the MC, has a low pass filter characteristics and attenuates everything after the switching frequency f_s. The slight notch in the magnitude plot exists at the resonant frequency of the L-C network. The damping resistor minimizes this resonant peak. The magnitude of the transfer function between input voltage to input current of MC, Fig. 2.9, is also very small near the switching frequency. Analyzing the circuit, for the fundamental component at grid frequency ω_g, it is possible to compute the ratio of the power loss P_{loss} in the damping resistor to the total output power P of the converter (2.18). The power loss is considered only due to fundamental component of the current as most of the higher order harmonics of the input current pass through the filter capacitor. Equations (2.16), (2.17) and (2.18) can be solved simultaneously to

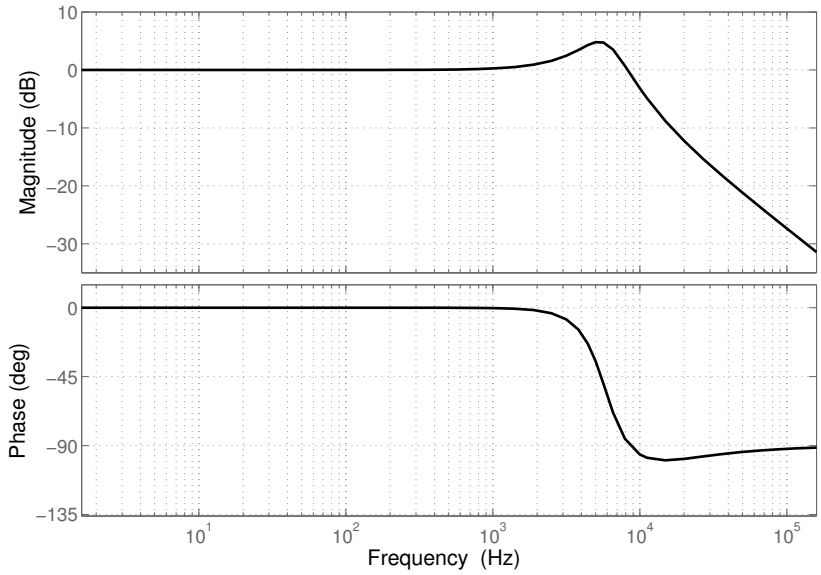


Figure 2.8: Bode magnitude and phase plots of the transfer function between grid current and input current of the MC

determine L, C and R_d.

$$I_{g_{SWRMS}} = \frac{I_{in_{SWRMS}}}{\sqrt{1 + \frac{(1-\omega_s^2 LC)^2 - 1}{\left(1 + \frac{\omega_s^2 L^2}{R_d^2}\right)}}} \tag{2.16}$$

$$V_{in_{SWRMS}} = \frac{I_{in_{SWRMS}}}{\sqrt{(\omega_s C - \frac{1}{\omega_s L})^2 + \frac{1}{R_d^2}}} \tag{2.17}$$

$$\frac{P_{loss}}{P} = \frac{I_{g_{RMS}}}{V_{g_{RMS}}} \left(\frac{\omega_g^2 L^2 R_d}{\omega_g^2 L^2 + R_d^2} \right) \tag{2.18}$$

By analyzing the model at grid frequency, Fig. 2.4, it is possible to check the design. In (2.19), θ_i is the grid power factor angle. It is necessary that the grid current must be drawn close to a unity power factor or the angle θ_i must be close to zero. As shown in Fig.

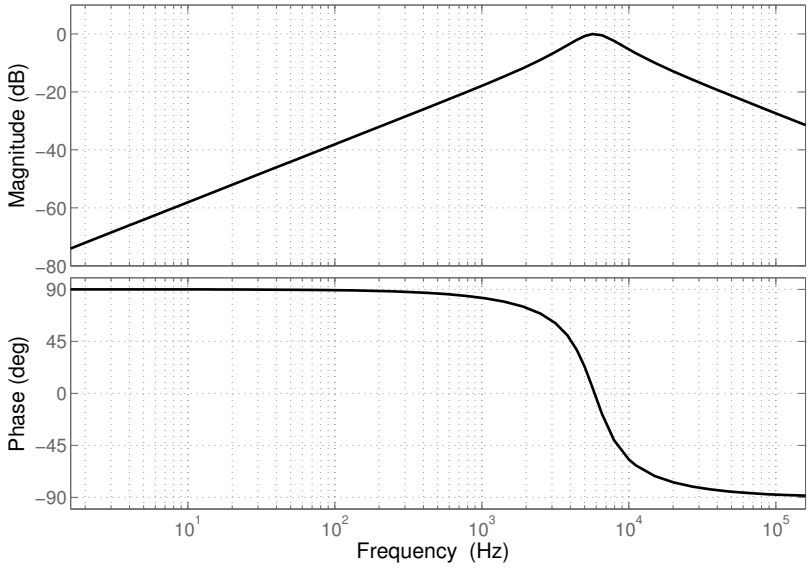


Figure 2.9: Bode magnitude and phase plots of the transfer function between input voltage and input current of the MC

2.10, the phase angle is very close to zero at the fundamental frequency. The voltage drop in the fundamental component across the filter must be negligibly small or the ratio of peak of grid voltage to that of the fundamental component of input voltage of the matrix converter must be close to unity (2.20). If these values are not within appreciable limits then we need to go back and change the specifications and recalculate the values of L, C and R_d. If the grid power factor is below a minimum required power factor pf and does not fall within appreciable limits, then the specification of $I_{g_{SWRMS}}/I_{in1_{RMS}}$ needs to be changed, and if there is a large drop across the filter, specification of $V_{in_{SWRMS}}/V_{g_{RMS}}$ should be modified, and filter parameters are recalculated. The entire design procedure is shown in the flowchart in Fig. 2.11.

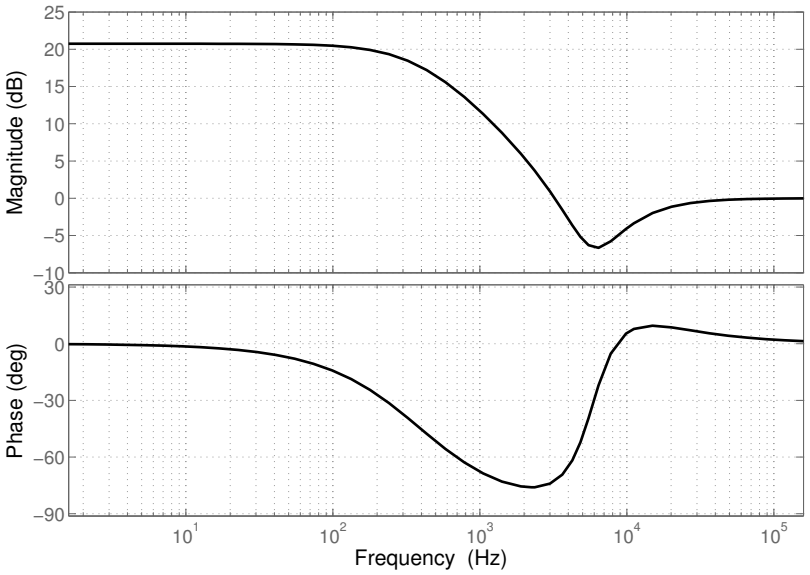


Figure 2.10: Bode magnitude and phase plots of the transfer function between grid voltage and grid current of the MC

$$\theta_i = \tan^{-1} \omega_g C R_e + \tan^{-1} \frac{\omega_g L}{R_d} - \tan^{-1} \frac{\omega_g L(R_e + R_d)}{R_e R_d (1 - \omega_g^2 LC)} \tag{2.19}$$

$$\frac{V_{in}}{V_g} = \frac{R_e \sqrt{R_d^2 + \omega_g^2 L^2}}{\sqrt{\omega_g^2 L^2 (R_e + R_d)^2 + R_e^2 R_d^2 (1 - \omega_g^2 LC)^2}} \tag{2.20}$$

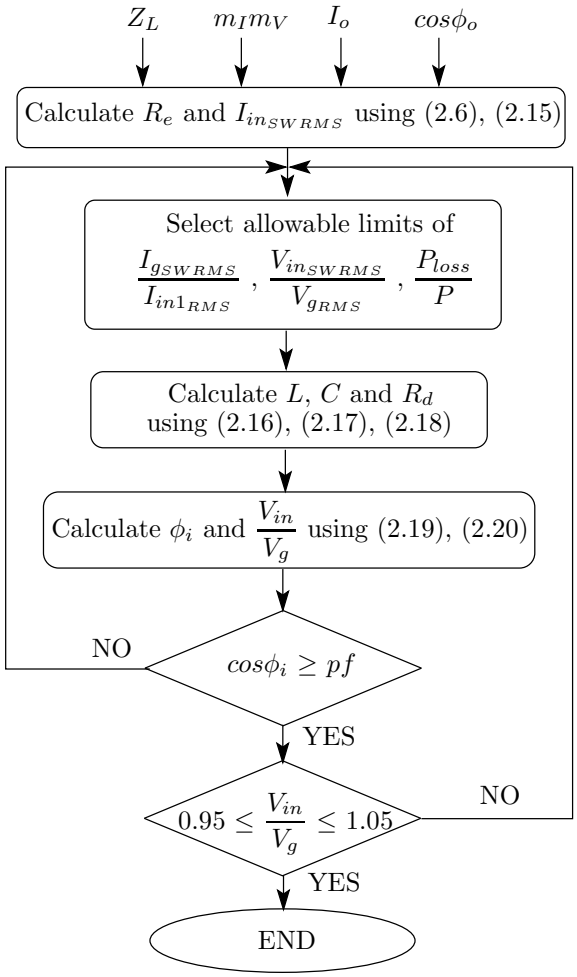


Figure 2.11: Flowchart for filter design of matrix converter

2.5 Simulation Results

The power electronic converter system in Fig. 2.1 with the modulation strategy described in Section II is simulated with ideal switches in MATLAB/Simulink for a medium voltage industrial drive of 1 MW, 3.3 kV line to line RMS (grid voltage). This section presents the simulation results.

The drive supplies a three phase R-L load with switching frequency($1/T_s$) of 10kHz. Different input and output frequencies of 60Hz and 30Hz respectively were selected to

Table 2.1: Simulation Parameters

$V_{s_{LL-RMS}}$	$3.3kV$
f_i	$60Hz$
P_o	$1MW$
$\cos\phi_o$	0.8
m_I	1
m_V	$\frac{1}{\sqrt{3}}$
$f_s = \frac{1}{T_s}$	10kHz
f_o	$30Hz$
L	0.175 mH
C	37.32 μF
R_d	10 Ω
R_e	10.89 Ω

show that the analytical expression (2.14), although derived for same input and output frequencies, remains unchanged otherwise as explained in Section II. Fig. **??** provides $I_{in_{RMS}}/I_o$ as a function of the modulation index and for three load power factors. The simulated points confirm the analytically predicted continuous plots. This verifies the analytical estimation of the RMS input current described in Section II.

For the rest of the simulation results, a *R-L* load of 0.8 power factor at a modulation index of $1/\sqrt{3}$ is considered. The effective resistance R_e of matrix converter is calculated to be 10.89 Ω and the RMS of switching current ripple $I_{in_{SWRMS}} = 127.34$A. The maximum allowable ripple in both the grid current and input voltage are assumed to be 2% of fundamental components and the power loss in damping resistor is restricted to be $3W$. Input filter components $L = 0.175$mH, $C = 37.32\mu$F and $R_d = 10\Omega$ are designed according to Section III. All parameters are shown in Table 2.1. Fig. 2.12(a) shows the output line to neutral voltage and 2.12(b) shows the line currents. Fig. 2.12(c) shows the input voltage and 2.12(d) shows the input current of phase a of the matrix converter. Frequency spectrum of various voltage and current waveforms are plotted in Fig. 2.13. From the FFT plot, it is evident that the voltage drop across the filter is negligibly small and the input voltage to the matrix converter is almost sinusoidal. The

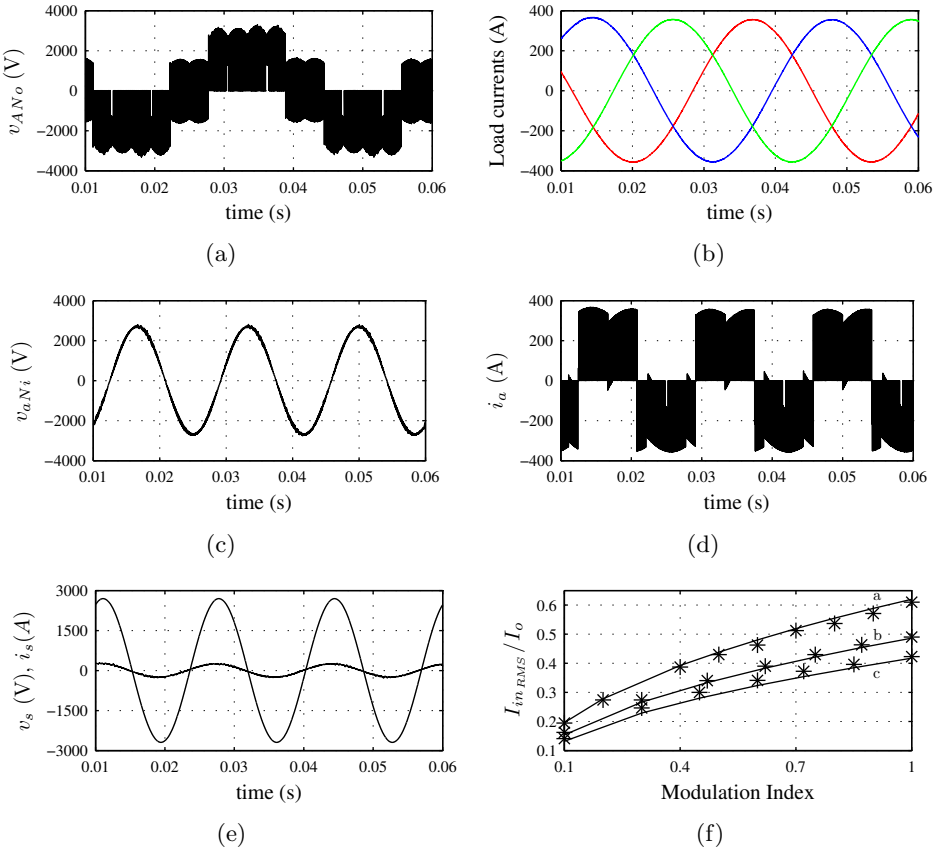


Figure 2.12: (a) Output line to neutral voltage, (b) Output line current. (c) Input line to neutral voltage, (d) Input line current, (e) Filtered grid voltage and current, (f) Variation of input RMS current with modulation index and load power factor ($\cos\phi_o$ a: 0.8, b: 0.6, c: 0.5)

input current RMS obtained from simulation is 216.20A which very closely matches the analytical value of 216.38A. Fig. 2.12(e) shows the grid voltage and corresponding line current. It can be seen that the line current is almost in phase with the voltage and nearly sinusoidal ($cos\phi = 0.9973$) which is confirmed by the frequency spectrum.

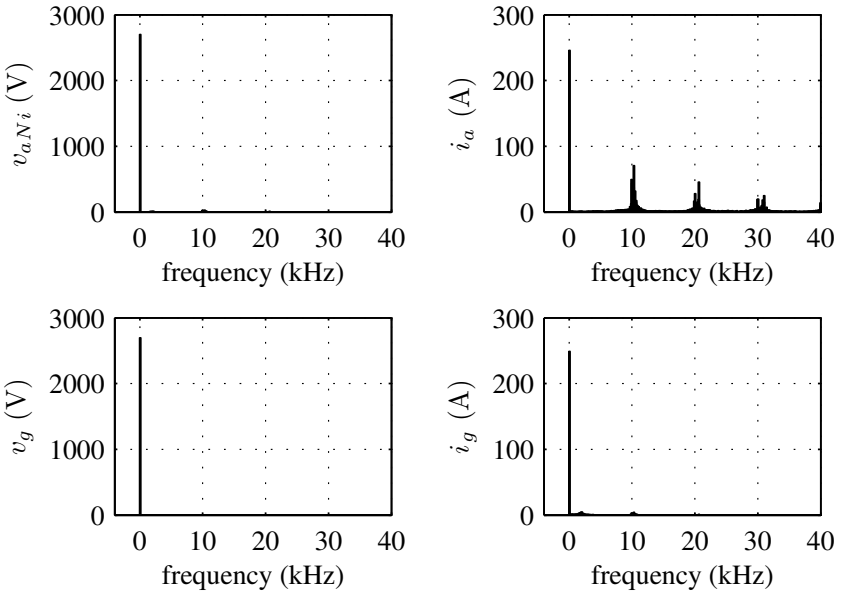


Figure 2.13: Simulation result: Frequency spectrum

2.6 Experimental Results

A scaled down laboratory prototype of the matrix converter system is developed as shown in Fig. 2.14 and important experimental results are presented in this section.

The matrix converter is implemented with an indirect topology as shown in Fig. 2.1(b). Integrated power module APTGT75TDU120PG and APTGT75A60T1G from Microsemi is used to implement the CSI and VSI respectively. IGBT driver 2SD106AI from CONCEPT uses a 15V DC supply to generate isolated ±15V gate pulses using digital/PWM signals coming from a FPGA. The entire modulation strategy is coded in verilog onto a control platform based on FPGA from Xilinx XC3S500E. A measurement board containing Hall effect voltage(LV25-P) and current sensors(LA55-P) followed by a Sallen key filter provides the output currents and input voltage measurements to the FPGA. The input voltage used for the experiment is 50V, line to neutral RMS at 60 Hz. The modulation index used are $m_I = 0.8$ and $m_V = 0.46$. The PWM switching frequency $(1/T_s)$ is set at 5 KHz. Output 3-phase sinusoidal currents are

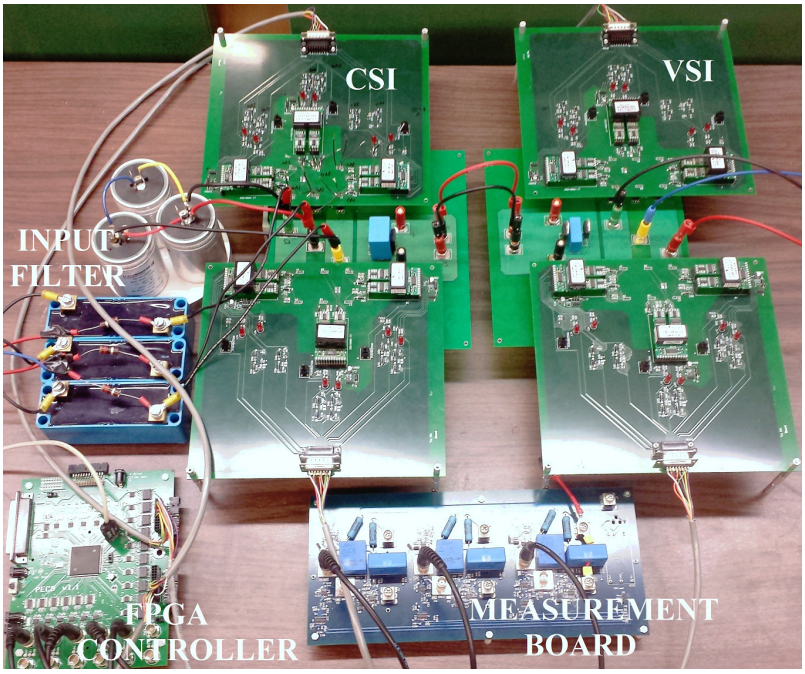


Figure 2.14: Hardware setup

generated at 30Hz across a R-L load with parameters: $R_{load} = 5.4\Omega$ and $L_{load} = 28mH$, $cos\phi_o = 0.72$. Using (2.6) and (2.15) it is possible to obtain matrix converter effective resistance of 34.37 Ω at 60Hz and RMS of input switching current ripple of $I_{in_{SWRMS}}$ = 1.77A respectively. The input filter parameters are calculated from Section III for allowable ripple of 2% in grid current and input voltage and power loss in damping resistor 2×10^{-5}% of total power. The designed values are L= 0.47mH, C= 36.2μF and $R_d = 12\Omega$. For the experiments, a 0.5μH and current rating of 25A power line choke B82506-W-A6 from EPCOS is used. AC capacitors E62-K85-223D10 from Electronicon of value 22μF and voltage rating 750VAC are star-connected. Also AC film capacitors ECQU2A225KL from Panasonic of rating 2.2μF, 275 VAC are cascaded in parallel to form 4.4μF and connected in delta. This effectively makes $3 \times 4.4 = 13.2\mu$F in star connection which results in a total filter capacitance value of 35.2μF. The power loss across the damping resistor calculated from Section II is approximately 2×10^{-4}W. Hence a 0.5W, 12Ω resistor was used to damp the oscillations. The current and voltage ratings of all semiconductor devices and passive components is chosen to be much higher

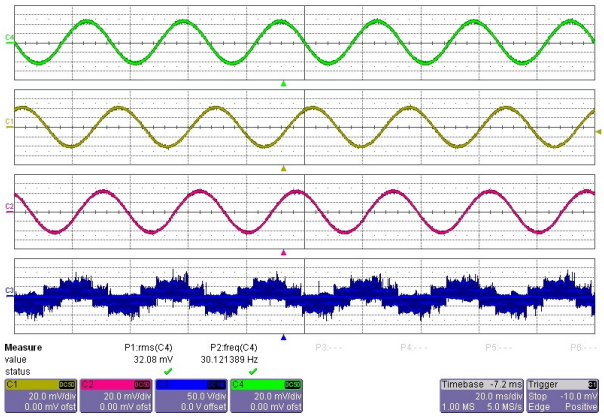


Figure 2.15: Three output line currents (2 A/div) and output line to neutral voltage (50 V/div) of one phase for R-L load

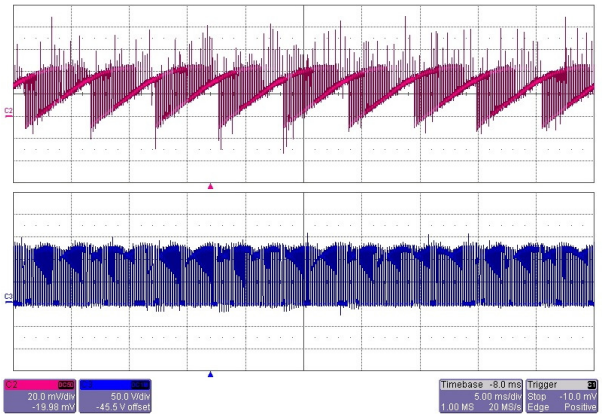


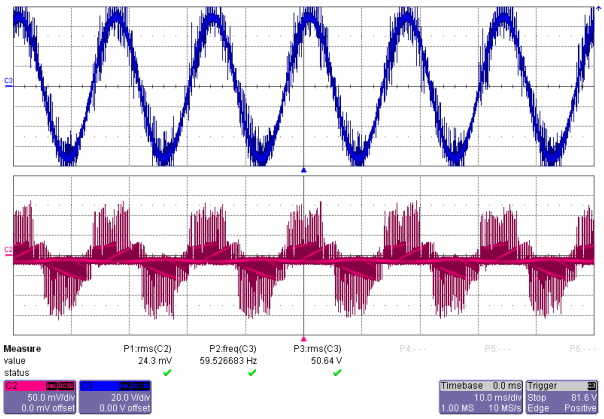
Figure 2.16: (top) DC link current (2 A/div), (bottom) DC link voltage (50 V/div)

than our operating conditions.

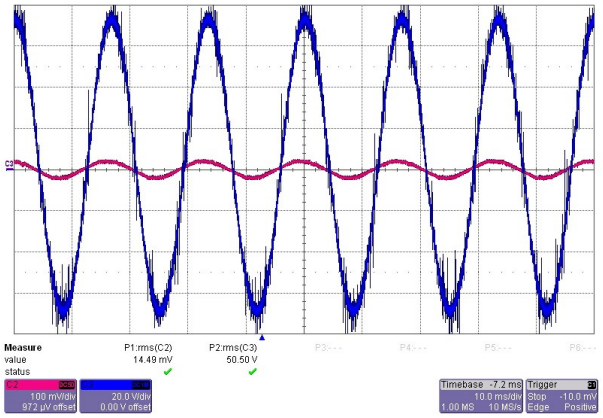
As opposed to the simulation model which used ideal switches and no commutation strategy, here we implement 4-step commutation of the input and output converters, A gate resistor of 18Ω is used to set the difference in ON times and OFF times to be 550 nsec. Hence the delay in various stages of 4-step commutation is selected to be 0.6μsec. During the 4-step commutation period, the current does not have a path to flow. A diode bridge based clamp circuit is hence used. These passive clamp circuits are connected during the commutation duration, and they also exist for protection. The clamp circuit is a basic diode bridge with a parallel capacitor and resistor. Two clamp

circuits are used: one on the input AC side ($C_{cl} = 15\mu F$, $R_{cl} = 10K\Omega$) and other across the DC link ($C_{cl} = 2.2\mu F$, $R_{cl} = 3K\Omega$). Also to maintain the diode bridge reverse biased under normal operation, a DC voltage of 150V is externally applied.

Fig. 2.15 shows 3-phase output line currents and line to neutral voltage of one phase at 30Hz. The experimental waveforms have a slightly lower current magnitude of 4.54A as compared to its analytical value of 5.19A. This can be attributed to the voltage drops across the semiconductor devices. Fig. 2.17(a) shows the input line to neutral voltage and switched line current of one phase. The RMS value of input current is 2.4A. The analytically calculated RMS value is 2.3A from (2.14) which closely matches the experimental value. The grid voltage and line current are shown in Fig. 2.19. This confirms almost unity power factor correction. The grid current is almost sinusoidal. The frequency spectrum of the four input side waveforms are shown in Fig. 2.18. As can be seen the fundamental component of the input voltage of the MC and grid voltage are almost equal. Thus there is negligible drop across the filter. Also the THD content in the grid current is very small which validates the filter design procedure. The FFT waveforms are taken at 2MS/sec to capture enough data points to plot the FFT. The total number of data points over which FFT is computed as set by the scope is N= 2^{15}. Hence for a frequency of 60Hz, the sampling frequency required is $f \times$N= 2MS/sec. The DC link current and voltage are shown in Fig. 2.16. The DC link current has some spikes which is because of the reverse recovery of the antiparallel diodes in the secondary side converter.



(a)



(b)

Figure 2.17: (a) (top) Input line to neutral voltage (20 V/div), (bottom) Input line current (5 A/div) for R-L load (b) Grid side per-phase voltage (20 V/div) and filtered line current (10 A/div) for R-L load

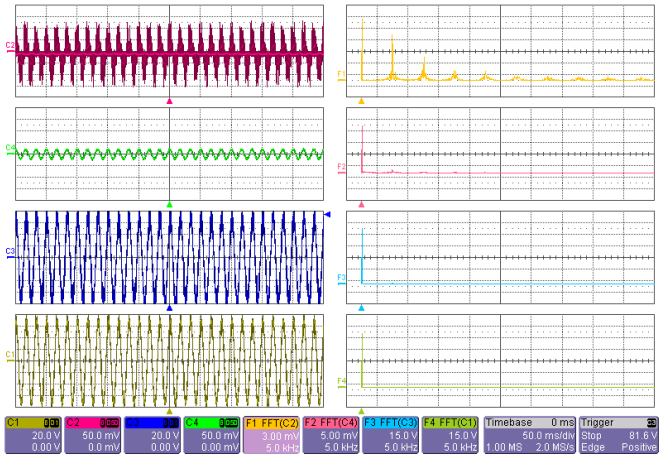
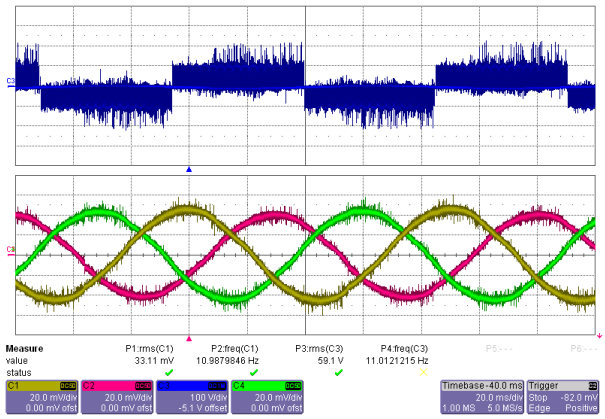


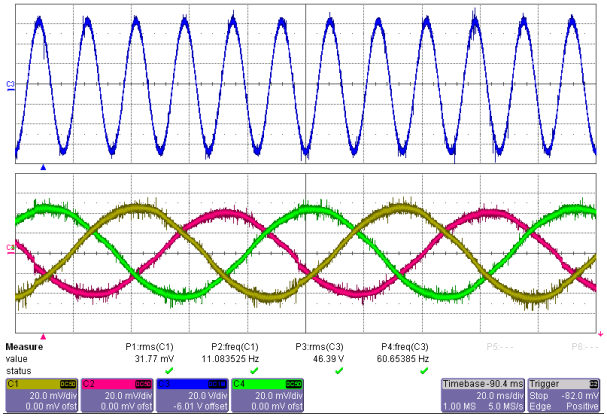
Figure 2.18: Frequency spectrum with corresponding signals : (top) Input line current (5 A/div) and FFT, (second from top) filtered grid current (5 A/div) and FFT, (third from top) input line to neutral voltage (20 V/div) and FFT, (bottom) grid line to neutral voltage (20 V/div) and FFT. (Sampling frequency: 2 MS/sec)

A 1 hp, three phase 230/460V, 60 Hz, 4 pole induction motor is run by the matrix converter under V/f (ratio of amplitude of line to neutral voltage to the frequency) control. The output frequency is set at 11Hz. For an input line to neutral voltage of 40V RMS and same modulation index, the matrix converter generates 31.35V at the output. The induction machine was loaded with a permanent magnet DC generator (1 hp, 180V) feeding a resistive load of 5Ω. The induced emf e of the generator is given by $e = K\omega$ where $K = 1$ and $\omega = (2\pi f_o) \times 2/p$. Here slip is neglected and p is the number of poles and ω the rotor speed in mechanical radians. Assuming both the machines to be lossless and neglecting any drop, the reflected component of rotor current is along input voltage and is given by (2.21). The no load magnetizing current of the induction motor is 1.8A (peak). Hence the amplitude of the resultant output load current comes out to be 5.37A. The actual current is 4.67A in magnitude as seen in Fig. 2.19(a). The load line to line voltage is also shown in Fig. 2.19(a). The input voltage with load currents is shown in Fig. 2.19(b) which shows the difference in frequency under V/f control. The filtering action of input current is shown in Fig. 2.19(c).

$$I_r = \frac{e^2}{3/2 V_o R} \tag{2.21}$$



(a)



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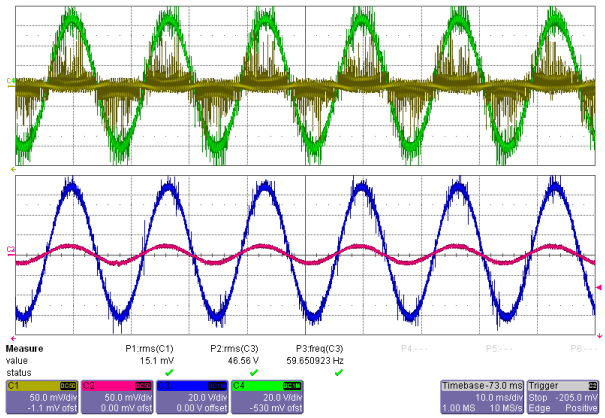


(c)

Figure 2.19: (a) (top) Output line to line voltage (100 V/div), (bottom) three line currents at motor terminal (2 A/div) (b) (top) Supply side line to neutral voltage (20 V/div), (bottom) three line currents at Motor terminal (2 A/div) (c) (top) Per phase input voltage (20 V/div) and line current (5 A/div), (bottom) Filtered grid side voltage (20 V/div) and current (5 A/div) for Induction Motor load

The system was run at different output frequencies with same 60Hz input frequency and the input RMS current was measured and is shown in Fig. 2.6 (top). Then the system was run for the same output frequency but different output alignment angles and results are shown in Fig. 2.6 (bottom). This was done maintaining all other parameters constant and the input current RMS remains constant regardless of the two parameters as explained in Section II.

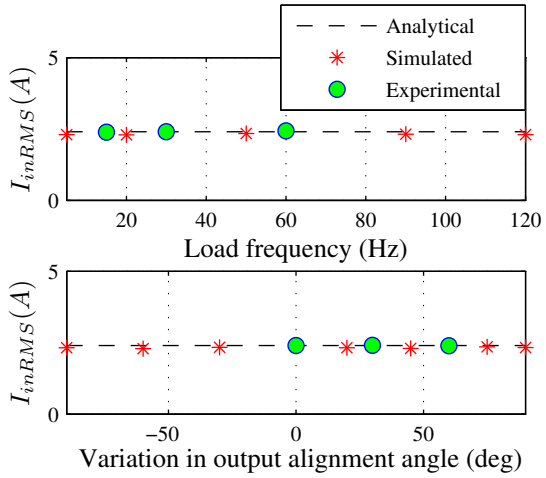
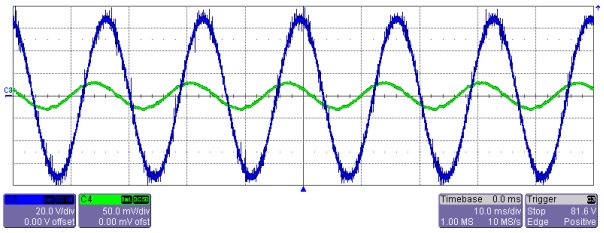
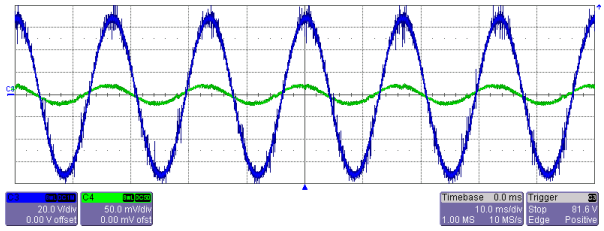


Figure 2.20: Variation of Input RMS current with output frequency (top) and output alignment angle (bottom)

The system was run with different set of filters for different allowable ripple specifications in the grid current. Fig. 2.21 shows the grid line to neutral voltage and grid current for allowable THD= 1% (L= 0.5mH, C= 77μF), THD= 2.5% (L= 0.5mH, C= 26.4μF) and THD= 5% (L= 0.5mH, C= 13.2μF). The resulting input power factor obtained is 0.904, 0.983 and 0.996 respectively. This implies that with the reduction in amount of allowable ripple in grid current for a fixed switching frequency, the inductance remains almost the same and capacitance increases resulting in reduction in grid power factor, Fig. 2.22.



(a)



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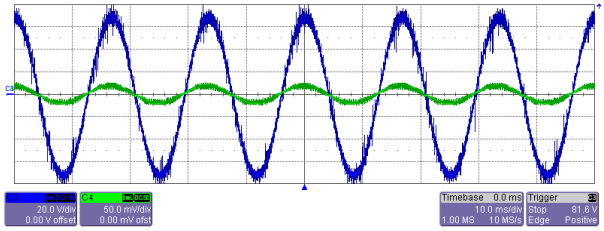


(c)

Figure 2.21: (a) grid voltage (20 V/div) and current (5 A/div) for allowable THD= 1.0%. (b) grid voltage (20 V/div) and current (5 A/div) for allowable THD= 2.5%. (c) grid voltage (20 V/div) and current (5 A/div) for allowable THD= 5.0%

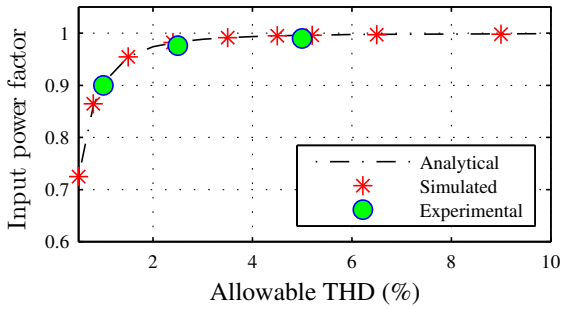


Figure 2.22: Variation of input power factor with allowable THD limit

2.7 Conclusion

A step-by-step design procedure to determine the input L-C filter components for a matrix converter is presented. An analytical approach to estimate the input RMS ripple current for the converter is presented based on conventional space vector modulation theory. This computation is independent of the ratio of the input to the output frequency, and depends only on the modulation index, the load and its power factor. The converter is modeled for different frequency components and simultaneous design equations are derived to calculate the L-C values based on specifications of allowable ripple in grid current and distortion in input voltage. The designed filter meets the THD specifications and ensures near unity power factor, negligible drop across it and minimum loss across the damping resistor. The matrix converter is simulated and a hardware prototype is built to verify the filter results.

Note: Part of this chapter is reproduced from my previous publications [54] [55]

Chapter 3

LCL Filter and DC-link Capacitor design of Back-to-Back Converter

3.1 Introduction

The back-to-back converter (B-BC) generates switched voltages at its input resulting in distortion of the grid currents. An inductive L element is required to provide attenuation of this voltage ripple. To relax the size of the basic L filter, an input LCL filter is more used to provide the required attenuation of harmonic components and obtain smooth continuous currents at the grid. The filter design requires modeling of the B-BC for the fundamental frequency and higher frequency components. For the switching frequency component, the RMS of the inverter voltage ripple is analytically computed. By the principle of superposition, both these components can be independently analyzed. Conventional space vector modulation is similar, but allows higher voltages to be synthesized, in comparison to the sine-PWM method. Therefore, it is only the conventional space vector modulation method that is considered in this chapter. Based on the analytically calculated ripple voltage amount and certain specifications in grid current, input current and reactive current limits, the input LCL filter parameters can be calculated.

The DC-link capacitor design requires the amount of current ripple flowing through it which is also analytically computed. The following sections describe the basic modulation, control and modeling of B-BC for filter design. A systematic filter design

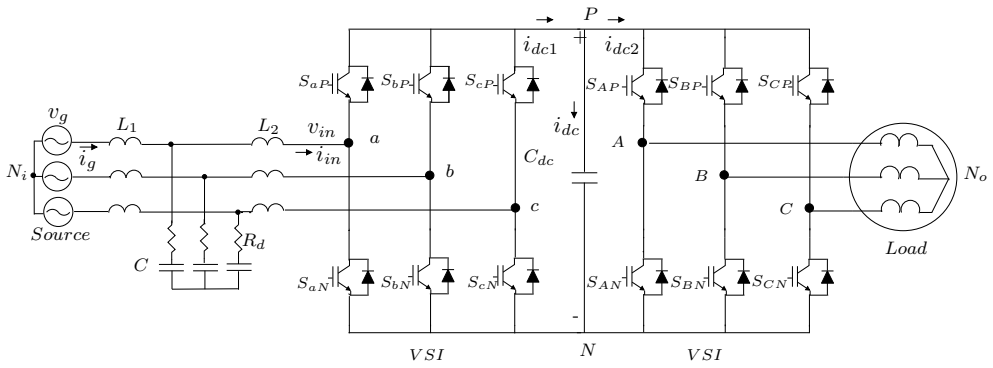


Figure 3.1: Topology : Back-to-Back Converter

procedure is then explained, followed by extensive simulation and experimental results for verification.

3.2 Modulation and Control

The back-to-back converter is composed of two voltage source inverters (VSI) connected in a back to back fashion with a DC-link capacitor as shown in Fig. 3.1. Each converter acts as an independent VSI and is modulated using the six active voltage space vectors as shown in Fig. 3.2(a) and Fig. 3.2(b) respectively. Considering the front end VSI, the reference voltage vector $\overline{\mathbf{V}}_{\mathbf{in}}$ is generated from two adjacent active vectors and one zero vector whose duty ratios are given by (3.1) where m_{V1} is the ratio of peak of the fundamental component of the input voltage to the DC-link voltage V_{dc} and α_1 is the angle between the first vector and $\overline{\mathbf{V}}_{\mathbf{in}}$. Similarly the load end converter is modulated by duty ratios as shown in (3.2) where m_{V2} is the ratio of peak of the fundamental component of the output voltage to the DC-link voltage V_{dc} and α_2 is the angle between the first vector and $\overline{\mathbf{V}}_{\mathbf{o}}$. The switching sequence applied over a switching cycle T_s in the front-end and load-end converter is as shown in Fig. 3.2(c).

$$\begin{aligned} dV_{11} &= \sqrt{3} m_{V1} \sin\left(\frac{\pi}{3} - \alpha_1\right) \\ dV_{21} &= \sqrt{3} m_{V1} \sin \alpha_1 \\ dz_1 &= 1 - dV_1 - dV_2 \end{aligned} \tag{3.1}$$

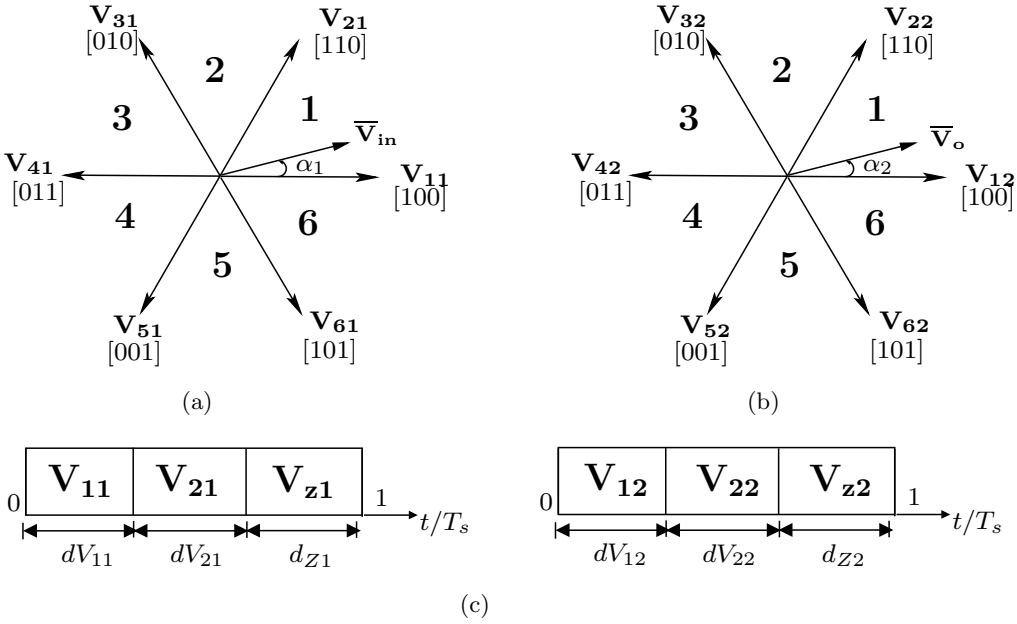


Figure 3.2: (a) Voltage space vectors of front end converter (b) Voltage space vectors of load end converter (c) Switching sequence of back-to-back converter

$$\begin{aligned} dV_{12} &= \sqrt{3} m_{V2} \sin\left(\frac{\pi}{3} - \alpha_2\right) \\ dV_{22} &= \sqrt{3} m_{V2} \sin \alpha_2 \\ dz_2 &= 1 - dV_1 - dV_2 \end{aligned} \tag{3.2}$$

The DC-link voltage is maintained constant with a closed loop control as described in [67]. It is based on the conventional vector control scheme used in electrical machines. An outer voltage loop maintains the DC-link voltage (V_{dc}) and two inner current loops control the real and reactive power flow between the DC-link and the grid. The 3-line currents are converted into their corresponding $d-q$ coordinates which result in dc-quantities. The $d-$component of the line currents is directly proportional to the real power flow, and $q-$components determines the reactive power flow. By just transferring real power demanded by the load, unity power factor is maintained at the grid. Thus i_q is made zero resulting in grid power factor correction.

3.3 Modelling of back-to-back converter for filter design

The modulation of the back-to-back converter generates switched voltages at its input v_{in}. To the input filter the back-to-back converter appears as a voltage source for both the fundamental and switching frequency components. In this section, the modeling of the B-BC for filter design is presented.

The instantaneous input phase voltage referred to grid neutral N_i can be expressed in terms of three instantaneous phase voltages referred to the negative DC link N (3.3). Fig. 3.3 shows three input phase to negative DC-link voltages and one input phase a to neutral voltage v_{aN_i}. Considering conventional space vector pulse width modulation, over one sampling cycle in the first sector, the instantaneous input line to neutral voltage is composed of levels $2V_{dc}/3$ and $V_{dc}/3$ as shown in Fig. 3.3. One sampling cycle T_s is composed of time periods $dV_{11}T_s$ and $dV_{21}T_s$ for the front-end converter. The DC-link voltage is assumed constant. In the first sector, during $dV_{11}T_s$ interval, when vector $\mathbf{V_{11}}$ [1 0 0] is applied, switches S_{aP}, S_{bN} and S_{cN} are ON. Hence the voltage applied across input phase a referred to DC-link negative is V_{dc}. The instantaneous input phase a voltage referred to grid neutral is $2V_{dc}/3$ ($v_{aN_i} = \frac{1}{3}(2V_{dc} - 0 - 0)$, Fig. 3.3. Similarly for $dV_{21}T_s$, when [1 1 0] is applied, $v_{aN} = V_{dc}$. Thus the instantaneous input phase a voltage $v_{aN_i} = V_{dc}/3$. Hence the RMS square of input line to neutral voltage over one sampling cycle in the first sector is given by (3.4). Similarly it is possible to obtain the expressions for the RMS square of inverter voltage over a sampling cycle in second and third sectors as given by (3.5) and (3.6) respectively. This is shown in Fig. 3.3(b) and Fig. 3.3(c) respectively. The computation repeats for the remaining sectors. Now the square RMS of input voltage over a sector is found by (3.7) where ω_g is the grid frequency. Assuming the DC-link voltage is constant and using (3.1), (3.2) the input RMS voltage over one fundamental cycle is found from the RMS of each sector (3.8) as a function of the modulation index m_{V1} (3.9) of the front-end converter. The ripple voltage needed for filter design is obtained by subtracting the square of fundamental component of input voltage from total RMS square voltage (3.10).

$$v_{aN_i} = \frac{1}{3}(2v_{aN} - v_{bN} - v_{cN}) \tag{3.3}$$

$$v^2_{aN_{iRMS,Ts_{SECTOR1}}} = dV_{11}\left(\frac{2V_{dc}}{3}\right)^2 + dV_{12}\left(\frac{V_{dc}}{3}\right)^2 \tag{3.4}$$

$$v^2_{aN_{iRMS,Ts_{SECTOR2}}} = dV_{11}\left(\frac{V_{dc}}{3}\right)^2 + dV_{12}\left(\frac{-V_{dc}}{3}\right)^2 \tag{3.5}$$

$$v^2_{aN_{iRMS,Ts_{SECTOR3}}} = dV_{11}\left(\frac{-V_{dc}}{3}\right)^2 + dV_{12}\left(\frac{-2V_{dc}}{3}\right)^2 \tag{3.6}$$

$$V^2_{aN_iRMS_{SECTOR}} = \frac{1}{\pi/3}\int_{SECTOR} v^2_{aN_{iRMS,T_S}} d(\omega_g t) \tag{3.7}$$

$$V^2_{aN_iRMS} = \frac{1}{3}\sum_{i=1,2,3} V^2_{aN_iRMS_{SECTORi}} \tag{3.8}$$

$$V^2_{aN_iRMS} = \frac{2\sqrt{3}m_{V1}}{3\pi}V^2_{dc} \tag{3.9}$$

$$V^2_{aN_{iSWRMS}} = \frac{2\sqrt{3}}{3\pi}mV^2_{dc} - V^2_{inRMS} \tag{3.10}$$

The model at switching frequency has a voltage source at frequency $1/T_s$ with the RMS given by (3.10). This is assuming all the ripple energy to be concentrated at the switching frequency f_s. The other harmonics occurring at multiples of switching frequency are all assumed to be concentrated at f_s. This results in a slight over-design of the filter components, which is a conservative approximation. For the fundamental frequency component, the B-BC is modeled as a sinusoidal voltage source at line frequency (60 Hz) with RMS given by $\frac{m_{V1}V_{dc}}{\sqrt{2}}$.

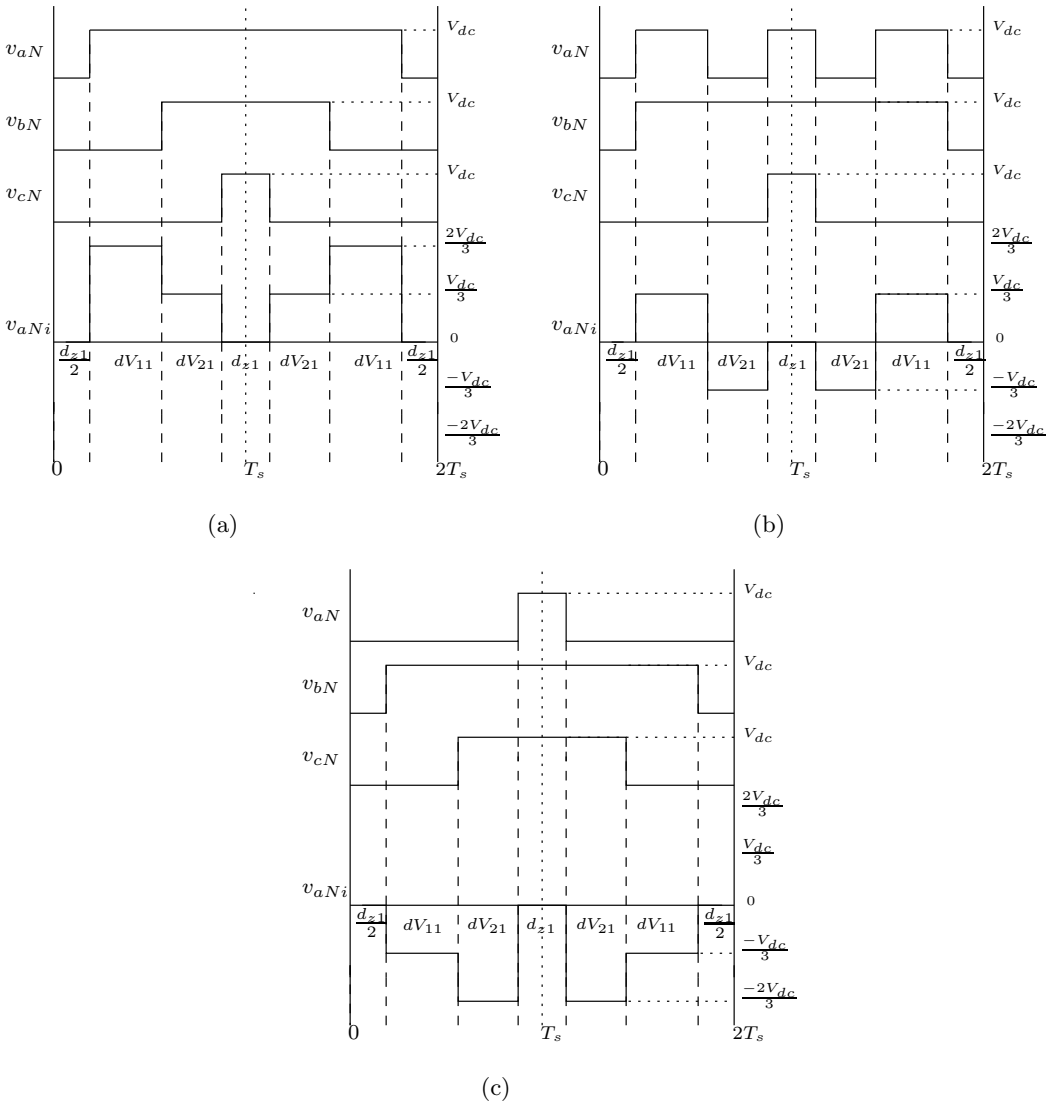


Figure 3.3: Instantaneous input line to neutral voltage generation from line to negative dc-link voltages in (a) first sector, (b) second sector and (c) third sector

3.4 Current stress on DC-link

For a suitable design of the DC-link capacitor, an accurate estimation of the current ripple flowing through it is a required parameter. The analytical calculations of the DC-link current stress is presented in this section.

The instantaneous current flowing into the capacitor is the difference of the two DC-link currents generated because of the switching of the two VSI's. Hence the square RMS of the capacitor current is as shown in (3.11). Considering just the output converter, one switching cycle is made up of time intervals $dV_{21}T_s$ and $dV_{22}T_s$ as shown in Fig. 3.2(c). During time interval $dV_{21}T_s$, when [1 0 0] is applied, the DC-link is directly connected to output phase A. Hence the instantaneous DC-link current $i_{dc2} = i_A$ during time interval $dV_{21}T_s$ in the first sector. Similarly during time interval $dV_{22}T_s$ in the first sector, the DC-link current $i_{dc2} = i_A + i_B = -i_C$. Hence the square RMS in the first sector for the DC-link current due to the output converter is as shown in (3.13). The RMS current obtained by considering just the first sector remains same in the other sectors. The output currents are assumed to be balanced sinusoidal with a peak current amplitude of I_o at frequency ω_o and load power factor of $cof\phi_o$ (3.12). Using (3.1), (3.12) and averaging over the entire sector by integration as done before, the RMS square of the DC-link current obtained by switching of just the load-side converter is as given by (3.14).

The RMS current expression due to switching of the input side converter is similar. Next the total average value of the remaining part $2I_{dc1}I_{dc2}$ is computed in a similar way. The instantaneous value in the first sector is as shown in (3.16). Similarly it is obtained for the second and third sectors as shown in (3.17) and (3.18) respectively. Three different expressions are obtained for the first three sectors which repeat for the other three sectors. The input currents are also assumed balanced sinusoidal with I_{in} being the input current amplitude, grid frequency of ω_g and unity power factor because of closed loop control (3.15). To make the calculations simpler, it is assumed that the input and output frequencies are same and the voltage space vectors for the input and output converters are aligned similarly i.e when the input voltage space vector is in the first sector, the output voltage space vector is also in the first sector. However it has been verified by simulations and experiments that the above assumptions are

completely general and the analytical expression obtained holds even when the above assumptions do not apply. Integrating over the switching time period T_s, and using (3.1), (3.2), (3.12) and (3.15), the net average value of $\int_0^{T_s} I_{dc1} I_{dc2}$ is calculated as shown in (3.19). Hence the net RMS current flowing through the capacitor is obtained as shown in (3.20). As can be seen, the expression obtained is a function of just the input and output current amplitudes, the modulation index of the B-BC and load power factor angle. It is independent of the variation in input and output frequencies and alignment angle of the space vectors of the two VSI's.

$$I_{dc,RMS}^2 = I_{dc1,RMS}^2 + I_{dc2,RMS}^2 - 2\int_0^{T_s} I_{dc1} I_{dc2} \tag{3.11}$$

$$\begin{aligned} \overline{i_A} &= I_o \cos\left(\omega_o t - \phi_o\right) \\ \overline{i_B} &= I_o \cos\left(\omega_o t - \frac{2\pi}{3} - \phi_o\right) \\ \overline{i_C} &= I_o \cos\left(\omega_o t + \frac{2\pi}{3} - \phi_o\right) \end{aligned} \tag{3.12}$$

$$i_{dc2_{RMS,Ts}}^2 = dV_{21}(i_A)^2 + dV_{22}(-i_C)^2 \tag{3.13}$$

$$I_{dc2_{RMS}}^2 = \frac{\sqrt{3}}{\pi} m_{V2} I_o^2 \left(2cos^2\phi_o + \frac{1}{2}\right) \tag{3.14}$$

$$\begin{aligned} \overline{i_a} &= I_{in} \cos\left(\omega_g t\right) \\ \overline{i_b} &= I_{in} \cos\left(\omega_g t - \frac{2\pi}{3}\right) \\ \overline{i_c} &= I_{in} \cos\left(\omega_g t + \frac{2\pi}{3}\right) \end{aligned} \tag{3.15}$$

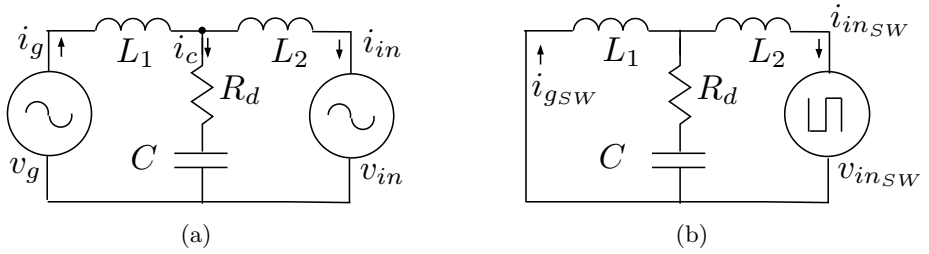


Figure 3.4: Per-phase equivalent circuit of back-to-back converter input filter at (a) fundamental frequency and (b) switching frequency

$$i_{dc1,Ts}i_{dc2,Ts_{SECTOR1}} = \{dV_{11}(i_a) + dV_{12}(-i_c)\}\{dV_{21}(i_A) + dV_{22}(-i_C)\} \tag{3.16}$$

$$i_{dc1,Ts}i_{dc2,Ts_{SECTOR2}} = \{dV_{11}(-i_c) + dV_{12}(i_b)\}\{dV_{21}(-i_C) + dV_{22}(i_B)\} \tag{3.17}$$

$$i_{dc1,Ts}i_{dc2,Ts_{SECTOR3}} = \{dV_{11}(i_b) + dV_{12}(-i_a)\}\{dV_{21}(i_B) + dV_{22}(-i_A)\} \tag{3.18}$$

$$\int_0^{T_s} I_{dc1}I_{dc2} = \frac{9}{4}I_{in}I_o m_{V1}m_{V2}cos\phi_o \tag{3.19}$$

$$I^2_{dc_{RMS}} = \frac{5\sqrt{3}}{2\pi}m_{V1}I^2_{in} + \frac{\sqrt{3}}{\pi}m_{V2}I^2_o\left(2cos^2\phi_o + \frac{1}{2}\right) - \frac{9}{2}I_{in}I_o m_{V1}m_{V2}cos\phi_o \tag{3.20}$$

3.5 Input LCL filter design of Back-to-back Converter

The back-to-back converter generates switched voltages at its input which flows a distorted current. To result in smooth sinusoidal currents at the grid, an input LCL filter is used. To design the filter components, the B-BC is modeled for different frequency components as given in the previous section. Using principle of superposition, both these components are independently analyzed and simultaneous design equations are derived. This section presents the systematic step-by-step filter design procedure.

The inverter side current ripple is generally restricted between 10-30% to reduce the losses due to switching currents in L_2. The grid side current THD should be within 5%

according to IEEE-519 standards. The LCL filter is modeled for both fundamental (Fig. 3.4(a)) and switching frequency (Fig. 3.4(b)) components. Principle of superposition is used to consider them independently. For the ripple component, the VSI is modeled as a switching voltage source, whose RMS is given by (3.10). The harmonic components occur at multiples of switching frequency. As the dominant harmonics occur at the switching frequency $1/T_s$, from the filter design perspective it is assumed that all of the ripple energy is concentrated at the switching frequency ω_s. A damping resistor R_d is connected in series with the capacitor C to damp any oscillations due to resonance. The switching ripple in the input current of VSI and the grid current can be expressed in terms of the inverter input voltage ripple as shown in (3.21) and (3.22). The magnitude plot of the transfer function between and grid current and input current of the B-BC shows a low pass filter characteristics, Fig. 3.5. The filter attenuates everything after the switching frequency f_s. The slight notch in the transfer function occurs at the resonant frequency of the LC components and is restricted by the value of the damping resistor R_d. Similar low pass filter charateristics also exists for the transfer function between input voltage and input current of the B-BC, Fig. 3.6.

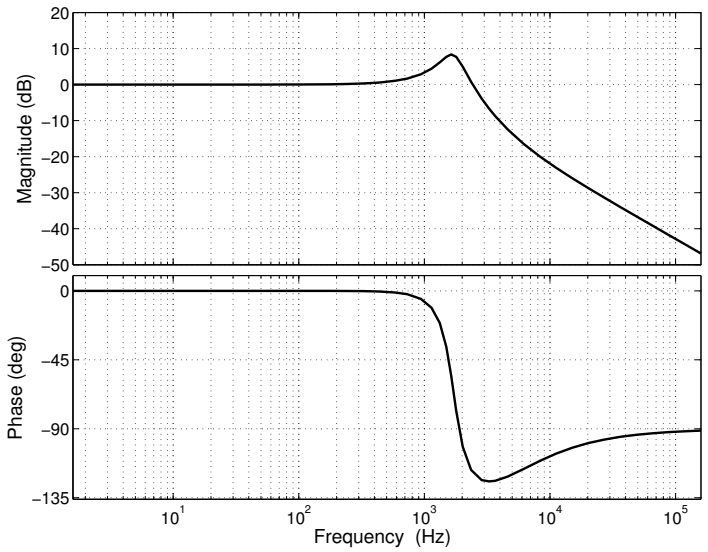


Figure 3.5: Bode magnitude and phase plots of the transfer function between grid current and input current of the B-BC

For the fundamental component, the B-BC is modeled as a sinusoidal voltage source V_{in}. With a larger capacitor, more reactive power flows raising the current rating of inductor L_2 and thus of the switches. But the capacitor can not be very small either which will increase the inductor size required to meet the same attenuation. Hence the capacitor current (3.23) is restricted to be 5-15% of grid current. The power loss in the damping resistor (3.24) should not exceed 0.001 fraction of the rated power P of the inverter (pf is power factor). The four equations can be solved to obtain L_1, L_2, C and R_d. A design check is done with respect to the maximum power transfer possible (3.24). The entire design method is shown in the flowchart in Fig. 3.7.

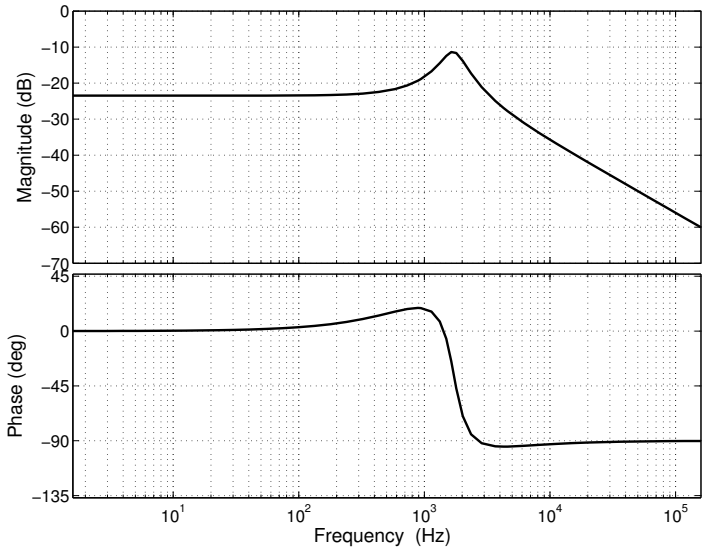


Figure 3.6: Bode magnitude and phase plots of the transfer function between input voltage and input current of the B-BC

$$I_{in_{SWRMS}} = V_{in_{SWRMS}} \left| \frac{\left(j\omega_s L_1 - \frac{j}{\omega_s C} + R_d \right)}{j\omega_s (L_1 + L_2) \left(\frac{-j}{\omega_s C} + R_d \right) - \omega_s^2 L_1 L_2} \right| \tag{3.21}$$

$$I_{g_{SWRMS}} = V_{in_{SWRMS}} \left| \frac{\left(-\frac{j}{\omega_s C} + R_d \right)}{j\omega_s (L_1 + L_2) \left(\frac{-j}{\omega_s C} + R_d \right) - \omega_s^2 L_1 L_2} \right| \tag{3.22}$$

$$I_{C_{RMS}} = \left| \frac{V_{g_{RMS}} - j\omega_g L_1 I_{g_{RMS}}}{\frac{-j}{\omega_g C} + R_d} \right| \tag{3.23}$$

$$\frac{P_{loss}}{P} = \frac{3R_d I_{C_{RMS}}^2}{3V_{g_{RMS}} I_{g_{RMS}} pf} \tag{3.24}$$

$$P_{max} = \frac{3}{2} \frac{m_{V1} V_{dc} V_g}{\omega_g (L_1 + L_2)} \tag{3.25}$$

3.6 DC-link capacitor design of Back-to-back Converter

The switching of converters generate high frequency current harmonics at the DC-link. This current ripple as given by (3.20) is taken by the capacitor C_{dc} for normal operation of the converter. The DC-link capacitor is designed based on a minimum ripple $V_{dc_{ripple}}$ (1-2%) on the DC-link voltage in order to maintain the modulation of both front and load end inverters, and can be calculated using expression (3.26). The DC-link capacitor value also depends on output torque ripple variations, unbalance issues and ride-through capability, but they are not considered in this design.

$$\frac{V_{dc_{ripple}}}{I_{dc_{RMS}}} = \frac{1}{\omega_s C_{dc}} \tag{3.26}$$

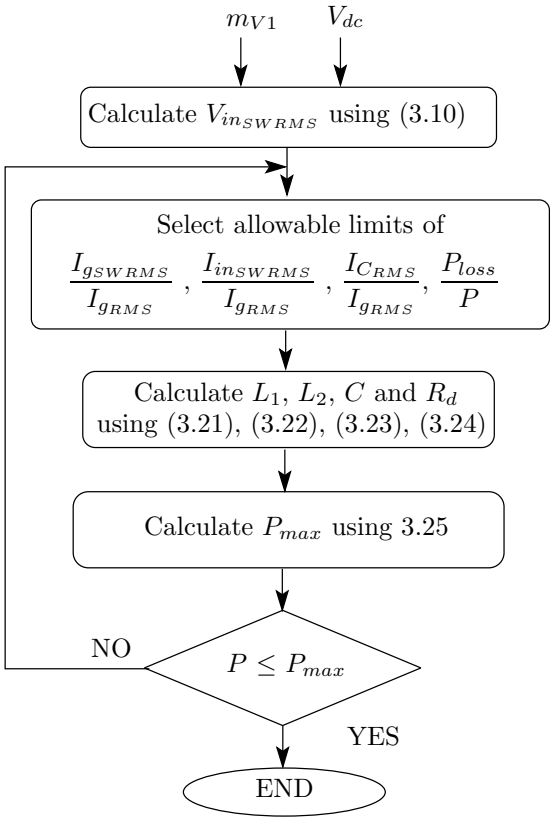


Figure 3.7: Flowchart for filter design of back-to-back Converter

3.7 Simulation Results

The analytical estimation of ripple quantities and passive components design is verified by simulation in MATLAB/Simulink. The simulation is done implementing space vector modulation as explained in Section II. Filter design is done with the specifications of allowable THD in grid current to be 2%, total maximum ripple in input current of VSI to be 15%, maximum reactive current drawn by filter capacitor to be 5% and power loss in damping resistor to be 0.001% of rated values. This section presents the simulation results.

The simulation is done with ideal switches for $3.3kV_{LL_{RMS}}$, $1MW$ VSI with modulation index $m_{V1} = 0.577$, $m_{V2} = 0.466$ and switching frequency of $10kHz$. The DC-link voltage is maintained at $5kV$ constant using a closed loop control. The load

Table 3.1: Simulation Parameters

$V_{s_{LL-RMS}}$	$3.3kV$
f_i	$60Hz$
P_o	$1MW$
$\cos\phi_o$	0.8
m_{V1}	$1/\sqrt{3}$
m_{V2}	0.466
$f_s = \frac{1}{T_s}$	10kHz
f_o	$30Hz$
L_1	0.176 mH
L_2	0.721 μH
C	12.18 μF
C_{dc}	492.8 μF
R_d	1 Ω

frequency is set at 30Hz and drives a $R-L$ load with 0.8 power factor. The RMS of switching voltage ripple in input voltage is calculated to be 176.74V from (3.10). Input filter components designed for simulation are $L_1 = 176\mu H$, $L_2 = 721\mu H$, $C = 12.18\mu F$, $R_d = 1\Omega$. The designed DC-link capacitor is $492.8\mu F$. All the parameters are shown in Table 3.1. Fig. 3.8(a) and Fig. 3.8(b) shows the output line to line voltage and three output line currents which are balanced sinusoidal. Fig. 3.8(c) and Fig. 3.8(d) shows the input voltage and input current of the VSI. The simulated input voltage RMS is 2225.3V which almost matches the analytically computed value of 2225.1V. The filtered grid current and voltage is shown in Fig. 3.8(e). As can be seen, the grid current is nearly sinusoidal with a THD content of 1.81% and is in phase with the grid voltage showing unity power factor. The frequency spectrum of various voltages and currents is shown in Fig. 3.9. Fig. 3.8(f) shows variation of $v_{aN_{iRMS}}/V_{dc}$ with the modulation index. The simulated points confirm the anlytically predicted continuous plots. This verifies the analytical estimation of input voltage RMS as described in Section II. The DC-link voltage and capacitor C_{dc} current are shown in Fig. 3.10(a). The analytical computed value of $i_{dc} = 154.1A$ closely matches the simulated value of 153.8A. Fig. 3.10(b) shows the DC-link currents from front-end and load-end converters.

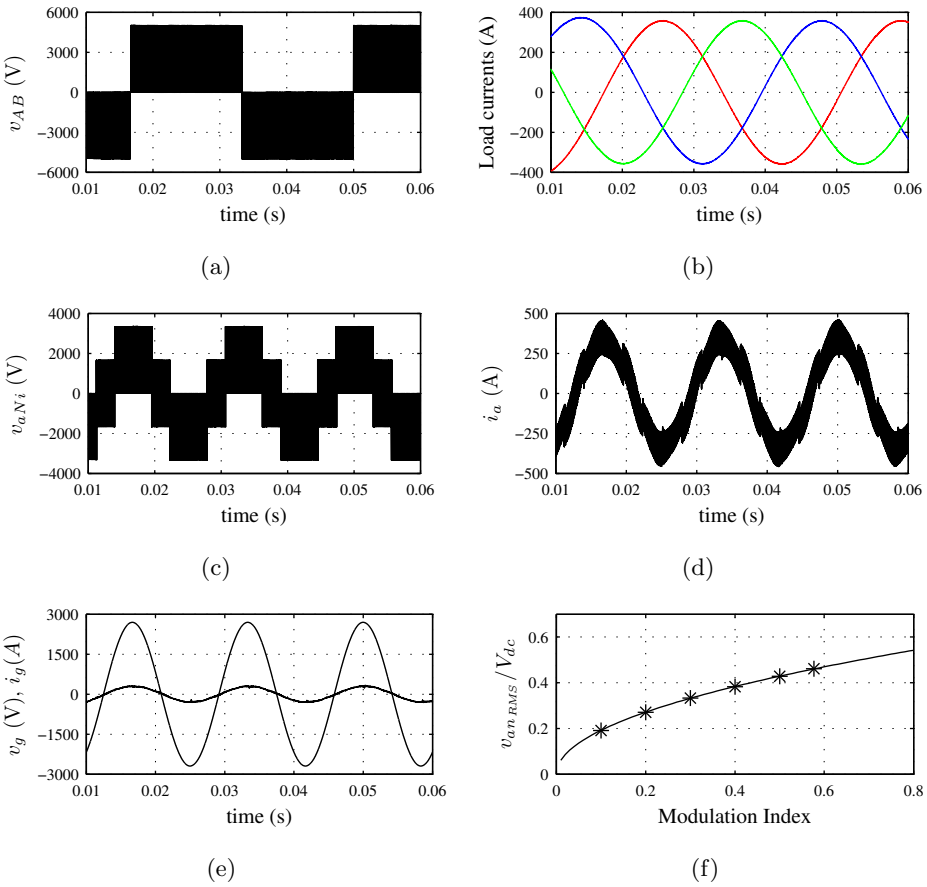


Figure 3.8: (a) Output line to line voltage, (b) Output line current. (c) Input line to neutral voltage, (d) Input line current, (e) Filtered grid voltage and current, (f) Variation of input RMS voltage with modulation index

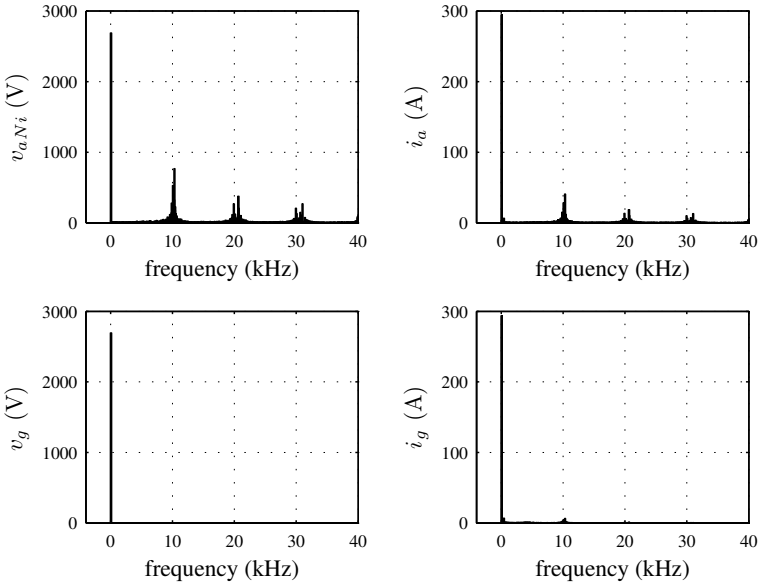


Figure 3.9: Simulation result: Frequency spectrum

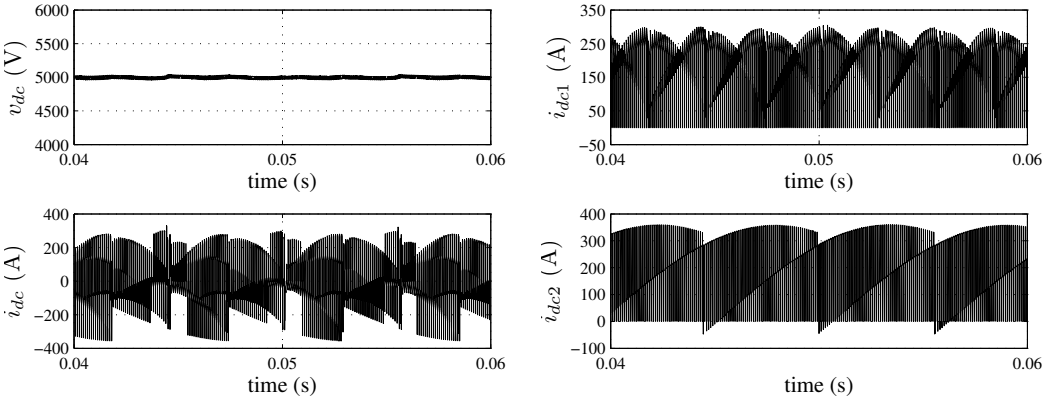


Figure 3.10: Simulation Results : (a) DC-link voltage v_{dc} (top), and total current through capacitor i_{dc} (bottom) (b) DC-link current from front end converter i_{dc1} (top), and DC-link current from load side converter i_{dc2} (bottom)

3.8 Experimental Results

This section presents the experimental results obtained on a scaled down laboratory prototype. Integrated power IGBT module APTGF90TA60PG from Microsemi is used to implement the VSI. Integrated gate driver 6SD106EI from CONCEPT are used to generate isolated gate pulses. Control signals for space vector modulation are generated from a FPGA (Xilinx XC3S500E). For sensing voltage and current signals, a measurement board with Hall effect voltage(LV25-P) and current sensors(LA55-P) is employed.

The experiments are run with a DC-link voltage of 120V and grid voltage of $55V_{LL_{RMS}}$ with a modulation index of $m_{V1} = 0.4$ of front end inverter at switching frequency of 5kHz. The drive feeds a $R - L$ load of 0.8 power factor with parameters $R_L = 10\Omega$, $L_L = 48mH$, $f_o = 30Hz$. The modulation index of output side converter is $m_{V2} = 0.5$. The designed filter components are $L_1 = 0.62mH$, $L_2 = 2.3mH$, $C = 13.94\mu F$, $R_d = 1\Omega$. Power line choke B82506-W-A6 from EPCOS ($0.5mH$, 25A) with fixed inductor 2313-V-RC ($120\mu H$, 7A) from Bourns is used in series for L_1. For L_2, fixed inductor 1140-222K-RC ($2.2\mu F$, 7A) from Bourns is used. AC film capacitors ECQU2A225KL from Panasonic of rating 2.2μF, 275 VAC are cascaded in parallel to form 4.4μF and connected in delta. This effectively makes $3 \times 4.4 = 13.2\mu$F in star connection for the filter capacitor. A 0.5W, 1Ω resistor is used as the damping resistor.

Unlike simulation where everything is ideal, dead time compensation is used between switchings in the leg. A dead time of $2\mu sec$ is used. Fig. 3.11 shows three output load currents and one line-to-line output voltage. The measured line current RMS is 2.72 A and the analytically calculated value is 3.2 A. The reduction can be attributed to the on-state voltage drop across semiconductor devices. The DC-link voltage and current due to one inverter action is shown in Fig. 3.12. The non-filtered input voltage and current are shown in Fig. 3.13(a). The RMS of the input voltage is 46.4V and the analytical value is 46.2V. The filtered waveforms and the FFT are shown in Fig. 3.13(b) and Fig. 3.14 respectively. As can be seen, the grid current is almost sinusoidal with unity power factor correction. This is verified from the FFT plot Fig. 3.14 which shows very low THD content in the grid current spectrum.

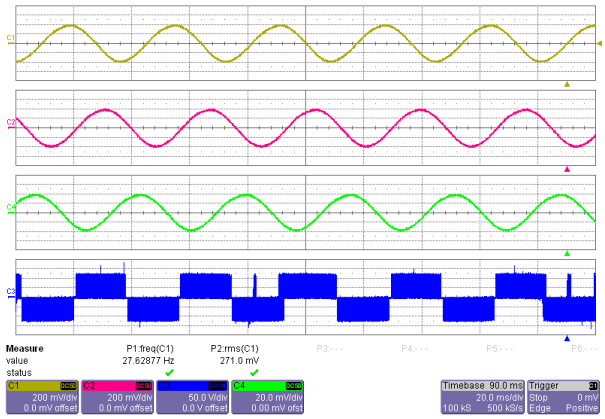


Figure 3.11: Three output line currents (2 A/div) and output line to neutral voltage (50 V/div) of one phase for R-L load

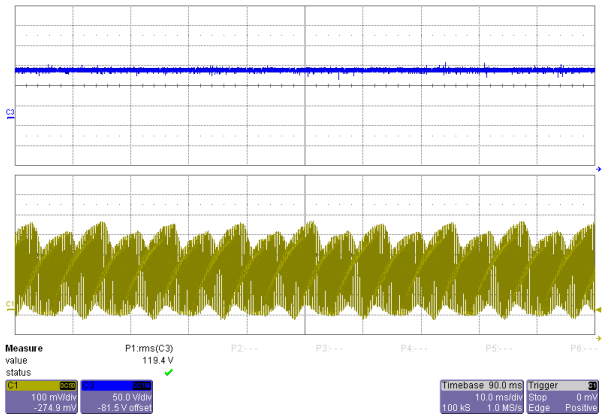
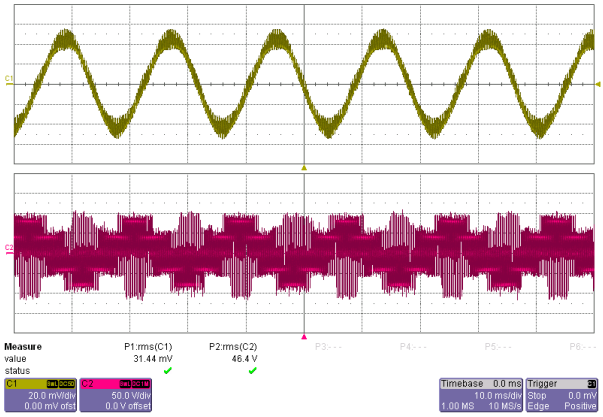
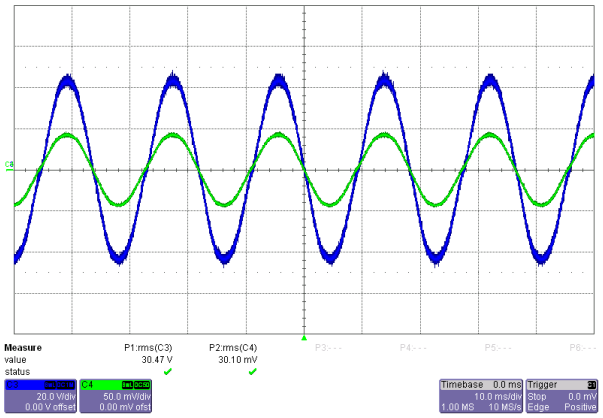


Figure 3.12: (top) DC link voltage (50 V/div), (bottom) DC link current (1 A/div)



(a)



(b)

Figure 3.13: Experimental Results : (a) Input line current (2A/div) and input line to neutral voltage (50V/div) (b) Filtered grid current (5A/div) and voltage (20V/div)

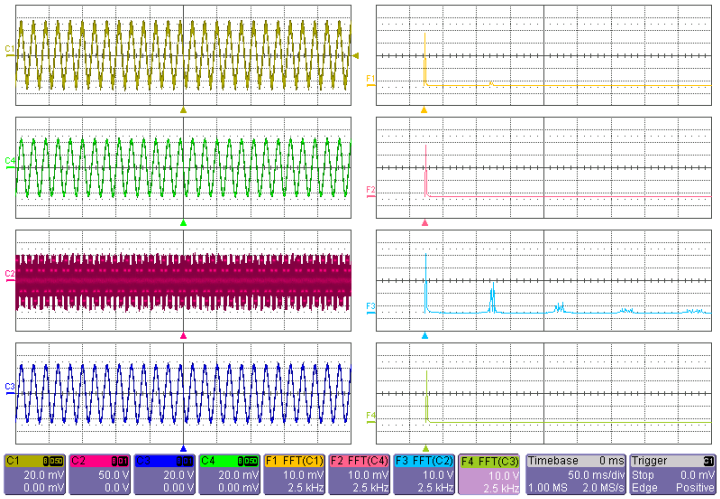


Figure 3.14: Frequency spectrum : Input and grid currents (2A/div), input voltage (50V/div), grid voltage (20V/div) with corresponding FFT (Timescale : 2MS/sec)

3.9 Conclusion

A systematic step-by-step design procedure is presented for input LCL filter design of grid connected voltage source inverters. An analytical closed form expression is derived for the input RMS voltage ripple based on modulation theory as a function of modulation index and DC-link voltage. The inverter is modeled for different frequency components and simultaneous design equations are derived to calculate the filter parameters. The design is based on specifications of allowable ripple in grid and input current and allowable reactive current drawn by filter capacitor. The designed filter provides sufficient THD elimination with minimum ohmic loss across damping resistor. The DC-link capacitor is designed based on an accurate estimation of the current ripple flowing through it. The analytical expressions and filter design is verified by simulations and experiments.

Note: Part of this chapter is reproduced from my previous publications [56] [57]

Chapter 4

Comparison of Passive Components in MC and B-BC

Matrix converter and back-to-back converter are two primarily known AC/AC power electronic converters that can be used in medium to high power applications. These two converters have been extensively compared over the years on several parameters like performance, efficiency, reliability issues, semiconductor power losses, volume of passive components, etc. A very important feature that decides the weight, volume and performance of a power electronic converter is the amount of passive components required. The matrix converter is not an all-silicon solution as described before. However it does not have the bulky DC-link capacitor as required in a back-to-back connected converter. The previous two chapters presented systematic design procedures for the passive components in a matrix converter and DC-link based back-to-back converter. This chapter presents a quantitative and qualitative comparison of the designed passive components of the two converters on different scales.

The matrix converter has a maximum voltage gain of 0.866 according to conventional space vector modulation approach. On the other hand, the voltage source based back-to-back converter has an upper hand here as it can result in much higher voltage gains due to the boost inductor. The B-BC is generally always used at a modulation index of 1. In this chapter two sets of comparison are done between the MC and B-BC based on maximum voltage gain, as described over the next two sections. In Case I of the

comparisons, the B-BC output converter modulation index is lowered to meet the same gain as a matrix converter. Hence it results in the same overall gain of 0.866 for both. Thus the same motor can be connected to the two converters which flows the same load current. All fundamental voltage and current magnitudes are uniform through out, which makes it easy for comparison. In Case II, both the converters are used at their full modulation index i.e matrix converter at a modulation index of 0.866 and the back-to-back converter at a modulation index of 1. For the same power rated motor, the B-BC will generate a higher voltage and hence result in lower load current amplitude. The MC can generate a slightly lower output voltage magnitude as compared to B-BC and hence flows a load current of higher RMS magnitude. The passive components are designed for the two cases and comprehensively compared under variation of switching frequency and for different power rated motors.

4.1 Case I

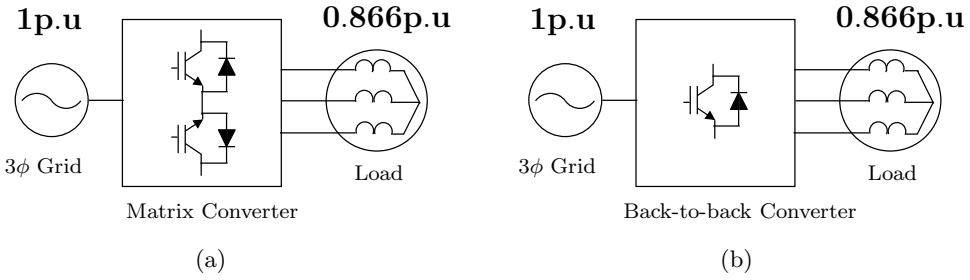


Figure 4.1: Voltage gains for Case I in (a) matrix converter and (b) back-to-back converter

The two converters are supplied from the same grid of 480 V line to line RMS, and feeds the same motor of 20 kW at 30 Hz. The modulation index is set at 0.866 for both at a switching frequency of 10 kHz. Hence it results in the same input and output currents. The designed values of the passive components are shown in Table 4.1. It is graphically shown by a bar graph in Fig. 4.2.

As can be seen, the grid side inductor L_1 of matrix converter is nearly 1.3 times larger in magnitude than that of the back-to-back converter. However, there is an additional large boost inductor L_2 present in the back-to-back converter. Thus the

combined inductance needed on the input side is four times larger for a B-BC than a MC. Both the converters see the same fundamental component of the input line currents and hence volume of the inductors scale directly according to the magnitude of inductance (volume $\propto LI^2$). However, the boost reactor of the B-BC has large iron loss due to high frequency components in the input current. In contrast, the input reactor of the MC experiences just the fundamental current as most of the high frequency ripple current flows through the filter capacitor. Hence it has small iron loss. The comparison of filter inductors along with the current and voltage stress is shown in Table 4.2 and graphically in Fig. 4.3.

The filter capacitance C of matrix converter is nearly three times larger in magnitude as compared to that of back-to-back converter. Both the capacitors are subject to same voltage stress. Thus volume scales directly according to magnitude of capacitance (volume $\propto CV^2$). However, the losses incurred which affect the overall lifetime also depend on the ripple current flowing through the capacitors. The matrix converter input filter is subject to much higher current stress as compared to the back-to-back converter. The RMS current flowing through the capacitors (3.2 A) in B-BC is composed of some reactive current and remaining ripple current. Whereas, the MC filter capacitors see a much larger current ripple (20.5 A) as analytically calculated in Chapter 2. This is shown in Table 4.3 and by bar graph in Fig. 4.4. So in a nutshell, the MC capacitors have three times the magnitude than that of B-BC and are also subject to 6.5 times higher current stress which reduces its overall lifetime. The back-to-back converter also has a DC-link capacitance of 529.6 μF which is subject to a current stress (24.5 A) as analytically calculated in Chapter 3 and an applied voltage of 750V. This unreliable DC capacitor, which is usually electrolytic is absent in case of a matrix converter.

Table 4.1: Comparison : Passive components

Parameters	**MC**	**B-BC**
$L_1(\mu H)$	248.20	187.01
$L_2(\mu H)$	-	804.48
$C(\mu F)$	33.28	11.51
$C_{dc}(\mu F)$	-	529.65

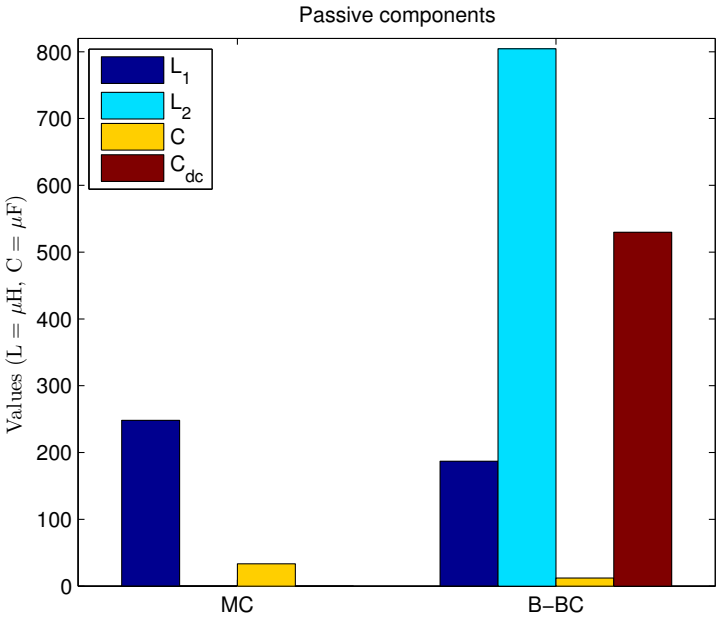


Figure 4.2: Passive component values in MC and B-BC

Table 4.2: Comparison : Inductor ratings

Parameters	**MC**	**B-BC**
$L_1(\mu H)$	248.20	187.01
$I_{L_1,RMS}(A)$	24.05	24.05
$V_{L_1,RMS}(V)$	277.12	277.12
$L_2(\mu H)$	-	804.48
$I_{L_2,RMS}(A)$	-	27.65
$V_{L_2,RMS}(V)$	-	277.12

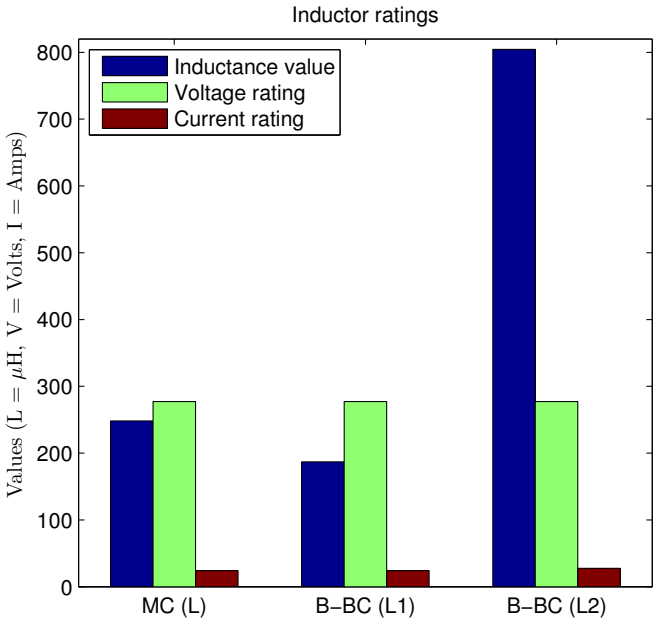


Figure 4.3: Inductor ratings of filter in MC and B-BC

Table 4.3: Comparison : Capacitor ratings

Parameters	**MC**	**B-BC**
$C(\mu F)$	33.28	11.51
$I_{C,RMS}(A)$	20.56	3.2
$V_{C,RMS}(V)$	277.12	277.12
$C_{dc}(\mu F)$	-	529.65
$I_{C_{dc},RMS}(A)$	-	24.5
$V_{C_{dc},RMS}(V)$	-	750

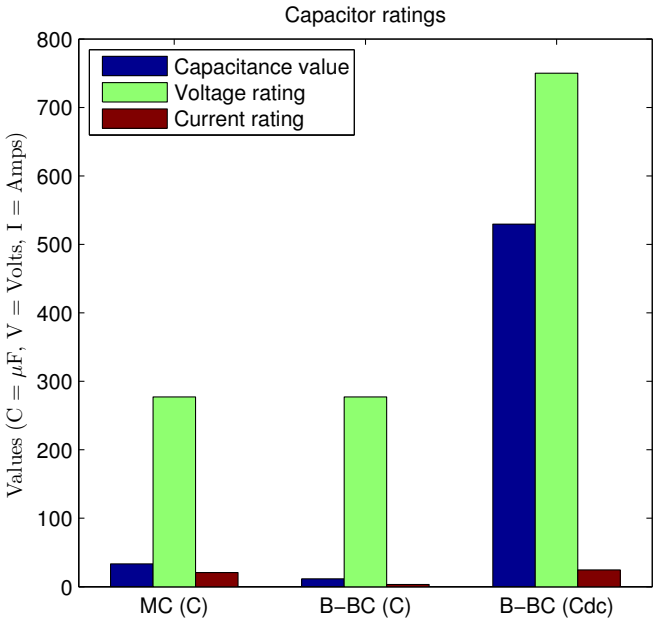
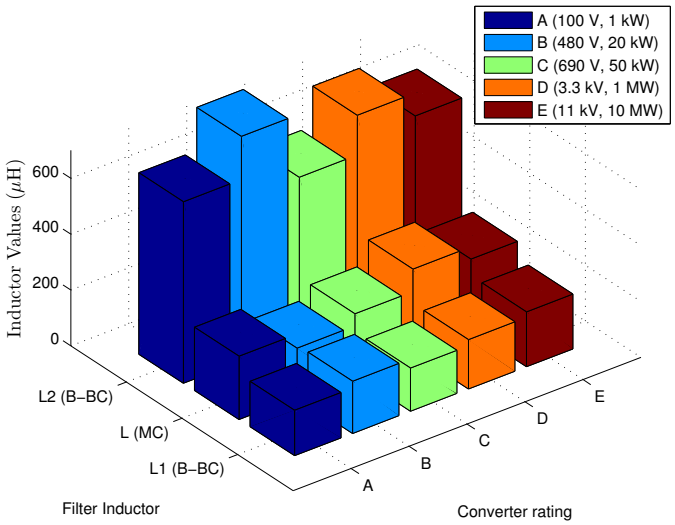


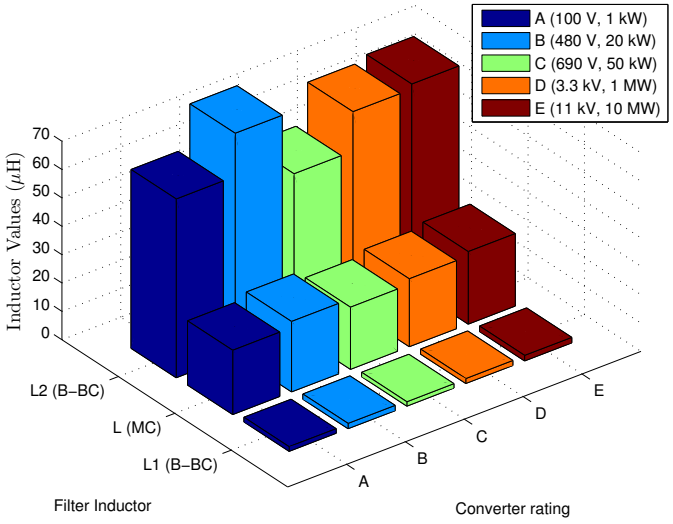
Figure 4.4: Capacitor ratings of filter in MC and B-BC

The comparison is done at different power levels and different grid voltages to see the variation in passive component values. For a switching frequency of 10 kHz, the passive components are designed for 5 sets of operating points. The grid line to line voltage RMS and motor power rating are : (100 V, 1 kW), (480 V, 20 kW), (690 V, 50 kW), (3.3 kV, 1 MW), (11 kV, 10 MW). It is observed that the ratio of capacitor and inductor values calculated for MC and B-BC still holds as described before. From Fig. 4.5(a), it can be said that the matrix converters input inductor value is nearly 4 times smaller than that of a back-to-back converter for all operating power at same voltage gain of 0.866 for both the converters. The filter capacitor of matrix converter is always nearly 3 times larger than that of a back-to-back converter. But including the DC-link capacitor, the MC capacitor requirements is much smaller, Fig. 4.6(a).

With increase in switching frequency, the filter values start decreasing because of an inverse relation. The dominant harmonics occur at the f_s. Now the filter needs to attenuate the harmonics at a much higher frequency than before, and hence results in relaxation of the filter size. With the advent of high speed and low on-state loss SiC power devices, this is a possibility. Fig. 4.5(b) and Fig. 4.6(b) show the results of passive component requirements at a higher switching frequency of 100 kHz at different power ratings. The input filter capacitor of the MC is the main element which results in attenuation of the ripple current. For the B-BC, the boost inductor attenuates the switching voltage ripple. The design of filter capacitor in B-BC is designed based on the reactive current drawn and hence its design is independent of the switching frequency. As can be seen from Fig. 4.5(b), inductor L_1 of B-BC has drastically reduced by nearly 100 times as compared to inductor L of MC which has reduced by nearly 10 times. The variation of filter inductors with frequency is shown in Fig. 4.7. Just comparing the grid side inductor, the filter inductor L of MC is now nearly 13 times larger than L_1 of B-BC. Overall both the inductors L_1 and L_2 of B-BC now are 3 times larger than that of MC at 100 kHz. For the input filter capacitor, the B-BC capacitor remains constant. The MC filter capacitor decreases exponentially as shown in Fig. 4.8. After a switching frequency of around 30 kHz, the matrix converter input filter capacitor actually becomes smaller than that of the back-to-back converter. As shown in Fig. 4.6(b), at 100 kHz, the MC filter capacitor is nearly 3.5 times smaller than that of the B-BC. The DC-link capacitor also adds to the net capacitance requirements of the B-BC.

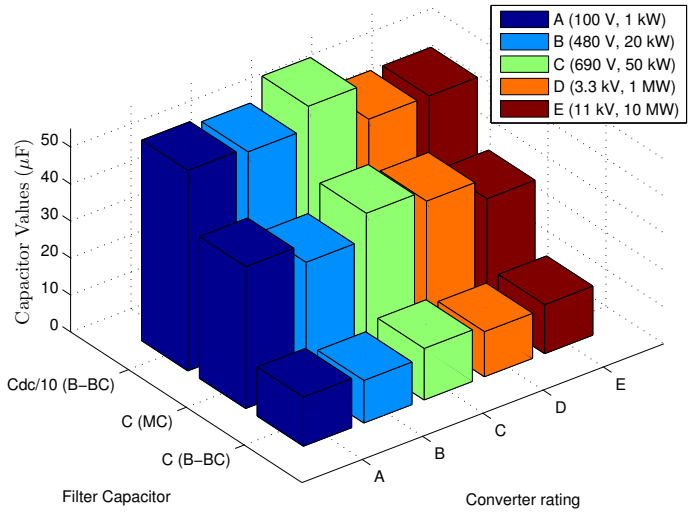


(a)

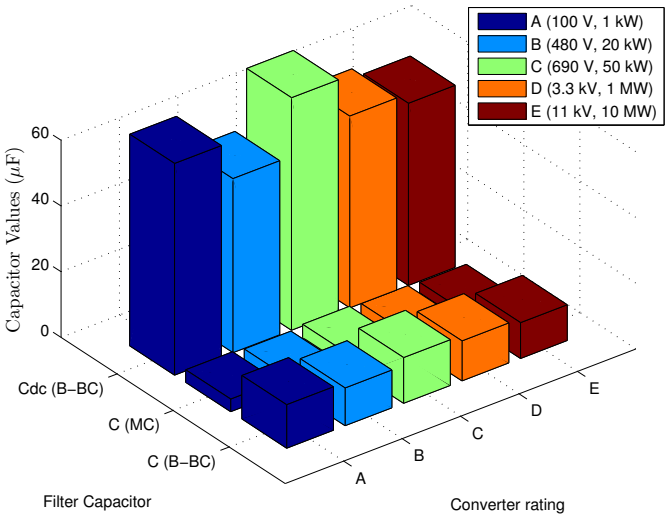


(b)

Figure 4.5: Variation of filter inductor values for different operating conditions for (a) switching frequency = 10 kHz and (b) switching frequency = 100 kHz



(a)



(b)

Figure 4.6: Variation of filter capacitor and DC-link capacitor values for different operating conditions for (a) switching frequency = 10 kHz and (b) switching frequency = 100 kHz

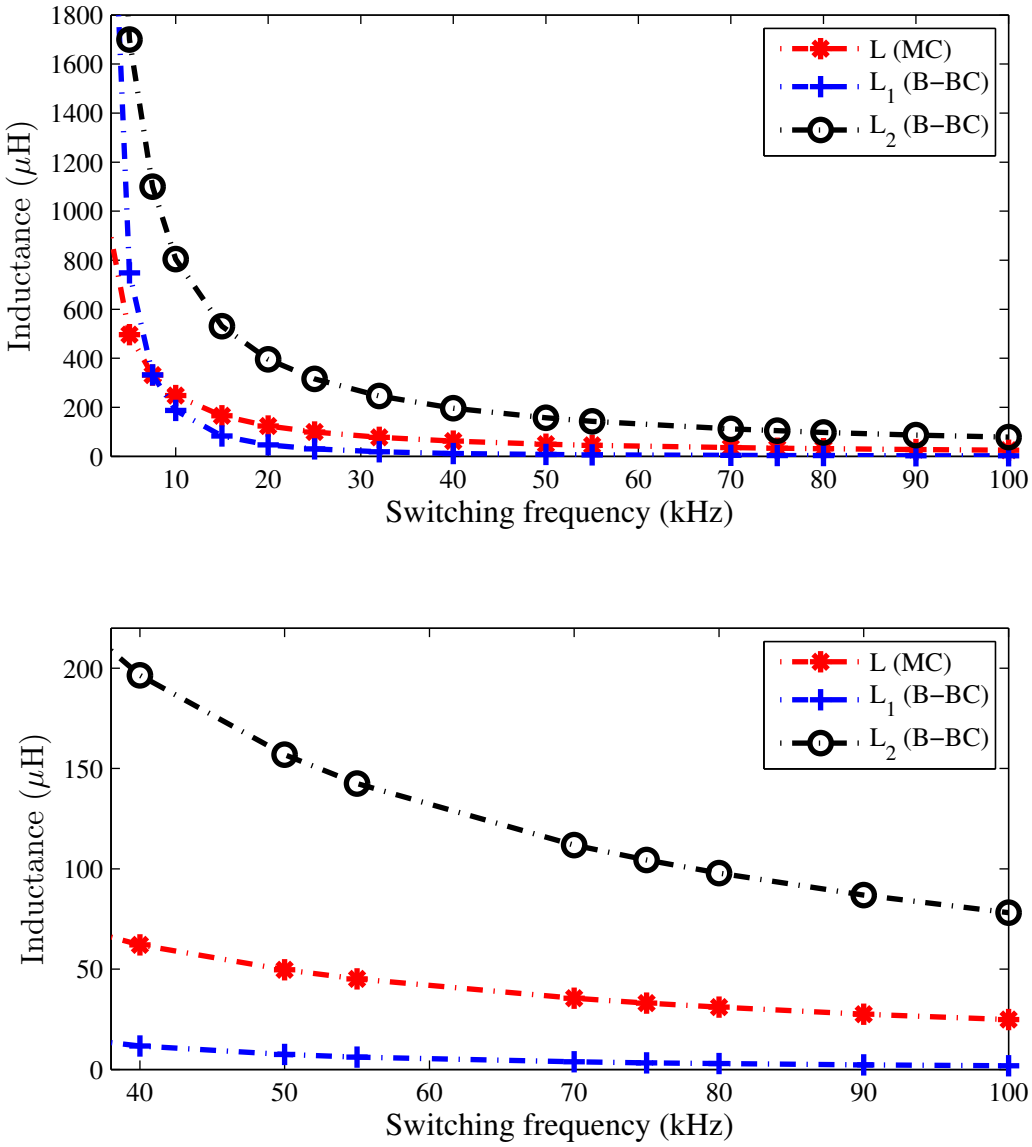


Figure 4.7: Variation of filter inductor values with switching frequency in MC and B-BC

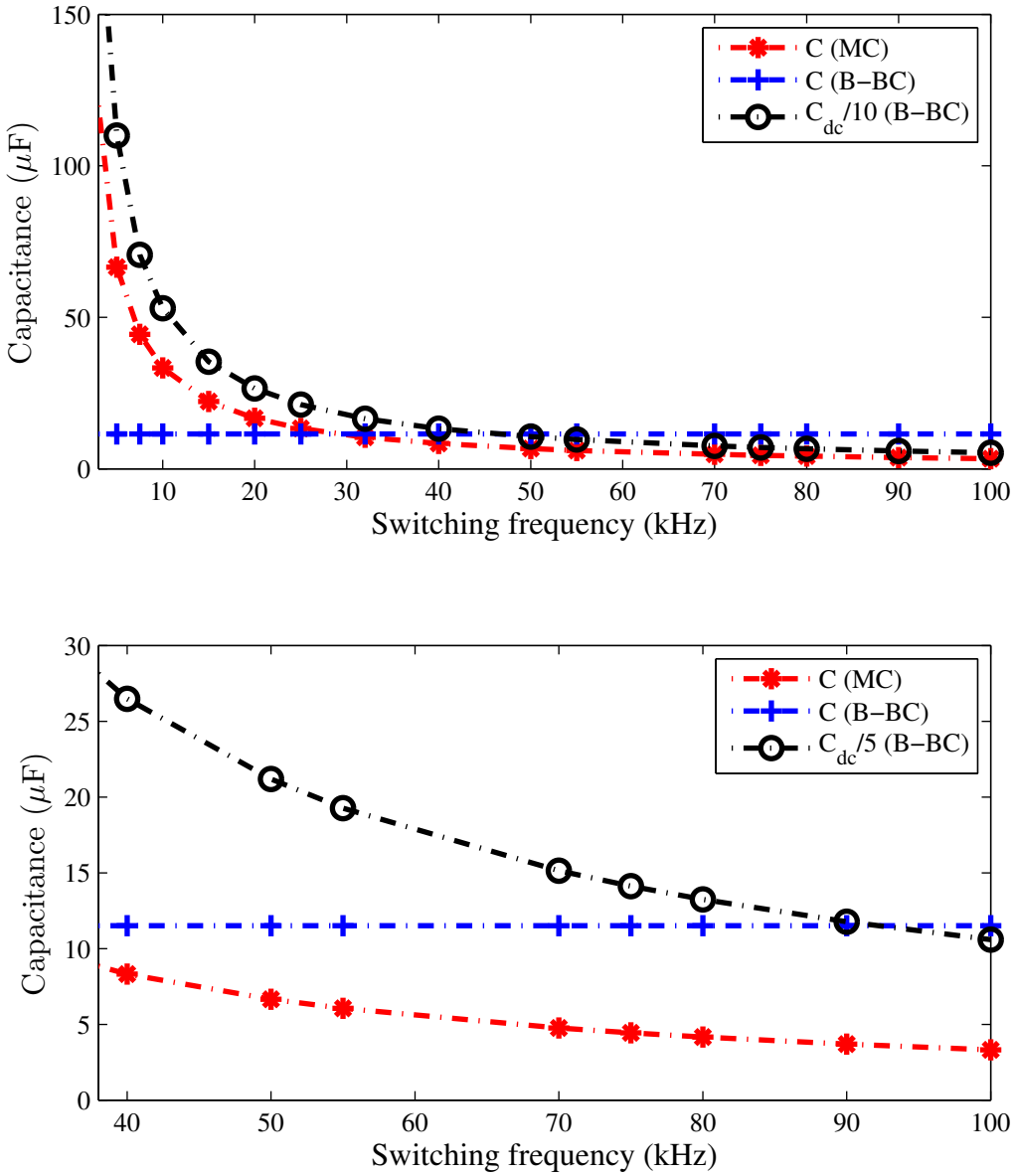


Figure 4.8: Variation of filter capacitor and DC-link capacitor values with switching frequency in MC and B-BC

4.2 Case II

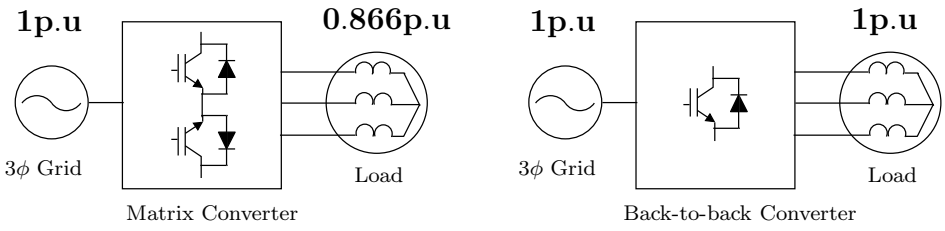
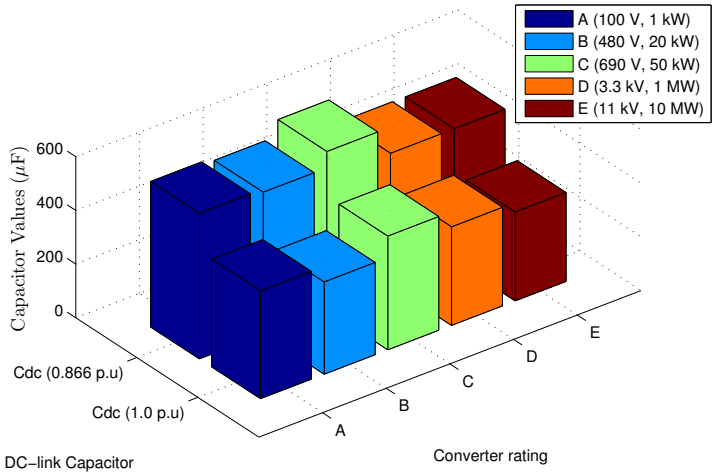
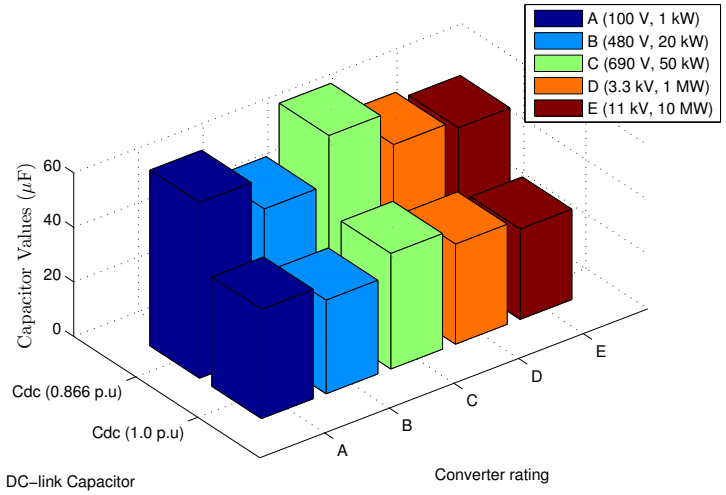


Figure 4.9: Voltage gains for Case II in (a) matrix converter and (b) back-to-back converter

In case II, the two converters are supplied by the same grid and drive the same motor at rated power. However now they both operate at their full modulation index i.e MC at its maximum modulation index of 0.866 at B-BC at its full modulation index of 1. Doing so, the B-BC generates a higher voltage output at the load end, and hence lesser load currents flow for the same rated power. It is to be noted that the input RMS voltage ripple in the B-BC is independent of the load currents as shown by the analytical expression (3.10) in Chapter 3. It is just a function of the modulation index of the front end inverter and DC-link voltage which is constant. Hence the design of the input LCL filter is unaffected by variation of the modulation index of the load end inverter. The difference observed is in the DC-link current ripple calculations. As discussed in Chapter 3, the square of DC-link current ripple (3.20) is a function of the modulation index of the front-end and load-end inverters along with the square of peak currents on both sides. Thus with reduction in load currents and variation in modulation index of load-end inverter, there is an overall reduction in DC-link current ripple. Thus it results in reduction in the value of the DC-link capacitor (3.26). As shown in Fig. 4.10(a) and Fig. 4.10(b), the DC-link capacitor has reduced by almost 1.5 times compared to before at switching frequency of 10 kHz and 100 kHz respectively. The variation of DC-link capacitor with switching frequency for the two different modulation indices is shown in Fig. 4.11.



(a)



(b)

Figure 4.10: Variation of DC-link capacitor values for two different modulation indices for (a) switching frequency = 10 kHz and (b) switching frequency = 100 kHz

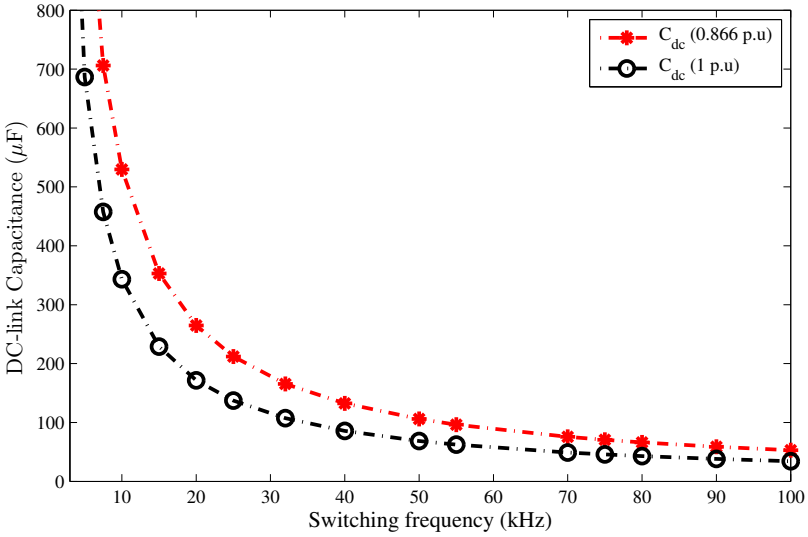


Figure 4.11: Variation of DC-link capacitor values with switching frequency at modulation index of 0.866 and 1.0

4.3 Summary

In summary, this chapter presented the comparison between the passive components of a matrix converter and DC-link based back-to-back converter. The inductor requirements in MC are lower as compared to that of a B-BC over all frequency and power range. Overall, the inductor requirements of B-BC is nearly 4 times higher at 10 kHz and 3 times higher at 100 kHz. The B-BC boost inductor also incurs higher iron losses due to switched currents, whereas the MC filter inductor sees just the fundamental current and hence has lower losses. The filter capacitor of MC at lower frequencies is nearly 3 times larger in magnitude than that of a filter capacitor of B-BC. The matrix converter C is also the primary element which takes in the ripple current and has nearly 6.5 times higher current stress than that of the B-BC which reduces its overall lifetime. However at higher frequencies ($\geq$ 30 kHz), the MC filter capacitor value becomes smaller than that of the back-to-back's capacitor. At 100 kHz, it is almost 3.5 times smaller than that of the B-BC. The ripple current in independent of the variation in switching frequency. The B-BC also has a much higher value DC-link capacitor which is bulky.

This unreliable DC-link capacitor is absent in a matrix converter which gives it an upper hand. Thus in a nutshell, it can be said that the matrix converter's passive component requirements are lesser than that of a voltage source based back-to-back converter.

Note: Part of this chapter is reproduced from my previous publication [57]

Chapter 5

Conclusion and Future Work

Passive components have a significant impact on the overall converter losses, volume, weight, and lifetime due to their physical properties. Therefore proper design of these passive components plays an important role in any power electronic converter system, which is the main contribution of this thesis. Because of ripple components in the input current of a matrix converter and input voltage of a back-to-back converter, input filters need to be present before interfacing it with the AC-grid. According to IEEE-519 standards the maximum THD in the grid current can not exceed 5% of the fundamental current. Hence a passive L-C filter and LCL filter are used in case of a matrix converter and back-to-back converter respectively. The performance comparison of the two converters depends a lot on the volume of passive components, which is presented in this thesis.

Chapter 2 presents a systematic step-by-step approach to design the filter components of a MC. The RMS input current ripple is analytically computed from the modulation theory and the converter is modeled for different frequency components. The expression obtained is independent of variation in input-output frequencies and variation in output space vector alignment angle, and only depends on the modulation index of the converter, the load and its power factor. Based on this accurate estimation of input ripple RMS and certain specifications like allowable THD in the grid current and distortion in the input voltage, the filter components are calculated. A passive damping resistor is designed based on minimum power loss. The designed filter results in smooth sinusoidal grid currents, near unity input power factor, negligible drop across

the filter and minimum loss in damping resistor.

Chapter 3 describes the input LCL filter and DC-link capacitor design of a voltage source based back-to-back converter. The switching of the front end inverter injects switched voltages into the grid. This voltage ripple is analytically evaluated for conventional space vector modulation as a function of the modulation index and constant DC-link voltage. An LCL filter is designed based on specifications of allowable THD in grid current, maximum allowable inverter input current and reactive current through filter capacitor. A damping resistor in series with the filter capacitor minimizes oscillations due to LC resonance and is designed for minimum ohmic loss. The DC-link capacitor current ripple is also analytically computed as a function of known parameters and is used for its proper design.

The designed passive components in Chapter 2 and 3 are compared over various scales in Chapter 4 for two cases of voltage gain. The voltage gain of a MC is lower (0.866) as compared to a B-BC (1.0). In case I , the modulation index of a B-BC is reduced to 0.866 to allow the same motor load with same load current drawn for an easy comparison. The comparison is done for five different sets of operating points and with variation in switching frequency. It is observed that the input inductor requirements of MC is nearly 4 times smaller than B-BC at 10 kHz and 3 times smaller at 100 kHz. The MC input filter capacitor sees much higher current ripple as compared to B-BC, resulting in reduced lifetime. However at higher frequencies ($\geq$ 30 kHz), the MC filter capacitor becomes lesser than that of a B-BC input capacitor. This is because the input filter capacitor of MC now has to attenuate the dominant harmonics at a much higher frequency. Because of inverse relation, the filter capacitor value decreases exponentially. However for a B-BC, the input filter capacitor is independent of the switching frequency. The DC-link capacitor is much larger than the input filter capacitor value and is highly unreliable too. This is absent in the matrix converter.

In short, this dissertation presented the design and comprehensive comparison between the passive component requirements of a matrix converter and DC-link based back-to-back converter.

5.1 Future Work

Based on the contributions of this thesis, several future research possibilities are as listed below:

- This dissertation presented the comparison of passive components values along with their current and voltage ratings. Based on that, the inductors and capacitors can be actually designed and built in the lab for a proper comparison of size and volume.
- Investigation of actual losses in passive components can be studied on an experimental setup.
- The variation of passive components with switching frequency and higher power levels should be experimentally evaluated at higher switching frequencies (for example at 100 kHz). SiC switches can be used for this application
- Closed loop control of front end rectifier in a B-BC should be experimentally verified for DC-link capacitor design. Also design considerations based on ride-through capability, unbalance at grid side, and load torque ripple variations can be investigated.
- Investigation into EMC input filter can be done.
- Other multistage filter topologies and active damping techniques can be further studied.

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