LOW VOLTAGE / LOW POWER RAIL-TO-RAIL CMOS OPERATIONAL AMPLIFIER FOR PORTABLE ECG

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Abstract

One of the most important building blocks in modern IC design is the operational amplifier. For the portable electrocardiogram (ECG), the operational amplifier is employed to sense and amplify the electrical signal of heartbeat of human body. For the battery powered portable ECG system, low supply voltage environments are required to reduce power consumption and the result is a reduced input common mode range (ICMR) of the op-amp. To overcome the reduced ICMR problem, complementary differential pairs operated in parallel are commonly used to achieve a rail-to-rail input common mode range. However, this complementary differential input pair structure can have a substantial transconductance (gm) variation problem and a dead zone problem in a low supply voltage environment and an extremely low supply voltage environment respectively. In the past years, a number of techniques have been proposed to overcome those problems for low- and extremely low-supply voltage environments. This dissertation is focused on an op-amp applicable to a portable ECG system and in total five novel rail-to-rail constant gm op-amps usful for circuits such as a portable ECG are proposed. Three of those op-amps work in the low supply voltage environment and two op-amps are proposed for the extremely low supply voltage environment. Cadence SPECTRE simulation and TSMC 0.25-μm CMOS technology are used to simulate and lay out these works.

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Chapter 1. Introduction

1.1 Background and Motivation

One of the main trends of electronic biomedical devices is portability and wireless operation. Because, for the future healthcare services, portable electronic health monitoring devices will enable 24 hour health monitoring, home healthcare systems, early detection of diseases and so on. Electrocardiogram (ECG) is one of the electronic biomedical systems which senses the electrical signal of the heartbeat to detect abnormal rhythms of the heart. A conventional ECG system, however, is very bulky and not convenient for 24 hour monitoring due to wired connections. Portable ECG facilitates 24 hour monitoring for patients who have heart diseases and need cardiac monitoring in their everyday life. With this trend of battery powered health monitoring systems, portable biomedical devices demand circuits operating in low supply voltage.

In the ECG system, an op-amp often senses and amplifies the electrical signal of the heart. The op-amp of the portable ECG may have to be operated in low supply voltage environments for lower power consumption and the result of lowered supply voltage is a reduced input common mode range (ICMR) of the op-amp. A commonly used way to overcome reduced ICMR problem and ensure rail-to-rail input common mode signal is complementary differential pairs operated in parallel (Figure 1.1). Because both N-type and P-type differential pairs are employed in the input stage, the entire range

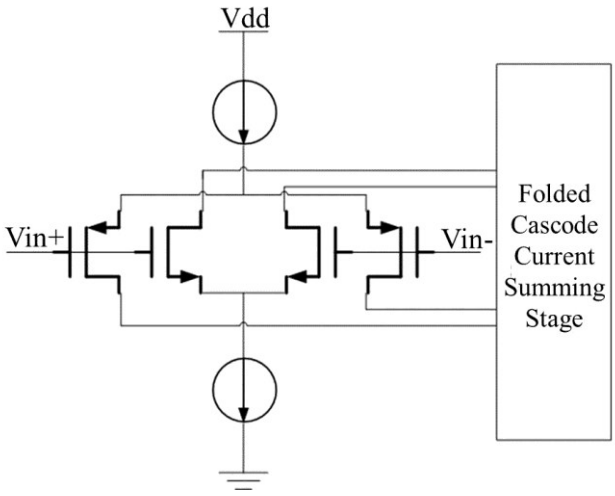
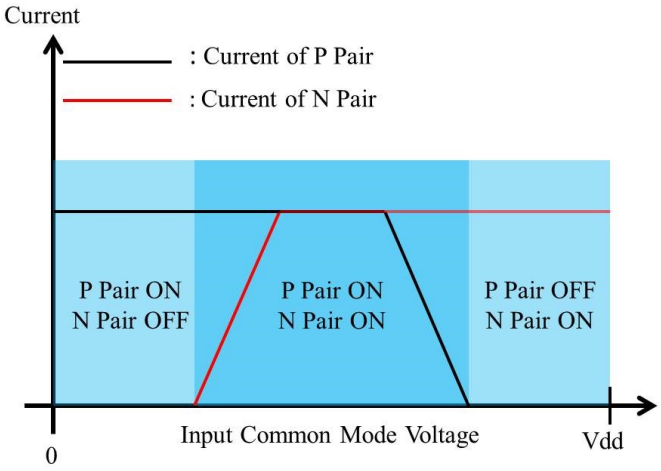


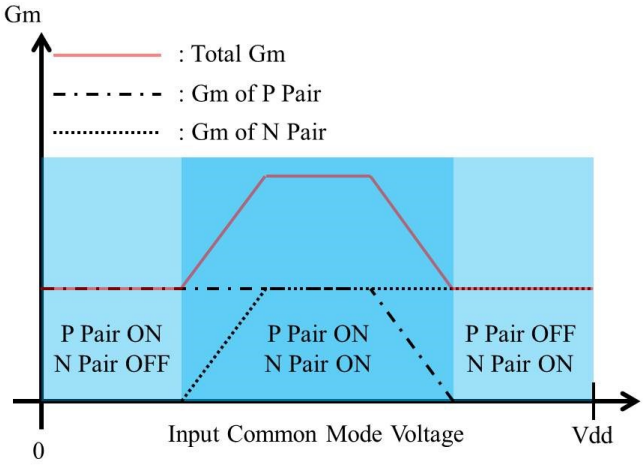
Figure 1.1 Complementary Input Differential Pair Structure

of supply voltage, rail-to-rail, can be an input common mode range. One problem with the complementary differential pair structure, however, is overall transconductance (gm) variation in the middle range of the common mode input signal. There are two possible situations according to the environment of supply voltage. The first situation is about two times the transconductance variation problem with low supply voltage environment and the second is dead zone problem with extremely low supply voltage environment.

Figure 1.2 shows that the working principle of complementary input differential pair structure and the transconductance variation problem with a low supply voltage environment. In Figure 1.2 (a), if a single input differential pair, either N-type or P-type, is used, the turn off region of the input common mode voltage of N-type or P-type input will limit a portion of the ICMR. The complementary input differential pair structure employs both of N-type and P-type input differential pairs and ensures rail-to-rail input common mode voltage range. The problem of this structure, however, with low supply



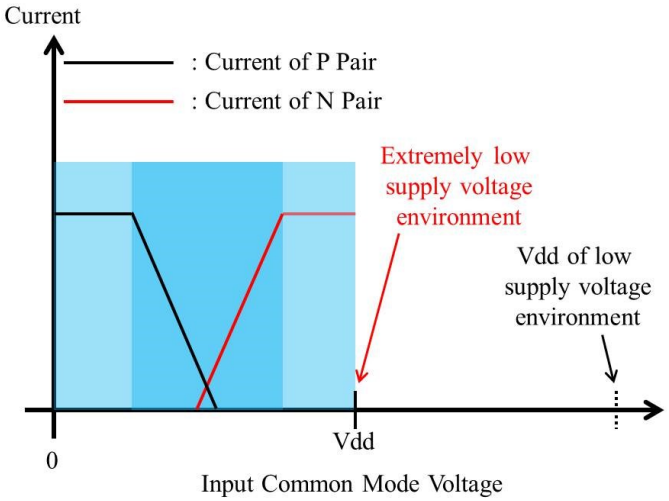
(a) Currents of Complementary Input Differential Pair Structure



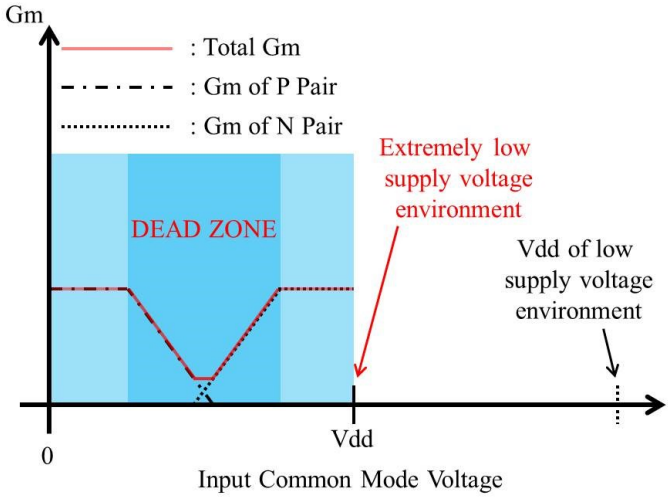
(b) Total Transconductance Variation with Low Supply Voltage

Figure 1.2 Working Principle and Total Gm Variation of Low Supply voltage Environment

voltage is that there is an approximately two-fold transconductance variation throughout the common mode input range which results in a variable unity gain frequency and a stability problem. Figure 1.2 (b) shows the total transconductance variation problem with low supply voltage. Both N-type and P-type input differential pairs are turned on at the same time in the middle range of common mode input signal and that causes about two times the transconductance variation. In the past years, a number of constant gm



(a) Currents of Complementary Input Differential Pair Structure



(b) Total Transconductance Variation with Extremely Low Supply Voltage

Figure 1.3 Working Principle and Dead Zone of Extremely Low Supply voltage Environment

techniques are proposed to overcome the transconductance variation problem of a low supply voltage environment and three typical techniques are briefly explained in chapter 2.

The situation of an extremely low supply voltage environment is totally different from the case of low supply voltage environment. With extremely low supply voltage, both of N-type and P-type differential input pairs of complementary input differential pair

structure are turned off or triode region in the middle range of common mode input signal. Figure 1.3 shows currents of input pairs and total transconductance variation of the extremely low supply voltage environment. Because the both input pairs are turned off or in the triode region, the total transconductance is very small or almost zero in the middle range of common mode input signal. Thus, this region is called the 'dead zone'. A few techniques are previously introduced to avoid the dead zone problem and some typical techniques are explained in chapter 4.

In this dissertation, five novel techniques are proposed. The first three are new level shifting technique, saturation point control technique, and modified new level shifting technique and these three techniques are working in low supply voltage environment. The other techniques are common mode elimination technique and new input signal compression technique. Those techniques can be made to work in the extremely low supply voltage environment.

1.2 Requirements of Portable ECG Amplifier

A conventional ECG system usually employs an instrumentation amplifier which is also employed by other biomedical instruments such as EEG, EMG, and so on. Figure 1.4 shows the structure of the instrumentation amplifier and this structure has some intrinsic characteristics which are suitable for ECG system. First, the instrumentation amplifier has very high input impedance. For ECG systems, electrodes are usually used to sense the electrical signal of heartbeat and a high input impedance is required for the

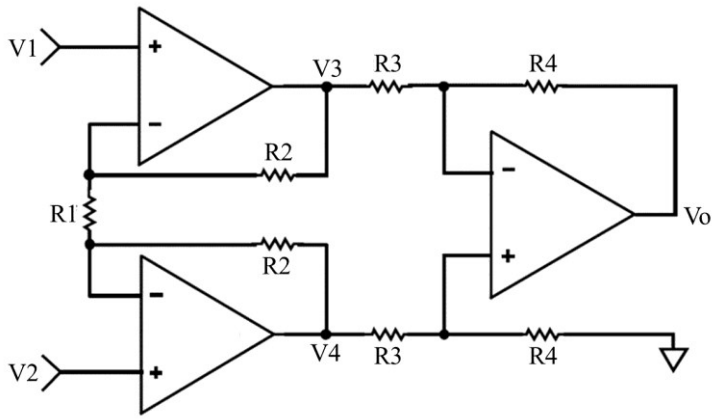


Figure 1.4 Structure of the Instrumentation Amplifier

ECG amplifier because of high impedance of electrode. The minimum allowable input impedance of the ECG amplifier is typically 10 MΩ ([3]) which is easily achieved in a MOSFET amplifier since the input of the instrumentation amplifier is directly connected to the gate of MOSFET and its input impedance is very high. The second requirement of ECG amplifier is high common mode rejection ratio (CMRR). The ECG system is required to sense only the cardiac signal and reject all other electrical common mode signals typically from larger muscles in the body. In Figure 1.4, if V_1 and V_2 which are two inputs of the instrumentation amplifier have same voltage, the current which flow through resistor R_1 is ideally zero and the voltage of V_3 and V_4 are the same. Thus, there is no amplification of common mode voltage and the instrumentation amplifier has very high CMRR. The third is a gain that can be changed by adjusting R_1. The gain of the instrumentation amplifier is expressed as below.

$$Gain = \frac{Vo}{V1 - V2} = \left(1 + \frac{2 * R2}{R1}\right)\left(\frac{R4}{R3}\right)$$

There are two registers for R_2, R_3, and R_4, while only one register is required for R_1 (Figure 1.4). Hence, the gain of the instrumentation amplifier is easily controlled by adjusting R_1.

For the amplifier of the portable ECG system, low power consumption is required as well as all other requirements for the conventional ECG system mentioned before. Basically, the portable ECG system is battery powered and for more battery life, low power consumption and low supply voltage for an amplifier is essential. This dissertation is focused on an operational amplifier for the portable ECG with low supply voltage and extremely low supply voltage environment.

Listed below are some target specifications for the novel low supply voltage rail-to-rail op-amps proposed in this dissertation. Gains of all amplifiers are larger than 40dB and 3dB frequencies are around 150Hz. Phase margins are larger than 55º. In [4], acceptable input referred noise of ECG amplifier is $30\mu V_{p\text{-}p}$ and $5\mu V/\sqrt{Hz}$ at 1Hz of input referred noise is good enough for ECG signal acquisition [3]. Large transistor sizes are used to reduce flicker noise at low frequencies and input referred noise is about $5\mu V/\sqrt{Hz}$ at 1Hz. CMRR, unity gain frequency, average power consumption, supply voltage, and gain variation of all proposed op-amps are compared with each other using post layout simulation results in Chapter 6.

1.3 Organization of The Dissertation

This dissertation is divided into seven chapters. Following this introduction, previously introduced rail-to-rail amplifiers for low supply voltage environment are described in Chapter 2. The low supply voltage environment is explained first and three typical rail-to-rail techniques are described. Three typical rail-to-rail techniques for the low supply voltage environment are tail current control technique, maximum/minimum current selection technique and level shifting technique. Not all rail-to-rail constant-gm techniques for low supply voltage amplifier can be categorized in these three techniques, but these techniques are typical method for constant-gm of rail-to-rail operational amplifier with low supply voltage.

In Chapter 3, three novel rail-to-rail constant-gm techniques for the low supply voltage environment are proposed. The first technique is new level shifting technique. This technique has similar concept with the conventional level shifting technique. For this novel technique, however, only one diode connected NMOS is required and that is the simplest method for rail-to-rail constant-gm op-amp. The second one is saturation point control technique. This is novel transition regions technique and proposed to overcome drawback of conventional and new level shifting technique. The last technique is the modified new level shifting technique which is hybrid of new level shifting technique and saturation point control technique. The transconductance variation of the new level shifting technique can be reduced considerably using this technique.

Literature review for previous technique of extremely low supply voltage rail-to-rail op-amp is given in Chapter 4. Previously introduced techniques are dynamic level shifting technique, depletion mode input pair technique, bulk driven input stage technique and input signal compression technique.

Two novel techniques for extremely low supply voltage rail-to-rail constant-gm op-amps are proposed in Chapter 5. The common mode elimination technique is the first technique. This technique employs conventional input signal compression technique and signal inverting blocks are introduced with resistors to eliminate the common mode input signal. Because the common mode input signal is eliminated, very high CMRR is achieved. The new input signal compression technique, is the second technique for the extremely low supply voltage environment, and has the same basic concept as the common mode elimination technique, but conventional input signal compression blocks are replaced by a new input signal compression block to improve bandwidth and noise performance, and reduce complexity.

In Chapter 6, all the post layout simulation results are shown and all proposed techniques are compared. The conclusion is given in Chapter 7.

Chapter 2. Literature Review for Low Supply Voltage Op-Amp

2.1 Low Supply Voltage Environment

As mentioned in Chapter 1, a low supply voltage often results in a reduced input common mode range problem. The conventional complementary differential input pair structure which overcomes reduced ICMR problem and ensures rail-to-rail input common mode range has double the transconductance in the middle range of the input common mode signal when compared to the higher and lower voltage regions of the common mode signal. This doubled transconductance variation implies a two-fold variation of gain and two-fold variation in unity gain frequency. The unity gain frequency variation can cause serious stability problems. When the compensation capacitor is optimized for sufficient phase margin for stable operation, the unity gain frequency varies by a factor of two depending on the value of input common mode voltage, and consequently the phase margin may not be enough and the whole system may be unstable for certain values of common mode input (usually midway between the power supplies). Therefore, constant transconductance as a function of common mode input is desirable for a low supply voltage rail-to-rail op-amp. For this reason, several constant transconductance techniques for low supply voltage rail-to-rail op-amp are proposed in the past. Three typical

techniques from among those techniques are briefly explained in the following sections of this chapter.

2.2 Tail Current Control Technique

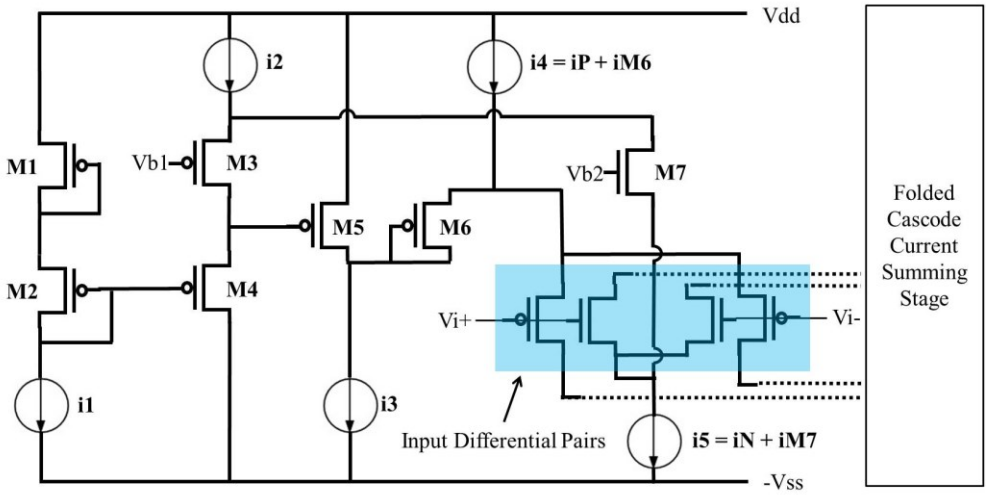
The first typical technique for low supply voltage rail-to-rail op-amp is the tail current control technique. In the low supply voltage environment, both N-type and P-type input differential pairs of the complementary input pairs structure are turned on at the same time in the middle range of the common mode input signal and the currents of the middle range of both input pairs cause two times the transconductance variation (Figure 1.2). Thus, if the currents of both input pairs are controlled in the middle range of the common mode input signal, the total transconductance can be kept constant. The currents and transconductance of input pairs, and the total transconductance are expressed as below.

$$I_{N,P} = \frac{1}{2}\mu_{n,p}C_{ox}\left(\frac{W}{L}\right)_{N,P}\left(V_{gs} - V_{th}\right)^2$$

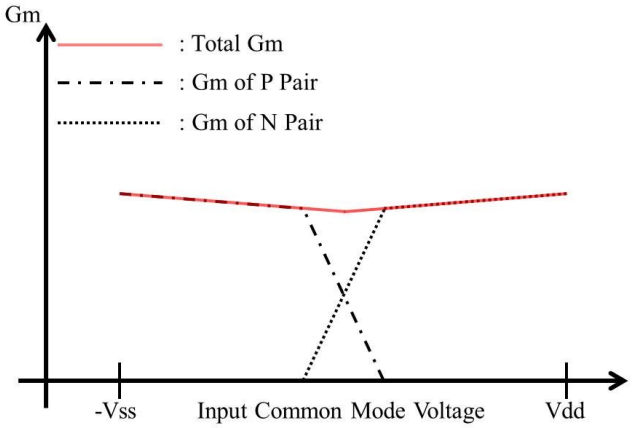
$$gm_{N,P} = \sqrt{2\mu_{n,p}C_{ox}\left(\frac{W}{L}\right)_{N,P} I_{N,P}} = \sqrt{2KP_{N,P}I_{N,P}}$$

$$gm_{total} = gm_N + gm_P = \sqrt{2KP}\left(\sqrt{I_N} + \sqrt{I_P}\right) \quad \text{(if } KP_N = KP_P = KP\text{)}$$

From the above equations, for the constant total transconductance, $\left(\sqrt{I_N} + \sqrt{I_P}\right)$ must be kept constant in the whole range of input common mode signal, because KP is constant. Therefore, in the middle range of input common mode signal, I_N and I_P should be one quarter of I_N of high input common mode voltage and I_P of low common mode voltage.



(a) Concept of Constant Square Root Current Circuit



(b) Total Transconductance Variation with Square Root Current Circuit

Figure 2.1 Tail Current Control using Square Root Current Circuit

A number of techniques employ this tail current control technique and Figure 2.1 shows the concept of this technique and total transconductance variation ([5]~[7]). Some equations for explanation of this circuit are given below.

$$V_{sg,M1} + V_{sg,M2} = V_{sg,M4} + V_{sg,M5} = Constant$$

$$V_{sg,M4} + V_{sg,M5} = \sqrt{\frac{2I_{M4}}{KP(W/L)}} + |V_{thP}| + \sqrt{\frac{2I_{M5}}{KP(W/L)}} + |V_{thP}| = Constant$$

$$\sqrt{I_{M4}} + \sqrt{I_{M5}} = Constant$$

$$I_2 = I_{M4} + I_{M7} = I_5 = I_N + I_{M7} \qquad I_{M4} = I_N$$

$$I_3 = I_{M5} + I_{M6} = I_4 = I_P + I_{M6} \qquad I_{M5} = I_P$$

$$\sqrt{I_{M4}} + \sqrt{I_{M5}} = Constant = \sqrt{I_N} + \sqrt{I_P}$$

The sum of source gate voltage difference, V_{sg}, of M1 and M2 is same as the sum of V_{sg} of M4 and M5. From the above equation, the sum of the square roots of I_{M4} and I_{M5} is constant. And the currents of M4 and M5 are same with I_N and I_P. I_N and I_P are currents of NMOS and PMOS input pairs, respectively. Therefore, $\left(\sqrt{I_N} + \sqrt{I_P}\right)$ can be kept constant and as a result, the total transconductance is constant in the whole range of input common mode signal (Figure 2.1 (b)).

Another method to control tail current is introduced in [8]~[10]. This technique employs current switch to control tail current and conceptual circuit of this technique is shown in Figure 2.2. When NMOS or PMOS input pair is turned off, the switch 2 (SW2) or the switch 1 (SW1) diverts tail current I_{ref}, respectively. Using 1:3 current mirror, $3I_{ref}$ is added to tail current I_{ref} of PMOS or NMOS input pair. As a result, the total current of NMOS or PMOS input pair when the common mode input signal is close to Vdd or Vss is $4I_{ref}$. Thus, $\left(\sqrt{I_N} + \sqrt{I_P}\right)$ and the total transconductance can be kept

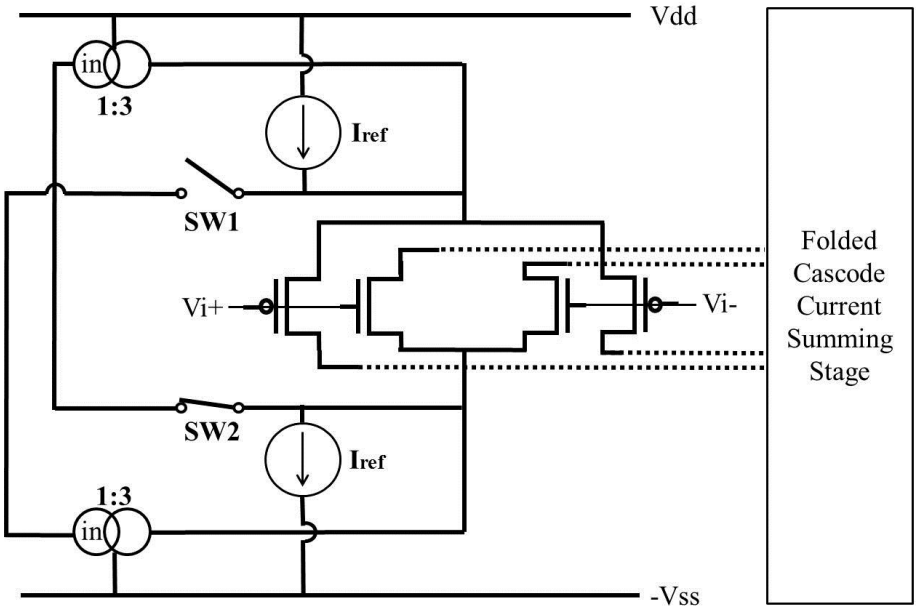


Figure 2.2 Tail Current Control using Current Switch

constant in the whole range of input common mode signal.

The above square root circuit and 1:3 current mirror circuit, however, have two limitations. The first limitation is that both techniques are based on drain current quadratic characteristic. Those techniques cannot apply to deep sub-micrometer CMOS devices because deep sub-micrometer CMOS devices do not follow quadratic characteristic accurately. The second is two times variation of slew rate. The above two techniques has two times the total current of input stage variation and that causes slew rate variation. In [11], hex-pair structure is proposed to overcome these limitations. The circuit of input stage of this technique is shown in Figure 2.3. There are three PMOS input pairs and three NMOS input pairs. When the common mode input signal is close to Vss, only PMOS input pairs, block P1 and block P2, are turned on. The total current of

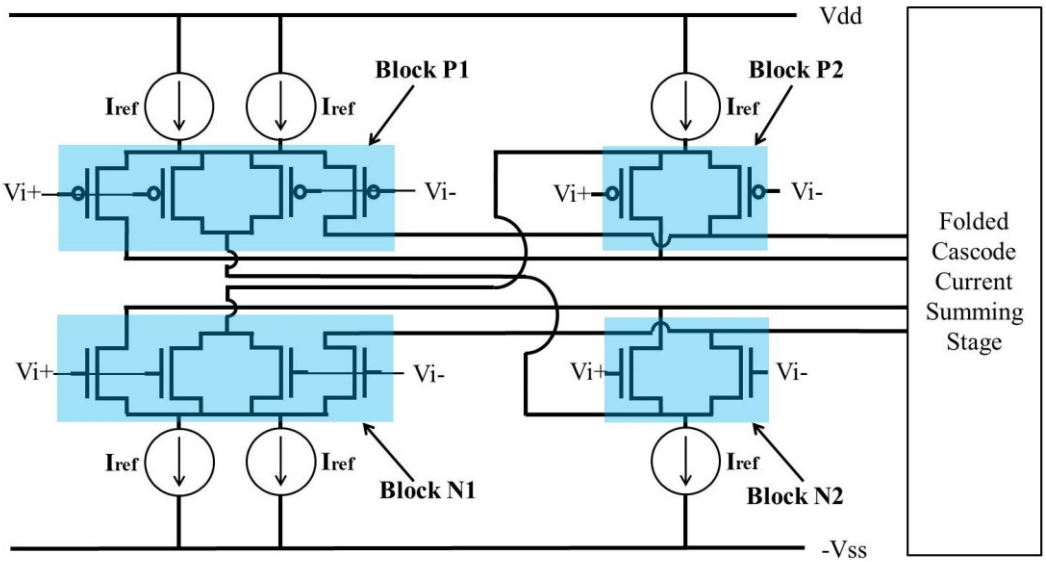
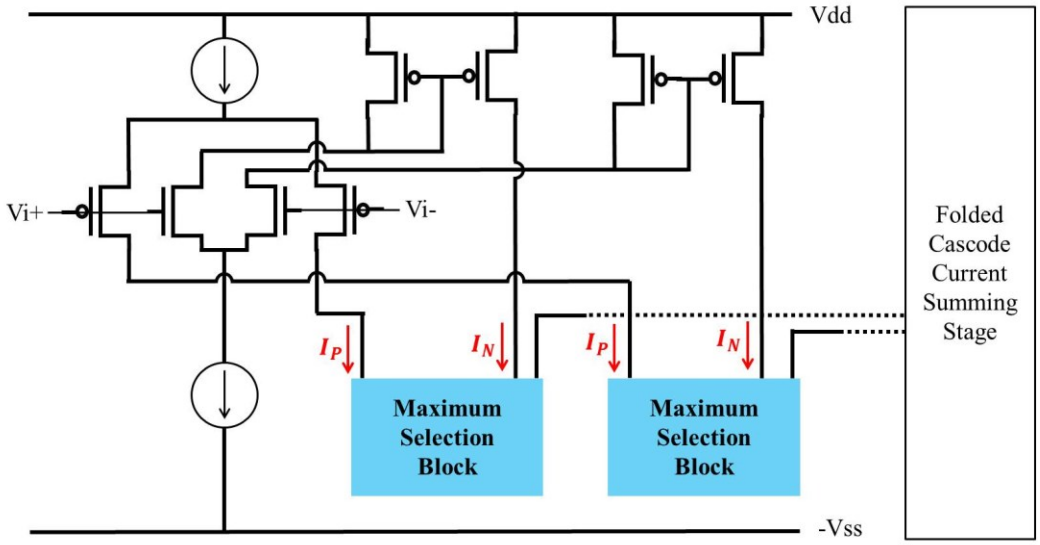


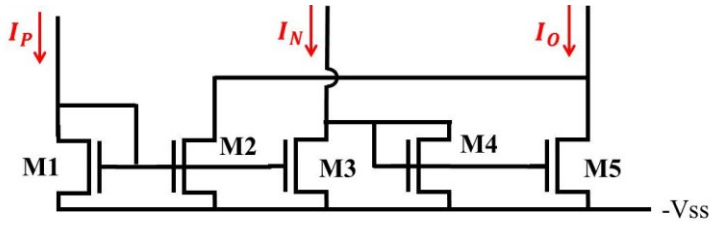
Figure 2.3 Tail Current Control using Hex-Pair Structure

block P1 is $2I_{ref}$ and one I_{ref} of this total current is diverted to block N2. Thus, $2I_{ref}$, one I_{ref} from block P1 and another I_{ref} from block P2, are transferred to the folded cascode current summing stage. When the common mode input signal is close to Vdd, only the input pairs of block N1 and N2 are turned on and, with the same working principle of PMOS input pairs' case, $2I_{ref}$ are transferred to the next stage. In the middle range of input common mode signal, only the input pairs of block P1 and block N1 are turned on. One I_{ref} from block P1 is diverted to block N2 and NMOS input pair of block N2 is turned off. And one I_{ref} from block N1 is diverted to block P2 and PMOS input pair of block P2 is turned off. Hence, $2I_{ref}$, one I_{ref} from block P1 and another I_{ref} from block N1, are transferred to the next stage. Because the total currents of input pairs are always $2I_{ref}$ in the whole range of input common mode signal, there are no significant variations of total transconductance and slew rate.

2.3 Maximum/Minimum Current Selection Technique



(a) Circuit of Maximum Current Selection Technique



(b) Maximum Current Selection Block

Figure 2.4 Maximum Current Selection Technique

The maximum/minimum current selection technique is the second typical technique for low supply voltage rail-to-rail op-amp. The basic concept of this technique is only the current of one pair, larger or smaller current, is transferred to the next stage. Therefore, the only one input pair's transconductance can affect the total gain. Maximum current selection technique is introduced in [13] and Figure 2.4 shows the circuit of the input stage of maximum current selection technique. When the current of PMOS input,

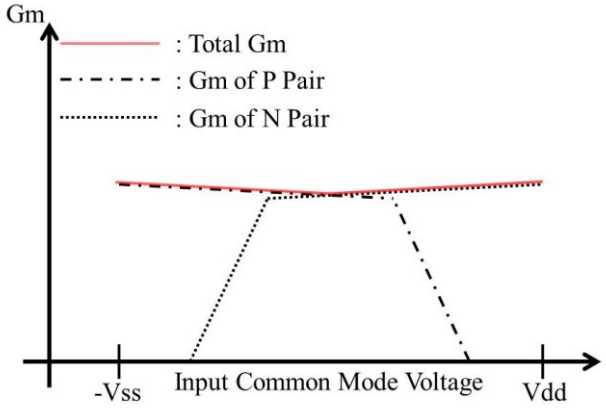


Figure 2.5 Total Transconductance of Maximum Current Selection Technique

I_P, is larger than the current of NMOS input, I_N, the currents of M1 and M2, I_{M1} and I_{M2}, equal I_P (Figure 2.4 (b)). Because I_N is smaller than I_P, the current of M3, I_{M3}, equals I_N. In this situation, M4 is turned off and the currents of M4 and M5, I_{M4} and I_{M5}, are zero. Thus, I_O equals $I_{M2} = I_P$, because I_O equals sum of I_{M2} and I_{M5}. On the contrary, if I_N is larger than I_P, the currents of M1, M2, and M3 equal I_P. Then, the currents of M4 and M5 are $I_N - I_{M3} = I_N - I_P$. Therefore, I_O equals I_N, because I_O equals sum of I_{M2} and I_{M5}, $I_O = I_{M2} + I_{M5} = I_P + I_N - I_P$. As a result, only the larger current and the larger transconductance can be transferred to the folded cascode current summing stage. Figure 2.5 shows the total transconductance variation of maximum current selection technique.

In [12], the minimum current selection technique (which has a similar concept to the maximum current selection technique) is proposed. The circuit of the minimum current selection block is illustrated in Figure 2.6. If I_1 is larger than I_2, $I_1 = I_{M5} = I_{M6} = I_{M7}$ and $I_2 = I_{M2}$. I_{M3} is $I_1 - I_2$, because I_{M6} is sum of I_{M2} and I_{M3}. I_{M4} equals I_{M3} and I_{M7} is sum of I_O and I_{M4}. So, I_O equals I_2, because $I_O = I_{M7} - I_{M4} = I_1 - (I_1 - I_2) = I_2$.

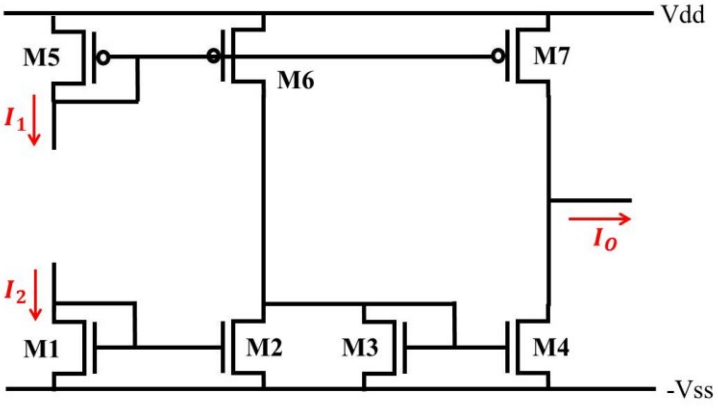


Figure 2.6 Minimum Current Selection Block

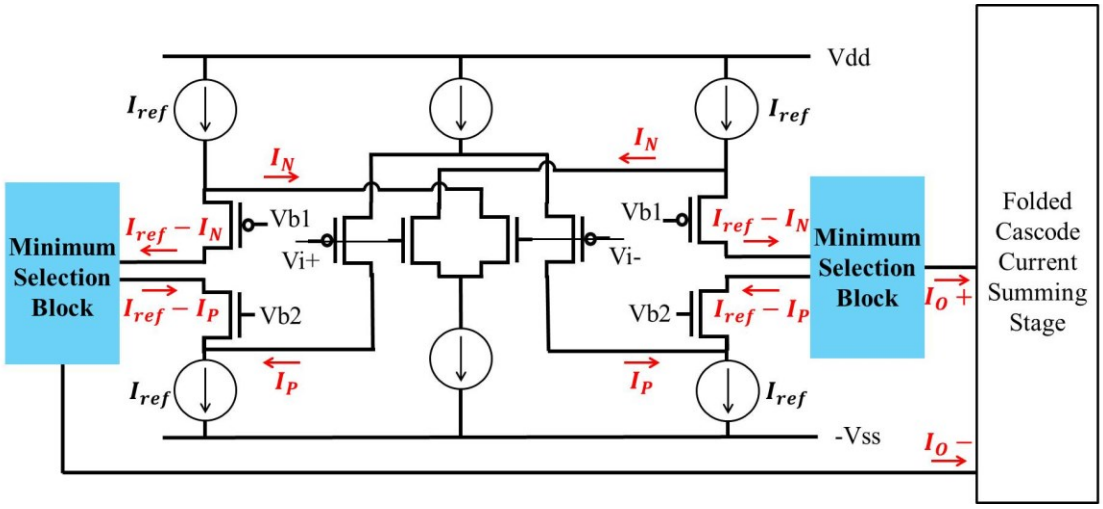


Figure 2.7 Minimum Current Selection Technique

On the other hand, when I_1 is smaller than I_2, $I_1 = I_{M5} = I_{M6} = I_{M7}$. In this situation, M2 works in triode region and M3 and M4 are turned off. Thus $I_O = I_{M7} = I_1$. As a result, the smaller current is selected as I_O for all cases.

Figure 2.7 shows the input stage circuit of minimum current selection technique. Two input currents of the minimum current selection block are $I_{ref} - I_N$ and $I_{ref} - I_P$. When the current of NMOS input pair, I_N, is larger than the current of PMOS pair, I_P,

$I_{ref} - I_N$ is smaller than $I_{ref} - I_P$, and $I_{ref} - I_N$ will be the output current of the minimum current selection block. Thus, the transconductance of NMOS input pair is transferred to the folded cascode current summing stage. If I_P is larger than I_N, $I_{ref} - I_P$ will be the output current of the minimum current selection block, and the transconductance of PMOS input pair is transferred to the next stage. As a result, total transconductance variation is same with the maximum current selection technique (Figure 2.5).

2.4 Level Shifting Technique

The previously explained techniques, in Chapter 2.3 and 2.4, require additional complex circuitry and often have degraded CMRR. To overcome these drawbacks, a simple constant transconductance rail-to-rail technique is proposed in [1]. This technique is level shifting technique and the input stage of this technique is illustrated in Figure 2.8. In this technique, two PMOS source followers are used for common mode input level shifting. The input signal of the amplifier is directly connected to the input of a PMOS source follower and N-channel input differential pair, and the output of the PMOS source follower is connected to the input of the P-channel differential pair. Thus, the shifted input signal is fed to the input of the P-channel differential pair.

$$V_{inp-sh} = V_{in} + |V_{gsp}|$$

$$|V_{gsp}| = V_{ovp} + |V_{thp}|$$

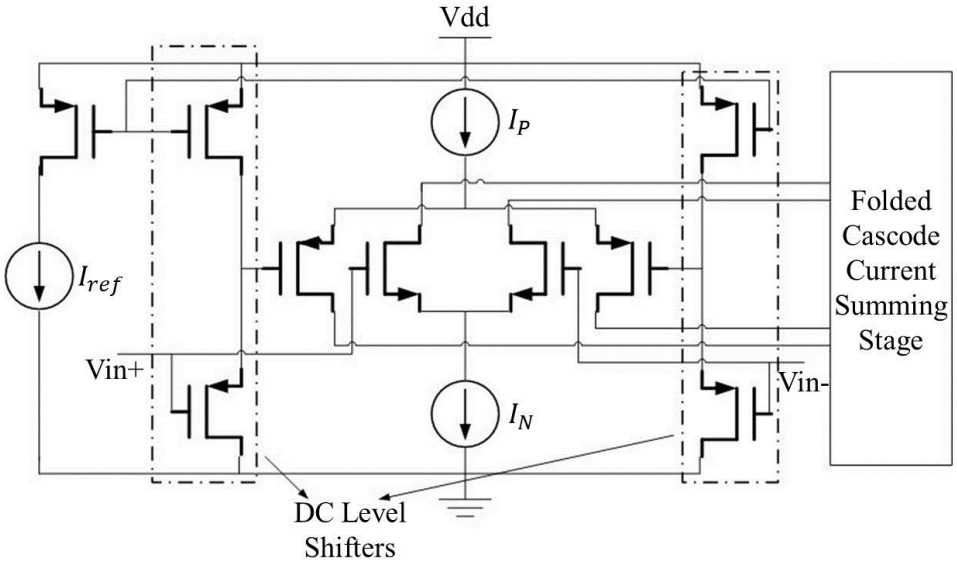


Figure 2.8 Input Stage of Level Shifting Technique

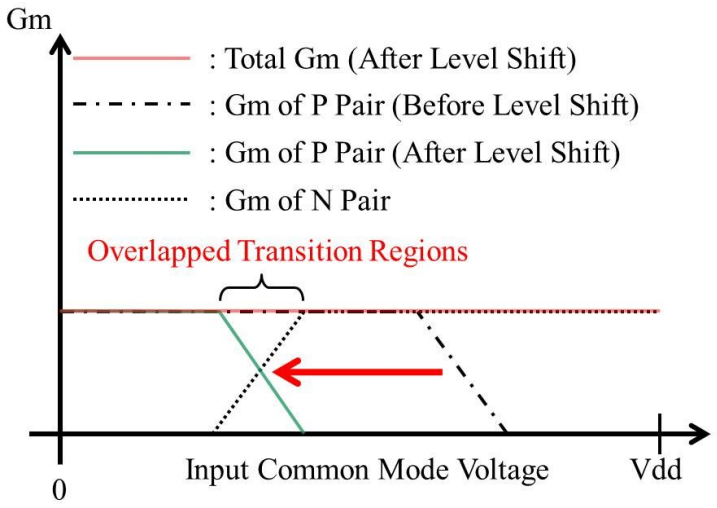


Figure 2.9 Total Transconductance of Level Shifting Technique

Where V_{inp-sh} is the shifted input signal (by the PMOS source follower) and V_{gsp} is the PMOS transistor gate-source voltage, and V_{ovp} and V_{thp} are the overdrive voltage and threshold voltage of the PMOS transistor, respectively. The current and transconductance of P-channel input differential pair are shifted towards the negative as much as $|V_{gsp}|$. As

a result, the transition regions of the N-channel and P-channel input differential pairs are overlapped.

The overall transconductance variation is shown in Figure 2.9. If PMOS source followers are not used to shift input common mode signal, the overall transconductance has doubles in the middle range of input common mode signal (Figure 1.2 (b)). But the transconductance of the PMOS input pair is shifted by the PMOS source follower and transition regions of NMOS and PMOS are overlapped (Figure 2.9). Therefore, total transconductance can be kept constant in the whole range of input common mode signal.

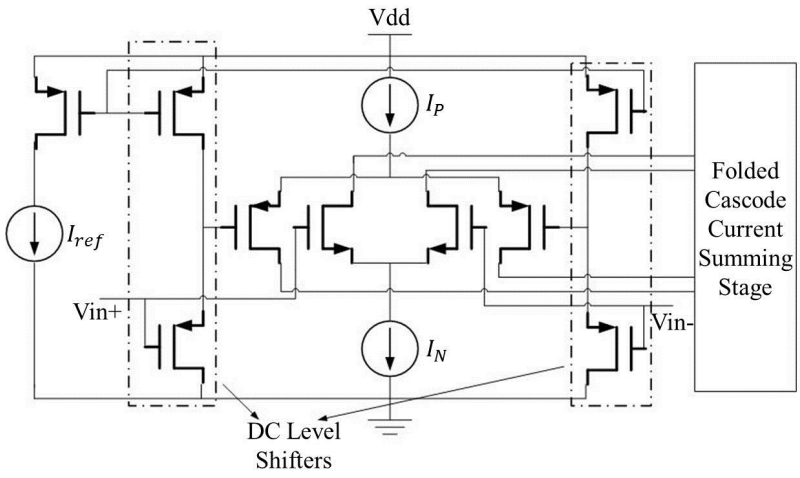
Chapter 3. Novel Low Supply Voltage Rail-to-Rail Op-Amps

In Chapter 2, some typical techniques which are previously proposed in the past years are briefly explained. In this chapter, three novel techniques for a constant transconductance rail-to-rail op-amp of low supply voltage environment are introduced. The first technique is new level shifting technique and the second one is saturation point control technique. The last technique is modified new level shifting technique which is hybrid of the first and the second technique.

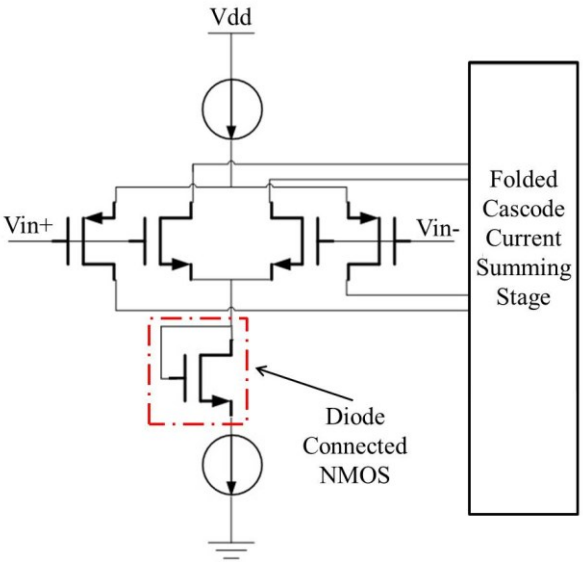
3.1 New Level Shifting Technique : The Simplest Technique

The conventional level shifting technique is proposed in [1] and briefly explained in Chapter 2. In [1], 1.2μm CMOS technology is used and the supply voltage is ±1.5V. New level shifting technique is designed with TSMC 0.25μm CMOS technology and 1.6V single supply voltage. For direct comparison, the conventional level shifting technique is re-designed and simulated with TSMC 0.25μm CMOS technology and 1.6V single supply voltage.

As explained in Chapter 2.4, the conventional level shifting technique is very simple and has no serious degradation of CMRR. New level shifting technique, however,



(a) Input Structure of Conventional Level Shifting Technique



(b) Input Structure of New Level Shifting Technique

Figure 3.1 Structure Comparison of Conventional and New Level Shifting Technique

has same concept and more simple structure. The conventional level shifting technique requires two PMOS source followers, totally four MOSFETs, but only one diode connected NMOS is employed for new level shifting technique. Figure 3.1 shows structure comparison of these two techniques. Figure 3.1 (a) is the input stage structure of

the conventional level shifting technique. Because of two PMOS source followers, the common mode input signal of PMOS differential input pair is shifted as much as $|V_{gsp}| = V_{ovp} + |V_{thp}|$ and the current and transconductance of PMOS input pair are shifted towards the negative as much as $|V_{gsp}|$ of PMOS source follower.

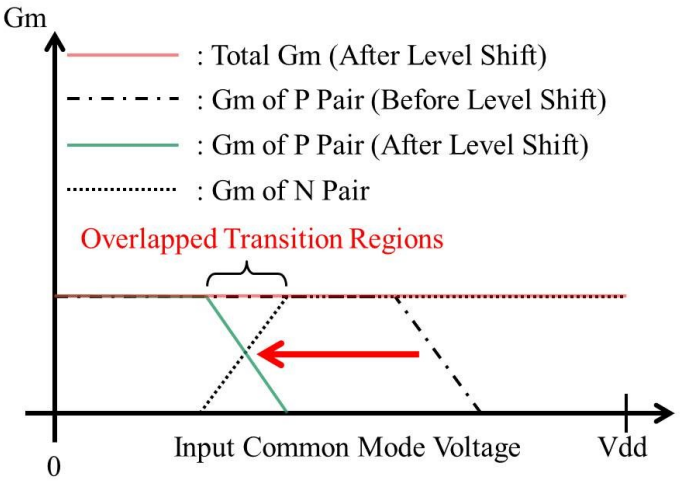
Figure 3.1 (b) shows the structure of new level shifting technique. There are complementary differential input pair operated in parallel and only one diode connected NMOS is added above the tail current source of the N-channel differential input pair. If a diode connected NMOS is not added, the structure is simply a conventional complementary differential input pair operated in parallel and the transconductance of the amplifier varies from gm to about 2gm in the middle range of the common mode input. For this conventional complementary differential input pair, the minimum input voltage of the N-channel input differential pair is given below.

$$V_{inn-min1} = V_{ovn} + V_{gsn}$$

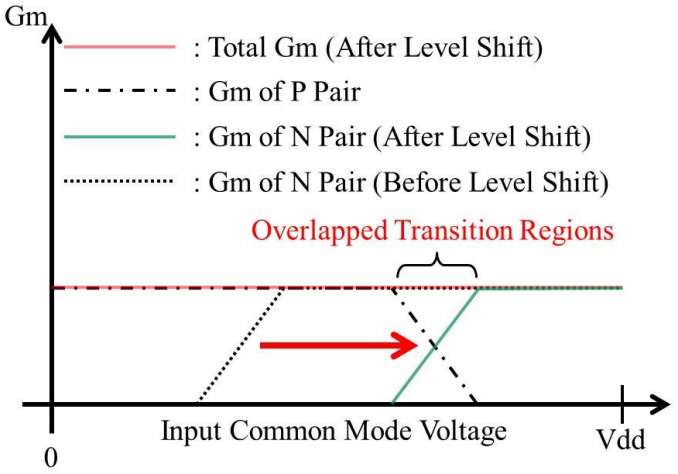
In the above equation, V_{ovn} is the overdrive voltage of NMOS tail current source and V_{gsn} is the gate-source voltage difference of the N-channel input differential pair. For the case of the proposed novel structure, the minimum input voltage of N-channel input differential pair is given below.

$$V_{inn-min2} = V_{ovn} + V_{gsn} + V_{gsn}$$

As shown in the above equation, another V_{gsn} is required because of diode connected NMOS above the NMOS tail current source. Thus, the current and transconductance of N-channel input differential pair are shifted as much as V_{gsn}. If $|V_{gsp}|$ of PMOS source



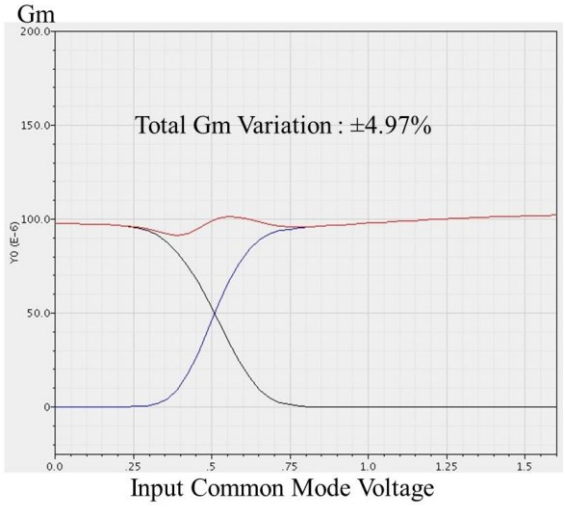
(a) Total Transconductance Variation of Conventional Level Shifting Technique



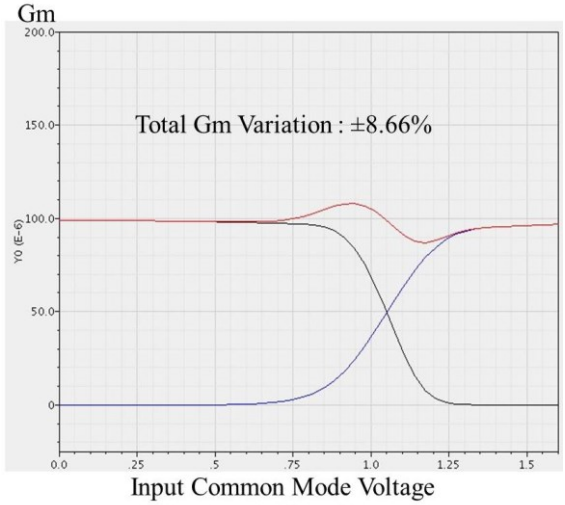
(b) Total Transconductance Variation of New Level Shifting Technique

Figure 3.2 Comparison of Total Transconductance Variation

follower of the conventional level shifting technique is same with V_{gsn} of diode connected NMOS of new level shifting technique, the shifting amount of two techniques is exactly same and the total transconductance variations have same result. Figure 3.2 shows the comparison of total transconductance variation concepts of two techniques.



(a) Simulation Result of Conventional Level Shifting Technique



(b) Simulation Result of New Level Shifting Technique

Figure 3.3 Simulation Results of Total Transconductance Variation

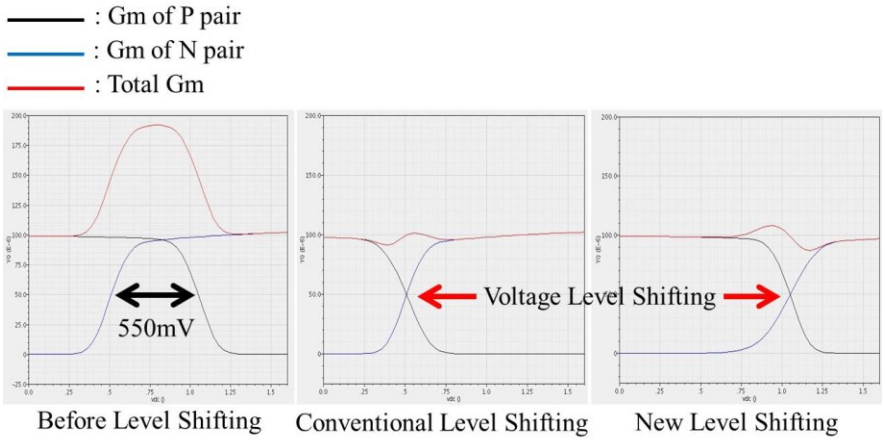
Figure 3.3 shows the simulation results of the total transconductance variations. Figure 3.3 (a) is the case of the conventional level shifting technique with 1.6V single supply voltage and TSMC 0.25μm technology. The result shows ±4.97% of total transconductance variation. The simulation result of new level shifting technique is shown in Figure 3.3 (b). Because of addition of diode connected NMOS, the slope of

transition region of NMOS is gentler than that of PMOS. This mismatch cause larger total transconductance variation and the result shows ±8.66% of total variation. To reduce this larger total transconductance variation, modified new level shifting technique is proposed in Chapter 3.3.

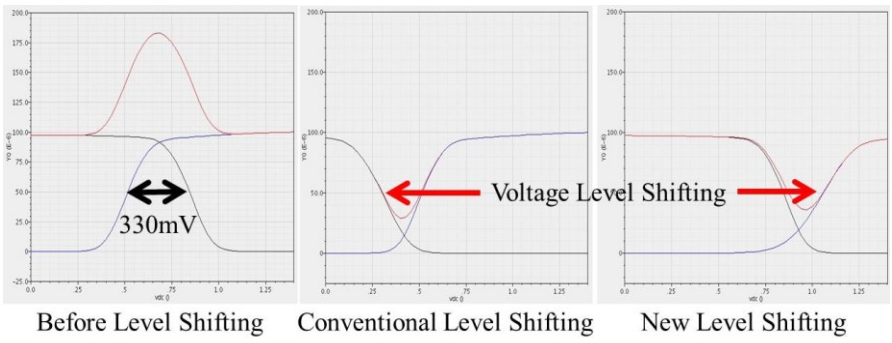
New level shifting technique proposed in this chapter requires only one MOSFET for a constant transconductance and that is the simplest technique for a rail-to-rail op-amp with low supply voltage environment. One drawback of this technique is relatively large total transconductance variation.

3.2 Saturation Point Control Technique

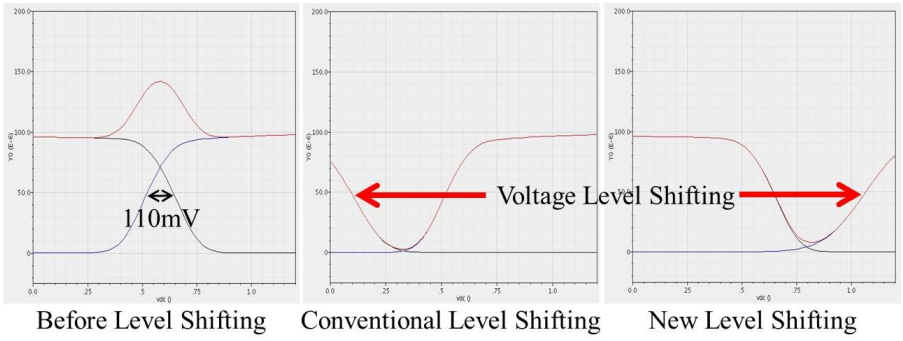
As mentioned before, the advantages of conventional and modified overlapped transition regions techniques using voltage level shifting are simplicity and high CMRR. One of the main drawbacks of those techniques, however, is a limited amount of voltage shifting. The comparison of two techniques, the conventional and new level shifting technique, is given in Chapter 3.1 with 1.6V single supply voltage. However, if supply voltage is lower than 1.6V, required amount of voltage shifting for a constant transconductance is smaller than what is required for a 1.6V supply voltage. Because of the minimum V_{gs} required for active mode operation of transistors, the voltage shifting amount of input common mode signal cannot be lower than the power supply limited amount of voltage shifting. Even if the shifted amount of input common mode signal is lower than the limited amount using sub-threshold current, the aspect ratio of transistors



(a) 1.6V Single Supply Voltage



(b) 1.4V Single Supply Voltage



(c) 1.2V Single Supply Voltage

Figure 3.4 Total Transconductance Variations with 1.6V, 1.4V, and 1.2V

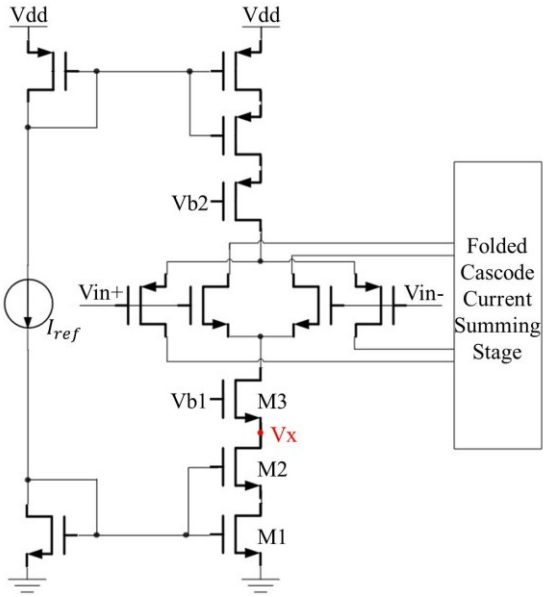
which are used to shift common mode input signal should be extremely large and those transistors cannot be used practically.

Figure 3.4 shows the simulation results of total transconductance variation for the conventional and new level shifting technique with the supply voltage of 1.6V, 1.4V, and 1.2V. TSMC 0.25-μm technology is used to simulate this work and the minimum threshold voltages of PMOS and NMOS are about -500mV and 450mV which are the minimum V_{gs} required for active mode operation of PMOS source follower and diode connected NMOS, respectively. The required voltage shifting amount for a constant transconductance is 550mV, 330mV, and 110mV with 1.6V, 1.4V, and 1.2V of supply voltage respectively. For the case of 1.6V supply voltage (Figure 3.4 (a)), required voltage shifting amount for a constant transconductance is 550mV which is larger than the minimum V_{gs} of PMOS and NMOS, and the simulation results show ±4.97% and ±8.66% variations of overall transconductance with aspect ratios of $(350/1)$ for PMOS source follower and $(77.5/1)$ for diode connected NMOS. However, with the same aspect ratios of PMOS source follower and diode connected NMOS, Figure 3.4 (b) and (c) show that overall transconductances cannot be kept constant because required voltage shifting amount for a constant transconductance is smaller than the minimum V_{gs}. Using sub-threshold drain current, overall transconductance can be kept constant, but the aspect ratios of PMOS source follower would need to be $(10^6/1)$ and $(10^9/1)$ with 1.4V and 1.2V supply voltages, respectively. For diode connected NMOS, $(3\times10^4/1)$ and $(3\times10^7/1)$ of the aspect ratio are required with 1.4V and 1.2V supply voltage. Those aspect ratios are obviously impractical and the conventional and new level shifting techniques have a limited amount of voltage shifting as a result.

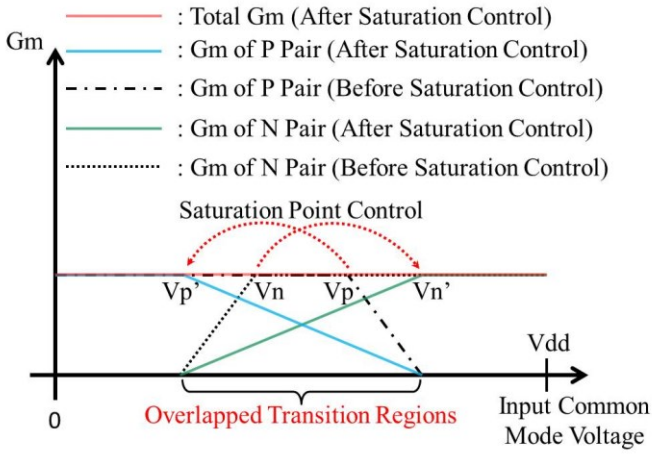
Basically, the concepts of the conventional and new level shifting technique are overlapped transition regions of the transconductances of NMOS and PMOS. With the DC voltage level shifting technique, another type of overlapped transition regions technique is also introduced in [1]. The main concept of that technique is saturation point control of current in N- and P-channel differential input pairs. This type of overlapped transition regions technique does not have a limited amount of voltage shifting. Proposed technique controls the aspect ratios of the input differential pairs transistors and the optimized aspect ratios for constant-gm are 1/5 and 1 for NMOS and PMOS respectively. As mentioned in [1], those aspect ratios are too small and degrade the noise performance and transistors mismatch insensitivity.

A novel overlapped transition regions technique proposed in this chapter has the same basic concept as a previously introduced technique that controls the current saturation points of differential input pairs. We do not control the aspect ratios of differential input pairs transistors, but rather control the saturation point of a current source.

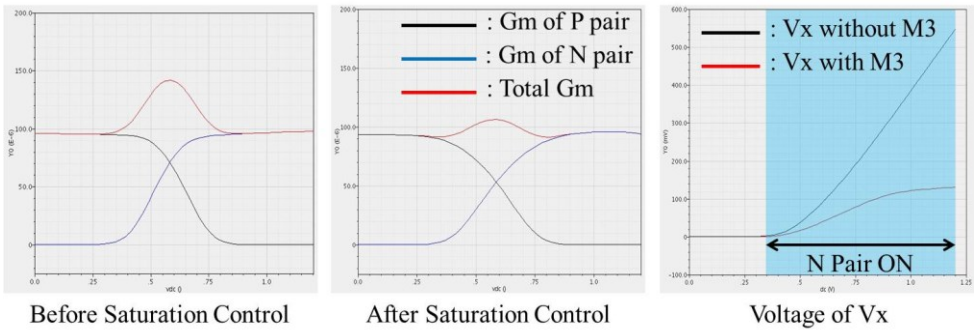
Figure 3.5 shows the structure and the basic working principle of saturation point control technique with simulation results. M1 and M2 in Figure 3.5 (a) are the current source of the N-channel input pair and M2 is added to lower transconductance variation in the saturation region. In Figure 3.5 (b), without saturation point control, the saturation point of current of the N-channel input pair is indicated as V_n. Without saturation point control, M3 is not added and V_x is voltage of sources of the N-channel input pair. With this condition, in the turn-on region, the triode region and the saturation region of N-channel



(a) Structure of Saturation Point Control Technique



(b) Working Principle



(c) Simulation Results with 1.2V Single Supply Voltage

Figure 3.5 Structure and Working Principle of Saturation Point Control Technique

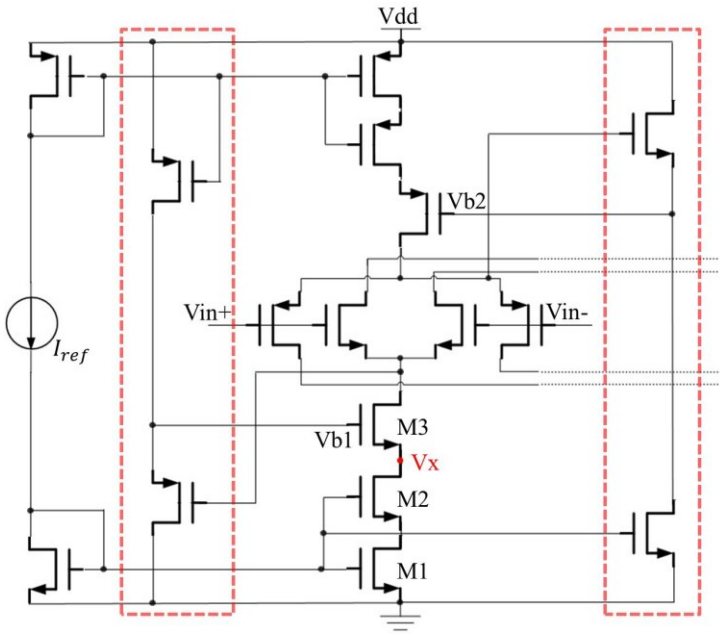
differential input pair, the voltage of V_x varies along with input common mode voltage (Figure 3.5 (c)). However, with saturation point control, the voltage of V_x is lowered because of the addition of M3 (Figure 3.5 (c)) and the voltage difference between the drain and source of M2, V_{dsM2}, is lowered. As a result, a larger input common mode voltage is needed to saturate M2 and the saturation point, V_n, is shifted to V_n' (Figure 3.5 (b)). In Figure 3.5 (c), the cut off voltage of the PMOS input pair is about 850mV of the input common mode voltage and that voltage must be the same as the shifted saturation point voltage of NMOS input pair, V_n'. For the saturation of M2 at 850mV of input common mode voltage, the voltage difference of V_{gsM2} and V_{thM2} must be the same as V_{dsM2}. V_{gsM2}, V_{thM2}, and V_{dsM2} are the gate-source voltage, threshold voltage, and drain-source voltage of M2 respectively. From the below equations, the value of V_x is about 160mV at 850mV of input common mode voltage and V_{b1} should be 880mV. The case of the P-channel input pair is symmetric with the case of the N-channel input pair and the value of V_{b2} is about 360mV when there is 300mV of input common mode voltage, which is the cut off voltage of N-channel input pair. The simulation result of saturation point control is shown in Figure 3.5 (c). For this simulation, 1.2V single supply voltage is used.

$$V_{gsM2} - V_{thM2} = V_{dsM2} \quad \text{(Saturation of M2)}$$

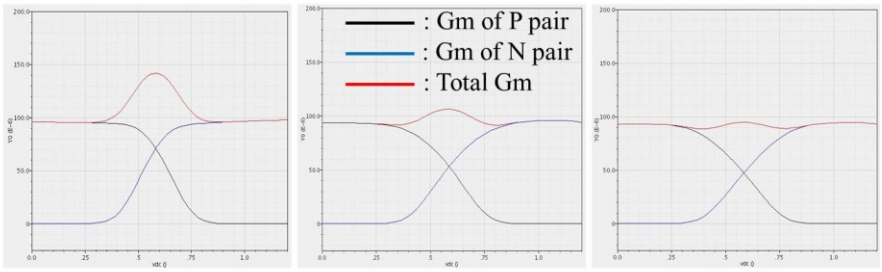
$$V_{gM2} - V_{sM2} - V_{thM2} = V_{dM2} - V_{sM2}$$

$$V_{gM2} - V_{thM2} = V_{dM2} = V_x$$

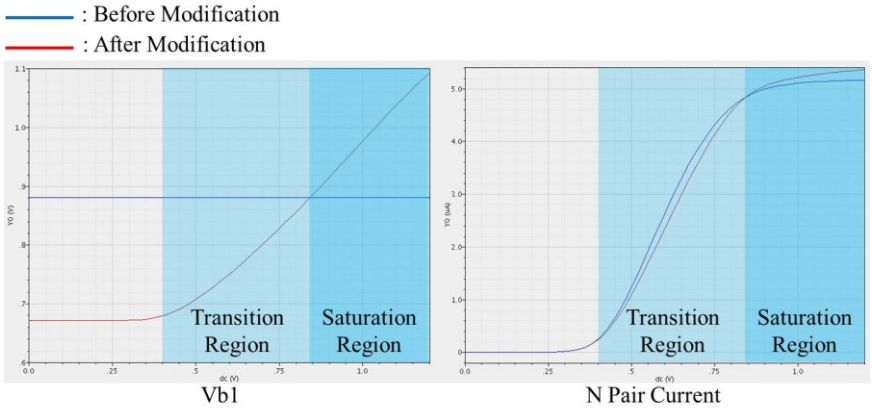
$$\left(\frac{1}{2}\right)\mu_n C_{ox}\left(\frac{W}{L}\right)_{M3}(V_{b1} - V_x - V_{thM3})^2 = I_{sat-M3}$$



(a) Structure of Modified Saturation Point Control Technique



(b) Simulation Results with 1.2V Single Supply Voltage



(c) V_{b1} and Current of NMOS Pair with Modified Technique

Figure 3.6 Modified Saturation Point Control Technique

The simulation result of Figure 3.5 (c) shows ±7.48% variation of overall transconductance and for better performance, some modification is required. Shifted saturation points, V_n' and V_p', are well controlled, but the variation of overall transconductance in the overlapped transition regions degrade the performance. To decrease this variation, the voltage of V_{b1} and V_{b2} are modified. Figure 3.6 (a) shows the structure of modified saturation point control technique. PMOS and NMOS source followers are added to control the voltage of V_n' and V_p', respectively. The input signal of the PMOS source follower comes from the sources of the N-channel input pair and this signal is the same as the signal of 'V_x without M3' of Figure 3.5 (c). PMOS source follower shifts this signal as much as $|V_{gs}|$ of PMOS and this shifted signal is connected to V_{b1}. Figure 3.6 (c) shows that before modification, V_{b1} is constant and cannot control the current of the N-channel input pair in the transition region. V_{b1} of the modified technique, however, varies along with the input common mode voltage and set to 880mV at 850mV of input common mode voltage to control V_n'. Thus, in the transition region of the modified technique, V_{b1} and V_{gs} of M3 are smaller than those of the unmodified technique. As a result, because of lowered V_{gs} of M3, the current of N-channel input pair is lowered in the transition region and the graph of transconductance is more linear than unmodified one (Figure 3.6 (c)). The case of the P-channel input pair is symmetric with the case of the N-channel input pair. The simulation result shows that the variation of overall transconductance of the modified saturation point control technique is ±3.35% (Figure 3.6 (b)).

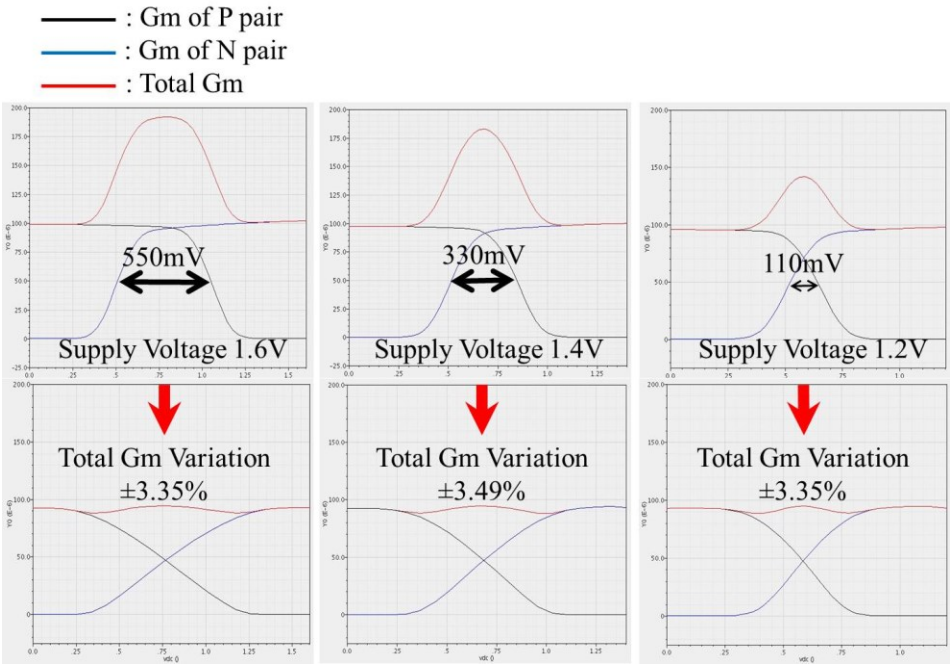


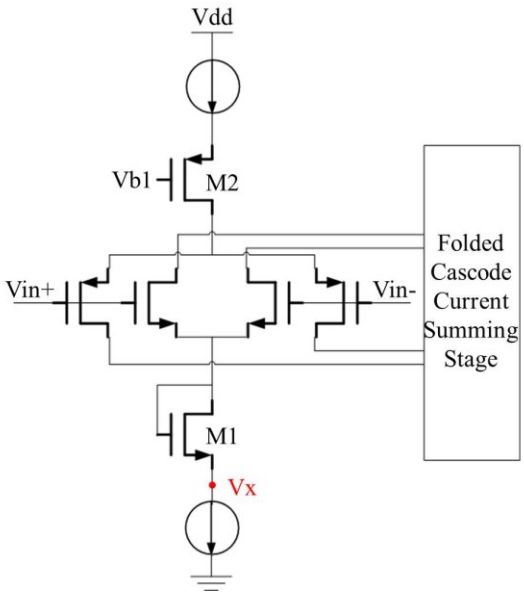
Figure 3.7 Total Transconductance Variations with Supply Voltage of 1.6V, 1.4V, and 1.2V

Figure 3.7 shows the simulation results of overall transconductance variation with supply voltage of 1.6V, 1.4V and 1.2V using the saturation point control technique which is the new overlapped transition regions technique proposed in this chapter. These results demonstrate that if overall transconductance is larger than the transconductance of N- or P-channel input pair in the middle range of common mode input signal, the saturation point control technique can be used generally with any supply voltage without limited amount of voltage shifting. In addition, with 1.6V supply voltage, the overall transconductance variation of the saturation point control technique is ±3.35% and better than the conventional and modified overlapped transition regions technique. Overall transconductance variations of the conventional and modified overlapped transition regions technique are ±4.97% and ±8.66%, respectively.

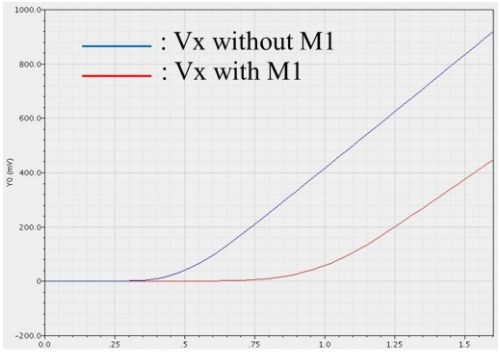
The saturation point control technique which is novel overlapped transition regions technique is introduced to overcome the drawback of the conventional and new level shifting technique. This technique has no limitation of voltage shifting amount which is one of main drawback of the conventional and new level shifting technique. Additionally, this technique has smaller total transconductance variation than that of the conventional and new level shifting technique with the same supply voltage even though this technique is slightly complicated.

3.3 Modified New Level Shifting Technique : Hybrid of 3.1 and 3.2

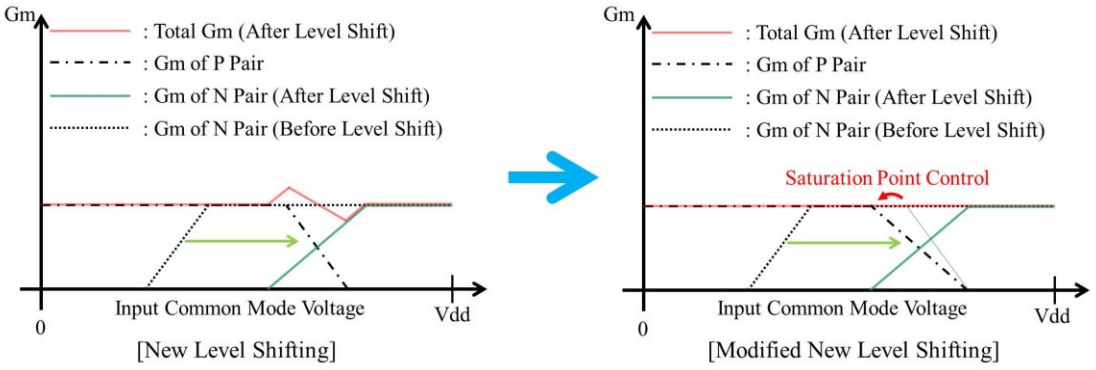
New level shifting technique is introduced in Chapter 3.1 and that is the simplest technique of constant transconductance rail-to-rail op-amp for the low supply voltage environment. As mentioned in Chapter 3.1, one of the main drawbacks is relatively large total transconductance variation, ±8.66%. That is caused by the slope mismatch of transconductance in the transition regions of NMOS and PMOS input differential pairs. Because of diode connected NMOS, the saturation point of NMOS input pair's current is shifted and that results in the gentle slope of NMOS transconductance in the transition region. In Chapter 3.2, saturation point control technique is proposed and that technique controls the saturation point of currents of NMOS and PMOS input differential pairs. Therefore, if the concept of saturation point control technique is employed for new level shifting technique, the slope mismatch of transconductance can be minimize.



(a) Structure of Modified New Level Shifting Technique



(b) Voltage of V_x

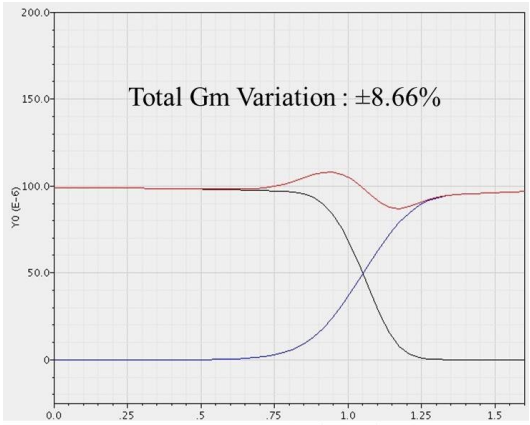


(c) Total Transconductance Variation

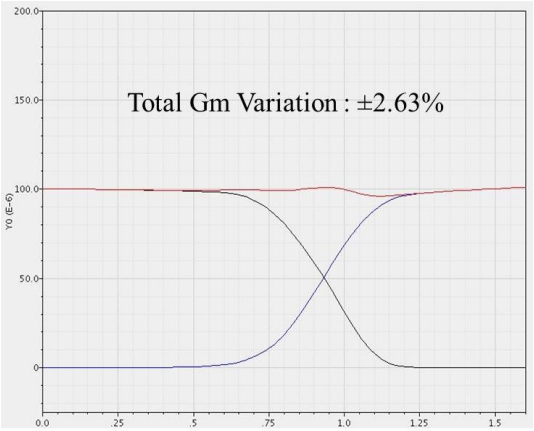
Figure 3.8 Structure and Working Principle of Modified New Level Shifting Technique

Figure 3.8 shows the structure and the working principle of modified new level shifting technique. The diode connected NMOS, M1, shifts the graph of voltage V_x as much as V_{gs} of M1 and that causes the shifting of transconductance of NMOS input pair. However, in turning on region of NMOS, the slope of V_x with M1 is gentler than that of V_x without M1 due to the diode connected NMOS, M1 (Figure 3.8 (b)). That is the source of slope mismatch of transconductance. The saturation point control technique introduced in Chapter 3.2 employs one NMOS above the NMOS tail current source and one PMOS below the PMOS current source to control saturation points of NMOS and PMOS input pairs' current. This concept is employed by modified new level shifting technique. In Figure 3.8 (a), M2 is added below the PMOS tail current source to control the saturation point of PMOS input pair current and the slope of PMOS transconductance is gentler than that of new level shifting technique (Figure 3.8 (c)).

Figure 3.9 shows the simulation results comparison of the total transconductance variations of two techniques. New level shifting technique has ±8.66% of total transconductance variation. But, modified new level shifting technique employs the saturation point control technique and only has ±2.63% of total transconductance variation. Modified new level shifting technique does not degrade the main advantage of new level shifting technique, simplicity, and dramatically reduces the total transconductance variation from ±8.66% to ±2.63%. Modified new level shifting technique requires only two MOSFETs. One is diode connected NMOS which is used to shift the transconductance of NMOS input differential pair and another is PMOS which is employed to control the saturation point of current of PMOS input differential pair.



(a) Simulation Result of New Level Shifting Technique



(b) Simulation Result of Modified New Level Shifting Technique

Figure 3.9 Comparison of Total Transconductance Variations

Chapter 4. Literature Review for Extremely Low Supply Voltage Op-Amp

4.1 Extremely Low Supply Voltage Environment

In Chapter 1, the total transconductance problems of low supply voltage and extremely low supply voltage environments are mentioned. As shown in Figure 1.2 and Figure 1.3, the dead zone problem of an extremely low supply voltage environment is totally different from the two-fold transconductance variation problem of a low supply voltage environment. For an extremely low supply voltage environment, some special techniques are required to increase the total transconductance of middle range of the input common mode signal to the level of the other regions of common mode input. In the dead zone of an extremely low supply voltage environment, the total transconductance is very small or almost zero. Therefore, the gain will be very small or almost zero and that is markedly different from the two-fold variation of the gain and the unity gain frequency in the low supply voltage environment. In the past years, several techniques have been proposed for an extremely low supply voltage op-amp. Some techniques use bulk of NMOS or PMOS input differential pair as a input node to avoid the dead zone, and some techniques modify or compress the input signal into the acceptable region of NMOS or PMOS input differential pair. In the following sections of

this chapter, four typical techniques for an extremely low supply voltage environment are explained.

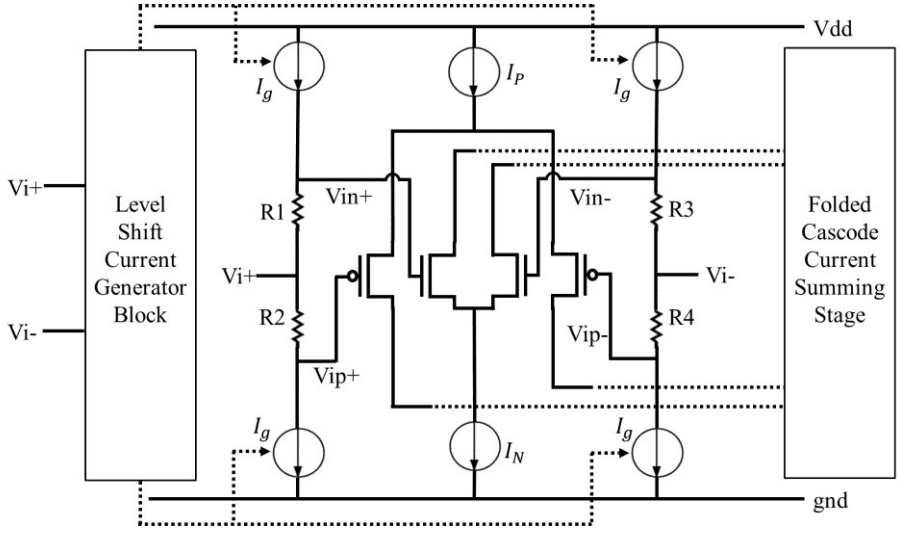
4.2 Dynamic Level Shifting Technique

Dynamic Level shifting Technique was first proposed in [14] and later studied in [15] ~ [17]. The basic concept of this technique is shown in Figure 4.1. Two inputs are directly connected to the resistors, R1 ~ R4. The top and bottom of resistors are connected to the variable current sources, I_g, which currents are generated by the level shift current generator. The conceptual graph of the generated current is shown in Figure 4.1 (b). The generated current, I_g, is controlled by the common mode input signal. When the common mode input signal is around the supply rail, ground or V_{dd}, the I_g is zero and at the middle point of the common mode input signal, the I_g reaches the maximum value. The input common mode voltages of NMOS and PMOS input pairs are given by

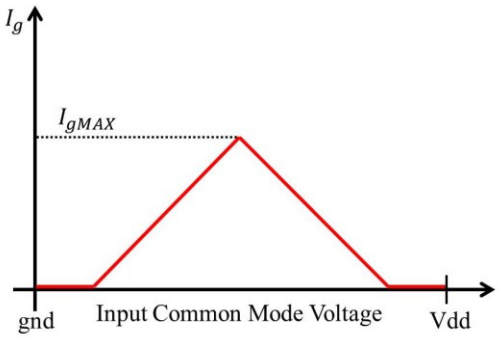
$$V_{iCMN} = V_{iCM} + I_g \times R$$

$$V_{iCMP} = V_{iCM} - I_g \times R$$

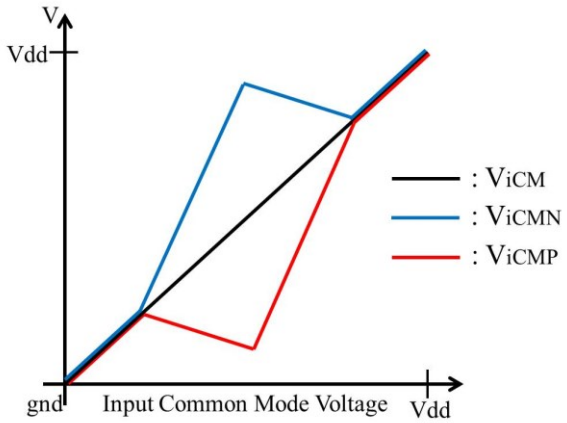
Where V_{iCMN} and V_{iCMP} are the input common mode voltages of NMOS and PMOS input pairs, respectively, and V_{iCM} is the original input common mode voltage. Figure 4.1 (c) shows the conceptual graph of V_{iCMN}, V_{iCMP} and V_{iCM}. In the left half region of the figure, the input common mode voltage of PMOS input pair, V_{iCMP}, exists in the acceptable region of PMOS input pair and the input common mode voltage of NMOS input pair,



(a) Conceptual Input Circuit of Dynamic Level Shifting Technique



(b) Current from the Level Shift Current Generator Block



(c) Shifted Input Common Mode Voltage of NMOS and PMOS Input Pairs

Figure 4.1 Basic Concept of Dynamic Level Shifting Technique

V_{iCMN}, exists in the acceptable region of NMOS input pair in the right half region. Therefore, the dead zone problem can be resolved by this technique.

The main part of this technique is the level shift current generator. Figure 4.2 (a) shows the level shift current generator block. Some equations for the explanation of this block are given below.

$$I_1 = I_N + I_B$$

$$I_2 = I_P + I_B$$

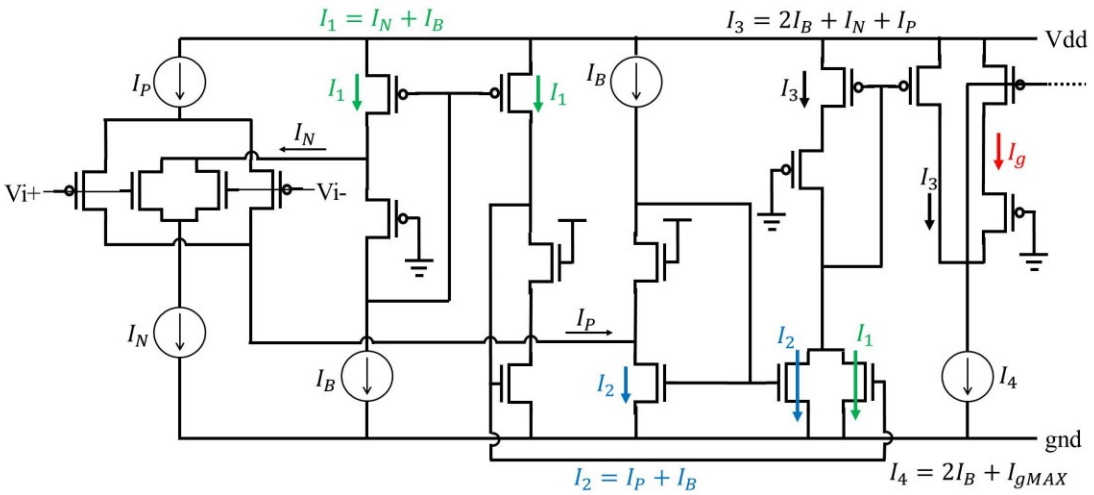
$$I_3 = 2I_B + I_N + I_P$$

$$I_4 = 2I_B + I_{gMAX}$$

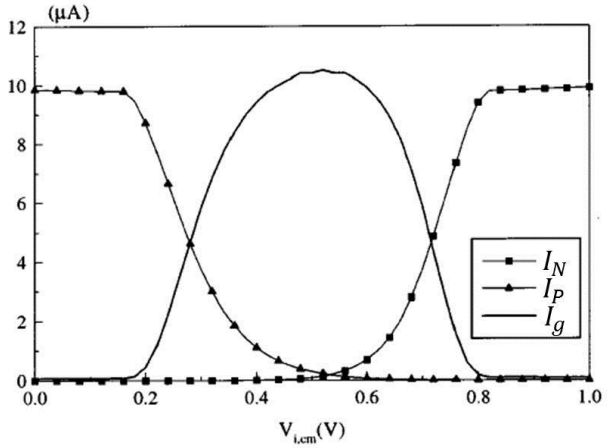
$$I_g = I_{gMAX} - (I_N + I_P)$$

The generated current, I_g, is current difference of I_3 and I_4, and that is difference of I_{gMAX} and $(I_N + I_P)$. When I_{gMAX} is larger than $(I_N + I_P)$, I_g is $I_{gMAX} - (I_N + I_P)$ and I_g is zero if I_{gMAX} is equal or smaller than $(I_N + I_P)$. Thus, in the middle range of input common mode signal, both pairs are turned off which means $(I_N + I_P)$ is zero, and I_g will be I_{gMAX}. Figure 4.2 (b) and (c) show simulation results of generated current, I_g, and input common mode voltages of NMOS and PMOS input pairs, V_{iCMN} and V_{iCMP}.

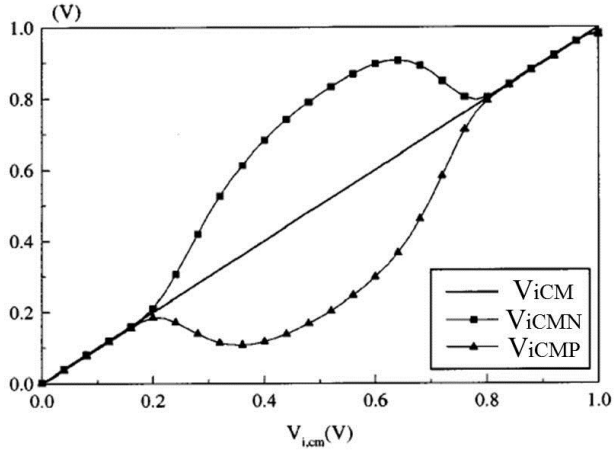
The basic concept of the dynamic level shifting technique is that the voltage shifting amount of input common mode signal is controlled by the common mode voltage. There is no voltage shifting around the supply rails, ground or V_{dd}, but in the



(a) Level Shift Current Generator Block



(b) Simulation Result of Generated Current I_g [15]



(c) Simulation Result of Input Common Mode Voltage of NMOS and PMOS Input Pairs [15]

Figure 4.2 Current Generator Block & Shifted Common Mode Voltages

middle range of the input common mode signal, the common mode voltages of NMOS and PMOS input pairs are shifted into the acceptable range of NMOS and PMOS input pairs. Thus, the dead zone problem can be avoided using this technique. In the input structure of this technique, however, two input signals of op-amp are directly connected to the resistors and this technique has finite input impedance. As mentioned in Chapter 1, one of the main requirements of the ECG amplifier is very high input impedance, almost infinity. Therefore, this technique is not suitable for the portable ECG amplifier.

4.3 Bulk Driven Input Stage Technique

In [18] and [19], several types of bulk driven input stage technique are proposed. The basic concept of bulk driven input stage technique is using bulk transconductance, g_{mb}, rather than g_m which is the transconductance when the gate of MOSFET is used as an input node. Usually, the gate of MOSFET is used as an input node and the voltage difference of gate and source of input MOSFET, V_{gs}, has to be larger than the threshold voltage, V_{th}, to turn on the input MOSFET. This threshold voltage of input MOSFET makes the dead zone problem difficult to avoid for the extremely low supply voltage environment. If the bulk of input MOSFET is used as an input node, however, the input MOSFET is turned on with very small input voltage even though the input voltage is smaller than the negative supply rail. Figure 4.3 ([19]) shows the comparison of gate driven case and bulk driven case. For the gate driven case, the bulk is connected to the source of NMOS which is grounded, and for the bulk driven case, the gate of NMOS is

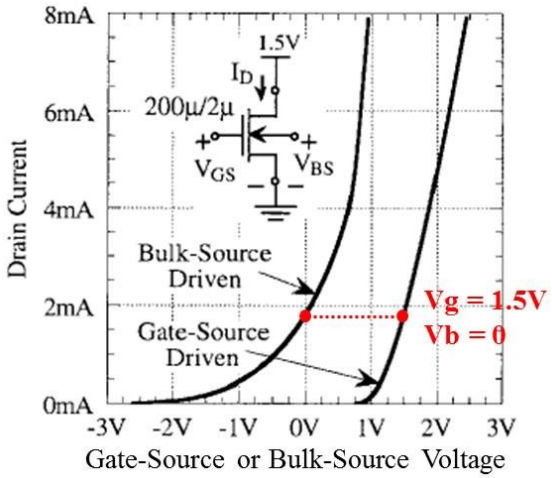


Figure 4.3 Comparison of Gate Driven and Bulk Driven [19]

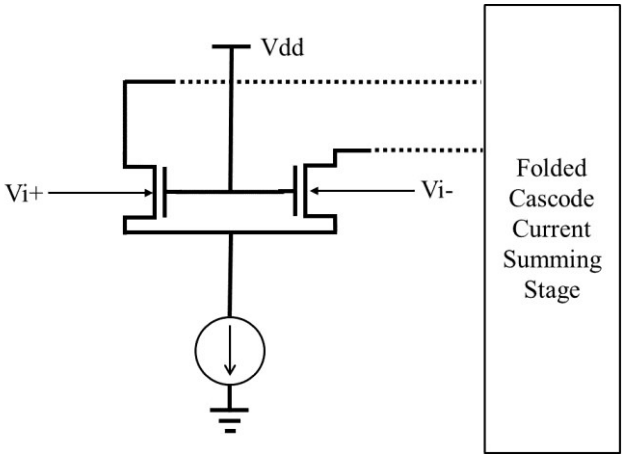


Figure 4.4 Concept of Bulk Driven Input Technique

connected to V_{dd}. In these cases, the supply voltage range is from ground to 1.5V. When the gate is used as an input node, the input voltage should be larger than about 1V to turn on the MOSFET. But for the bulk driven case, the MOSFET is turned on in the whole range of input voltage from 0 to 1.5V. Thus, the rail-to-rail input stage can be achieved using bulk driven input technique. Figure 4.4 shows simple conceptual input structure of bulk driven input stage technique.

One of the main disadvantages of this technique is low input impedance. As mentioned in Chapter 4.2, very high input impedance is required for the portable ECG amplifier. Another disadvantage of this technique is that g_{mb} is usually smaller than g_m. Thus, large body effect coefficient, γ, is required because bulk transconductance, g_{mb} is proportional to the body effect coefficient, γ. Because of these disadvantages, this technique is not appropriate for the portable ECG either.

4.4 Depletion Mode Input Pair Technique

The depletion mode input pair technique is proposed in [20]. The depletion mode MOSFET has a physically implanted channel. Because a channel is formed intrinsically, the depletion mode MOSFET has drain current even if the voltage difference between the gate and source is zero or negative. Figure 4.5 shows the current characteristic comparison of N-channel depletion mode MOSFET and enhancement mode MOSFET. Depletion mode input pair technique employs the depletion mode MOSFETs as an input pair and has no dead zone problem because the depletion mode MOSFET has intrinsic channel and negative value of the threshold voltage, V_{th} (Figure 4.6).

In this technique, because the input signal is directly connected to the gate of the depletion mode input pair, the input impedance of this structure is very high, almost infinity. Using this high input impedance characteristic of depletion mode input pair technique, hybrid type of depletion mode input pair technique and bulk driven input technique is proposed in [18]. Basic concept of the input stage of this technique is shown

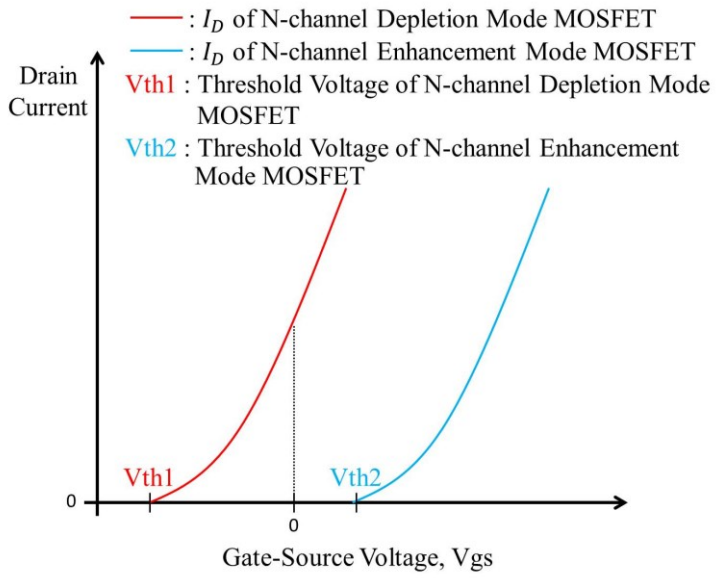


Figure 4.5 Current Characteristic Comparison

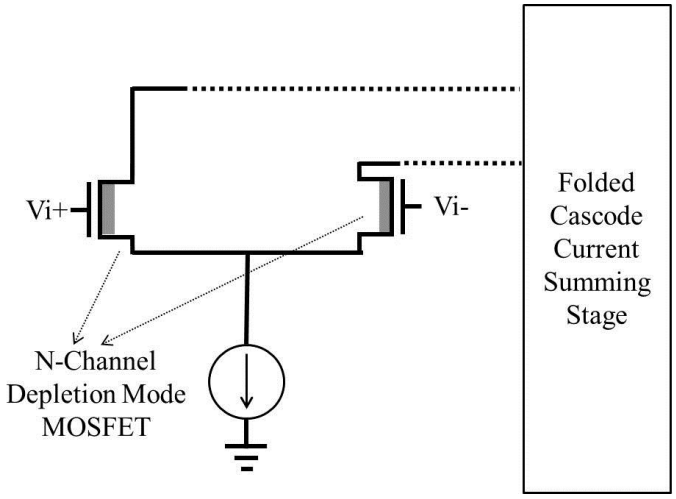


Figure 4.6 Concept of Depletion Mode Input Pair Technique

in Figure 4.7. Because the depletion mode input pair technique is employed, the input impedance of this structure is quite high, and the source of the depletion mode NMOS input differential pair is connected to the bulk of the PMOS pair. Thus, the original input signal is shifted by the depletion mode NMOS input differential pair and this shifted

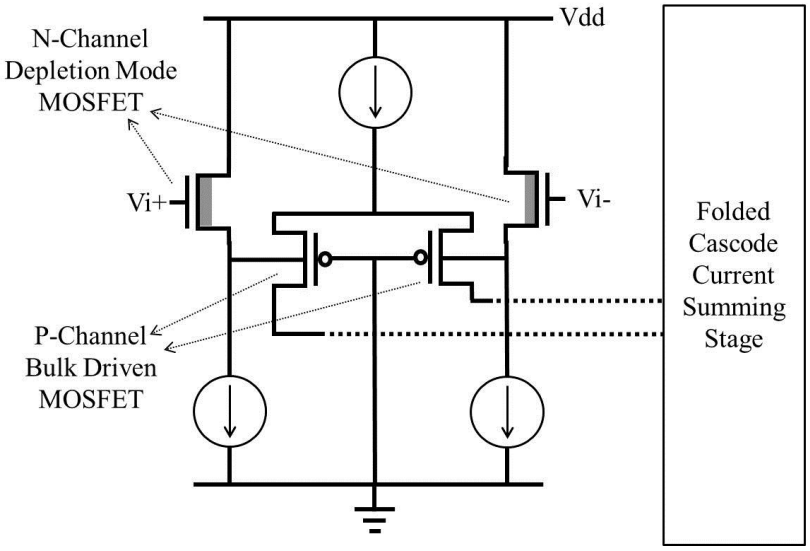


Figure 4.7 Hybrid Type of Depletion Mode Input and Bulk Driven Input Techniques

input signal is fed to the bulk of the PMOS pair which is the input pair of bulk driven input technique.

Depletion mode input pair technique overcomes the dead zone problem of the extremely low supply voltage environment with very high input impedance. However, the depletion mode MOSFET cannot be fabricated by the standard CMOS processes ([21]) and requires extra costs and processes. That is the main disadvantage of this technique.

4.5 Input Signal Compression Technique

Another technique to overcome dead zone problem of the extremely low supply voltage environment is input signal compression technique proposed in [21 and 22].The

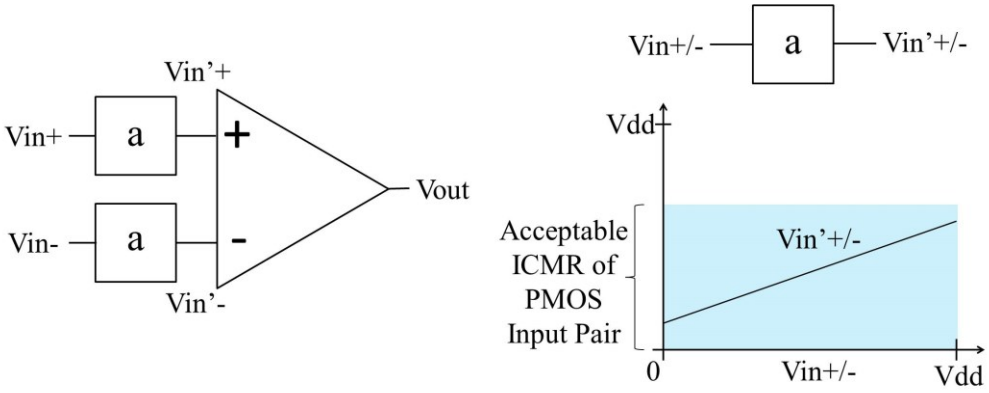
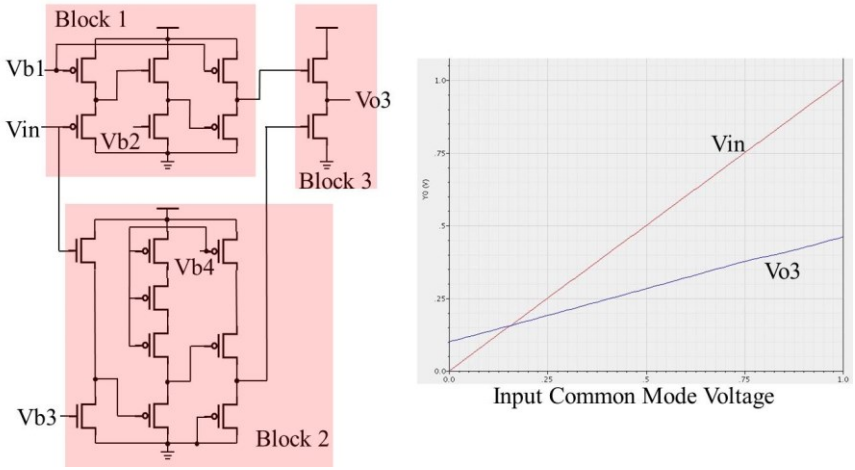


Figure 4.8 Basic Concept of Input Signal Compression Technique

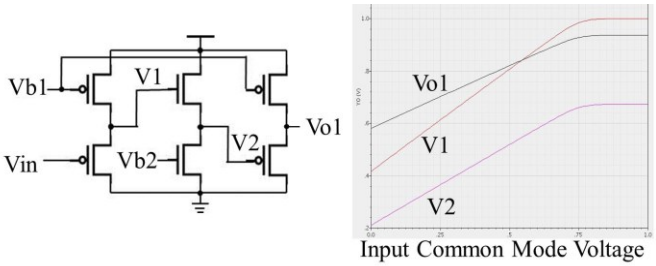
basic concept of this technique is that the rail-to-rail input common mode signal is compressed by the input signal compression block indicated as block 'a' in Figure 4.8 into the acceptable range of PMOS input pair of op-amp. Because this technique employs the PMOS pair input stage, not the complementary differential input structure, and the original input signal is compressed into the acceptable range of PMOS input pair, the dead zone problem can be avoided. Figure 4.8 shows the basic concept of this technique.

Figure 4.9 (a) shows the inside of block 'a', which is composed of 3 sub blocks. The input/output voltage characteristics of each block are shown in Figure 4.9 (b), (c) and (d). Block 1 consists of a PMOS source follower in the first stage, a NMOS source follower in the second stage, and a PMOS source follower in the last stage (Figure 4.9 (b)). This cascade of source followers shifts the input signal and the output voltage of block 1, V_{o1}, is shown in the graph.

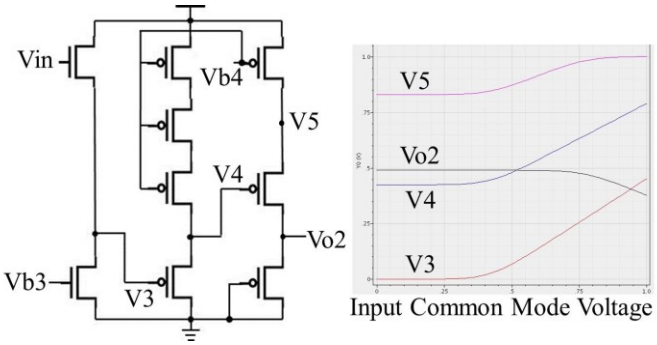
The first and the second stage of block 2 are a NMOS and a PMOS source follower, respectively (Figure 4.9 (c)). At the last stage of block 2, the output voltage V_{o2}



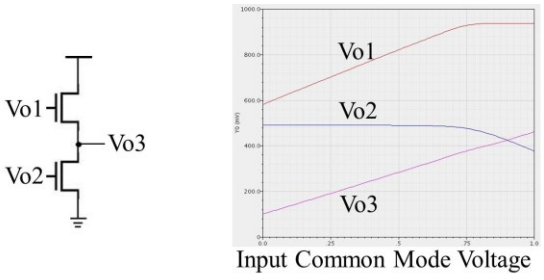
(a) Input Signal Compression Block



(b) Working Principle of Block 1



(c) Working Principle of Block 2



(d) Working Principle of Block 3

Figure 4.9 Basic Concept of Input Signal Compression Technique

is constant for low V_4 because of source follower operation of the last stage of block 2, while that works as a common-source amplifier which inverts V_4 voltage for high V_4. Figure 4.9 (c) shows the overall behavior of block 2.

Two inputs of block 3 are V_{o1} and V_{o2}. V_{o3} is the output of block 3 as well as the whole block of signal compression, block 'a' (Figure 4.9 (d)). When V_{in} is low, V_{o2} is constant and block 3 operates as a NMOS source follower. On the other hand, when V_{in} is high, V_{o1} is constant and block 3 inverts the signal of V_{o2}. The rail-to-rail input signal V_{in} is compressed as V_{o3} through block 'a', input signal compression block.

Using this concept of input signal compression, the dead zone problem of the extremely low supply voltage environment can be avoided. This input signal compression technique, however, has some drawbacks. First, the signal compression block, block 'a', is very complex and second, this technique has reduced bandwidth as mentioned in [22]. The third one is signal to noise ratio, SNR. In input signal compression technique, the original input signal is compressed by the signal compression block and this compressed input signal is fed to the PMOS input pair op-amp. The compressed differential input signal is obviously smaller than the original differential input signal. Therefore, the SNR of input signal compression technique is worse than that of other techniques which use the original differential input signal.

Chapter 5. Novel Extremely Low Supply Voltage Rail-to-Rail Op-Amps

5.1 Common Mode Elimination Technique

In Chapter 4.5, the input signal compression technique is briefly explained. Even if that technique has some drawbacks, the input signal compression technique does avoid the dead zone problem of the extremely low supply voltage. This technique works very well in the extremely low supply voltage environment, but we cannot achieve additional CMRR advantage from that technique, and has been stated before, portable ECG amplifiers require very high CMRR because of common mode noise from other muscles of human body.

In this chapter, a novel common mode elimination technique for the extremely low supply voltage environment is proposed using the basic concept of input signal compression technique. In Figure 5.1, the basic concept of novel common mode elimination technique is shown. Block ‘a’ is the signal compression block of input signal compression technique explained in Chapter 4.5. Using signal inverting block, named block ‘b’, and resistors, common mode input signal from 0 to 1V can be kept constant. While differential input signal is extracted and transferred to the following conventional PMOS input differential amplifier. The compressed input signal which is the output signal of block ‘a’ is inverted by block ‘b’ and using the ratio of two resistors, rail-to-rail

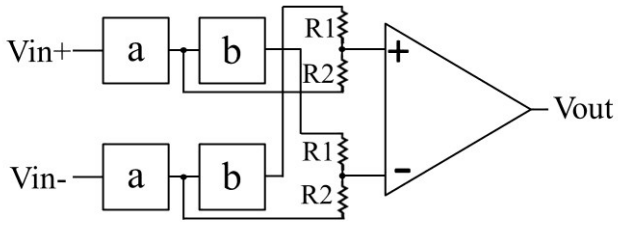
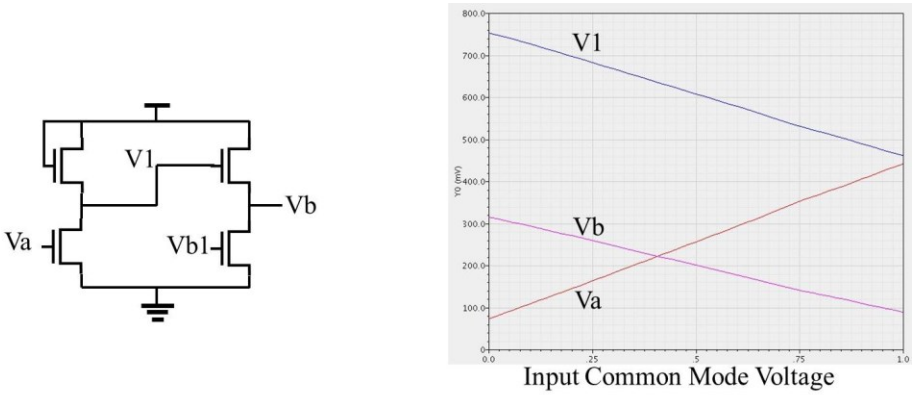
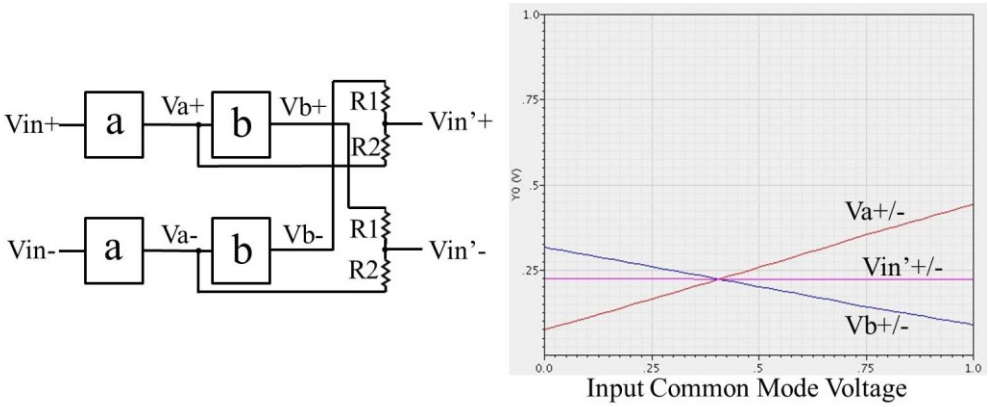


Figure 5.1 Structure of Common Mode Elimination Technique



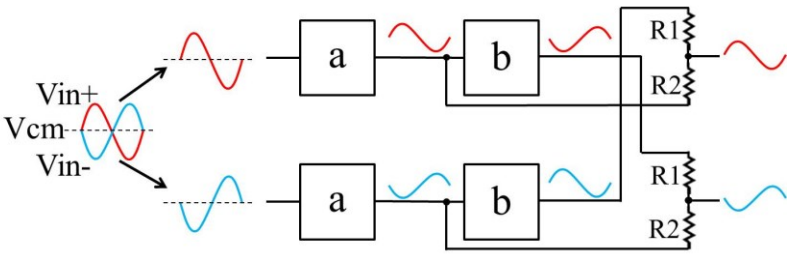
(a) Signal Inverting Block, Block 'b'



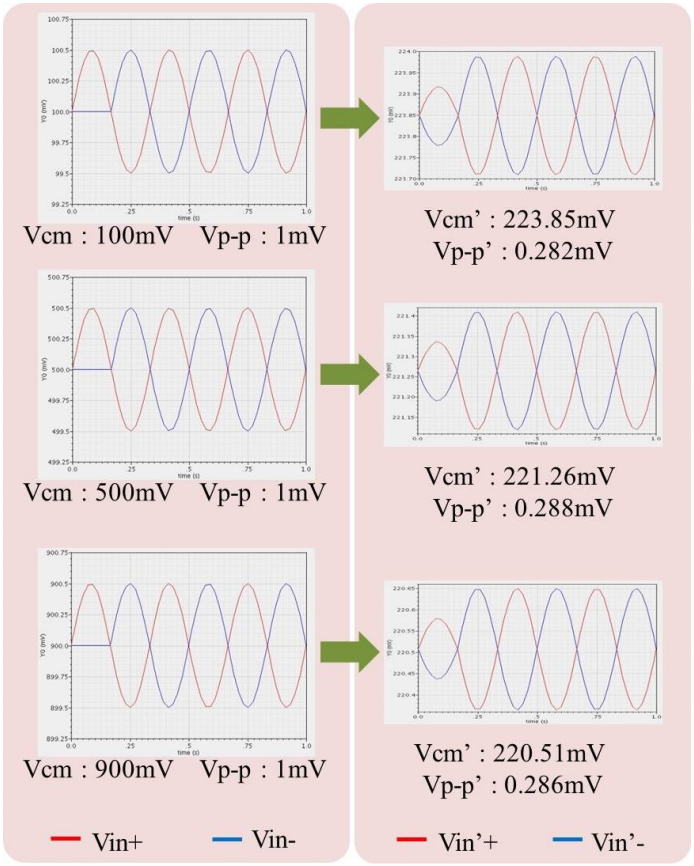
(b) Common Mode Elimination Block Followed by Op-Amp and Simulation Result

Figure 5.2 Basic Concept of Common Mode Elimination

variation of the input common mode signal is fixed at the crossing point of V_a and V_b which are the output signal of block 'a' and 'b' respectively. While differential input signal is still 'alive' and transferred to the following amplifier because V_a and V_b are cross connected when they are connected to resistors (Figure 5.2 and Figure 5.3).



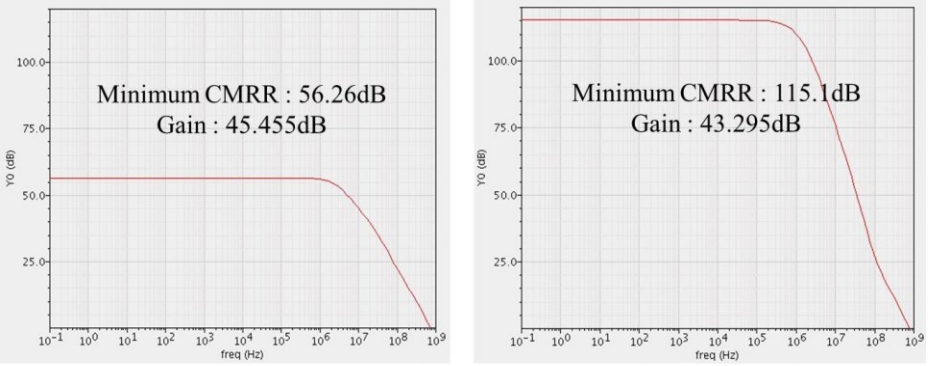
(a) Basic Concept of Differential Input Signal Extraction



(b) Simulation Result of Differential Input Signal Extraction

Figure 5.3 Differential Input Signal Extraction

Figure 5.4 shows the simulation results of minimum CMRR of input signal compression and common mode elimination technique. For input signal compression technique, rail-to-rail signal variation, 0 to 1V, compressed from 72.6mV to 449.4mV



[Input Signal Compression Technique] [Common Mode Elimination Technique]

Figure 5.4 Comparison of Minimum CMRR

and that means 62.32% of compression rate for common mode and differential signal. For the common mode elimination technique, the differential signal is compressed by about 71.4% as shown in Figure 5.2 (e). Because of the compressed differential signal, the common mode elimination technique has some loss of gain, but because of eliminated common mode signal, high CMRR has been obtained.

However, even if this technique has ultra-high CMRR using common mode elimination technique, the original disadvantages of the input signal compression technique are not resolved. This common mode elimination technique still employs a complex input signal compression block, block ‘a’, and has a reduced bandwidth. In addition, the signal to noise ratio, SNR, of common mode elimination technique is worse than that of input signal compression technique. Because the compression rate of common mode elimination technique is higher than that of input signal compression technique, the compressed differential input signal which is fed to the PMOS input pair op-amp of common mode elimination technique is smaller than that of the input signal compression technique. So, a novel technique for the extremely low supply voltage

environment is proposed in the following section to resolve these drawbacks of input signal compression and common mode elimination techniques.

5.2 New Input Signal Compression Technique

As mentioned in Chapter 4.5 and 5.1, input signal compression technique and common mode elimination technique have some disadvantages and modified technique which is more appropriate for the portable ECG system is required to overcome those disadvantages. In this chapter, new input signal compression technique which is the modified version of input signal compression and common mode elimination techniques is proposed to overcome some drawbacks of the previous techniques. Both the input signal compression technique and the common mode elimination technique employ a conventional PMOS input because the compressed input signal and common mode eliminated signal are located in the acceptable common mode range of PMOS input pair. For a novel input signal compression technique, however, the complementary differential input pair structure is employed. Figure 5.5 shows the structure of proposed novel input signal compression technique. For common mode input signal technique, only one common mode elimination block which is composed of 2 blocks of ‘a’, 2 blocks of ‘b’, and 4 resistors is required for the PMOS input pair op-amp. For a novel input signal compression technique, however, one more common mode elimination block is required for the complementary differential input pair op-amp which has both PMOS and NMOS input pairs.

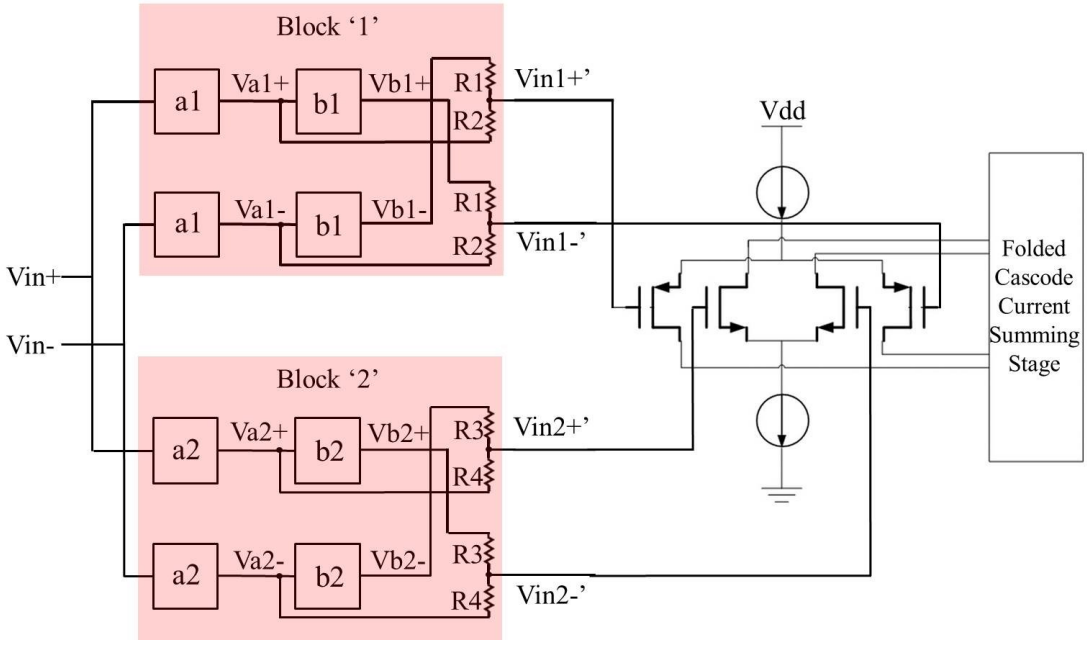


Figure 5.5 Structure of New Input Signal Compression Technique

Figure 5.6 shows working principle and the structure of block '1' which is composed of block 'a1', 'b1', and 4 resistors for PMOS input pair. The block a1 is a simple input signal compression block which is a NMOS source follower, not the complex input signal compression block which is employed in input signal compression and common mode elimination techniques, and the block b1 is a signal inverting block which is very similar with that of the common mode elimination technique. In region I, the block a1 is turned off and differential input signal is not transferred to the PMOS input pair. The block a1 is turned on in region II and III, but the transferred differential input signal of region II is smaller than that of region III because in region II, the NMOS source follower of the block a1 is in triode region and signal compression rate is higher than that of region III. This differential signal loss will be compensated by the signal from the block '2' which is connected to the NMOS input pair.

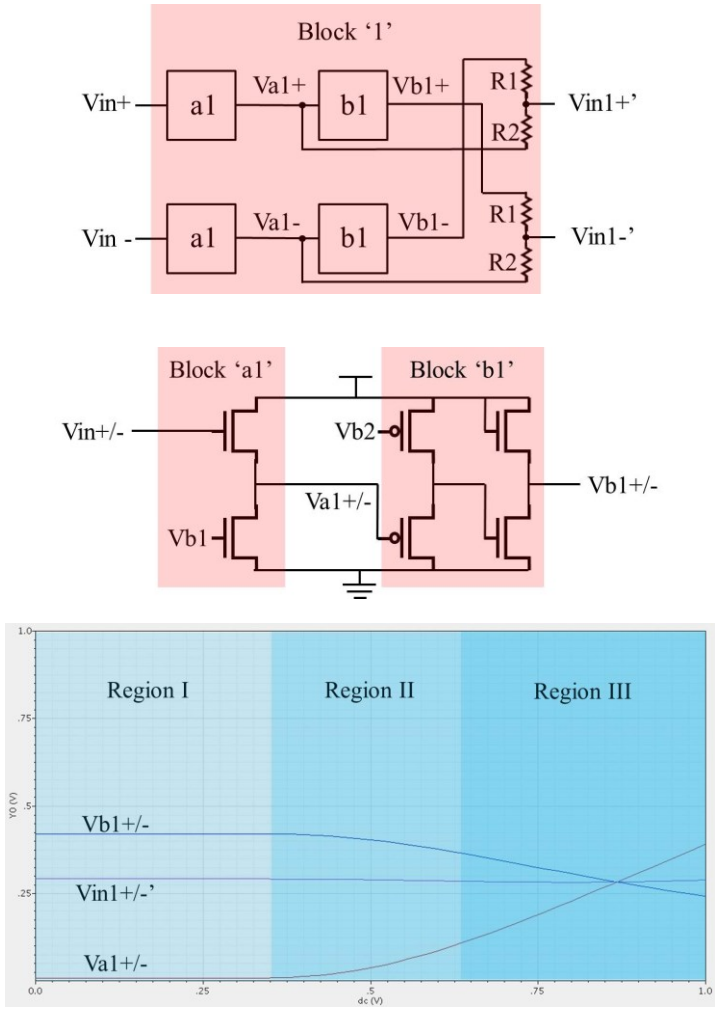


Figure 5.6 Structure and Working Principle of Block '1'

The structure and working principle of the block '2' which is similar to the block '1' is shown in Figure 5.7. The block a2 is an input signal compression block which is a simple PMOS source follower and the block b2 is a signal inverting block. In region I, only compressed differential input signal of the block '2' is transferred to NMOS input pair because the block a1 is turned off and no differential input signal from the block '1' is transferred to PMOS input pair. In region II, compressed differential input signal of the block '2' which is smaller than that of region I compensate the compressed differential

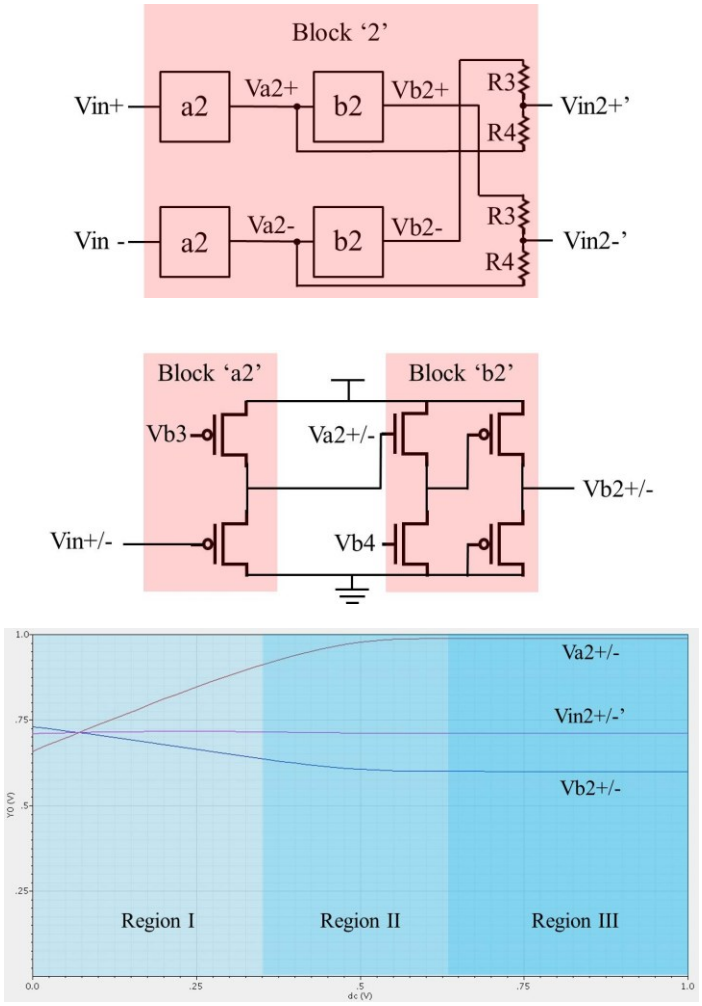


Figure 5.7 Structure and Working Principle of Block '2'

input signal of the block '1'. The block a2 is turned off in region III and no differential signal is transferred. The differential input signal transfer and compensation concept is shown in Figure 5.8.

For this technique, the common mode elimination technique is employed and the common mode variation of $V_{in1}+/-'$ and $V_{in2}+/-'$ is below 2mV. Thus, the transconductance variation of PMOS and NMOS input pair is almost '0'. But, because of compression rate difference among those regions, the gain variation at the output still

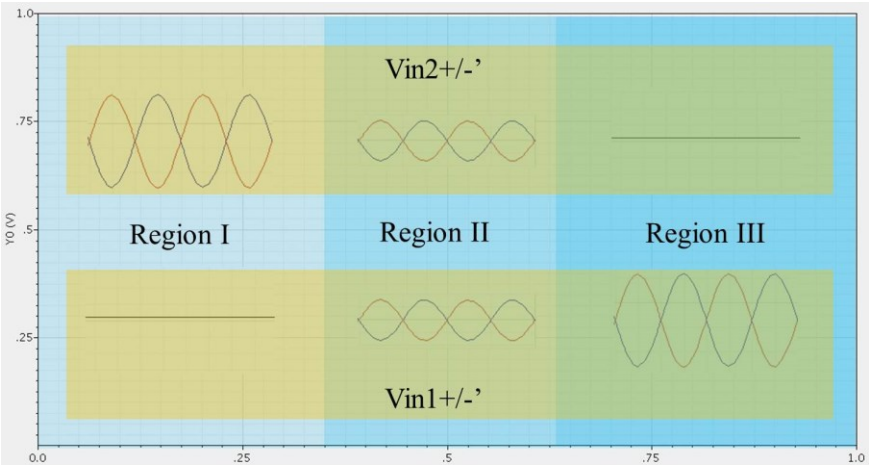


Figure 5.8 Concept of Differential Signal Extraction and Compensation

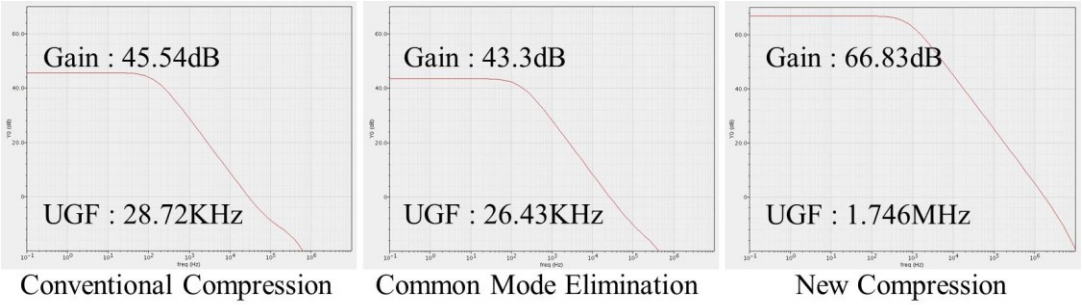


Figure 5.9 Comparisons of Gain and Unity Gain Frequency

exists. However, input signal compression technique and common mode elimination technique also have gain variation because of nonlinearity of compressed input signal. The overall gain variation of a novel technique is smaller than that of input signal compression technique and common mode elimination technique.

Figure 5.9 shows the gain and unity gain frequency comparisons of simulation results of 3 techniques, input signal compression technique, common mode elimination technique, and a proposed novel input signal compression technique. The unity gain frequencies of previously proposed techniques, input signal compression and common

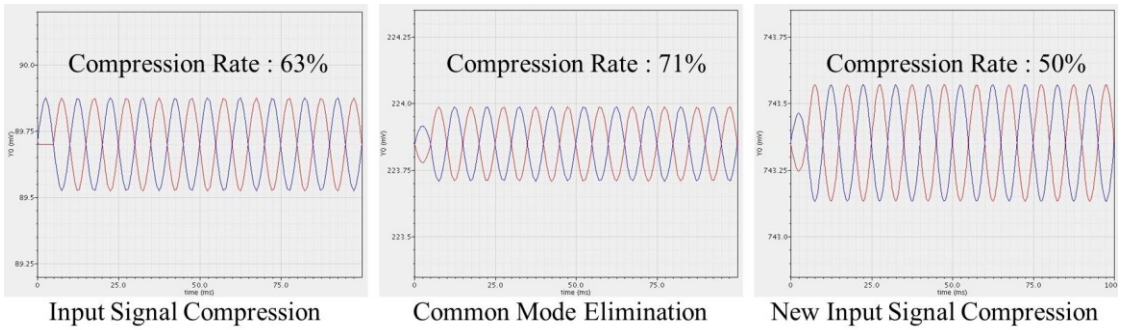


Figure 5.10 Comparison of Transferred Differential Input Signal

mode elimination techniques, are below 30KHz and that of a proposed novel technique expands to 1.746MHz.

A novel input signal compression technique proposed in this chapter overcomes some disadvantages of previously introduced techniques. First, the complex input signal compression blocks of input signal compression and common mode elimination techniques are replaced to the simple NMOS and PMOS source followers. Second, the unity gain frequency expands to 1.746MHz. Previously introduced techniques have reduced bandwidths and unity gain frequencies of those techniques are below 30KHz. For the last part, new input signal compression technique has better SNR than previous techniques. As mentioned in Chapter 5.1, the signal compression rate of input signal compression and common mode elimination techniques are about 63% and 71% respectively. That means if the original differential input signal is 1mV of peak-to-peak value, the compressed and common mode eliminated differential input signal of those techniques are 0.37mV and 0.29mV respectively. However, the signal compression rate of proposed novel input signal compression technique is 50% and 0.5mV peak-to-peak compressed differential input signal is transferred to the op-amp when the original peak-

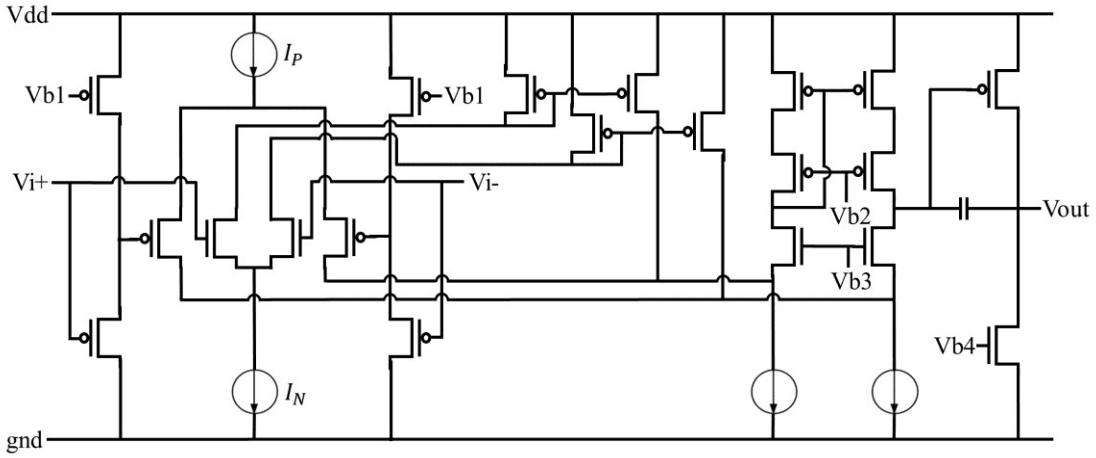
to-peak value of differential input signal is 1mV (Figure 5.10). Because bigger differential input signal is transferred, proposed technique has better signal to noise ratio than previous techniques.

Chapter 6. Simulation Results and Comparison

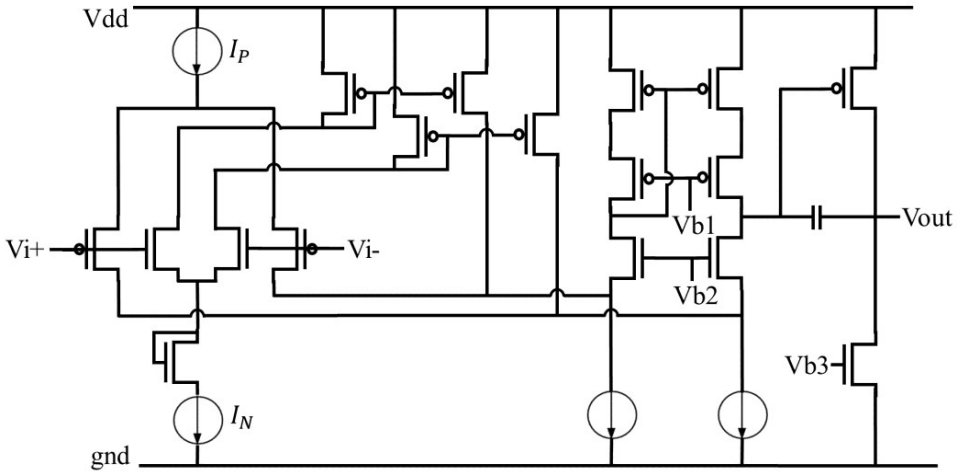
In this chapter, all simulation results and comparisons of five novel rail-to-rail op-amp techniques are described. Large transistor sizes are used to reduce noise as these designs, especially the input signal compression designs, can have substantial noise. As mentioned in Chapter 1.2, the target input referred noise level is about $5\mu V/\sqrt{Hz}$ at 1Hz. All rail-to-rail op-amp techniques proposed in this dissertation, except the common mode elimination technique, have acceptable input referred noise due to using large transistors. The common mode elimination technique, however, has limited bandwidth and poor SNR characteristic. Reducing noise by using large transistors is not appropriate for this technique because of the bandwidth problem. Therefore, only schematic simulation results without noise reduction will be given for the common mode elimination technique.

6.1 Simulation Results of New Level Shifting Technique

Figure 6.1 shows the overall structure comparison of the conventional level shifting technique and the new level shifting technique. As mentioned in Chapter 3.1, the new level shifting technique employs only one diode connected MOSFET while four resistors are required for the conventional level shifting technique. In Figure 3.3, the comparison of overall



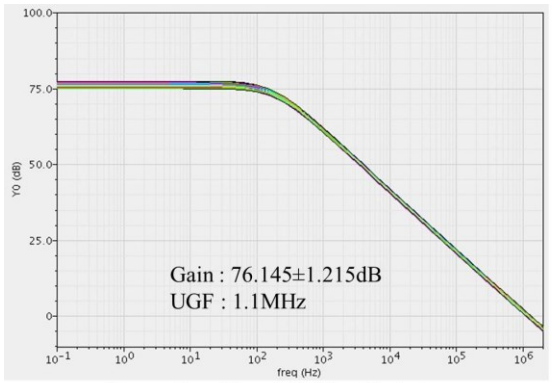
(a) Conventional Level Shifting Technique



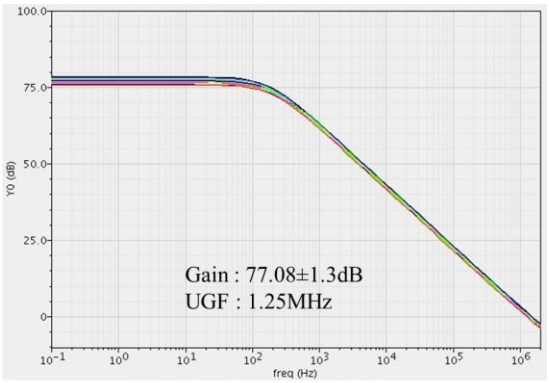
(b) New Level Shifting Technique

Figure 6.1 Overall Structure Comparison

transconductance variation is shown and the overall variation of new level shifting technique, ±8.66%, is higher than that of the traditional level shifting technique, ±4.97%. Because of this overall transconductance variation, the op-amp has gain variation over the entire rail-to-rail input common mode range. Figure 6.2 (a) shows the gain variation comparison of the conventional level shifting technique and new level shifting technique. The new level shifting technique has larger gain variation (±1.3dB) than the conventional level shifting technique (±1.215dB) because

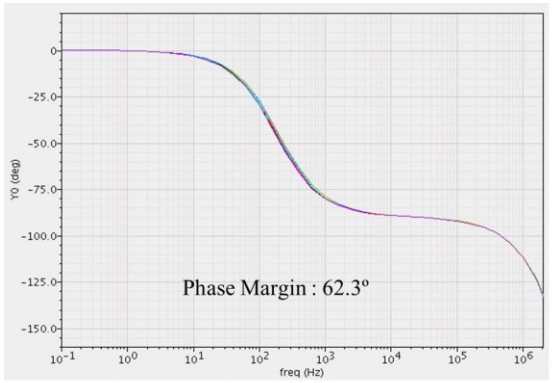


Conventional Level Shifting Technique

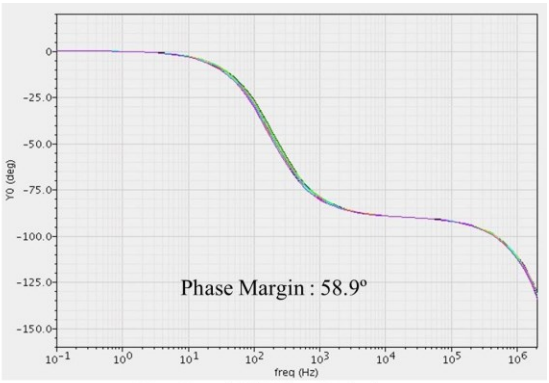


New Level Shifting Technique

(a) Comparison of Gain Variation



Conventional Level Shifting Technique



New Level Shifting Technique

(b) Comparison of Phase Margin

Figure 6.2 Comparison of Conventional and New Level Shifting Technique

of the larger overall transconductance variation. The unity gain frequencies of the conventional and new level shifting technique are 1.1MHz and 1.25MHz respectively. The phase margins of the conventional and new level shifting technique are 62.3º and 58.9º (Figure 6.2 (b)). Table 6.1 shows the comparisons of all simulation results of those two techniques. The minimum CMRR of the conventional and new level shifting technique are 80dB and 73.29dB. From Table 6.1, the new level shifting technique has lower power consumption than the conventional level shifting technique, as the conventional level shifting technique requires additional current for

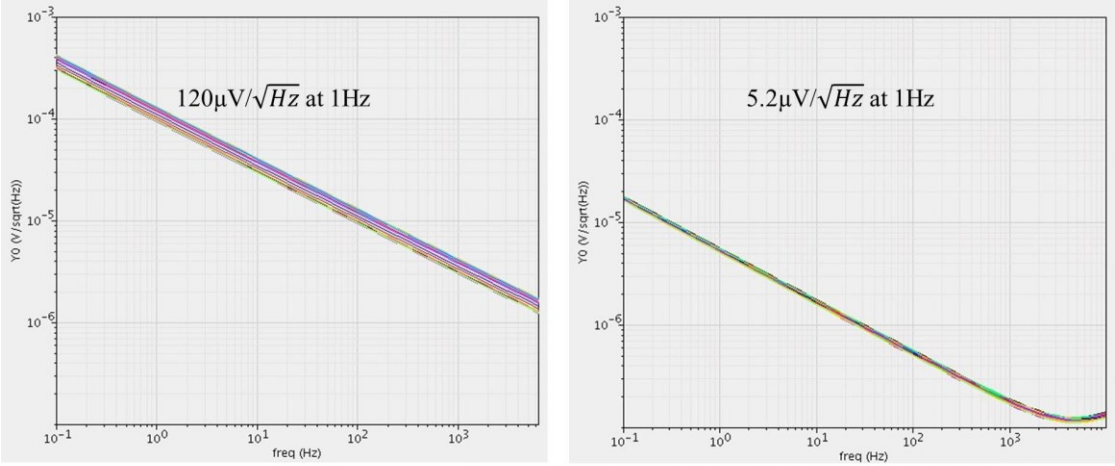
	Conventional Level Shifting Technique	New Level Shifting Technique
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
Gm Variation	±4.97%	±8.66%
Avg. Gain	76.145dB	77.08dB
Gain Variation	±1.215dB	±1.3dB
Unity Gain Freq.	1.1MHz	1.25MHz
Phase Margin	62.3º	58.9º
CMRR	≥ 80dB	≥ 73.29dB
Avg. Power Consumption (@150Hz)	89.48μW	79.14μW

Table 6.1 Simulation Results of Conventional and New Level Shifting Techniques

two PMOS source followers which shift input common mode signal for PMOS differential input pair. However, PMOS source followers are not required for new level shifting technique. Therefore, no additional currents are required and power consumption of the new level shifting technique is lower than that of the conventional level shifting technique.

The new level shifting technique is modified to reduce input referred noise. For the ECG amplifier, the frequency of input signal is very low, below 150Hz, and the flicker noise is dominant in this frequency range. Cadence SPECTRE simulator and TSMC 0.25-μm technology are used for this simulation and from [23], equation for flicker noise model used in SPECTRE simulator is given below.

$$S_{iD}(f) = \frac{KF \cdot (I_D)^{AF}}{f^{EF} \cdot C_{ox} \cdot W_{eff} \cdot L_{eff}}$$

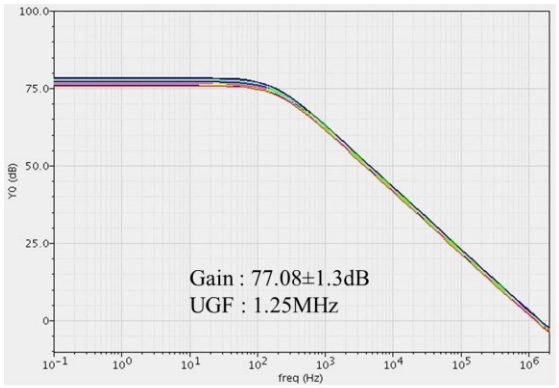


Input Referred Noise Before Noise Reduction Input Referred Noise After Noise Reduction

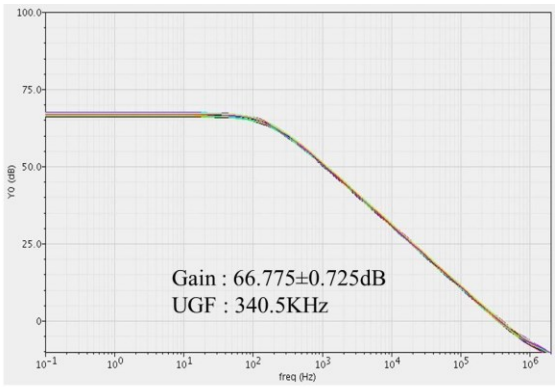
Figure 6.3 Input Referred Noise of New Level Shifting Technique

$S_{iD}(f)$ is the drain noise current spectral density and f, C_{ox}, W_{eff}, L_{eff} are frequency, oxide capacitance, effective gate width and length of MOSFET respectively. KF, AF, and EF are flicker noise coefficient, flicker noise exponent, and flicker noise frequency coefficient respectively. From the above equation, larger transistor has lower flicker noise. For the flicker noise reduction of new level shifting rail-to-rail op-amp, 25 times larger transistors than the original schematic transistors are used for the complementary input differential stage and the folded cascode current summing stage. Figure 6.3 shows the input referred noise comparison of before and after noise reduction. Before noise reduction, the average input referred noise is about 120μV/$\sqrt{Hz}$ at 1Hz. As mentioned in Chapter 1.2, the target noise level for this work is 5μV/$\sqrt{Hz}$ at 1Hz and after noise reduction, the average input referred noise is about 5.2μV/$\sqrt{Hz}$ at 1Hz.

This flicker noise reduction method using large transistors, however, has a main drawback which is reduced bandwidth. To reduce flicker noise, large transistors for the

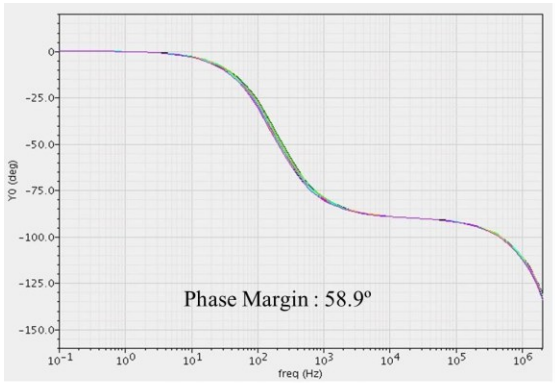


Before Noise Reduction

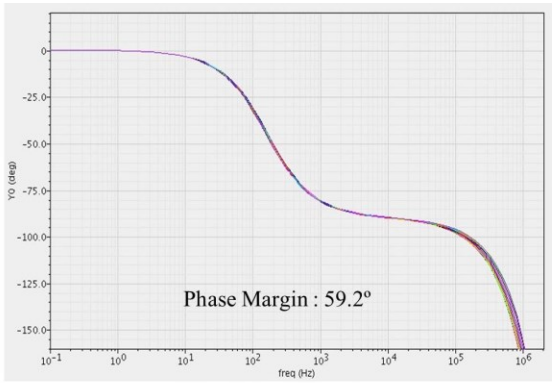


After Noise Reduction

(a) Comparison of Gain and Unity Gain Frequency



Before Noise Reduction



After Noise Reduction

(b) Comparison of Phase Margin

Figure 6.4 Simulation Results Comparisons of Before and After Noise Reduction

complementary input differential pairs are employed and because of these large input transistors, the bandwidth of op-amp is reduced. Figure 6.4 shows the simulation results comparisons of before and after noise reduction. Before noise reduction, the unity gain frequency of new level shifting technique is 1.25MHz but after noise reduction, the unity gain frequency is decreased to 340.5KHz. Because of the reduced bandwidth, gain has to be lowered from 77.08dB to 66.775dB for the 3-dB frequency of 150Hz which is the upper frequency range of the ECG amplifier. Table 6.2 shows the simulation results comparisons of before and after noise reduction. The main differences are noise, gain,

	Before Noise Reduction	After Noise Reduction
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	77.08dB	66.775dB
Gain Variation	±1.3dB	±0.725dB
Unity Gain Freq.	1.25MHz	340.5KHz
Phase Margin	58.9º	59.2º
CMRR	≥ 73.29dB	≥ 65.28dB
Avg. Power Consumption (@150Hz)	79.14μW	82.2μW
Input Referred Noise (@1Hz)	120μV/$\sqrt{Hz}$	5.2μV/$\sqrt{Hz}$

Table 6.2 Simulation Results Comparison of Before and After Noise Reduction

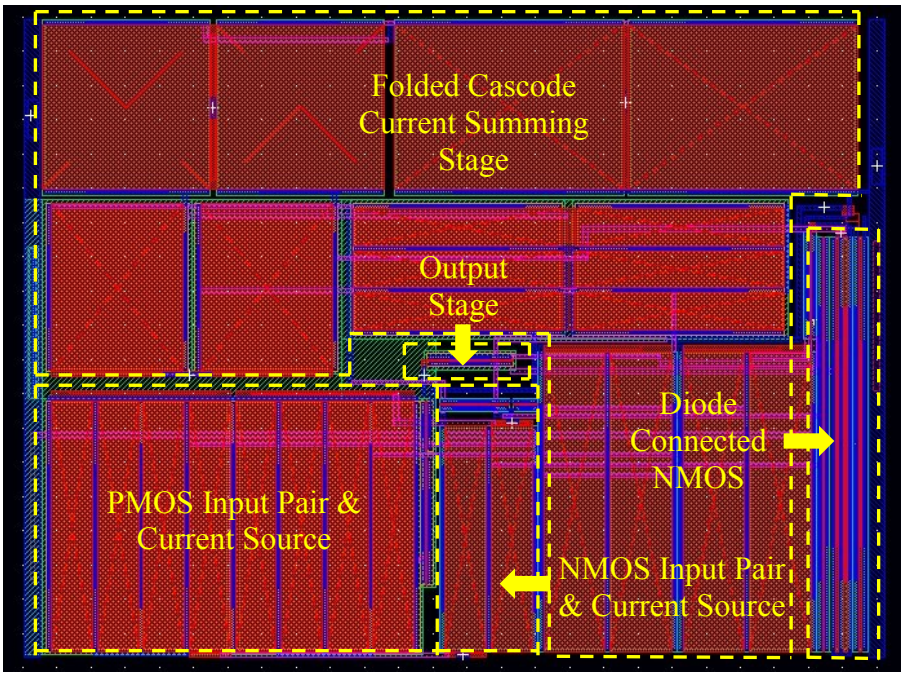
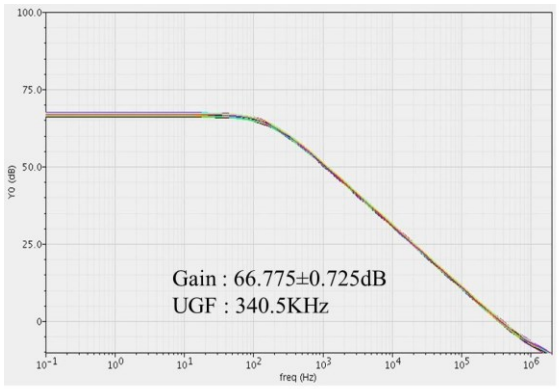
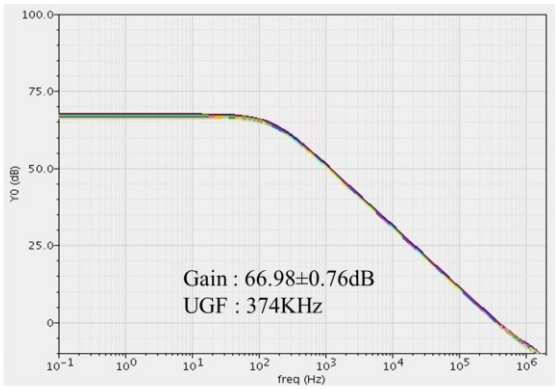


Figure 6.5 Layout Picture of New Level Shifting Technique (125.82μm×93.18μm)

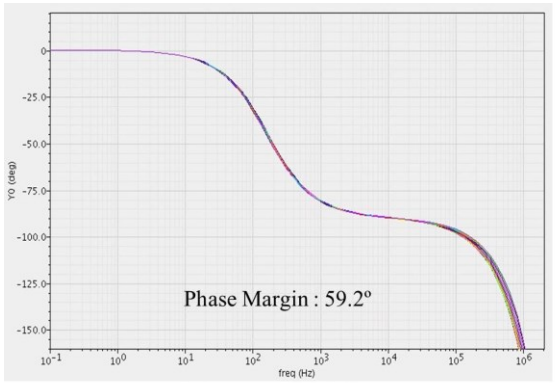


Schematic Simulation

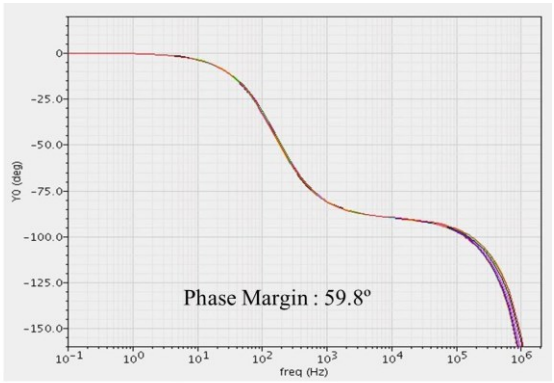


Post Layout Simulation

(a) Comparison of Gain and Unity Gain Frequency

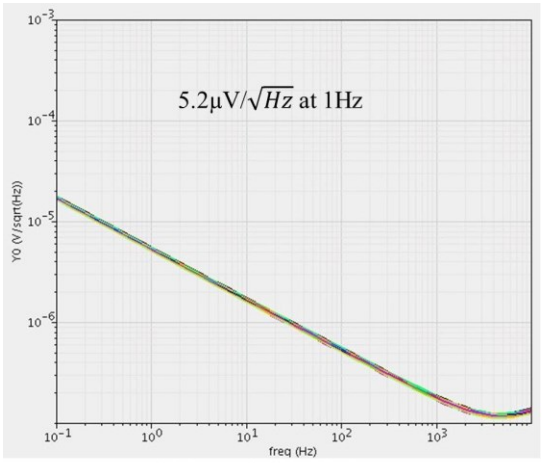


Schematic Simulation

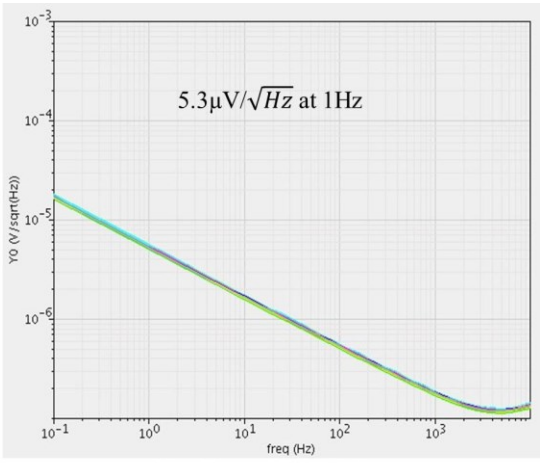


Post Layout Simulation

(b) Comparison of Phase Margin



Schematic Simulation



Post Layout Simulation

(c) Comparison of Noise

Figure 6.6 Comparisons of Schematic and Post Layout Simulations

	Schematic Simulation	Post Layout Simulation
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.775dB	66.98dB
Gain Variation	±0.725dB	±0.76dB
Unity Gain Freq.	340.5KHz	374KHz
Phase Margin	59.2º	59.8º
CMRR	≥ 65.28dB	≥ 65.33dB
Avg. Power Consumption (@150Hz)	82.2μW	84.7μW
Input Referred Noise (@1Hz)	5.2μV/$\sqrt{Hz}$	5.3μV/$\sqrt{Hz}$

Table 6.3 Comparison of Schematic and Post Layout Simulation Results

gain variation, and bandwidth. The other simulation results are almost same with the results without noise reduction. Figure 6.5 shows the layout picture of new level shifting technique and post layout simulation results are compared with schematic simulation results in Figure 6.6. Table 6.3 shows the comparison of post layout simulation and schematic simulation results. The post layout simulation results are almost same with the schematic simulation results with noise reduction.

6.2 Simulation Results of Saturation Point Control Technique

The overall structure of the saturation point control technique rail-to-rail constant transconductance op-amp is shown in Figure 6.7. As mentioned in Chapter 6.1, large transistors are employed to reduce input referred noise and simulation results

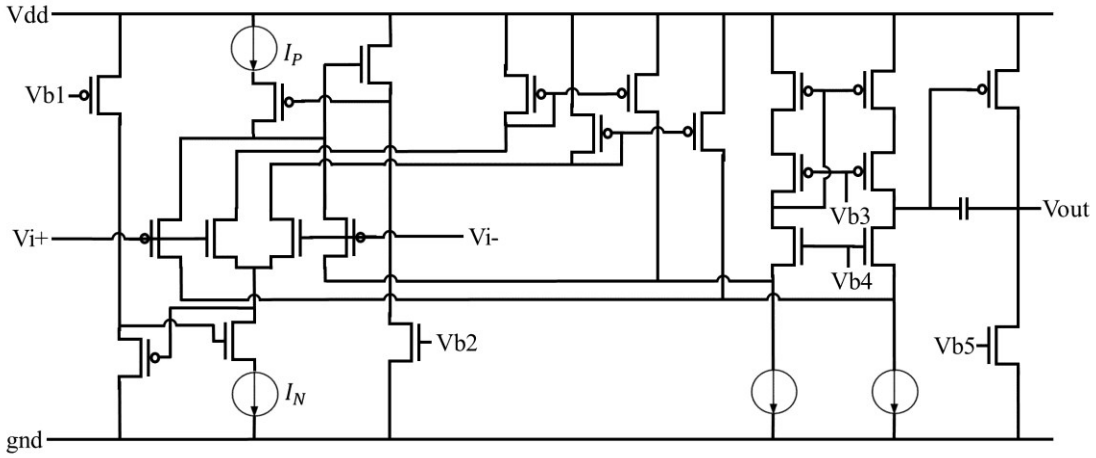
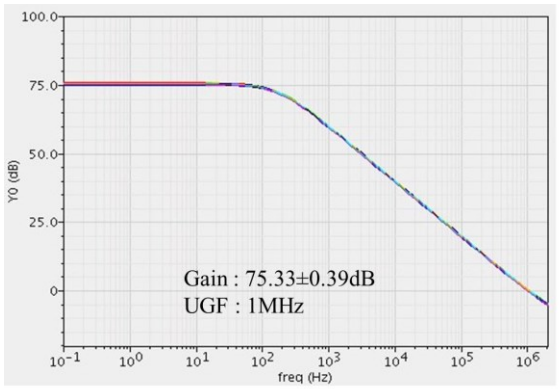


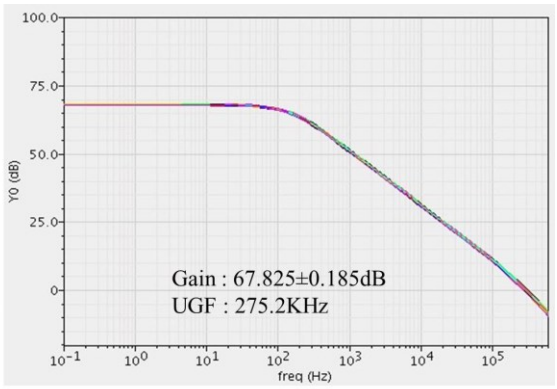
Figure 6.7 Overall Structure of Saturation Point Control Technique

comparisons of before and after noise reduction are shown in Figure 6.8. 25 times larger transistors than the schematic transistors without noise reduction are used for the complementary input differential stage and the folded cascode current summing stage. Because of large transistors of input differential pairs, the unity gain frequency is reduced from 1MHz to 275.2KHz and the gain is decreased from 75.33dB to 67.825dB. Before noise reduction, the input referred noise at 1Hz is about 120μV/$\sqrt{Hz}$. The input referred noise at 1Hz after noise reduction is decreased to 5.02μV/$\sqrt{Hz}$. Table 6.4 shows the simulation results comparison of before and after noise reduction.

The layout of the saturation point control technique op-amp is shown in Figure 6.9. Comparisons of schematic simulation results with noise reduction and post layout simulation results are shown in Figure 6.10 and Table 6.5. As shown in these results, the post layout simulation results are almost same with reduced noise schematic simulation results.

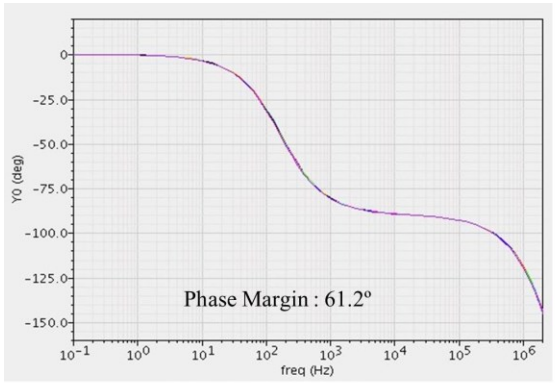


Before Noise Reduction

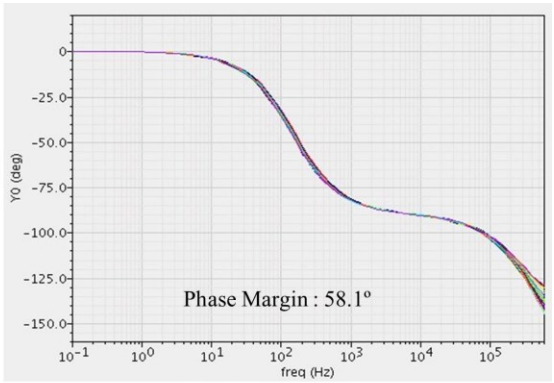


After Noise Reduction

(a) Comparison of Gain and Unity Gain Frequency

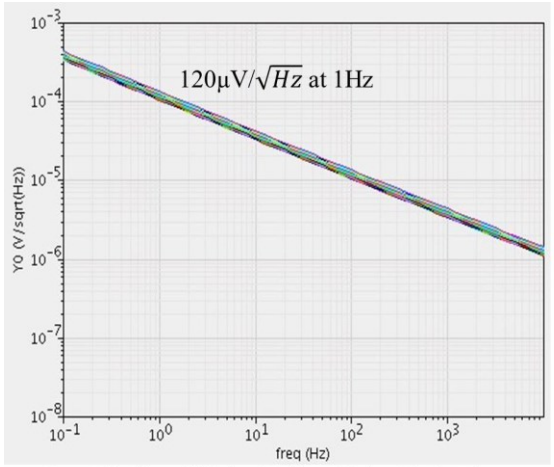


Before Noise Reduction

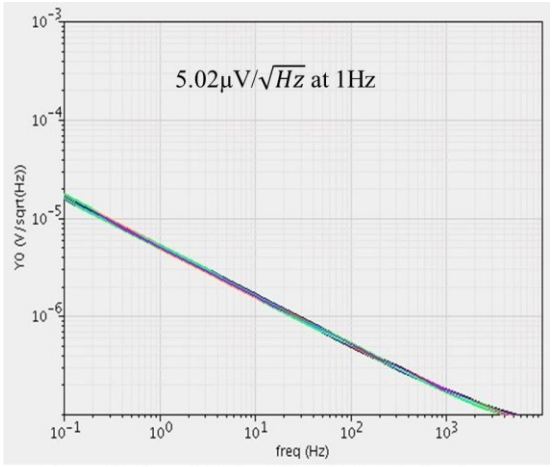


After Noise Reduction

(b) Comparison of Phase Margin



Input Referred Noise Before Noise Reduction



Input Referred Noise After Noise Reduction

(c) Comparison of Input Referred Noise

Figure 6.8 Simulation Results Comparisons of Before and After Noise Reduction

	Before Noise Reduction	After Noise Reduction
Supply Voltage	1.2V	1.2V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	75.33dB	67.825dB
Gain Variation	±0.39dB	±0.185dB
Unity Gain Freq.	1MHz	275.2KHz
Phase Margin	61.2º	58.1º
CMRR	≥ 80.71dB	≥ 66.98dB
Avg. Power Consumption (@150Hz)	57.64μW	62.47μW
Input Referred Noise (@1Hz)	120μV/$\sqrt{Hz}$	5.02μV/$\sqrt{Hz}$

Table 6.4 Simulation Results Comparison of Before and After Noise Reduction

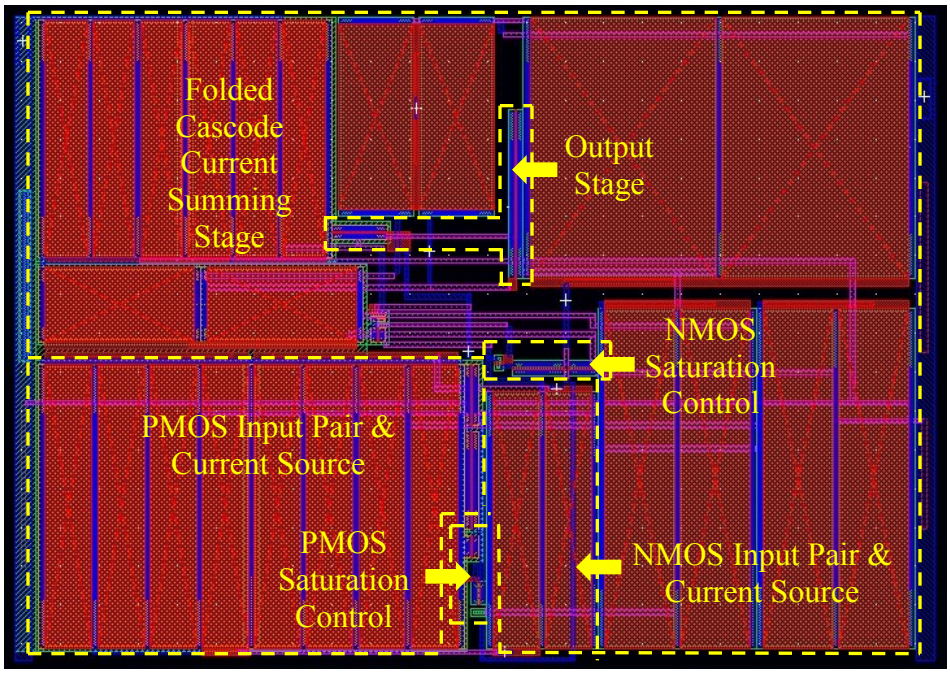
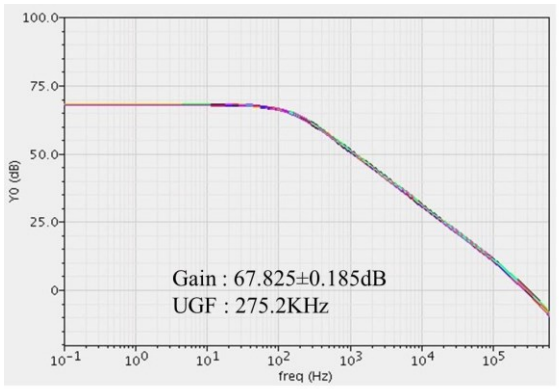
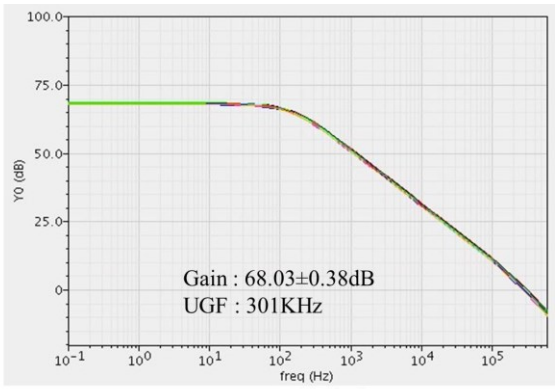


Figure 6.9 Layout of Saturation Point Control Technique (118.38μm×83.1μm)

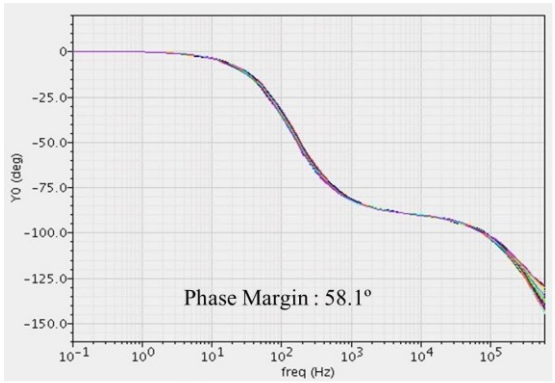


Schematic Simulation

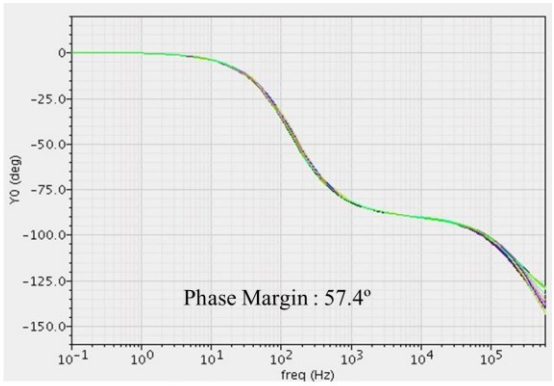


Post Layout Simulation

(a) Comparison of Gain and Unity Gain Frequency

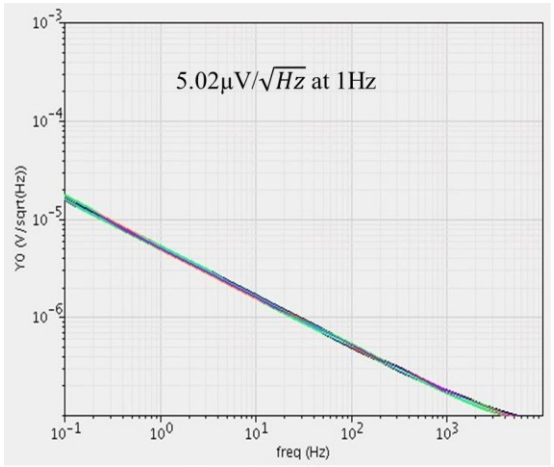


Schematic Simulation

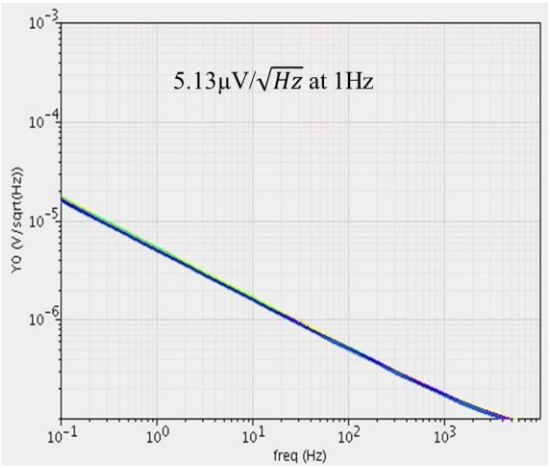


Post Layout Simulation

(b) Comparison of Phase Margin



Schematic Simulation



Post Layout Simulation

(c) Comparison of Input Referred Noise

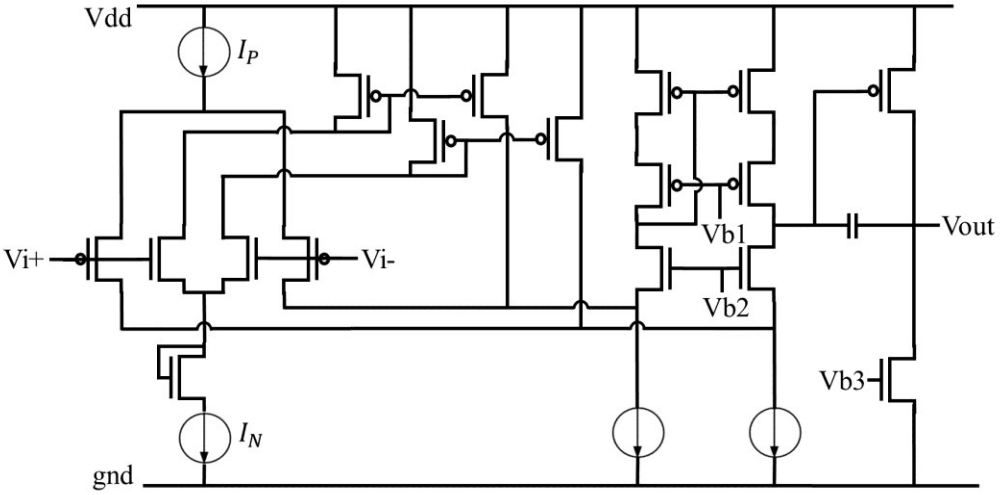
Figure 6.10 Comparisons of Schematic and Post Layout Simulations

	Schematic Simulation	Post Layout Simulation
Supply Voltage	1.2V	1.2V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	67.825dB	68.03dB
Gain Variation	±0.185dB	±0.38dB
Unity Gain Freq.	275.2KHz	301KHz
Phase Margin	58.1º	57.4º
CMRR	≥ 66.98dB	≥ 67.73dB
Avg. Power Consumption (@150Hz)	62.47μW	64.83μW
Input Referred Noise (@1Hz)	5.02μV/$\sqrt{Hz}$	5.13μV/$\sqrt{Hz}$

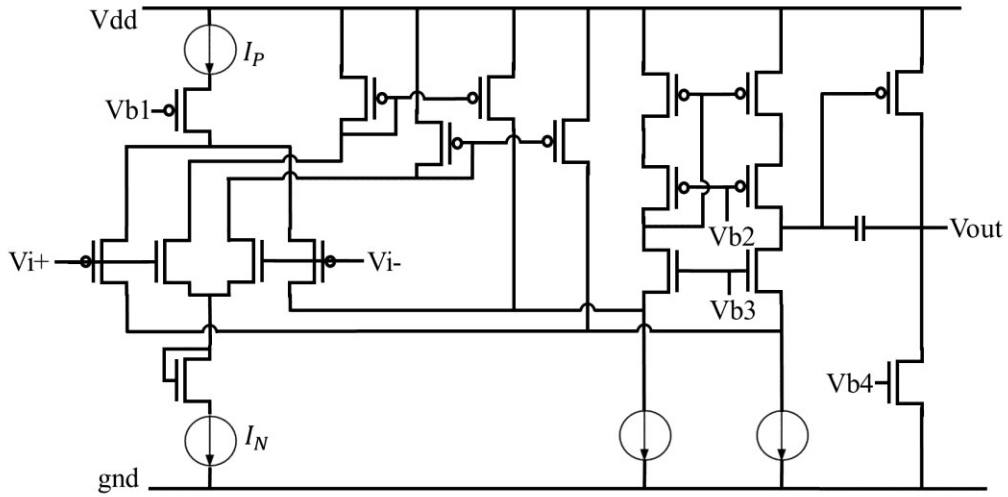
Table 6.5 Comparison of Schematic and Post Layout Simulation Results

6.3 Simulation Results of Modified New Level Shifting Technique

The whole structure of the modified new level shifting technique is compared with the structure of new level shifting technique in Figure 6.11. As mentioned in Chapter 3.3, in a modified new level shifting technique, one PMOS is added below current source of PMOS input pair to control saturation point of current of PMOS input pair while new level shifting technique requires only one diode connected NMOS above current source of NMOS input pair. Because of this PMOS saturation point controller, the overall transconductance variation of the modified new level shifting technique is smaller than that of the new level shifting technique (Figure 3.9) and as a result, the modified



(a) New Level Shifting Technique



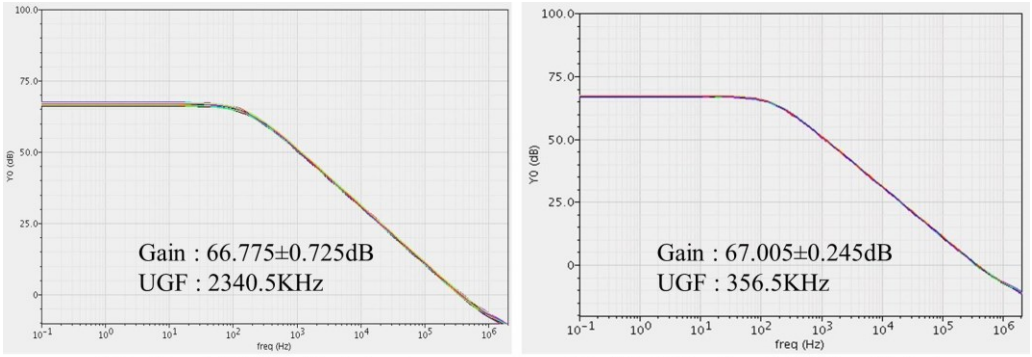
(b) Modified New Level Shifting Technique

Figure 6.11 Overall Structure Comparison of New and Modified New Level Shifting Technique

new level shifting technique has only ±0.245dB of gain variation at the output while the gain variation of the new level shifting technique is ±0.725dB (Table 6.6). The schematic simulation results comparisons of new level shifting and modified new level shifting techniques with noise reduction are given in Table 6.6, Figure 6.12 and Figure 6.13.

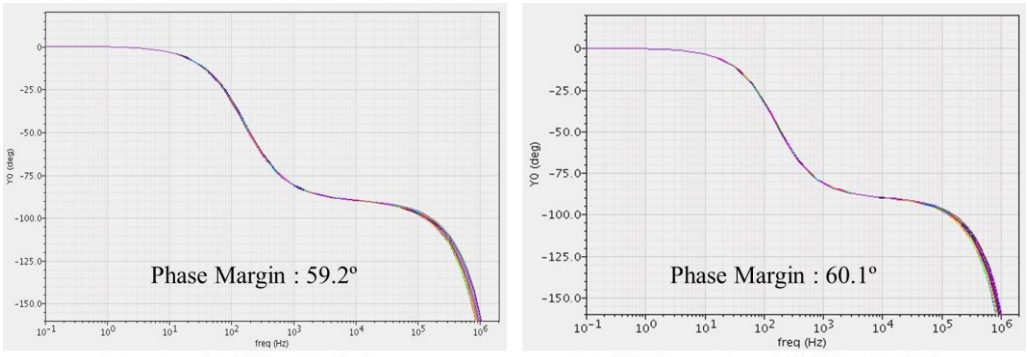
	New Level Shifting	Modified New level Shifting
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.775dB	67.005dB
Gain Variation	±0.725dB	±0.245dB
Unity Gain Freq.	340.5KHz	356.5KHz
Phase Margin	59.2º	60.1º
CMRR	≥ 65.28dB	≥ 74.59dB
Avg. Power Consumption (@150Hz)	82.2µW	81.7µW
Input Referred Noise (@1Hz)	5.2µV/$\sqrt{Hz}$	5.16µV/$\sqrt{Hz}$

Table 6.6 Schematic Simulation Results Comparison of Two Techniques



New Level Shifting Technique　　Modified New Level Shifting Technique

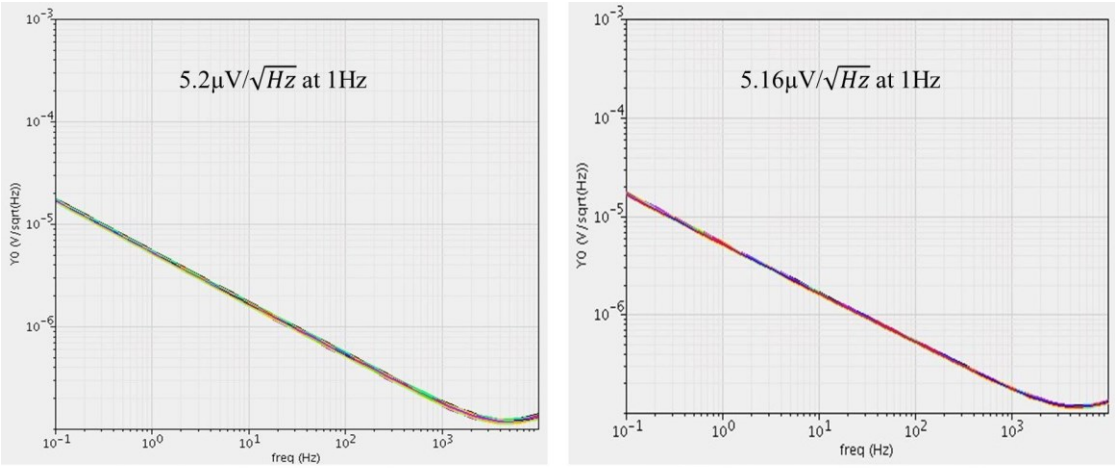
(a) Gain Variation and Unity Gain Frequency Comparison



New Level Shifting Technique　　Modified New Level Shifting Technique

(b) Phase Margin Comparison

Figure 6.12 Schematic Simulation Results Comparison of Two Techniques



New Level Shifting Technique　　Modified New Level Shifting Technique

Figure 6.13 Input Referred Noise Comparison of Two Techniques

The layout picture of the modified new level shifting technique is shown in Figure 6.14 and post layout simulation results comparisons are given in Figure 6.15 and Table 6.7. The post layout simulation results of modified new level shifting technique are almost same with reduced noise schematic simulation results.

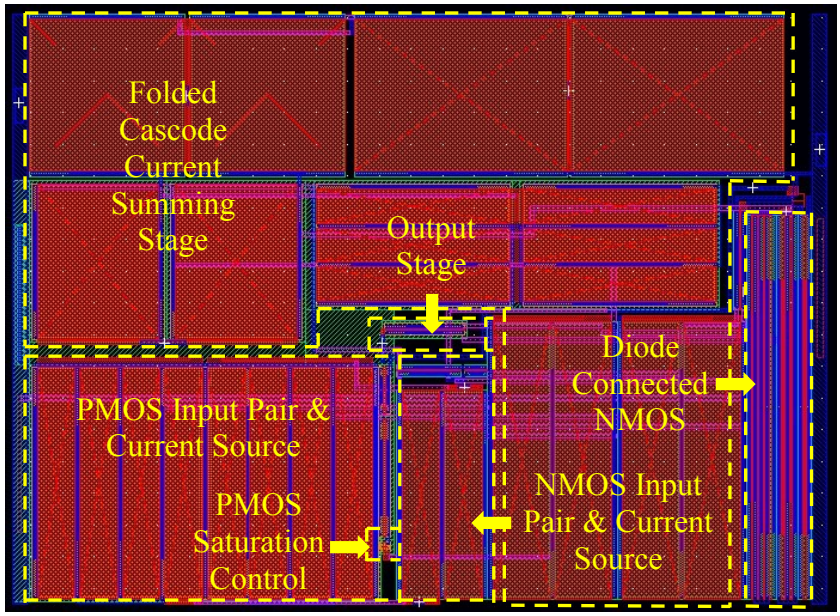
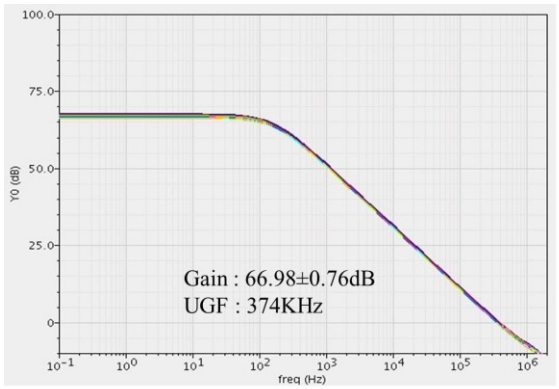
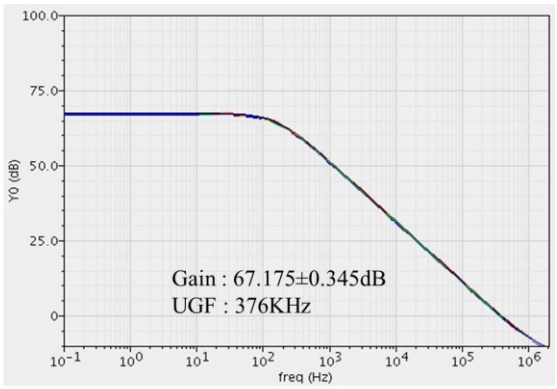


Figure 6.14 Layout Picture of Modified New Level Shifting Technique (128.7μm×93.18μm)

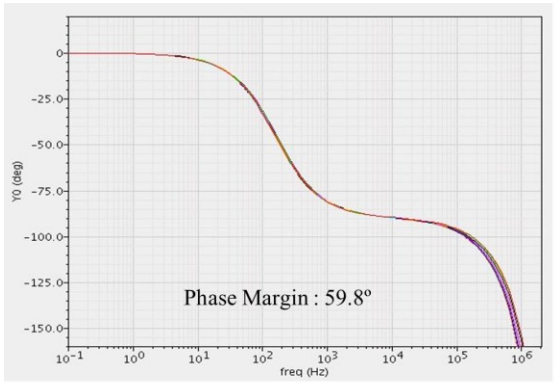


New Level Shifting Technique

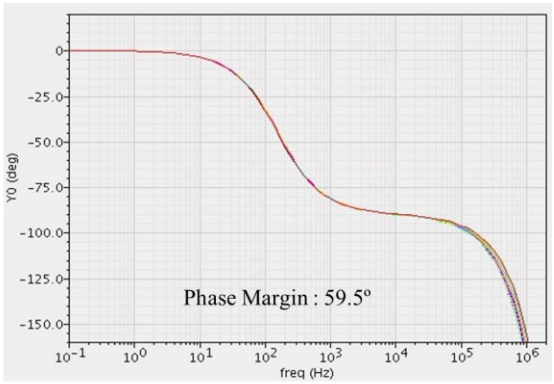


Modified New Level Shifting Technique

(a) Comparison of Gain and Unity Gain Frequency

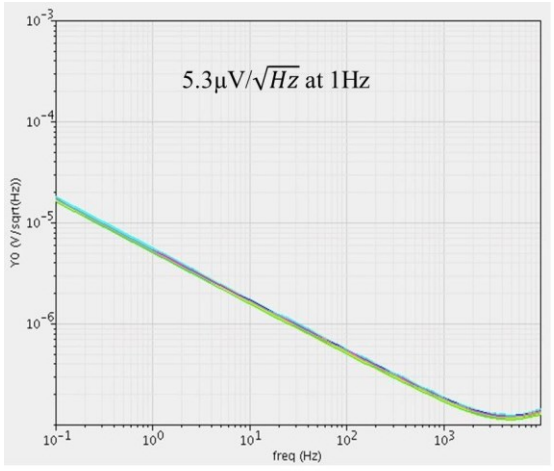


New Level Shifting Technique

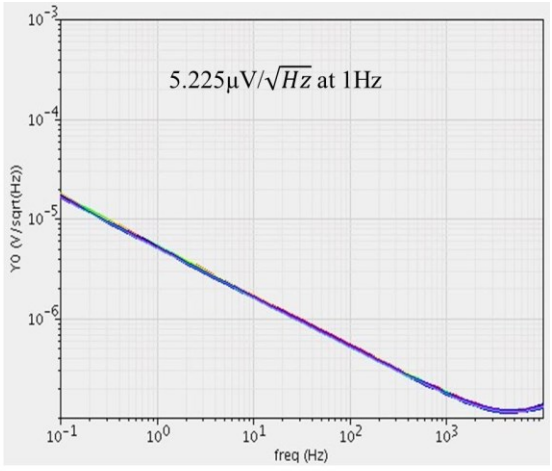


Modified New Level Shifting Technique

(b) Comparison of Phase Margin



New Level Shifting Technique



Modified New Level Shifting Technique

(c) Comparison of Noise

Figure 6.15 Post Layout Simulation Results Comparison of Two Techniques

	New Level Shifting	Modified New Level Shifting
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.98dB	67.175dB
Gain Variation	±0.76dB	±0.345dB
Unity Gain Freq.	374KHz	376KHz
Phase Margin	59.8º	59.5º
CMRR	≥ 65.33dB	≥ 74.8dB
Avg. Power Consumption (@150Hz)	84.7µW	82.9µW
Input Referred Noise (@1Hz)	5.3µV/$\sqrt{Hz}$	5.225µV/$\sqrt{Hz}$

Table 6.7 Post Layout Simulation Results Comparison of Two Techniques

	New Level Shifting	Saturation Point Control	Modified New Level Shifting
Supply Voltage	1.6V	1.2V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.98dB	68.03dB	67.175dB
Gain Variation	±0.76dB	±0.38dB	±0.345dB
Unity Gain Freq.	374KHz	301KHz	376KHz
Phase Margin	59.8º	57.4º	59.5º
CMRR	≥ 65.33dB	≥ 67.73dB	≥ 74.8dB
Avg. Power Consumption (@150Hz)	84.7µW	64.83µW	82.9µW
Input Referred Noise (@1Hz)	5.3µV/$\sqrt{Hz}$	5.13µV/$\sqrt{Hz}$	5.225µV/$\sqrt{Hz}$

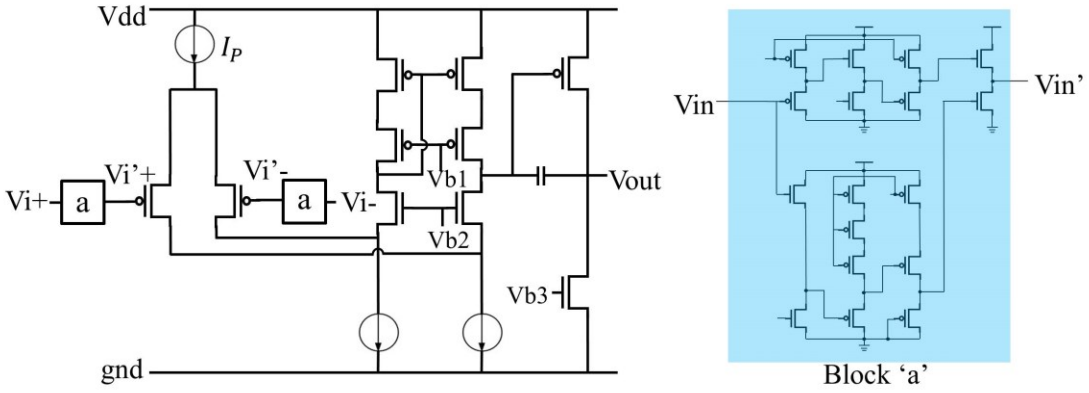
Table 6.8 Overall Simulation Results Comparison of Low Supply Voltage Techniques

Table 6.8 shows the overall simulation results comparing the three novel techniques for the low supply voltage environment. The new level shifting technique is

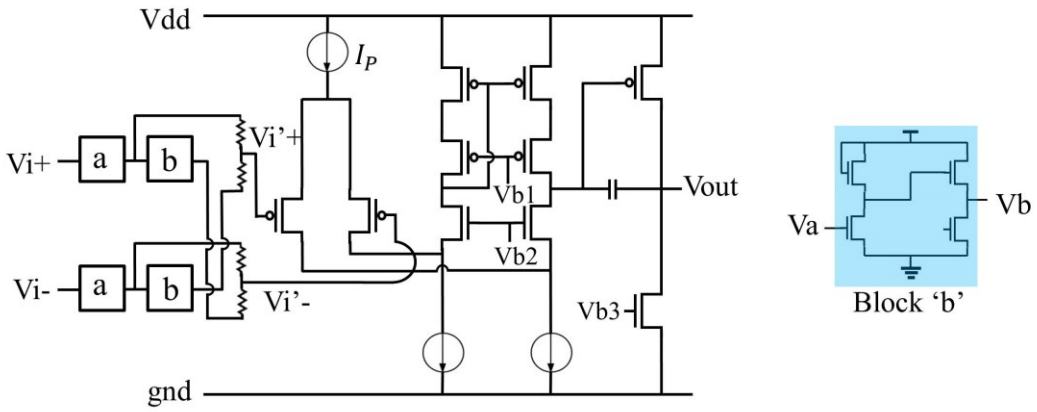
the simplest technique for the low supply voltage environment but this technique has the largest transconductance variation among those three novel techniques. That causes the largest gain variation in Table 6.8. the saturation point control technique does not have a limitation of a set voltage shifting amount which is one of main drawbacks of new level shifting and modified new level shifting techniques, and has the lowest supply voltage. That causes the lowest average power consumption. However, saturation point control technique is more complex than new level shifting and modified new level shifting techniques. Modified new level shifting technique is very simple and has the smallest transconductance and gain variations. But this technique still has limited amount of voltage shifting.

6.4 Simulation Results of Common Mode Elimination Technique

As mentioned in Chapter 5.1, the common mode elimination technique is a modification of the input signal compression technique. Figure 6.16 compares the whole circuit of the input signal compression and common mode elimination techniques. For common mode elimination technique, additional two signal inverting blocks and four resistors are required to eliminate common mode input signal. Figure 5.4 shows that ultra-high CMRR can be achieved using common mode elimination technique. The common mode variation of common mode eliminated input signal, $V_{in}' +/-$, is smaller than 2mV when the original common mode input signal, $V_{in} +/-$, varies from 0 to 1V. Therefore, the overall transconductance variation of PMOS input differential pair of



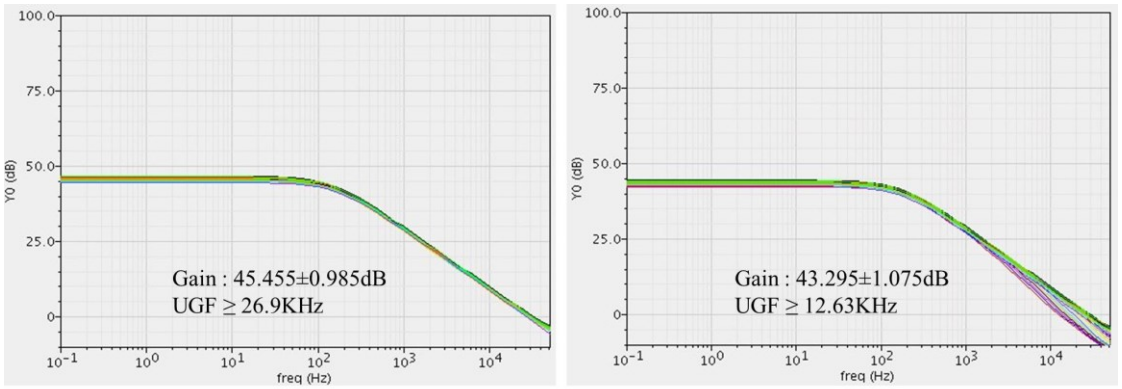
(a) Input Signal Compression Technique



(b) Common Mode Elimination Technique

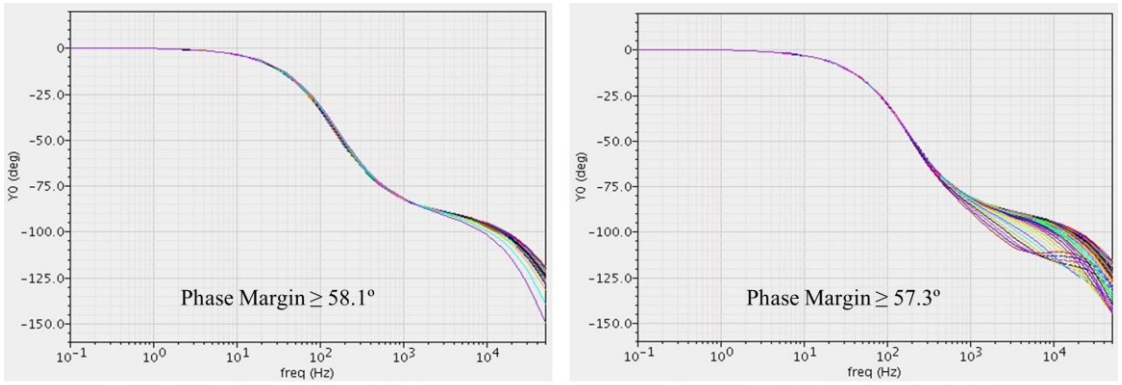
Figure 6.16 Overall Structure Comparison of Input signal Compression Technique and Common Mode Elimination Technique

common mode elimination technique is almost zero. From the cases of previous three novel techniques for the low supply voltage environment, the gain variation is directly proportional to the overall transconductance variation (Table 6.8). For the cases of input signal compression and common mode elimination techniques for the extremely low supply voltage environment, however, relatively large gain variations are achieved even though the overall transconductance variations are very small or almost zero as shown in Figure 6.17. That is caused by non-linearity of the compressed input signal. As shown in



Input Signal Compression Technique | Common Mode Elimination Technique

(a) Comparison of Gain and Unity Gain Frequency



Input Signal Compression Technique | Common Mode Elimination Technique

(b) Comparison of Phase Margin

Figure 6.17 Schematic Simulation Results Comparison of Two Techniques

Figure 4.9 and Figure 5.2, the compressed input signals of input signal compression and common mode elimination techniques are not perfectly linear. Thus, the differential input signal is not transferred uniformly according to the changing of common mode input signal and this un-uniform differential input signal is the main source of gain variation. Figure 6.17 and Table 6.9 shows the schematic simulation results comparison without noise reduction.

	Input Signal Compression	Common Mode Elimination
Supply Voltage	1V	1V
ICMR	Rail-to-Rail	Rail-to-Rail
CM Compression Rate	62.32%	99.63%
DM Compression Rate	62.32%	71.4%
Avg. Gain	45.455dB	43.295dB
Gain Variation	±0.985dB	±1.075dB
Unity Gain Freq.	26.9KHz	12.63KHz
Phase Margin	58.1º	57.3º
CMRR	≥ 56.26dB	≥ 115.1dB
Avg. Power Consumption (@150Hz)	38.875μW	40.39μW

Table 6.9 Schematic Simulation Results Comparison of Two Techniques

In Chapter 6.1, 6.2 and 6.3, simulation results of three novel techniques for the low supply voltage environment are shown and unity gain frequencies of those techniques are about 1MHz without noise reduction. As mentioned in Chapter 6.1, after noise reduction, the bandwidth of op-amp is reduced because of large transistors of input differential pairs and the unity gain frequencies of three novel techniques are reduced to several hundreds of KHz. As shown in Figure 6.17 and Table 6.9, input signal compression technique and common mode elimination technique has reduced bandwidth and the unity gain frequency of common mode elimination technique is 12.63KHz. If large transistors are used to reduce input referred noise, this technique will have more reduced bandwidth and that is not suitable for the ECG system. Another drawback of common mode elimination technique is degradation of SNR as mentioned in Chapter 5.1.

The higher compression rate means smaller differential input signal and this smaller signal reduces the SNR. In Table 6.9, the differential input signal compression rate of the input signal compression technique is 62.32% and that of common mode elimination technique is 71.4%. Therefore, the SNR of the common mode elimination technique is worse than that of the input signal compression technique. Because of these reasons, another technique is required for the portable ECG system and new input signal compression technique is introduced.

6.5 Simulation Results of New Input Signal Compression Technique

Figure 6.18 shows the overall structure of the new input signal compression technique. As mentioned in Chapter 5.2, the block ‘a1’ and ‘a2’ are simple source followers rather than the complex input signal compression block which is the block ‘a’ of input signal compression technique and common mode elimination technique. The block ‘b1’ and ‘b2’ are simple signal inverting block and similar with the block ‘b’ of common mode elimination block. Another main difference between the new input signal compression technique and two techniques shown in Figure 6.16 which are input signal compression and common mode elimination techniques is the structure of input differential pair. Conventional PMOS input differential pair is employed in input signal compression technique and common mode elimination technique (Figure 6.16). New input signal compression technique, however, employs complementary input differential pair structure which are commonly used for low supply voltage environment. The

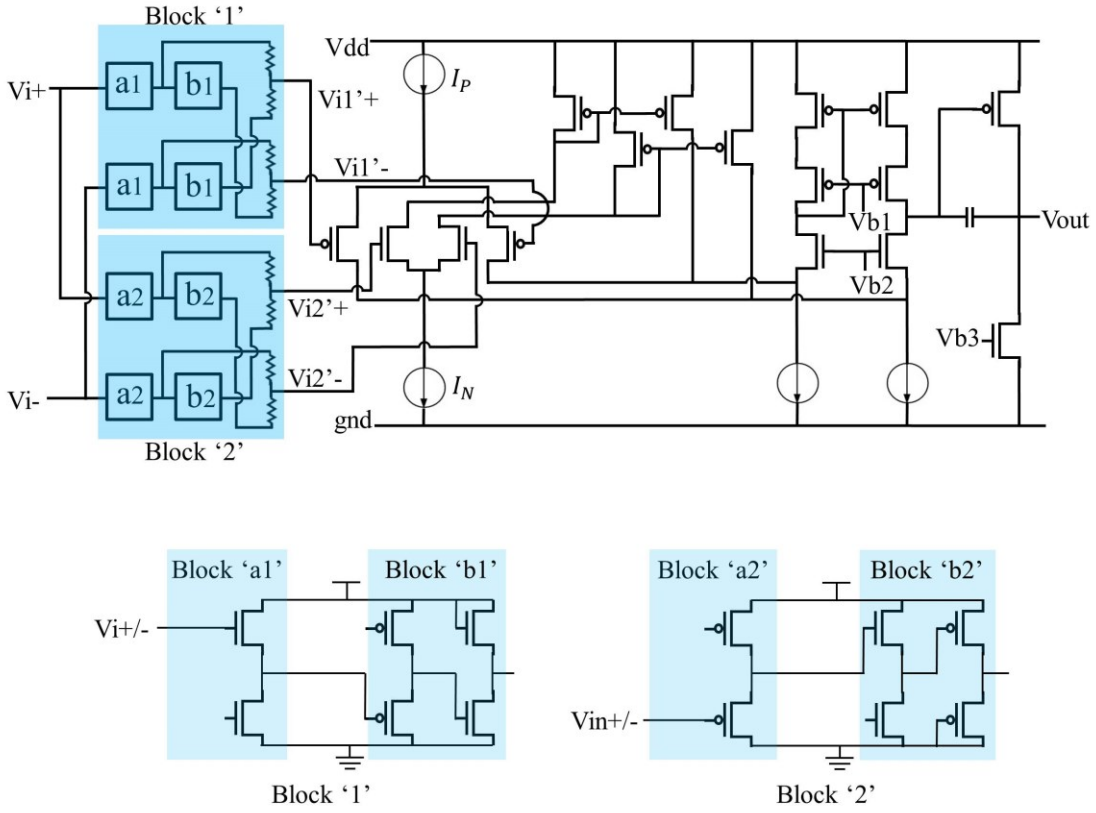
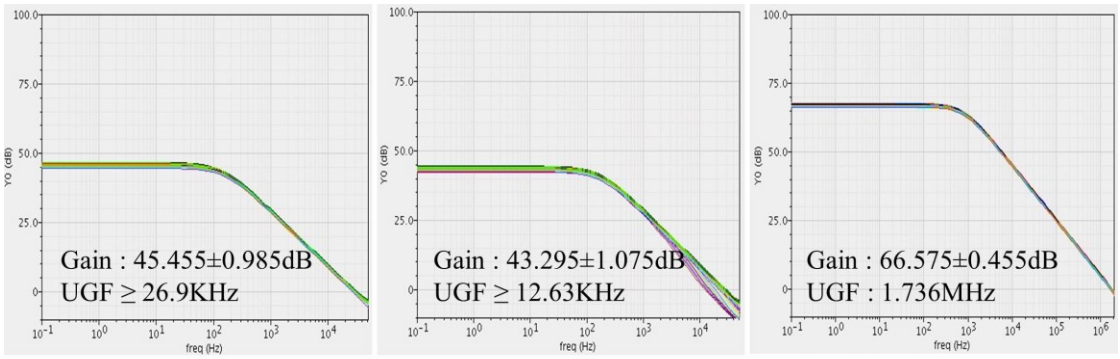


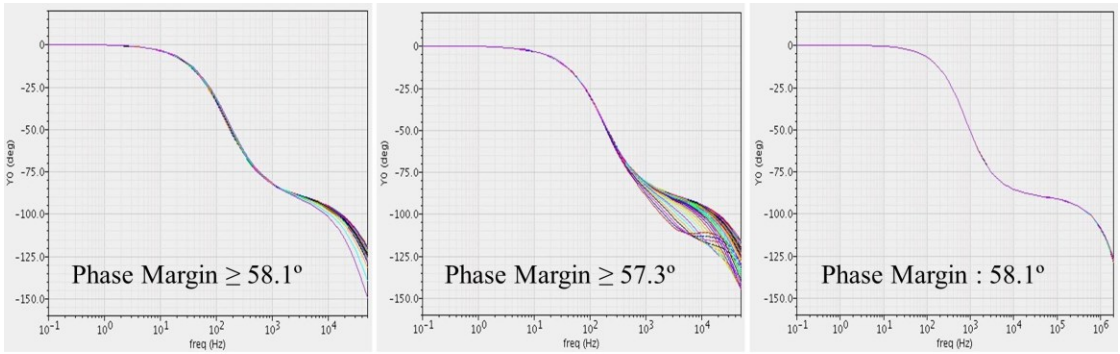
Figure 6.18 Overall Structure of New Input Signal Compression Technique

schematic simulation results comparisons without noise reduction are shown in Figure 6.19 and Table 6.10. As mentioned in Chapter 5.2, the band width of new input signal compression technique with simple signal compression block is much larger than that of input signal compression technique or common mode elimination technique. The unity gain frequency of new input signal compression technique is 1.736MHz while 26.9KHz and 12.63KHz are the unity gain frequencies of the other techniques. As mentioned in Chapter 6.4, the gain variations of input signal compression technique and common mode elimination technique are not caused by overall transconductance variation but rather



Signal Compression | Common Mode Elimination | New Signal Compression

(a) Comparison of Gain and Unity Gain Frequency



Signal Compression | Common Mode Elimination | New Signal Compression

(b) Comparison of Phase Margin

Figure 6.19 Schematic Simulation Results Comparison of Three Techniques

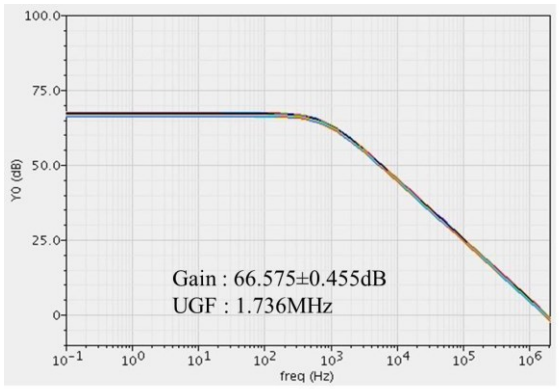
caused by non-linearity of compressed input signal. New input signal compression technique still has gain variation caused by non-linearity of compressed input signal, but the gain variation of new level shifting technique is much smaller than that of input signal compression technique and common mode elimination technique (Table 6.10). It is worth noting that the differential signal compression rate of new input signal compression technique is smaller than that of input signal compression technique or common mode elimination technique. The smaller differential signal compression rate means that the

	Input Signal Compression	Common Mode Elimination	New Input Signal Compression
Supply Voltage	1V	1V	1V
ICMR	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
CM Compression Rate	62.32%	99.63%	93.2%
DM Compression Rate	62.32%	71.4%	50%
Avg. Gain	45.455dB	43.295dB	66.575dB
Gain Variation	±0.985dB	±1.075dB	±0.455dB
Unity Gain Freq.	26.9KHz	12.63KHz	1.736MHz
Phase Margin	58.1º	57.3º	58.1º
CMRR	≥ 56.26dB	≥ 115.1dB	≥ 83.2dB
Avg. Power Consumption (@150Hz)	38.875μW	40.39μW	69.74μW

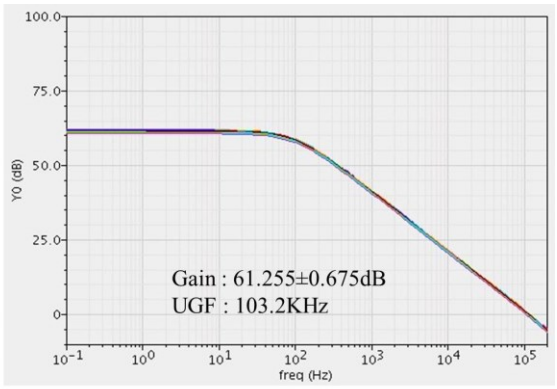
Table 6.10 Schematic Simulation Results Comparison of Three Techniques

larger differential signal can be transferred to the next stage. Therefore, the gain of new input signal compression technique is much larger than that of two techniques.

The noise of new input signal compression technique is reduced using large transistors of input differential pairs and folded cascode current summing stage. The schematic simulation results comparisons are given in Figure 6.20 and Table 6.11. Because of the noise reduction with large transistors, 1.736MHz of unity gain frequency of new input signal compression technique (Figure 6.19) is reduced to 103.2KHz (Figure 6.20 and Table 6.11). Even though the unity gain frequency of new input signal compression technique is reduced due to the noise reduction, reduced unity gain frequency, 103.2KHz, is larger than that of input signal compression technique, 26.9KHz,

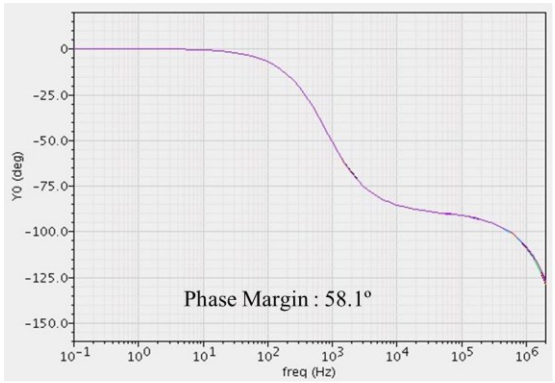


Before Noise Reduction

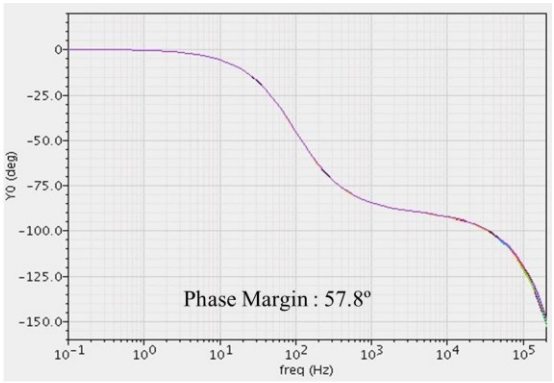


After Noise Reduction

(a) Comparison of Gain and Unity Gain Frequency

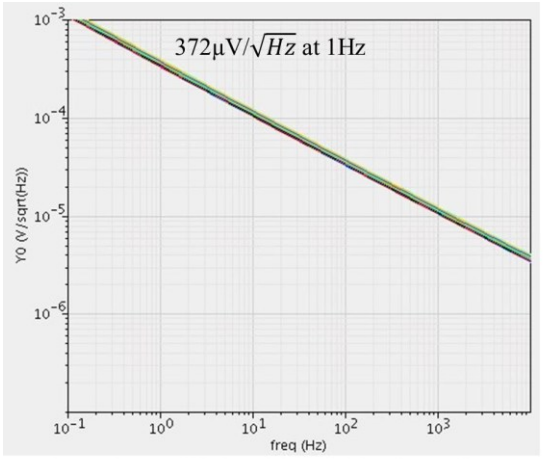


Before Noise Reduction

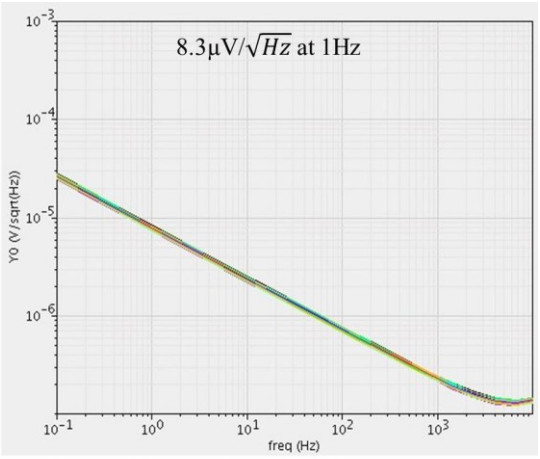


After Noise Reduction

(b) Comparison of Phase Margin



Input Referred Noise Before Noise Reduction



Input Referred Noise After Noise Reduction

(c) Comparison of Noise

Figure 6.20 Schematic Simulation Results Comparison of Before and After Noise Reduction

	Before Noise Reduction	After Noise Reduction
Supply Voltage	1V	1V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.575dB	61.255dB
Gain Variation	±0.455dB	±0.675dB
Unity Gain Freq.	1.736MHz	103.2KHz
Phase Margin	58.1º	57.8º
CMRR	≥ 83.2dB	≥ 84.83dB
Avg. Power Consumption (@150Hz)	69.74μW	68.23μW
Input Referred Noise (@1Hz)	$372\mu V/\sqrt{Hz}$	$8.3\mu V/\sqrt{Hz}$

Table 6.11 Schematic Simulation Results Comparison of New input Signal Compression Technique

or common mode elimination technique, 12.63KHz, without noise reduction. And the gain of new input signal compression technique is still much larger than that of the other techniques.

The layout picture of new input signal compression technique is shown in Figure 6.21. The comparisons of schematic simulation results with noise reduction and post layout simulation results of new input signal compression technique are given in Figure 6.22 and Table 6.12. All the results of post layout simulation are almost same with the schematic simulation results. As mentioned in Chapter 5.1 and 5.2, if the original input signal is compressed, the SNR of overall system is degraded because the compressed signal is transferred to the op-amp while the noise of op-amp is not changed. Even though the compression rate of new input signal compression technique is smaller than that of

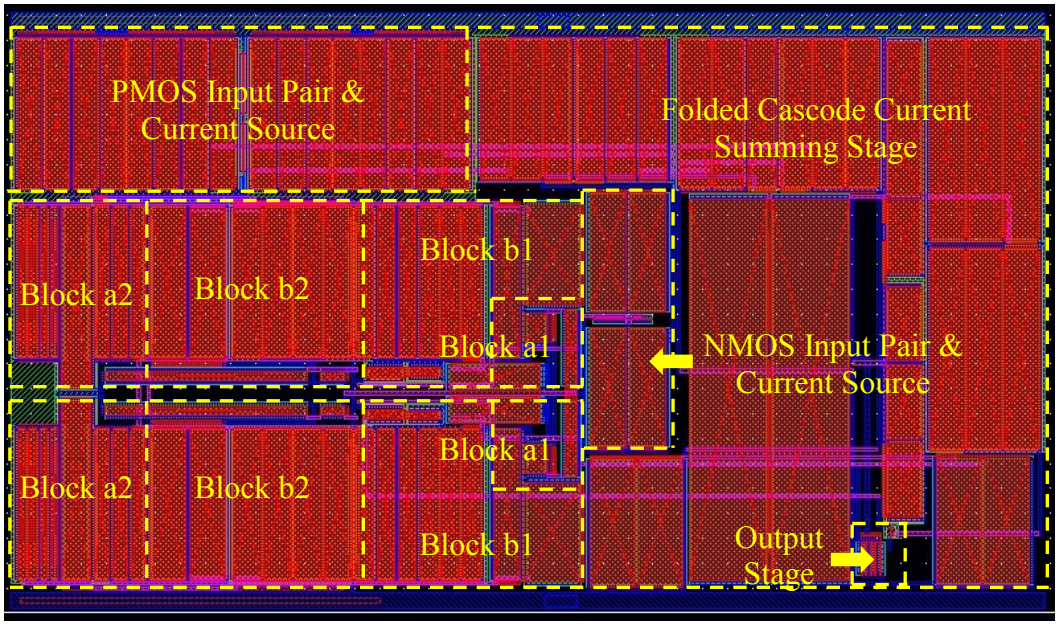
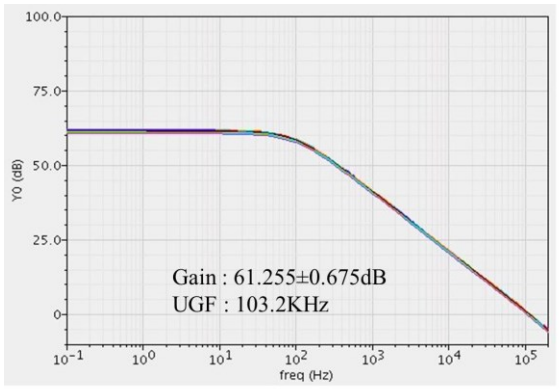
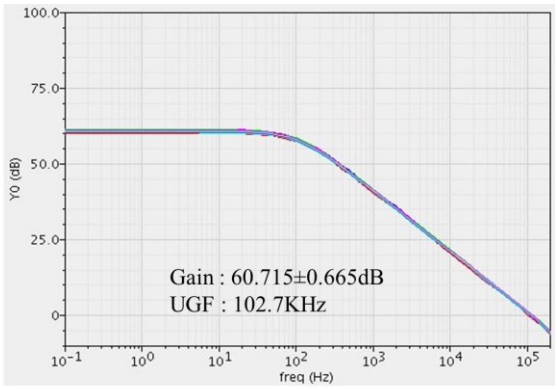


Figure 6.21 Layout Picture of New Input Signal Compression Technique
(207.78μm×119.46μm)

input signal compression technique or common mode elimination technique, the original input signal is compressed in new input signal compression technique and the SNR is degraded. And the input referred noise levels of novel three techniques for the low supply voltage environment, new level shifting, saturation point control, and modified new level shifting techniques, without noise reduction are about 120μV/$\sqrt{Hz}$ at 1Hz. The input referred noise of new input signal compression technique without noise reduction is 372μV/$\sqrt{Hz}$ at 1Hz. For these reasons, the transistors of reduced noise new input signal compression technique op-amp are 40 times larger than the transistors without noise reduction while 25 times larger transistors are employed for novel three techniques, new level shifting, saturation point control, and modified new level shifting techniques. In Figure 6.22 and Table 6.12, the input referred noise of new input signal compression

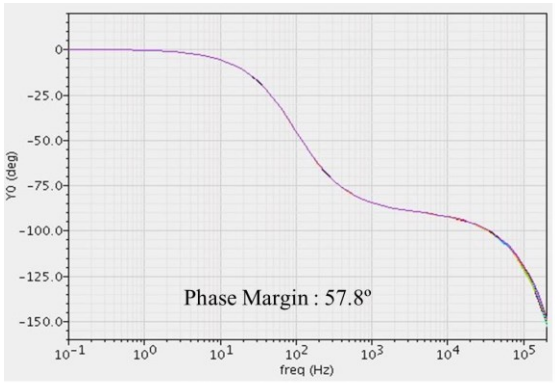


Schematic Simulation

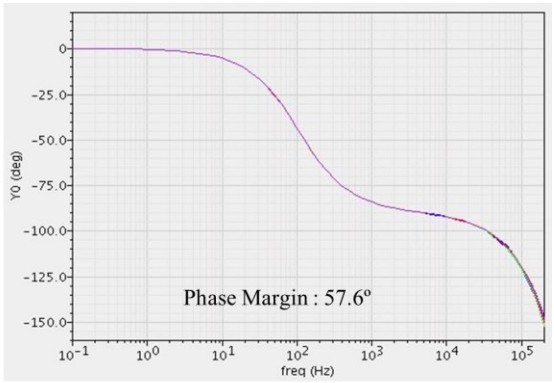


Post Layout Simulation

(a) Comparison of Gain and Unity Gain Frequency

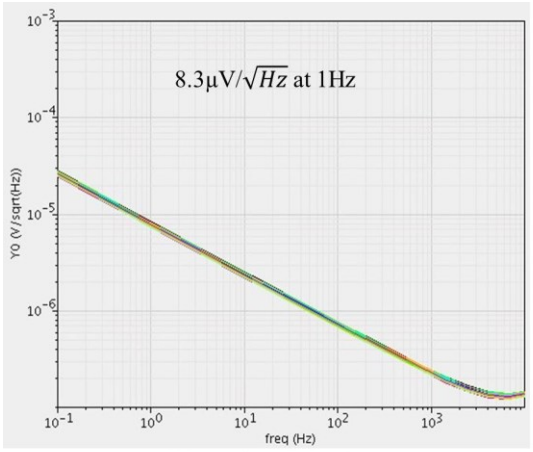


Schematic Simulation

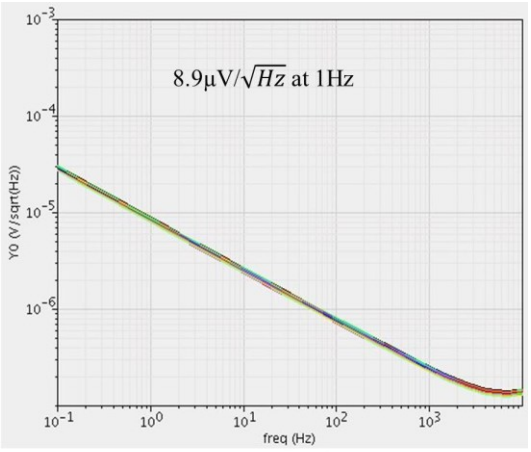


Post Layout Simulation

(b) Comparison of Phase Margin



Schematic Simulation



Post Layout Simulation

(c) Comparison of Noise

Figure 6.22 Comparison of Schematic and Post Layout Simulation Results

	Schematic Simulation Results	Post Layout Simulation Results
Supply Voltage	1V	1V
ICMR	Rail-to-Rail	Rail-to-Rail
Avg. Gain	61.255dB	60.715dB
Gain Variation	±0.675dB	±0.665dB
Unity Gain Freq.	103.2KHz	102.7KHz
Phase Margin	57.8º	57.6º
CMRR	≥ 84.83dB	≥ 82.97dB
Avg. Power Consumption (@150Hz)	68.23μW	70.02μW
Input Referred Noise (@1Hz)	8.3μV/$\sqrt{Hz}$	8.9μV/$\sqrt{Hz}$

Table 6.12 Comparison of Schematic and Post Layout Simulation Results

technique is 8.9uV/$\sqrt{Hz}$ at 1Hz. That is slightly larger than the input referred noises of novel three techniques for the low supply voltage environment, but 8.9uV/$\sqrt{Hz}$ at 1Hz is still lower than the typical noise from the electrode of ECG which is about 10uV/$\sqrt{Hz}$ at 1Hz [24].

The schematic simulation results comparisons without noise reduction of all five novel techniques proposed in this dissertation are given in Table 6.13. Table 6.14 shows the post layout simulation results comparisons of four novel techniques. New level shifting technique, saturation point control technique, and modified new level shifting technique are novel rail-to-rail op-amp techniques for the low supply voltage environment and new input signal compression technique is a novel technique for the extremely low supply voltage environment.

	New Level Shifting	Saturation Point Control	Modified New Level Shifting	Common Mode Elimination	New Input Signal Compression
Supply Voltage	1.6V	1.2V	1.6V	1V	1V
ICMR	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Avg. Gain	77.08dB	75.33dB	77.67dB	43.295dB	66.575dB
Gain Variation	±1.3dB	±0.39dB	±0.24dB	±1.075dB	±0.455dB
Unity Gain Freq.	1.25MHz	1MHz	1.3MHz	12.63KHz	1.736MHz
Phase Margin	58.9º	61.2º	60.72º	57.3º	58.1º
CMRR	≥ 73.29dB	≥ 80.71dB	≥ 82.74dB	≥ 115.1dB	≥ 83.2dB
Avg. Power Consumption (@150Hz)	79.14µW	57.64µW	80.2µW	40.39µW	69.74µW

Table 6.13 Schematic Simulation Results Comparison of All Five Novel Techniques without Noise Reduction

	New Level Shifting	Saturation Point Control	Modified New Level Shifting	New Input Signal Compression
Supply Voltage	1.6V	1.2V	1.6V	1V
ICMR	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Avg. Gain	66.98dB	68.03dB	67.175dB	60.715dB
Gain Variation	±0.76dB	±0.38dB	±0.345dB	±0.665dB
Unity Gain Freq.	374KHz	301KHz	376KHz	102.7KHz
Phase Margin	59.8º	57.4º	59.5º	57.6º
CMRR	≥ 65.33dB	≥ 67.73dB	≥ 74.8dB	≥ 82.97dB
Avg. Power Consumption (@150Hz)	84.7µW	64.83µW	82.9µW	70.02µW
Input Referred Noise (@1Hz)	5.3µV/$\sqrt{Hz}$	5.13µV/$\sqrt{Hz}$	5.225µV/$\sqrt{Hz}$	8.9µV/$\sqrt{Hz}$

Table 6.14 Post Layout Simulation Results Comparison of Four Novel Techniques

The new level shifting technique is the simplest technique among the novel rail-to-rail op-amp techniques proposed in this dissertation. However, this technique has the worst gain variation and average power consumption. Saturation point control technique has the smallest average power consumption and very small gain variation characteristic. The supply voltage of saturation point control technique is slightly larger than that of new input signal compression technique, but the structure is simpler than that of ne input signal compression technique. Therefore, the average power consumption of saturation point control technique is smaller than that of new input signal compression technique. The smallest gain variation technique is modified new level shifting technique. Using the advantages of new level shifting technique and saturation point control technique, the variation of gain can be minimized. The average power consumption of this technique, however, is higher than that of saturation point control or new input signal compression technique. One of the main advantages of new input signal compression technique is that this technique is working in the extremely low supply voltage environment and can overcome the dead zone problem of the extremely low supply voltage environment. The other techniques, new level shifting technique, saturation point control technique, and modified new level shifting technique, are working in the low supply voltage environment. Therefore, this technique has the smallest supply voltage among the proposed techniques. And new input signal compression technique has the largest CMRR because this technique employs the concept of common mode elimination technique. However, this technique has relatively large gain variation and the unity gain frequency of this technique is slightly smaller than the other three techniques. One of the main

disadvantages of new input signal compression technique is relatively large input referred noise.

Chapter 7. Conclusion

Five novel rail-to-rail op-amp techniques for the portable ECG amplifier are discussed in this dissertation. The gain, bandwidth, input impedance, and CMRR of all novel techniques are considered for the ECG system and especially, for the portable electronic biomedical device, operation in the low supply voltage environment is the main consideration of this research for low power consumption. Three techniques of novel rail-to-rail op-amp techniques, the new level shifting technique, the saturation point control technique, and the modified new level shifting technique are proposed for the low supply voltage environment and can avoid the transconductance variation problem of the complementary input differential pair structure. Two techniques of novel rail-to-rail op-amp techniques, the common mode elimination technique and the new input signal compression technique, are proposed for the extremely low supply voltage environment and overcome the dead zone problem.

Large transistors are employed for the input referred noise reduction for all novel techniques, except for the common mode elimination technique. One of the main drawbacks of common mode elimination technique is the reduced bandwidth problem and this noise reduction method with large transistors is not appropriate for this technique. All other novel techniques endure the reduced bandwidth because of large input transistors for the noise reduction, but still have enough bandwidth for the ECG system.

All novel techniques ensure constant operation over the entire rail-to-rail input common mode range. All the simulation results shows constant transconductance, constant gain, and unity gain bandwidth. Cadence SPECTRE simulator and TSMC 0.25-μm CMOS technology are used for the schematic and post layout simulations.

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Appendix

Low Power Weak Inversion Op-Amps

In [75], op-amps operating in the weak inversion region and strong inversion regions are compared and explained. Operating transistors in weak inversion has several advantages such as higher voltage gain, low power consumption, decreased distortion, higher output resistance, and so on. All five novel techniques of this dissertation are operated in strong inversion region and for the comparison of weak inversion and strong inversion regions operation, the new level shifting technique is simulated in weak inversion region as an example.

As mentioned in [75], V_{eff} of weak inversion region operation is below 20mV while that of strong inversion region operation is over 80 ~ 220mV. ($V_{eff} = |V_{gs}| - V_{th}$) The bias currents of the op-amp architecture used in the new level shifting technique were adjusted so the amplifies operated in the weak inversion region. The currents of complementary input differential pairs and folded cascode current summing stage were originally all 10μA and V_{eff} was about 250mV. For weak inversion region operation, the currents of complementary input differential pairs and folded cascode current summing stage were reduced from 10μA to 3.3μA. Because of reduced drain current, $|V_{gs}|$ of input stage and folded cascode stage devices were smaller than that of strong inversion region operation and as a result, V_{eff} of devices reduced to about 10mV. The simulation results

	Strong Inversion Region	Weak Inversion Region
Supply Voltage	1.6V	1.6V
ICMR	Rail-to-Rail	Rail-to-Rail
V_{eff}	≈ 250mV	≈ 10mV
Gm Variation	±8.66%	±9.78%
Avg. Gain	77.08dB	81.14dB
Gain Variation	±1.3dB	±1.34dB
Unity Gain Freq.	1.25MHz	1.3MHz
Phase Margin	58.9º	57.1dº
CMRR	≥ 73.29dB	≥ 83.66dB
Current Source	10μA	3.3μA
Avg. Power Consumption (@150Hz)	79.14μW	35.7μW

Table A. 1 Simulation Results Comparisons of Strong and Weak Inversion Regions Operation

comparisons are given in Table A. 1. Because of the reduced currents, the power consumption is decreased significantly. Notice that overall the specifications of the reduced power operation are very close to that of the higher power case, but some increased gain variation versus common mode input voltage is observed. Slew rate, which was not specified or simulated in this thesis, is also lower.