Design of a Fourth-Order Continuous-Time Delta-Sigma A/D Modulator with Clock Jitter Correction

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This thesis is dedicated to my family for years of support and love.

Abstract

In recent years, there has been growing interest in both industry and academia to use delta-sigma A/D converters for wideband wireless communication applications. Continuous-time (CT) delta-sigma modulators (ΔΣM) are of particular importance, mainly due to their advantages in terms of low power consumption, low noise, high speed and inherent anti-aliasing filtering capability. However, they are much more sensitive to clock jitters than their digital-time (DT) counterparts, limiting their practical applications.

In this project, we present a CT delta-sigma modulator design that can significantly reduce the clock jitter effects. A top-down methodology is utilized starting from the system-level design, and then followed by circuit-level design. In the system-level design, key design challenges are addressed and various non-ideal effects including clock jitter effects are modeled with MATLAB/SIMULINK to determine the specifications for each building block. In particular, it is shown that a simple fixed-width return-to-zero (RZ) current feedback technique can effectively reduce the SNR loss caused by clock jitters. System-level simulation outputs are then used as input constraints for the circuit-level design, which consists of a 1.5V CT ΔΣM in IBM 0.13μm process compatible for use with the WCDMA technology. The building blocks include operational transconductance amplifiers (OTAs), comparator, return-to-zero logic circuit, digital-to-analog (DAC) current feedback blocks and summing block. Circuit design and layout were completed using Cadence Design Systems software. Simulations show that this ΔΣM circuit has a SNR of 65.5dB for a 0.1V input at 468.75kHz.

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1.1 Introduction

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a converting system which converts continuous signals to discrete digital numbers. There are many different building circuits to perform A/D conversion, for example Nyquist-rate ADCs [52]. Conventional techniques require precise analog components and are susceptible to noise and interference. Delta-sigma modulators (ΔΣM) can achieve high performance through oversampling and noise-shaping, while at the same time require less strict component precisions [1],[2]. The implementation of ΔΣM circuits can be effectively realized using low-cost CMOS processes. Moreover, by choosing different sampling rates (i.e., different over-sampling ratios), the same delta-sigma modulator architecture can be adapted to meet different requirements [53]. This adaptability makes ΔΣM very suitable for a multi-standard scenario such as cellular applications, where wireless receivers have to support multiple technologies, such as GSM, DECT, and wideband CDMA (W-CDMA) operations [4],[6]. In the following of the chapter we will explain basic ideas behind ΔΣM, system design choices and examples.

1.2 Delta-Sigma Modulator

Figure 1-1 shows a general simplified block diagram of a digital Delta-Sigma modulator. A delta-sigma modulator consists of three main components: a loop filter (or loop transfer function *H(z)*), an analog-to-digital converter (or a clocked quantizer), and a feedback digital-to-analog converter (DAC) [2],[3],[4],[5]. As shown in the block diagram, the input *x* goes through the loop filter and then is converted to a digital word sequence whose spectrum approximates the input well in a narrow frequency range but with quantization noise. In the feedback loop, the digital output is then converted back to an analog signal which is fed back into the loop filter, and then the loop filter can "shape" the quantization noise away from the desired frequency range. This is how delta-sigma modulator works as an analog-to-digital converter.

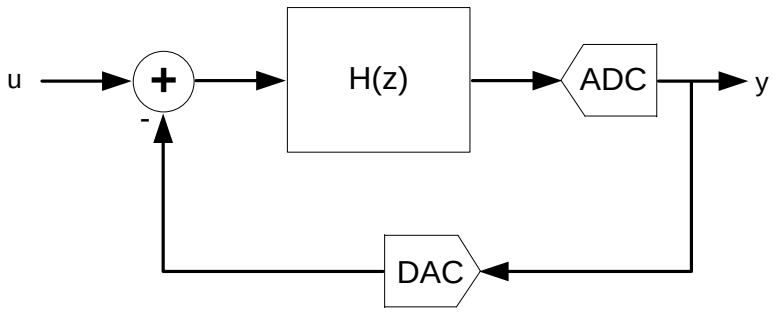

Figure 1-1 Simplified block diagram of a Delta-Sigma modulator

In a simplified linear model, the quantizer can be replaced by an adder and quantization noise *e* (approximated by white noise) which is independent of the input *u* [1],[2],[3],[4]. Then the system shown in Figure 1-1 can be replaced by the one in Figure 1-2. The output y can be written in terms of the two inputs *u* and *e* which is:

$$Y(z) = \frac{H(z)}{1+H(z)}U(z) + \frac{1}{1+H(z)}E(z)$$

$$= STF(z) \bullet U(z) + NTF(z) \bullet E(z) \qquad (1.1)$$

From the equation (1.1), we call STF (z) signal transfer function and call NTF (z) noise transfer function.

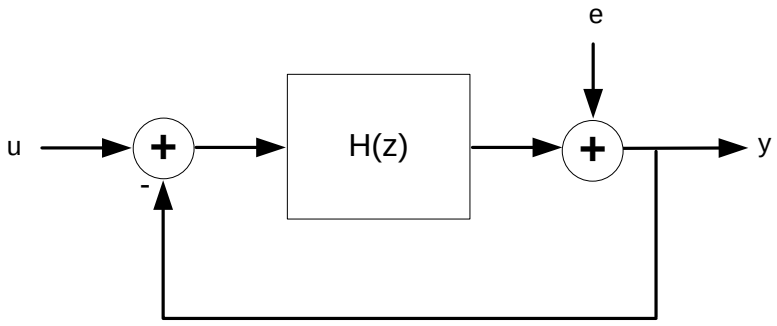

Figure 1-2 Linearized block diagram of a Delta-Sigma modulator

1.2.1 Over-Sampling

As we know, the Nyquist theorem states that in order to fully recover a sampled input signal, the samples must be taken at frequency greater than two times the bandwidth of the input signal. Aliasing will occur and the recovered signal will have distortion if the

sampling frequency does not meet requirements. Oversampling means sampling at a frequency much greater than the Nyquist frequency. We define the oversampling ratio (OSR) as the sampling frequency f_s over Nyquist frequency f_N. Compared to the Nyquist-rate data converters, over-sampled $\Delta\sum$M have demonstrated lower sensitivity to the analog component imperfections, thanks to a higher sampling rate and more complex digital signal processing. Quantization noise occurs when discrete-time analog sample values are converted to finite-state numbers. Oversampling will not reduce the amount of total quantization noise, but it will spread the noise across a larger frequency spectrum so that the power of in-band quantization noise is reduced [1],[2],[3],[4],[5]. Delta-sigma techniques make use of this characteristic by following the converter with a decimation filter and removing the high frequency noise.

1.2.2 Noise Shaping Technique

Noise shaping is further used to reduce the noise power in the signal band [1],[2],[3], [4],[5]. Its purpose is to increase the apparent signal-to-noise ratio (SNR) of the resultant signal by altering the spectral shape of the error that is introduced by quantization such that the noise power is at a lower level in frequency bands at which noise is perceived to be more undesirable and at a correspondingly higher level in bands where it is perceived to be less undesirable. Noise shaping happens because of the loop filter transfer function of a $\Delta\sum$M is composed of a STF and a NTF. The STF is designed to have constant gain over all frequencies, while the NTF is designed to have small gain at lower frequencies and larger gain at higher frequencies. Therefore, the NTF can be designed to have minimal gain around the band of interest. When followed by a filter, much of the noise can be removed.

In summary, over-sampling spreads the quantization noise power over a larger bandwidth, and noise shaping pushes the noise out of the band of interest. The output of a delta-sigma modulator is a high speed, low-resolution digital sequence. The out-of-band quantization noise is further removed with a decimation filter, and the final output is a

high-resolution digital signal at a lower speed usually equal to twice the frequency of the desired signal bandwidth.

1.3 Delta-Sigma Modulator Design Choices

When we start to design a ΔΣM, there are several aspects we need to consider: modulator order, oversampling ratio, quantizer resolution, filter type, and discrete-time versus continuous-time. The world of noise-shaping converters can be roughly divided into the following camps: single-bit single-loop low-order designs, single-bit single-loop high-order designs, multi-loop cascaded designs with feed-forward error cancellation, and multi-bit noise shapers (both low and high order). In general single–bit high-order designs are most attractive due to their simplicity and easiness of design.

1.3.1 Modulation Order

Modulator (or loop filter) order determines the noise shaping capability of the loop filter. A loop filter is realized by switched-capacitor integrators in a DT implementation and continuous-time integrator in CT implementation. Figure 1-3 and 1-4 are block diagrams of first order and n-th order modulators, respectively.

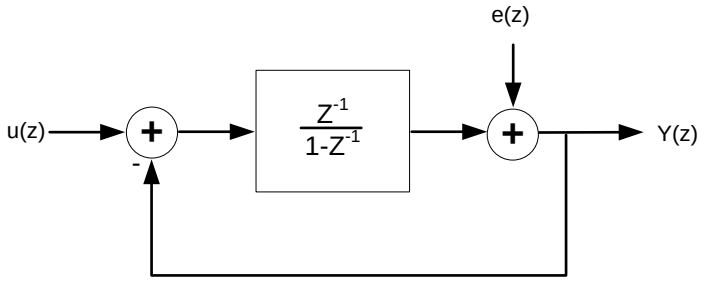

Figure 1-3 1st-order ΔΣM

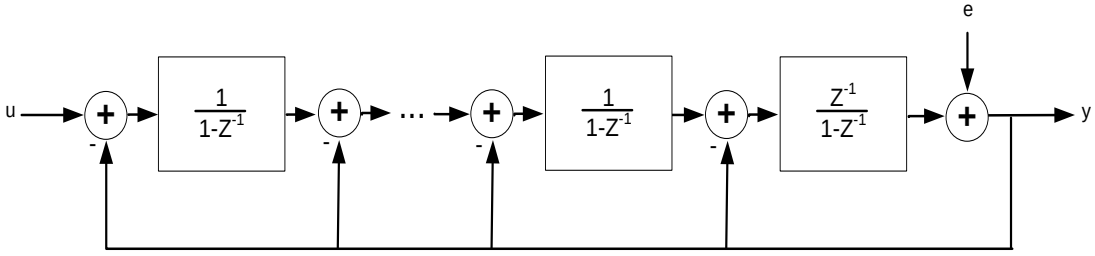

Figure 1-4 nth-order ΔΣM

In this project the specifications were designed for WCDMA-mode compatibility, for the channel bandwidth of 1.92MHz it requires around 70dB SNR [6]. Under such requirement, a 4th-order modulator was chosen. Of course, higher order modulators do have their limitations. The overall stability of the loop filter becomes conditional to the input after order greater than two [2]. Also, as order increases so does complexity of design and analysis.

1.3.2 Oversampling Ratio (OSR)

Oversampling Ratio defines as the ratio between sampling frequency and two times of signal bandwidth. Oversampling a signal spreads out the quantization noise over a greater frequency band. If the oversampling ratio is doubled, the noise is spread over twice the frequency band. If looking at just the band of interest, the amplitude of the quantization noise power has reduced by half, and thus SNR is increased by 3dB. Some limitations on increasing the OSR include clock speed and decimation filter complexity [5]. In this project, the OSR of 40 has been chosen for the 4th order $\Delta\sum$M.

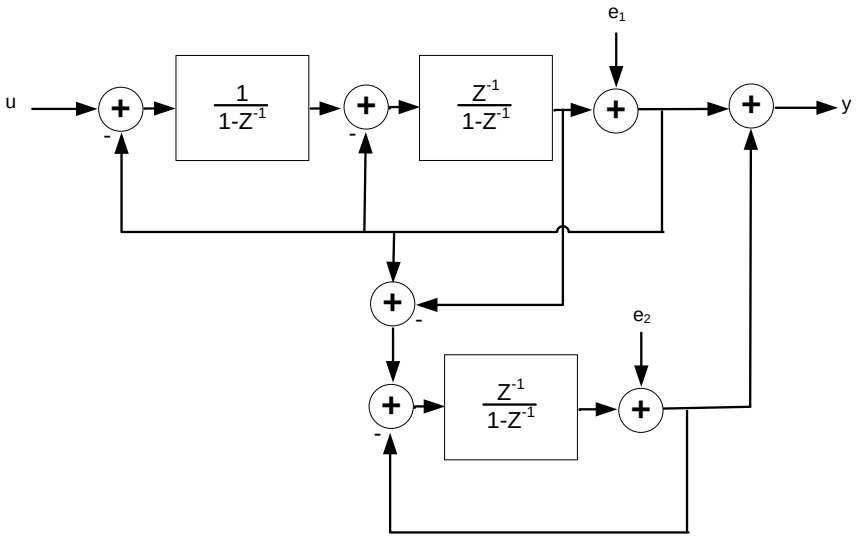

Figure 1-5 An example of multi-stage $\Delta\sum$Ms

1.3.3 Single-Stage and Multi-Stage

In single-stage modulators there is only a single quantizer. The digital output of the quantizer is the input to the DAC. Multi-stage is to cascade single-stage modulators. In this technique the quantization noise from the previous stage is the input to the next stage

[5]. The diagram in Figure 1-5 shows a first order modulator cascaded with a first order modulator multi-stage ΔΣM. There are many possible choices for cascaded multi-stage ΔΣM. Multi-stage ΔΣM has some drawbacks including sensitivity to the parameter mismatch between the digital and analog parts [2]. In this project, we chose a single-stage implementation.

1.3.4 Quantizer

The quantizer works as an internal A/D convertor to generate the modulator output. The output of a quantizer can be single-bit or multi-bit. A single-bit quantizer is realized by a comparator. A multi-bit quantizer is normally realized by a flash ADC to obtain higher speed conversion. In an ideal analog-to-digital converter, where the quantization error is uniformly distributed between −1/2 LSB and +1/2 LSB, and the signal has a uniform distribution covering all quantization levels, the signal-to-noise ratio (SNR) can be calculated from:

$$SNR_{ADC} = 20\log_{10}(2^N) \approx (6.0206 * N)dB \qquad (1.2)$$

where N is defined as number of bits. So from equation (1.2), a multi-bit quantizer can significantly reduce the quantization noise by 6dB when each bit is added. Multi-bit quantization can improve modulator resolution and tend to make higher order modulators more stable [5]. However, the complexity of a multi-bit quantizer is higher. In addition, since multi-quantization requires multi-bit feedback DAC, it increases the opportunity for DAC errors caused by DAC nonlinearity. Dynamic element matching techniques can help to compensate for multi-bit DAC errors, but at the expense of increased power and complexity [2]. In this project, a single-bit quantizer is selected.

1.3.5 Filter Choices

Whether we should use a low-pass (LP) modulator or a band-pass (BP) modulator depend on the specific application [2]. LP can be built from integrators since they have poles at DC, and thus building the loop filter with integrators will push noise away from dc. If the loop filter was built from resonators, or local feedback integrators, the noise is pushed away from the resonate frequency and the resulting modulator is BP. BP modulators can be obtained by first designing a LP one and then mapping the z^{-1} terms with z^{-2} [5] or

using other techniques [4]. In this project, a LP has been chosen which the loop filter with integrators will push noise away from dc.

1.3.6 Discrete-time or Continuous-time

ΔΣMs can be implemented using discrete-time (DT) or continuous-time (CT) techniques. Discrete-time (DT) modulators are typically implemented by switched-capacitors and therefore less suitable for high-speed conversions because settling time requirements for the charge transfer between the switched-capacitor integrators boost their power consumption. Therefore, they are used for high-accuracy conversions within a lower bandwidth, for example, in GSM communication [6]. On the contrary, the sampling speed in continuous-time (CT) converters is not limited by the settling requirements. Besides that, these converters have other advantages over their DT counterparts: no sample-and-hold in the front-end, an inherent anti-aliasing filter, and lower thermal noise generation by the filter circuits [5]. This leads to lower power consumption and smaller chip area. However, CT delta-sigma modulators have a few serious drawbacks: they are more sensitive to circuit non-idealities like excess loop delay, time-constant variation, and clock jitter [2]. Excess loop delay can be solved by either return-to-zero DAC feedback technique or by intentionally delaying the modulator output then adding compensation paths around the modulator loop filter. Process-induced time-constant variation can be minimized by on-chip tuning techniques [34]. However, clock jitter remains quite a challenge for CT modulators. In this project, we chose CT implementation of the delta-sigma modulator and proposed a jitter-correction technique to address the jitter effect as will be explained in Chapter 3.

1.4 Continuous-Time Delta-Sigma Modulator System Design

In this project, we design a 4^{th}-order, single-stage CT-ΔΣM with 1-bit quantizer and OSR equal to 40 that can meet 70dB Signal-to-Noise Ratio (SNR) with 1.92MHz signal bandwidth. The next step of system-level design includes modulator topology selection and Noise Transfer Function design (NTF).

1.4.1 Modulator Topologies and NTF Selection

There are two general single-stage topologies, they are: chain of integrators with weighted feed-forward summation (CIFF) and chain of integrators with distributed feedback (CIFB) [2]. Figure 1-6 and 1-7 show the 4th-order Δ-∑ A/D modulator with CIFF and CIFB topologies, respectively. Both have one local resonator feedback loop around a pair of integrators in the noise shaping filter which enables maximum noise-shaping.

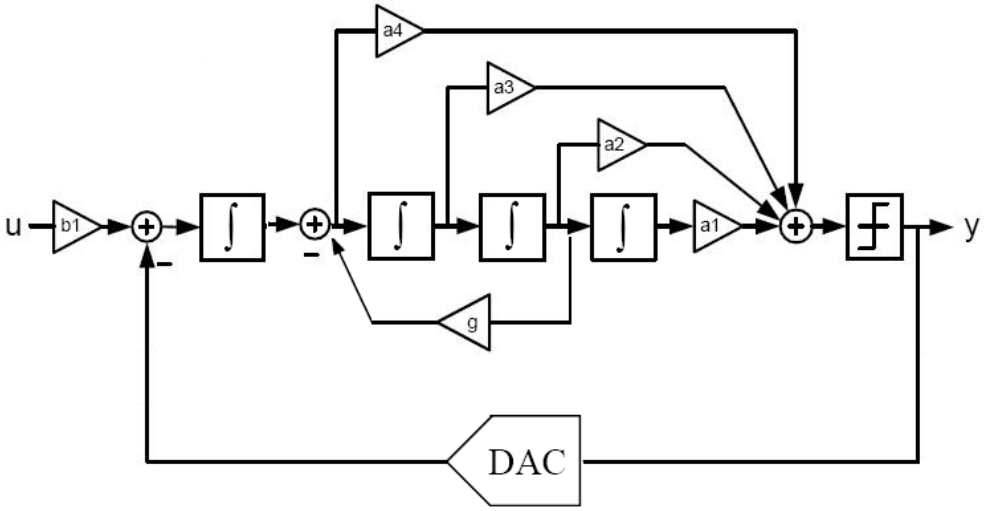

Figure 1-6 4th-order Δ-∑ A/D modulator with CIFF topology

In CIFF topology, the input signal and feedback signal go through the same loop filter. If we do not consider the local resonator, the corresponding STF and NTF are:

$$STF(z) = \frac{b_1 \sum_{i=1}^{4} a_i (z-1)^{i-1}}{(z-1)^4 + \sum_{i=1}^{4} a_i (z-1)^{i-1}} \tag{1.3}$$

$$NTF(z) = \frac{(z-1)^4}{(z-1)^4 + \sum_{i=1}^{4} a_i (z-1)^{i-1}} \tag{1.4}$$

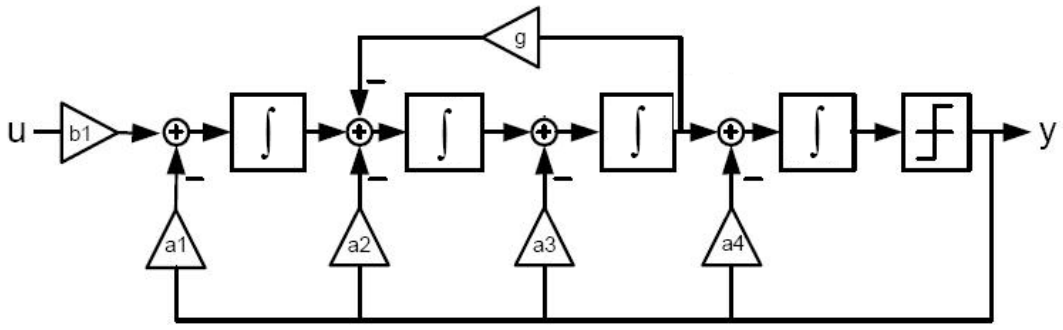

Figure 1-7 4th-order Δ-∑ A/D modulator with CIFB topology

In CIFB topology, the input signal and feedback signal go through different loop filters. Hence if not consider the local resonator the two loop filter transfer function, the corresponding STF and NTF are:

$$STF(z) = \frac{b_1}{(z-1)^4 + \sum_{i=1}^{4} a_i (z-1)^{i-1}} \tag{1.5}$$

$$NTF(z) = \frac{(z-1)^4}{(z-1)^4 + \sum_{i=1}^{4} a_i (z-1)^{i-1}} \tag{1.6}$$

Comparing both topologies, they have the same noise transfer functions. The differences can be found between the signal transfer functions. The STF of CIFB has much better filtering for high frequency signals than the STF of CIFF [49]. However, the drawback of CIFB is that all integrator outputs will contain both input signal as well as filtered quantization noise. This will result in large signal swings at integrator outputs and thus requires higher linearity [49],[50].

1.4.2 Modulator Coefficients

Given the modulator topology, modulator coefficients need to be obtained. A MATLAB toolbox called ‘delsig’ is used in the design as in [46], [8]. For a ΔΣM with 4-th order

and OSR 40, we can use toolbox command 'synthesizeNTF(4,40,1)' to obtain the following z-domain function (1 denotes optimized zeros for the local feedback)

$$NTF(z) = \frac{(z^2 - 1.999z + 1)(z^2 - 1.995z + 1)}{(z^2 - 1.491z + 0.5636)(z^2 - 1.701z + 0.7864)} \tag{1.7}$$

The loop function L(z) is then

$$L(z) = \frac{NTF(z) - 1}{NTF(z)} = \frac{0.802z^3 - 2.10181z^2 + 1.86279z - 0.556785}{z^4 - 3.994z^3 + 5.98801z^2 - 3.994z + 1} \tag{1.8}$$

This function can then be transformed into the continuous domain using the MATLAB function 'd2cm([0.802 -2.10181 1.86279 -0.556785],[1 -3.994 5.98801 -3.994 1],1,'zoh')' and we have

$$L_c(s) = \frac{0.6707s^3 + 0.2448s^2 + 0.0559s + 0.0062}{s^4 + 0.006s^2} \tag{1.9}$$

The continuous-time NTF is further found

$$NTF_c(s) = \frac{-1}{L_c(s) - 1} = \frac{s^4 + 0.006s^2}{s^4 + 0.6707s^3 + 0.2388s^2 + 0.0559s + 0.0062} \tag{1.10}$$

We choose modulator coefficients for topologies shown in Figures 1-6 and 1-7 to match the function given in equation (1.10). Although many solutions exist, we prefer those which do not provide large integrator outputs to avoid possible saturations. The final scaled values used are shown in Table 1-1 for CIFB and Table 1-2 for CIFF topologies. Notice that there is an additional scalar factor 0.634, which is introduced to optimize the modulator coefficients for better performance [49].

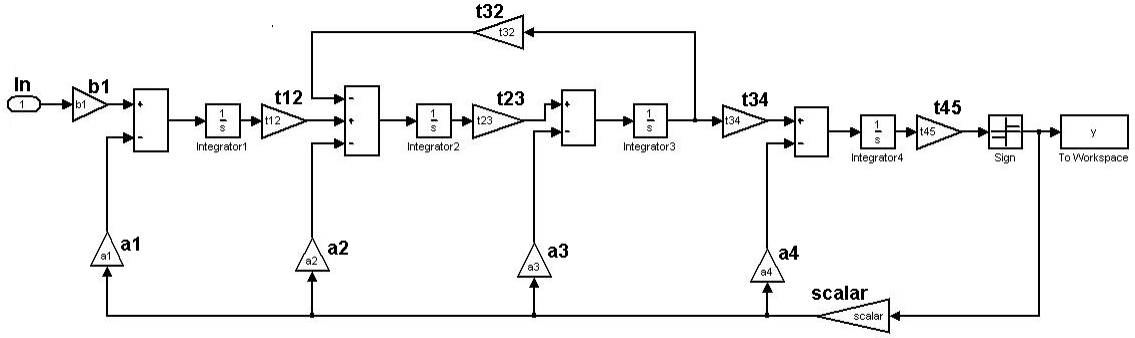

Figure 1-8 CIFB Modulator topology and coefficients

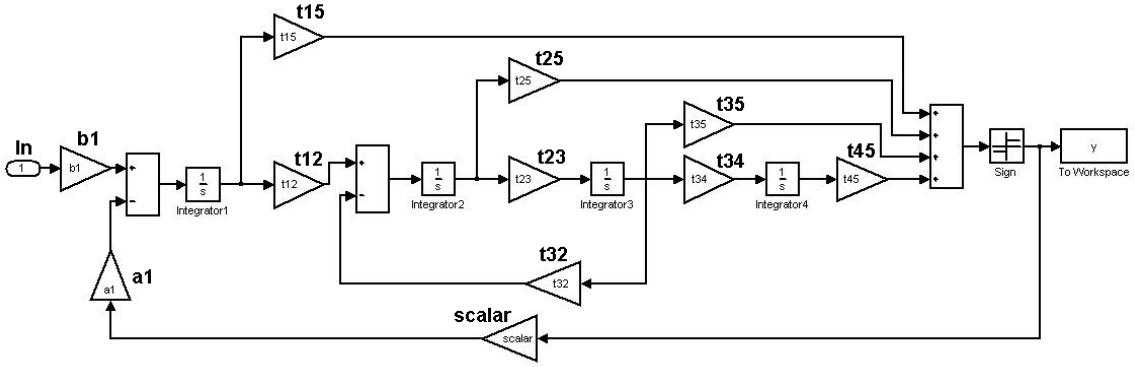

Figure 1-9 CIFF Modulator topology and coefficients

Table 1-1 CIFB Modulator coefficients

Coefficients	Value	Coefficients	Value
b1	0.0889	a1	0.0889
t12	0.1833	a2	0.1379
t23	0.3158	a3	0.2039
t34	0.5714	a4	0.3184
t45	2.1078	t32	0.0168
		scalar	0.634

Table 1-2 CIFF Modulator coefficients

Coefficients	Value	Coefficients	Value
b1	0.4	t15	0.8388
t12	0.5032	t25	0.6101
t23	0.2606	t35	0.5
t34	0.0962	t45	0.6143
a1	0.4	t32	0.02
		scalar	0.634

1.5 Summary

In this chapter we overviewed ΔΣM concepts, design choices and provided an example for WCDMA application. The CIFF and CIFB ΔΣMs we found will be used in the system-level as well as circuit-level simulations in the following chapters.

Chapter 2 Continuous Delta-Sigma Modulator Main Implementation Issues

2.1 Introduction

This chapter discusses main effects of component non-idealities commonly encountered in practice on the performance regarding continuous time delta-sigma modulators. We use the SIMULINK-based models designed in [46],[47] (except clock jitter) to perform system-level behavioral simulations in MATLAB for both CIFF and CIFB topologies. Simulation outputs can be used as inputs to a circuit-level design. Clock jitter models are re-designed and simulations will be presented in Chapter 3.

2.2 Non-Idealities in Delta-Sigma Modulators

A continuous-time delta-sigma modulator normally consists of operational amplifiers (OpAmp) or operational transconductance amplifier (OTA) used for integration, a comparator (single-bit) or a multi-bit quantizer used for quantization, and digital-to-analog (DAC) current feedback blocks. The non-idealities are associated with those components. In this design, OTA has been chosen for integration, single-bit comparator has been chosen for quantization and a switched current DAC has been chosen for digital-to-analog conversion. So the non-idealities of those blocks have been considered and simulated in Matlab and Simulink.

2.2.1 Non-Idealities at the Comparator

2.2.1.1 Hysteresis

Real comparators do not react immediately to the input voltage, which is referred to as hysteresis. Small levels of hysteresis can be considered negligible, due to the fact that since the quantizer is in the loop, any noise introduced by it will be noise shaped out of the signal band [5]. In [46], hysteresis was implemented by adding a small level shift to the quantizer input based upon the previous output, as shown in Fig. 2-1. Figure 2-2 and 2-3 show the PSD for hysteresis levels with values of 0.01, 0.1, and 0.115 for *thr* and compares to the ideal PSD for CIFB and CIFF, respectively. As shown, the PSD of the

modulator is not greatly affected by the quantizer hysteresis until the level of hysteresis is 11.5% of the output of the quantizer. In practice, hysteresis of much less than 1% of the quantizer output can be easily met.

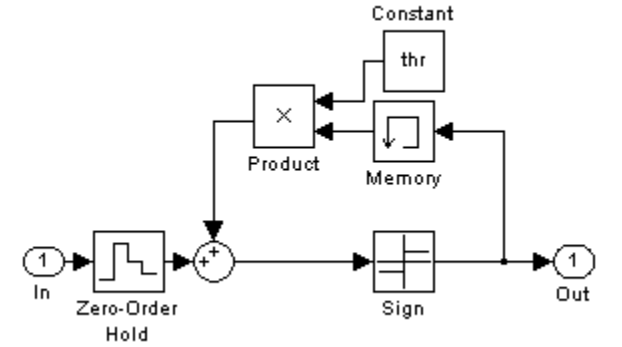

Figure 2-1 Model of quantizer with hysteresis

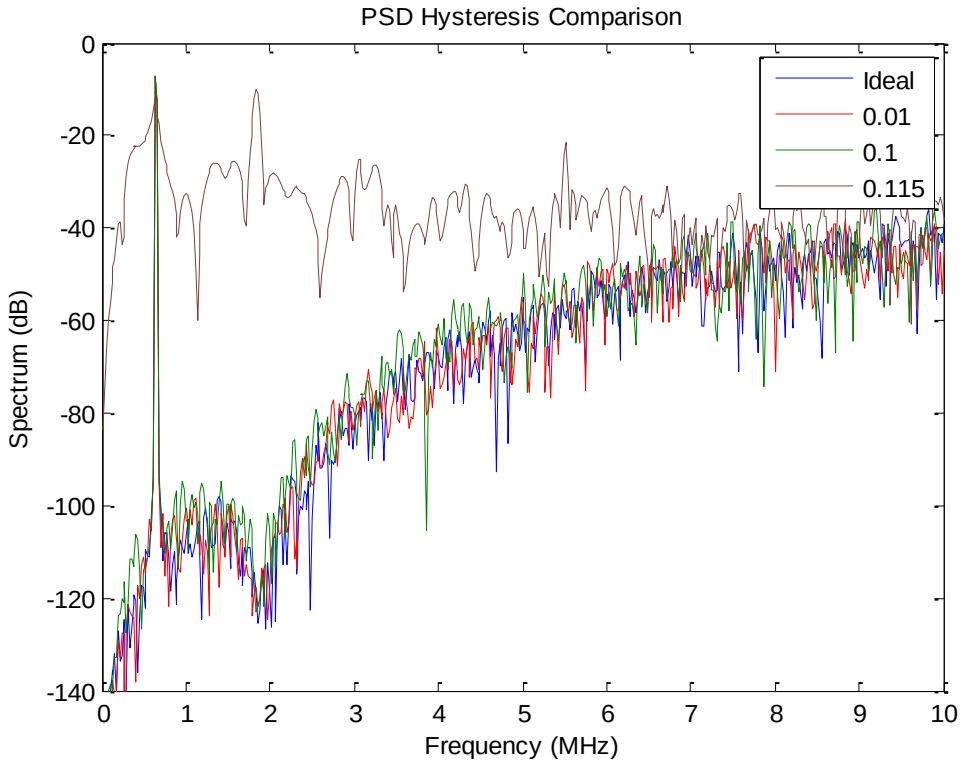

Figure 2-2 CIFB Modulator topology PSD Comparison of quantizer hysteresis

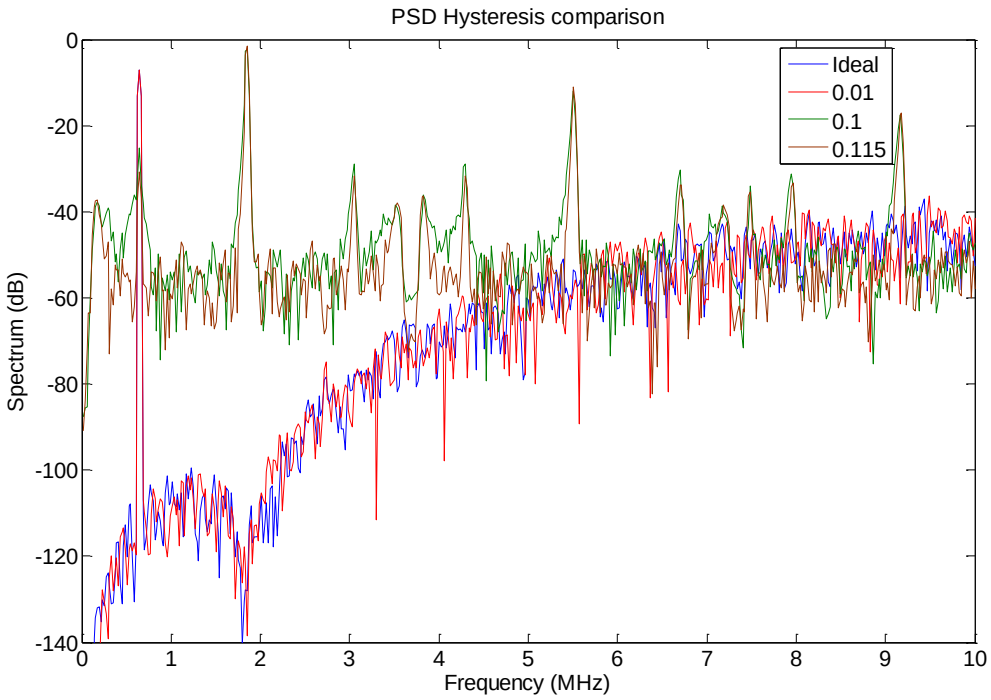

Figure 2-3 CIFF Modulator topology PSD Comparison of quantizer hysteresis

2.2.1.2 Clock Jitter

For comparator, clock jitter introduces sampling errors at the quantizer input (called pulse position jitter). It has been studied that pulse position jitter may be regarded insignificant due to noise shaping and high loop gain of the modulator [2],[3],[4]. For this reason, the jitter effect on comparator will not be studied here. However, the DAC feedback will be more affected which will be studied in detail in Chapter 3.

2.2.2 Non-Idealities at the Integrator

Integrators are the most important building blocks of a ΔΣM and therefore are the places where most of the non-idealities are located. The SIMULINK model of non-ideal integrator is shown in Figure 2-4 which includes [46]:

- Finite DC gain: an ideal integrator has an infinite DC gain, but due to circuit constraints only finite DC gain can be implanted resulting in leaky integration. A feedback loop in Figure 2-4 is used to model the finite DC gain.

- Saturation: saturation affects the dynamic range of signals in a ΔΣM and is modeled by placing the Saturation block from SIMULINK after the integrator as shown in Figure 2-4.
- Integrator nonlinearity: Nonlinearity in analog circuits generates harmonics, which reduces the overall SNR. There are no even order harmonics if the ΔΣM is implemented using a fully differentiable configuration, which makes the third-order harmonic the most significant. In SIMULINK, a user-defined function

$$u + n * u^3 \tag{2.1}$$

is used to model nonlinearity. Here, *u* is the input value and *n* is the nonlinearity coefficient.

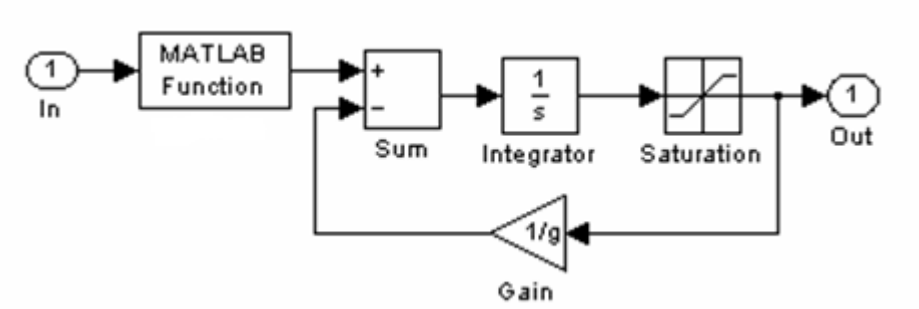

Figure 2-4 SIMULINK Model of non-ideal integrator

Simulations show that the nonlinearity is most important at the first integrating stage. Figures 2-5 and 2-6 compare non-linearity introduced at each integrator for 4-th order CIFB and CIFF, respectively. They are zoomed on the third harmonic as it is the best way to compare the effects. It was found that the non-linearity at the first integrating stage had the largest effect on the SNR. The simulation was done with a nonlinearity factor of 0.01 at each stage and then at all stages. This amount corresponds to about 60dB THD, which can be surpassed in a real circuit. Introducing nonlinearity at the second, third, and fourth stages causes very minute degradation of the SNR and can be considered negligible. This is shown by the distinct similarity when comparing the results of non-linearity at the first stage and the results of non-linearity at all stages.

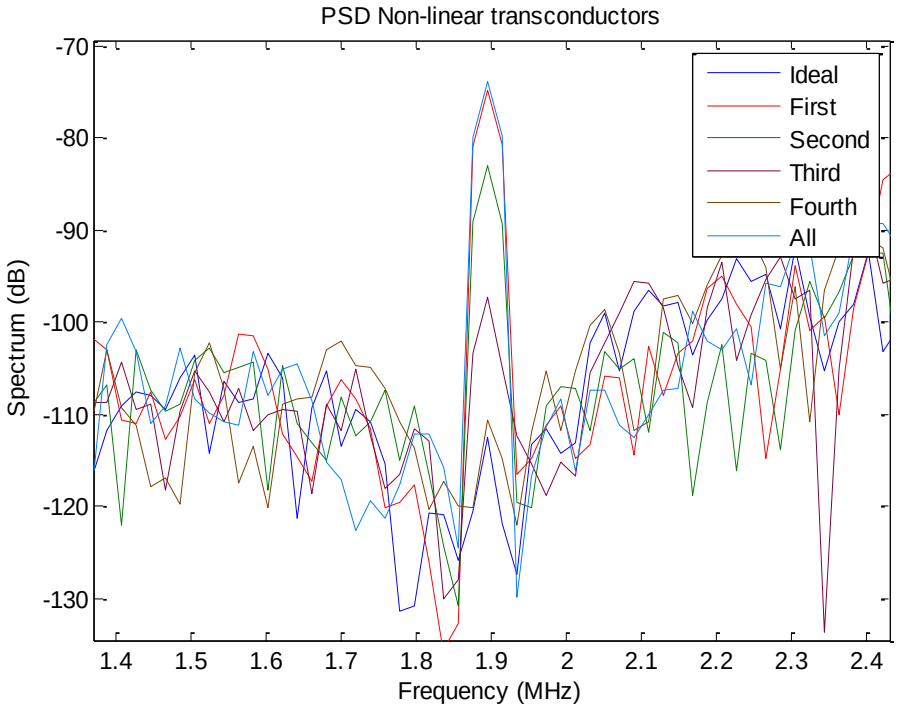

Figure 2-5 CIFB Comparison of third harmonic strength with non-linearity

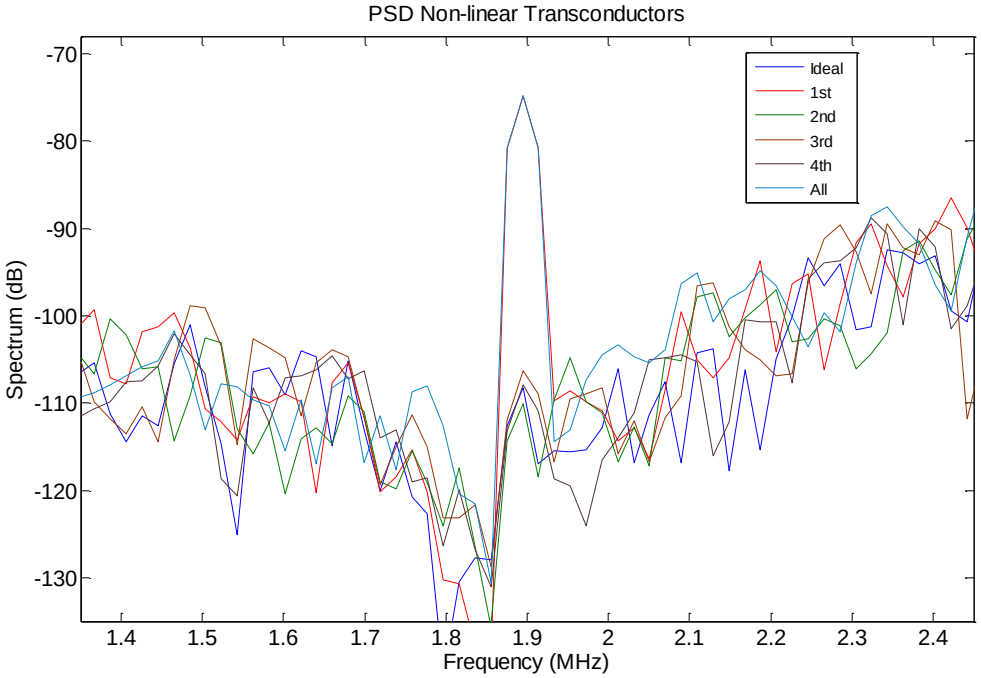

Figure 2-6 CIFF Comparison of third harmonic strength with non-linearity

2.2.3 Non-Idealities at the DAC

2.2.3.1 Clock Jitter

Clock jitter is a serious issue for feedback charge error at the DAC feedback (called pulse width jitter). Pulse width jitter is not noise shaped and any error is directly fed back to the input, which seriously degrades the performance of CT delta-sigma modulators [2],[3],[4]. We will discuss details about clock jitter modeling, jitter correction and simulation in Chapter 3.

2.2.3.2 DAC Feedback Current Variation

DAC feedback current variation (FCV) is caused by the varying integrator output voltage and finite output impedance of the current sources. It is found that the FCV is typically a nonlinear function of the varying integrator voltage. The SNR results in this case are shown in Column three of Table 2-1. It is studied in [51] that if FCV could be made linearly dependent on the integrator output voltage, then SNR would not be significantly degraded. The results in the linear case are shown in Column 4 of Table 2-1.

Figure 2-7 shows the power spectrum of the modulator in three different cases when input is 0.8 peak-to-peak sinusoidal signal at a frequency of 468.75kHz.

Table 2-1 SNR degradation with FCV

input amplitude	without FCV	with FCV	with FCV (linear model))
0.8Vpp	83.0dB	70.2dB	82.9dB
0.6Vpp	80.8dB	74.3dB	80.2dB
0.4Vpp	78.3dB	77.4dB	77.3dB
0.2Vpp	70.9dB	70.1dB	71.2dB

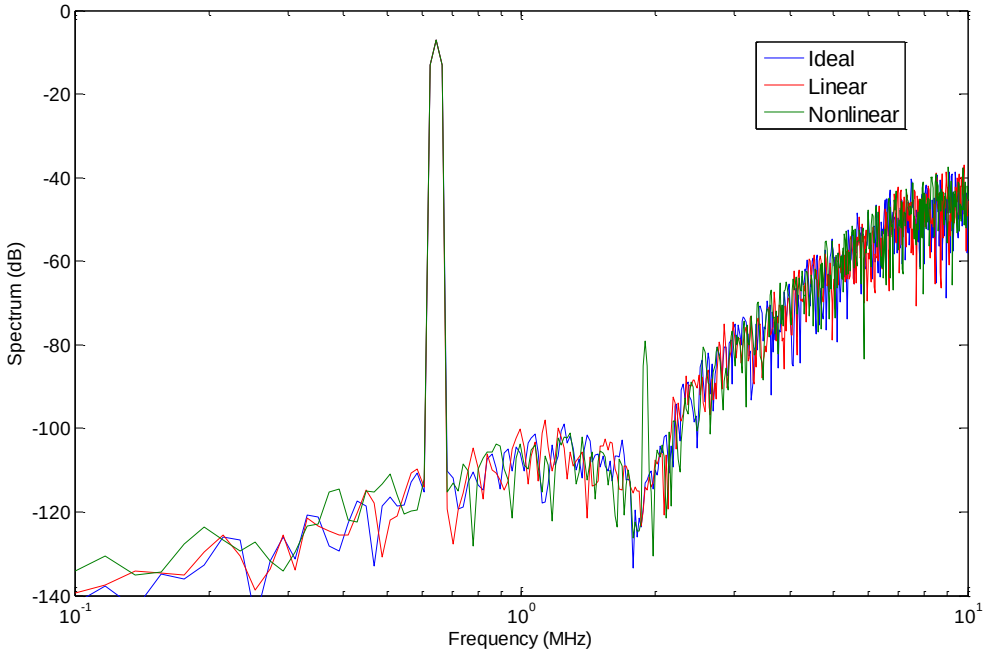

Figure 2-7 PSD comparisons with and without FCV

2.3 Summary

Although system-level simulations do not address all non-idealities in a real-life circuit, it provides valuable insight and design tradeoff for circuit designs. The most important conclusion is that the non-idealities at first-stage integrator in both CIFB and CIFF affect the modulator performance more significantly than other stages. Therefore, a circuit designer should spend more time on optimizing the linearity and noise performance for the first stage than other stages.

Chapter 3 Clock Jitter Analysis and Reduction

3.1 Introduction

As we can see in the previous chapter, the performance of continuous-time delta-sigma modulators depends on many non-idealities associated with the components used for implementation. In this chapter, we will focus on clock jitter effects since continuous-time delta-sigma modulators are very sensitive to clock jitters and various methods have been proposed to deal with this problem in the past years. We will present and simulate a new and simple method to reduce clock jitter effect in MATLAB/SIMULINK [48]. Simulation results show that this method is very effective to reduce the SNR degradation caused by jitter noise.

3.2 Clock Jitter

3.2.1 Clock Jitter Types

The clock jitter refers to the temporal variation of the clock period. There are two typical types of the clock jitter, ICJ (Independent Clock Jitter) which can be modeled as independent Gaussian white noise process, and ACJ (Accumulated Clock Jitter) due to the VCO phase noise which can be modeled as sums of independent jitters. In the case of ICJ, the sampling instants (including both clock rising edge and falling edge) are independent. Suppose the ideal sampling period is *Ts*. Without jitter, sampling instants occur at multiples of *Ts*. Due to jitter, the sampling instants become:

$$t_n = nT_s + \alpha_n, \mathrm{n} = 0,1,2,\ldots \tag{3.1}$$

where α_n is typically modeled as i.i.d. (independent and identically distributed) Gaussian noise. In MATLAB the code *randn* is used to generate a random number with normal distribution of zero mean which is added to the sample time. For ACJ, sampling instants are modeled as the accumulation of all previous sampling intervals. In this case, sampling instants become:

$$t_n = nT_s + \alpha_n, \alpha_n = \sum_{i=0}^{n} \tau_i, n = 0,1,2,\ldots \tag{3.2}$$

where τ_i is the extra jitter of the sampling interval *i* adding to existing jitter α_{n-1} accumulated up to the previous sampling period and is modeled as i.i.d. Gaussian noise [5]. Though the statistics of τ_i are independent and stationary, those of α_n are not. ACJ are typically caused by voltage controlled oscillator with limited stability [5]. In the following analysis, we will consider both types of clock jitters in CT modulators.

3.2.2 Clock Jitter Effects

In CT Δ-Σ A/D modulators, both the quantizer and the feedback DAC are driven by a clock. Clock jitter introduces sampling errors at the quantizer input (called pulse position jitter) and feedback charge error at the DAC feedback (called the pulse width jitter). It has been shown that pulse position jitter incurred at the quantizer input may be regarded insignificant due to noise shaping and high loop gain of the modulator. However, pulse width jitter is not noise shaped and any error caused by jitter is directly fed back to the input and therefore seriously degrades the modulator performance. Therefore, it is very important to reduce the clock jitter effect for CT modulators.

3.2.3 Overview of Clock Jitter Reduction Techniques

In literature, a number of techniques have been proposed to reduce clock jitter effects in CT Delta-Sigma modulators [38]. A simple but not very effective technique is to use NRZ (Non-Return-to-Zero) DAC feedback [5]. Finite impulse response DAC feedback is proposed in [39],[40]. The idea is to use a one-bit quantizer with DAC response widened over *n* clock cycles so as to average clock jitter effects over *n* clock periods. However, the jitter reduction performance is signal dependent and it also increases the loop delay of the modulator [38].

A recent technique is proposed in [41] by employing SC (Switched-Capacitor) feedback used in DT modulators. Instead of having the traditional SI (Switched-Current) DAC feedback over a clock cycle, an exponentially decreasing feedback is generated, as shown in Figure 3-1. Hence, at time of the clock transition, almost all charge has been transferred to the integrator outputs and clock jitter causes little error. But several drawbacks are associated with SC feedback. First, synthesis of a modulator employing

SC feedback is more complicated than a modulator using SI feedback [41]. Second, SC feedback results in integrator response having high-demand for OpAmp slew-rate and gain-bandwidth product, which also increases power consumption.

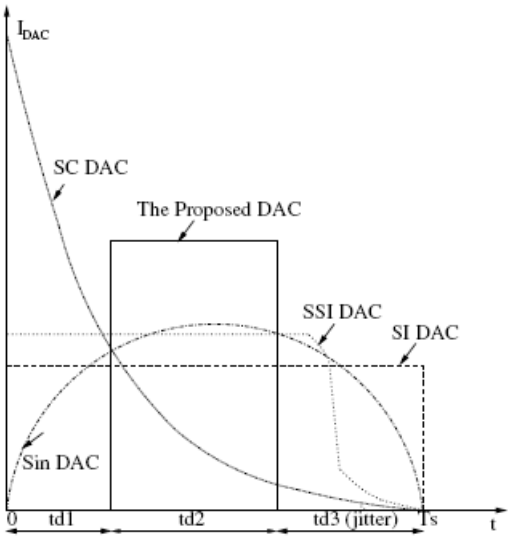

Figure 3-1 Illustration of different jitter reduction techniques

To solve some of the problems with SC feedback, [38] proposes a technique for clock jitter reduction by the use of SSI (Switched-Shaped-Current) DAC feedback. Instead of generating an exponentially decreasing feedback waveform over the whole clock period as in SC feedback, SSI feedback generates a nearly rectangular feedback in most of the clock period, and then exponentially decreasing feedback in the rest of the clock period (shown in Figure 3-1) so that almost all the charge is fed back when the clock jitter occurs. However, the circuit implementation may be difficult to achieve and needs extensive tuning. Besides, like the SC feedback, synthesizing modulators with SSI feedback is also complicated.

Another reported technique to reduce clock jitter explores the use of sin-shaped DAC feedback [42],[43] (shown in Figure 3-1). In this technique, clock transition takes place only when the sin-shaped feedback is at its minimum slope and hence results in a small charge error. But the circuit realization is difficult [38]. In addition, it is sensitive to pulse position jitter and loop delay [43]. Other techniques to reduce clock jitter effects include

revising NTF (Noise Transfer Function) based on an approximate relationship between jitter noise power and NTF of the modulator [44], [2].

3.3 Delayed RZ and Fixed-Width SI Feedback

Comparing all the techniques used on clock jitter reduction, the basic idea is to shape the DAC feedback waveform so that an insignificant amount feedback charge is transferred at time of clock transitions. When designing a DAC feedback for clock jitter reduction, all these factors such as circuit implementation overhead, effect on other circuit elements, power consumption etc, should be considered [38]. Ideally, we still would like to have the traditional SI rectangular DAC feedback waveform, but there has to be a way to finish supplying the nominal amount of feedback charge before clock transitions.

In this section, we propose such a technique. This technique is motivated from delayed RZ (Return-to-Zero) feedback. The idea is to generate a SI feedback pulse as shown in solid line in Figure 3-1, with first a fixed-width RZ time period *td*1, followed by a fixed-width time period *td*2 used for active feedback and finally another RZ time period *td*3. *td*3 is not fixed but subject to clock jitter. As will be shown later, such a technique is easy to implement and is very effective to reduce clock jitter effects.

Figure 3-2 illustrates the proposed technique. First, a jittered clock *CLKJ* is delayed by *td*2 and inverted by the inverter chain to obtain $\overline{CLKJ}$. Note that this inverter chain is very important and it sets a fixed delay between *CLKJ* and $\overline{CLKJ}$. In our design, we set *td*2 to 0.4*Ts*, where *Ts* is the ideal clock period. Then *CLKJ* is AND with $\overline{CLKJ}$ to obtain $CLKJ_N$, which is shown in Figure 3-2. Note that $CLKJ_N$ has a fixed-width time period of logic "1", whereas the time period of logic "0" is not fixed but variable depending on the amount of clock jitter. Further, $CLKJ_N$ is delayed by another inverter chain, the purpose of which is to give a fixed delay *td*1 of $CLKJ_N$. The resulting signal is $CLKJ_{ND}$, as shown in Figure 3-2. Note that now, it can be seen that the signal $CLKJ_{ND}$ is the same as the

desired DAC feedback signal shown in Figure 3-1. This is exactly what we need to correct pulse width jitter.

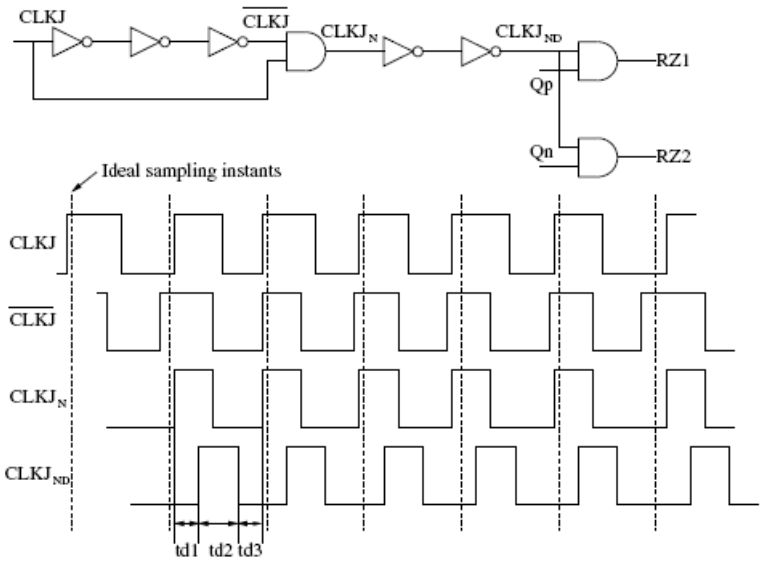

Figure 3-2 The proposed jitter reduction technique

Note that *td*1 and *td*2 are not subject to clock jitter effects since they are set by the delay of the inverter chains, whereas *td*3 is. Since the DAC feedback only supplies feedback charge during *td*2 and is anyway 0 during *td*3, therefore the proposed DAC feedback can supply a constant amount of charge during each (jittered) clock cycle and thus corrects pulse width jitter. Here, we favor the use of *td*1 RZ period mainly because it is preferred in circuit design to eliminate loop delay and memory effect otherwise occurred in NRZ DAC feedback [5],[37].

Finally, note that the signal $CLKJ_{ND}$ is AND with *Qp* and *Qn* to obtain the RZ logic signal *RZ*1 and *RZ*2, which can be used to control a differential DAC feedback circuit, such as a current-steering DAC [5], that is connected to the integrator output terminals in the modulator. We call this technique delayed RZ and fixed-width SI DAC feedback. In Figure 3-2, we assume that the modulator employs single-bit quantization. It is clear this technique also can be applied in multi-bit quantization in CT modulators.

3.4 Behavioral Model Simulations

3.4.1 MATLAB/SIMULINK Models

In order to validate the proposed technique, we perform behavioral simulation in MATLAB/SIMULINK [9]. First, the SIMULINK model used to generate jittered clock is needed. Figures 3-3 and 3-4 show models for generating ICJ and ACJ, respectively. Figure 3-5 shows the jitter correction logic. Since the adopted RZ waveform has the logic "1" with a duration of *0.4Ts*, the total DAC feedback should be scaled up by 0.4.

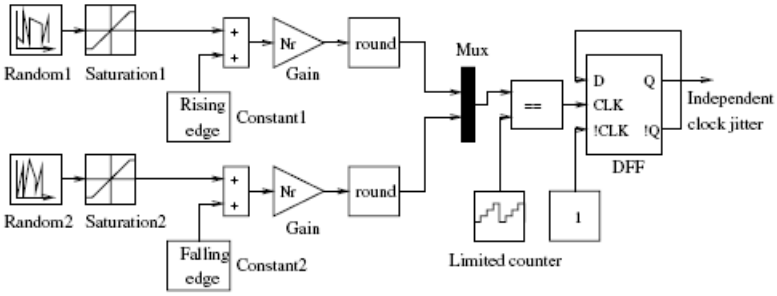

Figure 3-3 SIMULINK model for independent clock jitter generation

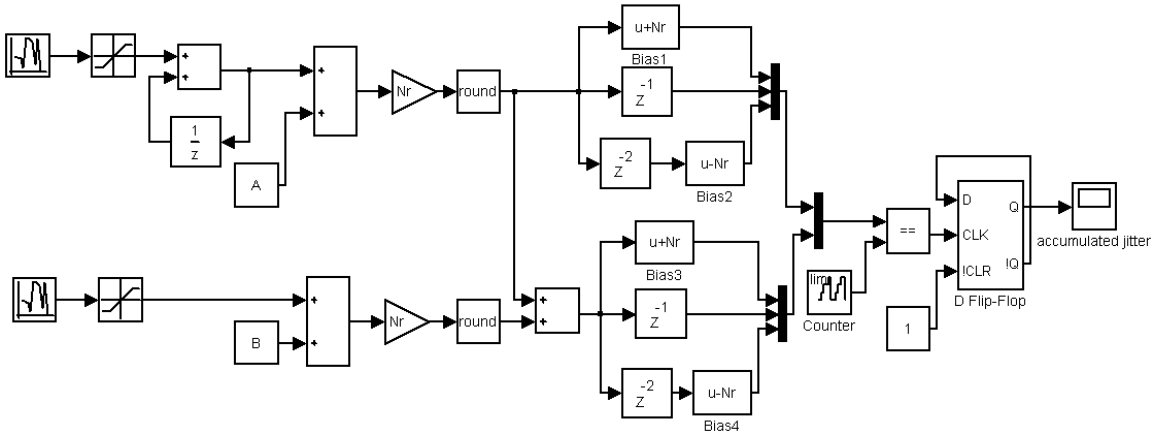

Figure 3-4 SIMULINK model for accumulated clock jitter generation

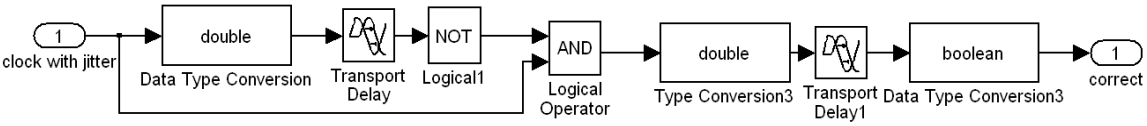

Figure 3-5 The correction logic SIMULINK model

We use a 4-th order CIFF topology as well as a 4-th order CIFB topology to verify the proposed technique. Those topologies are shown in Figure 3-6 and Figure 3-7.

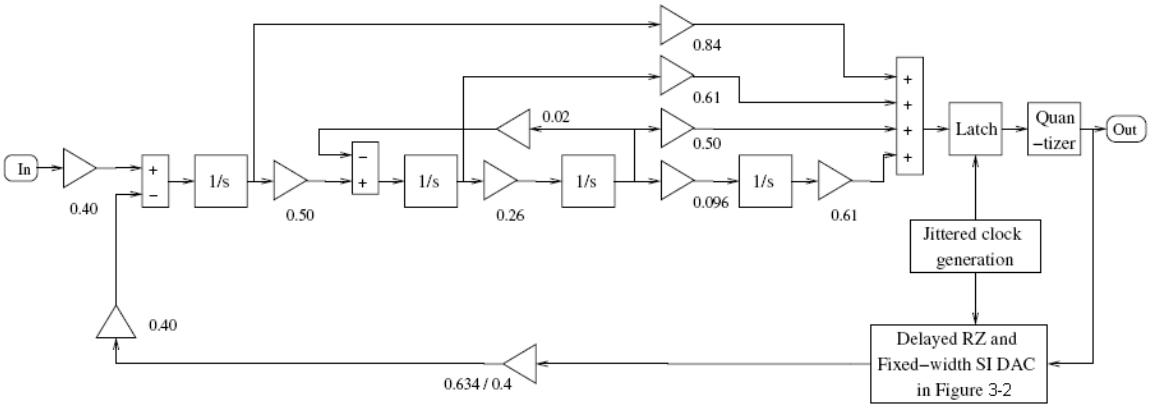

Figure 3-6 SIMULINK model for a 4th-order CIFF modulator topology

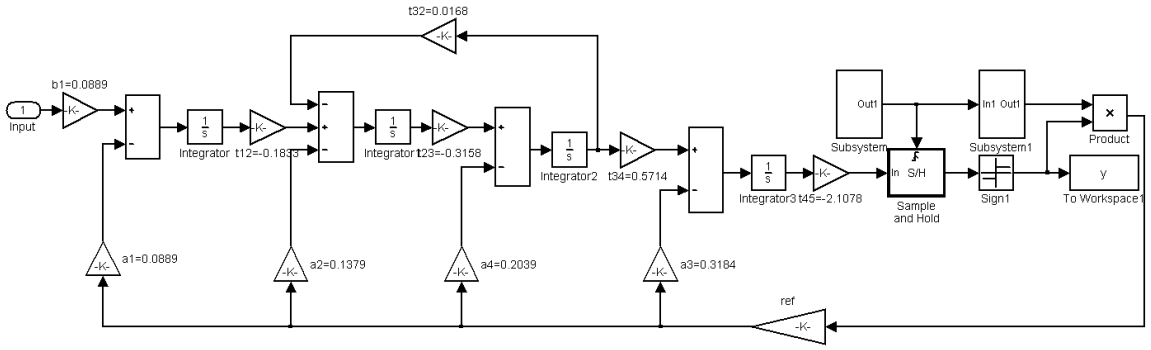

Figure 3-7 SIMULINK model for a 4th-order CIFB modulator topology

3.4.2 Behavioral Model Simulation Results

We first show experiment results in the case of ICJ. Figure 3-8 shows the comparison of SNR of the CIFF modulator with clock jitter and with the proposed clock jitter reduction technique. Note that SNR of the modulator with clock jitter degrades significantly when σ_{CLK} increases. However, when delayed RZ and fixed-width SI feedback is applied in the modulator, the SNR remains quite stable. For example, when σ_{CLK} is $10^{-2}Ts$, the SNR is 76dB, about 33dB higher than SNR of the modulator with clock jitter.

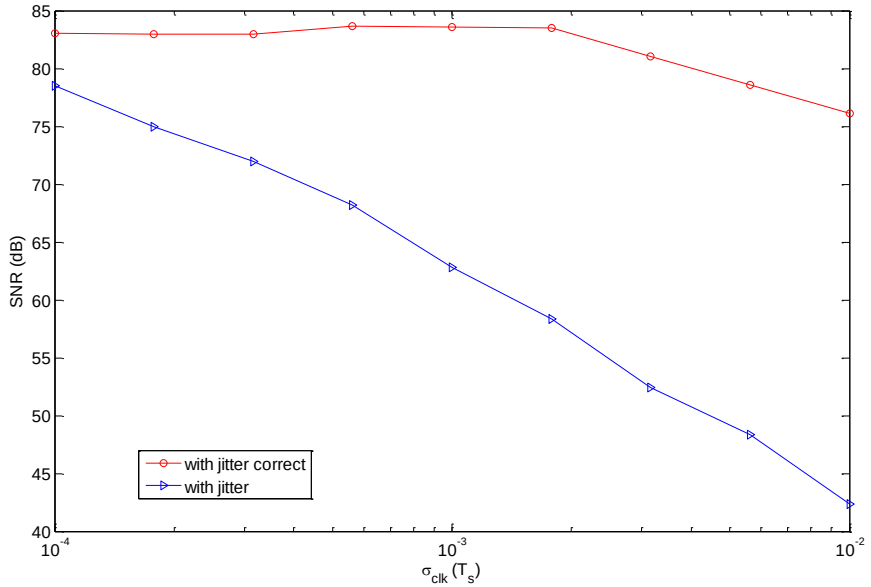

Figure 3-8 SNR comparison of a 4th-order CIFF modulator topology

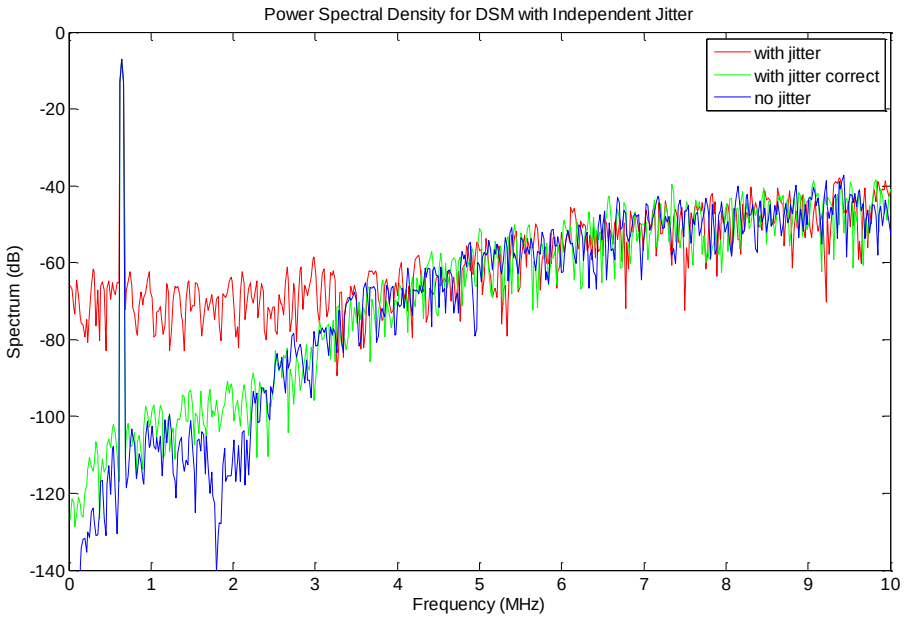

Figure 3-9 PSD comparison of a 4th-order CIFF modulator topology

Figure 3-9 shows a comparison of power spectral density of the CIFF modulator without clock jitter, with clock jitter and with the proposed clock jitter reduction technique when σ_{CLK} is set to $10^{-2}Ts$. In the case of clock jitter, the noise spectrum in the bandwidth

(2MHz in the example) is dramatically whitened. When the jitter reduction technique is applied, the noise spectrum in the bandwidth is close to that of the ideal modulator without clock jitter.

Figure 3-10 shows a comparison of SNR of the CIFB modulator with clock jitter and with the proposed clock jitter reduction. The result is very similar to the CIFF case. When σ_{CLK} is $10^{-2}Ts$, the SNR is 73dB, 30dB higher than SNR of the modulator with clock jitter. Figure 3-11 shows the SNR comparison of a 4th-order CIFB modulator in both behavioral model and transistor level model (a fourth-order CIFB modulator circuit in TSMC 250nm process). It can be seen that in both behavioral model and the transistor level, the proposed jitter reduction method is very effective to the ICJ.

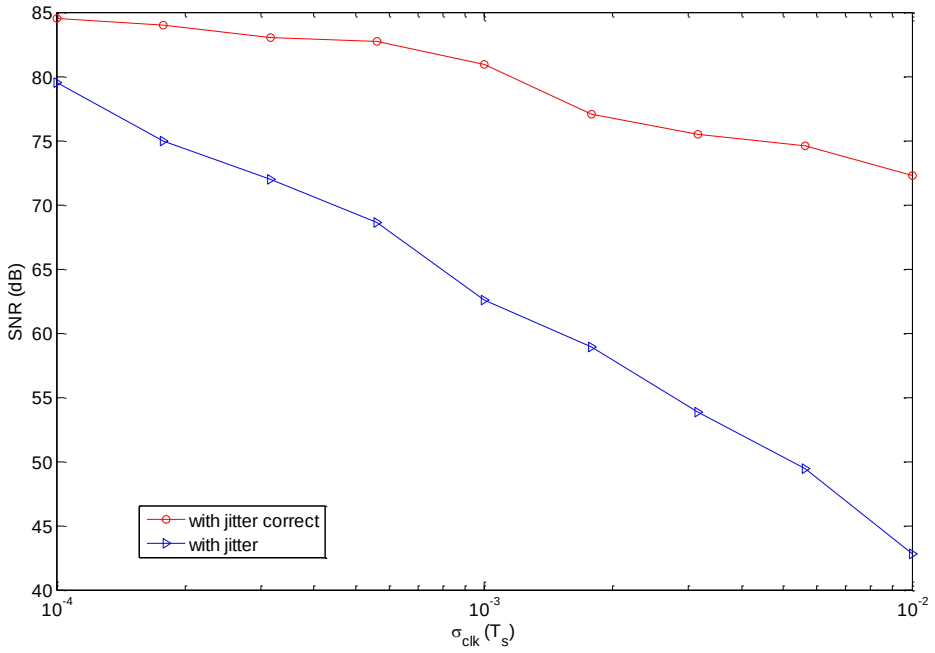

Figure 3-10 SNR comparison of a 4th-order CIFB modulator

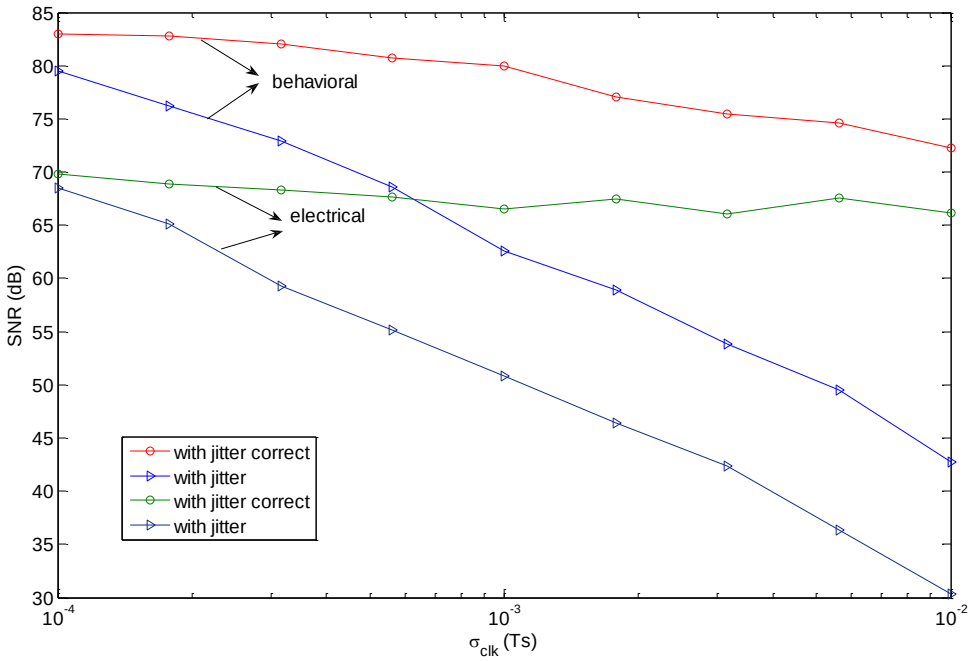

Figure 3-11 SNR comparison of a 4th-order CIFB modulator in both behavioral model

Next, we study the performance of the proposed technique in the case of ACJ. When σ_{CLK} is equal to $10^{-4}Ts$, $10^{-3}Ts$ and $10^{-2}Ts$, the SNR of the modulator is 79dB, 64dB and 43dB, respectively. When the proposed delayed RZ and fixed-width SI feedback is applied in the modulator, the SNR of the modulator is marginally improved to 82dB, 67dB and 48dB respectively. It is obvious that the proposed technique is less effective for ACJ than ICJ. This is due to the significant effect of pulse position jitter in the case of ACJ. In ACJ, the sampling instants could be highly misaligned to the ideal sampling instants (up to $\pm 160\sigma_{CLK}$ observed in our simulations), whereas in ICJ the sampling instants is at most $\pm 5\sigma_{CLK}$ away from the ideal sampling instants. Therefore, ACJ is much more harmful than ICJ. Note that in our simulations, we consider a relatively large clock jitter range ($\pm 5\sigma CLK$). If it is set smaller, the proposed technique would work better for ACJ, since the effect of pulse position jitter is less serious compared to pulse width jitter which can be reduced. This was observed in our simulations.

Compared to other jitter reduction techniques reported in literature [2],[38-44], which consider only the case of ICJ, the proposed technique is more effective in terms of SNR improvement. For example, when σ_{CLK} is $10^{-2}Ts$, the reported SNR improvement employing Switched-Capacitor feedback is up to 20 to 30dB [41]. For the proposed technique, the SNR improvement is up to 33dB. This is understandable if we compare their respective feedback waveforms shown in Figure 3-1. For the proposed technique, all required feedback charge is supplied before clock transitions. Whereas in the Switched-Capacitor feedback, there are still some leftover charges, the amount of which depends on the time constant [41]. Also, the proposed technique makes circuit implementation easy, renders easy synthesis of the modulator by retaining traditional SI feedback and causes mild power consumption overhead. Finally, the proposed technique has only moderate demand for performance of active elements, such as OpAmp slew rate and gain bandwidth product.

3.5 Summary

We have proposed a simple clock jitter reduction technique which employs delayed RZ DAC feedback together with the RZ time period and the active DAC feedback time period fixed by two delay elements. We verify the proposed technique on a 4th-order CIFF modulator as well as a 4th-order CIFB modulator. Simulations show that this technique is very effective to reduce independent clock jitter effects while marginally effective to independent clock jitter.

Chapter 4 Circuit and Layout Level Design

4.1 Introduction

In this chapter, the schematic and layout of a 4-th order continuous-time delta-sigma modulator with CIFF topology will be presented. For the loop filter implementation, OTA-C (Operational Transconductance Amplifier Capacitor, also called Gm-C) integrators are chosen to improve system linearity and save power and area. The remaining blocks are simple OTA for resonator, one-bit comparator, return-to-zero (RZ) logic with clock jitter reduction, simple resistor-based summing block and one-bit feedback DAC. The design of these blocks is next discussed in more details.

4.2 Circuit Parameters

The overall CIFF ΔΣM Circuit block diagram is shown in Figure 4-1. There are three types of commonly used continuous-time integrators: R-C integrator, Gm-C integrator and MOSFET-C integrators. We use Gm-C integrators with source degeneration because they show a better tradeoff between power, speed, and accuracy than RC integrators [35],[46],[49]. The integrator parameters can be derived by comparing transfer functions with the CIFF topology given in Figure 4-2 and coefficients given in Table 4-1. For example, for the first stage, the integrator transfer functions for both should be equal

$$\frac{Gm_1}{sC_1} = \frac{b_1}{sT_s} \tag{3.1}$$

Proper transconductance Gm1 and capacitor C1 values should be chosen to satisfy equation (3.1). Other integrator stage parameters can be obtained in a similar way. The local feedback OTA should be designed to satisfy

$$Gm_9 = \frac{t_{32}}{t_{12}} Gm_2 \tag{3.2}$$

The output currents of feed-forward OTA flow through the load resistor and they jointly accomplish the voltage amplification and summing function. Therefore, in the four forward gain stages Gm5 through Gm8, the product of *Gm* and *R* should be equal to the

feed-forward coefficients given in Table 4-1 (t15, t25, t35 and t45). At first, choose Gm8 same as Gm2 then find out the value of the loading resistor R. Follow the equation (3.3), we derived summing resistor R equal to 1.5K. Then the transconductance of Gm5 through Gm7 can be found use forward coefficient over summing resistor.

$$Gm_8 R = t_{15} \tag{3.3}$$

Finally, DAC current values are given by

$$I = Gm_1 \frac{a_1}{b_1}(scalar)\frac{1}{Fraction} \tag{3.4}$$

Where *Fraction* is the RZ logic fixed-width period percentage (in this design the fraction of 0.4 has been chosen). Based on these equations, final parameters are chosen as shown in Table 4-2.

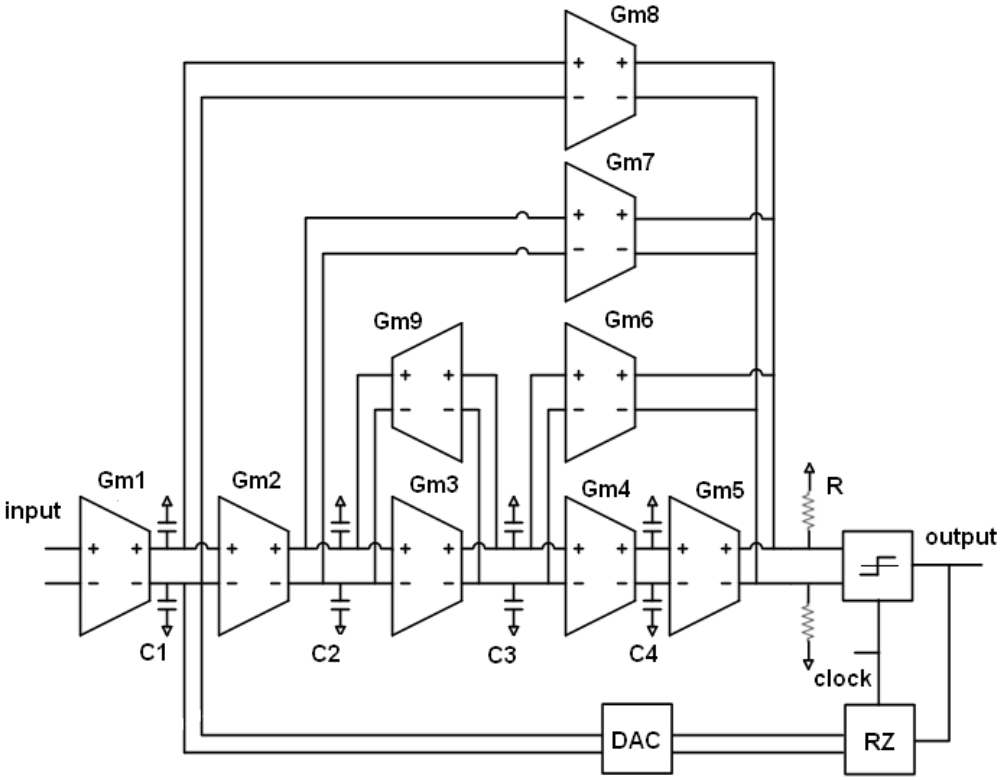

Figure 4-1 Transistor level model of ΔΣM Circuit Blocks using CIFF topology

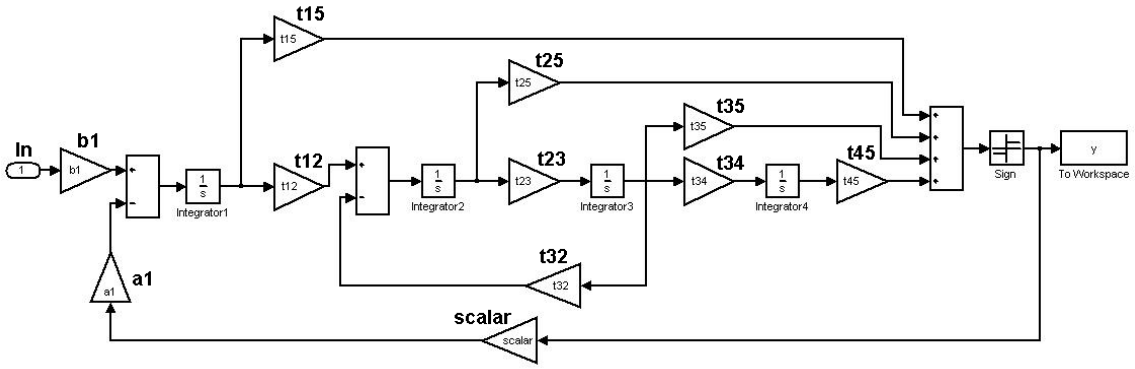

Figure 4-2 SIMULINK model of CIFF ΔΣM Topology

Table 4-1 CIFF Modulator coefficients

Coefficients	Value	Coefficients	Value
b1	0.4	t15	0.8388
t12	0.5032	t25	0.6101
t23	0.2606	t35	0.5
t34	0.0962	t45	0.6143
a1	0.4	t32	0.02
		scalar	0.634

Table 4-2 Derived component parameters

Parameters	Values	Parameters	Values	Parameters	Values
Gm1	560μS	Gm6	410uS	C1	8.5pF
Gm2	542μS	Gm7	333uS	C2	6.73pF
Gm3	542μS	Gm8	407uS	C3	13pF
Gm4	542μS	Gm9	542uS	C4	35.2pF
Gm5	21μS	I	880uA	R	1.5kΩ

4.3 Gm-C Integrator, Feed-forward OTA and Summing Block

Figure 4-3 shows the schematic of a Gm-C integrator with folded-cascode structure. Resistor-based source degeneration is used to increase the linearity of the transconductance of the input stage. The output impedance of the current transistors is increased with cascode transistors, which forces all small-signal current to flow through the degeneration resistors. When the degeneration product is much larger than one, the resistor determines the effective transconductance of the input stage which is thus

linearized due to the linearity property of the resistor [35]. Figure 4-4 shows the common-mode feedback circuit for this double differential OTA.

In the CIFF topology, the first stage is most critical, requiring high linearity as well as large currents [49],[50]. For that reason, we select a high $Gm_1 = 560uS$ for the first stage and a smaller $542uS$ for other integrator stages. Figure 4-5 shows the simulated transconductance waveform for $Gm_1 = 560uS$. For this OTA, the total harmonic distortion percentage is 12.12m% (-80dB) when the input voltage is 0.3V and the input frequency is 468.75KHz.

In the CIFF topology, the last stage before comparator is a summing block. A simple resistor-based implementation is used as shown in Figure 4-1. The transconductance of these feed-forward OTAs and the resistor value given in Table 4-2 are chosen to match the feed-forward coefficients shown in Table 4-1. Here the resistor is chose to be 1.5kΩ. Those OTAs also use the same architecture with those integrators as shown in Fig. 4-3.

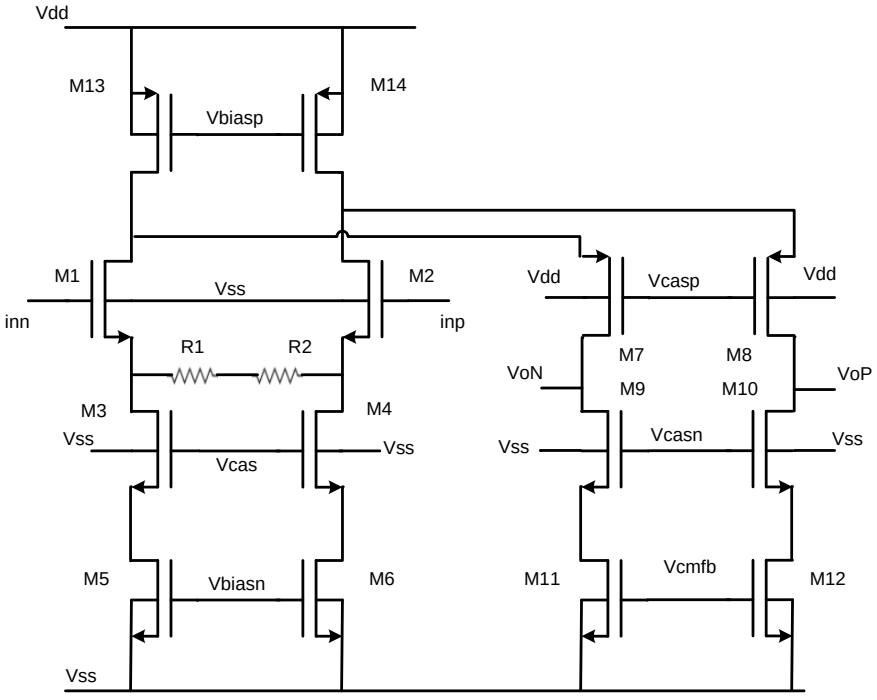

Figure 4-3 Resistor-based source-degeneration OTA

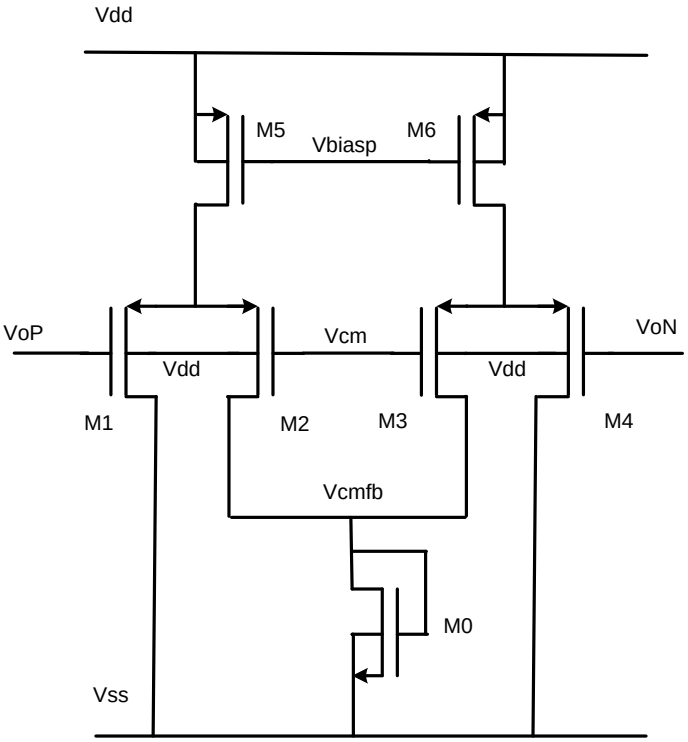

Figure 4-4 Common-mode Feedback circuit for resistor-based source-degeneration OTA

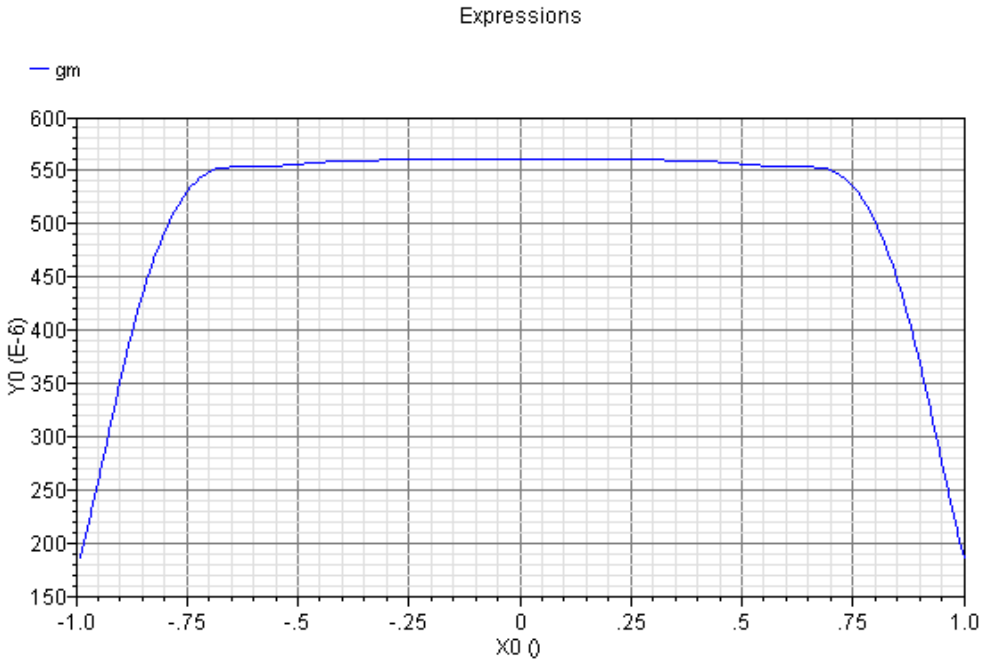

Figure 4-5 First integrator with Gm=560uS

4.4 Transistor-Only Simple OTA

Compared with the first stage OTA used in Gm-C integrators, the local feedback has a more relaxed requirement on the linearity [46],[49]. Therefore a transistor-only simple OTA is used. Its schematic is shown in Figure 4-6 and its transconductance waveform is shown in Figure 4-7.

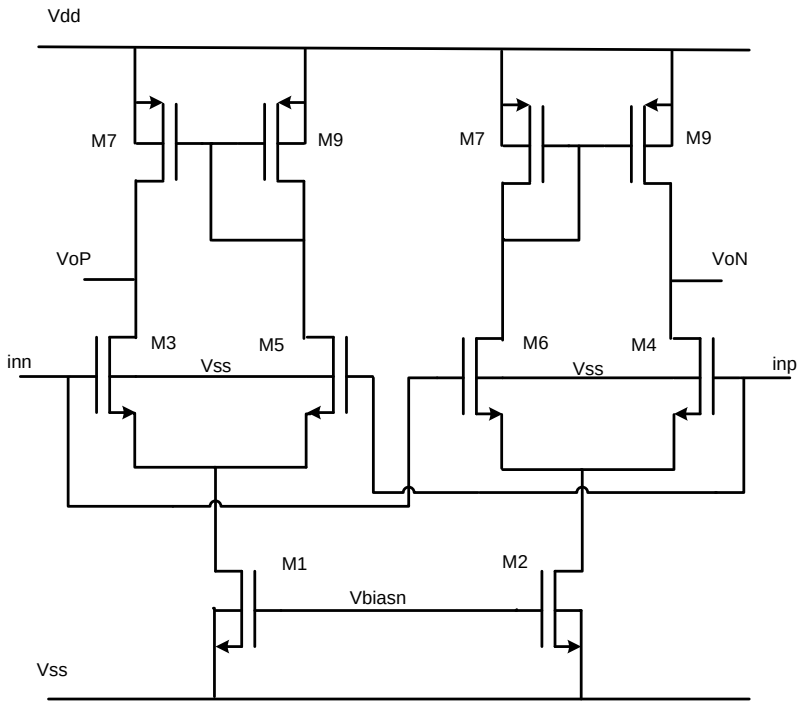

Figure 4-6 Transistor-only simple OTA

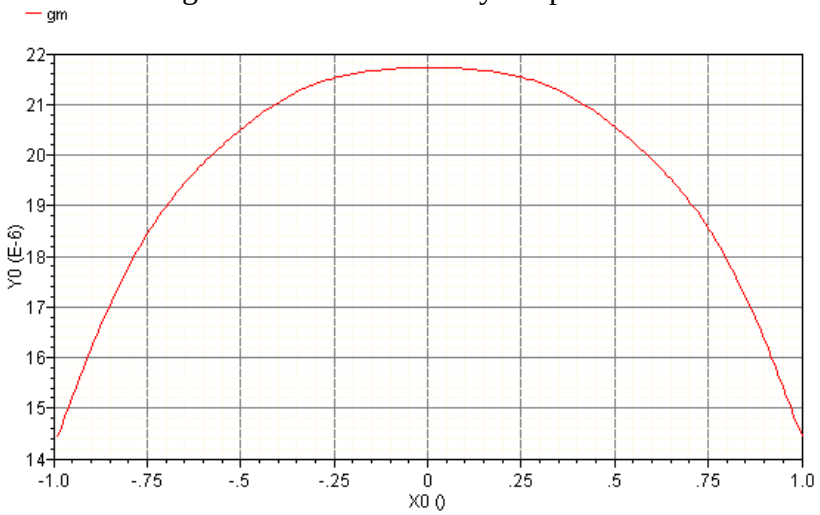

Figure 4-7 Transistor-only simple OTA waveform

4.5 One-Bit Comparator

A typical one-bit comparator consists of preamplifier and a SR-latch as shown in Figure 4-8. The circuit schematic is shown in Figure 4-9. The load for the preamplifier is a PMOS latch, which uses positive feedback to provide a faster switching time [46],[49]. When the clock signal switches from low to high, the preamplifier outputs quickly rise to low or high due to positive feedback and the stabilized preamplifier outputs are fed to the SR-latch and being stored there. When the clock signal goes low, the preamplifier outputs are always high and the S-R latch keeps its states. Figure 4-10 shows the comparator response. By zooming in the switching period as in Figure 4-11, we can see that the comparator delays for all inputs are less than 250ps, which is very small.

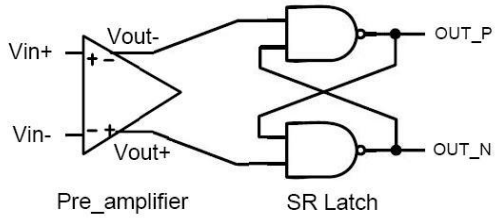

Figure 4-8 SR Latched comparator block diagram

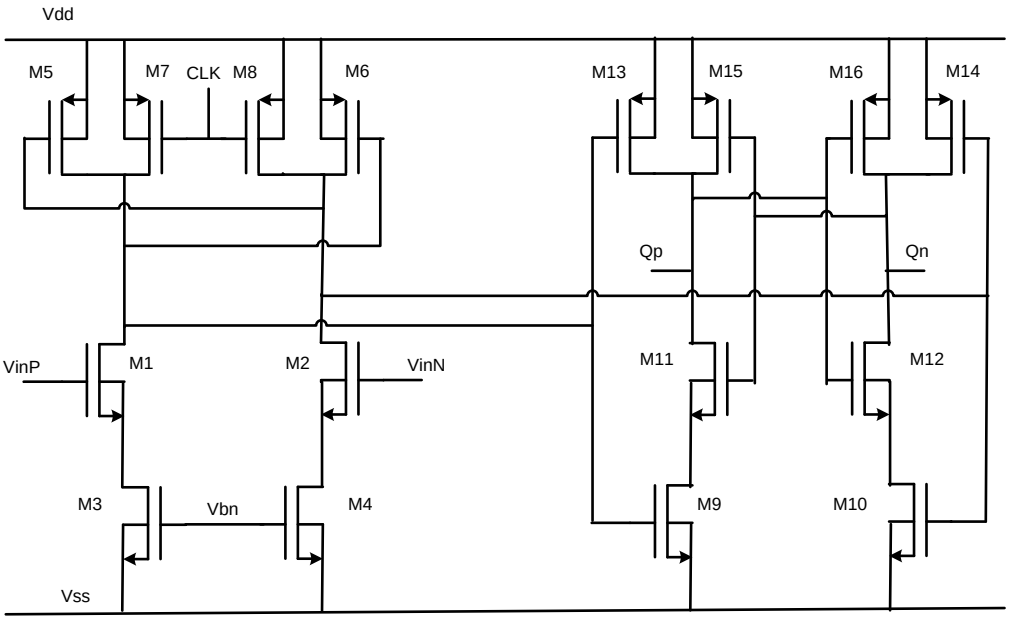

Figure 4-9 SR Latched comparator circuit

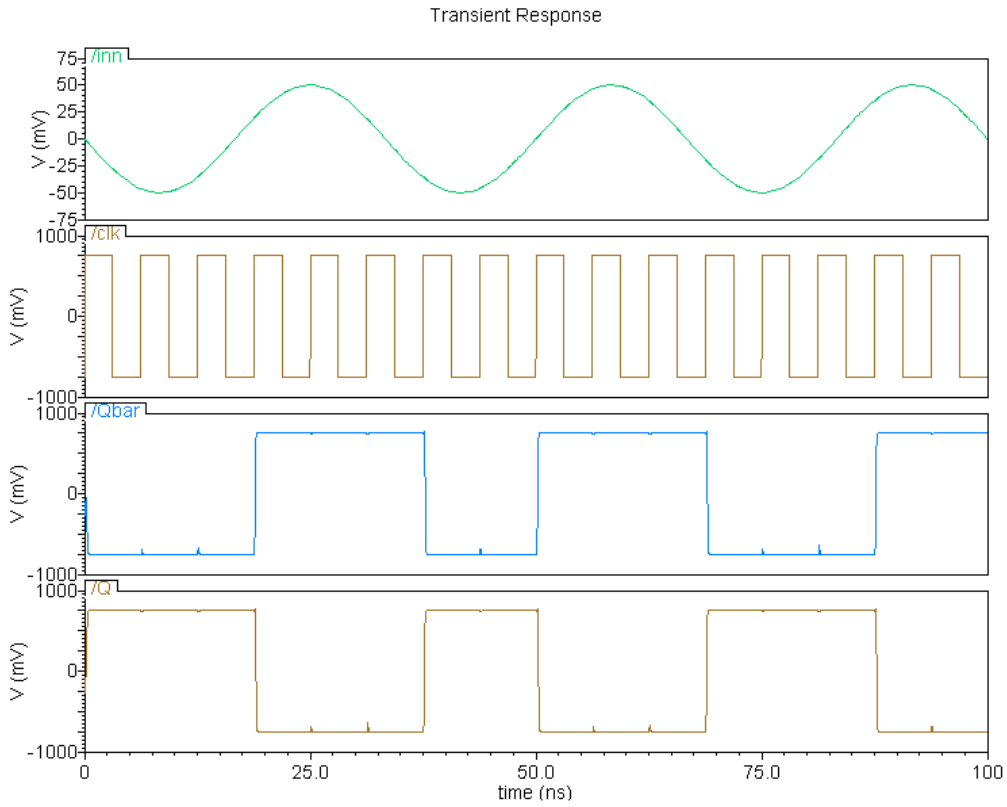

Figure 4-10 SR Latched comparator output waveform

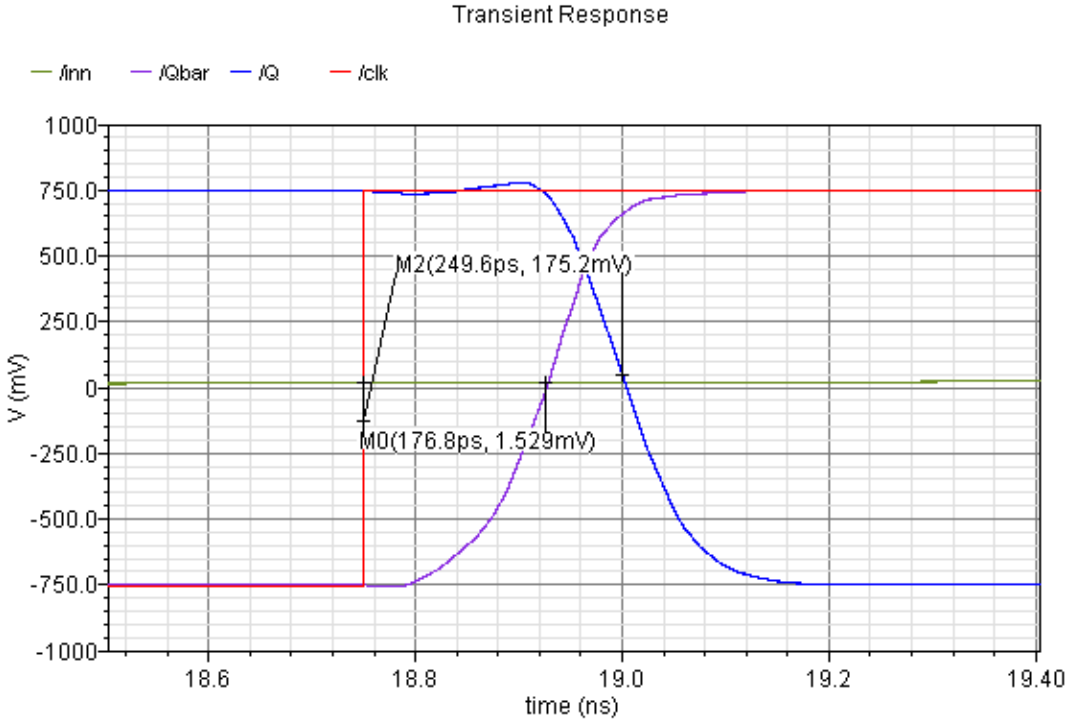

Figure 4-11 SR Latched Comparator output waveform timing

4.6 Return-to-Zero Logic with Clock Jitter Reduction

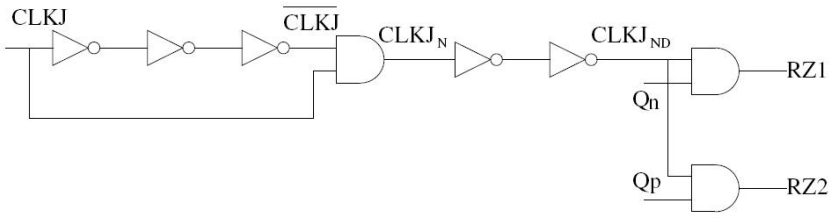

Figure 4-12 Return-to-Zero Logic block diagram

As we have shown in Chapter 3, a delayed return-to-zero logic with fixed-width square wave circuit can effectively reduce the clock jitter effect. The logic is shown in Fig 4-12. Chains of inverters are carefully designed to control delays to generate the correct delayed RZ logic with a fixed-width of 0.4Ts, and this RZ signal is used further to control the DAC feedback elements. Figure 4-13 shows the circuit simulation results.

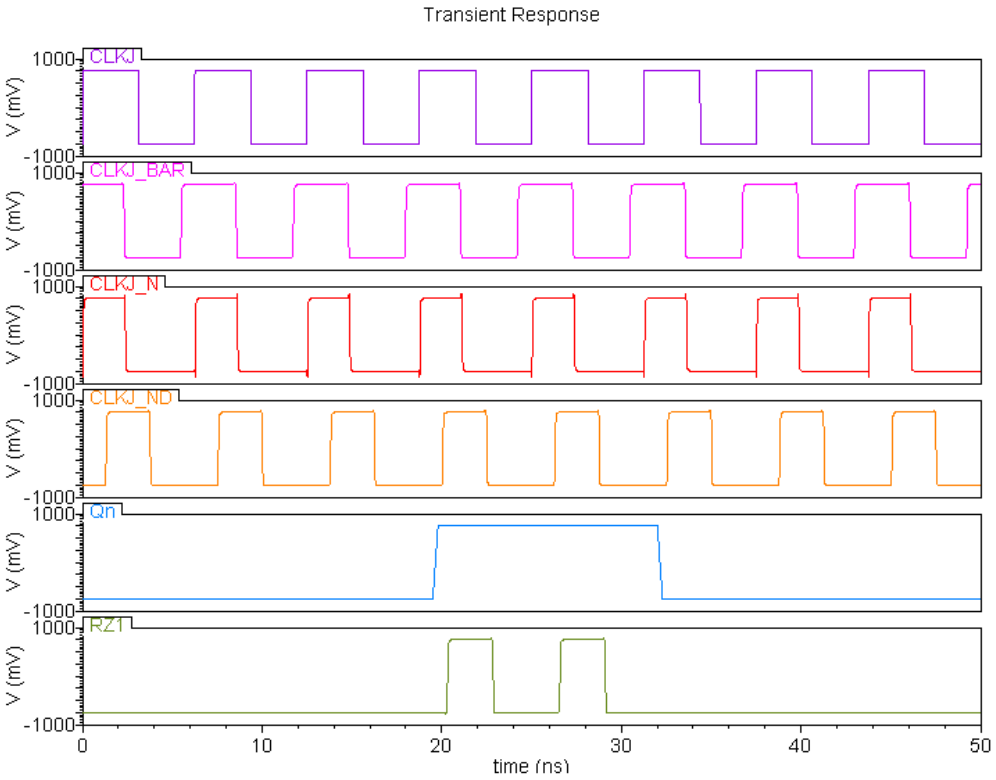

Figure 4-13 Return-to-Zero logic waveform

4.7 DAC Feedback

For the DAC, a NMOS current source is chosen. The schematic is shown in Figure 4-14. Cascode transistors are used to improve the output impedance [46] and small PMOS capacitors were attached to the branches which help compensate the errors or switching current spikes [22]. Figure 4-15 shows the output waveform of the DAC feedback circuit.

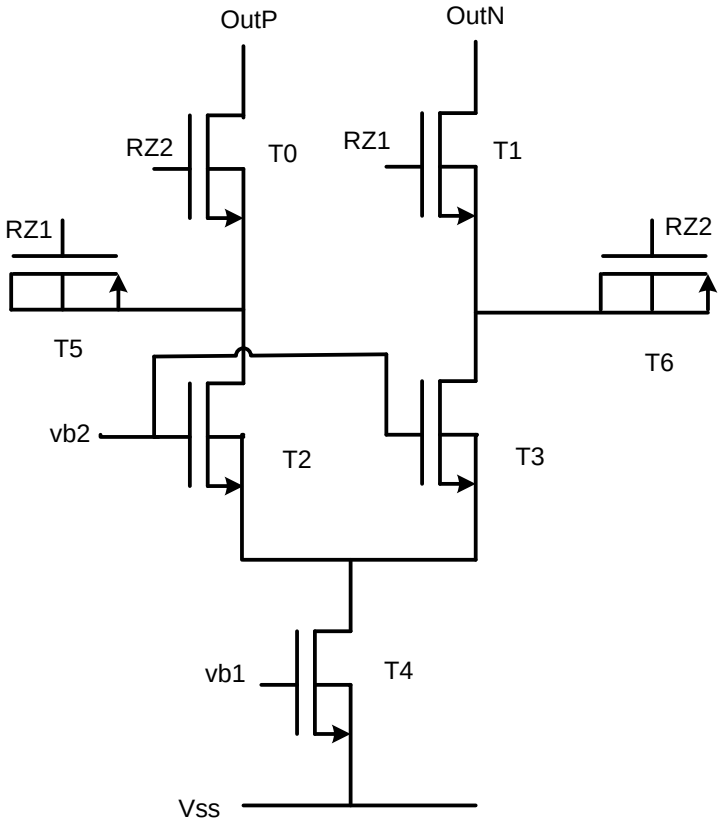

Figure 4-14 DAC feedback block circuit

4.8 Summary

In this chapter, we discussed all building blocks for a CT ΔΣM. All circuits are designed and simulated using Cadence software and IBM 130nm CMOS process. The power supply is set to be 1.5V. Cadence simulations show that this circuit can achieve a SNR of

65.5dB for a 0.1V input at 468.75kHz. Figure 4-16 shows the chip layout, which has an area of 0.79mm by 0.79mm.

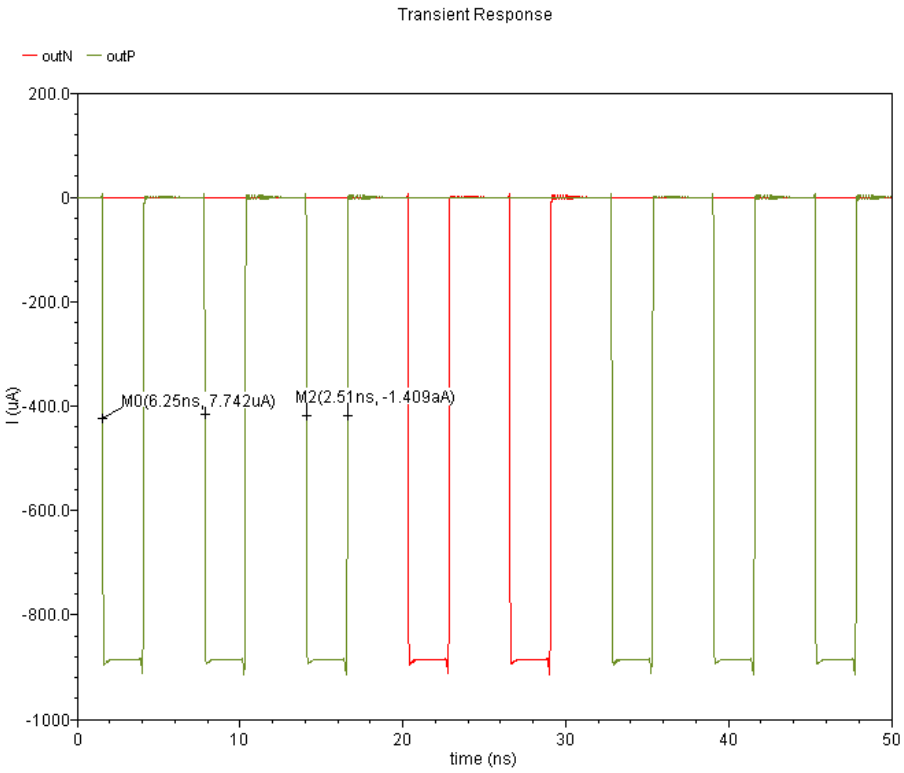

Figure 4-15 DAC feedback waveform

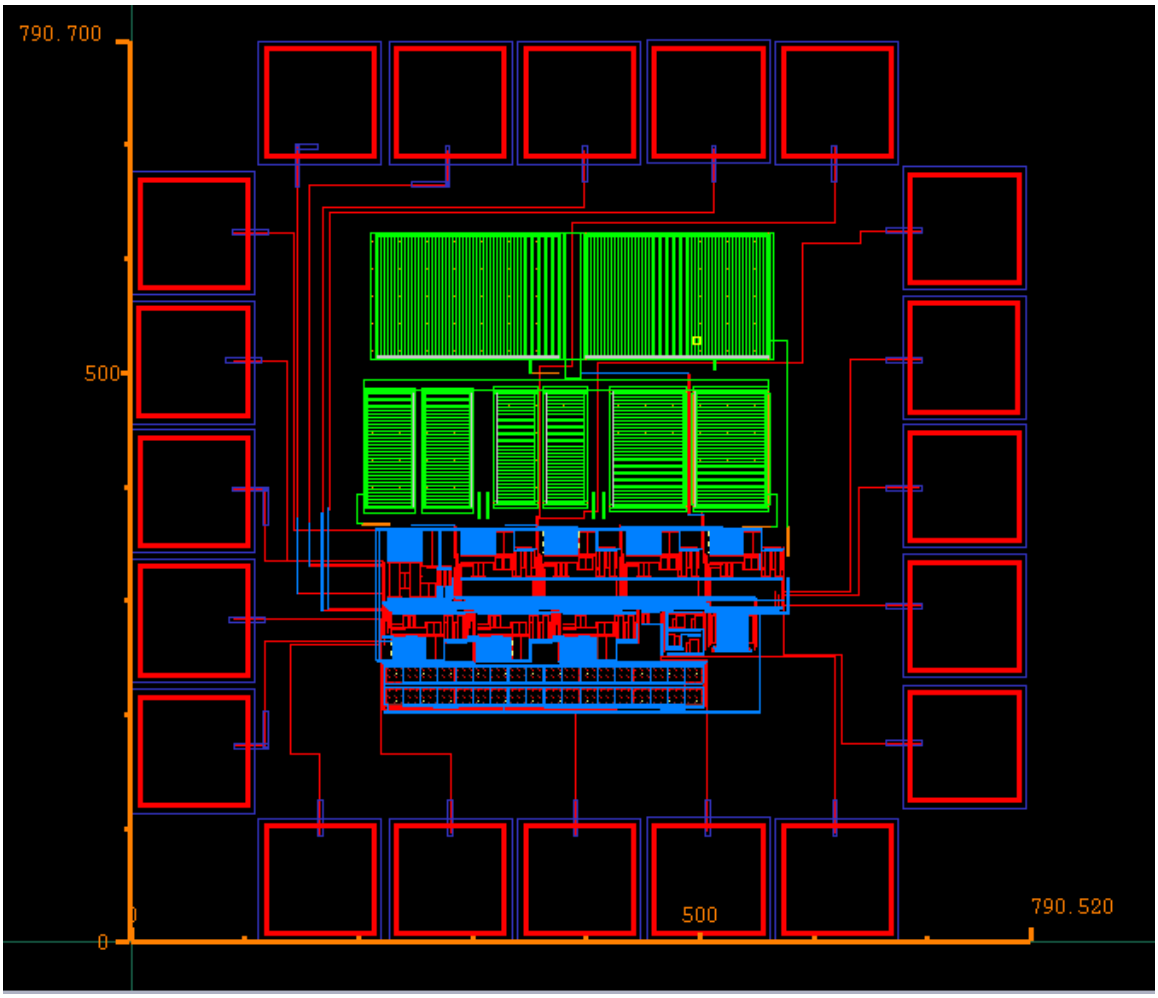

Figure 4-16 Circuit layout of the 4th-order CT-Δ∑M

Chapter 5 Conclusion and Future Work

5.1 Summary

Delta-sigma modulators exploit oversampling and noise shaping to achieve high-performance ADCs. Continuous-Time Delta-sigma modulators have the benefits of high-speed and low-power but suffers from clock jitter effects. In this thesis, we have investigated various critical design issues in CT-Δ∑M through both system-level and circuit-level simulations. Further, we presented a simple but effective clock jitter reduction technique using delayed RZ and fixed SI feedback, which was verified by both system-level and circuit-level simulations. Finally, we presented a circuit design of a single-stage 4th-order CT-Δ∑M with 1-bit quantizer and OSR 40 using the IBM 0.13um CMOS process.

5.2 Future Works

We can extend the work in this thesis in several ways. First, for the system-level simulations, the MATLAB/SIMULINK can be extended to include multi-stage multi-bit CT-Δ∑Ms. Second, the presented jitter reduction technique does not address accumulated clock jitter very well and new techniques should be developed. Finally, the performance of the designed CT-Δ∑M circuit can be further improved through optimizing the integrator, DAC and comparator blocks. Since the first-stage is most critical, an OpAmp based integrator may result in better performance.

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