Advanced Architectures for Next Generation Wireless Integrated Circuits

---

A DISSERTATION

SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL

OF THE UNIVERSITY OF MINNESOTA

BY

Liuchun Cai

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

Professor Ramesh Harjani, Advisor

May 2009

Acknowledgments

First of all, I wish to thank my advisor, Professor Ramesh Harjani, for his continued encouragement and guidance throughout my Ph.D. study at the University of Minnesota. His enthusiasm inspires me to explore the challenging and the interesting world of the circuit design. It has been a great honor to have Prof. Ramesh Harjani as my advisor. I would also like to thank Professor Anand Gopinath, Professor Chris Kim, and Professor Bruce Hammer for their support as members of my Ph.D. committee. Their comments and suggestions helped me improve my thesis.

I would like to acknowledge the significant sacrifice of my wife Yanxia, daughter Maggie and son Victor during my many years of academic pursuit. I would like to give special thanks to my parents and parents-in law for their love, encouragement and constant support to continue my studies because without them this work would not have been possible.

I feel privileged to work in the Analog Group, an amicable and exciting research environment. I am grateful to all the group members(current and previous) for their dedication and hard work, which in many ways have helped in my research works.

I also would like to thank: Dale Swanson, Chimai and Carlos for their technical support during both my teaching and research; I would like to thank the staff in machine shop for their kind and expedient immediate help.

My thanks also go to Jian Xu from Intel Inc., Xiaoyong Li from Qualcomm Inc., Hosaeng, Pongstorn, Hushrav and Aaron in ECE department at UMN. Additionally, I would like to thank my friends at this University and elsewhere for their assistance and encouragement to continue my studies.

Finally, I would like to thank the Electrical and Computer Engineering department to provide me with this opportunity to study at the University of Minnesota, Twin Cities.

Abstract

In this thesis, we present and discuss two advanced architectures of wireless integrated circuits.

In the first part of this thesis we will focus on the design of a inductorless receiver, which include a LNA, mixer and frequency synthesizer. Inductors are used in RF design to extend the bandwidth by resonating out the load and/or parasitic capacitance. However, on-chip inductors are large and cannot be ported easily from one process to the next. Due to modern CMOS scaling, inductorless RF design is rapidly becoming possible. In this thesis we describe a new methodology for designing the RF frontends necessary for the wideband 1GHz-10GHz bandwidth in a 0.13μm CMOS technology. To validate our design methodology two receiver RF frontends were designed; a traditional inductor based design and an inductorless design. A common-gate LNA transconductor is followed by a capacitive peaking LNA-mixer pair (CPLM). Measurement results indicate that CPLM with the same bandwidth has better linearity, comparable noise figure and uses only 17% more power. The silicon area for the CPLM is only 22% of the IPLM. Both designs can be mated with an inductorless, ring-oscillator based, wide lock range and low power PLL also shown in this thesis.

We present theory and prototype results for injection-locked frequency dividers based on differential ring oscillators (D-ILFD) and single-ended ring oscillators (S-ILFD), which can be locked to all harmonics (i.e., *even* and *odd*). We have developed a general theory for lock range and phase noise for all harmonics for both topologies. Measurement results for the D-ILFD and the S-ILFD show that the lock range decreases with increasing harmonics at the low harmonics while leveling off for larger division ratios. Measured integrated phase noise for D-ILFD and S-ILFD also show that the integrated phase noise decreases with increasing harmonics. The measure-

ment results corroborate our theory. Ring oscillator based D-ILFDs and S-ILFDs are compact and consume low power making them well suited for wideband low power PLLs.

We exploit the ring VCO based on an updated Maneatis delay cell with self-boosted biased techniques, which has a ultra wide tuning range of 1 GHz to 10.3GHz. The injection-locked frequency divider (ILFD), which can lock to all harmonics, has been used. A wide lock range, low power PLL based ring VCO and ILFD has been designed for UWB radio. Experimental results indicate that integrated phase noise is below a 3^0 and power consumption is only 8.1 mA to 21.85 mA for the entire frequency bands.

In the second part of this thesis, we focus on noise isolation for mixed-signal (RF/analog/digital) design in CMOS 3D ICs. Faraday cages have traditionally been used to provide isolation from electromagnetic fields. In this thesis, we describe the use of Faraday cages for reducing crosstalk in 3D ICs. We validate our methodology with a combination of simulation and measurements from fabricated prototype designs. Measurement and simulation results show that the crosstalk between the transmitter and receiver reduces by about 75dB up to 10GHz by using a Faraday cage in combination with tier-to-tier isolation, which is one of best performance reported so far. Measurement results indicate that the Faraday cages have no effect on the S-parameters and linearity of inductorless RF circuits. We further develop a lumped equivalent model for crosstalk with and without a Faraday cage. There is good agreement between measurement, 3D electromagnetic simulation and lumped circuit simulation.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Introduction

In the past decade silicon-based RF and microwave technology has had a dramatic impact on the world of wireless technology. Wireless communication has experienced a global boom because it enables easier communication among individuals. Today we can access data and entertainment in virtually every corner of the globe, from short range bluetooth and WiFi networks, to cellular and stelelite networks, to meet different range and throughput requirements.

The current exponential growth of the wireless market requires wireless transceivers with ever increasing bandwidth, better quality, lower cost, and longer battery life. To get the required RF performance out of standard digital CMOS technologies, new system architectures and circuits topologies need to be developed.

Wideband radio receivers are of interest for a variety of application, including

the MBOA-UWB standard, multi-band cellular and software-defined radios. The operational frequency of wireless designs has traditionally been extended by utilizing bandpass resonant circuits or with broadband transmission line circuits. Both on-chip inductors and integrated transmission lines tend to consume significant chip area and increase design complexity. Additionally, the increased number of radio protocols used in modern handsets places added pressure on silicon real estate [5]. However, as device technologies and their associated cutoff frequencies (f_Ts) have increased, it is rapidly becoming possible to design circuits without large on-chip inductors or area consuming transmission lines. In particular, deep submicron CMOS devices have F_Ts in the 100+GHz range, shown in Fig 1.1 [1], i.e, parasitic device capacitances are very small such that we can potentially replace active bandpass RLC circuits with active lowpass RC circuits.

Fig 1.2 shows an example modern wireless transceiver architecture. All circuits prior to and including the up and down conversion mixers typically utilize inductors (e.g., LNA, PA, RX mixer, TX mixer and PLL). Circuits after the frequency translation step (i.e, IF and baseband) are already possible to realize using lowpass RC circuits. So, we shall focus on the RF frontend circuits. In particular, we shall focus on circuit designs for the RF frontend that operates between 1GHz-10GHz for the wideband standard. CMOS wideband RF frontend circuits are particularly interesting as they have traditionally been designed using multiple inductors [6, 7]. In the first part of this thesis we will focus on the design of a inductorless receiver, which include LNA, Mixer and frequency synthesizer.

Recently, another emerging technology, called three dimensional integrated cir-

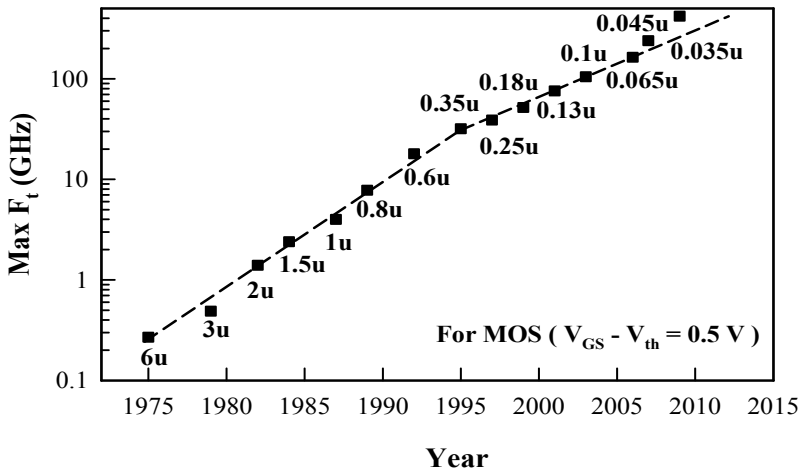


Figure 1.1: $MOSFET$ maximum F_T evolution versus time [1]

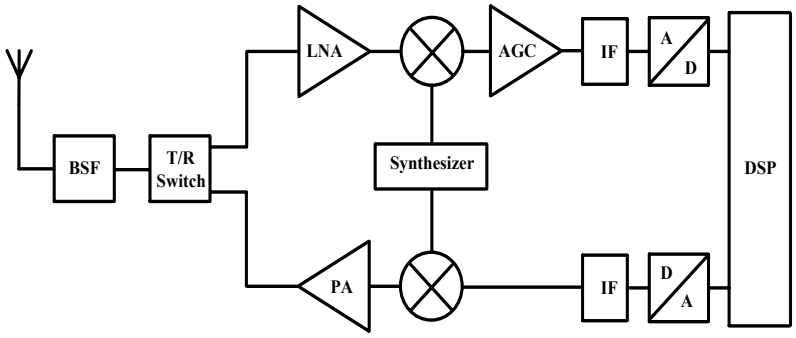


Figure 1.2: Example low-IF or Zero-IF transceiver architecture

cuit(3D ICs)is a promising to be a high density integrated circuit fabrication technology. 3D ICs provide an attractive alternative to traditional two dimensional integrated circuits (2D ICs). In the case of homogenous integration (i.e., same technology), they provide increased computational power with reduced wiring and additionally, provide the possibility of heterogenous integration (i.e., different technologies) that may be more suitable for RF and mixed-signal circuits.

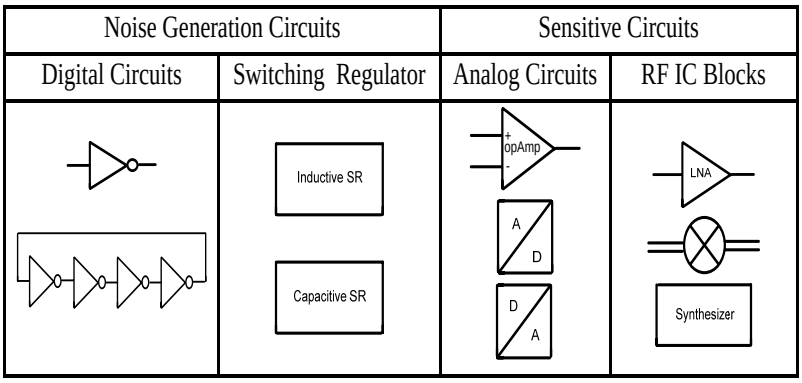


Figure 1.3: Typical noise generators and sensitive circuits in mixed-signal ICs

In the second part of this thesis, we will focus on mixed-signal (RF/analog/digital) design in CMOS 3D ICs. Such 3D ICs allow for the integration of full systems that include RF circuits with significant digital signal processing capability. However, for such integration to be feasible it is critical to provide sufficient isolation between the sensitive analog/RF circuits and the digital circuits. Noise injected by digital circuits into the substrate can severely degrade the performance of RF/analog circuits,as illustrated in Fig 1.3.

In this thesis, we evaluate the noise coupling problem for mixed digital-RF circuits and propose techniques to reduce this problem. In particular, we evaluate the efficacy of using separate tiers for digital and analog/RF circuits and the use of Faraday cages to shield sensitive circuit blocks. Verification is done using a combination of EM simulation and measurements from fabricated test structures on the 0.18μm fully-depleted silicon-on-insulator (FDSOI) technology [2] shown in Fig 1.4.

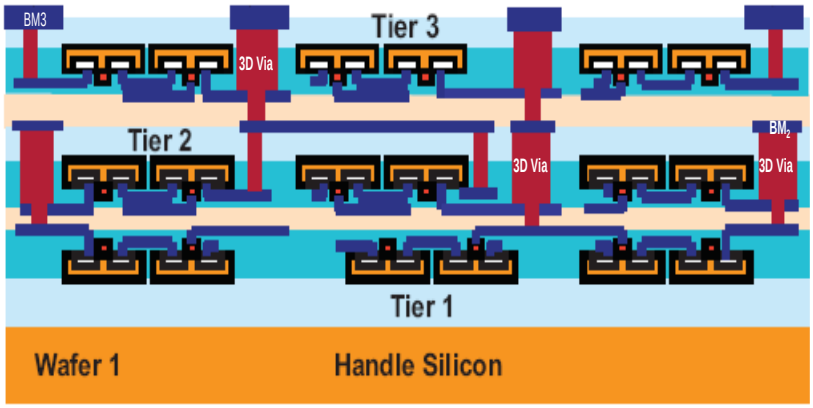


Figure 1.4: The 3-tier 3D IC cross-section used for prototype designs [2]

1.2 Overview

This thesis is organized as follows. In Chapter 2, two receiver RF frontends designs are presented and compared: a traditional inductor peaking LNA and mixer and a capacitive peaking LNA and mixer circuit. Power gain, linearity, noise figure and silicon area of measurement results are discussed.

Theory and prototype results for injection-locked frequency dividers based on differential ring oscillators (D-ILFD) and single-ended ring oscillators (S-ILFD) are introduced in Chapter 3. The measured integrated phase noise and lock range for D-ILFD and S-ILFD are addressed.

Chapter 4 introduces a wide lock range, low power PLL based ring VCO and ILFD for UWB radio. The ring VCO is based on the updated Maneatis delay cell with self-boosted biased techniques. The design of each block for PLL are discussed in details.

Chapter 5 describes the use of Faraday cages for reducing crosstalk in 3D ICs. Our

methodology with a combination of simulation and measurements from fabricated prototype designs have been validated. A lumped equivalent model for crosstalk with and without a Faraday cage have been developed.

Finally, Chapter 6 concludes with a summary of the contributions of this thesis.

Chapter 2

Low Noise Amplifier and Mixer

2.1 Introduction

Wideband LNA designs usually use inductor degenerated transconductor with LC ladder input matching networks to achieve wideband impedance matching [6]. Inductive peaking techniques are used to extend the bandwidth at the output of the LNA. The large number of inductors required in these circuit designs increases cost [7]. Recently a resistive feedback LNA without inductors based on a current-reuse transconductance-boosting technique for wideband have been reported in a 90 nm technology [8].

The LNA is often directly followed by a down conversion mixer whose input bandwidth also needs to be wide. The extended bandwidth requirement for a wideband mixer in [9] was achieved by using a LC ladder network for wideband impedance matching. Alternately, the bandwidth extension was achieved by using a distributed

mixer in [10]. All these designs consume large area due to the use of on-chip inductors and distributed structures.

Traditionally, the design of each block is performed separately and matched to the I/O impedances, In this thesis we develop a new circuit architecture and design methodology to optimize the LNA and mixer together [11]. The design and implementation of LNAs and mixers in a 0.13 μm CMOS technology for the receiver path of wideband system will be discussed.

Wideband inductorless CMOS front-ends have appeared recently in [12–14]. However, these designs have covered only a small fraction of the total UWB spectrum from 3.1GHz to 10.6GHz. In this thesis we will present the design of an inductorless wideband front-end that operates from 1G to 10GHz. A mathematical treatment of new methodology, which will be useful as a guide in future design efforts, Circuit designs with corroborating measurement results for RF frontend consisting of an LNA, mixer are displayed in this chapter.

This chapter is organized as follows: In the next section we theoretically analyze the new circuits, this is followed by details for the LNA and mixer pair in the following section. Section 2.4 provides experimental measurement results and Section 2.5 provides some conclusions.

2.2 New Circuit Design Methodology

Before delving into the overall frontend design let us consider the circuits shown in Fig 2.1. At this time let us assume that the LNA and the rest of the IF can be

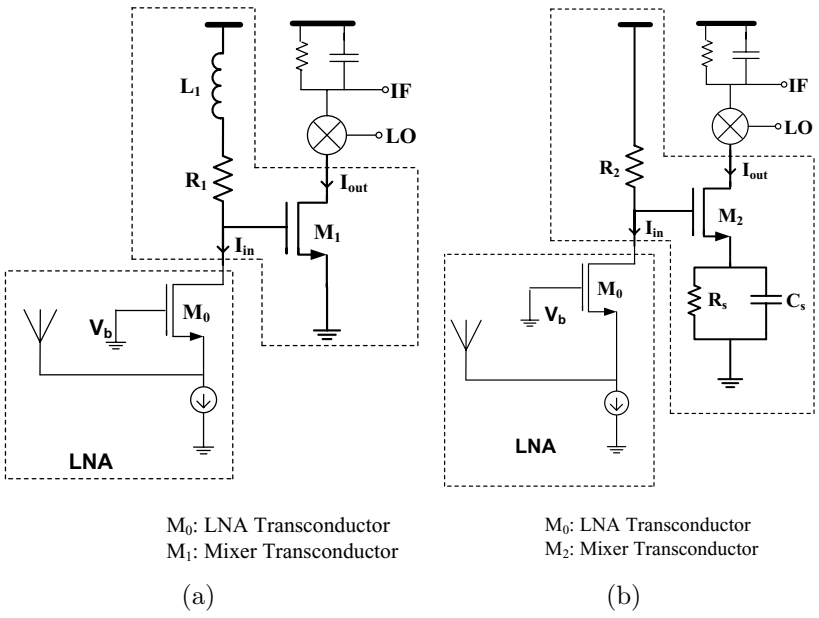


Figure 2.1: Simplified circuits for inductive and capacitive peaking (a) inductive peaking and (b) capacitive peaking

realized without inductors. Fig. 2.1(a) shows a simplified interface between the LNA and mixer. Biasing and AC coupling capacitors have been omitted for clarity. In this figure M_0 represents the LNA transconductor, which may be realized as a common-gate or a common-source device. Further, M_1 represents the RF transconductor of the mixer. To bound our discussion, let us focus on the interface circuits shown within the dashed lines. The circuit in Fig. 2.1(a) shows the use of conventional inductive peaking to extend the bandwidth at the LNA output (It is really the LNA-mixer interface bandwidth that is being extended.). This bandwidth extension occurs due to the addition of a zero in the transfer function due to the inductor. A zero can also be introduced by capacitive degeneration as shown in Fig. 2.1(b) [15]. In this circuit, the RC combination of C_s and R_S provides a zero that extends the

high frequency response. Effectively, capacitive degeneration provides bandwidth extension properties similar to inductive peaking [7]. In the next few sub-sections we provide detailed comparisons between the two bandwidth extension techniques in terms of gain, noise, and linearity.

2.2.1 Gain analysis

To understand the overall gain of the RF frontend let us focus on the current gain, (I_{out}/I_{in}) from the output of the LNA transconductor to the drain of the mixer transconductor, as shown in Fig 2.1. The current gain for the inductive peaking circuit shown in Fig. 2.1(a) is given by (2.1). While the current gain for the capacitive degeneration circuit shown in Fig. 2.1(b) is given by (2.2), where C_{gs} is the gate-source capacitance of the mixer RF transistor (M_1or M_2), and g_m is their transconductance.

$$A_{i\,L} = \frac{I_{out}}{I_{in}} = \frac{g_{m1}R_1\left(\frac{s\,L_1}{R_1}+1\right)}{s^2 L_1 C_{gs1} + s\,R_1 C_{gs1} + 1} \tag{2.1}$$

$$A_{i\,C} = \frac{\frac{g_{m2}R_2}{1+g_{m2}R_s}(s\,R_s C_s + 1)}{s^2\frac{R_s C_s R_2}{1+g_{m2}R_s} + s\frac{C_{gs2}R_s + R_s C_s + C_{gs2}R_2}{1+g_{m2}R_s} + 1} \tag{2.2}$$

Both circuits have one zero and two poles. The voltage gain for the overall RF frontend is given by the product of the LNA transconductance, the current gain calculated in the previous equations, the mixer load resistance and the mixer commutation gain (ideally $2/\pi$). In turn the power gain can be derived by also considering the input and output impedances.

2.2.2 Noise analysis

Let us now consider the noise figure (NF) for the inductive peaking interfaces shown in Fig. 2.1. The overall NF can be derived using traditional Friis equations [15]. In this analysis the overlap capacitance C_{gd} has also been neglected for simplicity. The NF for inductive peaking is given by (2.3), where γ is the short channel noise factor, α is the short channel transconductance reduction factor and ω_T is the cutoff frequency of the device.

$$NF_L = 1 + \frac{\gamma}{\alpha}\frac{\omega^2}{\omega_T} C_{gs1} R_1 \left| 1 + \frac{s\, L_1}{R_1} \right|^2 \tag{2.3}$$

The NF for capacitive peaking can be computed by using the noise figure definition in [16], where N_0 (eqn (2.5)) is the noise power of R_2, N_d (eqn (2.6)) is the channel thermal noise power of M_2, and N_s (eqn (2.7)) is the noise power of the degeneration resistor R_s, all referred to the output.

$$NF = \frac{\text{Total output noise}}{\text{Output noise due to the source}} = 1 + \frac{N_s + N_d}{N_0} \tag{2.4}$$

$$N_0 = \left| \frac{g_{m2}(s^2 \frac{R_2 R_s C_{gs2} C_s - C_{gs2}^2 R_s}{g_{m2}^2 R_s} + s\,\frac{R_2 C_{gs2}}{R_s g_{m2}} + 1)}{(s^2 \frac{R_2 R_s C_{gs2} C_s}{g_{m2}} + s\,\frac{R_2 C_{gs2} + R_s C_{gs2}}{g_{m2} R_s} + 1)(1 + s\, R_2 C_{gs2})} \right|^2 (4kT_0 R_2) \tag{2.5}$$

$$N_d = \left| \frac{1}{(\frac{g_{m2}}{1 + s\, C_{gs2} R_2}) - \frac{(1 + s\, R_s C_s)}{R_s} - \frac{1}{R_2 + s\, C_{gs2}}} \frac{g_{m2}}{(1 + s\, R_2 C_{gs2})} - 1 \right|^2 (4k_0 T_0 \gamma \frac{g_{m2}}{\alpha}) \tag{2.6}$$

$$N_s = \left| \frac{g_{m2}}{\frac{s\, C_{gs2} - 1}{s\, R_2 C_{gs2} + 1} + s\, C_{gs2} + \frac{1}{R_s}} \frac{1}{(1 + s\, C_{gs2} R_2) R_s} \right|^2 (4kT_0 R_s) \tag{2.7}$$

2.2.3 Linearity analysis

Short channel MOSFET vertical field mobility degradation and velocity saturation can be captured using the form in (2.8).

$$I_{ds} = \left[\frac{1}{2}\frac{W}{L}\mu_n C_{ox}\right]\frac{V_{ov}^2}{1+\alpha V_{ov}} \tag{2.8}$$

where α is a short channel effective mobility degradation factor. The IIP3 for the two circuits can be derived by evaluating the power series expansion for (2.8) [16]. We use the power series due to the limited Qs of our circuits [17]. The IIP3 for inductive peaking is given by (2.9), while that for capacitive peaking is given by (2.10).

$$IIP3_L^2 = \frac{4 \mid 2V_{ov} + \alpha V_{ov}^2 \mid}{3\alpha} \tag{2.9}$$

$$IIP3_C^2 = \left|\frac{8I^{(1)}}{I^{(3)}}\right| \tag{2.10}$$

$$I^{(1)} = \frac{2KV_{ov} - \alpha I}{1+\alpha V_{ov} - \alpha I R_s + 2R_s K V_{ov}} \tag{2.11}$$

$$I^{(2)} = \frac{2K - 2(2KR_s+\alpha)I^{(1)} + (2\alpha R_s + \alpha R_s^2 K)(I^{(1)})^2}{1+\alpha V_{ov} - \alpha I R_s + 2R_s K V_{ov}} \tag{2.12}$$

$$I^{(3)} = \frac{3(2\alpha R_s + \alpha R_s^2 K)I^{(2)}I^{(1)} - 3(2R_s K + \alpha)I^{(2)}}{1+\alpha V_{ov} - \alpha I R_s + 2R_s K V_{ov}} \tag{2.13}$$

where $I^{(1)}$, $I^{(2)}$ and $I^{(3)}$ are the first, second and third order derivatives of the saturation current shown in (2.8).

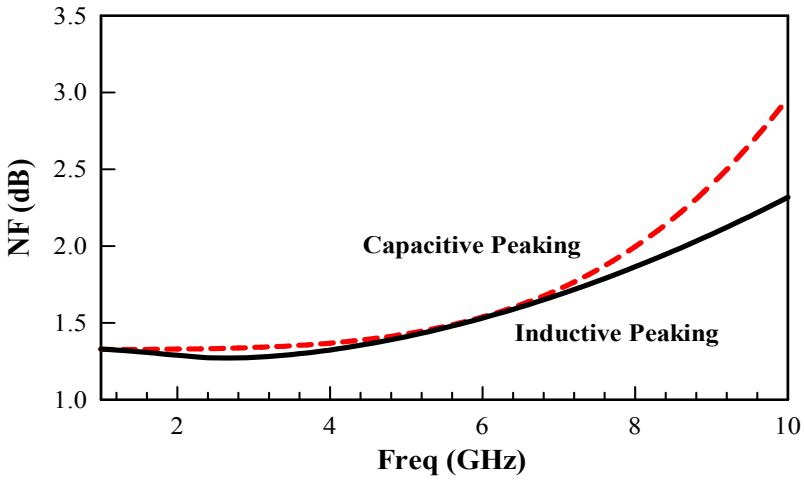


Figure 2.2: Numerical noise figure calculations for inductive and capacitive peaking

2.2.4 Graphical analysis

The equations above are quite complex and more insight is provided by graphically plotting the various terms. Detailed BSIM3V3 MOS model parameters for a $0.13\mu m$ CMOS process were used in MathCAD for these plots . We maintain the same total gain and bandwidth (1GHz-10GHz) for the inductive and capacitive peaking topologies. Because of the negative feedback associated with capacitive feedback maintaining the same gain requires higher power; the power was increased from 5.4mW to 6.3mW, i.e., an increase of 16.7%. Fig. 2.2 shows the NF for the two circuits as a function of frequency. It is clear that the noise figures are comparable with each other. This is not surprising that though we have added more components the negative degeneration does not allow all the noise to be input referred [18]. The IIP3, the first and the third derivatives of I_{ds} as a function of MOSFET width (M_1 or M_2) are displayed in Fig. 2.3. Due to the negative feedback, the IIP3 for capacitive peaking

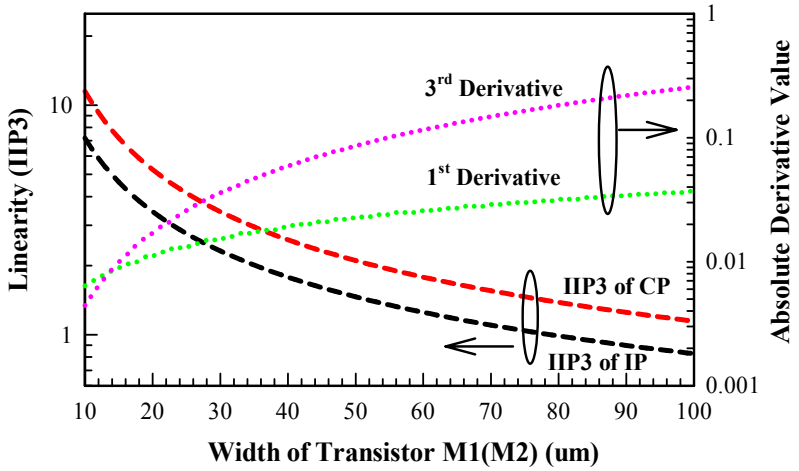


Figure 2.3: Numerical linearity calculations for inductive and capacitive peaking

is higher than that for inductive peaking.

2.3 RF Frontend Circuit Design

The analysis of the previous section is now used in designing both the LNA and mixer together. It provides insight into the choice of the appropriate blocks for LNA and mixer to build new technology methodology.

From inductive peaking and capacitive peaking shown in Fig. 2.1, the current sources can be chosen as LNAs, and M_1(and M_2) can be chosen as mixers. So, a new concept of inductive peaking LNA and mixer (IPLM) and capacitive peaking LNA and mixer (CPLM) are formed. To understand the implication of this new concept, we first discuss circuit design issues for the LNA and mixer separately.

2.3.1 Low Noise Amplifier (LNA)

The LNA design involves tradeoffs between noise figure, linearity, input matching and power dissipation. The basic common-source (CS) and common-gate (CG) LNA circuits are widely used. CS LNA is currently popular because of its superior noise and gain. One solution expanded the use of an inductively degenerated CS amplifier, a technique widely used in narrow-band designs by embedding the input network of the amplifying device in a multsetion reactive network so that the overall input reactance is resonated over a wide bandwidth [6]. Obviously, inductors consume main chip area. In contrast, the CG LNA topology provides a wideband input match that is less sensitive to input parasitic capacitances. Chip area is saved without using inductors for the input network.

In this paper, a general g_m-boosted design technique for common gate wideband LNA is discussed [3]. In a CG LNA, the input impedance of 50 Ohm is approximately $1/g_m$. The noise figure is

$$F_{CG-LNA} = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_s} \tag{2.14}$$

where induced gate noise is negligibly small.

The above equation illustrates the fundamental tradeoff between noise figure and input matching in a conventional CG amplifier. More specifically, if some input mismatch can be tolerated, g_m can be increased to decrease the noise figure (shown in Eqn. (2.14)) while the input reflection is maintained below some reasonable value. If the condition of input matching can be separated from noise performance, the possibility of improving noise figure arises. The proposed scheme is based on an

important observation [3]: two g_m values are used in calculating the noise factor of the CG amplifier. One is the effective transconductance into the source terminal; denote it as G_m. The other is the intrinsic transconductacne of the amplifying device, which is related to drain current channel noise and is denoted as g_m. A design challenge in improving CG-LNA is to modify the topology so that $G_m \neq g_m$. Specifically, to make $G_m \neq g_m$, a couple mechanisms may be introduced between the gate and source terminals. Fig. 2.4(a) depicts the topology of the proposed g_m-boosted CG-LNA. In this structure, rather than connecting the gate terminal to a dc bias voltage, an inverting amplification is introduced between the source and gate nodes of the MOSFET. The input impedance is

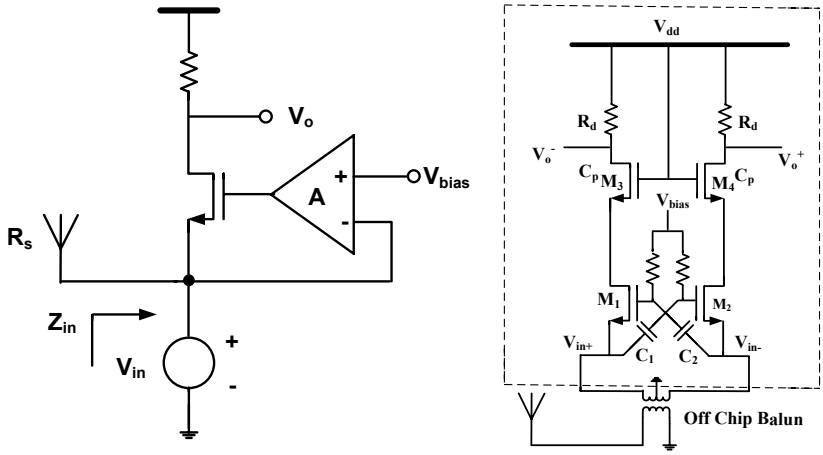
$$R_{in}(f) = \frac{1}{g_m(1+A)} \tag{2.15}$$

The noise factor becomes

$$\begin{aligned} F_{CG-LNA} &= 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A)^2 g_m R_s} \\ &= 1 + \frac{\gamma}{\alpha}\frac{1}{(1+A) g_m R_s} \end{aligned} \tag{2.16}$$

Capacitor cross-coupled CG LNA can be realized as one possible implementation of a g_m-boosted CG LNA with inverting gain (A) equal to 1. New structures for designing wideband LNA with gm-boosted CG-LNA topology without inductors were proposed in Fig. 2.4(b).

The LNA design uses an external balun to transform the single ended antenna



(a) (b)

Figure 2.4: (a) The G_m-boosted common-gate low noise amplifier (b) Capacitor cross-coupled common-gate low noise amplifier [3]

signal to differential signals. We utilize it presence to provide DC ground and an RF signaling path for the LNA. If an external balun is not desired then the sources of the input transistors can be biased with tail currents and the RF signal capacitively coupled. However, the use of the balun reduces headroom loss and improved noise figure. Simulation results of Fig. 2.4(b) are shown in Figs. 2.5and 2.6. The input reflection coefficient (S_{11}) is less than -12dB over the wideband (1GHz- 10GHz, shown in Fig. 2.5. Linearity (IIP3) is maintained at around 5dBm and NF is less than 3dB for the whole wideband band, shown in Fig. 2.6.

2.3.2 Mixer

A commonly used mixer in a RF system is the double-balanced Gilbert mixer. The mixer consists of differential transcondutors, a mixer core, and a load. The transcon-

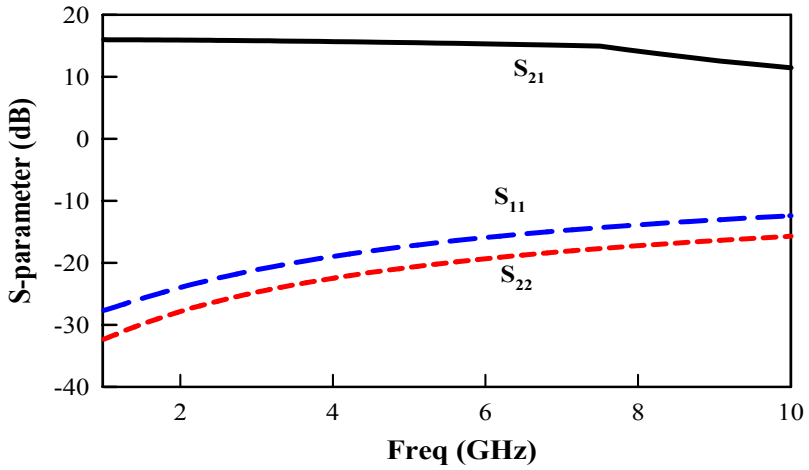


Figure 2.5: S parameters of capacitor cross-couple common-gate LNA under simulation

ductor converts the input voltage into a current, which is then switched by the mixer core into the load, and a voltage is produced. Both LO and RF are balanced, providing both LO and RF rejection at the IF output. The double-balanced Gilbert mixer also improved suppression of spurious products and is less susceptible to supply voltage noise due to differential topography. For a down-conversion double balanced Gilbert mixer, two signals,which are one from LO plus IF frequency, another from LO minus the IF frequency, are mixed to the same IF frequency. One of these signals is the desired signal, and the other is the image signal which corrupts the desired signal. A way of avoiding the image problem is the use of a quadrature down-conversion mixer [19]. In the quadrature down-conversion mixer, the RF signal is multiplied by both the in-phase (I) LO signal and a quadrature (Q) LO signal. Then the image and desired signals remain distinct in the complex IF signal. In order to maintain this image rejection, a high degree of amplitude and phase matching between I and

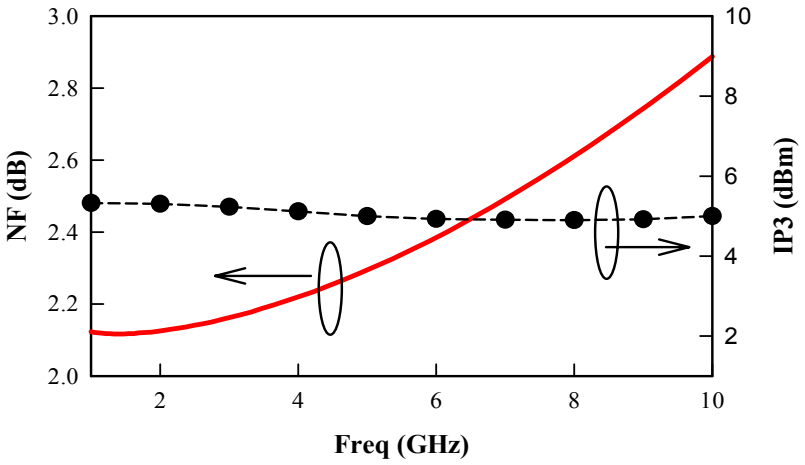


Figure 2.6: Linearity and NF of capacitor cross-couple common-gate LNA under simulation

Q channels is required [20].

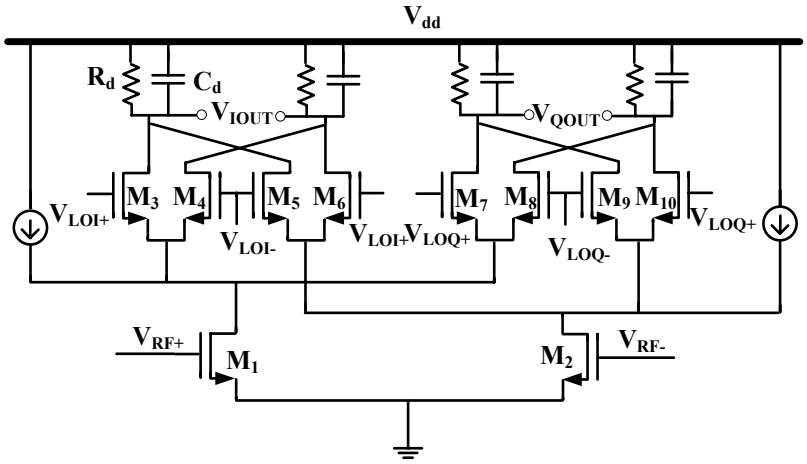


Figure 2.7: Schematic of the CMOS quadrature mixer

The quadrature mixer, consisting of two double balanced Gilbert mixers with the same RF input and quadrature LO signals is shown in Fig. 2.7. The operation of the quadrature mixer relative to a pair of double balanced Gilbert mixer depends on the LO signal used. The input RF and LO signals can vary in the range of 0.5

-11GHz. The output IF signal is in low frequency and is set at 300MHz. The current inject method is used to increase the linearity of this mixer [21]. Two dc currents are injected at the drains of the bottom stage transistors. The value of this dc current is optimized, so that it provides best the tradeoffs between high linearity, noise figure, conversion gain, power consumption, and bandwidth for the mixer. Simulation results are shown below. Conversion gain is about 6dB. The Noise figure (NF) is about 7.1 to 8.2dB, and the IIP3 maintains about 0.8 to 1.8dBm. The power consumption is about 13.5mW.

2.3.3 Combined LNAs and Mixers

Fig. 2.8 shows the simplified schematic of a capacitive peaking LNA and mixer (CPLM). Specifications were satisfied by changing the sizing of the transistors and setting the appropriate bias voltages for LNA and mixer. Due to noise and cutoff frequency, we choose minimum channel length (0.13 μm) for all devices. For LNA, Input match and linearity decide the size of M_1. The cascade device is chosen to be as small as possible to reduce the parasitic capacitances. The load is designed to achieve flat gain over the whole bandwidth. An upper limit to the load is set by the voltage headroom. The LNA is biased by means of current mirrors, not shown in Fig. 2.8. The transistors of current mirrors work under the saturation region. Because noise inverts to the overdrive voltage, make the overdrive voltage as large as possible. After first deciding all component values, the design is then optimized to maximize bandwidth, gain, noise figure, and input matching.

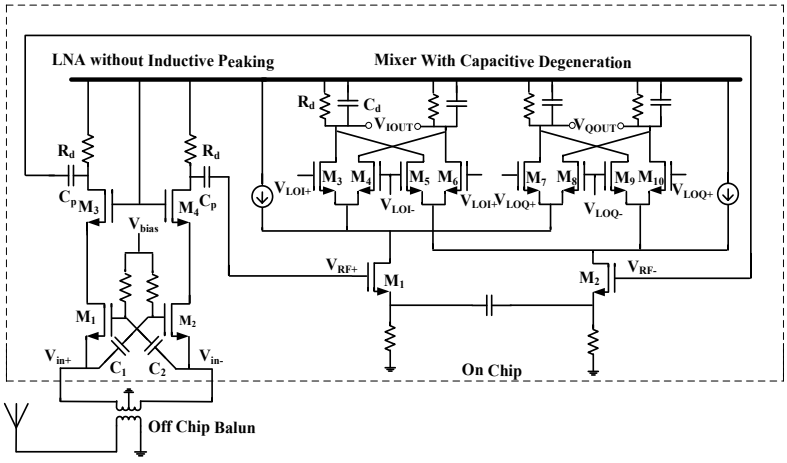


Figure 2.8: The simplified schematic of capacitive peaking LNA and mixer

The quadrature mixer follows a LNA and therefore the performance of the mixer also determines the performance of the overall system. The design of the mixer involves tradeoffs between linearity, noise figure, conventional gain and power dissipation. In a quadrature system, it is additionally required that there is little mismatch in amplitude and phase response between I and Q channels [16]. Due to the gain of the LNA, the mixer can have a higher noise figure but also requires a higher IP3. The noise figure of the mixer is usually designed to be smaller than the gain of LNA so that its noise contribution is smaller than that of the LNA [22], [19]. Because the input signal to the mixer is higher than that of the LNA, the linearity requirement of the mixer is higher than that of the LNA. In most cases, the mixer's IP3 limits the IIP3 of the front-end. For the quadrature mixer, all transistors are to operate in the saturation region. The differential transcondutors should be biased such that they have enough head room to swing without leaving the saturation region. The gain of the mixer is proportional to g_m of transcondutors, and mixer core transistors

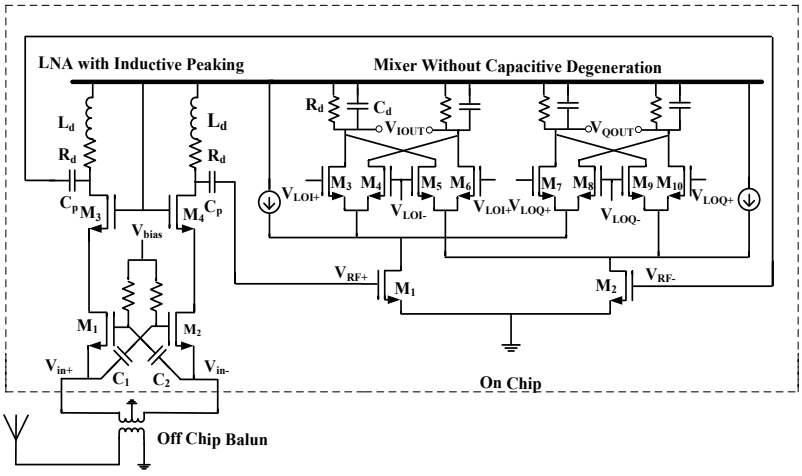


Figure 2.9: The simplified schematic of inductive peaking LNA and mixer

are chosen for proper switching.

To compare CPLM with inductive peaking LNA and mixer (IPLM), which is shown in Fig. 2.9, we keep the same total gain and bandwidth of mixer tailers. Inductors of IPLM, R_s and C_s in CPLM and loads (R_d)of both IPLM and CPLM are decided by above comparison. C_d in mixers is set to satisfy the cutoff frequency of the output IF signal. The capacitor (C_p) between LNA and mixer is chosen to avoid affect of DC from the LNA on the mixer. The buffer to drive a 50 external load for testing is also designed, but not shown in Figs. 2.8 and 2.9. The design procedure of CPLM and IPLM is basically comprised of executing several simulations until a desired result is achieved. The experimental measurement results are discussed in next section.

2.4 Measurement Results

Fig. 2.10 shows the measured receiver conversion gain (S_{21}) from 1 GHz to 11.0 GHz. A fairly flat power conversion gain of 20 dB is achieved over 1GHz to 10GHz for both CPLM and IPLM designs. There is a slight reduction in gain at both ends of the frequency with frequency degradation for CPLM being slightly worse (< 0.5dB) at the higher end. The measured input reflection coefficients (S_{11}) for both designs are also shown in Fig. 2.10. The S_{11} is better than -14dB from 1GHz to 10GHz for both designs. The gradual degradation in S_{11} at higher frequencies is expected for common-gate LNAs due to gate and pad parasitics.

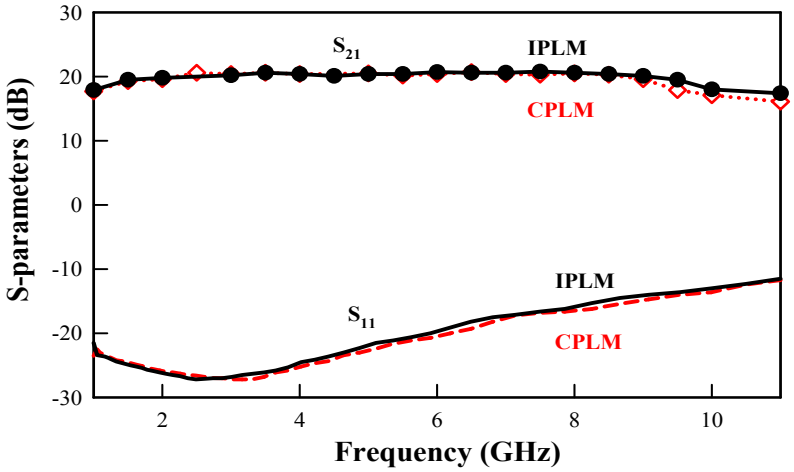


Figure 2.10: Measured S-parameters for CPLM and IPLM designs

The noise figure for both designs are shown in Fig. 2.11. For NF measurements, a fixed IF frequency of 300MHz is used and both RF and LO frequencies are swept from 0.5 GHz to 11 GHz. The LO power is maintained at 0dBm. The measured NF varies between 4.5dB to 6dB for both designs for the entire frequency range. The NF for

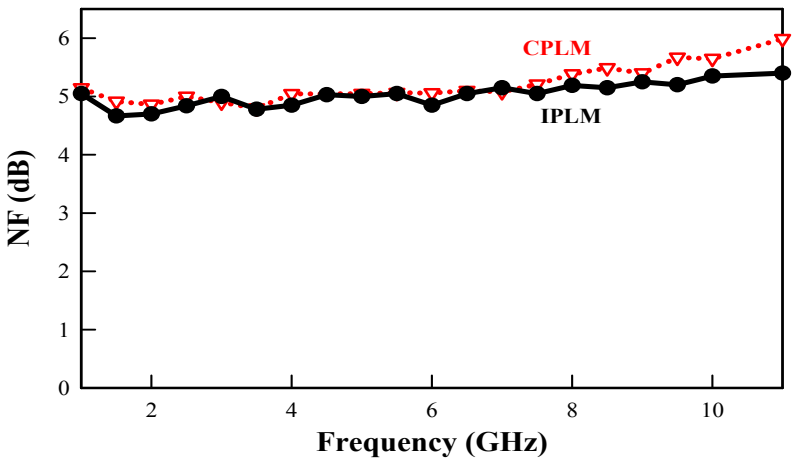


Figure 2.11: Measured noise figure for CPLM and IPLM designs vs. RF frequency @ IF=300MHz

CPLM is comparable to IPLM even though we have added more components because the degeneration does not allow all the noise to be input referred. The IIP_3 and P_{1dB} for both designs versus the input RF frequency are shown in Fig. 2.12. The measured P_{1dB} and IIP_3 for the CPLM design are roughly 3dB higher than those for the IPLM design. This is due to the negative feedback effect of capacitive degeneration which increases the transconducor linearity. Due to test equipment limitations, IIP_3 was measured up to 5 GHz only. Power consumption for the IPLM and CPLM frontend designs are 18 and 21 mW respectively. The 17% increase in power for CPLM is due to the negative feedback associated with capacitive degeneration which reduces the effective transconductance of M_2 in Fig. 2.1. Test results shown in Fig. 2.13 indicate that the IF bandwidth extends beyond 500MHz.

Appropriate figure of merits (FOM) are often used to compare the relative benefits of different circuits. For narrow-band circuits the FOM used to compare the relative

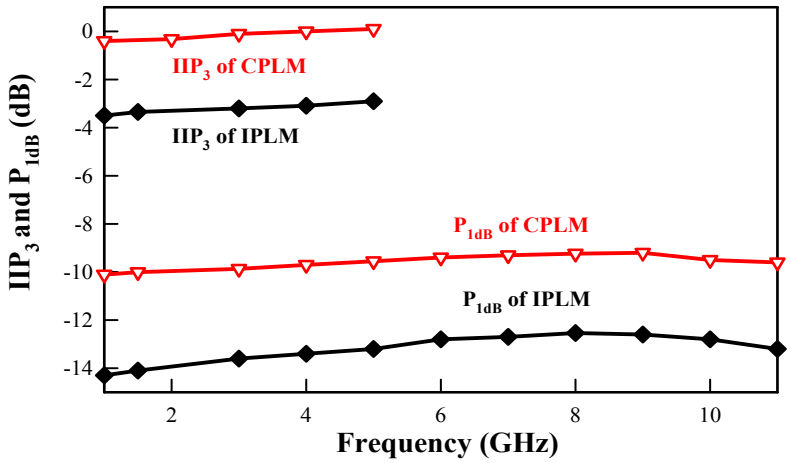


Figure 2.12: Measured IIP3 and P_{1dB} for CPLM and IPLM designs vs. RF frequency @ IF=300MHz

merits of different circuits does not include the bandwidth. We have augmented the traditional FOM for RF circuits by adding a criteria for signal bandwidth as wideband circuits are harder to design.

The new FOM is shown in (2.17). The new additional terms are shown after the $\times$ sign.

$$FOM_{new} = \frac{Gain_{lin} IIP3_{mW}}{(NF_{lin} - 1)P_{mW}} \times BW_f \tag{2.17}$$

Here $Gain_{lin}$ is the linear gain, $IIP3_{mW}$ is the linearity in mWs, NF_{lin} the linear noise figure, BW_f is the fractional bandwidth, P is the power in mWs.

In Table 2.1 we compare published results for LNAs, I/Q mixers and RF frontends with our designs. The FOM for CPLM is much higher than that for IPLM, and any of the other recently published results. The core layout area of CPLM is also about 22% of the area of IPLM. The area of the core circuits listed in the table, is re-calculated by eliminating test pads and test structures. The results show good agreement with

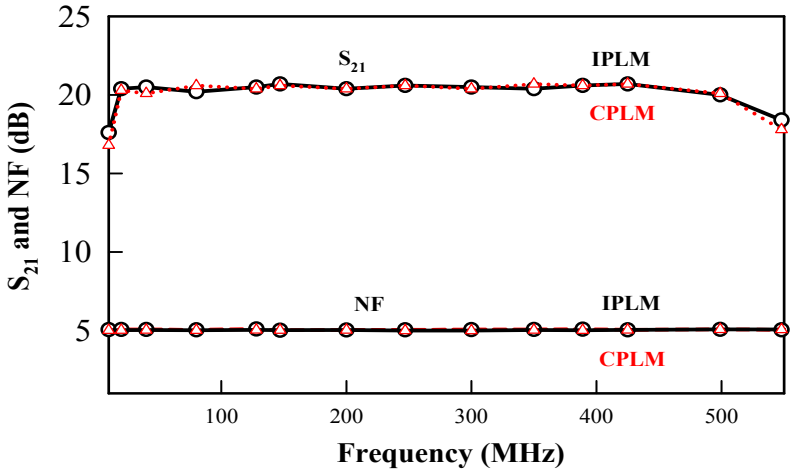


Figure 2.13: S_{21} and NF of CPLM and IPLM vs IF frequency @ RF=5 GHz

our numerical analysis results from Section 2.2.

The CPLM, IPLM and PLL circuits were fabricated in the 8 metal layer UMC 0.13 μm CMOS technology. Two chip micrographs are shown in Fig. 2.14.

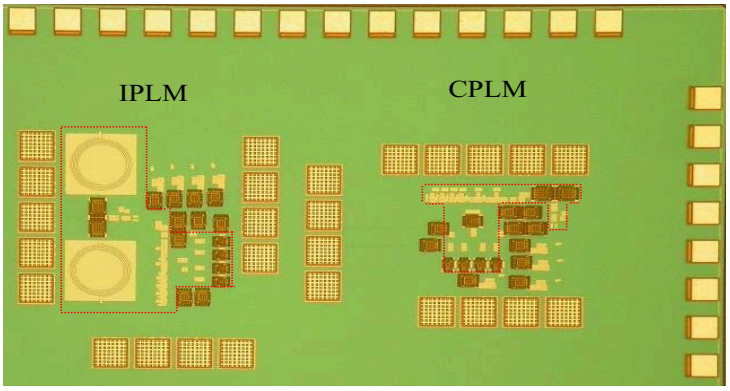


Figure 2.14: Micrograph of CPLM and IPLM fabricated in 130 μm COMS

Table 2.1: Summary of experimental results for UWB LNA, mixer, IPLM, CPLM and other recently published results

	Tech. [nm]	S_{11} [dB]	B [GHz]	NF [dB]	IIP3 [dBm]	Gain [dB]	P [mW]	Core Area $[mm^2]$	FOM_{new}
STD LNA [6]	180	≤ -9.9	2.3-9.2	≥ 4.0	-6.7	9.3	9	0.5	0.14
LNA [23]	180	≤ -5	1.5-12.3	4.4-5.3	7.4-8.3	8.5	4.5	0.46	3.27
LNA [7]	180	≤ -9.5	2-9.6	3.6-4.8	-7.2	11	19	0.03	0.11
LNA [24]	180	≤ -10	3-10	2.5-4.2	-5.5	21	30	1.8	1.21
LNA [8]	90	≤ -10	0.5-7	2-2.7	-4--8	24.5	42	0.013	5.02
LNA [25]	130	≤ -12	3.1-4.9	≥ 3.3		22	3.75		
SSB Mixer [25]	130		3.1-4.9	16		10	3.75		
Mixer [26]	180		3.1-10.6	10	4	10	10	0.54	0.30
Mixer [10]	180		3.1-8.72	6.8-7.3	5	2.5-5	10.4	0.8	0.18
Mixer [9]	180		0.5-25		-5	11	71	0.3	
LNA + Mixer [13]	65	< -10	0.5-7	5.5	-3	18	16	<0.01	5.04
LNA + Mixer [14]	65	< -8	2-8	4.5	-7	23*	31	0.09	4.22
Our LNA (no inductor)	130	≤ -12	1-10	2.1-2.8	5	16	3.5	0.015	8.03
Our Mixer (no DEG)	130		1-10	7.1-8.2	0.8-1.8	6	13.5	0.031	0.06
IPLM	130	≤ -14	1-10	4.7 - 5.35	-3.5 - -2.9	20	18	0.18	11.5
CPLM	130	≤ -14	1-10	4.8 - 5.65	-0.4 - 0.1	20	21	0.039	18.4

$*$: includes IF-amp

2.5 Conclusions

In this paper we introduced a inductorless wideband RF frontend from 1GHz to 10GHz. To validate our design methodology two receiver RF frontend were designed; a traditional inductor based design and a inductorless design. A common-gate LNA transconductor is followed by a capacitive peaking LNA-mixer pair (CPLM). Experimental measurement results show that a CPLM with the same bandwidth has better linearity, comparable noise figure and uses only 17% more power. The silicon area for the inductorless LNA and I/Q mixers is roughly 22% of traditional inductor based designs showing area savings and improved portability. In this chapter we focused on broad-band RF design. However, the techniques developed here are easily adapted to narrow-band RF design.

Chapter 3

Injection-locked Frequency Dividers

3.1 Introduction

With the growing demands of wideband mobile data services such as the MBOA-UWB standard, multi-band cellular and software-defined radios, the required operating frequency of the PLLs within these systems has been forced to increase due to the increasingly crowded spectrum. Frequency dividers are an essential component of PLLs are required to provide a range of division ratios. Traditionally, such dividers have been implemented as a string of wideband static frequency dividers based on flip flops, with the first divide-by-two usually implemented utilizing current-mode logic to obtain suitable high frequency operation. The power consumption of a static divider increases proportionately with operating frequency due to the complete charging

and discharging of capacitances in each cycle. More recently, narrow band injection locked frequency dividers (ILFD) based on LC resonators have been used to reduce power dissipation [27]. LC resonator based ILFDs are capable of very high frequency operation while dissipating relatively low power in the tank [28].

As with VCOs both LC resonator based and ring oscillators based injection locked dividers are possible. However, due to the high tank Q, limited tuning range and large die area consumption, the application of LC based ILFDs has been limited [29]. Ring oscillator VCOs on the other hand have large tuning range but have traditionally poor phase noise performance [30]. However, as the phase noise performance of appropriately designed injection locked oscillators is dominated by the injected signal rather than by the injection locked oscillator performance this is not an issue for ring oscillator based ILFDs [31]. With the result that there is significant research interest in ring oscillator based ILFDs with larger locking ranges and higher division ratios.

The highest division ratios of 18 for differential ring oscillator based ILFDs and a division ratio of 5 for single-ended ring oscillator based ILFDs have been presented [32, 33]. The majority of ring oscillator ILFD research has focused on limited division ratios on either single-ended or differential designs, with typically an emphasis on odd division ratios. The theory for differential ILFDs to even numbers and low division ratios was originally developed in [34]. In this chapter we extend these results and discuss the mechanisms and theories for both single-ended and differential ILFDs that allow for all division ratios, i.e., not limited to *even* or *odd* division ratios or to *low division numbers*.

The chapter is organized as follows: Section 3.2 introduces a general ILFD model

and circuits for both single ended ILFDs (S-ILFD) and differential ILFDs (D-ILFD). Section 3.3 provides measurement results to corroborate our theory. We provide some concluding remarks in Section 3.4.

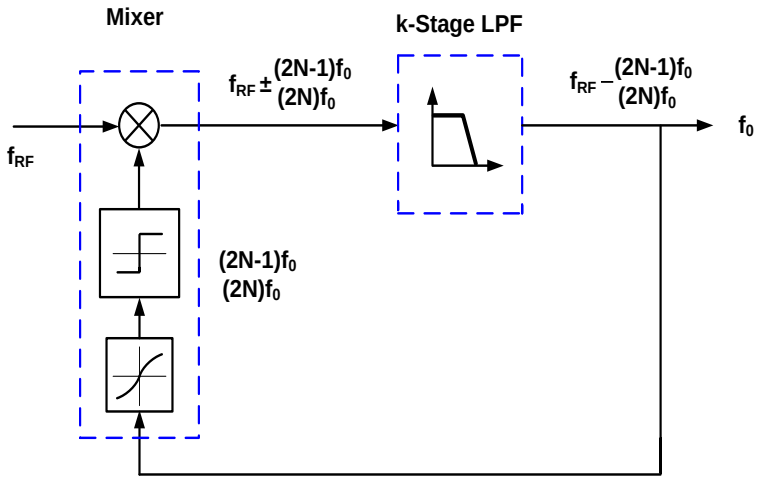


Figure 3.1: Block diagram model for injection locked divider behavior

3.2 ILFD model and circuits

3.2.1 Injection-locked frequency divider model

A simplified block diagram to explain the inner workings of ILFDs is shown in Fig. 3.1. A slightly simplified version of this model, originally presented in [34], focused on D-ILFDs and is limited to even division ratios. The model consists of a mixer and the squarer block emulating the behavior of a differential pair, a lowpass filter that emulates the band limited behavior of the multi-stage oscillator, and device level nonlinearity block that introduces even order harmonics in differential structures. The lowpass filter model is used to limit the harmonics to the desired tone and

suppresses all the other spurs. Our model can be used to describe both D-ILFDs and S-ILFDs and therefore both even ($2Nf_0$) and odd ($2N-1f_0$) harmonics are available.The mixer multiplies the input signal (f_{RF}) with the output signal (f_0) and generates frequency components at $f_{RF} \pm$ (2N-1)f_0 or 2Nf_0.

When the loop is locked, the output frequency (f_0) will be synchronized with one of the sub-harmonics of the input signal f_{RF}/(2N)) or (f_{RF}/(2N-1) within the locking range of the divider. When no signal is injected, the ILFD free runs and f_0 is solely determined by circuit parameters. When the output amplitude of f_0 is sufficiently large, the injection locking dynamics are determined primarily by the phase relationship around the loop [34]. The mixing function for a differential design has slightly different dynamics from those for a single-ended design. In the following subsections we discuss the division ratios, locking range and phase noise for D-ILFDs and S-ILFDs.

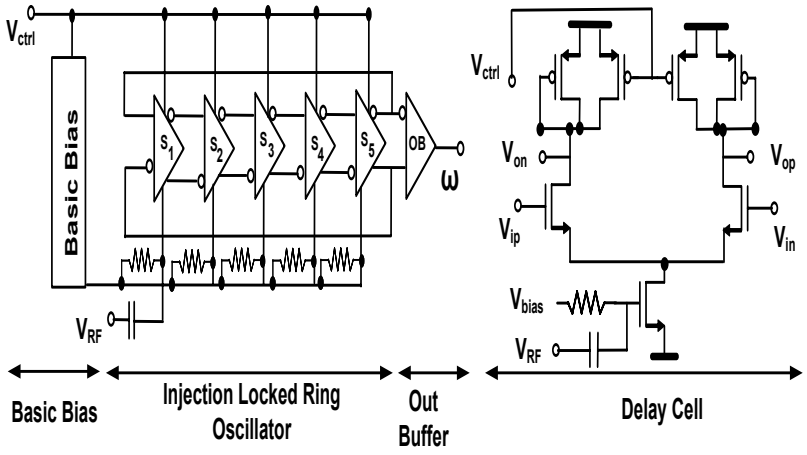


Figure 3.2: Circuit schematic diagram of the D-ILFD used in prototype design

3.2.2 ILFD based on differential ring oscillator (D-ILFD)

In a D-ILFD the differential pair is normally modeled as a pure squarer that generates only odd harmonics. However, as device sizes shrink short-channel effects increases the nonlinearity of transistors. With the result that the differential pair and tail device in the single-balanced mixer no longer follows the pure square-law. Short channel MOSFET vertical field mobility degradation and velocity saturation can be captured using the form in Eqn (3.1), where α is the short channel degradation factor.

$$I_{ds} = \left[\frac{1}{2}\frac{W}{L}\mu_n C_{ox}\right]\frac{V_{ov}^2}{1+\alpha V_{ov}} \tag{3.1}$$

The drain current of the tail device now contains the higher harmonics as well. The combined output of the mixer and tail device can now be written as shown in Eqn (3.2), where $\Pi(t)+\Lambda(t)$ is the new mixing function; $\Pi(t)$ is a square wave; $\Lambda(t)$ is the mixing function due to the short channel effects and θ is the phase difference with reference to the input [25].

$$I_{out} = [\Pi(t)+\Lambda(t)][I_{RF}cos(\omega t+\theta)+I_{bias}] \tag{3.2}$$

The Fourier coefficients, C_n, of the mixing function can by approximated by Eqn (3.3), where n is an integer; β is a fixed short channel coefficient whose value is usually less than 1 for the D-ILFD and equal to 1 for the S-ILFD.

$$\begin{aligned} C_n &= \frac{1}{n\pi} \cdot (-1)^{\frac{n-1}{2}} \text{ for n = odd} \\ &= \frac{\beta}{n\pi} \cdot (-1)^{\frac{n}{2}} \text{ for n = even} \end{aligned} \tag{3.3}$$

The impact of the lowpass filter can be modeled by Eqn (3.4), where ω_0 is the frequency of the free running oscillator and k is the number of stages in the oscillator.

$$H(j\omega) = \frac{H_0}{\left[1 + j\frac{\omega}{\omega_0} tan\left(\frac{\pi}{k}\right)\right]^k} \tag{3.4}$$

The phase expression around the loop in Fig. 3.1 can be expressed for n = odd in Eqn (3.5) and for n = even in Eqn (3.6).

For n = odd

$$\begin{aligned} \arctan\left[\frac{\gamma(C_{n-1} - C_{n+1})\sin(\theta)}{C_1 + \gamma(C_{n-1} + C_{n+1})\cos(\theta)}\right] = \\ k \arctan\left[\frac{\omega}{\omega_0} tan\left(\frac{\pi}{k}\right)\right] - \pi \end{aligned} \tag{3.5}$$

For n = even

$$\begin{aligned} \arctan\left[\frac{\gamma(C_n - C_{n+2})\sin(\theta)}{C_2 + \gamma(C_n + C_{n+2})\cos(\theta)}\right] = \\ k \arctan\left[\frac{\omega}{\omega_0} tan\left(\frac{\pi}{k}\right)\right] - \pi \end{aligned} \tag{3.6}$$

Here γ is the injection efficiency, Q is the quality factor of the tank and V_{osc} and V_{inj} are the amplitudes of the oscillator and injection signals respectively.

The phase introduced by the D-ILFD can be approximated by Eqn (3.7), which includes extensions for the nth order subharmonic injection [25].

$$\sin\theta \approx \frac{2Q}{\omega_0} \cdot \frac{V_{osc}}{V_{inj}} \left(\omega_0 - \frac{\omega_{inj}}{n}\right) \tag{3.7}$$

Using Eqn (3.3), Eqn (3.5), Eqn (3.6) and Eqn (3.7), we can get two approximate analytical expressions for the locking range. Here, C_n, is the Fourier coefficients from Eqn (3.3) and κ is a fixed coefficient obtained by setting n large in Eqn (3.5) and Eqn (3.6).

For n = small

$$\Delta\omega \approx \gamma C_n \frac{\omega_0}{2Q} \frac{V_{inj}}{V_{osc}} \tag{3.8}$$

For n = large

$$\Delta\omega \approx \gamma \kappa \frac{\omega_0}{2Q} \frac{V_{inj}}{V_{osc}} \tag{3.9}$$

Once injection locked, the phase noise of ILFDs has two contributors; the phase noise contributions of the free running oscillator itself (L_{free}) and the phase noise contribution from the externally injected signal (L_{ext}). As these two sources are uncorrelated random processes, the total phase noise of ILFDs can be obtained by taking the sum of noise powers as shown in Eqn (3.10). This equation, based on work from [25, 31, 35], includes extensions for the nth order subharmonic injection.

$$\begin{aligned} L_{locked,tot} = & \frac{(\Delta\omega)^2 \cdot \cos^2\theta}{(\omega_0 - \frac{\omega_{inj}}{n})^2 + \Delta\omega^2 \cdot \cos^2\theta} \cdot L_{ext} \\ & + \left(\frac{\omega_0 - \frac{\omega_{inj}}{n}}{(\Delta\omega)^2}\right)^2 \cdot L_{free} \end{aligned} \tag{3.10}$$

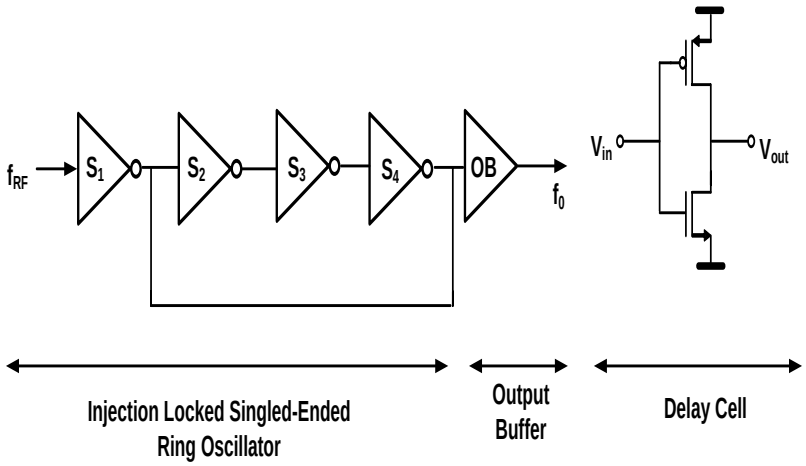


Figure 3.3: Circuit schematic diagram of the S-ILFD used in prototype design

3.2.3 ILFD based on single-ended ring oscillator (S-ILFD)

The circuit schematic for the S-ILFD is shown in Fig. 3.3 [31]. In this model, S_1 is treated as a mixer based on an inverter. Here, S_2, S_3 and S_4 form the three-stage ring oscillator and is modeled as a lowpass filter. Because of its single-ended nature, both even and odd harmonics are contained in the mixer output. However, compared to the differential structure the magnitude of the even harmonics are larger. So, other than the relative magnitude of the even and odd harmonics the equations developed in the previous sub-section regarding the locking range and phase noise developed are also applicable for the S-ILFD.

3.3 Experimental Results

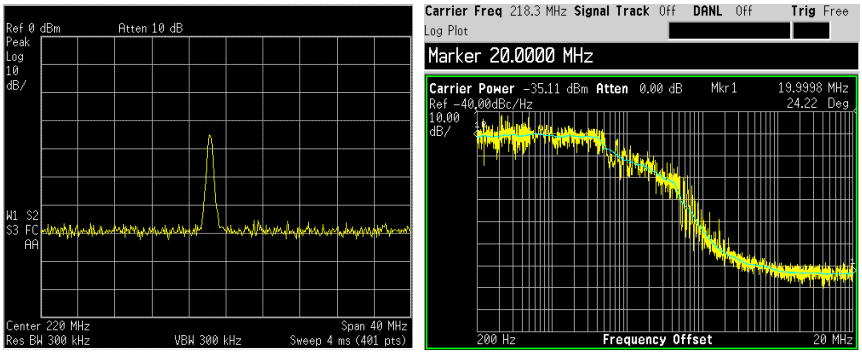
In this section we provide measurement results for two prototypes. One design implements the differential ILFD shown in Fig. 3.2 and the second design implements the

single-ended ILFD shown in Fig. 3.3. The free running frequencies for the D-ILFD and the S-ILFD are 264MHz and 220MHz respectively. The power consumption for the core D-ILFD is 3.0mW and 1.2mW for the core of the S-ILFD. In the next set of tests we measure the lock range and the integrated phase noise for different division ratios. The injection signal is provided by a low-noise sine-wave generator at a constant power level of about -5dBm. The input frequency is varied from 528MHz to 10.56GHz for the D-ILFD and from 440MHz to 9.9GHz for the S-ILFD. For calculating the RMS phase noise we integrate the phase noise from 200Hz to 20MHz for both D-ILFD and S-ILFD on an Agilent E4407 spectrum analyzer.

The output spectrum and measured phase noise for the free running S-ILFD is shown in Fig. 3.4. The integrated phase noise is quite large at approximately 24^o. In Fig. 3.5 we show the output spectrum and measured phase noise for the D-ILFD for a division ratio equal to 40. The free running RMS phase noise for the D-ILFD is approximately 15^o which reduces to approximately 2.7^o after being injection locked.

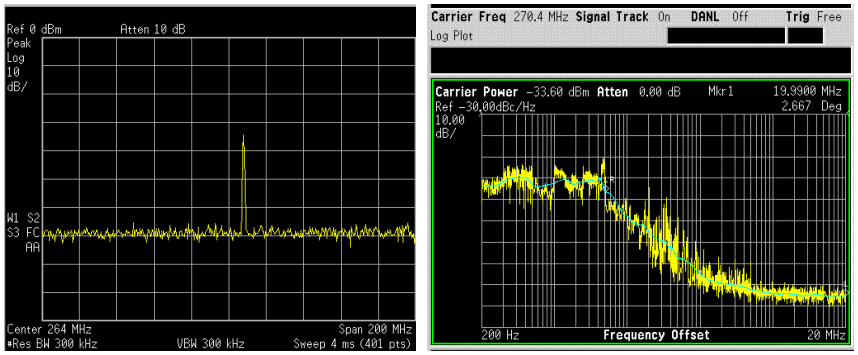
The lock range versus division ratios for the D-ILFD are shown in Fig. 3.6. The lock range for both n=odd and n=even deceases with increasing n and levels off to a constant, which is consistent with our lock range theory developed above. Additionally, the lock range for n=odd is larger than the lock range for n=even when the division ratio is low due to the β factor in Eqn (3.6) which is smaller than 1. The lock range levels off to a constant ($\approx 30MHz$) as described by Eqn (3.9) when the division ratio is large.

The measured integrated RMS phase noise for different division ratios for the D-ILFD is shown in Fig. 3.7. The free running RMS phase noise is shown as division



(a) (b)

Figure 3.4: Output spectrum (a) and measured phase noise (b) for a free running S-ILFD at 220MHz



(a) (b)

Figure 3.5: Output spectrum (a) and measured phase noise (b) for a injection locked D-ILFD at a division ratio of 40

ratio equal to zero. As the division ratio increases, the integrated RMS phase noise deceases, which can be explained by Eqn (3.10). For increasing the division ratio, the phase noise of the locked oscillator is dominated by the injection signal. The noise rejection of the injection signal noise increases when the division ratio increases [35].

Fig. 3.8 shows the lock range with different division ratios for n=odd and n=even for the S-ILFD. As with the D-ILFD the lock range for odd and even numbers decease

and become constant with increasing the division ratios. However, here the lock range of n=odd number is similar to the lock range of n=even when the division ratios are low because the β factor in Eqn (3.6) is equal to 1 for single-ended designs. The lock range levels off to a constant ($\approx 40MHz$) again consistent with Eqn (3.9).

Fig. 3.9 shows the measured integrated RMS phase noise versus division ratios for S-ILFD. As the division ratios increases, the integrated RMS phase noise deceases, which is also consistent with Eqn (3.10).

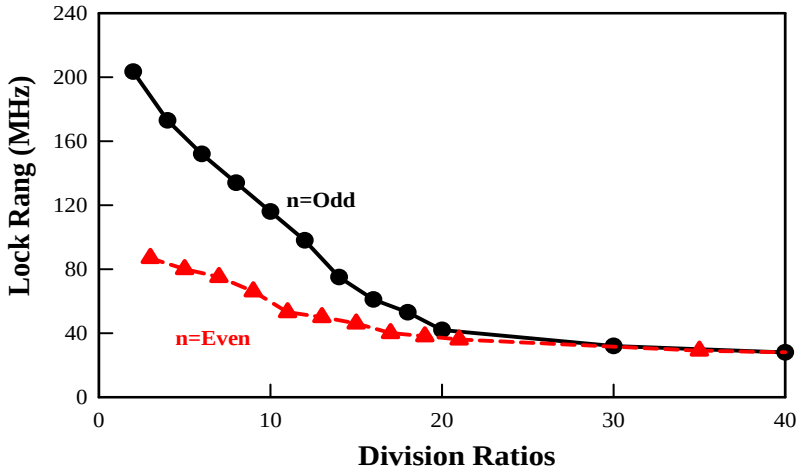


Figure 3.6: The measured lock range with division ratios for D-ILFD

From experimental results presented above, we note that the lock range for the D-IFLD is smaller than that for the S-IFLD under similar experimental conditions. We also note that the phase noise for the single-ended design is larger than for the differential design due to the reduced power consumption of the S-ILFD ($\approx 2.5\times$ lower).

The D-ILFD and S-ILFD designs were fabricated in the 8 metal layer UMC 0.13μm CMOS technology. Two chip micrographs are shown in Fig. 3.10. The core areas are

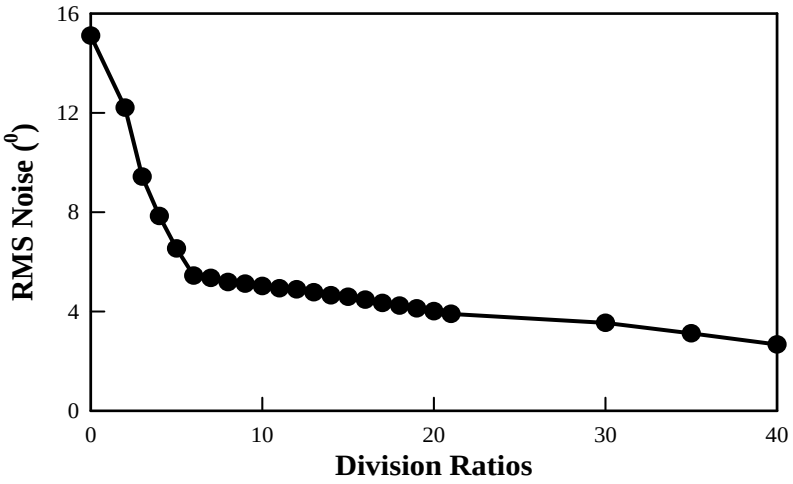


Figure 3.7: Integrated RMS phase noise with division ratios for D-ILFD

0.34mm×0.05mm and 0.168mm×0.022mm for the D-ILFD and the S-ILFD respectively.

3.4 Conclusions

In this chapter we developed theory for the lock range and phase noise for both differential and single-ended ILFDs. We showed that both D-ILFDs and S-ILFDs can be made to lock to even and odd harmonics. Measurement results for the D-ILFD and S-ILFD show that the lock range of all harmonics decreases with increasing n at the beginning and then levels off to a fixed level. Measured integrated phase noise for D-ILFD and S-ILFD also show that it decreases with increasing division ratio. Ring oscillator based D-ILFDs and S-ILFDs operate at low power, consume small area, have large tuning range, and can be made to operate at low phase noise making them particularly well suited for wideband PLLs. We provided measurement

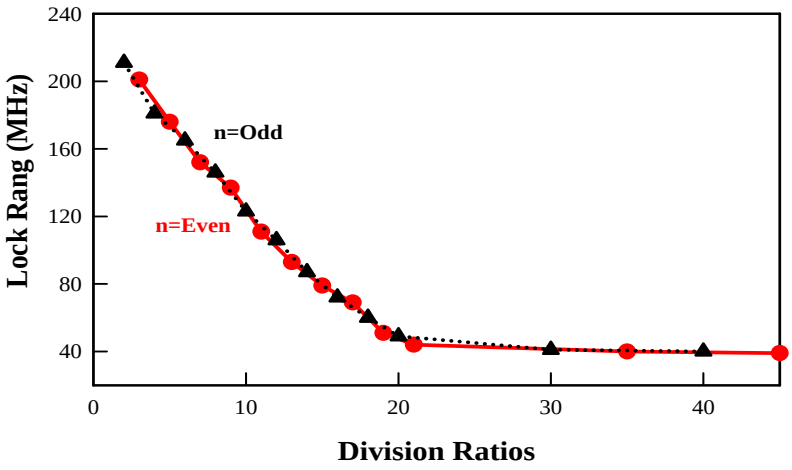


Figure 3.8: The measured lock range with division ratios for S-ILFD

results for division ratios of 40 for D-ILFDs (corresponding to $f_{RF} = 10.56$GHz) and 45 (corresponding to $f_{RF} = 9.9$GHz) for S-ILFDs respectively showing their high frequency potential.

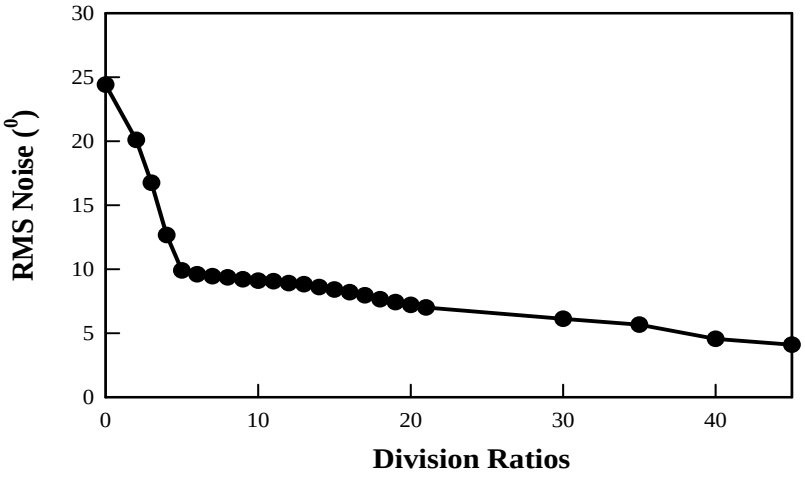
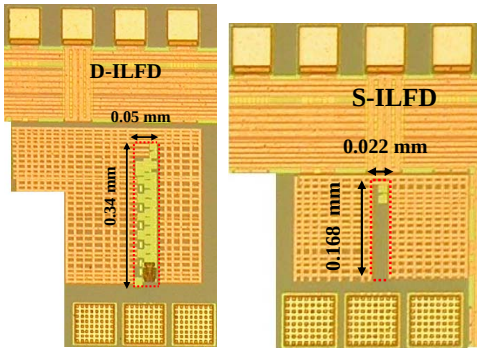


Figure 3.9: Integrated RMS phase noise with division ratios for S-ILFD



(a) (b)

Figure 3.10: Micrograph of the chip fabricated in 130 μm COMS (a) D-ILFD and (b) S-ILFD

Chapter 4

Inductorless Phase-locked Loop

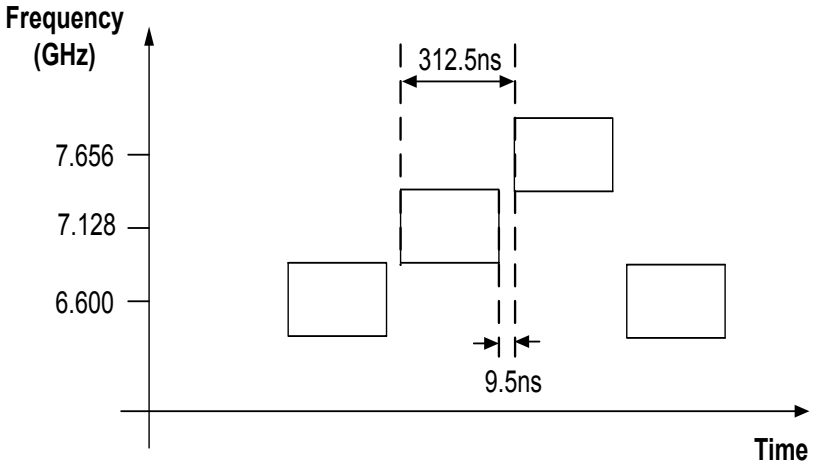
4.1 Introduction

Wide lock range PLL are of interest for a variety of applications, including the the UWB-MBOA standard, multi-band cellular and software-defined radios. The design of wide lock range PLL based on ring VCO is a challenging task due to the conflicting requirements of small integrated phase noise, fast settling time, small spurl levels and low power consumption. The need to meet theses specification in a given UWB standard further complicates the design. In early 2002, the Federal Communications Commission (FCC) has approved allocation of 7.5GHz of spectrum for unlicensed use of ultra-wideband (UWB) devices for commercial applications in the 3.1-10.6GHz frequency band with an equivalent isotropically radiated power (EIRP) of only -41.3 dBm/MHz [36]. Significant research and industrial effort have been invested in this, mainly to focus on its high bandwidth potential intended for short range and

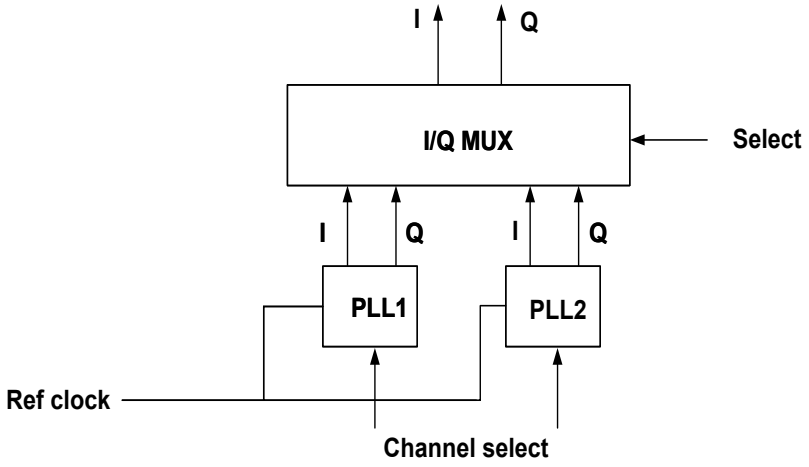
high data rates applications, such as wireless multimedia and high performance PC peripherals [37]. Several proposals have been presented to realize a short-range high data rate communication. Currently two proposals under consideration are multi-band OFDM Alliance (MBOA) and direct-sequence UWB (DS-UWB). The MBOA standard proposes a channelized UWB, dividing the UWB spectrum into five bands. Each band consists of multiple channels of 528MHz. The data is frequency-hopped QPSK OFDM-modulated on 128 sub-carriers. The proposed symbol length is 312.5ns, with a guard interval of 9.5ns [36] shown in Fig. 4.1(a), which sets high demands on the applicable frequency synthesizer for UWB radio.

Methods to produce UWB standard frequency synthesizers include SSB mixing method, LO signal multiplexing and Dual PLL shown in Fig. 4.1(b) . It is hard to achieve spectral purity better than -40 dBc in SSB mixing and LO signal multiplexing, which also consume a lot of chip power and area [38]. The dual PLL offer alternative with better spectral purity, low chip power and area. But the requirement for PLL in dual-PLL is fast settling time, wide tuning range. A very fast settign PLL design for this type PLL has been presented in [39], which consume a significant amount of power and die area. The PLL using interpolative ring-VCO for dual-PLL have been reported in [40], which just covers part of UWB bandwidth. In this chapter, we will display the PLL based on ring VCO and injection locked frequency divider for dual-PLL with lowest power and die area consumption in extended whole UWB bands.

The chapter is organized as follows: In the next section we discuss specification of PLL, this is followed by details for design blocks of PLL design in the following section.



(a)



(b)

Figure 4.1: (a) Frequency hopping for each band in MBOA (b) Fast hopping synthesizer by using Dual PLL

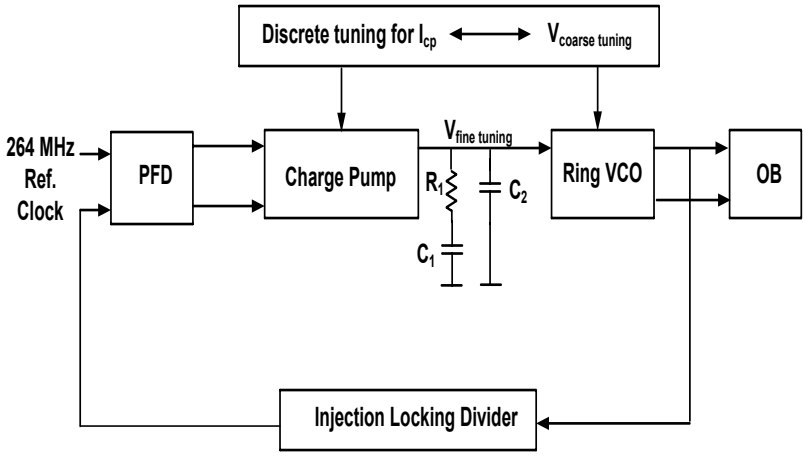


Figure 4.2: The proposed PLL block diagram

Section 4.4 provides experimental measurement results and Section 4.5 provides some conclusions.

4.2 Specification of PLL Design

Fig. 4.2 illustrates the block diagram for the proposed inductorless, ring-oscillator based PLL. It comprises of a 4-stage ring VCO, injection locking divider, a phase-frequency detector (PFD), a charge pump, and an integrated third order passive loop filter. This design uses an updated self-boosted bias technique for the ring VCO [41], which includes an additional opamp to minimize supply and substrate noise induced jitter. In addition a 5-stage injection locking ring oscillator frequency divider, which can lock to all harmonics, has been developed. A simple linear PFD based on two re-settable D flipflops is used to generate an up and a down signal that switches the current of the charge pump. We utilize a differential charge pump with a single-ended

passive loop filter [16]. The circuits block will be discussed in the next section.

The settling time of the synthesizer is set by the open-loop bandwidth. A larger loop bandwidth results in a faster setting time and rejects more of the VCO phase noise. However, the higher the loop bandwidth, the higher the degradation to the residual frequency modulation of the free-running oscillator will be. In order to comply with the settling time requirements it is preferable to limit the loop bandwidth to the maximum necessary. On the other hand, a small loop bandwidth results in large filter component values, leading to large silicon area and large noise contribution of the loop filter's resistor [42]. This PLL for UWB is designed to settle in approximately 100ns to guarantee a settling time below 310 ns over process and temperature variation. The minimum open-loop bandwidth to achieve a setting time of 100 ns can be roughly given as following:

$$f_c = \frac{1}{t_{lock}\xi_e(\phi_m)} ln(\frac{f_{step}}{f_{error}}) \tag{4.1}$$

Where $\xi_e(\phi_m)$ is the effective damping coefficient as a function of the loop's phase margin ϕ_m , f_{error} is the allowable frequency error after a predefined locking time t_{lock}, and f_{step} is the magnitude of the frequency jump. For the fastest settling time, the phase margin should be set to 50^0, and $\xi_e(\phi_m)$ will be approximately equal to 5 [43]. In the UWB case of 528 MHz frequency jump and 1-kHz frequency tolerance, f_c is about 26MHz. In a typical design, the loop bandwidth is smaller than one-tenth of the reference frequency to guarantee loop stability. The referencee frequency will be set to 264 MHz in this design.

The design of a PLL also involves trades offs between stability, locking time, chip area, phase noise, spurious response, loop bandwidth and power consumption. Design variables in this PLL includes the loop order, the gain of VCO K_{VCO}, the divider ratio M and the charge pump current I_p, which are decided by operational center frequency (ω_0). The proposed PLL are the third order PLL. The 3^{th} order loop filter can be modeled by the transfer function $F(\Delta\omega)$, which is decided by R_1, C_1, C_2 shown in Fig. 4.2; The additional pole of a third order PLL provides more spurious suppression. However, the extra phase lag associated with this pole introduces a stability issue. Thus loop filter must be designed carefully to provide the required filtering while maintaining the loop stability, which will be discussed in next section. In this design, the Phase margin is about 50^0 and f_c is about 26MHz.

The noise requirement set by the UWB proposals, which is defined as the overall integrated rms phase noise from 0Hz to infinity and this one should be bellow 3.5^0. To understand the total phase noise at the output of the system, the effect of various noise sources has to be calculated first. Due to our PLL covering from 1GHz to 10GHz, we calculate the phase noise at 10GHz. Noise sources include ring-based VCO, the reference, charge pump, and loop filter, crystal oscillator and injection locked frequency divider.

The 3^{th} order loop filter transfer function is listed as following:

$$F(\Delta\omega) = \frac{\Delta\omega R_1 C_1 + 1}{(\Delta\omega R_1 C_1 C_2 + C_1 + C_2)(\Delta\omega)} \tag{4.2}$$

Phase noise due to R_1 is calculated to be:

$$L_{R_1}(\Delta\omega)_{close} = \frac{4KTR_1}{2\pi}\frac{1}{2}[\frac{\frac{1}{\Delta\omega C_2}}{R_1+\frac{1}{\Delta\omega C_2}+\frac{1}{\Delta\omega C_1}}]^2 [\frac{\frac{K_{vco}}{\Delta\omega}}{1+F(\Delta\omega)\frac{K_{vco}I_p}{\Delta\omega 2\pi M}}]^2 \tag{4.3}$$

where the first term represents the spectral density of R_1 in terms of $\Delta\omega$; K is the Boltzmann constant; T is absolute temperature; The factor $\frac{1}{2}$ is for double sideband spectral density. This phase noise is from R_1 source to the output, which have been multiplied by the square of the transfer function.

For a linear model, the phase noise for an N-stage ring oscillator can be written in terms of the Q factor as [44]:

$$L_{VCO}(\Delta\omega)_{open} = \frac{4NFKTR}{V_{pp}^2}(\frac{\omega_0}{Q\Delta\omega})^2 \tag{4.4}$$

$$L_{VCO}(\Delta\omega)_{close} = L_{VCO}(\Delta\omega)_{open} [\frac{1}{1+\frac{F(\Delta\omega)K_{vco}I_p}{\Delta\omega 2\pi M}}]^2 \tag{4.5}$$

Where F is excess noise factor, which accounts for the total noise from the passive resistor R and the active device (-G_m); V_{pp} repents the peak-to-peak signal voltage; ω_0 is the center frequency of oscillation, and $\Delta\omega$ is the offset from the center frequency; R is passive resistor.

The phase noise contribution from charge pump can be calculated:

$$L_{CP}(\Delta\omega)_{close} = (\sum I_{total}(\Delta\omega))\Delta t\frac{f_0}{2} \left[\frac{\frac{F(\Delta\omega)K_{vco}}{\Delta\omega}}{1+F(\Delta\omega)\frac{K_{vco}I_p}{\Delta\omega 2\pi M}}\right]^2 \tag{4.6}$$

Where $\sum I_{total}(\Delta\omega)$ is sum of total noise, which include thermal noise and flicker noise by adding the uncorrelated noise sources in the transistors of the charge pump; Δt is the pulse width of the up and down signals in locked condition, which is about 0.2ns in our design. $\Delta t f_0$ is the fraction of time during the charge pump is active [45].

The resulting closed loop phase due to the input signals to PFD, which include the phase noise from crystal oscillator and injection locking divider:

$$L_{input}(\Delta\omega)_{close} = (\sum(L_{crystal}(\Delta\omega)) + L_{divider}(\Delta\omega)) \left[\frac{\frac{I_p}{2\pi}\frac{F(\Delta\omega)K_{vco}}{\Delta\omega}}{1+F(\Delta\omega)\frac{K_{vco}I_p}{\Delta\omega 2\pi M}}\right]^2 \tag{4.7}$$

The equations above are quite complex and more insight is provided by graphically plotting the various terms. Detailed BSIM3V3 MOS model parameters for $0.13\mu m$ CMOS process were used in MathCAD for these plots. The sum of all these uncorrelated noise sources gives the total phase noise at the output, which are shown in Fig. 4.3.

The overall integrated phase noise in degrees can be roughly calculated by the

following formula [39] for UWB technology:

$$noise_{rms} = \frac{180}{\pi} 10^{\frac{k}{20}} [f_c(1 + 10^{\frac{p}{10}}) + 2(10^{\frac{p}{10}})]^{0.5} \tag{4.8}$$

Where f_c is the loop bandwidth (Hz), k is the in-band phase noise density (dBc/Hz), and p is the peaking of k. From the Fig. 4.3 our integrated phase noise is about 2^0 with a loop bandwidth of 26 MHz.

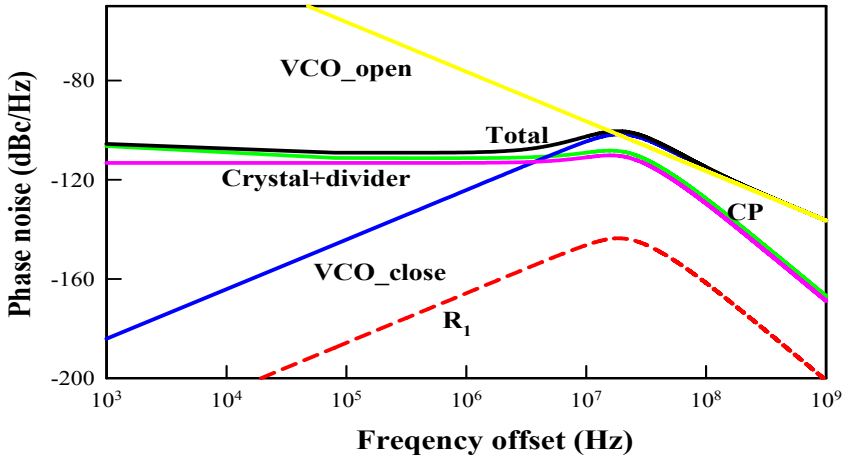


Figure 4.3: Output phase noise due to different sources @ f=10GHz

4.3 Circuit design

4.3.1 Phase/frequency detector (PFD)

The PFD has been implemented with two D-type flip-flops (DFF), shown in Fig. 4.4. This PFD generates an Up and a Down signal that switches the current of the charge pump.The DFFs are triggered by the inputs to the PFD. Initially, both outputs are

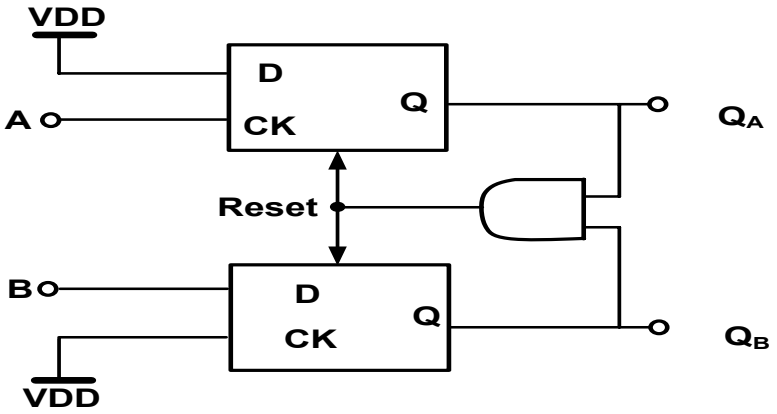


Figure 4.4: Implementation of PFD architecture

low. When one of PFD inputs rises, the corresponding output becomes high. The state moves from an initial state to an Up or Down state. The state is held until the second input goes high, which in turn resets the circuit and returns the initial state.

The PFD's characteristic is ideally linear for the entire range of input phase differences from -2π to 2π. Due to the delay of the reset path, the linear range is less than 4π. The reduced phase comparison range Δ is given by the following:

$$\Delta = 2\pi \frac{t_{reset}}{T_{CKref}} \tag{4.9}$$

Where t_{reset} is the reset path delay and T_{CKref} is the reference period. Here t_{reset} is determined by the delay of logic gates in the reset path and is not a function of input frequency [46]. Our simulation and calculation indicates that the Δ in our PFD is about 0.18π.

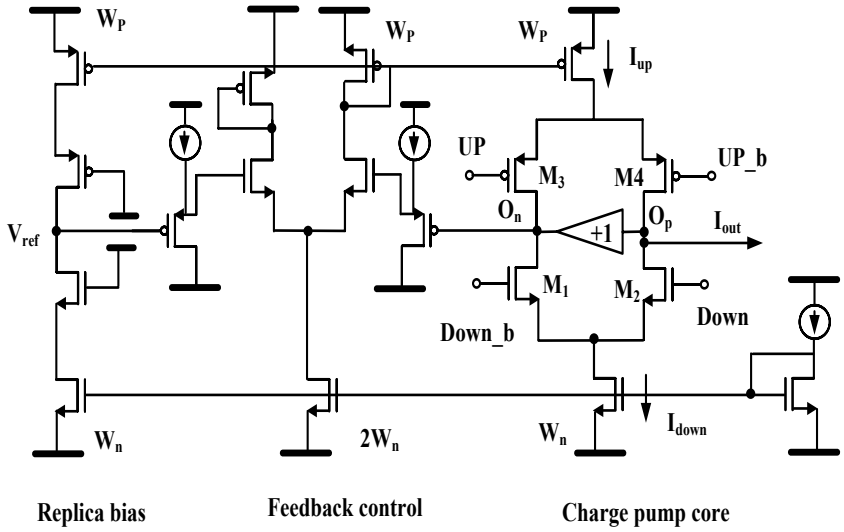


Figure 4.5: Schematic of the charge pump

4.3.2 Charge pump (CP) and the third order loop filter

The charge pump is based on the topology in [16] and shown in Fig. 4.5. In this charge pump the Up and Down current sources are always on and transistors M_1-M_4 are used as switches to steer the current from one branch of the charge pump to the other. The charge pump has a differential architecture. But only a single output node, drives the loop filter. To prevent output node from drifting to the rails when neither of the Up and Down signals is active, a rail to rail unit gain buffer is placed between the two output nodes. This buffer keeps the two output nodes at the same potential and thus reduces the systemic charge pump offset [47]. This architecture is useful when the parasitic capacitance is comparable to the value of the capacitor in the loop filter.

To compensate for the finite output impedance of the Up and Down current sources

and match their currents more precisely over all output voltages, the Up and Down currents are monitored in a replica circuit. A feedback network measures the output voltage (V_{O_P}), and compares it with the voltage of the replica circuit(V_{ref}), and equates the Up and Down currents at every output voltage [47]. The change of the charge pump current I_p corresponds the operational frequency.

The third-order passive loop filter is used as shown in Fig 4.2. The loop filter consists of a resistor R_1 with a series with a capacitor C_1. The CP current source source and the capacitor C_1 form an integrator in the loop and the resistor introduces a stabilizing zero to improve the phase margin and hence improve the transient response of the PLL. However, the resistor causes a ripple of value I_pR_1 on the control voltage at the beginning of each PFD pulse. At the end of the pulse, a ripple of equal value occurs in the opposite direction. This ripple modulates the VCO frequency and introduces excessive jitter in the output. To suppress the ripple induced jitter a small capacitor C_2 is added in parallel with the R_1 and C_1 network. Due to the loop bandwidth is 26MHz, the values for the filter components are quite small and on-chip integration is possible in a small area. From our calculation shown in Fig. 4.3, the phase noise from R_1 is quite small.

4.3.3 Ring Voltage-Controlled Oscillator (R-VCO)

Fig. 4.6 shows the proposed 4-stage ring VCO, which can generate the frequency from 1GHz to 10GHz. Compared with LC VCO, Ring VCO consumes less current and small chip area; Quadrature signals are inherently generated from the 4-stage ring

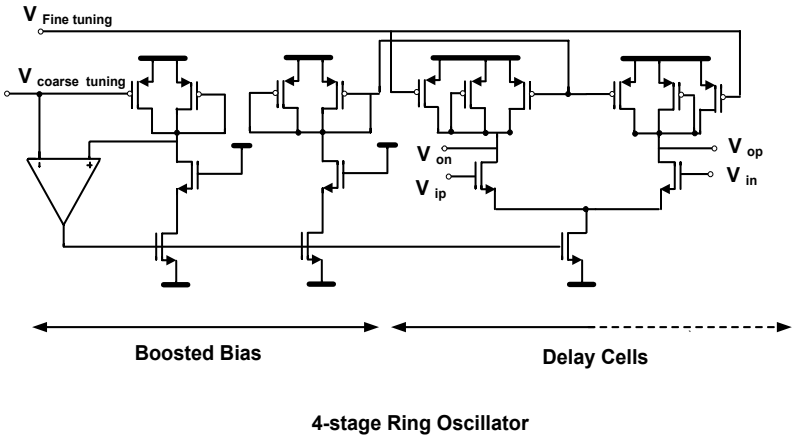


Figure 4.6: The proposed schematic of 4-stage ring VCO

VCO. One drawback of ring-VCO is its poor phase noise characteristic comparing with LC VCO. Due to the sub-carrier frequency spacing consisting of OFDM signals is wide enough, ring VCO can be adopted effectively for multi-band OFDM UWB systems. Our phase noise simulation in Fig. 4.3 shows that ring VCO can satisfy the rms noise requirement of UWB proposal.

An ring oscillator can be realized with any single-ended or differential inverting delay stage. In order to provide precision delays at high resolution and low jitter, our 4-stage ring VCO employed updated Maneatis delay cell, which have high supply noise immunity while being able to operate at low supply voltages.

The Maneatis delay cell usually consists an NMOS source-coupled pair with symmetric load elements and a dynamically-biased simple NMOS current source [48]. The coupling input is formed from an additional source-coupled pair sharing the same loads and current source. The bias voltage of the simple NMOS current source is continuously adjusted in order to provide a bias current that is independent of

supply and substrate voltages. The load elements are composed of a diode-connected PMOS in shunt with an equally sized biased PMOS device. They are symmetric load because their I-V characteristics are symmetric about the center of the voltage swing. The control voltage voltage (V_{ctrl}) is bias voltage for the PMOS device. It is used to generate the bias voltage for the NMOS current source and provides control over the delay of the buffer stage [48].

In our design, the updated Maneatis delay cell have been used. The control voltage voltage (V_{ctrl}) have been used as coarse tuning for ring VCO for differently operational center frequency, which cover frequency from 1GHz to 10.3GHz. A small sized biased PMOS device are also parallel with the diode-connected PMOS as fine tuning shown in Fig. 4.6, which covers frequency about 200MHz.

The current source bias shown in Fig. 4.6 is self-boosted biased circuit, which includes an additional opamp to reduce the supply sensitivity. When the PMOS devices of the delay cell are controlled and an opamp feedback loop is introduced in the bias network, the amplifier detects changes in the replica bias due to supply variations and adjusts the NMOS current sources. This maintains a constant output siwng and bias current in the delay cells despite the finite impedance of the tail current source [41, 49].

4.3.4 Injection-locked frequency divider

In this PLL, The differential injection locked frequency dividers (D-ILFD),shown in Fig. 4.7 are used as the frequency divider. The locking range and phase noise of

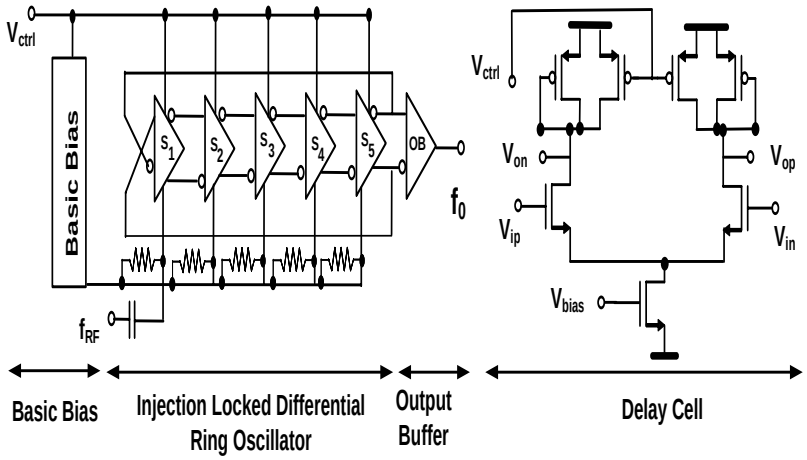


Figure 4.7: Circuit schematic diagram of the D-ILFD used in prototype design

D-ILFD have been discussed in details in chapter 3.

4.4 Experimental Results

The Fig. 4.8 shows the coarse frequency and power characteristics of the ring VCO varying the control voltage with the fixed fine tuning voltage set to 0V. The coarse frequency tuning range is from 1GHz to 10.3GHz and power combustion for core ring VCO is from 3.5 mA to 17.25mA. The fine frequency tuning range is about 200MHz.

The measurement results shown Fig. 4.9 for the injection locked ring oscillator frequency divider indicate that the locking range of all harmonics decreases with increasing harmonics at the low harmonics and levels off to a fixed value at large harmonic numbers.

In Table 4.1 we compare recently published results for UWB PLL with our designs. Our results indicated that we have lowest power consumption, wide lock range and

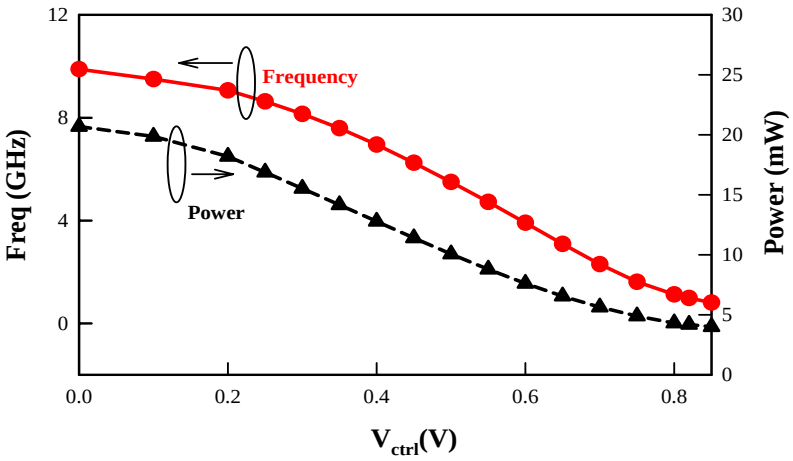


Figure 4.8: The measured oscillation frequency and power consumption with the control voltage

smaller chip area. The micrograph of the chips fabricated in 0.13 μm COMS are shonw in Fig. 4.10.

Parameters	LCVCO [39]	Ring VCO [40]	Our Design
Tech. (nm) CMOS	180	90	130
Voltage Supply (V)	1.8	1.5	1.2
Output frequency (GHz)	6.33-8.976	3.432-4.488 6.60-9.240	1.0-10.3
Channel spacing (MHz)	528	528	528
Core Area (mm^2)	0.7×1.1	0.15×0.6	0.21×0.34
Integrated RMS noise (^{0})	1.5	< 4	< 3
VCO (mA)	8		3.5 - 17.25
Divider (mA)	17.5		2.5
PFD+CP+LPF (mA)	2.8		2.1
Output buffer (mA)	15		4.9
Total PLL core power (mA)	32.2	30 - 37	8.1 - 21.85

Table 4.1: Comparison of PLL performance with recently published designs

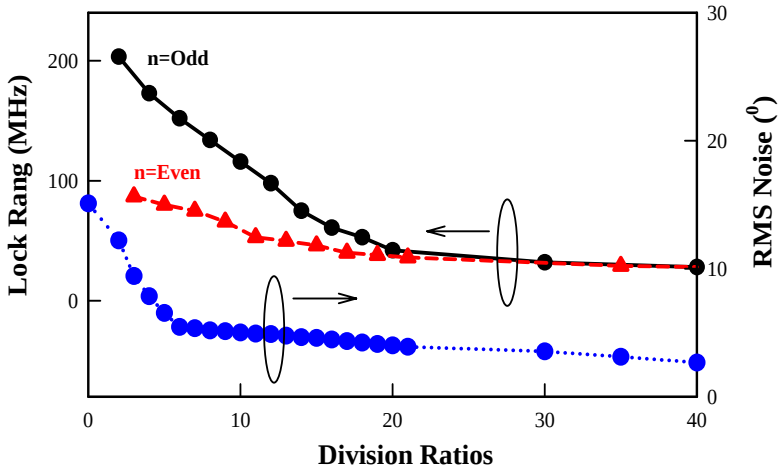


Figure 4.9: The measured lock rang and integrated RMS phase noise with division ratios for D-ILFD

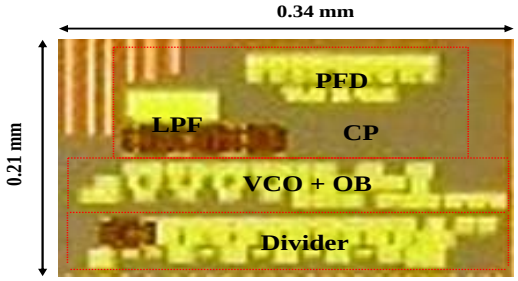


Figure 4.10: PLL Micrograph of the chip fabricated in 130 μm COMS

4.5 Conclusions

In this paper a wide lock range, low power PLL based ring VCO and ILFD has been designed for an UWB radio. The ring VCO based on the updated Maneatis delay cell, which cover from 1GHz to 10.3GHz. The injection-locked frequency divider, which can lock to all harmonics have been used. Experimental results indicate that integrated phase noise is below a 3^0 and power consumption is only 8.1 mA to 21.85 mA for whole frequency bands.

Chapter 5

Crosstalk Noise Coupling in 3D ICs

5.1 Introduction

Over the years, in 2D planar ICs a number of techniques for reducing crosstalk via the substrate has been developed. Guard rings around a noise source provide a low resistance path to AC ground and minimize the amount of noise injected into the substrate. Well-designed guard rings can suppress the amount of coupling at frequencies below 1GHz, but have proven to be quite ineffective above 3GHz [50]. Deep trench technologies have shown isolation that is better than 40dB for 0.5-20GHz, but result in fairly complex processes [51]. Patterned ground shields under inductors improves isolation for RF circuits by an additional 25dB [52]. Other noise isolation technologies that perform well at frequencies below 1GHz, include triple well, on-chip

decoupling and buried oxide. The isolation frequency performance can be increased to approximated 10GHz by using SOI technology with a high resistivity substrate [53].

In this chapter, we present and verify noise isolation in 3D ICs by using separate tiers and Faraday cages (FC). The design and implementation are based on a 0.18μm fully-depleted silicon-on-insulator (FDSOI) technology shown in Fig. 5.1 [2, 4]. The three active tiers, with three metal layers each, are first individually fabricated using a FDSOI CMOS process. The resistivity of each tier is about 2000 Ohms·cm. The handling wafers of the top two tiers are then removed and these tiers are flipped over and integrated with the bottom tier by using intertier vias. Faraday cages have traditionally been used to block-out external EM fields. We evaluate the efficacy of using such cages in 3D ICs. It is critical to note that Faraday cages are not possible in traditional 2D ICs because metal layers are only available above the active devices. In the MITLL 3D IC technology FCs can be created by using metal layers in any two tiers and using the inter-tier vias to complete the sides of the Faraday cage.

The chapter is organized as follows. In Section II we describe the test chip and the experimental and simulation setup for the different coupling conditions in detail. Section 5.3 provides measurement and simulation results. Section 5.4 presents a lumped model of the coupling effects based on physical parameters, simulations and calculations. Section 5.5 provides some concluding remarks.

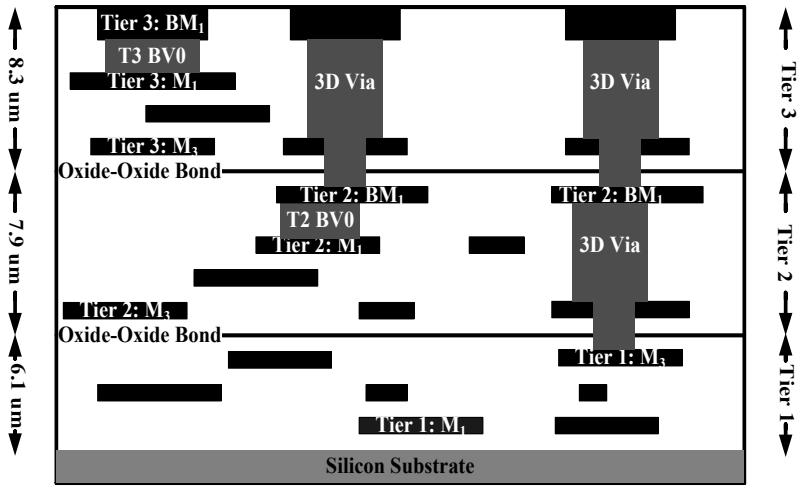


Figure 5.1: A 3-tier 3D-IC layout including layer thickness information [2, 4]

5.2 Experimental & Simulation Setup

3D ICs allow for significant digital signal processing to be available in close proximity to analog/RF circuits which is of great interest for future programmable and cognitive radios. However, the close proximity also introduces the potential problem of noise coupling. In the next subsections we explore an experimental setup that confirms the coupling problem and also identify techniques that are valuable for their mitigation.

5.2.1 Experimental Setup for Inductors

Fig. 5.2 shows the microphotograph for a 5mm $\times$ 2.5mm test chip that was used to investigate noise coupling in 3D ICs. Test structures without Faraday cages on tier 3, displayed in Fig. 5.2, are used as a reference for test structures with Faraday cages on the same tier. The transmitter (TX) and receiver (RX) sections in this experiment use identical inductors. The transmitter consisted of four inductors at

different distances from the receiver. The distances between transmitter inductor centers and receiver inductor centers are 710μm, 510μm, 435μm and 430μm. The thickness of metal layers 1-3 on the tier 3 are all 630nm. All inductors are based on a square spiral structure where metal 3 is used to form the coil and metal 2 is used for the underpass. Inductors for test structures in Fig. 5.2(a) have 3.25 turns with an inner diameter of 88μm, and the width and the spacing of the spiral are 10μm and 4μm respectively. The inductors are configured as a one-port device with the other port connected to ground. The ground ring serves as a current return path, and is at a fixed distance of 100μm away from the outer diameter of the inductor.

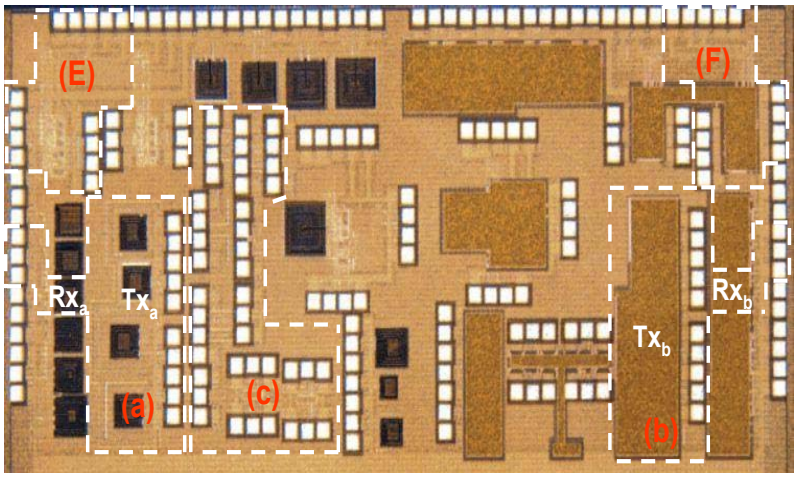


Figure 5.2: Micrograph of test die (a) test structures without Faraday cage on tier 3 (b) test structures with Faraday cage on tier 3 (c) de-embedding structures (e) low noise amplifier without Faraday cage (F) low noise amplifier with Faraday cage

The test structures with Faraday cages (FC) on tier 3 are shown in Fig. 5.2(b). The test structures for the TX and RX are identical except for the Faraday cage. The two set of structures, with and without Faraday cage, are on opposite sides of the chip. We ensure that the distance between the TX center and RX center remained

unchanged with and without the FC. For this experiment, the FC consists of the back metal (BM_1) on tier 3, the back metal (BM_1) on tier 2 and intertier vias between tier 3 and tier 2. It is important to note that creating this FC does not involve any additional fabrication steps. The two different kinds of Faraday cages are shown in Fig. 5.3.

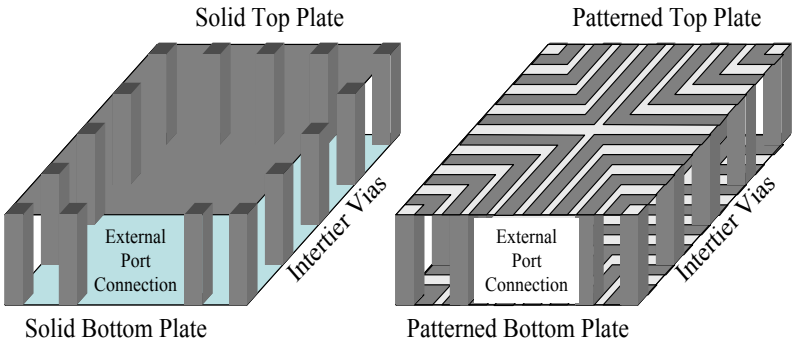


Figure 5.3: Cross sectional view of Faraday cages; Left: solid top and bottom layers; Right: patterned top and bottom layers

For our experiment, we use the measured S_{21} as the figure of merit for isolation. Measurements were done from 50MHz to 10GHz with the help of an Agilent 8719Es two-port network analyzer for the test structures shown in Fig. 5.2(a) and 2(b). The network analyzer is configured to perform broadband measurements. Probe calibration was done using CASCADE's 101-190 substrate using a Short-Open-Load-Thru technique. De-embedding structures shown in Fig. 5.2(c) were used to eliminate the influence of the transition region between the probe, probe contact and the device under test.

5.2.2 Electromagnetic Simulation Methodology for Inductors

Not all test cases could be verified via the test setup above. Therefore, to complete the picture we supplement the measurements from the experimental setup with full-wave electromagnetic (EM) simulations. EM simulations were validated via measurements and will be used to guide future isolation structure design. Ansoft HFSS was used for our EM simulations [54].

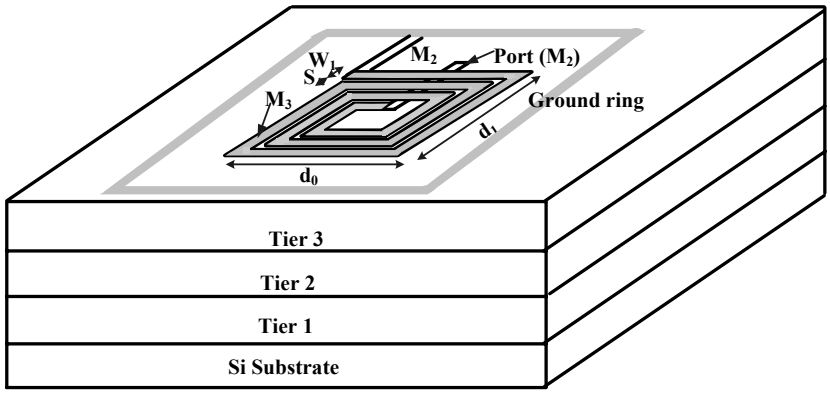


Figure 5.4: Cross-sectional view of a spiral inductor on tier 3

The solid model used within HFSS for the FDSOI CMOS 3D IC is shown in Fig. 5.4. The details of the structures used to simulate noise coupling correspond to the test structures shown in Fig. 5.2(a) and (b). Two other simulation structures are also discussed; one is that of test inductors on the different tiers (tier 3 and tier 2) with/without Faraday cages; another one is the same structure as shown in Fig. 5.2 (b) except that the Faraday cage uses patterned top and bottom plates. All inductor design parameters are exactly the same as those shown in Fig. 5.2(a) and (b).

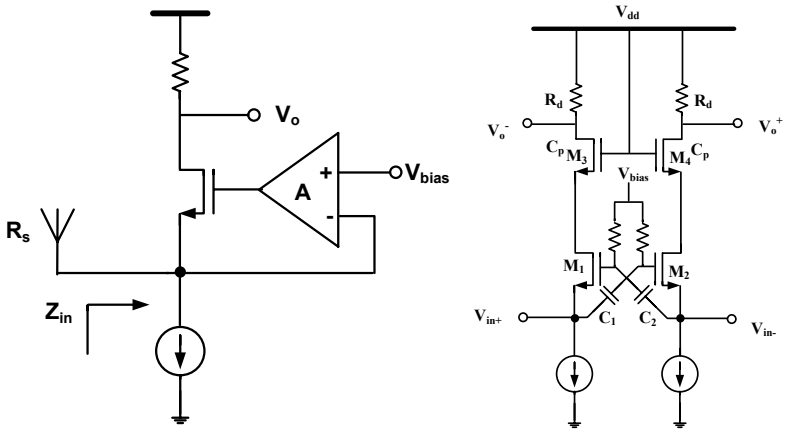
5.2.3 Experimental Setup for Inductorless Low Noise Amplifier (LNA)

For the second set of experiments the Faraday cage for the noise coupling problem for mixed digital-RF circuits was directly evaluated by a LNA on the test chip. The LNA is usually the first active stage in RF receivers and amplifies the input signal from the antenna and suppresses noise contributions from subsequent stages. Therefore, the LNA usually sets the noise performance for the entire RF system.

The LNA design, shown in Fig. 5.5, included on this chip was a broadband g_m-boosted common gate circuit [3]. For an input impedance equal to $1/g_m$ the noise figure is given by $F_{CG-LNA} = 1+\gamma/(2\alpha)$, where the additional factor of $1/2$ is a result of the g_m-boosted technique. Fig. 5.5(a) depicts the topology of the proposed g_m-boosted CG-LNA. Capacitor cross-coupled CG LNA can be realized as one possible implementation of a g_m-boosted CG LNA with inverting gain (A) equal to 1, proposed in Fig. 5.5(b). The LNA design uses an external balun to transform the single ended antenna signal to differential signals. The Faraday cage designs for the LNA are similar to those designed for the inductors. The test structures for LNAs with/without Faraday cages in tier 3 are shown in Fig. 5.2(E) and (F).

5.3 Results and Discussions

Fig. 5.6 shows measured and simulation results for the reference structures in Fig. 5.2(a). The graph plots the measured S_{21} with the probes in the air and measured



(a) (b)

Figure 5.5: (a) The G_m-boosted common-gate low noise amplifier (b) Capacitor cross-coupled common-gate low noise amplifier [3]

and simulated values of S_{21} at different separations between the two structures. The separation between the structures is varied from 430μm to 710μm. We note a good matching between measurement and simulations. Additionally, we note that increasing the distance between TX and RX by about 200μm reduces the crosstalk only 5dB at 1GHz. Clearly, distance alone is not the solution.

Fig. 5.7 shows the measurement and simulation results for the structures in Fig. 5.2(b). We note that that magnitude of crosstalk is much lower (on average 30dB) than shown in Fig. 5.6. However, these results include the effects of the metal connection between the inductors and the pads that were used for testing purposes but were outside the Faraday cages, which unfortunately also contribute to crosstalk. In fact, the metal connection outside the Faraday cage is the primary contributor to the increase in crosstalk with frequency. Unfortunately, it is not possible to make measurements without these interconnections. We note that there is a good agreement

with measurement and simulations at higher frequencies. The discrepancy at lower frequencies (below 2.5GHz) can be attributed to the crosstalk between the probes in the air. We also note that, unlike the results in Fig. 5.6, spacing between the structures has very limited impact on the crosstalk.

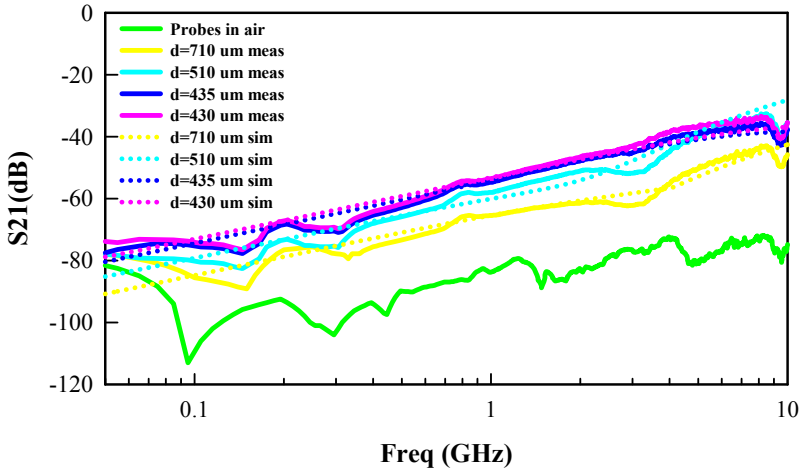


Figure 5.6: Measurement and simulation results without Faraday cage [Fig. **??**(a)]

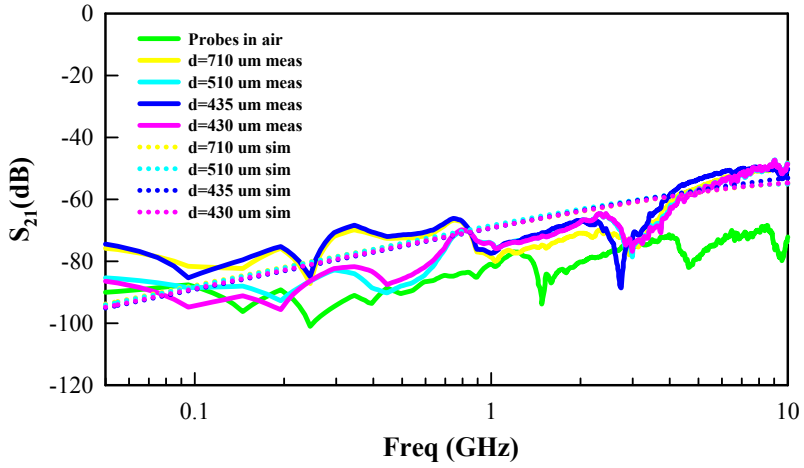


Figure 5.7: Measurement and simulation results with Faraday cage [Fig. **??**(b)]

As we are unable to eliminate the connection to the outside for our FC measure-

ments and we have validated the close agreement between measurement and simulation results, we can now use HFSS as a tool to show the real impact of these cages. Fig. 5.8 shows the simulation results for inductors that are similar to the ones shown in Fig. 5.2(b) but are completely enclosed within a Faraday cage. In comparison to the measurement results shown in Fig. 5.6 the crosstalk is reduced by an additional 100dB, which is the highest value ever reported. The slight increase in crosstalk with frequency is due to a combination of numerical precision and port to port coupling during simulations.

A solid Faraday cage provides excellent isolation, however, the image current induced by the magnetic field in the solid surface of the Faraday cage flows in opposite direction and will reduce the total inductance and Q (i.e., Eddy current effect). Orthogonally slotting the top and bottom plates can be used to eliminate this effect without reducing the isolation properties [52]. The slots, which should be smaller than the operation wavelength, act as an open circuit to the induced current. To evaluate this property we pattern the top and bottom plates of the Faraday cages while maintaining everything else. Simulations for patterned FCs show a reduction in the isolation by 10dB (for 430μm separation) as shown in Fig. 5.8. Note, this is insignificant in comparison to the absolute values. However, both the inductance and inductance Q increase by about 40% at 5GHz.

Next, we evaluate tier-to-tier noise coupling with and without Faraday cages using the same structures shown in Fig. 5.2(a) and 5.2(b). For our first experiment, the TX and RX are placed without Faraday cages and are separated 430μm. The receiver is kept on tier 3 while one transmitter each are placed on tier 2 and tier 3. The

simulation results included in Fig. 5.9, show that using different tiers increases the isolation by an additional 10dB. For the second experiment, we repeat the procedure done in the previous experiment, but this time we include one of either the TX or RX in a Faraday cage. Here we see that using separate tiers increases isolation by 20dB. However, more importantly, using Faraday cages improves isolation by over 75dB.

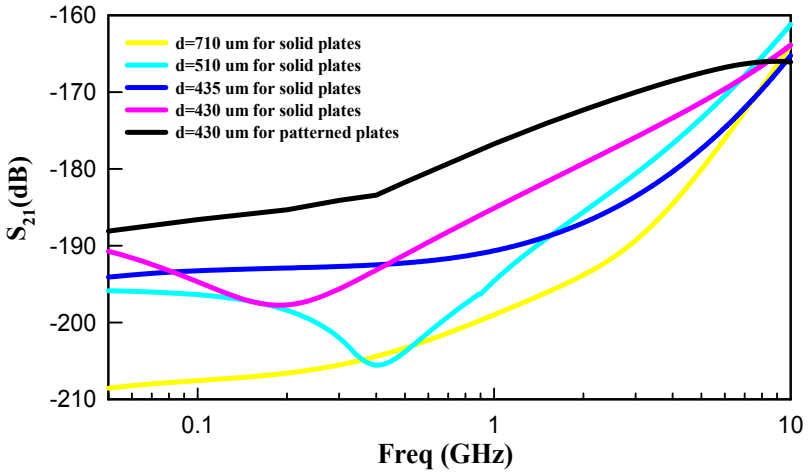


Figure 5.8: The simulation performance of TX and RX both with Faraday cage

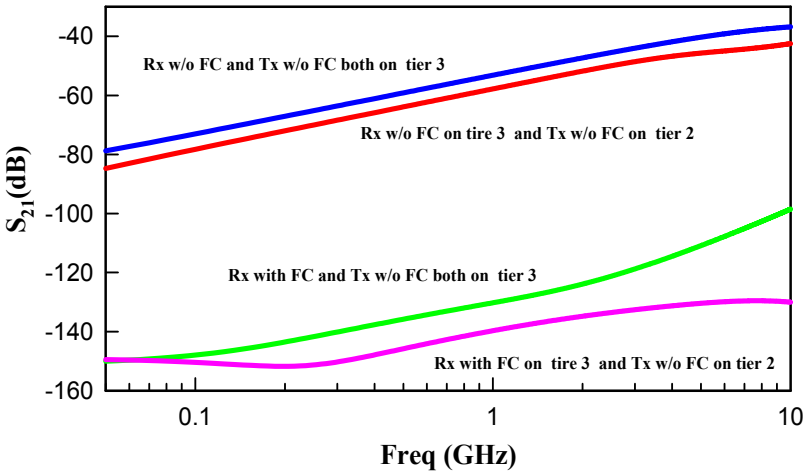


Figure 5.9: Simulation results for different structures (d= 430μm)

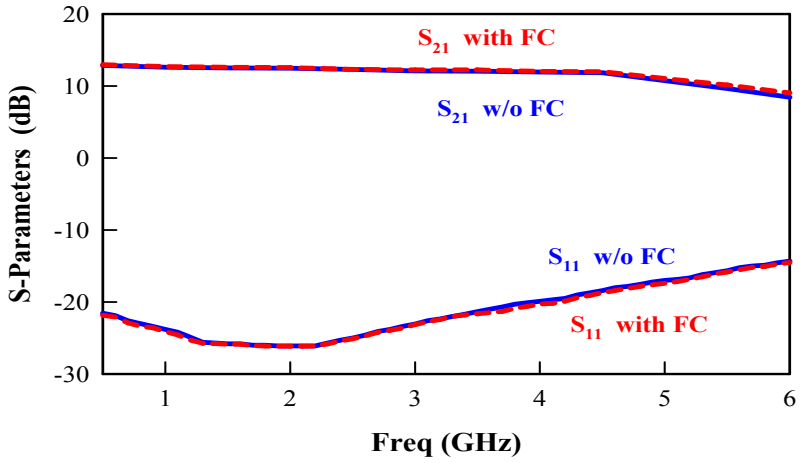


Figure 5.10: Measured S parameters of capacitor cross-couple common-gate LNA with and w/o Faraday cage

Fig. 5.10 shows the measured LNA conversion gain (S_{21}) from 0.5GHz to 6GHz. A fairly flat power conversion gain of 12 dB over0.5GHz to 5.4GHz for both with Faraday cage and without Faraday cage. The measured input reflection coefficients (S_{11}) for both designs are also shown in Fig. 5.10. The S_{11} is better than -13dB from 1GHz to 6GHz for both designs. The S-parameters for both designs are almost the same, which indicates the Faraday cage do not affect the S-parameters of LNA. The IIP3 for both designs versus the input frequency are shown in Fig. 5.11. The results of IIP3 for both designs shows that the Faraday cage do not impact on IIP3 of inductorless LNA. The experimentally measured performance for our LNA with/without Faraday cage have been summarized in Table 5.1.

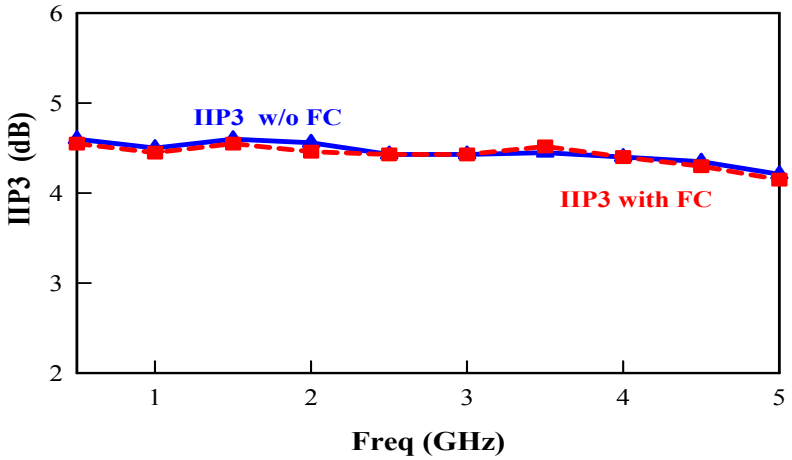


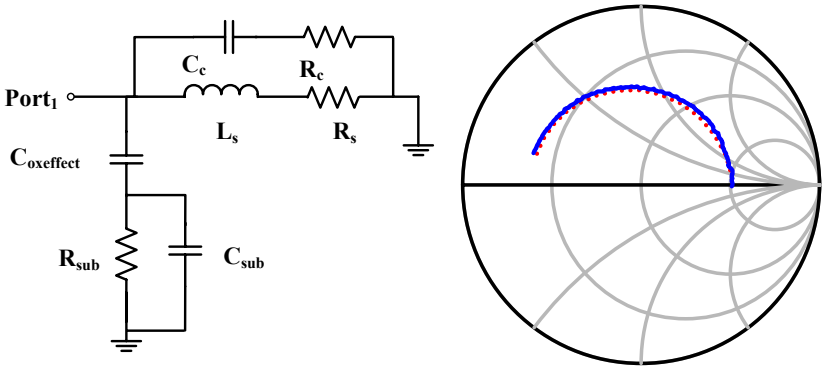
Figure 5.11: Measured IIP3 of capacitor cross-couple common-gate LNA with and w/o Faraday cage

Specification	LNA without FC	LNA with FC
Technology	$0.18\mu m$	$0.18\mu m$
S_{11}	$\leq -13dB$	$\leq -13dB$
Bandwidth	$1-5.4GHz$	$1-5.4GHz$
IIP3	$+4.3dBm$	$+4.3dBm$
Power gain (S_{21})	$12dB$	$12dB$
Power dissipation	$5.4mW$	$5.4mW$

Table 5.1: Summary of measurement results for wideband LNA with/without Faraday cages

5.4 Lumped Modeling of Noise Coupling Effects

Several equivalent circuit models have been developed to model crosstalk in integrated circuits [55–58]. In order to accurately understand the physical behavior of the Faraday cage, Fig. 5.12(a) shows a simplified equivalent circuit used for modeling each single spiral inductor [59]. The spiral inductor structure is represented by an inductance L_s, a series resistance R_s, the coupling capacitance C_c and resistance R_c. The parallel parasitics result from a combination of oxide capacitance $C_{oxeffect}$ representing the capacitance value of the oxide layer in each tier between the inductor and the top of silicon substrate. The substrate parasitics are represented by R_{sub} and C_{sub}. The value of each of the elements in the equivalent circuit is optimized to match the measured results. As seen in Fig. 5.12(b) there is there is extremely good matching between measured and modeled parameters.



(a) (b)

Figure 5.12: (a) Equivalent circuit model for inductors from Fig 2; (b) Modeled data (dotted line) and measurement data (solid line) from 1GHz to 10GHz

To evaluate the coupling effects between two inductors with/without Faraday cages, a simple lumped element equivalent circuit is shown in Fig. 5.13. This noise

coupling effect (crosstalk) is modeled by an RC path ($R_{cp}//C_{cp}$). Expressions of equivalent elements R_{cp} and C_{cp} have been derived for inductors without Faraday cage in [56, 60, 61] and are included here for completeness.

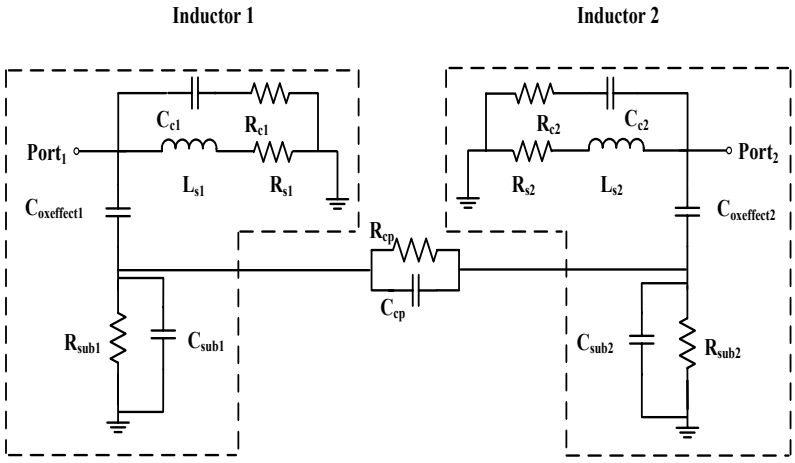


Figure 5.13: The lumped equivalent circuit for the crosstalk between two inductors

$$R_{cp} = [K_1 \frac{\pi \varepsilon_0 \sigma_{si}}{4ln[\frac{\pi(d-W)}{W+t} + 1]} W]^{-1} \tag{5.1}$$

$$C_{cp} = [K_1 \frac{\pi \varepsilon_0 (\varepsilon_{si} + 1)}{4ln[\frac{\pi(d-W)}{W+t} + 1]} W] \tag{5.2}$$

Here K_1 is the fringing factor. For our test structures without a Faraday cage K_1 is equal to 1.37 for d= 430μm. W is the average outer diameter of the inductor and t is the thickness of conductors. Fig. 5.14 shows very good agreement between the results of crosstalk simulation using the simple equivalent circuit presented above and the measurements for the test structure (d= 430μm) listed in Fig. 5.2(a) without FC.

When two inductors are close to each other, their electromagnetic field patterns

interact, a portion of the signal present at one inductor will be transferred to the other one by coupling through $C_{oxeffect}$. Simulations for structures with Faraday cages indicated that oxide capacitance $C_{oxeffect}$ can be treated as an effective coupling factor for the Faraday cage. For the receiver with Faraday cage and transmitter without Faraday cage, the $C_{oxeffect}$ for the receiver part is about $1/100^{th}$ of that for the receiver without a Faraday cage. The fringing factor K_1 is reduced to one third. For both receivers and transmitters with Faraday cages, the $C_{oxeffect}$ for both the receiver and the transmitter is $1/1000^{th}$ of that for receiver and transmitter without Faraday cages. The fringing factor K_1 is reduced to one tenth. This simple lumped model can be used to accurately predict the impact of coupling with and without Faraday cages by just modifying the value of $C_{oxeffect}$ as shown in Fig. 5.14.

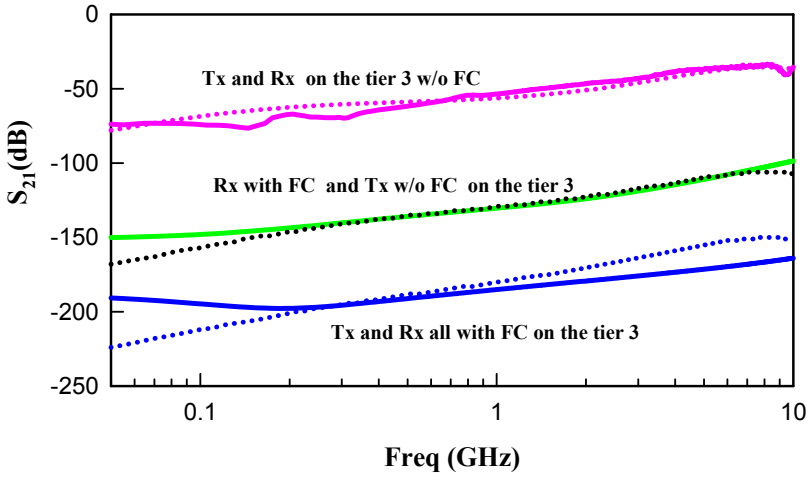


Figure 5.14: Lumped circuit simulation results for different structures (d= 430μm). Good agreement between lumped circuit simulation data, measured data and HFSS simulation data. The doted line is lumped circuit simulation data

5.5 Conclusions

In this chapter, we model and measure noise coupling in 3D ICs. We also develop a new technology for reducing this crosstalk. To validate our model and our design techniques we used a combination of simulation and measurement results from inductors (implemented on different tiers) with and without Faraday cages. We use the structure without a Faraday cage as our reference. Measurement and simulation results show that isolating either the TX or RX alone reduces the noise coupling by 75dB. However, enclosing both the TX and RX in Faraday cages reduces the noise coupling by an additional 25dB. We also developed and verified a simplified lumped equivalent circuit model for noise coupling. In 3D ICs the use of Faraday cages, combined with placing the RF/analog circuits and digital circuits on separate tiers, results in extremely good noise isolation. Measurement results also indicate that the Faraday cages have no effect on S-parameters and linearity of inductorless RF circuits.This allows us to fully integrate system that have both sensitive analog/RF circuits and require significant digital signal processing. Additionally, it is well known that noise isolation decreases at higher frequencies, therefore 3D ICs using Faraday cages may be the preferred process technology for high performance mixed-signal systems in the future.

Chapter 6

Conclusions and Research Contributions

6.1 Summary

In this thesis we introduced, analyzed and verified via simulations and measurements from prototype circuits, two advanced circuit architectures for wireless integrated systems. In the first part of this thesis the design of a inductorless receiver, which include LNA, Mixer and frequency synthesizer are presented. In Chapter 2 we introduced a inductorless wideband RF frontend from 1GHz to 10GHz. To validate our design methodology two receiver RF frontends were designed; a traditional inductor based design and a inductorless design. A common-gate LNA transconductor is followed by a capacitive peaking LNA-mixer pair (CPLM). Experimental measurement results show that a CPLM with the same bandwidth has better linearity, comparable noise

figure and uses only 17% more power. The silicon area for the inductorless LNA and I/Q mixers is roughly 22% of traditional inductor based designs showing area savings and improved portability. In Chapter 3 we developed theory for the lock range and phase noise for both differential and single-ended ILFDs. We showed that both D-ILFDs and S-ILFDs can be made to lock to even and odd harmonics. Measurement results for the D-ILFD and S-ILFD show that the lock range of all harmonics decreases with increasing n at the beginning and then levels off to a fixed level. Measured integrated phase noise for D-ILFD and S-ILFD also show that it decreases with increasing division ratio. Ring oscillator based D-ILFDs and S-ILFDs operate at low power, consume small area, have large tuning range, and can be made to operate at low phase noise making them particularly well suited for wideband PLLs. We provided measurement results for division ratios up to 40 for D-ILFDs (corresponding to $f_{RF} = 10.56$GHz) and up to 45 (corresponding to $f_{RF} = 9.9$GHz) for S-ILFDs respectively showing their high frequency potential. In Chapter 4 a wide lock range, low power PLL based ring VCO and ILFD has been designed for UWB radio. The ring VCO based on the updated Maneatis delay cell, which covers the frequency range from 1GHz to 10.3GHz. The injection-locked frequency divider, which can lock to all harmonics have been used. Experimental results indicate that integrated phase noise is below a 3^0 and power consumption is only 8.1 mA to 21.85 mA for whole frequency bands.

In the second part of this thesis we model and measure noise coupling in 3D ICs. We also develop a new technology for reducing this crosstalk. To validate our model and our design techniques we used a combination of simulation and measurement

results from inductors (implemented on different tiers) with and without Faraday cages. We use the structure without a Faraday cage as our reference. Measurement and simulation results show that isolating either the TX or RX alone reduces the noise coupling by 75dB. However, enclosing both the TX and RX in Faraday cages reduces the noise coupling by an additional 25dB. We also developed and verified a simplified lumped equivalent circuit model for noise coupling. In 3D ICs the use of Faraday cages, combined with placing the RF/analog circuits and digital circuits on separate tiers, results in extremely good noise isolation. Measurement results also indicate that the Faraday cages have no effect on S-parameters and linearity of inductorless RF circuits.This allows us to fully integrate system that have both sensitive analog/RF circuits and require significant digital signal processing. Additionally, it is well known that noise isolation decreases at higher frequencies, therefore 3D ICs using Faraday cages may be the preferred process technology for high performance mixed-signal systems in the future.

6.2 Research Contributions

In this thesis the research has focused on advanced architectures for the next generation of wireless integrated circuits. Several interesting topologies have been developed. The research presented here has laid a solid foundation on to which further research will be built. The research contributions include: a wideband inductorless RF frontend, which includes a low noise amplifier, mixer; theory for the lock range and phase noise for both differential and single-ended ILFDs have been developed; a wide lock

range, low power PLL based ring VCO and ILFD has been designed for UWB radio; model and measure noise coupling in 3D ICs have been shown. Each of these research contributions are summarized in the following paragraphs.

–**Inductorless Design of Wireless CMOS Frontends** Prior to this research the traditional architecture of wireless integrated circuits have been using bandpass resonant circuits and broadband transmission line circuits to extend the operational frequencies. Both on-chip inductors and integrated transmission lines tend to consume significant chip area. Results of our new design, which is a common-gate LNA transconductor followed by a capacitive peaking LNA-mixer pair (CPLM), indicate that CPLM with the same bandwidth has better linearity, comparable noise figure and uses only 17% more power. The silicon area for the CPLM is roughly 22% of traditional inductor based designs showing area savings and improved portability.

–**All division ratio injection-locked frequency dividers based on ring oscillators** Frequency dividers are an essential component of PLLs and are required to provide a range of division ratios. Traditionally, such dividers have been implemented as a string of wideband static frequency dividers based on flip flops, with the first divide-by-two usually implemented utilizing current-mode logic to obtain suitable high frequency operation. The power consumption of a static divider increases proportionately with operating frequency due to the complete charging and discharging of capacitances in each cycle. New theory and prototype designs for injection-locked frequency dividers based on differential ring oscillators (D-ILFD) and single-ended ring oscillators (S-ILFD), which can be locked to all harmonics (i.e., *even* and *odd*), have been displayed in this thesis. Analytical models for the lock range and phase

noise for all harmonics for both topologies have been presented.

–**An inductorless, ring-oscillator based, wide lock range and low power PLL** A novel PLL based on ILFD and ring oscillator VCO was proposed for inductorless architectures of wireless integrated circuits. Output frequency coverage is from 1GHz to 10GHz, which is suitable for not only the UWB specification but also for other wideband standards. Total power consumption for the PLL core is extremely low due to the use of a injection-locked frequency divider. The integrated RMS phase noise is below 3 degrees, which easily satisfies the requirements for the MBOA-UWB standard.

–**Modeling, measurement and mitigation of crosstalk noise coupling in 3D-ICs** 3D ICs provide an attractive alternative to traditional two dimensional integrated circuits (2D ICs). Over the years, in 2D planar ICs a number of techniques for reducing crosstalk via the substrate has been developed. In this thesis it is the first time to describe reducing crosstalk in 3D ICs by using Faraday cages. Our results show that the crosstalk between the transmitter and receiver reduces by about 75dB up to 10GHz by using a Faraday cage in combination with tier-to-tier isolation, which is one of best performance reported so far. A lumped equivalent model for crosstalk with and without a Faraday cage have been reported. Measurement results also indicate that Faraday cages have no effect on S-parameters and linearity of inductorless RF circuits.

Bibliography

[1] *International Technology Roadmap for Semiconductors*, Available: http://www.itrs.net.

[2] "MITLL low-power FDSOI CMOS process: Design guide," 2006.

[3] D. J. Allstot, X.Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," *RFIC Sym.*, pp. 97–100, 2004.

[4] C. K. et.al., "3D integration for integrated circuits and advanced focal planes," 2007.

[5] B. Krenick, "personal communication," 2006.

[6] A. Bevilacqua and A.Nikejad, "An UWB LNA for 3.1 to 10.6GHz wireless receivers," *IEEE JSSC*, vol. 39, pp. 2259–2268, Aug. 2004.

[7] Q. Li and Y. P. Zhang, "An inductorless LNA with noise cancellation for UWB receiver front-end," *IEEE ASSCC*, 2006.

[8] B. G. Perumana, J. Zhan, S. Taylor, and J. Laskar, "A 0.5-6GHz improved linearity, resistive feedback 90-nm CMOS LNA," *IEEE A-SSCC*, pp. 263–266, June 2006.

[9] M.Tsai and H. Wang, "A 0.3-25 GHz UWB mixer using commercial 0.18μm CMOS technology," *IEEE MWCL*, pp. 522–524, Nov 2004.

[10] A. Safarian, A. Yazdi, and P. Heydari, "Design and analysis of an ultrawide-band distributed CMOS mixer," *IEEE T. on VLSI Systems*, pp. 618–629, May 2005.

[11] B. Jung, S. B., and R. Harjani, "Power optimized LC VCO and mixer co-design," *IEEE ISCAS*, May 2005.

[12] R. Harjani and L. Cai, "Inductorless design of wireless CMOS frontends," *IEEE ASICON*, pp. 1367–1370, Oct. 2007.

[13] S. Blaakmeer, E. Klumperink, d. Leenaerts, and B. Nauta, "A wideband balun LNA I/Q mixer combination in 65nm CMOS," *IEEE ISSCC*, pp. 326–327, Feb 2008.

[14] S. Lee, J. Bergervoet, K. Harish, and G. Weide, "A broadband receiver chain in 65nm CMOS," *IEEE ISSCC*, pp. 418–419, Feb 2007.

[15] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw Hill, 2002.

[16] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits(2th edition)*. New York: Cambridge University Press, 2004.

[17] S. A. Maas, *Nonlinear Microwave and RF Circuits*, 2nd ed. Artech House, 2003.

[18] R. Harjani, "A 455mb/s MR preamplifier design in a 0.8μm CMOS process," *IEEE JSSC*, pp. 862–872, June 2001.

[19] J. Harvey and R. Harjani, "An integrated quarature mixer with improved image rejection at low voltage," *14th International Conference on VLSI Design*, pp. 269–273, January 2001.

[20] ——, "Analysis and desing of an integrated quadrature mixer with improved noise, gain and image rejection," *ISCAS*, vol. 4, pp. 786–789, May 2001.

[21] L. A. MacEachern and T. Manku, "A charge-injection method for Gilbert cell biasing," *IEEE CCECE/CCGEI*, vol. 1, pp. 365–368, May 1998.

[22] H. Sjoland, A. K. Sanjaani, and A. Abidi, "A merged CMOS LNA and mixer for a WCDMA receiver," *IEEE JSSC*, vol. 38, pp. 1045–1050, June 2003.

[23] S. Shekhar, J. S. Walling, and D. J. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE JSSC*, vol. 41, pp. 2424–2439, November 2006.

[24] A. Ismail and A. A. Abidi, "A 3-10 GHz LNA with wideband LC-ladder matching network," *IEEE JSSC*, vol. 39, pp. 2269–2277, Dec. 2004.

[25] B. Razavi, "A UWB CMOS transceiver," *IEEE JSSC*, vol. 40, pp. 2555–2561, December 2005.

[26] A. Motieifar, Z. Pour, and L. Shafai, "An (UWB) mixer with 0.18μm RF CMOS technology," *IEEE CCECE/CCGEI*, pp. 697–700, May 2006.

[27] M. Acar and B. Nauta, "A wide-band CMOS injection-locked frequency divider," *IEEE RFIC*, pp. 211–214, June 2004.

[28] W. Z. Chen and C. L. Kuo, "18GHz and 7GHz superharmonic injection-locked dividers in $0.25\mu m$ CMOS," *ESSCIRC*, pp. 89–92, June 2002.

[29] H. Wu and A. Hajimiri, "A 19GHz 0.5mw $0.35\mu m$ CMOS frequency divider with shunt-peaking," *IEEE ISSCC*, Feb. 2001.

[30] L. Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Transactions on Circuits and Systems II*, vol. 49, May 2002.

[31] B. Mesgarzadeh and A. Alvandpour, "First-harmonic injection-locked ring oscillators," *IEEE Custom Integrated Circuits Conference*, pp. 733–736, Sept. 2006.

[32] F. Huang, D. Lin, H. Wang, and Y. Chan, "20GHz CMOS injection-locked frequency divider with variable division ratio," *IEEE RFIC*, pp. 469–472, June 2005.

[33] H. Tong, S. Cheng, and J. Martinez, "An injection-locked frequency divider with multiple highly nonlinear injection stages and large division ratios," *IEEE Trans. on Circuits and Systems*, pp. 313–317, April 2007.

[34] R. J. Betancourt-Zamora, S. Verma, and T. H. Lee, "1GHz and 2.8GHz CMOS injection-locked ring oscillator prescalers," *IEEE Symposium on VLSI Circuits*, pp. 47–50, June 2001.

[35] H. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE Journal of Solid-State Circuits*, pp. 813–821, June 1999.

[36] *Multi-band OFDM physical layer proposal for IEEE 802.15.3a.* Multi-band OFDM Alliance, Available: http://www.ieee802.org/15/pub/TG3a.html.

[37] T. K. K. Tsang and M. N. El-Gamal, "Ultra-wideband(UWB) communications systems: an overview," $IEEE_N EWCAS$ *Conference*, pp. 381–386, June 2005.

[38] K. Stadius, T. Rapinoja, and K. halonen, "Multitone fast frequency-hopping synthesizer for UWB radio," *IEEE Trans. Micro. Theory and Tech.*, pp. 1633–1641, Aug. 2007.

[39] G. Y. Tak, S. B. Hyun, and S. S. Park, "A 6.3-9GHz CMOS fast settling PLL for MB-OFDM UWB applications," *IEEE JSCC*, pp. 1671–1679, August 2005.

[40] H. Kodama, H. Okada, and A. Tanaka, "Wide lock-range, low phase-noise PLL using interpolative Ring-VCO with coarse frequency tuning and freqeuncy linearization," *IEEE CICC*, pp. 349–352, Sept. 2007.

[41] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE JSCC*, pp. 1723–1732, Nov. 1996.

[42] D. Leenaerts, C. Vaucher, and K. Moore, "A 15mw fully integrated I/Q synthesizer for bluetooth in $0.18\mu m$ CMOS," *IEEE ISSCC*, pp. 1155–1161, July 2003.

[43] C. Vaucher, "An adpative PLL tuning system architecture combining hgih spectral purity and fast settling time," *IEEE JSCC*, pp. 490–502, Apr. 2000.

[44] L. Dai and R. Harjani, "Design of low-phase-noise CMOS ring oscillators," *IEEE Trans. on Circuits and Systems*, pp. 328–338, May 2002.

[45] A. Lehner, R. Weighel, and A. Hajimiri, "Design of a novel low-power 4th-order1.7GHz CMOS frequency synthesizer for DCS-1800," *IEEE ISCS*, pp. 637–640, May 2000.

[46] M. Mansuri, D. Liu, and C. Yang, "Fast frequncy acquisition phase-frequency detectors for Gsamples/s phase-locked loops," *IEEE JSSC*, pp. 1331–1334, Oct. 2002.

[47] H. R. Rategh and T. H. Lee, *Multi-GHz Frequency syntehsis and Division*. Kluwer Academic Publishers, 2001.

[48] J. G. Maneatis and M. A. Horowitz, "Precise delay generation using coupled oscillators," *IEEE JSCC*, pp. 1273–1282, Dec. 1993.

[49] I. V. J. Carnes and U. Moon, "Design and analysis of noise tolerant ring oscillators using maneatis delay cells," *IEEE ICECS*, pp. 494–497, Dec. 2007.

[50] A. L. P. et.al., "Substrate noise coupling through planar spiral inductor," *IEEE JSSC*, pp. 877–884, June 1998.

[51] C. S. K. et.al., "Deep trench guard to suppress coupling between inductors in RF ICs," *IEEE MTT-S Digest*, pp. 1873–1876, 2001.

[52] C. P. Y. et.al., "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *VLSI Symposium*, pp. 85–86, 1997.

[53] T. B. et.al., "On-chip RF isolation techniques," *IEEE BCTM*, pp. 205–211, 2002.

[54] "HFSS, Ansoft Inc," 2004.

[55] K. Joardar, "A simple approach to modeling cross-talk in integrated circuits," *IEEE JSSC*, pp. 1212–1219, Oct. 1994.

[56] J. P. R. et.al., "Substrate crosstalk reduction using SOI technology," *IEEE Trans. on Electron Devices*, pp. 2252–2261, December 1997.

[57] C. J. C. et.al., "Characterization and modeling of on-chip inductor substrate coupling effect," *IEEE RF IC*, pp. 311–314, 2002.

[58] J. H. M. et.al., "Crosstalk coupling effects of CMOS co-planar spiral inductors," *IEEE CICC*, pp. 371–374, 2004.

[59] C. L. Chen, "Effects of CMOS process fill patterns on spiral inductors," *Microwave and Optical Technology Letters*, pp. 462–465, March 2003.

[60] J. H. M. et.al., "Coupled microstrip parallel-gap model for improved filter and coupler design," *Electron Lett.*, pp. 377–379, 1983.

[61] M. Kirschning and R. H. Jansen, "Accurate wide-rang design equations for the frequency-dependent chararersitics of parallel coupled micristrip lines," *IEEE Trans. Microwave Theory Tech.*, pp. 83–90, 1984.