CROSSTALK MITIGATION TECHNIQUES IN HIGH-SPEED SERIAL LINKS

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Abstract

One of the primary challenges in high-speed chip-to-chip serial link design is maintaining signal integrity in the presence of inter-symbol interference and crosstalk. Far-end crosstalk (FEXT), the interference from an adjacent aggressor line, has become a major noise source as data rates continue to increase. In addition to reducing the effective signal-to-noise and interference ratio (SNIR), FEXT introduces deterministic crosstalk-induced jitter (CIJ) in the received signal, thereby degrading the receiver's bit error rate (BER). By mitigating FEXT, inter-chip I/Os can have higher aggregate data throughput and interconnects can be placed closer together, which reduces the board area needed and the cost associated with it. In this thesis, two different techniques have been proposed to mitigate the effect of FEXT. The first technique employs FIR filters to implement FEXT cancellation (XTC) at the transmit end, which removes FEXT on each channel to further improve the SNIR of the received data and reduce the CIJ. The second technique staggers the multilane I/Os by adding a variable delay to every other channel at the transmit end, thus shifting the coupled FEXT away from the zero-crossing points of the victim channel. Although I/O staggering can lower CIJ and increase timing margin with relatively little added power, it comes at a cost of decreasing the existing voltage margin. The proposed techniques provide the required groundwork for developing MIMO communication methods that will effectively extricate additional information from FEXT to further reduce the BER during data detection. New I/O transceiver designs with the two techniques have been implemented and fabricated in CMOS processes.

In addition, a novel multilane PRBS generator has been designed to test the fabricated multilane transceivers. As data rates approach higher speeds and FEXT becomes a dominant noise source, the research presented has shown that FEXT mitigation is critical to enhance jitter performance and improve eye openings in high-speed serial links.

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Chapter 1

Introduction

The development of computer technologies in the past fifty years has significantly impacted our society, revolutionizing communications and the spread of information through the pervasiveness of personal computers, the introduction of the internet, and the advent of mobile networks. The constant reduction in the cost of manufacturing silicon integrated circuits (ICs) for consumer electronics has fueled many breakthroughs in computer technologies. Recent advances in computers have provided people with the computational means to solve complex problems and store vast amounts of data ranging from analyzing the stock market to deciphering the human genome. As our society continues to thrive on technological progress, the growth of computer networks and the need for more computational power has created a never-ending demand for faster and more powerful microprocessors, where current IC technology has pushed their speeds over a few GHz. Although microprocessors in the past have been able to double their

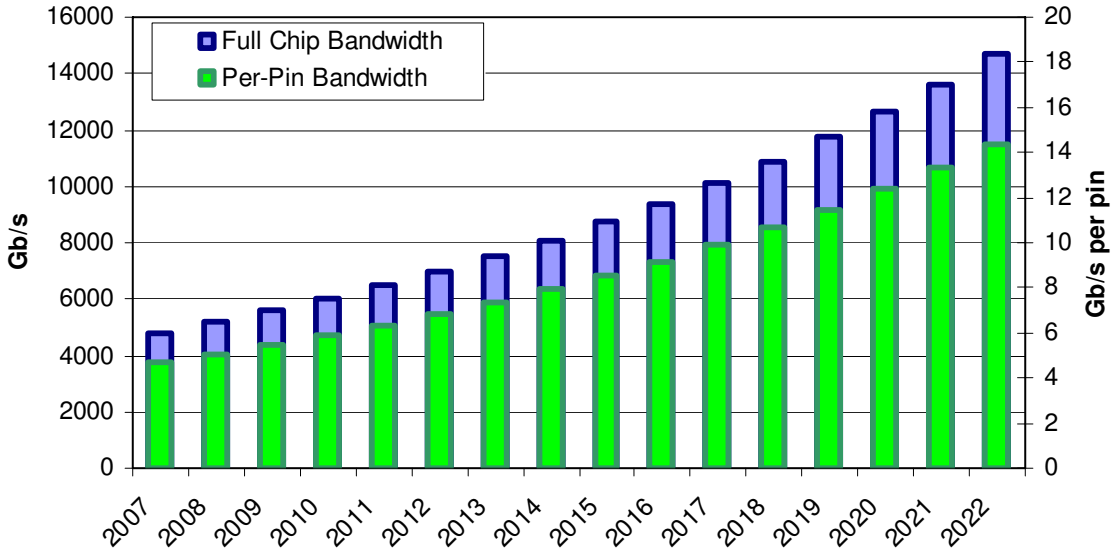

Figure 1.1: Projected aggregate throughput of future CPUs and data rates per pin

processing speed every eighteen months following Moore's Law, the data rates of communication interfaces between different computer components have been increasing at a much slower pace as illustrated in Fig. 1.1 [1]. Furthermore, as demonstrated by Rent's rule [2],

$$P = 7G^{0.21} \tag{1.1}$$

where P is the number of input/output (I/O) pins and G is the number of gates, microprocessors are becoming severely pin-limited due to the widening gap between the number of available signal pins for off-chip communication and the increasing on-chip bandwidth. Therefore, I/O interfaces have gradually become a critical performance bottleneck in multi-gigahertz (GHz) high-speed digital systems.

1.1 The Basics

In general, I/Os are used to transmit and receive data over a channel, which in most cases are copper lines on a board connecting two integrated chips. A basic communication link contains a transmitter that sends a single data stream through a fixed channel, while the receiver processes the incoming signal and recovers the transmitted bits. There are two important types of I/Os that are required within a computer. First, parallel buses between the processor and its peripheral memory are necessary for storing and accessing information. Second, serial links between two processors, also known as chip-to-chip communication, are essential to high-speed computing since they enable simultaneous data processing. Although the aggregate data rate at which information is transferred can be enhanced by increasing the number of parallel serial links, size and area constraints often limit the maximum number of parallel serial links that can be realized. Thus, the data rate of each link must be increased to further improve the overall system performance.

Errors can occur when the receiver interprets the transmitted signal incorrectly such that the transmitted bits differ from the recovered bits at the receiver end. In order to design a reliable communication link, a low bit error rate (BER) is desired, thereby maintaining the signal integrity of the transmitted data. Signal amplitude perturbation and timing variation, also known as jitter, caused by various noise sources are the two ways that can increase the BER of a serial link. Both phenomena diminish the receiver's ability to process and decipher the transmitted data correctly. Data transmission at low

speed is primarily limited by the speed of the integrated circuits since the undesirable effects of the channel and its environment are negligible. However, as the data rates continue to increase into the multi-GHz domain, attenuation and distortion of the transmitted signal due to the nonidealities of the copper line generates a type of noise known as inter-symbol interference (ISI) which significantly reduces the signal integrity of the transmitted data [3]. In systems with many serial links in parallel, far-end crosstalk (FEXT), the noise interference due to adjacent channels, is another major noise source at high speeds. Besides introducing amplitude perturbation, FEXT also induces jitter, thereby increasing the BER noticeably [4].

Considerable research has been done on eliminating or compensating for ISI. Several integrated circuit transmitter designs have been proposed that implement pre-emphasis equalization, which pre-distort the transmitted data to equalize the effect of ISI [5–7]. Receiver designs have also been presented that employ decision feedback equalization (DFE), which eliminates ISI as the receiver is detecting the incoming signal [8–11]. Although many researchers have addressed problems caused by ISI, few researchers have investigated methods to remove or alleviate problems caused by FEXT. This thesis focuses on techniques to eliminate and cancel the effects of FEXT.

1.2 New Challenges in Future I/O Designs

One of the primary challenges in high-speed serial link design is maintaining signal integrity in the presence of ISI and FEXT. FEXT is one of the dominant noise sources as

data rates continue to increase. By eliminating or equalizing FEXT, amplitude perturbation and crosstalk-induced jitter (CIJ) in the received signal can be reduced, thereby increasing the maximum achievable data rate at a given BER. In addition to examining the different FEXT mitigation techniques, integrated circuits have been designed and fabricated in silicon technology to implement and test these methods.

Two different techniques have been presented in this thesis to mitigate the effect of FEXT. The first technique "staggers" the multilane I/Os by adding a delay to every other channel on the transmit end, thus shifting the FEXT coupled from the adjacent channels in order to reduce the BER. Although the method presented can lower CIJ with relatively little added power consumption, it comes at a cost of increasing signal perturbation. An analysis of the delicate tradeoff between signal perturbation and jitter is required to fully understand the consequences of staggered I/Os (SIO). The second technique employs filters similar to pre-emphasis equalization in order to efficiently implement FEXT cancellation on the transmit end. This method removes FEXT on each channel to further improve the signal integrity of the received data and reduce CIJ. The two FEXT mitigation techniques will provide the necessary foundation for the development of the third FEXT mitigation approach using multiple-input-multiple-output (MIMO) communication methods to effectively extrapolate information from FEXT and further lower the BER during data detection.

New I/O architectures that implement the three techniques have been developed. In order to verify these methods, system simulations have been completed, demonstrating

the effectiveness of FEXT mitigation. In addition, I/O designs employing the three techniques have been created and fabricated in sub-micron silicon technology processes. A multilane pseudo-random bit sequence (PRBS) generator has also been created on-chip to supply the random data streams needed for testing the proposed architectures. High-speed measurement results from the ICs running at 5 Gb/s have been taken to verify the first-cut prototype design. The same rigor has been used for the other designs.

As data rates approach higher speeds and FEXT becomes a dominant noise source, the research will show that FEXT mitigation is necessary to enhance jitter performance and improve signal integrity in high-speed serial links. Moreover, communication links using the techniques proposed can dramatically scale in performance at similar rates as the processing speed, enabling faster and more powerful computers and consumer electronics. Besides granting the expansion of mobile and wi-fi networks, the research can increase the processing power and memory speed of current technology by several folds providing the computational means for solving problems that were previously too computationally intensive to solve. Eliminating the interference caused by adjacent channels presents an opportunity to place channels or copper lines closer to each other without noticing any of the deleterious effects due to FEXT. This reduces the board area needed for the channels, and thus the manufacturing and material costs associated with it. The reduction in cost will play a role in giving people access to technologies such as personal computers that were previously too expensive for them to afford.

Chapter 2

Signal Integrity Issues in Wireline Communications

Reliable signaling is accomplished when the information being transferred is correctly interpreted by the receiving end even in the presence of noise and jitter. When noise and jitter significantly alter the desired signal such that the receiver cannot properly detect the incoming data, a breakdown in communication occurs. Signal integrity is a measure of the quality of the signal arriving at the receiver which can be quantified by the achievable bit error rate (BER) of the communication system.

For two components to communicate within a digital system, data signals are sent from the transmitters of one component and detected by the receivers in the other. The basic wireline communication link consists of three key pieces as depicted in Fig. 2.1. The first part is the transmitter which generates a signal, $x(t)$, that represents the outgoing

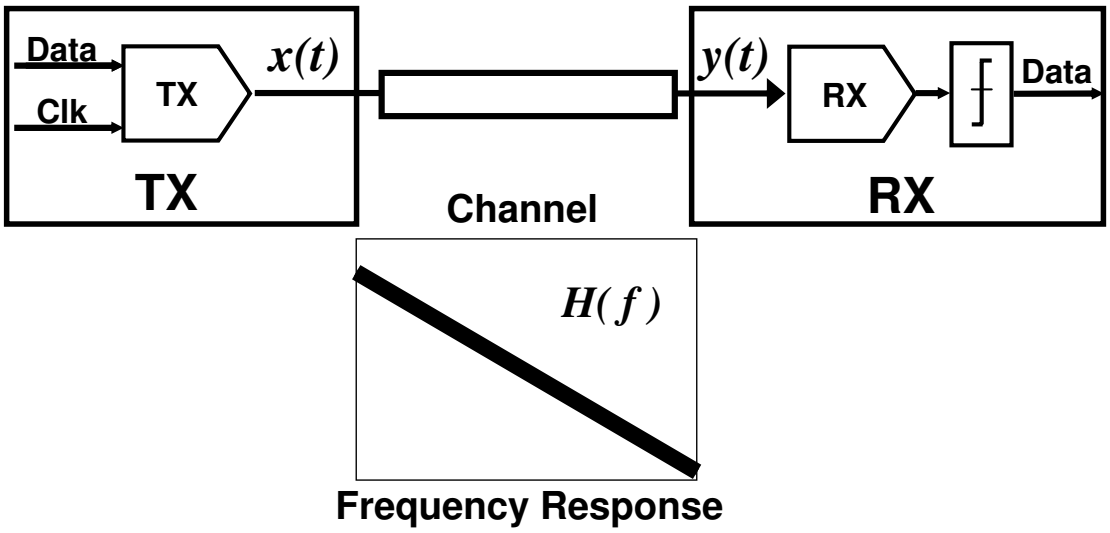

Figure 2.1: Basic wireline communication link

digital data. The second component is the channel which can be characterized by a low-pass response, $H(f)$. Due to its low-pass nature, the channel dramatically affects the propagating signal, producing a distorted signal, $y(t)$. The final piece of the basic communication link is the receiver that detects and converts the incoming signal to digital bits. High signal integrity is achieved when the recovered bits at the receiver perfectly match the outgoing digital data of the transmitter.

In general, transmitters and receivers are designed to operate with a low BER for a given channel by compensating for the channel's undesirable effects on the signal. Therefore, having a full understanding of the channel of interest is essential for implementing new transceivers. To that end, this chapter will provide the basic knowledge of transmission lines and describe its associated noise sources. Since all three components contribute to the noise and jitter of the system, this chapter will also focus on the different types

of noise and jitter that they generate. Finally, an overview of traditional equalization techniques will be given to illustrate previous work that attempted to mitigate problems caused by the channel.

2.1 Transmission Lines

Early digital systems treated wires and interconnects as simple lines that had no impact on the electrical characteristics of the signal. As the data rate of communication interfaces between components improved, copper traces on printed circuit boards (PCB) were represented with lumped models to adequately characterize the slower rise and fall times of the transmitted signal due to the line. This is a simple yet effective way of modeling wires when the signal's transition time is much slower than the delay of the wire. However, when the transmission speed became fast enough such that the rise time of the incoming signal is smaller than the RC delay of the line [12]

$$t_{rise} < RC, \tag{2.1}$$

where R and C are the total line resistance and capacitance, then a rc distributed model is required to accurately illustrate the effect of the wire's delay. As data transmission reaches a point where the rise and fall times are comparable to the propagation time T_{prop} that takes the signal to travel across the wire such that [12]

$$t_{rise} < 2.5T_{prop}, \tag{2.2}$$

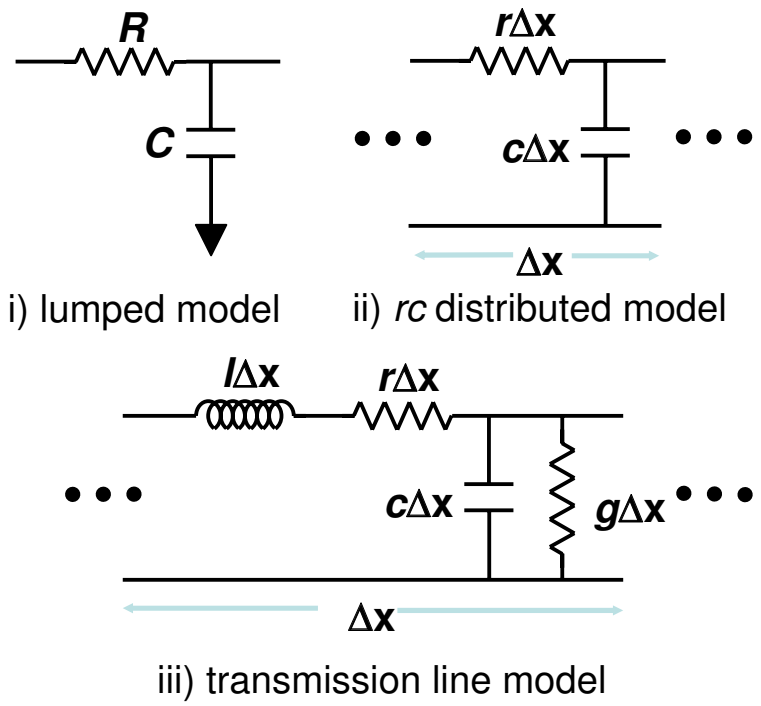

Figure 2.2: Lumped model, rc distributed model, and transmission line model for channel modeling

then PCB traces must be treated as transmission lines to properly capture all the unwanted effects of wire parasitics. Fig. 2.2 depicts the different models used to characterize interconnects depending on the I/O speed and channel length. Note that the remainder of the thesis will focus on signaling techniques and I/O architectures used in multi-GHz high-speed systems, therefore all the channels from this point forward will be modeled as transmission lines [13].

There are several important electrical parameters used to characterize a transmission line. The characteristic impedance, Z_0 of a transmission line is defined by the ratio of the voltage and current waves at any point of the interconnect, represented by the following

equation [14],

$$Z_0 \approx \sqrt{\frac{l}{c}}, \tag{2.3}$$

where l is the inductance per unit length and c is the capacitance per unit length. Since the propagating speed of electrical signals depends on the dielectric material that the transmission line is surrounded by, the propagation velocity, v_{prop}, can be expressed in terms of the dielectric constant as follows [15]:

$$v_{prop} = \frac{c_{light}}{\sqrt{\epsilon_r}}, \tag{2.4}$$

where c_{light} is the speed of light in a vacuum, and ϵ_r is the relative dielectric constant. In addition, the propagation velocity can also be derived from l and c as shown below [16],

$$v_{prop} = \frac{1}{\sqrt{lc}}. \tag{2.5}$$

Given the length of the transmission line, x, the propagation time T_{prop}, otherwise commonly known as the time of flight (TOF), can be determined based on (2.4) and (2.5) as [15]

$$T_{prop} = x\sqrt{lc} = \frac{x\sqrt{\epsilon_r}}{c_{light}}. \tag{2.6}$$

It is important to point out that a transmission line is completely characterized by its characteristic impedance and TOF. Furthermore, these easily measured parameters can be used to solve for inductance and capacitance per unit length. This insight is extremely useful and will be utilized in the later chapters for channel modeling.

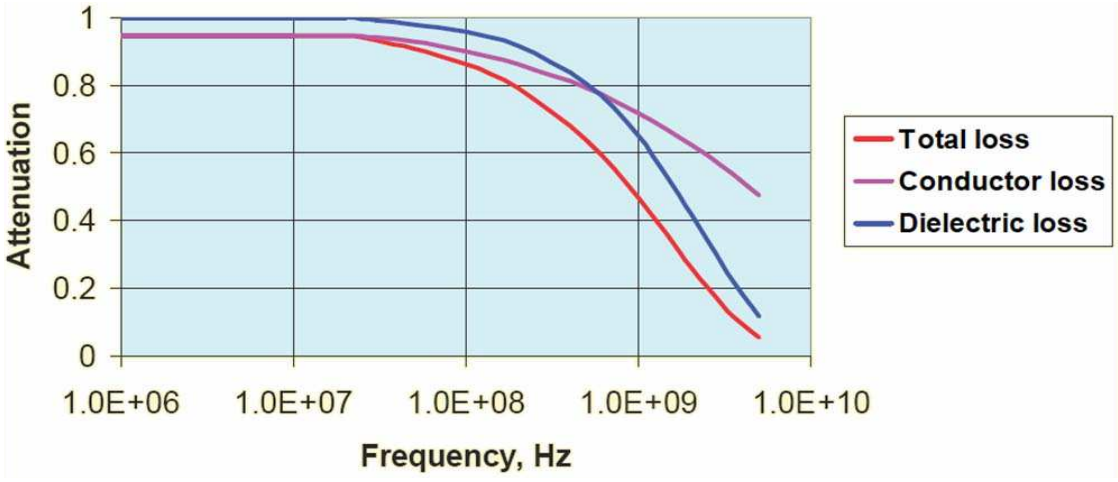

Figure 2.3: FR4 PCB channel frequency response due to skin effect (conductor loss) and dielectric loss

2.1.1 Frequency-Dependent Channel Loss at High Frequencies

Although less lossy PCB dielectric can be used for digital system designs, FR4 is frequently the dielectric of choice due to its low cost and wide availability. Thus, non-ideal effects previously considered to be negligible have become major signal integrity issues. As data rate increases, significant signal attenuation and distortion occur due to frequency-dependent losses and impedance discontinuities. At high frequencies, these problems are mainly due to skin effect and dielectric loss as depicted in Fig. 2.3 [14].

2.1.1.1 Skin Effect

Skin effect is a phenomenon that pushes high-frequency current toward the conductor's surface. This occurs at the multi-MHz frequencies when the interconnect's internal self inductance overpowers the resistance, thereby boosting the impedance of the conductor

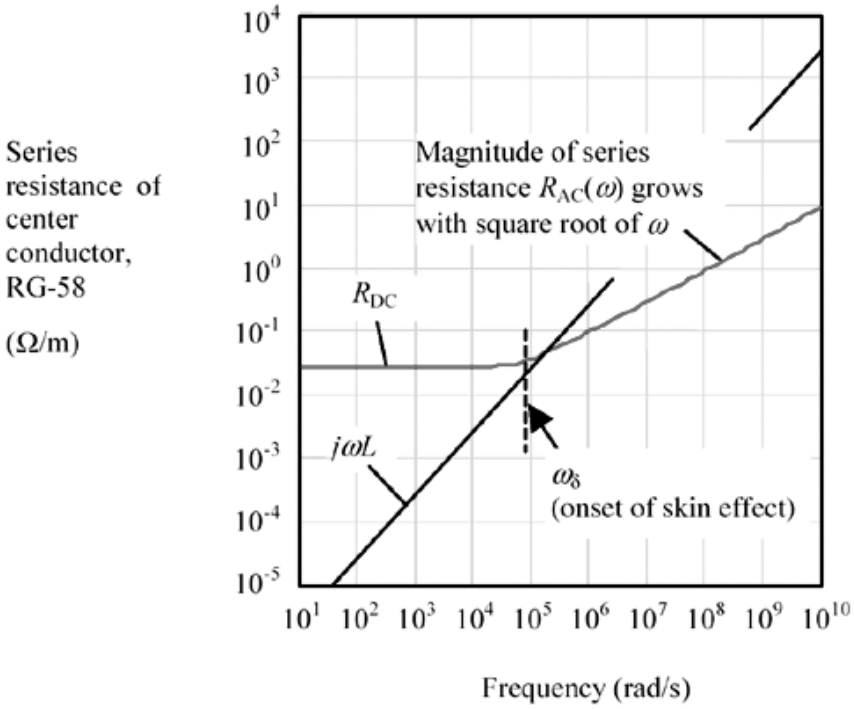

Figure 2.4: A conductor's series resistance illustrating the result of skin effect vs frequency

as exhibited in Fig. 2.4 [17]. Frequency-dependent resistance, $r_{ac}(\omega)$, is roughly proportional to $\sqrt{f}$ at frequencies above the skin-effect cutoff frequency, ω_δ, based on [15]

$$r_{ac}(\omega) \approx \frac{\rho}{W\delta} = \frac{1}{W}\sqrt{\frac{\rho\mu\omega}{2}}, \tag{2.7}$$

$$\omega_\delta = \frac{8\rho}{H^2\mu}, \tag{2.8}$$

where ρ is the resistivity of the metal, W is the width of the interconnect, H is the height of the interconnect, δ is the skin depth, μ is the permeability of free space, and ω is the

frequency. The attenuation factor, $\alpha_\delta(f)$, due to skin effect can be expressed as

$$\alpha_\delta(\omega) = \frac{R_{DC}}{2Z_0}\sqrt{\frac{\omega}{\omega_\delta}}, \tag{2.9}$$

where R_{DC} is the DC resistance of the channel and Z_0 is the characteristic impedance. The approximations made in (2.7) and (2.9) are pessimistic estimates since they assume that all the current is flowing in the skin depth of the conductor.

2.1.1.2 Dielectric Loss

Dielectric loss is the energy dissipated by the dielectric material when the transmitted signal's electromagnetic power is converted to thermal heat. Although this occurs at all frequencies, frequency-dependent dielectric loss becomes significant at frequencies beyond ω_θ when it surpasses attenuation due to skin effect in the GHz region. The attenuation factor, α_θ, due to dielectric loss is approximately

$$\alpha_\theta(\omega) = \frac{\omega\sqrt{\epsilon_r}tan\theta}{2c_{light}}, \tag{2.10}$$

where ω is the frequency of interest, $tan\theta$ is the loss tangent, ϵ_r is the relative permittivity of the material, and c_{light} is the speed of light [14]. At low frequencies, losses due to dielectric absorption are eclipsed by skin-effect losses. As the frequency increases, dielectric loss worsens at a faster rate since it is linearly proportional to frequency f as depicted in (2.10).

PCB dielectric materials have distinct ϵ_r and $tan\theta$. These parameters also vary with board thickness. From (2.10), materials with lower ϵ_r and $tan\theta$ have less attenuation

Table 2.1: Electrical properties of PCB dielectric materials

Material	ϵ_r	$tan\theta$
FR4 Epoxy Glass	4.1	0.02
Polymide Glass	4.1	0.015
Nelco N4000-6	4	0.012
GETEK	3.9	0.008
Cyanate Ester	3.8	0.005
Teflon	2.2	0.0002

as listed in Table 2.1 [18]. However, these materials such as Teflon are prohibitively expensive. This is why more complicated I/O architectures are implemented to mitigate channel loss instead of replacing FR4 PCBs with higher performance dielectric PCBs.

2.2 Timing Jitter & Amplitude Noise

Timing jitter is the variation of a signal's transition edge while amplitude noise is the unintentional deviation to its actual voltage amplitude. Both jitter and noise disrupt clean signals, reducing the I/O signal integrity. With data rates constantly rising, the effects of these phenomena become more pronounced. Therefore, a good understanding of the different types of jitter and noise is necessary in order to actively minimize their detrimental effects on signal integrity when designing high-speed wired communication

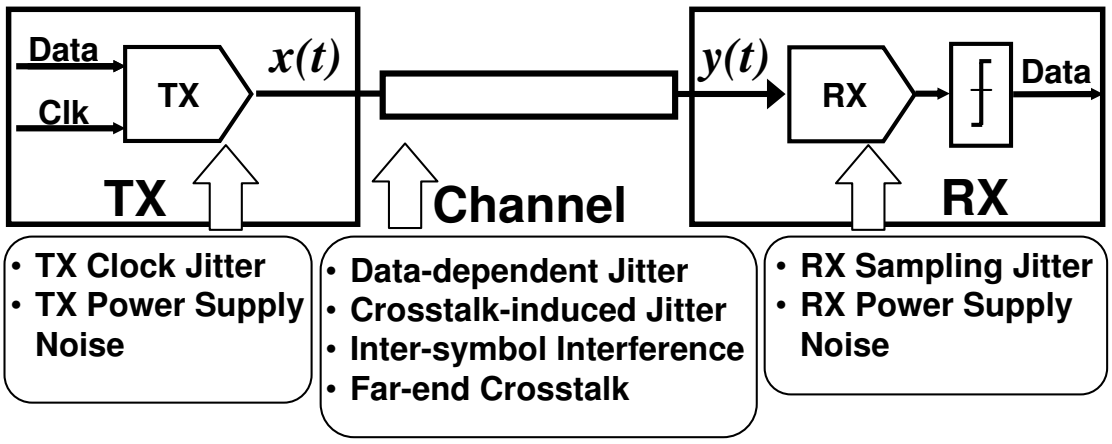

Figure 2.5: Different noise and jitter within a typical serial link

interfaces.

Although random jitter and thermal noise can be introduced through external sources, they are usually negligible compared to the noise and jitter that are generated by the three different components of a common communication link within the data or clock path. As shown in Fig. 2.5, the two important sources of noise and jitter on the transmitter (TX) side is the TX clock jitter and the TX power supply noise [14]. Any phase noise on the transmit clock translates into timing jitter, therefore a low phase noise phase-locked loop (PLL) is imperative for generating the transmit clock. The TX power supply noise is induced by the asynchronous current switching of all the I/Os, which may couple into the transmitted signal. Careful layout and decoupling capacitors can lower the TX power supply noise.

Similar to the TX end, the receiver (RX) also causes RX sampling jitter and RX power supply noise. However, the received signal is much more sensitive to the noise and

jitter since the detected signal has a smaller voltage amplitude and a slower transition edge. For example, serial links operating at 4Gb/s have been observed to have 20mV noise on the power supply [19], which can have an effect of reducing the the received signal swing by 10% or increase jitter by 1ps. The uncertainty in the RX clock due to the clock recovery circuit introduces sampling jitter at the slicer, thereby further lowering the allotted timing budget.

The channel is the final element of a communication link that generates noise and jitter as illustrated in Fig. 2.5. The channel's limited bandwidth produces inter-symbol interference (ISI), which varies the transition edge slope, inducing data-dependent jitter (DDJ). Signaling in adjacent channels couples deterministic noise. This is known as far-end crosstalk (FEXT). Since FEXT occurs during data transitions, it inherently causes crosstalk-induced jitter (CIJ) [4]. The following two subsections will focus on these jitter and noise sources since the remainder of the thesis analyzes techniques that mitigate them.

2.2.1 Inter-symbol Interference & Data-dependent Jitter

A symbol that is being sent across a channel can be corrupted by previously transmitted symbols when some of the energy from the transmitted symbols remains in the transmission line. This is referred to as inter-symbol interference (ISI). The phenomenon is caused by the channel's finite bandwidth, which forces the channel to retain memory of the previous bits as shown in Fig. 2.6. To put it another way, the channel low-pass filters the data stream such that the slope of the data transition becomes so slow that it

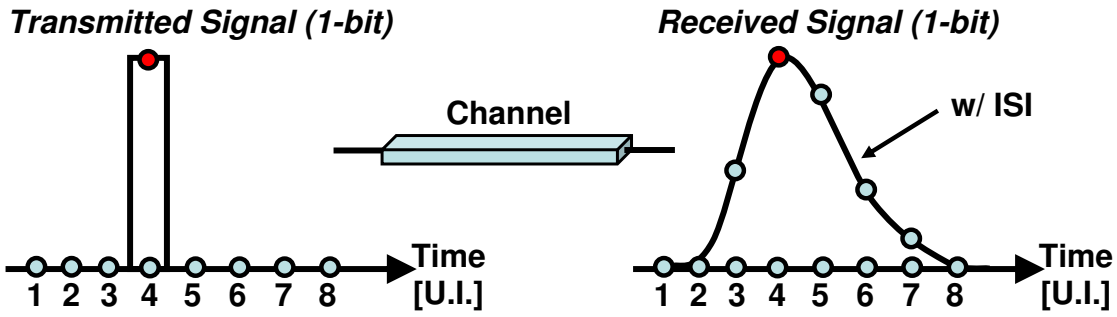

Figure 2.6: Transmitted data signal vs. received data signal with ISI

interferes with the next approaching data edge. At each transition edge, ISI due to preceding bits alters the transition such that the time at which the edge crosses a decision threshold changes. This deterministic timing variation is known as data dependent jitter (DDJ). Note that the deviation in the threshold-crossing time due to DDJ, $\delta t_{c,DDJ}$ has an expression [4]

$$\triangle t_{c,DDJ} = \frac{1 - s(t_0 + T)}{s\prime(t_0 + T)s\prime(t_0)}, \tag{2.11}$$

where $s(t)$ is the step response, t_0 is the time at which $s(t)$ crosses a voltage threshold, and T is the bit time.

In order to capture all the transitions, the channel cutoff frequency must include at least the fundamental frequency of the fastest bit transition of a nonreturn-to-zero (NRZ) data pattern, which is one half of the data rate. Moreover, from Fig. 2.7, it can be observed that more than 94% of the power in random NRZ data is contained in the spectrum between the frequencies of 0 and 0.75X of the data rate [20]. This implies that ISI occurs when the channel bandwidth is between 50% to 75% of the data rate. As data rate increases, equalization is employed to extend the cutoff frequency such that it

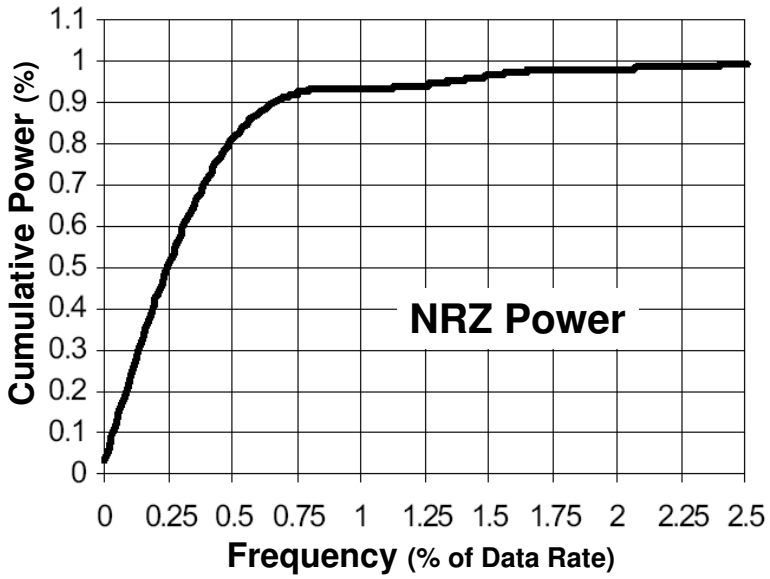

Figure 2.7: Percentage of NRZ power spectrum vs. frequency

continues to contain majority of the power in NRZ data.

2.2.2 Far-end Crosstalk & Crosstalk-induced Jitter

Crosstalk arises whenever energy is coupled during data transitions in adjacent lines. The channel that is causing the crosstalk is known as the aggressor line while the channel that experiences the induced crosstalk noise is called the victim line. The coupling is due to the mutual inductance and mutual capacitance between the two lines, which results in far-end crosstalk (FEXT) at the far end of the victim line as shown in Fig. 2.8. When FEXT appears during a data transition in the victim line, it shifts the threshold-crossing time, thereby inducing deterministic jitter known as crosstalk-induced jitter (CIJ).

Mutual inductance L_m triggers a voltage perturbation in the victim line when a data

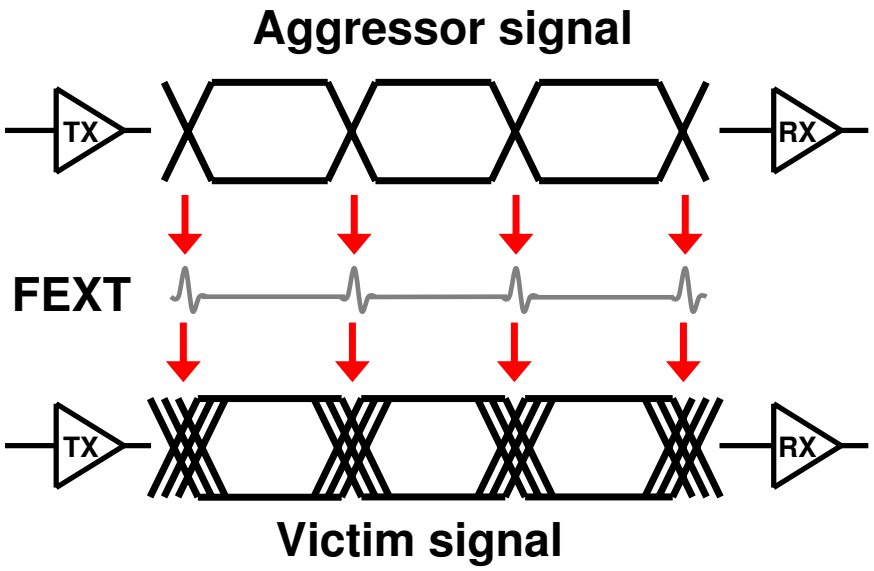

Figure 2.8: The effect of FEXT on the victim data signal

transition takes place in the aggressor. The change in current in the aggressor causes a change in the magnetic field it creates. Since the victim line is adjacent to the aggressor line, the change in magnetic field affects the victim line as well, which in turn induces noise. Mutual capacitance C_m models the second mechanism that contributes to FEXT. The coupling from the electric field due to a change in voltage during a data transition in the aggressor line injects a current onto the victim line. Note that the induced voltage and current perturbations are proportional to the rate of change and worsens exponentially as the spacing between adjacent lines reduces [15]. In addition, mutual inductance is the dominant source of FEXT for low-impedance line whereas mutual capacitance is the dominant source of FEXT for high-impedance line [21]. An in-depth analysis of FEXT and CIJ is presented in Chapter 5.

2.3 Voltage & Timing Margin

In order to examine the signal integrity of a communication link, the received signal is observed by segmenting it into single period intervals and then overlaying them on top of each other. This type of plot is known as an eye diagram. Eye diagrams are used to quantify noise margin degradation as displayed in Fig. 2.9. An ideal eye diagram would show a perfect rectangle. However, ISI and other channel noise cause the transition slope to be slower, thereby closing the eye opening. An eye closure depicts a drop in signal-to-noise ratio (SNR) and an increase in bit error rate(BER).

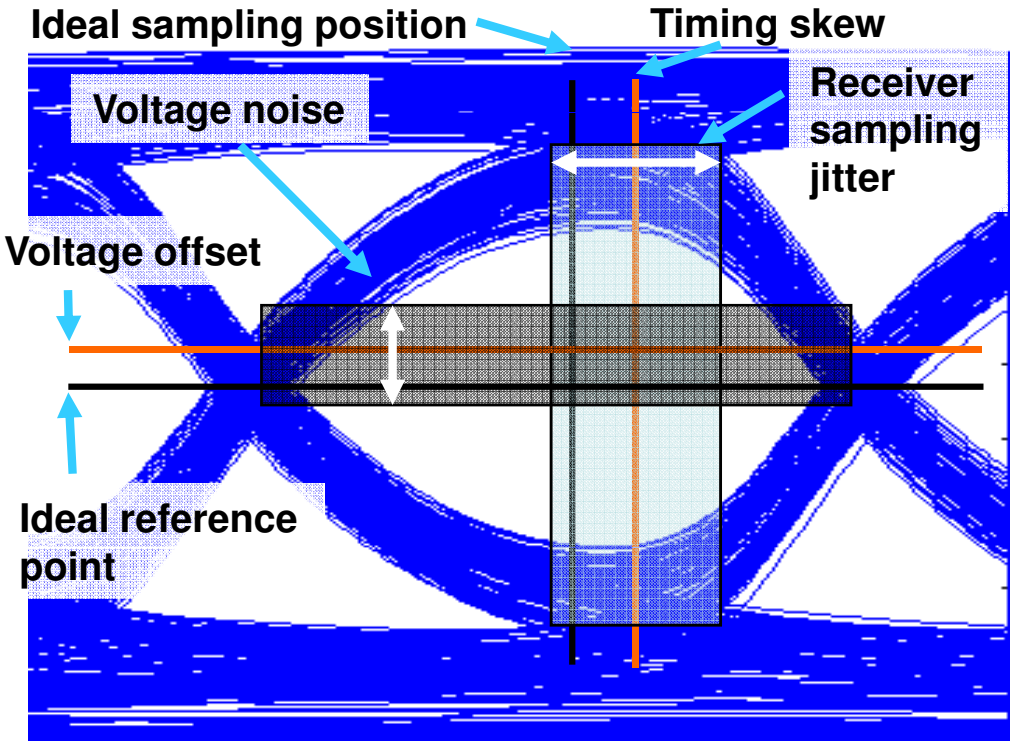

Figure 2.9: The effects of nonidealities on an eye diagram

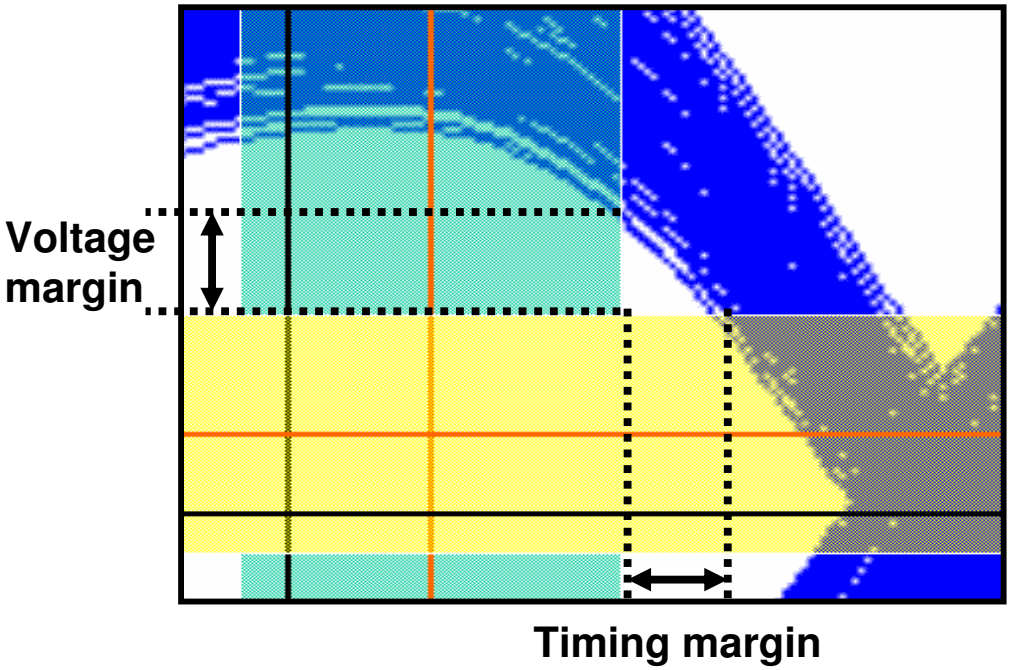

Figure 2.10: The voltage and timing margins of an eye diagram

As shown in Fig. 2.9, the ideal reference point is typically one-half of the peak-to-peak voltage swing, $0.5V_{PP}$. The vertical eye opening must be large enough such that it can still detect the signal reliably even in the presence of a voltage offset on the voltage threshold and additional noise. On the matter of timing, the ideal sampling time is approximately one-half of the bit time, $0.5T_{bit}$. Adequate horizontal eye opening is required to accommodate for timing skew of the sampling time and jitter. The overlapping part of the horizonal and vertical bars illustrated in Fig. 2.9 is the minimum eye opening required to detect digital bits from the incoming analog signal.

Voltage and timing margins are defined as the extra vertical and horizontal eye opening beyond the required minimum eye opening for signal detection. As pointed out

in Fig. 2.10, the voltage margin $\triangle V$ and the timing margin $\triangle T$ are defined as

$$\triangle V = V_{PP} - V_{ISI} - V_{noise} - V_{offset}, \tag{2.12}$$

$$\triangle T = T_{bit} - T_{skew} - T_{jitter}. \tag{2.13}$$

Eye diagrams will be utilized in the remainder of the thesis to observe the eye-opening effect of the proposed FEXT mitigation techniques.

2.4 Traditional Equalization for ISI

In traditional I/O designs, the data rate is slow enough such that interconnects can be modeled by ideal wires. However, the performance of these I/O interfaces is dependent on the wire length. To achieve higher speeds, modern I/O designs use incident-wave signaling such that the signal sent is detected on the first traversal of the PCB line and absorbed by the receiver termination. This allows the data rate to scale with technology independent of the signal line length. Matched termination is needed at both ends to suppress reflections in incident-wave signaling since reflected waves will distort the transmitted signal [3]. As discussed in Section 2.2, ISI and FEXT distort the transmitted signal, which leads to a lower SNR and a higher BER. Traditional equalization is used to overcome ISI caused by the channel. Equalizers are frequency shaping filters that flatten the channel response up to the Nyquist frequency, which increases the maximum achievable data rate [22]. The conceptual diagram in Fig. 2.11 shows two ways of performing equalization. Method A attenuates the low frequencies of the signal spectrum while method B amplifies the high frequencies [23].

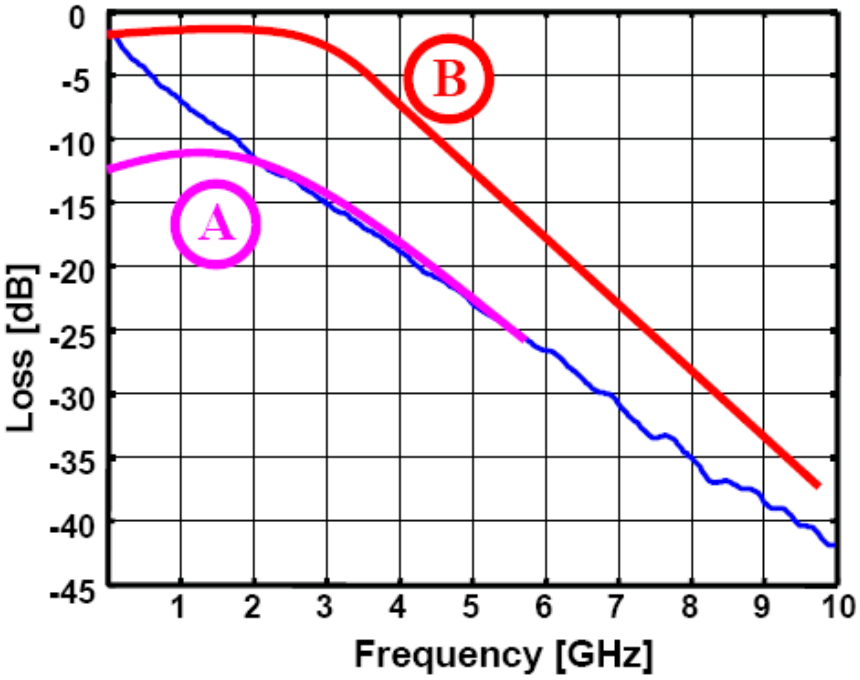

Figure 2.11: Frequency response that shows two ways of equalization

Although equalization can be accomplished at the transmitter or the receiver, in most cases, it is usually performed at both ends for the best performance [24–27]. Transmit equalization can be realized as a simple N-tap FIR filter. The basic idea is to preshape the transmitted data in order to attenuate the low-frequency portion of the signal spectrum while maintaining the high-frequency part. Because of this, transmit equalizers are also referred to as pre-emphasis filters. Typical filters range from having 2 to 5 taps. As the number of taps increases, the equalization becomes more ideal. However, each additional tap requires more power and area, thus there is a tradeoff that has to be made when designing a discrete-time transmit equalizer. Furthermore, as the number of taps increases the received voltage swing is reduced, hence the SNR cannot be improved. In

>5-Gb/s transmission, the ideal number of taps for an acceptable amount of equalization is about four [25–27].

A 3-tap pre-emphasis equalizer is shown in Fig. 2.12. The data is delayed by an unit interval (UI) each time it passes through a flip-flop. The delay line drives the pre-cursor, the cursor and the post-cursor taps which adds the current provided by each driver to produce the final transmitted signal. The taps are set by digital-analog converters (DACs) that control the tail current source [7]. The output of the pre-emphasis transmitter and the resulting received equalized eye diagram are depicted in Fig. 2.13.

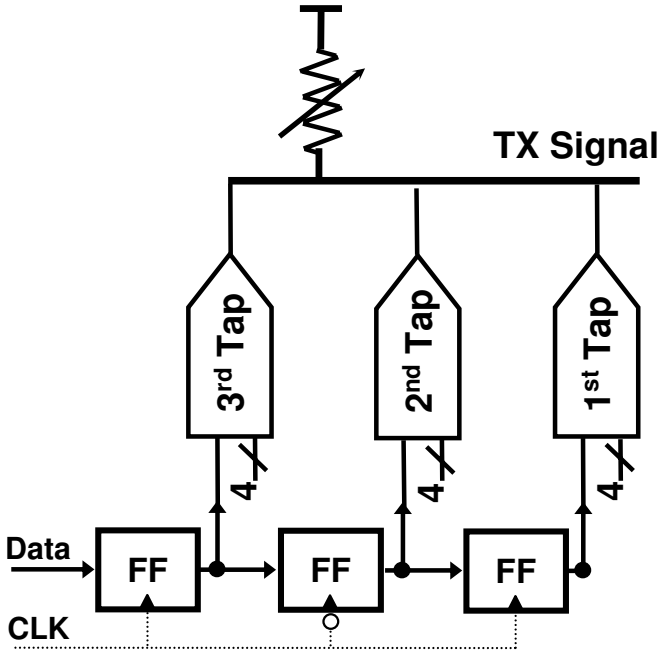

Figure 2.12: 3-tap TX pre-emphasis equalizer

Receive equalization can be implemented in several different manners. Digital FIR filters can be implemented in much of the same way as the transmit equalizer. However,

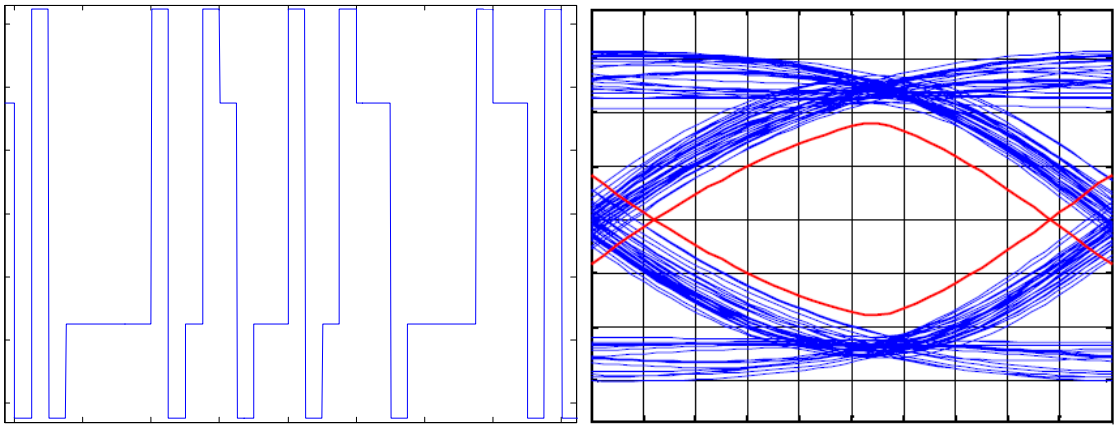

Figure 2.13: 5-Gb/s pre-emphasis TX output and its resulting equalized eye diagram

in order to get the sampled data, an ADC is required to sample the received signal. This type of equalizer is limited by the speed of the ADC which is often used in the MHz range. Another type of equalizer used is a continuous-time passive high-pass filter as shown in Fig. 2.14 [23]. This filter employs passive components to produce the high-pass response. The main limitation for using this type of filter is the amount of space necessary for creating the inductors and capacitors on chip. In addition, the filter is not adaptable and offers narrow compensation gain. The two filters described above only attenuate the low frequency portion and do not improve the SNR unlike the transmit equalizer.

A kind of receive equalizer that is frequently implemented is an continuous-time active filter as shown in Fig. 2.15. It is common to use this as the first stage of the receiver since the circuit is a common source amplifier with capacitive degeneration. G_{CTRL} controls the low-frequency gain, while Z_{CTRL} controls the high-frequency boosting. The resistor

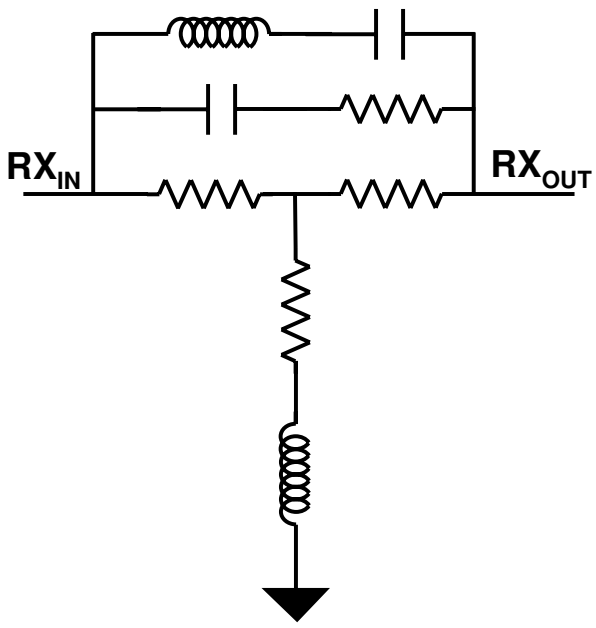

Figure 2.14: Passive high-pass filter

between the two legs controls the minimum low-frequency gain. The shunt capacitor establishes a zero to boost the high frequency [27].

The last type of filter used for receive equalization is a non-linear equalizer called decision feedback equalizer (DFE) as illustrated in Fig. 2.16. It uses past decisions to determine what the actual postcursor ISI should be and then remove the postcursor ISI caused by that bit in the data that follows. DFE equalizers are widely used in high-speed I/O design because they improve SNR by amplifying the signal without increasing the noise [8, 10, 11, 24]. However, error propagation occurs when the slicer makes a wrong decision, triggering a series of incorrect ISI removal or lack thereof. This could lead to a chain of data detection errors, which the receiver is unable to recover from.

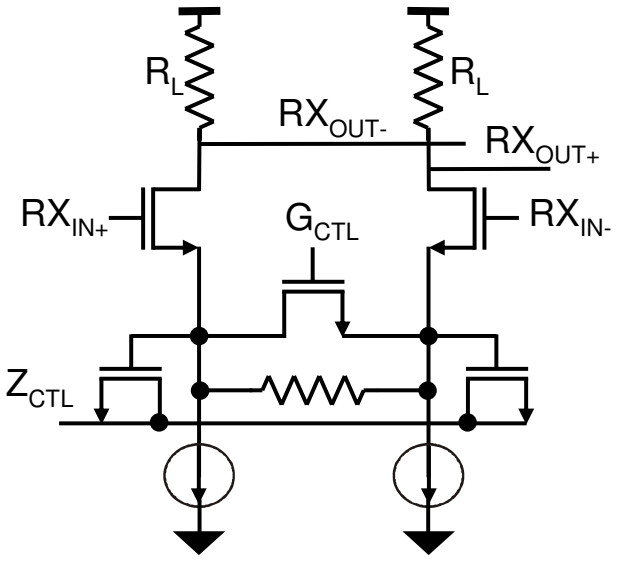

Figure 2.15: Active continuous-time filter

Although FEXT is slowly becoming a significant noise source as data rate increases, none of the traditional equalizers described in this section mitigates FEXT or reduces CIJ. Conversely, pre-emphasis equalization even amplifies FEXT. Therefore, new techniques are needed to diminish the effects of FEXT. The remainder of the thesis will explore different FEXT mitigation methods and verify them with simulations and measurement results.

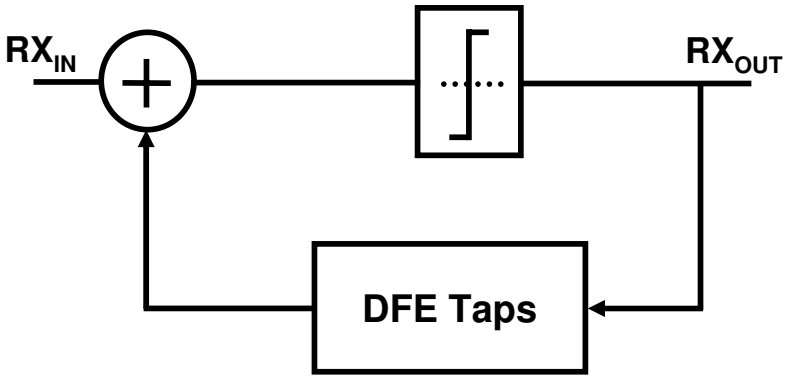

Figure 2.16: N-tap decision feedback equalizer

Chapter 3

An Accurate & Efficient FEXT Model Using a Two-Pole Moment Matching Technique

Today's high-performance microprocessors have created a trend for designing faster chip-to-chip wireline communication links. Traditional equalization techniques have been used to remove inter-symbol interference (ISI) caused by bandwidth-limited channels. However, even with the ability to eliminate ISI, maintaining high signal integrity remains an issue as data rates continue to increase into the multi-Gb/s region. This is because previously negligible noise sources are becoming much more prominent at high frequencies. One of the dominant high-frequency noise sources is far-end crosstalk (FEXT), which is the induced noise interference due to inductive and capacitive coupling of adjacent

channels [16].

An accurate FEXT model is vital in assessing the impact of FEXT on I/O performance. Moreover, fast and efficient FEXT modeling provides designers immediate insights that are critical to the development of new FEXT mitigation techniques [21,28,29]. Although simulation tools such as 2D field solvers or simulation program with integrated circuit emphasis (SPICE) give the most accurate FEXT characterization, these tools are computationally expensive. 2D field solvers employ the finite-difference time-domain (FDTD) method to solve Maxwell's equations as the fields vary over time, which requires excessively large computational power [30]. For SPICE, extracted capacitance and inductance data based on S-parameter models is required to produce accurate results [31].

Various analytical models and closed-form formulas have also been proposed for characterizing FEXT and its associated crosstalk-induced jitter (CIJ). These models are used to investigate the effects on FEXT due to changes in the physical parameters of the interconnects and provide the means to quickly calibrate different FEXT mitigation techniques without long simulation times. Models that are based on the well-understood coupled transmission-line theory are typically very complex and difficult to evaluate [32–35]. Buckwalter provided a simple yet effective approximation for analyzing CIJ [21]. However, it only offers insight into the jitter that FEXT induces and not the amplitude noise it creates. A moment-matching-based model for estimating FEXT in coupled RC tree networks on chip has been formulated using a recursive algorithm developed in [36]. Al-

though the model simplified FEXT by model order reduction, it only observed the peak and the delay of the induced FEXT.

The model presented in this chapter will provide a simple yet accurate technique through moment matching to estimate the FEXT response between two off-chip interconnects. The next section will begin by describing the relationship between the channel and its associated FEXT. Section 3.2 will discuss a first-order approximation based on the Elmore time constant while Section 3.3 will reveal a two-pole approximation based on moment matching.

3.1 Relationship between Channel & FEXT Impulse Responses

Capacitive and inductive coupling between the aggressor, channel 1, and the victim, channel 2, results in FEXT at the end of channel 2. This phenomenon can be expressed by a time-domain expression based on the telegrapher's equations used to describe two coupled transmission lines [17]. As the aggressor signal propagates along channel 1 and couples its derivative into the victim line, a forward-traveling FEXT wave on channel 2 travels with it. Given that channel 1's received signal without FEXT is $r_1(t)$, the induced coupling, $v_{FEXT}(t)$, in channel 2 can be denoted as [14]

$$v_{FEXT}(t) = \tau_f \frac{dr_1(t)}{dt}, \tag{3.1}$$

where τ_f is the forward-coupling time constant. Note that τ_f is a function of the physical parameters of the coupled transmission lines such that

$$\tau_f = \frac{l}{2}(C_m Z_0 - \frac{L_m}{Z_0}), \tag{3.2}$$

where l is the length of the line, C_m is the mutual capacitance, L_m is the mutual inductance, and Z_0 is the characteristic impedance. The L_m term dominates in lines with a characteristic impedance of 50Ω, thereby simplifying τ_f to

$$\tau_f \approx \frac{-l}{2}(\frac{L_m}{Z_0}). \tag{3.3}$$

Since a transmission line is a linear, time-invariant (LTI) system which can be completely characterized by its impulse response, the received signal of channel 1 can be expressed as

$$r_1(t) = \int_{-\infty}^{0} x(t)h_1(t-\tau)d\tau \tag{3.4}$$

where $x(t)$ is the input signal, and $h_1(t)$ is the impulse response of channel 1. This can be converted into the frequency domain, resulting in

$$R_1(s) = X(s)H_1(s). \tag{3.5}$$

Based on (3.1) and (3.5), FEXT can be defined in the frequency domain as

$$\begin{aligned} V_{FEXT}(s) &= \tau_f(sR_1(s)) \\ V_{FEXT}(s) &= \tau_f[s(X(s)H_1(s))]. \end{aligned} \tag{3.6}$$

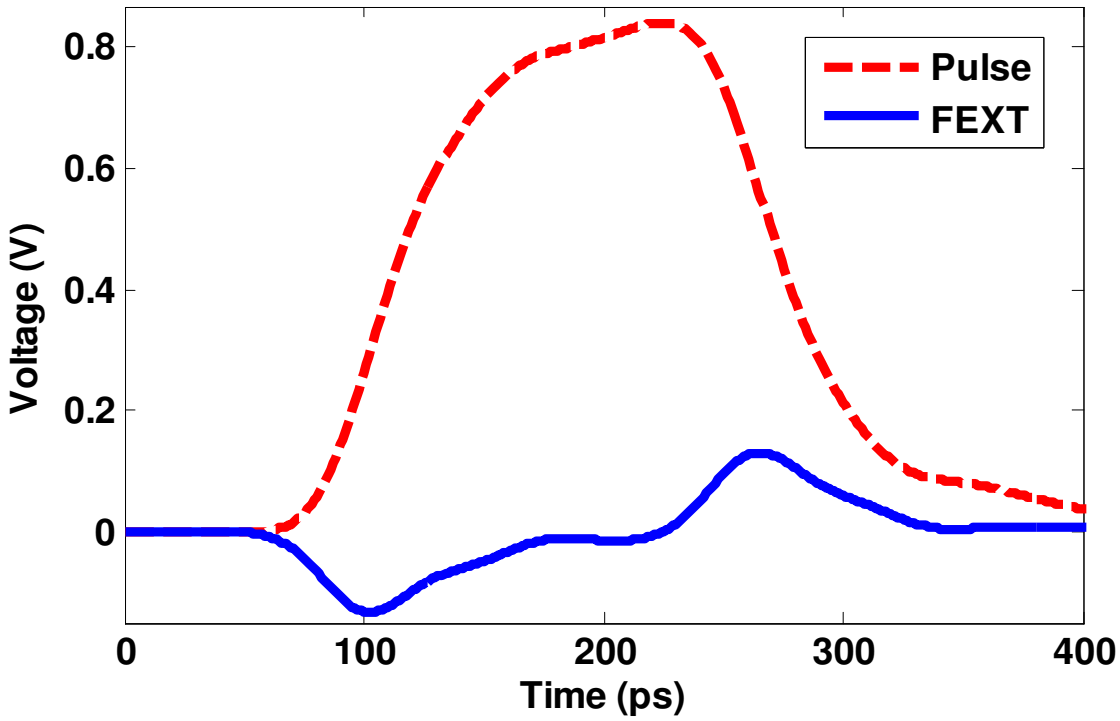

Figure 3.1: Measured channel pulse response & its associated FEXT

By manipulating the transfer function, $V_{FEXT}(s)$ can be rearranged to

$$\begin{aligned} V_{FEXT}(s) &= \tau_f[(sH_1(s))(X(s))] \\ V_{FEXT}(s) &= s(\tau_f H_1(s))X(s). \end{aligned} \tag{3.7}$$

Therefore, the FEXT impulse response, $h_{FEXT}(t)$, is a function of channel 1's impulse response as defined by

$$\begin{aligned} H_{FEXT}(s) &= s(\tau_f H_1(s)) \\ h_{FEXT}(t) &= \tau_f \frac{dh_1(t)}{dt}. \end{aligned} \tag{3.8}$$

In general, if $h_i(t)$ represents channel i, the weakly-coupled FEXT from the aggressor

channel i to the victim channel j, $h_{FEXT}(t)$, is proportional to the derivative of $h_i(t)$ as demonstrated in (3.8). This is further supported by Fig. 3.1, which shows a measured channel pulse response and its associated FEXT response.

3.2 Elmore First-Order Approximation

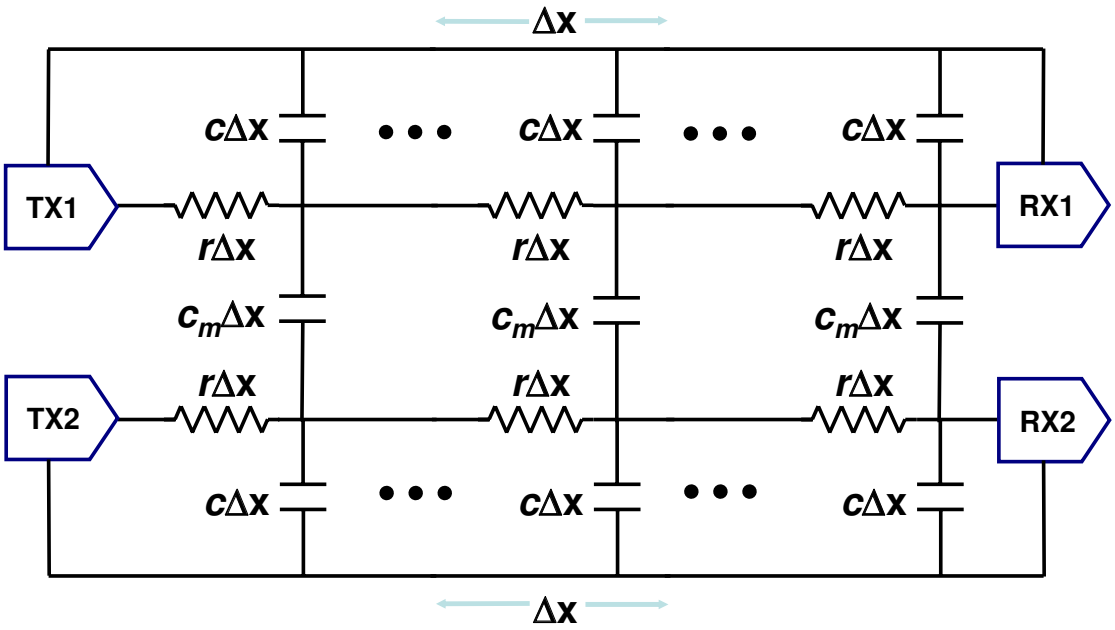

Figure 3.2: a rc distributed circuit model of two coupled channels

A channel can be represented by a distributed circuit model as shown in Fig. 3.2. As the number of unit length rc segments increases to infinity, the number of poles in the system also approaches infinity. This suggests that the channel's frequency response can be expressed as

$$H(s) = \sum_{j=1}^{\infty} \frac{k_j}{s - p_j}, \tag{3.9}$$

where k_j is the j^{th} constant and p_j is the j^{th} pole. The frequency response in (3.9) can be converted to a time-domain impulse response in the form of

$$h(t) = \sum_{j=1}^{\infty} k_j \cdot e^{p_j t}. \tag{3.10}$$

In order to take the distributed transmission line effect of the channel into account, a first-order approximation of the system can be made using an Elmore time constant, τ_e, such that [37]

$$\frac{1}{p_1} \approx -\tau_e. \tag{3.11}$$

The Elmore time constant of a N-segment channel is computed by [12]

$$\begin{aligned} \tau_e &= \sum_{i=1}^{N} r_i \sum_{j=1}^{i} c_j \\ &= rc\frac{N(N+1)}{2} \\ &\approx \frac{RC}{2}, \end{aligned} \tag{3.12}$$

where $R = rN$ and $C = cN$ are the total lumped resistance and capacitance of the line as $N \to \infty$.

Given the Elmore time constant, the frequency response of the channel can be estimated as

$$H(s) = \frac{k_1}{s - p_1} = \frac{\tau_e^{-1}}{s + \tau_e^{-1}}, \tag{3.13}$$

where $k_1 = \tau_e^{-1}$ and $p_1 = -\tau_e^{-1}$. The time-domain impulse response of a channel can be estimated by its first-order, one-pole approximation, (3.13) such that

$$h(t) = \frac{1}{\tau_e} e^{-\frac{t}{\tau_e}} \cdot u(t). \tag{3.14}$$

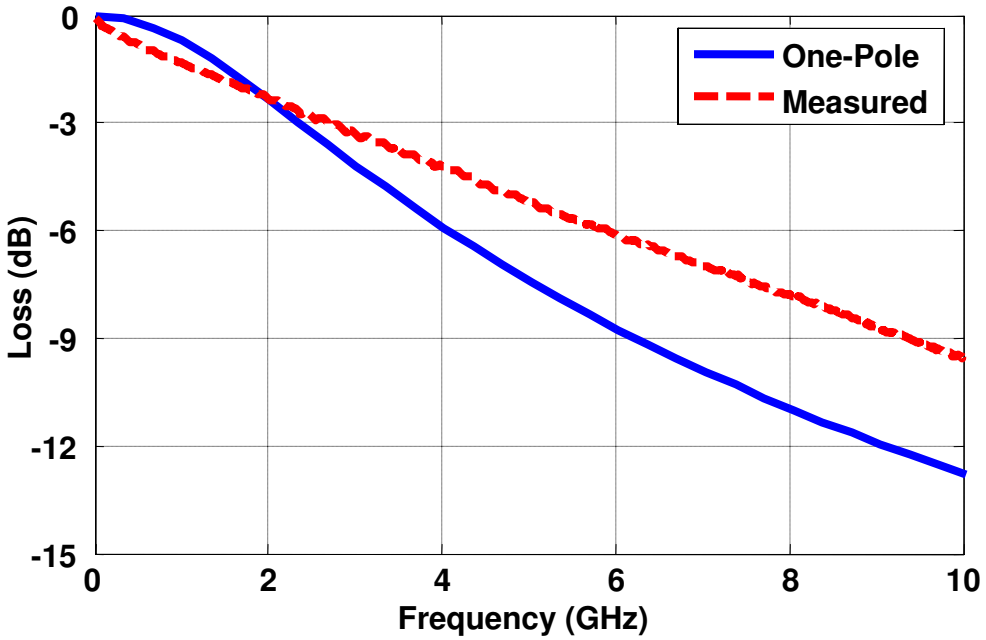

Figure 3.3: 12-inch microstrip frequency response: one-pole model vs measured

Based on (3.8), taking the derivative of (3.14) yields the associated FEXT impulse response

$$h_{FEXT}(t) = \tau_f \cdot \frac{1}{\tau_e} e^{-\frac{t}{\tau_e}} \cdot (\delta(t) - \frac{1}{\tau_e} u(t)). \tag{3.15}$$

Using (3.14) and (3.15), the computed channel's step response and its associated weakly-coupled FEXT response are graphed in Figs. 3.4 and 3.5 where

$$s(t) = V_{DD}(1 - e^{-\frac{t}{\tau_e}}) \tag{3.16}$$

$$s_{FEXT}(t) = \frac{\tau_f V_{DD}}{\tau_e} \cdot e^{-\frac{t}{\tau_e}}. \tag{3.17}$$

As shown in Fig. 3.3, the one-pole response is a good estimate of the actual channel response up to 3 GHz. A comparison between the step response of the derived one-pole channel and a measured step response of a microstrip channel in Fig. 3.4 further rein-

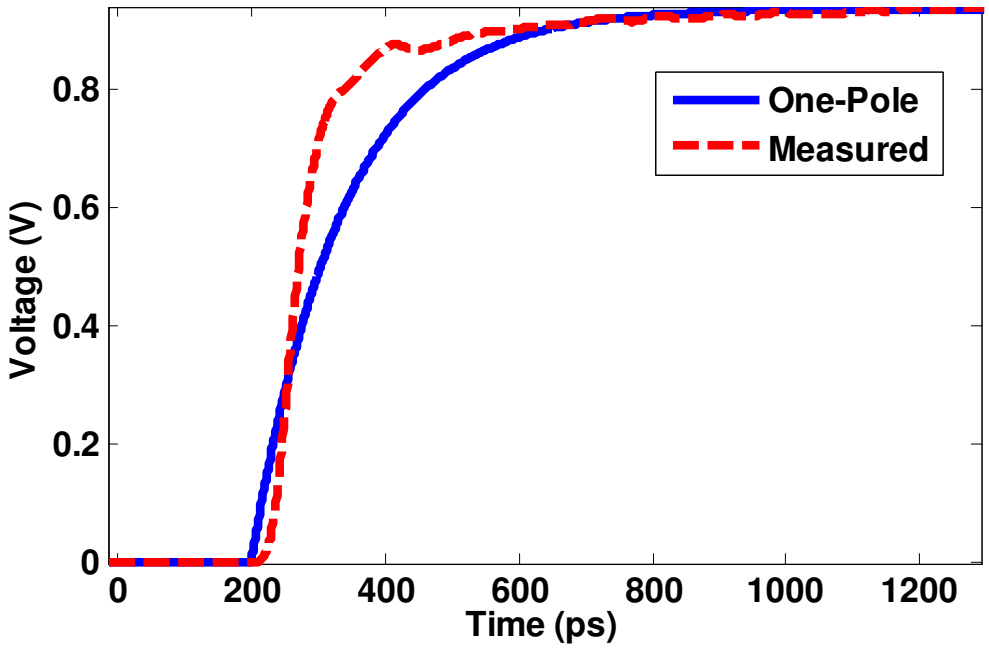

Figure 3.4: 12-inch microstrip step response: one-pole model vs measured

forces the accuracy of the model in low frequencies. However, as illustrated in Fig. 3.5, the FEXT's peak occurs at $t = 0$, which clearly deviates from the measured FEXT. Therefore, higher-order models are required to provide a simple yet accurate approximation of FEXT.

3.3 Two-Pole Approximation by Moment Matching

The frequency response of any channel can be written as

$$H(s) = \frac{B(s)}{A(s)} = \frac{1 + b_1 s + \ldots + b_{N-1} s^{(N-1)}}{1 + a_1 s + \ldots + a_N s^N}, \tag{3.18}$$

as $N \to \infty$. By taking the formal definition of the Laplace transform and expanding $H(s)$ about $s = 0$, the transfer function can also be approximated with a infinite series

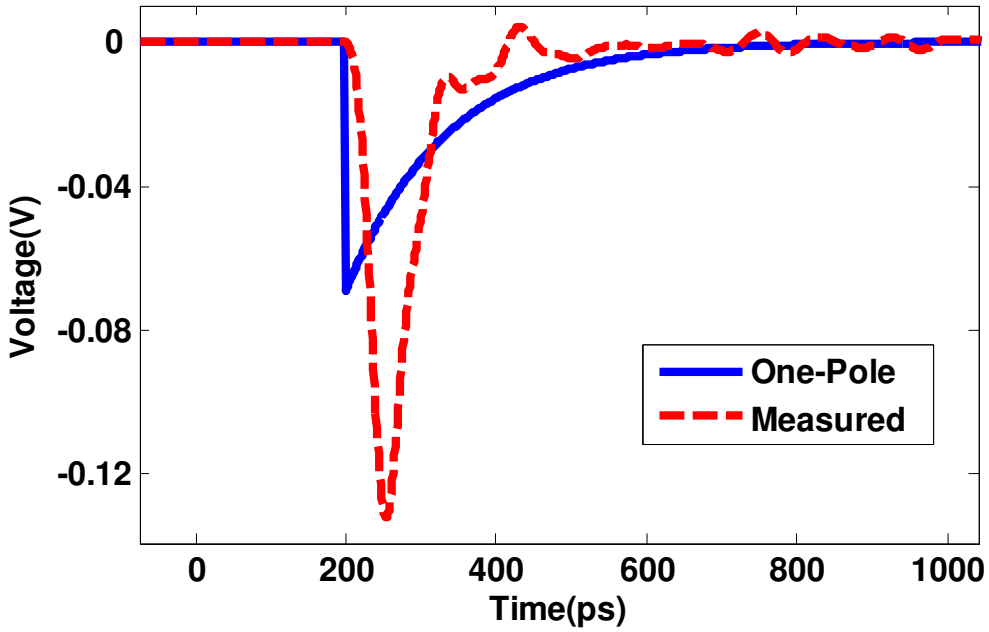

Figure 3.5: 12-inch microstrip FEXT step response: one-pole model vs measured

defined by the moments of $h(t)$ as demonstrated below [38]:

$$\begin{aligned} H(s) &= \int_0^\infty h(t)e^{-st}dt \\ &= \int_0^\infty h(t)(1 - st + \frac{s^2t^2}{2} - \frac{s^3t^3}{6} + \ldots)dt \\ &= \sum_{k=0}^{\infty} \frac{(-1)^k}{q!} s^k \int_0^\infty t^k h(t)dt \\ &= \sum_{k=0}^{\infty} s^k m_k, \end{aligned} \tag{3.19}$$

where the k^{th} moment of $h(t)$ is defined as

$$m_k = \frac{(-1)^k}{k!} \int_0^\infty t^k h(t)dt. \tag{3.20}$$

From (3.18) and (3.19),

$$(1 + a_1 s + a_2 s^2 + \ldots)(m_0 + m_1 s + m_2 s^2 + \ldots) = 1 + b_1 s + b_2 s^2 + \ldots \tag{3.21}$$

can be obtained by multiplying the denominator of (3.18) on both sides. For a two-pole approximation, (3.21) can be simplified to

$$(1 + a_1 s + a_2 s^2)(m_0 + m_1 s + m_2 s^2 + \ldots) = 1 + b_1 s. \tag{3.22}$$

Since b_2 and b_3 are equal to zero, the coefficient terms for s^2 and s^3 can be completely expressed in terms of m_k's and a_k's, which can be rearranged into

$$\begin{bmatrix} m_0 & m_1 \\ m_1 & m_2 \end{bmatrix} \begin{bmatrix} a_2 \\ a_1 \end{bmatrix} = - \begin{bmatrix} m_2 \\ m_3 \end{bmatrix}. \tag{3.23}$$

By solving the matrix equation, a_1 and a_2 can be defined in terms of m_k, where

$$\begin{aligned} a_1 &= \frac{m_3 m_0 - m_2 m_1}{m_1^2 - m_2 m_0} \\ a_2 &= \frac{m_2^2 - m_3 m_1}{m_1^2 - m_2 m_0}. \end{aligned} \tag{3.24}$$

This shows that the first four moments are required to create a two-pole model approximation.

For a distributed channel, moments can be easily determined based on the method discussed in [39]. The four moments computed are as follows:

$$\begin{aligned} m_0 &= 1 \\ m_1 &= -\frac{1}{2} RC \\ m_2 &= \frac{5}{24} R^2 C^2 \\ m_3 &= -\frac{61}{720} R^3 C^3, \end{aligned} \tag{3.25}$$

where R and C are the total lumped resistance and capacitance of the line similar to (3.12). Substituting the calculated moments in (3.25) into the two equations in (3.24),

a_1 and a_2 can be reduced to

$$\begin{aligned} a_1 &= \frac{7}{15}RC \\ a_2 &= \frac{1}{40}R^2C^2. \end{aligned} \tag{3.26}$$

The first two dominant poles of the distributed channel, p_1 and p_2, can be derived by solving

$$1 + a_1 p + a_2 p^2 = 0. \tag{3.27}$$

Given (3.26), the two poles are

$$\begin{aligned} p_1 &= \frac{4}{3}(-7 + \sqrt{26.5}) \cdot R^{-1}C^{-1} = -2.47 \cdot R^{-1}C^{-1} \\ p_2 &= \frac{4}{3}(-7 - \sqrt{26.5}) \cdot R^{-1}C^{-1} = -16.20 \cdot R^{-1}C^{-1}. \end{aligned} \tag{3.28}$$

Since the time-domain impulse response of the second-order approximation has the form of

$$h(t) = k_1 e^{p_1 t} + k_2 e^{p_2 t}, \tag{3.29}$$

the moments of $h(t)$ can be determined by directly solving (3.20) for each of the moments. The four moments of (3.29) can be characterized by [40]

$$\begin{aligned} \frac{k_1}{p_1} + \frac{k_2}{p_2} &= -m_0 = -1 \\ \frac{k_1}{p_1^2} + \frac{k_2}{p_2^2} &= -m_1 = \frac{1}{2}RC \\ \frac{k_1}{p_1^3} + \frac{k_2}{p_2^3} &= -m_2 = -\frac{5}{24}R^2C^2 \\ \frac{k_1}{p_1^4} + \frac{k_2}{p_2^4} &= -m_3 = \frac{61}{720}R^3C^3. \end{aligned} \tag{3.30}$$

In order to solve for k_1 and k_2, the poles calculated in (3.28) are substituted into any two equations from (3.30). By evaluating the resulting set of linear equations, k_1 and k_2 are computed to be

$$\begin{aligned} k_1 &= \frac{p_1^2 + \frac{1}{2}RC \cdot p_1^2 p_2}{p_2 - p_1} = 3.15 \cdot R^{-1}C^{-1} \\ k_2 &= \frac{p_2^2 + \frac{1}{2}RC \cdot p_2^2 p_1}{p_1 - p_2} = -4.49 \cdot R^{-1}C^{-1}. \end{aligned} \tag{3.31}$$

Based on (3.28) and (3.31), the second-order frequency response approximation can be denoted as

$$H(s) = \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2} = \frac{3.15 \cdot R^{-1}C^{-1}}{s + 2.47 \cdot R^{-1}C^{-1}} + \frac{-4.49 \cdot R^{-1}C^{-1}}{s + 16.20 \cdot R^{-1}C^{-1}}. \tag{3.32}$$

This in turn can be converted to a time-domain impulse response representing the two-pole model of a distributed channel, such that

$$h(t) = (\frac{3.15}{RC}e^{-\frac{2.47t}{RC}} - \frac{4.49}{RC}e^{-\frac{16.20t}{RC}}) \cdot u(t). \tag{3.33}$$

By taking the derivative of (3.33), the FEXT impulse response of the two-pole model can be calculated where

$$h_{FEXT}(t) = \tau_f[(\frac{3.15}{RC}e^{-\frac{2.47t}{RC}} - \frac{4.49}{RC}e^{-\frac{16.20t}{RC}}) \cdot \delta(t) - (\frac{7.78}{R^2C^2}e^{-\frac{2.47t}{RC}} - \frac{72.74}{R^2C^2}e^{-\frac{16.20t}{RC}}) \cdot u(t)]. \tag{3.34}$$

Using (3.33) and (3.34), the step response and its corresponding FEXT response of

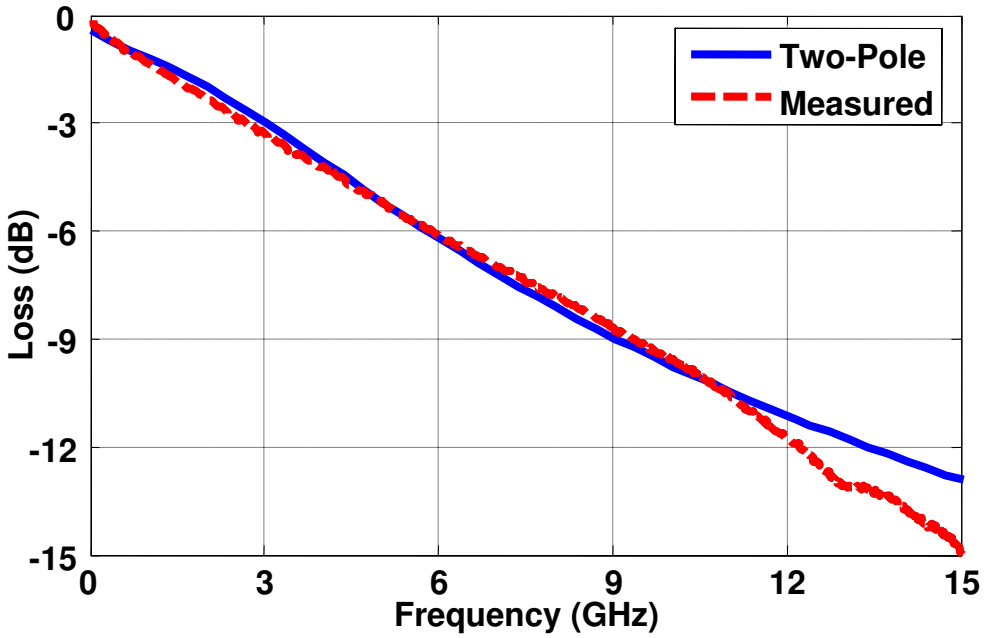

Figure 3.6: 12-inch microstrip frequency response: two-pole model & measured

a second-order channel approximation can be computed as follows:

$$\begin{aligned} s(t) &= V_{DD}(1+\frac{k_1}{p_1}e^{p_1 t}+\frac{k_2}{p_2}e^{p_2 t}) \\ &= V_{DD}(1-1.28e^{-\frac{2.47t}{RC}}+0.28e^{-\frac{16.20t}{RC}}) \qquad (3.35) \\ s_{FEXT}(t) &= \tau_f V_{DD}(\frac{3.15}{RC}e^{-\frac{2.47t}{RC}}-\frac{4.49}{RC}e^{-\frac{16.20t}{RC}}). \qquad (3.36) \end{aligned}$$

A comparison between a two-pole model and a measured frequency response for a 12-inch microstrip reveals that the model only deviates from the measurement by 2.5dB at 15 GHz as shown in Fig. 3.6. This implies that the model can accurately predict responses for data rates up to 20 Gb/s as suggested in Section 2.2.1. The step response resulting from the second-order approximation is illustrated in Fig. 3.7. As expected, the model provides a better representation of the measured response. Unlike the one-pole model,

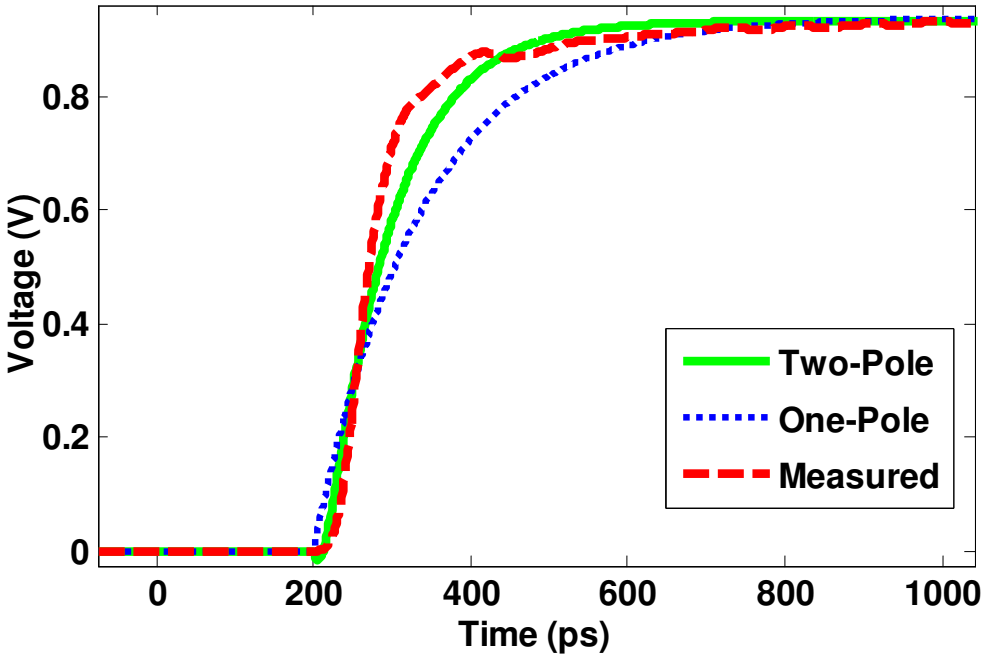

Figure 3.7: 12-inch microstrip step response: one-pole model, two-pole model & measured

the derived FEXT step response in (3.36) does not peak at $t = 0$. Instead, it roughly models the measured FEXT as shown in Fig. 3.8. Therefore, by knowing the lumped resistance, capacitance, mutual inductance and mutual capacitance, the two-pole model simplifies the impulse response of FEXT to (3.34), creating a simple equation that models weakly-coupled FEXT in high-speed serial links.

3.4 Chapter Conclusions

An accurate FEXT model is important when determining the impact of FEXT on high-speed serial link performance. Furthermore, a simple and efficient method to approxi-

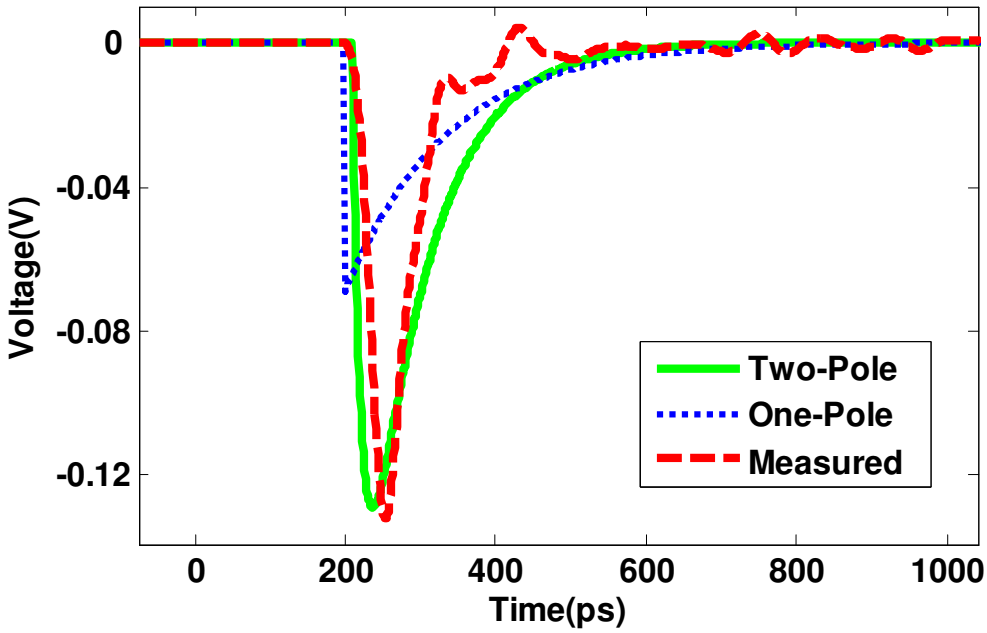

Figure 3.8: 12-inch microstrip FEXT step response: one-pole model, two-pole model & measured

mate FEXT allows fast calibration in FEXT mitigation techniques without lengthy simulations. The presented two-pole model provides a straightforward yet accurate closed-form expression through moment matching to estimate the FEXT response between two off-chip interconnects. A comparison between a two-pole model and a measured frequency response demonstrates that the model is accurate up to 15 GHz with a worst-case deviation of 2.5dB. Moreover, the second-order approximation provides an equation for an impulse response that accurately characterizes FEXT. By knowing the lumped resistance, capacitance, mutual inductance and mutual capacitance, the channel and FEXT impulse responses of the two-pole model can be computed and used to model FEXT in high-speed I/Os.

Chapter 4

A Low-Power 3×5Gb/s Multi-Lane Pseudo-Random Bit Sequence Generator

Increasing clock speeds in microprocessing cores has created a growing demand for higher data rates in inter-chip input-outputs (I/Os). This, in turn, has escalated the need for a reliable yet low-cost and low-power method for testing multi-Gb/s serial links. To avoid using expensive high-speed test equipment, on-chip pseudo-random bit sequence (PRBS) generators have been developed to provide a cost-effective way to stress wireline transceivers. The bit error rate (BER) and the jitter performance of these transceivers can be measured through the received eye diagrams produced by the PRBS [41].

As data rates continue to increase well into the multi-Gb/s region, far-end crosstalk

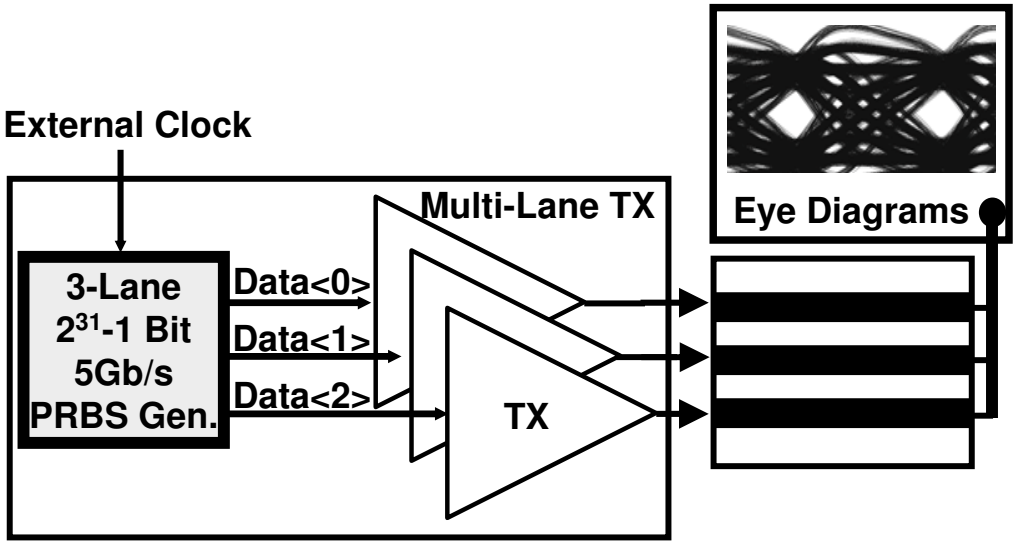

Figure 4.1: Multilane transmitter test setup with proposed PRBS generator

(FEXT) has quickly emerged as a major noise source. New research has produced high-speed serial link designs that maintain signal integrity in the presence of inter-symbol interference (ISI) and FEXT [21, 28]. In order to reduce the difficulty of testing such multi-lane transceivers, the proposed on-chip, low-power, $2^{31} - 1$ PRBS generator has been designed to generate multiple streams of synchronized data such that the FEXT between channels does not cause any significant channel-to-channel correlation as shown in Fig. 4.1. In addition, a parallel PRBS generator architecture has been exploited to further reduce power by avoiding additional phase shifting circuitry needed in traditional series architectures and employing low-power static CMOS logic to implement the lower-clock-rate linear feedback shift register (LFSR) core.

4.1 Analysis of Channel-to-Channel Correlation

Recent advances in chip-to-chip communications have created designs with multi-lane transceivers that mitigate FEXT, such as the ones described in [21, 28]. These serial link designs require multiple PRBS data streams to observe the effect of FEXT between channels. In the case of testing a single channel transceiver, a fully integrated PRBS generator that produces a $2^{31}-1$ bit pattern can stress the system with every permutation of a 31-bit sequence to determine its jitter and BERs performance. However, in a multi-lane transceiver system, besides guaranteeing that each transceiver individually operates at a low BER, it is also necessary to ensure that the interaction between adjacent serial links does not greatly reduce the system's overall jitter and BER performance. If FEXT introduces correlation between the data in adjacent channels, then it can be removed simply by a pre-emphasis equalizer. Therefore, the multiple PRBSs used to stress the multi-lane transceiver and test FEXT mitigation techniques must be generated in such a manner that for each bit period, the received signals on each of the channels are uncorrelated.

In order to ensure that FEXT is an uncorrelated noise source and its induced jitter is a bounded uncorrelated jitter, FEXT from adjacent aggressor channels should not contain any information on the bit being received by the victim channel. This can easily be done by having an independent PRBS generator for each transceiver. However, if a single PRBS generator can produce multiple streams of uncorrelated data, then the power consumption can be amortized across all the channels, reducing the power per

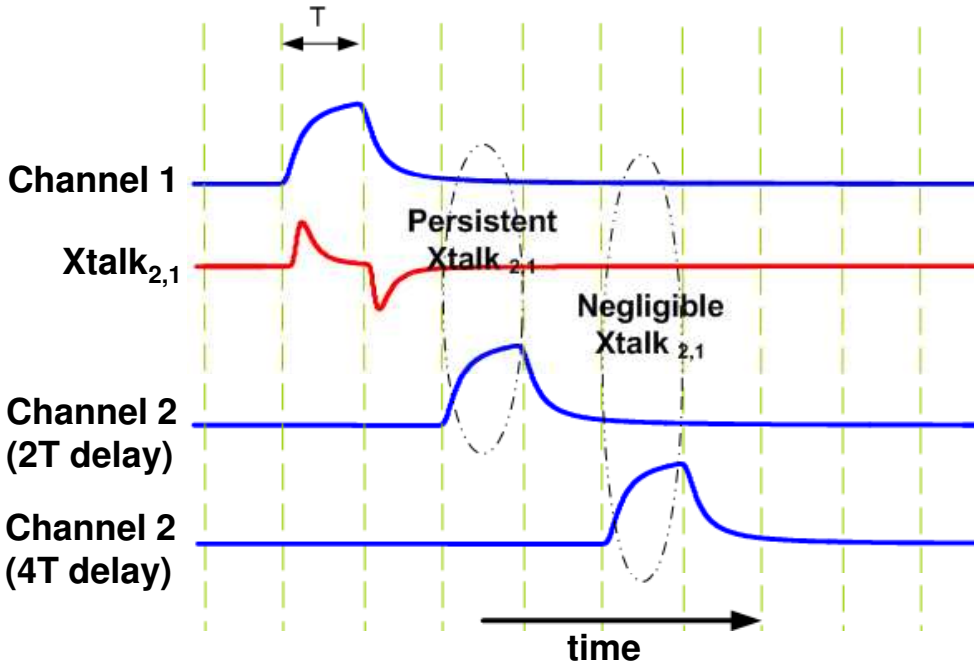

Figure 4.2: The effect of FEXT on channel 2 due to channel 1

channel significantly.

Fig. 4.2 shows a received pulse on channel 1 and the FEXT it induces in channel 2. If the multilane transmitter sends the same test pattern on both channels, the FEXT coupled from the aggressor channel will be directly correlated to the signal in the victim channel. In the given example, there is correlated FEXT in channel 2 due to the received signal in channel 1 for slightly greater than $2T$ periods. However, when the data streams in adjacent channels are separated by η clock periods (where $\eta \geq 2$), FEXT reduces to negligible values, removing any correlation between the received signals and the coupled FEXT. Stated otherwise, multiple data streams will have minimal correlation when delayed by η clock periods, where η is the number of bit times for which ISI and crosstalk

persist. In this chapter, we exploit this feature to realize a low-power, multi-lane PRBS generator by tapping different points of one LFSR to create three $4T$-delayed versions of the PRBS.

4.2 PRBS Generator Architecture

There are two primary PRBS architectures that have been developed to generate high-speed pseudo-random bit sequences. The series architecture uses a single-loop LFSR with n flip-flops operating at a data rate of R_{LFSR} to create a sub-sequence which has a length of

$$L_k = 2^n - 1. \tag{4.1}$$

To produce the final high-speed PRBS, k number of such sub-sequences spaced q bits apart are multiplexed up to the final data rate of R_{BIT}, where k and q are defined as follows,

$$k = \frac{R_{BIT}}{R_{LFSR}}, \tag{4.2}$$

$$q = \frac{L_k - 1}{k}. \tag{4.3}$$

The phase shifts between the sub-sequences require a large number of XOR gates, which grows exponentially with k [42]. Conversely, a parallel architecture outputs k phase-shifted sequences directly from a multi-loop LFSR. The LFSR implements the

function below which advances the n^{th} state, $\mathbf{S}_n$, of the LFSR by p states

$$\mathbf{S}_{n+p} = \mathbf{T}^p \mathbf{S}_n, \tag{4.4}$$

where $\mathbf{S}_{n+p}$ is the $(n+p)^{th}$ state of the LFSR and $\mathbf{T}$ is the $n \times n$ transition matrix describing the characteristic polynomial of the PRBS [43]. The final sequence is produced by multiplexing k parallel sub-sequences with a high-speed k:1 multiplexer (MUX). As shown in [41], parallel PRBS generators are much more power efficient compared to the series generators when the LFSRs are operated at a lower data rate due to the reduced overhead. This is because high-speed phase-shifting circuitry is only necessary in the series architecture. Therefore, the proposed multi-lane generator is designed using the parallel architecture to efficiently generate three high-speed $2^{31} - 1$ sequences.

Besides choosing the appropriate overall architecture, the number of multiplexing stages also influences the overall power consumption. In both architectures, the necessary operating speed of the LFSR decreases as the number of parallel sub-sequences, k, increases. Although the power consumption of the LFSR is reduced at lower operating speeds, the additional clock buffers, XOR gates, and MUXes needed to combine the parallel sub-sequences into the final high-speed PRBS can null out the power savings. However, if the LFSR operates at a data rate close to the f_T of a process, the amount of power devoted to the LFSR and its less complex clock tree increases dramatically [44]. Thus, a tradeoff between lower operating speeds and higher circuit complexity has to be made to minimize the overall power consumption.

4.2.1 3 × 12-Gb/s Multi-Lane PRBS Generator Design

A parallel $2^{31} - 1$ PRBS generator architecture has been designed to produce twelve 3-Gb/s outputs, where each of the three final 12-Gb/s maximum-length PRBS is formed by multiplexing four appropriately selected 3-Gb/s outputs. The three 12-Gb/s data streams, which have minimal channel-to-channel correlation due to FEXT, are $4T$-delayed version of the same high-speed PRBS.

Although static CMOS logic has been shown to consume less power at lower operating speeds, CML logic has been proven to expend less power at higher speeds [45, 46]. More specifically, when the maximum operation frequency is roughly $\leq$ 2.5 GHz, [46] has shown that static CMOS logic requires less power compared to CML logic in a 0.18-μm CMOS process. In order to implement a large part of the proposed design in low-power static CMOS logic, the operating speed of the LFSR, R_{LFSR}, is set to 3-Gb/s. This establishes the number of sub-sequences ($k = 4$) needed to generate each of the final data streams using (4.2). The parallel quarter-rate LFSR is realized by emulating the function,

$$\mathbf{S}_{n+4} = \mathbf{T}^4 \mathbf{S}_n, \tag{4.5}$$

where $\mathbf{T}$ represents the transition matrix of the $2^{31} - 1$ PRBS characteristic polynomial,

$$f_{31}(x) = 1 + x^{28} + x^{31}. \tag{4.6}$$

The 31-bit shift registers in the core are created using a novel low-power high-speed CMOS latch, which is described in Section 4.3.1. As shown in Fig. 4.3, the four static logic XOR gates provide the necessary feedback loops in the LFSR.

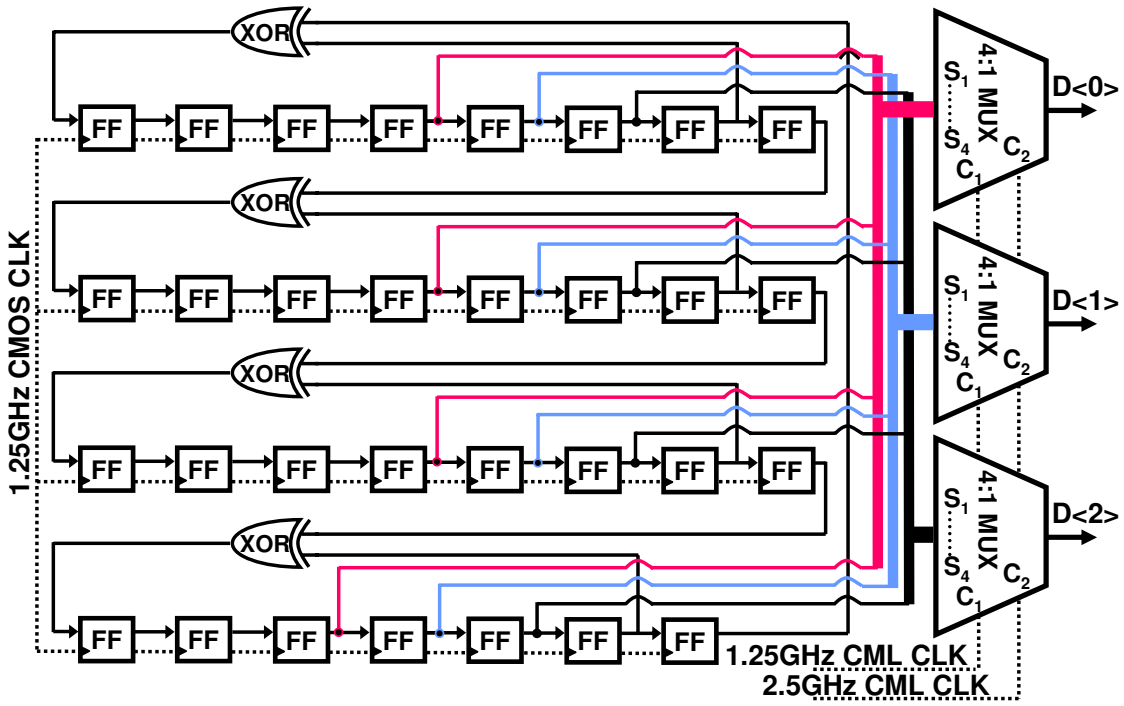

Figure 4.3: 3 × 12-Gb/s PRBS generator architecture design

The sub-sequences produced by the quarter-rate LFSR are multiplexed up to generate a 12-Gb/s PRBS through two stages of 2:1 multiplexing for each final data stream. CML MUXes are used to multiplex the data at 12 Gb/s in the proposed design. In order to operate at the final data rate, CML MUXes with modified active inductor loads have been designed for bandwidth extension, as depicted in Section 4.3.2. Note that $1T$-delayed versions of the 3-Gb/s sequence are tapped off from the LFSR so that when multiplexed together, each 12-Gb/s PRBS will be delayed by $4T$.

Through the careful selection of k and the clever partitioning of the system into static logic and CML, an ultra low-power 3×12Gb/s multi-lane PRBS generator has

been designed in a 0.18μm CMOS process. In addition, the use of a single LFSR core to generate multiple PRBS streams results in a lower power per channel compared to other designs [41, 47–49].

4.2.2 CMOS & CML Clock Distribution

The static LFSR clock is obtained by dividing the system 6GHz clock using a CML latch and then converting it to static logic levels with a CML-to-static-CMOS converter. The converter is comprised of two stages of capacitive-degenerated amplifiers that translate the common-mode level from 1.5V to 0.9V [50]. The second amplifier contains a common-mode feedback circuit that tracks the common-mode voltage of a shorted inverter and biases the output to the inverter threshold to remove process-temperature variations. The final output of the converter drives the static CMOS clock tree in the 3-Gb/s LFSR core. The delay of the static CMOS clock-path due to the CML-to-static-CMOS converter and the static CMOS clock-tree must match the delay of the CML clock-tree to ensure proper functionality.

A variable delay has been implemented in the CML clock path for post-fabrication tuning by using variable positive feedback [50]. The delay is controlled without altering the output swing by changing the current differentially through the buffer and the negative-g_m cell.

4.3 High-Speed Circuit Techniques

Two high-speed circuit blocks have been developed to operate at the speed required by the multi-lane PRBS generator design. A 3-Gb/s static CMOS latch and a 12-Gb/s CML multiplexer with modified active inductor loads are described in detail in the following sections.

4.3.1 3-Gb/s High-Speed Static CMOS Latch

A traditional high-speed static CMOS latch commonly consists of a pair of back-to-back inverters that uses two clock-controlled transmission gates to introduce incoming data through two stages of operation. The sample phase breaks the feedback loop of the inverters and samples the input voltage. During the hold phase, the latch not only retains memory, but also brings the sampled voltage to the correct output value through positive feedback since the initial sampled voltage is not pre-charged to the appropriate levels. This directly causes a longer latch time in the hold phase, as well as, indirectly increases the sampling time due to the additional loading from the larger back-to-back inverters at the storage nodes.

In order to increase the latch's maximum achievable frequency of operation, the sampling time and the latch time must be reduced, which are defined as follows. The sampling time of the latch to get to 90% of the final value is given by

$$T_{samp} = 2.2 \cdot R_{on} \cdot C_L \tag{4.7}$$

where R_{on} is the resistance of the switches and C_L is the effective capacitance at the

output nodes [51]. The latch time is given by

$$T_{latch} = \frac{KL^2}{\mu V_{eff}} log_{10}(V_{logic}/V_0) \tag{4.8}$$

where K is a constant, L is the device length, μ is the mobility, V_{eff} is the overdrive voltage, V_{logic} is the output swing of the latch, and V_0 is the voltage at the end of the sample phase [52].

As depicted in (4.8), the latch time T_{latch} is inversely proportional to the voltage V_0. Thus, by bringing V_0 closer to the final output level as it enters the hold phase, a latch will achieve a shorter latch time. A shorter latch time also implies that smaller inverters are needed for the regenerative structure since they are only required to maintain memory. By reducing C_L at the storage nodes, (4.7) asserts that the sampling time will also decrease. In the proposed latch design, we take advantage of these observations to create a faster latch.

The improved 3-Gb/s static CMOS latch used in the quarter-rate LFSR is shown in Fig. 4.4. During the sample phase, both storage nodes (Q, QZ) are pre-charged by gating the series NMOS and PMOS switches with the clock and data signals. Once the voltage is sampled, the latch enters the hold phase. All the switches are opened and the latch utilizes positive feedback to maintain the sampled value. Since the outputs are already pre-charged to their final values, the regenerative back-to-back inverters can be minimally sized, significantly reducing the parasitic capacitance at the storage nodes, thereby enabling the pre-charge switches to operate at higher speeds. However, due to the decreased storage capacitance, the output nodes are now more susceptible to coupling

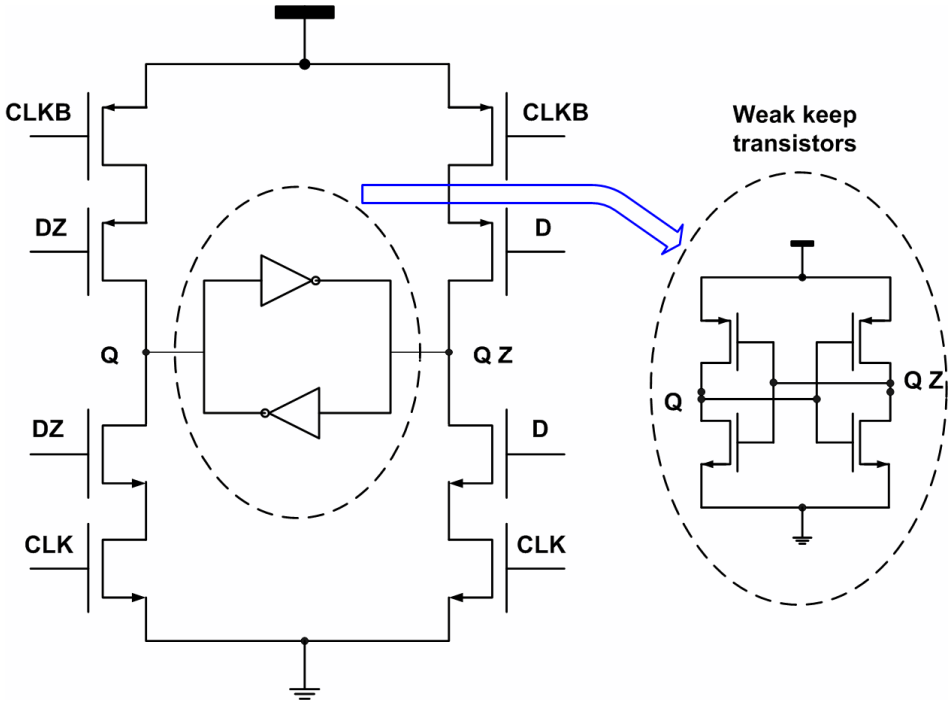

Figure 4.4: Schematic of a 3-Gb/s CMOS latch

from nearby lines. Thus, careful layout is vital to guarantee minimal coupling between the noisy nodes and the sensitive storage nodes.

It is important to note that the highest speed that can be achieved from this architecture is now limited by the total R_{on} of the two PMOS switches in series, which is approximately

$$R_{on} \approx \frac{2}{g_m}. \tag{4.9}$$

Since the PMOS switch is roughly sized 2× larger than the NMOS switch, the input capacitance of the latch C_{IN} becomes

$$C_{IN} = 3 \cdot (C_{GS} + C_{GD}), \tag{4.10}$$

where C_{GS} is the gate-to-source capacitance and C_{GD} is the gate-to-drain capacitance. The latches in the proposed PRBS generator are designed to have a maximum fan-out of two, thereby indicating that the load capacitance, C_L, at the output node is

$$C_L = fanout \cdot C_{IN} = 2 \cdot C_{IN}. \tag{4.11}$$

Based on (4.9), (4.10), and (4.11) and assuming a 50% duty cycle, (4.7) simplifies to

$$F_{max} = \frac{1}{2 \cdot T_{samp}} \approx \frac{f_T}{4.4 \cdot fanout}. \tag{4.12}$$

The maximum achievable frequency is a fraction of the f_T of the slowest device. Since PMOS devices have a low f_T in a 0.18-μm CMOS process, its f_T of approximately 13-GHz limits the maximum attainable frequency to about 2 GHz which matches simulation results [51]. However, the speed is roughly 2$\times$ of a traditional latch operating in the same process.

4.3.2 12-Gb/s CML MUX with Modified Active Inductor Loads

In order to operate at 6 GHz, a simple PMOS load is insufficient in the high-speed CML MUX due to the lower f_T of the PMOS device in a 0.18-μm CMOS process. The speed of the MUX can be increased slightly by using resistive loads since the limiting factor in this case becomes the RC constant at the output nodes. However, for a full peak-peak swing of 0.5 V at 12 Gb/s, the bandwidth of the CML MUX must extend beyond 8.4 GHz or 70% of the data rate to reduce distortion and increase SNR [20]. There are several existing bandwidth extension methods such as the usage of peaking inductors or Cherry-Hooper

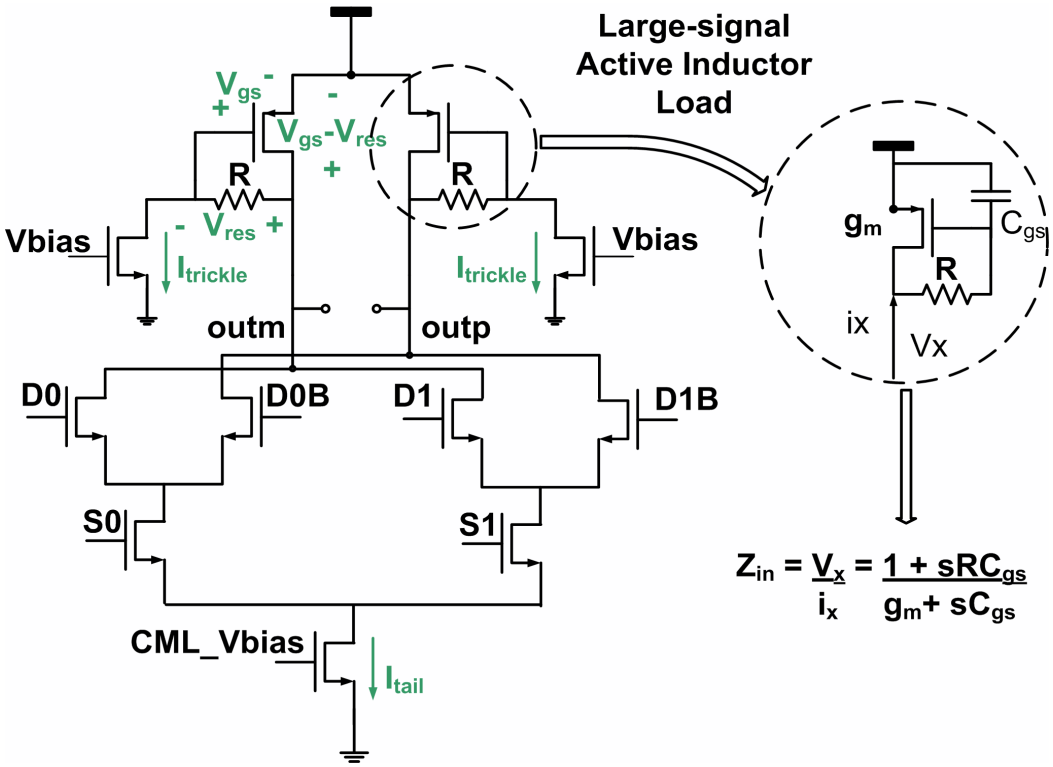

Figure 4.5: Schematic of a 12-Gb/s CML MUX with active inductor loads

amplifiers [50]. Although both techniques extend the bandwidth, inductive peaking requires too much area for its inductors and the Cherry-Hooper amplifier consumes too much power. Active inductor loads have also been used to boost bandwidth for small signal swings [50]. However, as the current through the load varies during large voltage swings, the g_m of the PMOS fluctuates significantly, causing duty cycle distortion in its large signal behavior, which in turn increases transmit jitter. Furthermore, headroom is severely limited due to the diode voltage drop introduced by the PMOS.

The high-speed CML MUX uses the modified active inductor loads, shown in Fig. 4.5,

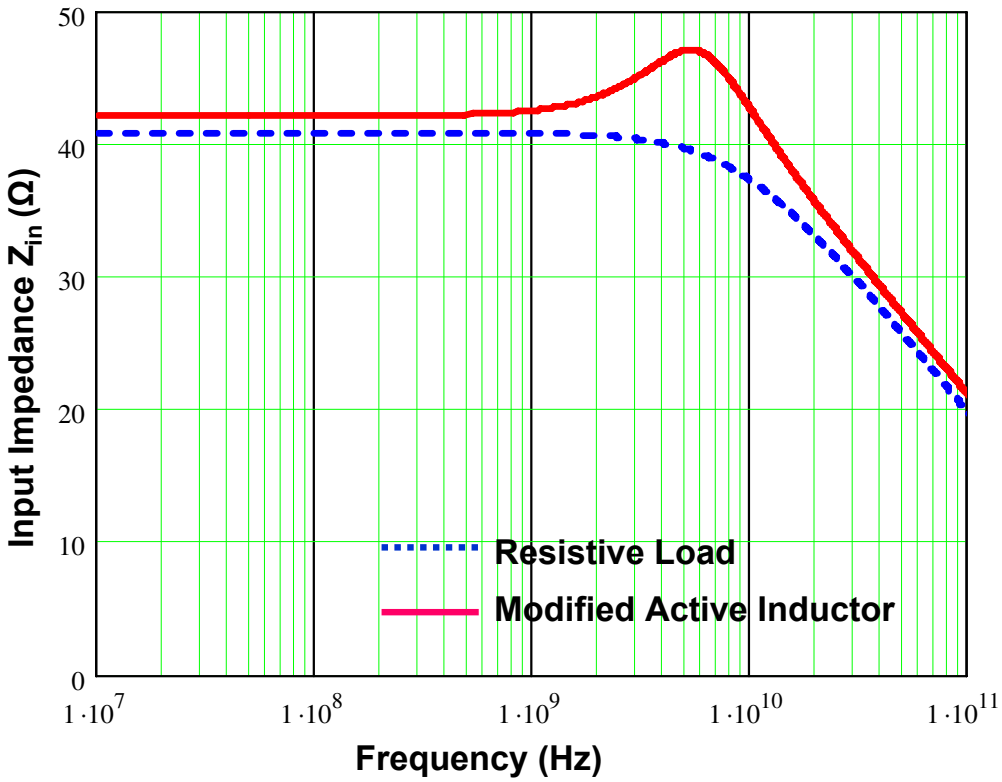

Figure 4.6: Bandwidth comparison of a MUX w/ resistive load & w/ modified active inductor load

to provide bandwidth boosting. The traditional active inductor load is modified by inserting a trickle current source at the gate of the PMOS. This improves the bandwidth of the circuit for large signal swings through three mechanisms. First, headroom is increased by causing a voltage drop across the resistor so that $V_{DS} < V_{GS}$, which increases the headroom by approximately 0.3 V. Second, the trickle current supplies current to the PMOS during the "off" state so that g_m is only 3 to 4 times lower compared to g_m during the "on" state. The load impedance equation in Fig. 4.5 shows that by reducing

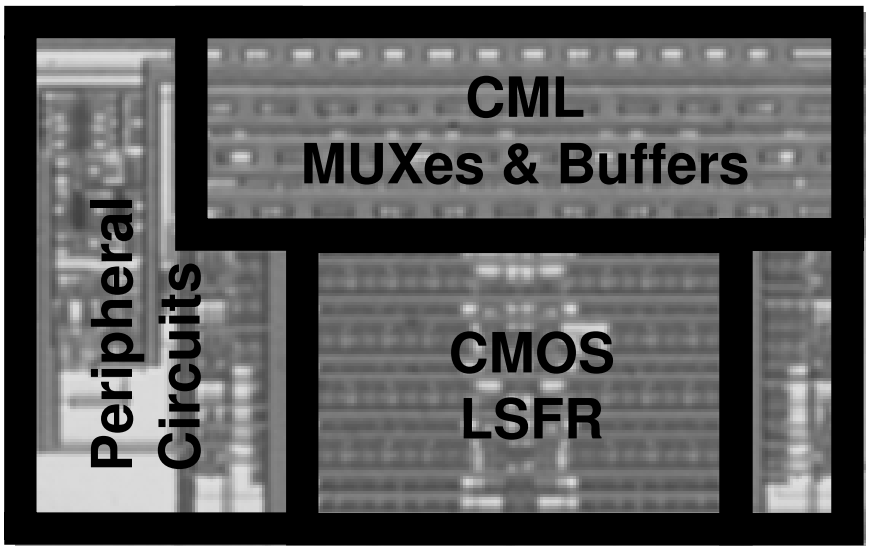

Figure 4.7: Test chip micrograph

the variation in g_m, the load impedance fluctuates much less even with the introduction of an inductive term [51]. This means that the effective impedance remains relatively steady during large swings. Third, a constant current is continuously applied to the PMOS providing it with extra drive capability. Simulation results as depicted in Fig. 4.6 show that with only an additional power overhead of 25%, the modified active inductor load extends the bandwidth by 2× from 5 to 10 GHz, increases the output swing and minimizes distortion during large signal swings.

4.4 Experimental Results

The high-speed multi-lane PRBS generator has been fabricated in the 0.18-μm TSMC CMOS process. Although the PRBS generator was designed to operate at 12-Gb/s,

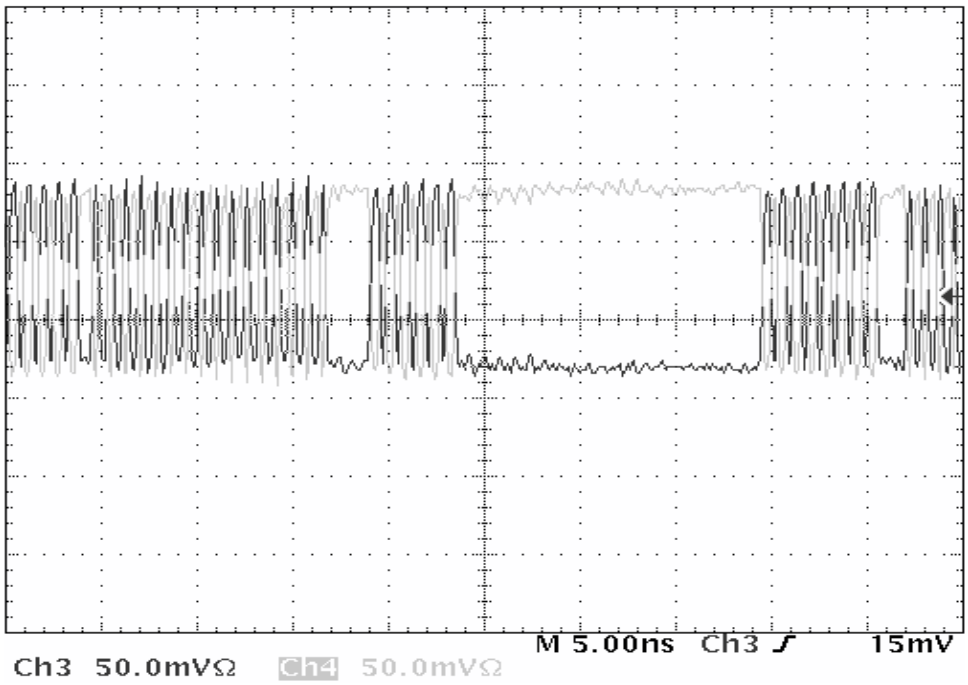

Figure 4.8: Transient measurement of the 5-Gb/s PRBS

measurement results have only been acquired at 5-Gb/s due to poor packaging parasitics and test setup limitations to measure transient signals. However, a 6-GHz phase-locked loop (PLL), which uses the same 12-Gb/s CML MUX described in Section 4.3.2, has been verified to operate at 6 GHz on the same test chip through probe measurements. The chip microphotograph, shown in Fig. 4.7, occupies an area of 500μm×700μm and consumes 131mW per lane while operating at 5 Gb/s. Simulated power at 12 Gb/s uses 262 mW per lane.

In order to observe the 5-Gb/s PRBS, the chip was placed in an open-cavity LQFP package, which was then soldered to a FR4 PCB test board. The final data stream is transmitted using a tapered CML buffer with 50Ω loads through a SMA connection

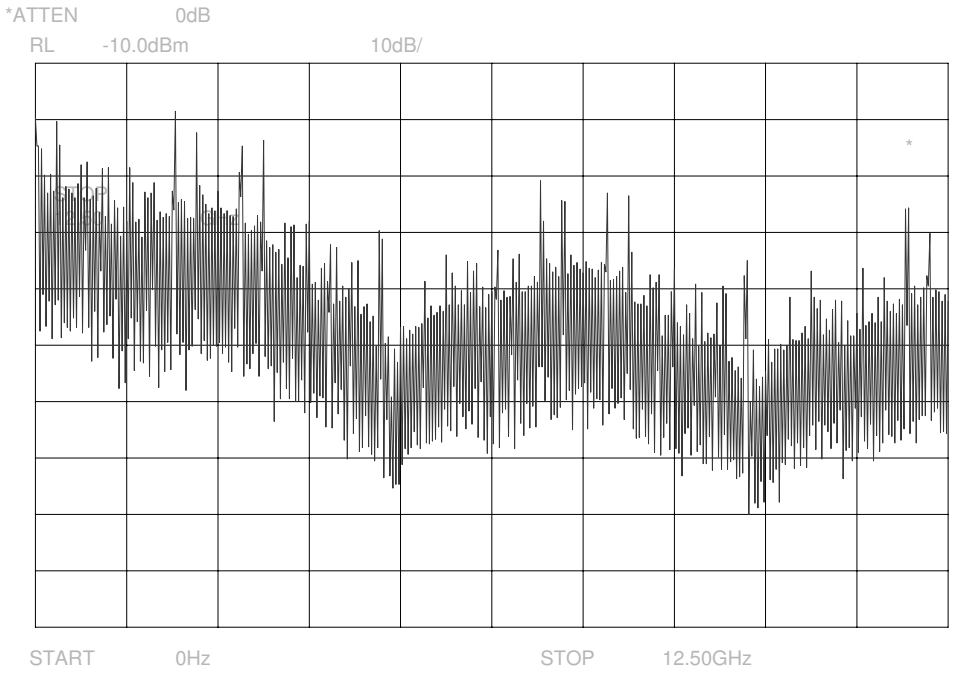

Figure 4.9: Power spectra density of the 5-Gb/s PRBS

to a Tektronix TDS 6804B oscilloscope and an Agilent 8563 spectrum analyzer. The 5-Gb/s data stream is generated by supplying a 2.5-GHz clock with a Cascade GSG probe. The transient waveform shown in Fig. 4.8 depicts rise and fall times of 54 ps. For a nonreturn-to-zero (NRZ) PRBS with a pattern length of L_p, the power spectra density should contain discrete spectral lines separated by

$$\frac{R_{BIT}}{L_p} = 2.3Hz, \tag{4.13}$$

where R_{BIT} is the bit rate of the NRZ data. However, the spectrum analyzer used did not have sufficient spectral resolution to show these discrete spectral lines. The measured total power spectra density of the 5-Gb/s PRBS is illustrated in Fig. 4.9, which has nulls at 5 and 10 GHz as expected for a 5-Gb/s NRZ spectrum.

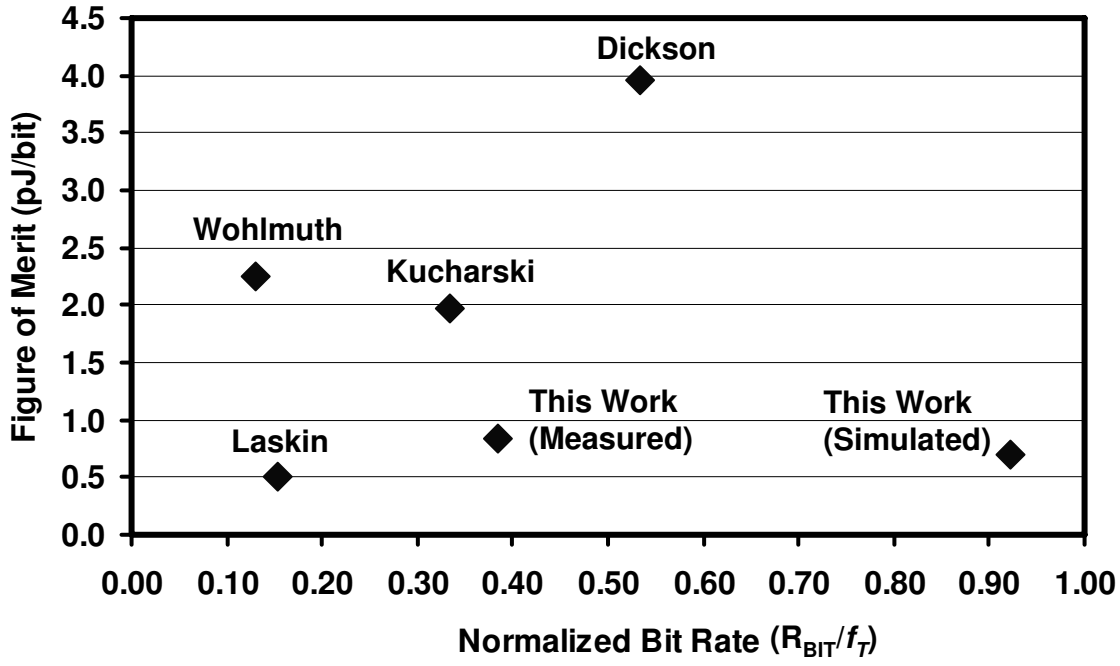

Figure 4.10: FOM comparison with previously published results

For proper comparisons with previously published designs, a figure of merit (FOM) has been defined as,

$$FOM = \frac{P}{log_2(L_p) \cdot R_{BIT}} \tag{4.14}$$

where P is the power, L_p is the bit length, and R_{BIT} is the bit rate [41]. To compare designs from different processes, the FOM is plotted against R_{BIT}/f_T, which is a measure of how close the data rate is to the f_T of the process, thereby providing a first-order metric independent of the process technology. The ideal PRBS design will have the highest R_{BIT}/f_T and the lowest FOM possible. Using (4.14), we have calculated the measured and simulated FOM per lane to be 0.84 pJ/bit and 0.70 pJ/bit, respectively. As shown in Fig. 4.10, the presented PRBS generator has the lowest FOM by 2.6× with a much

higher R_{BIT}/f_T compared to prior CMOS designs [47]. Furthermore, our design has one of the lowest FOM compared to previously published SiGe BiCMOS results [41, 48, 49].

4.5 Chapter Conclusions

A 3 × 12-Gb/s, $2^{31} - 1$ multi-lane PRBS generator has been fabricated in the 0.18-μm TSMC process to stress a prototype multi-lane FEXT cancellation transmitter. It employs a CMOS latch optimized for high-speed and a CML MUX with modified active inductor loads for bandwidth extension. A trickle current source is added to the traditional active inductor load to provide a better large-signal behavior. The prototype has been tested at 5 Gb/s and demonstrated a FOM per lane of 0.84 pJ/bit, which is better than other previously published designs. The implementation of the parallel architecture with careful partitioning of CMOS and CML allows ultra-low power consumption per lane, making this a cost-effective method for on-chip I/O testing. Furthermore, by creating $4T$-delayed versions of the 12-Gb/s PRBS, the system is able to produce multiple data streams that have minimal channel-to-channel correlation due to FEXT.

Chapter 5

FEXT Shifting: Staggered I/Os

Increasing on-die bandwidth in microprocessors has created a growing demand for faster off-chip links [3]. Besides enhancing the data rates of individual links, a greater number of serial links must be crowded into a finite area to accommodate the higher aggregate data throughput requirement. In a space-limited, multi-lane I/O communication system, the data rate of each link becomes severely limited by inter-symbol interference (ISI) and crosstalk at multi-Gb/s transmission.

As data rates increase, interconnects used in off-chip communication begin to behave like lossy transmission lines, severely degrading the signal integrity of the transmitted data. These interconnects mainly suffer from ISI, which is caused by frequency-dependent attenuation in high frequencies. To make matters worse, in order to boost the aggregate data rate, the interconnect density is increased by expanding the number of parallel lanes in a given space. The reduced trace separations between the interconnects cause

the transmitted signals to couple significantly more energy into neighboring channels [4]. This induced electromagnetic coupling in unidirectional I/Os appears as far-end crosstalk (FEXT) [16].

As shown in Fig. 5.1, serial links are more susceptible to FEXT at higher data rates because signal magnitude decreases with frequency while FEXT magnitude increases with frequency, which lowers the effective signal-to-noise-and-interference ratio (SNIR). Furthermore, FEXT introduces deterministic jitter (DJ) in the received signal by altering the amplitude of the signal at the threshold-crossing points. This reduces the sampling range of the data as well as the horizontal opening of the data eye, thereby degrading the receiver's bit error rate (BER) performance [28]. Therefore, minimizing the effect of FEXT is critical in realizing a high-speed I/O with a low BER.

Equalization techniques, such as transmit pre-emphasis and receive decision-feedback equalization, have been widely used to mitigate the impact of ISI on link performance. Techniques to cancel FEXT have also been explored in recent years [28,53,54]. However, most of these methods do not ameliorate the detrimental effects of high-frequency FEXT on timing jitter. Although [28] and [21] have successfully reduced crosstalk-induced jitter (CIJ), both implementations require additional chip area and expend noticeable amounts of power.

In order to reduce CIJ in existing external communication interfaces, the transmitter architecture presented in this chapter improves the timing margin (TM) of the received data with negligible area and power overhead by shifting the FEXT noise from

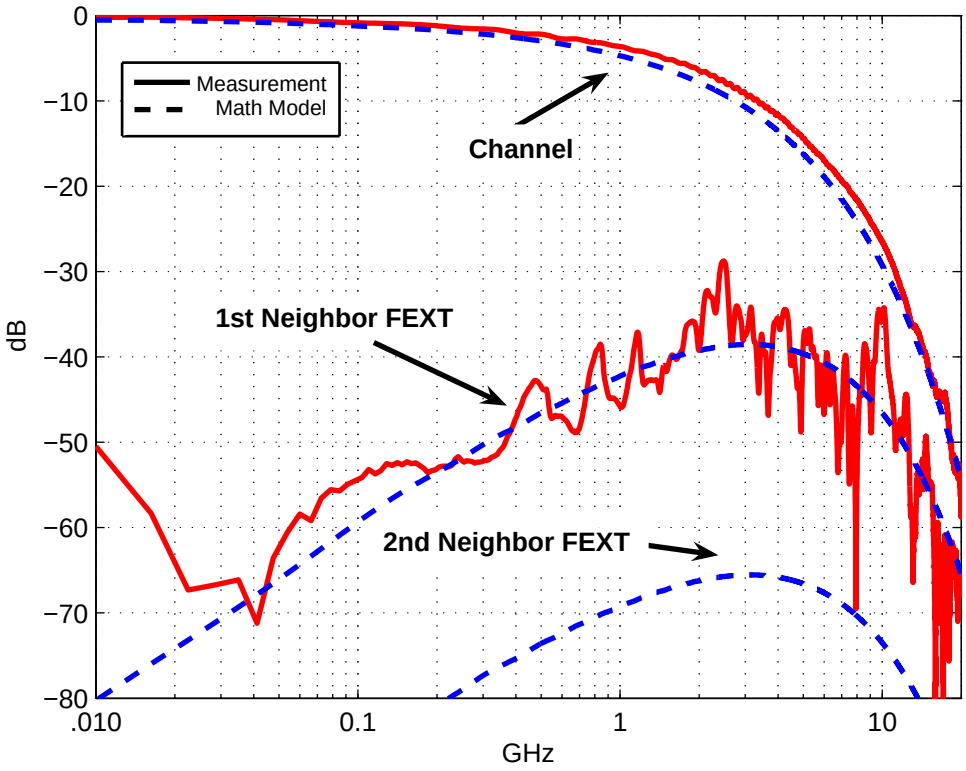

Figure 5.1: Measured & modeled channel, 1N-FEXT & 2N-FEXT responses

the threshold-crossing points to the peak of the vertical eye opening. In the case of DDR2, this is achieved while staying within the voltage margin (VM) limits defined in the recommended SSTL_18 standard by JEDEC as suggested by the DDR2 SDRAM Specification [55, 56]. The proposed technique offers an efficient method to reduce trace separations in parallel I/Os for a given BER without major system re-design when excess voltage margin is available.

The remainder of this chapter is organized as follows. In Section 5.1, an analysis of the different excitation modes in coupled transmission lines is briefly discussed. Section 5.2 provides an mathematical analysis of FEXT mitigation using the proposed staggered

I/O. In Section 5.3, the staggered I/O system architecture is described in detail, while comparing it to existing FEXT mitigation techniques. Simulation and measurement results are presented in Section 5.4 to demonstrate the benefits of staggered I/Os. Lastly, the chapter concludes with a summary of the research findings in Section 5.5.

5.1 Excitation Mode Analysis for Coupled Transmission Lines

Far-end crosstalk (FEXT) is one of the primary interference/noise sources that prevents higher data throughput in parallel point-to-point I/O interfaces [3]. It is induced by electromagnetic coupling through the mutual inductance and capacitance between two links. This deleterious effect can be modeled with the help of coupled transmission lines. By solving the telegrapher's equations that depict the voltage and current of two coupled transmission lines with respect to distance and time, three modes of excitation are established in source-synchronous transmission [16]. The even mode is stimulated when data transitions on adjacent lines occur in the same direction at the same time, while the odd mode is stimulated when data transitions occur in the opposite direction. The superposition mode takes place when there is no data transition in the aggressor line.

The three excitation modes cause the data transitions on the lines to have slight differences in their propagation times. As derived in [21], the even and odd mode propagation times, T_e and T_o, can be represented as variations from the superposition mode

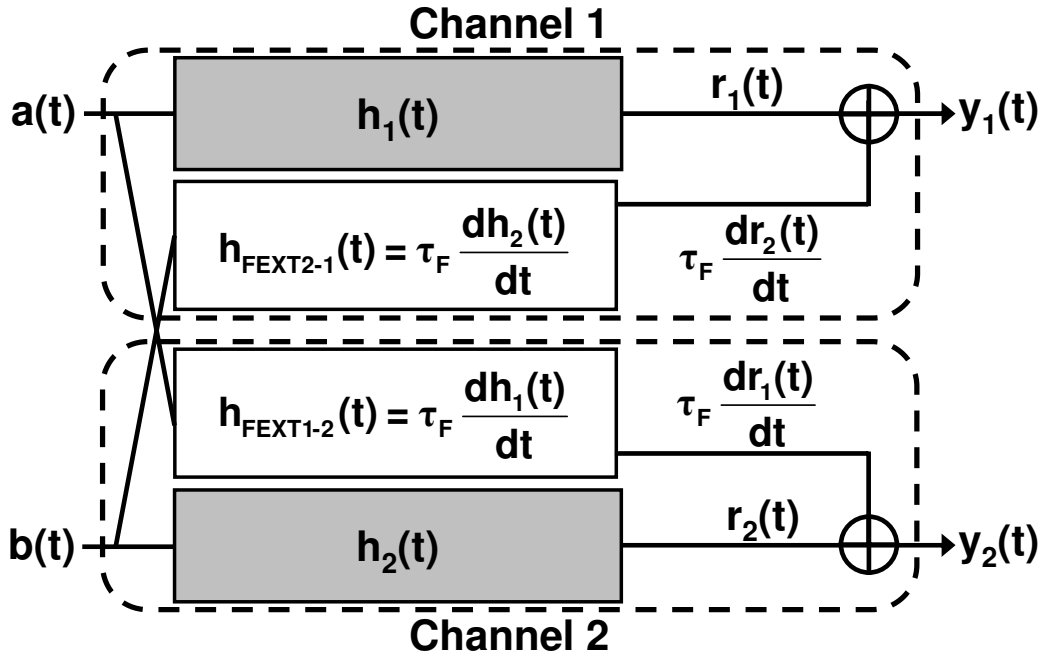

Figure 5.2: 1N-FEXT and channel model for two coupled transmission lines

propagation time T,

$$T_{o(e)} \approx T \pm \frac{l}{2}(C_m Z_0 - \frac{L_m}{Z_0}). \tag{5.1}$$

Moreover, the fluctuations in (5.1) can be denoted as a forward coupling time constant, τ_f, which accurately defines a high-pass filter that produces a FEXT impulse response, $h_{FEXT}(t)$, where τ_f is given by (3.2) [16, 21].

As shown in Fig. 5.2, each channel in the coupled transmission lines can be characterized by the summation of the channel response and the FEXT response due to the adjacent aggressor channels [28].

Although any neighboring aggressor lines can contribute to the total FEXT noise, only the nearest adjacent lines (1N-FEXT) have been included to simplify the channel

model. This is a reasonable approximation since FEXT diminishes by an estimated factor of D^{-2}, where D is the trace separation between two microstrip lines as depicted in Fig. 5.3 [17]. To further reinforce this point, Fig. 5.4 shows that the voltage peak of the second neighbors' FEXT (2N-FEXT) is roughly 20 times smaller than the voltage peak of 1N-FEXT, therefore the amplitude perturbation due to 2N-FEXT and beyond can be considered negligible. Hence, mitigating only the effects of 1N-FEXT is sufficient for improving the jitter of the received signal.

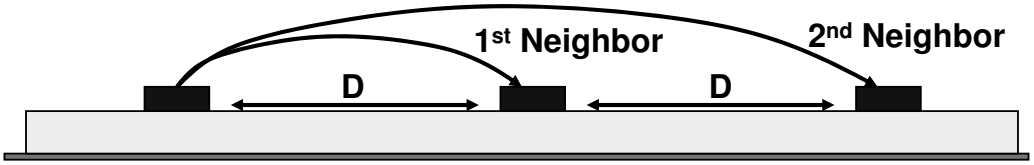

Figure 5.3: Three channels with D trace separation

5.2 Staggered I/O FEXT Mitigation Analysis

In a source-synchronous I/O architecture, all the lines are assumed to have the same length and the data transmitted in each line are timed with the same clock. This implies that the data transitions in adjacent lines are aligned such that the FEXT introduced by an aggressor occurs during a transition in the received victim signal.

When a data transition is transmitted at $t = 0$ in an environment with no aggressor-induced FEXT as shown in Fig. 5.5, the threshold-crossing time of the transition, t_c, is

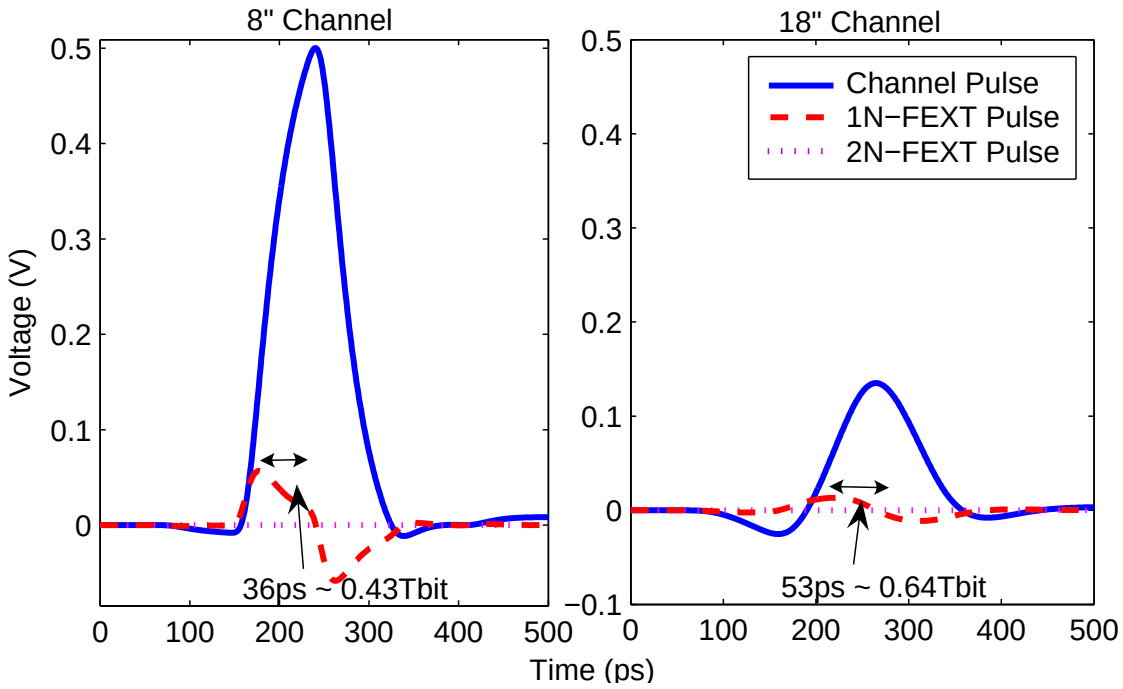

Figure 5.4: Channel, 1N-FEXT & 2N-FEXT pulse responses after pre-emphasis for 8" and 18" microstrips at 12Gb/s

calculated by manipulating the equation

$$y_1(t_c) = r(t_c) = v_{th}, \tag{5.2}$$

where $y_1(t)$ is the received signal at the receiver input and v_{th} is the threshold voltage [4]. However, in the presence of FEXT, the arrival time of the data transition at the decision threshold, t_x, is determined by solving the following equation,

$$y_2(t_x) = v_{th} = r_2(t_x) + \tau_f \frac{dr_1(t_x)}{dt} \tag{5.3}$$

where channel 1 is the aggressor line, channel 2 is the victim line and $r_1(t)$ and $r_2(t)$ are the received signals of channel 1 and channel 2 without FEXT.

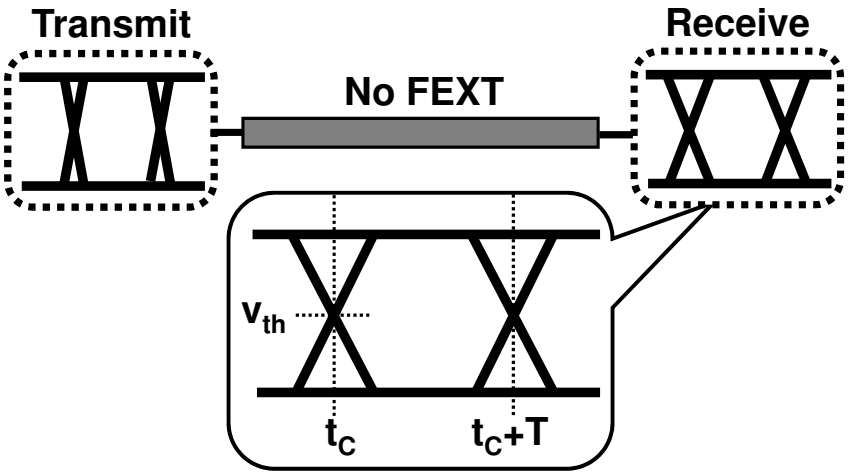

Figure 5.5: Single I/O and an eye diagram at its receiver input with no FEXT

A typical eye diagram of the received victim signal is depicted in Fig. 5.6, revealing three distinct threshold-crossing times, t_1, t_c, and t_2. The difference in the propagation times is due to the three possible excitation modes between the two coupled transmission lines. As described in (5.1), t_1 and t_2 correspond to the even and odd mode propagation times, which are approximately

$$t_1 = t_c - \tau_f$$

$$t_2 = t_c + \tau_f. \tag{5.4}$$

Therefore, the variation of the threshold-crossing time due to CIJ is roughly $2\tau_f$.

It is important to realize that CIJ is only introduced when a data transition simultaneously occurs in both the victim and the aggressor lines since the induced FEXT alters the threshold-crossing point during the transition in the victim line [28]. If a transition in the victim data takes place at a time when there is no transition in the aggressor data,

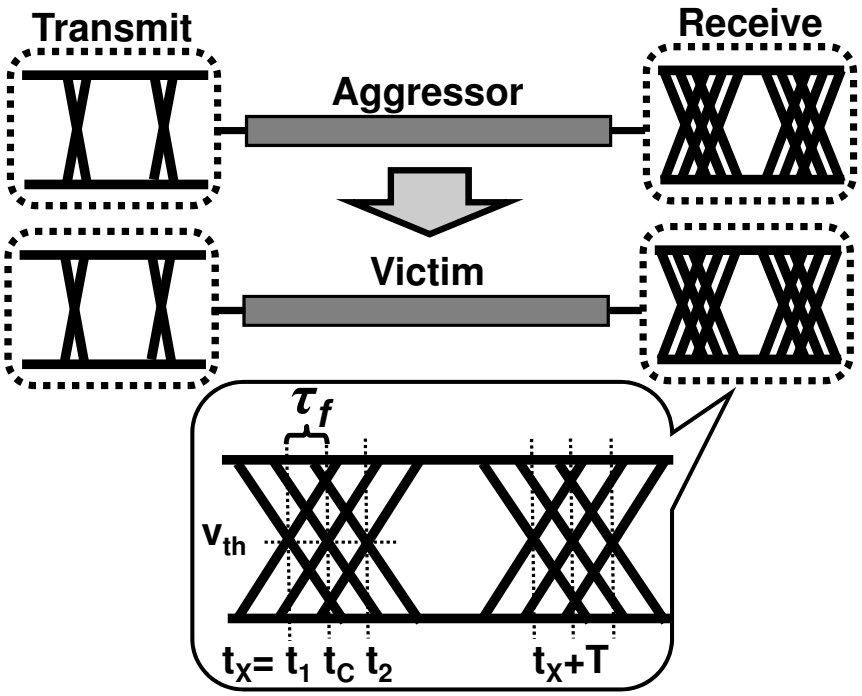

Figure 5.6: Two coupled source-synchronous I/Os and the received eye diagram

then the threshold-crossing time remains unchanged. This fact is exploited in Fig. 5.7.

A 90° phase shift is established between the data being transmitted in the two channels in order to position the transitions in the victim data at the center of the aggressor's vertical eye opening. Similar to the previous analysis of (5.3), the arrival time of the data transition at the decision threshold in the victim line, t_s, is determined by solving the modified equation below,

$$y_2(t_s) = v_{th} = r_2(t_s) + \tau_f \frac{dr_1(t_s)}{dt} \approx r_2(t_s) \tag{5.5}$$

where channel 1 is the aggressor line and channel 2 is the victim line. Since the FEXT term in (5.5) is proportional to the derivative of the received aggressor signal, $r_1(t)$, negligible FEXT noise is introduced when $r_1(t)$ does not change significantly with respect

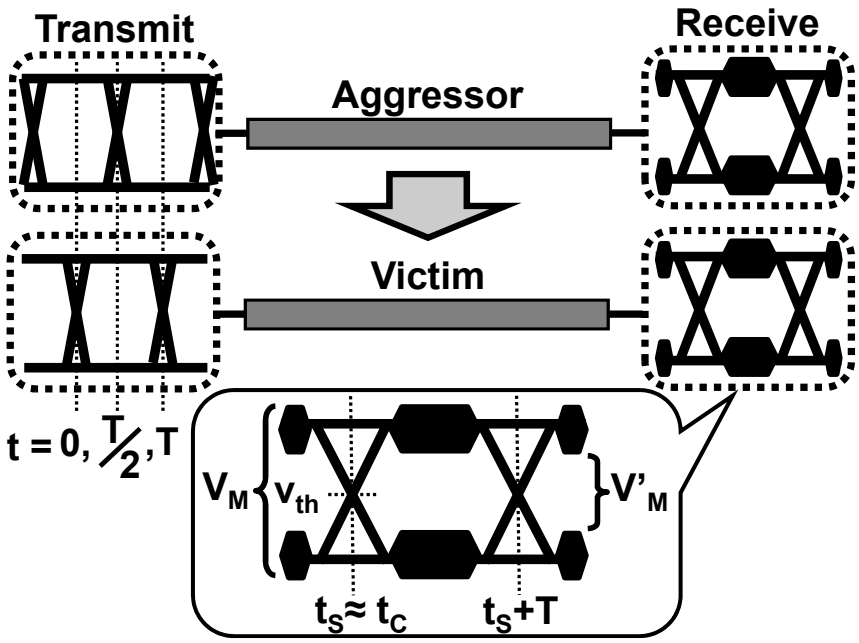

Figure 5.7: Two coupled "staggered" I/Os and the received eye diagram

to time. In this case, the aggressor data has reached its digital level while a transition in the victim data is taking place, implying that the derivative of $r_1(t)$ with respect to time evaluated at t_s is approximately zero. Thus, (5.5) is reduced to (5.2), which is used to determine the threshold-crossing time in Fig. 5.5 when there is no FEXT present.

As shown in Fig. 5.7, the aggressor signal does not introduce any CIJ, thereby improving the peak-to-peak TM by $2\tau_f$. However, the new VM, V'_M, is lower than the original VM, V_M, because the aggressor now injects FEXT in the middle of the victim's vertical eye opening. The amount of reduction can be determined by estimating the level of FEXT noise that is coupled during a transition in the aggressor data. A first-order

approximation of FEXT is given by

$$\tau_f \frac{dr_1(t_s)}{dt} \approx \tau_f \frac{V_{pp}}{t_{rise}} \tag{5.6}$$

where V_{pp} is the peak-to-peak received voltage and t_{rise} is the rise/fall time of the received data transition. Assuming that there are no other noise sources, the nominal V_M is roughly V_{pp}. An expression for the reduced VM, V'_M, in terms of V_M can be derived as follows,

$$V'_M = V_M(1 - \frac{2\tau_f}{t_{rise}}). \tag{5.7}$$

This is an interesting result because it clearly illustrates that when a 90° phase-shift is inserted between adjacent lines, V'_M can be increased by having slow transitions. In a typical source-synchronous I/O, CIJ is not sensitive to the transition slope [21]. Although decreasing the slope induces less FEXT noise, the slower edges become more susceptible to CIJ at the threshold-crossing points. Therefore, simply changing the sharpness of the data edge does not reduce CIJ. However, when adjacent data streams are "staggered" as shown in Fig. 5.7, CIJ is significantly reduced, and the VM can be maximized by changing the transition slope. We will exploit the observations seen in this analysis in the proposed staggered I/O (SIO) architecture.

5.3 Staggered I/O Architecture

The architecture presented in Fig. 5.8 consists of multiple I/Os that are synchronized in a "staggered" manner such that the transmitted signals in adjacent lines are offset by a

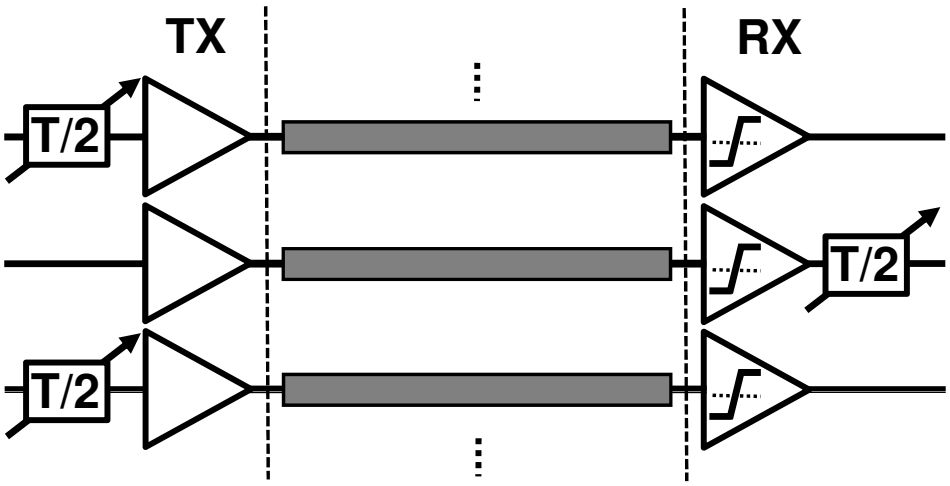

Figure 5.8: Staggered I/O system architecture

known delay. CIJ is decreased in this proposed architecture because the FEXT induced by neighboring aggressor signals are specifically positioned away from the threshold-crossing points of the victim signal. This is easily realized by inserting variable delays on the transmit end of alternating channels. Note that the receiver also has variable delays added to the remaining channels in order to properly realign the final output in each lane.

The amount of delay necessary for minimizing CIJ depends on the channel loss and the line separation since these are the physical factors that determine the actual shape of FEXT. The data in every other line is delayed by a fractional amount of bit-time (T_{bit}) relative to the data transmitted in the neighboring lines. The delay can be adjusted to shift the data transitions in adjacent aggressor signals to ensure that the coupled FEXT occurs at the center of the victim signal's data eye.

The presented method of lowering CIJ can increase the TM of each channel with almost no increase in power consumption except for the small amount of power required for a single variable delay per channel. However, it comes at a cost of decreasing the existing VM, thereby reducing the SNR of the signal at the moment when it is sampled by the receiver. Therefore, in order to benefit from the proposed architecture and still meet a low BER requirement, an excess amount of VM is necessary such that the slicer at the receive end can still discern between a "1" and a "0" even after the decrease in SNR. This is the case in short DDR2 interfaces that follow the SSTL_18 standard [55,56]. Assuming that the receiver offset is negligible, the following relationships must be met to achieve a given BER,

$$S_{min} \geq V'_M \tag{5.8}$$

$$J_{sample} \leq T'_M \tag{5.9}$$

where S_{min} and J_{sample} are the minimum receiver sensitivity and sampling jitter for a given BER, V'_M is the reduced VM, and T'_M is the improved TM.

Besides the amount of loss in the interconnects, large timing skews between different channels due to unequal interconnect lengths as shown in Fig. 5.9 and clocking variations can also limit the effectiveness of the architecture. The issue has been resolved by using a variable delay for deskewing with a maximum delay of $1T_{bit}$ and a default setting of $0.5T_{bit}$. If the transition edge of the aggressor occurs at t_P which precedes the center of the victim's data eye t_O, the variable delay can shift the aggressor signal by $t_O - t_P$ to remove the unwanted timing variation. On the other hand, if the data transitions in the

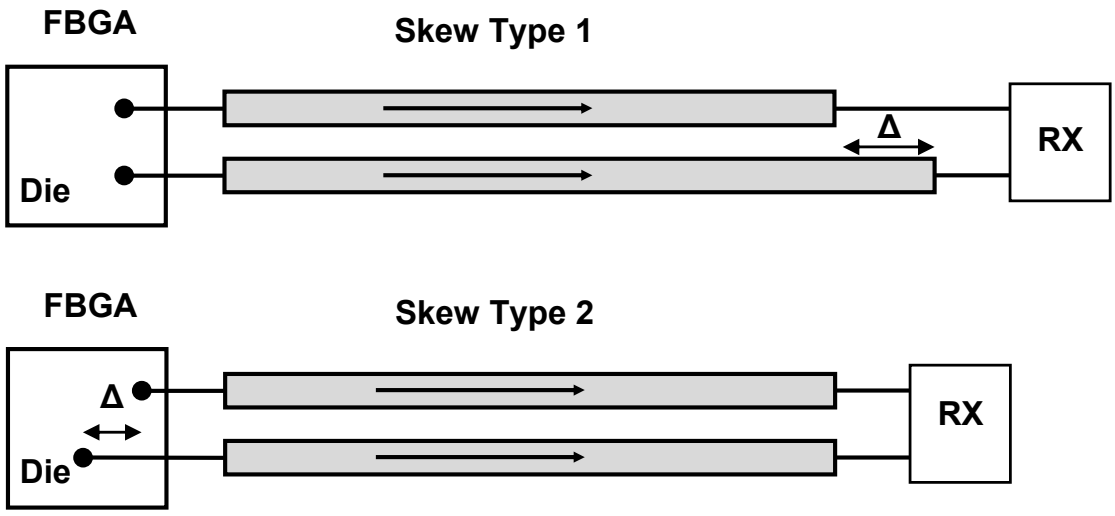

Figure 5.9: Type 1 skew is benign while Type 2 skew requires to be deskewed

aggressor signal occurs at t_Q after the optimal point t_O, then the variable delay can offset the data in the aggressor line by $1T_{bit} - (t_Q - t_O)$. Since a delay-locked loop (DLL) already exists in most communication interfaces for retiming purposes, the variable delays can easily be implemented without considerably changing the existing system.

The majority of FEXT mitigation techniques that have been reported employ crosstalk equalizers (CE). The CE proposed in [21] adaptively adjusts the timing of the threshold-crossing points at the receiver to improve CIJ without actually removing FEXT. [53] implemented a CE that uses a 1-tap FIR to reduce the amplitude perturbation caused by FEXT. Since most of the FEXT coupled energy is introduced at the transitions, the architecture does not provide any significant reduction of CIJ. The CE depicted in [28] applies a 3-tap FIR with a quarter-clock delay to cancel FEXT, which almost completely removes CIJ. However, all the methods mentioned above require a

significant amount of power to mitigate FEXT due to the additional circuitry needed.

The proposed architecture increases the TM in a high-speed, multilane environment by converting CIJ into an amplitude perturbation in order to relax the timing budget and reduce the trace separations for a more compact interconnect design. The presented design has the ability to greatly reduce CIJ without requiring a major design overhaul in existing external interfaces. Furthermore, after modifying the basic I/O architecture in [28] to perform I/O staggering, the new design only consumes an additional 1% of power per lane.

5.4 Experimental Results

5.4.1 Simulations

In order to easily test a variety of data rates and different channel parameters, a three-channel model has been created and analyzed in Matlab/Simulink, where the middle channel is only affected by its 1N-FEXT. A causal mathematical model developed by [35] is used to emulate copper microstrip lines, providing the flexibility needed to simulate various channel lengths and line separations. This model has been fitted to actual S-parameter measurements of a microstrip line on FR4 that has a line width of 5 mil and a line height of 0.65 mil as shown in Fig. 5.1. All simulations have been conducted in a low noise environment to clearly demonstrate the beneficial impact of I/O staggering. The delay values have also been adjusted to achieve minimum CIJ for each set of lines that were tested.

A 12-Gb/s multilane pre-emphasis transmitter with variable delays on alternating lines has been implemented in Simulink to conduct two sets of experiments. The first set of simulations examines the amount of delay that is required to minimize CIJ for two different channel lengths each with a 25-mil separation. The resulting RMS jitter (J_{RMS}) due to the different amounts of delay is illustrated in Fig. 5.10 for both the 8-inch and 18-inch channels. From the graph, the minimum J_{RMS} that is achieved in the 8-inch lines occurs when the delay is fixed at $0.43T_{bit}$. By adding the delay, J_{RMS} reduces by 66.7% which corresponds to a 15.0% increase in the TM and a 19.5% decrease in the VM as depicted in Fig. 5.11. For the 18-inch lines, the optimal delay for minimizing CIJ is set at $0.64T_{bit}$. Here, in Fig. 5.12, we see the J_{RMS} and the TM improve by 11.0% and 9.9%, respectively, while the VM shrinks by 15.5%.

The change in the optimal delay when the channel length increases is due to the increase in channel loss and distortion. As the channel loss worsens, the slope of the data transition decreases, causing the peak of the crosstalk to occur even earlier relative to the peak of the pulse. Thus, in order to reduce CIJ, the data transitions must be delayed slightly longer so that the bulk of FEXT is coupled at the peak of the victim's pulse.

The second set of experiments evaluates the effectiveness of the proposed architecture for different line separations. Simulations with line spacings of 15, 20, and 25 mil have been conducted while keeping the data rate at 12 Gb/s and the line length at 8 inches. Simulation results are summarized in Table 5.1. Note that J_{RMS} almost doubles when

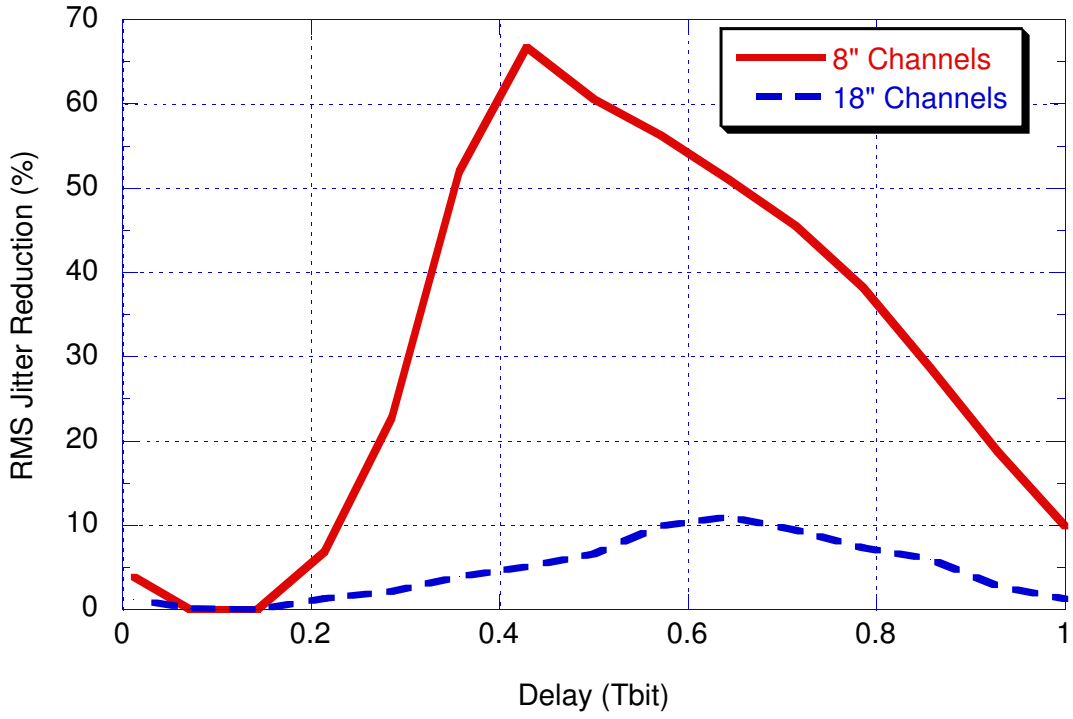

Figure 5.10: RMS jitter vs delay for 8" and 18" channels

the separation is reduced from 25 to 20 mil. In addition, J_{RMS} and the TM improve by 65.4% and 17.6%, respectively, while the VM deteriorates by 41.6% for a line separation of 20 mil. Although there is comparable jitter and TM improvements when the line separation is reduced, the change in the VM is almost doubled. However, in low-loss channels such as the 8-inch lines, the 41.6% drop only degrades the vertical eye opening from 225 to 132 mV. The remaining VM is more than adequate for the receiver to achieve the required BER performance. When the line separation is reduced to 15 mil, the eye completely closes. This implies that the amplitude perturbation caused by the crosstalk is too large to allow the SIO architecture to have any positive impact on reducing CIJ.

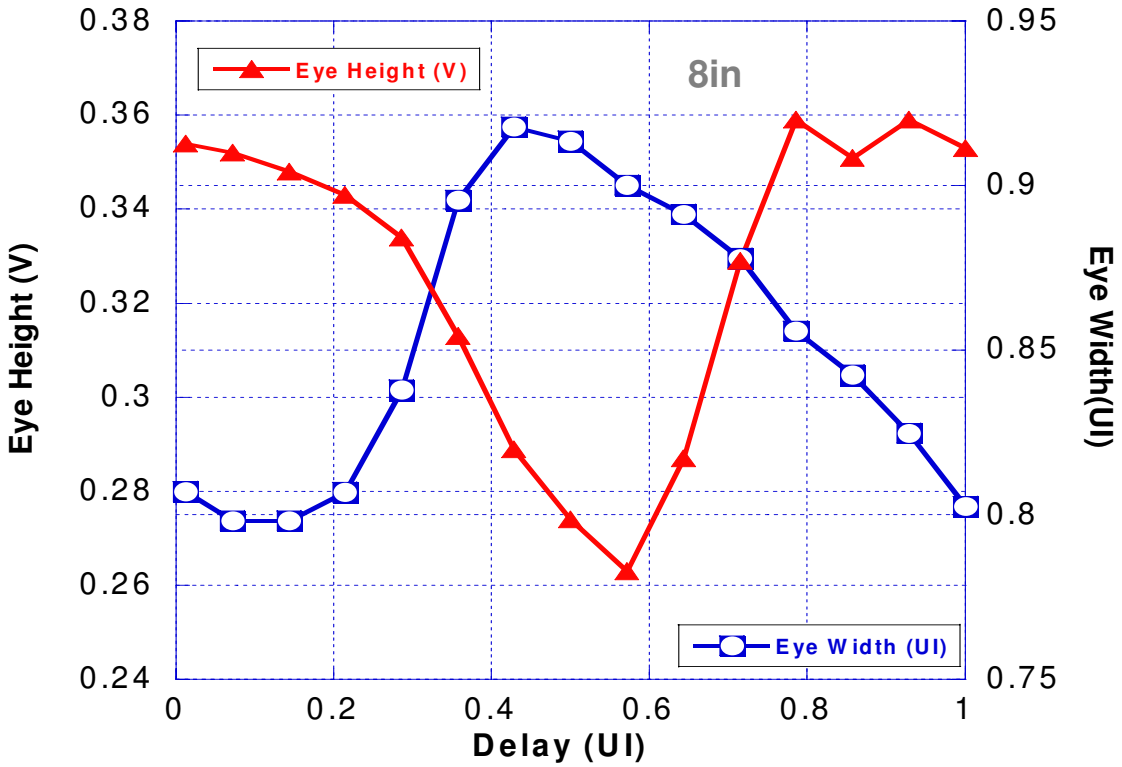

Figure 5.11: Eye height and eye width vs delay for 8" channel

5.4.2 Measurements

In addition to verifying the SIO architecture through multiple simulations, measurement results for selected test cases have also been acquired to further validate its CIJ-reducing capability. Although measurements at higher data rates could not be taken due to test setup limitations, data have been obtained at 600 Mb/s with minimal ISI that clearly illustrates the removal of CIJ at the expense of decreasing the VM. Four 8-inch, 50Ω microstrip lines, each with a line width (W) of 121 mil, have been fabricated on a FR4 board. The line separation between each channel is scaled to the line width in decreasing

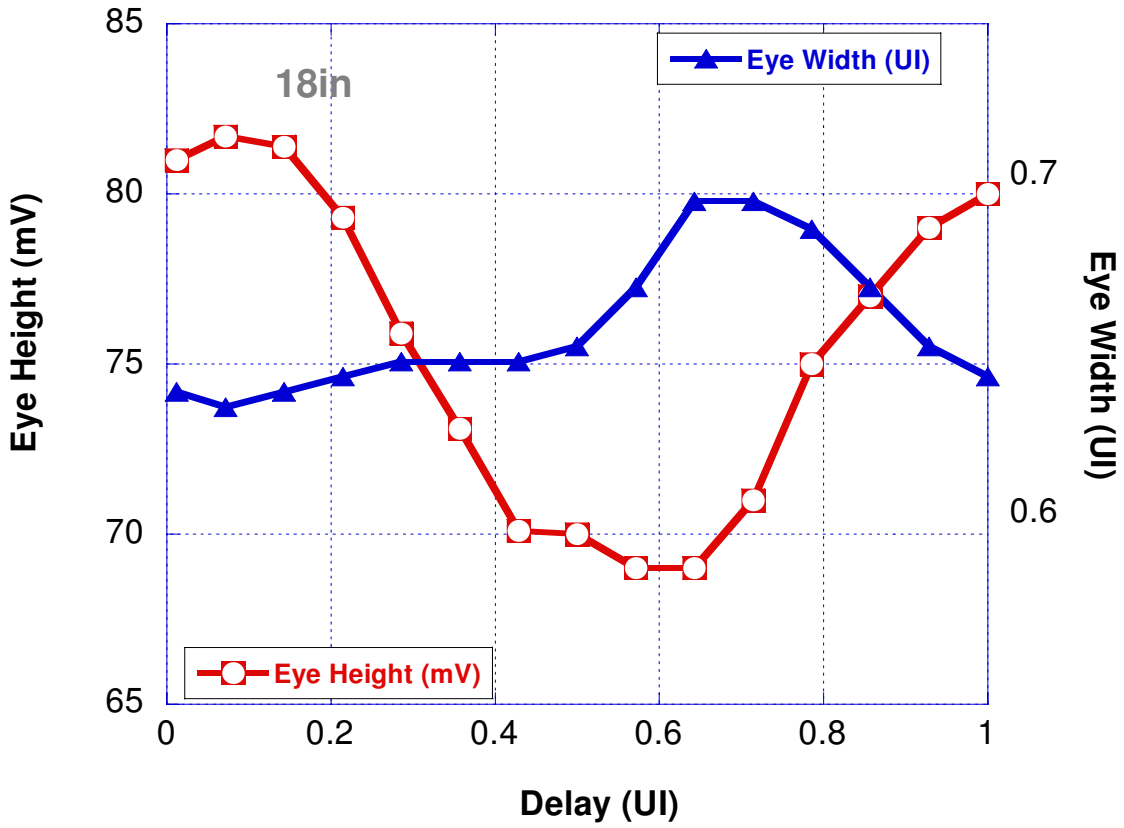

Figure 5.12: Eye height and eye width vs delay for 18" channel

order of $1.5W$, $1.0W$, and $0.5W$ to provide the means of stressing the architecture with varying amounts of FEXT. Two adjacent lines with a given line separation can be observed by properly terminating all the other lines to remove any type of unwanted interference due to reflections and coupling.

In order to demonstrate the impact of I/O staggering, repeated data streams generated by a Tektronix HFS 9003 Stimulus System were transmitted across adjacent microstrip lines with different line separations. The 500-mVpp data streams have been deliberately designed such that the received signal of the victim channel will experience

Table 5.1: Simulated voltage margin, timing margin & jitter at 12 Gb/s

Delay (T_{bit})	**Separation (mil) Length (inch)**	J_{RMS} **(ps)**	ΔJ_{RMS} (%)	**ΔVM** (%)	**ΔTM** (%)
0	25 / 8	3.91	-66.7	-19.5	15.0
0.43		1.30			
0	25 / **18**	6.52	-11.0	-15.5	9.9
0.64		5.80			
0	**20** / 8	6.67	-65.4	-41.6	17.6
0.43		2.31			

all three modes of excitation on both the rising and falling edges. The delay between the two data patterns was changed between 0 and $0.5T_{bit}$ to emulate both source-synchronous I/Os and SIOs. The data eyes of the received signal were then captured using Agilent's Infinium DCA-J 86100C.

Measurement results are summarized in Table 5.2. Similar to the simulation results discussed earlier, in every case when I/O staggering is introduced, the TM and J_{RMS} improve as the VM decreases. More importantly, CIJ is virtually eliminated such that the resulting J_{RMS} is approximately equal to 7.5 ps, which is the J_{RMS} when no FEXT is coupled. This implies that the approximation made to simplify (5.5) is fairly accurate. A data eye comparison is shown in Fig. 5.13 to illustrate the benefit of the SIO architecture. Note, we are assuming the worst case vertical opening at the center of the eye.

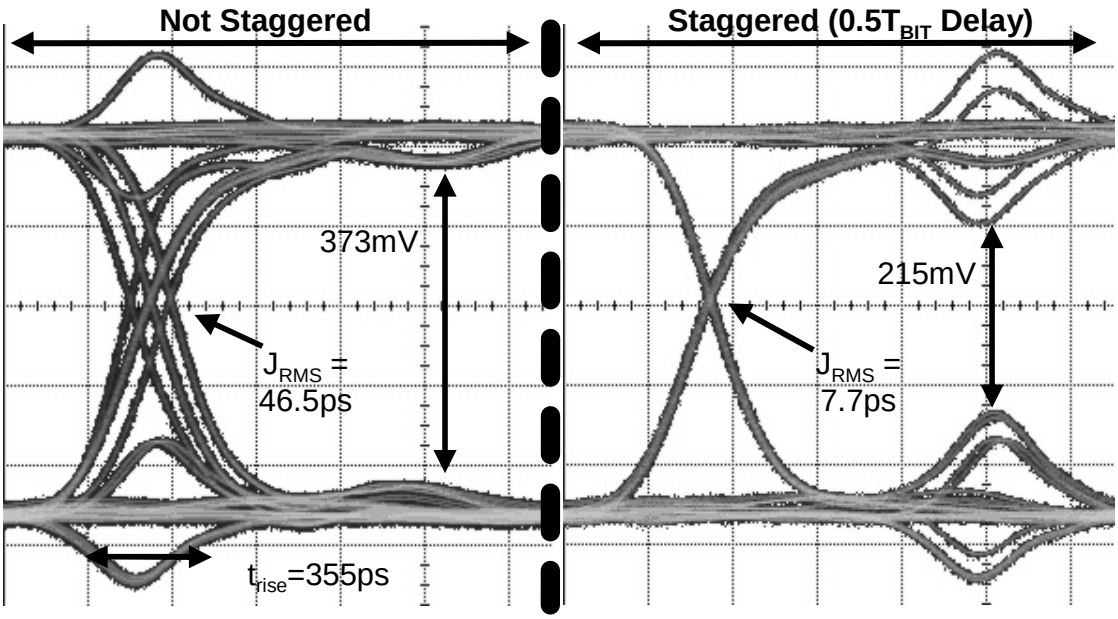

Figure 5.13: Data eyes illustrating the benefit of I/O staggering for 8-inch microstrips with 0.5W separation

Additional measurements of FEXT and t_{rise} have been taken for the different line separations to validate (5.6) and (5.7). τ_f have also been extracted from the corresponding J_{RMS} [21]. A comparison between measured and calculated FEXT and VM is presented in Table 5.3, showing a maximum deviation of 10.3% in FEXT and -9.2% in VM. These results confirm that our theoretical analysis of SIOs can accurately predict their actual behavior in real implementations.

Table 5.2: Measured voltage margin, timing margin & jitter at 600 Mb/s

Delay (T_{bit})	**Separation (width) Length (inch)**	J_{RMS} **(ps)**	ΔJ_{RMS} **(%)**	**ΔVM (%)**	**ΔTM (%)**
0	N/A / 8	7.5	N/A	N/A	N/A
0	**1.5W** / 8	25.5	-70.6	-17.1	7.1
0.50		7.5			
0	**1.0W** / 8	35.6	-78.7	-24.1	12.0
0.50		7.6			
0	**0.5W** / 8	46.5	-83.4	-42.4	14.2
0.50		7.7			

Table 5.3: Measured and calculated FEXT and SIO's VM at 600 Mb/s

Data Type	**Separation (width) Length (inch)**	τ_f **(ps)**	**FEXT (mV)**	**(%)**	**VM (mV)**	**(%)**
Calc'd	**1.5W** / 8	36.1	38.6	10.2	303	3.9
Meas'd			43		315	
Calc'd	**1.0W** / 8	50.3	53.5	1.0	270	5.6
Meas'd			54		286	
Calc'd	**0.5W** / 8	65.8	69.1	10.3	235	-9.2
Meas'd			77		215	

5.5 Chapter Conclusions

This chapter has presented an ultra-low power multilane transmitter architecture to reduce CIJ in a high-speed I/O design. In this implementation, variable delays are placed in alternating lines at the transmit end to shift the data transitions such that the induced FEXT occurs at the center of the vertical eye opening. The low-power technique decreases CIJ and improves TM at the expense of losing VM. Therefore, a low-loss environment is necessary to maximize the positive impact of the proposed architecture. Simulation results show that SIOs can successfully reduce jitter by 66.7% and widen the eye by 15.0%. Furthermore, results indicate that the new technique can still improve jitter and increase TM even for reduced line separations and longer line lengths. Measurements have reinforced the simulation results and verified the presented theoretical analysis. The measured data at 600 Mb/s demonstrated a complete removal of CIJ while reducing the VM by 42.4%. By employing the SIO method, the I/O specifications can be relaxed providing additional timing budget and reduced trace separation in current external off-chip communication interfaces.

Chapter 6

FEXT Cancellation: Removing Crosstalk in High-Speed I/Os

Technology scaling has increased the on-die bandwidth exponentially, making off-chip data transmission the bottleneck in high-speed systems [3]. To improve the overall system performance, the data rate of chip-to-chip communication must increase commensurately with on-chip clock speeds despite being limited by inter-symbol interference (ISI) and crosstalk [16]. Far-end crosstalk (FEXT), as discussed in previous chapters, is rapidly becoming a major noise source at high speeds. This problem is exacerbated at high frequencies because signal magnitude decreases with frequency, while FEXT magnitude increases with frequency reducing the effective signal-to-noise and interference ratio (SNIR) as shown in Fig. 6.1. Additionally, FEXT introduces deterministic jitter (DJ) in the received signal by altering the amplitude of the signal at the threshold-crossing

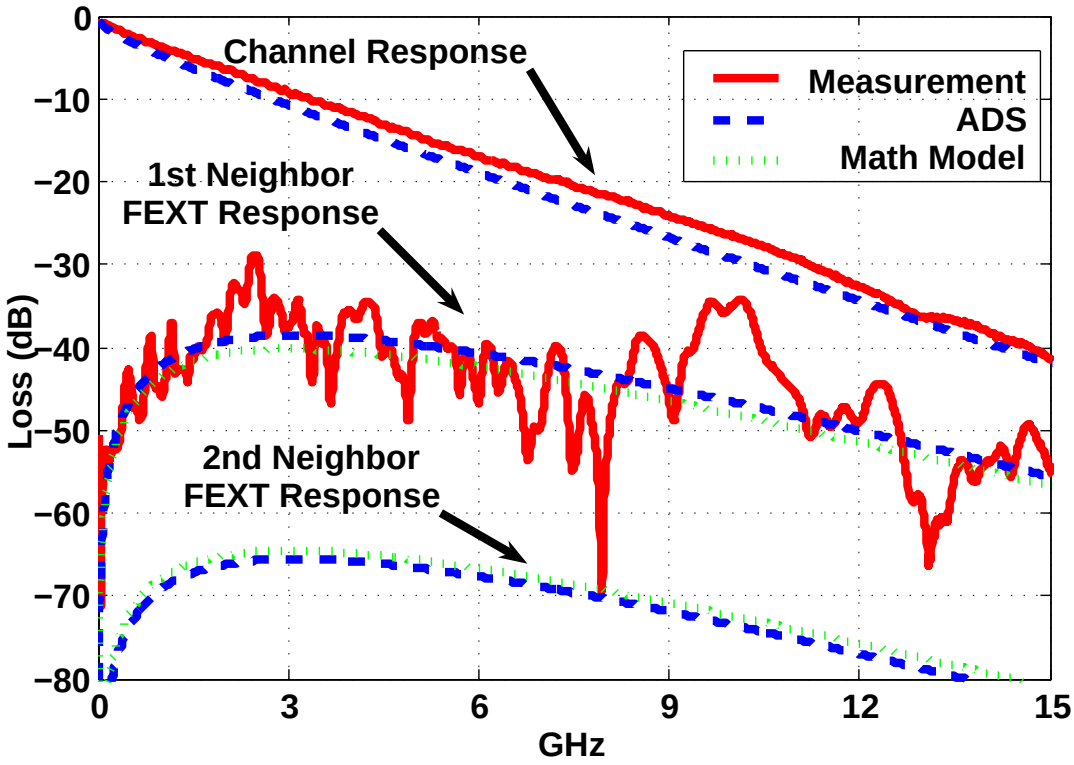

Figure 6.1: Measured, modeled, and simulated frequency responses: channel, 1N-FEXT and 2N-FEXT

points, thereby further degrading the receiver's bit-error rate (BER) performance [4].

Although conventional transmit (TX) pre-emphasis can be used to mitigate ISI, it also causes an undesired boost in high-frequency FEXT, which decreases the effectiveness of the TX equalization for high data rates [53]. The work presented in this chapter employs TX pre-emphasis and FEXT cancellation (XTC) to improve the SNIR of the received data and reduce DJ by compensating for frequency dependent channel loss and removing crosstalk.

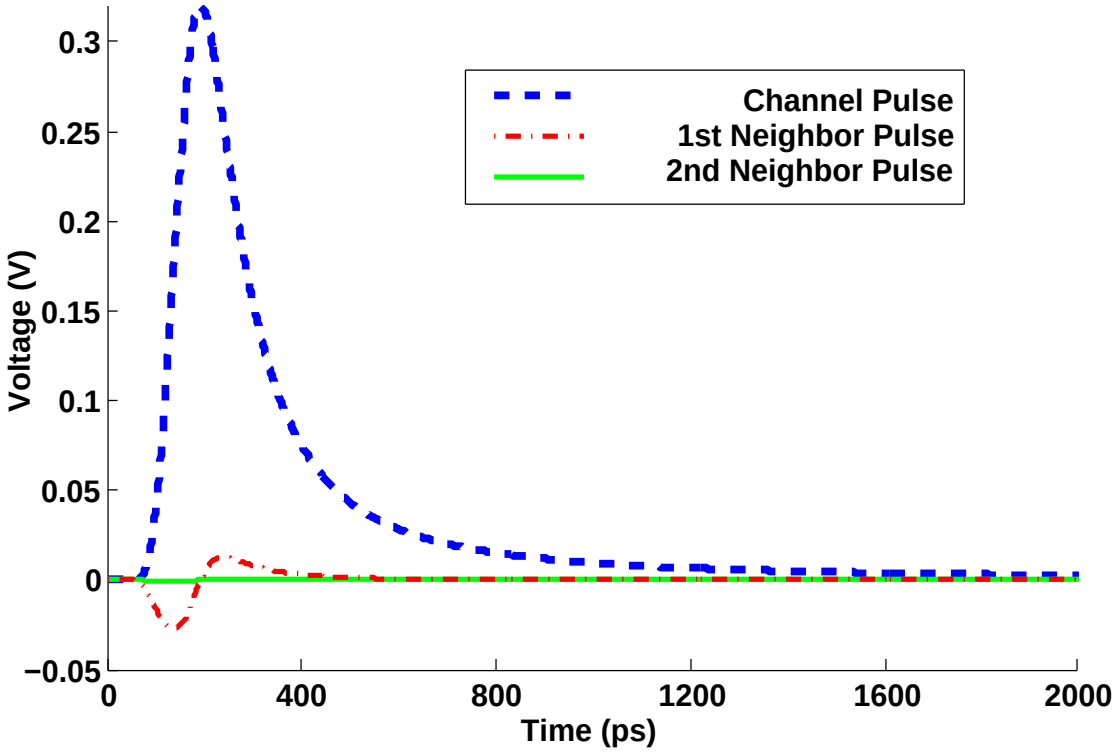

Figure 6.2: Channel, 1N-FEXT and 2N-FEXT pulse responses for coupled 20-in microstrips at 12.8 Gb/s

6.1 Analysis of FEXT Cancellation

It has been known that one of the major factors that prevents higher data rates on legacy backplanes besides ISI is FEXT [14]. In particular, data rates of multiple point-to-point I/O interfaces, such as HyperTransport [57] and PCI-Express [58], are limited by this problem due to the number of high-speed lines that runs parallel to each other. FEXT is induced in the victim line during a transition in the aggressor line as shown in Figure 6.2. Assuming that all the lines are aligned with the same clock, then FEXT will alter the

threshold-crossing point and introduce jitter if a transition occurs simultaneously in both the victim and aggressor lines. There is also a slight reduction in the vertical eye opening similar to the impact of ISI.

As discussed in Section 5.1, the energy coupled from neighboring differential lines diminishes approximately by a factor of D^{-2}, where D is the spacing between the differential lines. For the microstrips with the measured S parameters shown in Fig. 6.1, the spacing (D) is 30 mils. To obtain a BER of 10^{-12}, SNIR should be greater than 14.1 dB. From Fig. 6.1, since the second neighbors' FEXT (2N-FEXT) is approximately 20 dB below the first neighbors' (1N-FEXT), the SNIR due to 2N-FEXT alone will always be greater than 14.1 dB. As a result, 1N-FEXT cancellation is sufficient for improving the SNIR and jitter of the transmitted signal. In Section 6.3, the results will demonstrate that even for reduced spacing, the improvement in SNIR is significant when canceling just 1N-FEXT. This observation is exploited to simplify the system architecture.

Although there have been other reported crosstalk equalizers (CE) as listed in Section 5.3, the architecture proposed in this chapter fully eliminates FEXT using a FIR filter with a quarter-clock delay. This approach allows for almost complete removal of CIJ and is not limited by the technology. The main difficulty in implementing XTC is that cancellation must occur in the victim line at the moment when the aggressor line introduces FEXT. Thus, timing information is critical for removing FEXT. Timing skews between different channels due to unequal interconnect lengths can severely limit the effectiveness of any XTC scheme. This also implies that XTC is harder to implement

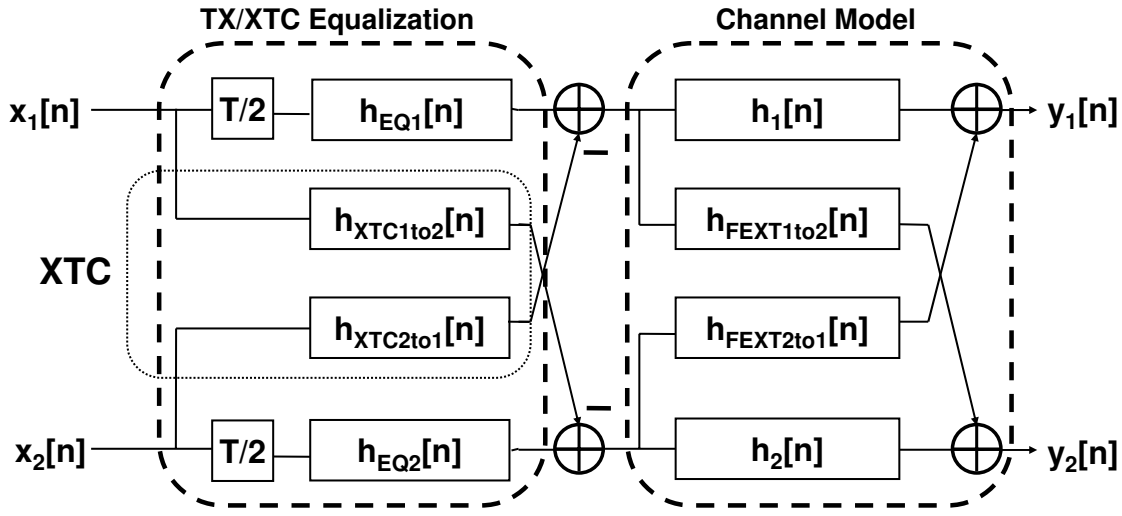

Figure 6.3: Block diagram of transmit/XTC equalization (1N-FEXT only) and channel model

on the receive end since the extraction of timing information from the received signal and elimination of timing skews are tightly coupled together.

The proposed technique performs XTC on the transmit side since it has the best possible timing information for all the channels. In addition, the XTC filter can easily be implemented as an extension of the pre-emphasis filter. For simplicity, the XTC filter is estimated as an FIR filter and implemented to subtract current from the transmit path [24]. Similar to TX pre-emphasis, the XTC tap weights have to be adapted for each board design. In addition, a variable $T/2$ delay is used to adjust for unwanted timing skews.

As derived in Section 3.1, the FEXT impulse response from aggressor channel i to the victim channel j, is approximately proportional to the derivative of the aggressor

channel i's impulse response (3.8) [21].

If the channel and its FEXT are modeled as discrete-time sampled responses, then, using Fig. 6.3, FEXT can be completely removed using the XTC filter

$$h_{XTC_{itoj}}[n] = [d_{-M} d_{-M+1} \cdots d_M], \tag{6.1}$$

if the condition

$$x_i[n] * h_{EQ_i}[n] * h_{FEXT_{itoj}}[n] = x_i[n] * h_{XTC_{itoj}}[n] * h_j[n] \tag{6.2}$$

is satisfied. Note that $x_i[n]$ is the nonreturn-to-zero (NRZ) data stream sent through channel i and its corresponding transmit pre-emphasis FIR filter has the tap coefficients of

$$h_{EQ_i}[n] = [w_{-M} w_{-M+1} \cdots w_M] \tag{6.3}$$

By expanding (6.2) based on the formal definition of convolution, the equation can be represented as

$$\sum_{k=-M}^{M} h_j[(m-k)T] \cdot d_k = \sum_{k=-M}^{M} h_{FEXT_{itoj}}[(m-k)T] \cdot w_k \tag{6.4}$$

Equation (6.4) can be rearranged into the following matrix equation

$$\begin{bmatrix} d_{-M} \\ \vdots \\ d_M \end{bmatrix} = \begin{bmatrix} h_j[(m+M)T] \\ \vdots \\ h_j[(m-M)T] \end{bmatrix}^{-1} \begin{bmatrix} h_{FEXT_{itoj}}[(m+M)T] \\ \vdots \\ h_{FEXT_{itoj}}[(m-M)T] \end{bmatrix} \begin{bmatrix} w_{-M} \\ \vdots \\ w_M \end{bmatrix}. \tag{6.5}$$

Given the channel impulse response and the transmit pre-emphasis tap coefficients (6.3), the XTC tap weights (6.1), can be calculated by solving the matrix equation (6.5).

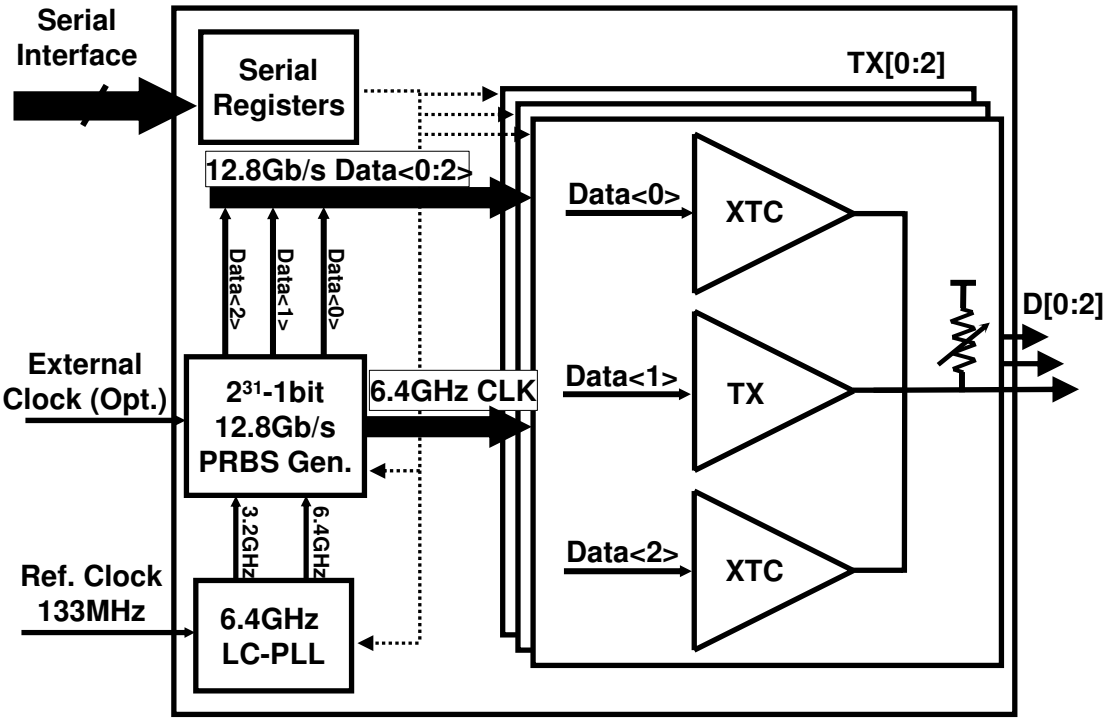

Figure 6.4: System architecture of the multi-channel transmitter with XTC

6.2 Proposed System Architecture for XTC

The complete 3-lane transmitter system architecture is shown in Fig. 6.4. A low-spur charge-pump LC-PLL produces 6.4-GHz and 3.2-GHz clocks from a 133-MHz off-chip reference. The two clocks are sent directly to a low-power, $2^{31} - 1$ bit, pseudo-random binary sequence (PRBS) generator described in Chapter 4, which produces three 12.8-Gb/s non-correlated data streams for testing the multilane transmitter.

A CML buffer network is applied to distribute the 6.4-GHz clock and the data streams to the three transmitters. Although an inverter network could have been implemented for lower power consumption, [59] has shown that a CML clock distribution network

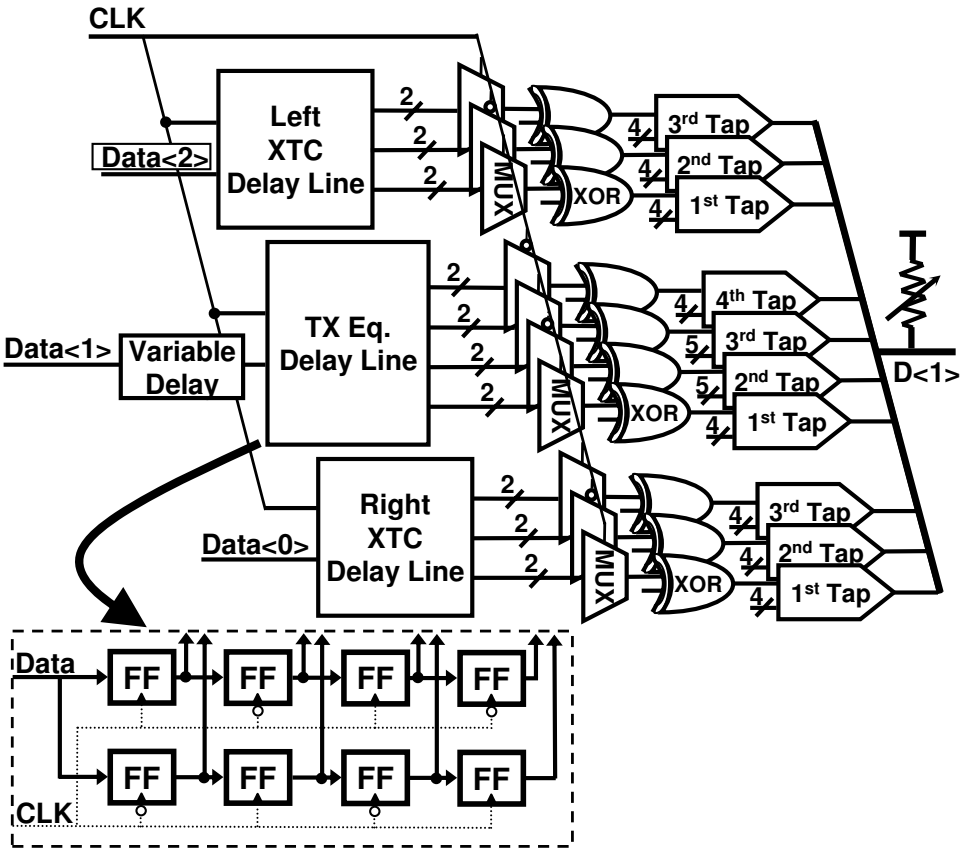

Figure 6.5: Design architecture of the center transmitter with pre-emphasis and XTC equalization

reduces jitter by 50% as it is less susceptible to power supply noise. In order to reach the achievable data rate given a 6.4-GHz clock, a half-rate 12.8-Gb/s TX design is used for all three transmitters in the proposed system despite the additional area required. The XTC and pre-emphasis filters are constructed in the same manner such that the XTC filters can be easily inserted by extending the existing pre-emphasis filters in the TX. In the proposed design, the pre-emphasis filters have four taps while the XTC filters have

three taps since additional taps had limited impact on eliminating ISI and FEXT. Data streams from the adjacent lanes are delayed by a quarter-clock cycle and then fed into the XTC filters for optimal cancellation.

As shown in Fig. 6.5, the shift registers operate on a 6.4-GHz clock to create a full clock period delay between each single-edge triggered flip-flop (FF). Triggering on opposite clock polarities, the two delay lines have a phase difference of exactly 90 degrees. The outputs of each set of FFs in the delay lines are then multiplexed using a 6.4-GHz clock to generate copies of the 12.8-Gb/s data delayed by half a clock period between each tap. The output drivers for each tap have programmable tail currents to establish the correct tap coefficients of the FIR filter. The cursor and the first postcursor taps of the pre-emphasis filter have a 5-bit dynamic range while the precursor and the second postcursor taps have a 4-bit dynamic range. The CML logic used in the transmitters all employ modified active inductors to achieve full voltage swing at 12.8 Gb/s [50].

6.3 Simulation Results

To verify the XTC technique proposed in the previous section, a five-channel model has been designed in Matlab/Simulink. In this model, the primary channel is affected by the FEXT from two 1N-FEXT and two 2N-FEXT. In order to accurately simulate the multilane transmitter system, a causal mathematical model developed in [35] has been fitted to actual measurements as shown in Fig. 6.1. Although the ADS model matches the measured frequency response of the channel and its induced FEXT, the time-domain

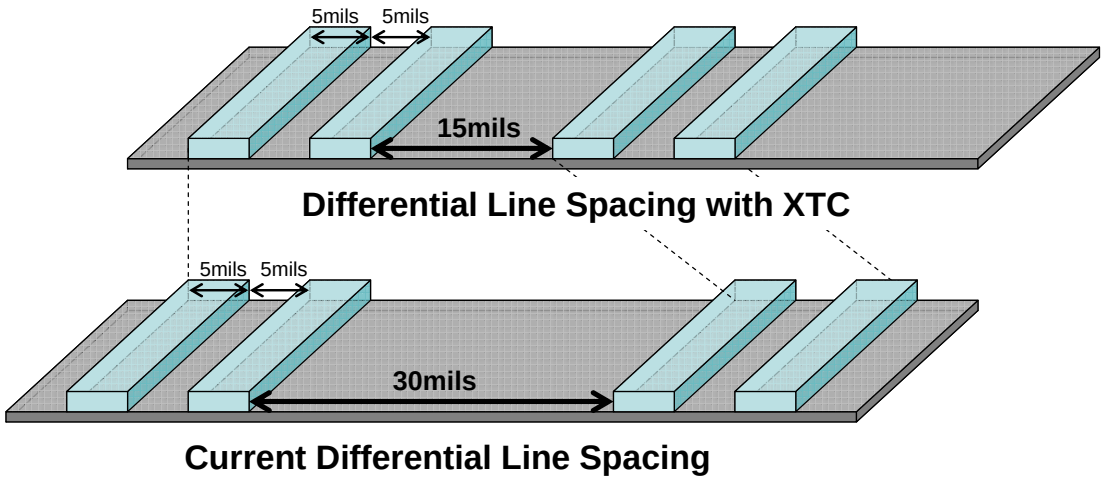

Figure 6.6: Diagram of multiple differential microstrip lines before and after XTC

simulations in ADS are unfortunately non-causal. Instead, the mathematical model is adjusted to match the ADS frequency response and then the time-domain response is determined by taking the inverse FFT of the model.

The proposed system shown in Fig. 6.4 has been simulated with a 4-tap pre-emphasis and 3-tap XTC filters for 1N-FEXT cancellation as implemented in Fig. 6.5. XTC has been implemented only for the two first neighbors even though both the first and second neighbors are contributing FEXT in the simulations. All simulations are conducted in a low noise environment in order to clearly illustrate the positive impact of FEXT cancellation. Furthermore, this permits peak-to-peak jitter (J_{pp}) comparisons even though traditionally J_{pp} with added random noise is unbounded. J_{pp} is used for comparison purposes in preference to RMS values because the resulting jitter probability density functions (PDF) are not uniform across simulations.

To validate the presented architecture and the performance of XTC, four sets of

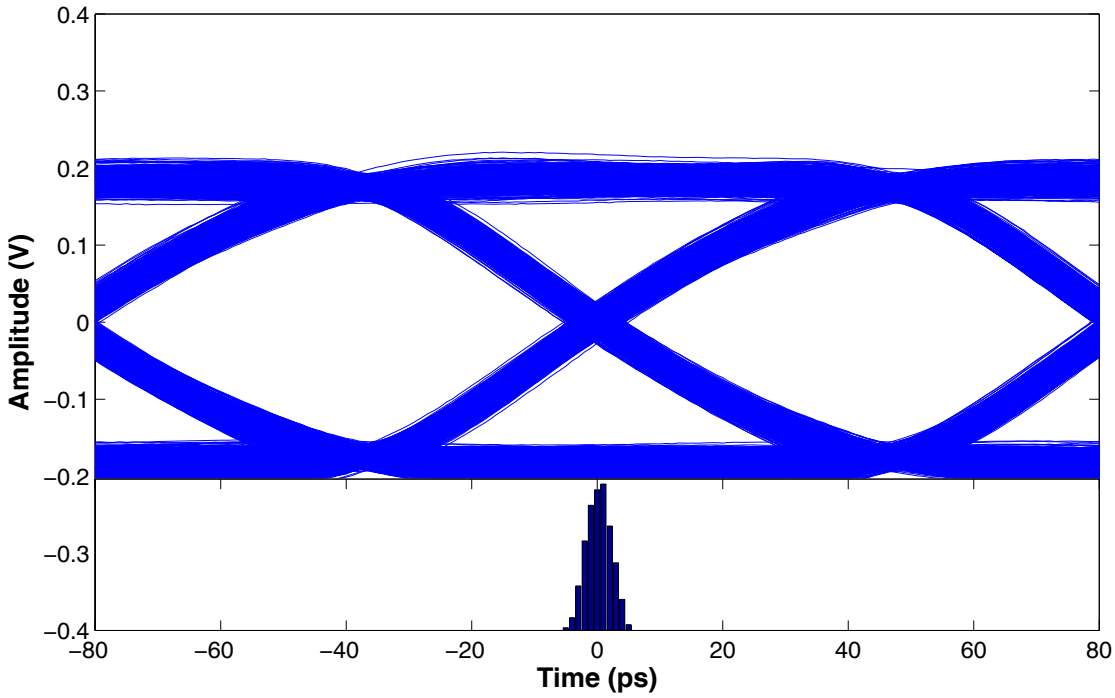

Figure 6.7: Eye diagram & jitter histogram with XTC at (12.8Gb/s & 30-mil)

experiments have been conducted.

1^{st} **experiment:** A 12.8-Gb/s transmitter with XTC is used to drive a differential 12-inch FR4 microstrip line with 30-mil separation. The microstrip line dimensions and spacing are shown in Fig. 6.6. The results are shown in the second row of Table 6.1. Here, XTC reduces the jitter from 18 ps to 10 ps, which translates to a 10.2% UI reduction, and provides a small vertical eye opening improvement. The eye pattern and jitter histogram for this experiment with XTC is shown in Fig. 6.7. Note that FEXT is not a major noise source when the lines are placed sufficiently far apart. This is considered the base-line experiment.

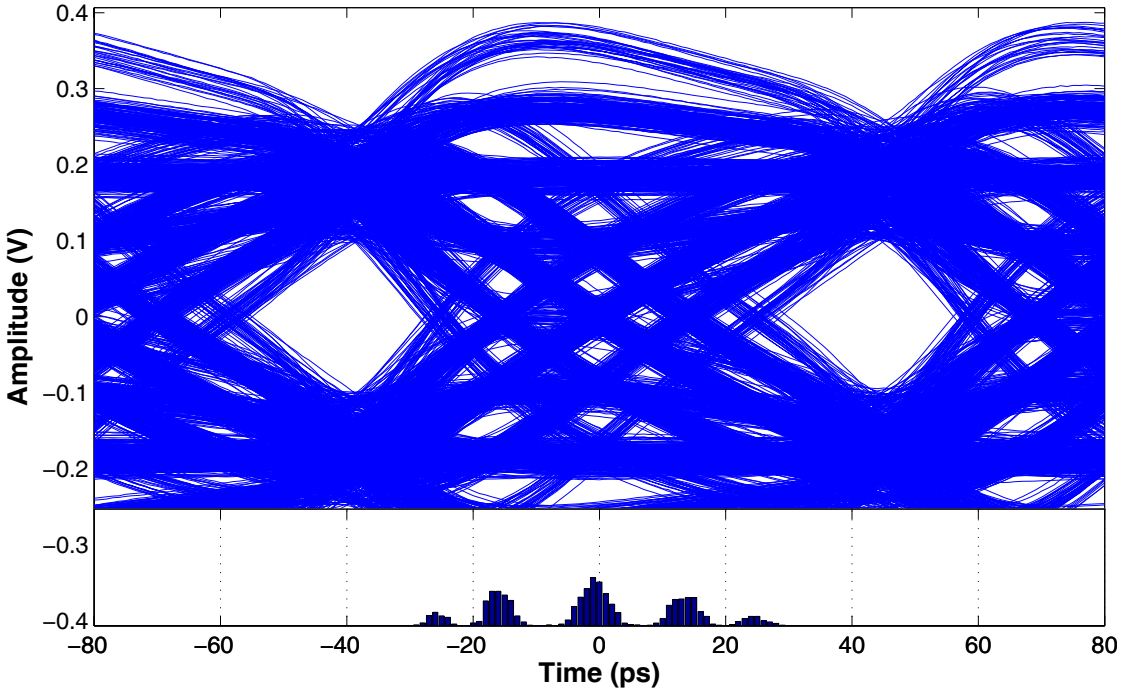

Figure 6.8: Eye diagram & jitter histogram without XTC @ (12.8Gb/s & 15-mil)

2^{nd} **experiment:** For this experiment, the line separation has been reduced to 15-mils while keeping all the other parameters the same. Figs. 6.8 and 6.9 shows the eye patterns and the jitter histograms of the 12.8-Gb/s transmitter without XTC, and with XTC. The numerical results for this experiment are shown in the third row of Table 6.1. The eye without XTC is nearly closed due to the dramatic increase in CIJ, while the eye with XTC is open due to the removal of FEXT. Furthermore, XTC reduces the jitter by 51.2% UI and increases the vertical eye opening by 14.5%. Note that the jitter PDF without XTC shows a five-modal distribution with a J_{pp} of 58 ps. This is due to the introduction of additional DJ from the two adjacent neighbors to the Gaussian RJ [4].

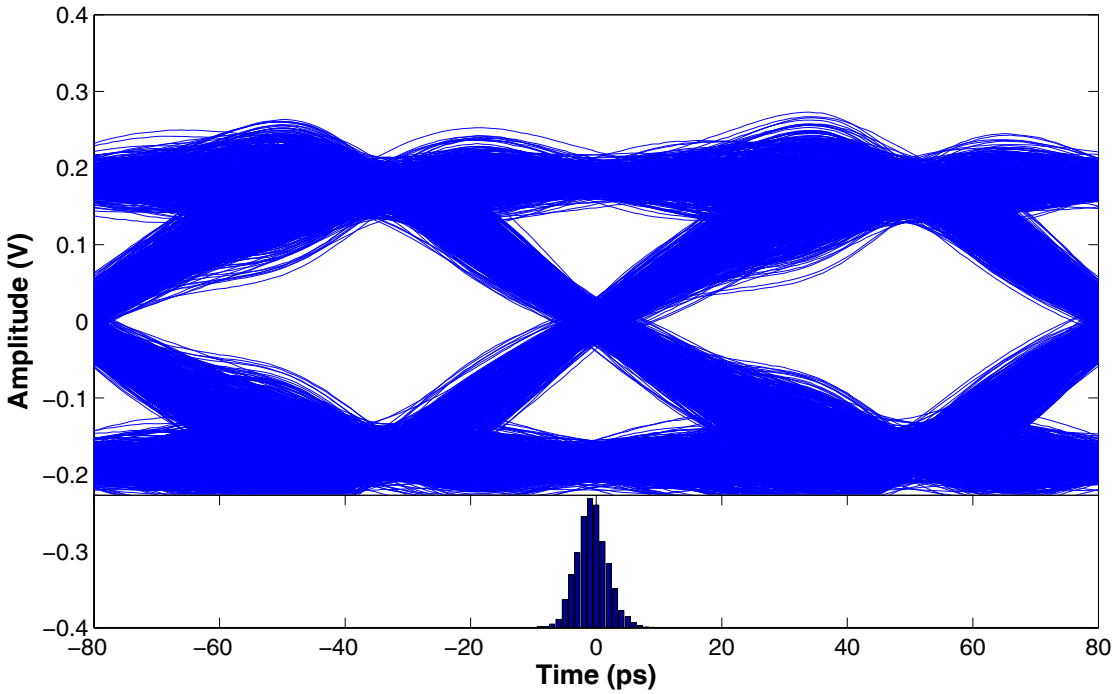

Figure 6.9: Eye diagram & jitter histogram with XTC @ (12.8Gb/s & 15-mil)

3^{rd} **experiment:** In this experiment, a longer 20-inch line has been used to determine the effect of line length in XTC. The results are shown in the fourth row of Table 6.1. Here the improvement due to XTC in the jitter and eye opening is less dramatic. The reason for this limitation is that the overall received amplitude is reduced and a 4-tap pre-emphasis filter still has residual ISI which becomes the major source of jitter.

4^{th} **experiment:** The last test operated the original base-line at a higher data rate of 25.6 Gb/s. The results are shown in the fifth row of Table 6.1. It can be observed that the jitter is reduced by 17.9% UI and the vertical eye opening is improved by 10% due to XTC. At higher speeds, FEXT has more impact but the fixed pre-emphasis tap length

Table 6.1: Simulations results for vertical eye & jitter with and without XTC

Speed (Gb/s) Separation (mils) Length (inch)	**Jitter p-p (pS)**	**Δ UI (%)**	**Vertical Eye (mV)**	**Improv. (%)**
no XTC	18		285.4	
12.8 / 30 / 12		10.2		1.4
XTC	10		289.5	
no XTC	58		172.1	
12.8 / **15** / 12		51.2		14.5
XTC	18		197.1	
no XTC	28		97.7	
12.8 / 30 / **20**		7.7		4.3
XTC	22		101.9	
no XTC	19		72.3	
25.6 / 30 / 12		17.9		10.0
XTC	12		79.5	

does not allow for XTC to have as great an impact as the UI shrinks.

The proposed XTC technique helps with reduced line separation and for higher speed operation. It provides limited improvement for longer line lengths. The architecture is an extension of the TX pre-emphasis FIR filter allowing for simple implementation since an RX implementation based on DFE architectures would require a extremely fast feedback loop. Traditionally, channel equalization is split between the TX and RX sections because TX equalization, though simpler to implement, increases FEXT. However, by employing XTC, the entire equalization can be accomplished on the TX side.

6.4 Prototype Implementation & Measurements

The proposed system has been implemented in the TSMC 0.18-μm CMOS technology. As shown in Fig. 6.4, the system consists of three transmitters, a charge-pump PLL that generates a 6.4-GHz clock, and a PRBS generator that produces three sets of uncorrelated 12.8-Gb/s data. A low-speed serial interface has also been designed to program the control bits used to adjust the tap weights of the equalizers, set the resistive termination for impedance matching, and coarse tune the PLL.

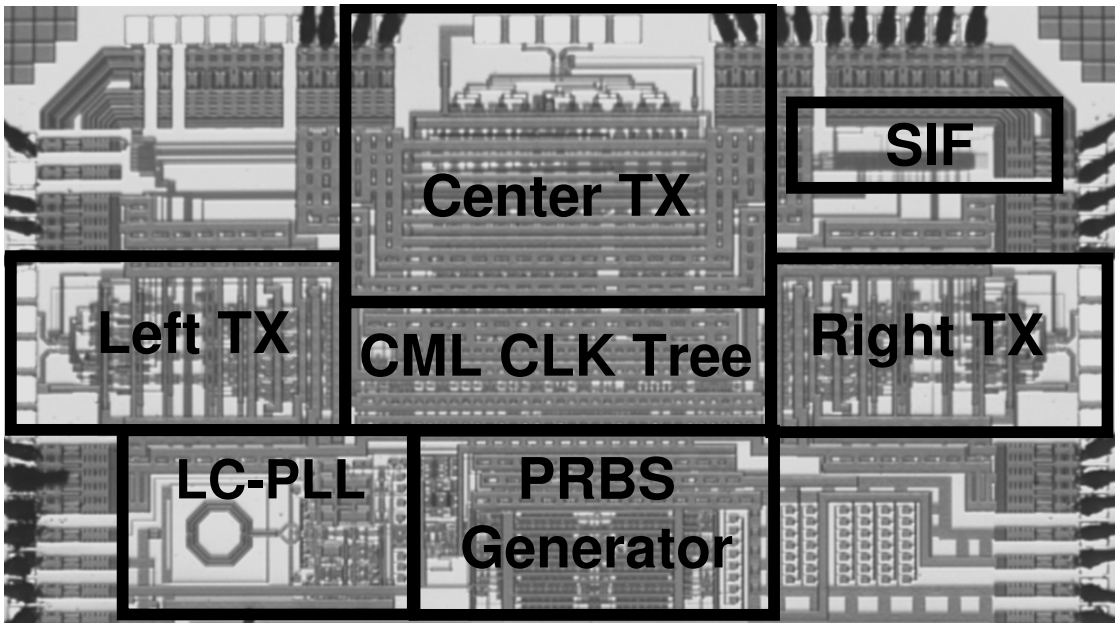

Figure 6.10: Microphotograph of 12.8-Gb/s multilane transmitter with XTC

The chip shown in Fig. 6.10 consumes 1.8 W and occupies 1.5x2.5mm^2 of silicon area. As depicted in Fig. 6.11, the chip is mounted on a custom PCB which powers the system and supplies it with a 133-MHz reference clock. The outputs of the transmitters are

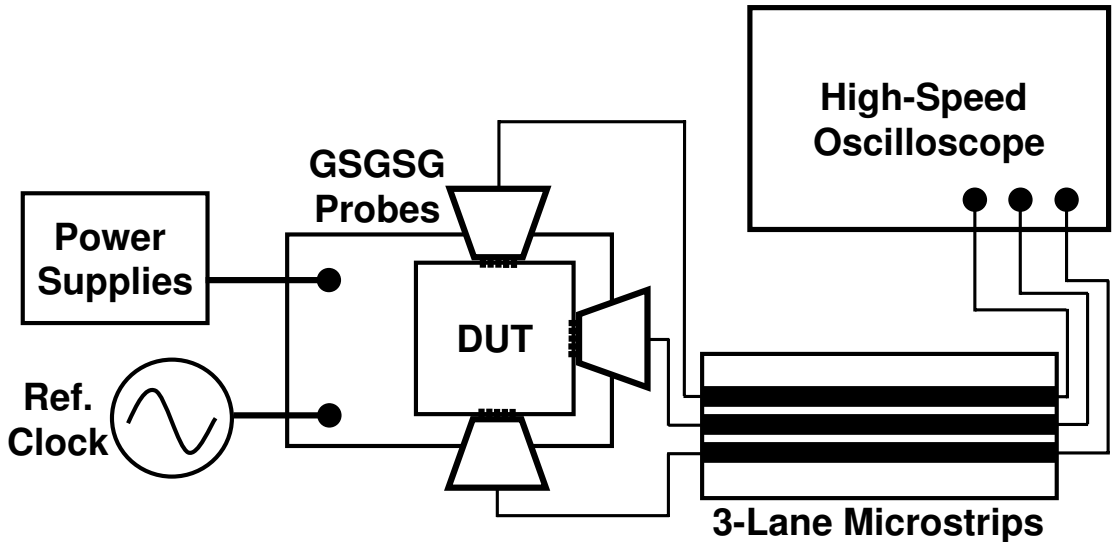

Figure 6.11: 3-lane transmitter test setup

probed using Cascade GSGSG probes and then sent through the microstrip lines. The received data is analyzed using Agilent's DCA-J 86100C high-speed oscilloscope. The outputs for the two first neighbors are placed at right angles to center transmitter for ease of testing. The power consumption of only one transmitter with XTC is measured and calculated to be 25 mW/Gb/s. Although the chip ran at a maximum clock speed of 5 GHz and had the ability to transmit data at 10 Gb/s, there were issues with the serial interface, inhibiting further testing of the XTC.

6.5 Chapter Conclusions

An efficient architecture for a high-speed I/O design has been proposed that implements far-end crosstalk (FEXT) cancellation. This design combines TX pre-emphasis to re-

duce ISI and FEXT cancellation to remove crosstalk-induced jitter and interference. A 12.8-Gb/s 3-lane transmitter has been realized in a 0.18-μm CMOS process where the presented multilane transmitter has been implemented to operate at a maximum frequency close to $f_T/4$ of the process. Simulation results show that, even with a 2X reduction in line separation, FEXT cancellation can successfully reduce jitter by 51.2% UI and widen the eye by 14.5%. The architecture presented in this chapter is a simple extension of the TX pre-emphasis, thereby significantly simplifying its implementation. As data rates approach higher speeds, using the proposed technique to cancel FEXT can enhance jitter performance and improve the eye opening even with reduced line separation.

Chapter 7

Conclusions & Future Directions

As stated in the "International Technology Roadmap for Semiconductors (ITRS) 2005: System Drivers", the bandwidth of chip-to-chip I/Os is often the performance bottleneck in desktop and server applications. Due to the finite board area and the high throughput requirements, which are critical to multi-core architectures, such interconnects have typically been single-ended. However, as data rates continue to soar, the increase in far-end crosstalk (FEXT) and simultaneous switching output (SSO) perturbations in single-ended parallel link designs have forced some high-speed I/Os to become differential in spite of the area, power, and I/O pin overhead. Furthermore, jitter caused by the crosstalk reduces the overall jitter budget and the sampling range of the data, thereby degrading the bit error rate (BER). Developing techniques to combat FEXT and CIJ in high-speed I/Os will ultimately result in smaller packages, lower power, and higher data throughput. In this thesis, different mitigation techniques that shift or cancel FEXT

have been explored. Integrated circuits have also been designed and fabricated to test the feasibility of these new approaches.

This chapter will offer a glimpse of the ongoing research that has stemmed from the work presented in this thesis. Section 7.1 gives an overview of a wireline multi-input multi-output (MIMO) technique that can be used to implement FEXT friendly parallel I/Os. Instead of suppressing or eliminating crosstalk, MIMO techniques can potentially exploit and use the crosstalk energy introduced into the adjacent channels to improve the BER performance of the channel of interest. Crosstalk energy increases with frequency so a substantial increase in SNR should be observed as data rate increases. Section 7.2 provides a summary of a novel 5Gb/s-per-lane programmable transmitter that can be used to test various MIMO techniques. Simulation results are presented to demonstrate its operation. In Section 7.3, the research described in this thesis is summarized and its significance and contributions are highlighted. Finally, the last section will indicate the future direction of high-speed I/O design and the potential limitations that will require additional research.

7.1 MIMO Techniques in High-Speed Serial Link

MIMO techniques have been used in wireless communications to enhance system capacity and link reliability for many years. The most basic form of wireless MIMO is obtained by defining a transformation on the channel input and output via transmit precoding and receiver shaping such that parallel channels do not interfere with each other [60].

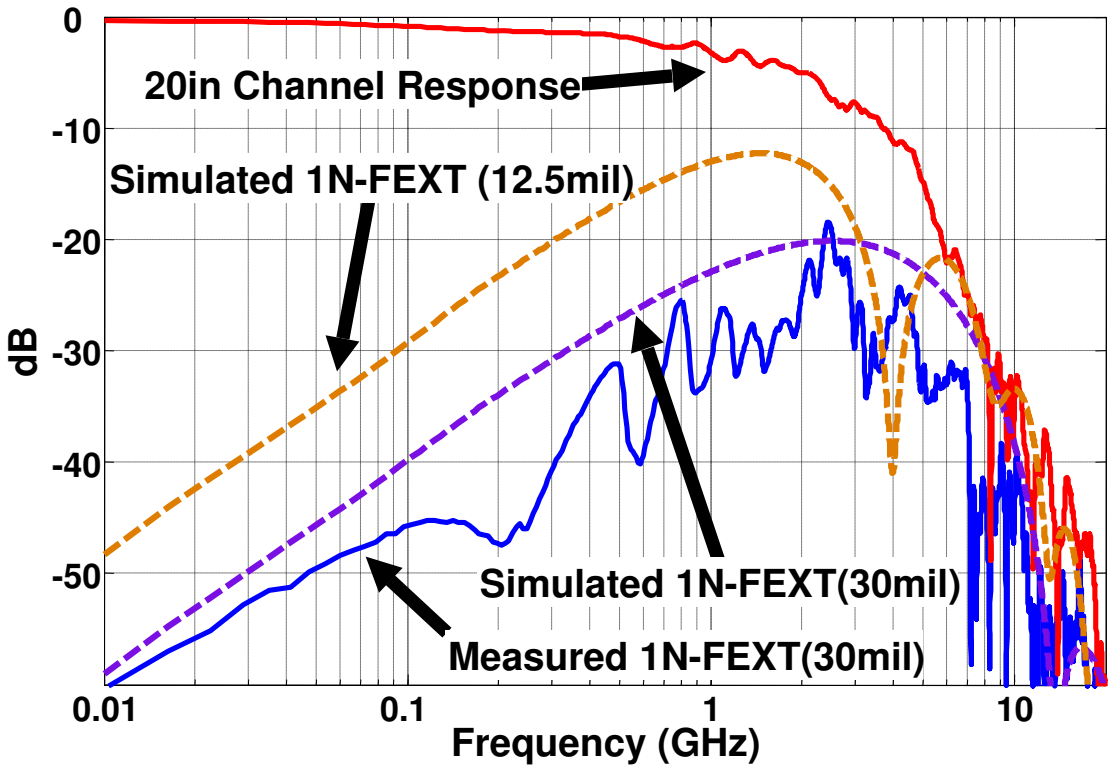

Figure 7.1: Measured & modeled channel, 1N-FEXT with 12.5-mil & 30-mil separations

The proposed research focuses on adapting similar MIMO techniques to high-speed parallel I/O in order to introduce multiplexing gain. MIMO processing method uses the unwanted crosstalk energy to improve BER performance unlike previous techniques that only cancel or suppress crosstalk. Since crosstalk is no longer a major noise source but an extra source of information, lines can be placed closer together to reduce board area needed. Furthermore, data rates can be increased since crosstalk is now used to increase SNR.

In the example provided in Fig 7.1, some of the faster single-ended I/Os that are currently available have a data rate of 2.5-Gb/s per pin with a trace separation of 30

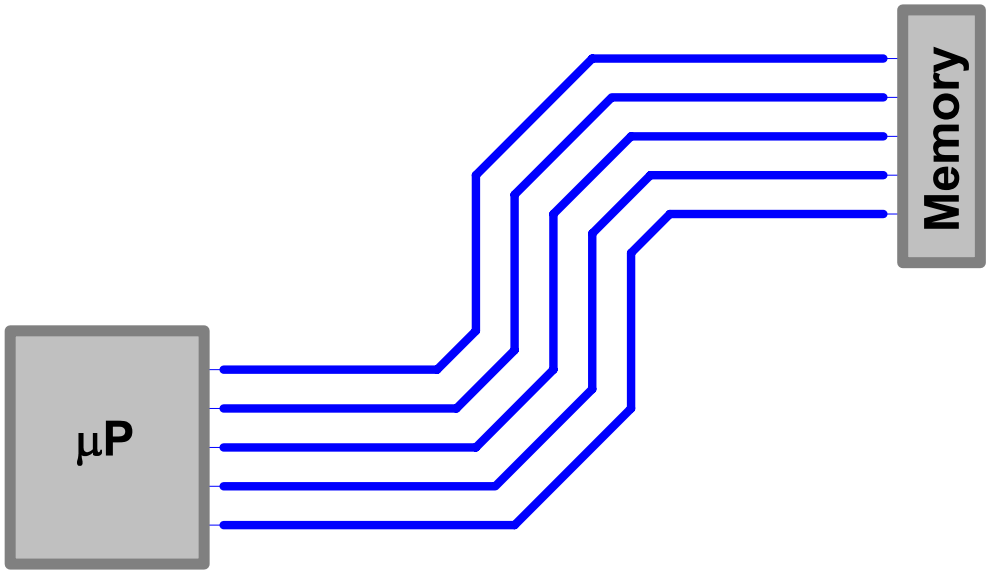

Figure 7.2: Microprocessor-memory parallel bus

mil to ensure that FEXT is 15 dB below the channel response, otherwise negligible, at 2.5GHz. By reducing the trace separation to 12.5 mil, the FEXT amplitude increases to approximately half of the received signal amplitude such that it is only 6dB below the channel response. The proposed MIMO technique can use the FEXT energy to preserve BER performance in this case, allowing the number of parallel links within a given board area to increase by two-fold, which in turn would double the aggregate data throughput.

Unlike most wireless communication systems, chip-to-chip I/O signaling has linear time-invariant channels with similar channel and FEXT responses for each channel. This additional information can be exploited to simplify the application of current wireless MIMO techniques when transferred to wireline systems.

The matrix form of the MIMO channel model for a parallel bus, as illustrated in

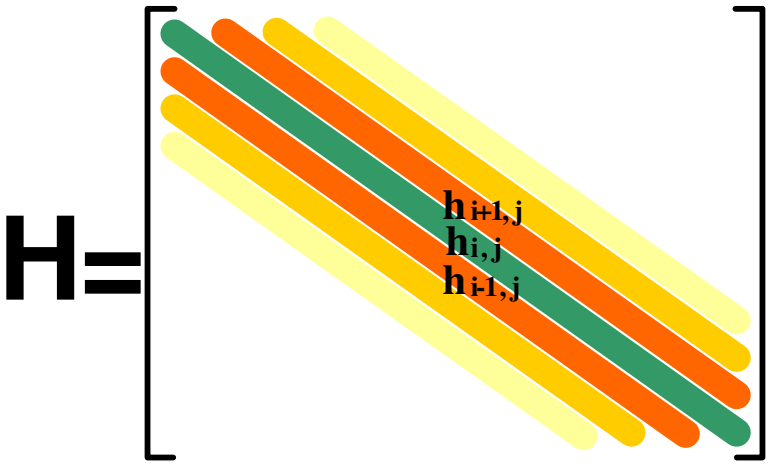

Figure 7.3: Microprocessor-memory parallel bus

Fig. 7.2, can be expressed in the form denoted in Fig. 7.3. Note that the main diagonal of the matrix represents the parallel channels' impulse responses and the diagonals adjacent to the main diagonal correspond to the FEXT terms. The sparseness of the matrix is primarily due to the fact that only close neighbors contribute significant FEXT to the victim line. As described in Section 5.1, the magnitude of the crosstalk terms roughly decreases by D^{-2}, where D is the separation between channels. Therefore, the magnitude of the crosstalk terms decreases for the terms further away from the diagonal.

For any matrix $\mathbf{H}$, its singular value decomposition (SVD) is

$$\mathbf{H} = \mathbf{U}\mathbf{\Sigma}\mathbf{V}^H, \tag{7.1}$$

where the $M_R \times M_R$ matrix $\mathbf{U}$ and the $M_T \times M_T$ matrix $\mathbf{V}$ are unitary matrices and $\mathbf{\Sigma}$ is a $M_R \times M_T$ diagonal matrix of singular values σ_i of $\mathbf{H}$. The parallel decomposition of the MIMO channels can be obtained by manipulating the channel input and output

using transmit precoding and receiver shaping. Multiple FIR filters can be used to implement the matrix $\mathbf{V}$ for precoding, while a similar scheme can be generated at the receiver output to create the matrix $\mathbf{U}^H$. The two matrices transform the MIMO channels into independent single-input single-output channels in parallel. This shapes the crosstalk such that it facilitates the SNR improvement in the channel of interest. The SVD transformation can be mathematically proven as follows:

$$\begin{aligned}
\tilde{\mathbf{y}} &= \mathbf{U^H y} \\
\tilde{\mathbf{y}} &= \mathbf{U^H}(\mathbf{Hx}) \\
\tilde{\mathbf{y}} &= \mathbf{U^H}(\mathbf{U\Sigma V^H})\mathbf{x} \\
\tilde{\mathbf{y}} &= \mathbf{U^H}(\mathbf{U\Sigma V^H})(\mathbf{V}\tilde{\mathbf{x}}) \\
\tilde{\mathbf{y}} &= (\mathbf{U^H U})\mathbf{\Sigma}(\mathbf{V^H V})\tilde{\mathbf{x}} \\
\tilde{\mathbf{y}} &= \mathbf{\Sigma}\tilde{\mathbf{x}}, \qquad (7.2)
\end{aligned}$$

where $\tilde{\mathbf{x}}$ and $\tilde{\mathbf{y}}$ are the transmitted and the received digital bits for the parallel channels and $\mathbf{x}$ and $\mathbf{y}$ are the outgoing and incoming off-chip signals. Since $\mathbf{\Sigma}$ is a diagonal matrix, it shows that the resulting parallel channels do not interfere with each other. This simplified MIMO technique can be extended to multiple lines with varying amounts of crosstalk.

The tangible benefits of this technique are best illustrated with a simple numerical example. To demonstrate the feasibility of the proposed wireline MIMO technique, a $M_R \times M_T$ MIMO channel response matrix $\mathbf{H}$ representing two coupled channels is

constructed such that

$$\mathbf{H} = \begin{bmatrix} h_{channel}[n] & h_{FEXT}[n] \\ h_{FEXT}[n] & h_{channel}[n] \end{bmatrix}, \tag{7.3}$$

where $h_{channel}[n] = h_{1,1}[n] = h_{2,2}[n]$ is the channel response for channel 1 and 2, and $h_{FEXT}[n] = h_{1,2}[n] = h_{2,1}[n]$ is the 1N-FEXT term. For simplicity, the matrix only contains information on two serial links in parallel, which can be easily extended for multiple lines. ISI is ignored in this example to emphasize the benefits of utilizing FEXT energy to improve SNR. In addition, the temporal relationship between FEXT and the received signal is ignored so that the channel and the FEXT responses can each be represented by a simple gain value. Using the channels in Fig. 7.1, the reduced trace separation of 12.5 mil causes the FEXT amplitude to be only 6 dB below the channel's. This means that if the received signal has an amplitude of 1V, the FEXT will have a corresponding amplitude of 0.5V. In order to offer a fair comparison, the transmitter must have a fixed power output, where

$$P_{FEXT} + P_{DATA} = P_{TX}. \tag{7.4}$$

If the received signal of a single link with no FEXT coupling has 1V amplitude, then the amplitude of the received signal of an aggressor line is 0.894V and the coupled FEXT amplitude is 0.447V based on (7.4). Applying the SVD transformation,

$$\mathbf{H} = \begin{bmatrix} 0.894 & 0.447 \\ 0.447 & 0.894 \end{bmatrix} \Rightarrow$$

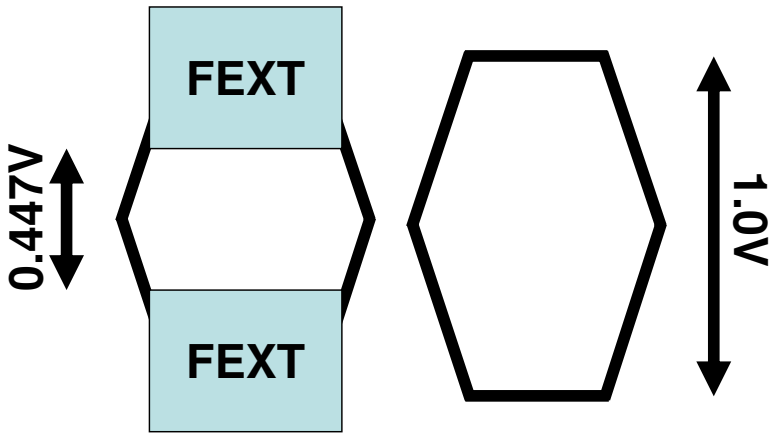

Figure 7.4: Received signal eye without & with MIMO FEXT mitigation

$$\mathbf{U}^H = \begin{bmatrix} -1.057 & 1.057 \\ 0.602 & 0.611 \end{bmatrix}, \mathbf{V} = \begin{bmatrix} -1.057 & 0.612 \\ 1.057 & 0.611 \end{bmatrix}, \mathbf{\Sigma} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \tag{7.5}$$

a transmit precoding filter $\mathbf{V}$ and a receive shaping filter $\mathbf{U}^H$ can be computed such that the two serial links in parallel appear to be independent of one another. Figure 7.4 gives a graphical depiction of the improvement seen in the eye diagram using the MIMO technique, which results in a 124% increase in eye height. Realistic extensions to this example would require incorporating ISI, the temporal relationship between FEXT and the channel, considerations for low power implementations and algorithms for calibration and channel estimation.

7.2 Programmable 7.5-Gb/s MIMO Transmitter

A programmable 7.5Gb/s-per-lane multilane transmitter has been implemented in IBM 0.13μm CMOS process as shown in Fig. 7.5. The proof-of-concept transmitter consists of

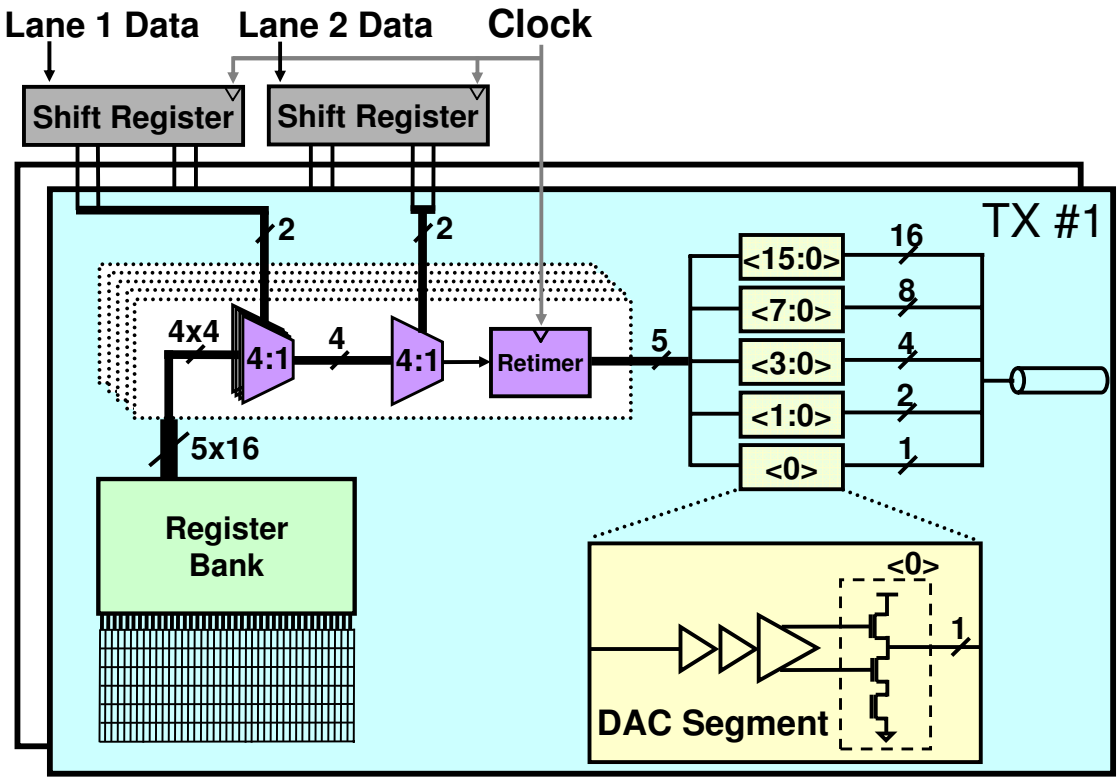

Figure 7.5: System architecture of the programmable 7.5Gb/s-per-lane multilane transmitter

two single-ended lanes each with a maximum achievable data rate of 7.5Gb/s per lane. In order to explore various linear and non-linear MIMO FEXT mitigation techniques, a fully programmable architecture is created such that each output bit of the transmitter can be configured and programmed based on the current and adjacent channel bit sequences. More specifically, the transmitter can store a 5-bit digital-to-analog converter (DAC) value that corresponds to each of the 16 possible 2-bit sequence of the current channel and of the adjacent channel. A 5×16-bit register bank has been implemented for storing all the DAC values for each lane, which can be programmed using a low-speed serial

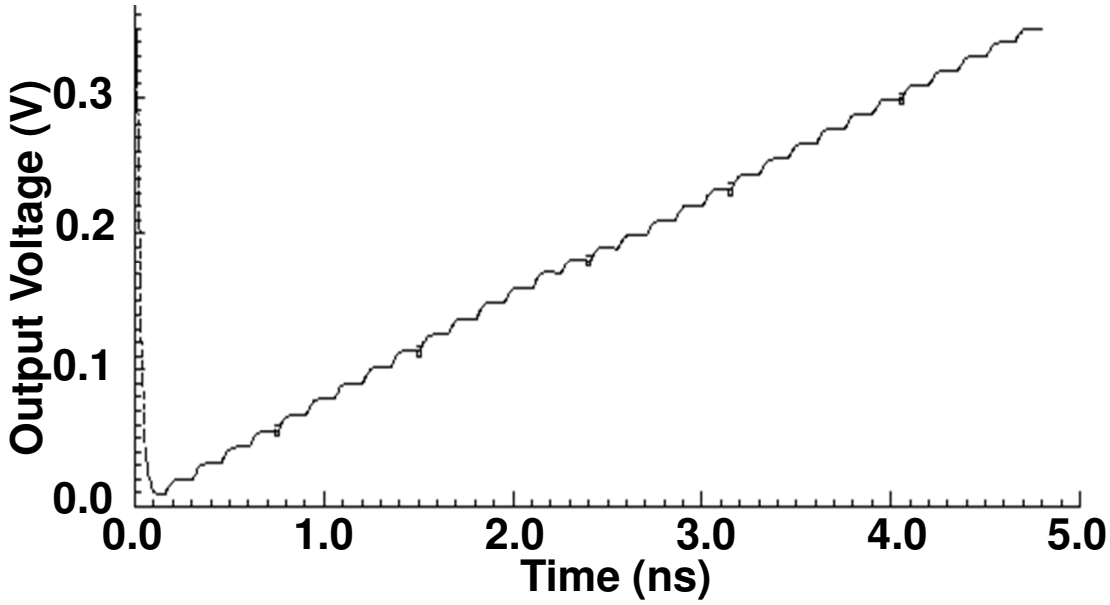

Figure 7.6: Simulation result of all the possible voltage levels in the 5-bit output DAC interface.

To select the proper DAC value at each unit interval, five high-speed 4-bit decoders have been designed to take the cursor and postcursor bits of the two channels and use them as selection bits for each of the five 16:1 MUXes. As depicted in Fig. 7.5, each of the 16:1 MUXes comprises of two stages of 4:1 MUXes and a full-rate retimer. The outputs of the decoders are sent to an efficient, low-power 5-bit DAC that generates a 350-mV$_{pp}$ signal for driving single-ended lines. Simulations show that the DAC can successfully produce 32 different voltage levels as demonstrated in Fig. 7.6. To ensure low power operation while providing 50Ω impedance matching, the output driver uses a 750-mV power supply and controls the output impedance by adjusting the gate voltages of the NMOS transistors in triode. As shown in Fig. 7.7, the output impedance is 50Ω

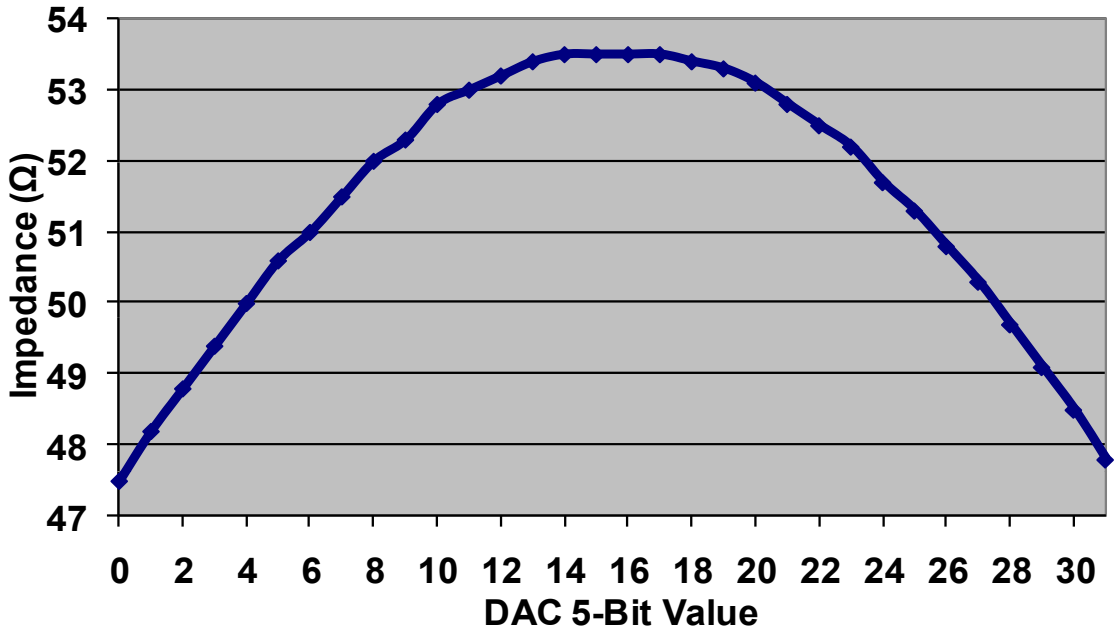

Figure 7.7: A graph of the output impedance vs all possible DAC values

with a tolerance of ± 3.5Ω across all 32 voltage levels.

The chip pictured in Fig. 7.8 occupies 540x380nm^2 of silicon area. Additional chip testing is currently being performed to verify its functionality. Due to its flexible architecture, the transmitter presented in this section can be used in future investigations of MIMO techniques as well as other non-linear equalization schemes.

7.3 Contributions

The research presented in this thesis has shown that FEXT mitigation is necessary to improve signal integrity in high-speed serial links as data rates continue to increase and FEXT becomes a principal noise source that significantly reduces the BER performance

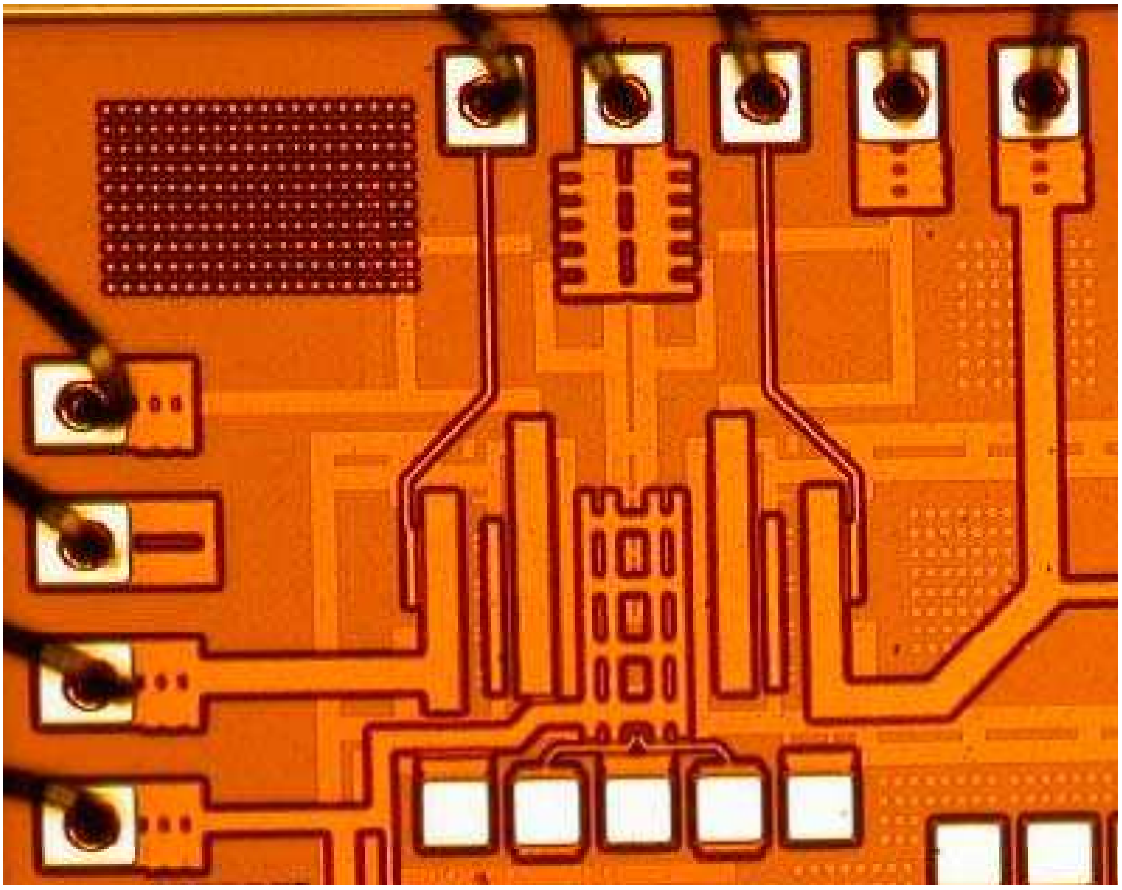

Figure 7.8: Microphotograph of the fully programmable 7.5Gb/s-per-lane multilane transmitter

in chip-to-chip I/Os. There are three different approaches to mitigate FEXT. FEXT can be shifted to eliminate CIJ. It can also be canceled to completely remove the coupled FEXT energy. The third method is to utilize the FEXT energy to help improve the SNR. The main contribution of this thesis is the analysis, design and implementation of the first two techniques.

Although I/O staggering only provides a 10% to 18% improvement in timing margin,

it is simple to incorporate into existing I/O architectures with little additional power and area overhead. Since the technique decreases the voltage margin by shifting the FEXT to the center of the data eye, it is best suited for short distances at high speed, such as processor-memory or core-to-core interfaces. The second technique discussed in this thesis is FEXT cancellation. It reduces CIJ and eliminates FEXT by pre-distorting the transmitted data signal to cancel out the FEXT from adjacent channels. While the technique completely opens the eye, it is power-hungry and area-expensive since it requires two additional XTC FIR filters to cancel FEXT. Therefore, FEXT cancellation should only be used for higher performance I/Os in desktop and server applications. To implement and test the two techniques, the research has contributed and developed many novel high-speed circuits such as the modified active inductor load, a high-speed CMOS flip-flop and a low-power multilane PRBS generator.

In addition to the two FEXT mitigation methods, this thesis has provided new insights and approaches for analyzing and modeling high-speed I/Os. In Chapter 3, an efficient and accurate two-pole FEXT model has been developed using moment matching. The model offers a quick way to estimate the FEXT response between two off-chip interconnects for calibrating the two FEXT mitigation techniques. Analysis has also been done on creating multiple uncorrelated PRBS signals using one PRBS generator. This has significantly facilitated the ability to test multiple transceivers in parallel.

The research presented in this thesis will have a major impact in today's wireline communication interface design. By removing the interference caused by adjacent channels

using the proposed techniques, designers will now have the option to place interconnects closer together. The resulting board area reduction will lower the manufacturing and material costs of the PCB. This is extremely important to consumer electronic manufacturers due to their inherent low profit margins and high price sensitivity. In addition, the new FEXT mitigation methods will permit designers to increase data rates while maintaining the BER performance or use longer interconnects at a fixed data rate. With the on-chip bandwidth exceeding 1THz in future multi-core microprocessors, these techniques will provide the ability to send large amounts of data between different cores and their associated memory.

7.4 Future Directions

Future development in high-speed serial links will focus on boosting the data rate per pin, minimizing the power consumption per I/O, and increasing the number of I/O pins per chip. In order to maximize the I/O speed, advancement in new equalization and coding techniques will be necessary to combat a variety of high-frequency noise including n^{th}-neighbor FEXT, transceiver power supply noise and receiver sampling jitter. Complex algorithms will be created such as the MIMO technique described in Section 7.1 to maintain high signal integrity. Moreover, reducing the complexity of the algorithms will be the key to decreasing its associated power consumption. As technology scaling continues, the power supply will also drop, inherently lowering the power consumption. However, the reduced power supply makes it even more critical to simplify the circuit implementation.

With chips becoming more pin-limited, new methods of communication between chips will also be explored. Research in short-distance wireless chip-to-chip communication and optical communication interfaces will increase the data rate dramatically, thereby reducing the necessary I/O pins.

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