

**Electromigration-Induced Interconnect Aging  
and its Repercussions on the Performance of  
Nanometer-Scale VLSI Circuits**

**A DISSERTATION  
SUBMITTED TO THE FACULTY OF THE GRADUATE SCHOOL  
OF THE UNIVERSITY OF MINNESOTA  
BY**

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**IN PARTIAL FULFILLMENT OF THE REQUIREMENTS  
FOR THE DEGREE OF  
Doctor of Philosophy**

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**June, 2016**

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# Acknowledgements

I am thankful to have worked with my adviser, Prof. Sapatnekar. Stating that I would not be at this stage of writing my PhD thesis without his guidance, is an understatement. In the past five years, which I consider as my most valuable years during which I have struggled, thereby learned a lot, Prof. Sapatnekar has been extremely supportive in every aspect. He has taught me what it really means to think scientifically. He has taught me the importance of being meticulous, in all aspects of work, and in life. I will remember his words about treating success or failure with equanimity, and performing a task with full dedication. I want to express my gratitude to Prof. Sapatnekar for his guidance and support, and I am lucky that I had an opportunity to work with him.

I want to thank my committee members at the University of Minnesota: Prof. Kim, Prof. Yew, and Prof. Sartori, for their constructive feedback about my research. I am grateful to the Doctoral Dissertation Fellowship and the ECE Department Fellowship at the University of Minnesota, Semiconductor Research Corporation (SRC), and the National Science Foundation (NSF), for the resource and financial support towards my thesis project. I want to express my gratitude to the ECE staff, especially Carlos and Chimai, for their help and support. I also want to thank the Minnesota Supercomputing Institute (MSI) at the University of Minnesota, which has been helpful in enabling me to perform simulations and generate results efficiently.

I am grateful to my teachers and my mentors at IIT Bombay. I want to thank Prof. H. Narayanan for his enlightening lectures which got me interested in graphs and network theory. I also want to express my gratitude to Prof. S. B. Patkar, Prof. D. K. Sharma, and Prof. M.P. Desai. Their passion and enthusiasm while teaching the courses in electrical engineering and VLSI, has been an important factor which got me interested in the subject. I also want to thank my friends at IIT Bombay for making life at IIT a memorable experience. I want to express my gratitude to Nikhil, for introducing me to various aspects of computers and making it fun. Thanks to my seniors Vineet and Hrishikesh for looking out for me. I also want to thank Vinay and Anurag, working as a team with them for the design projects was a great learning experience for me.

I would not be at this stage of my life without the support of my family. I want to thank my mother, Dr. Aparna Mishra, for being an everlasting light and a constant source of motivation. I also want to express my gratitude to my grandparents, A. N. Mishra and Indu Mishra for the care, love and affection. I want to thank Dr. Anamika Mishra, Shruti Mishra, Smriti Mishra, and Shweta Tiwari, for teaching me the right values and for making childhood so much fun. I want to thank my sister and my friend, Suvarna for always being by my side, my brother-in-law, Saurabh for being my go-to guy and for all his suggestions and guidance. I want to thank my dear wife, Malveeka, for her encouragement, patience, and for making me realize the importance of humor. Graduate school was stressful sometimes and I feel lucky that she has been around to see through the fog and show me the path.

I want to thank Dr. Marella, Prof. Zhou, Dr. Gupta, and Dr. Boghrati for the help during the starting years of graduate school. I also feel lucky to have collaborated on project and research papers with intelligent minds. I want to thank Palkesh for the brainstorming sessions and his questions which helped me improve my research work. I would also like to thank Dr. Posser, Meghna, Deepashree, Zhaoxin, and Sriharsha for the discussions about my research.

Last but not least, I want to thank my friends in Minneapolis, I feel lucky to have come across such thoughtful individuals during my PhD. Thanks to Neel, Harshada, Mangirish, Prashant, Anuj, Pragya, Arpan, and Brandon for giving me the opportunity to have discussions and arguments with them about various interesting topics and issues, and for making graduate school a joyful experience.

# Dedication

To the memory of my father, Badri Narayan Mishra.

## Abstract

Modern electronic machines are powered by the integrated-circuit (IC), a semiconductor device consisting of compact electronic circuits on a silicon substrate. ICs can contain over a billion fundamental computing elements (transistors) that are connected by a network of metal wires called interconnects. Presently, interconnects constitute a primary bottleneck in achieving required IC performance. One of the major hurdles towards achieving good interconnect performance is electromigration (EM), a physical wear-out mechanism that occurs in metal wires carrying electrical current. EM is projected to limit the performance in future generations of ICs, especially for the wires carrying unidirectional (DC) currents, and is becoming a growing concern in on-chip interconnects across applications ranging from mobile computing to automotive domains.

EM results in redistribution of metal atoms in interconnects that may result in the formation of either voids (empty spaces inside the wire) or extrusions (metal accumulation into the dielectric), and for modern copper-based interconnects, experimental works have observed that failure happens typically through the formation and growth of voids. For modern interconnects carrying large current densities, EM-induced voids can cause a resistance increase in the wire, rendering a wire EM-mortal. The resistance increase in these mortal interconnects can potentially result in circuit performance failure within the lifetime of a product.

The classical methods for EM circuit analysis that are used in the industry to design EM-safe ICs do not capture the reality of EM physics in the realm of modern copper-based interconnects. IC designers use simple, deterministic, empirical EM models and there is a significant gap between such empirical models and the physics-based models that accurately capture the effect of EM in interconnects. The focus of this thesis is to attempt to reduce this gap by combining the two types of models efficiently, capturing the essence of physics-based models into the IC design, thereby enabling the design of EM-robust IC in future technologies. Unlike the classical EM analysis methods that rely on determining failure by extrapolating the EM characteristics of isolated single wires to IC operating conditions, the approach described in this thesis captures the circuit context and uses system failure rather than single-wire failure as the criterion for determining the lifetime of a circuit.

The first part of the thesis proposes a statistical framework to evaluate the circuit performance degradation in on-chip wires through circuit level analysis. Typical on-chip power grids are inherently robust to EM due to redundancies in the interconnect network structure. In these grids, where interconnects typically carry unidirectional currents, the traditional approach to EM analysis is based on the weakest link model, whereby a single wire failure causes the grid to

fail. It is shown here that the power grid can maintain supply integrity even under multiple elemental failures, and this can result in longer and more realistic lifetime predictions as compared with classical approaches.

The next part of the thesis addresses signal interconnects that carry bidirectional (AC) currents as they transport logic signals within the digital system. For these wires, it is shown that EM is not only a catastrophic failure problem, but is also capable of causing parametric shifts in circuit performance over time. We perform HSPICE-based Monte Carlo simulations on a standard on-chip structure to quantify the impact of EM on circuit performance degradation. Although the damage due to EM degradation under bidirectional currents is reduced relative to the unidirectional current case due to partial EM recovery, it is demonstrated that, depending on the level of recovery, the circuit performance may degrade beyond acceptable limits and can be comparable to other transistor degradation mechanisms.

The third part of the thesis addresses the issue of EM mortality in interconnects. A wire may be prevented from being mortal under EM if the maximum stress build-up, corresponding to the equilibrium between the current-induced forward stress and the back stress due to the gradient in atomic concentration along the wire, does not exceed the critical stress due to void nucleation. Alternatively, it may also not be mortal if the stress build-up does not exceed the critical stress over the lifetime of the circuit. A new efficient approach, based on multiple filters, is developed for determining the mortality of wires in a circuit. These filters greatly reduce circuit analysis time by predicting which wires can never be mortal over the circuit lifetime under its operating conditions so that detailed analysis must only be performed over a small subset of all interconnects.

The final part of the thesis studies the effect of EM on via arrays, which redundantly connect the wires in multiple levels of metal in an IC. A stress analysis technique for via arrays is proposed, accounting for differential coefficients of thermal expansion in the materials that make up these structures. The combined impact of thermomechanical stress and redundancy on the via array is determined, and a new model for the impact on the failure of a larger interconnect network is developed. Using the new model, we analyze the EM-induced performance degradation in via arrays of an industrial power grid benchmark circuit.

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# Chapter 1

## Introduction

Integrated circuits (ICs) constitute the core of almost all modern electronic machines that influence our day-to-day lives, from laptops, smartphones to automotive applications. Modern digital ICs contain over a billion fundamental computing units connected by a network of billions of metal wires to perform functional and storage operations in a modern microprocessor. The computing performance of the IC is governed by two fundamental electronic components, namely: (1) transistors, which are the logic-computing units of the IC, and (2) interconnects, which are the network of metal wires linking the transistors to evaluate a desired logic function.

The research and development in the semiconductor industry has been guided by Moore's law [5], which states that the number of transistors in a dense IC doubles in approximately every two years. This trend has been realized in modern-day IC chips by shrinking the sizes of transistors. The integration of billions of transistors and interconnects has been made possible by the progress in the IC manufacturing technology in conjunction with the developments in IC design methods using computer-aided design (CAD) techniques that enable the design of such large circuits efficiently.

Improvements in IC manufacturing design and technology, guided by the predictions (often treated as specification guidelines) from Moore's law, have resulted in an exponential increase in computing power per unit area, arising from the combined effect of individual transistor speedup and the reduction in transistor sizes that allows more transistors to be packed on a chip.

### 1.1 The interconnect crisis in ICs

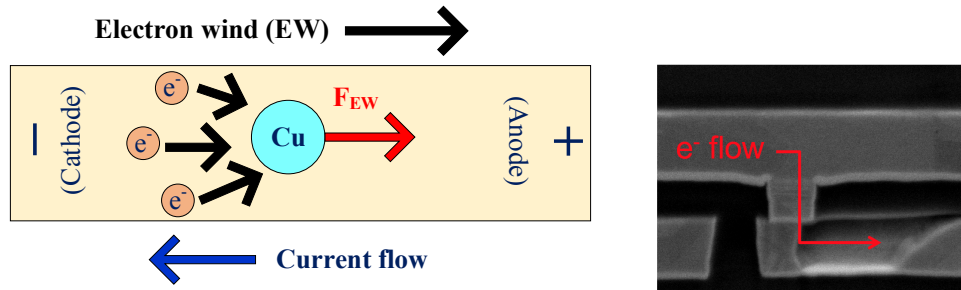
Concurrently with transistor shrinks, the size of the interconnects linking the tightly packed transistors have also been shrunk. However, unlike the transistor performance trend, which

shows an improvement with technology advancement, the interconnect network shows performance degradation [4]. This has become a challenge for the IC technology since there is a rising gap between the performance of transistors and the interconnect. This has resulted in an interconnect crisis for IC technology. The limited interconnect performance is unable to sustain the performance improvement in transistors which results in a large electrical stress in the interconnects. The large electrical stress is quantified by the current density, defined as the electrical current flowing per unit area through the wire. The large current density in the wires as a result of shrinking dimensions and increasing performance requirement can cause interconnect wear-out and affect the reliability of IC, i.e., its capability to function correctly over the lifetime of the product it is embedded into.

## 1.2 Electromigration (EM)

A significant hurdle towards the achievement of reliable interconnect performance is caused by a phenomenon known as electromigration (EM). EM is an interconnect aging mechanism involving gradual migration of the metal atoms activated by momentum transfer from collisions with conducting electrons that are flowing due to electrical current flow in the interconnect [6].

Figure 1.1(a) illustrates the EM phenomenon in an interconnect. The force on the metal (Cu) atoms as a result of momentum transferred by the fast moving electrons is called the electron wind force  $F_{EW}$ . The activated metal atoms move in the same direction as the flow of electrons, from the negative terminal (cathode) to the positive terminal (anode).



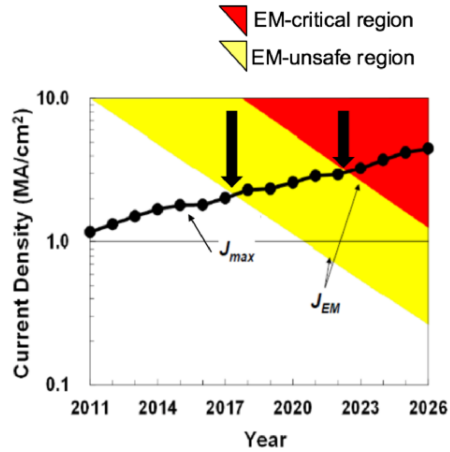
(a) Schematic of the interconnect cross section illustrating EM. (b) SEM image of an EM-induced spanning void [7].

**Figure 1.1:** EM in modern copper interconnects.

When bounded by an atomic blocking boundary, such as an encapsulating barrier layer that prevents metal diffusion in modern copper dual-damascene (Cu DD) wires, this movement causes a depletion of atoms at the cathode, which eventually leads to void nucleation and subsequent

growth [1]. Figure 1.1(b) is an image captured by a scanning electron microscope that shows an interconnect in which a void that is spanning the interconnect cross section, is created as a result of downstream electron flow. The presence of voids can increase the electrical resistance of the interconnect, causing electrical connection damage between transistors thereby causing IC malfunction.

The EM phenomenon in the present era of increasing current densities is considered as a serious issue in the IC industry. The future technology predictions from semiconductor IC experts, as documented in an industry-wide consensus document, The International Technology Roadmap for Semiconductors [4], projects that the technology advancement of ICs is expected to hit a roadblock. Figure 1.2 illustrates the maximum current density trends (corresponding to minimum-sized interconnect) with respect to device performance requirement for future ICs. The two colored regions indicate the current density limits with respect to the target lifetime requirements. For the larger region that is colored in yellow, process solutions exist to tackle the EM problem, such as Cu surface engineering, and adding dopant atoms [4], but for the red region, there are no known proposed process solutions.



**Figure 1.2:** Projected worst-case current density trends [4].

Looking ahead, the process solutions may not be enough to bridge the gap between performance requirement and adequate EM-reliability beyond the year 2023. Even though there may be limited relief available from process enhancements in IC manufacturing technology by building improved materials, it is expected that computer-aided design (CAD) techniques for ICs shall share the bulk of the burden in overcoming EM.



### 1.3 Classical circuit approaches for EM

The classical approach to analyzing EM in circuits involves comparing the current density flowing through a wire, against a global limit. The wire is declared as having failed if it does not adhere to the limit. The EM current density limit has been derived using the following models:

- **The Blech criterion:** In the traditional design flow, some wires in a circuit may be considered immortal, i.e., immune to EM if they satisfy the Blech criterion [8]. The root cause of immortality is related to a back-stress force that is created after the movement of atoms due to EM, which induces a back-flow of atoms to counteract the forward EM-induced atomic flow: when these two balance, the wire is immortal. The details about the role of back-stress are discussed in Section 2.2 and Section 5.3. The Blech criterion states that for a wire with current density  $j$  and length  $L$ , if the product ( $jL$ ) is below a threshold, then it is immortal. Conversely, wires that violate the Blech criterion will be deemed mortal, and the EM wire mortality condition can be written as

$$j L \geq (j L)_{\text{crit}} \quad (1.1)$$

where  $j$  is the current density;  $L$  is the wire length;  $(j L)_{\text{crit}}$  is a constant for the metal.

- **Black's equation:** The wires that are rendered mortal by the Blech criterion need further analysis to check if they can cause EM damage during the lifetime of the product. This has been accomplished by deriving a maximum current density limit rule based on a wire failure criteria measured under accelerated aging conditions through the application of temperature and current stress in a set of interconnect test structures. Under such conditions, failure is deemed to occur when the interconnect resistance crosses a predetermined threshold, and the time at which this occurs is defined as its time to failure. The time to failure parameters from accelerated aging conditions (of the order of hours) are extrapolated to normal operating conditions (of the order of years) using Black's equation [9], which describes the mean time to failure,  $MTTF$  for a wire under EM as

$$MTTF = \frac{A}{j^n} \exp \frac{E_a}{k_B T} \quad (1.2)$$

Here,  $A$  and  $n$  are constants and typical values of  $n$  are between 1 and 2;  $j$  is the current density flowing through the interconnect;  $E_a$  is the activation energy required for EM;  $k_B$  is the Boltzmann's constant;  $T$  is the interconnect temperature.

- **Weakest-link approximation:** The industry practice involves setting up a current density limit, for a given target  $MTTF$  by extrapolating the failure characteristics of test structures as described in the previous paragraph. The time to failure of the test structure

is evaluated by assuming that the circuit fails due to EM at the instant the first component fails. Assuming a system is made up of identical elements, each having a failure probability  $F_1$ , then the failure probability of the system composed of  $N$  such elements can be written according to the weakest-link approximation as

$$F_{\text{system}} = 1 - (1 - F_1)^N$$

This approach is commonly known as the weakest-link approximation (WLA), and is applied to estimate chip level reliability from individual elements [10].

## 1.4 Limitations of the classical approaches

- **The Blech criterion:** Despite the simplicity of the Blech criterion, one of its limitations is that it is based on the assumption that a steady state is achieved between the electron wind and back-stress. For some wires, the time to steady state may surpass the product lifetime, and the Blech criterion may estimate the stress at a time later than the circuit lifetime, leading to inaccurate mortality estimates. This can be a significant problem especially for short-lifetime application such as mobile-computing. This has been discussed in Section 5.1
- **Black's equation:** The issue with using a current density limit derived from Black's equation has to do with its empirical nature, which does not capture the dependence of EM on all the related circuit and process parameters. Moreover, for Cu DD interconnects, complexities in the manufacturing process imply that a straightforward application of Black's equation is untenable. A previous study has indicated that the Black's equation based approach, which was originally meant for aluminum interconnects, is not valid for copper interconnects [11].
- **Weakest-link approximation:** The problem with using the weakest-link approximation has to do with the pessimism in such an approach. The weakest-link approximation will work accurately for a chain-like structures. However, it should be noted that in circuits, variety of topologies occur, and often there is redundancy, which implies that the failure of the first component does not imply circuit failure. Additionally, for interconnects in ICs, as against interconnects in accelerated experiments, the EM failure is context-dependent, i.e., in some cases, small changes in resistance may cause performance failures in the circuit even before the resistance crosses a large threshold, e.g., on critical paths in a clock and data networks in circuits [12]. In other cases, a large failure may be tolerated due to the inherent resilience in the circuit, e.g., due to redundancy in a power grid, where the failure of one wire may be compensated by current flow through other paths, which results in a more resilient performance of the circuit [13].

## 1.5 Thesis objectives

In the previous section, we claim that IC designers use simple, deterministic, empirical EM models throughout the chip design flow, and there is a significant gap between such models and physics-based models that accurately capture the effect of EM in interconnects. The thesis aims to reduce this gap between the two approaches by capturing the essence of physics-based models into the IC design. The thesis project aims at accomplishing the following objectives:

- **Physics-based modeling:** One major objective of this thesis is to use the information from the latest material science and device physics research for modern copper interconnects [10, 14–19] to analyze circuits and accounting for all the important process, material, and environment parameters that can affect EM dynamics in a circuit. Given that EM is a statistical process, the circuit models, in addition to accounting for the physical parameters, should also be able to capture the variation in EM.
- **Accounting for circuit effects:** The existing approaches fail to capture all the important factors that dictate the behavior of EM in modern copper interconnects, such as accurate current density dependence, local self-heating, bidirectional currents, the effect of neighboring wires, and the impact of structural redundancies in the circuit. The thesis aims to account for the influence of such topological, electrical effects that can affect EM.
- **Analyzing EM impact on circuit performance:** Unlike the weakest-link approximation approach, we aim to analyze the direct impact of EM on IC performance, relating the variations in circuit performance metrics with statistical physics based models, an area that has hitherto been unexplored. The emphasis is to enable the design of an EM-robust IC design through developing accurate physical modeling approaches and automated circuit analysis methodologies.
- **Performing computationally efficient EM analysis:** Although, the existing current density checking based models do not capture the EM physics, but they have an advantage of being computationally efficient. In contrast, the EM device-physics based models that capture the physics are accurate, but computationally intensive, and therefore, not applicable for performing EM analysis on billions of interconnects in a modern IC. The thesis focuses on tackling the trade-off between efficiency and accuracy while capturing the physics of EM.

Based on these objectives, the thesis illustrates the accomplishments of the following tasks:

1. **EM-induced probabilistic wire resistance modeling:** This thesis has formulated a non-empirical, probabilistic, physics-based, analytical model that captures the direct

impact of EM on circuit behavior by evaluating the electrical resistance increase due to EM in an interconnect as a function of electrical and interconnect material parameters. Given that EM is a statistical process, the electrical resistance change due to EM which is also a random variable, can vary depending on the variation in the microstructure related properties of the interconnect.

2. **Analysis of signal delay variability due to AC EM:** The thesis incorporates effects arising due to bidirectional (AC) currents. Wires undergoing bidirectional currents may observe near-complete [15] or partial recovery [20] as metal migration occurs in both directions. The thesis captures the performance impact for both partial and complete recovery across multiple process technology nodes.
3. **Accounting for stress-related parameters that affect EM:** The thesis investigates the stress-related parameters that can affect EM, such as the back-stress and the thermo-mechanical stress. The thesis proposes new methods to predict EM wire mortality as a function of product lifetime by accurately and efficiently accounting for back-stress. The thesis also models the role of mechanical stress, which has been observed to be another major driving force for EM at chip operating conditions, in addition to electrical stress for advanced IC technologies. This analysis realistically assumes the connections between multi-layered interconnects as an array of vias.

## 1.6 Thesis organization

The thesis is organized as follows:

- Chapter 2 introduces the physics behind EM and explains the physical model that we have used to account for process, material, and environment parameters that affect EM.
- Chapter 3 describes the probabilistic EM modeling and the circuit analysis framework.
- Chapter 4 discusses the AC EM modeling and the circuit impact on signal wires.
- Chapter 5 and Chapter 6 discuss the circuit modeling techniques that account for the role of stress-related parameters, Chapter 5 discusses the role of temperature, product lifetime, and Chapter 6 illustrates the role of thermomechanical stress and redundancy in via arrays, using finite element analysis and compact modeling to account for the impact of EM-induced via arrays performance degradation in power grids.
- Chapter 7 concludes the thesis.

## Chapter 2

# EM modeling

This chapter describes the basic physics of EM, and discusses the fundamental forces that result in EM-induced atomic flow from the cathode to the anode. The EM-induced atomic flow eventually leads to failure in copper interconnects through the formation of voids or empty space inside the interconnect. The EM-induced voids in Cu interconnects evolve in two different phases, and this chapter discusses the physical model from [1] that captures the multiple phases of void evolution.

### 2.1 EM electron wind force

The fundamental phenomenon responsible for EM in metal interconnects consists of the electron wind force that drives atoms from the cathode end of the wire to the anode. This force is caused by transfer of momentum from moving electrons to the atoms as current flows [9]. The electron wind force,  $F_e$ , is a function of the electric field and material properties of the interconnect and has the form

$$F_e = eZ_{eff}^* E = eZ_{eff}^* \rho j \quad (2.1)$$

where  $e$  is the elementary electron charge,  $Z_{eff}^*$  is a constant that represents the apparent effective charge number, and  $E = \rho j$  is the electric field, where  $\rho$  is the resistivity of Cu and, as before,  $j$  is the current density through the wire. The electron wind force makes it possible for thermally-activated metal atoms to be displaced from their lattice sites and to move in the direction of electron flow through one or more diffusion pathways, producing regions of uneven atomic concentration, i.e., depletion and accumulation. The drift velocity,  $v_d$ , of atoms moving due to the electron wind is

$$v_d = \mu_e F_e \quad (2.2)$$

where  $\mu_e$  is the mobility of metal atoms. The atomic flux due to the electron wind force from the cathode to the anode is given by [6]

$$Nv_d = N\mu_e F_e \quad (2.3)$$

where  $N$  is the atomic density. Further, using the Nernst-Einstein relation as discussed in [21], we have

$$\mu_e = \frac{D_{eff}}{k_B T} \quad (2.4)$$

where  $D_{eff}$  is the effective diffusivity for EM,  $k_B$  is Boltzmann's constant, and  $T$  is the temperature. Using (2.1), (2.2), and (2.4), the drift velocity can be rewritten as

$$v_d = \frac{D_{eff}}{k_B T} (eZ_{eff}^* \rho j) \quad (2.5)$$

and the atomic flux due to electron wind in (2.3) becomes

$$N \left( \frac{D_{eff}}{k_B T} \right) (eZ_{eff}^* \rho j) \quad (2.6)$$

## 2.2 EM-induced back-stress

The diffusion of atoms causes metal depletion at the cathode, resulting in tensile stress, and accumulation at the anode, resulting in compressive stress. This stress gradient results in a stress-induced backflow of atoms, from the anode (site of compressive stress) to the cathode (site of tensile stress), i.e., in a direction that opposes the flux due to the electron wind [8]. The magnitude of this reverse atomic flux is given as

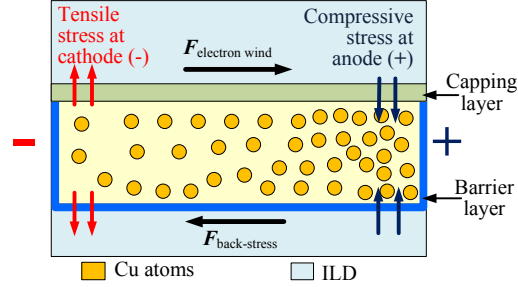
$$N \left( \frac{D_{eff}}{k_B T} \right) \left( \Omega \frac{\partial \sigma_H}{\partial x} \right) \quad (2.7)$$

where  $\Omega$  is the atomic volume,  $\sigma_H$  is the hydrostatic stress, defined as

$$\sigma_H = \frac{\sigma_{xx} + \sigma_{yy} + \sigma_{zz}}{3} \quad (2.8)$$

Here  $\sigma_{xx}$ ,  $\sigma_{yy}$ , and  $\sigma_{zz}$  are the three normal stress components along the conventional Cartesian coordinate system. In the rest of the thesis, the usage of the term stress implies the hydrostatic stress, unless mentioned otherwise. The expression  $\frac{\partial \sigma_H}{\partial x}$  in (2.7) represents the stress gradient along the wire as a result of EM-induced mass transfer from cathode to anode. Therefore, combining (2.6) and (2.7), the net atomic flux due to the combined effect of electron wind and back-stress is formulated as

$$J_{flux}^{EM} = N \frac{D_{eff}}{k_B T} \left( eZ_{eff}^* \rho j + \Omega \frac{\partial \sigma_H}{\partial x} \right) \quad (2.9)$$



**Figure 2.1:** Cross section of a Cu wire indicating the back-stress and the electron wind force.

Figure 2.1 illustrates the two driving forces – the electron wind force, due to the current flow, and the back-stress force. As the movement of migrated atoms is blocked at either end due to the atom-impermeable Ta barrier layer, the electron wind force results in atomic depletion at the cathode, resulting in a tensile stress generation at the cathode. At the anode, the migrated atoms accumulate, creating a compressive stress. As a result of the tensile stress, the voids tend to form at the cathode. In principle, voids may form either inside the via or along the wire. However, process advances using improved liner deposition [10] virtually remove the possibility of voids inside the via.

The work in [8] observed that for a certain range of current and wire length combinations, the wire is immune to EM degradation if the product of the current density through the wire,  $j$ , and the wire length,  $L$  is below a threshold. For these wires, no EM-induced damage occurs because an equilibrium between the back-stress force and the electron wind force is accomplished. This steady state is reached once the two forces balance, and no further net EM-induced atomic flow occurs, i.e., achievement of the steady state, i.e.,  $J_{\text{flux}}^{\text{EM}} = 0$ . Using the above condition in (2.9)

$$\Omega \frac{\partial \sigma_H}{\partial x} + eZ_{\text{eff}}^* \rho j = 0 \quad (2.10)$$

For a constant current flow, the slope of the stress profile at steady state is a constant, i.e.,

$$\left| \frac{\partial \sigma_H}{\partial x} \right| = \left| \frac{\Delta \sigma_H}{L} \right| = \frac{eZ_{\text{eff}}^* \rho j}{\Omega} \quad (2.11)$$

At **steady state**, the stresses at the cathode and anode are anti-symmetric [22], and the stress gradient at the cathode can be written as  $\frac{\Delta \sigma_H}{L} = \frac{2\sigma_{\text{cathode}}}{L}$ , where  $\sigma_{\text{cathode}}$  is the tensile stress at the cathode. If the tensile stress at the cathode, at steady state, is smaller than the critical value required for the nucleation of void,  $\sigma_c$ , the wire will be literally immortal to EM damage, for all time, i.e., the stress  $\sigma_{\text{cathode}} < \sigma_c$ . Using the above relations, along with (2.11), we obtain

$$\frac{eZ_{eff}^* \rho j}{\Omega} = \frac{2\sigma_{cathode}}{L} \leq \frac{2\sigma_c}{L} \quad (2.12)$$

$$\implies \frac{eZ_{eff}^* \rho j}{\Omega} \leq \frac{2\sigma_c}{L} \quad (2.13)$$

$$\implies (j L) \leq \frac{2\sigma_c \Omega}{eZ_{eff}^* \rho} = (j L)_{crit} \quad (2.14)$$

This is the threshold used in the Blech criterion described in Section 1.3

## 2.3 Critical stress

Note that the critical stress is treated as the *effective value* which incorporates the residual stress(es) in the interconnect, such as the tensile stress due to thermomechanical properties mismatch between copper and surrounding materials. Experimental works characterize the effective value of critical stress using (2.14) [22]. This effective value,  $\sigma_c$ , can be written in terms of the absolute value of critical stress,  $\sigma_{abs}$ , and the residual stress,  $\sigma_o$  as

$$\sigma_c = \sigma_{abs} - \sigma_o$$

In the thesis, critical stress refers to the effective critical stress value unless explicitly mentioned otherwise. For simplicity, in all but Chapter 6, the critical stress value is a constant effective value, chosen as the stress over and above the residual stress in the interconnect. In Chapter 6, we will elaborate an approach which attempts to model the possible causes of variation in critical stress and residual stress.

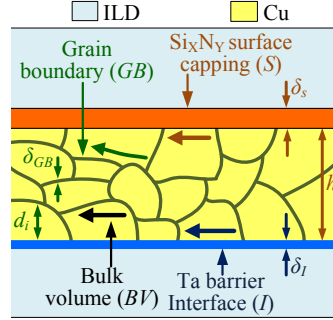
The critical stress for Cu interconnects has been observed to have a smaller value compared to their predecessors, the Al interconnects. There has been research works which have investigated the reasons behind the low critical stresses in Cu as compared to Al, and this is attributed to a weaker bonding between the Cu liner and metal [23]. The problem is exacerbated by the usage of low-k dielectric [22, 24]. In contrast, Al bonds well with its oxide coating and is manufactured using SiO<sub>2</sub> as dielectric instead of low-k dielectric, such as SiCOH.

## 2.4 EM diffusion in Cu DD

We will discuss the EM-induced atomic diffusion mechanism in modern Cu interconnect, under the influence of the driving forces that were described in the previous section. We begin by outlining a typical Cu DD process. At the position where the wire is to be located, a trench is first etched into the interlayer dielectric (ILD). Next, a Ta-based barrier is deposited therein, and the Cu used to construct the interconnect is then deposited within the trench. The role of



the barrier is to prevent Cu from diffusing into the ILD. Finally, the wires are capped above by a silicon nitride ( $\text{Si}_x\text{N}_y$ ) layer.



**Figure 2.2:** Cu DD interconnect cross-section showing possible atomic diffusion paths.

The structure of a Cu DD interconnect is key to understanding the effective diffusivity,  $D_{eff}$ , an important parameter in (2.9) that affects EM-induced performance degradation. This parameter can be considered as the sum of the contributions of atomic transport along various diffusion paths. These diffusion paths are a function of the microstructure of the interconnect, which is the arrangement of grains, i.e., regions of similar physical properties that are visible at microscopic levels of magnification. Figure 2.2 is a schematic that illustrates the cross-section of a Cu DD interconnect, showing grains within the metal wire and the regions of intersection of the grains, known as the grain boundaries. The diffusion pathways available for the migration of metal atoms are as follows

- along the grain boundaries ( $GB$ ),
- through the bulk volume ( $BV$ ),
- through the nonideal Ta barrier interface ( $I$ ), and
- through the capping surface ( $S$ ).

For a wire of height  $h$  and width  $w$ ,  $D_{eff}$  can be considered as a sum of contributions of atomic transport along these four pathways, and can be modeled as [25]

$$D_{eff} = D_I \delta_I \left( \frac{2}{w} + \frac{1}{h} \right) + D_S \delta_S \left( \frac{1}{h} \right) + D_{GB} \delta_{GB} \left( \frac{1}{d} \right) + n_{BV} D_{BV} \quad (2.15)$$

where the subscripts correspond to the diffusion pathway,  $D_I$ ,  $D_S$ ,  $D_{GB}$ , and  $D_B$  are diffusion constants,  $\delta_I$ ,  $\delta_S$ , and  $\delta_{GB}$  denote the effective thicknesses,  $d$  is the grain size along the longitudinal direction (Figure 2.2 shows  $d_i$  which is the grain size of the  $i^{\text{th}}$  grain), and  $n_{BV}$  is the fraction of atoms diffusing through the bulk volume.

Typically it has been observed that the bulk and interface diffusion contribution can be neglected compared to diffusion along the capping surface and grain boundaries [21]. This results in the following simplified expression

$$D_{eff} = D_S \delta_S \left( \frac{1}{h} \right) + D_{GB} \delta_{GB} \left( \frac{1}{d} \right) \quad (2.16)$$

Depending on the properties of the interconnect microstructure, additional terms can be omitted. For instance, the grain boundary component can be neglected in interconnects that have a bamboo-like grain structure wherein the grain boundaries are perpendicular to the width of the wire [21] and there is no continuous path for EM-induced atomic diffusion. For EM modeling in such a scenario, the surface diffusivity term dominates and the effective diffusivity can be simplified as

$$D_{eff} = D_S \delta_S \left( \frac{1}{h} \right) \quad (2.17)$$

For previous technology nodes, the Cu microstructure was composed of bamboo-like grains and (2.17) could be used to model the effective diffusivity. However, it is observed that the Cu microstructure has become increasingly polygranular, with a mixture of bamboo-like and polycrystalline microstructure. At present technology nodes, the Cu microstructure is dominated by fine grains, resulting in a largely polycrystalline structure [10]. This polycrystalline structure introduces a large number of grain boundaries, adding more potential paths for grain boundary diffusion. Additionally, process enhancements such as the introduction of CoWP as an alternative material to  $\text{Si}_x\text{N}_y$ , have retarded the electromigration diffusion along the capping surface [4, 14, 26]. Therefore, for advanced technology nodes, the primary diffusion path for EM is along the grain boundaries and the effective diffusivity becomes

$$D_{eff} = D_{GB} \left( \frac{\delta_{GB}}{d} \right) \quad (2.18)$$

The correct expression to be used for EM modeling depends on the context with respect to the microstructure of the wire. In this chapter, we compare our results against the 3-D EM model based simulation work in [27] in Section 3.4.1 that performs statistical EM analysis for single Cu DD interconnects, using Finite Element Analysis (FEA) for simulating void nucleation, supplemented with a compact modeling approach for void growth. For comparison with the FEA results in [27], we use (2.17) since those, simulations are performed on wires with a bamboo-like grain structure. In contrast, for our power grid simulations in Section 3.4.2, we use (2.18) in order to be consistent with the process conditions in state-of-the-art technologies, where as noted above, the microstructure is observed to be polygranular.

## 2.5 EM-induced void evolution

The diffusion of atoms eventually leads to formation and growth of *voids* or empty spaces in the interconnects. For both Al and Cu, experiments indicate that EM failure in Cu interconnects occurs in two phases [11, 27], which are described as follows:

- *Void nucleation*: Under EM, the depletion of atoms at the cathode creates a tensile stress. Once this exceeds a critical stress threshold value, the void nucleates.
- *Void growth*: After nucleation, further movement of metal atoms from the void results in void growth, resulting in increased wire resistance since the void effectively reduces the cross-section available for current flow.

In order to evaluate the dynamics of the void evolution, we need to model the stress inside the interconnect. There are multiple models that can be used for modeling the physics of EM-induced void in circuits. One of the most popular approach is based on the work from Korhonen [1]. Recent works in power grid analysis have proposed EM modeling approaches based on evolution of vacancy and plated atom concentrations, e.g., the model from [28], which is used in power grid analysis [29]. In this thesis, we will use the model from [1], commonly referred to as the Korhonen model.

The Korhonen model uses the atomic flux relation in (2.9) in conjunction with the continuity equation to represent the dynamics of EM atomic flow in interconnects. The dynamic interplay between electron wind and back-stress forces is described by a differential equation, given as

$$\frac{\partial \sigma_H}{\partial t} = \frac{\partial}{\partial x} \left[ \kappa \left( \frac{\partial \sigma_H}{\partial x} + G \right) \right] \quad (2.19)$$

where  $\kappa = \frac{D_{eff} B \Omega}{k_B T}$ ,  $G = \frac{e Z_{eff}^* \rho j}{\Omega}$ , and  $B$  is the effective bulk modulus for the Cu and interlayer dielectric system; other terms have been defined previously in Section 2.1 and Section 2.2. The work in [1] also proposes solutions to this differential equations under appropriate boundary conditions, corresponding to two scenarios:

1. Semi-infinite (*SI*) wire, i.e., a wire of infinite length bounded at one end by a via.
2. Finite length (*F*) wire, i.e., a wire of finite length,  $L$ , bounded at both ends by a via.

The cathode for the wire is at  $x = 0$  in both cases; for the semi-infinite case, the anode is at  $\infty$ , while for the finite wire, the anode is at a finite  $x = L$ . For each case, the solution is based on the boundary condition that the net atomic flux at the endpoints enclosed by vias is zero. The zero flux at an interconnect endpoint occurs because the Ta barrier at the vias in a Cu DD

process blocks the flow of metal atoms. The zero flux boundary conditions (*BC*) for each of these two scenarios are given as:

$$BC_{SI} : \frac{\partial \sigma}{\partial x} + G = 0, \text{ at } x = 0, \text{ for all } t \quad (2.20)$$

$$BC_F : \frac{\partial \sigma}{\partial x} + G = 0, \text{ at } x = 0, x = L, \text{ for all } t \quad (2.21)$$

The analytical solutions of (2.19), corresponding to the above two scenarios, were originally proposed in [1] and a detailed derivation leading to the solution is performed in Appendix A. The solutions can help to predict the conditions for formation and growth of EM-induced voids in a wire, and constitute the foundation for EM physical models in older Al and current-day Cu interconnect metallization technologies.

If  $m_n = (2n + 1)\pi$ , the stress solutions are [1]

$$\sigma_{SI}(x, t) = G \left[ \sqrt{\left(\frac{4\kappa t}{\pi}\right)} e^{-\frac{x^2}{4\kappa t}} - x \operatorname{erfc}\left(\frac{x}{\sqrt{4\kappa t}}\right) \right] \quad (2.22)$$

$$\sigma_F(x, t) = GL \left[ \frac{1}{2} - \frac{x}{L} - 4 \sum_{n=0}^{\infty} \frac{e^{-m_n^2 \frac{\kappa t}{L^2}} \cos\left(\frac{m_n x}{L}\right)}{m_n^2} \right] \quad (2.23)$$

For copper interconnects voids typically form near the cathode [30], and the stress evolution at the cathode ( $x = 0$ ) is of primary interest. The stress solutions at  $x = 0$  are [1].

$$\sigma_{SI}(0, t) = 2G \sqrt{\frac{\kappa t}{\pi}} \quad (2.24)$$

$$\sigma_F(0, t) = GL \left( \frac{1}{2} - 4 \sum_{n=0}^{\infty} \frac{e^{-m_n^2 \frac{\kappa t}{L^2}}}{m_n^2} \right) \quad (2.25)$$

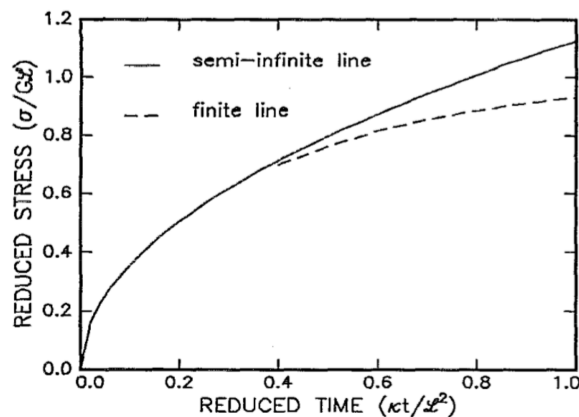
The time for nucleation of the void can be evaluated by evaluating the time when the stress inside the interconnect is equal to the critical stress. if the stress at the cathode is denoted as  $\sigma(0, t_n)$ , then at nucleation time,  $t_n$ ,

$$\sigma(0, t_n) = \sigma_c \quad (2.26)$$

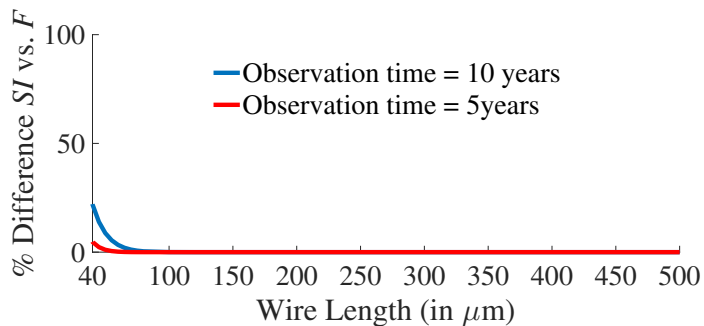
In order to evaluate the nucleation time,  $t_n$ , we can chose either the *SI* or the *F* solution from (2.25), but there are trade-offs with respect to computational efficiency and accuracy. For wires in ICs, the length,  $L$ , may vary from a scale of micrometers to hundreds of micrometers. The solution corresponding to the finite wire BC is a realistic choice, since it directly models the length dependency. However, the finite wire solution,  $\sigma_F$ , includes an infinite series, which makes its exact evaluation computationally difficult.

The advantage of the solution for the *SI* boundary condition is compact, and thus useful in circuit analysis for multi-million wire systems [13,31]. However,  $\sigma_{SI}$  is pessimistic since the *SI*

case experiences lower back-stress. Moreover, the *SI* model has no length dependence since the wire has infinite length. In Chapter 5, we discuss the details about the trade-off between the usage of two solutions for EM analysis. However, the semi-infinite solution has a simple form which is easy to compute, is guaranteed-pessimistic, and closely matches the accurate stress solution as shown as indicated in Figure 2.3. For, an observation time of 10 years, the error arising as a result of usage of the *SI* solution is <20% for wire length  $L \geq 40\mu$  as indicated in Figure 2.4. For a smaller observation time of 5 years, corresponding to mobile computing, the two solutions almost completely match for the range of wire lengths from  $40\mu\text{m}$  to  $500\mu\text{m}$  as shown in the figure. The process parameters for the simulation are imported from Table 3.4.



**Figure 2.3:** Stress at the blocking boundary (cathode): Comparison between the *SI* and *F* solutions as shown in [1], using normalized parameters.



**Figure 2.4:** Percentage difference between the *SI* and *F* solutions from [1], evaluated for typical wire lengths at  $T=100^\circ\text{C}$ .

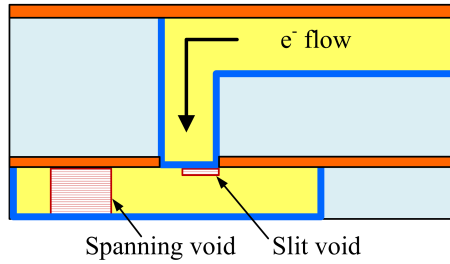
Therefore, for our probabilistic analysis of power grids, we choose the solution from corresponding to the semi-infinite wire. The analytical solution from [1] states that the time,  $t_n$ , at which a void nucleates

$$t_n = \frac{K_{t_n}}{D_{eff}} \quad (2.27)$$

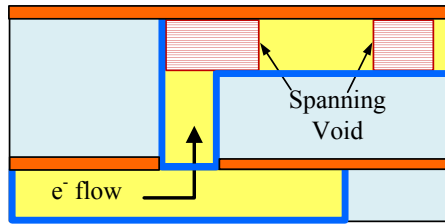
$$\text{where } K_{t_n} = \frac{\pi}{4} \left( \frac{\sigma_c^2 \Omega k_B T}{(e Z_{eff}^* \rho j)^2 B} \right) \quad (2.28)$$

where  $\sigma_c$  is the *effective critical stress* for void nucleation.

After nucleation, the void begins to grow. Various void growth scenarios have been observed in Cu DD structures, depending on the direction of the current [31]. The scenario where the electron flow is downwards, shown in Figure 2.5(a) corresponds to the via-above case (i.e., the via is located above the void), and results in potential void formations at the via or in the wire, as illustrated. For the case where the electron flow is upwards, shown in Figure 2.5(b), an upstream void is potentially formed in the upper wire, typically at a corner of the wire or within the wire, as shown (i.e., the via is located below the void). Through process enhancements, voids inside the via trench have been resolved [32] and are therefore not considered here.



(a) Via-above case.



(b) Via-below case.

**Figure 2.5:** Mechanisms of void evolution for the via-above and via-below cases (microstructure not shown for simplicity).

The mechanics of void formation in each case – *spanning growth* (for both the via-above and via-below cases), when the void spans the entire interconnect, and *slit growth*, where it forms along the via (for the via-above case) – is different and necessitates different modeling approaches. Although slit voids tend to form earlier than spanning voids, it is easy to build redundancy into the power grid to guard against slit voids by inserting redundant vias; in fact, this is often implemented during the wire routing stage. Moreover, recent process enhancements in Cu DD metallization technology, such as the introduction of new barrier technologies [18] can mitigate the possibility of slit void formation. Regardless, for via arrays the slit voids may affect EM performance in addition to spanning voids, and in Chapter 5 we will focus our attention on slit voids in via arrays. Prior to Chapter 5, we focus our attention on the impact of spanning voids only.

For spanning voids, once a void is formed, the primary mechanism of growth in the void size is due to drift under an electron wind force, with a constant drift velocity  $v_d$  [27, 33]. If the void nucleates at time  $t_n$ , then at an observation time  $t_o$ , the void has been growing for a length of time,  $t_o - t_n$ . The length of the void increases due to drift, as given by

$$L_{void}(t_o) = v_d \cdot (t_o - t_n) = \left( \frac{D_{eff}}{k_B T} \right) e Z_{eff}^* \rho j (t_o - t_n) \quad (2.29)$$

where the second equality follows from (2.5).

The equations for the model that we use have a simple form, and the stress predicted is pessimistic [1]. This has been the basis of its usage in other circuit analysis works such as [31, 34]. Additionally, note that the equations are valid for single isolated interconnects. However, in power grid circuits, the interconnects are connected through vias. In Section 3.2.4, we illustrate that the impact of current flowing through neighboring wires can be modeled using the idea of current divergence.

## 2.6 The role of temperature and Joule heating on EM

At first sight, if we observe the temperature dependence of the nucleation time,  $t_n$ , drift velocity,  $v_d$ , and void length,  $L_{void}$ , in (2.5), (2.27), and (2.29), we notice that  $t_n$  appears to increase, while  $v_d$  and  $L_{void}$  reduce as temperature increases. However, accelerated temperature EM experiments indicate the opposite trends. This apparent anomaly is explained by examining the exponential dependence of EM diffusivity on temperature [31]

$$D_{eff} = D_0 \exp \left( - \frac{E_a}{k_B T} \right) \quad (2.30)$$

where  $D_0$  depends on the microstructure of the wire, as discussed in Section 2.4, and  $E_a$  is the activation energy for EM diffusion, which signifies the amount of energy that a thermally

activated metal atom must gain in order to dislocate from its lattice site and migrate in the direction of electron flow along the dominant diffusion path(s). Alternatively,  $E_a$  represents the energy barrier that a thermally activated metal atom needs to overcome in order to dislocate and move in the direction of electron flow.

Observing the form of (2.30), it is clear that as the temperature increases, there is an exponential increase in effective diffusivity, thus resolving the apparent anomaly in (2.5), (2.27), and (2.29) reported above, and showing that EM causes more damage at higher temperatures.

In fact, the above argument shows that small perturbations in  $T$  can offset EM calculations significantly, and using an accurate temperature value is of utmost importance in order to accurately analyze performance degradation due to EM. In a circuit context, current flow in a wire can result in Joule heating, which causes an increase in the temperature and thereby accelerates EM. Therefore, to quantify the performance impact of EM accurately, the temperature increase due to Joule heating must be accounted for.

We use the model described in [35] to evaluate the interconnect temperature due to Joule heating given as

$$T = T_{\text{ref}} + \Delta T_J \quad (2.31)$$

where  $T_{\text{ref}}$  is the reference temperature of the interconnect, and  $\Delta T_J$  depends on the RMS current through the wire [35]

$$\Delta T_J = I_{\text{rms}}^2 R R_\theta \quad (2.32)$$

where  $R$  is the wire resistance and  $I_{\text{rms}}$  is the RMS current flowing through the interconnect. In our case, since the logical blocks which drive current are assumed to have steady state DC currents, therefore, the RMS current flowing through the wire is taken as the corresponding DC current. The parameter,  $R_\theta$ , represents the thermal impedance and is given by

$$R_\theta = \frac{t_{\text{ins}}}{K_{\text{ins}} L_{\text{wire}}(w + 0.88t_{\text{ins}})} \quad (2.33)$$

where  $t_{\text{ins}}$  is the thickness of the dielectric below the interconnect and is a function of the metal layer occupied;  $K_{\text{ins}}$  is the thermal conductivity;  $L_{\text{wire}}$  and  $w$  denote the length and the width of the wire, respectively.



## Chapter 3

# Probabilistic wire resistance degradation due to EM

This chapter discusses the detailed derivation of the analytical probabilistic EM modeling in the context of power grid circuits. Section 3.1 provides an introduction to our probabilistic EM analysis formulation, Section 3.2 describes our EM model that incorporates the variation in interconnect microstructure parameters that influence void dynamics, and thereby predicts the probabilistic evolution of EM-induced voids and the consequent probabilistic change in resistance. The impact of EM-induced wire resistance change on circuit performance parameters is observed by performing Monte Carlo (MC) circuit simulation using our statistical framework that is described in Section 3.3, and in Section 3.4 we numerically evaluate our approach and compare our results works that perform finite element simulation at accelerated conditions to observe EM dynamics. We also discuss the results and implications of our analysis to capture the impact of EM on the IR drop for a set of industrial power grid circuit benchmarks.

### 3.1 Introduction

As discussed in Section 1.3, traditional EM analysis is based on failure criteria measured under accelerated aging conditions through the application of temperature and current stress in a set of interconnect test structures. Under such conditions, failure is deemed to occur when the interconnect resistance crosses a predetermined threshold, and the time at which this occurs is defined as its time-to-failure. Also, in the traditional design flow, some wires in a circuit may be considered immortal, i.e., immune to EM. For mortal wires that do not satisfy the Blech criterion described in Section 1.3, Black's equation is applied to derive maximum current density

limit rules, declaring a wire as having failed if it does not adhere to the limit.

There are several problems with such an approach. First, in a real circuit, the impact of such failures is context-dependent. In some cases, small changes in resistance may cause performance failures in the circuit even before the resistance crosses a large threshold, e.g., on critical paths in a clock and data networks in circuits [12]. In other cases, a large failure may be tolerated due to the inherent resilience in the circuit, e.g., due to redundancy in a power grid, where the failure of one wire may be compensated by current flow through other paths, which results in a more resilient performance of the circuit [13,29]. Therefore, the use of a single threshold for the resistance change may either be excessively conservative, or not conservative enough, depending on how the threshold is chosen and on the sensitivity of circuit failure to a resistance change in a specific interconnect. Second, for Cu DD interconnects, complexities in the manufacturing process imply that a straightforward extension of prior EM approaches is untenable. A previous study has indicated that the Blech criterion based approach, which was originally derived for aluminum interconnects, is not valid for copper interconnects, and that some lines fail *probabilistically* even if they satisfy the Blech criterion on the value of their  $jL$  product [36,37].

These peculiarities for Cu DD wires indicate the need to develop EM models that incorporate the physics specific to such interconnects, and to enable probabilistic circuit analysis in a context-sensitive manner. The probabilistic viewpoint reflects both the fact that EM mechanisms are stochastic, and that the number of interconnects on a chip is large enough that these effects may be manifested over the chip.

There have been few prior publications that have explored these directions. The work in [34] built up on [31] to consider some EM issues beyond the conventional Black’s equation, but it was partly based on the traditional Blech criterion. The resilience of power grids to EM due to structural redundancies has been utilized in the industry, and has been pointed out in [13], which is based on a physics-based statistical method. The idea of accounting for redundancy in power grids while analyzing EM was subsequently also used in [38,39], but these methods were primarily based on Black’s equation. The work in [29] uses a physics-based model that incorporates the role of mechanical stress. The authors indicate that the variation in EM lifetimes is caused due to the variation in the structure of the metal interconnect at the microscopic level, i.e., its microstructure. Their consideration of the statistical nature of EM focuses on evaluating the mean of the EM-induced circuit performance shift, and the variation in the circuit performance shift due to probabilistic EM-induced degradation is not captured.

We propose a probabilistic EM analysis framework that incorporates the impact of variation in the material properties of the interconnect on EM performance of a circuit. Starting from the known distributions of parameters related to the microstructure, such as activation energy

and grain size, our framework uses an analytical model to predict the distribution of EM-induced void growth and consequently, the EM-induced resistance change in the wire. A new mortality criterion is developed, based on the underlying statistics that drive EM. Based on the distribution of the change in the wire resistance, we calculate the circuit performance degradation by observing the IR-drop variation in standard power grid benchmarks.

## 3.2 Probabilistic modeling of EM failure

The conventional explanation of EM in interconnects was predicated on the interaction between the electron wind force and the back-stress force as described in Section 2.2. For some interconnects, with low current and/or small length, the two forces could be in equilibrium in the steady state so that the critical stress  $\sigma_c$  for void nucleation is never reached, implying that these wires are immortal to EM effects. For a wire of length  $L$  with current density  $j$ , the Blech criterion for immortality can be derived from (2.9) by considering the steady state scenario where the stress does not change with respect to time and the forward and backward flux are in equilibrium.

As noted in Section 3.1, it has been observed that the immortality property does not hold for Cu DD interconnects. This is due to a significantly lower value of critical stress,  $\sigma_c$  for Cu DD compared to Al interconnects, which results in voids being formed easily in Cu DD interconnects, and lines are apt to show probabilistic behavior [36, 37]. In effect, every line has a nonzero probability of failure, regardless of its  $jL$  value and it is possible for voids to nucleate early, before providing the opportunity for opposing back-stress forces to build up to balance them. This nonzero failure probability is our motivation for using an analytical model for probabilistic EM. Void evolution characteristics, which are required to calculate the EM-induced probabilistic resistance increase, are imported from the nucleation and growth model formulae discussed in Section 2.5. Unlike the Blech criterion, these formulations consider the transient as well as the steady state for stress.

We construct our model by attributing the causes of variation to fundamental material parameters that impact the EM-induced void nucleation and growth, characterized by (2.27) and (2.29). In the remainder of this section, we will derive the formulae that predict the statistics of EM-induced void evolution as a result of the possible sources of variation. This analysis will allow us to evaluate the resistance change as a result of nucleation and growth of voids.

### 3.2.1 The role of microstructure in probabilistic EM behavior

Recent works have observed that EM failure is correlated to uncertainties in the microstructure parameters of an interconnect, which relate to the statistical distribution of the activation energy [27] and/or grain size [40].

### Activation energy variation

As discussed in Section 2.6, the activation energy,  $E_a$ , is a property of the microstructure. It has been experimentally observed that  $E_a$  can vary within the wire depending on the grain boundary orientation. For instance, EM activation energy can vary between grains depending on the orientation of the grain with respect to each other and with respect to the interfacial layer [41, 42]. Therefore, we work with the idea of the effective activation energy for each wire, which is an averaged activation energy value for that wire. In the rest of this thesis, we use  $E_a$  to refer to the effective activation energy for each wire, taken at a macroscopic level. This parameter has been experimentally found to be normally distributed, and we model it as an independent Gaussian random variable; further, it is reasonable to assume that the effective activation energy is same for a wire and varies only between the wires [27, 41, 43–46].

### Grain size variation

Experiments in [40] have shown a correlation between the experimental EM lifetimes and another microstructure property, the effective grain size, defined as the grain size value averaged over all grains in a wire.

## 3.2.2 Statistical models for void dimensions

Based on the assumptions mentioned in the previous section about  $E_a$  and  $d$ , we will now present a probabilistic framework that will enable us to obtain the EM-induced void characteristics and the corresponding resistance change as a result of void nucleation and growth.

In our discussion below, for a distribution  $Z = N(\mu, \sigma)$  with the mean  $\mu$  and standard deviation  $\sigma$ , we denote a lognormal  $X = e^Z$  as  $\text{LogN}(\mu, \sigma)$ .

**Effective diffusivity:** The effective diffusivity,  $D_{eff}$ , plays a key role in the EM degradation of Cu DD wires, as discussed in Section 2.4, and affects the physics of void nucleation and growth, as indicated in (2.27) and (2.29), respectively. Therefore, we investigate the statistics of  $D_{eff}$ .

As indicated in Section 2.4, the primary diffusion mechanism in modern Cu DD interconnects is grain boundary (*GB*) diffusion. Due to this, the parameter  $D_0$  in (2.30) is determined by this mechanism. Using (2.18), we have

$$\begin{aligned} D_0 &= D_{0GB} \left( \frac{\delta_{GB}}{d} \right) \\ \text{or } \log D_0 &= \log(D_{0GB} \delta_{GB}) - \log d \end{aligned} \quad (3.1)$$

where  $D_{0GB}$  is a temperature independent constant. This shows that  $D_0$  is a random variable that depends on the effective grain size,  $d$ , which follows a lognormal distribution [40], i.e.,  $d = \text{LogN}(\mu_d, \sigma_d)$ , where  $\mu_d$  and  $\sigma_d$  represent the mean and standard deviation of the underlying

Gaussian,  $\log d$ . Specifically,  $D_0 = \text{LogN}(\mu_{D_0}, \sigma_{D_0})$ , where the mean,  $\mu_{D_0} = \log(D_{0GB}\delta_{GB}) - \mu_d$  and the standard deviation,  $\sigma_{D_0} = \sigma_d$ .

Therefore, to model the variation in  $D_{eff}$ , we use the above, and the fact that  $E_a$  for a wire follows a Gaussian distribution. From (2.30), it is obvious that  $D_{eff}$  is the product of two lognormals, one attributable to  $D_0$  (via  $d$ ) and the other attributable to  $E_a$ , and such a product results in a lognormal distribution. If  $E_a = N(\mu_{E_a}, \sigma_{E_a})$ , then  $D_{eff} = \text{LogN}(\mu_{D_{eff}}, \sigma_{D_{eff}})$ , where

$$\begin{aligned}\mu_{D_{eff}} &= \log(D_{0GB}\delta_{GB}) - \mu_d - \frac{\mu_{E_a}}{k_B T} \\ \sigma_{D_{eff}}^2 &= \sigma_d^2 + \left(\frac{\sigma_{E_a}}{k_B T}\right)^2\end{aligned}\quad (3.2)$$

The diffusion pathways during nucleation and growth may be different [27]. We refer to the effective diffusivity for the nucleation and growth phases as  $D_{eff,n}$  and  $D_{eff,g}$ , respectively, and next, we consider the impact of each of these individually.

**Nucleation:** The expression for nucleation time  $t_n$  was provided in (2.27). From this, it is clear that  $t_n = \text{LogN}(\mu_{t_n}, \sigma_{t_n})$ , where

$$\begin{aligned}\mu_{t_n} &= \log(K_{t_n}) - \mu_{D_{eff,n}} \\ \sigma_{t_n} &= \sigma_{D_{eff,n}}\end{aligned}\quad (3.3)$$

the above result relies on the observation that the distribution of a reciprocal of a lognormal  $\text{LogN}(\mu, \sigma)$  is another lognormal characterized as  $\text{LogN}(-\mu, \sigma)$ .

**Growth:** During void growth, the length of a void evolves with time according to (2.29). Grouping together all deterministic parameters in this equation, if a void nucleates, then from (2.29), its length at given observation time,  $t_o$ , has the form

$$L_{void}(t_o) = c_1 D_{eff,g} - c_2 t_n D_{eff,g} \quad (3.4)$$

where  $c_1 = (eZ_{eff}^* \rho_j t_o) / k_B T$  and  $c_2 = c_1 / t_o$ . The first term,  $c_1 D_{eff,g}$ , is lognormal, since  $c_1$  is a deterministic constant and  $D_{eff,g}$  is lognormal, and the product of a lognormal random variable with a scalar results in another lognormal random variable; the second term,  $c_2 t_n D_{eff,g}$  is a scaled product of lognormals, which is also a lognormal.

Therefore,  $L_{void}(t_o)$  is a difference of two correlated lognormals,  $c_1 D_{eff,g}$  and  $c_2 t_n D_{eff,g}$ . The difference of two lognormal random variables is approximated by a lognormal using a moment matching approach, similar to the widely-used Wilkinson approximation [47], which has been used to approximate the sum of two correlated lognormal random variables. The correlation between the random variables  $c_1 D_{eff,g}$  and  $c_2 t_n D_{eff,g}$  is required for evaluating the statistics, and the correlation coefficient  $r$  can be evaluated as

$$r = \frac{c_1 c_2 \frac{\text{mean}(t_n) \text{variance}(D_{eff,g})}{\sqrt{\text{variance}(c_1 D_{eff,g}) \text{variance}(c_2 D_{eff,g} t_n)}}}{\sqrt{\text{variance}(c_1 D_{eff,g}) \text{variance}(c_2 D_{eff,g} t_n)}}$$

where the mean() and variance() for the corresponding lognormal variables. From (3.2) and (3.3), which provide the mean and variance of the underlying Gaussians, it is easy to compute these quantities. Specifically, if  $\mu_X, \sigma_X$  ( $\mu_Y, \sigma_Y$ ) are the mean and standard deviation of the underlying normal distribution for  $c_1 D_{eff,g}$  ( $c_2 t_n D_{eff,g}$ ) then we have

$$\begin{aligned}\mu_X &= \log c_1 + \mu_{D_{eff,n}} & \sigma_X &= \sigma_{D_{eff,n}} \\ \mu_Y &= \log c_2 + \mu_{D_{eff,g}} + \mu_{t_n} & \sigma_Y &= \sqrt{\sigma_{D_{eff,g}}^2 + \sigma_{t_n}^2}\end{aligned}$$

In order to find the analytical expression for the distribution of void length,  $L_{void}(t_o) = \text{LogN}(\mu_{L_{void}(t_o)}, \sigma_{L_{void}(t_o)})$ , we can use the above set of equations to compute the parameters of the distribution by applying the moment matching approach used in Wilkinson approximation. This will lead to the following set of equations

$$\begin{aligned}u_1 &= e^{(\mu_X + \sigma_X^2/2)} - e^{(\mu_Y + \sigma_Y^2/2)} \\ u_2 &= e^{(2\mu_X + 2\sigma_X^2)} + e^{(2\mu_Y + 2\sigma_Y^2)} - 2e^{\left(\mu_X + \mu_Y + \frac{(\sigma_X^2 + \sigma_Y^2 + 2r\sigma_X\sigma_Y)}{2}\right)} \\ \mu_{L_{void}(t_o)} &= 2 \log(u_1) - \log(u_2)/2 \\ \sigma_{L_{void}(t_o)}^2 &= \log(u_2) - 2 \log(u_1)\end{aligned}$$

### 3.2.3 Statistics of the EM-induced resistance change

We will now use the void length distribution to evaluate the distribution of resistance change due to EM-induced growth of a spanning void. For the case of the spanning void, the change in resistance,  $\Delta R$ , is given as [33]

$$\frac{\Delta R}{R_0} = \left( \frac{\rho_{Ta}}{\rho_{Cu}} \frac{A_{Cu}}{A_{Ta}} - 1 \right) \frac{L_{void}(t_o)}{L_{wire}} \quad (3.5)$$

Here,  $\rho_{Cu}$  and  $\rho_{Ta}$  are, respectively, the resistivities of copper and tantalum,  $R_0 = \rho_{Cu} L_{wire} / A_{Cu}$  is the resistance of the interconnect wire segment, which is assumed to have length  $L_{wire}$  and cross-sectional area  $A_{Cu}$ , and  $A_{Ta}$  is the cumulative cross-sectional area of the tantalum barrier. Recall that the void length at time  $t_o$ ,  $L_{void}(t_o)$ , was shown in Section 3.2.2 to be lognormally distributed after nucleation. If we introduce a new symbol,  $k_R$ , defined as

$$k_R = \left( \frac{\rho_{Ta}}{\rho_{Cu}} \frac{A_{Cu}}{A_{Ta}} - 1 \right) \frac{R_0}{L_{wire}}, \quad (3.6)$$

we can rewrite (3.5) as

$$\Delta R = k_R L_{void}(t_o) \quad (3.7)$$

Since  $k_R$  is constant in (3.7), it can be seen that for a spanning void, for both the via-above and via-below cases,  $\Delta R$  is lognormal, since it is the product of a lognormal random variable with

a scalar. The resistance change distribution can then be expressed as  $\Delta R = \text{LogN}(\mu_{\Delta R}, \sigma_{\Delta R})$ , where  $\mu_{\Delta R}$  and  $\sigma_{\Delta R}$  are the mean and standard deviation of the underlying Gaussian, given by

$$\begin{aligned}\mu_{\Delta R} &= \mu_{L_{\text{void}}(t_o)} + \log k_R \\ \sigma_{\Delta R} &= \sigma_{L_{\text{void}}(t_o)}\end{aligned}\tag{3.8}$$

We summarize the conditions that must be satisfied to achieve a resistance change of  $\Delta R$  at an observation time  $t_o$ . First, a void must nucleate, and then this nucleated void must grow to the point where the wire resistance increases by  $\Delta R$ . Using these notions, we can now determine the probability that a given wire will have a resistance change  $\Delta R$  as

$$\Pr(\Delta R) = \begin{cases} \Pr(\Delta R \mid \text{nuc}) \cdot \Pr(\text{nuc}) & \text{if } \Delta R > 0 \\ 1 - \Pr(\text{nuc}) & \text{if } \Delta R = 0 \end{cases}\tag{3.9}$$

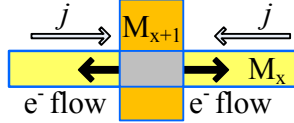
The first case corresponds to a nonzero resistance change, i.e., the product of  $\Pr(\Delta R \mid \text{nuc})$ , the probability of a resistance change given that nucleation has occurred, and the probability of nucleation,  $\Pr(\text{nuc})$ . The probability distribution for  $\Delta R$  for a nucleated void is given by  $\text{LogN}(\mu_{\Delta R}, \sigma_{\Delta R})$  as derived above, with the mean and standard deviation given by (3.8). The nucleation probability is given by  $\text{LogN}(\mu_{t_n}, \sigma_{t_n})$  in (3.3), and  $\Pr(\text{nuc})$  corresponds to the probability that the nucleation time,  $t_n$ , is less than the observation time,  $t_o$ , i.e., the cumulative distribution function (CDF) of  $t_n$ , evaluated at time  $t_o$ . The second case corresponds to the scenario where the void does not nucleate, with a probability of  $1 - \Pr(\text{nuc})$ .

### 3.2.4 Incorporating the effect of current divergence

The conventional approach to estimating EM failure is based on a current density-based model. Under this model, for two wires of equal length, the one with the larger current density should have a shorter mean time to failure. However, the work in [48] demonstrated experimentally that this is not always the case, by showing test circuit where one wire has twice the current density as another, but experiences consistently later failures. This is consistent with other reported work where the *current divergence* effect comes into play: for example, [49] shows fabricated test structures where the failure rates on a wire segment depends not only on the current density on the segment, but also on those on adjacent segments that share via(s) with this segment. The flux-divergence is a simple way to account for atomic blocking boundaries and does not account for back-stress effects, and this results in pessimistic predictions for nucleation time.

We compute the effective current density by considering the magnitude and directions of currents in neighboring wires. The effective current density for a wire is computed, pessimistically, in terms of the flux-divergence criterion, similar to the work in [48]. This is illustrated in

Figure 3.1, which shows two wires on metal layers  $M_x$  and  $M_x + 1$  connected by a via. A via in a Cu DD interconnect structure acts as a blocking layer so that metal atoms are not permitted to migrate through it. Therefore, any flux that would have gone to the via is transmitted to a neighboring wire.



**Figure 3.1:** A via-tree structure where the effective current density is more than the density of current flowing through the wire.

In this example, the current on both segments of the wire on layer  $M_x$  flows towards the via, i.e., the electron flow direction is away from the via for both segments. Assuming equal current densities  $j$  on each segment, this implies that there is an effective divergence, which can eventually lead to void nucleation and growth, equivalent to a current density of  $2j$  on both wires. In other words, as compared to the case where the left-hand segment is missing and the right-hand segment has the same current density of  $j$ , the expected rate of atomic transfer is doubled at this node. Using the via node vector notion [48], an effective current density of  $2j$  is used for this wire instead of the actual current density of  $j$ .

### 3.2.5 Mortal wire prediction under probabilistic EM

The Blech criterion, outlined in Section 3.2, is predicated on the achievement of a steady state between the electron wind and back-stress forces, so that the stress gradient settles to a linear trend in space. The achievement of steady state requires significant mass transfer from the cathode to anode to balance the forward EM flux, and immortality cannot be guaranteed unless this steady state is reached soon. The observation that a finite time, which may be comparable to circuit lifetime, is elapsed before the achievement of steady state, can be backed up by experimental data, based on extrapolating experimental EM and back-stress results from [50], which observe the time elapsed for achievement of back-stress, in Cu wires of multiple wire lengths.

According to [1], the time taken to reach steady state can be written as

$$t_{ss} = \frac{L^2}{4 \kappa} \quad (3.10)$$

where  $\kappa = \frac{D_{eff} B \Omega}{k_B T}$ , as in Equation (2.19). For wires where the steady state may not be achieved, we propose an alternate void-nucleation-based mortality criterion, considering three cases:



**Case I:** A wire can be EM-mortal if it does not satisfy the Blech criterion ( $jL < (jL)_{crit}$ ). For these mortal wires, we have

$$jL > (jL)_{crit} \quad (3.11)$$

**Case II:** A wire can be EM-mortal if a void can nucleate before steady-state is achieved, i.e.,  $t_n < t_{ss} = L^2/4\kappa$ . Since  $\kappa = (D_{eff} B \Omega / k_B T)$ , from Equations (2.27) and (2.28),

$$\frac{\pi}{4} \left( \frac{\sigma_c^2 \Omega k_B T}{(eZ_{eff}^* \rho j)^2 B D_{eff}} \right) < \frac{L^2}{4} \frac{k_B T}{D_{eff} B \Omega} \quad (3.12)$$

$$\text{i.e., } jL > \frac{\sqrt{\pi}}{2} (jL)_{crit} \quad (3.13)$$

where  $(jL)_{crit}$  is the conventional critical  $jL$  value from the Blech criterion, given by Equation (2.14). Note that in the first inequality, both the left and right hand sides are statistical quantities. However, both depend on  $D_{eff}$ , which cancels out, resulting in a deterministic criterion.

**Case III:** Let the earliest reasonable void nucleation time of a wire, taken to be the  $\mu - 3\sigma$  point of the underlying Gaussian of the nucleation time,  $t_n$ , be denoted as  $t_n^{\mu-3\sigma}$ . A wire is effectively EM-immortal if this earliest nucleation time is beyond the projected lifetime,  $t_{life}$ , of the circuit. In other words, it is EM-mortal if

$$t_n^{\mu-3\sigma} < t_{life} \quad (3.14)$$

Using (3.3), this inequality can be written as

$$\begin{aligned} t_n^{\mu-3\sigma} &= e^{\mu t_n - 3\sigma t_n} = e^{\log K_{t_n} - \mu D_{eff,n} - 3\sigma D_{eff,n}} < t_{life} \\ \text{i.e., } K_{t_n} &< t_{life} e^{\mu D_{eff,n} + 3\sigma D_{eff,n}} \end{aligned} \quad (3.15)$$

Substituting  $K_{t_n}$  from Equation (2.28) and rearranging a few terms, this translates to the following mortality criterion for a wire carrying current  $j$ :

$$j > \frac{\sigma_c}{eZ_{eff}^* \rho} \sqrt{\frac{\pi \Omega k_B T}{4 B t_o e^{\mu D_{eff,n} + 3\sigma D_{eff,n}}}} \quad (3.16)$$

For a wire to be EM-mortal, the criteria under all three cases must be satisfied. Since  $\sqrt{\pi}/2 \approx 0.89 < 1$ , the criterion for Case I is automatically satisfied by Case II. *Therefore, the EM-mortality criterion is given by (3.13) and (3.16).* Further, for both inequalities (3.13) and (3.16), all parameters on the right-hand side of the inequality are fundamental parameters of the technology; in particular, from (3.2), the statistics of  $D_{eff,n}$  can be seen to be based on the underlying process, and can be cheaply precomputed for a technology, without the need for any

Monte Carlo simulations. We apply the mortality criteria, (3.13) and (3.16) to filter out wires that are safe with respect to EM, during the product lifetime. For the mortal wires, we perform Monte Carlo circuit simulations (described in the next section) to analyze the impact on the power grid.

Our mortality criteria are simple to apply, and pessimistically filter out mortal wires for further EM analysis. There is one drawback of our mortality criteria, which is in the definition of arrival of steady state, taken *approximately* as  $\frac{L^2}{4\kappa}$ . In Chapter 5, we fix this by efficiently and accurately calculating the stress dynamics without making any approximations on the arrival of steady state.

### 3.3 Power grid simulation framework

We use our probabilistic resistance model to perform Monte Carlo analysis of power grids in the presence of probabilistic resistance variations. Our probability distribution function (PDF) for the resistance change, derived in Section 3.2.3 builds a simple circuit-level abstraction for complex physical phenomena, facilitating simplified analysis at the circuit level by considering  $\Delta R$  as a random variable. However, given that EM is (and should be) a relatively unlikely event, it is essential for our Monte Carlo analysis to be biased appropriately: a truly random set of samples would probably see no resistance change in most (and possibly, for a small set of samples, no) wires. Most importantly, such an approach would see a large number of samples go to waste as they provide little meaningful information.

To overcome this, we use the notion of importance sampling, which biases the distribution, but “unbiases” it as it interprets the results of sampling. Importance sampling is a Monte Carlo method that computes the expected value of a function  $f(x)$  of a random variable  $x$ , which is defined over a set of values  $\chi$ , and specified in terms of a distribution  $p(x)$ . This method is particularly useful when  $p(x)$  is skewed or unevenly distributed, i.e., some values of  $x$  have a low probability of occurrence and are not sampled frequently enough, causing sampling errors. Importance sampling resolves this by sampling according to a function  $q(x)$  that is uniformly distributed over the range of  $x$ , and then correcting the error due to sampling from this different distribution by adding appropriate weights to  $f(x)$ . For example, the expectation of  $f(x)$  under the distribution  $p(x)$ , denoted  $E_p[f(x)]$ , is computed as:

$$\begin{aligned} E_p[f(x)] &= \int_{\chi} f(x)p(x)dx = \int_{\chi} f(x)p(x).q(x)/q(x)dx \\ &= \int_{\chi} w(x)q(x)dx = E_q[w(x)] \end{aligned}$$

where  $w(x) = f(x)p(x)/q(x)$  and  $E_p[f(x)]$  is the expectation of  $f(x)$  under the new probability

distribution  $q(x)$ .

We use a sampling distribution  $q(x)$ , which is a uniform distribution that stretches from 0 to the tail of the lognormal distribution of  $\Delta R$ : the values of this lognormal range from  $\Delta R = 0$  to the  $(\mu + 3\sigma)$  point of the underlying Gaussian,  $\log(\Delta R)$ , where  $\mu$  and  $\sigma$  represent, respectively, the mean and the standard deviation of the underlying Gaussian. If  $K$  is the span of this distribution from  $\Delta R = 0$  to the  $(\mu + 3\sigma)$  point of the underlying Gaussian, then every point within the span has a uniform probability of  $1/K$  under  $q(x)$ . The method samples points on this distribution, feeds them into a power grid simulator based on DC modified nodal analysis, and determines the voltage distribution at each node. The voltages are then translated back to the original distribution by scaling them to the original lognormal using the  $w(x)$  factor. The pseudocode for our framework is shown in Algorithm 1

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**Algorithm 1** Power grid Monte Carlo simulation

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- 1: Solve power grid to obtain nominal  $j$  for each wire
  - 2: Calculate effective current density (Section 3.2.4)
  - 3: Filter immortal wires that are EM-safe (Section 3.2.5)
  - 4: **for** each mortal wire **do**
  - 5:     Use the resistance evolution model to obtain  
           lognormal PDFs of wire resistance (Section 3.2.3)
  - 6: **end for**
  - 7: **for** each Monte Carlo iteration **do**
  - 8:     **for** each mortal wire **do**
  - 9:         Sample the wire resistance using IS (Section 3.3)
  - 10:     **end for**
  - 11:     Build a circuit sample for the power grid using the  
           above set of wire resistances
  - 12:     Solve the sample power grid and tabulate the IR drop
  - 13: **end for**
  - 14: Report statistics (mean, standard deviation)
-

## 3.4 Results

### 3.4.1 Failures in a single wire

To calibrate the correctness of our probabilistic model, we first work under assumptions similar to [27], which computes  $t_n$ , the time elapsed before a void nucleates in a wire, and  $t_g$ , the time elapsed from nucleation up to the instant at which length of the void,  $L_{void}$  becomes equal to  $L_{via}$ , i.e., allowing the void to grow until it spans across the length of the via. Our predicted values are then compared against the published Finite Element Analysis (FEA) simulations in [27]. For evaluating the corresponding values of time elapsed for void nucleation and growth, we use the probabilistic framework derived in Section 3.2 under accelerated aging conditions for temperature and current stress.

#### Calibration of correctness under accelerated aging

The material parameters for accelerated aging are set to ensure a fair comparison, drawing parameter values from [27] where available. Table 3.1 list the EM parameters along with their description, values, and the corresponding reference from where the values are imported. Some parameters that were unavailable were extracted from the literature. Specifically,  $B = 1\text{GPa}$  was used from [51].

The standard deviation for the normally distributed  $E_a$  is obtained from [41], by using the  $3\sigma$  value in  $E_a$ , which is specified as  $0.11\text{eV}$ . Here  $\sigma$  denotes the standard deviation for  $E_a$ , and is obtained as  $0.037\text{eV}$ . For our calibration simulations, we used the value for effective diffusivity and activation energy corresponding to the capping surface diffusion to align with the simulation setup in [27], which uses bamboo-like grains where the capping surface diffusion is the dominant EM mechanism, as discussed briefly in Section 2.4.

Name	Description	Value
$\Omega$	Atomic volume	$1.18 \times 10^{-29} \text{m}^3$ [6]
$j$	Current density	$1.33 \times 10^{10} \text{A/m}^2$ [27]
$\rho$	Cu resistivity	$2.5 \times 10^{-8} \Omega\text{m}$ [27]
$T$	Accelerated aging temperature	$295^\circ\text{C}$ [27]
$B$	Effective bulk modulus	$1\text{GPa}$ [51]
$\sigma_c$	Critical stress for void nucleation	$41\text{MPa}$ [36]
$Z_{eff}^*$	Atomic charge number	5 [41]
$D_o$	Diffusivity constant	$6.7 \times 10^{-13} \text{m}^2/\text{s}$ [41]
$E_a$	Effective surface activation energy	$0.45 \pm 0.11 \text{eV}$ [41]

**Table 3.1:** EM parameters used for the single wire case.

Table 3.2 lists the expected value,  $\mu$ , of the lognormal and standard deviation,  $\sigma$ , for the underlying Gaussian of the lognormal for the failure parameters,  $t_n$  and  $t_g$ , obtained by our model, against the corresponding values obtained from FEA, mentioned in [27]. The values show a good level of consistency, despite some differences in the underlying assumptions. The discrepancies are attributed to factors such as the unavailability of some parameters in [27], and differences in the setup between the fully three-dimensional numerical simulations in the FEA approach against our analytical approach. Clearly, our method is much faster than the FEA approach since it merely involves the evaluation of an analytical expression. The three-dimensional models used by the numerical simulations in the FEA approach give an accurate estimate of the EM dynamics. However, due to the large simulation runtime, even for a single wire, the usage of such models for the statistical analysis of a multimillion-wire power grid system is unrealistic. Our work presents an approach that enables this level of scalability.

$\mu, \sigma$	Nucleation		Growth	
	$\mu_{t_n}$	$\sigma_{t_n}$	$\mu_{t_g}$	$\sigma_{t_g}$
From [27]	8.5h	0.4h	8.0h	0.7h
Analytical	7.2h	0.7h	8.4h	0.8h

**Table 3.2:** Void nucleation time ( $t_n$ ) and growth time ( $t_g$ ) comparison: Analytical method vs. FEA values.

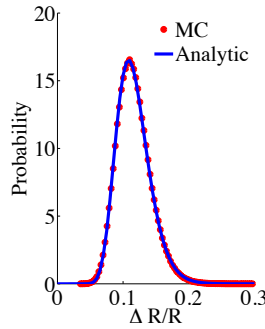
Under the assumptions in [27], failure is defined as the time when  $L_{void} = L_{via}$ , and the time-to-failure (TTF) is the sum of the nucleation time,  $t_n$ , and the growth time,  $t_g$ . We apply the Wilkinson approximation [47] to obtain TTF as the sum of lognormal distributions of  $t_n$  and  $t_g$ . The TTF values for the 0.3%ile, 50%ile, and 99.7%ile points under accelerated aging are 12.7h, 15.6h, and 19.1h, respectively. These numbers indicate that every wire has a nonzero probability of failure, regardless of the value of its  $jL$  product that is traditionally used to screen out wires that are immortal under the Blech criterion. Indeed, wires that satisfy the Blech criterion will fail, as observed experimentally in [36, 37]. However, below a lifetime of 12.7h, there is very low probability that a specific wire will fail in any manufactured part, and wires that fall below this threshold can effectively be considered immortal.

### Single-wire simulation at chip operating conditions

Now that we have compared our statistics with published work under accelerated aging conditions, we revert to performing our remaining evaluations under normal operating conditions. We use a similar setup as described in Section 3.4.1, but we perform this analysis at room

temperature, using a current density value of  $1 \times 10^{10} \text{A/m}^2$ . As expected, the reduction in temperature reduces the rate of EM degradation, and the TTF is now of the order of several years, as against accelerated aging, where it is of the order of several hours. We also perform MC simulations at these conditions to validate our approach using  $10^6$  samples on a normal distribution of activation energy.

We evaluate the resistance change ratio,  $\Delta R/R$ , of a wire according to our probabilistic formulation in (3.9), for the observation time,  $t_o = 12$  years. Figure 3.2 shows the comparison for the PDF of  $\Delta R/R$  as predicted by our formulation against a plot for the same PDF obtained from MC simulations. This figure demonstrates a close match between our analytical approximation with MC simulation



**Figure 3.2:** PDF of  $\Delta R/R$  for a wire under normal operating conditions.

### 3.4.2 Power grid simulation

Moving beyond a single wire, we now focus on analyzing the impact of EM on a set of power grid benchmark circuits described in [2]. Table 3.3 lists the power grid benchmarks that were evaluated for our EM analysis. For each power grid, the table lists the name, total number of wires, number of metal layers occupied, and the percentage nominal IR-drop of the power grid, defined as the IR-drop value of the node with the largest value of IR-drop among all the nodes expressed as a percentage of supply voltage, evaluated at time 0, i.e., prior to EM degradation.

Name	Total # wires	# Metal layers	% Nominal IR-drop
PG1	30027	2	8.2
PG2	208325	5	13.4
PG3	1401572	5	10.1
PG4	1560645	5	0.2
PG5	1076848	6	2.3
PG6	1649002	3	6.3
new1	2352355	6	12.2
new2	1422830	6	12.2

**Table 3.3:** Power grid benchmarks from [2] that are evaluated in the thesis.

For power grids PG1 and PG2, it was observed that the nominal IR-drop for the original benchmarks, as described in [2], was abnormally high (>20% of the supply voltage). Similar to [29], we scale the original values of the current loads for these benchmarks such that the worst-case IR-drop at nominal conditions is below 15% of the supply voltage.

For these benchmarks, we analyze the interconnects for EM risk in the power grid and simulate the distribution of the IR-drop by solving the power grid to obtain the node voltage at every node for a given circuit lifetime,  $t_{life}$ . We assume constant current sources drawing current from the power grid, which consists of only resistive elements.

For the accelerated aging simulations described in Section 3.4.1, the capping surface diffusion was considered as the primary EM diffusion mechanism to align with the FEA simulations from [27]. However, for power grid simulations, we choose the process parameters corresponding to the grain boundary (*GB*) diffusion mechanism, since diffusion through the grain boundaries is indicated as the primary EM diffusion mechanism for advanced technology Cu DD interconnects, as indicated in [4], and briefly discussed in Section 2.4. Table 3.4 lists the values of the process parameters used in our simulations. We remind the reader again that for the lognormals, we provide mean and variance values that refer to the underlying Gaussians. Therefore, a negative mean value for the Gaussian is permissible since it translates to a positive mean for the lognormal.

Name	Description	Value
$T$	Chip operating temperature	105°C [52]
$B$	Effective bulk modulus	28GPa [31]
$\sigma_c$	Critical stress for void nucleation	41MPa [36]
$Z_{eff}^*$	Atomic charge number ( $GB$ )	1 [31]
$D_o$	Diffusivity constant ( $GB$ )	$1.3 \times 10^{-9} \text{m}^2/\text{s}$ [31]
$\delta_{GB}$	Effective $GB$ width	0.5nm [53]
$\mu_d$	Mean of underlying Gaussian of $d$	-16.2m [40]
$\sigma_d$	Standard deviation of underlying Gaussian of $d$	0.38m [40]
$E_a$	Effective $GB$ activation energy	$0.8 \pm 0.11 \text{eV}$ [31, 41]

**Table 3.4:** EM parameters used in power grid simulation.

We perform MC circuit simulation using samples from the EM-induced resistance increase,  $\Delta R$ , for every wire in the power grid using a statistical importance sampling approach, described in Section 3.3. We realize our implementation using C++ and MATLAB. For a confidence of  $P_{\text{target}}$  that the worst-case IR-drop predicted from our MC simulation does not cross the 99.7%ile value predicted by our method, it can be shown that the number of simulations,  $N_{MC}$ , can be evaluated as  $N_{MC} = \frac{\log(1-P_{\text{target}})}{\log(0.997)}$ . We choose  $P_{\text{target}} = 95\%$ , which provides  $N_{MC} = 997$ , and for convenience, we round this upwards to 1000 simulations.

In our implementation, for convenience, we have used the matrix solver from MATLAB. However, to demonstrate that it is realistic to run a Monte Carlo simulation with 1000 simulations on these power grids, we use the runtime per iteration from [3], listed in Table 3.5, to estimate realistic runtimes if a specialized power grid simulator were to be used instead. This table indicates that the MC-based evaluation is computationally reasonable.

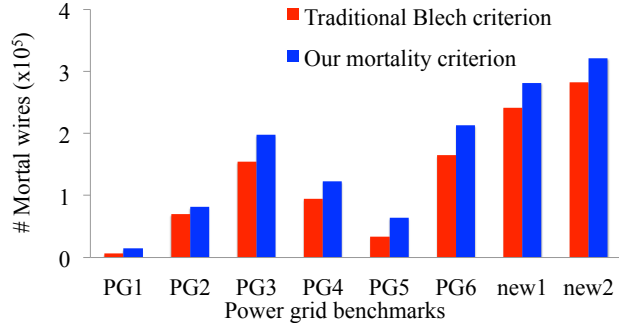
	Single iteration runtime [3]	Peak Memory in MB [3]	Expected runtime for 1000 MC simulations
PG1	0.2s	4	4min
PG2	1.4s	72	24min
PG3	8.3s	172	139min
PG4	19.4s	606	325min
PG5	9.4s	296	156min
PG6	15.4s	406	257min
new1	14.6s	349	243min
new2	16.4s	495	273min

**Table 3.5:** Expected runtime values for MC power grid evaluation based on single iteration runtimes from [3].



### 3.4.3 Mortal wire prediction

We now evaluate our new mortality criterion from Section 3.2.5. We identify the number of mortal wires predicted from our proposed mortality criterion with those from the traditional deterministic Blech criterion, and list the number of such wires for each benchmark in Figure 3.3.



**Figure 3.3:** Mortal wire comparison: Our criterion vs. traditional Blech criterion.

It can be seen that our implementation indicates that a larger number of wires must be considered mortal under our probabilistic formulation. As derived in Section 3.2.5, the mortal wires identified by our approach is a superset of those that are mortal under the traditional criterion, and therefore the number of mortal wires is larger than the traditional number.

### 3.4.4 EM-induced IR-drop degradation

Next, for the power grid benchmarks, we discuss the statistics of performance degradation from part to part. This variation is a result of EM-induced increases in wire resistances due to probabilistic variations in  $E_a$  and  $d$ , which leads to statistical shifts in the IR-drop, and is computed through an MC simulation on each power grid.

For each MC sample, we tabulate the IR-drop value of power grid, defined previously as the IR-drop value of the node which has the largest IR-drop, since it is this node which will decide the overall performance of the circuit. Based on this distribution of IR-drop values, we define the maximum IR-drop value,  $V_{\max}$ , as the 99.7%ile point of this distribution, and the spread,  $\Delta V$ , in the IR-drop values, as the difference between the 99.7%ile and 0.3%ile values. The maximum IR-drop is normalized as a percentage of the supply voltage,  $V_{dd}$ , and the spread as a function of the maximum IR-drop.

### Impact of $E_a$ and $d$ on IR-drop

In order to quantify the impact on IR-drop due to variations in activation energy,  $E_a$ , and grain size,  $d$ , we perform three sets of circuit simulations, for a specific lifetime  $t_{life} = 10$  years. In the first set, we do not consider any variation in both activation energy,  $E_a$ , and grain size,  $d$ , and we choose fixed values for  $E_a$  and  $d$ , which correspond to the mean values of their corresponding distributions.

For the second set of simulations, we consider variations in the activation energy and a constant grain size, and in the third set, we assume variation in both  $E_a$  and  $d$ . Table 3.6 shows the normalized maximum IR-drop value and the normalized spread, as defined previously, for every benchmark for each of the three sets of simulations.

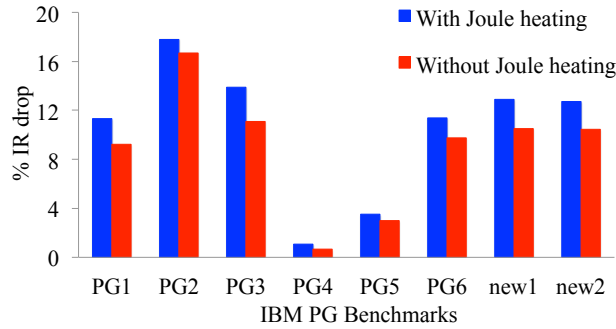
	No variation	$E_a$ variation		$E_a, d$ variation	
	$\frac{V_{max}}{V_{dd}}$	$\frac{V_{max}}{V_{dd}}$	$\frac{\Delta V}{V_{max}}$	$\frac{V_{max}}{V_{dd}}$	$\frac{\Delta V}{V_{max}}$
PG1	9.1%	10.5%	18.1%	11.1%	22.3%
PG2	15.8%	17.3%	5.9%	17.8%	9.3%
PG3	12.3%	12.8%	0.2%	13.9%	0.3%
PG4	0.7%	0.9%	2.2%	1.1%	3.2%
PG5	3.1%	3.4%	20.2%	3.7%	24.7%
PG6	8.9%	10.8%	9.1%	11.5%	6.4%
new1	12.7%	12.8%	0.3%	12.9%	0.4%
new2	12.4%	12.5%	0.2%	12.7%	0.3%

**Table 3.6:** The impact of  $E_a$  and  $d$  variation on the normalized 99.7%ile value and normalized spread of IR drop.

For the first set, clearly, the spread is zero since no variation is assumed. For the second and third set, the normalized maximum IR-drop increases and there is a clear spread in the IR-drop. The spread due to variation in both  $E_a$  and  $d$  variation, in the third simulation set, is observed to be marginally more than the spread due to variation in only  $E_a$ , in the second set. This indicates that the variation in  $E_a$  has a relatively larger impact on the overall variation in IR-drop. This can be attributed to the actual values chosen for mean and standard deviation of the process parameters which have been extracted from literature. Besides showing the relative contributions of process parameter variations on the IR-drop of power grids, we also want to emphasize the fact that, under statistical variation of process parameters, the IR-drop is not a fixed value but follows a distribution.

### Impact of temperature variation due to Joule heating

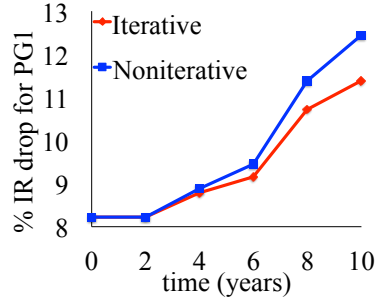
In order to quantify the impact of temperature rise due to Joule heating we repeat the third set in the previous circuit simulation, but this time we artificially force temperature rise due to Joule heating,  $\Delta T_J$ , in (2.31) to zero in our simulation. Figure 3.4 shows the normalized maximum IR-drop for the eight benchmarks, and demonstrates that the maximum IR-drop values for each benchmark is lower when Joule heating is not incorporated. The percentage error in the IR-drop, relative to its correct value after considering  $\Delta T_J$ , varies from 6% (for PG2) to 40% (for PG4). These variations across benchmarks can be attributed to multiple factors that vary between the power grids, such as the RMS current and the ILD thickness, which depends on the metal layers used.



**Figure 3.4:** Effect of Joule heating on IR-drop.

### Impact of current redistribution

The flow of current in the power grid drives EM, which induces probabilistic wire resistance changes. These changes, in turn, affect the distribution of current through the wires, thereby impacting further EM-induced degradation. In order to capture the evolution of IR-drop, our MC circuit simulation are performed using an iterative approach where the wire resistance and the current density value are updated after incremental steps leading to the circuit lifetime. For the power grid benchmarks, when we compare this iterative approach with a noniterative method, where the currents are not updated after  $t = 0$ , we observe that the noniterative approach predicts a larger IR-drop compared to the iterative approach for all benchmarks. Figure 3.5 illustrates the normalized maximum IR-drop for a representative benchmark, PG1, as a function of time.

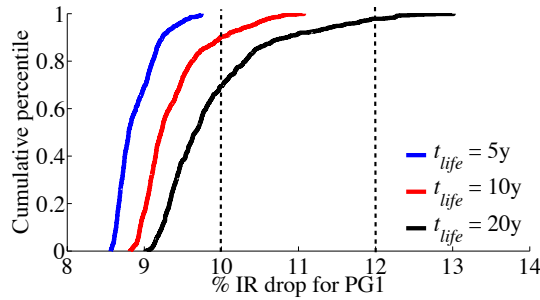


**Figure 3.5:** IR-drop evolution of PG1 (iterative vs. noniterative).

The lower IR-drop values in the iterative approach can be attributed to the current redistribution in the redundant paths of the power grid. This results in lower current flow through the EM-affected wires, thereby attenuating further EM-induced resistance degradation. In contrast, for the noniterative case, the current stress for the EM-affected wires remains constant predicting a relatively larger damage than is really seen. For PG1 the error in the IR-drop at circuit lifetime,  $t_{life} = 10$  years, is observed to be 9% of the IR-drop value at that instant.

### Statistics of the worst-case IR-drop for the power grid

In order to study the evolution of variation of the IR-drop, we observe the CDF of the IR-drop corresponding to the node with the largest value, according to our definition of  $V_{max}$ , for power grid PG1. The data is generated for various values of the lifetime,  $t_{life}$ , using our iterative MC approach. Figure 3.6 shows the CDF of the IR-drop at  $t_{life} = 5, 10,$  and  $20$  years, corresponding to the typical product lifetime values for mobile, computing, and automotive applications.



**Figure 3.6:** CDF plots for IR-drop of PG1 for various circuit lifetimes,  $t_{life}$ .

For a given threshold value, e.g., 10% as indicated by a vertical line on the  $x$ -axis, the CDF

corresponding to  $t_{life} = 5$  years lies completely to the left of this threshold. This implies that for short lifetime applications (e.g., mobile), the power grid will remain functional since the IR-drop is below the threshold for all the samples. In contrast, the worst percentage resistance degradation in PG1 at  $t_{life} = 5$  years is 48%, which is above the typical 10–20% resistance increase criterion that is typically used by designers today. This demonstrates that the circuit lifetime, which corresponds to the time during which the IR-drop is satisfactory, can be longer than the lifetime of any of its component wires. In other words, the power grid is robust to some EM failures in individual wires.

The probability that the IR-drop is larger than 10% increases with lifetime since a larger fraction of the samples crosses the chosen threshold for larger values of  $t_{life}$ . For the CDF corresponding to  $t_{life} = 10$  years, 9% of the samples cross the threshold, resulting in functional failure, and this value increases to a value of 33% for  $t_{life} = 20$  years as more voids nucleate and grow over this longer period, thereby resulting in larger EM-induced IR-drop degradation. Thus, for long lifetime applications, a significant fraction of samples will be EM-affected if the IR-drop threshold is chosen as 10%. On the other hand, if the design specifications are changed so that the IR-drop threshold criterion is relaxed from 10% to 12%, there is a 98% likelihood that the power grid will remain functional up to 20 years for the modified threshold. We also observe the worst resistance increase corresponding to  $t_{life} = 10$  years and  $t_{life} = 20$  years to be 124% and 287% respectively. Thus, even though the EM-induced wire resistance change increases by  $2.3\times$  between  $t_{life} = 10$  years to  $t_{life} = 20$  years, the IR-drop threshold changes by only 2% in order to maintain a significantly large (98%) probability for correct circuit functioning. This reemphasizes the resiliency of the power grid to EM-induced wire resistance change.

Note that for a well-designed power grid the fraction of samples crossing the IR-drop threshold, thereby resulting in functional failure, should be a low value. Depending on the product lifetime this value can be of the order 1000ppm to 1ppm depending on the product lifetime [54]. However, the failure fraction is significantly larger than 1000ppm. This is due to the fact the power grid benchmarks are not completely optimized. However, the designer may encounter them during design iterations, and it is important to analyze them to inform the designer that the grid has EM problems. The designer can then reduce the failure rate, for example, by adjusting the current densities, by changing the wire widths, and such optimization would be informed by the analysis of the type proposed here.

## Chapter 4

# Delay variability due to resistance evolution under AC EM

This chapter describes the AC EM analysis, which considers near-complete and partial AC recovery due to bidirectional current flow and estimates circuit performances for various technology nodes. The chapter proposes a change in paradigm for AC EM analysis aimed at capturing the effect of EM on circuit performance parameters such as delay for standard circuit topologies. The thesis proposes the idea to move beyond simple MTTF metrics and incorporate the circuit impact of wire resistance changes arising from EM, which is observed to be probabilistic. Section 4.1 introduces the AC EM and describes features specific to AC EM in signal wires, Section 4.2 describes an EM model that incorporates probabilistic resistance evolution, the peculiarities of AC EM, and the impact of bidirectional currents in neighboring wires. Section 4.3 describes our Monte Carlo simulation framework and Section 4.4 presents our simulations that report the impact of EM on the performance of a standard circuit structure in advanced technology nodes.

### 4.1 Introduction

Electromigration (EM) is a significant problem in interconnects in nanometer-scale technologies. Due to the scaling of wire dimensions, current densities in successive technologies have increased [4] to the point that EM-induced void nucleation and growth may occur during product lifetimes, leading to significant performance shifts. In this work, we analyze such shifts caused by bidirectional (AC) EM in copper dual damascene (Cu DD) wires. We perform analyses on typical circuit topologies in on-chip signal and clock networks and link the physics of

AC EM in Cu DD wires to circuit-level outcomes, i.e., circuit performance metrics that are meaningful to a designer, such as delay.

Prior works on circuit-level EM primarily use Black’s equation [55] and consider EM as a catastrophic failure. These are often based on a mean time to failure (MTTF) criterion that assumes that a wire will fail due to EM when its resistance increase crosses a threshold limit. Typically, this limit is the same for all wires. However, the change in circuit performance characteristics in a wire depends on its context. For some wires, it is possible that the circuit performance can degrade beyond the target specification before this limit, and others may function correctly even beyond the limit. For example, wires on timing-critical paths can only tolerate very small changes in delay, while wires on noncritical paths can tolerate larger resistance changes. A related idea has recently been explored in DC-EM-related works [13,29] that directly study the impact of EM wire degradation on circuit performance parameter such as voltage (IR) drop. However, a circuit-performance-based AC EM analysis has not been proposed so far, and this is one contribution of our work.

We propose a paradigm for AC EM analysis aimed at capturing the effect of EM on circuit performance parameters, such as delay. We move beyond simple MTTF metrics and incorporate the circuit impact of wire resistance changes arising from EM void nucleation and growth [1], which is observed to be probabilistic [36,56]. We employ a probabilistic wire resistance evolution model for AC EM. Under probabilistic resistance evolution, voids nucleate and grow, causing parametric changes in wire resistance over time, resulting in a probabilistic impact on circuit performance that causes a spread in the lifetimes of manufactured parts.

Besides quantifying the impact of EM probabilistic behavior, we incorporate the special characteristics of AC EM arising as a result of the flow of bidirectional currents. Unlike DC EM, where the electron wind force responsible for EM occurs only in one direction, the electron wind is bidirectional in AC EM. The bidirectional current has been observed to cause near-complete [15] or partial recovery [20] with respect to EM as metal migration occurs in both directions. The question whether the EM recovery is near-complete [15] or partial [20] has been a topic of debate, and is something that should be given as an input to our simulation framework. To address the observation of multiple values of recovery factors observed in experimental works, we perform our EM circuit analysis using multiple recovery factors ranging from the smallest value of 0.7 [20], indicating partial recovery, to a value of 1 [15], indicating complete recovery with respect to EM.

We address recent experimental results on bidirectional currents, which show that void can be nucleated at both ends of a wire carrying an AC signal [57,58]. We also include the effect of temperature rise due to local wire Joule heating, using the model from [35]. In addition, our analysis considers EM flux divergence [59], which models the impact of current flowing in

neighboring wires on the EM atomic flux. Thus, we link the important facets of the mechanism of AC EM in Cu DD wires to circuit-level performance metrics.

We link our AC wire resistance evolution model and HSPICE-based circuit simulation to analyze parametric variations in circuit delay arising as a result of probabilistic resistance increase due to void nucleation and growth. We consider typical on-chip circuit structures at multiple technology nodes and observe that AC EM causes not only catastrophic functional failures, but also parametric delay variations over the chip lifetime, an effect that becomes more acute in scaled technologies.

## 4.2 Modeling AC EM

As an EM-induced void evolves in a Cu DD wire, its resistance shows a temporal change. This is because the absence of Cu metal in a void spanning through the cross section of the wire forces more current to flow through the resistive Ta barrier layer and causes an increase in the effective wire resistance, which is proportional to the size of the void [33]. This resistance increase due to EM-induced voids will first change the circuit performance parameters such as the delay and eventually cause functional failure, when the circuit performance degrades beyond a threshold margin.

As described in Section 2.5, we model the EM-induced void physics based on [1], which assumes that the void evolution occurs in two steps: void nucleation, where the void begins to form, and void growth, where the nucleated void, increases in size as more metal atoms migrate in the direction of electron flow. A key factor influencing void evolution is the effective activation energy [60],  $E_a$  for EM void nucleation and growth: this is experimentally observed to be normally distributed between metal lines [56, 60–62]. The resistance change under probabilistic void evolution must be modeled probabilistically.

We build our AC EM framework based on the probabilistic resistance evolution model for DC EM described in Chapter 3. Our starting point is the model for effective diffusivities for void nucleation and growth, as described in (2.30) in Section 2.6.

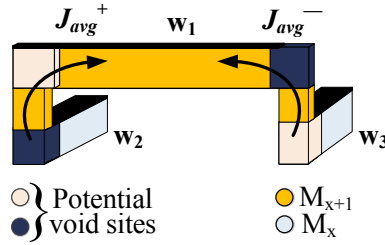
### 4.2.1 AC EM effects: Recovery and multiple void sites

For signal wires, the passage of AC current in opposite directions in a wire results in partial EM degradation and recovery. This is because the forward current flow in one direction changes the structural properties (grain boundary locations) of the wire [63], and the reverse current heals some of this restructuring. A recovery factor  $r$  models this [15, 20, 64] and determines an “effective current density” for the signal wire which corresponds to the equivalent DC current density for bidirectional signals. The expressions for DC EM are then used for AC EM modeling,



with the effective current density replacing the DC current density. However, it is important to emphasize that AC and DC EM are manifested in different ways. In DC EM, the current direction is unchanged, the cathode and anode locations stay the same, and void formation is seen near one end, the cathode. In contrast, for AC EM, the cathode and anode are exchanged whenever the current direction reverses. This can lead to void possibilities at either endpoint of the Cu DD wire.

Starting from Section 3.2 which describes the probabilistic DC EM model, we incorporate the possibilities of voids at either ends in our framework by calculating average current densities in the forward and reverse cycle separately and extend the DC EM model for AC EM. Consider a Cu DD wire carrying a bidirectional current (Figure 4.1). The arrows are in the directions of electron average current; conventional currents flow in opposite directions.



**Figure 4.1:** Potential void locations for AC EM.

In the forward cycle, due to the current density  $J_{avg}^+$ , electrons flow from left to right in wire  $w_1$  in metal layer  $M_{x+1}$ , leading to potential void sites at the left end of  $w_1$  and below the via in wire  $w_3$  on layer  $M_x$ . For  $w_1$ , the effective current density at the left end of the wire,  $J_{EM^L}$  is given by:

$$J_{EM^L} = J_{avg}^+ - r \cdot J_{avg}^- \quad (4.1)$$

where  $r$  is the recovery factor [20]. In the reverse cycle, the current density  $J_{avg}^-$  may cause voids at the right end of  $w_1$  and under the via in  $w_2$ . the effective current density at the right end of the wire,  $J_{EM^R}$ , is given by:

$$J_{EM^R} = J_{avg}^- - r \cdot J_{avg}^+ \quad (4.2)$$

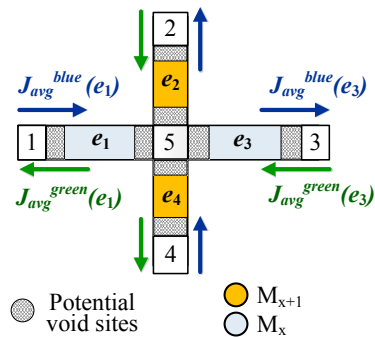
Therefore, to extend the DC resistance evolution model to AC EM, we derive a model for AC-EM-based on current density calculations using Eq. (4.1) and Eq.(4.2). However, special attention should be made while calculating the probability distribution function (PDF) of resistance change to incorporate multiple void sites. For each potential void site, the PDF of the resistance change using Eq. (3.9) should be evaluated.

## 4.2.2 AC EM flux divergence

The effective current for AC EM in a wire is not necessarily given by  $J_{EM^L}$  and  $J_{EM^R}$  (Eq. (4.1) and Eq. (4.2)) for all wires. In circuits, when multiple segments are connected by a via, the void evolution at the vias depends on the direction and magnitude of current flow in neighboring wires [59]. For such vias in Cu DD interconnect stacks, the flux divergence comes into play because the Ta barrier layer at the via acts as a barrier to the migration of metal atoms. Therefore, if a current flows through a via, any metal flux that approaches the via cannot go through the via, but instead, proceeds in the direction associated with flux divergence. In such cases, the effective current is calculated by accounting for the flux divergence.

The work in [59] incorporates the DC EM atomic flow in the wire as well as the divergence flow from neighboring wires, and we have discussed the current divergence for power grid wires in Section 3.2.4. For AC EM, the flux divergence calculations are more involved as they must keep track of bidirectional currents and the recovery factor. We show here that the way to incorporate divergence into AC EM leads to relatively simple equations, although these have not been derived in the published literature.

We consider a generic multi-layer interconnect scenario shown in Figure 4.2 in which the nets have multiple fanouts and are routed over adjacent multiple metal layers connected by vias 1 through 5. The current density in each direction through each wire is shown by the arrows, which point in the direction of electron flow. These current flows are in the directions of electron avg current; conventional currents flow in opposite directions. For each edge  $e_i$  in the figure,  $J_{avg}^{blue}(e_i)$  is the average current density flowing from left to right in a horizontal wire, and bottom to top in a vertical wire; average currents in the opposite direction are denoted by  $J_{avg}^{green}(e_i)$ .



**Figure 4.2:** Current divergence calculation example.

We consider one edge  $e_1$  and compute its effective current density, incorporating flux divergence. Using the notation in the figure, for a candidate void location at the left end of edge  $e_1$ ,

at node 1, the effective flux (including divergence) away from the node is  $J_{avg}^{blue}(e_1) + J_{avg}^{blue}(e_3)$ . The effective sweep-back flux due to current in the opposite direction is  $J_{avg}^{green}(e_1) + J_{avg}^{green}(e_3)$ . Similarly, at the right end of edge  $e_1$ , at node 5, the effective flux away from the node is  $J_{avg}^{green}(e_1)$  and  $J_{avg}^{blue}(e_3)$ , while the effective sweep-back flux is  $J_{avg}^{blue}(e_1) + J_{avg}^{green}(e_3)$ . Thus, the net effective flux, accounting for divergence as well as recovery, for voids at left and right end points of  $e_1$ , is given by:

$$\begin{aligned}
J_{flux^L}(e_1) &= \{J_{avg}^{blue}(e_1) + J_{avg}^{blue}(e_3)\} - r \cdot \{J_{avg}^{green}(e_1) + J_{avg}^{green}(e_3)\} \\
&= \{J_{avg}^{blue}(e_1) - r \cdot J_{avg}^{green}(e_1)\} + \{J_{avg}^{blue}(e_3)\} - r \cdot \{J_{avg}^{green}(e_3)\} \\
&= J_{EM^L}(e_1) + J_{EM^L}(e_3) \\
J_{flux^R}(e_1) &= \{J_{avg}^{green}(e_1) + J_{avg}^{blue}(e_3)\} - r \cdot \{J_{avg}^{blue}(e_1) + J_{avg}^{green}(e_3)\} \\
&= \{J_{avg}^{green}(e_1) - r \cdot J_{avg}^{blue}(e_1)\} + \{J_{avg}^{blue}(e_3) - r \cdot J_{avg}^{green}(e_3)\} \\
&= J_{EM^R}(e_1) + J_{EM^L}(e_3)
\end{aligned}$$

For edge ( $e_1$ ), the expressions for effective current density for a void at the left endpoint ( $J_{flux^L}(e_1)$ ) and the right endpoint ( $J_{flux^R}(e_1)$ ), mirror Eq. (4.1) and Eq. (4.2), but  $J_{EM^L}(e_3)$  is added to *both* terms here to allow for current divergence: this is a new result. The effective current densities for  $e_2$ ,  $e_3$  and  $e_4$  can be calculated in a similar way.

### 4.3 Monte Carlo simulation framework

To observe the effect of EM on signal wires, we perform probabilistic EM analysis on a set of typical on-chip signal interconnects where the performance parameter of interest is the delay of a signal net. Since our focus is on accuracy, we use HSPICE based simulations at various values of circuit operation time:  $t_o$ .

Our circuit simulations follow a Monte Carlo (MC) approach. We model the wire as a distributed RC line, with potential void locations near the vias that could cause resistance change. As described previously in Section 3 and Section 4.2.1, we model the resistance change at the end-point segments near vias as a lognormal random variable.

For the test case, the first step is to perform a single HSPICE circuit simulation to extract the effective average current density (previously discussed in Section 4.2.2) to be used for void resistance calculations and RMS current density to calculate temperature change due to Joule heating using (2.31) and (2.32). This nominal case represents the circuit state at time zero, with no EM damage. The EM average and RMS current density values are passed on to the probabilistic AC EM model, described in Section 4.2, which predicts the resistance change distribution for each wire. Using a set of 5000 samples from the probability distribution of each

wire’s resistance change, we perform circuit simulation, and extract the statistics of EM-induced timing shifts over all samples.

The process parameters for the EM model are [36, 65]:  $\sigma_c = 41\text{MPa}$ ,  $Z_{eff}^* = 1$ , and  $D_{eff} = 1.3 \times 10^{-9}\text{m}^2/\text{s}$ ,  $E_a = 0.80 \pm 0.06\text{eV}$ . The metal layer technology parameters are derived from 45nm FreePDK [66] and Joule heating parameters are taken from [35]. Our simulations are performed at temperature  $T = 105^\circ\text{C}$  and use a range of recovery factor from  $r = 0.7$  to  $r = 1$  [15, 20].

Our analysis spans multiple technology nodes starting from the 45nm technology node and projected up to the 7nm technology node. For circuit construction of the base case node: 45nm, the standard cells are taken from the NANGATE open standard cell library [67] based on the 45nm FreePDK [66]. For other technology nodes, the physical layout parameters of the standard cells are obtained by shrinking the transistor and wire features within the cell by the appropriate scaling factor [68, 69],  $S$ , which is taken to be  $\frac{1}{0.7}$  for successive technologies. For performance analysis, we perform circuit simulation using the PTM SPICE models [70–72]. Our MC simulation framework is summarized in Algorithm 2.

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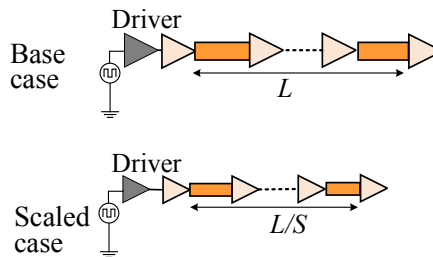
**Algorithm 2** HSPICE Monte Carlo simulation.

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- 1: Run HSPICE to obtain  $J_{flux}^L$ ,  $J_{flux}^R$  and  $J_{rms}$  for each wire.
  - 2: **for** each wire **do**
  - 3:     Use the resistance evolution model to obtain  
       lognormal PDFs of wire resistance
  - 4: **end for**
  - 5: **for** each Monte Carlo iteration **do**
  - 6:     **for** each wire **do**
  - 7:         Sample the wire resistance values
  - 8:     **end for**
  - 9:     Build a circuit sample for the netlist using the  
       above set of wire resistances
  - 10:     Perform HSPICE simulation for this netlist
  - 11:     Tabulate the value of the performance  
       parameter (delay) for the sample
  - 12: **end for**
  - 13: Report statistics (mean, standard deviation, etc.)
-

## 4.4 Results: EM-induced delay degradation of a buffered wire

We use our MC simulation method described in Section 4.3, to observe the impact of EM degradation on the circuit performance. We perform simulations at various values of circuit operation time for advanced technology nodes. We will now discuss the impact of EM on a buffered wire shown in Figure 4.3.



**Figure 4.3:** Schematic of the buffered wire for the base case 45nm technology node and the successive 32nm technology node.

A buffered wire topology is commonly observed in buses, clock networks and in general logic for carrying signals across blocks. We construct this circuit by stitching together multiple instances of  $32\times$  size inverter cell, INV\_X32, using Cu DD wires routed in one metal layer, as shown in Figure 4.3. The total wire length  $L$  is  $2000\mu\text{m}$  for the base case of a 45nm technology. The cell and the wire dimensions are chosen to construct a balanced design of an RC-loaded wire, such that neither the cell delay nor the net delay solely dominates the total delay of the buffered wire. For advanced nodes, the standard cell and the wire geometry are scaled by a scaling factor,  $S$ , as described in Section 4.3. The total wire length of a buffered wire also scales between successive technology nodes, as shown in Figure 4.3, since the circuitry shrinks. The number of repeaters remains roughly constant over all technologies.

We apply the framework described in Section 4.3 to perform MC simulation on the buffered wire. We observe the EM-induced delay degradation from the input pin of the first repeater to the input pin of the last repeater. Since our EM analysis is probabilistic, the delay degradation due to EM is also observed to be probabilistic. Given two identical parts with identical process variations and identical stimuli and environments in the field, it is impossible to predict which part will age faster in the field. Thus, margins for EM-related delay shifts must correspond to worst-case aging: we take this to be the 99.7 percentile point.

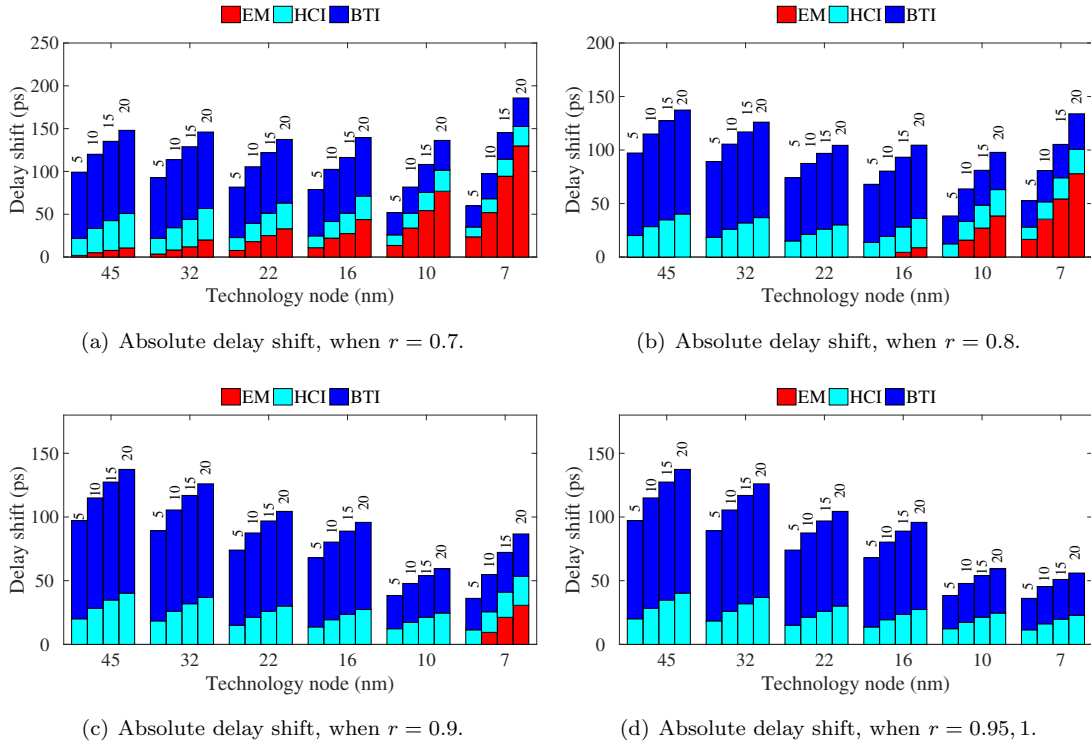
#### 4.4.1 Delay degradation: EM vs. BTI and HCI

We compare this worst-case EM-induced delay degradation against the delay degradation caused by other circuit aging mechanisms: Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI). The BTI and HCI mechanisms result in an increase in the standard cell delay while EM results in an increase in the wire delay. For calculating the delay degradation due to BTI and HCI in the INV\_X32 repeater cells we use an aging model based on [73] and [74], respectively. Figure 4.4 shows the absolute delay shift caused by the various aging mechanisms for the buffered wire, for various values of recovery factor,  $r = 0.7, 0.8, 0.9, 0.95$  and 1. It was observed that at  $T = 105^\circ\text{C}$ , there was no EM delay-shift corresponding to the recovery factor values,  $r = 0.95$  and  $r = 1$ , and we plot the delay shifts corresponding to these values together for simplicity.

The plots indicate the magnitude of the delay shift values at various values of circuit operation time,  $t_o = 5, 10, 15,$  and 20 years, for advanced technology nodes ranging from 45nm to 7nm. The absolute delay shift values are plotted on the y-axis for various technology nodes on the x-axis. Figure 4.4 indicates that for a given technology node, the contribution due to each aging mechanism increases with circuit operation time because of the increased impact with time on both transistor and wire degradation.

Notice that, for a fixed circuit operation time, as technology advances, the absolute BTI- and HCI-induced delay shift monotonically decreases while the absolute EM-induced delay shift monotonically increases. The magnitude of EM-induced delay shift is a strong function of the recovery factor  $r$ . The delay shift trends due to EM are largest corresponding to the recovery factor  $r = 0.7$  as shown in Figure 4.4(a), and for  $r = 0.8, 0.9$ , EM induced delay shift become a concern only for the advanced technology nodes, 10nm and 7nm as indicated in 4.4(b) and (c). The zero delay-shifts for  $r = 0.95, 1$  shown in Figure 4.4(d) is likely due to the low average EM current density evaluated using (4.1), which is not significant to cause sufficient mass transfer during the time period of observation at the given temperature conditions.

We also notice that although the absolute BTI- and HCI-induced delay shift decreases with technology, but the percentage degradation, as shown in Figure 4.4(b), is roughly constant. This is consistent with technology scaling trends for ring oscillators frequency degradation in [75–77].

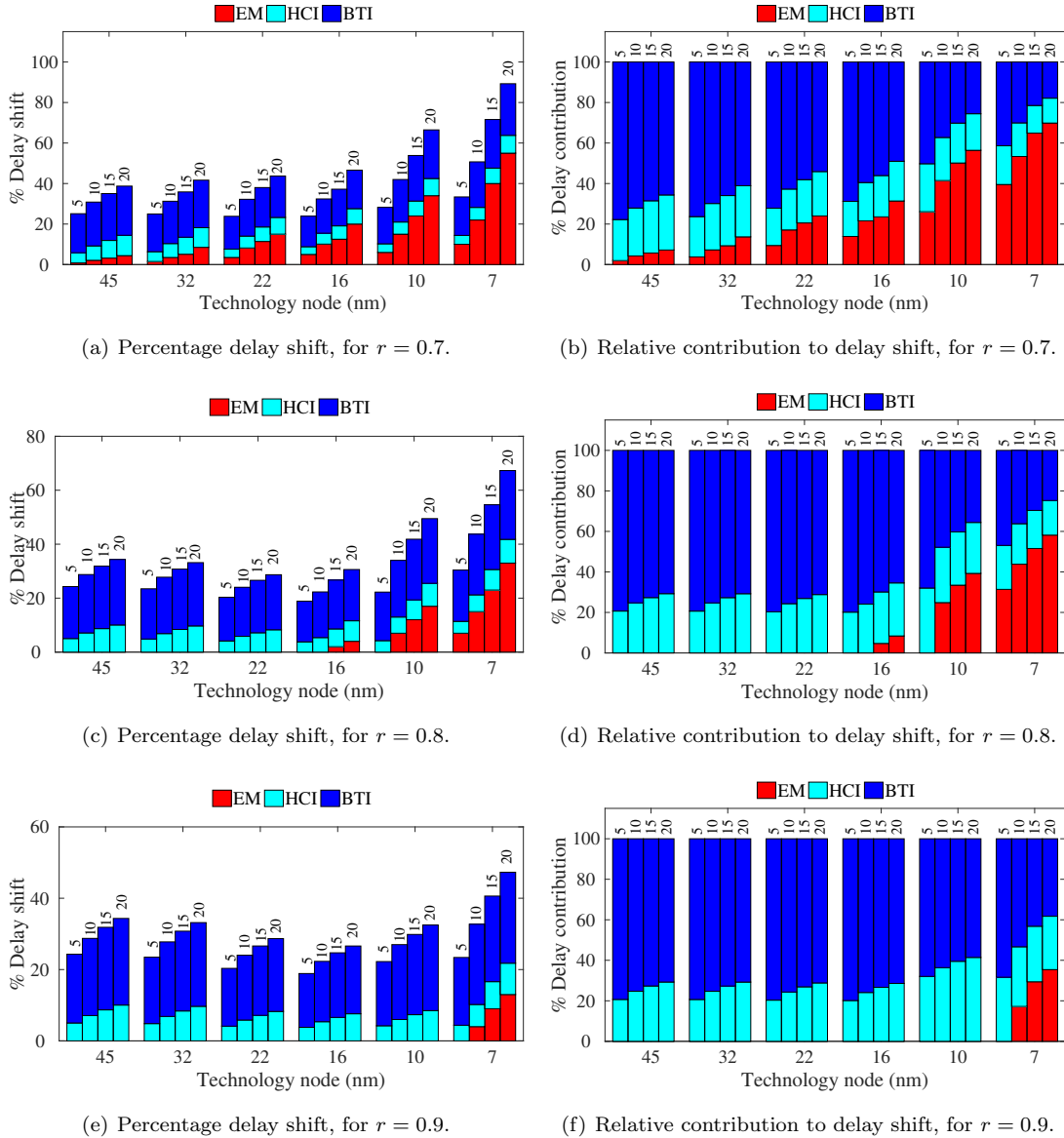


**Figure 4.4:** EM-induced absolute delay shift due to various aging mechanisms for advanced technology nodes at various values of circuit operation time, for various recovery factors,  $r = 0.7, 0.8, 0.9, 0.95$ , and  $1$ .

For quantifying the relative contribution of each aging mechanism, we show, in Figure 4.5, the percentage delay shift relative to the nominal delay (delay at the beginning of circuit operation) and the relative contribution of each aging mechanism, normalized by the total delay shift. Figure 4.5(a)-(f), indicate these parameters for  $r = 0.7, 0.8, 0.9$ . Since, the EM-induced absolute delay shift was not observed for  $r = 0.95, 1$ , as indicated in Figure 4.4(d) we are not showing the percentage delay shift and the relative contribution corresponding to these recovery factors.

Each of the charts in Figure 4.5 indicates that BTI is the dominant mechanism during early circuit operation. In other words, BTI is “front-loaded” with largest impact during the early circuit operation ( $t_o = 5$  years). As circuit operation time increases, BTI occupies a smaller fraction and the impact due to both HCI and EM increases. The magnitude of the delay degradation due to the “back-loaded” EM and HCI mechanisms increases as technology node scales further. For large values of circuit operation time, the delay contribution due to EM increases sharply, for  $r = 0.7$  and  $r = 0.8$ , especially for more deeply scaled technologies. The

amplified EM contribution is due to the increase in the wire current density as wire geometries shrink, thereby increasing the EM driving force and accelerating resistance change due to void formation and growth with advanced technology and large circuit operation time.



**Figure 4.5:** Percentage delay shift, relative to the nominal value ((a),(c),(e)) and relative delay contribution normalized by the total delay shift ((b),(d),(f)), for various values of the recovery factor,  $r = 0.7, 0.8, 0.9$ .

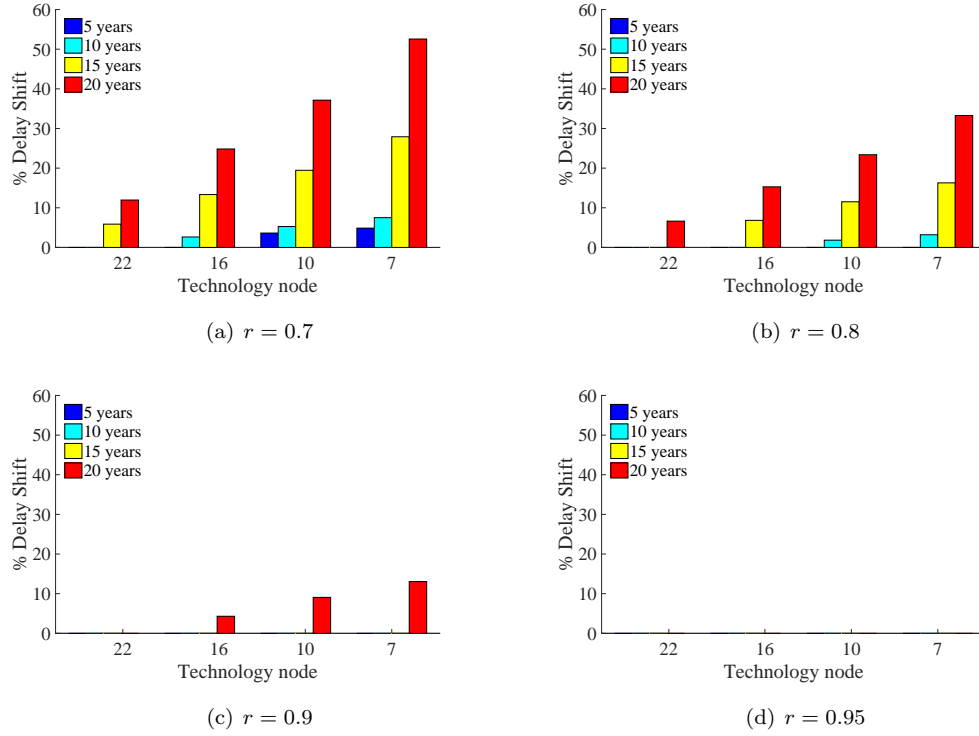


For the data point corresponding to the 7nm technology at 20 years for  $r = 0.9$ , shown in Figure 4.5(f), our simulations show that EM can contribute as much as 30% of the total delay shift due to all the mechanisms. This indicates that even for a large recovery factor of  $r = 0.9$ , EM-induced delay degradation is significant. Such large degradation can cause serious problems for high stress, long lifetime parts, e.g., in automotive applications. The AC EM-induced delay shift will not be of concern for recovery values of  $r = 0.95$ ,  $r = 1$  as indicated in Figure 4.5(g) and Figure 4.5(h). Although such large values of recovery have been reported in recent experimental works [15]. However, because there are other experimental works [20] that report lower values. Until there is a consensus on the accurate value for EM recovery for high-frequency design at chip-operating conditions, it is suggested to use a slightly pessimistic value for recovery factor (say 0.9 or 0.8), given the sensitivities of EM-induced delay shifts to the amount of recovery.

#### 4.4.2 Delay degradation: EM recovery effects at various temperatures

From the previous section, it may seem that for  $r \geq 0.95$ , EM is not a concern for the buffered-wire test case. However, a latent parameter that can change this observation is the operating temperature. Therefore, we also perform our analysis for multiple technology nodes for two values of operating temperatures: 105°C and 125°C, which can be considered as representative worst-case temperature values for server and automotive applications respectively.

We observe the variation in delay degradation focusing solely on the EM-induced delay shift, for advanced technology nodes at various values of circuit operation time. Figure 4.6 shows our results corresponding to advanced technology nodes: 22nm, 10nm, 16nm and 7nm for  $T = 105^\circ\text{C}$ . The percentage delay shift as a fraction of the nominal delay is plotted for various circuit operation time. Each of the five data points for every circuit operation time value corresponds to the recovery value,  $r$ . Each bar in these figures, shows the delay shift as a percentage of nominal delay. Since EM is probabilistic, the failure time varies from part to part, the value of the delay the value corresponds to the 99.7%ile point from our statistical HSPICE simulation.

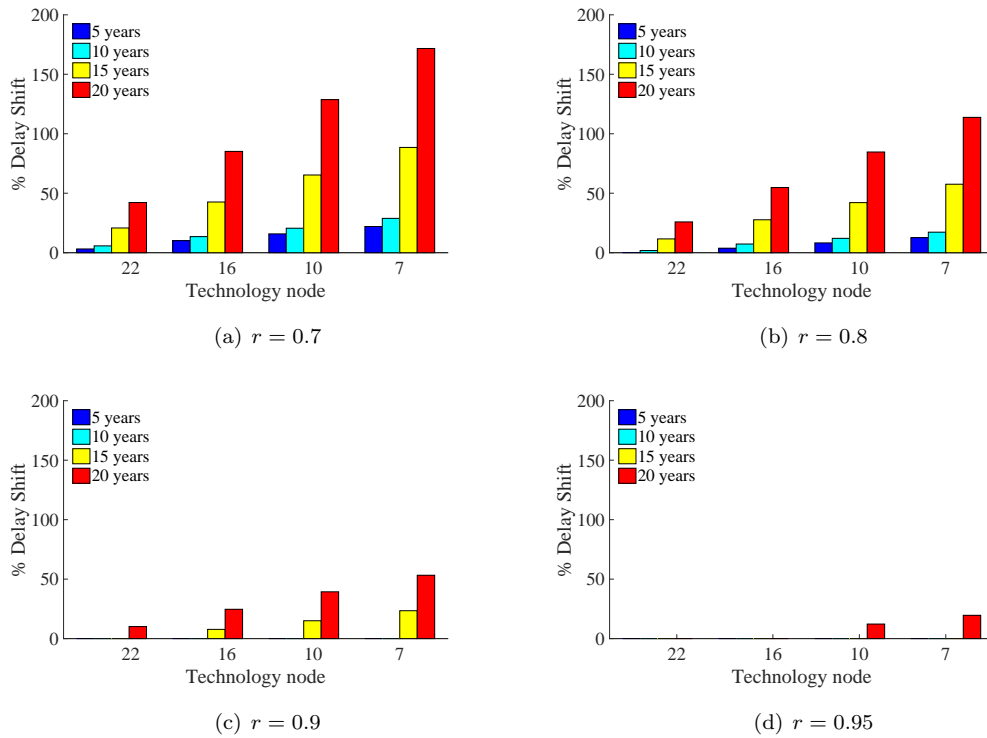


**Figure 4.6:** Delay degradation for various technology nodes at multiple circuit operation times, for various values of EM recovery at  $105^{\circ}\text{C}$ .

In all cases, we observe that the rate of EM degradation with respect to time, increases as technology scales from 22nm to 7m node. For a fixed circuit operation time, the increase in delay shift with technology is primarily attributed to the increase in the current density in the wires, exacerbating EM damage. The current density is directly related to the recovery factor, this implies that a lower recovery factor results in larger current density (4.2), thereby causing a larger EM-induced delay degradation. For a fixed technology node, the delay shift is magnified for a larger circuit operation time, since the EM voids grow to larger sizes as circuit operation time increases and more voids keep being formed.

Note that at the 10nm technology node at observation time 10 years, for recovery values beyond  $r = 0.8$ , there is practically no performance degradation due to AC EM. This is because for the larger recovery factors, the average current density is not able to cause significant EM-induced mass transfer leading to a wire resistance change. However, for scaled technologies like 7nm, even if the recovery is near-complete ( $r = 0.9$ ), AC EM may still cause significant delay degradation.

From Figure 4.6(d), we notice that for  $r = 0.95$ , there is no EM-induced delay degradation at  $T = 105^\circ\text{C}$ . However, at large value of temperature,  $T = 125^\circ\text{C}$ , the delay degradation is exacerbated as shown in Figure 4.7. Thus, the circuit performance degradation depends on the recovery factor, and the performance shift reduces for a large recovery values that are reported in [15]. However, unless it is established that there is complete recovery with respect to EM for AC current flow, circuit performance degradation may be significant depending on the technology node as well as the environment parameters, which are a strong function of application in which the circuit will be utilized. We have shown that for a 20-year target lifetime, at a temperature  $125^\circ\text{C}$ , typical of automotive applications, even a recovery factor of 0.95, indicating near-complete recovery may result in a 15% performance degradation for 7nm.



**Figure 4.7:** Delay degradation for various technology nodes at multiple circuit operation times, for various values of EM recovery at  $125^\circ\text{C}$ .

## Chapter 5

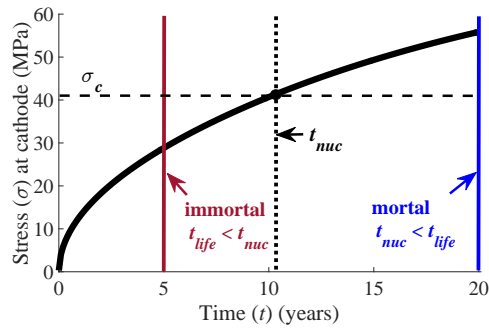
# Role of back-stress: EM mortality under temperature and product lifetime specifications

This chapter builds on the formulation for wire mortality discussed in Section 3.2.5, and evaluates the transient evolution of stress, relative to the product lifetime, for the range of wire lengths observed in circuits. The chapter presents an improved set of simple, practical EM mortality criteria, and illustrate our results using a set of power grid benchmarks. Section 5.1 introduces the concept of mortality relative to the product lifetime and Section 5.2 provides a quick summary of the classical approach towards mortality, which has been based on the Blech-Black approach that was discussed in Section 1.3. Section 5.3 discusses our transient modeling approach leading to our hierarchical mortality criteria and in Section 5.4 we discuss the results of our mortality criteria for different industrial power grid benchmarks, and we compare our results with the traditional methods.

### 5.1 Introduction

As EM considerations become more critical, there is a need for circuit analysis and design techniques to incorporate the knowledge of EM reliability physics to realize a design which meets the expected performance as well as the reliability targets. From Section 1.3, we know that the typical signoff flows [78] first filter out EM-immortal wires based on Blech criterion [8]. For the remaining wires, a current density limit, based on Black's equation [9], is applied to check mortality.

In this chapter, we perform a rigorous analysis of the dynamics of EM stress evolution to provide concrete product-lifetime-specific criteria for mortality. Figure 5.1 shows the stress evolution for a wire with length,  $L = 100\mu\text{m}$ , which is carrying a current density  $j = 0.5\text{MA}/\text{cm}^2$  at an operating temperature  $T = 105^\circ\text{C}$ . We use the process parameters corresponding to modern Cu Dual Damascene (Cu DD) based technology, listed in Table 3.1. For a product lifetime of 5 years, the wire is immortal, since the stress does not cross the critical stress,  $\sigma_c$ , in this interval. For a 20-year lifetime, the same wire is mortal since its stress crosses  $\sigma_c$  in this interval. For a 20-year lifetime, the same wire is mortal since its stress crosses  $\sigma_c$ .



**Figure 5.1:** Wire mortality and product lifetime.

Most designers realize that compared to long-lifetime (e.g., automotive) parts, products with shorter lifetimes (e.g., mobile clients) should have fewer EM-susceptible mortal wires. The Blech criterion is inherently unable to capture lifetime considerations because it is valid only for wires that achieve steady state [22, 79], and it does not consider transient EM behavior. While the current density check based on Black’s equation [9] is lifetime-dependent, it is limited due to its simple and empirical nature: it does not capture the dependence on all process parameters [11], and its current density limit is the same for all wires, and cannot capture the dependence of EM on wire length [19].

The idea of comparing the nucleation time with lifetime to determine mortality has been introduced in [13] and also in Chapter 2, but their analysis is simpler and less rigorous than our approach. Unlike those approaches, we concretely incorporate the effects of line lengths, which can be significant. The Blech criterion also predicts immortality, but it is based on a steady state, and unlike our work, does not consider the transient, which can be long. The work in [29] proposes an approximate physics-based model, but it relies on the Blech criterion, and as shown in Section 5.3.2, its approximate truncation for finite lines incurs significant errors.

We present a new criterion that accounts for the role of product lifetime and temperature in determining wire mortality for a given set of process parameters. Our criterion for mortality analyzes the stress evolution in the interconnect.

## 5.2 Traditional method for determining EM mortality

As discussed in Chapter 1, the conventional method for EM analysis for interconnects involves a two-step process. The first step involves filtering out EM immortal wires using the Blech criterion [8]. Mortal wires are susceptible to EM and can potentially cause EM failure. In the second step, the current density flowing through these wires is checked against a global limit, which is determined using the Black's equation [9]. Despite the simplicity of the Blech criterion, one of its limitations is that it is based on the assumption that a steady state is achieved between the electron wind and back-stress.

However, recent Cu DD process enhancements for performance improvement may challenge the above assumption. Recent technology upgrades, such as the introduction of low-k inter-layer dielectric (ILD), and usage of ultra-thin Ta barrier layer has resulted in lower back-stress compared to earlier interconnect technologies [19, 79]. This can result in an increase in the time required for sufficient mass transfer to generate a back-stress to balance the electron wind force [80]. For some wires, the time to steady state may surpass the product lifetime, and the Blech criterion may estimate the stress at a time later than the circuit lifetime.

Wires that are rendered mortal by the Blech criterion need further analysis to check if they can use EM damage during the lifetime of the product. This is done using the Black's equation [9], which describes the mean time to failure, *MTTF* for a wire under EM according to (1.2) The issue with using a current density limit derived from Black's equation shown in (1.2) has to do with its empirical nature, which does not capture the impact of some EM related circuit and process parameters. Moreover, the value of the exponent  $n$ , is a matter of controversy for Cu DD interconnects [11].

Further, the current density limit imposed is not context-dependent, but is identical for all wires. Experiments show that short and long wires show different EM characteristics due to the role of mechanical properties [19], and such parameter dependence should be accounted for while performing EM-mortality check.

## 5.3 Transient stress modeling

The temporal evolution of EM-induced stress involves the interaction between electron wind and back-stress. As indicated in Chapter 2, this is modeled by the partial differential equation [1]

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[ \kappa \left( \frac{\partial \sigma}{\partial x} + G \right) \right] \quad (5.1)$$

Here, the part involving  $G$  corresponds to the electron wind force and the one including  $\frac{\partial \sigma}{\partial x}$  represents the back-stress force as described in Section 2.2 The partial derivatives are with respect to  $x$ , the distance from the cathode, and time,  $t$ .

For modern interconnect Cu interconnects, steady state may not be achieved during the product lifetime. We check for EM-susceptibility based on the evolution of stress as a function of time. For our analysis, we are interested in the general solution for stress evolution. We will discuss the two solutions relevant to our analysis, corresponding to the two cases – a semi-infinite (*SI*) line and a finite (*F*) line as described in [1]. The cathode for the line is at  $x = 0$  in both cases; for the semi-infinite case, the anode is at  $\infty$ , while for the finite line, the anode is at a finite  $x = L$ .

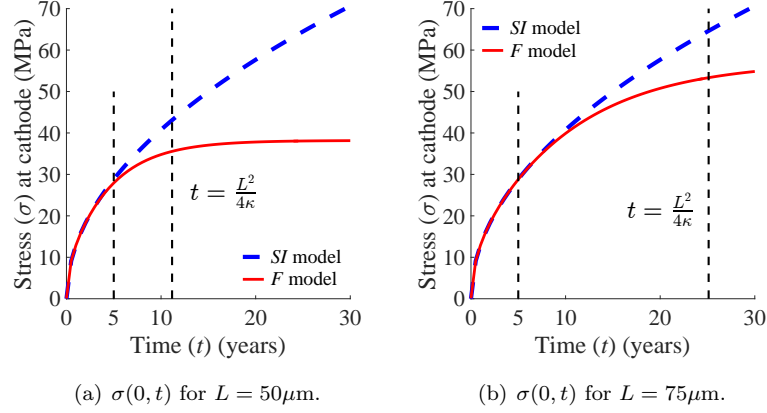
### 5.3.1 Stress evolution at the cathode

As discussed in Section 2.5, for copper interconnects voids typically form near the cathode [30], and the stress evolution at the cathode ( $x = 0$ ) is of primary interest. The stress solutions at  $x = 0$  have been described in (2.22) and (2.23), corresponding to the semi-infinite *SI* wire, and the finite *F* wire. The solution for the *SI* boundary condition is compact, and thus useful in circuit analysis [13, 31]. However,  $\sigma_{SI}$  is pessimistic since the *SI* case experiences lower back-stress. Moreover, the *SI* model has no length dependence since the wire has infinite length.

For wires in power grids, the length,  $L$ , may vary from a scale of micrometers to hundreds of micrometers. The solution corresponding to the finite line BC is directly models the length dependency. However, the finite wire solution,  $\sigma_F$ , includes an infinite series, which makes its exact evaluation computationally difficult.

### 5.3.2 Analysis: Semi-infinite and finite line model

Figure 5.2 shows the stress as a function of time, for the *SI* and *F* cases, for two values of wire length,  $L = 50\mu\text{m}$  and  $75\mu\text{m}$ . The current density used for the above simulation,  $j = 0.5\text{MA}/\text{cm}^2$ . The process parameters along with the sources are listed in Table 3.1. It can be seen that the solutions for the *SI* and *F* cases differ for  $L = 50\mu\text{m}$  (as shown in Figure 5.2(a)), and the differences reduce for a larger value of  $L = 75\mu\text{m}$ , as shown in Figure 5.2(b). Notice that the two solutions begin to diverge after an initial period. The work in [1] observes that the steady state for a line of length,  $L$ , can be achieved in time  $t \approx \frac{L^2}{4\kappa}$ , and we can observe that at this instant the stress prediction between the two lines can differ significantly. However, we observe that the two solutions do not differ significantly, during initial stages up to  $t = 5\text{years}$  for both cases. This is because sufficient back-stress has not built up during this time.



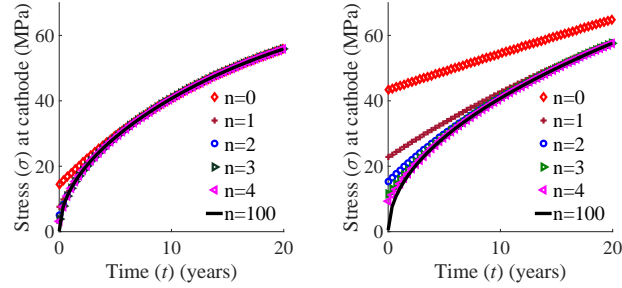
**Figure 5.2:** Stress at the cathode, as predicted by  $SI$  and  $F$  model at multiple wire length,  $L$ .

To predict the wire mortality as a function of the product lifetime, we use the formulation for stress at the cathode in the  $SI$  line, as in (2.24), and the  $F$  line, as in (2.25).

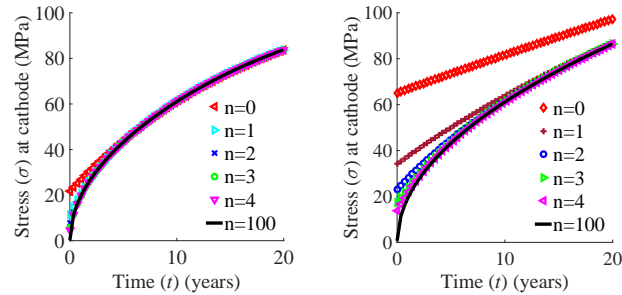
In fact, the solution corresponding to the semi-infinite line,  $\sigma_{SI}$ , shown in (2.24) is an upper bound on  $\sigma_F$ , which is also observed in Figure 5.2. This occurs because a finite line sees a larger back-stress than the semi-infinite line, and the larger back-stress attenuates the net stress at the cathode. This larger back-stress is a result of a larger stress gradient compared to the semi-infinite line. The implication of this observation is that if the stress predicted by the  $SI$  solution shown in (2.24) is less than the critical value,  $\sigma_c$ , *the wire is sure to be immortal*. In this case, we do not need to evaluate the more accurate stress using the  $F$  solution shown in (2.25), which involves the evaluation of an infinite series. Additionally, for the solution corresponding to the finite line  $\sigma_F$  in (2.25), we study the variation in the error in predicting  $\sigma_F$  by considering truncation of the infinite series for multiple values of  $n$ , for multiple wire length,  $L$ . The accurate stress corresponds to the truncation at  $n = 100$ .

The analysis in [29] truncates the series to only one term, corresponding to  $n = 0$ . For  $L = 100\mu\text{m}$ , Figure 5.3(a) shows that such a truncation does not differ from the accurate solution. In contrast, for  $L = 300\mu\text{m}$ , Figure 5.3(b) demonstrates that the stress computed by the  $n = 0$  truncation leads to significant deviation from the correct value. The truncated sum converges as the number of terms increases from  $n = 0$  to  $n = 4$ , and the plots corresponding to  $n = 4$  matches the accurate solution. We choose a value of  $n = 20$  to cover the range of wire length up-to a worst-case limit of  $2000\mu\text{m}$  and a worst-case current density of  $3\text{MA}/\text{cm}^2$ . We use the process parameters from Table 3.1. For a different process, the number of terms may be determine through a single characterization for the longest wire length.





(a) Finite line:  $L = 100\mu\text{m}$ ,  $j = 0.5\text{MA}/\text{cm}^2$  (b) Finite line:  $L = 300\mu\text{m}$ ,  $j = 0.5\text{MA}/\text{cm}^2$



(c) Finite line:  $L = 100\mu\text{m}$ ,  $j = 0.75\text{MA}/\text{cm}^2$  (d) Finite line:  $L = 300\mu\text{m}$ ,  $j = 0.75\text{MA}/\text{cm}^2$

**Figure 5.3:** Finite line model prediction, for different  $n$  in (2.25), at multiple scenarios of  $j, L$ .

For this technology, for wire lengths larger than  $100\mu\text{m}$ , the solution corresponding to the semi-infinite line ( $SI$ ) closely matches the numerical solution corresponding to the finite line ( $F$ ). This is also indicated by observing the reduction in the difference between stress prediction using the  $SI$  and  $F$  models as the wire length increases, as shown in Figure 5.2.

### 5.3.3 Hierarchical mortality criteria

We discuss our framework, which uses the previous observations to predict wire mortality in power grid. We take as input the current density  $j$  and the length  $L$  for every wire, and the process and environment specifications. The output of our framework is the set of EM-susceptible wires. Note that we use “mortal” and “EM-susceptible” as synonyms.

As shown in the schematic in Figure 5.4, our framework sequentially filters out wires that are immortal stage-by-stage in order to reduce the number of candidates for the finite wire model  $F$ , since it is the most computation intensive by virtue of its structure as it involves computation of non-linear series involving wire length,  $L$ .

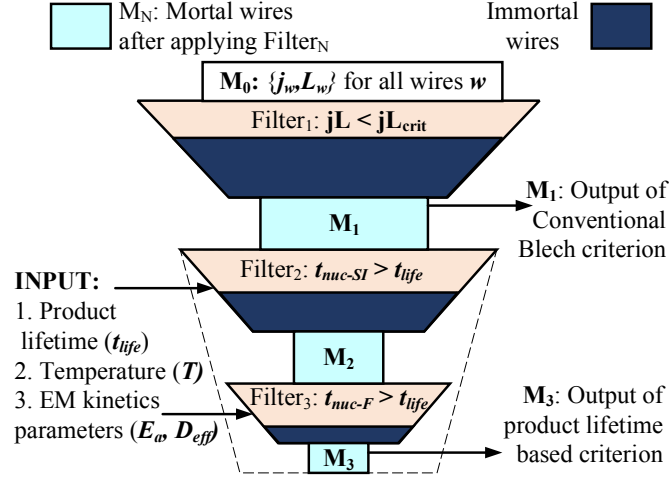


Figure 5.4: Sequential filtering of mortal wires.

We sequentially use the Blech criterion, the semi-infinite line ( $SI$ ) solution (2.24), and the finite line ( $F$ ) solution (2.25). This enables us to tackle the trade-off between the limited accuracy and lifetime-independence of the easy to compute Blech-criterion, against the more accurate, but computation intensive finite line formula. We now discuss the three stages utilized to filter out the immortal wires in order to obtain the final, realistic estimate for the number of mortal wires corresponding to the lifetime, and process specifications.

**Filter 1:** We first use the Blech criterion discussed in Section 1.3 to filter out wires that are immortal under any product lifetime. The Blech criterion is based on the peak stress achievable, and if this never crosses  $\sigma_c$  then the wire is immortal regardless of lifetime.

**Filter 2:** Next, for the remaining wires, we obtain an optimistic estimate of the nucleation time,  $t_{nuc-SI}$  by using (2.24) to solve for the time at which the stress at the cathode reaches the critical stress, i.e.,  $\sigma_{SI}(0, t_{nuc-SI}) = \sigma_c$ , i.e.,

$$t_{nuc-SI} = \frac{\pi \sigma_c^2}{4 G^2 j^2 \kappa} \quad (5.2)$$

The estimate is optimistic because the actual stress is at most  $\sigma_{SI}$ , and the actual value of  $t_n$  is no smaller than the value predicted here. Therefore, any wire for which the estimated  $t_{nuc-SI} > t_{life}$  also has the property that its real nucleation time  $t_n > t_{life}$ , i.e., it is effectively immortal.

**Filter 3:** For the remaining wires, the actual nucleation time may or may not exceed the product lifetime. For these potentially mortal wires, we compute the precise nucleation time,  $t_{nuc-F}$ , for the wire by numerically solving the stress expression in (2.25), truncated to 20 terms,

to solve for  $t_{nuc-F}$

$$\sigma_F(0, t_{nuc-F}) = \sigma_c \quad (5.3)$$

using a Newton-Raphson approach. If the final value of  $t_{nuc-F}$ , as predicted by our iterative procedure, exceeds the product lifetime,  $t_{life}$ , then the wire is effectively immortal.

As indicated previously, the first two criteria are simple to evaluate and involve closed-form expressions. The last criterion requires a numerical procedure to solve (2.25). This step involves more (but manageable) computation than the first two criteria, but applied to a smaller set of wires that are not already eliminated as immortal by the previous criteria.

## 5.4 Results

We implement our method described in Section 5.3.3, using MATLAB and C++, and we test our analysis on a set of standard power grid circuits to estimate the number of mortal wires as a function of the product lifetime for a set of temperature and Cu DD process specifications, listed in Table 5.1.

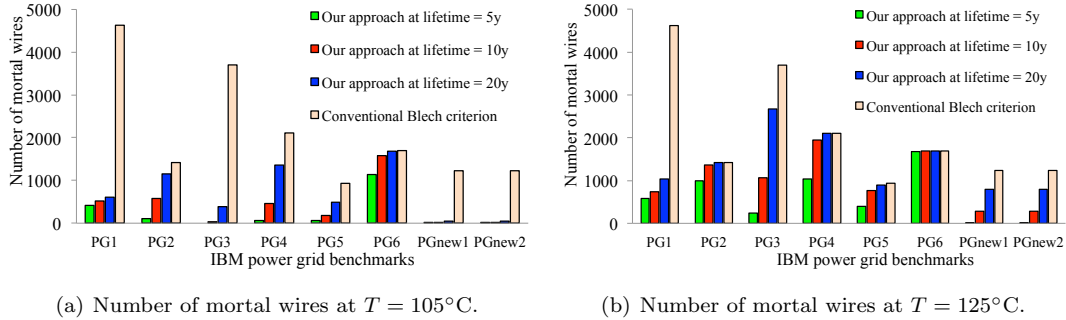
Symbol	Definition	Value
$\rho$	Cu Resistivity	$2.25 \times 10^{-8}$ Ohm-m
$\Omega$	Atomic volume	$1.18 \times 10^{-29}$ m <sup>3</sup>
$B$	Effective bulk modulus	28GPa [31]
$\sigma_c$	Critical stress	41MPa [31]
$Z_{eff}^*$	Atomic charge number	1 [31]
$D_0$	Diffusivity constant	$1.3 \times 10^{-9}$ m <sup>2</sup> /s [31]
$E_a$	Activation energy	0.8eV [31]

**Table 5.1:** EM process parameters for Cu DD interconnects.

The power grid circuits used in our simulations are a set of industrial benchmarks imported from [2]. Note that the percentage nominal IR drop, defined as the worst IR drop value among all the nodes as a percentage of supply voltage at time  $t = 0$ , was unrealistically large in some of the original benchmarks ( $> 20\%$ ), and in a similar manner as discussed in [29], we have scaled the original value of current loads for these benchmarks, such that the percentage nominal IR drop is in the 11-12% range for all the circuit benchmarks.

We take as input the process parameters, corresponding to the Cu DD technology from Table 3.1, along with the current density and wire length for every wire.

**Comparison with Blech:** Figure 5.5 shows the number of mortal wires as predicted by our approach at multiple product lifetime values of 5, 10, and 15 years, representing the mobile, computing, and automotive application lifetime values. We compare our prediction against the classical Blech criterion. We show our calculations for two values of operating temperature  $T = 105^\circ\text{C}$  (Figure 5.5(a)) and  $T = 125^\circ\text{C}$  (Figure 5.5(b)). We do not show wires caught by Black’s equation here, but will do so later.



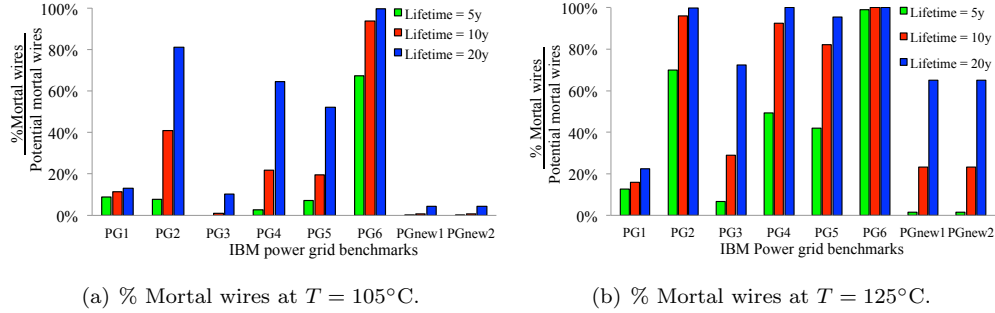
**Figure 5.5:** Mortal wires: Conventional Blech criterion vs. our product lifetime based approach.

For all power grid circuits, the number of mortal wires from our approach is smaller or equal to the number of mortal wires predicted by the conventional Blech criterion, for each specification of product lifetime. This is not surprising because Filter 1 in our approach is the Blech criterion. Our mortal set is provably a subset of Blech-mortal wires.

The difference in the prediction between the two approaches is largest for short-lifetime (5 years) applications, and the difference reduces for larger lifetimes. This is because at smaller lifetime values, most of the wires do not undergo significant mass transfer which can generate enough stress for void nucleation. The Blech criterion, by construction bases its analysis at the time when steady state is achieved, and thereby renders some of these wires as mortal wires.

In Figure 5.5(b), for a fixed lifetime, the number of mortal wires is seen to increase for a larger value of temperature. This is because the transient stress characteristics are a strong function of temperature due to the Arrhenius relationship between  $D_{eff}$  and  $T$ . In contrast, the steady state characteristics in (2.14) are temperature independent, and that is why the number of mortal wires predicted by the conventional Blech criterion are the same for both temperatures.

Figure 5.6 shows the number of mortal wires as a fraction of those predicted by the Blech criterion. We observe an increase in the number of mortal wires for a larger temperature of  $T = 125^\circ\text{C}$  (Figure 5.6(b)) as compared to  $T = 105^\circ\text{C}$  (Figure 5.6(a)). This increase occurs over all benchmarks.

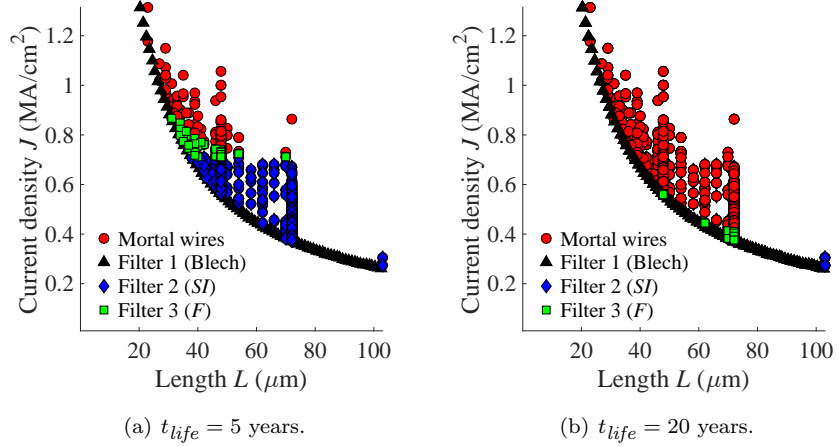


**Figure 5.6:** Mortal wires expressed as a percentage of the potential mortal wires predicted by the conventional Blech criterion.

For a lifetime of 20 years, data corresponding to the power grid benchmarks: PG2, PG4, PG5, and PG6 indicates that close to 100% of the wires predicted as potentially mortal by the Blech criterion are indeed mortal by our criteria. For the remaining benchmarks, there the gap between the two approaches is significant. Some of the wires predicted by Blech as mortal, are immortal even at a lifetime of 20 years. This is possibly due to the fact that power grids PG1, PG3, PGnew1, and PGnew2 have longer wires, some of the order  $1000\mu\text{m}$ , in PG1. Due to the large wire length, the  $jL$  product for these wires is large, even for a small current density value, and may cross the critical value, which renders them mortal. However, because of the low current density, the time taken for the mass transfer required for steady state will exceed the lifetime. A current density filter such as Black’s equation or the Filter 2 proposed in our approach will see that this wire does not experience EM degradation, thus averting the pessimism due to the Blech criterion.

**Effectiveness of each filter:** Next, we observe the distribution of wires, which are filtered out after application of each of the three wire mortality filters, as described in Section 5.3.3. Figure 5.7 shows this statistic, for the benchmark circuit IBMPG2. The data is shown for different values of product lifetimes,  $t_{life} = 5, 20$  years. The wire lengths are indicated on the  $x$  axis and the corresponding current density is plotted on the  $y$  axis. The plot shows the number of mortal wires as predicted by our approach, along with the wires which, although predicted as mortal by the Blech criterion (Filter 1), but are filtered out as immortal by us.

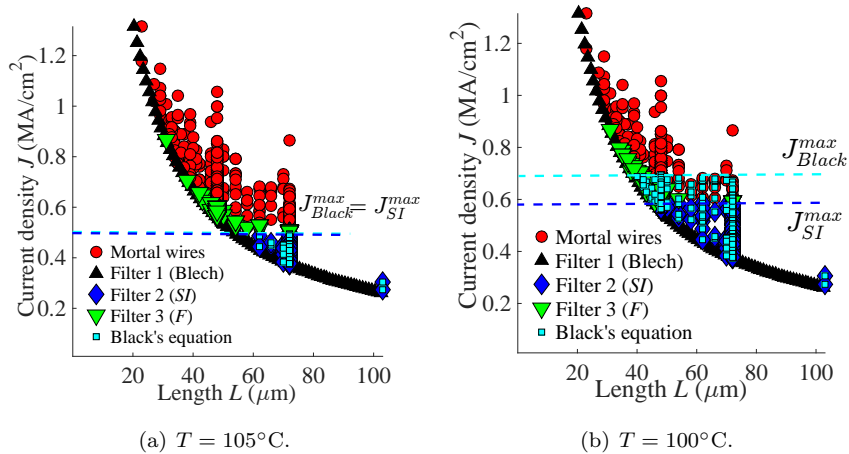
From Figure 5.7(b) we can observe that for a lifetime of 20 years, almost all the wires are mortal and the number of mortal wires decreases corresponding to shorter lifetime of 5 years shown in Figure 5.7(a). Furthermore, notice that the simple to compute Filter 2 filters out a majority of wires compared to the computation intensive Filter 3, which is in agreement with our observation in Section 5.3.2.



**Figure 5.7:** Distribution of mortal wires for IBMPG2 at various lifetime values,  $t_{life}$ , for  $T = 105^\circ\text{C}$ .

These observations highlight the pessimism in the Blech criterion and emphasize the importance of a lifetime-based mortality filter, such as the one obtained by Black's equation or ours from Section 5.3.3, which we show to be better.

**Comparison with Blech+Black:** We now compare the distribution of wires filtered out using our framework with the traditional current density filter derived from Black's equation. Figure 5.8 shows the distribution of wires filtered as immortal using our criterion and the Black's equation, for two different temperature values of  $T = 105, 100^\circ\text{C}$ .



**Figure 5.8:** Distribution of mortal wires for IBMPG2 at two different temperatures,  $T$ , at  $t_{life} = 10$  years.

The Blech filter removes many wires below the  $jL=\text{constant}$  curve and to reduce clutter, we only show the frontier of the curve in these plots. To characterize the pre-exponential constant in Black’s equation, we assume that a wire with current density  $0.5\text{MA}/\text{cm}^2$ , has a lifetime of 10 years at temperature,  $T = 105^\circ\text{C}$ . This assumption enables us to have the same current density limit at  $T = 105^\circ\text{C}$ , as shown by  $J_{Black}^{max}$  and  $J_{SI}^{max}$  in Figure 5.8(a). However, *both of these criteria miss wires (green points) that are captured only by our Filter 3*. A constant  $j$  filter would mix these green points with red mortal wires, because neither Black’s equation nor our Filter 2 can fully capture the role of wire length in EM evolution.

From Figure 5.7(b), we observe that at a smaller temperature value  $T = 100^\circ\text{C}$ , the maximum current density limit as obtained using the Black’s equation and our filter 2 increases. This is because of the exponential dependence of EM dynamics on temperature, which is modeled by both the above formulations. However, the jump in the current density criterion from using the Black’s equation is larger than that observed by our Filter 2. This is because the pre-exponential factor in Black’s equation is temperature independent in the way it is used today in industry settings. However, in reality the pre-exponential factor has a temperature dependency [11]. Our model and framework explicitly captures this temperature dependency.

**Impact of process:** Lastly, we perform simulations which use different specifications of process parameters corresponding to the Cu Dual Damascene interconnect technology, which are listed in Table 3.1 and Table 5.2. We perform our simulation, corresponding to two alternate Cu DD process, which are differ the Cu-capping materials used. The EM diffusion process parameters are taken from [15] and listed in Table 5.2. The grain size is assumed to be  $0.1\mu\text{m}$ .

Cu DD Process			
Grain size = $0.1\mu\text{m}$		Set I	Set II
$E_a = 0.84\text{eV}$		Cu/dielectric	Cu/CoWP
$Z_{eff}^*D_0(m^2/s)$		$5\times 10^{-9}$	$4\times 10^{-9}$
Lifetime (years)	Blech Mortal	% Mortal wires for IBMPG2	
		Set I	Set II
5	1418	11.6	5.3
10	1418	51.2	35.7
20	1418	84.8	73.8

**Table 5.2:** Mortal wire prediction for IBMPG2.

Notice that, the conventional Blech criterion, predicts the same number of mortal wires (=1418), for two processes. This is because the conventional criterion is oblivious to EM parameters like  $D_0$ , as they do not appear in (2.14) or (1.2). In contrast, the number of mortal

wires as predicted by our work vary depending on the process parameters. Table 5.2 list the number of mortal wires predicted by our criterion as a percentage of the number of mortal wires predicted by the conventional Blech criterion. Notice, that for a larger value of EM diffusivity constant  $D_0$ , corresponding to process Set I, the percentage mortal wires are larger. This is intuitive, since a larger diffusivity implies faster mass transfer.



## Chapter 6

# Role of thermomechanical stress: IR-drop degradation in power grid via arrays

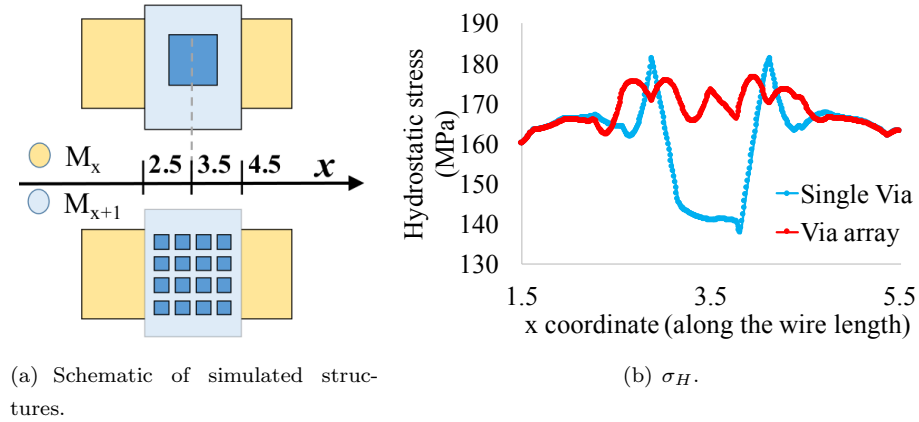
In this chapter, we discuss the performance degradation in a power grid circuit, as a result of EM, in the context of via array structures, commonly observed in modern power grids, which connect the interconnects located at different metal layers. The analysis captures the thermomechanical stress in via arrays that can potentially influence EM through an FEA based approach. The work also accounts for redundancy as a result of using redundant structures such as via arrays in a redundant power grid system, and predicts the EM performance of power grid by using a statistical approach. Section 6.1 briefly introduces the prior work with respect to modeling the via arrays, Section 6.2 describes the EM physical model that has been employed for via arrays in this work, Section 6.3 describes our analysis of the thermomechanical stress in power grids using finite element analysis based approach, Section 6.4 discusses the differences in the electrical and mechanical properties when the vias are modeled as via arrays as against single vias. Our circuit simulation framework is also described at the end of this section. Lastly, Section 6.5 discusses the result of our simulations on a standard power grid circuit.

### 6.1 Introduction

As a result of the sensitivity of EM in modern copper dual damascene (Cu DD) interconnects to layout, process, and environmental parameters [11], interconnect failure times can show significant levels of variation. Recent works on EM circuit analysis [13, 29, 38] account for EM physics

in wires, but implicitly model power grids vias as single via structures that span the width of the wire, or make no comments about the role of vias. However, connections between the metal layers of the power grid in modern circuits, which can use wires as wide as  $2\text{--}3\mu\text{m}$ , almost always involve an array of vias instead of a single via. These via arrays have complex geometrical and electrical characteristics that can affect EM, and we examine this relationship in this work. Preliminary work on examining via array structures has been performed in [81] and [82]. The work in [81] performs stress-EM analysis to determine the time to failure, TTF, for via array configurations, and [82] is one of the early circuit analysis works that addresses redundancy and current crowding in via arrays. However, for chip operating conditions, the combined impact of stress and redundancy factors on circuit performance has not been adequately addressed. This is the focus of our work.

In the present methodology for EM, circuit designers typically guard against EM by comparing current densities against a foundry-specified limit for a process technology. The conventional current density limit is characterized through experiments performed on interconnect test structures stressed at elevated temperatures and high voltages to induce EM failure in a practical time frame, and the failure times are mapped back to normal chip operating conditions [11]. While such experiments have been widely used to characterize EM in Cu DD interconnects, they fail to capture the effect of thermomechanical stress, which influences EM at normal chip operating conditions. This stress is generated due to a mismatch in the coefficient of thermal expansion (CTE) of the metallization (copper metal and passivation layers) and the surrounding dielectric [83]. The CTE differential results in compressive and tensile stresses in the wire when the wafer is annealed from high-temperature manufacturing conditions to normal operating temperatures. Moreover, the thermomechanical stress is a function of the layout and the composition of the surrounding layers.



**Figure 6.1:** (a) A  $1 \times 1$  and  $4 \times 4$  via array. (b) The corresponding hydrostatic stress along the wire beneath the via (in Pascal) for the  $1 \times 1$  and  $4 \times 4$  via.

Figure 6.1(a) shows two via configurations, corresponding to a single via and a  $4 \times 4$  via array. The vias connect an upper level of metal  $M_{x+1}$  with the next lower level,  $M_x$ , and the metal layer heights are taken to correspond to M7 and M8 in a 32nm technology node [84]. The wire widths are chosen as  $2\mu\text{m}$  for the interconnects, and are representative of wires in a power grid. Both vias have an effective area  $1\mu\text{m}^2$ , and therefore correspond to the same resistance between  $M_x$  and  $M_{x+1}$ . Fig 6.1(b) shows the hydrostatic stress, computed on the lower metal layer  $M_x$ , along the wire length, along the centre of the interconnect (width/2), and just underneath the  $\text{Si}_3\text{N}_4$  capping layer: this is the site where a void is likely to form. Note that the stress minima occur at points where the via touches the lower metal, and the maxima occur in the regions between the vias, since the lower metal layer is exposed more to the ILD in between the vias. It can be seen that the stress for the  $4 \times 4$  case is larger by about 30MPa.

The above differential translates into a change in the lifetime of the via. For a critical stress,  $\sigma_c = 340\text{MPa}$  [85], we can calculate that a differential of 30MPa can result in approximately 30% change in the mean time to failure of a single line. As established in [13, 29, 38], this affects the electrical characteristics of the power grid: each via failure perturbs the power grid, and after a sufficient number of vias fail, the power grid may not longer meet its IR-drop specifications. The use of via arrays introduces a greater amount of redundancy than a single via, and solutions that lump the via array into the single-via model may be pessimistic in analyzing the EM-induced IR-drop degradation since they do not account for this redundancy.

The contribution of this work is to combine the known physics behind void evolution due to EM with the layout-dependent impact of thermomechanical stress on via arrays in power grids. Based on the experimental observations from [86] that the void under vias often result

in early failures, we build a framework for EM analysis incorporating via arrays and percolate this analysis to compute the probability distribution of EM-induced IR-drop. We incorporate deterministic variations due to thermomechanical stress as a function of layout of the power grid and the via array configuration. We develop a hierarchical methodology wherein we characterize the performance of via arrays, and use it to predict the overall performance degradation in power grid.

## 6.2 EM modeling for via arrays

EM failures in Cu DD wires occur through the formation and growth of voids [11]. For copper interconnects, experimental works have reported two types of voids that form near/under the via at the cathode end – slit voids that result in early failure, characterized by rapid wire resistance increase, and voids spanning interconnects that result in late failure due to gradual resistance increase [86].

This work focuses on slit voids under vias. The time-to-failure (TTF) for slit voids can be modeled by the time,  $t_n$ , at which the void nucleates: this is a slightly pessimistic, but accurate, estimate since it neglects the rapid growth time [86] for the void to grow to an open circuit, once nucleated. In Appendix B, we attempt to model the void growth scenario for a slit void, and we verify that the via resistance as a result of slit void growth, rises rapidly. Thus, the voids once nucleated rapidly cause failure, and their growth time can be neglected. The nucleation time is given by [1]:

$$\text{TTF} \approx t_n = \frac{(\sigma_C - \sigma_T)^2 C_{t_n}}{D_{eff}} \quad (6.1)$$

$$D_{eff} = D_o \exp(-E_a k_B T) \quad (6.2)$$

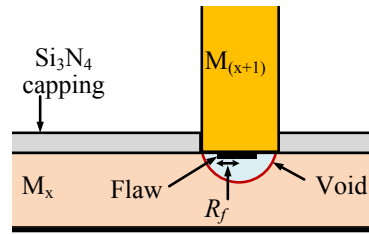
$$C_{t_n} = \frac{\pi}{4} \left[ \frac{\Omega k_B T}{(e Z_{eff}^* \rho_{Cu} j)^2 B} \right] \quad (6.3)$$

Here,  $\sigma_C$  is the critical stress for void nucleation;  $\sigma_T$  is a term that accounts for the thermomechanical stress and package stress in the wire;  $C_{t_n}$  is a constant that is dependent on properties of the Cu DD metallization;  $D_o$  is the EM diffusivity constant;  $E_a$  is the effective activation energy for EM;  $\Omega$  is atomic volume;  $k_B$  is Boltzmann's constant;  $T$  is the temperature;  $e$  is the elementary charge on an electron;  $Z_{eff}^*$  is the effective charge number;  $\rho_{Cu}$  is the resistivity of copper and  $j$  is the current density in the wire;  $B$  is the bulk modulus for the Cu-dielectric system [22].

Note that the nucleation time is related to  $(\sigma_C - \sigma_T)$ , which represents the *effective critical stress*. This difference signifies the threshold value of stress after which a void will nucleate in the wire. We now further elaborate upon the stress-related parameters,  $\sigma_C$  and  $\sigma_T$ .

### 6.2.1 The role of critical stress

In order to model the critical stress, we base our formulation for  $\sigma_C$  using the work in [87], which attributes the reason for void nucleation to the existence of circular flaws present at the copper bulk and  $\text{Si}_3\text{N}_4$  capping layer interface, as illustrated in Fig. 6.2. In the flaw region, the capping layer does not adhere to the copper metal: such a situation can occur during the Cu DD process as a result of a surface defect or contamination during the manufacturing process steps. A typical model assumes the flaw to be circular with radius  $R_f$ , as indicated in the figure.



**Figure 6.2:** Cross-section of Cu DD interconnect showing a circular flaw of radius  $R_f$  leading to void.

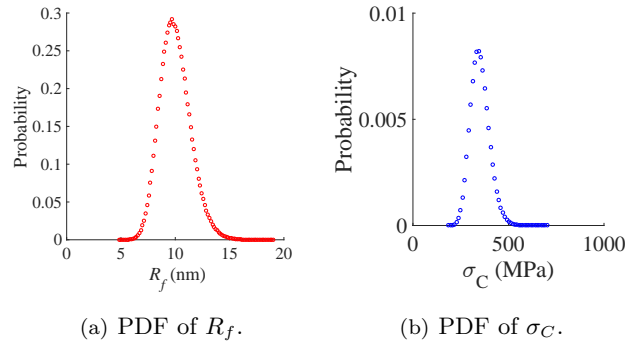
As the stress in the wire increases due to the combination of EM-induced atomic depletion combined with preexisting thermomechanical and package stress, the nucleation of a small void embryo at the flaw location becomes thermodynamically feasible. When the tensile stress in the line crosses the critical stress value, void nucleation becomes feasible. The critical stress value required to achieve this is [87]:

$$\sigma_C = \frac{2\gamma_s \sin \theta_C}{R_f} \quad (6.4)$$

where  $\gamma_s$  is the surface free energy for copper,  $\theta_C$  is the contact angle, defined as the angle which the tangent to the void makes from the horizontal capping surface, chosen as  $90^\circ$  for the circular flaw;  $R_f$  is radius of the circular patch described previously and shown in Fig. 6.2. It should be noted that the flaw size can possibly have multiple values, as indicated in [85]. For a power grid, which can consists of millions of wires, the size of the flaw may vary significantly across the large number of wires, leading to a variation in critical stress according to (6.4). Working backwards from the idea that the TTF for slit voids is experimentally seen to be lognormally distributed [11], it is reasonable for the flaw size distribution to be lognormal.

We set the mean value of  $R_f$  as 10nm, with a standard deviation of 5% of the mean value. Based on these values we simulate the probability distribution of the critical stress,  $\sigma_C$ , which by virtue of being a reciprocal of  $R_f$ , is also lognormally distributed. The PDFs for  $R_f$  and  $\sigma_C$  are shown in Fig 6.3. Notice that the spread in the value of  $\sigma_C$  can be as much as 100 MPa, which can be a potential cause of shift in the time-to-failure for slit void, depending on

the magnitude of other EM-related parameters such as the current density (6.1). Based on the lognormal model for  $R_f$  and the theory for nucleation, we attempt to derive a closed form for nucleation time  $t_n$  while incorporating the variability in  $\sigma_C$  (See Appendix C ). The impact of critical stress variation can be incorporated by using the updated formula (C.1) to determine the lognormal statistics for nucleation time.



**Figure 6.3:** Assumed statistics for  $R_f$  and  $\sigma_C$ .

## 6.2.2 The role of thermomechanical stress

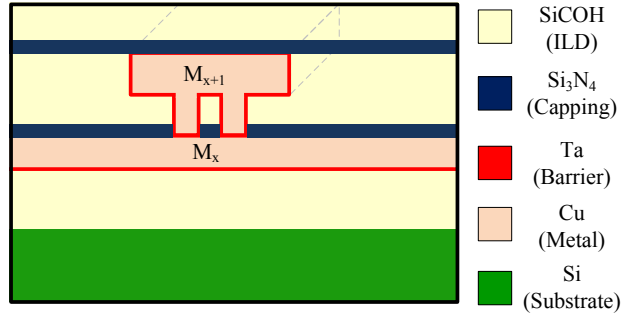
We now elaborate on the thermomechanical stress component,  $\sigma_T$ , in (6.1). The magnitude of this term is determined in our flow based on a model that is built from exact finite element analysis (FEA) of typical Cu DD layout structures encountered in power grids.

One source of thermomechanical stress in interconnects is the mismatch in the CTE of the materials used in the structures used for Cu DD manufacturing. This component is local in nature and depends purely on interconnect geometry. A second component is attributable to the CTE mismatch between underfill, package bump, and the silicon chip causes stresses to develop in the interconnect layers. This stress depends on the relative location of the interconnect and packaging connections and is independent of interconnect geometries. In this work, the package stress is treated as a user-specified input.

The thermomechanical stresses that modulate the tensile and compressive stresses developed within the line during electromigration are computed using the techniques described in Section 6.3. For EM, the hydrostatic stress, defined in (2.8) is of interest [1]. Our FEA evaluates these normal components and computes the hydrostatic stress used to evaluate EM degradation.

## 6.3 Interconnect FEA

We summarize the typical copper dual-damascene structure. The copper interconnect is cladded with Ta barrier layer on the sides and bottom. The top surface is bounded by the  $\text{Si}_3\text{N}_4$  capping layer, while the inter layer dielectric (ILD), made of low-k material such as SiCOH, lies between the copper lines. The whole structure rests on a silicon substrate that has a height of the order of hundreds of microns.



**Figure 6.4:** Cu DD structure simulated in FEA (layers not drawn to scale).

Figure 6.4 shows the structure that we have used to perform FEA simulations to evaluate local thermomechanical stress distributions. We use the ABAQUS [88] finite element package to simulate the copper dual-damascene structure. The material parameters used in this work for thermomechanical stress computations are shown in Table 6.1.

Structure	Material	E (GPa)	$\nu$	CTE (ppm/°C)
Substrate	Silicon	162.0	0.28	3.05
Bulk	Copper	111.6	0.34	17.7
ILD	SiCOH	16.2	0.27	12
Barrier	Ta	185.7	0.342	6.5
Capping	$\text{Si}_3\text{N}_4$	222.8	0.27	3.2

**Table 6.1:** Mechanical properties of materials in Cu DD.

### 6.3.1 Factors affecting thermomechanical stress

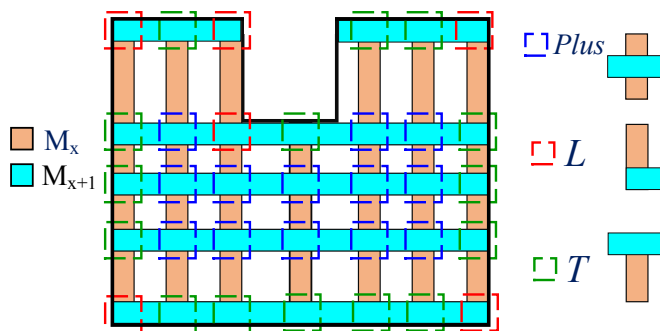
The multi-level Cu DD interconnect structure is fabricated at a high temperature of  $400^\circ\text{C}$  [89], while ICs typically operate at  $100\text{--}125^\circ\text{C}$  in the worst-case. Thus, post manufacturing, due to

the CTE mismatch between the materials, thermomechanical tensile stress develops inside the interconnects and the vias. Due to the close proximity of thermally mismatched materials, the magnitudes of stress depend upon the geometry of the interconnect.

### 6.3.2 Typical topologies in power grid

In VLSI layouts, power grid networks have a two-dimensional mesh-type structure, where horizontal and vertical metal layers often run from one end of the chip boundary to other. Vias or via-arrays are placed at the intersections of the mesh, where the horizontal and vertical wires are connected. The interconnects at the edges of the mesh network boundaries have a larger volume of adjacent ILD than the ones within the boundary, thereby causing differences in the magnitude of thermomechanical stress that they experience. Figure 6.5 illustrates an example two-dimensional power grid mesh. The intersection patterns are of three types, as indicated in the figure.

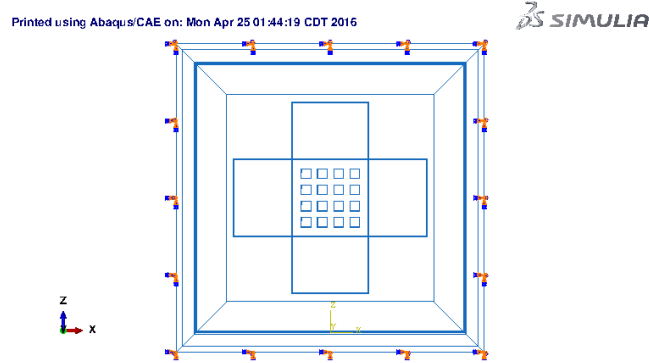
- *Plus-shaped* patterns inside the mesh boundary,
- *T-shaped* patterns at the edges of the mesh, and
- *L-shaped* patterns at the corners of the mesh.



**Figure 6.5:** Typical intersection patterns observed in power grid.

Even identical via array configurations experience different stresses in these three cases due to disparities in the volume and location of surrounding material such as the ILD.





**Figure 6.6:** FEA model snapshot of the plus-shaped structure simulated using ABAQUS.

In the upper layers of the power distribution interconnects, which typically carry the most current and are most susceptible to EM, the typically wire width is significantly larger than the minimum width allowed in a technology. Although interconnect thickness for a specific metal layers is fixed for a given technology, the width and the pitch of the wires could be design-dependent. Since it is prohibitively expensive to run FEA simulations on an entire power grid, we precharacterize a set of two-level interconnect patterns using in FEA, with a lower and upper-level metal layers intersecting orthogonally at the via location, for a specific via array configuration and wire width. Due to space limitations, we focus our discussion on the *plus-shaped* pattern, which is the commonly occurring intersection structure in typical power grids. This structure, where the interconnects run continuously on both sides of a via location, is illustrated in the magnified image from our FEA model in Figure 6.6.

## 6.4 EM in via arrays vs. EM in vias

In our work, we accurately account for the stress-related parameters responsible for EM, in the context of via arrays. In addition, we accurately account for circuit impact arising due to redundancy in via arrays. We will elaborate our methodology in the rest of the section.

### 6.4.1 Characterizing thermal stress

As indicated in the example in Figure 6.1, the use of single vias or via arrays of different dimensions affects the thermomechanical stress,  $\sigma_T$ , and therefore impacts the TTF of the via according to (6.3). Therefore, for accurate TTF characterization, the appropriate stress value, as a function of the via configuration should be used.

We propose a methodology that characterizes the thermomechanical stress in common via

array configurations: for different wire widths, we store the peak tensile thermomechanical stress values underneath the vias as observed from the individual FEA simulations. We perform this analysis for pairs of adjacent layers since our simulations show that the impact of thermomechanical stress is *very local*, the stress at the base of a via connecting two metal layers is not affected by the configuration of a third metal layer. We characterize via structure connecting intermediate and top metal layer configurations, which are the commonly used metal layers for power grid. The total number of characterizations, therefore, must cover:

- $Mx$  and  $Mx+1$  pairs, where  $x$  and  $x+1$  may be either intermediate or top layers (3 combinations: intermediate–intermediate, intermediate–top, and top–top)
- L-shaped, T-shaped, and plus-shaped junctions (3 combinations)
- the number of possible via configurations,  $v_n$
- the number of wire widths  $w_n$

Therefore, the number of FEA simulations required to cover all via configuration is  $9 \times w_n \times v_n$ . While this may sound expensive, it is a one-time characterization for a process technology, similar to standard cell characterization.

*Note that since the TTF scales with the current, is adequate to characterize the TTF for a reference current value. For any other current, the TTF can be scaled using (6.3).*

#### 6.4.2 Electrical redundancy in via arrays

The work in [90] demonstrates an analysis framework to perform statistical analysis of redundant systems such as a clock-mesh by accounting for the impact of current crowding on the TTF distribution for the redundant system. We leverage this to model the redundancy in via arrays. For modeling the time to failure, TTF, of the individual vias in the via array, we use (C.1), which depends on the critical stress, thermomechanical stress, and the current flowing through the via.

The failure criterion of the via relates to the degradation in resistance as successive vias in the array fail. As each via fails, more current is redirected to other vias, potentially reducing their TTF. Figure 6.7(a) shows the variation in resistance as each via in a  $4 \times 4$  array fails. For initial failures, the resistance barely changes and the power grid is not significantly impacted. For subsequent failures, given the inherent resiliency due to redundancy in power grids [13], the power grid may continue to function within its IR-drop specifications.

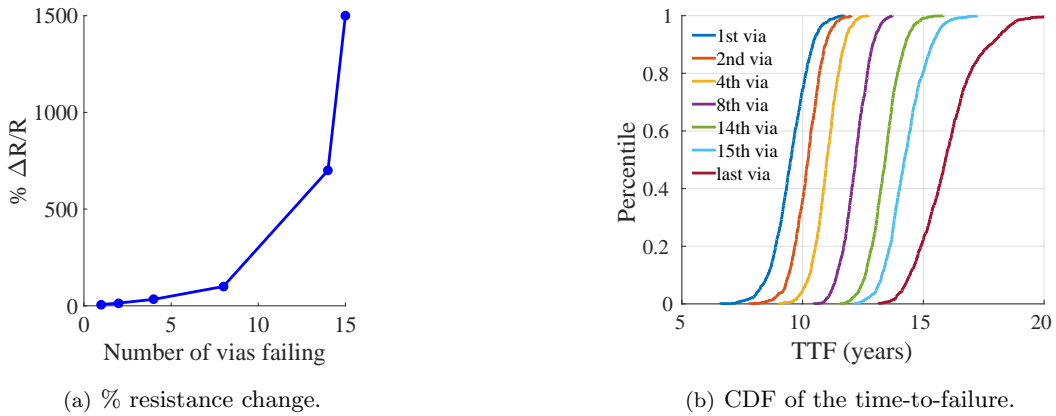
To maintain a simple methodology, we separate the failure of a via array from the system-level power grid failure. We frame the failure criterion for a via array in terms of the allowed percentage shift in the via array resistance. This parameter can be designer-specified. For a

fixed resistance increase criterion, our model calculates an upper bound on the number of vias in the via array whose failure will cause that resistance change, and we will declare the via array as having failed at that point. To be specific, for  $4 \times 4$  via, the failure of 1 results in a 6% resistance change, and the failure of 8 vias will result in a 100% increase. At a specified resistance increase, we will declare the via array as having failed, and analyze the power grid to determine the impact of the change. As stated earlier, the power grid may continue to function within specifications even after a few failures.

### 6.4.3 Via array TTF characterization

We perform statistical simulations to simulate the failure probability of via array under different failure criteria represented by the number of vias, which is given as an input to our via array characterization framework. We perform Monte Carlo simulations corresponding to each sequential failure up to the number of vias required for failure criterion.

We illustrate the characterization process using the example of a  $4 \times 4$  via array in Figure 6.1(a). The 16 vias in via array jointly conduct a total current density of  $4 \times 10^{10} \text{ A/m}^2$ . We plot the distribution of failure time, TTF, which in this work is simply the nucleation time calculated using (C.1) for an operating temperature  $125^\circ\text{C}$ . Figure 6.7(b) shows the CDF of the failure time, TTF, corresponding to different failure criterion based on the number of vias failing.

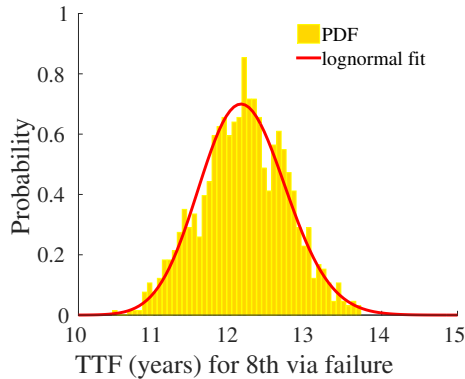


**Figure 6.7:** Failure scenarios in a  $4 \times 4$  via array.

In reality, the vias are likely to fail sequentially [81]. Moreover, with each subsequent failure, the current flow through the vias will redistribute after every failure. Similar to the thermomechanical stress information, the distribution for TTF of the via array, corresponding to a fixed

failure criterion, based on the allowed percentage resistance increase should be passed on to the circuit simulation framework. For convenience, we fit the distribution of TTF of via array to a two parameter lognormal distribution.

Although in this case, it is possible to obtain a good fit for the distribution using a normal distribution, we proceed with a lognormal fit because (a) EM TTFs generally show lognormal behavior (b) the lognormal ensures that any sample of the TTF is always  $> 0$ , but the Gaussian does not guarantee this (c) the fit is clearly seen to be good.



**Figure 6.8:** PDF of failure time for via array corresponding to 8th via fail criterion.

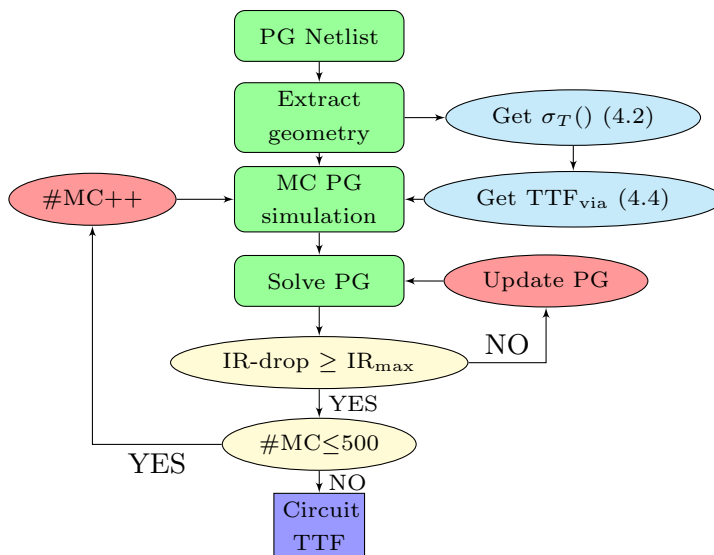
#### 6.4.4 MC simulation methodology

We now describe our power grid simulation work, which uses the characterization steps discussed earlier in this section. Our framework is illustrated using Figure 6.9. The power grid circuit is stored as an SPICE netlist [2] and is passed to our parser developed in C++, which extracts the power grid topological information, such as wire-geometries and occupied metal layers.

This information is given to the ABAQUS FEA engine, along with the choice for the via array configuration, e.g.,  $4 \times 4$ ,  $2 \times 2$ , etc., for estimating the impact of thermomechanical,  $\sigma_T$ . We use our characterization table, which stores the wire information as parameters, and stores the thermomechanical stress value corresponding to the power grid topology.

The choice of via configuration is also passed to the redundancy calculations described in Section 6.4.2, which calculates the distribution for TTF corresponding to the via configuration and the via array failure criterion.

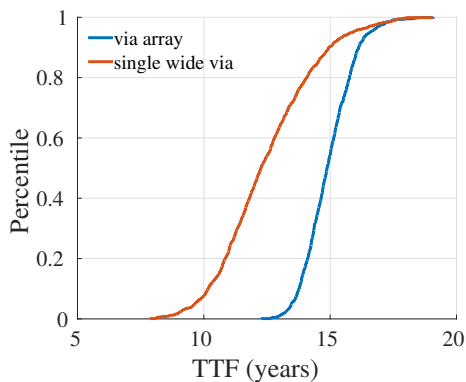
The output of these characterization is passed on to the MC circuit simulation framework which is motivated from the power grid circuit analysis implementation in [90]. This MC engine enables the performance analysis for power grid, by estimating the TTF of power grid, for a given failure criterion chosen as a fraction of the nominal IR-drop.



**Figure 6.9:** Circuit simulation framework for circuit TTF analysis.

## 6.5 Power grid simulation

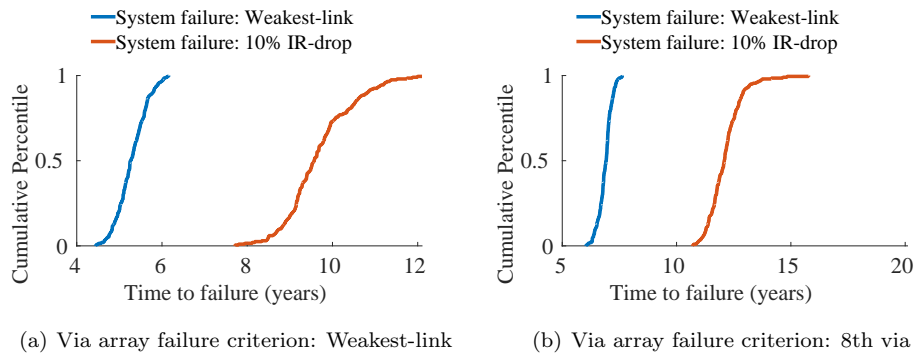
**Via reliability:** For a via array, redundancy is expected to result in longer lifetimes. We can quantify the impact of via redundancy by comparing the failure time corresponding to via array with that of a single wide via, under similar conditions of current stress. Figure 6.10 compares the TTF for the open-circuit failure criterion for the two scenarios. From the figure it can be seen that the lumped approximation will result in TTF which can be significantly pessimistic as compared to the realistic situation with via arrays.



**Figure 6.10:** TTF comparison: single via vs. redundant via array.

**Circuit reliability:** We will now discuss the results of MC circuit simulation for one of the power grid benchmarks PG1. Note that we have modified the power grid wire geometry and tuned the via resistances to obtain a reasonable IR-drop. For PG1, we assume that  $4 \times 4$  via arrays are used, and we fix the performance failure criterion as an IR-drop specification of 10% of  $V_{dd}$ . We observed that to achieve this drop criterion, contrary to the weakest-link that allows only one via array failure, more than one via array could fail and the circuit could continue to meet the IR-drop specifications, due to the inherent resiliency of power meshes.

In order to quantify the role of redundancy due to via arrays, we also perform simulations corresponding to a relaxed failure criterion for the via array. As stated earlier, this is said to occur when the 8th via in the array fails. In Figure 6.11, we compare two scenarios: first, when the via array is said to fail at the first via failure (weakest-link), shown in Figure 6.11(a), and second, when we use the 8th via failure criterion for the via array, shown in Figure 6.11(b). Under each assumption, we have two curves, which indicate the CDF of the TTF for two scenarios: the first curve corresponds to the situation when the circuit is said to fail at the first via array fail (weakest-link), and the second curve corresponds to failing the IR-drop specification.



**Figure 6.11:** TTF for PG1 for various choices of via array failure criteria.

Notice that for the circuit performance failure criterion (10% of IR-drop), the median time to failure increases from about 9.6 years to 12.1 years for the circuit under the relaxed via array failure criterion. This simulation shows the direct benefit of modeling vias as via arrays that have redundant conducting elements, in contrast to modeling them as single conducting elements, as done in prior power grid analysis works. While it may seem clear that a via array cannot fail when its first via fails, this may not seem obvious to a typical EM methodology, which does not recognize that redundant vias should be clubbed together as a single unit. Therefore, we claim that the notion of treating a via array as a single unit, with its own characterized TTF, can provide significantly better estimates of the circuit TTF.

## Chapter 7

# Conclusion

The thesis develops an approach for EM analysis of circuits accounting for the effects neglected in past works. The methodology utilizes physics-based models to circuit analysis of the large number of IC interconnects using a probabilistic analytic model that is both computationally efficient, and accounts for material, electrical, and environmental parameters that affect EM.

We capture the physics of EM for both types of on-chip wires, those that carry DC currents, such as the wires in power grids, and those that carry AC currents, such as signal wires. For power grids the analysis shows that the power grid has inherent resilience to EM failures due to structural redundancies. Using our circuit simulation approach on a set of industrial circuit benchmarks, we demonstrate the inherent robustness of power grids, which maintain supply integrity even under multiple EM failures.

For signal wires, it is demonstrated that in contrast to assuming EM as a catastrophic failure, the impact of EM on performance parameters can be directly calculated. It is observed that the variation in performance parameters, such as delay, are both technology- and circuit-dependent. We demonstrate that the magnitude of EM-induced performance degradation depends upon the amount of EM recovery, and we evaluate the performance for various scenarios of recovery, and for various advanced technology nodes.

We develop new methods that evaluate the transient evolution of stress in interconnects incorporating the role of EM-induced back-stress. Through accurate and efficient analysis of the parameters related to stress, the framework presented in this thesis can help to predict EM mortal wires accurately by directly accounting for material parameters, as well as product lifetime context. Lastly, we have demonstrated a methodology to analyze performance of power grids in the context of via arrays. Our analysis shows that the important parameters which determine EM performance degradation, such as thermomechanical stress and the electrical redundancy are function of the via array configuration.

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## Appendix A

# Derivation of the finite and semi-infinite solution in [1]

The atomic flux due to electric field and back-stress can be written as follows:

- Flux due to the electron wind

$$\frac{C_a D_{eff}}{k_B T} e Z_{eff}^* E$$

- Flux due to back-stress

$$\frac{C_a D_{eff}}{k_B T} \Omega \frac{d\sigma}{dx}$$

Here,  $C_a$  is the atomic concentration, which has been previously denoted by  $N$  in the thesis. Here, the new notation is chosen to align with the notation used in the [1]. The net atomic flux can be written as

$$J_a = -\frac{C_a D_{eff}}{k_B T} \left( e Z_{eff}^* E + \Omega \frac{d\sigma}{dx} \right) \quad (\text{A.1})$$

Consider a small elemental volume in the cross section within the interconnect, the number of atoms entering the volume in time  $dt$ , are  $\text{div } J_a dt$ . These atoms either change the vacancy concentration  $C_v$ , and/or get deposited in the grain boundaries, thereby changing the number of atomic sites per unit volume  $C$ . Therefore, using the continuity equation, we have

$$\begin{aligned} -\text{div}(J_a)dt &= dC_v - dC \\ -\frac{\partial J_a}{\partial x} &= \frac{\partial C_v}{\partial t} + \frac{\partial C}{\partial t} \\ \text{Now use, } B &= -\frac{dC}{C} \\ \implies -\frac{\partial J_a}{\partial x} &= \frac{\partial C_v}{\partial t} + \frac{C}{B} \frac{\partial \sigma}{\partial t} \end{aligned} \quad (\text{A.2})$$

According to [1], the vacancies are in equilibrium with the stress, and under this assumption the vacancy concentration  $C_v$  can be written as

$$C_v = C_{v_0} \exp\left(\frac{\Omega \sigma}{k_B T}\right)$$

$$\implies \frac{\partial C_v}{\partial t} = \frac{\Omega C_{v_0}}{k_B T} \exp\left(\frac{\Omega \sigma}{k_B T}\right) \frac{\partial \sigma}{\partial t}$$

Combining these, we obtain  $\frac{\partial C_v}{\partial t} = \frac{\Omega C_v}{k_B T} \frac{\partial \sigma}{\partial t}$

Substitute the expression above in (A.2)

$$\frac{\partial J_a}{\partial x} = \frac{C}{B} \left( \frac{\Omega B}{k_B T} \frac{C_v}{C} + 1 \right) \frac{\partial \sigma}{\partial t} \quad (\text{A.3})$$

Again, using the assumptions (See [1] for details.)

$$\frac{C_v}{C} \ll \frac{B \Omega}{k_B T}$$

$$\implies \frac{C_v B \Omega}{C k_B T} \ll 1$$

$$\implies -\frac{\partial J_a}{\partial x} = \frac{C}{B} \frac{\partial \sigma}{\partial t} \quad (\text{A.4})$$

Now, let's evaluate  $-\frac{\partial J_a}{\partial x}$  by differentiating (A.1), with respect to  $x$  and use the identity  $C_a = C = \frac{1}{\Omega}$ . We obtain

$$-\frac{\partial J_a}{\partial x} = \frac{\partial}{\partial x} \left[ \frac{D_{eff}}{k_B T} \left( \frac{e Z_{eff}^* E}{\Omega} + \frac{\partial \sigma}{\partial x} \right) \right] \quad (\text{A.5})$$

Using the fact that the L.H.S is same for (A.5) and (A.4), and applying the substitutions:  $C = \frac{1}{\Omega}$ ,  $G = \frac{e Z_{eff}^* E}{\Omega}$ , and  $\kappa = \frac{D_{eff} B \Omega}{k_B T}$ , we have

$$\implies \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[ \kappa \left( \frac{\partial \sigma}{\partial x} + G \right) \right] \quad (\text{A.6})$$

### Solution for the semi-infinite line

Assuming that initially the stress in the line is zero. For the semi-infinite line, (A.6) needs to be solved with the zero flux boundary condition, that can be written as

$$\frac{\partial \sigma}{\partial x} = -G \text{ at } x = 0 \text{ for all time } t$$

Let's propose a new variable  $f = \frac{\partial \sigma}{\partial x}$ . Now,  $f$  satisfies the partial differential equation (PDE) (A.6). Substituting  $f$  and rewriting (A.6)

$$\frac{\partial f}{\partial t} = \kappa \frac{\partial^2 f}{\partial x^2} \quad (\text{A.7})$$

The solution of (A.7) with the boundary condition  $f = -G$  at  $x = 0$  is discussed in [91], and can be written as

$$f = G \operatorname{erfc}\left(\frac{x}{2\sqrt{\kappa t}}\right) \text{ where } \operatorname{erfc}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} dt$$

Now, substitute  $f = \frac{\partial\sigma}{\partial x}$ , we have

$$\begin{aligned} \frac{\partial\sigma}{\partial x} = G \operatorname{erfc}\left(\frac{x}{2\sqrt{\kappa t}}\right) &\implies \int_\sigma^0 \frac{\partial\sigma}{\partial x} = G \int_x^\infty \operatorname{erfc}\left(\frac{x}{2\sqrt{\kappa t}}\right) dx \\ \sigma = 2G \left[ \sqrt{\frac{\kappa t}{\pi}} \exp\left(\frac{-x^2}{4\kappa t}\right) - \frac{x}{2} \operatorname{erfc}\left(\frac{x}{2\sqrt{\kappa t}}\right) \right] &\quad (\text{A.8}) \end{aligned}$$

This is the same form as described in [1].

### Solution for the finite line case

For the finite line, the zero flux boundary condition transforms to

$$\frac{\partial\sigma}{\partial x} = -G \text{ at } x = 0, x = L \quad (\text{A.9})$$

Let  $f = \frac{\partial\sigma}{\partial x} + G$ , then  $f$  also satisfies the PDE (A.6). We will proceed by using the variable separable technique [91]. Let the solution be  $f = X(x) T(t)$

Since,  $f$  satisfies (A.6), we have

$$\begin{aligned} X(x) \dot{T}(t) &= \kappa X''(x) T(t) \\ \implies \frac{1}{\kappa} \frac{T'(t)}{T(t)} &= \frac{X''}{X(x)} = \phi \\ \implies T' - \kappa \phi T &= 0 \\ \text{and } X'' + \phi X &= 0 \end{aligned}$$

The following solution satisfy the above equations

$$\begin{aligned} X(x) &= [A \sin \lambda x + B \cos \lambda x] \\ T(t) &= C \exp(-\lambda^2 \kappa t) \end{aligned}$$

and  $f$  can be written as

$$f = [A \sin \lambda x + B \cos \lambda x] C \exp(-\lambda^2 \kappa t)$$

Now we apply the boundary conditions given in (A.9), after using  $f = \frac{\partial \sigma}{\partial x} + G$ . We have,  $f(0, t) = 0 \implies B = 0$  and  $f(L, t) = 0 \implies \lambda L = n\pi$ . The general solution can be written as

$$f = \sum_n A_n \exp\left(\left(\frac{-n\pi}{L}\right)^2 \kappa t\right) \sin\left(\frac{n\pi x}{L}\right) \quad (\text{A.10})$$

To find  $A_n$ , we can use the equality

$$\int_0^1 \sin(n\pi x) \sin(m\pi x) dx = \begin{cases} 0 & \text{when } m \neq n \\ \frac{1}{2} & \text{when } m = n \end{cases}$$

$$\implies A_m = \begin{cases} \frac{4G}{m\pi} & \text{when } m = 2n + 1 \\ \frac{1}{2} & \text{when } m = 2n \end{cases}$$

$$A_m = \frac{4G}{m_n} \text{ where } m_n = (2n + 1)\pi$$

$$\begin{aligned} f &= \sum_n \frac{4G}{m_n} \exp\left(\left(\frac{-n\pi}{L}\right)^2 \kappa t\right) \sin\left(\frac{n\pi x}{L}\right) \\ \frac{1}{L} \frac{\partial \sigma}{\partial \xi} + G &= \sum_n \frac{4G}{m_n} \exp(-m_n^2 \tau) \sin(m_n \xi) \text{ where } \xi = \frac{x}{L} \\ \implies \int \frac{1}{L} \frac{\partial \sigma}{\partial \xi} + G &= \int \sum_n \frac{4G}{m_n} \exp(-m_n^2 \tau) \sin(m_n \xi) + \text{const.} \\ \implies \frac{\sigma}{L} + G \xi &= -\frac{4G}{m_n} \sum_n \exp(-m_n^2 \tau) \frac{\cos(m_n \xi)}{m_n} + \text{const.} \end{aligned}$$

At steady state,  $\frac{\partial \sigma}{\partial t} = 0$ . Using this in (A.6), we can obtain  $\frac{\partial \sigma}{\partial x} + G = 0$ , which indicates that the stress profile along the wire is linear (this is essentially another way to derive the Blech criterion). In this scenario, the stress can be written as

$$\sigma = G L \left(\frac{1}{2} - \xi\right) \implies \text{const.} = G L \left(\frac{1}{2} - \xi\right) + G \xi \implies \text{const.} = \frac{G L}{2} \quad (\text{A.11})$$

$$\sigma = G L \left(\frac{1}{2} - \xi - \frac{4}{m_n^2} \sum_n \exp(-m_n^2 \tau) \frac{\cos(m_n \xi)}{m_n}\right) \quad (\text{A.12})$$

This is the solution for the finite line described in [1].

## Appendix B

# Derivation of resistance change for slit void growth

In order to derive a closed form solution for the resistance increase of the slit void, we assume that the region of the via subtended by the slit-void becomes non-conducting. Thus, for a slit-void of length,  $L_{void}$ , as shown in Fig. B.1(a), we assume that only the trapezoidal region of the via conducts the current, and we attempt to derive the effective resistance of the trapezoidal via in order to capture the resistance increase  $\Delta R$ . Prior works suggest that the slit void is nucleated typically near the via corners [27]. Therefore, we assume that a slit void is formed at the via-corner and expands in the direction of electron flow from left to right. Notice that by symmetry argument, a slit void nucleation at the right corner will also result in same scenario. For the right-angled triangle with the base of length,  $L_{void}$ , in Fig. B.1(a), we have:

$$\begin{aligned}\frac{z}{L_{void}} &= \frac{H_{via} - y}{H_{via}} \text{ and } x = L_{via} - z \\ \implies x &= L_{via} - L_{void}\left(1 - \frac{y}{H_{via}}\right) \\ \implies x &= L_{via} - L_{void} + \frac{yL_{void}}{H_{via}}\end{aligned}$$

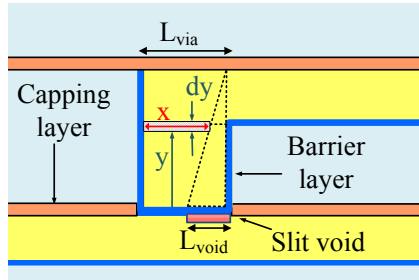
Resistance change  $dR$  for an element rectangular strip of thickness  $dy$  (as shown in the figure) can be written as:

$$\begin{aligned}dR &= \frac{\rho dy}{Wx} \\ \implies dR &= \frac{\rho dy}{W\left(\left(y\frac{L_{void}}{H_{via}}\right) + L_{via} - L_{void}\right)}\end{aligned}$$

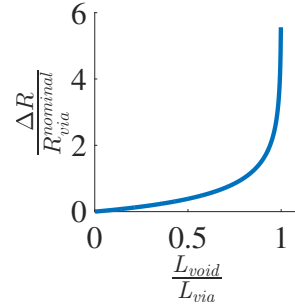
Assuming  $A = \frac{L_{void}}{H_{via}}$  and  $B = L_{via} - L_{void}$ , we have:

$$\begin{aligned}
\Rightarrow dR &= \frac{\frac{\rho}{W} dy}{Ay + B} \\
\Rightarrow \int dR &= \frac{\rho}{W} \int_0^{H_{via}} \frac{\rho dy}{Ay + B} \\
\Rightarrow R_{new} &= \frac{\rho}{WA} \log(Ay + B) \Big|_0^{H_{via}} \\
\Rightarrow R_{new} &= \frac{\rho}{WA} \log(AH_{via} + B) - \log(B) \\
\Rightarrow R_{new} &= \frac{\rho H_{via}}{W L_{void}} \log\left(\frac{L_{via}}{L_{via} - L_{void}}\right) \\
\Rightarrow \Delta R &= R_{new} - \frac{\rho H_{via}}{W L_{via}} \\
\Rightarrow \Delta R &= \frac{\rho H_{via}}{W} \left( \frac{1}{L_{void}} \log\left(\frac{L_{via}}{L_{via} - L_{void}}\right) - \frac{1}{L_{via}} \right) \tag{B.1}
\end{aligned}$$

We use (B.1) to evaluate the resistance increase,  $\Delta R$  for the via, as a function of void length,  $L_{void}$ . The process parameters used for this simulation are:  $H_{via} = 2\mu\text{m}$ ;  $L_{via} = 70\text{nm}$ ;  $\rho = 2.25 \times 10^{-8}\text{Ohm-m}$ . Figure B.1(b), plots the resistance increase normalized by the nominal via resistance,  $R_{via}^{nominal}$ , for various values of void length,  $L_{void}$  normalized by  $L_{via}$ .



(a) Derivation for resistance change for slit voids.



(b) Via-resistance increase relative to void growth for slit void.

**Figure B.1:** Slit void growth.

## Appendix C

# Nucleation time for lognormally varying flaw size

Rewriting (6.1) by expanding the  $(\sigma_C - \sigma_T)^2$  term we have  $t_n = C_{t_n} T$ , where  $T = \frac{((\sigma_C^2 + \sigma_T^2 - 2\sigma_C\sigma_T))}{D_{eff}}$ .

If  $\sigma_C \sim \text{LogN}(\mu_{\sigma_C}, \sigma_{\sigma_C})$ , each term in  $T$  is a lognormal:

$$\begin{aligned} \frac{\sigma_C^2}{D_{eff}} &: \text{LogN}(2\mu_{\sigma_C} - \mu_{D_{eff}}, \sqrt{4\sigma_{\sigma_C}^2 + \sigma_{D_{eff}}^2}) \\ \frac{\sigma_T^2}{D_{eff}} &: \text{LogN}(2 \log \sigma_T - \mu_{D_{eff}}, \sigma_{D_{eff}}) \\ 2\sigma_T \frac{\sigma_C}{D_{eff}} &: \text{LogN}(\log(2\sigma_T) + \mu_{\sigma_C} - \mu_{D_{eff}}, \sqrt{\sigma_{D_{eff}}^2 + \sigma_{\sigma_C}^2}) \end{aligned}$$

This can be rewritten in a compact, parametric form:

$$\frac{\sigma_C^2}{D_{eff}} : \text{LogN}(\mu_1, \sigma_1); \quad \frac{\sigma_T^2}{D_{eff}} : \text{LogN}(\mu_2, \sigma_2); \quad \frac{\sigma_C}{D_{eff}} : \text{LogN}(\mu_3, \sigma_3);$$

Now,  $T$  is an algebraic sum of three lognormals, and we can use an approach similar to [13] to approximate  $T$  as a lognormal.

$$\begin{aligned} u_1 &= e^{(\mu_1 + \frac{\sigma_1^2}{2})} + e^{(\mu_2 + \frac{\sigma_2^2}{2})} - e^{(\mu_3 + \frac{\sigma_3^2}{2})} \\ u_2 &= e^{(2\mu_1 + 2\sigma_1^2)} + e^{(2\mu_2 + 2\sigma_2^2)} + e^{(2\mu_3 + 2\sigma_3^2)} + 2e^{(\mu_1 + \mu_2 + \frac{\sigma_1^2 + 2\sigma_2^2}{2})} \\ &\quad - 2e^{(\mu_2 + \mu_3 + \frac{\sigma_2^2 + 2\sigma_3^2}{2})} - 2e^{(\mu_1 + \mu_3 + \frac{\sigma_1^2 + 2\sigma_3^2}{2})} \\ (\mu_T, \sigma_T^2) &= (2 \log(u_1) - \log(u_2))/2, \log(u_2) - 2 \log(u_1) \end{aligned}$$

Thus, the nucleation time incorporating critical stress,  $t_n = C_{t_n} T$ , will also be a lognormal random variable and can be written as:

$$\text{New } t_n : \text{LogN}(\log C_{t_n} + \mu_T, \sigma_T) \tag{C.1}$$