

Characterization and Loss Modeling of Silicon Carbide Based Power Electronic Converters

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Dedication

To My Parents.

Abstract

Silicon Carbide (SiC) based power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are great candidates for high-voltage, high-frequency and high-temperature power switching applications because of their favorable material properties when compared with Silicon (Si) power MOSFETs. In this thesis, the design, characterization, and modeling of a power electronic converter based around SiC MOSFETs is investigated. The test converter circuit is designed to be general enough that it can represent a half bridge converter, a DC chopper circuit or an output phase of an inverter for flexibility in testing. A practical characterization procedure is proposed which takes a circuit-level approach, as opposed to a device-level approach, using only the actual power electronic circuit under study and no additional test circuitry. Therefore this study takes into account the inherent parasitic impedances associated with the test circuit and its influence on the SiC devices' high-speed switching behavior. The hardware setup is operated at frequencies up to 200 kHz and efficiencies up to approximately 99% were recorded.

Based on the characterization data and analysis, a model is constructed using MATLAB (a mathematical modeling software) for predicting converter and gate driver losses at different load currents, DC bus voltages, and operating temperatures (for both a DC-DC synchronous buck converter and a DC-AC three phase, two-level Voltage Source Inverter). Good agreements are obtained between the model outputs and experimental results. Possible future extensions to the work are discussed.

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Chapter 1

Introduction

1.1 Evolution of Semiconductor Materials

Power Electronics is an integral part of several systems in areas of industrial automation, renewable energy technology and automotive drives. Silicon has been the primary material used in fabrication of power semiconductor devices since their commercial introduction in the late 1900s. This can be attributed to the development of fabrication techniques that allow Si to be grown in a single crystal form with larger diameters and greater purity of any available semiconductor [5]. Present day power converter applications have brought about a pressing need for high temperature, high frequency and power-dense semiconductor devices. The fundamental limitations of Si based power devices make them unsuitable to meet these demands. Research and development in semiconductor physics show that wide band gap semiconductor materials including Silicon Carbide (SiC) and Gallium Nitride (GaN) are the solution to current and future needs of the power industry [3], [8]-[10].

1.2 Wide Band Gap Semiconductors

Wide Band Gap (WBG) semiconductor materials, as the name suggests, have a larger energy gap when compared with Silicon. This translates to a host of desirable features: lower leakage currents with higher operating temperatures; higher breakdown field

strength, higher electron saturation velocity, which leads to faster turn-on and turn-off transitions; and higher thermal conductivity. The material properties of Si, SiC and GaN are summarized in Table 1-1 below.

Property	Si	6H-SiC	GaN
Bandgap at 300 K (eV)	1.12	2.9	3.4
Relative dielectric constant	11.8	10	9.5
Saturated drift velocity (cm/s)	1×10^7	2.5×10^7	2.5×10^7
Thermal conductivity (W/cm °C)	1.5	5	1.3
Melting temperature (°C)	1415	>2200	2500
Breakdown electric field (V/cm)	3×10^5	4×10^6	3.5×10^6

Table 1-1: Material Properties of Semiconductor Materials [5], [31]

As seen from above, SiC offers a critical electric field of 4.0×10^6 V/cm – an order of magnitude higher than Si. This allows an increase in the blocking capability of SiC power devices and also allows them to be fabricated with much thinner and higher doped drift layers, significantly reducing the on-state resistance [11]. The high thermal conductivity of SiC (5 W/cm°C) enhances heat dissipation and coupled with the wide band gap energy (2.9 eV) allows high-temperature operation above 300 °C. All of these above advantages make SiC power devices an ideal substitution for Si counterparts in future high-voltage and high-power converter systems [34]-[37].

In the last couple of years, several SiC WBG devices have been commercialized [6], [7].

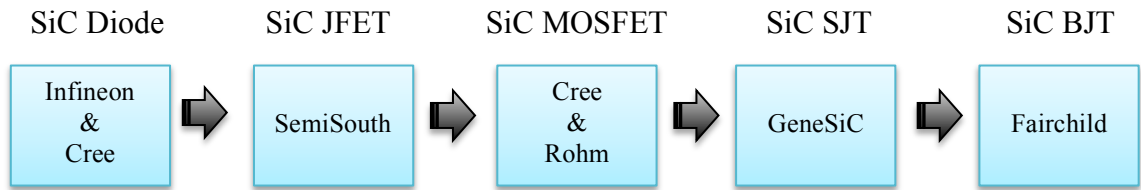


Figure 1-1: SiC Power Devices Evolution

GaN WBG devices are nearing commercial readiness, with professional samples already available [3], [8]–[10]. Figure 1-1 shows the commercialization of SiC devices in the power market over the last few years.

Measurement of WBG device parameters has been widely considered by researchers, for example [1], [9]–[13]. The potential impact of these devices in power electronic circuits has also been widely considered, such as in [1], [4], [12]–[15] where it has been shown that WBG devices can lead to more compact and efficient power electronic converter designs as a direct result of their material properties.

1.3 Power MOSFET

MOSFETs are commonly used in high frequency applications due to their superior switching performance over BJT, IGBT, thyristor, etc [5]. They need lower gate drive power, and they have faster switching time, no secondary breakdown, stable gain and response time over a wide temperature range. Several power MOSFET structures have been explored since the 1970s. Most power MOSFETs have a vertical structure with source and drain on opposite sides of the wafer in order to support higher current and voltage. The first high-voltage power MOSFET structure was developed by using a V-

groove (V-MOSFET) etching process during the 1970s. Then, during the late 1980s, the technology for etching trenches in silicon became available and this process was adopted by the power semiconductor industry to develop the trench-gate or U-MOSFET structure. Another widely used structure is the vertical D-MOSFET, which uses a double-diffusion process [19]. This work utilizes SiC-based power D-MOSFETs as the primary switching power device (test device details to be discussed in Chapter 2). This section summarizes the D-MOSFET structure for better understanding of the device under consideration.

A cross-section of the basic cell structure for the D-MOSFET structure is illustrated in Figure 1-2. The device is fabricated by starting with an N-type epitaxial layer grown on a heavily doped N+ substrate. The channel is formed by the difference in lateral extension of the P-base and N+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left and right of the gate region during ion-implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures.

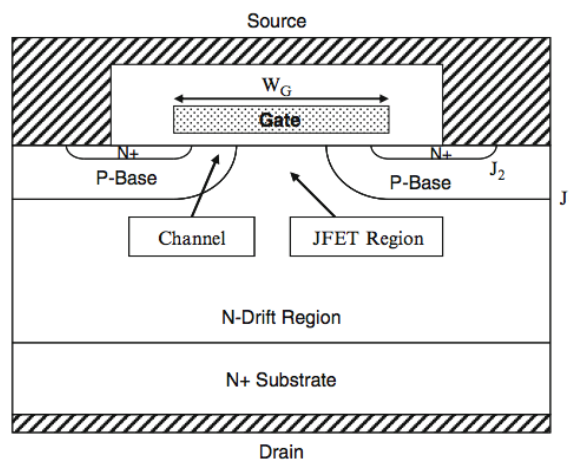


Figure 1-2: D-MOSFET Structure

Without the application of a gate bias, a high voltage can be supported in the D-MOSFET structure when a positive bias is applied to the drain. In this case, junction J1 formed between the P-Base region and the N-drift region becomes reverse biased. The voltage is supported mainly within the lightly doped N-drift region. Drain current flow in the D-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. This inversion layer channel provides a path for transport of electrons from the source to the drain when a positive drain voltage is applied.

After transport from the source region through the channel, the electrons enter the N-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent P-base regions within the D-MOSFET structure. The constriction of the current flow through the JFET region substantially increases the internal resistance of the D-MOSFET structure. A careful optimization of the gate width is required, in order to minimize the internal resistance for this structure. [19]

1.4 Thesis Objectives

This MS thesis project aims to develop a simplified and accurate circuit model for power electronic circuits (specifically a DC-DC synchronous buck converter and a DC-AC three phase, two-level VSI) incorporating SiC MOSFETs that can be used for real world simulations. In a switching power converter application, an increase in the switching speed and power level of the converter causes the parasitic impedances of the interconnections and the circuit layout to affect the efficiency and waveforms of the

system. This thesis will investigate device characteristics taking into consideration the circuit parasitic impedances and its effect on device behavior and circuit operation.

The primary objective is to build a MATLAB-based model of a working SiC power electronic converter, which can be used to simulate the operation of the same with accuracy. A highly general SiC-based converter is designed and used as a test circuit. The test circuit is then subjected to a characterization procedure over a wide range of operating conditions that allows for device and circuit parameters to be studied and their dependencies extracted for constructing the circuit model. The model is then designed to predict power loss and thermal behavior of the test circuit in question. Finally, the model's output data is validated against experimental results at various operating points.

1.5 Thesis Organization

Based on the above objectives, the thesis is thus organized as follows:

Chapter 2 describes the idea behind the SiC based test converter design along with a detailed description of the components used in the design and their selection procedure. Chapter 3 expands on the converter model delving into details of the modeling procedure for power and gate drive circuits. Chapter 4 presents an extensive characterization procedure conducted on the test converter. Based on the characterization data different device parameters required by the model are extracted and presented. In Chapter 5 the model results are validated with comparisons to actual hardware test data. It also summarizes the research work and provides suggestions on future improvements to this work.

Chapter 2

Test Converter

2.1 Introduction

Power electronics circuits involving WBG devices need to take into consideration the effects of parasitic inductances in the power device as well as the circuit layout. Specific importance needs to be attributed to switching conditions where device voltage overshoots can be a concern, as well as EMI considerations. This chapter describes the test converter circuit, design considerations and delves into a detailed discussion of the selection procedure of circuit elements: power device and gate drive components [28].

Incorporating SiC technology into power electronics systems allows for combination of fast switching speed of Si MOSFETs with the low conduction loss of Si IGBTs at blocking voltages of 1200V and higher. The key to making use of these advantages, especially the faster switching speed, requires paying careful attention to system and device parasitics; specifically stray inductances. The effects of parasitic impedances can include voltage and current overshoots and ringing. These parasitics have always existed and are a natural consequence of the device physics and packaging involved. However, the combination of high voltage, high current and increased switching speed of SiC MOSFETs requires careful consideration of the circuit layout to reduce the effects of these parasitics. Another important design consideration is to keep in mind that faster

switching speed at high voltages and currents give rise to higher dV/dt and dI/dt device stresses [28].

2.2 Power Circuit

During the design phase of this project, the following SiC power MOSFETs, with similar device ratings, were commercially available:

1. *Rohm Semiconductors* SCH2080KE
2. *Cree* CMF20120D

The following table (Table 2-1) shows the device ratings for both devices:

Parameter	Rohm SCH2080KE	Cree CMF20120D
$R_{DS,ON}$ (m Ω)	80	80
V_{DSS} (V)	1200	1200
I_D (A) at 25°C	40	42
T_j (°C)	175	135
V_{GSS} (V)	-6/22	-5/25
Integrated with SiC SBD	Yes	No
Q_{rr} (nC)	60 (SiC SBD)	142 (SiC body PiN)
Package	TO-247	TO-247

Table 2-1: Device Rating Comparison [6],[7]

Like other power MOSFETs, the SiC devices also have an intrinsic body diode. The body diode is a SiC PiN diode that has an on-state voltage drop much higher when compared to

a Si MOSFET's body diode. Use of this diode is not recommended due to its high forward drop. An external SiC Schottky diode is suggested, to bypass the intrinsic body diode of the SiC MOSFET [27].

From Table 2-1 above, it is concluded that the SCH2080KE [7], manufactured by Rohm Semiconductors is a suitable option for the test converter due to its co-packaged SiC Schottky Body Diode (SBD) within the TO-247 package. This allows for a more compact circuit design. It is important to note that the manufacturer recommends a negative gate bias for faster turn-off.

In this work, the simple power electronic circuit shown in Figure 2-1 is designed and constructed. This circuit is general enough that it could represent a half-bridge converter, one output phase of a two-level inverter, or a part of a multilevel inverter. This allows flexibility in circuit configuration (for example, stacking several test circuits on bus bars) for future testing.

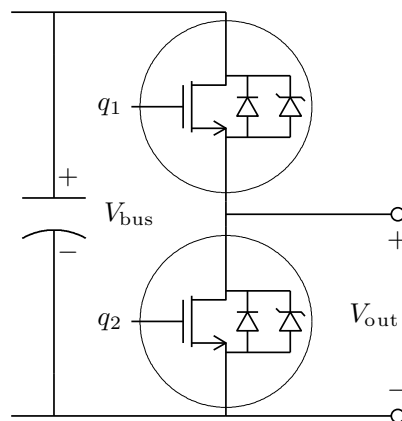


Figure 2-1: Test Converter Schematic

For a robust power circuit design, the layout planning should begin during initial system block diagram phase. This leads to a systematic and intelligent partitioning of various system blocks. A good layout adds little or no additional parasitics to that already existing within the power device. The test circuit is designed and laid out bearing these considerations in mind. In order to achieve fast switching with minimum oscillations, the gate drive connections need to minimize parasitic inductances: this requires the gate driver to be located as close as possible to the MOSFET gate [27]. For this reason, the MOSFETs along with their gate drive circuit are laid out on a single PCB. The back pad of the SCH2080KE is electrically connected to its Drain terminal. An electrically isolating Sil-Pad is placed between the switch and the heat sink to prevent physical contact. The Sil-Pad has good thermal properties to facilitate heat transfer.

The converter PCB is designed with four layers having distinct signal ground polygons separated by an earth ground plane for shielding. A $2.2\mu\text{F}$ capacitor is placed across the DC bus in close proximity to both MOSFETs to provide relief during transient states. In addition to this, the test set-up uses an external DC bus capacitor bank of six $75\mu\text{F}$ film capacitors in parallel. Each of these capacitors has a low Equivalent Series Inductance (ESL) of 38 nH and Equivalent Series Resistance (ESR) of 2.1 m Ω . This arrangement keeps the power losses occurring in the capacitor bank negligible, which allows for the same to be overlooked while developing the MATLAB loss model. The converter and the external capacitor bank are mounted on bus bars to minimize the DC bus inductance, as shown in Figure 2-2.[2]

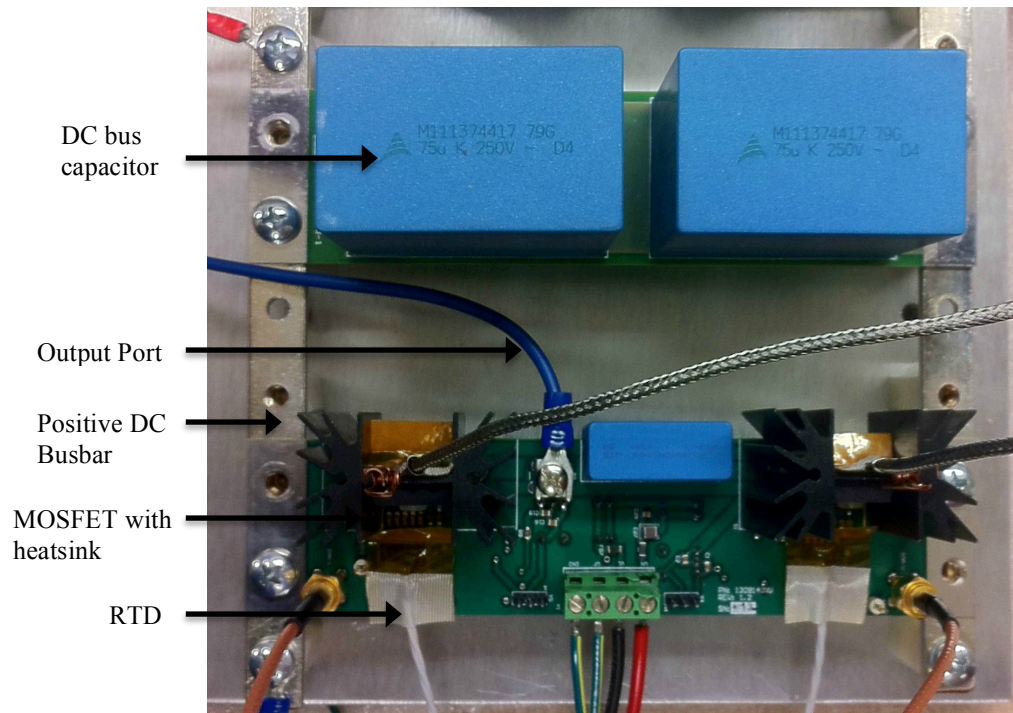


Figure 2-2: Test Converter Hardware Setup

2.3 Gate Driver Design

The gate drive requirements of a SiC MOSFET is much more demanding when compared to a Si MOSFET. The lower carrier mobility in SiC, in spite of their lower drift layer resistance, means that their channel resistance is higher. For this reason, the higher the gate voltage, V_{GS} , the lower the on-resistance, $R_{DS,ON}$. Resistance becomes progressively saturated, as V_{GS} gets higher than 20V. A typical Si MOSFET gate driver uses a MOSFET gate turn-on voltage of $\sim +10$ V and turn-off voltage of 0 V [5], whereas best practice for SiC devices typically requires a gate turn-on voltage in the range of 15 – 22 V and a turn-off voltage of approximately -5 V to minimize the switching and conduction losses. [7] recommends driving the SiC SCH2080KE with a V_{GS} set to 18V

for turn on and -5V for turn off. Unfortunately, the commercial availability of gate-drivers that can supply these voltages is extremely limited.

The design for the gate driver used in this project is based on [20], where a low-side MOSFET gate driver [21] with a wide input voltage range is supplied by isolated DC-DC converters biased by the MOSFET source voltage, see Figure 2-3. These converters are inexpensive with an isolation voltage rating of 5.2kV and also have very low isolation capacitance. The logic input is isolated using an opto-isolator. With this connection scheme, V_{CC} determines the gate pulse positive voltage and $-V_{EE}$ determines the negative gate pulse voltage. The $-V_{EE}$ node is used as the ground reference for the gate driver and a digital isolator for the gate signals. The gate supply voltage values were chosen as the manufacturer-recommended values. Operation of the gate driver is as follows: a high-going (3.3V) pulse is applied to the opto-isolator and causes the gate terminal to go high. The intent of this circuit is to afford the maximum flexibility in operation. Therefore, unregulated DC-DC converters were used so that the output gate pulse positive and negative voltage levels can be adjusted at ground level [20].

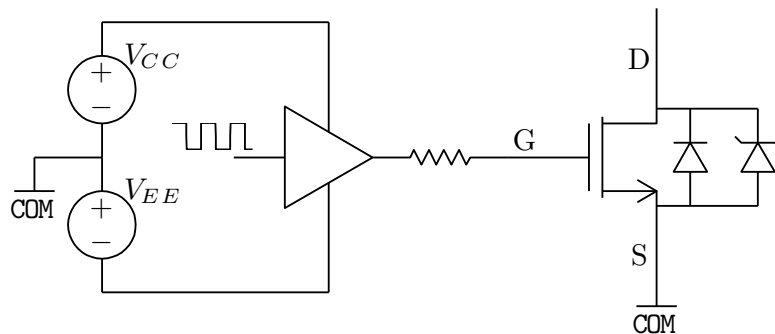


Figure 2-3: Gate Driver Schematic

The internal gate resistance of the MOSFET is dependent on the sheet resistance of gate electrode material and chip size. Other things being equal, the internal gate resistance is inversely proportional to the chip size: the smaller the chip, the higher the gate resistance. At the same rating, SiC-MOSFET die is smaller than Si die. Therefore, SiC-MOSFETs tend to have lower junction capacitances but higher gate resistance. The internal gate resistance of the SCH2080KE is approximately 6.3Ω . The total resistance in the gate circuit is a combination of the internal and external gate resistors. Switching time is severely dependent on the external gate resistance (R_G). In order to implement fast switching operation, it is recommended to use low external gate resistor of several ohms while monitoring surge conditions. The external gate resistance yielding the lowest switching energy while suppressing the ringing in the signal to stay within the recommended V_{GS} range of the device is selected. In this section, the steps involved in choosing the optimal external gate resistance for the SiC MOSFETs will be shown.

In an attempt to determine optimal R_G , the gate turn-on and turn-off waveforms are monitored for different values of R_G (0Ω , 2Ω , 5.11Ω , 8.66Ω , 13.3Ω , 20Ω). The waveforms are captured using a Tektronix DPO7054 digital oscilloscope and plotted using MATLAB. The test converter circuit is operated as a synchronous buck converter (see Figure 2-4 below) for each value of R_G with the following operating conditions:

Parameter	Set Point
DC Bus Voltage V_{bus} (V)	200
Input Inductance L_{in} (mH)	3

Input DC Bus Capacitance C_{in} (μF)	450
Load Resistance R_{load} (Ω)	10
Load Inductance L_{load} (mH)	43
Switching Frequency f_{sw} (kHz)	100
Fixed Duty Cycle D (%)	50

Table 2-2: Test Setup Operating Conditions

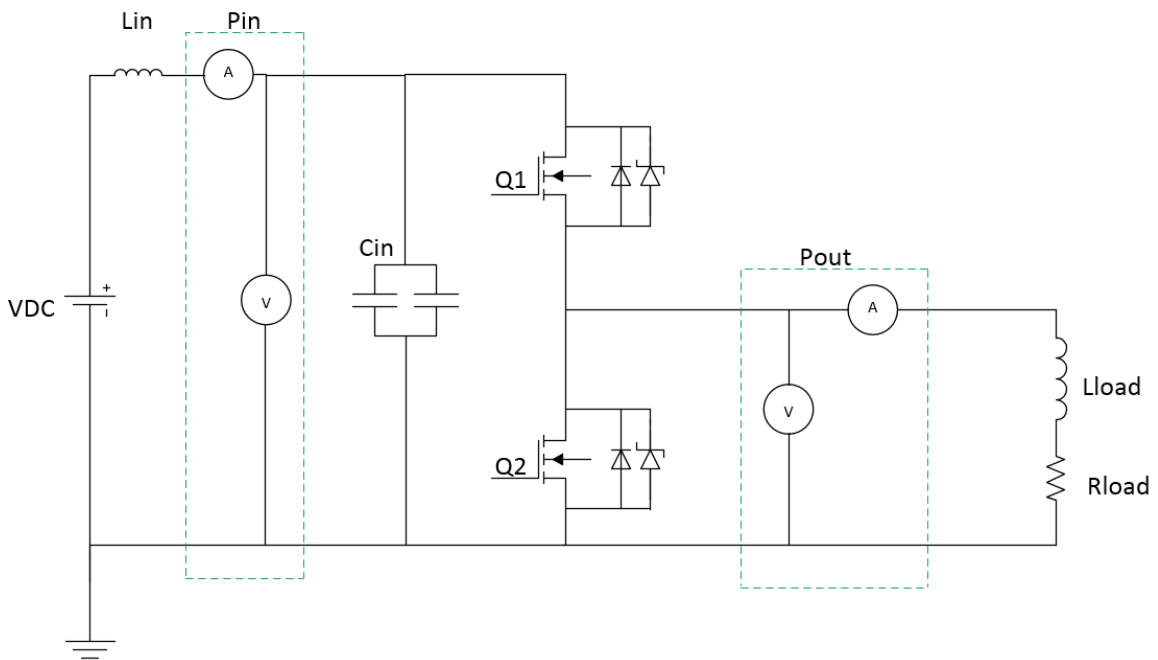


Figure 2-4: Synchronous Buck Converter Test Setup

With all operating conditions being the same, the channel losses are recorded using a power analyzer and analyzed for all values of R_G . The following plots help in choosing the optimal value of R_G . It is important to note that the absolute maximum V_{GS} rating for the SCH2080KE is +22V/-6V. Care should be taken to make sure that this driving signal does not exceed these limits. This becomes a crucial factor in the selection process.

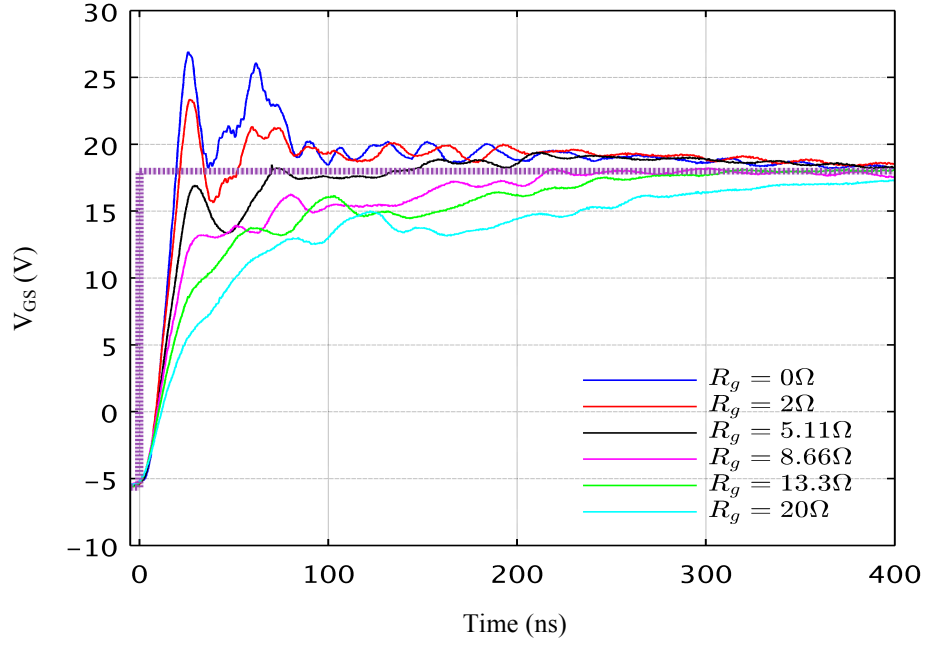


Figure 2-5: V_{GS} Turn-On for Various Values of R_G

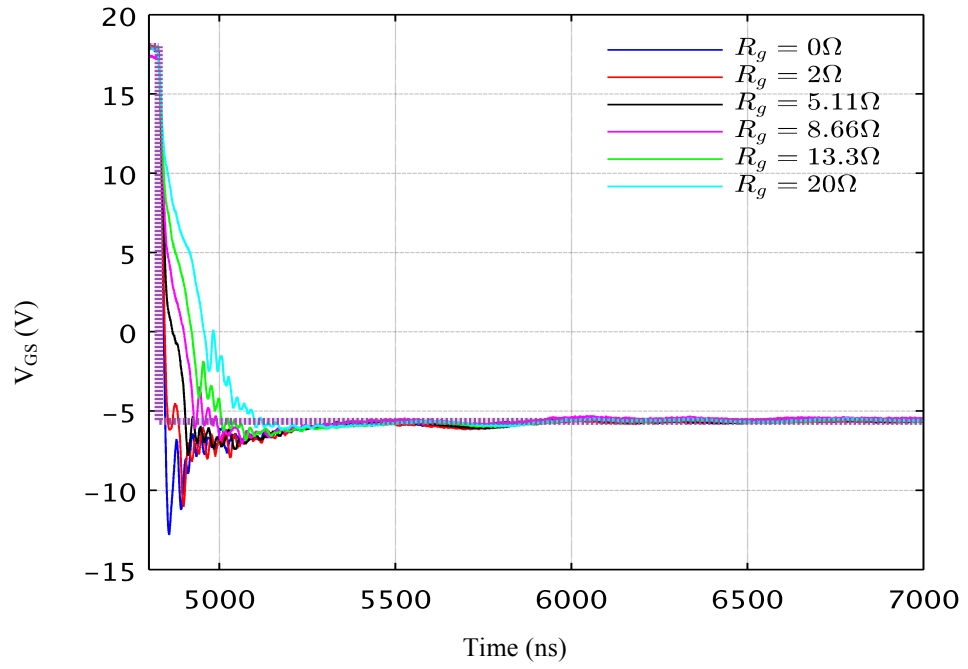


Figure 2-6: V_{GS} Turn-Off for Various Values of R_G

When no external gate resistor was added, the SCH2080KE experienced noticeable ringing in both gate turn-on and turn-off waveforms (Figure 2-5 and Figure 2-6). As expected the total loss in the circuit increases with higher values of R_G (see Figure 2-7). The plots show that $R_G = 8.66\Omega$ is the smallest resistance at which the V_{GS} limits were observed. Thus this was chosen as the optimal value of external gate resistance.

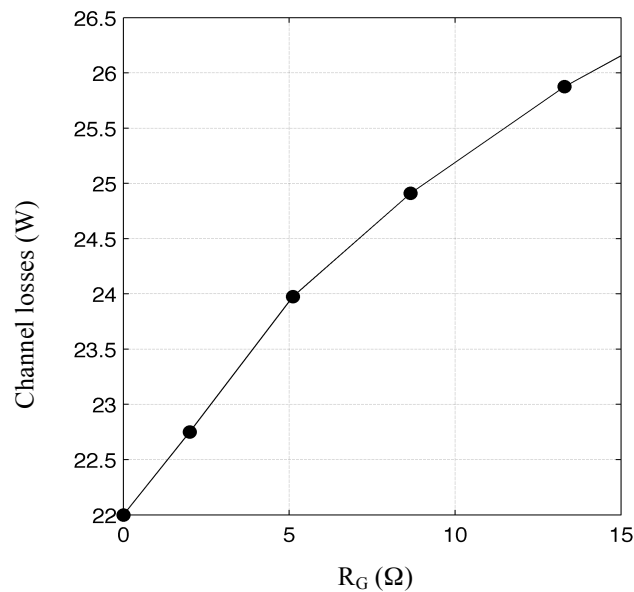


Figure 2-7: Variation of Channel Losses with R_G

2.4 Conclusion

This Chapter presented important design considerations for SiC based power electronics circuits. The test converter circuit was discussed including the power circuit and the auxiliary gate drive circuit. Selection processes for power device and gate resistance were covered.

Chapter 3

Converter Model

3.1 Introduction

Power loss is an important issue that must be considered in performance evaluation and cooling method design of power electronic systems. Many loss drivers exist within these systems. The operating conditions such as switch voltage, current, switching frequency and temperatures have significant impacts on component losses. These impacts are nonlinear which makes it quite complex to analyze the combined influence of several varied loss drivers on the system losses. Therefore, analysis of the system losses in multi-domain is time-consuming and not straightforward. This Chapter presents a simplified approach to modeling the losses in the test converter circuit.

The component losses and system losses could be defined as a function of many variables: operating points (DC bus voltage V_{bus} , output voltage V_o , switching frequency f_{sw} and load current I_o), designed circuit parameters (e.g. parasitics inherent to the test circuit, external gate resistance and other circuit elements) and heat sink temperature T_{sink} . The outputs of the loss model include the component losses, system losses and even the heat sink temperature of semiconductors if needed.

A model to predict the converter's overall performance as well as losses in the individual components is now described. The model is based off of parameters that can be readily measured using the converter test circuit and standard power electronic laboratory

equipment. The model provides the user the option to choose between two end circuit configurations:

- i. A synchronous buck converter
- ii. A three phase, two-level voltage source inverter (VSI)

The modeling process can easily be extended to other situations, such as modeling multiple phase oscillating output voltage and currents for a multi-level inverter. A procedure for obtaining the required model parameters is explained in Chapter 4. The input to this model is information about the circuit's operating point: DC bus voltage V_{bus} , output voltage V_o , output current I_o , switching frequency f_{sw} , ambient temperature $T_{ambient}$, fundamental frequency f_{fund} and phase peak voltage V_{ph} (last two parameters are used as inputs to the VSI model).

3.2 Modeling Approach

The model is able to simulate the actual circuit hardware and predict losses in power and gate drive components. This section establishes modeling relationships and procedures for both power and gate drive circuitry.

3.2.1 Converter Efficiency

The overall converter efficiency is defined by (Equation 3-1), where P_{out} is the total output power, P_{loss} is the total power lost in the converter, and $P_{dev,i}$ is the loss in a single device (this includes gate drive components and power switches) within the circuit.

$$\eta = P_{out} / (P_{out} + P_{loss}) \quad (\text{Equation 3-1})$$

$$P_{loss} = \sum_i P_{dev,i} \quad (\text{Equation 3-2})$$

3.2.2 MOSFET Losses

The losses in each switch consist of the conduction loss and the switching loss (Equation 3-3), where P_{MOSFET} is the total loss in a switch, D is the switch duty ratio, t_d is dead-time between the on-states of the complementary switches, $R_{DS,ON}$ is the on-state resistance, f_T is a polynomial function modeling the switching loss dependence on heat sink temperature, f_I is a polynomial function modeling the switching loss dependence on load current, both of which are measured in the characterization procedure (discussed in detail in Chapter 4), and are found to be of the form (Equation 4-2)(Equation 4-3) respectively, and V_{sw} is the voltage across the switch post turn-off. Note that the status of the anti-parallel diode determines V_{sw} . For example, in the case of a synchronous buck converter, $V_{sw} = V_{bus}$ for the top switch and $V_{sw} = 0$ for the bottom switch. In the case of a VSI, $V_{sw} = V_{bus}$ for both the top and the bottom switches.

$$P_{MOSFET} = P_{cond} + P_{sw} \quad (\text{Equation 3-3})$$

$$P_{cond} = P_{cond,Top} + P_{cond,Bot} \quad (\text{Equation 3-4})$$

$$P_{cond,Top} = (D - t_d f_{sw}) R_{DS,ON} I_o^2 \quad (\text{Equation 3-5})$$

$$P_{cond,Bot} = (1 - D - t_d f_{sw}) R_{DS,ON} I_o^2 \quad (\text{Equation 3-6})$$

$$P_{sw} = f_I(I_o) f_T(T_{sink}) f_{sw} V_{sw} \quad (\text{Equation 3-7})$$

Note that the conduction losses in the anti-parallel diode have been neglected in these expressions. This is because at all operating points considered; these losses are negligible compared to the losses associated with $R_{DS,ON}$.

The conduction losses (see (Equation 3-4), (Equation 3-5) and (Equation 3-6)) of the MOSFET are directly dependent on its on-state resistance. The on-state resistance varies as a function of the MOSFET's junction temperature. This dependence is modeled as a polynomial (see (Equation 3-8)) with constants fit to data measured in the characterization procedure, where T_{sink} is the heat sink temperature. The reason that the data is fit to the heat sink temperature, as opposed to the junction temperature, is because of its accessibility for physical measurement.

$$R_{DS,ON} = r_0 + r_1 T_{sink} + r_2 T_{sink}^2 \quad (\text{Equation 3-8})$$

3.2.3 Switch Thermal Modeling

The thermal circuit of Figure 3-1 is used to relate the heat sink temperature to the total MOSFET loss P_{MOSFET} and ambient temperature $T_{ambient}$, resulting in (Equation 3-9). Here, $R_{\theta,sa}$ is the sink-to-ambient thermal resistance. The temperature dependence of $R_{\theta,sa}$ is modeled as a power law (see (Equation 3-10)) whose coefficients are determined by the characterization procedure.

$$T_{sink} = T_{ambient} + P_{MOSFET} R_{\theta,sa} \quad (\text{Equation 3-9})$$

$$R_{\theta,sa} = s_0 T_{sink}^{s_1} \quad (\text{Equation 3-10})$$

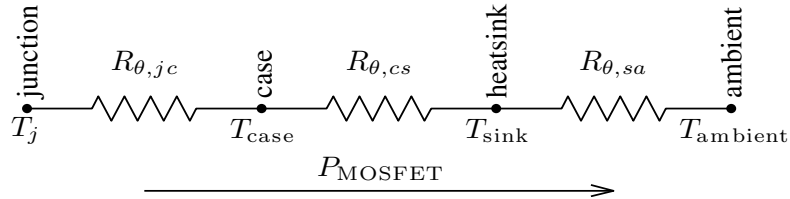


Figure 3-1: MOSFET Thermal Model

3.2.4 Gate Driver Circuit Losses

The total input power and losses in the gate driver circuit must be considered to calculate the overall converter efficiency and to ensure that all components operate within their limits at any given operating point. The gate drive design for the test circuit is based off of [20]. The total power supplied to the gate drive circuit is the sum of the losses in each DC-DC converter $P_{l_{DC,i}}$, each gate driver IC's internal circuitry and its hi/low resistances $P_{l_{gd,i}}$, and the power delivered to the RC equivalent networks $P_{l_{rc,i}}$ composed of each MOSFET gate and external gate resistance.

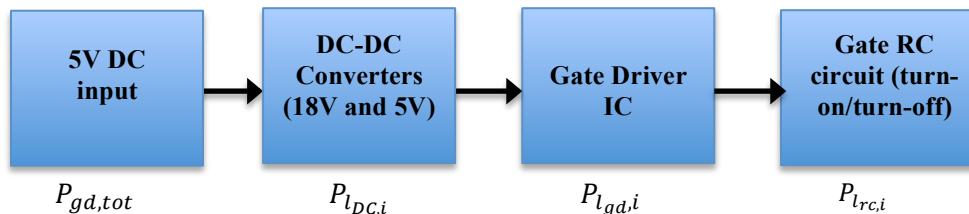


Figure 3-2: Gate Driver Power

Determining each of these loss components requires careful consideration of the unconventional use of a single-ended gate driver with bipolar power rails (Figure 2-3). The datasheet for the gate driver IC [21] specifies the total required input power as a function of the amount of external capacitance attached to the driver's output, the driver supply voltage, and the switching frequency. This data is intended for the traditional use-case where the driver has a single sided power supply. To model the losses in this converter's configuration, the input power is interpreted as having two components: power which is delivered to the attached RC network $P_{l_{rc}}$ and power required by the internal circuitry of the gate driver $P_{l_{rd}}$. The losses in the internal circuitry can be found as a function of gate capacitance by subtracting calculated losses in an RC network from the total driver input power specified in the datasheet.

During turn-on and turn-off, the MOSFET gate and related resistances appear as the equivalent circuit shown in Figures Figure 3-3, Figure 3-4, which can be used to calculate the total RC network power:

$$P_{l_{rc}} = P_{l_{rc,ON}} + P_{l_{rc,OFF}} \quad (\text{Equation 3-11})$$

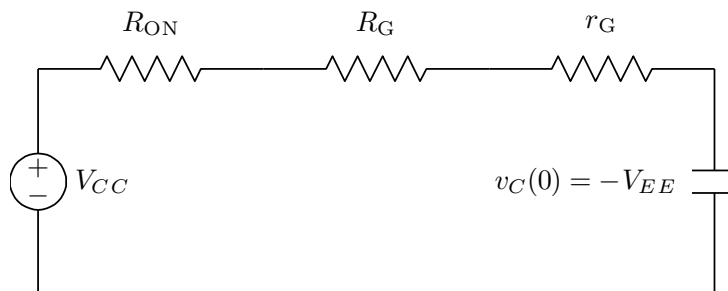


Figure 3-3: MOSFET turn-on Equivalent Circuit

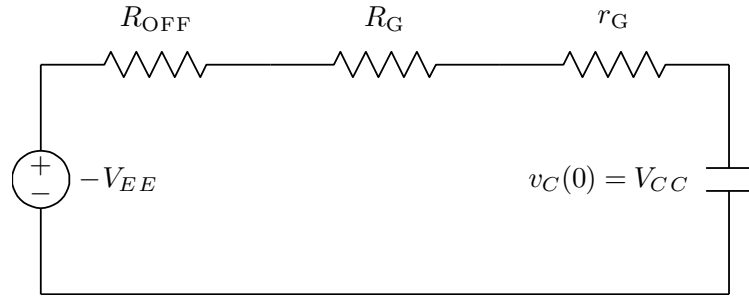


Figure 3-4: MOSFET turn-off Equivalent Circuit

The total power consumed by the gate driver IC depends on both the power dissipated in the internal circuitry and the power dissipated in the high and low output resistances of the IC [21]:

$$P_{l_{gd}} = P_{l_{rd}} + \frac{R_{ON}}{R_{tot,ON}} P_{l_{rc,ON}} + \frac{R_{OFF}}{R_{tot,OFF}} P_{l_{rc,OFF}} \quad (\text{Equation 3-12})$$

where $R_{tot,ON}$ is the total gate charging resistance during turn-on, and $R_{tot,OFF}$ is the total gate discharging resistance during turn-off. The datasheet for the DC-DC converters [22] specifies their efficiency as a function of their output power, which is $P_{l_{rd,i}} + P_{l_{rc,i}}$. The calculations for charging and discharging the MOSFET gate in this section require that the MOSFET gate resistance and capacitance be measured in the characterization procedure. It is discussed later in Chapter 4 that both of these parameters vary as a function of switch voltage and they are therefore modeled as polynomials (Equation 4-8)- (Equation 4-9), whose coefficients will be measured using actual test data.

3.3 Conclusion

At the top level the model accepts all the input operating conditions as discussed in Section 3.1. Armed with this information and the model parameters (determined using characterization procedure to be discussed in Chapter 4) that are inherent to the actual test circuit hardware, the algorithm guesses at a heat sink temperature to compute losses associated with circuit components (conduction and switching losses in the power circuit and gate drive power). The power losses are used in the switch thermal model to determine the heat sink temperature associated with the power flow. This process is iteratively repeated until the two temperatures (initial guess and thermal model output) match each other with an accuracy of 1%.

Chapter 4

Characterization Procedure

4.1 Introduction

While designing a power electronic converter, it is important to obtain the key characteristics of the power devices (in this case, the MOSFETs) in order to be able to model the converter's performance. The device's parameters help understand their realistic application prospect in present day power circuits. This chapter introduces and describes characterization procedures that are designed to capture the change in key device parameters with changing operating points and conditions.

Device characterization is often done using special test circuitry to measure device parameters, such as E_{ON} , E_{OFF} , gate capacitance, on-state resistance, etc., which are then used to predict the device's behavior in a converter. In circuits containing WBG devices, the switching transients are typically much faster than those containing Si devices, causing parasitic inductances and capacitances to have a greater effect on circuit performance. This decreases the accuracy of any modeling approach that relies on device parameters measured outside of the actual power-electronic circuit under consideration.

This chapter proposes an alternative circuit-level characterization approach that analyzes the behavior of the power devices within the power circuit to estimate the overall performance, without using external testing circuits and special equipment such as curve

tracers. The equipment required is commonplace in power electronic laboratories: an oscilloscope, digital multi-meters, a power analyzer, and temperature measurement devices. All data are obtained using a Yokogawa model WT1600 power analyzer, a Tektronix DPO7054 oscilloscope, a 100 Ω SA1 RTD from Omega Engineering, and a 34401A precision multi-meter from Agilent Technologies.

The idea is to use the results from the extensive characterization study, to be discussed in this chapter, to create a loss model (presented in Chapter 3) that can predict losses and thermal behavior of the test circuit under various operating conditions. The power circuit characterization procedures presented are generic, so that they can be applied to the study of any power electronic converter.

4.2 Power Device and Power Circuit Characterization

4.2.1 MOSFET on-state resistance and MOSFET sink to ambient thermal resistance

When the MOSFET is turned on, it approximates a very small resistance $R_{DS,ON}$. This resistance is an inherent property of the device dependent on its physical composition and structure. The on-resistance can be defined as:

$$R_{DS,ON} = R_{Source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcm} \quad (\text{Equation 4-1})$$

Where,

R_{Source} = Source diffusion resistance

R_{ch} = Channel resistance

R_A = Accumulation resistance

R_J = Component-resistance of the region between the two-body regions

R_D = Drift region resistance

R_{sub} = Substrate resistance

R_{wcm1} = Sum of bond wire resistance, the contact resistance between the source and drain metallization and lead frame contributions. [25]

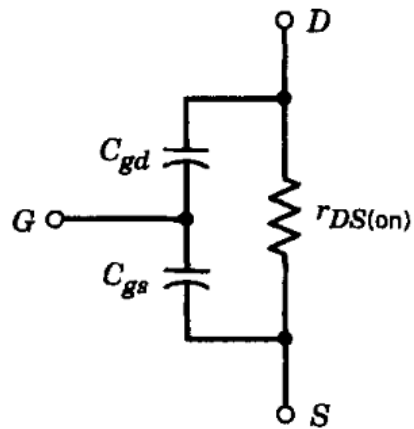


Figure 4-1: MOSFET Equivalent Circuit in the on-state [5]

Since SiC has dielectric breakdown field strength that is ten times higher than that of Si, high breakdown voltage devices can be achieved with a thin drift layer with high doping

concentration. This means, at the same breakdown voltage, SiC devices have quite low specific on-resistance (on-resistance per unit area). For example, 900V SiC-MOSFET can provide the same on-resistance as Si-MOSFETs and Si super junction MOSFETs with a chip size 35 times and 10 times respectively smaller [23]. The higher the gate voltage, the lower the on-resistance due to lower channel resistance.

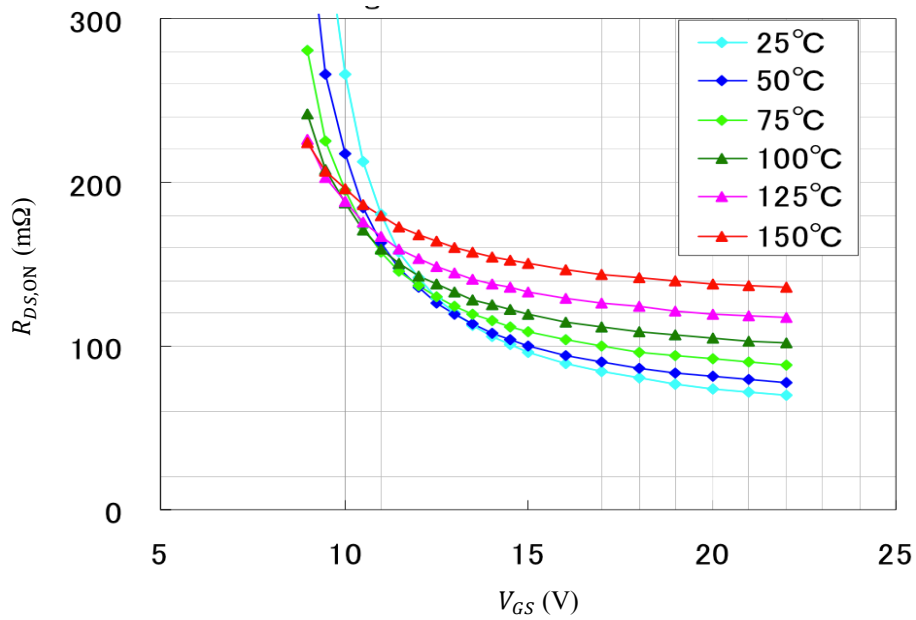


Figure 4-2: Dependence of on-state resistance of MOSFET on V_{GS} [23]

The power dissipated in this $R_{DS,ON}$ contributes to the conduction losses of the device. It is also important to note that the on-state resistance of the MOSFET, $R_{DS,ON}$, has a positive temperature co-efficient: which means that it increases with an increasing junction temperature (which in turn depends on load current flowing through it). This subsection describes a test designed to characterize the variation of SCH2080KE's on-state resistance with temperature.

The converter test circuit described in Chapter 2 is operated with the top switch held on, the bottom switch off, and a load resistance connected between the converter output and the negative voltage bus. A DC supply is used to apply a voltage across the bus bars, resulting in a DC current I_{DC} flowing through the top switch. The heat sink temperature T_{sink} and voltage drop $V_{DS,ON}$ between the drain and the source terminals of the top switch are measured. The ambient temperature $T_{ambient}$ is also monitored throughout the test. Different values of I_{DC} are used to obtain different heat sink temperatures (larger the current higher the heat sink temperature).

The $V_{DS,ON}$ data measured in the characterization procedure is used to estimate corresponding $R_{DS,ON}$ which is then modeled to fit the polynomial in (Equation 3-8) and (Equation 3-10). The measured ambient temperature $T_{ambient}$ is used in conjunction with T_{sink} and power lost in the top switch ($V_{DS,ON} \times I_{DC}$) as per the thermal circuit in Figure 3-1 to estimate $R_{\theta,sa}$.

Parameter	$R_{DS,ON}$			$R_{\theta,sa}$	
Coefficients	r_0	r_1	r_2	s_0	s_1
	76.3891	0.0770	0.0058	-1.2660	-0.5293

Table 4-1: Coefficients of polynomials in Equations 3–8 and 3--10

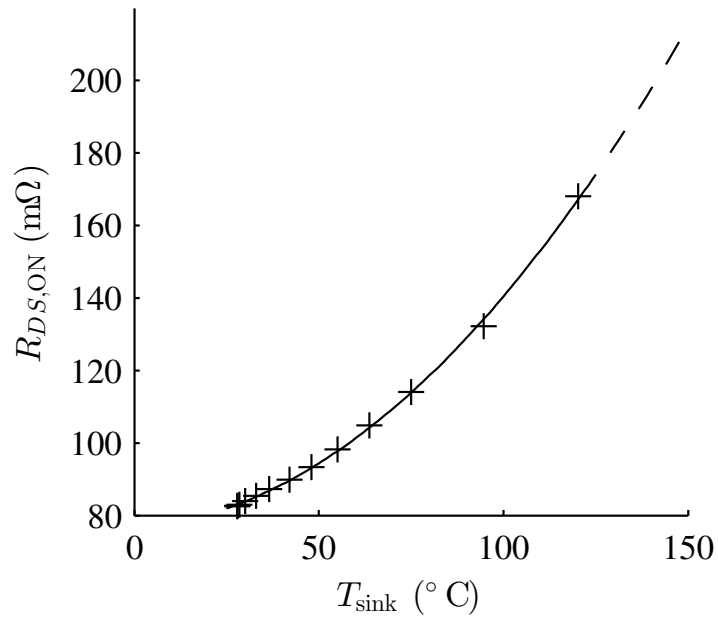


Figure 4-3: On-state resistance dependence on heat sink temperature

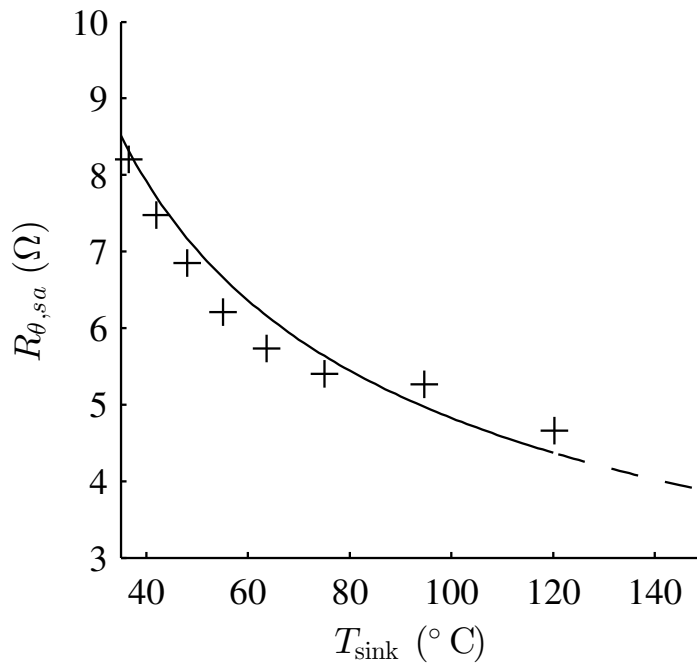


Figure 4-4: Sink-to-ambient thermal resistance dependence on heat sink temperature

These dependencies help in calculating the conduction losses in the MOSFET at different heat sink temperatures.

4.2.2 Switching Loss Dependence on Heat Sink Temperature and Load Current

Power MOSFETs have good switching characteristics as there is no storage delay caused by minority carriers as in the case of IGBTs (causing tail currents). The turn-on and turn-off sequence of a power MOSFET is explained below: [24]

Turn-on Transition

Turn-on delay time ($t_{d(on)}$)

This is the time for the gate voltage, V_{GS} , to reach the threshold voltage $V_{GS(th)}$. The input capacitance during this period is $C_{GS} + C_{GD}$. This period is the charging period to bring up the capacitance to the threshold voltage.

Rise Time (t_r)

It is the period after the V_{GS} reaches $V_{GS(th)}$ to complete the transient. It can be divided into two regions. One is the period where the drain current starts from zero (increasing with the gate voltage in accordance with the transfer characteristics) and reaching the load current. The other region is when the drain voltage starts to drop and reaches the on-state voltage drop. During the rise time, as both the high voltage and the high current

exist in the device, high power dissipation occurs. The rise time should be reduced by reducing the gate series resistance and the drain-gate capacitance (C_{GD}). After this, the gate voltage continues to increase up to the supplied voltage level; but, as the drain voltage and the current are already in steady state, they are not affected during this region.

Turn-off transition

Turn-Off Delay ($t_{d(off)}$)

At the start of the turn-off transient, the gate voltage starts to decrease and move towards its off-state value. The $t_{d(off)}$ is the time for the gate voltage to reach the point where it is required to make the drain current become saturated at the value of load current. During this time, there are no changes to the drain voltage and the current.

Fall time (t_f)

Fall time is the time where the gate voltage reaches the threshold voltage after $t_{d(off)}$. It is divided into the region where the drain voltage reaches the supply voltage from its on-state value and the region where the drain current goes from 90% to 10% of the load current.

Similar to power dissipation observed in the t_r region during turn-on state, power is lost in the t_f region during turn-off state. Hence, t_f must be reduced as much as possible. After this, the gate voltage continues to decrease until it reaches zero. As the drain voltage and

the current are already in steady state, they are not affected during this region.

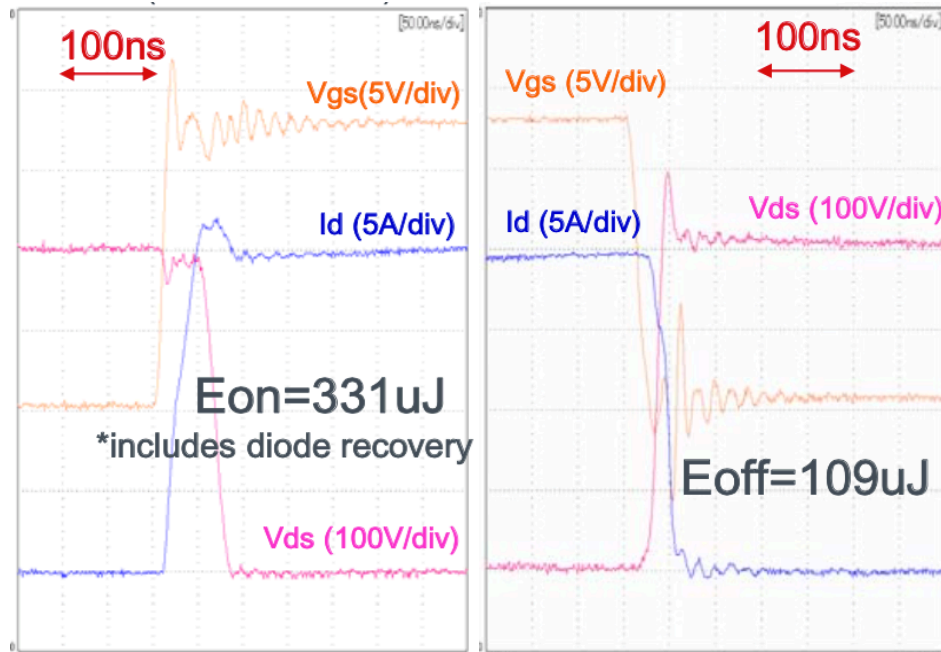


Figure 4-5: Turn-on and Turn-off observed in ROHM's SCH2080KE

The switching energy lost in a given power device is influenced by junction temperature (and in turn, the heat sink temperature), voltage across the device terminals and the commutated current as was expressed in (Equation 3-7). For a detailed investigation of the switching behavior, the test circuit was operated as a synchronous buck converter. A DC bus voltage was applied across the bus bars and an RL load was connected between the output terminal and the negative bus bar. The functional diagram of the setup is shown in Figure 2-4.

From the results of the test procedure that follows, the dependence on the heat sink temperature T_{sink} and the load current I_o are modeled by the polynomials (Equation 4-2) and (Equation 4-3) as shown below. Investigations showed that the dependence on switch

voltage V_{sw} (in this test setup also equal to DC bus voltage V_{bus}) is linear.

$$f_T(T_{sink}) = g_0 + g_1 T_{sink} + g_2 T_{sink}^2 \quad (\text{Equation 4-2})$$

$$f_I(I_0) = k_0 + k_1 I_0 + k_1 I_0^2 \quad (\text{Equation 4-3})$$

The equations above show the dependence of switching losses with heat sink temperature and load current. The coefficients of (Equation 4-2) are measured first, with the following procedure:

- 1) The DC bus voltage V_{bus} and load current I_o are fixed and the switching frequency is swept over a wide range to vary the operating temperature. For each switching frequency, the channel losses and MOSFET heat sink temperatures are measured.
- 2) The measured temperature is used to estimate $R_{DS,ON}$ and the conduction losses in the two switches to isolate the switching losses at each frequency. Note that switching losses will only occur in the top switch.
- 3) $f_T(T_{sink})$ is calculated using the switching losses above as $P_{sw}/(f_{sw}V_{sw})$ and (Equation 4-2) is fit to the results.

Parameter	$f_T(T_{sink})$		
Coefficients	g_0	g_1	g_2
(x10⁻⁶)	-0.5062	-0.0005	0

Table 4-2: Coefficients of Equation 4--2

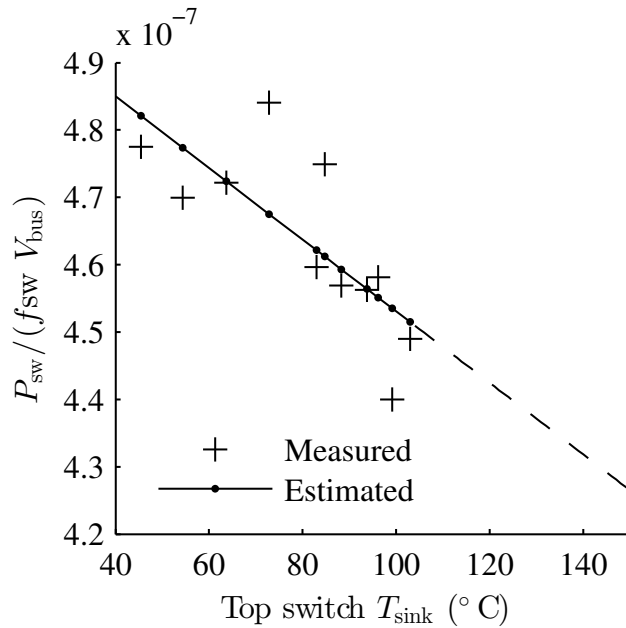


Figure 4-6: $f_T(T_{sink})$ as a function of the heat sink temperature. The solid line represents the data fit to Equation 4--2

The coefficients of (Equation 4-3) are measured with the following procedure:

- 1) The DC bus voltage V_{bus} and switching frequency f_{sw} are fixed and the load current I_o is varied. For each load current, the channel losses and switch temperature are measured.
- 2) The measured switch temperatures are again used to isolate the switching losses at each load current.
- 3) Equations 3--7 and 4--2 are used to calculate $f_I(I_o)$ for each load current and (Equation 4-3) is fit to the results.

Parameter	$f_1(I_o)$		
Coefficients	k_0	k_1	k_2
	0.2520	0.1323	0

Table 4-3: Coefficients of Equation 4--3

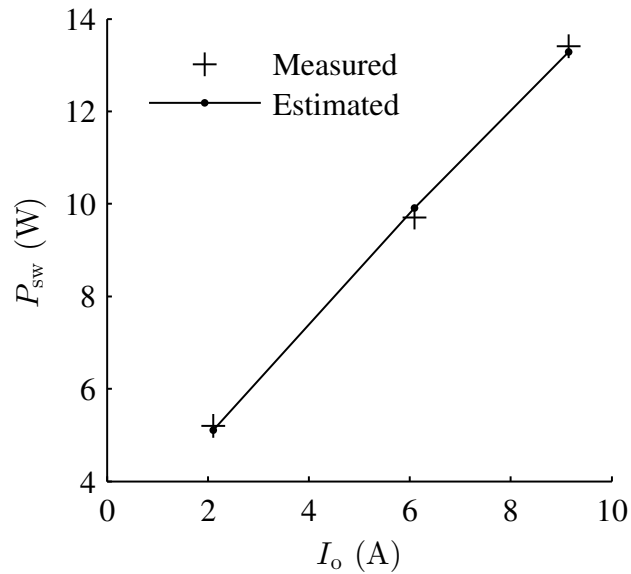


Figure 4-7: $f_1(I_o)$ as a function of the load current. The solid line represents the data fit to Equation 4--3

4.2.3 Gate Drive Circuit Characterization

The gate region of the MOSFET is composed of the gate metallization, the silicon dioxide underneath the gate conductor, which is termed the gate oxide, and the silicon beneath the gate oxide. This region forms a high quality capacitor, as is shown in Figure 4-8, and it is sometimes termed a MOS capacitor.

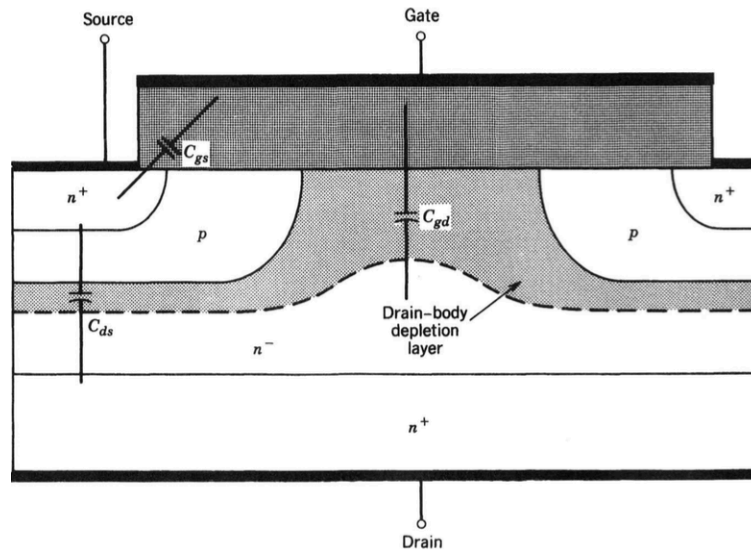


Figure 4-8: Cross-sectional view of a n-channel MOSFET showing parasitic capacitances

During the MOSFET's switching transitions, the only charges that must be moved are those on the stray capacitances and depletion layer capacitances, which are shown in the figure above [5].

These capacitances become important while trying to understand the behavior of the MOSFET. C_{GS} is the capacitance brought about by the overlap of the source and the channel regions by the polysilicon gate. C_{GD} consists of two parts, the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. Both the C_{GS} and the C_{GD} are not constant but vary with voltage across the device [5].

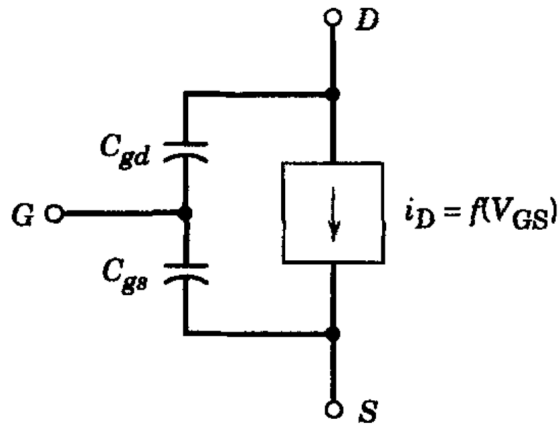


Figure 4-9: MOSFET equivalent circuit in cutoff and active regions

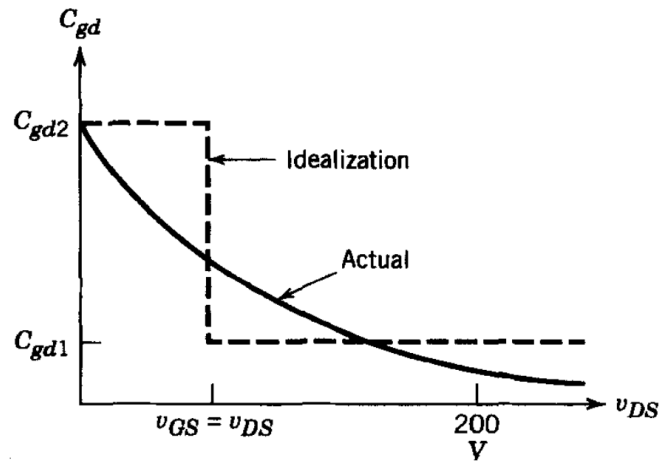


Figure 4-10: Variation of gate-drain capacitance with drain-source voltage

The MOSFET gate has an internal resistance, r_G , which as discussed earlier is dependent on the sheet resistance of gate electrode material and chip size.

The following test procedure establishes dependencies between the gate-source capacitance C_{GS} and the internal gate resistance r_G with the voltage across the switch V_{sw} .

The test circuit is operated like a synchronous buck converter. The voltage across the

external gate resistor V_{R_G} is measured using an oscilloscope and is used to calculate the gate charge at turn-on:

$$I_G = \frac{V_{R_G}}{R_G} \quad (\text{Equation 4-4})$$

$$Q_G = \int i_G dt \quad (\text{Equation 4-5})$$

The gate capacitance is calculated as $C_{GS} = Q_G/V_G$ where $V_G = V_{CC} + V_{EE}$. The resulting fit is depicted in Figure 4-15, where the DC bus voltage is varied from 50V to 200V.

The MOSFET's internal gate resistance was also measured for every value of bus voltage and was observed to have an unexpected dependence on the switch voltage. To measure the resistance, the gate-source voltage is measured on an oscilloscope at gate turn-on in addition to the above data for I_G . The gate current is used to calculate the voltage across the gate capacitance as:

$$V_C = \frac{1}{C_G} \int i_G dt \quad (\text{Equation 4-6})$$

$$V_{GS,calc} = V_C + i_G r_G \quad (\text{Equation 4-7})$$

The internal gate resistance is then estimated so as to minimize error between a calculated and measured gate-source voltage, $V_{GS} - V_{GS,calc}$, for each value of DC bus voltage. The results are fit to (Equation 4-9). Figure 4-11, Figure 4-12, Figure 4-13 and Figure 4-14 show the estimates calculated using the above and the resulting polynomial fit is shown in Figure 4-15.

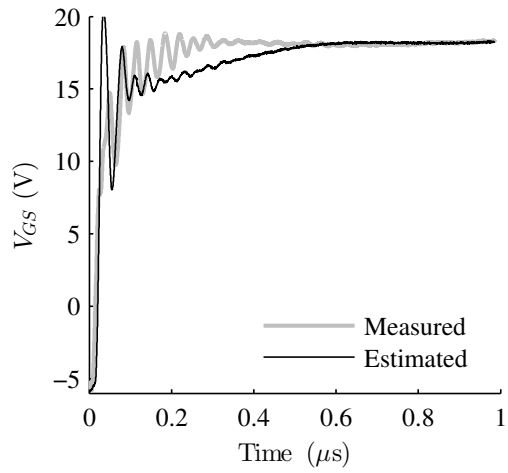


Figure 4-11: Example waveform for determining an r_G value that minimizes error between measured and calculated V_{GS} ; $V_{DS} = 50 V$. r_G was determined to be 12.03Ω

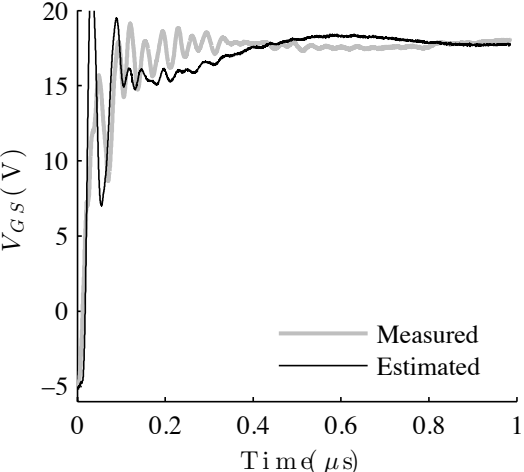


Figure 4-12: Example waveform for determining an r_G value that minimizes error between measured and calculated V_{GS} ; $V_{DS} = 100 V$. r_G was determined to be 13Ω

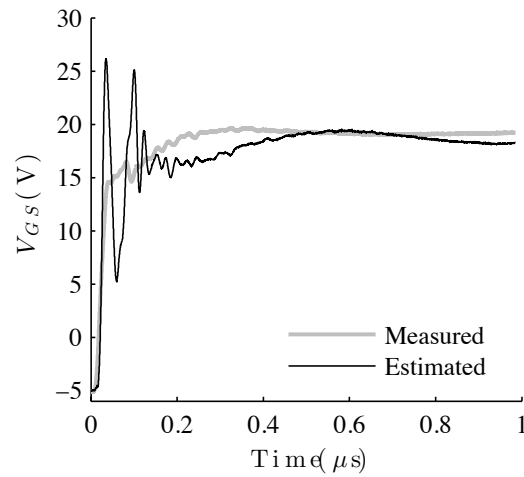


Figure 4-13: Example waveform for determining an r_G value that minimizes error between measured and calculated V_{GS} ; $V_{DS} = 150\text{ V}$. r_G was determined to be $13.92\ \Omega$

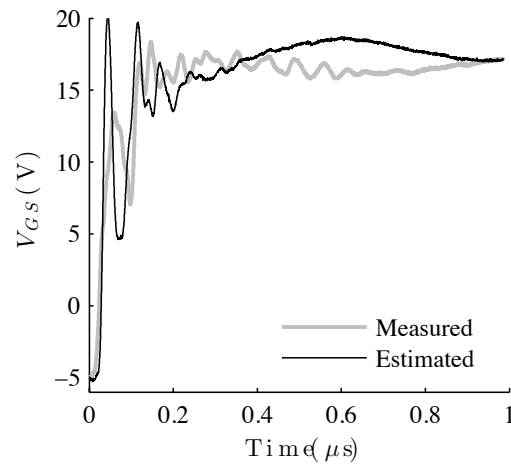


Figure 4-14: Example waveform for determining an r_G value that minimizes error between measured and calculated V_{GS} ; $V_{DS} = 200\text{ V}$. r_G was determined to be $14.39\ \Omega$

The results from the procedure are fit to the following polynomials:

$$C_{GS} = c_0 + c_1 V_{sw} \quad (\text{Equation 4-8})$$

$$r_G = r_{G_0} + r_{G_1} V_{sw}$$

(Equation 4-9)

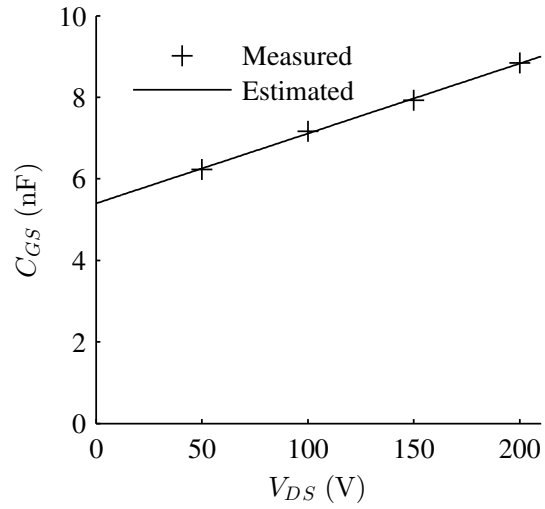


Figure 4-15: Variation of C_{GS} with V_{sw}

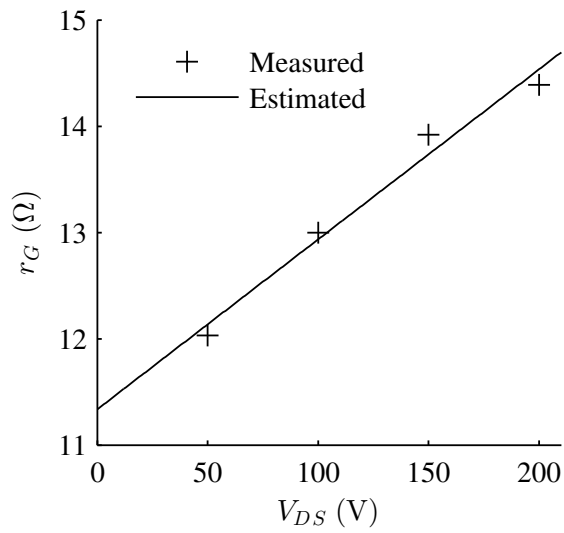


Figure 4-16: Variation of r_G with V_{sw}

Parameter	C_{GS}	
Coefficients	c_0	c_1
(x 10^{-8})	0.5395	0.0017

Table 4-4: Coefficients of Equation 4--8

Parameter	r_G	
Coefficients	r_{G_0}	r_{G_1}
	11.3350	0.0160

Table 4-5: Coefficients of Equation 4--9

4.3 Conclusion

This chapter presented characterization test procedures that can be used to extract power device information that are pertinent to calculating the device losses in a power converter application. The estimates and dependencies derived from the procedure are useful in creating the loss model presented in Chapter 3. All the dependency polynomials are fit to actual hardware results collected during the characterization. The tests presented are not specific to a particular device and can be used to model a circuit similar to the test converter used in this project. Furthermore, the dependencies established using the characterization procedure could also be used to create more accurate SPICE models for the power devices.

Chapter 5

Results and Conclusions

5.1 Introduction

SiC possesses superior material properties compared to Si as discussed in Chapter 1. SiC-based power devices are currently revolutionizing the semiconductor market for high-power, high-temperature and high-frequency end applications. For example, one of the potential applications of high temperature power electronics is in electric transportation. The DC-DC converters and inverters used in hybrid electric vehicles, require a number of switches and diodes. Hence, there is a great demand for wide band gap semiconductors like SiC in automotive electronics. There is always a need for reliable device characterization techniques to study the device behavior and evaluate its characteristics. A good loss model derived through the characterization procedure can predict circuit behavior quite accurately enabling the end user to perform adequate thermal designs.

This Chapter focuses on validating the loss model built as a part of the thesis. The previous chapters discussed in detail the loss model layout and the device parameter extraction procedure. The test converter is operated both as a DC-DC synchronous buck converter and a DC-AC three phase VSI where the input and output powers are monitored using a Yokogawa WT 1600. The hardware results are then compared against the model outputs for verification. Considerations and measures for model improvement

have also been discussed. Model limitations have been explained as well.

The parameters measured in the characterization procedure are now combined with the model from Chapter 3 to predict converter (DC-DC and DC-AC) performance under various operating conditions. The results are shown in Figure 5-1, Figure 5-2, Figure 5-3 and Table 5-1: DC-AC Three Phase VSI Model Verification Data (Total Power Consumption), which display very good agreement between predicted and measured values. The overall efficiency of the DC-DC converter is shown in Figure 5-2 and is broken down into conduction losses (not shown), switching losses in Figure 5-1, and drive circuit losses in Figure 5-3 for different loads. The power loss estimates of the DC-AC VSI are shown in Table 5-1. The different frequencies and loads tested represent a wide range of operating conditions: heat sink temperatures vary from 31.7°C up to 132.2°C and load currents range from 2A to 9A. The estimated values are predicted by the model using (Equation 3-1), (Equation 3-4) and (Equation 3-7) which only require knowledge of the operating point (the load, bus voltage, and switching frequency).

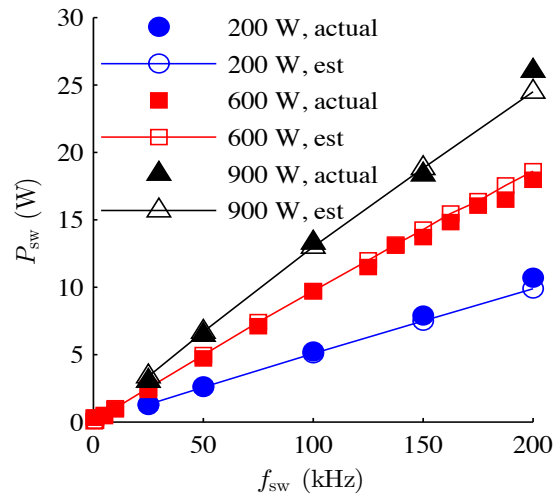


Figure 5-1: DC-DC Converter Switching Losses Comparison

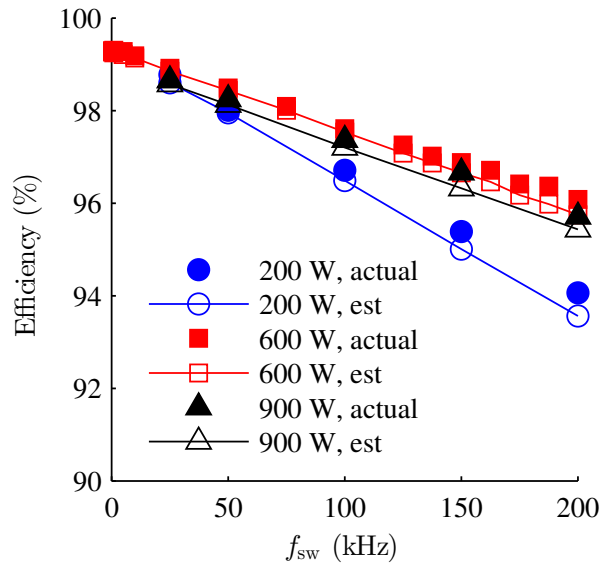


Figure 5-2: DC-DC Converter Efficiency Comparison

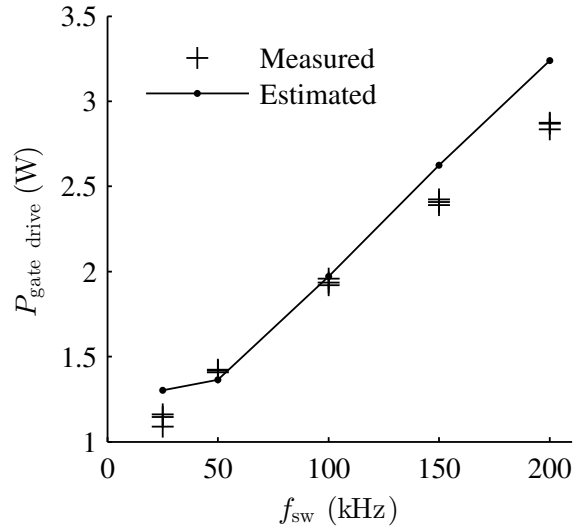


Figure 5-3: Gate Drive Power Consumption Comparison

Operating Conditions	Model Outputs (W)		Hardware Measurements (W)	
	P_{loss}	P_{gd}	P_{loss}	P_{gd}
V_{bus} : 200V f_{sw} : 97kHz 1 KW load				
f_{fund} : 60Hz	30.148	6.55	28.4	6.02
f_{fund} : 45Hz	31.113	6.51	29.6	6.1
V_{bus} : 200V f_{sw} : 195kHz 1 KW load				
f_{fund} : 60Hz	52.62	10.61	49.3	8.82
f_{fund} : 45Hz	51.38	10.67	53.9	9.38

Table 5-1: DC-AC Three Phase VSI Model Verification Data (Total Power Consumption)

5.2 Model Limitations

The plots show that the model outputs are accurate within 10% of the hardware results; with the maximum error showing up in the gate drive power estimates. This can be attributed to the fact that the gate driver characterization is based on data interpolation from the component datasheets of the circuit elements. This brings about a level of uncertainty to the gate driver characterization procedure—it would help to have more

complete information on the components from their respective manufacturers. All of the model dependencies and circuit parameters are derived with hardware results measured using the Yokogawa WT 1600 power analyzer: any error in measurement or tolerances in the display will cause the model predictions to stray away from the actual behavior of the circuit. The power analyzer also has limits that are dependent upon frequency and the power range being measured: the characterization tests involve a good amount of power flow to cover various operating conditions, since the absolute value of the losses is low (due to higher throughput of SiC devices), the relative error (in losses) could be considerably unacceptable

5.3 Summary

A SiC-based power electronic converter was presented and a loss-model and practical characterization procedures were proposed. A circuit-level, as opposed to a device-level, approach was taken to modeling the converter in order to minimize inaccuracies that can arise due to the combination of leakage inductances and capacitances and the fast transition times of wide band gap devices. The proposed characterization procedure uses laboratory equipment standard to any power electronics lab. Experimental results show that the model is able to predict the converter's (DC-DC and DC-AC) performance over a wide range of operating points.

5.4 Future Work

The model is currently based off of characterization of a single test circuit. Further improvements can be made by considering multiple test circuits and taking into account

changes and similarities in parameter dependencies over multiple boards. More intense characterization tests are needed and more investigations are required to improve the accuracy of the model. The models can be extended to analyze and evaluate the system level performances of multi-level converters and dual open-ended drives for motors. More investigation is required to examine the system level benefit of using SiC power devices.

References

- [1] L. Stevanovic, K. Matocha, P. Losee, J. Glaser, J. Nasadoski, and S. Arthur, “Recent advances in Silicon Carbide MOSFET power devices,” in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, Feb 2010, pp. 401–407.
- [2] L. Ravi, E. Severson, S. Tewari, N. Mohan, “Circuit-level characterization and loss modeling of SiC-based power electronic converters,” in *Industrial Electronics Conference (IECON), 2014 IEEE*, Oct 2014.
- [3] M. Briere, “The power electronics market and the status of GaN based power devices,” in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE*, Oct 2011, pp. 1–4.
- [4] J. Glaser, J. Nasadoski, P. Losee, A. Kashyap, K. Matocha, J. Garrett, and L. Stevanovic, “Direct comparison of Silicon and Silicon Carbide power transistors in high-frequency hard-switched applications,” in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, March 2011, pp. 1049–1056.
- [5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Wiley, 2002.
- [6] “CMF20120D data sheet rev. D,” Cree, Inc., Durham, NC.

- [7] “SCH2080KE data sheet rev. C,” Rohm Co., Ltd., Kyoto, Japan.
- [8] M. Briere, “Progress in silicon-based 600 V power GaN,” in *Power Electronics Europe*, June 2013, pp. 30–32.
- [9] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, “GaN on Si technologies for power switching devices,” *Electron Devices, IEEE Transactions on*, vol. 60, no. 10, pp. 3053–3059, Oct 2013.
- [10] R. Reiner, P. Waltereit, F. Benkhelifa, S. Muller, M. Wespel, R. Quay, M. Schlechtweg, M. Mikulla, and O. Ambacher, “Benchmarking of large-area GaN-on-Si HFET power devices for highly-efficient, fast-switching converter applications,” in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013 IEEE*, Oct 2013, pp. 1–4.
- [11] Z. Chen, Y. Yao, M. Danilovic, and D. Boroyevich, “Performance evaluation of SiC power MOSFETs for high-temperature applications,” in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, Sept 2012, pp. DS1a.8–1–DS1a.8–9.
- [12] A. Merkert, T. Krone, and A. Mertens, “Characterization and scalable modeling of power semiconductors for optimized design of traction inverters with Si- and SiC-devices,” *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2238–2245, May 2014.
- [13] J. Wang, T. Zhao, J. Li, A. Huang, R. Callanan, F. Husna, and A. Agarwal,

- “Characterization, modeling, and application of 10-kV SiC MOSFET,” *Electron Devices, IEEE Transactions on*, vol. 55, no. 8, pp. 1798–1806, Aug 2008.
- [14] J. Reed, J. McFarland, J. Tangudu, E. Vinot, R. Trigui, G. Venkataramanan, S. Gupta, and T. Jahns, “Modeling power semiconductor losses in HEV powertrains using Si and SiC devices,” in *Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE*, Sept 2010, pp. 1–6.
- [15] S. Hazra, S. Madhusoodhanan, S. Bhattacharya, G. Moghaddam, and K. Hatua, “Design considerations and performance evaluation of 1200 V, 100 A SiC MOSFET based converter for high power density application,” in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, Sept 2013, pp. 4278–4285.
- [16] Xiangxiang Fang (2012), “Characterization and Modeling of SiC Power MOSFETs,” Master’s Thesis, Ohio State University, Columbus, USA.
- [17] Zheng Chen (2009), “Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices,” Master’s Thesis, Virginia Polytechnic Institute & State University, Blacksburg, USA.
- [18] Christina Marie DiMarino (2014), “High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power Semiconductor Transistors,” Master’s Thesis, Virginia Polytechnic Institute & State University, Blacksburg, USA.

- [19] B.J. Baliga, *Advanced Power MOSFET Concepts*. Springer, 2010.
- [20] B. Callanan, “SiC MOSFET Isolated Gate Driver,” App. Note, Cree, Inc., Durham, NC.
- [21] “IXD630 data sheet rev. 3,” IXYS Co., Santa Clara, CA.
- [22] “RP Series data sheet rev. o/2014,” RECOM Electronic GmbH., NeuIsenburg, Germany.
- [23] Rohm Semiconductors, “SiC Power Devices and Modules,” App. Note, Rev. 001.
- [24] Fairchild Semiconductors, “AN-9010 MOSFET Basics,” App. Note, Rev. 1.0.5.
- [25] Abdus Sattar, “IXAN0061 Power MOSFET Basics,” App. Note, IXYS Corporation, Milpitas, CA.
- [26] Jamie Dunn, “AN 799 Matching MOSFET Drivers to MOSFETs,” App. Note, Microchip Technology Inc, Chandler, AZ.
- [27] Cree Inc., “Application Considerations of Silicon Carbide MOSFETs,” App. Note.
- [28] Cree, Inc, “Design Considerations for Designing with Cree SiC Modules Part 1. Understanding the Effects of Parasitic Inductance,” App. Note, Rev. A.
- [29] T. R. McNutt, A. R. Hefner, Jr., H. A. Mantooth, D. Berning, and S. H Ryu, “Silicon carbide power MOSFET model and parameter extraction sequence,”

IEEE Trans. Power Electron., vol. 22, no. 2, pp. 353–363, Mar. 2003.

- [30] Md Hasanuzzaman (2005), “MOSFET Modeling, Simulation and Parameter Extraction in 4H- and 6H- Silicon Carbide,” Master’s Thesis, University of Tennessee, Knoxville, USA.
- [31] United States. Rohm Semiconductor. *The Next Generation of Power Conversion Systems Enables by SiC Power Devices (white paper)*. San Diego. 2003. 05 Jan 2014<www.rohm.com/documents/11308/f75d744e-efd3-480e-9c9634e7db3fad9d
- [32] U. Drogenik, J. W. Kolar, “A General Scheme for Calculating Switching- and Conduction-Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems,” Power Electronic Systems Laboratory (PES), ETH Zurich.
- [33] Alpha & Omega Semiconductors, “Power MOSFET Basics,” App. Note.
- [34] A. Elasser, T. P. Chow, “Silicon carbide benefits and advantages for power electronics circuits and systems,” in *Proc. of the IEEE*, vol. 90, no. 6, Jun. 2002, pp. 969-986.
- [35] J. C. Zolper, “Emerging silicon carbide power electronics components,” in *Proc. IEEE APEC 2005*, vol. 1, pp. 11-17, Mar. 2005.
- [36] P. Friedrichs, R. Rupp, “Silicon carbide power devices – current developments and potential applications,” in *Proc. EPE 2005*, pp. 1-11, 2005.

- [37] P. Friedrichs, “Silicon carbide power devices – status and upcoming challenges,”
in *Proc. EPE 2007*, pp. 1-11, Sept. 2007.

Appendix

This section is intended to provide more information on the PCB layout of the test converter used in this project. The following figure (Figure A-1) shows the top and bottom layers of the PCB outline.

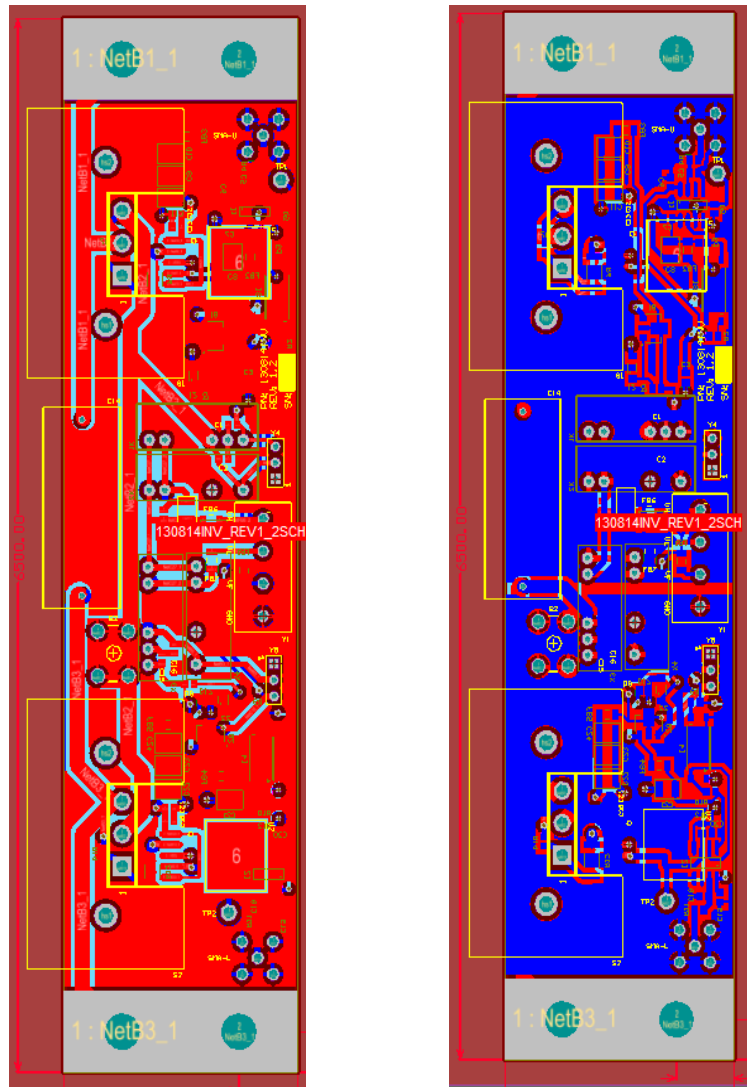


Figure A-1: PCB Layout of Test Converter

The dimensions of the board are 6.5 x 1.5 inches. A four-layer design has been adopted with a layer stack shown by Figure A-2. Interconnection among the various layers is achieved using vias.

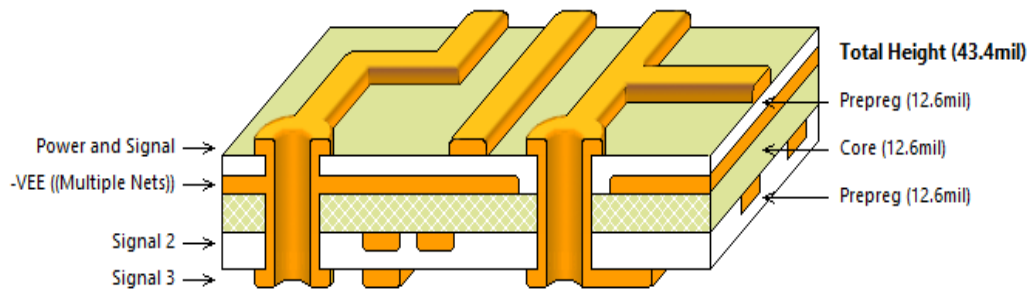


Figure A-2: Layer Stack of Test Converter Layout