Grid Fault Ride-through in Matrix Converters for Adjustable Speed Drives

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Dedication

This dissertation is dedicated to my wife, Heather, whose strength, support, and love made this journey possible. She is and always will be my best friend. A special dedication goes to our three children, Gavin, Siri, and Bridget whom make life truly joyful. Thank you all for sustaining me through this work.

Abstract

A novel ride-through approach for matrix converters in adjustable speed drives is presented, utilizing the input filter capacitors as an energy transfer mechanism to support motor flux during grid fault events. The addition of three bi-directional switches is required to isolate the input filter capacitors from the collapsed grid voltages. The additional input switches, a new ride-through vector control strategy, and the post fault reconnection logic are shown to enable ride-through of many cycle faults without the use of an additional energy storage devices. The proposed architecture is verified in theory, simulation, and hardware.

The architecture is valid for both indirect and direct matrix converters, provides full bi-directional power flow, and requires no additional reactive components. Additional benefits include reduced in-rush current, reduced transient voltage overshoot at plug-in, reduced damping losses, and potential harvesting of energy from remaining active grid phases.

To support the work, a review of power quality assessments is included. Through this review it is shown that the proposed architecture allows matrix converter-based adjustable speed drives to successfully operate in >95% of grid fault events.

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Chapter 1

Introduction

1.1 Historic and Current use of Matrix Converters for ASDs

Adjustable speed drives (ASDs) are a growing segment of modern industrial infrastructure. The market for them is expected to be $18.8B by 2017 with a growth rate of approximately 8.7% [2]. ASDs are often more efficient, more reliable, and easier to control than other drives.

In today's environment, industrial ASDs are largely operated by voltage source inverter (VSI) based power converters [3]. Matrix converters, introduced by Venturini in 1980, are capable of direct AC-to-AC conversion [4]. Unlike VSIs, matrix converters do not require an intermediate energy storage element. The lack of a bulky and relatively low reliability DC-link capacitor inherently gives matrix converters advantages which may be leveraged to improve size, cost, and reliability. Adoption continues to be slow, and presently only one company produces a commercial matrix converter [2]. The continuous advancement of power semiconductor technologies, including the recent commercialization of SiC MOSFETs [5, 6], will continue to make matrix converter based architectures more attractive over time.

1.2 Research Focus Areas within Matrix Converter-based ASDs

A very helpful overview of matrix converters and a review of current research areas has been addressed in [7]. These include:

1. Commutation strategies
2. Protection issues
3. Switch development
4. Abnormal operation
5. Input filter design
6. Fault ride-through

This work will focus on the last of these major areas, fault ride-through. In conventional matrix converters, fault ride-through capabilities are weak or non-existant. Due to the lack of an internal energy storage element, any change in the input AC source directly impacts the output AC load. Without actively designing for fault ride-through support, fault events cause a rapid loss in torque and a reduction of flux in the motor. In the worst case event, a complete loss of synchronism may occur. This will significantly impact the ability of the motor to recover beyond clearing of the grid fault, potentially requiring a complete stop and restart to occur [8].

Based on the source of energy utilized to sustain the system and the goal during ride-through events, fault ride-through can be split into two categories [9]:

1. Residual Energy Ride-through - Energy is harvested from existing components in the system and motor flux is maintained while minimizing the impact on cost.
2. Stored Energy Ride-through - An external energy source is utilized, usually a large capacitor, battery backup, or secondary AC source. Often full torque output is made available to the system during ride-through. The impact to the operation of the industrial system is minimized.

As the main advantage of matrix converter based ASDs is the lack of an energy storage element, this work will address "residual energy ride-through".

1.3 Literature Review in Matrix Converter Ride-through

Several solutions to the ride-through issue have previously been proposed. Holtz originally reviewed the issue of ride-through for back-to-back inverter based power converters [10]. The DC link capacitor and the spinning inertia of the motor were utilized to sustain the system. Klumpner and Blaabjerg applied the same concept to matrix converters utilizing the clamp capacitor and zero vectors [9, 8]. Prasad, et. al further developed this idea by applying a full suite of grid, zero, and open/clamp vectors in a hysteresis control method [11, 12]. However, in the later two cases, the clamp capacitor only reclaims power and cannot supply power to the motor due to the diode bridge connection. Cha and Enjeti added three additional switches and an additional DC capacitor to allow bi-directional power flow to the motor in ride-through operation [13, 14]. This modification required that a significant DC capacitor be added to the system. This capacitor or battery could be sized to meet any required ride-through capability. However, this resulted in effectively a stored energy ride-through solution.

This thesis presents a new solution to grid fault ride-through for matrix converters in ASDs. It is shown that the input filter capacitors may be utilized as an energy transfer mechanism, with the addition of three bi-directional switches. These filter capacitors are a required part of the MC-based ASD. They are utilized to make the inductive grid look like a voltage port. A zero-power vector control strategy is implemented to harvest the required energy to support motor flux from the motor inertia in the presence of changing speed, voltage, and torque without requiring external energy from the filter capacitors. An on-the-fly grid reconnection strategy is employed to return to normal grid connections. It is shown that >95% of faults are <0.5 seconds in duration. In this thesis the proposed solution is shown to ride-through grid faults of up to 0.5 seconds in duration with a 1 HP induction motor.

1.4 Research Goals for Matrix Converters during Grid Fault Events

The core contribution in this work is that fault ride-through inherently requires an energy storage device. Matrix converters themselves have no energy storage. Thus for a silicon only solution to enable ride-through it must utilize sources of energy already present in the system. These include the input filter reactors, motor flux, and the spinning inertia of the drive system itself. Utilisation of the these energy sources, plus the a minimal addition of switching devices should make ride-through possible.

As described in Section 1.2, this work will be concentrating on Residual Energy Ride-through. The primary goals of such a ride-through scheme, in order of importance, are:

1. Limit currents such that over-current faults do not occur
2. Maintain control of flux
3. Minimize impact to the mechanical system (usually speed)
4. Return control back to standard control method after fault clears

During a grid fault event proceeding with normal modulation and control schemes will rapidly result in negative consequences. For example, if the a-phase were to short to ground, then the still spinning motor would result in a large current driven back into the grid, causing rapid braking in the motor and large resistive losses, likely over current faults would result in the complete shutdown of the adjustable speed drive. It is because of this excessive fault current that we must modify our modulation and control schemes during a fault.

Maintaining control of flux is important in induction machines. Unlike DC motors and permanent magnet AC motors, there is no intrinsic alignment of rotor flux to the position of the rotor. When flux in the motor decays it is very difficult to do the calculations necessary to model the rotor flux position. Without knowledge of rotor flux it is impossible to determine the required stator voltage necessary to control the flux and torque. Motors are operated at a rated flux for the intended maximum speed of operation. In this work, it will be assumed that the required flux doesn't change during fault events. The control scheme will attempt to maintain this level of flux during faults.

An ASD deployed in an industrial system will likely have serious economic implications if a motor has a rapid deviation in applied torque. For example, in a printing press, if a roller were to stutter or break sharply (due to an uncompensated grid fault) a large amount of material could be destroyed or worse damage to the press itself may occur. In this work, since there is no alternative source of power, it will be assumed that a controlled deceleration is acceptable.

Upon clearing of the fault, the system must be reconnected to the grid and control returned back to standard control methods thereby accelerating the motor to the target speed in a controlled fashion.

1.5 Detailed Listing of Chapter Contents

- Chapter 1 - Introduction: reviews the value of ASDs and MC-based ASDs to industry, the scope, and end goals of this work.
- Chapter 2 - Reviews the structure of MC-based ASDs and the vector control theory behind their operation.
- Chapter 3 - A review of fault events and estimates of the fault event coverage with the addition of this work.
- Chapter 4 - A description of the primary original contribution of this work, using zero-power control mode to allow a relatively small input capacitor and motor inertia to sustain the ASD through a fault event.
- Chapter 5 - Reviews additional benefits of this architecture to the system.
- Chapter 6 - Reviews limp-along mode, a further original contribution of this architecture allowing extended ride-through of faults.
- Chapter 7 - Conclusion and Discussion

Chapter 2

Control of ASD Power Converters

This chapter reviews the assumptions about how the system is setup, how to control the system in normal operation, and briefly reviews the modifications necessary to control the system in the presence of a grid fault.

2.1 The ASD System

The system typically consists of a squirrel cage induction machine implemented as an adjustable speed drive in an industrial application. The system inputs are the grid voltages and a commanded speed. The output is electromagnet torque, which acts on a simple inertial model of a rotational system resulting in a radial speed. A diagram of the assumed system is shown in figure 2.1.

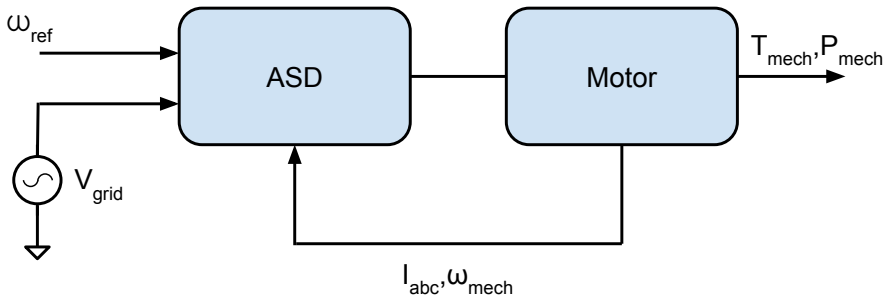

Figure 2.1: High-level Diagram of an ASD system

A 3-phase matrix converter based ASD schmatic is shown in 2.2. Due to the capacitive input source (filter) and the inductive output load (motor), Matrix converters in this configuration are traditionally operated as a voltage source converter. The output is assumed to be a PWM voltage with a commanded average value for each v_A, v_B, and v_C. Resulting in sinusoidal output currents of i_A, i_B, and i_C. The input is assumed to be a sinusoidal voltage source with values of v_a, v_b, and v_c. Throughout this manuscript we will discriminate between the grid voltage by a "g" sub-script (ie., v_{ga}) and the matrix converter input (ie., v_{ma}). However, in typical matrix converters these nodes are shorted, thus at the same potential. During normal operation the grid disconnect switches displayed on the left side of 2.2 are closed.

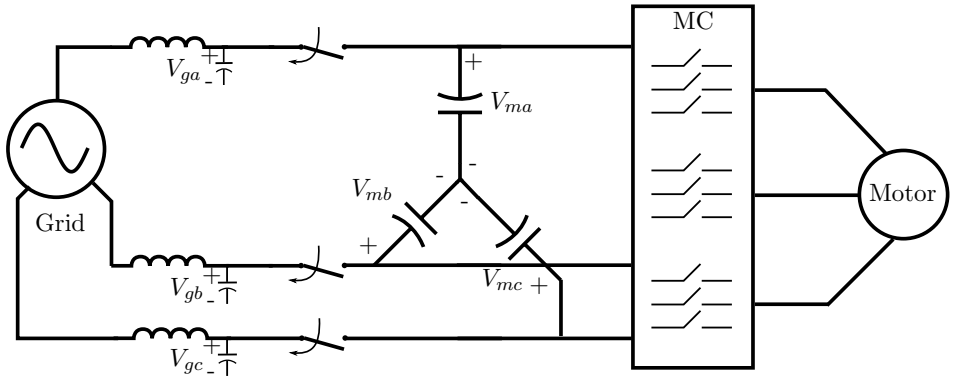

Figure 2.2: Schematic of the 3-phase ASD matrix converter

There are two basic hardware implementations of matrix converters. The first is a direct matrix converter shown in Figure 2.3. This has 9 bi-directional switches or 18 independently switched gate-drives and IGBTs. The second is a indirect matrix convert shown in Figure 2.4. This has 6 bi-directional switches and 6 uni-directional switches. That require a positive voltage between V_h and V_l at all times. The indirect matrix converter requires 18 gate-drivers and IGBTs.

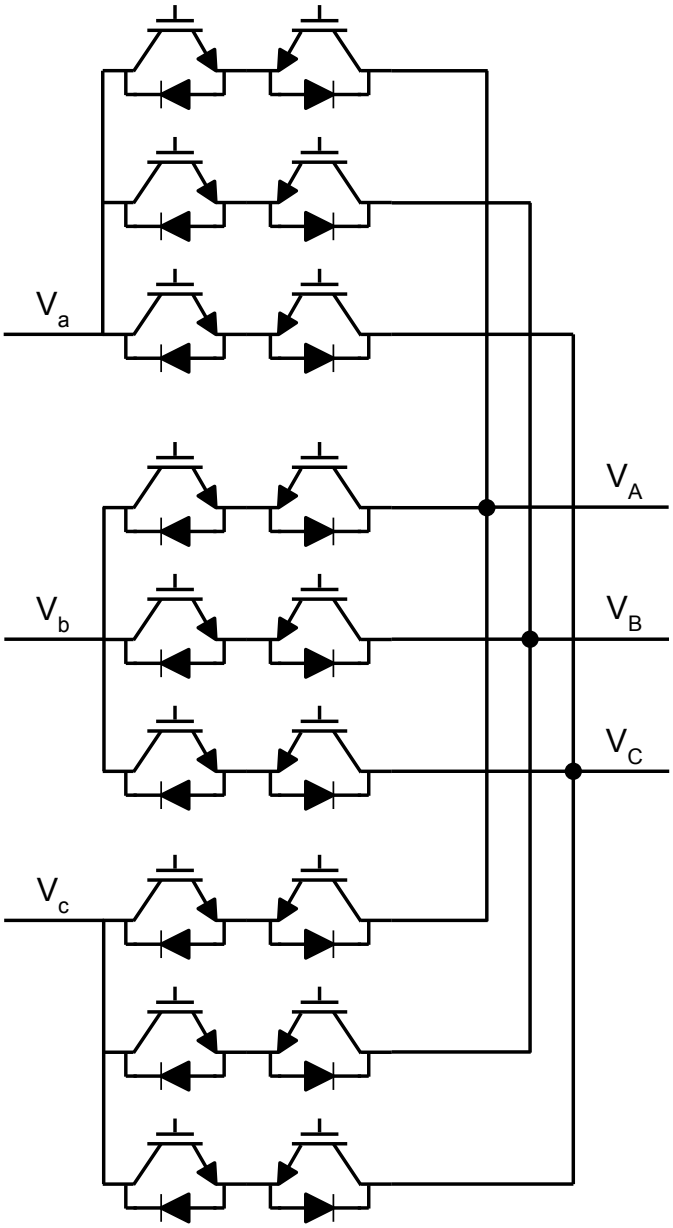

Figure 2.3: A direct matrix converter

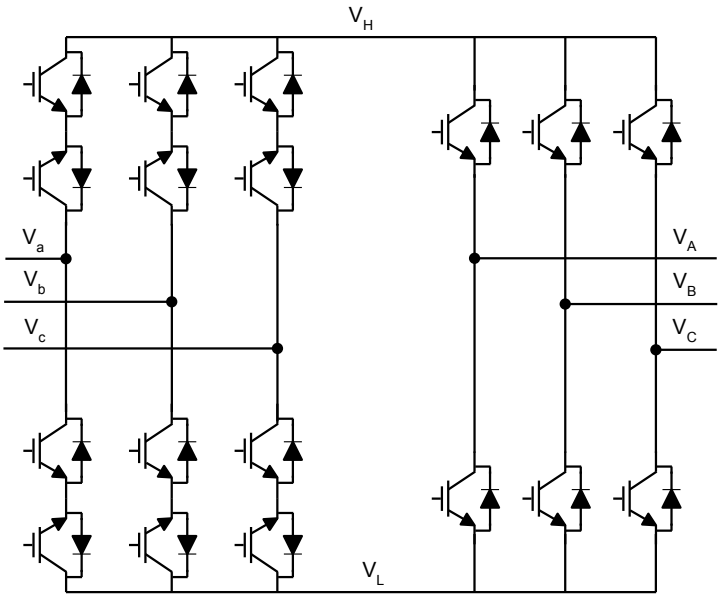

Figure 2.4: An indirect matrix converter

Both configurations of matrix converters are identical from the instantaneous circuit perspective of shorting a given input phase to a given output phase. (They do differ from a transient and commutation point of view.) The control signals for either hardware implementation can be converted from one to the other. Furthermore, either hardware implementation may be used interchangeably from the controls point of view. They both act as a DC-transformer [15] with a variable turns ratio (based on duty ratio) between the input phases and the output phases. More discussion on this topic is available in Appendix A.2.2.

2.2 Space Vectors

This section will provide a short review of space vectors for quick reference. The reader is encouraged to review an appropriate text (e.g. Chapter 2-6 [16]) for a proper discussion of this subject.

Most motors can be modeled as a 2.5D system, with 2 full dimensions and a third fixed depth dimension. The cross section is shown in figure 2.5. Due to the fact the

system is rotational in nature it is most convenient to describe the relevant voltages, currents, and fluxes as 2-D space vectors (depicted by the symbols V, I, λ on figure 2.5. These vectors represent the physical angle within the motor not just a mathematical construct.

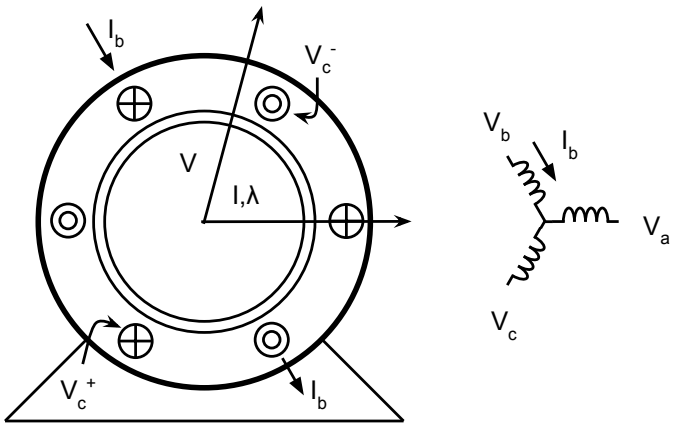

Figure 2.5: Cross section of motor and equivalent circuit

Assuming a sinusoidally distributed winding, the output voltages v_A, v_B, and v_C, when applied to the stator terminals of a three-phase induction machine, can be transformed into a single complex quantity. The stator voltage space vector defined as follows:

$$\vec{v_s}(t) = v_A(t) + v_B(t)e^{j120^\circ} + v_C(t)e^{j240^\circ} \tag{2.1}$$

In the case of sinusoidal and balanced voltages,

$$\vec{v_s}(t) = |V_{ABC}|\angle\theta_{ABC}(t) \tag{2.2}$$

where, only θ_{ABC} varies with time, representing the spacial direction of the voltage applied to the stator. Similarly, space vectors can be defined for the resulting currents and fluxes that flow in the machine due to these applied voltages.

$$\vec{i_s}(t) = i_A(t) + i_B(t)e^{j120^\circ} + i_C(t)e^{j240^\circ} \tag{2.3}$$

$$\vec{\lambda_s}(t) = \lambda_A(t) + \lambda_B(t)e^{j120^\circ} + \lambda_C(t)e^{j240^\circ} \tag{2.4}$$

The flux vectors are particularly useful in that they represent the physical position of an equivalent dc magnet at that moment in time. This can give useful insight into the forces present within the motor.

It should be noted that these quantities are referenced to the stator A-axis which we'll define as 0°. It is often necessary to rotate a space vector quantity to a different rotational reference (for example the when the rotor turns.) Utilizing space vectors makes this easy. For example, when the rotor is at 15° and we wish to determine the relative position of the applied voltage vector from the point of view of the rotor a-axis. All that is required is to multiply the space vector by the difference in position between the current axis and the new axis, as shown below:

$$\vec{v_s}^r(t) = (|V_{ABC}|\angle\theta_{ABC}(t))e^{j(0^\circ - 15^\circ)} \tag{2.5}$$

2.3 d-q Reference Frame

This section will review the conversion of a space vector to a two dimensional vector within an arbitrary reference frame.

The concept of a moving reference frame is common in vector control systems. Using the idea of rotating a space vector shown in Section 2.2, it is easy to transform an a-phase referenced (static) space vector into an alternative reference frame (for example the rotor flux aligned reference frame).

Before we begin treating the conversion between reference frames we need to review definitions of the various axises present in the motor. The a-axis is the stator a-phase location, usually assumed to be fixed at 0°. The A-axis is the rotor a-axis with position equal to that of the rotational position of the rotor. The final axis, the d-axis, is often aligned with quantities of interest in the motor and is utilized to simplify analysis.

It is important to note the voltage, current, and flux space vectors (in Section 2.2,) have been defined with reference to the a-axis. Some common alignments of the d-axis include stator (non-moving), stator voltage space vector (rotating at 60Hz), and rotor flux (rotating at 60Hz minus slip speed with some offset angle due to leakage). A full

discussion of the alternatives for the d-axis definition is outside the scope of this work. However, a basic review of the most common alternatives is given below.

The simplest definition of the d-axes location is simply to set $\theta_d = \theta_a = 0°$ Thus the d-axis is locked to the stator a-phase axis. This is the simplest to understand but results in sinusoidally varying quantities for all the control variables.

In traditional grid connected induction machines the voltage supplied by the grid can be used to define the d-axis location (for example when the a-phase voltage peaks the angle $\theta_{da} = 0°$), this is referred to as a grid-aligned or synchronous speed d-axis as the d-axis rotates with a speed equal to the synchronous speed of the grid space vector. This is convenient because at steady state, the currents and fluxes developed in the machine are fixed angles from the voltage on the stator terminals. Thus, within the grid-aligned d-q reference frame they are static. Resulting in easier calculation of applied torque and control inputs.

However, when an induction machine is connected to an ASD power converter, the d-axis is more commonly aligned with the air-gap flux. In the literature, this is generally referred to as flux-aligned control. In ASDs the machine is free to operating at any speed. During changes in speed the angular offset between the applied voltage and the generated flux varies significantly. Aligning the d-axis to flux offloads the calculation of this offset from the control system, again resulting in static values of current and flux within the d-q reference frame.

Flux-aligned control requires an accurate estimation of the flux. This can be difficult, especially at low speed or rapidly changing currents (for example during a fault event.) It is because of this reason that allowing short circuit currents or rapid motor deceleration adversely impacts the ability of the system to recover from grid faults. The loss of accuracy in the estimation of the flux angle, is often referred to as a "loss of synchronism."

2.4 Current control in the rotor-flux-aligned d-q reference frame

Once a system is defined in terms of vector quantities and these vector quantities are referenced to the rotor-flux-aligned d-q frame. We can fairly intuitively picture how

the machine works. Since the reference frame d-axis is aligned with the air gap flux, the q-axis flux must be zero ($\lambda_{rq} = 0$.) This results in the basic analogy that any current delivered to the stator d-axis (i_{sd}) results in flux generation within the induction machine. In addition, any current delivered to the stator in the i_{sq} direction leads to the generation of electromagnetic torque to the load.

These two parameters i_{sd} and i_{sq} are our primary control inputs to the system. They are developed by applying v_{sq} and v_{sd} to the terminals of the motor. This is usually done through a PI control loop as shown in figure 2.6.

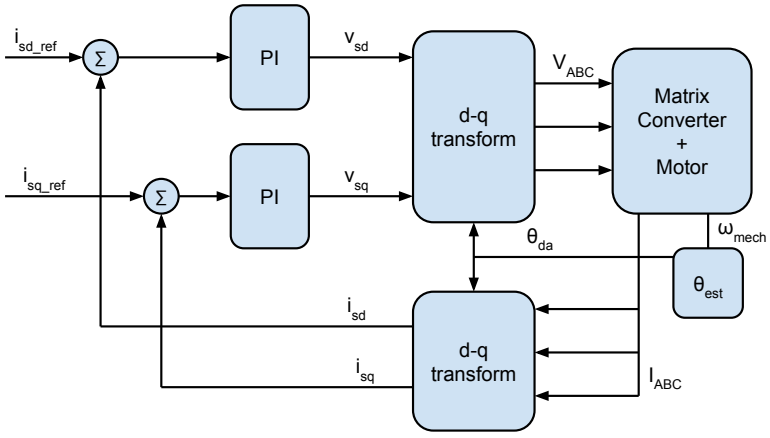

Figure 2.6: Standard PI control of current

The operation of the flux estimator and assertion of the angle of air gap flux (θ_{rd}, shown in Figure2.6) is beyond the scope of this work (see Chapter 5-1 [16]), but sufficed to say they require well behaved currents and voltage on the stator terminals. Without accurate estimation, the control loop rapidly degenerates into non-synchronous oscillations.

2.5 Speed control in the d-q reference frame

Once current control of i_{sd} and i_{sq} is implemented it is simple to control motor/system speed and flux. The mechanical system is modeled as a first-order system with inertial

mass (J), load torque (T_{load}), and acted upon by an electromagnetic torque (T_{em}),

$$\frac{d}{dt}\omega_{mech} = \frac{T_{em} - T_{load}}{J_{eq}} \tag{2.6}$$

The addition of another PI controller can be utilized to control speed with zero steady-state error. It is also common to put some feed-forward control on i_{sd} in order to limit flux during low voltage or high speed operation. This is represented by the $f()$ function between i_{sd} and λ_{ref}.

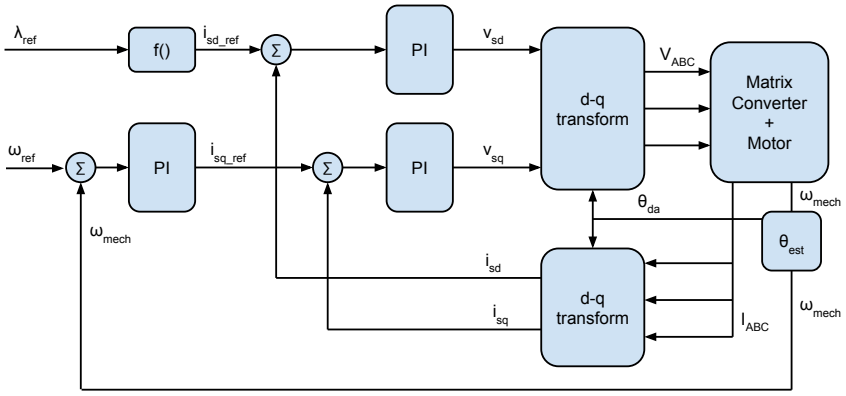

Figure 2.7: Standard PI control of speed

The final speed controlled ASD model with d-q transform is shown in figure 2.7. This represents the standard operational controls model of the ASD. The goal of this research is to modify this model to allow operation of during fault events. The next chapter will discuss the types of faults that will be addressed and the frequency of occurance of those events.

Chapter 3

Fault Events: Prevalence and Detection

This chapter reviews the basic structure of faults and implications of fault detection on ride-through event handling. The detection and types of three-phase fault events was undertaken in this work only to identify likely cases to assist in the verification of the intended design.

3.1 Fault Types and Prevalence

Grid faults come in many forms. Dorr, et al. conducted a comprehensive study of fault type, duration, and magnitude in 1997 [17, 1]. This assessment draws on three power quality surveys by the National Power Laboratory (NPL), Canadian Electrical Association (CEA), and Electric Power Research Institute (EPRI). Combined, these surveys consist of over 7000 monitor-months of data. Reviewing the data gives an overview of the importance of particular ride-through amplitude and duration targets. The summary of fault events can be seen in Fig. 3.1.

Fig. 3.1 shows that a large number of faults are in the 80% to 110% range. These ranges are likely serviceable with current ASDs, assuming motors are slightly over engineered to be able to operate at maximum speed at 80% of rated input voltage. Most power converters can safely operate at 110% of rated voltages. Modifying the system considerations would allow operation of ASDs in 56% of all faults recorded in these

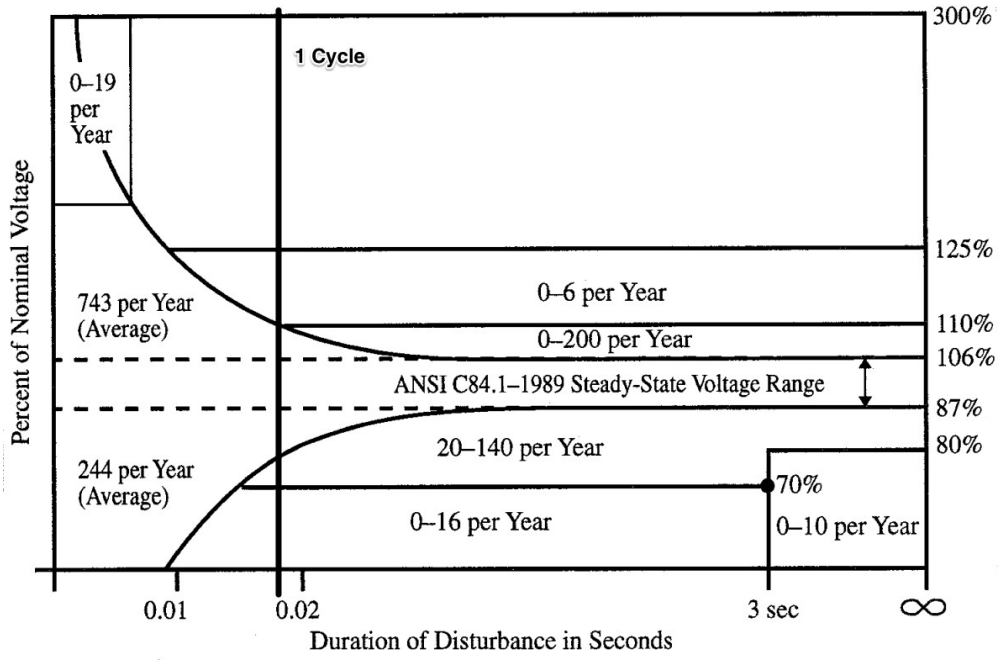

Figure 3.1: Distribution of grid faults vs. voltage and duration, image reproduced with permission from [1]

surveys.

Dur. of RT (sec)	0.1	0.166	0.333	0.5	1	2	10	inf
Coverage LV Flts	0.457	0.602	0.681	0.728	0.780	0.825	0.903	1.000
Coverage of All Flts	0.935	0.952	0.962	0.967	0.974	0.979	0.988	1.000

Table 3.1: Coverage of Faults with a Maximum Duration of Ride-through Control

This leaves a target region from zero to ∞ seconds of faults with less than 0.7pu (low voltage, LV faults) to be handled by the new fault ride-through solution. Obviously, without an external energy source the motor can not be sustained indefinitely. The goal for the ride-through will be to sustain the motor for as long as possible with the given capacitors and motor inertia. Specifically, an ASD with the improvements described in this thesis would cover a very large portion of all fault events. For example, 0.5 seconds of ride-through (RT) would yield >96% of all faults covered, as shown in Table 3.1 (calculations based on Table III in [17]).

There is limited consensus on the behavior of power converters during fault events.

For the bulk of this work it is assumed the best activity for a converter is to disconnect from the grid entirely. In this case any fault, from 0pu to 0.7pu, will be handled by complete disconnection from the grid for the duration of the fault. However, chapter 6 will look at some ideas on how to make use of partially available phase voltages to extend ride-through. This does come at a cost of additional non-sinusoidal loading of the grid during fault events.

3.2 Fault Detection

The subject of fault detection in three-phase system is beyond the scope of this work [18, 19, 20]. It is assumed that faults can be detected within a fraction of a cycle. Specifically, in simulations this is determined to be when the input waveform drops below 95% of the nominal amplitude. In the hardware results of this thesis the three-phase power supply can not generate transient fault events and the hardware is hard disconnected by IGBT switches then the control electronics are notified of the fault.

It should be noted that rapid detection of faults is critical to the operation of a ride-through scheme. If the grid voltages are allowed to collapse significantly before the control electronics are notified of a fault, additional steps will be required to operate the drive. The remaining capacitor voltage may need to be restored utilizing a boosting mode immediately after faults are detected. This will further reduce ride-through duration.

3.3 Modulation During Fault Events

Modulation of matrix converters is a heavily treated subject. Typically a matrix converter operates with a modulation scheme that supports sinusoidal input and output currents during steady state operation. However, during heavy acceleration, fault events, and other transient events these modulation schemes generally fail to maintain sinusoidal input currents. Similarly, all modulation schemes require that you give up some voltage headroom in order to modulate the current at the input (in the case of steady state operation, this headroom is not needed). However, in fault events this headroom

could be critical to transitioning modes or extending ride-through. This thesis will operate with a simple active rectifier front-end. This will allow the absolute maximum voltage to be made available to the motor.

Chapter 4

Input Filter Method of Fault Ride-through

This chapter reviews the original contribution of "Utilization of the input filter capacitors to exchange energy between the motor inertia and the motor flux during faults events," thus allowing MC-based ASDs to ride-through grid fault events without additional energy storage elements.

4.1 Proposed Ride-through Solution

This section describes the following three subcomponents of the proposed solution:

- Subsection 4.1.1 - Input-filter-based voltage source to replace the grid during a fault event
- Subsection 4.1.2 - A zero-power vector control strategy to maintain flux in the motor and alignment information while no energy is available from the grid
- Subsection 4.1.3 - An on-the-fly reconnect strategy to resume normal operation after the fault has cleared

The methods in Subsection 4.1.1 to isolate the matrix converter from the grid and the method in Subsection 4.1.2 to control the motor without using external energy are

highly interdependent. A short review of the control concept will help to understand the motivation behind the isolation method.

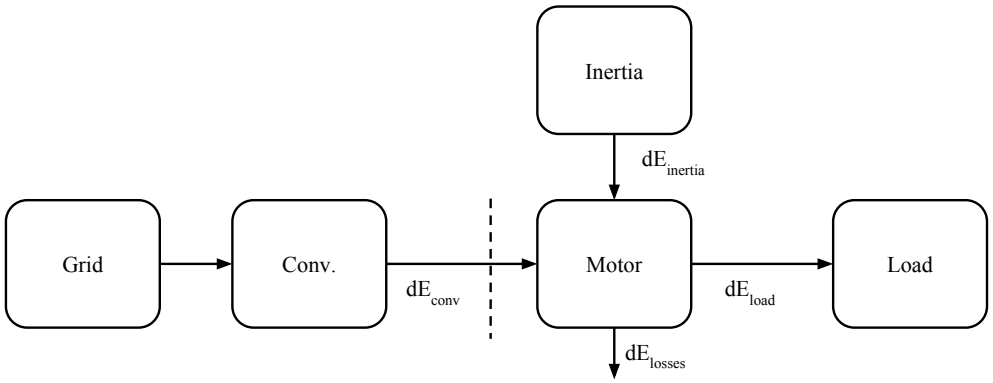

Figure 4.1: Energy flow diagram

Looking at the change in energy at the motor (described in Fig. 4.1), the energy balance equation can be written as Eq. 4.1.

$$dE_{conv} = dE_{losses} + dE_{load} - dE_{inertia} \tag{4.1}$$

Assuming that we can control the power delivered by the converter then, $dE_{conv} = P_{ref}\, dt$. Setting P_{ref} to zero results in $dE_{conv} = 0$ as well. Inserting $dE_{conv} = 0$ and re-arranging Eq. 4.1 yields Eq. 4.2.

$$dE_{inertia} = dE_{losses} + dE_{load} \tag{4.2}$$

Setting dE_{conv} to zero requires the power transfer be zero at any point between the grid and the motor. In Fig. 4.1 above, we chose the dashed line. However, this could be accomplished where ever knowledge of all three phase-voltages and currents is available. Both the input and the outputs of the filter elements and the input terminals of the motor could potentially work. In this work, it is assumed that the motor input terminals are a convenient place to do this.

It can be seen in in Eq. 4.2, the losses and load will be inherently supplied with energy from the inertial energy of the system. Thus this control scheme is referred to

as zero-power control. The zero-power control scheme has the inherent advantage that it requires no external energy source to maintain the specified motor flux.

However, in reality, the stator currents of the induction machine cannot be controlled arbitrarily. A voltage source is required, essentially equal to the effective back-emf of the spinning motor in the presence of the specified flux. During a grid fault, one or more of the input phase voltages may be low or even zero thus making control difficult or impossible[21]. An alternative voltage source is required. When utilizing zero-power control this alternative voltage source is not required to provide any energy ($dE = 0$).

The alternative voltage source can be accomplished in number of ways. As discussed in the introduction, this element has been implemented in other works [14, 12, 8]. This paper will present the use of the input filter capacitor for this purpose.

4.1.1 Input-filter-based voltage source

The first element of the proposed solution is to provide an alternative source of voltage in the absence of the grid during a fault condition. A set of three switches between the grid and the filter capacitors is proposed as shown in Fig. 4.2.

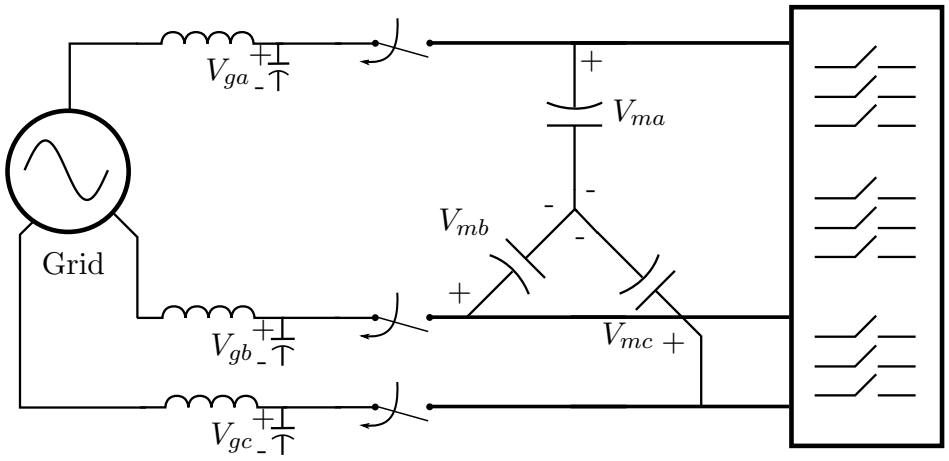

Figure 4.2: Schematic of the 3-phase input filter grid disconnect switches

These filter capacitors are required in matrix converters to make the input a voltage port. The input filter capacitors are typically large compared to clamp capacitors, but small compared to DC-link capacitors in conventional ASDs [22]. The proposed use of

the input capacitors plus disconnect switches for ride-through will allow bi-directional power transfer to the motor during ride-through.

In the event a grid fault is detected, the switches are opened allowing the residual voltage present on the filter capacitors to be utilized by the converter. While these need to be bi-directional blocking switches, they only require switching speeds in excess of a fraction of the line frequency. This reduces the associated cost and losses. The switches can be implemented by nearly any semiconductor switching device, IGBTs, or MOSFETs. IGBTs were used in this paper.

At the moment of a disconnect event, a load current may be flowing in the inductor L. This current must be allowed to decay slowly or it will cause an over voltage condition. As shown in Fig. 4.3, it is recommended that there is a small capacitor to ground (C_1 in Fig. 4.3) in order to absorb the remaining inductor current at the time of the disconnect event. During normal operation the sum of C_1 and C_2 will be effectively equal to the designed filter capacitance value.

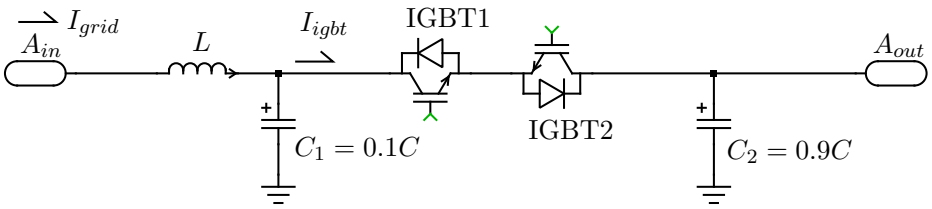

Figure 4.3: Schematic of an IGBT implementation of a single phase of the grid disconnect switch

Simulations across power factor and fault phase angle were completed. No input over currents, over voltages, or other anomalies were found. An example simulation is shown in Fig. 4.4. In this simulation a single phase fault on phase-a occurs and is detected. This is shown in Fig. 4.4 by the signal FaultGate transitioning low. At this time, the IGBTs are open circuited and the current I_{igbt} immediately becomes zero. The current, I_{grid}, going through the inductor cannot immediately stop and decays through the C_1 capacitor, ringing slightly.

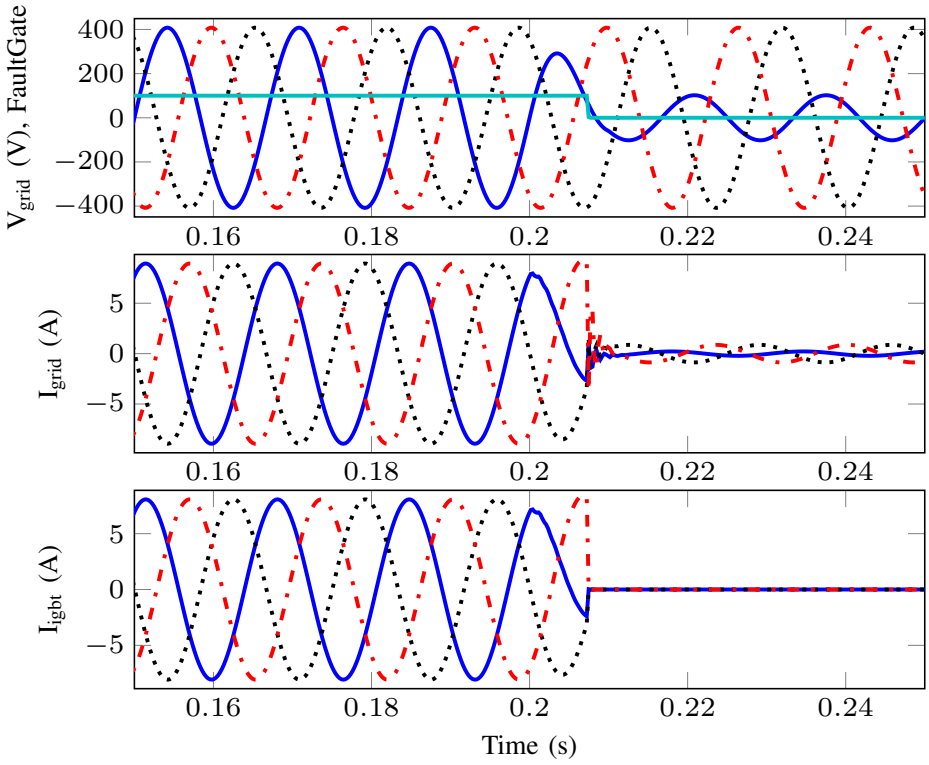

Figure 4.4: Grid disconnect event: Input voltage and currents

4.1.2 Zero-Power Control

As described previously, zero-power control consists of forcing the power transfer to be zero. This could be satisfied any place between the grid input terminals and the motor terminals. However, in the basic vector control the stator terminal voltages are directly controlled while measuring the stator terminal currents. Thus voltage and current are known at this point, making it a convenient place to measure and control the power flow.

In standard rotor-aligned field-oriented control [23, 16], flux is controlled independently from torque, where i_{sd} controls flux and i_{sq} controls torque. The proposed zero-power control scheme operates only on torque, leaving flux to be controlled independently.

Figure 4.5 shows a standard d-q or rotor-flux-oriented control scheme for ASDs.

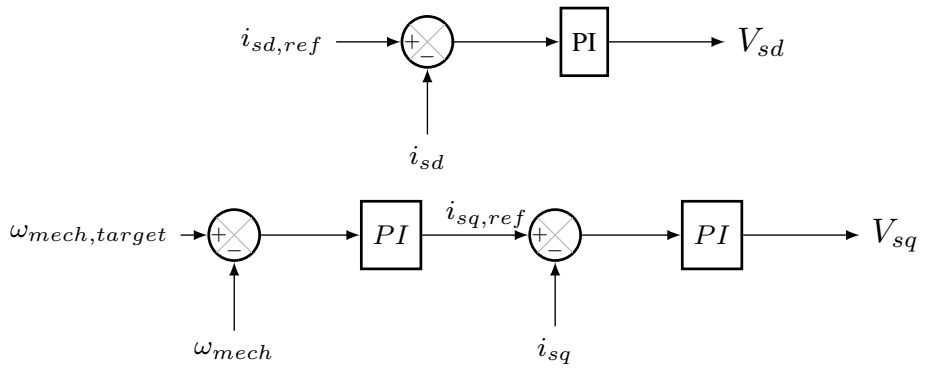

Figure 4.5: Rotor-flux-oriented control scheme (d-q), with speed control

In the event of a fault, control is switched from speed control (Figure 4.5) to power control as shown in Figure 4.6.

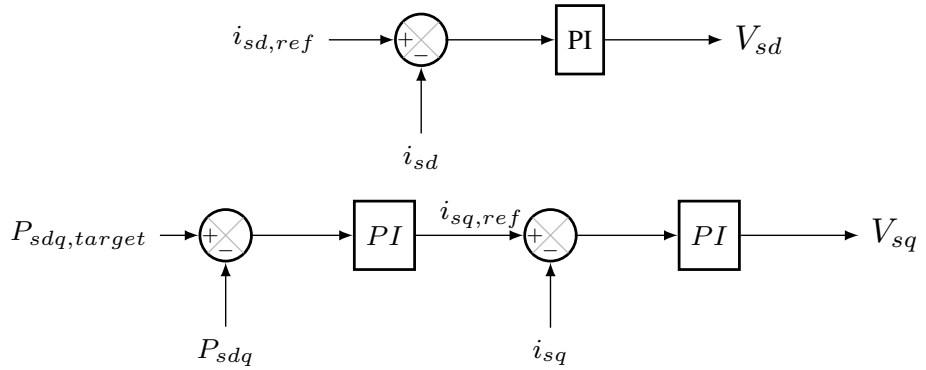

Figure 4.6: Rotor-flux-oriented control scheme (d-q), with zero-power control

We will implement zero-power control by setting the input reference $P_{sdq,target}$ to zero. P_{sdq} is the power delivered by the matrix converter at the stator terminals defined as:

$$P_{sdq} = v_{sd}i_{sd} + v_{sq}i_{sq} \tag{4.3}$$

.

It can be shown that P_{sdq} is a squared function of i_{sq}, therefore linearization is needed in order to solve for $\frac{\Delta P_{sdq}}{\Delta i_{sq}}$.

In the Laplace domain, the standard form equations for d-q rotor-flux-oriented control of an induction machine are as written in Eq. 4.4 and Eq. 4.5.

$$v_{sd} = R_s i_{sd} + s\lambda_{sd} - \omega_d \lambda_{sq} \tag{4.4}$$

$$v_{sq} = R_s i_{sq} + s\lambda_{sq} + \omega_d \lambda_{sd} \tag{4.5}$$

where λ_{sd} and λ_{sq} are defined in Eq. 4.6 and Eq. 4.7, assuming $\lambda_{rq} = 0$ (rotor d-axes aligned flux model)

$$\lambda_{sd} = \sigma L_s i_{sd} + \frac{L_m}{L_r}\lambda_{rd} \tag{4.6}$$

$$\lambda_{sq} = \sigma L_s i_{sq} \tag{4.7}$$

and $\sigma = 1 - \frac{L_m^2}{L_r L_s}$.

From [16], λ_{rd} is just the time delayed and inductance scaled d-axis current written in the laplace domain as:

$$\lambda_{rd} = \frac{L_m}{1 + s\tau_r} i_{sd} \tag{4.8}$$

Plugging Eq. 4.8 into Eq. 4.6 yields λ_{sd} in terms of only i_{sd}

$$\lambda_{sd} = A(s) i_{sd} \tag{4.9}$$

where,

$$A(s) = \frac{(\sigma L_s + \frac{L_m}{L_r} L_m)(1 + \frac{\sigma L_s \tau_r}{\sigma L_s + \frac{L_m}{L_r} L_m} s)}{(1 + s\tau_r)} \tag{4.10}$$

and

$$\tau_r = \frac{L_r}{R_r} \tag{4.11}$$

Substituting λ_{sd} (Eq. 4.9) and λ_{sq} (Eq. 4.7) into v_{sd} (Eq. 4.4) and v_{sq} (Eq. 4.5) yields:

$$v_{sd} = R_s i_{sd} + sA(s) i_{sd} - \omega_d \sigma L_s i_{sq} \tag{4.12}$$

$$v_{sq} = R_s i_{sq} + s\sigma L_s i_{sq} + \omega_d A(s) i_{sd} \tag{4.13}$$

Substituting v_{sd} (Eq. 4.12), v_{sq} (Eq. 4.13), into the original equation for P_{sdq} (Eq. 4.3), then taking the differential with respect to Δi_{sq} and ignoring Δ^2 terms yields Eq. 4.14.

$$\begin{aligned} &\frac{\Delta P_{sdq}}{\Delta i_{sq}} = \\ &-\omega_d \sigma L_s i_{sd} + (R_s + s\sigma L_s) 2 i_{sq} \\ &+\omega_d \frac{(\sigma L_s + \frac{L_m}{L_r} L_m)(1 + \frac{\sigma L_s \tau_r}{\sigma L_s + \frac{L_m}{L_r} L_m} s)}{(1 + s\tau_r)} i_{sd} \end{aligned} \tag{4.14}$$

A more extensive derivation is available in the Appendix B.

Eq. 4.14 is the plant response for the the induction machine machine under power loop control ($\frac{\Delta P_{sdq}}{\Delta i_{sq}}$) Assuming selected machine parameters, the transfer function is shown in Fig. 4.7.

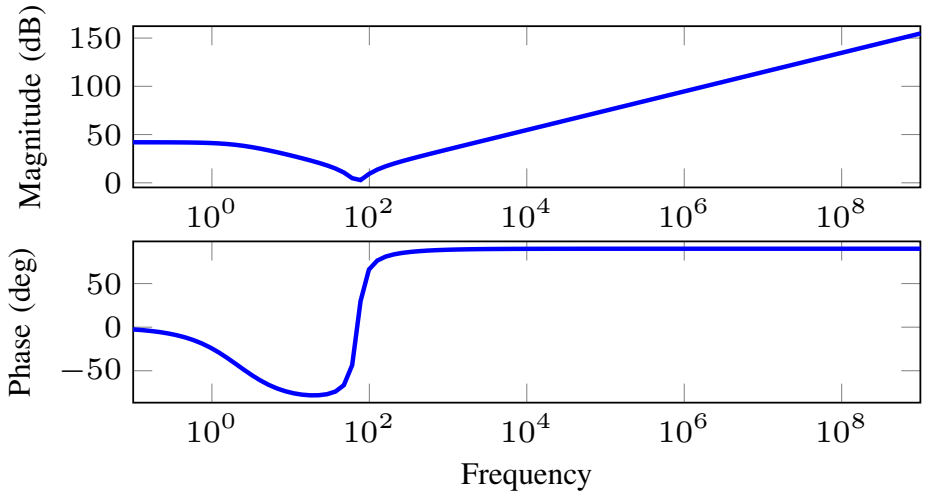

Figure 4.7: Example zero-power control plant transfer function

In the example shown, the plant contains predominately a left-half plane zero, thus is controllable by a single integrator (k_p/s). Adding this integrator and looking at the controller plus plant open-loop transfer function shown in Fig. 4.8. It can be seen that the gain margin remains finite at high at high-frequency. This is not optimal however

it is unlikely to result in significant noise coupling due to unmodeled high frequency poles in the sensors and digital-to-analog converters (1MHz). If high frequency noise coupling is noticed in the control system, the addition of a high-frequency pole to the controller should remain stable and reject the noise.

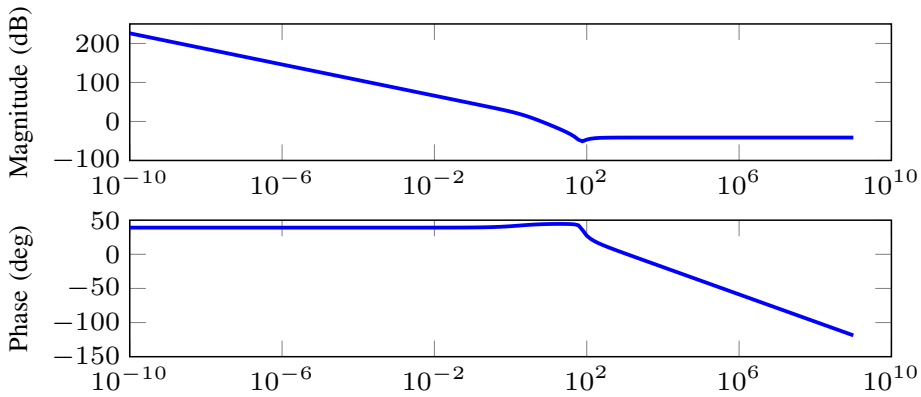

Figure 4.8: Example zero-power control open-loop transfer function with controller

Now that a plant transfer function has been obtained and a controller has been identified, the implementation of a ride-through scheme utilizing this control method can be realized.

The benefit of controlling for zero-power is two-fold. First, the motor will support its own losses based entirely on its own inertia. Second, the voltage source, discussed in Subsection 4.1.1, does not need to support any real power transfer. In addition, due to the orthogonal nature of field-oriented control one can maintain a constant flux in the motor independent of the power control loop. The usefulness of this feature will be discussed further in the ride-through sequencing and control (Subsection 4.2) of the dissertation below.

4.1.3 Reconnecting to the Grid

When the fault clears, the matrix converter must be reconnected to the grid. The voltages on the grid side of the disconnect switch are different than the voltages on the matrix converter side. Both sides of the switch have a moderate sized capacitor on them, see Fig. 4.3. If the input switches should be reconnected arbitrarily, a large

current will flow causing an over-current fault and potentially damaging the switch.

In order to facilitate a description of the reconnect strategy, t_d will be defined as the time at which the input switches are disconnected from the grid and t_c is the time at which the grid has returned to 3-phase balanced sinusoids and the fault has cleared. The node voltages for all three phases are denoted as V_{ga}, V_{gb}, V_{gc} (the grid side) and V_{ma}, V_{mb}, V_{mb} (matrix converter side) of the disconnect switch.

An example simulation is shown in Fig. 4.9, where $t_d = 0.07$ seconds and $t_c = 0.013$ seconds.

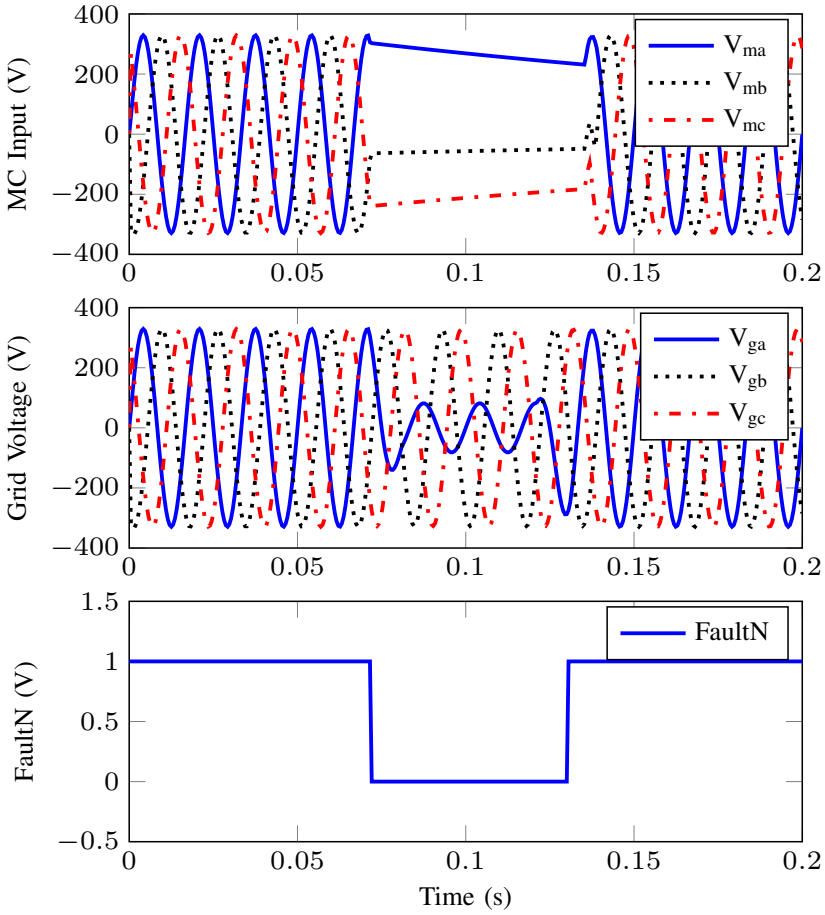

Figure 4.9: Grid and capacitor voltages during fault event

At t_d, the matrix converter inputs cannot be assumed to be balanced. In addition,

as the fault progresses there will be small reductions in the isolated matrix converter voltages due to sensor network losses and other similar non-idealities. Due to these issues, $V_{m,abc}(t_c)$ cannot be assumed to be three-phase balanced voltages. It is unlikely there will ever be a point in time when all three phases simultaneously match such that all three disconnect switches can be closed simultaneously. Furthermore, reconnecting at the wrong time could result in a total voltage collapse at the input terminals of the matrix converter. This would cause the motor currents to become uncontrolled, triggering faults and a loss of synchronism.

Thus to determine the best time to reconnect the three disconnect switches, the following three conditions must be met:

1. Over-currents do not occur,

2. The virtual DC bus voltage should not decrease, and

3. Minimize reconnect time

It is assumed that $V_{g,abc}(t > t_c)$ are sinusoidal and balanced with an A-B-C phase order. $V_{m,abc}(t_c)$ are assumed to be nearly DC with an amplitude less than $V_{m,abc}(t_d)$.

In order to facilitate the reconnect methodology, the case where $V_{ma} > V_{mb} > V_{mc}$ is analyzed. In this case, the matrix converter is operating on only the V_{ma} and V_{mc} phases. As stated from the second requirement above, the voltage between these two phases cannot be allowed to reduce during the reconnect event otherwise the operation of the matrix converter may be impacted. For this to remain true, the highest-phase (A-phase) must reconnect while V_{ga} is increasing and the lowest phase (C-phase) must reconnect while V_{gc} is decreasing. The first requirement can be met by reconnecting each phase only when $V_{gx} \approx V_{mx}$. Restated, the phases will reconnect near zero voltage switching (ZVS) conditions.

Mathematically stated, the A-phase requirements are:

$$\frac{\delta V_{ga}}{\delta t} > 0 \tag{4.15}$$

$$V_{ga} - V_{ma} \approx 0 \tag{4.16}$$

The C-phase requirements are:

$$\frac{\delta V_{gc}}{\delta t} > 0 \tag{4.17}$$

$$V_{gc} - V_{mc} \approx 0 \tag{4.18}$$

The middle phase is less critical and only needs ZVS to occur:

$$V_{gb} - V_{mb} \approx 0 \tag{4.19}$$

These requirements fundamentally define the best time to connect each phase individually. Due to the fact that these requirements occur each cycle, the reconnection must occur in a specific order to guarantee the second and third requirements. For the case $V_{ma} > V_{mb} > V_{mc}$, the correct connection order is ACB. If the switches were to reconnected in the CAB order, then there would be approximately $\frac{5}{6}$ of a cycle where only one phase is connected. This would result in a prolonged common-mode voltage excursion and a total collapse of the virtual DC bus.

Shown in Fig. 4.10 is a detailed simulation zoomed in on the grid reconnect period.

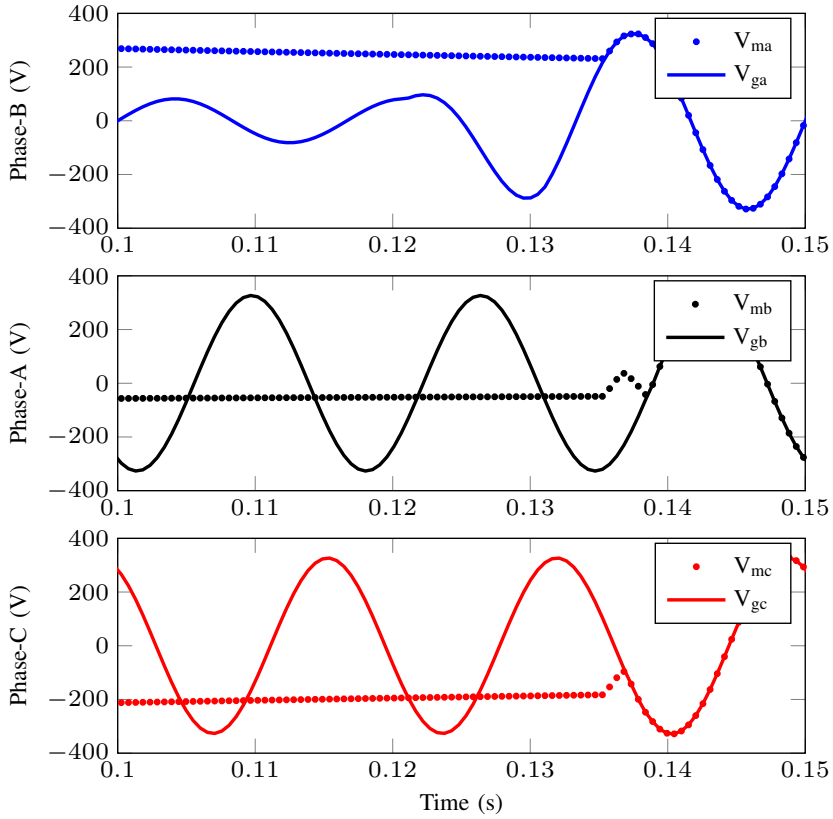

Figure 4.10: Grid and matrix converter voltages during reconnections

During a proper reconnect there is a short common-mode excursion as the first phase is connected, before the third phase is connected. However, this excursion is of the same order as the common-mode signal that results due to single phase fault. An example simulation is included below in Fig. 4.11.

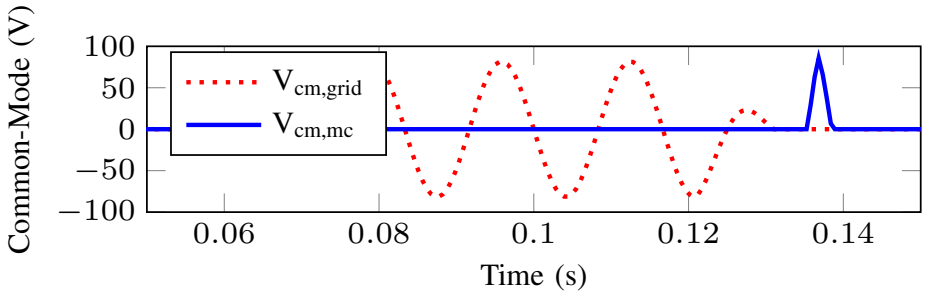

Figure 4.11: Example of common-mode voltage during single phase fault event

4.2 Ride-Through Sequencing and Control

To successfully handle a ride-through event, there are a number of criteria that must be met [13]:

1. Limit excessive currents,
2. Minimize the disturbance to the load,
3. Maintain the required flux magnitude and alignment information, and
4. At the end of fault re-accelerate the motor

Ride-through requires the system to accurately detect a fault in the grid. This could be done in a number of ways, but investigation into optimal fault detection in 3-phase systems is outside the scope of this work. For the purposes of this paper, it is assumed that fault detection is in place. A fault is declared in the event any single phase drops below 0.9pu of rated voltage amplitude.

When a fault is detected, the system will open the input switches and switch to zero-power control mode. The system maintains a constant flux by utilizing the system inertia. When the fault event clears, the input switches are closed and control is handed back to the speed controller. Both transitions require appropriate resetting of the integrators during mode transitions.

During fault operation, the matrix converter switching strategy is implemented as an indirect drive with active rectifier front-end. This allows for the absolute maximum

available voltage to be made available for the motor driver output during fault events. No attempt to generate sinusoidal currents is possible in fault situations, due to the non-sinusoidal natures of the input voltages. During normal operation, any modulation strategy may be employed with this solution. The matrix control need only be switched between normal and fault modes at the time of the fault.

In the event that a very high output torque (i_{sq}) is present, it may be preferable to add an intermediate phase where torque is brought to zero in rate limited manner, before handing control over to the zero-power controller. Alternatively, the reset value on the power-controller could be calculated in advance. In the simulations below, it was found unnecessary to include the zero torque stage. A direct handoff to the zero-power controller was implemented without problems.

4.3 Full System Modeling Results

Simulations of a 3-phase induction motor, matrix converter, and input disconnect switches were completed. The machine parameters utilized are listed in Table 4.1.

Table 4.1: Motor Parameters

P	1 HP
V	230 V
p	4 poles

R_s	3.96 Ω
R_r	2.45 Ω
L_{ls}	7.4 mH
L_{lr}	11.1 mH
L_m	162 mH

An average-model matrix converter [24, 15] was utilized. This model was a reasonable choice for 5-20 second mode switching and control simulations, where switching characteristics are not needed and lead to much longer simulation times. MATLAB Simulink was used to simulate the motor model and control systems. The integrated version of the PLECs simulator was used to simulate the power electronics. The motor was operated during a single phase 0.1pu fault of 0.5 second at an initial speed of 90

rad/s. The inertia utilized in the simulation was approximately that of the induction motor, the DC motor, and the coupling used for characterization.

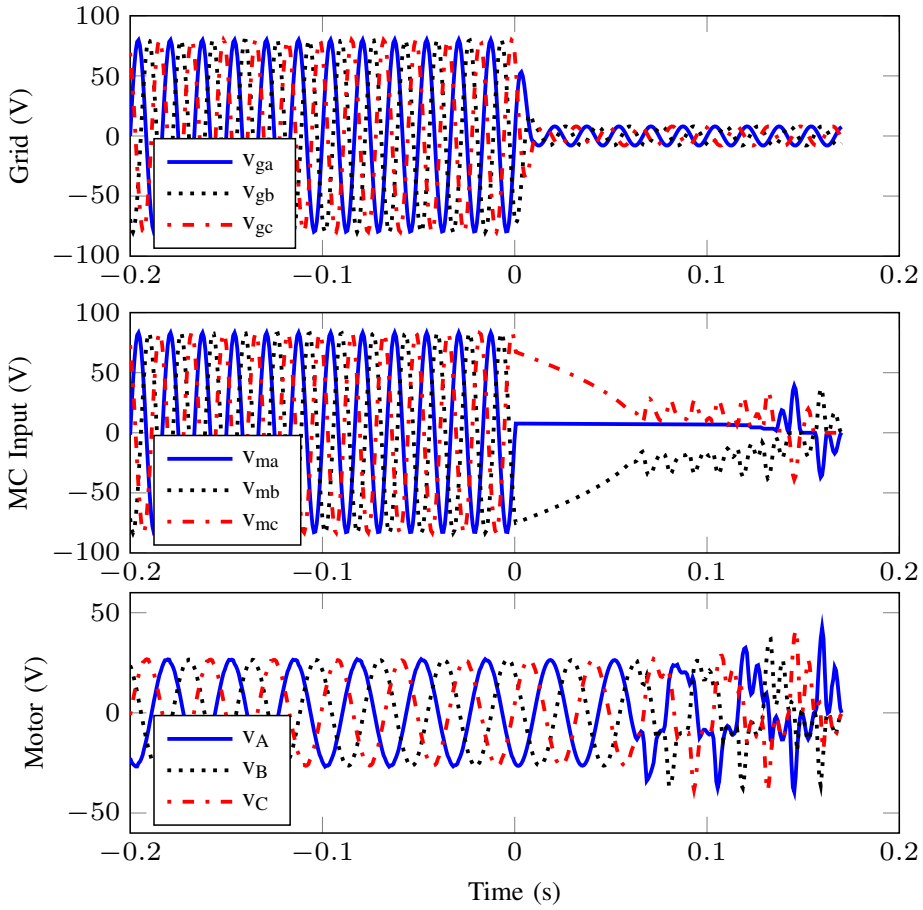

Figure 4.12: No ride-through control: Zoomed in terminal voltages of a 0.5 second 3-phase fault

The simulations shown in Fig. 4.12 and Fig. 4.13 contrast the addition of zero-power control. The simulation shown in Fig. 4.12 shows a normal matrix converter-driven, speed-controlled motor in the presence of the grid fault. As can be seen, the matrix converter input voltage collapses within 0.05 seconds. Control of the motor is lost due to the inability of the matrix converter to provided the commanded voltages to the motor.

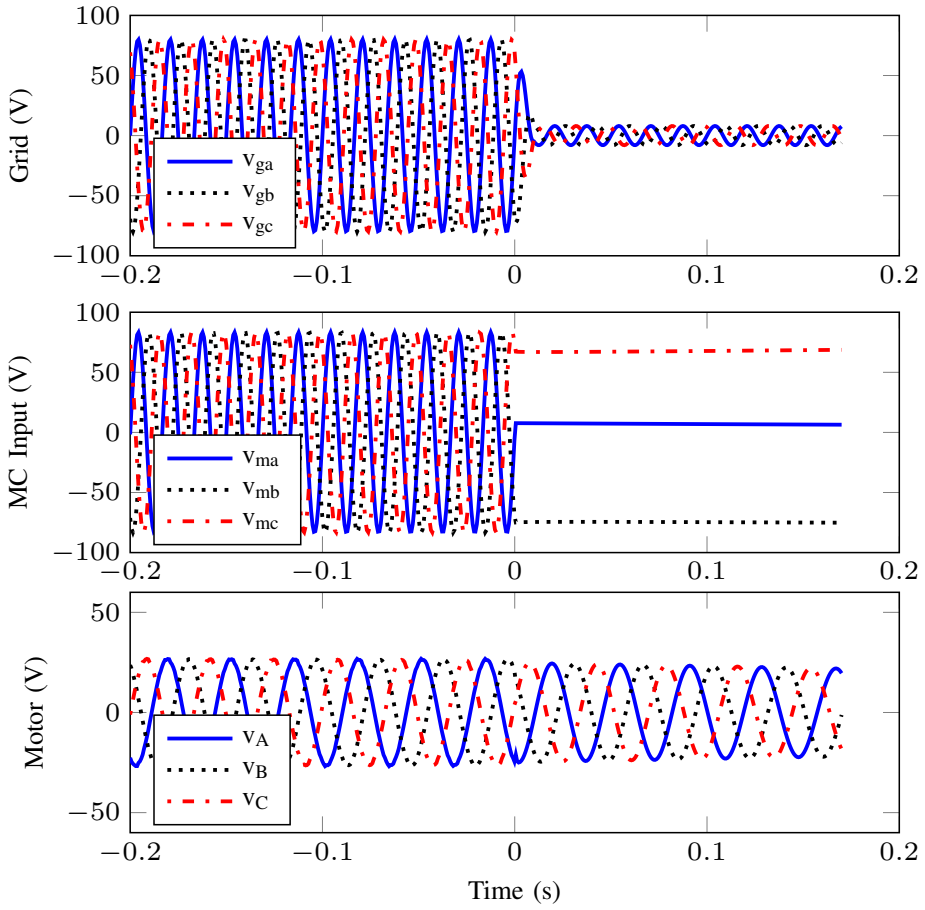

Figure 4.13: Proposed ride-through control: Zoomed in terminal voltages of a 0.5 second 3-phase fault

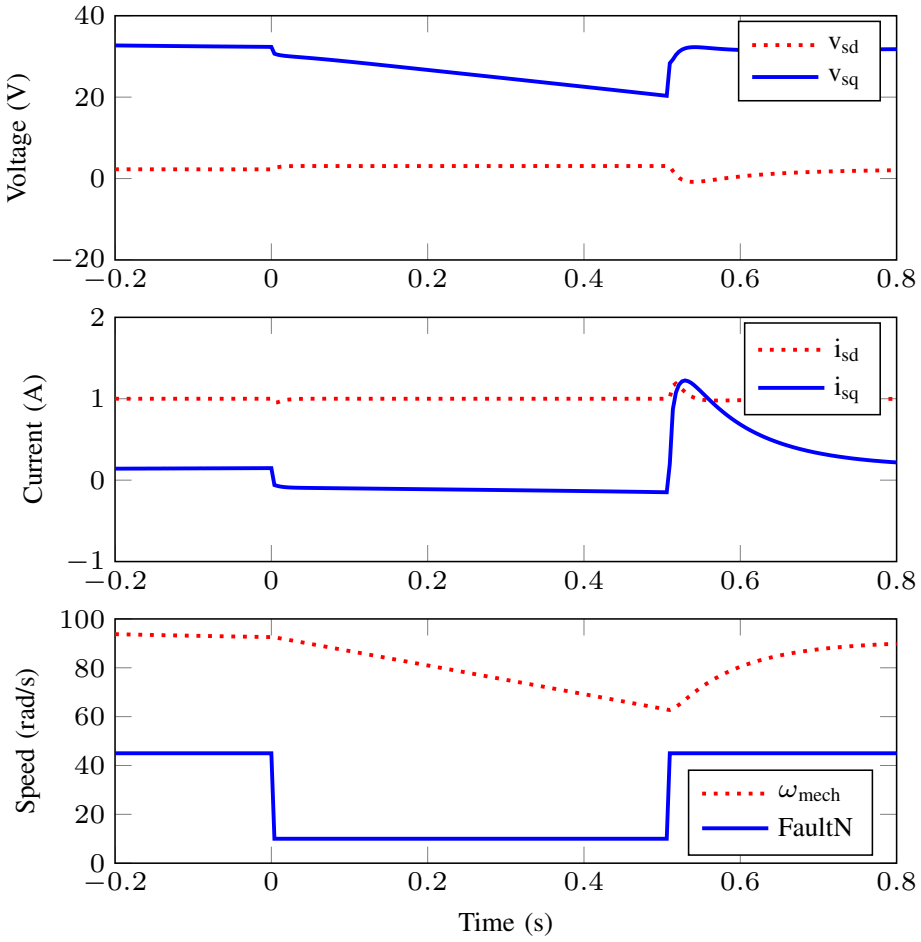

Figure 4.14: Proposed ride-through control: Vector control parameters of a 0.5 second 3-phase fault

Returning to the proposed solution, Fig. 4.13 shows the response to the same 0.5 second fault, but with the full proposed ride-through solution. The vector control quantities are shown in Fig. 4.14. Torque goes from positive to slightly negative keeping the capacitor voltage from collapsing. The proposed solution resulted in a loss of speed of 30 rad/s over the duration of the fault. It can be seen that during a grid fault with a long duration, the system is limited by the total inertia available to the system.

4.4 Experimental Results

The hardware consists of several independent components, listed below:

1. Input disconnect switches and filter,
2. Matrix converter with indirect drive modulation scheme,
3. 1HP DC motor coupled to 1HP AC induction machine,
4. DC motor driver and controller,
5. Fault sequence controller, and
6. Control loop hardware

The disconnect board is implemented with IGBT switches and contains the input side 10% capacitors. The filter components are discrete, as are the grid side voltage sensors. The matrix converter board is realized by IGBTs switches and contains the matrix converter input voltage sensors and output current sensors. The matrix converter modulation scheme is implemented on FPGA1 utilizing XILINX ISE. The disconnect logic, safety logic, and DC motor driver controller are implemented on FPGA2 utilizing XILINX System Generator. Finally, the control loops are implemented by a DSPACE DS1104 rapid prototyping system utilizing MATLAB Simulink.

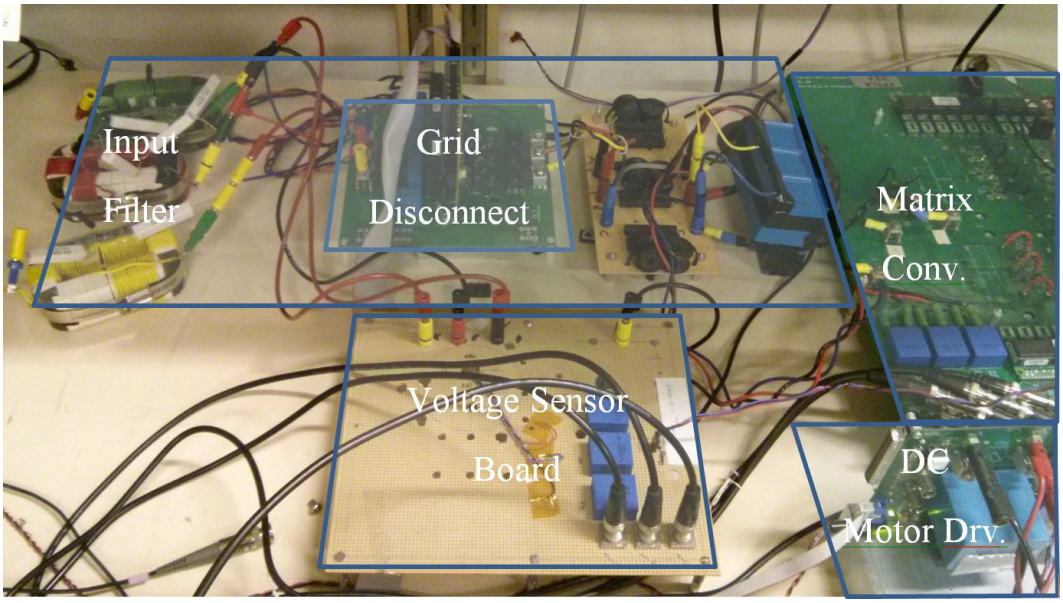

Figure 4.15: Photo of experimental hardware: Input filter, disconnect board, and matrix converter

The motors are a Baldor VECTOR Drive induction motor and a Leeson permanent magnet DC motor.

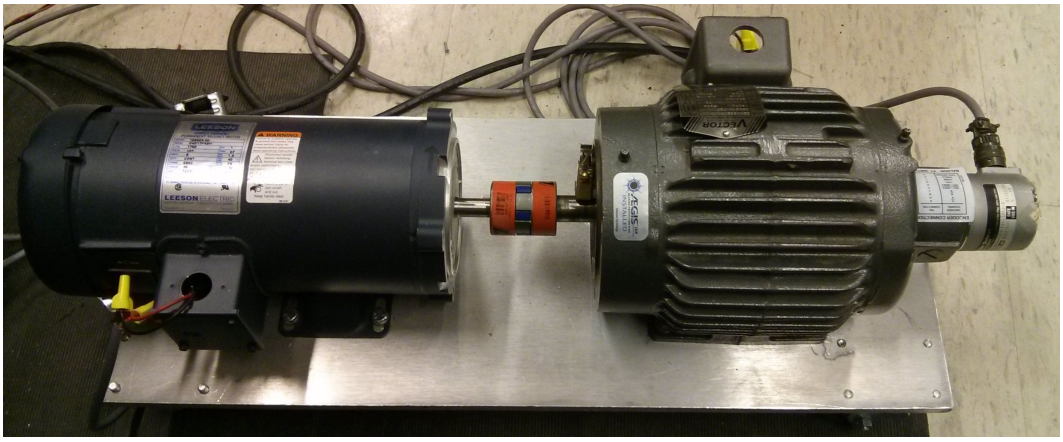

Figure 4.16: Photo of experimental hardware: 1HP motors

A 0.5 second grid fault is created by the input grid disconnect switch, during which the DSPACE controller is given a signal to switch into ride-through mode. The control

mode switches to zero-power control and waits until the fault is declared over. The reconnect logic then takes over and sequentially reconnects the phases of the matrix converter. When the reconnect is complete, the DSPACE controller is switched back into normal operation.

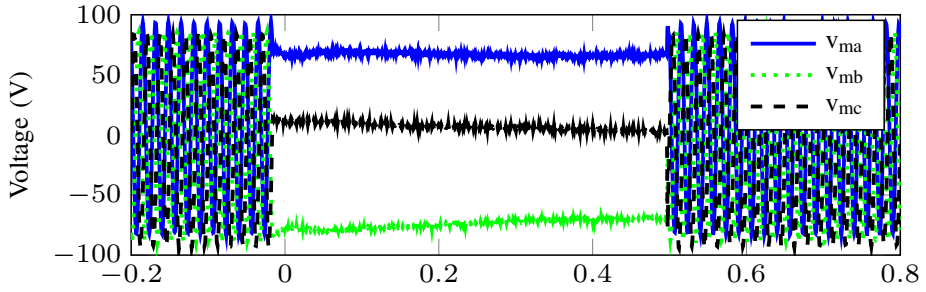

Figure 4.17: Experimental results: Matrix converter input voltages during a 0.5 second fault and recovery

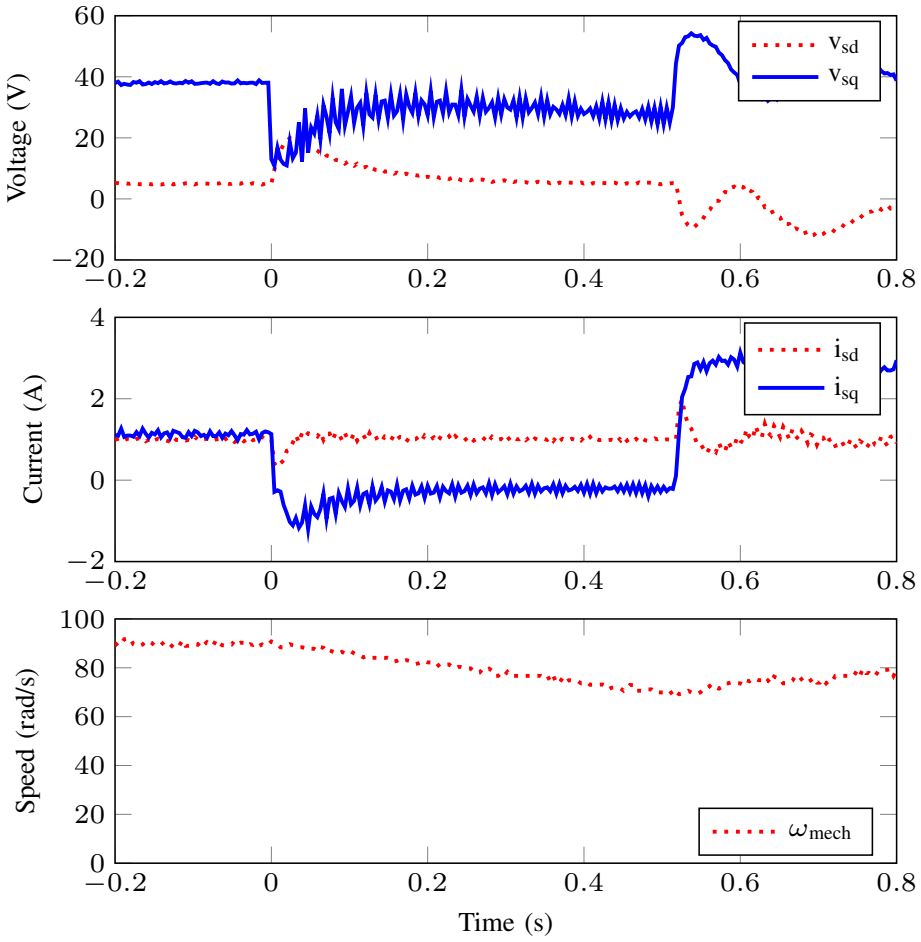

Figure 4.18: Experimental results: Vector control parameters during a 0.5 second fault and recovery

In the 3-phase waveform, there is a transient response due to the system's initial positive i_{sq} that must rapidly slew to slightly below zero, resulting in overshoot. The available voltage on the capacitor has an integrated component due to this dynamic response of the power loop, thus a voltage limiter may be needed. A voltage limiter may also be useful in the case that the speed controller is regenerating energy from the load at the time of disconnect (negative i_{sq}). This extra energy could be limited and utilized to recharge the filter capacitors and extend ride-through duration.

The hardware shows no faults and operates correctly for faults up to 0.5 seconds in duration. This is primarily limited by the inertia available within the tested motors.

Chapter 5

Additional Benefits of Input Disconnect Switches

5.1 Input disconnect switch effects on in-rush currents and over voltage

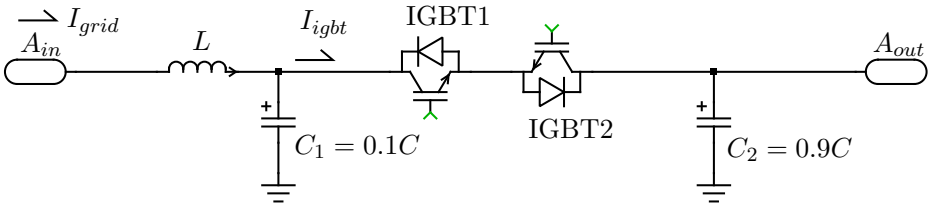

Figure 5.1: Schematic of an IGBT implementation of a single phase of the grid disconnect switch

The input filter disconnect switch schematic is shown in Figure 5.1. It can be seen that the input disconnect switches are normally open (standard operation for most power switches) and therefore block $0.9C_{flt}$ of the filter capacitor from being visible during energization of the motor driver (plug-in). Having a smaller input capacitor ($0.1C_{flt}$) significantly improves in-rush current and overshoot voltage given the same damping resistors around the inductor.

5.1.1 Simulation results

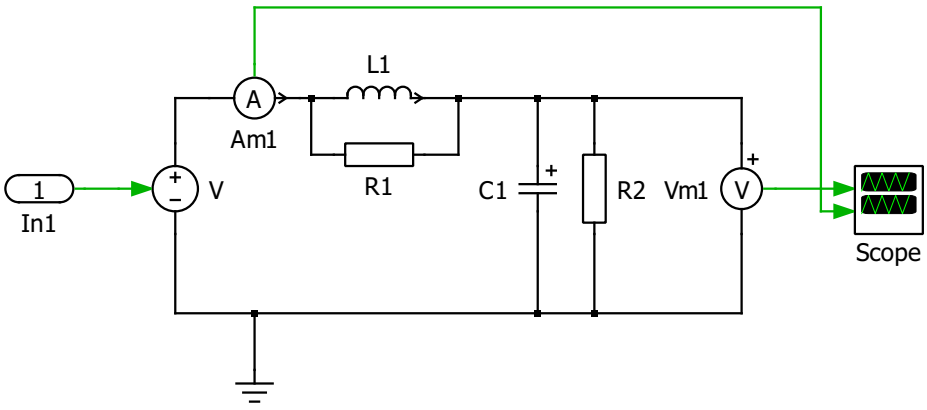

Figure 5.2: Single phase representation of simple LC input filter

Figure 5.2 shows the simulation schematic of the L-C filter with damping resistors. The input $In1$ is stimulated with a step voltage representing the connection of the circuit to a live phase voltage not equal to zero.

Figure 5.3 shows the response of the simplified input filter Figure 5.1, with approximately the designed values of the resistors, capacitors, and inductors.

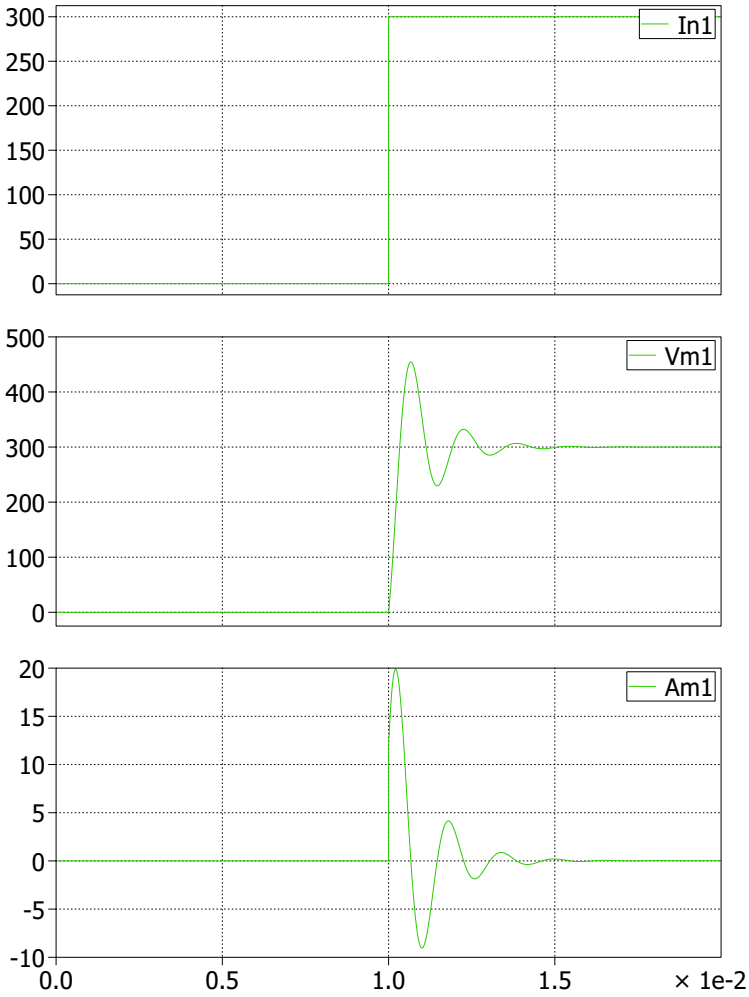

Figure 5.3: Step response of standard input filter ($C_{apparent}$ = 20uF)

This can be compared to the Figure 5.4, where the apparent input capacitor value is reduced by a factors of $C_{ratio} = 0.1$ as implemented in the input disconnect switch filter method of ride-through.

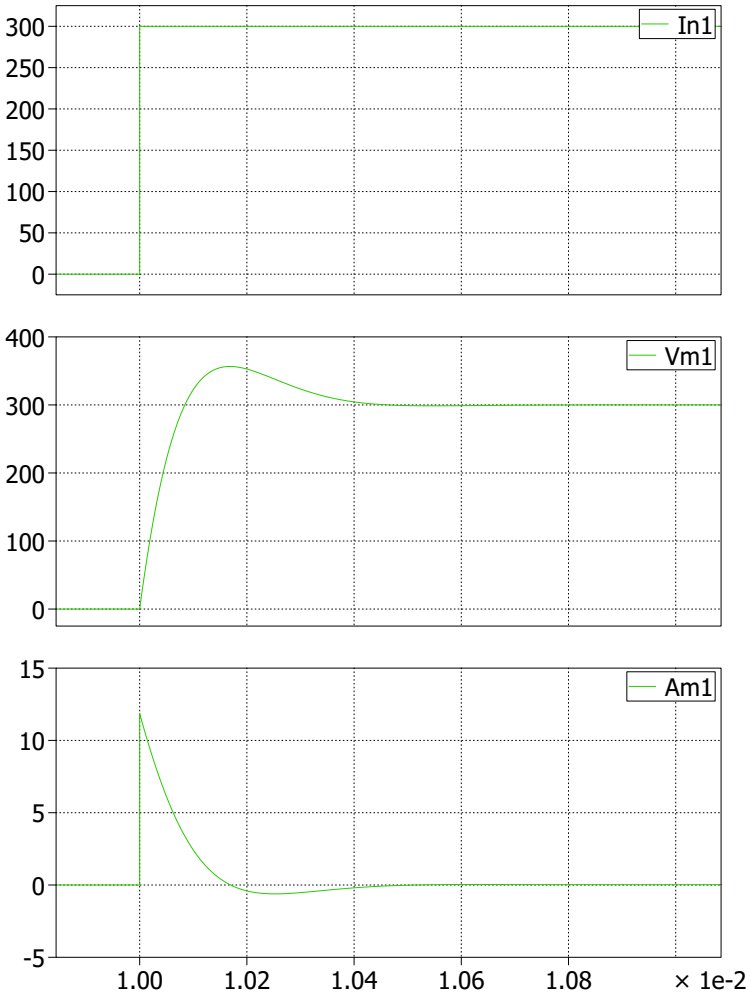

Figure 5.4: Step response of input filter with input-disconnect-switch in place ($C_{apparent}$ = 2uF)

It is apparent in the simulation results that a significant reduction in voltage overshoot is possible with the same losses in damping resistors.

5.1.2 Analytic expressions of overshoot and loss

The input power to a system is P_i and the grid voltage is V_i, then the three phase input current is shown in Equation 5.1.

$$I_i = \frac{P_i}{V_i} \tag{5.1}$$

Since the current will divide equally between L_1 and R_1, the input current through the resistor is simply the resistor divider ratio shown in Equation 5.2.

$$I_{R1} = \frac{sL_1}{R_1 + sL_1} I_i \tag{5.2}$$

The power dissipated in the damping resistor is shown in Equation 5.3.

$$P_{R1} = I_{R1} I_{R1}^* R_1 \tag{5.3}$$

$$P_{R1} = (\frac{sL_1}{R_1 + sL_1} I_i)^2 R_1 \tag{5.4}$$

$$P_{R1} = (\frac{sL_1}{R_1 + sL_1})(\frac{sL_1}{R_1 + sL_1})^* I_i^2 R_1 \tag{5.5}$$

$$P_{R1} = (\frac{w^2 L_1^2}{R_1^2 + w^2 L_1^2}) I_i^2 R_1 \tag{5.6}$$

The power dissipated in the damping resistor P_{R1} is thus inversely proportional to R_1, for $R_1^2 << w^2 L_1^2$.

$$P_{R1} \propto \frac{1}{R_1}; R_1^2 << w^2 L_1^2 \tag{5.7}$$

Since overshoot is dependant on ζ (Equation 5.8), equating two ζ's is sufficient to compare values of R_1 and C_1 with the same overshoot.

$$\%\, Overshoot = 100 e^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}} \tag{5.8}$$

Neglecting R_2, the damping factor (ζ) is equal to Equation 5.9 for the simple RLC circuit depicted in Figure 5.2.

$$\zeta = \frac{R_1}{2}\sqrt{\frac{C_1}{L_1}} \tag{5.9}$$

And thus, for the same overshoot, R is inversely proportional to the square root of C as shown in Equation 5.10

$$\frac{R_1}{R_{1,new}} = \sqrt{\frac{C_{1,new}}{C_1}} \tag{5.10}$$

$\frac{C_{1,new}}{C_1}$ is just the C_{ratio} described in the input filter disconnect switch design. Comparing Equation 5.7 and Equation 5.10 shows that this topology provides a $\sqrt{\frac{1}{C_{ratio}}}$ improvement in filter losses due to the damping resistor R_1.

Chapter 6

Limp-along Mode

6.1 Circuit Description and Operation

During moderate all-phase voltage faults (0.7pu) and major single-phase faults (0pu) there is still substantial energy available from the grid. This energy could be harvested to extend the duration of a successful ride-through.

The reconnect strategy defined in sub-section 4.1.3 allows for connecting two three-phase power systems on the fly. Applying this logic during active use of the converter will reconnect the phases that would benefit from the increasing grid voltage. This is done without transient current or voltage excursion. The end result allows the converter to draw additional power from the grid whenever the phase voltage would be beneficial to the matrix converter.

If the neutral point connection is available, as shown in Figure 6.1, then each individual input phase can be reconnected when it is both at the same voltage as the capacitor (zero voltage switching) and has a beneficial derivative (the most positive phase going more positive and the most negative phase going more negative.) An example of the recharging the a-phase capacitor when the a-phase is at a high voltage is shown in Figure 6.2. It is clear that the ground connection will have to support load level currents in this configuration.

The switch for each phase is now completely independent. Where, the necessary conditions to enable the phase switch are based only on the input phase voltage and the phase capacitor voltage. An example code snippet is shown in Listing 6.1. Clearly

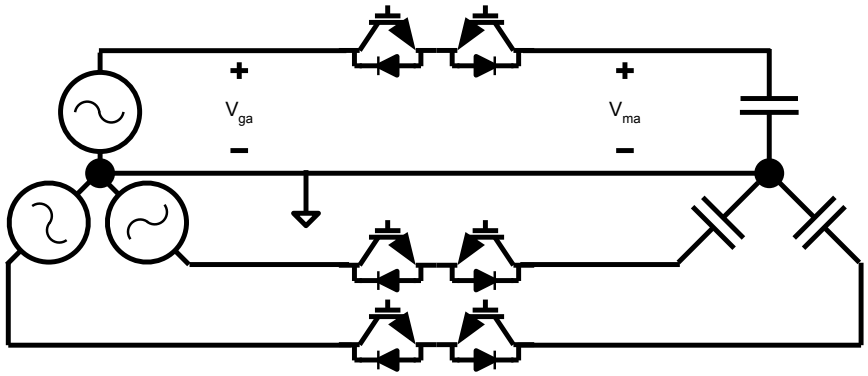

Figure 6.1: Input Filter Isolation with Ground Connection

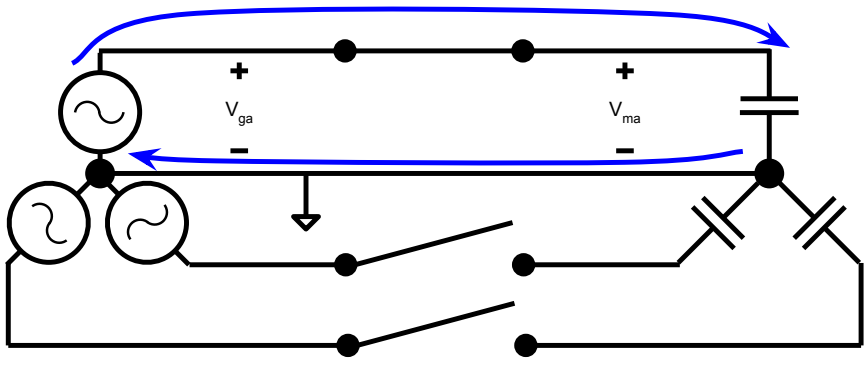

Figure 6.2: Input Filter Isolation with Ground Connection

the state of switch A is only dependant on the voltages $\frac{dV_{ga}}{dt}$, V_{ga}, and V_{ma}.

Listing 6.1: Example code for Vc >Vb case

```
if LimpAlongEn==1
    if dVga>0 && abs(Vga–Vma) < Threshold
        swA = closed;
    end
    if dVgb<0 && abs(Vgb–Vmb) < Threshold
        swB = closed;
    end
    if dVgc>0 && abs(Vgc–Vmc) < Threshold
        swC = closed;
    end
end
```

Ride-through duration can be extended by adjusting the output power in zero-power control mode to a slightly positive value (from zero). Two example simulations, Figure 6.3 and Figure 6.4 are provided that show two different values of power control mode. The control system will need to monitor the DC bus to ensure it remains above the required back EMF of the motor. The current output duty cycle, modulation index, and/or speed of the motor could be used to estimate this target minimum voltage. Since back-EMF is proportional to speed and flux, the amount of energy that can be harvested from the grid will increase as speed decreases, further extending ride-through duration.

Utilizing the code modifications shown in Listing 6.1 and a full speed-control, unlimited ride-through duration was accomplished in simulation with a single phase fault with limited output torque capability. Figure 6.5 and Figure 6.6 show the response of the system to remaining in full speed control mode through all of the fault event. It should noted that this mode, without intelligent oversight, would result in the collapse of the virtual DC bus and resulting complete loss of synchronism if the output power were to exceed the available energy from the grid. However, it clearly illustrates the potential of this mode of operation.

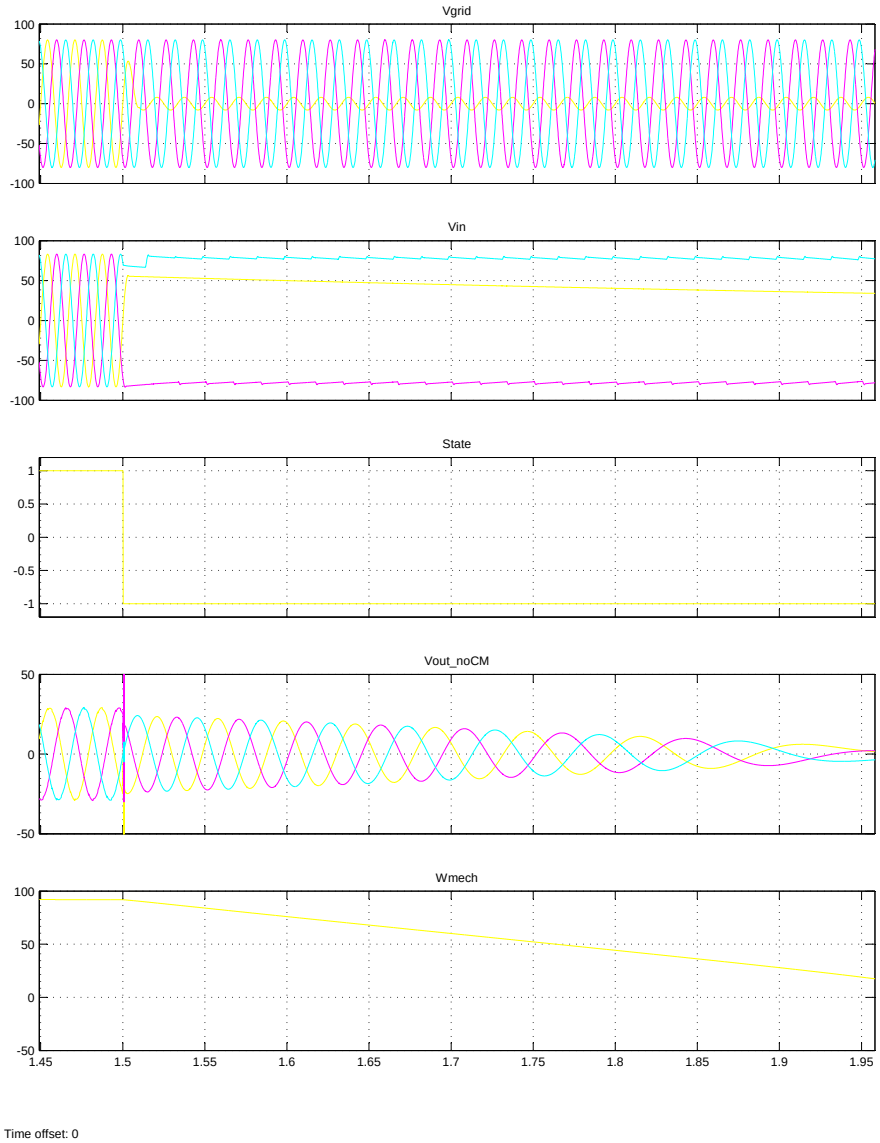

Figure 6.3: Example of Limp-along Mode: Zero/Low Output Power (Zoomed)

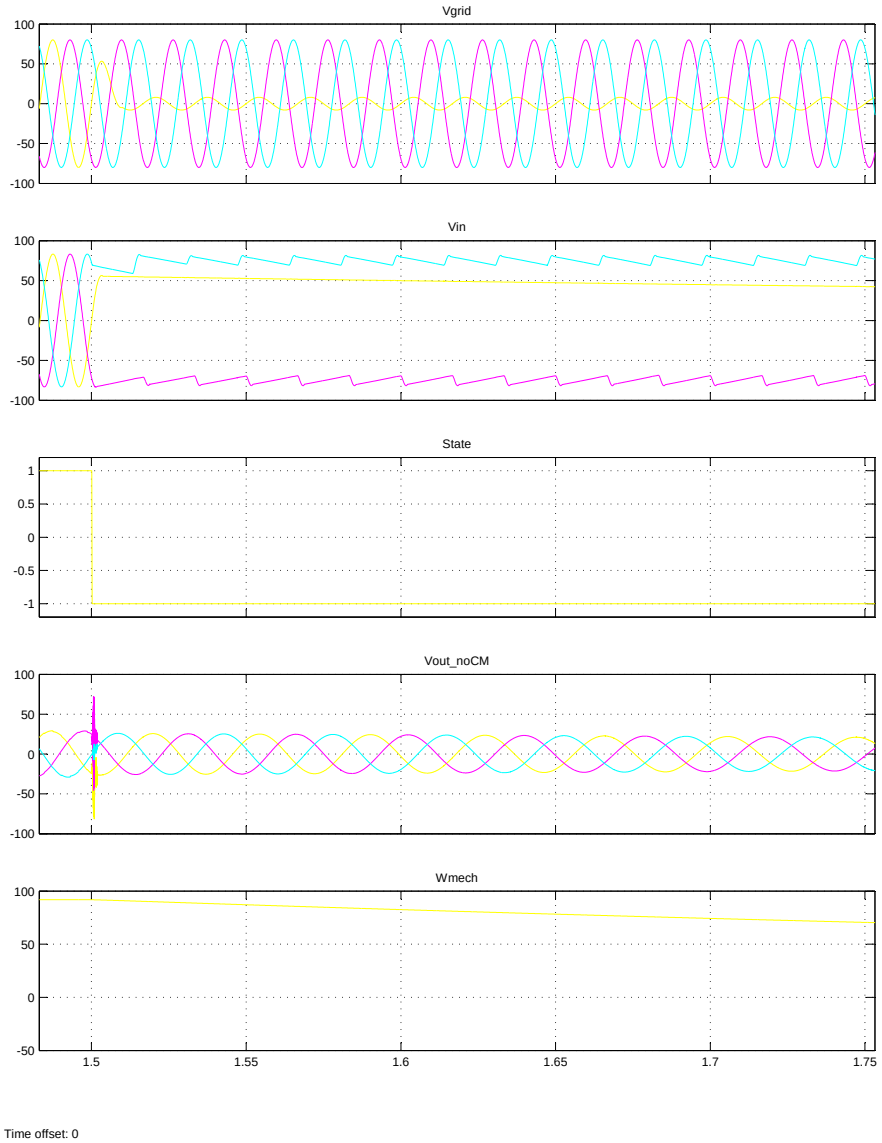

Figure 6.4: Example of Limp-along Mode: Moderate Output Power (Zoomed)

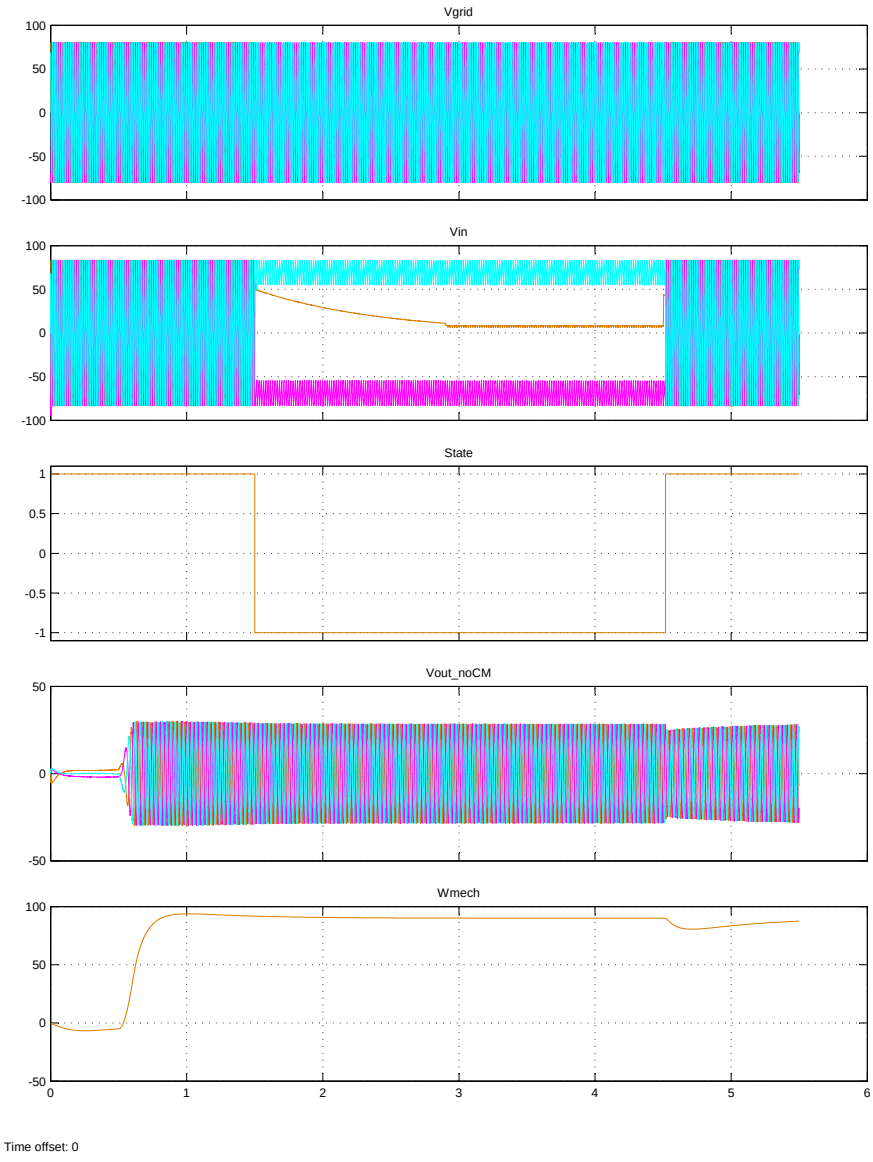

Figure 6.5: Example of Limp-along Mode: Full Speed Control during 2 second grid-fault event

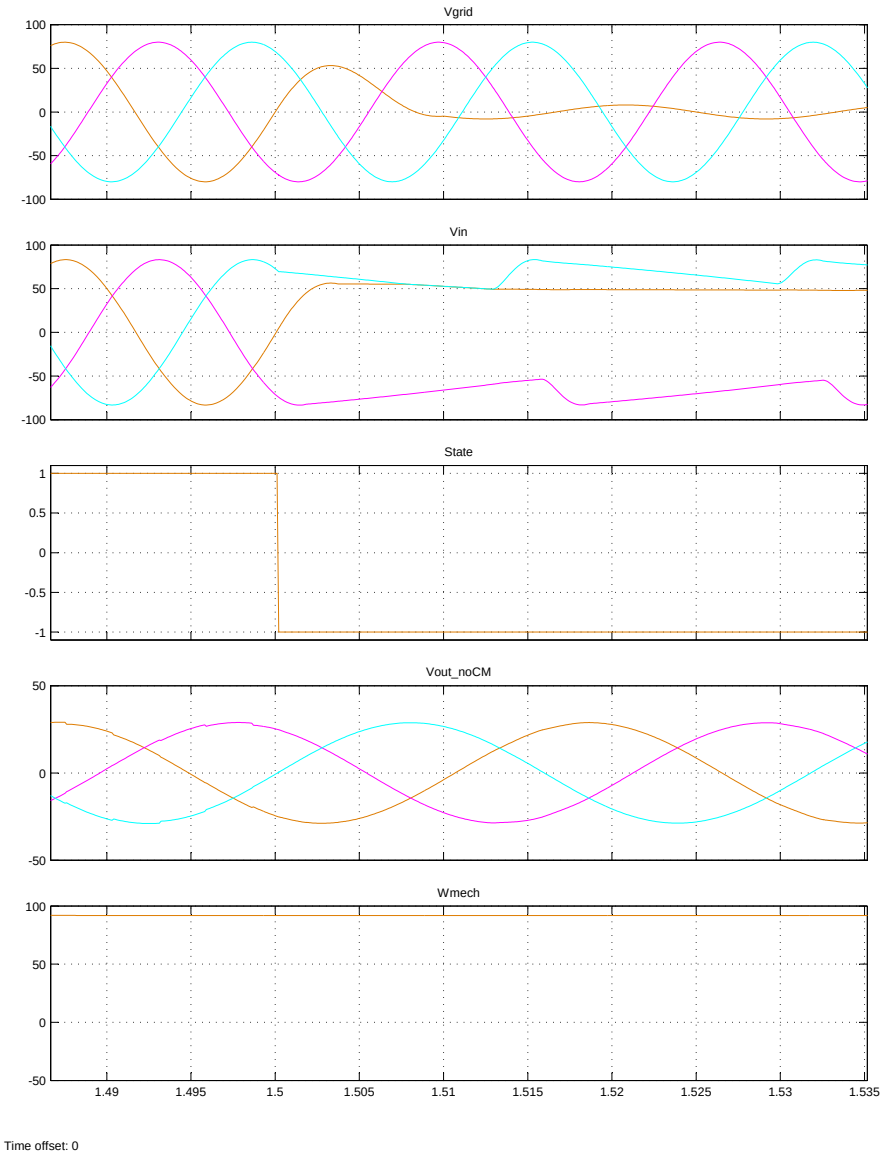

Figure 6.6: Example of Limp-along Mode: Full Speed Control during 2 second grid-fault event (Zoomed)

6.2 Limitations

Until this point the type of filter capacitor has largely been unimportant. A delta or a wye arrangement of the input filter is workable. However, for limp-along mode to work, the filter must be connected in wye format.

By drawing extra current from the remaining grid phases during fault events the motor may exacerbate the fault (from the perspective of the grid), putting additional stress on already stressed components in the power system (transformers, transmission lines, etc). This stress includes significant harmonic current injection.

It is important to note the power connection must have some short term load current carrying capacity on the neutral wire. Thus, any drive operating in limp-along mode must have a 5 terminal power connection (X, Y, Z, N, and earth ground).

Chapter 7

Conclusion

This dissertation established the value of adjustable speed drives and the advantages of matrix-converter-based adjustable speed drives. While matrix converters have several advantages one of the challenges to wider adoption was identified as a lack of fault ride-through support. A literature review of matrix converter ride-through capabilities was completed. A number of existing solutions to enabling fault ride-through were identified. However, existing solutions either focused on adding energy storage devices, involved non-linear control, and/or provided only uni-directional power flow. The need for a silicon only solution with bi-directional power flow was realized.

This work has shown a novel method for sustaining a matrix converter-based adjustable speed drive through grid fault events. This method of ride-through utilizes the input capacitor to transfer energy from the spinning inertia of the motor into sustaining the flux inside the motor. This energy transfer is done with zero power drawn from the input port. Thus even the relatively small capacitors of the input filter can replace the grid voltage source for a short period of time. This method allows the controller to continue tracking the motor position and flux vector position, eliminating the need to stop and restart the motor after a brief grid fault event. The fault ride-through potential is limited only by the available inertia in the motor system. Simulation and experimental verification of this method was completed. The duration due to inertial energy was shown to be around 0.5 seconds for a minimal system of induction motor, coupler, and DC load motor. It was shown through grid quality survey results that the solution presented allows coverage of 96% of all faults.

This new method is both robust and applicable to direct and indirect matrix converters (and potentially other converters.) The addition of input disconnect switches has additional benefits enabling a reduction in-rush current, plug-in voltage overshoot, and enables limp-alone mode. Between the improved fault coverage and ancillary benefits the presented solution clearly adds significantly to the available knowledge and capabilities of matrix converters for adjustable speed drives.

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Appendix A

Detailed Simulation Description

The purpose of this section is to describe the details of the simulation side of this thesis to ensure this work can be verified and more importantly re-used such that other matrix converter topologies can more easily be made ride-through capable.

All simulations in this project were done with MATLAB Simulink and the PLECS plugin. This allows for easy simulation of both the control loops and the circuit elements. There are two major branches to the simulations done to verify this work.

The first is the interruptible input filter simulation, this is primarily a circuit simulation to test for transient behavior of the filter components under switching conditions. This simulation is smaller and designed to allow easier iteration of the design. Additionally, due to the faster simulation time it is possible to test disconnect and reconnect events with many varieties of fault delay (time between fault and a-phase peak voltage) and power factor (time between a-phase peak voltage and a-phase peak current).

The second is the full controls simulation with matrix converter. This simulation is much more complicated and can simulate the control loops, input filter, matrix converter, and the mechanical operation of the drive. The primary purpose of the full control simulation is to verify the operation of the control loop mode switching.

The following two sections will go into more detail on these elements.

A.1 Interruptible Input Filter Simulation

The first simulation that is reviewed is the Interruptible Input Filter Simulation. This schematic is primarily designed to verify switching event transients. The top level schematic is shown in Figure A.1 and . No other inputs are required other than the 3-phase sinusoidal source and the envelope of that source to aid fault detection.

The top level model is available under the file name, "Sim07_PaperSims.mdl" and requires the file "Sim07_PaperSims.m" to initialize variables.

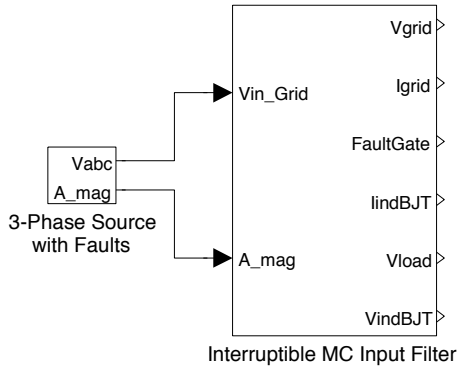

Figure A.1: Interruptible Input Filter: Top Schematic

This top schematic is then broken down into two sub-sections (shown in Figure A.2). First is the control logic (shown in Figure A.3). This is digital control logic that describes how and when to connect and disconnect from the grid on each phase. It consists of inputs measuring grid voltages and outputs controlling the disconnect switches.

As can be seen on the left side of Figure A.3 there are several MATLAB Simulink implemented filter elements for the calculation of the derivative of the input voltage. These filters and derivatives are implemented slightly differently in hardware and software. Both had to be hand tuned to balance noise (lower low-pass frequency) and give relatively low delay (higher low-pass frequency). There is plenty of margin between the sampling rate of the grid voltage measurements (MHz) and the required response rate of the filter (600 to 6k Hz), but care must still be taken to ensure valid operation of the system.

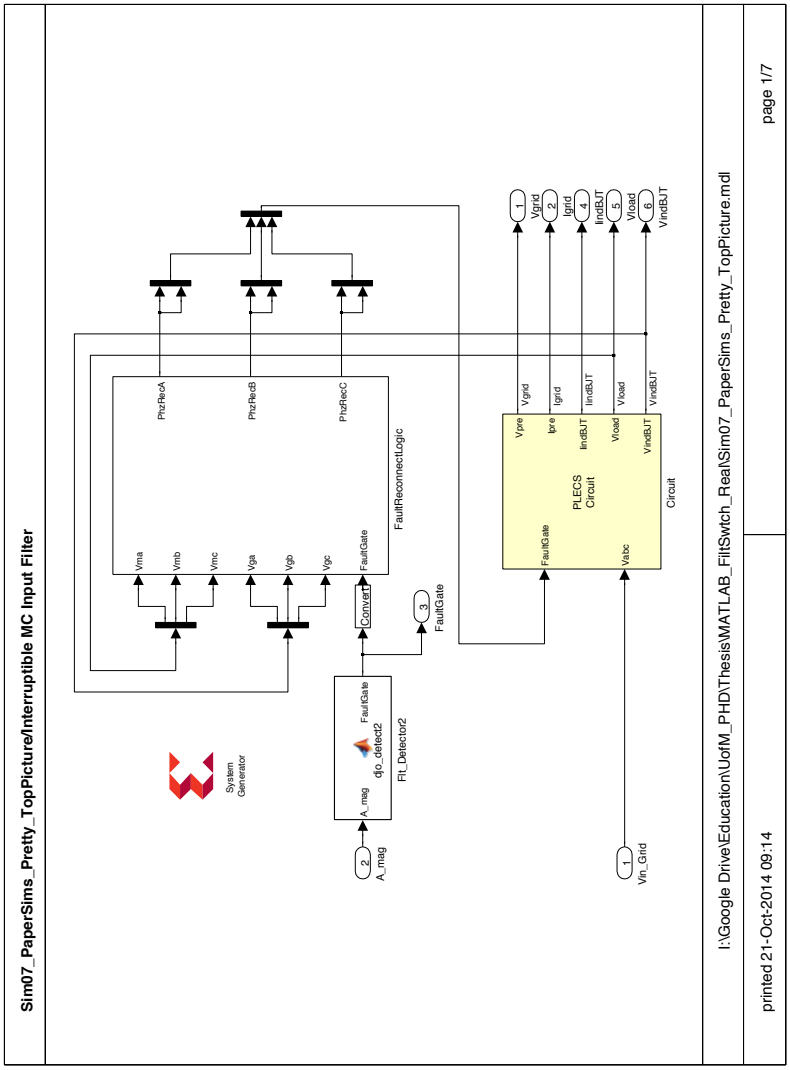

Figure A.2: Interruptible Input Filter: Control Logic and Circuit Model

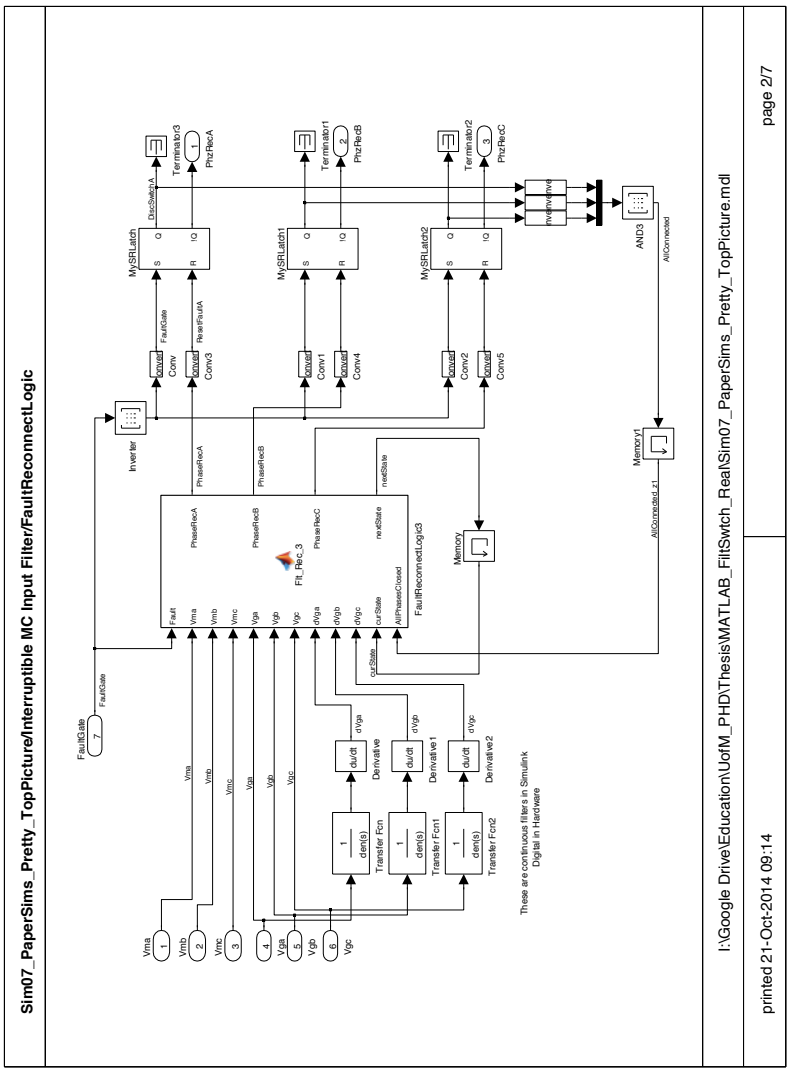

Figure A.3: Interruptible Input Filter: Control Logic

As can be seen on the right side (latches) and beneith the control logic ("Memory" and "Memory1" elements) this design has states and requires some small amount of memory. M-code blocks do not handle memory well, as such the memory elements are handled by Simulink. The M-code block gets called once per solution point in Simulink.

The block labeled "FaultReconnectLogic3" contains the core digital logic and state machine that controls reconnecting of the switches. It is described in a general overview in 4.1.3. It should be noted that the objective of "FaultReconnectLogic3" is to trigger the SRlatchs to reconnect a given phase. The action of disconnecting from the grid is handled directly and immediate upon fault detection. "FaultReconnectLogic3" It has the the following inputs and outputs:

Listing A.1: Fault Reconnect Logic Code

```
1 function [PhaseRecA,PhaseRecB,PhaseRecC,nextState] = Flt_Rec_3(Fault,
      Vma,Vmb,Vmc,Vga,Vgb,Vgc,dVga,dVgb,dVgc,curState,AllPhasesClosed)
```

The fault reconnect logic block "FaultReconnectLogic3" is primarily a state machine. The following states are defined:

Listing A.2: Fault Reconnect Logic Code

```
14     % State 0 = Initialization
15     % State 1 = Normal Operation
16     % State 2 = Faulted
17     % State 3 = Fault Cleared - Waiting to Reconnect 1st Phaze
18     % State 4 = Fault Cleared - Waiting to Reconnect 2nd+3rd Phaze
```

First, the state is updated, constants are defined, and the initial conditions are set. The default state for the reconnect command is for the switches to remain open (zero).

Listing A.3: Fault Reconnect Logic Code

```
20     nextState = curState;
21
22     % Configuration Variable(s)
23     Threshold = 3;
24
25     %Initialization with defaults (don't reconnect)
26     PhaseRecA = 0;
```

```
27      PhaseRecB = 0;
28      PhaseRecC = 0;
```

A switch statement is utilized to select which code block to run for the given state. The states Initialization (State 0), Normal (State 1), and Faulted (State 2) have no active code and just monitor the state of the Fault input variable, switching to the appropriate following state.

State 3, Fault Cleared – Waiting to Reconnect 1st Phase, identifies which sector the input voltage is in and the appropriate phase to reconnect first. If this phase has a beneficial derivative and is within the reconnect threshold (approximately zero voltage) then the reconnect command is issued. This all takes place within a fairly deep if/then structure. An excerpt is shown below.

Listing A.4: Fault Reconnect Logic Code

```
48          case 3  % Fault Cleared, wait for 1st Phase to ZVS
49              % Case 1: A>B>C at matrix converter side
50              if Vma >= Vmb && Vmb >= Vmc
51                  if dVga>0 && abs(Vga-Vma) < Threshold
52                      PhaseRecA = 1;
53                      nextState=4;
54                  end
55              end
56
57              % Case 2: B>A>C at matrix converter side
58              if Vmb >= Vma && Vma >= Vmc
```

Finally the second and third phases are reconnected in State 4, Fault Cleared – Waiting to Reconnect 2nd+3rd Phases. This is done in a similar fashion to State 3 waiting for zero voltage switching, however there is no condition on the next phase to connect and all phases are given the reconnect signal when they pass zero-voltage-switching levels.

Listing A.5: Fault Reconnect Logic Code

```
96          case 4  % Fault Cleared, wait for 2nd and 3rd Phases to ZVS
97              if abs(Vga-Vma) < Threshold
98                  PhaseRecA = 1;
```

```
99              end
100             if abs(Vgb–Vmb) < Threshold
101                 PhaseRecB = 1;
102             end
103             if abs(Vgc–Vmc) < Threshold
104                 PhaseRecC = 1;
105             end
106             if AllPhasesClosed == 1
107                 nextState=1;
108             end
```

AllPhasesClosed is an input from outside the FaultReconnectLogic3 block (shown in Figure A.3). This is the signal that waits until the output of all the SR latches have processed and all phases are reconnected, to initiate the return to normal operation (State 1).

The conversation from MATLAB signals (numerical) to circuit signal sources (current and voltage), occurs at the first level down from the control circuitry. This is shown in Figure A.4. It should be noted that in PLECS you can multiplex circuit wires and that each circuit connection (black wires) at this level has 3-phase.

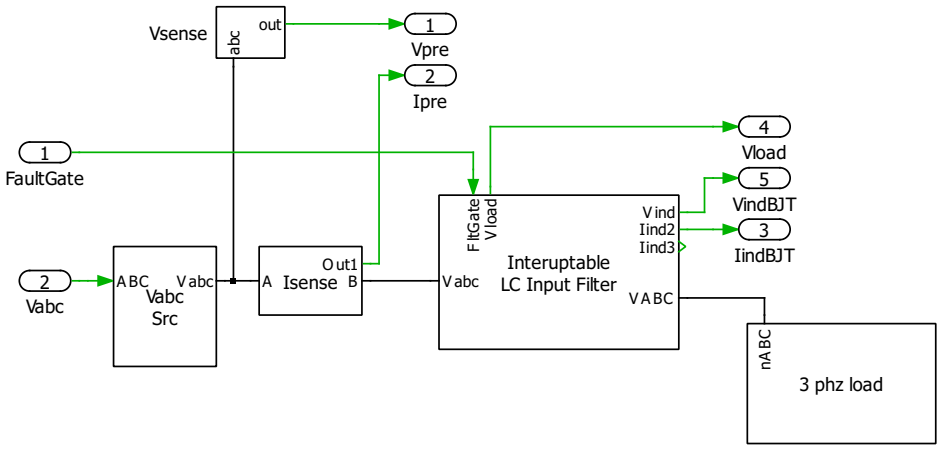

Figure A.4: Interruptible Input Filter: Schematic Top

The core of the schematic simulation is shown next in Figure A.5. Here you can see the 3-phase structure of the full interruptible input filter. Significant issues with

convergence were found throughout this design process. Each of the resistors seen in Figure A.5 and many in the follow figures are utilized to help identify and mitigate convergence issues. Voltage and current sensors are found throughout to allow easy debugging.

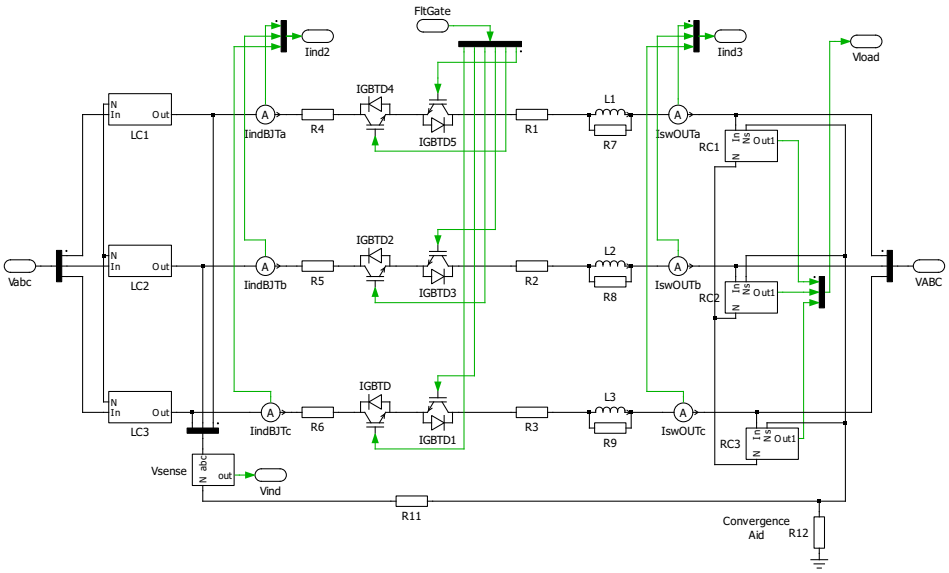

Figure A.5: Interruptible Input Filter: Schematic Core

Due to the schematic getting messy and the need to easily make certain that all three phases were modeled the same, the input LC filter and the output RC filter components are contained in subcircuits. These are shown in Figure A.6 and Figure A.7.

It may be noted that the RC filter component has two neutral connection points. One for the capacitor (N) and one for the voltage sensor resistor divider (Ns). This is one of the finer points of the design. The neutral points can transport current, especially in the case of Limp Along Mode, but also in normal operation during connect and disconnect events. This transient current can disturb sensors and must but monitored to make sure it doesn't get too high.

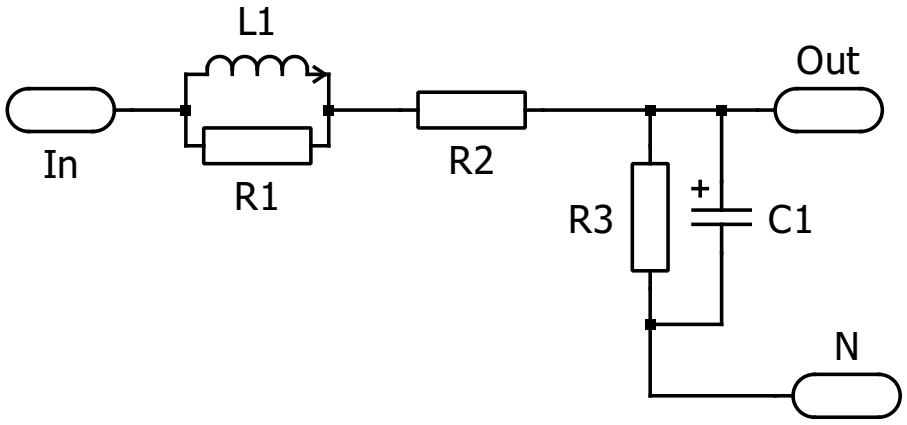

Figure A.6: Interruptible Input Filter: Schematic of LC filter component

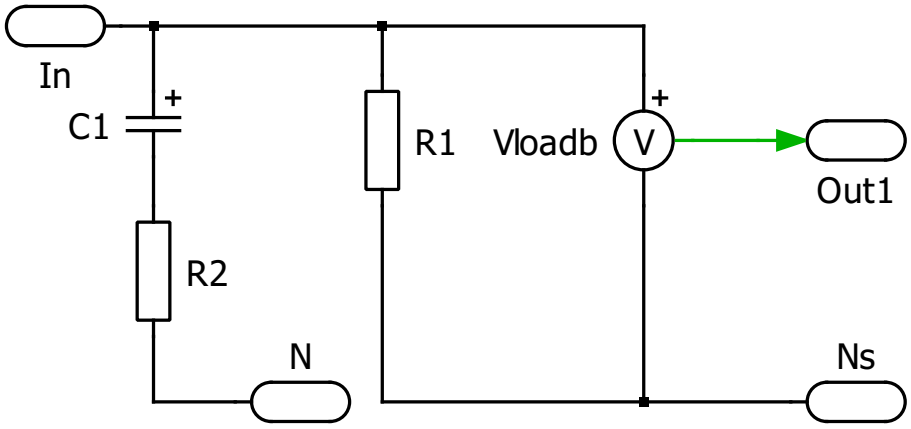

Figure A.7: Interruptible Input Filter: Schematic RC of filter component

A.2 System Level Control Simulation

The second major component of verifying this work is the system level control simulations. These consist of longer simulations (sim time and real time) which attempt to model the full mechanical and electrical response of the system to ride-through events.

The description of this simulation is broken into two parts. The first, in Subsection A.2.1, describes the controls, including state switching and resets. The second, in Subsection A.2.2, describes the circuit level simulations and switching speed logic.

A.2.1 Top Level and Controls

The top level of these simulations is shown in Figure A.8. It can be seen that this is very similar to the standard control architecture shown in Figure 2.7. There is a d-q based control loop that is fed by a PI current controller which is in turn fed by a PI speed controller. This speed controller can be swapped out with the PI power controller by the State Sequencer.

The state sequencer shifts between Speed, Current, and Power control modes via changing its output "State". According to the Table A.1. The state sequencer appropriately resets the integrators such that large disturbances and wind-up are minimized.

Table A.1: Control State Table

1	Speed Control Mode
0	Fixed Current Control Mode
-1	Power Control Mode

It should be noted that no feedforward function ($f()$) is implemented in the i_{sd} control input. For all simulations i_{sd} is just set to a constant.

The CalcPower block causes algebric solution problems and required the addition of a "Transport Delay" element. This has a very short delay of 10us and is only intended to aid in simulation. This is shown in Figure A.9.

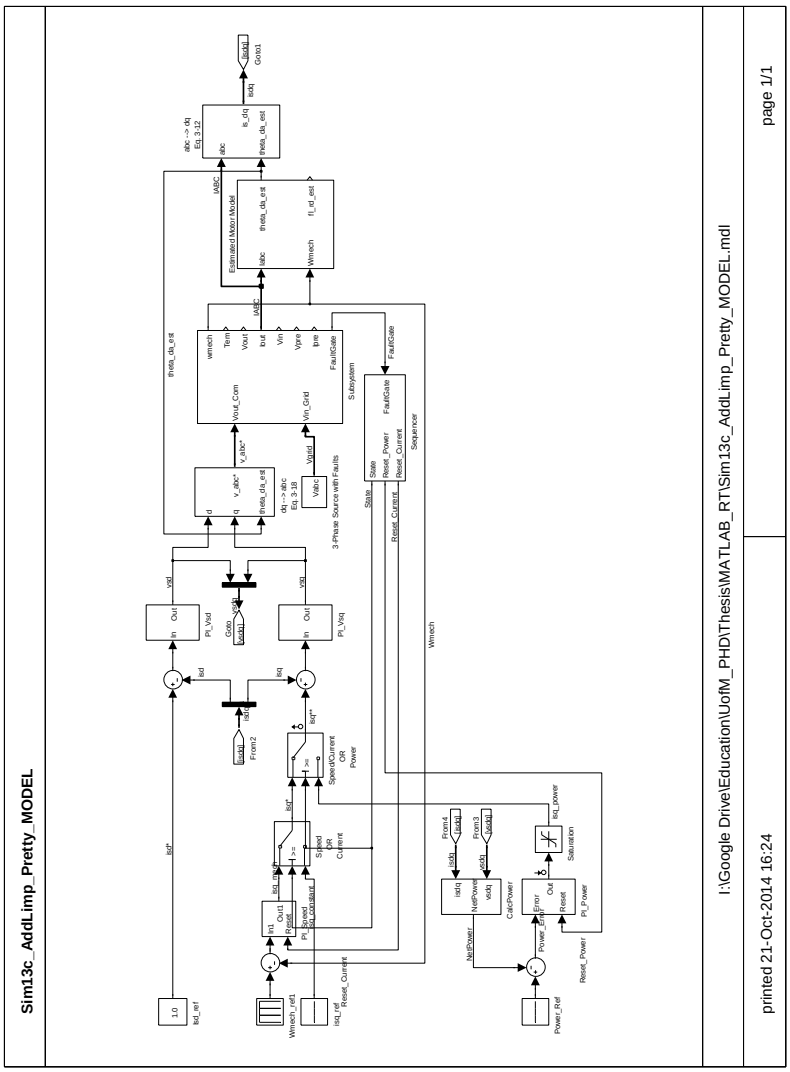

Figure A.8: System Level Control: Top level schematic

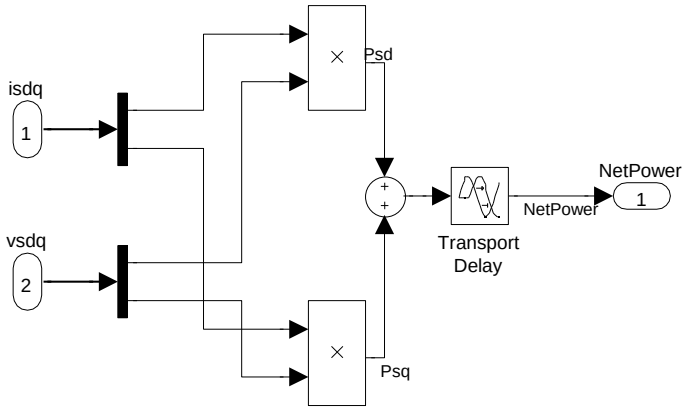

Figure A.9: System Level Control: CalcPower Block

There are four PI controllers implemented in the design. They are implemented with reset, limiter, and continuous time filter options (though the filter is disabled in these simulations). An example PI controller block is shown in Figure A.10. The limiter is critical to both the safety of the system (current limits for example) as well as allowing faster recovery from large excursions. These limits should be picked to remain within the operating points of the system. Table A.2 shows the limits adopted for this particular simulation.

Table A.2: Integrator limits for simulation

Control Variable	Upper Limit	Lower Limit
Power	+200 W	-200 W
Current	+8 A	-8 A
Voltage	$1.5V_a$ V	$-1.5V_a$ V

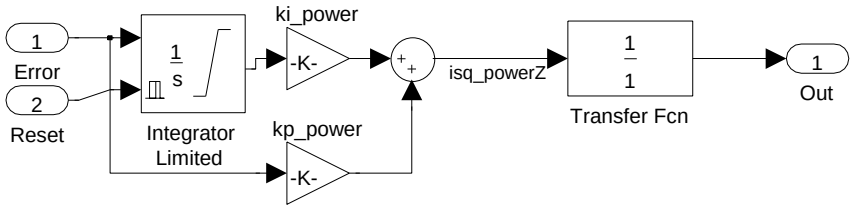

Figure A.10: System Level Control: Example PI Controller

The abc to dq transformation is done using a matrix and the angle difference between the stator a-phase reference frame and the rotor flux aligned d-axis frame. The transforms are shown in Figure A.11 and Figure A.12.

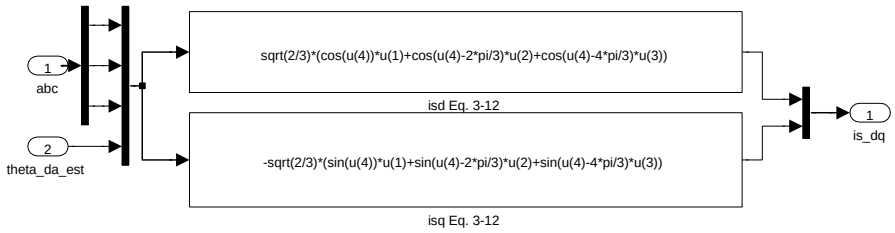

Figure A.11: System Level Control: ABC to d-q transform

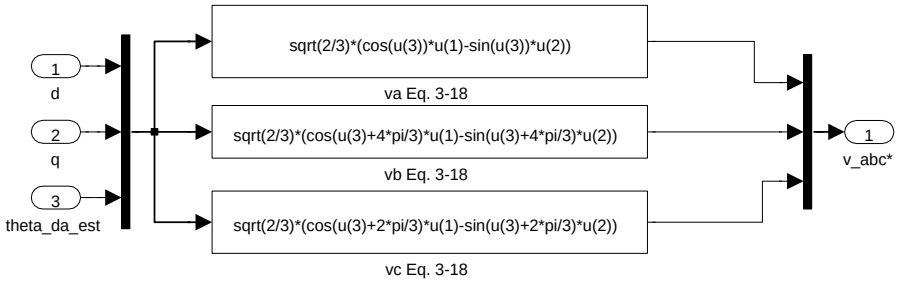

Figure A.12: System Level Control: d-q to ABC transform

One of the more complicated tasks for an induction machine ASD is the determination of the rotor flux angle. This is done by the block "Estimated Motor Model". The implementation of this function is taken directly from Chapter 5-1 in [16]. θ_{da}

is calculated from the motor currents and measured speed as shown in the following equations:

$$\theta_{da} = \int_t^0 \omega_{dA}(\tau) + \omega_m(\tau)\, d\tau \tag{A.1}$$

$$\omega_{dA} = \frac{-L_m}{\tau_r \lambda_{rd}} \tag{A.2}$$

$$\lambda_{rd}(s) = \frac{L_m}{1 + s\tau_r} i_{sd}(s) \tag{A.3}$$

$$\omega_m = \frac{p}{2} \omega_{mech} \tag{A.4}$$

The Simulink model implementation is shown in Figure A.13.

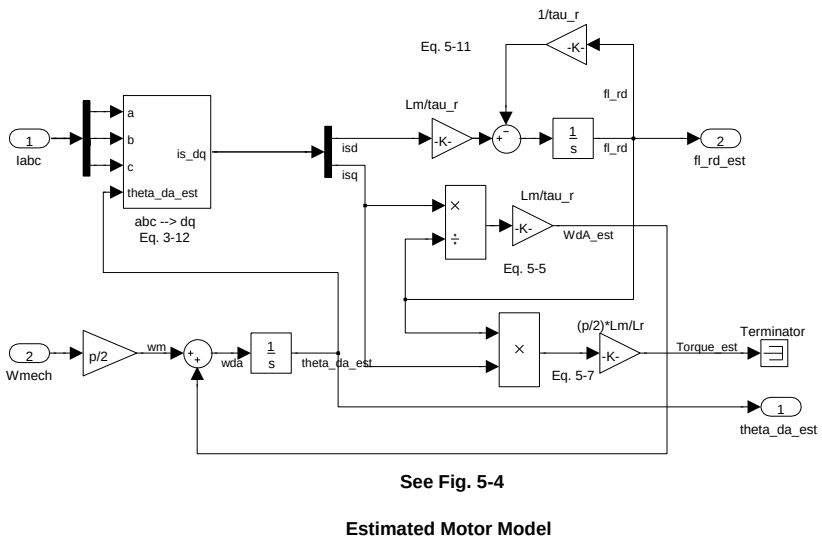

Figure A.13: System Level Control: Motor Estimator

A.2.2 Circuits and Switching Logic

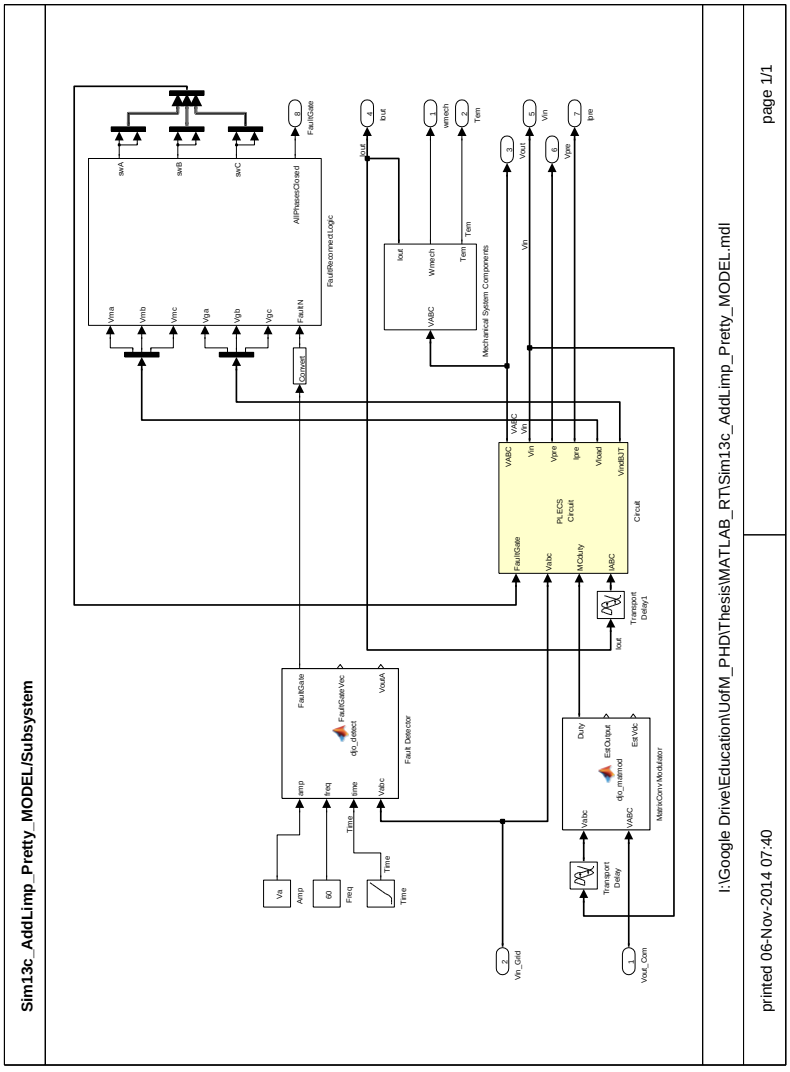

Figure A.14: System Level Control: Primary Subsystem for switching level circuit simulations

The "Subsystem" block in the middle of the Figure A.8 contains the switching level controls, circuit simulations, and actual mechanical induction motor model (vs. estimated). The contents of the "Subsystem" model is shown in Figure A.14.

The "Fault Detector" is implemented as a MATLAB function block. The logic simply flags a fault in the event that the a-phase voltage drops below a threshold percentage of ideal. In general this percentage was between 90% and 99%.

The "FaultReconnectLogic" block is almost identical to the logic block in Section A.1. Please refer to that description for more details.

The "Mechanical System Components" block simply implements the same model as in the Controls level, but at a local level to facilitate mismatched machine/model parameters.

The "MatrixConv Modulator" calculates the matrix converter switch duty cycles. In this case it contains a custom unity-power-factor input current methodology that is highly fault tolerant. This was primarily an exercise of personal interest that doesn't effect simulation results and it could contain standard SV-PWM logic.

The "Circuit" block contains the PLEC simultions elements for the input disconnect switches, an average model matrix converter and load current generating block. It is shown in Figure A.15. At the top level is looks very similar to its sister block in Section A.1, Figure A.5.

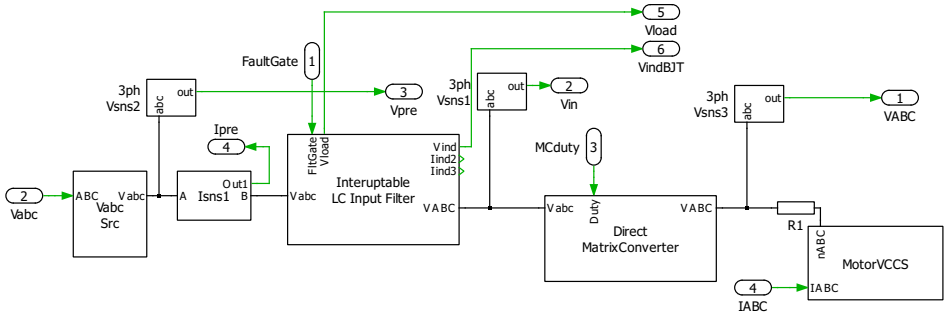

Figure A.15: SLC Circuit: Core circuit diagram

The only difference is in the output load for the "Interuptable LC Input Filter". This load is now an average model direct matrix converter, which in turn is loaded by an voltage-controlled-current-source based on the motor model (shown in Figure A.16).

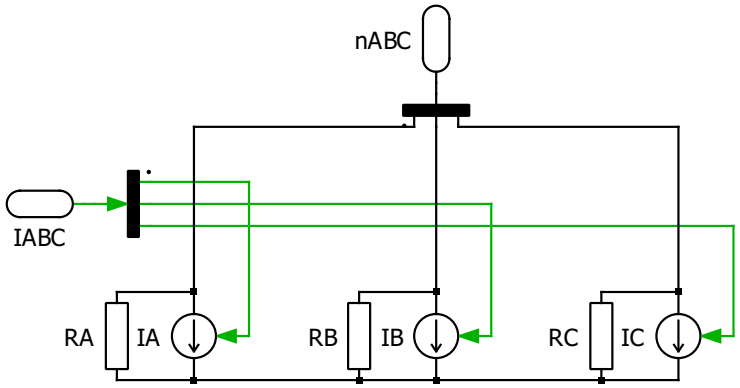

Figure A.16: SLC Circuit: Motor Load Current Generator (VCCS)

The average model direct matrix converter is utilized to greatly speed up simulations (10-20kHz switching events are removed). It is based off the description in Chapter 12.9 [15] and implemented as nine variable turns dc-transformers. The direct matrix converter schematic is shown in Figure A.17.

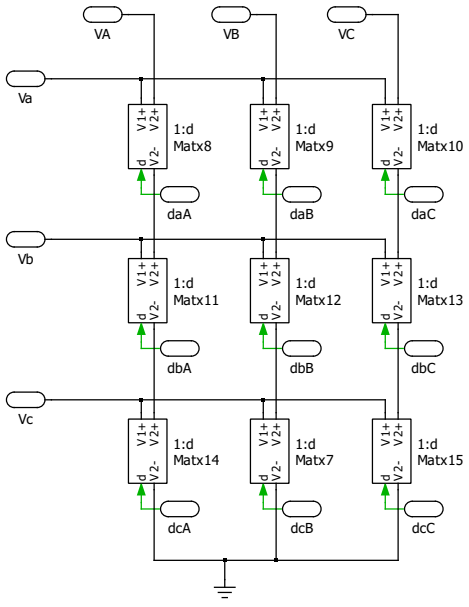

Figure A.17: SLC Circuit: Average Model Matrix Converter

Each of the boxes shown represents a variable turn transformer which is not a standard element in a electronics simulator. This was implemented with a set of current-controlled-current-sources and voltage-controlled-voltage-sources. This is shown in Figure A.18. Again, a transport delay of 1e-5 seconds is provided to break algebraic loops in Simulink.

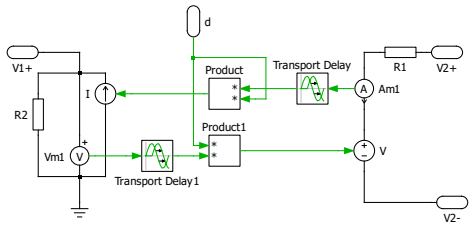

Figure A.18: SLC Circuit: Variable turn-ratio transformer implementation

This completes the review of all the major simulation blocks. There is a lot of information here, but a comprehensive overview would take far too much time. The information presented here should be sufficient to implement future matrix converter with ride-through support simulations.

Appendix B

Detailed Derivation of Power Control Loop

Where P_{sdq} is the grid delivered/consumed power defined by:

$$P_{sdq} = v_{sd}i_{sd} + v_{sq}i_{sq}$$

We will see that P_{sdq} is a squared function of i_{sq}, therefore we need to do linearization in order to solve for $\frac{\Delta P_{sdq}}{\Delta i_{sq,ref}}$.

In the Laplace domain, our standard equations for d-q field oriented control are as follows:

$$v_{sd} = R_s i_{sd} + s\lambda_{sd} - \omega_d \lambda_{sq}$$

$$v_{sq} = R_s i_{sq} + s\lambda_{sq} + \omega_d \lambda_{sd}$$

Now we replace the fluxes (λ's) with the following, assuming $\lambda rq = 0$ (rotor d-axes aligned flux).

$$\lambda_{sq} = \sigma L_s i_{sq}$$

$$\lambda_{sd} = \sigma L_s i_{sd} + \frac{L_m}{L_r}\lambda_{rd}$$

Which after some manipulation yields (using Mohan Adv. Electric Drives book, eqn. 5-10, 5-16, and 5-17):

$$\lambda_{sd} = \frac{(\sigma L_s + \frac{L_m}{L_r}L_m)(1 + \frac{\sigma L_s \tau_r}{\sigma L_s + \frac{L_m}{L_r}L_m}s)}{(1 + s\tau_r)} i_{sd}$$

Which will be shortened to:

$$\lambda_{sd} = A(s)i_{sd}$$

Substituting λ_{sd} and λ_{sq} into v_{sd} and v_{sq} yields:

$$v_{sd} = R_s i_{sd} + sA(s)i_{sd} - \omega_d \sigma L_s i_{sq}$$

$$v_{sq} = R_s i_{sq} + s\sigma L_s i_{sq} + \omega_d A(s) i_{sd}$$

Then:

$$P_{sdq} = v_{sd} i_{sd} + v_{sq} i_{sq}$$

$$P_{sdq} = (R_s i_{sd} + sA(s)i_{sd} - \omega_d \sigma L_s i_{sq}) i_{sd} + (R_s i_{sq} + s\sigma L_s i_{sq} + \omega_d A(s) i_{sd}) i_{sq}$$

Distribute and collect terms:

$$P_{sdq} = (R_s + sA(s))i_{sd}^2 - \omega_d \sigma L_s i_{sq} i_{sd} + (R_s + s\sigma L_s) i_{sq}^2 + \omega_d A(s) i_{sd} i_{sq}$$

Take the differential where $P_{sdq} = (P_{sdq} + \Delta P_{sdq})$ and $i_{sq} = (i_{sq} + \Delta i_{sq,ref})$:

$$\begin{aligned} P_{sdq} + \Delta P_{sdq} =& (R_s + sA(s))i_{sd}^2 \\ & - \omega_d \sigma L_s (i_{sq} + \Delta i_{sq,ref}) i_{sd} \\ & + (R_s + s\sigma L_s)(i_{sq} + \Delta i_{sq,ref})^2 \\ & + \omega_d A(s) i_{sd} (i_{sq} + \Delta i_{sq,ref}) \end{aligned} \tag{B.1}$$

Then multiply out $(i_{sq} + \Delta i_{sq,ref})^2$, assume Δ^2 term to be small, and subtract the original P_{sdq} from both sides yields:

$$\begin{aligned} \Delta P_{sdq} =& - \omega_d \sigma L_s (\Delta i_{sq,ref}) i_{sd} \\ & + (R_s + s\sigma L_s)(2 i_{sq} \Delta i_{sq,ref}) \\ & + \omega_d A(s) i_{sd} (\Delta i_{sq,ref}) \end{aligned} \tag{B.2}$$

Dividing by $\Delta i_{sq,ref}$ yields:

$$\frac{\Delta P_{sdq}}{\Delta i_{sq,ref}} = -\omega_d \sigma L_s i_{sd} + (R_s + s\sigma L_s) 2 i_{sq} + \omega_d A(s) i_{sd}$$

Substituting $A(s)$ back into the equation we get the full form:

$$\begin{aligned}\frac{\Delta P_{sdq}}{\Delta i_{sq}} = &- \omega_d \sigma L_s i_{sd} + (R_s + s\sigma L_s) 2 i_{sq} \\ &+ \omega_d \frac{(\sigma L_s + \frac{L_m}{L_r} L_m)(1 + \frac{\sigma L_s \tau_r}{\sigma L_s + \frac{L_m}{L_r} L_m} s)}{(1 + s\tau_r)} i_{sd}\end{aligned} \tag{B.3}$$

In short, $\frac{\Delta P_{sdq}}{\Delta i_{sq,ref}}$ is found by linearization to be exclusively a function of R's, L's, ω_d, i_{sd}, and i_{sq}. If we assume ω_d and i_{sd} is held constant, then a fairly simple plant results based only on fixed real component values.