A Low Power Biosensor for Medical Applications

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Thesis is dedicated to my parents,

Yung-Fa Hu and Su-Yun Wang

To my father,

This is for your 90th birthday gift.

Thank you for understanding and supporting me for so long.

To my mother,

Thank you for encouraging and supporting me for most of your life.

Abstract

This research presents on a CMOS sensor, which includes a chopper stabilized front-end amplifier with DC suppressed feedback and a 12-bit successive approximation register (SAR) analog-to-digital converter (ADC) with background calibration. It could reduce the flicker noise interference in the low frequency and suppressed the DC offset voltage between the two input signals. Therefore, this structure is suitable for bio-medical applications. The bio-medical signals are smaller than 5 mV in the low frequency between 0.01 Hz and 1 kHz. After amplifying, the signals will be digitized by a 12-bit SAR ADC.

The chopper stabilized amplifier has a clock rate, 16 kHz, controlling the chopper switches and shifting the original signals to 16 kHz in order to reducing the flicker noise. In our case, the flicker noise could lower at least 80 times at this clock rate. The two-Thomas Biquad low-pass filter, as the anti-aliasing filter, could suppress the harmonic signals at least 40dB before digitalized by ADC.

For the 12-bit SAR ADC, the differential nonlinearity (DNL) is +0.576/-0.96 least significant bit (LSB), and the integral nonlinearity (INL) is +0.534/-0.655 LSB. The signal-to-noise and distortion ratio (SNDR) can be estimated 69dB. The effective number of bits (ENOB) is 11.17. The total power dissipation of the ADC is 60-μW at 500-KS/s sampling rate and the supply voltages are ±0.5V. The figure of merit (FOM) is 52.08-fJ/conversion step.

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CHAPTER 1

INTRODUCTION

Motivation

Our body generates several bio-electrical signals which can be detected and visualized through electrocardiograms (EKG), electromyograms (EMG), and electroencephalograms (EEG). For some time now, physicians have depended on these bio-signals to diagnose different kinds of diseases and to monitor these signals in an effort to control the patients' health conditions and give them suitable treatment, including medication, physical therapy, and/or nourishment.

Portable health monitors or devices are becoming increasingly important and necessary in modern society where people are living longer through advancing technologies. Portable health monitors can not only improve the living quality of seniors and chronic patients, but can also build a better connection between patients and doctors. For example, a diabetic would not need to stay in a hospital or health center for a long period of time. They can still maintain their regular activities; working, studying, sporting, and in this way, reduce a huge health care budget without sacrificing health care quality.

Low-power circuit design is a critical factor for portable devices. With a proper design, a device can have a long operating period and/or perform more functions to obtain detailed data which could help doctors and nurses more accurately diagnose health parameters. Continual monitoring of patients with portable devices can be a significant improvement to patients with chronic ailments, but also to members of the healthcare

profession as a front-line defense system. Doctors could review the long-term recorded data when prescribing medications and their dosages.

This research project focuses on the low-power, battery-operated front-end analog circuit design for a bio-sensor, which could collect and digitalize the bio-electrical signals based on 0.18μm TSMC process. It can operate with as little as 1.0 volt power supply, which is suitable for portable medical devices.

Biosignal Introduction and Recording Technology [1]

Bioelectric potentials are generated by excitable cells which are components of many different tissues, like neurons, muscles, or organs. There are two electrical potentials which displayed on these cells. One is a resting potential, the other is an action potential. Without stimulator, the cell stays in a resting potential (dc offset potential) in the range -50 mV to -100 mV. There is the membrane threshold potential (usually about 20 mV more than the resting potential) of a cell. When the stimulus exceeds this potential, an unattenuated action potential travels with a constant velocity along the membrane of the excitable cell.

The electrocardiogram (ECG) recordes the electrical activity during the four chambers of the heart contract or rest in the circulatory system. As shown in Figure 1.1 [2], the sinoatrial (SA) node is a pacemaker of the heart generating the initial cardiac impulse, conducting to the atrial muscle and spreading to the atrioventricluar (AV) node. Then the impulse goes through bundle branches and purkinje fibers the heart returning to the initial state (resting state), eventually. During the cardiac electrical activity, ECG waves can be measured using body-surface electrodes by 12 standard leads from different angles. These signals have amplitude between 10 μV and 5 mV, and a bandwidth from 0.05 to 100 Hz.

Each lead has P, Q, S, R, T and U waves as illustrated in Figure 1.2 and Table 1.1 presents the normal duration intervals. The P wave is produced by left atrial excitation; the QRS complex by atrial systole, diastole and ventricular excitation; the T wave is caused by ventricular systole; the U wave is generated by ventricular diastole. According to the wave duration, magnitude, and relationships, physicians can diagnostic or monitor patients' condition.

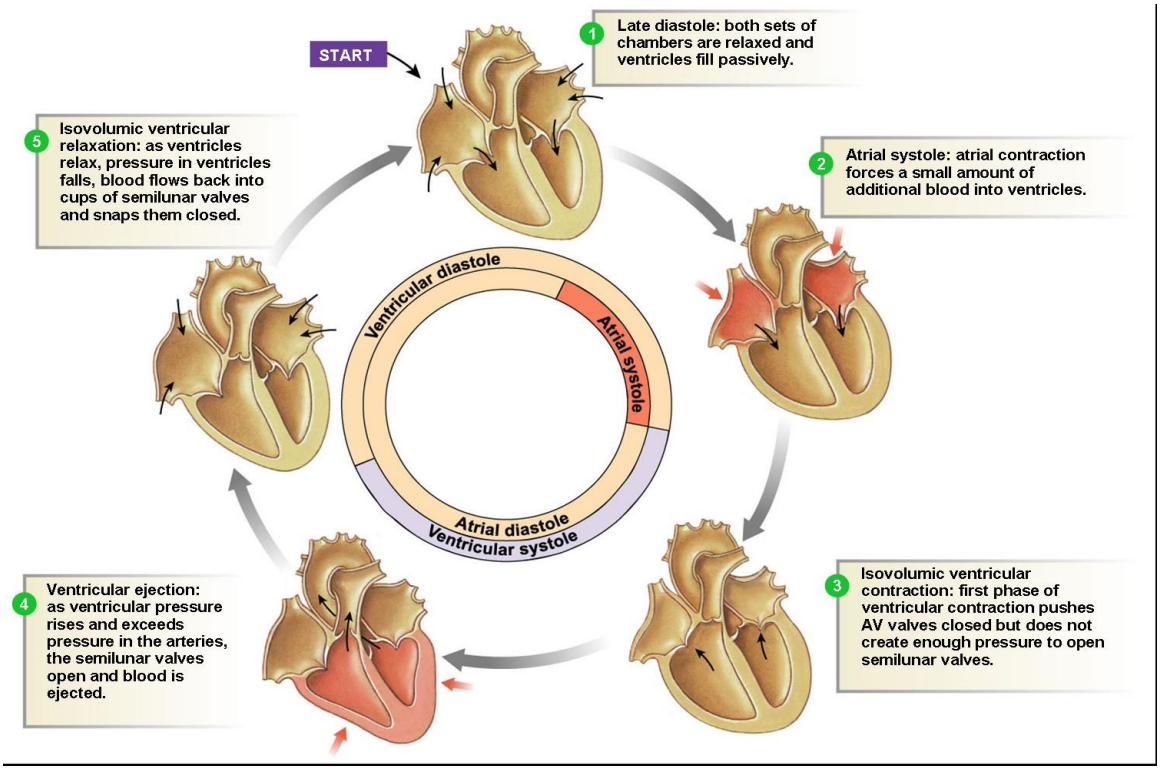


Figure 1.1 The electrical activity of the heart **[2]**.

Table 1.1 ECG intervals **[3]**.

	Normal duration (sec)	
	Average	Range
PR interval	0.18	0.12-0.20
QRS duration	0.08	0.07-0.10
QT interval	0.40	0.33-0.43
ST interval (QT minus QRS)	0.32	

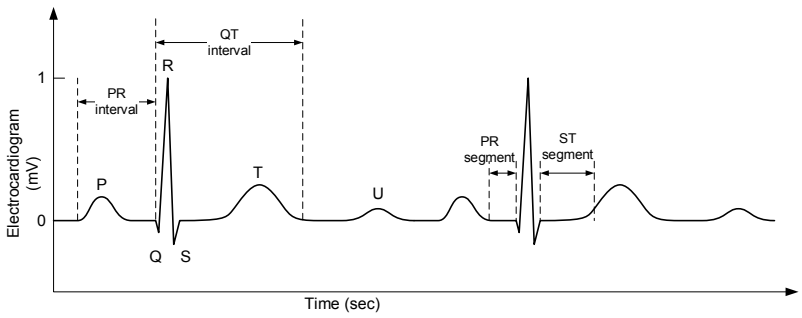


Figure 1.2 ECG waves.

The electromyogram (EMG) recordes the electrical activity on superficial muscles by using the surface electrodes. The amplitude is in the range 20 to 2000 μV at the variable frequency from 6 to 30 Hz. The electroencephalogram (EEG) records the potential fluctuations from the brain. There are several different ways to measure the brain activity. An electrocorticogram (ECoG) is the external way using electrodes placing on different exposed positions of the surface of the brain, as shown in Figure 1.3. The frequencies of these brain waves range from 0.5 to 100Hz and the magnitudes of the potential voltage are between 20 to 200 μV. Table 1.2 is a summary of the common bio-signals.

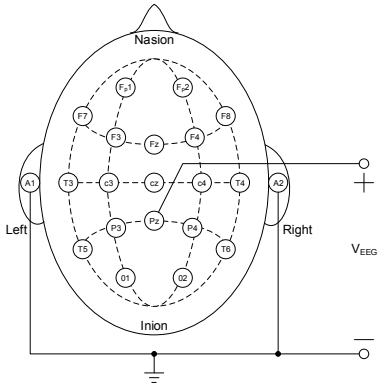


Figure 1.3 The International Federation 10-20 electrode system.

Table 1.2 Common bio-signals.

Biosignals	Bandwidth	Magnitude
ECG	0.05 ~ 100 Hz	10 ~ 5000 μV
EMG	10 ~ 1K Hz	20 ~ 2000 μV
EEG	0.5 ~ 100Hz	1 ~ 500 μV

Figure 1.4 is a conventional bio-potential recording system. Two skin electrodes are glued on the human body to get the signal into an instrumentation amplifier (IA) increasing amplitude, passing through a bandpass filter (BPF) to get rid of the noise, then digitalizing it by an analog-to-digital converter (ADC), finally a digital signal processor (DSP) analyzing the data.

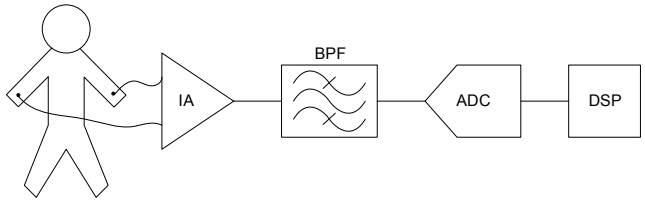


Figure 1.4 A conventional bio-potential recoding system.

Several important issues for designing a conventional bio-potential recoding system should be considered. First, the bio-signals are the low frequencies and narrow bandwidths. There is a difficulty to design a simple and suitable BPF. Second, there is the differential electrode offset (DEO), which comes from the two skin electrodes. Traditional, the IA is a combination of several amplifiers to compensate this offset. Third, the flicker noise and common-mode noise are generated from the IA. It is inversely proportional to the frequency. When CMOS integrated circuits operate at low frequency, it becomes an important part of noise source. The common-mode noise depends on the architecture of the amplifier.

Goals and Dissertation Organization

The goal of this research is to implement a suitable and simple architecture of the bio-signal recording system without external components for 1.0 volt battery-operating.

Chapter 2 presents the behavior simulation of the bio-signal recording system using MATLAB®. Chapter 3 describes the chopper stabilized front-end amplifier instead of the traditional instrument amplifier, a MOSFET lowpass filter for the low frequency and narrow bandwidth without external capacitances, and finally an anti-aliasing lowpass filter. And Chapter 4 demonstrates a low saving power 12-bit ADC design. The chip layout, PCB layout and testing issues are discussed in Chapter5.

CHAPTER 2

The System Level Simulation

Introduction

The system level simulation has been used to estimate the performances of the design methodologies under fundamental specifications. When designers provide more detail factors, the more accurately evaluation we could get. It saves a lot of iteration time optimizing the design or choosing a suitable methodology to the system. MATLAB® is a very adequate simulation tool for the system level simulation.

In this chapter, flicker noise, low input frequencies and narrow bandwidths, will be parameterized and become factors in the system level simulation. First, the flicker noise could be considered very carefully in order to choosing a suitable architecture for the front-end amplifier; the order of a BPF depends on the input frequency and the bandwidth requirements. And then the behavior models are presented. Finally, the simulation results are shown.

Noise Analysis [4] [5] [6]

In order to finding the lower limitation of the electrical signal and optimal the size of the circuit, it is necessary to analysis the noise inside the circuits. The noise comes from the electrical phenomena in the CMOS integrated circuits which this research is complimented by. They are caused by small current or voltage fluctuations, temperature drift, or operating frequencies, etc. It is different types of noise which come from different sources. In this research, the thermal noise and flicker noise (1/f noise) are the most

important issues. Therefore, the following paragraphs will present the fundamental concepts of these two types of noise.

Thermal noise is due to the random thermal motion of the electrons in devices. This noise is directly proportional to the temperature (T: absolute temperature) and can be represented by a series voltage generator $\overline{v^2}$ or by a shunt current generator $\overline{i^2}$ in a resistor R, as shown in Table 2.1 (a.2) and (a.3). The equivalent equations are

$$\overline{v^2} = 4kTR\Delta f \tag{2.1}$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \tag{2.2}$$

where k is Boltzmann's constant (1.38×10^{-23} V-C/K). At room temperature $4kT = 1.66 \times 10^{-20}$V-C.

Flicker noise is also named 1/f noise, because the power spectral density is inversely proportional to the frequency. It is due to the fluctuations in the MOSFET surface by trapping and releasing the carriers and generated the noise concentrated at low frequencies. The flicker noise is always associated with the direct current. It is the difference between the thermal noise and the flicker noise. The equivalent function is

$$\overline{i^2} = K_1\frac{I^a}{f^b}\Delta f \tag{2.3}$$

where

Δf = a small bandwidth (typically 1 Hz) at frequency f
I = direct current
K_1 = constant for a particular device
a = constant in the range 0.5 to 2
b = constant of about unity

Burst noise is another type of low-frequency noise. Its equivalent function is

$$\overline{i^2} = K_2\frac{I^c}{1+(\frac{f}{f_c})^2}\Delta f \tag{2.4}$$

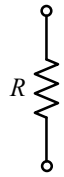
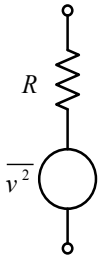
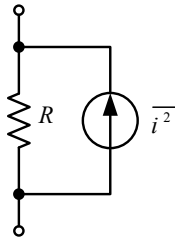
where

I = direct current
K_2 = constant for a particular device
c = constant in the range 0.5 to 2
f_c = particular frequency for a given noise process

The noise spectral density drops very fast as $1/f^2$. Therefore, in this research the flicker noise is the mainly issue in the low-frequency. Table 2.1 is a summary of the small-signal equivalent circuits with noise sources and the correspondent noise equations for the resistor, diode, and MOSFET.

The MOSFET small-signal equivalent circuit as shown in Table 2.1(c.2) and the noise equations (2.9) and (2.10), the noise currents are in two different terminals, drain and gate. The drain noise current is caused by the thermal noise and flicker noise. In the thermal noise term, it is proportional to T and the small-signal transconductor (g_m), which is defined as (2.11) and (2.14). It is proportional to the drain DC current (I_D) or the width to length ratio (W/L) of MOSFET. The second term, flicker noise, is also proportional to I_D, but inverse proportional to the frequency and the square of the length of MOSFET. It implies increasing the length of MOSFET can reduce the noise current in the drain terminal.

Table 2.1 The small signal equivalent circuits with noise sources and the noise equations.

			$\overline{v^2} = 4kTR\Delta f$ (2.5) $\overline{i^2} = 4kT\frac{1}{R}\Delta f$ (2.6)
(a.1)	(a.2)	(a.3)	

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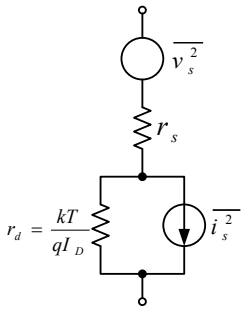
(b.1)</td>
<td> 
(b.2)</td>
<td>$\overline{v_s^2} = 4kTr_s\Delta f$ (2.7)
$\overline{i^2} = 2qI_D\Delta f + K\frac{I_D^a}{f}\Delta f$ (2.8)</td>
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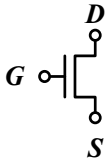
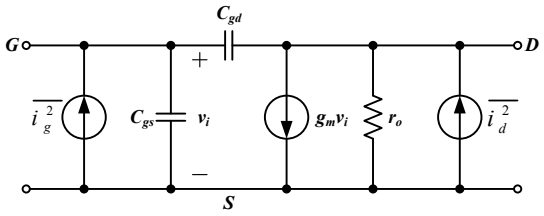
<td rowspan="5"> 
(c.1)</td>
<td rowspan="5"> 
(c.2)</td>
<td>$\overline{i_d^2} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + K_F\frac{I_D}{fC_{ox}L^2}\Delta f$ (2.9)</td>
</tr>
<tr>
<td>$4kT(\frac{2}{3}g_m)\Delta f$:Thermal noise
$K_F\frac{I_D}{fC_{ox}L^2}\Delta f$:Flicker noise</td>
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<tr>
<td>K_F :flicker noise coefficient</td>
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<tr>
<td>$\overline{i_g^2} = 2qI_G\Delta f + \frac{16}{15}kT\omega^2C_{gs}^2\Delta f$ (2.10)</td>
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<tr>
<td>I_G :gate leakage current
$C_{gs} = \frac{2}{3}C_{ox}WL$</td>
</tr>
</table>

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \tag{2.11}$$

$$i_D = \frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right)(v_{GS} - V_{TH})^2, \;\; 0 \le v_{DS} \le (v_{GS} - V_{TH}) \tag{2.12}$$

$$K = \mu_0 C_{ox};\; \beta = K\frac{W}{L} = \mu_0 C_{ox}\frac{W}{L} \;\; (A/V^2) \tag{2.13}$$

$$g_m = \beta(v_{GS} - V_{TH}) = \sqrt{2\beta I_D} = \frac{2I_D}{(v_{GS} - V_{TH})} \tag{2.14}$$

The gate noise current (2.10) is caused by the gate leakage current and the thermal noise. The leakage current is very small compared with the drain current. The second term is the thermal noise and usually considered as a high frequency noise. Therefore, the gate noise current can be ignored in this research since the bio-signals are in the low frequency.

In HSPICE BSIM3 model [7], the MOSFET noise power spectra density is presented in (2.15). The thermal noise and the flicker noise asymptote meet at a frequency f_c, which is called the flicker noise corner frequency.

$$i_{nd}^2 = (channel\ thermal\ noise)^2 + (flicker\ noise)^2 \tag{2.15}$$

$$(channel\ thermal\ noise)^2 = \frac{8kT \cdot g_m}{3} \tag{2.16}$$

$$(flicker\ noise)^2 = \frac{K_F \cdot g_m^2}{C_{ox} W_{eff} L_{eff} f^{AF}} \tag{2.17}$$

Where

AF: flicker noise exponent.

K_F: flicker noise coefficient in the range 10^{-19} to $10^{-25}\ V^2 \cdot F$

NLEV: noise equation selector.

In order to having reasonable noise parameters for system level simulation, a simple fully differential amplifier is simulated by HSPICE with AF=1, NLEV=2, and K_F=3×10^{-24} ,10^{-24}, 5×10^{-25} and 10^{-25}. Figure 2.1 presents the simulation results with these 4 cases. The corner frequency drifts from 10 KHz to 3.17 MHz. However, the bio-signals' bandwidth is below 100Hz. Assuming the minimum input signal is 10μV at 0.05 Hz, in the worst case the input noise is $0.5\mu V^2/Hz$. It is impossible to sense the bio-signal directly. Therefore, the chopper stabilization technique is used to shift the input signals to higher frequency bandwidth by a proper clock rate, which above the corner frequency, f_c. In this way, the minimum input noise will depend on the thermal noise (2.16), which is proportional to the transconductor (g_m) of the amplifier. The chopper amplifier will be discussed more detail in the next chapter.

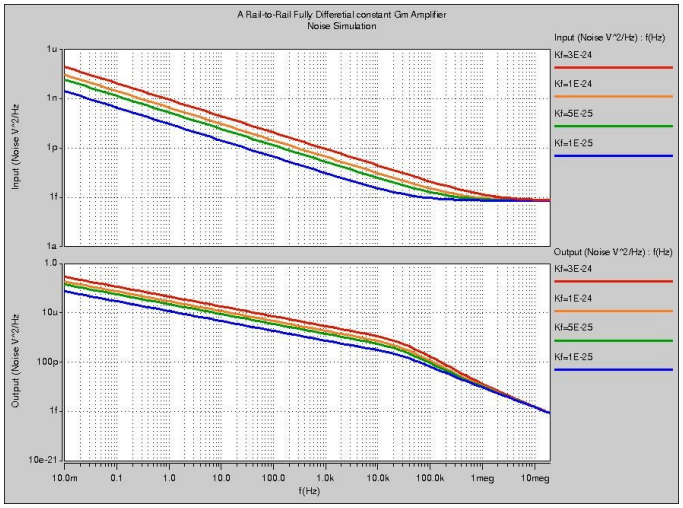

Figure 2.1 The spectral density of the drain-current noise generator in a fully differential amplifier

The Behavior of Models and Simulation Result

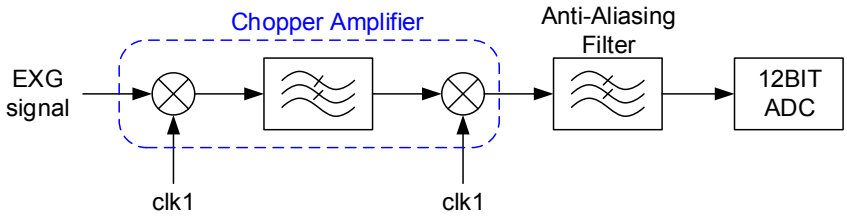

Figure 2.2 Block diagram for the system level simulation.

The behavior of model for each circuit block and the connections are represented in Figure 2.2. The chopper amplifier, which has flicker noise and thermal noise, includes a low gain amplifier and two modulators; the first one shifts the bio-signal to the higher frequency; the other shifts the amplified signal to the original frequency and generates harmonic signals based on the clock frequency (clk1). The following block is an anti-aliasing filter (AAF) to eliminate the harmonic signals. The analog-to-digital converter samples and digitalizes the signal.

The main issues for the system level simulation are to select the suitable clock frequency for the chopper amplifier and the lowest order of the AAF. The clock frequency

should between the corner frequency and the -3dB frequency of the low gain amplifier. The order of the AAF also depends on the clock frequency. Since the ADC has 12 bits and 1volt, the gain of the chopper amplifier can be estimated as follow:

$$SNR_{ADC} = 6.02N + 1.76 = 6.02 \times 12 + 1.76 = 74\ (dB) \tag{2.18}$$

$$LSB = \frac{1\ volt}{2^{12}} = 244.14 \approx 250\ (\mu V); \tag{2.19}$$

$$signal_{min} = 1\ (\mu V) \Longrightarrow Gain \approx 48dB \tag{2.20}$$

After several iterations, the following simulation results, as demonstrated in Figure 2.3 and Figure 2.4, show the clock rate is 16 kHz and the order is 1for AFF, and then the reasonable SNR is for the 12 bit ADC.

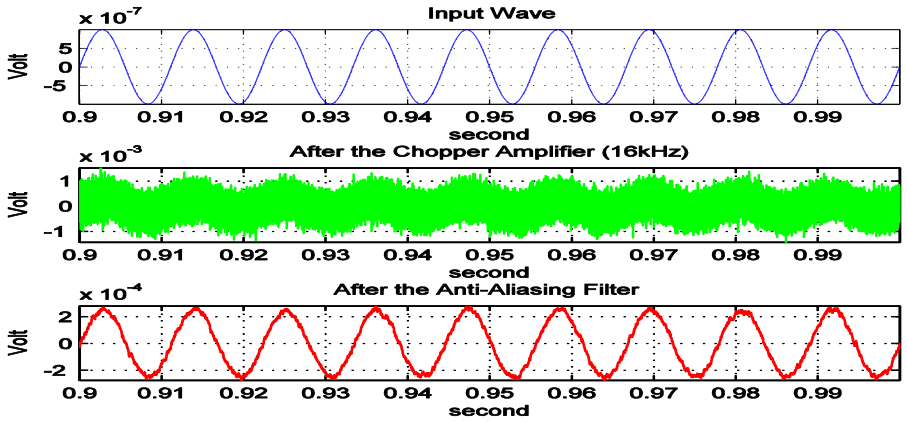

Figure 2.3 The transient simulation results.

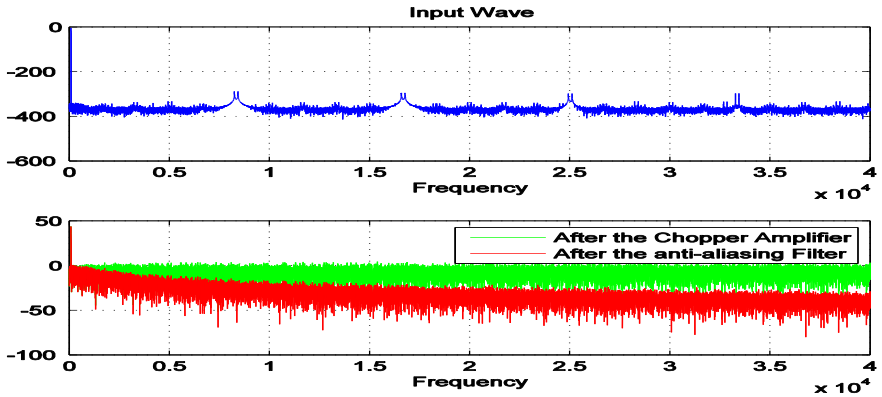

Figure 2.4 The frequency domain simulation results.

CHPATER 3

The Chopper Amplifier

Introduction

There are two critical issues for sensing small amplitudes of bio-signals in a low frequency. One is the differential electrical offset (DEO) voltage, which cause a DC offset voltage. The other is the flicker noise in low frequency, which is larger than the input signal. In the chapter, the DEO voltage in bio-signals is introduced, first. A chopper amplifier, switched-cap lowpass filter, and an anti-aliasing lowpass filter are represented, and the simulation results are shown.

The Differential Electrical Offset (DEO) voltage

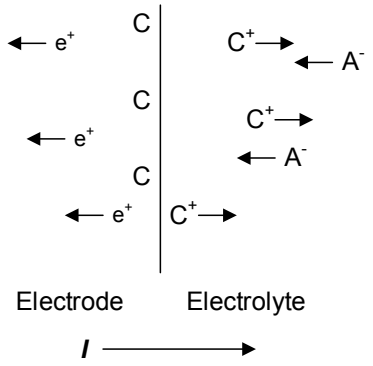

Figure 3.1 Electrode-electrolyte interface.

The passage of electric current from the body to an electrode can be presented by examining the electrode-electrolyte interface [1], as shown in Figure 3.1. The electrolyte represents the body fluid containing ions. A current crosses the interface from the electrode to the electrolyte.

A half-cell is a structure that contains a conductive electrode and a surrounding conductive electrolyte separated by a naturally occurring Stern layer. Chemical reactions with this layer momentarily pump electric charges between the electrode and the electrolyte, resulting in a potential difference known as the ***half-cell potential***, as illustrated in Table 3.1. Here is an example as shown below:

The standard hydrogen half-cell:

Original equation

$$Zn + Cu^{2+} \longrightarrow Zn^{2+} + Cu \tag{3.1}$$

Half-cell (anode) of Zn

$$Zn \rightarrow Zn^{2+} + 2e^{-} \tag{3.2}$$

Half-cell (cathode) of Cu

$$Cu^{2+} + 2e^{-} \rightarrow Cu \tag{3.3}$$

Table 3.1 Half-cell Potentials for Electrode Materials at 25ºC **[1]**

Metal and Reaction	**Potential Eº (V)**
$Ag + Cl^{-} \longrightarrow AgCl + e^{-}$	+0.223
$Ag \rightarrow Ag^{+} + e^{-}$	+0.799
$H_2 \longrightarrow 2H^{+} + 2e^{-}$	0.0 by definition

In electrochemistry, the ***Nernst equation***, as shown in, is an equation that relates the equilibrium reduction potential of a half-cell in an electrochemical cell to the standard electrode potential, temperature, activity, and reaction quotient of the underlying reactions and species used.

$$E = E^0 + \frac{RT}{nF}\ln\frac{a_1}{a_2} \tag{3.4}$$

where

E = half-cell potential

E^0 = standard half-cell potential

n = the number of moles of electrons transferred in the half-reaction

F = the Faraday constant; $F = 9.64853399 \times 10^4\ C/mol$

R = the universal gap constant; $R = 8.314472\ J/(k \cdot mol)$

T = the absolute temperature

a_1 = the chemical activity of the ions outside the cell

a_2 = the chemical activity of the ions inside the cell

At room temperature (25°C) $RT/F \approx 25.693mV$ for cells

The silver/silver chloride (Ag/AgCl) electrode is a practical electrode that approaches the characteristics of a ***perfectly nonpolarizable electrode***, in which current passes freely across the electrode-electrolyte interface, requiring no energy to make the transition.

The behavior of the Ag/AgCl electrode is governed by two chemical reactions. The first involvers the oxidation of silver atoms on the electrode surface to silver ions in solution at the interface. The second reaction occurs immediately after the formation of A_g^+ ions. These ions combine with Cl^- ions already in solution to form the ionic compound AgCl.

$$A_g \leftrightarrows A_g^+ + e^- \tag{3.5}$$

$$A_g^+ + Cl^- \leftrightarrows A_g Cl \downarrow \tag{3.6}$$

The silver chloride's rate of precipitation and of returning to solution is a constant K_s known as the ***solubility product***. For AgCl, the solubility product is $K_s = 1.56 \times 10^{-10}$. The first and second terms on the right-hand side are constants; only the third is determined by the activity of the Cl^- ion, which is caused by the current through the electrode.

$$a_{Ag^+} \times a_{Cl^-} = K_s \tag{3.7}$$

$$E = E^0_{A_g} + \frac{RT}{nF} \ln K_s - \frac{RT}{nF} \ln a_{Cl^-} \tag{3.8}$$

Although theoretically every Ag/AgCl electrode should have the same half-cell potential, there are usually differences from one to another. These differences as known the ***differential electrical offset*** (DEO) [8] [9] [10] should be quite small, of the order of millivolts. However, occasions can arise in which the differences can be as high as tens – or in extreme cases, even hundreds – of millivolts.

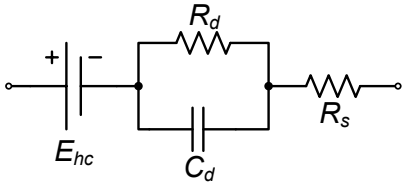

Figure 3.2 Equivalent circuit for a biopotential electrode.

The equivalent circuit for a biopotential electrode is shown in Figure 3.2. E_{hc} is the half-cell potential. C_d represents the capacitance across the double layer of charge at the electrode-electrolyte interface. R_d represents the leakage resistance across this double layers. R_s is the resistance of the electrolyte. At the low frequencies, where $1/\omega C \gg R_d$, the impedance is $R_d + R_s$. At the high frequencies, where $1/\omega C \ll R_d$, the impedance is R_s. (Typical values are R_s = 2kΩ, R_d = 10kΩ and C_d = 10μF).

Figure 3.3 (a) is a simple illustration to show the Ag/AgCl electrode connecting with the skin. The epidermis is the outermost layer and dermis and subcutaneous layer contain the vascular and nervous components. The electrical equivalent circuit is shown in Figure 3.3 (b). There is a potential difference E_{se} between gel and epidermis, which is given by

the Nernst equation. In Figure 3.3 (c) the typical values are presented. Usually, the skin potential, E_{se}, changes by 5 to 10 mV as motion artifact.

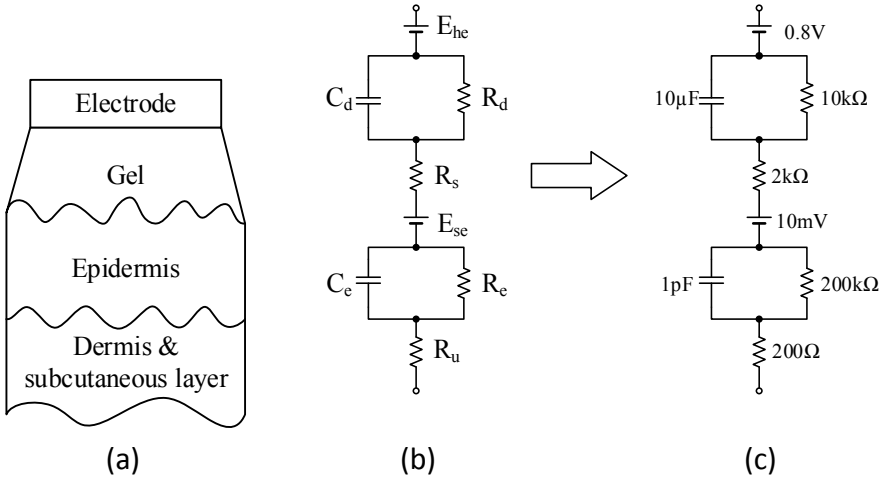

Figure 3.3 (a) A body-surface electrode placed against skin, (b) The electrical equivalent circuit, (c) The typical values for the modeling circuit

According to previous paragraphs, the E_{he} and E_{se} drift very slowly by time and there is a standard to rule this drift voltage. Therefore, the DC-offset exists when we use two Ag/AgCl electrodes to measure the biopontential from human bodies. Figure 3.4 demonstrates an equivalent circuit for the interface of two Ag/AgCl electrodes and the bio-medical amplifier. The input common mode voltage, $V_{in,cm}$, is shown in (3.9). The input differential mode voltage, $V_{in,diff}$, is shown is (3.10) assuming the primary differential voltage between E_{he1} and E_{he2}.

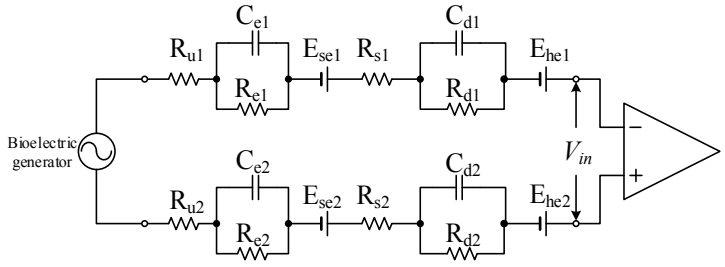

Figure 3.4 The equivalent circuit for tissue and electrode system.

$$V_{in,cm} = E_{he} + E_{se} \tag{3.9}$$

$$V_{in,diff} = V_{ac,bio-gen} + \Delta E_{he} \tag{3.10}$$

American National Standard/Association for the Advancement of Medical Instrumentation (ANSI/AAMI) [11] defines the standards for "***EGC Disposable Electrodes***". Some of the key points are shown below:

Gel-to-gel measurements: a pair of electrodes connected gel-to-gel shall, after a 1 minute stabilization period

1. The average value of 10 Hz ac impedance shall not exceed 2 kΩ.
2. The maximum dc-offset is 100 mV after 1 minute stabilization period.
3. The offset voltage shall be smaller than 150 μV_{p-p} in the pass band of 0.15 to 100 Hz.
4. The observed dc voltage offset change across a pair of electrodes connected gel-to-gel shall not exceed 100 mV. In no case shall this period be less than 8 hours.

Measurements on human skin [12]:

1. The short-term impedance generally decreases over time (4 hours) and ranged 10 to 100 kΩ for different makes. The impedance can decrease up to 50% in one hour.
2. The offset ranges from 2 to over 100 mV for different makes.
3. The "dynamic offset" is also measured. It ranged from 1 mV for the best electrode after one day of application, to over 125 mV (the limit of the recording equipment) for the worst.

A Chopper-Stabilized Amplifier with DC offset suppressed feedback

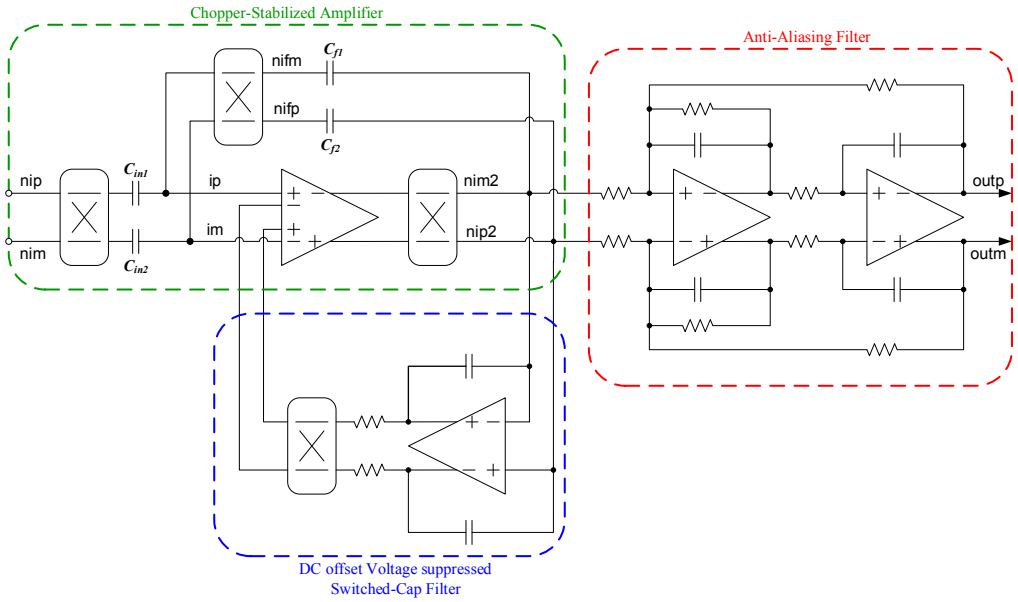

Figure 3.5 The simplified front-end amplifier structure.

Figure 3.5 illustrates the simplified structure of the front-end amplifier [13] [14] [15] which includes a chopper-stabilized amplifier, a DC offset suppressed feedback, and an anti-aliasing filter. The chopper-stabilized amplifier is based on a fully differential difference amplifier (DDA), as shown in Figure 3.6, with a mid-band gain, C_{in}/C_f, by using switches chopper the input signal to the higher frequency and after the amplifier, shifting the output signal to the original frequency.

The DDA [16] [17] has four inputs,which are V_{pp}, V_{pn}, V_{np}, and V_{nn}, and suppresses the input DC offset voltage caused by "V_{pp}-V_{np}", which can be expressed as (3.11). V_{pn} and V_{np} are the detected DC offset voltages from the feedback switched-cap lowpass filter. V_{pp} and Vnn are the input choppered signals; subtract the DC offset; and then compare them to generate the outputs, V_{op} and V_{on}, with a gain, A_0.

$$V_o = V_{op} - V_{on} = A_0[(V_{pp} - V_{pn}) - (V_{np} - V_{nn})] \tag{3.11}$$

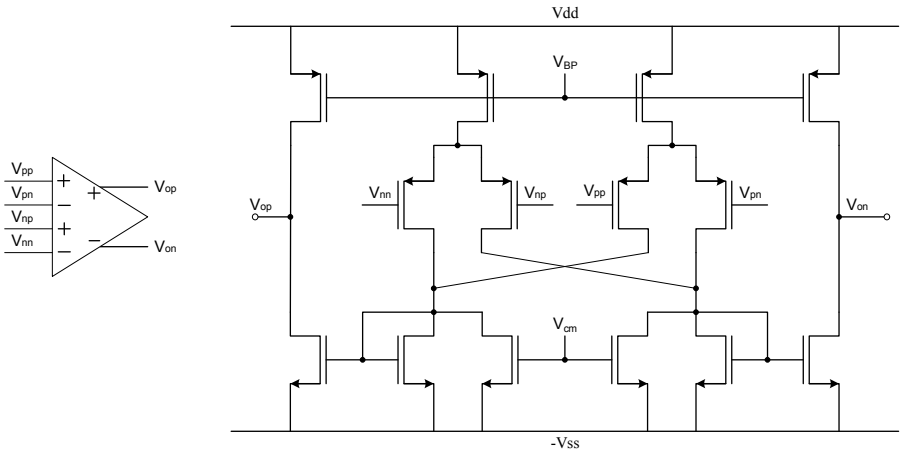

Figure 3.6 The fully difference differential amplifier.

In the chopper stabilized amplifier, there are two non-overlapping clocks, which control the switches, and the clock rate is 16 kHz. When “ph2n” is active, the signals pass directly. “no1” equals to “ni1” and “no2” equals to “ni2”. When “ph1n” is active, the signals swap. Figure 3.7 shows the relationship of the switches and the clocks. The input-referred noise simulation results [18] are illustrated in Figure 3.8, Figure 3.9, and Table 3.2. At 1Hz, The input-referred noise is decreased 80 times with chopper switches when the clock rate is 16 kHz.

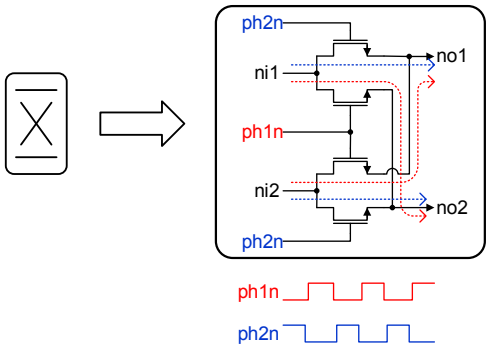

Figure 3.7 The chopper switches.

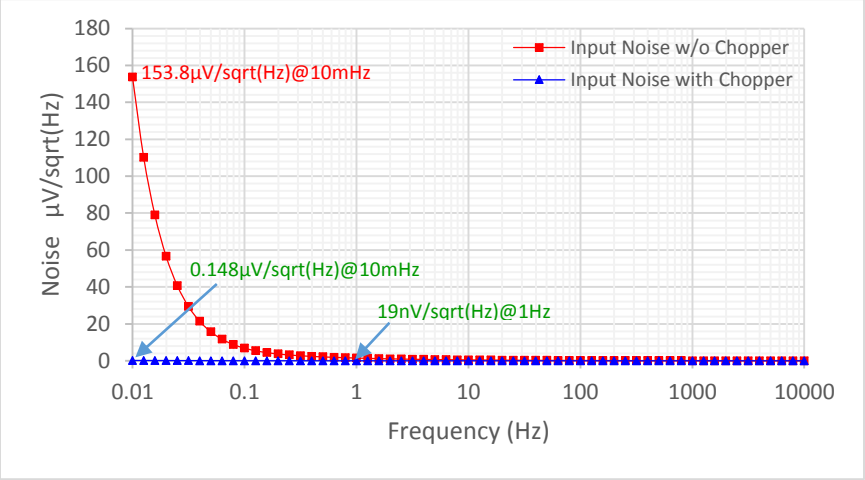

Figure 3.8 The input-referred noise with and without the chopper switches.

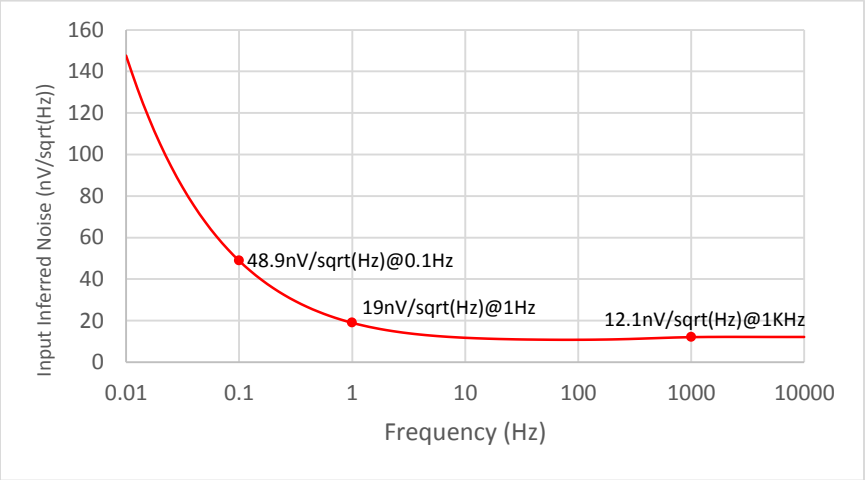

Figure 3.9 The input-referred noise which chopper switches at 16 kHz clock rate.

Table 3.2 The summary of the input-referred noise.

Frequency (Hz)	Input-referred noise without chopper	Input-referred noise with chopper
0.01	153.80 $\mu V/\sqrt{Hz}$	148.0 $nV/\sqrt{Hz}$
0.1	6.89 $\mu V/\sqrt{Hz}$	48.9 $nV/\sqrt{Hz}$
1	1.54 $\mu V/\sqrt{Hz}$	19.0 $nV/\sqrt{Hz}$

The DC offset value is extracted by a MOSFET-capacitor LPF with a dominate pole about 0.01Hz, as shown in Figure 3.10. In order to create a very low frequency pole, we need a large time constant, τ. The transform function of the LPF is

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\frac{1}{sR_1C_1} \tag{3.12}$$

$$\omega = \frac{1}{\tau} = \frac{1}{R_1C_1} = 2\pi f_o \tag{3.13}$$

$$R_1 = \frac{1}{2\pi f_0 C_1} = \frac{1}{2\pi \times (0.1Hz) \times (2pF)} \tag{3.14}$$

Equation (3.14) shows the input resistor is too large to implement inside a chip. Using MOSFET resistor is suitable way. The frequency and transient simulation results are shown in Figure 3.11 and Figure 3.12. The dominate pole is about 0.1Hz and the low frequency signal could be extracted successfully. For the transient simulation, there are two different input signals. One is 10 kHz with ±10 mV amplitude; the other is 0.01 Hz with ±200 mV amplitude.

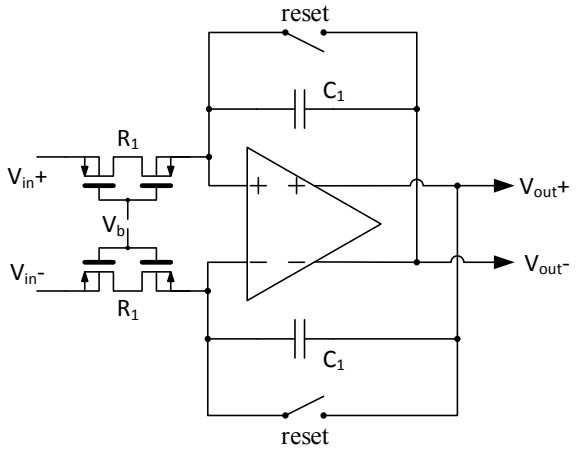

Figure 3.10 The MOSF-capacitor LPF.

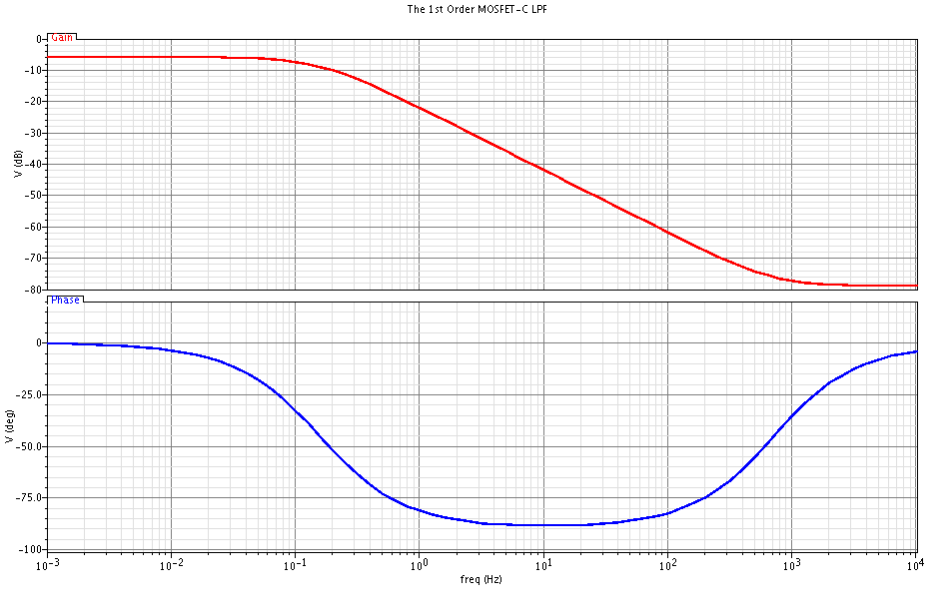

Figure 3.11 The frequency response of the feedback MOSFET-C LPF.

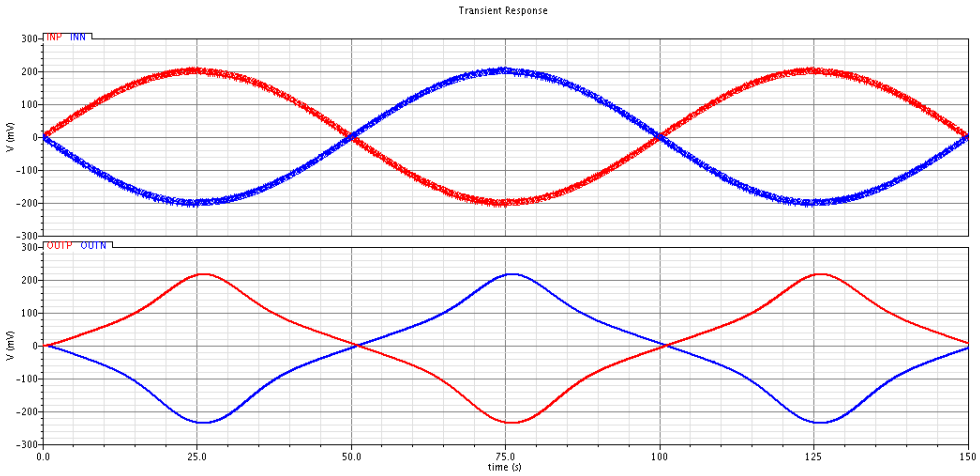

Figure 3.12 The transient simulation result.

Figure 3.13 is the 2nd order Tow-Thomas Biquad low-pass filter [6] which is used as an anti-aliasing filter and replacing the resistors to the MOSFET resistors, as shown Figure 3.14. The price by using MOSFET type resistors is that it needs an extra bias voltage, V_b, to control the resistors' values. The advantage of this structure is the less sensitive to finite opamp gain effects.

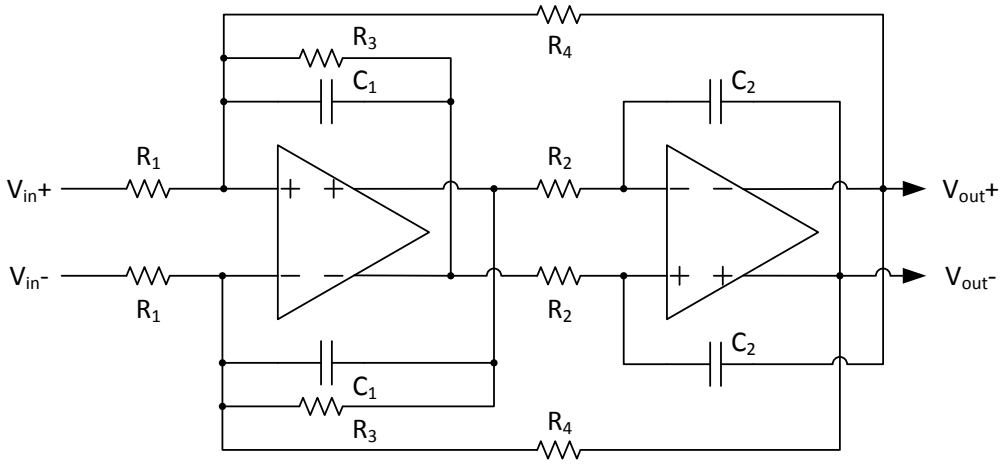

Figure 3.13 The 2nd order lowpass filter.

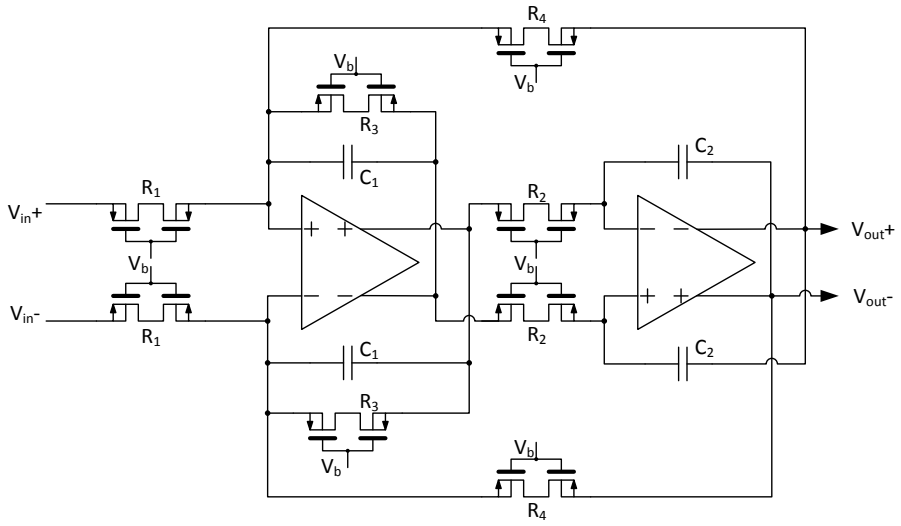

Figure 3.14 The Two-Thomas Biquad (MOSFET-C) lowpass filter.

In order to filter the noise and folded signals in harmonic frequencies because of the chopper clock, we assume the signal should be attenuated about 40dB at 16 kHz and the -3dB bandwidth frequency, ω_o, is lower than 1 kHz; and then calculate the suitable values for each component by using the transfer function of the 2nd order Tow-Thomas Biquad low-pass filter as shown below:

$$H(s) = \frac{1}{R_1 R_2 C_1 C_2} \times \frac{1}{s^2 + \frac{1}{R_3 C_1} s + \frac{1}{R_2 R_4 C_1 C_2}} \tag{3.11}$$

$$H(s) = k_0 \times \frac{1}{s^2 + \left(\frac{\omega_o}{Q}\right) s + \omega_o^2} \tag{3.12}$$

$$\omega_o = \frac{1}{\sqrt{R_2 R_4 C_1 C_2}} = \frac{1}{R_2 C_1} \quad ; R_2 = R_4;\ C_1 = C_2 \tag{3.13}$$

$$\frac{\omega_o}{Q} = \frac{1}{R_3 C_1} \Rightarrow Q = \frac{R_3}{R_2} = \frac{1}{\sqrt{2}} \Rightarrow R_3 = \frac{R_2}{\sqrt{2}} \tag{3.14}$$

After several times iterations, the reasonable values for the components are presented in Table 3.3 and the frequency simulation result is illustrated in Figure 3.15.

Table 3.3 The component values.

$R_1 = 4\ M\Omega$	$W/L = 275nm/880nn$
$R_2 = R_4 = 50.0\ M\Omega$	$W/L = 4.295\mu m/220nm$
$R_3 = 35.33\ M\Omega$	$W/L = 2.73\mu m/220nm$
$C_1 = C_2 = 2\ pF$	Area: $121\mu m \times 29.6\mu m$
Vb=140mV – Vss	

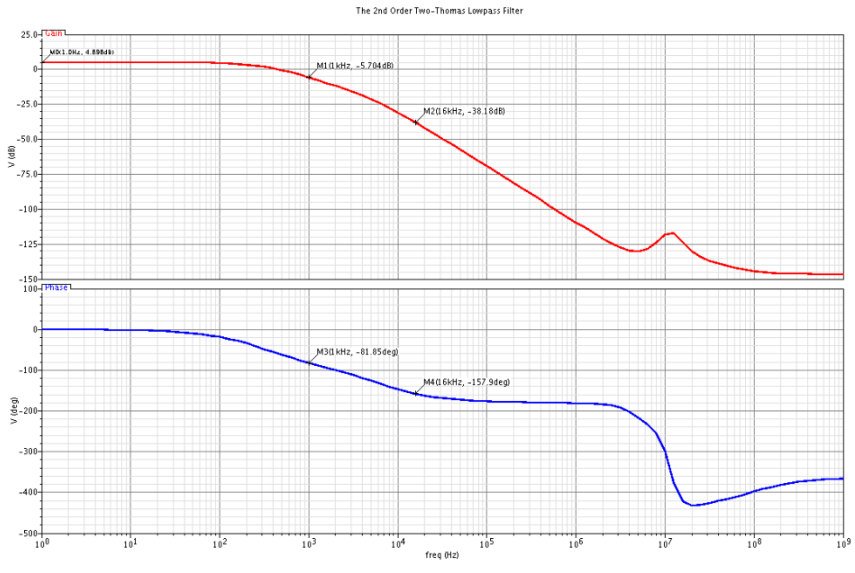

Figure 3.15 The frequency response of the anti-aliasing filter.

Simulation Results

In this section, the different transient simulation results are presented. Figure 3.16 shows the input signals have the ±2 mV amplitude with DEO voltage, 2 mV, in the first row. The second row shows the outputs of the amplifier. The third one illustrates the outputs of the anti-aliasing filter. The last one is the feedback signals. Figure 3.17 illustrates the input signals have the same amplitude with DEO voltage, 10 mV. The outputs of the anti-aliasing filter could recover the DEO effect. Figure 3.18 shows the input signals with the chopper clock frequency, 16 kHz. The outputs of the anti-aliasing filter can extracted the low frequency amplified signals.

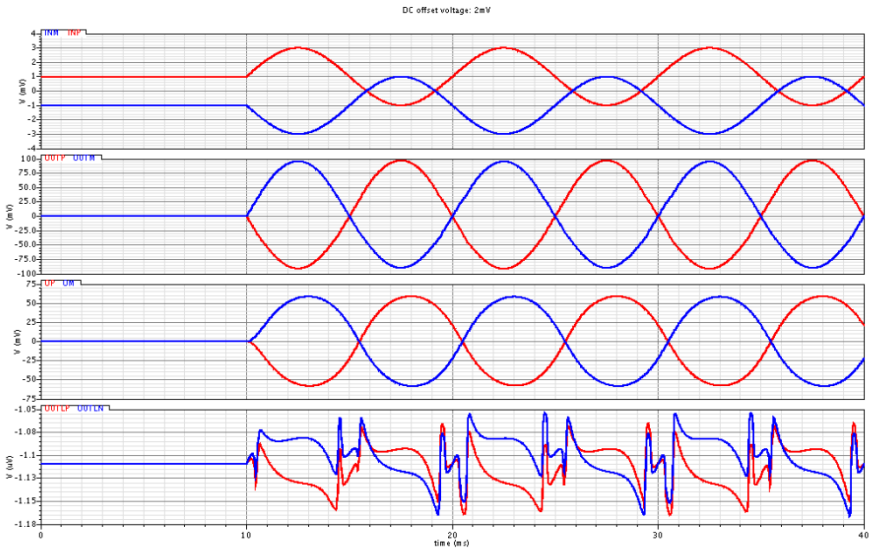

Figure 3.16 The transient simulation with DEO voltage 2mV.

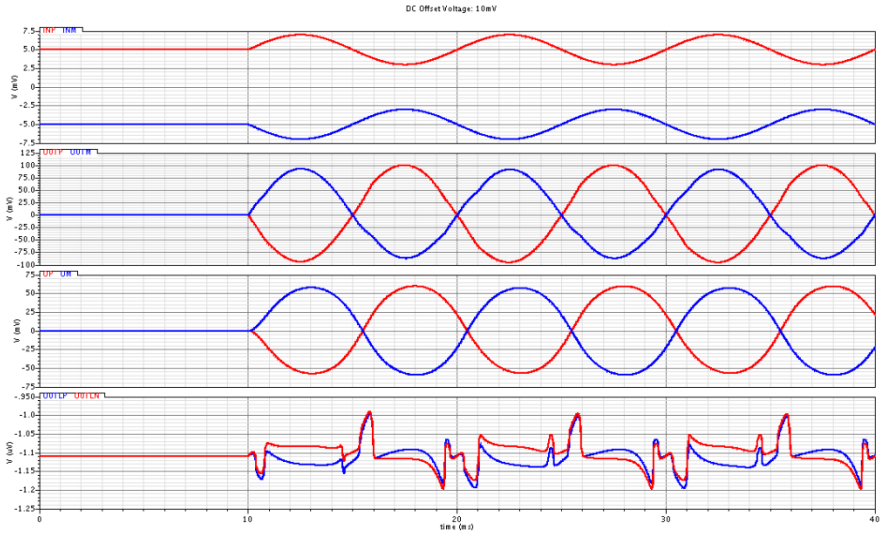

Figure 3.17 The transient simulation with DEO voltage 10mV.

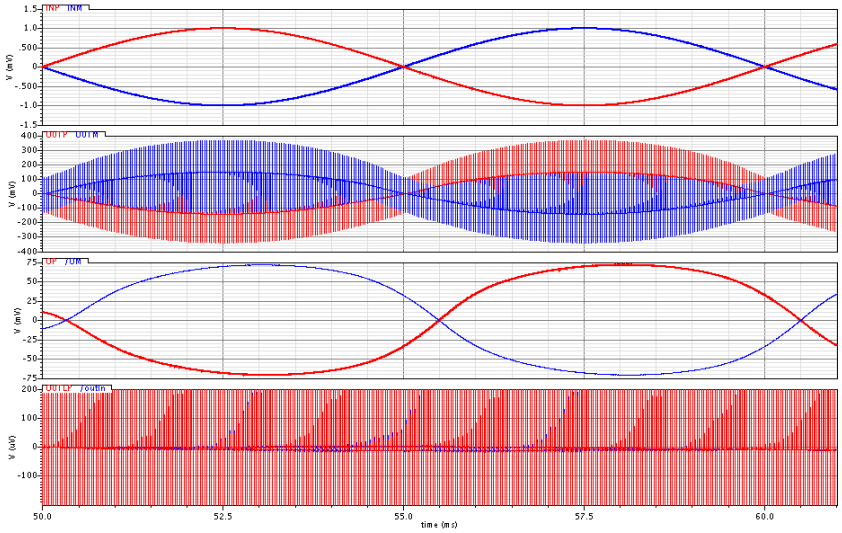

Figure 3.18 The transient simulation with 16 kHz chopper clock rate.

CHAPTER 4

A Low Power 12-bit SAR ADC with background calibration

Introduction

The analog-to-digital converter (ADC) is one of the key components in many medical devices. It is also one of the main components which cost most power in these devices. The advantages of the successive approximation register (SAR) ADC [19] [19] [20] are low power dissipation, medium speed, medium resolution and low energy per conversion-step.

A low-power, high resolution with background calibration SAR ADC is implemented, which is suitable for medical applications. First, the conventional SAR ADC will be brief review and the power saving method is introduced. Second, the capacitor array [21] will be described and modified. Third, the structure of the comparator with auto-zero technology is demonstrated. Fourth, the methodology of background calibration. Finally, the simulation results and summary are presented.

The conventional SAR ADC

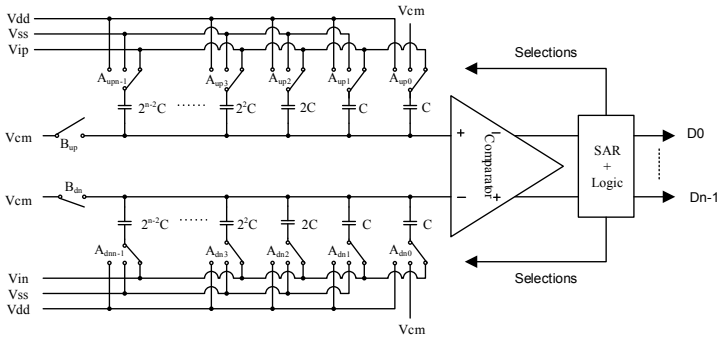

Figure 4.1 A conventional SAR ADC.

A conventional SAR ADC is shown in Figure 4.1. There are three main components, which are two capacitor arrays, a comparator and digital logic control block. For every

capacitor in the array, one terminal connects with the reference voltage, Vcm, and the other connects to the input signal during the sampling period. And during the comparing period, the capacitors disconnect with the reference voltage and the other connect to power supply. Every clock cycle, the comparator compares the storage voltages between the two capacitor arrays. According to the logic controller choose the selectors to charge one capacitor and discharge the other voltage in different capacitor arrays. The controller will repeat this compare function for 12 clock cycle. And then it starts the sampling period again.

The typical capacitor array

Figure 4.2 is a simplified SAR ADC block diagram. The DAC capacitor array is shown in Figure 4.3. There are three switches at the bottom plate of each capacitor. One switch connects with the reference voltage, "V_{REF}", which is usually the highest power supply, the second one connects with the input voltage, "V_{IN}". And the last one connects with the lowest power supply, "ground". There is only one switch at the bottom of each capacitor turned on at the same time.

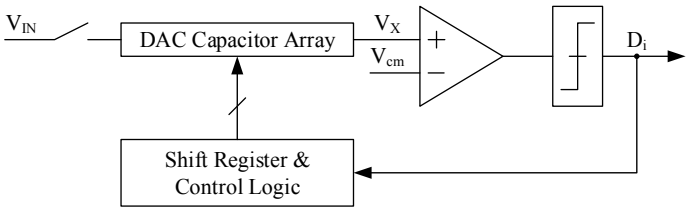

Figure 4.2 A simplified block diagram of a SAR ADC **[21]**.

During the sampling time, as illustrated in Figure 4.4 (a), all the bottom plates of capacitors switches to the input voltage, "V_{IN}". All the top plates connect to the half voltage, "V_{cm}" of the difference between the highest supply voltage, "V_{REF}", and the lowest supply voltage, "ground". The relationship can be expressed as

$$V_{cm} = \frac{1}{2}(V_{REF} - V_{ss}) \tag{4.1}$$

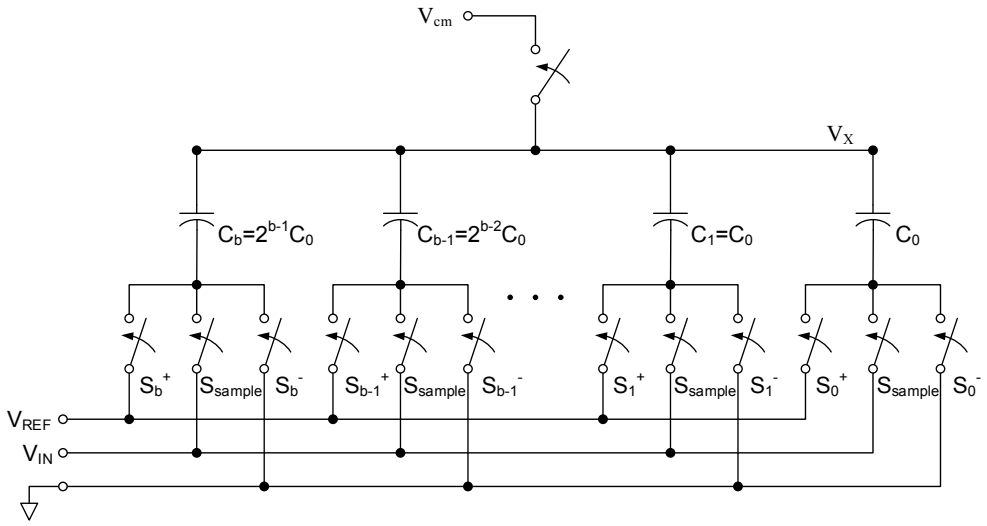

Figure 4.3 b-bit single-ended DAC capacitor array.

During the sampling period, the input voltage is fully stored in the capacitor array. During the comparing period, at time 0, which is the beginning at the 1st clock, as shown in Figure 4.4 (b) and (c), the bottom plate of the MSB capacitor is switched to V_{REF}, which means the switch, "S_b^+", turns on. For other capacitors, the switches, "S_{b-1}^- to S_0^-", turn on and the bottom plates connect to ground. The capacitor array is charged to reach the value as

$$V_X[1] = V_{cm} - V_{IN} + \frac{1}{2}V_{REF} \tag{4.2}$$

and the output of the latch is

$$D_1 = \begin{cases} 1, & V_{IN} < \frac{1}{2}V_{REF} \\ 0, & V_{IN} > \frac{1}{2}V_{REF} \end{cases} \tag{4.3}$$

If D_1 is low, "0", the 2nd largest capacitor, "C_{b-1}", is connected to V_{REF}, which means the switch, "S_{b-1}^+", is turned on at the next comparing clock cycle. However, if D_1 is high,

"1", the capacitor, "C_b", is switched to ground and the "C_{b-1}" is connected to "V_{REF}". Following this switch rules, the flowchart is drawn in Figure 4.5.

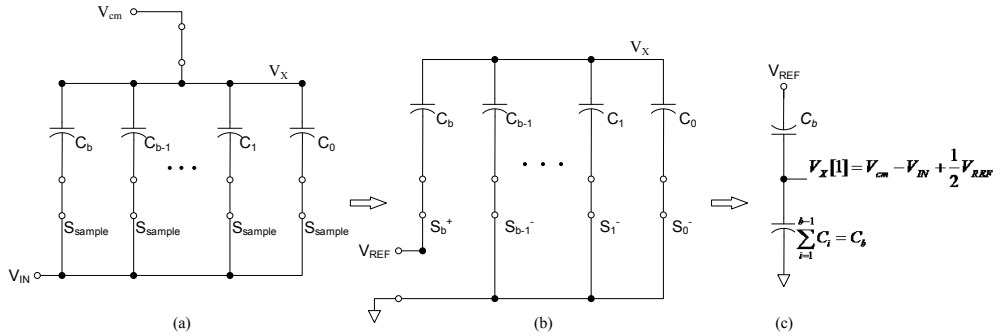

Figure 4.4 (a) The sampling period, (b) The 1st clock cycle of the comparing period, (c) The equivalent circuit of (b).

For a 3-bit SAR single-ended ADC, as shown in Figure 4.6, the bottom plate of the MSB capacitor, C_3=4C, is switched to V_{REF}. If the capacitor array settles in time T_P, the total energy can be derived from V_{REF} is

$$E_{0\to1} = \int_0^{T_P} i_{REF}(t)V_{REF}\,dt = V_{REF}\int_0^{T_P} i_{REF}(t)\,dt \tag{4.4}$$

$$i_{REF}(t) = -\frac{dQ_{C_3}}{dt},\ Q_{C_3}(0^+) = Q_{C_3}(0^-) = 4CV_X[0] \tag{4.5}$$

$$\Rightarrow E_{0\to1} = -V_{REF}\int_0^{T_P}\frac{dQ_{C_3}}{dt}dt = -V_{REF}\int_{Q_{C_3}(0)}^{Q_{C_3}(T_P)} dQ_{C_3} = -V_{REF}\times(Q_{C_3}(T_P)-Q_{C_3}(0)) \tag{4.6}$$

$$= -V_{REF}\times 4C\times\left((V_X[1]-V_{REF})-V_X[0]\right)$$

$$= -V_{REF}[C_3(V_X[1]-V_X[0])-C_3(V_{REF})]$$

$$= -V_{REF}[C_3(\Delta V_{X10})-C_3V_{REF}]$$

$$= C_3\times\left(-\frac{1}{2}V_{REF}^2\right)+C_3V_{REF}^2 = 2CV_{REF}^2$$

$$= E_{STEP0}+E_{SW0}$$

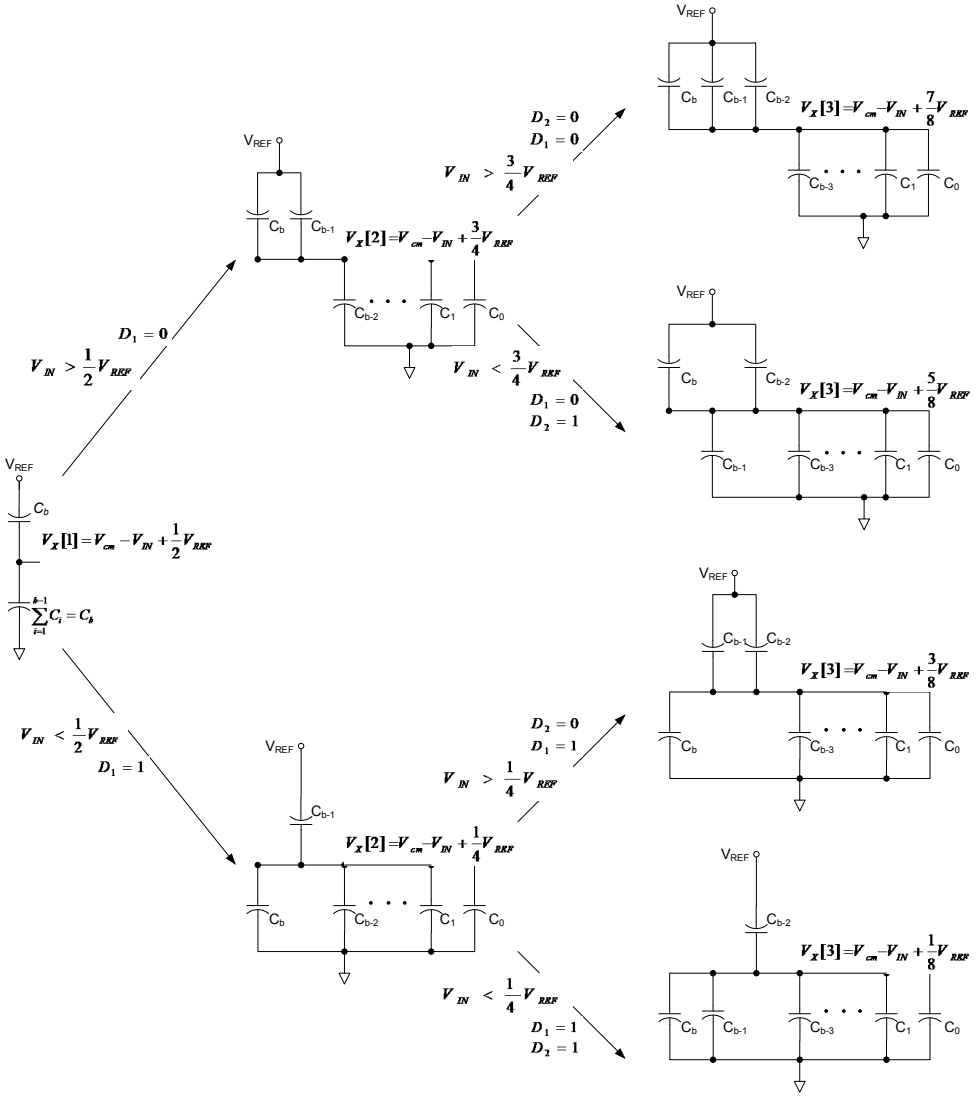

Figure 4.5 The flowchart of the first 3 clock cycles during the comparing period.

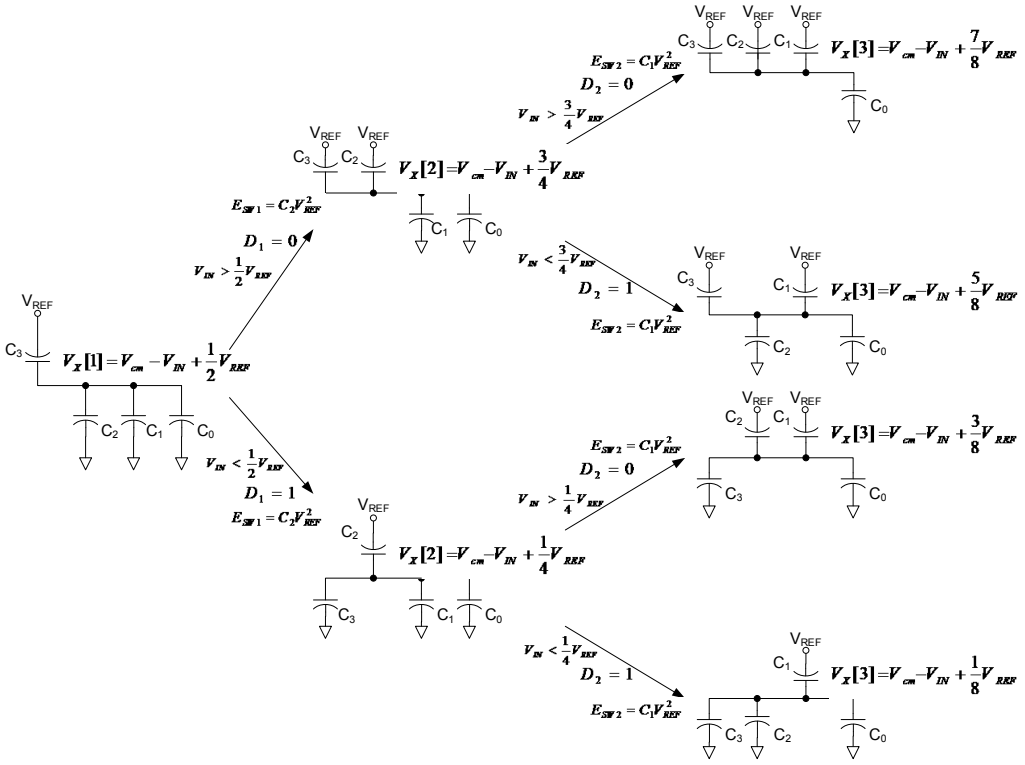

Figure 4.6 A 3-bit single-ended capacitor array.

During each comparing clock cycle, the total energy can be separated into two parts. One is named step energy, "E_{STEP}", the other is named switching energy, "E_{SW}". The step energy depends on the number of capacitors which connect to the reference voltage, "V_{REF}"; the switching energy depends on the smallest value of capacitors which connect to the reference voltage, "V_{REF}". The latch makes the decision, D_1, as expressed in (4.7), and the total energy, "$E_{1\rightarrow2}$", is calculated in (4.8) and (4.9). The output voltage of the capacitor at the 2nd comparing clock cycle is marked as, "$V_X[2]$". If "D_1" is high, the bottom plate of C_3 switches to ground, and C_2 connects to "V_{REF}". On the other hand, if "D1" is low, both of the bottom plates of C_3 and C_2 connect to "V_{REF}".

$$D_1 = \begin{cases} 0, & \Rightarrow V_X[2] = V_{cm} - V_{IN} + \frac{3}{4}V_{REF} \\ 1, & \Rightarrow V_X[2] = V_{cm} - V_{IN} + \frac{1}{4}V_{REF} \end{cases} \tag{4.7}$$

$D_1 = 0 \Rightarrow$

$$\begin{aligned} E_{1\to2} &= -V_{REF}\big[C_3\big((V_X[2] - V_{REF}) - (V_X[1] - V_{REF})\big) \\ &\quad + C_2\big((V_X[2] - V_{REF}) - V_X[1]\big)\big] \\ &= -V_{REF}[(C_3 + C_2)(V_X[2] - V_X[1]) - C_2(V_{REF})] \\ &= -V_{REF}[(C_3 + C_2)(\Delta V_{X21}) - C_2 V_{REF}] \\ &= (C_3 + C_2)\left(-\frac{1}{4}V_{REF}^2\right) + C_2 V_{REF}^2 = \frac{1}{2}CV_{REF}^2 \\ &= E_{STEP1\_0} + E_{SW1} \end{aligned} \tag{4.8}$$

$D_1 = 1 \Rightarrow$

$$\begin{aligned} E_{1\to2} &= -V_{REF}\big[C_2\big((V_X[2] - V_{REF}) - V_X[1]\big)\big] \\ &= -V_{REF}[C_2(V_X[2] - V_X[1]) - 2CV_{REF}] \\ &= -V_{REF}[C_2(\Delta V_{X21}) - C_2 V_{REF}] \\ &= C_2\left(\frac{1}{4}V_{REF}^2\right) + C_2 V_{REF}^2 = \frac{5}{2}CV_{REF}^2 \\ &= E_{STEP1\_1} + E_{SW1} \end{aligned} \tag{4.9}$$

(4.10) and (4.11) illustrate the output decisions at the 2nd clock cycle and the controller selects the switches to generate the output voltage of the capacitor array, "$V_X[3]$", at the 3rd comparing clock cycle.

$$D_1 = 0, D_2 = \begin{cases} 0, & \Rightarrow V_X[3] = V_{cm} - V_{IN} + \frac{7}{8}V_{REF} \\ 1, & \Rightarrow V_X[3] = V_{cm} - V_{IN} + \frac{5}{8}V_{REF} \end{cases} \tag{4.10}$$

$$D_1 = 1, D_2 = \begin{cases} 0, & \Rightarrow V_X[3] = V_{cm} - V_{IN} + \frac{3}{8}V_{REF} \\ 1, & \Rightarrow V_X[3] = V_{cm} - V_{IN} + \frac{1}{8}V_{REF} \end{cases} \tag{4.11}$$

There are 4 different conditions for the 3rd comparing clock cycle as shown in Figure 4.5. The total energy for these cases depend on the switches. Equations (4.12), (4.13), (4.14) and (4.15) are the detail calculations.

$D_1 = 0, D_2 = 0 \Rightarrow$

$$\begin{aligned} E_{2\to3} &= -V_{REF}\big[C_3\big((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})\big) \\ &\quad + C_2\big((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})\big) + C_1((V_X[3] - V_{REF}) - V_X[2])\big] \\ &= -V_{REF}[(C_3 + C_2 + C_1)(V_X[3] - V_X[2]) - C_1(V_{REF})] \\ &= -V_{REF}[(C_3 + C_2 + C_1)(\Delta V_{X32}) - C_1 V_{REF}] \\ &= (C_3 + C_2 + C_1)\left(-\frac{1}{8}V_{REF}^2\right) + C_1 V_{REF}^2 = \frac{1}{8}CV_{REF}^2 \\ &= E_{STEP2\_00} + E_{SW2} \end{aligned} \tag{4.12}$$

$D_1 = 0, D_2 = 1 \Rightarrow$

$$\begin{aligned} E_{2\to3} &= -V_{REF}\big[C_3\big((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})\big) + C_1((V_X[3] - V_{REF}) - V_X[2])\big] \\ &= -V_{REF}[(C_3 + C_1)(V_X[3] - V_X[2]) - C_1(V_{REF})] \\ &= -V_{REF}[(C_3 + C_1)(\Delta V_{X32}) - C_1 V_{REF}] \\ &= (C_3 + C_1)\left(-\frac{1}{8}V_{REF}^2\right) + C_1 V_{REF}^2 = \frac{3}{8}CV_{REF}^2 \\ &= E_{STEP2\_01} + E_{SW2} \end{aligned} \tag{4.13}$$

$D_1 = 1, D_2 = 0 \Rightarrow$

$$E_{2\to3} = -V_{REF}\big[C_2\big((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})\big) + C_1((V_X[3] - V_{REF}) - V_X[2])\big] \tag{4.14}$$

$$= -V_{REF}[(C_2 + C_1)(V_X[3] - V_X[2]) - C_1(V_{REF})]$$
$$= -V_{REF}[(C_2 + C_1)(\Delta V_{X32}) - C_1 V_{REF}]$$
$$= (C_2 + C_1)\left(+\frac{1}{8}V_{REF}^2\right) + C_1 V_{REF}^2 = \frac{11}{8}CV_{REF}^2$$
$$= E_{STEP2\_10} + E_{SW2}$$

$D_1 = 1, D_2 = 1 \Rightarrow$

$$E_{2\to3} = -V_{REF}[C_1((V_X[3] - V_{REF}) - V_X[2])]$$
$$= -V_{REF}[C_1(V_X[3] - V_X[2]) - C_1(V_{REF})]$$
$$= -V_{REF}[C_1(\Delta V_{X32}) - C_1 V_{REF}]$$
$$= C_1\left(-\frac{1}{8}V_{REF}^2\right) + C_1 V_{REF}^2 = \frac{7}{8}CV_{REF}^2$$
$$= E_{STEP2\_11} + E_{SW2} \qquad (4.15)$$

According to the above process, the value of V_x at every comparing clock cycle, after switching transients have settled, is below

*At the **n**th comparing clock cycle*
$$V_X[n] = V_{cm} - V_{IN} + \frac{C_T}{C_T + C_B}V_{REF} \qquad (4.16)$$

Where C_T is the sum of all capacitors connected to the reference voltage, and C_B is the sum of all capacitors connected to ground.

$$C_T = \sum_i 2^{i-1}C \qquad \text{for } i \text{ such that } D_i=0 \qquad (4.17)$$
$$C_B = \sum_i 2^{i-1}C \qquad \text{for } i \text{ such that } D_i=1 \qquad (4.18)$$

and then the total energy of the capacitor array at the ***n**th* comparing clock cycle is defined as

$$E_{(n-1)\to n} = E_{STEP\_n} + E_{SW\_n} \qquad (4.19)$$
$$E_{STEP\_n} = C_T V_{REF}(V_X[n] - V_X[n-1]) = C_T V_{REF}(\Delta V_X) \qquad (4.20)$$
$$E_{SW\_n} = C_n V_{REF}^2 \qquad (4.21)$$

The energy saving capacitor array

A b-bit single-ended energy-saving capacitor array is illustrated in Figure 4.7. The difference between the conventional capacitor array and the energy-saving capacitor array is that the MSB capacitor, which is in the conventional array, replaced to the (b-1)-bit capacitor array. Therefore, in a b-bit energy-saving capacitor array there are two (b-1)-bit capacitor arrays, "upper array" and "lower array" connected together.

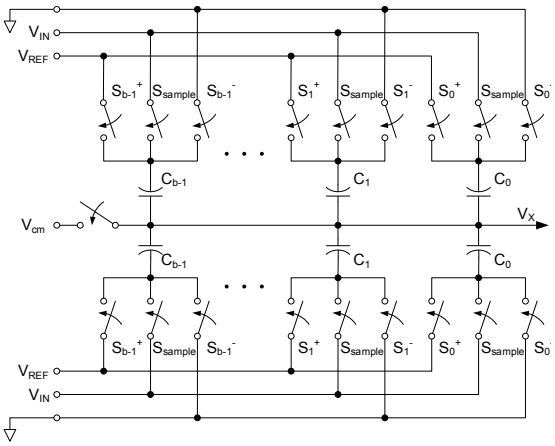

Figure 4.7 The b-bit single-ended energy-saving DAC capacitor array.

Figure 4.8 (a) demonstrates the sampling period for the b-bit energy-saving capacitor array and (b) is the 1st comparing clock cycle; (c) is the equivalent circuit which is the same as Figure 4.4 (c).

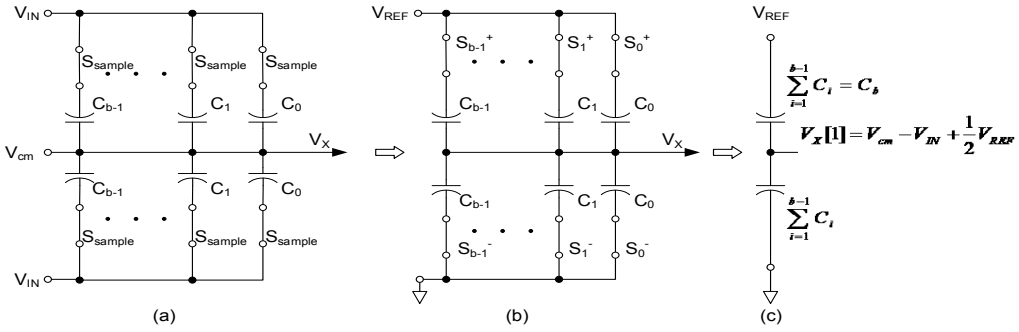

Figure 4.8 (a) The sampling period, (b) The 1st clock cycle of the comparing period, (c) The equivalent circuit of (b)

A 3-bit SAR DAC single-ended capacitor array, as shown in Figure 4.9, , has the same step energy with the conventional one. However, there is no the switching energy when D_n is "1" during the ***nth*** comparing clock cycle. The equations from (4.22) to (4.27) are the calculation. Finally, the total energy of the capacitor array at the ***nth*** comparing clock cycle is defined as

$$E_{(n-1)\to n} = E_{STEP\_n} + E_{SW\_n} \tag{4.19}$$

$$E_{STEP\_n} = C_T V_{REF}(V_X[n] - V_X[n-1]) = C_T V_{REF}(\Delta V_X) \tag{4.20}$$

$$E_{SW\_n} = C_n \cdot \overline{D_n} \cdot V_{REF}^2 \tag{4.21}$$

$D_1 = 0 \Rightarrow$

$$\begin{aligned} E_{1\to 2} &= -V_{REF}[(C_2 + C_1 + C_0)\big((V_X[2] - V_{REF}) - (V_X[1] - V_{REF})\big) \\ &\quad + C_2((V_X[2] - V_{REF}) - V_X[1])] \\ &= -V_{REF}[(C_3 + C_2)(\Delta V_{X12}) - C_2 V_{REF}] \\ &= -V_{REF}(C_3 + C_2)\left(\frac{1}{4}V_{REF}\right) + C_2 V_{REF}^2 = -\frac{1}{2}C_2 V_{REF}^2 \\ &= E_{STEP1\_1} + E_{SW1} \end{aligned} \tag{4.22}$$

$D_1 = 1 \Rightarrow$

$$\begin{aligned} E_{1\to 2} &= -V_{REF}[(C_1 + C_0)\big((V_X[2] - V_{REF}) - (V_X[1] - V_{REF})\big)] \\ &= -V_{REF}[C_2(\Delta V_{X12})] \\ &= -V_{REF}[C_2\left(-\frac{1}{4}V_{REF}\right)] = \frac{1}{4}C_2 V_{REF}^2 \\ &= E_{STEP1\_0} \end{aligned} \tag{4.23}$$

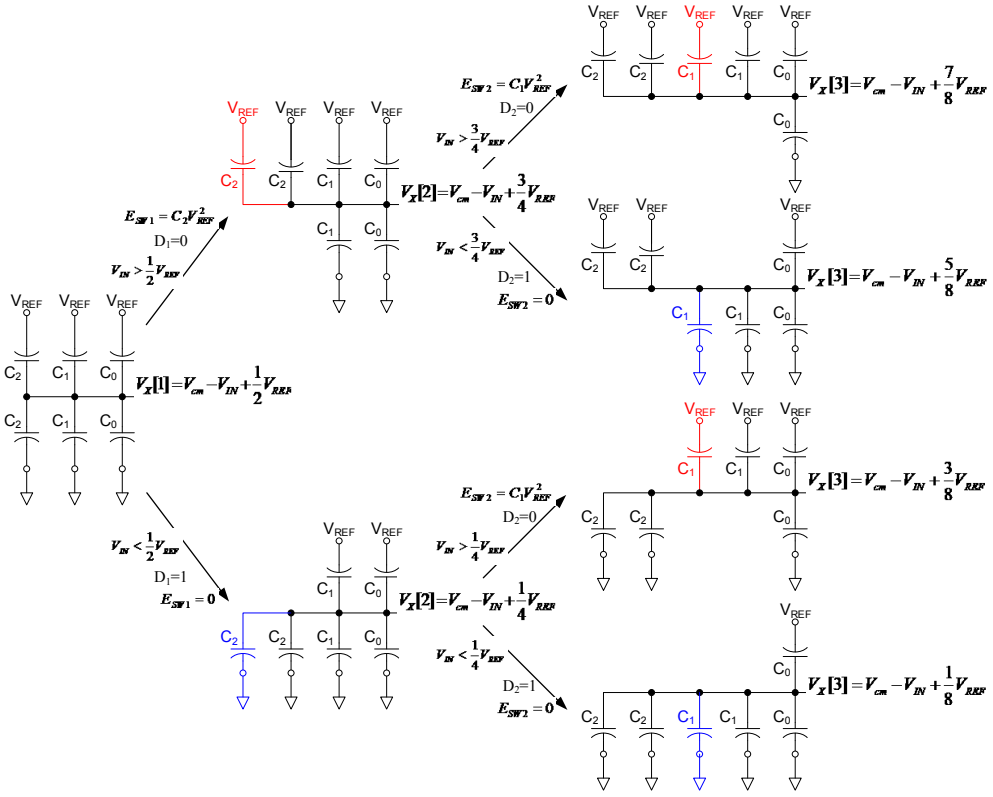

Figure 4.9 A 3-bit single-ended energy-saving capacitor array.

$D_1 = 0\,, D_2 = 0 \Rightarrow$

$$\begin{aligned} E_{2\to3} &= -V_{REF}[(C_2 + C_2 + C_1 + C_0)((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})) \\ &\qquad + C_1((V_X[3] - V_{REF}) - V_X[2])] \\ &= -V_{REF}[(C_3 + C_2 + C_1)(\Delta V_{X23}) - C_1 V_{REF}] \\ &= -V_{REF}(C_3 + C_2 + C_1)\left(\frac{1}{8}V_{REF}\right) + C_1 V_{REF}^2 \\ &= E_{STEP2\_00} + E_{SW2} \end{aligned} \tag{4.24}$$

$D_1 = 0\,, D_2 = 1 \Rightarrow$

$$\begin{aligned} E_{2\to3} &= -V_{REF}[(C_2 + C_2 + C_0)((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})) \\ &\qquad + C_1(V_X[3] - V_X[2])] \\ &= -V_{REF}[(2C_2 + C_1 + C_0)(\Delta V_{X23})] \end{aligned} \tag{4.25}$$

$$= -V_{REF}(C_3 + C_1)\left(-\frac{1}{8}V_{REF}\right)$$

$$= E_{STEP2\_01}$$

$D_1 = 1, D_2 = 0 \Rightarrow$

$$E_{2\to3} = -V_{REF}[(C_1 + C_0)((V_X[3] - V_{REF}) - (V_X[2] - V_{REF})) + C_1((V_X[3] - V_{REF}) - V_X[2])]$$

$$= -V_{REF}[(2C_1 + C_0)(\Delta V_{X23}) - C_1 V_{REF}] \quad (4.26)$$

$$= -V_{REF}(C_2 + C_1)\left(\frac{1}{8}V_{REF}\right) + C_1 V_{REF}^2$$

$$= E_{STEP2\_10} + E_{SW2}$$

$D_1 = 1, D_2 = 1 \Rightarrow$

$$E_{2\to3} = -V_{REF}[C_0(V_X[3] - V_{REF}) - (V_X[2] - V_{REF}))]$$

$$= -V_{REF}[C_0(\Delta V_{X23})] \quad (4.27)$$

$$= -V_{REF}(C_1)\left(-\frac{1}{8}V_{REF}\right)$$

$$= E_{STEP2\_11}$$

Comparing the conventional and energy-saving capacitor arrays [22]

The 3-bit SAR ADC examples are illustrated in Figure 4.10 and Figure 4.11. During the sampling period, one terminal connects to the input, “Vip” or “Vin”, and the other connects to the reference voltage, “Vcm”, as shown in Figure 4.10. Each capacitor array has 4 capacitors, C_0, C_1, C_2 and C_3. C_1 is the minimum value, called the least significant bit (LSB). C_3 is the maximum value, called the most significant bit (MSB). The minimum unit of the capacitor is C, 20fF, and the area is 4.08μm×4.08μm. C_0 and C_1 have the same value, C. C_2 is 2^{2-1} times as C_0, and C_3 is 2^{3-1} times as C_0, as shown in Table 4.1.

During the comparing period, there are different switching energies, illustrated in Figure 4.12 and Figure 4.13. In the first cycle, only the MSB capacitor connects with the high power supply voltage, “Vdd”, others connect with the low power supply voltage, “Vss”, in the upper capacitor array; the opposite connections are in the lower capacitor array.

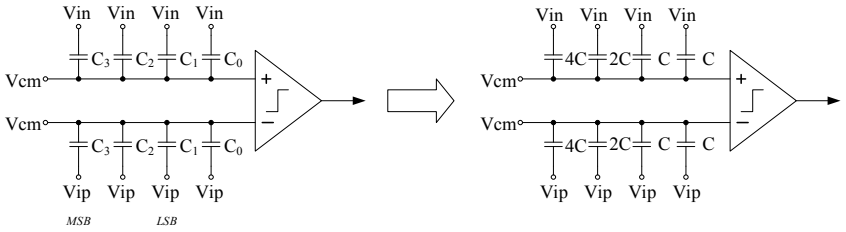

Figure 4.10 A 3-bit SAR ADC with conventional capacitor arrays in both inputs at sampling period.

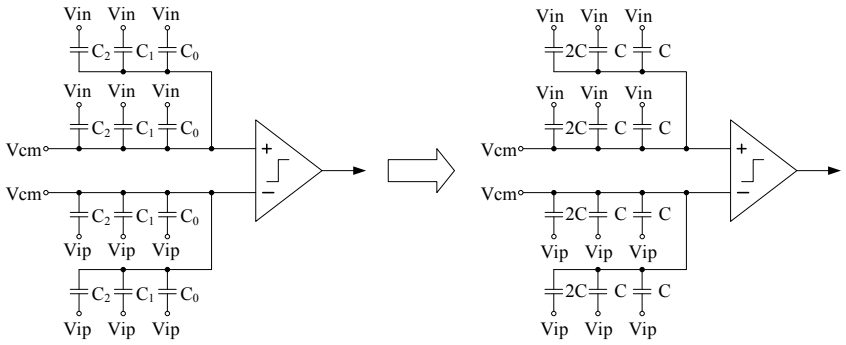

Figure 4.11 A 3-bit SAR ADC with energy-saving capacitor arrays in both inputs at sampling period

Table 4.1 The value of the upper capacitor array for the example 3-bit SAR ADC.

Name	Value
C_0	C = 20fF
C_1	C = 20fF
C_2	2C = 40fF
C_3	4C = 80fF

According to the rules from (4.7) to (4.21), the n-bit total energy of the conventional SAR ADC with two input capacitor arrays are derived as

$$E_{total_n-bit} = \sum_{i=1}^{n} 2^{n+1-2i}(2^i - 1) \cdot C \cdot V_{ref}^2 \tag{4.28}$$

According to the rules from (4.22) to (4.27), the n-bit total energy of the energy-saving SAR ADC with two input capacitor arrays are derived as

$$E_{total_n-bit} = [2^{n-2} + \sum_{i=1}^{n-1} 2^{n-1-2i}(2^i + 1)] \cdot C \cdot V_{ref}^2 \tag{4.29}$$

- $V_{cm} = \frac{1}{2}(V_{dd} + V_{ss})$ (4.30)
- $V_{ref} = V_{dd} - V_{ss}$ (4.31)

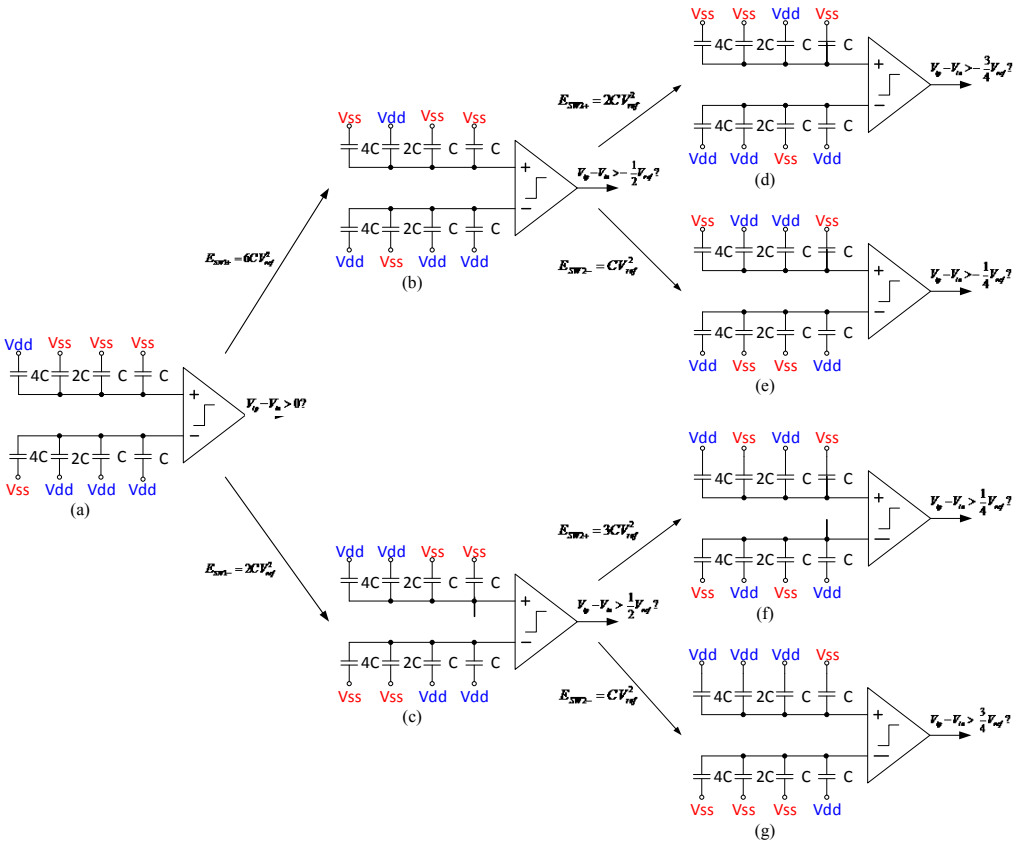

Figure 4.12 A 3-bit conventional SAR ADC.

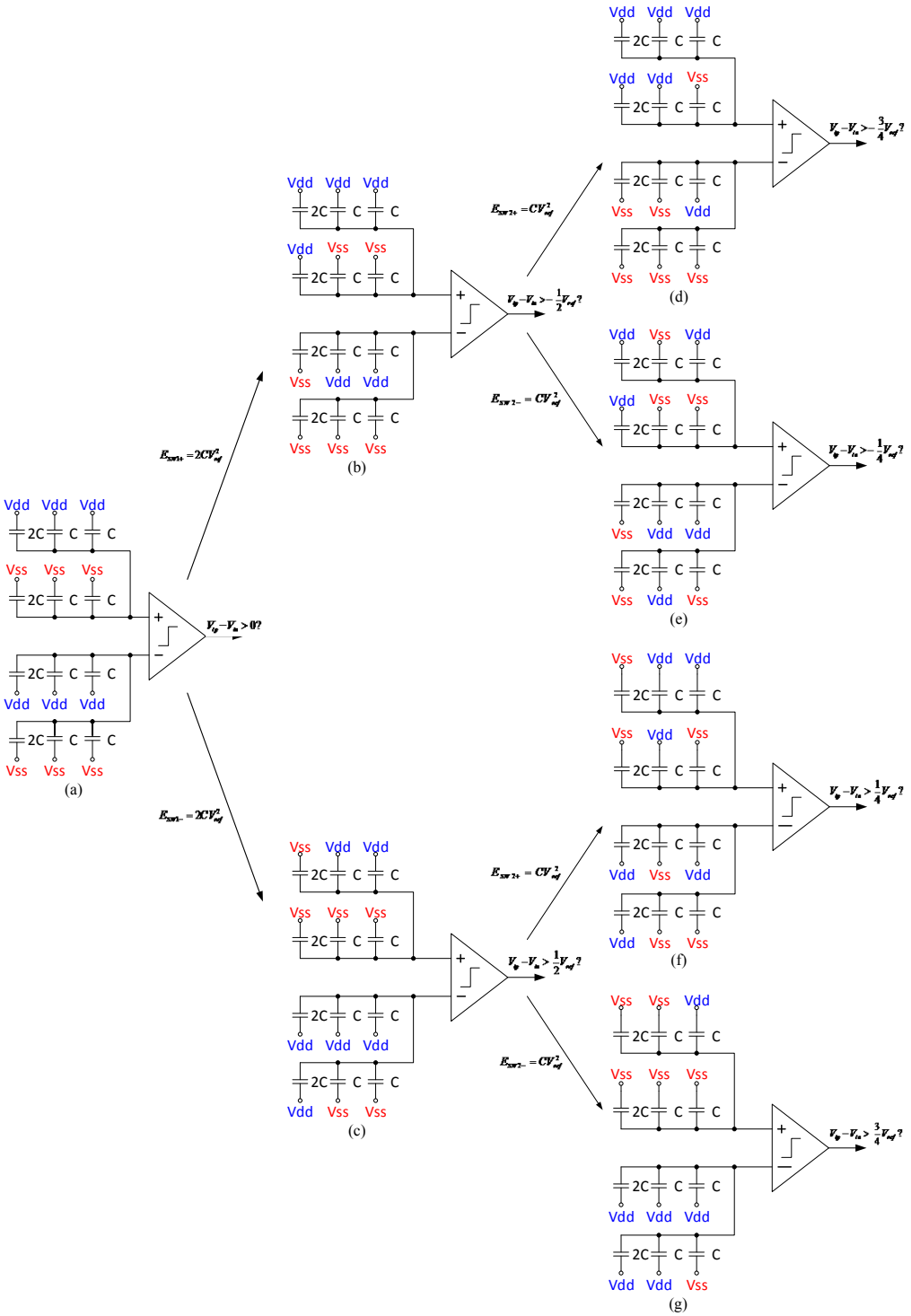

Figure 4.13 A 3-bit energy saving SAR ADC.

The Split Capacitor Array

For a conventional SAR DAC capacitor array, the maximum capacitor value is 2^{N-1} times the minimum one. N is the number of bits of the ADC. Our design is a 12 bits SAR ADC, so the minimum capacitor is 20fF, which is 4.08μm×4.08μm area. The maximum capacitor would be 40.96pF and the area is 2048 times of the minimum capacitor. It is not reasonable implementation for VLSI. Therefore, the split capacitor is used to separate one capacitor array into two arrays, a main capacitor array and a sub capacitor by using a bridge capacitor, "C_{bg}," connected these arrays, as shown in Figure 4.14. The combination capacitor of the bridge capacitor and the sub capacitor array should be the minimum capacitor value, which can expressed as

$$\frac{C_{bg} \times \sum_{i=0}^{N-M} C_{S,i}}{C_{bg} + \sum_{i=0}^{N-M} C_{S,i}} = \frac{C_{bg} \times [\sum_{i=1}^{N-M}(2^{i-1} \times C) + C]}{C_{bg} + [\sum_{i=1}^{N-M}(2^{i-1} \times C) + C]} = C \tag{4.32}$$

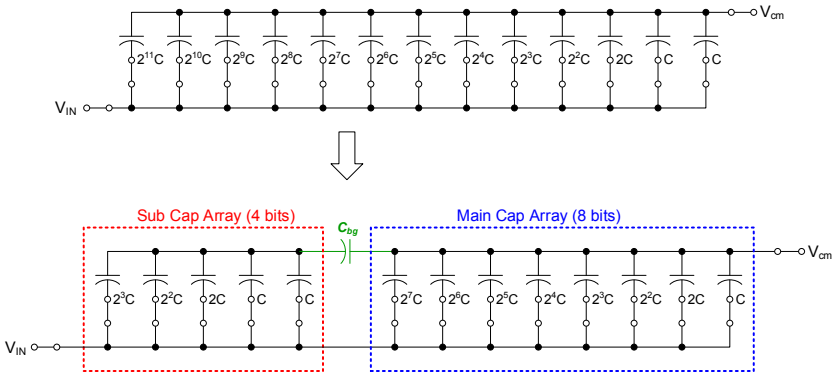

Figure 4.14 An example of the spilt capacitor array during the sampling period.

Separating a 12-bit conventional capacitor array into a 8-bit main capacitor array and a 4-bit sub capacitor array, the maximum capacitor would be reduced from 2^{11}C to 2^{7}C, which is 2.56pF. Finally, combining the two different separated methodologies, as shown in Figure 4.15, we propose another split capacitor array which not only can save more

energy, but also can reduce the area of capacitors. The maximum energy for the nth-bit can be derived as

$$k \le m \quad E_{n-bit} = 2^{k-1} \cdot (1 - \frac{2^k - 1}{2^{m+1}}) \cdot CV_{ref}^2 \tag{4.33}$$

$$k > m \quad E_{n-bit} = 2^{-(k+1)} \cdot (2^n - 2^m - 2^{-(1+n-m)} - 2^{-(n+m-k)} - 1) \cdot CV_{ref}^2 \tag{4.34}$$

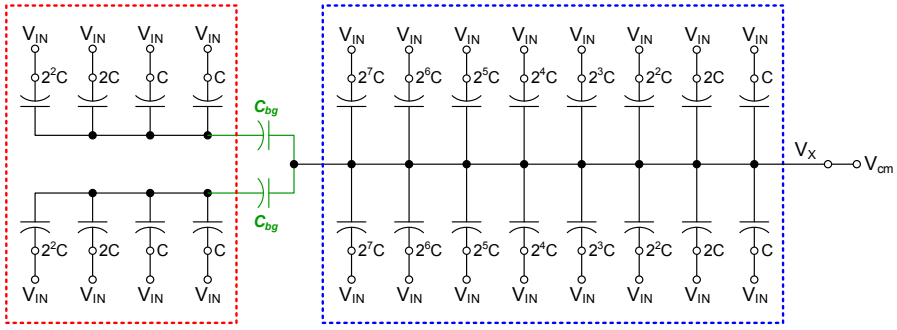

Figure 4.15 The proposed split capacitor array during sampling period.

There are two examples to illustrate this split capacitor array works by using the same method controlled the switches. Figure 4.16 and Figure 4.17 are the first single split capacitor array, which has a 3-bit main DAC capacitor array and a 2-bit sub DAC capacitor array. There are 5 comparing clock cycles to decide the ADC outputs. At the first three cycles, the main capacitor array would be selected from MSB to LSB, as shown in Figure 4.16. During the rest cycles, the sub capacitor array would be operated like Figure 4.17, which illustrates the selections after the first three bits is "111." We could treat the voltage nodes "V_{z1}" and "V_{z2}" are the same node during the period. Then the switches follow the same rules as selecting the main capacitor array.

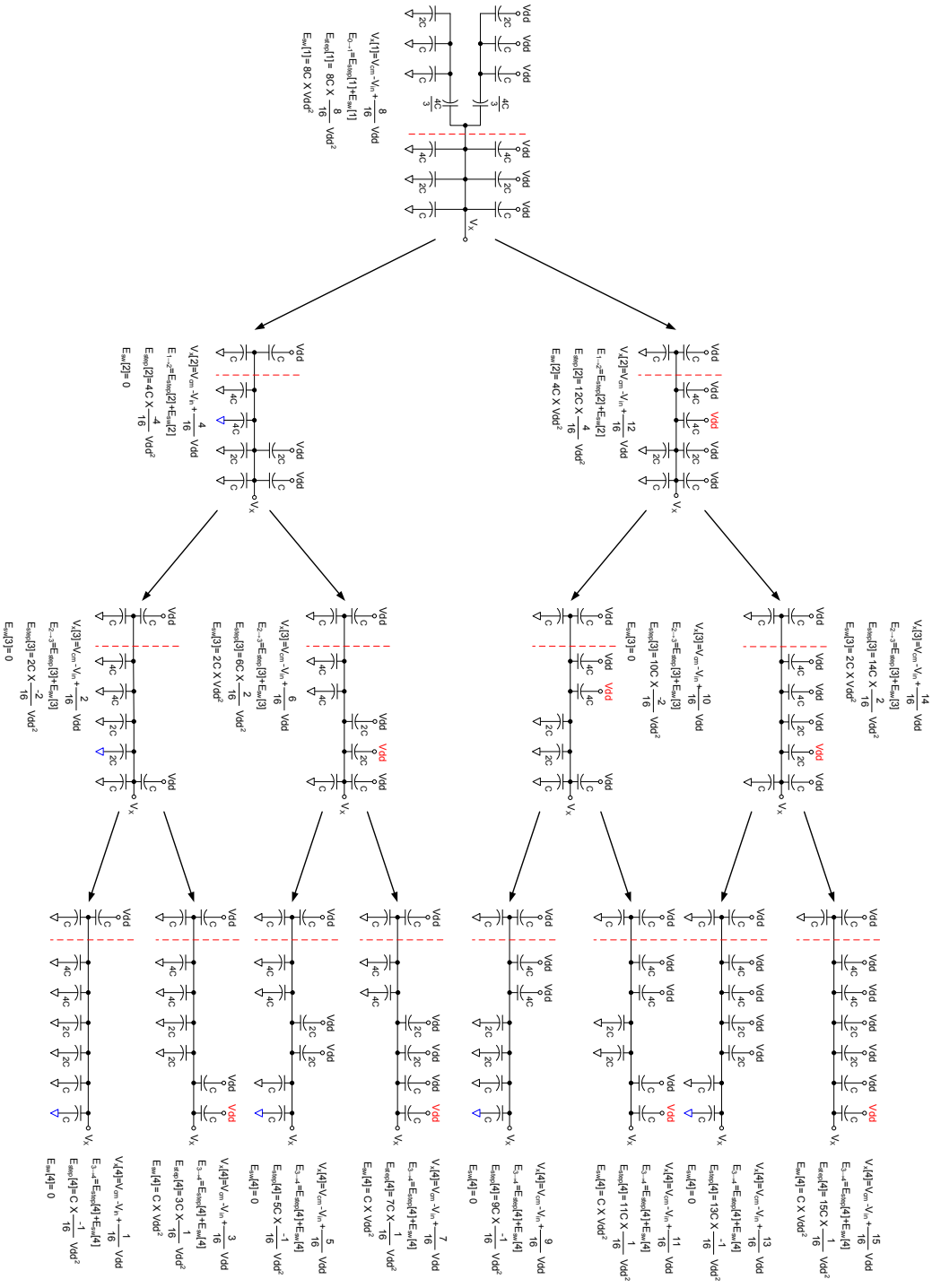

Figure 4.16 An example of 3-bit main and 2-bit sub capacitor array (part I).

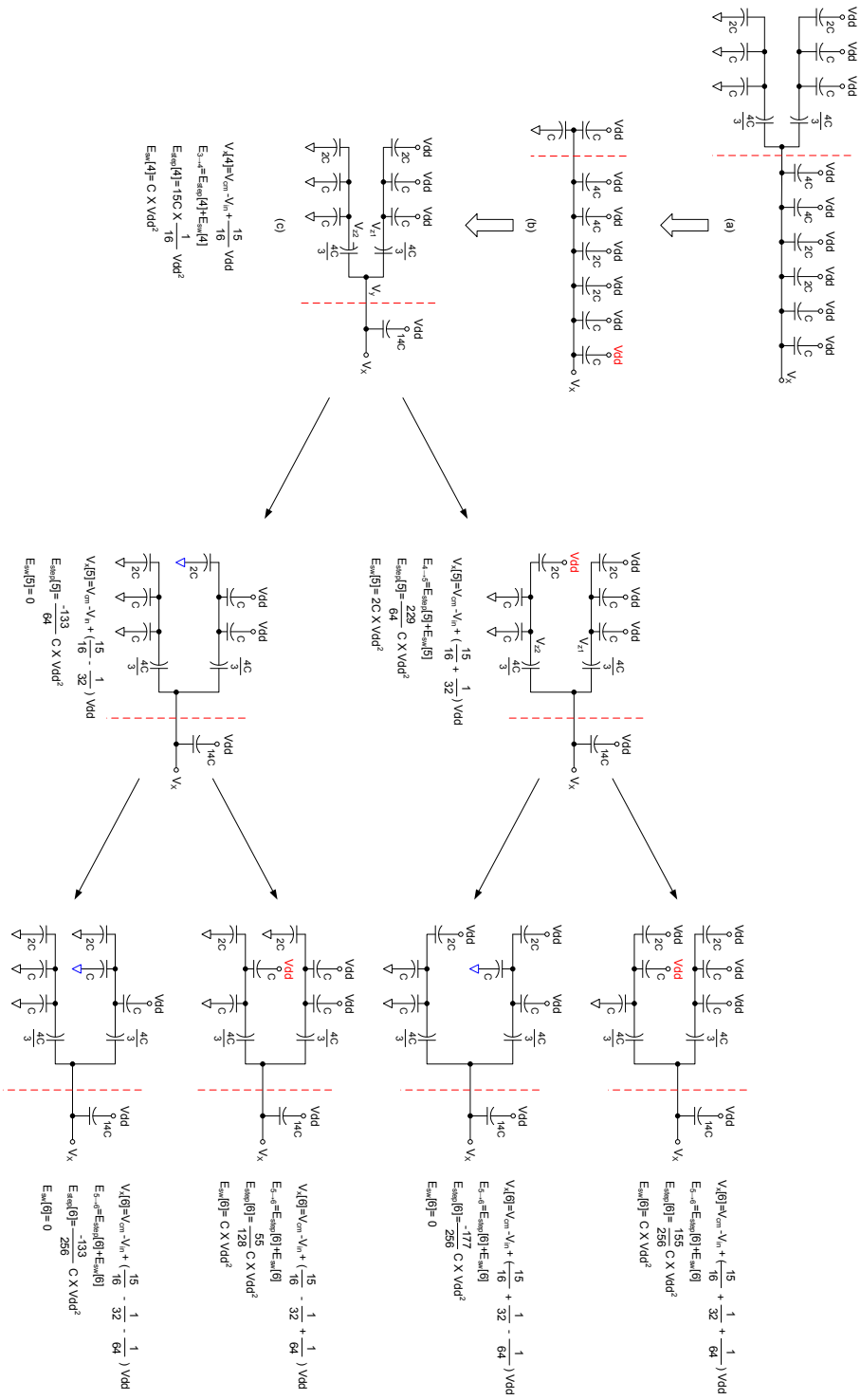

Figure 4.17 An example of 3-bit main and 2-bit sub capacitor array (part II).

Finally, we can compare these three different switching energies, as shown in Figure 4.18 and Figure 4.19. The new method has only 10% switching energy compared to the conventional method. The total capacitor array are is about 21.1pF, only 12.8% compared to the conventional method. Table 4.2 is a summary of these three ways of the capacitor array.

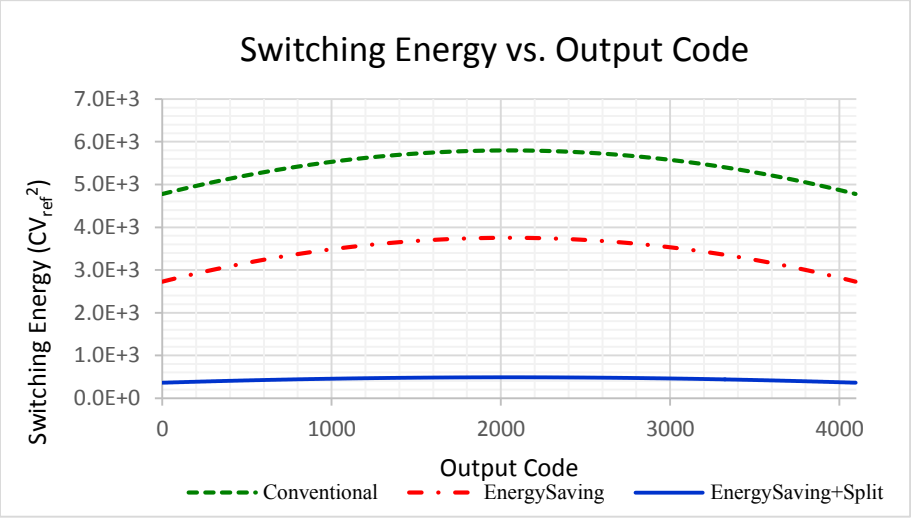

Figure 4.18 Switching Energy vs. Output Code.

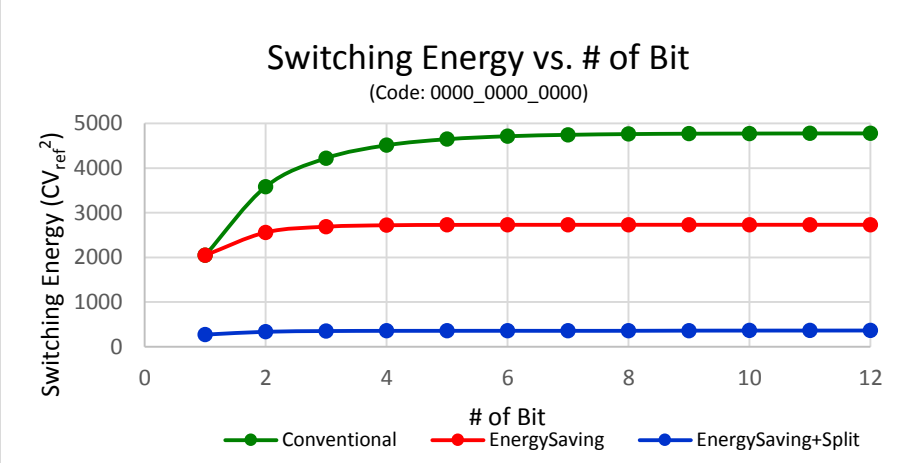

Figure 4.19 Switching Energy vs. #of Bit.

Table 4.2 Summary of three methods for the capacitor array.

Method	Area (μm^2)	C_{total}	# of Switches	Average Switching Energy ($C \times V_{ref}^2$)
Conventional	131,072	163.84pF	72	5.46×10^3
Energy Saving	131,072	163.84pF	144	3.41×10^3
Energy Saving + Split	16,880	21.10pF	144	446.3

Clock generation circuit

The maximum sampling rate is 500 kHz; and there are 1 sampling cycle and 12 comparing cycles. The clock rate is 6.5 MHz. The switches of capacitor array are CMOS pairs, therefore we need two nonoverlapping phase clocks to control the switches, as illustrated in Figure 4.20, which make sure there is only one potential voltage connected with capacitors. Since the power supply is 1 volt, the switches will not turn on completely. Therefore, the bootstrapping circuit, as shown in Figure 4.21 is added to double the voltage to 1.8 volt for sampling switches.

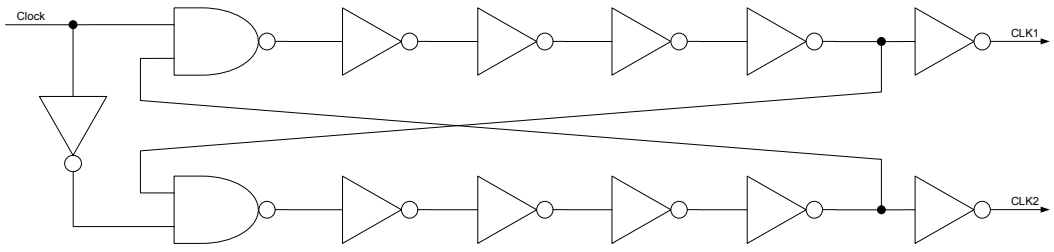

Figure 4.20 Nonoverlapping clock generation circuit.

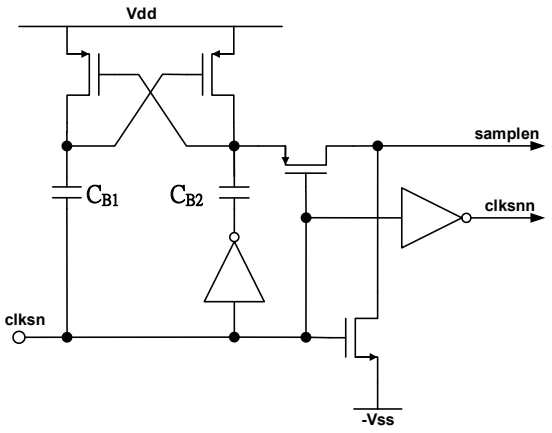

Figure 4.21 The bootstrapping circuit.

The structure of the comparator

Figure 4.22 is the comparator which includes three series pre-amplifiers and a latch. The first pre-amplifier is a rail-to-rail amplifier with a common mode feedback, as shown in Figure 4.23 and Figure 4.24. The others are the same with the nmos input pair. The total gain is about 10 V/V (≈ 20dB).

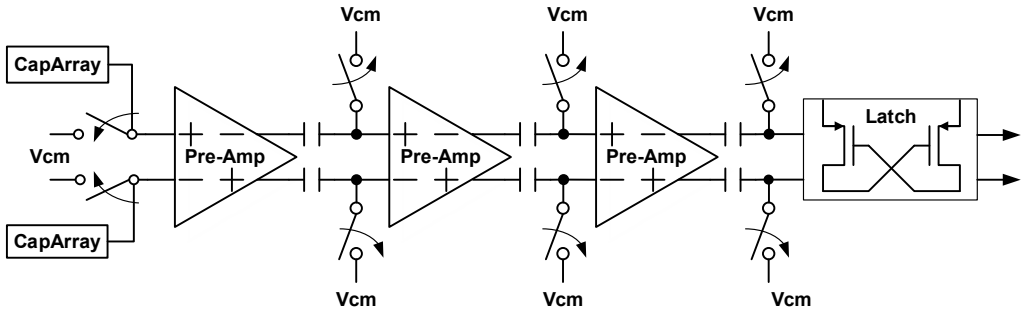

Figure 4.22 The comparator with input offset voltage cancellation by auto-zero technique

The auto-zero technique is used to cancel the input offset voltage, which comes from the mismatch of the pre-amplifier. During the sampling period, the switches turn on and all inputs of the pre-amplifiers and the inputs of the latch connect to the reference voltage, "V_{cm}". Each offset voltage is storage in the capacitors which connect with outputs of each pre-amplifier and inputs of the next stage. However, the auto-zero technique cannot compensate the input offset of the latch. Therefore, the digital background calibration helps to improve the accuracy of the SAR ADC.

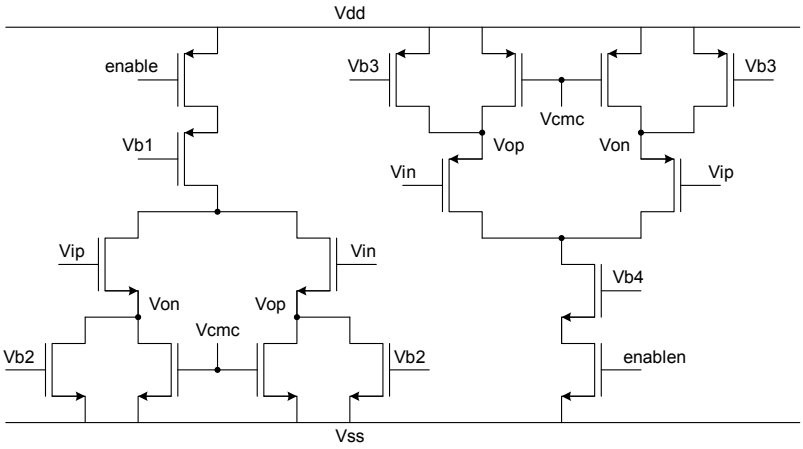

Figure 4.23 The rail-to-rail pre-amplifier.

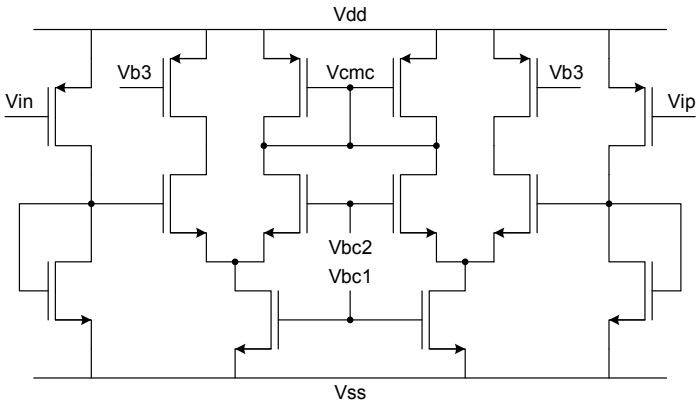

Figure 4.24 The common mode feedback circuit.

The background calibration [23] [24] [25]

For differential devices, the most important part of the input offset voltage comes from the input pair mismatch, which can be categorized into threshold mismatch, ΔV_{th}, and the current factor mismatch, $\Delta\beta$. In this latch design, the drawn size of input transistor is W/L=1.44μm/1.44μm, and the fingers, "nf," is 16. The equations are derived as below:

$$I_D = \frac{1}{2} C_{ox} \mu_n \left(\frac{W}{L}\right) \cdot (V_{GS} - V_{th})^2 = \frac{\beta}{2}(V_{GS} - V_{th})^2 \tag{4.35}$$

$$\Rightarrow \quad g_m = \sqrt{2\beta I_D} = \frac{2I_D}{V_{GS} - V_{th}} \tag{4.36}$$

$$\Rightarrow \Delta I_D = \frac{\Delta\beta}{2} \cdot (V_{GS} - V_{th})^2 - \Delta V_{th} \cdot \beta \cdot (V_{GS} - V_{th}) + \Delta V_{GS} \cdot \beta \cdot (V_{GS} - V_{th}) \tag{4.37}$$

Assuming the constant current $\Rightarrow \Delta I_D = 0$

$$\Rightarrow 0 = \frac{\Delta\beta}{2}(V_{GS} - V_{th}) + \beta(\Delta V_{GS} - \Delta V_{th}) \tag{4.38}$$

$$\Rightarrow \Delta V_{GS} = -\frac{\Delta\beta}{\beta} \cdot \frac{1}{2} \cdot (V_{GS} - V_{th}) + \Delta V_{th} = -\frac{\Delta\beta}{\beta} \cdot \frac{I_D}{g_m} + \Delta V_{th} \tag{4.39}$$

$$\Rightarrow \sigma(\Delta V_{GS}) = \sqrt{\left(\frac{\sigma(\Delta\beta)}{\beta} \cdot \frac{I_D}{g_m}\right)^2 + (\sigma(\Delta V_{th}))^2} \tag{4.40}$$

Consider the "self-mismatch"

$$\Delta V_{th} = V_{th1} - V_{th2} \tag{4.41}$$

$$\sigma_{\Delta V_{TH}} = \sqrt{\sigma_{V_{th1}}^2 + \sigma_{V_{th2}}^2} = \sqrt{2\sigma_{V_{th}}^2} = \frac{A_{V_{th}}}{\sqrt{WL}} \tag{4.42}$$

The differential input pair of the latch could be modeled as Figure 4.25. The effective channel length, "L_{eff}," for the drawn length of 1.44μm is 1.372μm. The standard deviation of the random mismatches can be approximated by [5],

$$\sigma^2(\Delta V_{th}) = \frac{A_{V_{th}}^2}{WL_{eff}} \tag{4.43}$$

$$\frac{\sigma^2(\Delta\beta)}{\beta^2} = \frac{A_\beta^2}{WL_{eff}} \tag{4.44}$$

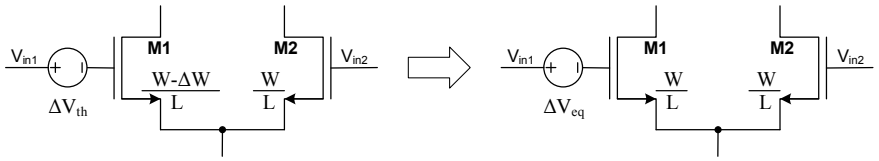

Figure 4.25 Model of device mismatch and the input referred offset in differential pair.

$\sigma(\Delta V_{th})$ and $\sigma(\Delta\beta)$ are standard deviations of ΔV_{th} and $\Delta\beta$, respectively, $A_{V_{th}}^2$ and A_β^2 are area proportionality constant which could be found from a lookup table for a given oxide spacing in TSMC 0.18μm technology report. It is found that $A_{V_{th}} = 5.13$ mV-μm, A_β=1%μm. In order to get the accurately estimation, the Hspice monte carlo simulation of the latch, as shown in Figure 4.26, included the extracted parasitic capacitors and resistors for $\sigma(\Delta I_{d1})$ and $\sigma(\Delta V_{th1})$ as shown in Figure 4.27 and Figure 4.28. An ideal voltage source on transistor gate with magnitude ΔV_{th1}=6$\sigma(\Delta V_{th1})$, which is about 74.4 mV. The current factor mismatch as error in channel width, $\frac{\Delta W}{W} = 6\frac{\sigma(\Delta\beta)}{\beta}$. The equivalent input offset dues to current factor mismatch of M_1, $\Delta V_{eq,due\ to\ \Delta\beta 1}$, is

$$\begin{aligned}\Delta V_{eq,due\ to\ \Delta\beta_1} &= \frac{1}{2}\left(\frac{\Delta W}{L_{eff}}\right)(V_{GS1} - V_{th}) \\ &= \frac{1}{2}\left(\frac{3.93\mu m}{1.37\mu m}\right)(497.67 - 4.86.18)(mV) \\ &= 16.465\ (mV)\end{aligned} \tag{4.45}$$

The total equivalent input offset dues to M_1 is

$$\Delta V_{eq,due\ to\ M_1} = \Delta V_{th1} + \Delta V_{eq,due\ to\ \Delta\beta_1} \approx 90.87\ (mV) \tag{4.46}$$

Using the same way, the mismatch parameters of transistor pair, M_3 and M_4, can be calculated as

$$\Delta V_{th3} = 19.532\ (mV) \tag{4.47}$$

$$\Delta V_{eq,due\ to\ \Delta\beta_3} = 9.283\ (mV) \tag{4.48}$$

The total equivalent input offset dues to M_3 is

$$\Delta V_{eq,due\ to\ M_3} = \Delta V_{th3} + \Delta V_{eq,due\ to\ \Delta\beta_3} \approx 28.82\ (mV) \tag{4.49}$$

For the initial state, we could just consider the mismatch of M_1, M_2, M_3 and M_4. Therefore, the total equivalent input offset is

$$\Delta V_{eq} = \Delta V_{eq,due\ to\ M_1} + \Delta V_{eq,due\ to\ M_3} \approx 119.69\ (mV) \tag{4.50}$$

The total input-referred offset voltage is ±60 mV.

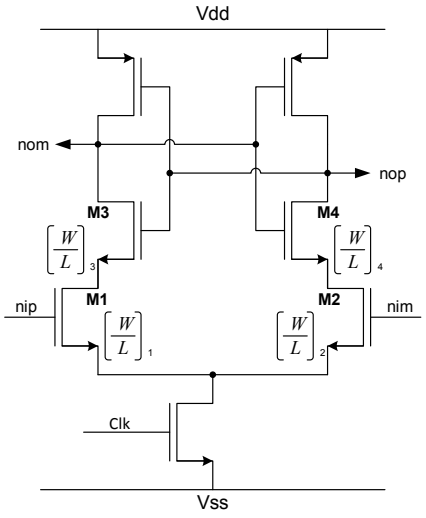

Figure 4.26 The latch module for mismatch calculation.

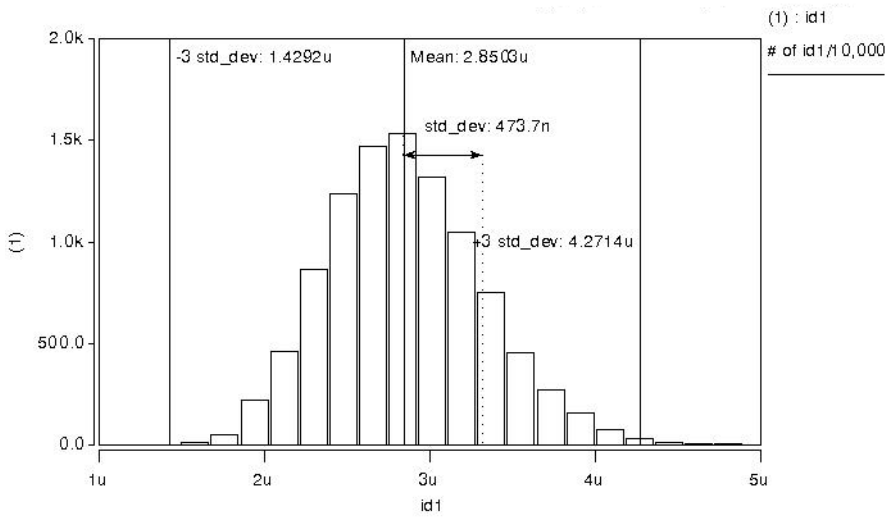

Figure 4.27 The drain current standard deviation of M_1.

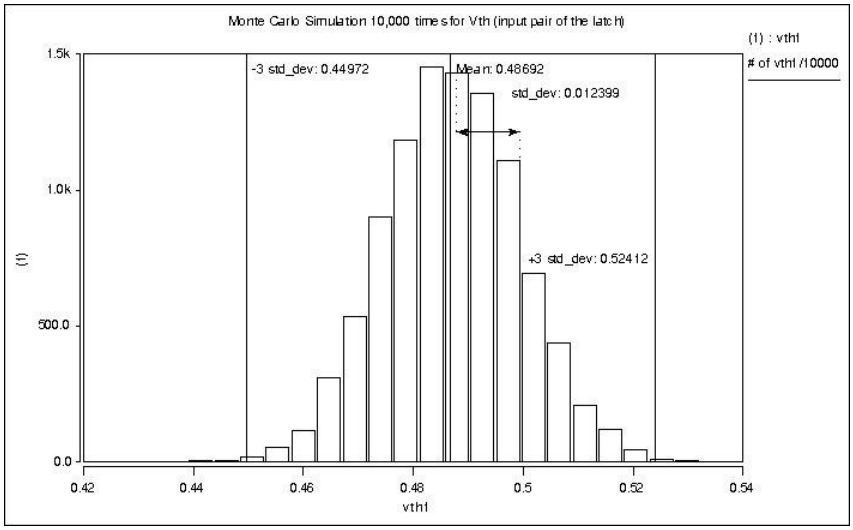

Figure 4.28 The threshold voltage standard deviation of M_1.

In order to compensate this input-referred offset, the architecture is shown in Figure 4.29, used by [25]. During the sampling period, the inputs of the latch connect to the reference voltage, "Vcm," so the input difference voltage should be caused by the referred-offset voltage. Therefore, we can use the output of the latch to decide turning on/off the

right hand side or the left hand side of the latch. A digital FSM controls this mechanism. And we don't need an extra clock cycle to compensate this offset.

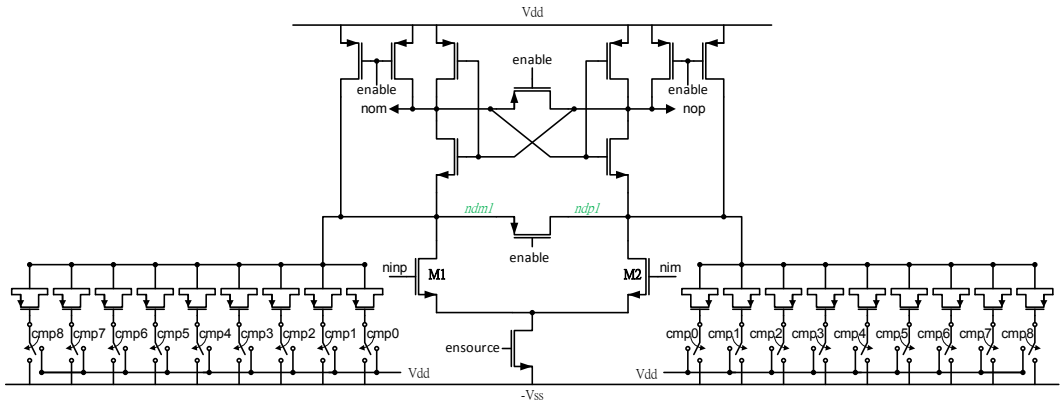

Figure 4.29 The latch with compensation capacitors.

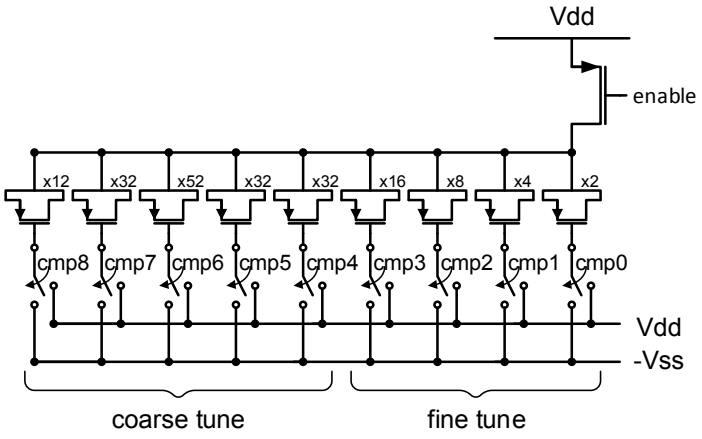

Figure 4.30 The schematic of PMOS type capacitors for input-referred offset cancellation

Figure 4.30 is the detail schematic for the compensated PMOS type capacitors, which separated into fine and coarse tune parts. For fine tuning, each step is 1 mV. For coarse tuning, each step is about 15 mV and the total steps are 4. The first two coarse tunes are linear, which is from 0 mV to 30 mV. The third and fourth coarse regions have some

nonlinear, therefore, there are extra PMOS type capacitors added during these two regions. Figure 4.31 is the simulation result when the input-referred offset is 42 mV. The first waveform is the coarse trimming switches on/off. The second one is the fine trimming switches on/off. The third one is the outputs of the latch. The last waveform is the sampling period.

Figure 4.31 A post simulation result of the input-referred offset cancellation.

Simulation Results

The performance of this 12-bit SAR ADC will be simulated in this section. For the static nonidealities, the differential nonlinearity (DNL) and the integral nonlinearity (INL) are presented. For an ideal ADC, the output code would have equal width. For example, a 3-bit ADC and the input range is 1 volt. There are 8 output codes. Each code has the same input range, which is 1/8 volt. The input range for the code number, “000,” is from 0 volt to 0.125 volt. For the code number, “001,” it is from 0.125 volt to 0.25 volt. The noise and mismatch would cause the nonlinearity problem. Therefore, the input range would not be

the same in the real world. To measure the nonlinearity, DNL and INL, the ramp signal from -0.5 volt to +0.5 volt is given as an input signal. After getting the digital 12-bit output data, the DNL and INL can be calculated by using Matlab, as shown in Figure 4.32 and Figure 4.33. The DNL is +0.576/-0.96 LSB, and the INL is +0.534/-0.655 LSB.

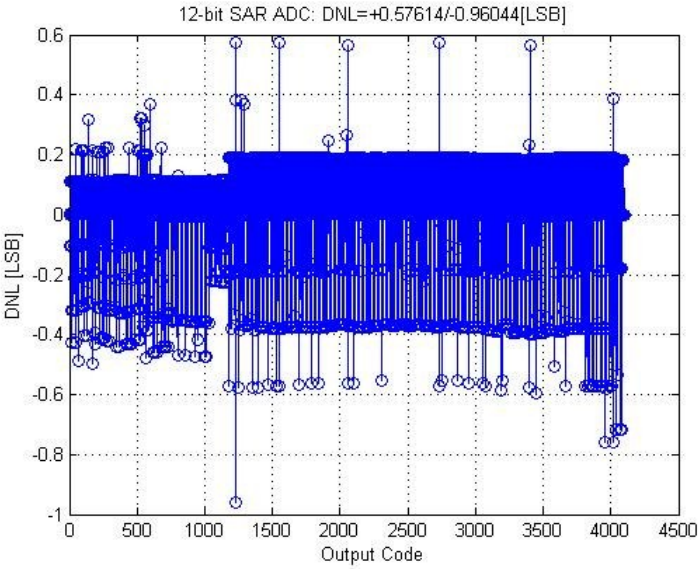

Figure 4.32 DNL simulation result

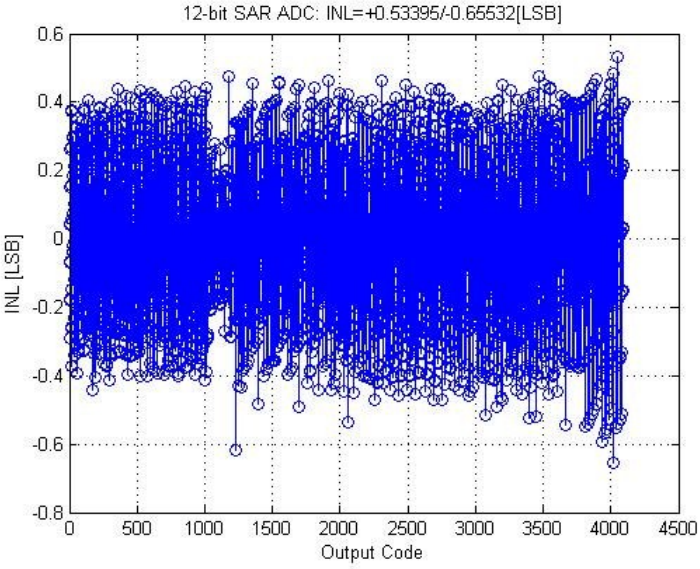

Figure 4.33 DNL simulation result.

For the dynamic performance, Figure 4.34 is the FFT spectrum simulation result by setting the input signal at 249 kHz, which is close to the Nyquist sampling frequency. The SNDR can be estimated 69dB. The effective number of bits (ENOB) is 11.17. The total power dissipation of the ADC is 60-µW at 500-KS/s sampling rate and the supply voltages are ±0.5V. The figure of merit (FOM) is 52.08-fJ/conversion step, which can be express in

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} = \tag{4.51}$$

$$FOM_3 = \frac{Power}{2 \cdot Conversion\ Bandwidth} = "Energy\ per\ Nyquist\ Sample" \tag{4.52}$$

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{4.53}$$

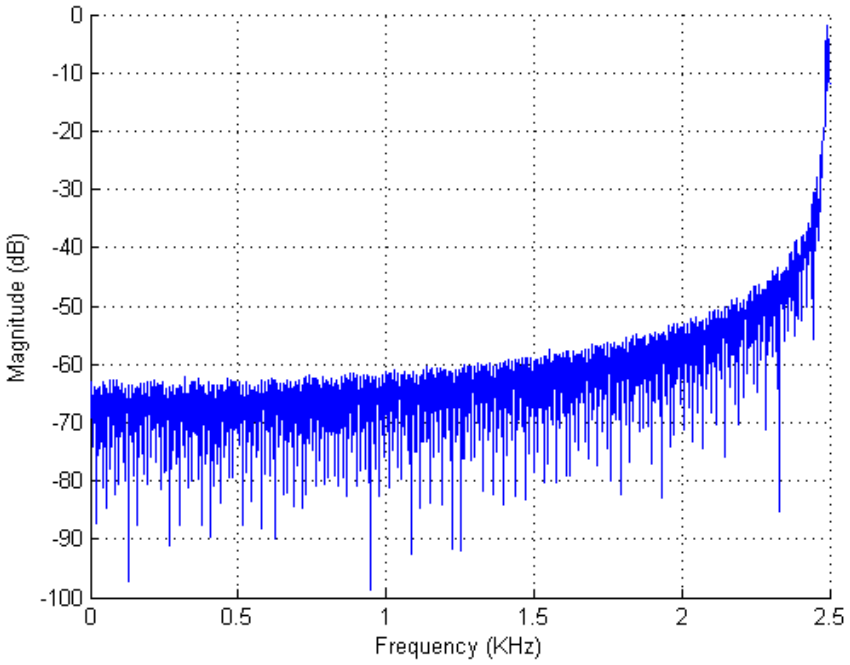

Figure 4.34 FFT spectrum with 249 kHz input signal.

CHAPTER 5

Implementation

Figure 5.1 and Figure 5.2 are the layout arrangement and the chip with I/O pads. The whole chip area is 1150μm×890μm. Table 5.1 is the pin assignment. There are two pairs analog power supplies and two pairs digital power supplies and 1 pair I/O buffers power supply. Figure 5.3 is the 48 pins footprint. The PCB layout and the testing chip are shown in Figure 5.4. The input testing signals and the output signals of the chopper amplifier are presented in Figure 5.5 and Figure 5.6. The testing results show that the chopper amplifier could functional work if the input signal is large, because the small amplitude low frequency input signals will be decoupled by the front-end capacitor. Therefore, the chopper switches should put in front of the capacitor shifting the input signals to a higher frequency.

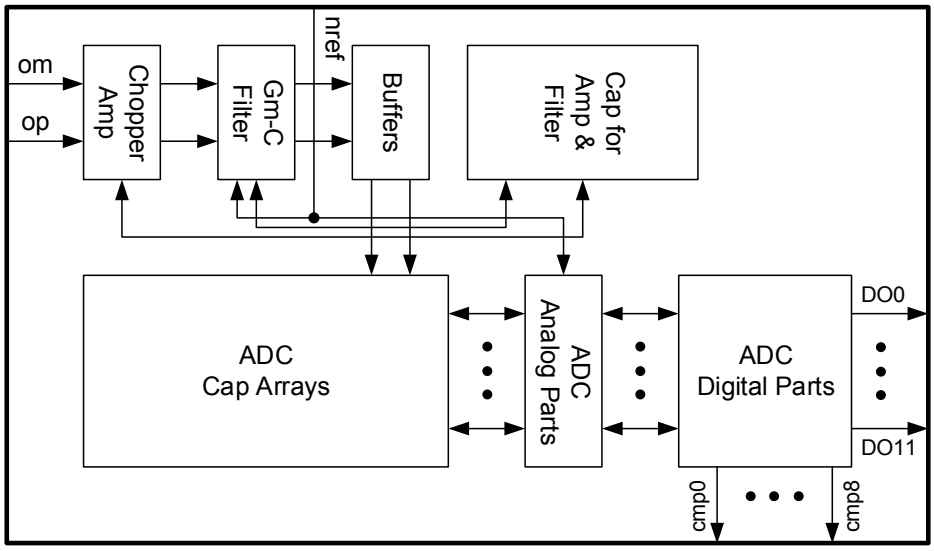

Figure 5.1 The layout arrangement.

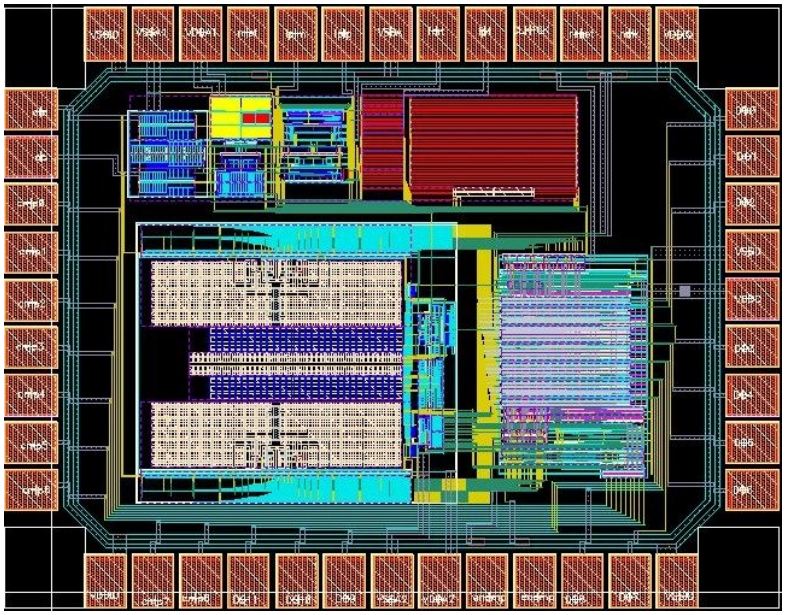

Figure 5.2 Layout

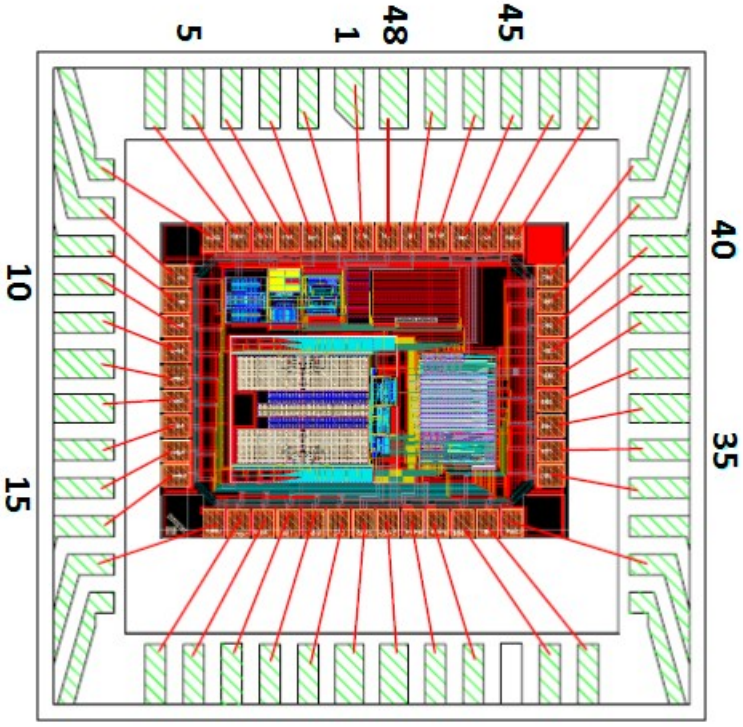

Figure 5.3 The 48 pins footprint.

Table 5.1 Pin assignment.

PIN #	Name	PIN #	Name	PIN #	Name	PIN #	Name
1	VSSA	13	cmp3	25	VDDA2	37	DO3
2	lpip	14	cmp4	26	enamp	38	VDDD
3	lpim	15	cmp5	27	encmp	39	VSSD
4	nref	16	cmp6	28		40	DO2
5	VDDA1	17	VDDIO	29	DO8	41	DO1
6	VSSA1	18		30	DO7	42	DO0
7	VSSIO	19	cmp7	31		43	VDDIO
8	om	20	cmp8	32	VSSIO	44	nclk
9	op	21	DO11	33		45	reset
10	cmp0	22	DO10	34	DO6	46	CLK16K
11	cmp1	23	DO9	35	DO5	47	ipt
12	cmp2	24	VSSA2	36	DO4	48	imt

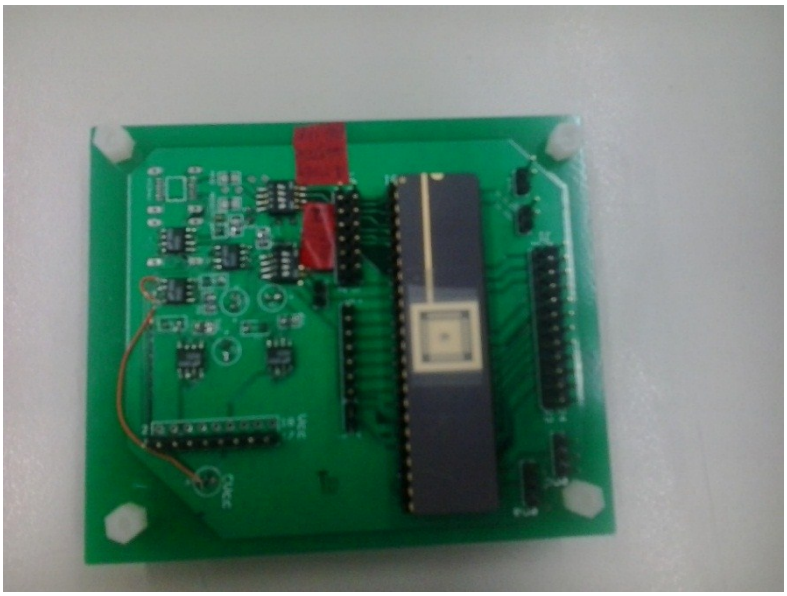

Figure 5.4 The PCB and testing chip.

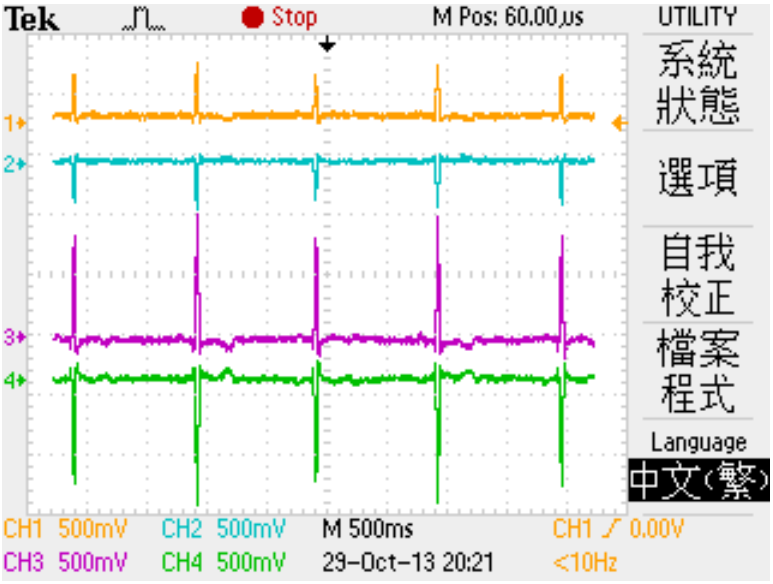

Figure 5.5 The input testing signals

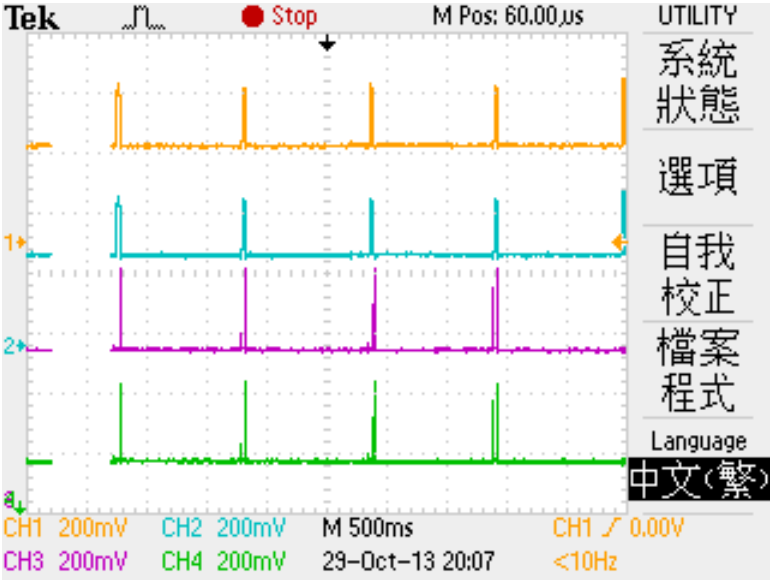

Figure 5.6 The output signals of the chopper amplifier.

Conclusions

In this research, a 1-V low power biosensor have been proposed for a front-end chopper stabilized amplifier with DEO suppressed feedback, the 2nd order anti-aliasing

low-pass filter, and a 12-bit SAR ADC with digital calibration. The flicker noise and the DEO could be eliminated by the chopper stabilized amplifier. The harmonic signals and noise could be removed by the anti-aliasing filter. Combining the energy-efficient and splitting methods, the switching energy could be reduced 90% comparing with the conventional method.

Future Work

There are two different applications based on this bio-sensor in the future circuit design. One is to improve the power consumption and accuracy for the future portable blood glucose monitor systems. The frequency is below 10 Hz and it needs a 10 to 12-bit SAR ADC. The other is for tumor cell detection using an electrochemical impedance technique. The noisy environment, and high accuracy are the challenges in this medical field. It needs a 7 to 8-bit ADC.

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