# A STATISTICAL APPROACH TO ERROR PREDICTION IN APPROXIMATE SEQUENTIAL CIRCUITS

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## Dedication

This thesis is dedicated to my parents Shivshankar Kapare and Sandhya Kapare.

**Abstract**

Low power and high performance requirements have increased focus on Approximate Computing which uses designs that approximate the functionality of a precise design while still achieving acceptable quality of results and consuming lower energy than the precise designs. To perform design automation for approximate designs, modern CAD tools should have the ability to quickly estimate the output quality of designs that include approximate design modules. Previous research on output quality estimation for approximate designs has focused on using an interval based approach [2][11] which introduces quantization error, or lookup table-based techniques [7], which mainly emphasize on output quality estimation for approximate combinational circuits and have large overheads for storing the lookup tables for different error metrics. Other works like [3] use an unrolling based approach to estimate the output quality which requires large characterization time.

In this work, I propose a methodology to estimate the output quality of approximate sequential circuits based on deriving analytical expressions for predicting approximation errors from statistical data gathered from performing limited characterization of the approximate circuits. I show that limited characterization is sufficient to accurately characterize approximation errors since in many cases, the error behavior of approximate circuits follows a pattern. As such, I show that we can achieve high accuracy of prediction for average approximation error, even with this limited characterization. I also demonstrate that the methodology is more scalable than [7] and reduces characterization time by 90% on average compared to [3].

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# 1. Introduction

Meeting performance and power constraints required by computational systems in modern VLSI designs has become an important concern. Typically, designers expect a circuit to produce correct results and thus the design is always produced to provide a perfect result even in worst case scenario. There are, however, some applications that do not require perfect computations to produce acceptable results. Processes such as video/audio encoding, approximations, etc. do not require exact computational results and can produce acceptable results even with an imprecise computations [14]. Thus, it is possible to exploit this error resilience of the applications to simplify the design approach or change the algorithm for the computation with aggressive optimizations [4]. These type of design changes may lead to less computation time, circuit optimizations, and power savings.

Approximate computing has been seen as potential way to improve energy efficiency for error resilient applications. Approximate computational circuits have proven to be energy efficient at the cost of obtaining functionally accurate result. The pace of progress in developing new energy-efficient applications is not matched by the CAD tools as they are unable to perform design automation in approximate sequential circuits. One major roadblock for CAD tools dealing with approximate computational circuits is inability to estimate output quality of designs quickly and efficiently. If this functionality is enabled, it will help CAD tools in reducing the energy of designs while maintaining an acceptable output quality which will be specified by designers during various operations. In this thesis work, I propose a new approach to analyze the error

origination and propagation in case of approximate sequential circuits and use that to derive a new technique that can quickly and accurately estimate output quality of approximate designs based on deriving analytical expressions for the approximation errors in approximate circuits.

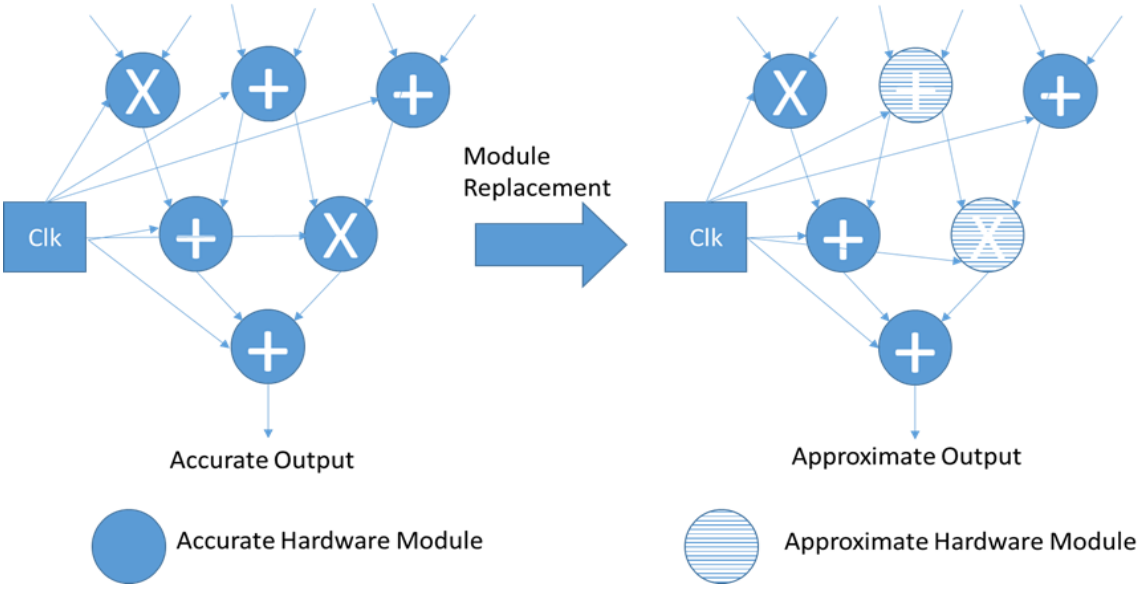


Figure 1. Illustration of formation of approximate circuit, by replacing accurate modules with approximate modules

Following terminologies are useful in the approach used for approximate circuits in this work:

- Approximate hardware module: A hardware module which is functionally incorrect by design (e.g., approximate adders, multipliers, MAC circuits, etc.).

- Approximate Circuit: A circuit containing one or more approximate hardware modules.

- Accurate Circuit: A circuit containing all functionally correct hardware module by design.

- Approximation error (AE): A unit of measure that quantifies the difference between output of accurate circuit and approximate circuit.

- Predicted average approximation error (PAAE): A unit of measure to estimate the value of average approximation error arising due to the approximations performed in the circuit.

- Accuracy of prediction: A unit of measure which quantifies difference between predicted average approximation error and average observed approximation error, relative to average observed approximation error.

Accuracy of Prediction = |predicted average approximation error – average (observed approximation error)| / average (observed approximation error)

In this research work, I propose an automated methodology to estimate PAAE at any nodes of an approximate computational circuits. The approach is derived from the error characterization of various sequential circuits which is obtained by simulating the

circuit for a few cycles and observing the pattern in which the error shifts from ith cycle to i+1th cycle of the circuit. I also demonstrate how errors propagate through topology of approximate circuits. I validate my methodology using several benchmark circuits with varying complexity as well as designs evaluated in previous works (e.g. MAC circuits, FIR filter, etc.)

Contributions made by me to the research are:

- I analyze the previous techniques to determine the output quality of components in [2] [3] [4] [7] [11] to identify their potential limitations.
- I propose a methodology for estimating the output quality of an approximate sequential circuit based on deriving an analytical expression for the approximation errors produced by the circuit in a given cycle.
- My approach provides only 0.4% estimation inaccuracy and 90% reduced characterization time, on average compared to previous approaches [7] [3].

The remainder of this work is organized as follows. Section II studies the previous works which present different techniques to estimate accuracy in an approximate circuits. Section III discusses various issues faced in previous methodologies, design approach adopted in this work and the rules plus the steps that contribute to estimating output quality. Section IV describes how I applied this methodology to pre-characterize individual components and use them to obtain the estimates for output quality for different approximate circuits and also presents the results obtained from the experiments

and compares them with the previous work done. Section V summarizes the results obtained, discusses the advantages of using this methodology and concludes the work.

## 2. Related Works

Approximate computing employs deterministic designs to produce imprecise results. It uses statistical properties of data and algorithms, applying architecture level and circuit level techniques to trade quality of the output to achieve energy reduction. Earlier research in approximate computing focused on designing simple arithmetic units manually as in [2], [11]-[13]. The efforts largely focus on reducing the severity of errors to achieve a configurable error rate which is achieved by breaking critical paths in approximate modules. To use these individual components in complex approximate circuits, many existing CAD tools have the capability to determine the energy consumption of an approximate circuit but the ability to determine the output quality of these component i.e. how much the approximate output will differ from the accurate circuit output is needed.

With this need in mind, recent efforts have proposed improving the design of adders and multipliers and also using statistical approximation for errors by using single interval as variable and then estimating PMF for errors produced using modified interval arithmetic to determine best design for given constraints [2]. Unlike other VOS techniques in [4] [5], this technique does not rely on Monte Carlo simulations for which the simulation time grow exponentially with data width and computation length. However, the accuracy of this interval based approach is affected if the range of characterization does not match the range of inputs or if the actual error distribution has high variability within a single interval.

In [7], the limitations of [2] are addressed by estimating output quality of an approximate hardware circuit by pre-characterizing the relationship between Error metric behavior and characteristics of approximate hardware circuits. These values are stored in lookup tables which are used to retrieve Error metric composition for a given approximate hardware module and then compose error metrics for output quality using regression based models. This approach also takes into consideration the input distributions of the approximate circuit. However, there are certain disadvantages of using this technique. First, this technique is limited to only adders and circuits constructed using blocks of adders. It is not scalable to multipliers or sequential circuits as the regression based model is not applicable for these circuits as this approach requires error metrics to be additive in some way to use regression-based approach. Secondly, the characterization time increases as the number of nodes increase in the circuit as larger number of simulations are required. In addition, the memory overhead required is large as we need to store multiple lookup tables for this approach. Hence, this technique is not particularly useful for complex circuits or for circuits having high number of nodes.

Another recent technique to estimate the output quality of an approximate circuit is used in [3] which uses the concept of unrolling the circuit each clock cycle and compares this unrolled approximate circuit with the original circuit using a quality evaluation circuit and generates some vectors which indicate the quality of the circuit at that cycle. Unless the quality constraints are satisfied the approximate circuit is unrolled

every cycle with incremental improvements in each cycle. Thus, if the desired output quality is high, the cost of unrolling and analyzing error metric also increases substantially.

Compared to previous work, my work mainly focuses on formulating analytical expressions for describing the error propagation the approximate circuits, deriving output quality expressions and marginalizing the memory overheads required by previous approaches.

## 3. Problem Formulation and Analytical approach on Error Estimation

### A. Analysis of Existing Regression- based approach

Chan et al. have focused on determining the output quality (output error metric) of an approximate circuit by taking into account the hardware characteristics, input distributions, and characteristic error metric behavior in [7]. The work is based on characterizing the output error metric for an individual approximate arithmetic unit and propagating the error metrics from approximate arithmetic units connected together in a network to obtain the output error metric for the network. Since the error metric for an individual approximate arithmetic unit depends on its input distribution and hardware characteristics, characterization is performed for each combination of input distribution and hardware configuration and stored in a lookup table. The lookup table is indexed by the standard deviation of each input assuming a normally-distributed input distribution and the hardware configuration of the approximate arithmetic circuit to look up the pre-characterized error metric.

The work uses a three-step process to calculate the output error metric for a particular network of approximate arithmetic units. The first step is to navigate through the nodes in the network and generate the standard deviation of the input distribution at each input in the network. This step is done using another lookup table that describes the output standard deviation in terms of the input standard deviation of an approximate arithmetic unit. The next step is to traverse the network again to look up the output error metric for each node in the network using the pre-characterized lookup tables and the standard deviation values from the previous step. The final step is to calculate the output

error metric of the entire network using regression. The regression equation is composed by either taking the product of pass rates (1 - error rate) and regression coefficients of approximate arithmetic units (for rate-based error metrics) or summing the error magnitudes multiplied by regression coefficients (for amplitude-based metrics). The output error metric for the network is then calculated by solving the regression using Matlab.

I observe several drawbacks in this regression based approach. It requires pre-characterization of every error metric type for each approximate arithmetic unit under all possible combinations of input distributions and hardware configurations. Pre-characterization of output distribution standard deviation in terms of input distribution standard deviation is also required. The approach also requires two topological passes through the circuit, one to propagate the standard deviations and one to determine the intrinsic error metrics at each node. Following these traversals, formulation and solving of the regression equation are required. For ex, the runtime for building pre-characterized lookup tables for a 4-tap FIR filter, it takes about 1.37 hours.

In addition to its longer characterization time, the regression-based approach requires a large memory overhead, since it must store two lookup tables for each possible combination of input distributions and hardware configurations for every possible approximate arithmetic unit.

The regression-based approach is also more limited in its applicability. First of all, the approach is only applicable for combinational logic, since it does not specify how to

propagate error metric values across multiple cycles in a circuit. Secondly, the regression-based approach only works for networks containing approximate adders. This limitation is due to the fact that the regression formulation only works when the error metrics can be summed together in some fashion. This is only the case when the underlying approximate arithmetic units are adders. It is not clear how to formulate the regression equation for other approximate computation circuits (i.e., circuits where error metrics do not simply add together).

In addition, due to small range magnitude of inputs, the prediction error is high if number of nodes in the circuit are small. This is not a problem with my approach as I can predict the output error quality with the same accuracy for circuits having multiple number of nodes as I use an analytically derived formula.

## B. Composition of analytical expressions for approximate circuits

For deriving the analytical expression for predicting the average approximation error, I adopt following methodology:

### Step 1: Gather statistical data for analysis

To characterize the approximation error in an approximate circuit, I first simulate the accurate circuit and approximate version of circuit for limited number of characterization cycles and take multiple samples. In these simulations, I record the approximation error which is the difference between the output of approximate circuit and the output of the accurate circuit for the given input distribution. This step is used to

gather the data to determine the relationship between approximation error and circuit characteristics.

**Step 2: Curve Fitting of the Statistical Data**

From the data obtained in Step 1, I observe how the average approximation error in the circuit changes with increasing number of cycles. I use this statistical data to define an equation to describe the relationship between the average approximation error and the cycle number using a curve fitting approach. To achieve this, I try to find a fitting function for the data obtained in the previous step. An appropriate fitting function is selected that minimizes least mean squared error between predicted and simulated approximation error values for the statistical data obtained in Step 1. The analytical expression obtained in this step is then used to predict the value of average approximation error for the circuit.

To verify the correctness of this analytical expression-based methodology, I simulate different approximate circuits and the corresponding accurate circuits for about 2000 cycles to determine the average approximation error for the circuit over these cycles. The simulation length of 2000 cycles was chosen empirically, based on the number of cycles that guarantees accurate statistical characterization of circuit behavior. I then predict the average approximation error using the analytical expression derived from the methodology used in steps 1 and 2. I compare the actual value of average error against the value obtained from the analytical expression for these cycles and determine the prediction accuracy for the circuit.

To understand why the methodology works for approximate circuits, I analyze an adder circuit. For an N-bit adder with lower k-bits approximated by setting all of them to 1, I observe that if I increase k, the average approximation error increases. For any value of k<n, the approximation error ranges from 0 to $2^k$-1. I simulated the approximate and accurate version of the adder circuit for 4 cycles and the histogram for the errors pattern is given in Figure 2**.** From the simulation results**,** the average error for a uniform distribution of inputs in the adder is given by equation (1).

$$Average\ Approximation\ Error_{\text{adder}} = \frac{(2^k - 1)}{2} \qquad (1)$$

The equation is derived from the histograms of error produced for different input combinations in the adder circuit from Figure 2.

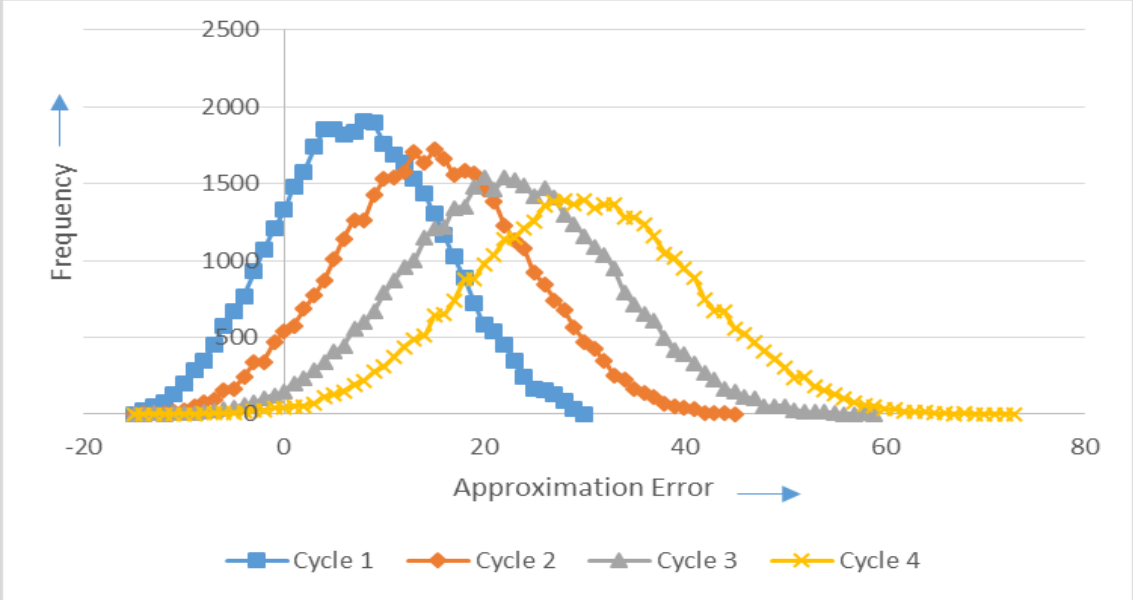


Figure 2. Histograms for Approximation Error values vs. cycle number in an adder circuit.

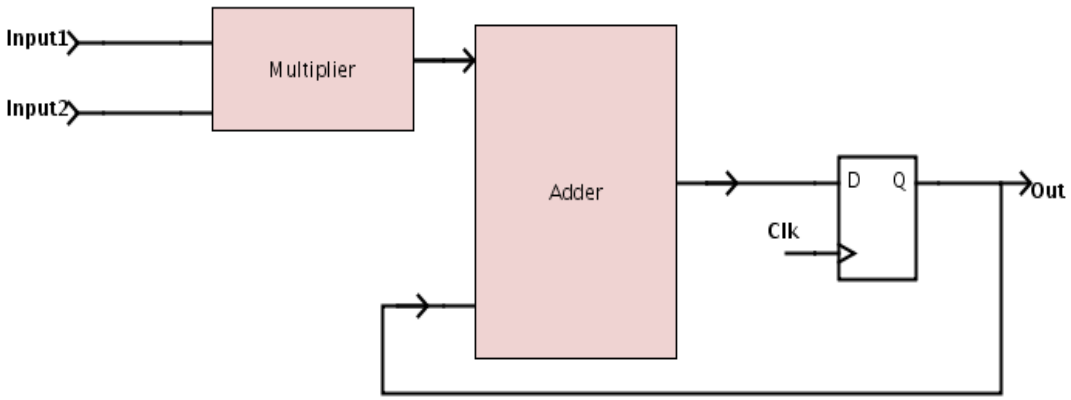


Figure 3. Multiply Accumulate circuit

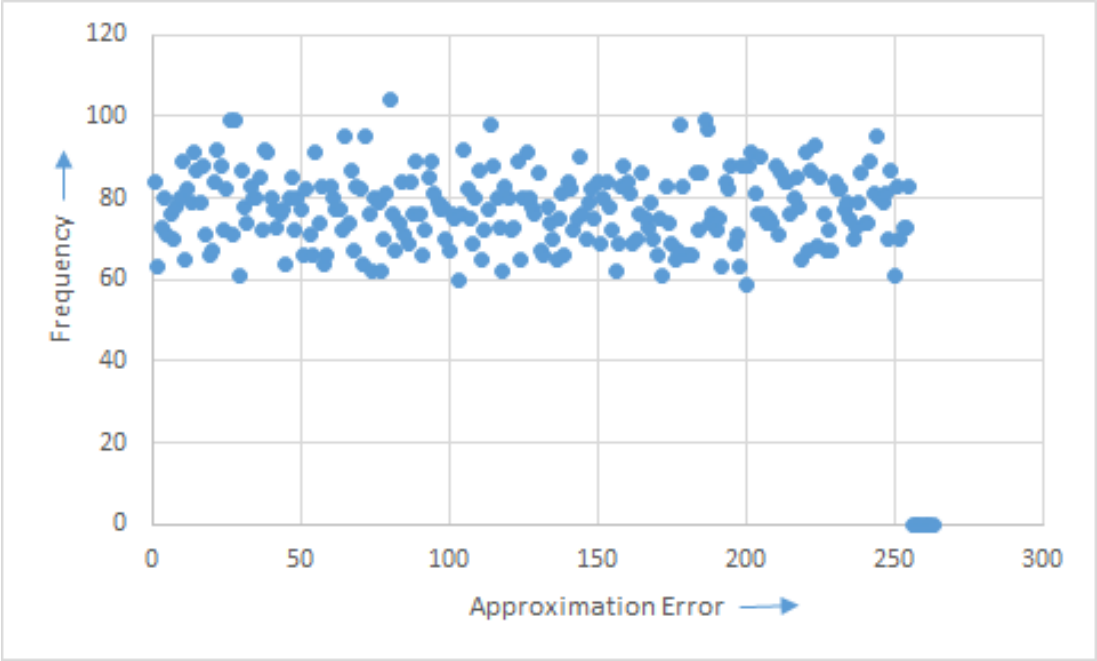


Figure 4. Histogram for Approximation Error values in a multiplier circuit. Please note there is a point at value 0 whose frequency = 20232.

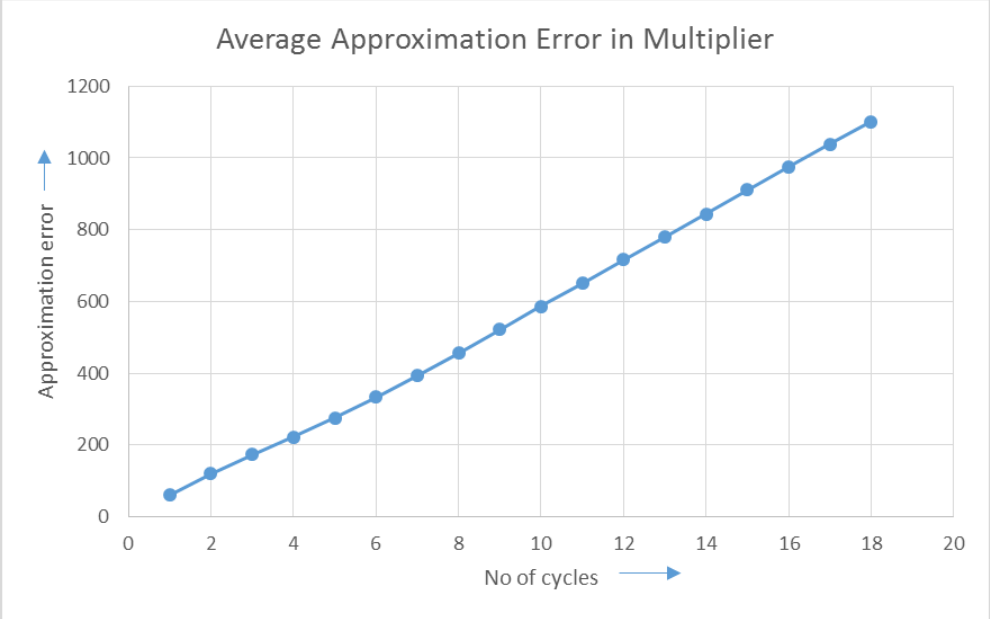


Figure 5. Approximation errors against cycle number for a 8x8 Multiplier circuit

To further understand why the methodology works, I study an approximate multiplier circuit for n-bit multiplication which is approximated by not performing shift-and-add operation on the LSB of the multiplier. Due to the way the approximation is performed, when the multiplier factor is an even number, the approximation error will be zero as the circuit will produce the same result as an accurate circuit. When the multiplier coefficient is an odd number, the approximation error will be equal to the value of the multiplicand. Therefore, for a uniform random distribution, half of the samples will have approximation error equal to 0 and half of the samples will have approximation error of the value of the multiplicands, thus the average value for these samples will be half the range of the multiplicand input as demonstrated in Figure 4. Thus, the average approximation error in a multiplier can be predicted using equation (2):

$$Average\ Approximation\ Error_{multiplier} = \frac{(2^n - 1)}{4} \qquad (2)$$

I validate this equation by simulating this approximate multiplier and observing the error pattern generated (Figure 5).

Now, when I observe the error pattern for a Multiply Accumulate circuit (Figure 3), I find that the average approximation error (AE) at the output node increases linearly as number of cycles increase. Thus, I discover that circuits using combination of approximate modules generate a predictable approximation error pattern. This gives me the basis to find an analytical expression to predict the approximation error after a given number of cycles in an approximate circuit.

## 4. Experiments and Results

This section presents the results of various experiments I performed to evaluate my methodology for a collection of sequential benchmark circuits listed in Table 1. First, I determine how many characterization cycles and samples are needed to accurately characterize the statistical behavior of sequential circuits. This is an important step since the data gathered in this step are used to generate the analytical expression for the average approximation error of the circuit. Choosing too few characterization cycles and samples might produce an incorrect analytical expression for predicting the average approximation error and lead to a low prediction accuracy. On the other hand, choosing too many characterization cycles and samples will lead to higher characterization time. I present the findings and accuracy results obtained using my methodology for various sequential circuits. Finally, I show how the characterization time is reduced using my methodology compared against the approach used in [3].

| Name | Function |
|---|---|
| Adder | 16-bit adder |
| Multiplier | 8x8 bit multiplier |
| MAC | 16-bit multiply accumulator Circuit |
| L1 Norm | Sum of absolute difference |
| L2 norm | Euclidean distance |
| FIR Filter | 4-tap FIR filter |
| DCT | 8 input discrete cosine transform |

Table 1. Benchmark circuits used for evaluation.

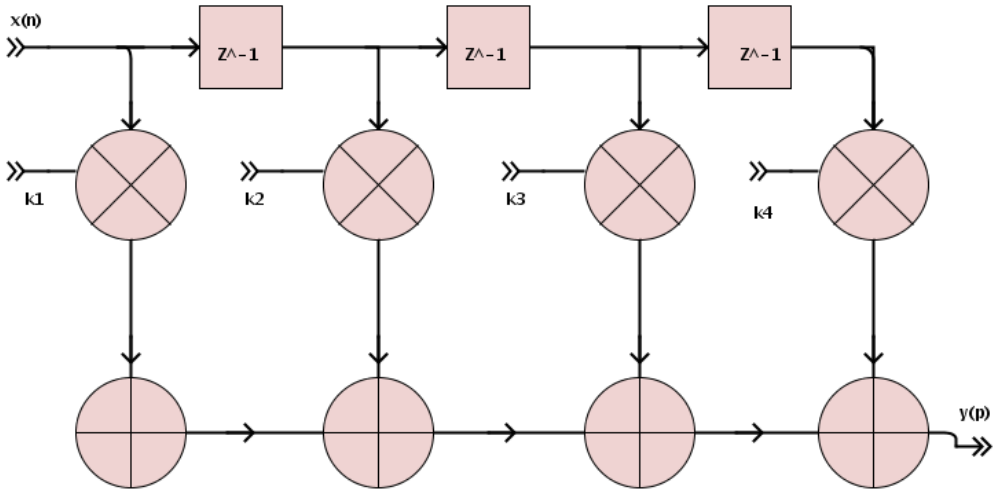


Figure 6. Circuit for 4-tap FIR Filter example.

**A. Comparison of accuracy and characterization parameters for approximate circuits**

Figure 7 and Figure 8 show the accuracy of prediction from the analytical expressions obtained from the statistical data gathered for varying number of characterization cycles. This plot is used to determine the exact number of characterization cycles required to generate a precise analytical expression for given sequential circuits. The inaccuracy measured on the Y-axis is the absolute value of inaccuracy in prediction of the average approximation error in various approximate sequential circuits. These values are obtained by simulating both approximate and accurate version of the circuits for limited number of characterization cycles plotted on X-axis and taking limited number of samples. I then derive an analytical expression for the average approximation error to fit the data gathered from this simulation.

The analytical expression is then used to estimate the accuracy of prediction for the approximate circuit for several cycles. It can be observed that the inaccuracy of prediction initially decreases with increase in number of characterization cycles and becomes stable after a few cycles. It should be noted that characterization cycles required to accurately characterize a circuit depends on the function the circuit represents i.e., the pattern of error behavior vs cycle number for a given approximate sequential circuit can be characterized accurately by a different number of cycles. For example a linear pattern can be characterized by sampling the behavior over only two cycles.

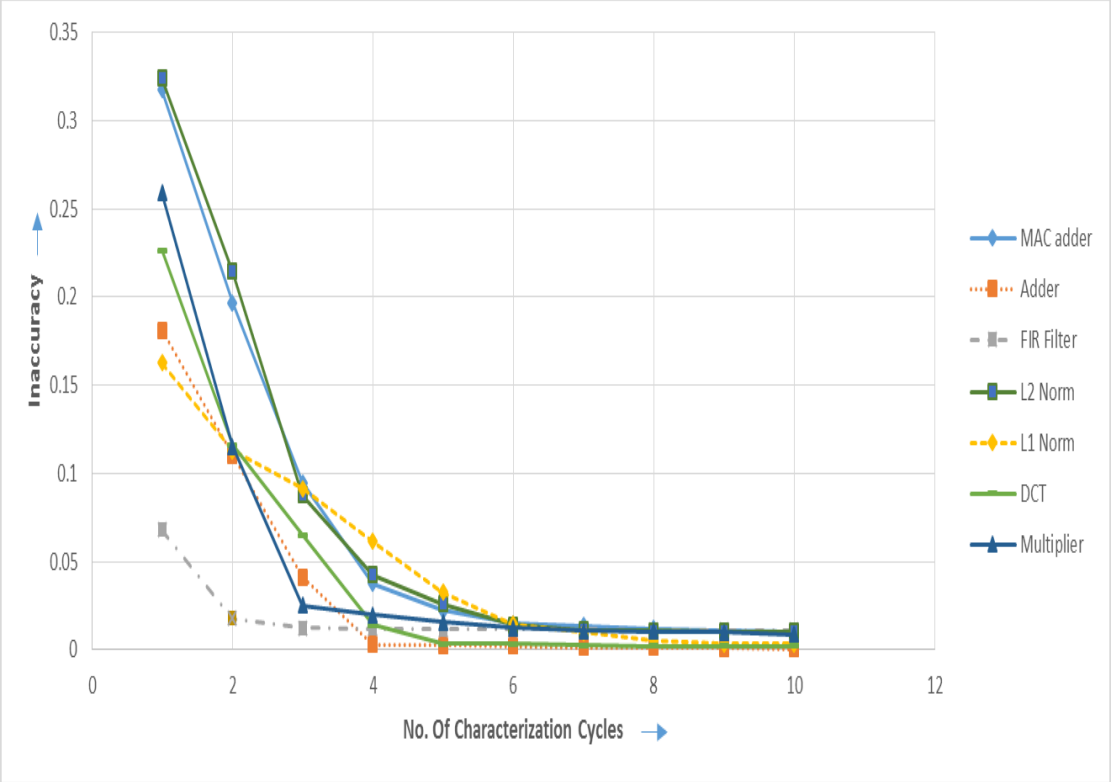


Figure 7. Inaccuracy in the Output error prediction in an approximate circuit for various number of characterization cycles.

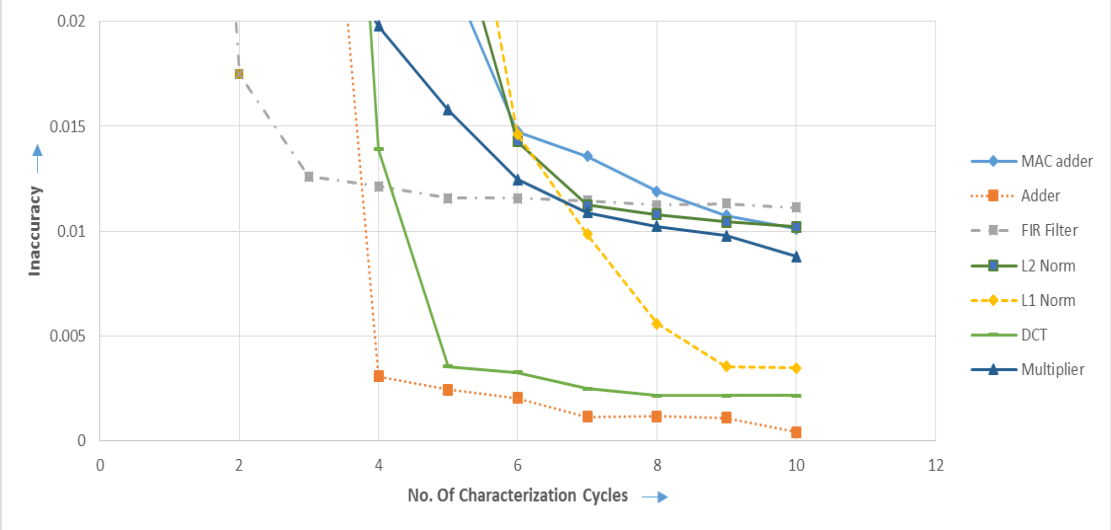


Figure 8. Inaccuracy in the Output error prediction against no. of characterization cycles (closer look).

Similar to determining the number of characterization cycles required to obtain a precise analytical expression, I also determine the number of samples required to determine an accurate analytical expression for various sequential circuits. Figure 9 shows the plot for inaccuracy in prediction against the number of samples taken to determine the analytical expression which can predict the approximation error in the sequential circuit. Figure 9 captures the inaccuracy of prediction for given number of samples. The high inaccuracy for smaller values of samples can be accounted for as insufficient statistical data to make an accurate prediction for average approximation error. It can be seen that for any circuit, a certain minimum number of samples must be obtained to make an accurate prediction for the approximation error.

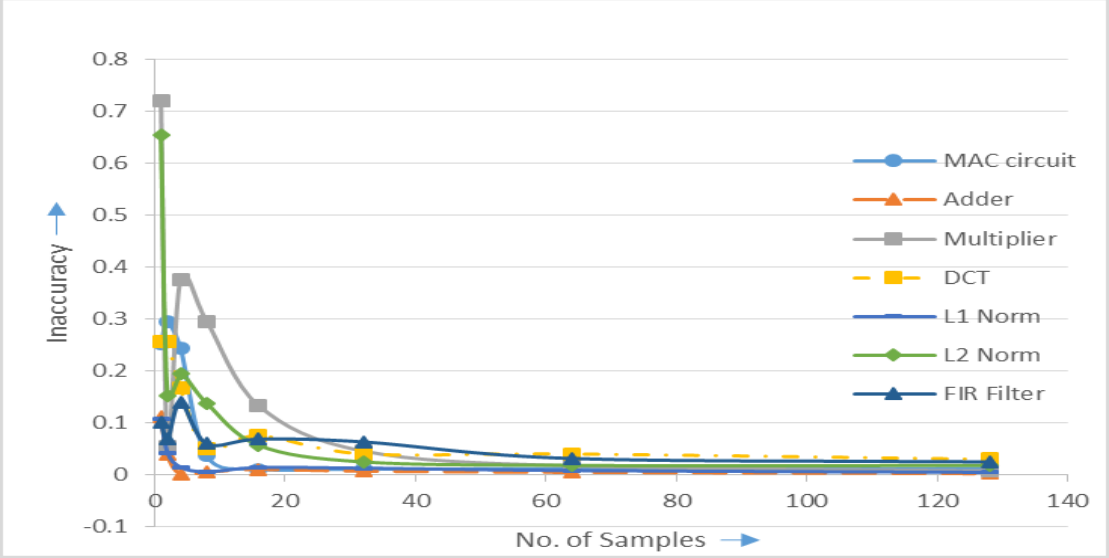


Figure 9. Inaccuracy in the output error prediction in an approximate circuit against number of samples taken to obtain the analytical expression for prediction.

**B. Results for output error prediction accuracy**

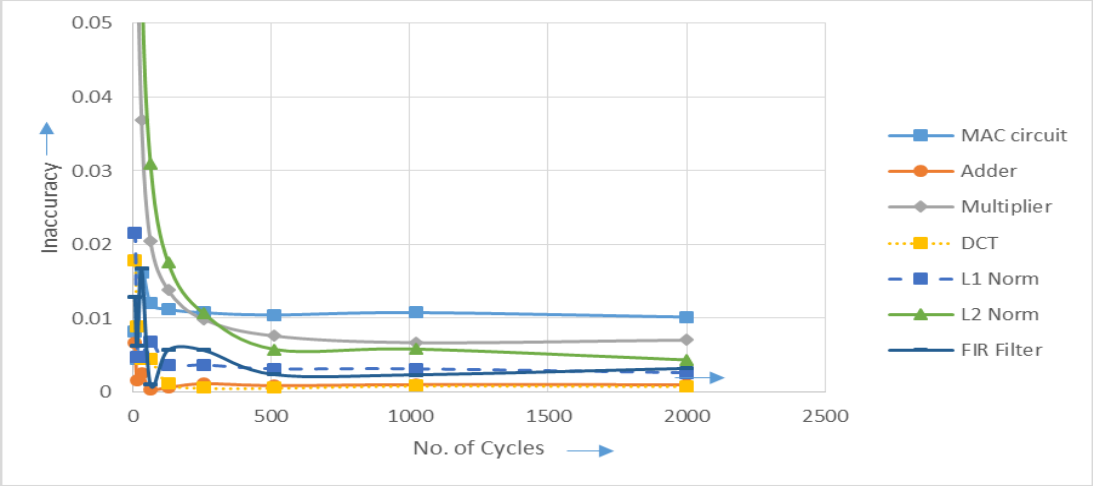


Figure 10. Inaccuracy of prediction for approximate sequential circuits.

Figure 10 shows the results for the inaccuracy of prediction of the approximation error for various approximate sequential circuits. I simulate the accurate sequential circuits and the approximate sequential circuits for several cycles and evaluate the average approximation error for the given circuits. I then predict this average approximation error value using the analytical expression determined by characterizing the circuits for limited number of cycles and limited sample data. Figure 10 presents the resultant inaccuracy of prediction for the average approximation error obtained from applying the methodology to various sequential circuits. The inaccuracy in prediction is high for initial cycles but decreases rapidly and stabilizes after a few cycles. From the plot in the Figure 10**,** it is evident that the methodology is able to predict the output approximation error in the sequential circuits accurately. Even while predicting the average approximation error after several thousand cycles, the quality of prediction does not degrade. This shows that in order to characterize a sequential circuit, only limited characterization data are required to produce accurate results. This is possible because the average approximation errors produced by many sequential circuits follow a pattern. Thus, by learning the relationship between the average approximation error and the number of clock cycles, approximation errors can be predicted for an arbitrary cycle number. The accuracy of prediction depends on the analytical expression used and in turn on number of characterization cycles and the number of samples taken to generate the analytical expression.

This methodology is applicable to any sequential circuit whose approximation error can be defined to fit a particular pattern based on the behavior of the circuit. For

example, for an adder circuit used in this work, the approximation error increases linearly with the number of cycles. For this methodology to work, we should be able to establish some kind of relationship like linear, constant, exponential, etc. between the approximation error in the given circuit and the number of cycles. So far, I have observed that arithmetic computation circuits and circuits used in digital signal processing applications exhibit this patterned error behavior.

During my experiments, I found that the methodology was not able to predict the average approximation errors for IIR filter, FFT circuit, or Sobel operator circuits. For IIR filter and FFT circuits, I found the variation in the average approximation to be very high with respect to cycle number and the analytical equation obtained was not able to describe output errors with high accuracy. The Sobel operator circuit did show a predictable pattern in output errors. However, the pattern was periodic in nature, and the curve fitting approach used in this methodology was unable to account for this periodicity. Future work will improve on the curve fitting approach to recognize and characterize periodic output error patterns.

In this work, I have focused on predicting the average approximation error but this methodology can be extended to predicting other parameters like Error Rate, Error Significance, Average Relative Error Significance, Mean Squared Error, Maximum Error, and Minimum Error of the sequential circuits [7]. This can be done by taking appropriate number of characterization cycles and number of samples and determining the pattern followed by the particular metric of interest. From the given results, we can

form an analytical expression to characterize the relationship of the parameter to be predicted with the number of cycles. This analytical expression can then be used to predict the value of parameter after any given number of cycles.

### C. Comparing the characterization time

Figure 11 compares characterization time for the circuits in the test set for the methodology used in [3] and my methodology. In [3], the authors characterize a circuit for *n* cycles by unrolling the accurate and approximate versions of the circuit *n* times and add circuitry to compare the quality of output at the end of each unrolled cycle. Thus, the characterization time increases as the number of cycles (*n*) increases. Characterization time also increases with the complexity of the circuit.

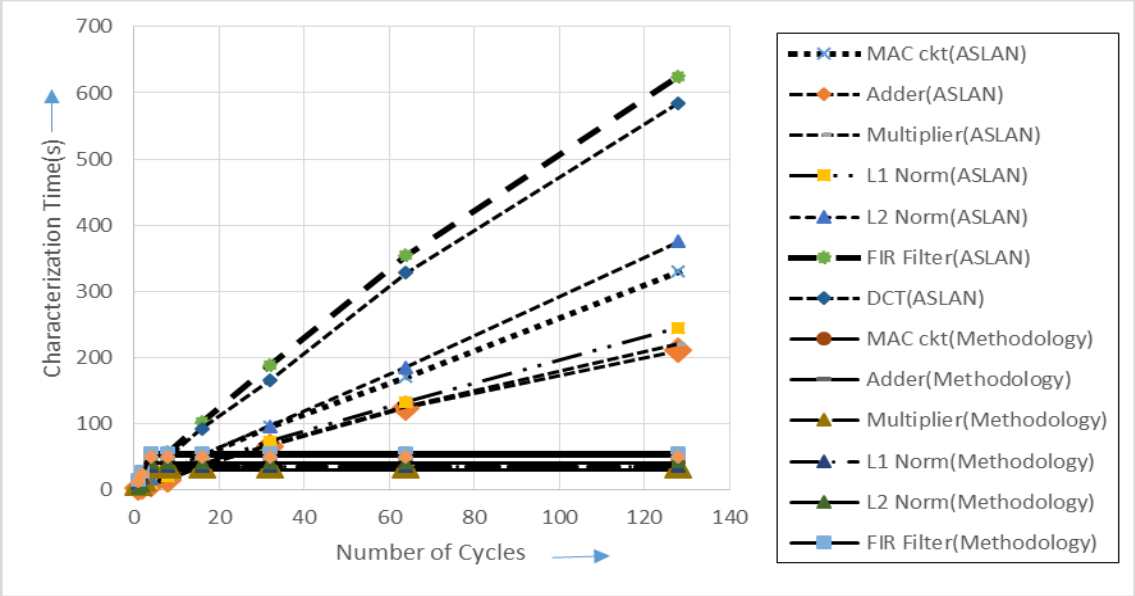


Figure 11. Comparison of characterization time for ASLAN vs my methodology.

On the contrary, my methodology uses a certain fixed number of cycles to characterize a particular circuit. As I formulate an analytical expression to predict the error at the end of any cycle in the circuit using limited characterization data, I save the cost of unrolling for $n$ cycles and also save on the overhead of quality comparison circuits. Thus, even for characterizing a circuit for a large value of $n$, my methodology requires only a few cycles of characterization. To characterize the errors in a circuit for 100 cycles, my methodology reduces characterization time by 90% compared to the methodology in [3]. Reduction in characterization time for my approach increases with increasing cycle number and complexity of the characterized circuit. These results demonstrate that the methodology in [3] over-characterizes the circuit and only limited data is needed to characterize a circuit correctly and achieve accurate results.

## 5. Conclusions

In this work, I have proposed a methodology to predict the average approximation error in approximate sequential circuits. I prove that we can establish a pattern between the average approximation error in the circuit and the cycle number. By establishing a methodology to derive analytical expressions from statistical analysis of data obtained from characterizing the approximate sequential circuits for a limited number of cycles and taking limited samples, I am able to make a prediction for the average approximation error in a circuit after an arbitrary number of cycles. I demonstrate that the methodology is applicable for a number of approximate sequential circuits and show that it produces accurate approximation error predictions. I have also addressed the limitations of this methodology by analyzing the circuits for which it was not able to produce accurate results. On average, inaccuracy is only 0.4% over the set of studied circuits. With my methodology, I show that only limited characterization of sequential circuits is needed to accurately predict their error behavior, avoiding over-characterization. I also eliminate the need for using look-up tables to produce accurate predictions for approximation error. I achieve 90% improvements for runtime characterization compared to [3] for characterizing 100 cycles. I also substantiate that the quality of prediction does not degrade with increasing number of cycles.

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