DESIGN OF RAIL-TO-RAIL OPERATIONAL AMPLIFIER USING XFAB 0.35µM PROCESS

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Abstract

Operational amplifier is an integral part of analog circuits. With the advent of portable device technology, power consumption has become an area of concern.

To reduce power consumption and improve battery life performance, supply voltages are scaled. This leads to a reduced input common mode range for an operational amplifier. A rail-to-rail amplifier composed of complementary CMOS differential pairs is employed to obtain a wider input common mode range.

However, the complementary differential pairs, when operated in parallel lead to a large variation in the total transconductance thereby making the circuit highly unstable. A simple and novel technique to remedy this is to use a diode connected NMOS to shift the transition region of the NMOS differential pair. This circuit is simple and consumes less power.

XFAB 0.35µm process technology is used in the design of the circuit. Cadence SPECTRE simulator is used for all the simulations.

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Chapter 1: Introduction

In recent years, much of research has been going on in the design of portable devices be it PDAs, handheld computers or biomedical instruments. A concern in the design of portable devices is battery life. For better battery life management by reducing power consumption, supply voltages are scaled. However with the scaling of supply voltages, the input common mode range shrinks.

A rail-to-rail amplifier circuit can be used to improve the input common mode range. In this circuit the input signal can vary over the entire supply voltage range. When a PMOS and a NMOS differential pair are operated in parallel, rail-to-rail or higher input common mode range is obtained. However, use of complementary differential pairs lead to a large variation in the transconductance gm especially in the middle range of the common mode input which makes the circuit highly unstable.

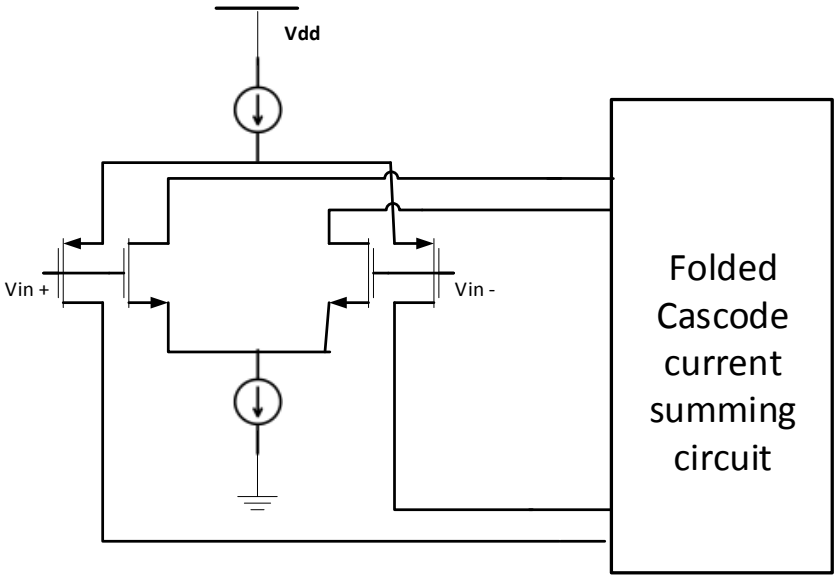

Figure 1.1 Complementary differential pair

Figure 1.1 shows the complementary differential input pair structure. In this circuit, only one differential pair is turned ON at the lower and the upper ends of the input voltage range respectively. Only PMOS differential pair is ON towards the lower end of the input common mode range whereas the NMOS differential pair is in cut off. Only NMOS differential pair is ON towards the higher end of the input common mode range. In the middle range of the input common mode voltage both PMOS and NMOS differential pairs are ON.

As seen in Figure 1.4, in the middle range of the input common mode voltage both the differential pairs are ON and a variation in the tranconductance of almost 2 times is observed. Such a variation in gm is undesirable as it leads to variation in gain and hence unity gain frequency. This makes the circuit unstable.

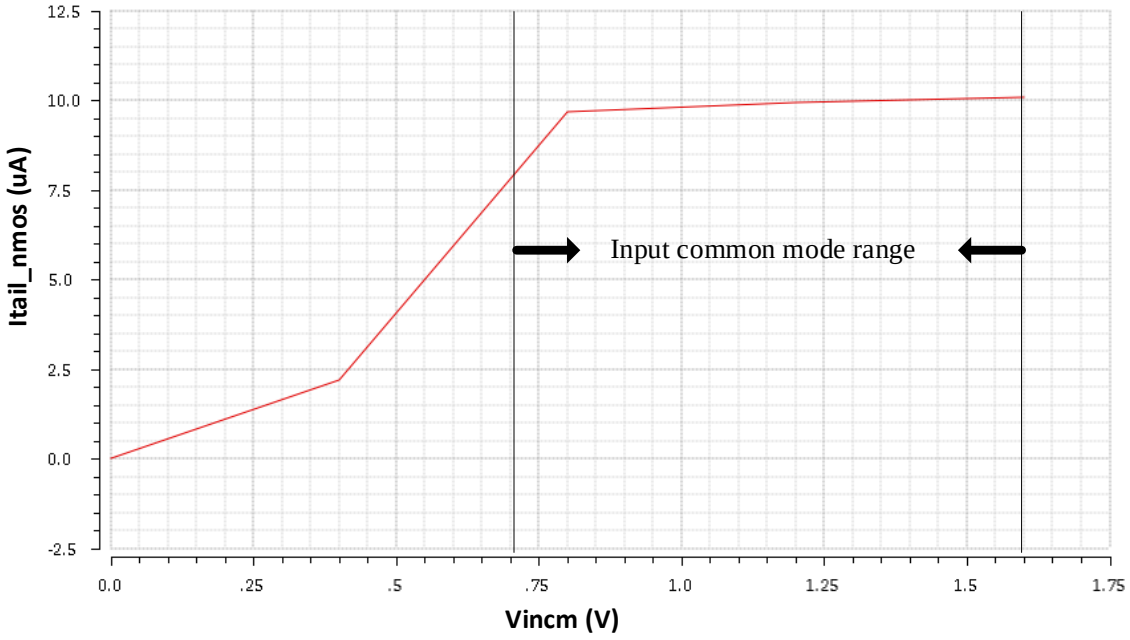

Figure 1.2: Input common mode range of NMOS differential pair

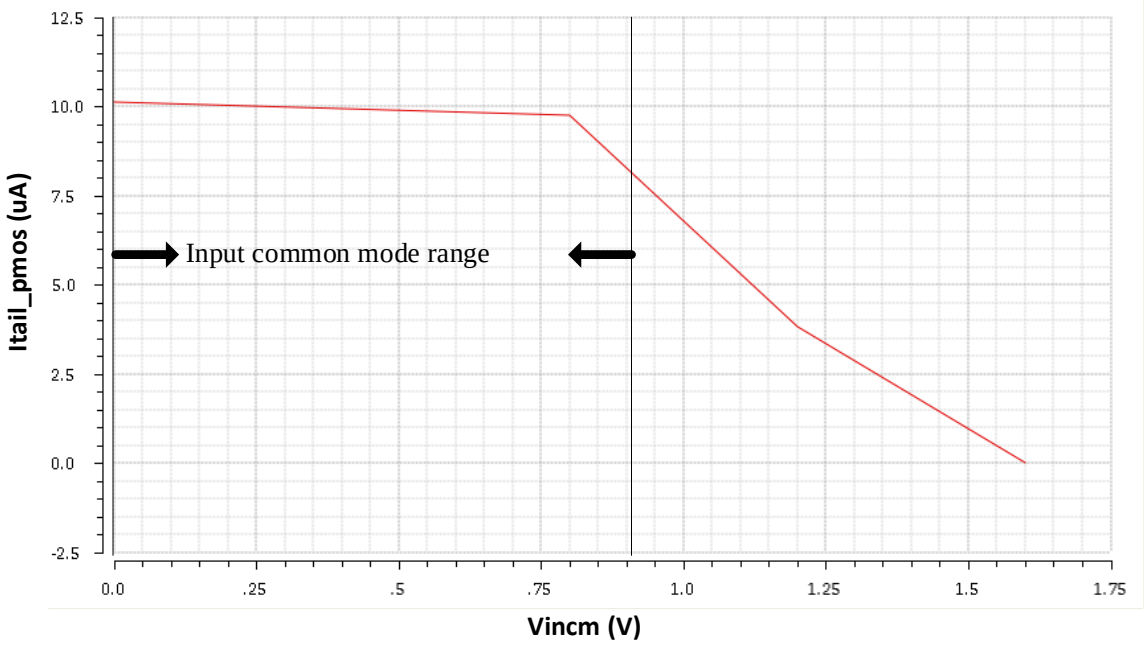

Figure 1.3: Input common mode range of PMOS differential pair

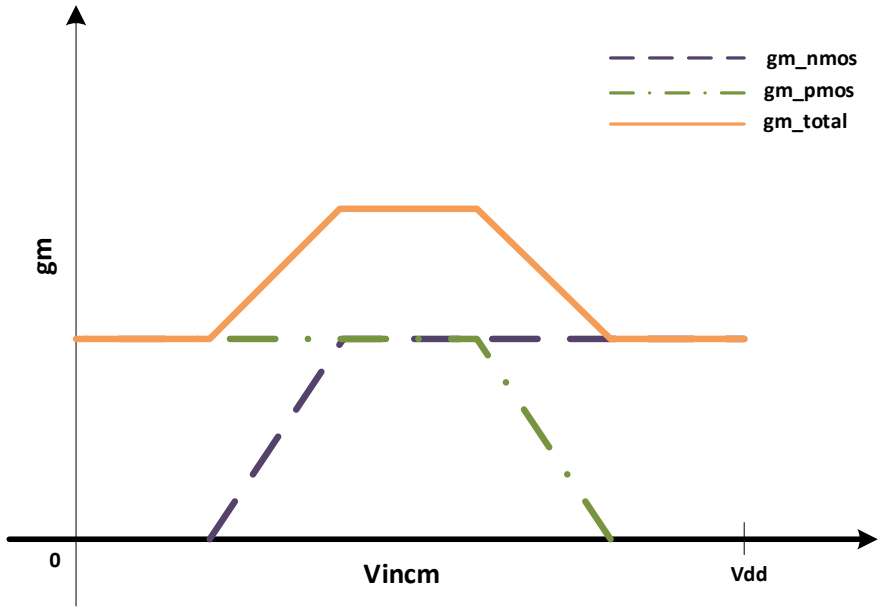

Figure 1.4: Variation in the transconductance throughout the input common mode range

Different techniques have been proposed to achieve a rail-to-rail input common mode range along with a constant transconductance function.

These various techniques to achieve constant transconductance are discussed in Chapter 2. In Chapter 3, an extremely simple technique of achieving constant transconductance by DC level shifting as proposed in [1] is explained. Chapter 4 contains a discussion of the simulation results and Chapter 5 gives the conclusion.

Chapter 2: Survey of accepted techniques for constant transconductance

For the circuit to be stable, constant transconductance is required throughout the input common mode range. Constant transconductance can be achieved by maintaining the sum of the tail currents through the complementary differential pair constant. Another technique to achieve constant transconductance is to employ a maximum or minimum current selection circuit. The tail current through the NMOS and PMOS differential pair is sensed and compared and the one with the higher or the lower value is selected. Some techniques use current switches to adjust the tail current through the complementary differential pairs. [3]

All these techniques require extra circuitry for achieving a constant transconductance leading to an increase in the overall area as well as power consumption. Some techniques also lead to a degraded CMRR and slew rate.

2.1 Level shifting technique

The level shifting technique is one of the simplest techniques to achieve a constant transconductance. In [2] a simple circuit is used to achieve constant transconductance through the use of level shifting technique. A PMOS source follower is used for DC level shifting. The circuit is shown in Figure 2.1. In this circuit the input signal is directly connected to the NMOS differential pair whereas it is connected to the PMOS differential pair through the PMOS source follower circuit.

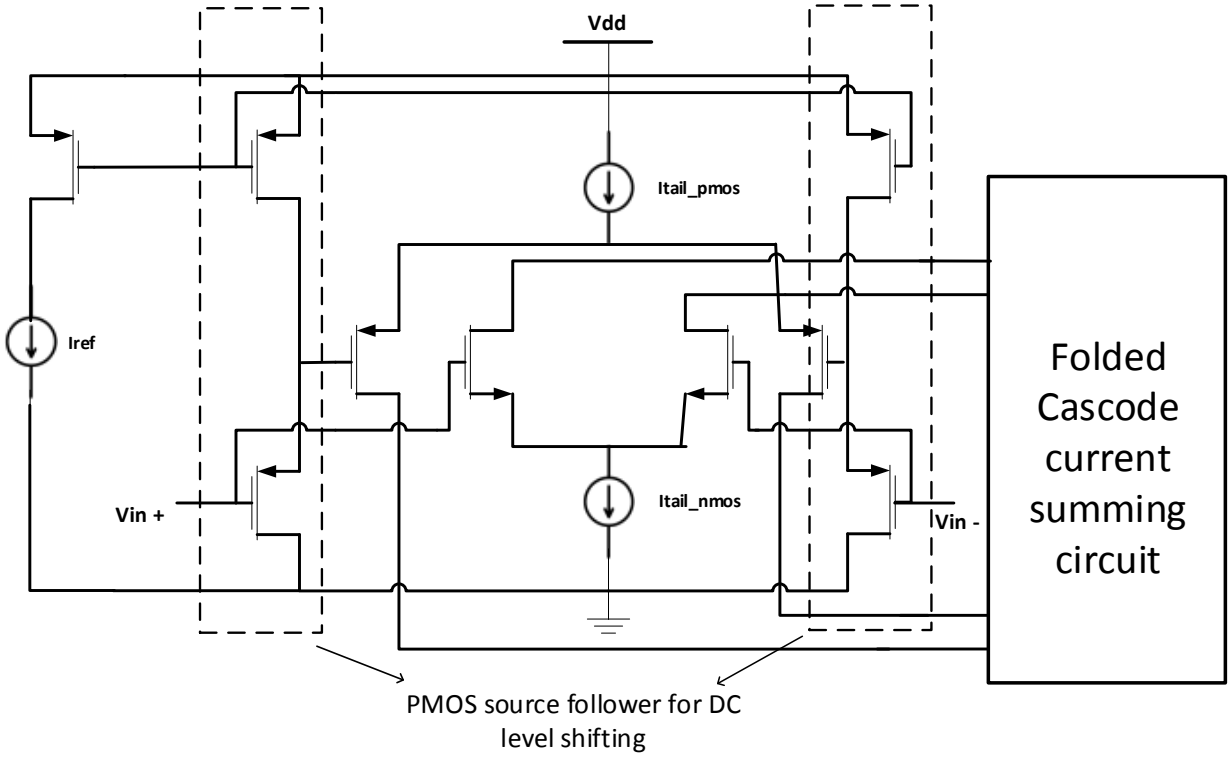

Figure 2.1: DC level shifting using PMOS source follower

The input signal to the PMOS differential pair is shifted by $|V_{gsp}|$ which is the gate to source voltage of the PMOS source follower. The input to the PMOS differential pair V_{inp-sh} is given by the following equation:

$$V_{inp-sh} = V_{in} + |V_{gsp}|$$

$$|V_{gsp}| = V_{ovp} + |V_{thp}|$$

The input signal is shifted toward the lower end of the supply voltage by $|V_{gsp}|$. V_{ovp} is the gate overdrive voltage for PMOS and $|V_{thp}|$ is the threshold voltage for PMOS. The shifting of the transition region of PMOS results in the overlapping of NMOS and PMOS differential pair transition regions leading to a constant transconductance function. With the proper amount of shifting of the transition region a variation in gm of around +/-5% is obtained.

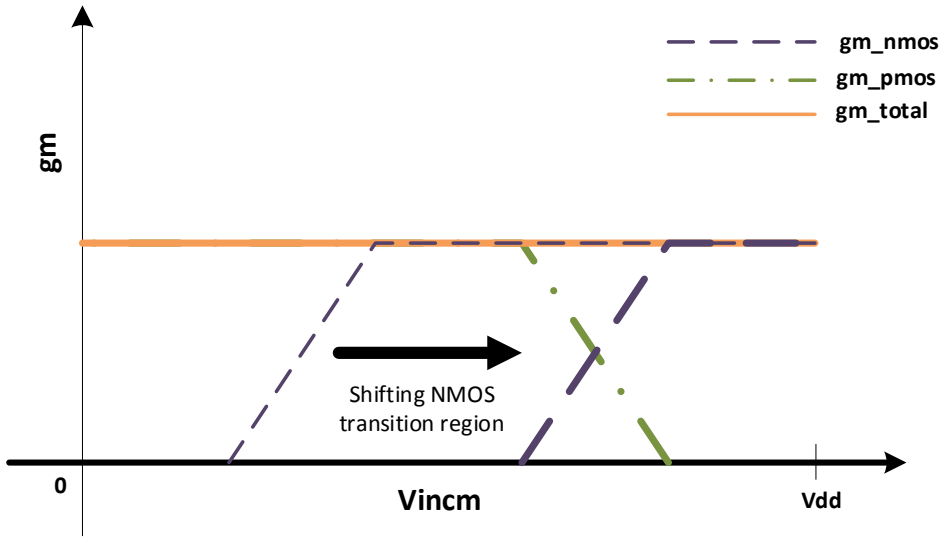

Figure 2.2: Overlapping PMOS transition region for constant transconductance

This circuit however requires 4 additional transistors for the PMOS source follower. [1] proposes a simpler technique for achieving constant transconductance by shifting the transition region of the NMOS differential pair.

Chapter 3: Novel constant transconductance technique

The level shifting technique using PMOS source follower circuit requires 4 additional PMOS transistors to implement the level shifter. In [1] a simpler circuit for level shifting is proposed which uses only one additional transistor. A diode connected NMOS is used to shift the transition region of the NMOS differential pair so as to achieve a constant transconductance. As compared to other techniques, this technique is one of the simplest as it requires just one additional transistor.

Figure 3.1 shows the structure of the simple, novel technique proposed in [1]. The diode connected NMOS is placed above the NMOS tail current source. The NMOS transition region is shifted to the right by a voltage equal to the gate to source voltage of the diode connected NMOS. The value of V_{shift} which is the voltage by which the transition region of NMOS differential pair is shifted can be adjusted by adjusting the size of the diode connected NMOS.

Minimum input voltage for the NMOS differential pair is given by the following equation:

$$V_{in-min} = V_{ovn} + V_{gs1} + V_{gs2}$$

Where V_{gs1} is the gate to source voltage of the NMOS input differential pair. V_{gs2} is the gate to source voltage of the diode connected NMOS and V_{ovn} is the gate overdrive voltage of the NMOS tail current source.

For PMOS differential pair, the minimum input voltage is given by

$$V_{in-min} = |V_{ovp}| + |V_{gsp}|$$

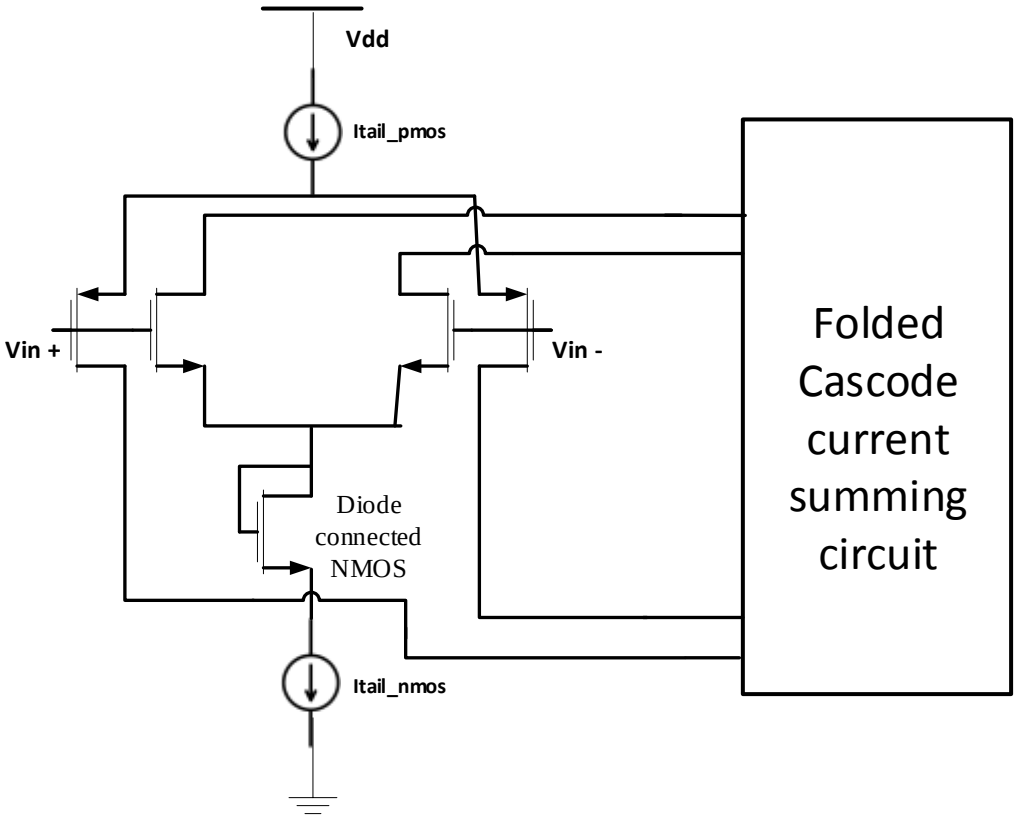

Figure 3.1: Level shifting using diode connected NMOS

Where $|V_{gsp}|$ is the gate to source voltage of the PMOS input differential pair and $|V_{ovp}|$ is the overdrive voltage of the PMOS tail current source.

Thus the diode connected NMOS shifts the transition region of the NMOS differential pair such that the transition regions of the PMOS and NMOS differential pairs overlap and a constant transconductance is obtained throughout the input signal range. The diode connected NMOS gives similar results to that using a source follower circuit for level shifting.

The circuit was designed using XFAB 0.35 µm process technology. XFAB XH035 is a 0.35 micron single poly, triple metal process. It focuses on applications involving high precision, low power mixed signal circuits. It provides various modules such as the low threshold voltage module, low leakage process module, etc.

The MOSLT (low threshold MOS module) has been used in the design of the circuit. Minimum feature size is 0.35µm. It has a 3.3V operating voltage. The threshold voltages for PMOS and NMOS transistors are 0.5V and 0.55V respectively.

The amplifier is a differential input- differential output amplifier.

The circuit is simulated for different values of V_{shift} and the resulting variation in transconductance is observed. The optimum value of V_{shift} which gives the least variation in gm is selected. Figure 3.2 shows the % variation in gm with respect to V_{shift}.

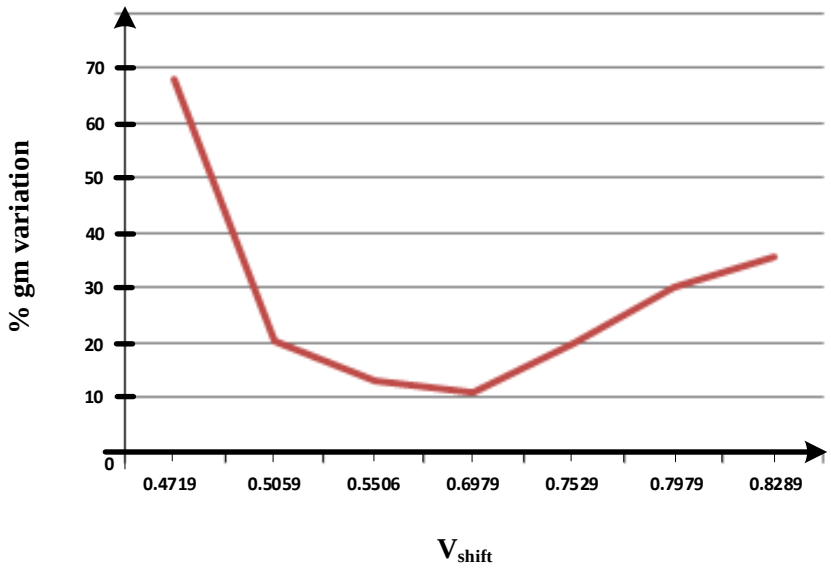

Figure 3.2: Variation in gm w.r.t. the amount of shift in the transition region

Chapter 4: Simulation Results

The circuit is simulated using XFAB 0.35 µm technology. Figure 4.1 shows the complete circuit diagram.

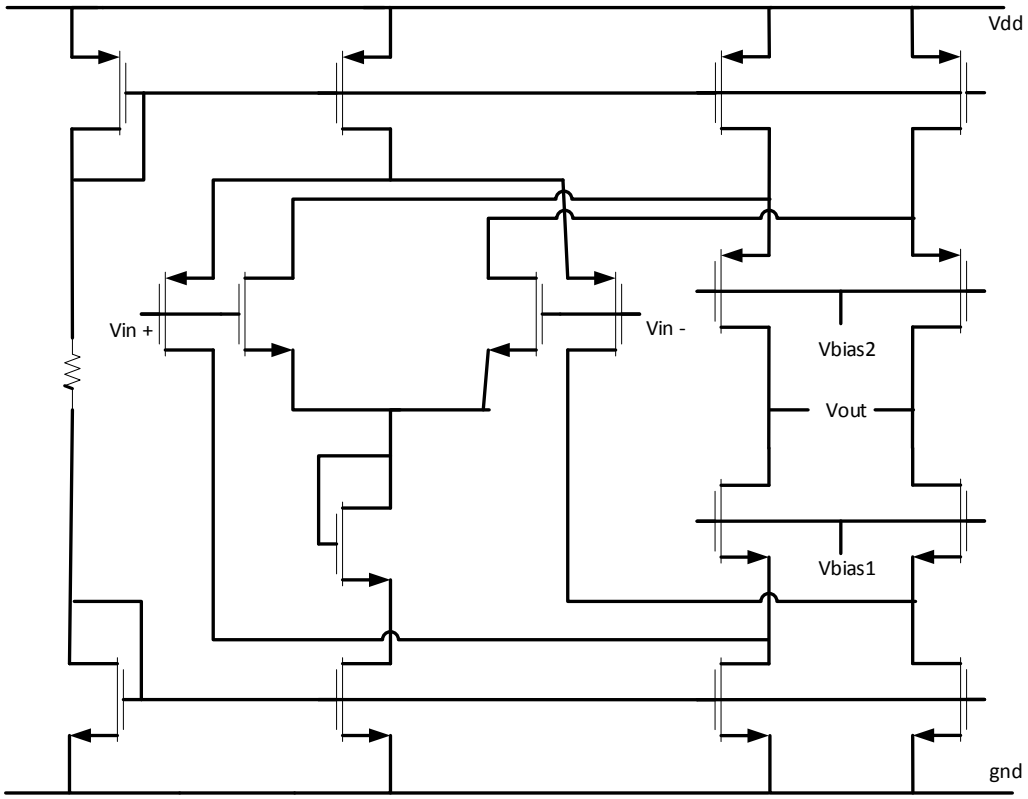

Figure 4.1: Complete circuit for constant transconductance using diode connected NMOS

Cadence SPECTRE simulator is used for simulations. A supply voltage of 1.6V is used. With a shift in the transition region of NMOS differential pair of 0.69V, a variation of 11.3% is observed in the transconductance throughout the input signal voltage range. The variation in gm is higher than that obtained by using the conventional level shifting technique with PMOS source follower. The unity gain frequency is 71 MHz.

The simulation results obtained are summarized in the table below:

Parameter	Value
Supply voltage	1.6V
Gain	40.53dB
Phase Margin	62.77
% gm variation	11.3%
CMRR	174.26dB
Unity Gain frequency	71.06MHz
Average Power Consumption	23.65µW

Table 4.1: Simulation results for level shifting circuit using diode connected NMOS

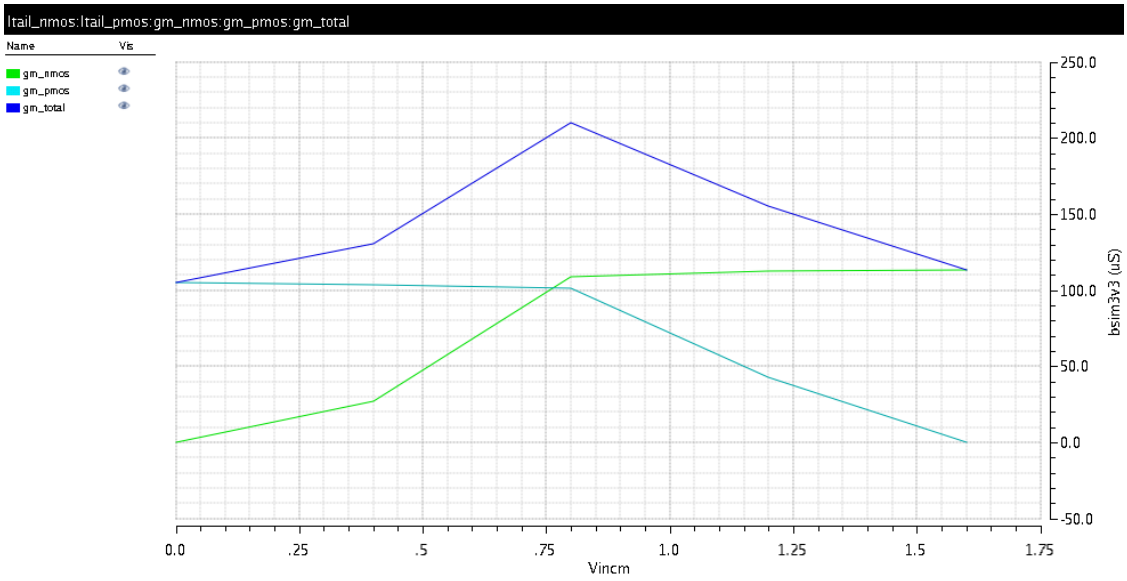

Figure 4.2a: Variation in gm without diode connected NMOS

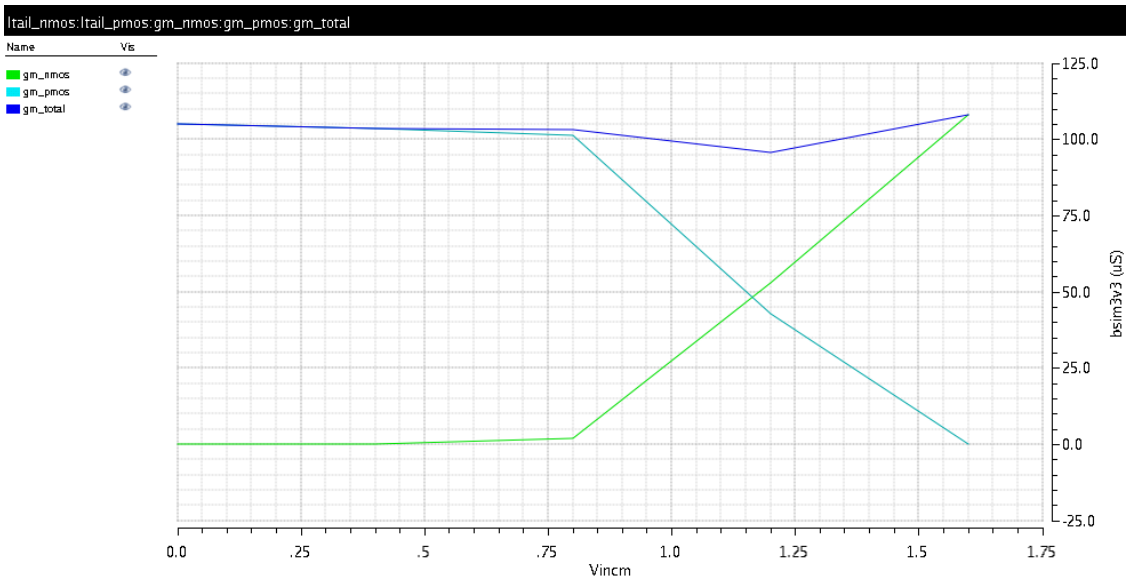

Figure 4.2b: Variation in gm with diode connected NMOS

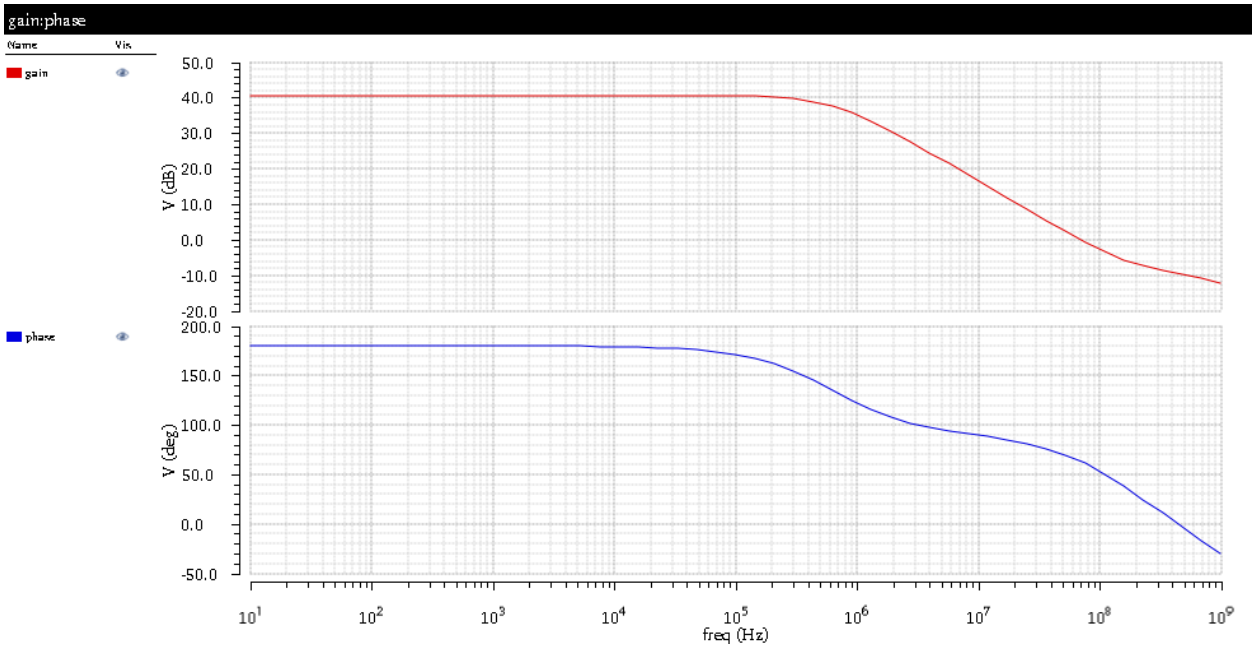

Figure 4.3: Gain and phase of the simulated circuit

The power consumed by this circuit is 23.65 µW which is significantly less. This circuit consumes less power as compared to conventional PMOS source follower level shifting

circuit due to lesser number of devices used. Due to its low power consumption, it is a good choice for battery operated devices. A very high CMRR is obtained.

Figure 4.4 shows the layout of the circuit. The core area is 46.87 x 67.92 µm.

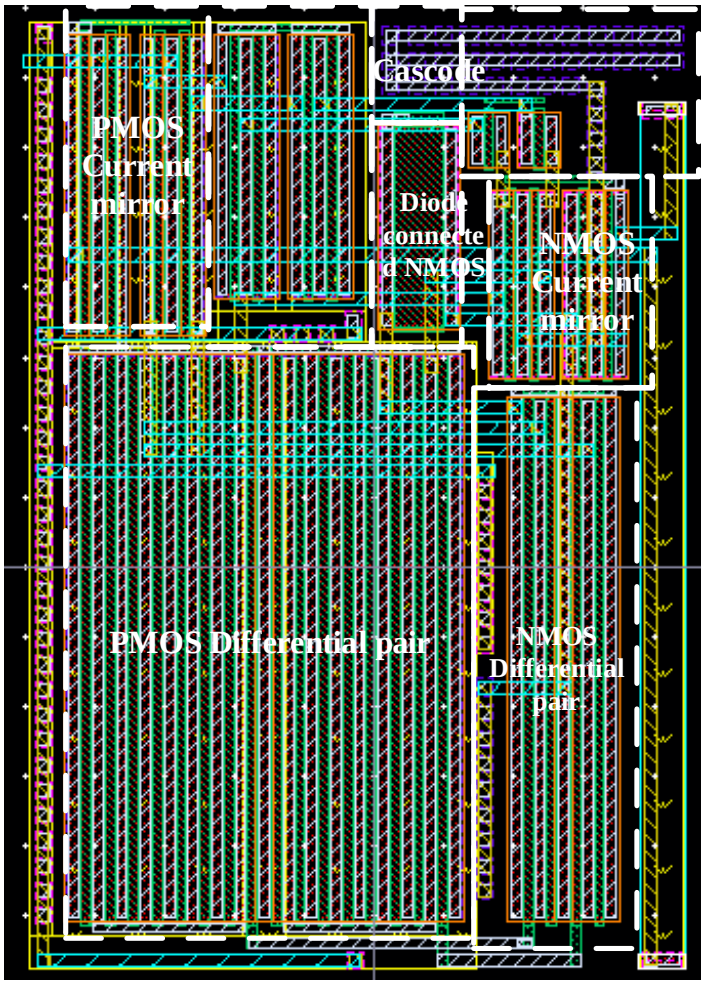

Figure 4.4: Layout of circuit using diode connected NMOS. (Area: 46.87 x 67.92 µm)

Chapter 5: Conclusion

The novel technique proposed in [1] is a simple circuit to achieve constant transconductance by employing the level shifting method. The concept presented in [1] is implemented using XFAB 0.35µm technology. The low threshold MOSLT module has been used for proper voltage headroom. Cadence SPECTRE simulator has been used for all the simulations.

The circuit has a very low power consumption of 23.65uW which makes it suitable for use in circuits for portable devices. Variation in gm of 11.3% is higher than that using PMOS source follower level shifter.

References

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