

**Controlling Harmonic Distortion in Power Electronics  
using Active Power Filters**

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## **Abstract**

Power electronics are used in power systems extensively for power conversion and control, but can generate harmonic distortion in the current that is being drawn. Harmonic distortion can have deleterious effects on the power system, degrading power quality, system performance, and efficiency. Active harmonic filters have gained attention due to the decreasing price and improved availability of power electronics. This thesis discusses some of the conventional methods for correcting harmonic distortion using shunt-connected pure active filters. A novel circuit topology is introduced which utilizes a clamp circuit often used in electric drive systems, allowing the system to have less frequent switching and reduced switching power loss. Simulation results are presented, along with experimental data to confirm the operation.

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# Chapter 1

## Introduction

### 1.1 The Need for Power Electronics

Power electronic converters are widely used in the electrical grid to supply power to consumer electronics, commercial lighting, computing systems, and adjustable speed motor drives for industrial pumps and fans. This demand has increased because of the need for specific voltage and frequency requirements of each load and the gains in efficiency and controllability as opposed to using direct utility grid voltage. Many of these converters control the voltage delivered to the load through pulse-width modulated (PWM) waveforms, using high-frequency switching signals generated by a control system on a microcontroller or FPGA. AC loads such as motors required an AC voltage, which is generated by a PWM inverter using solid-state transistors as switches. These switches utilize a constant DC bus voltage and “chop up” the voltage at the load to generate an average voltage according to the frequency and voltage requirements.

In order to generate the DC voltage needed for the PWM output inverter, an AC to DC stage is required which will convert the grid-side utility AC voltage to a constant DC value. Diode rectifiers are commonly used as the most economical and simplest strategy, which are self-commutating devices that will naturally conduct according to the instantaneous AC voltage values. In a three-phase power system, for example, among the three voltages there will always be one phase whose voltage is maximum and one phase whose voltage is minimum at any instant. The third phase will be neither max or min, and will be referred to as the middle voltage. The diodes connected to the

maximum and minimum voltages will always be conducting, and thus the DC voltage will always represent the maximum line-to-line voltage, which will be utilized by the PWM inverter. In motor applications where regenerative braking is desired, or in wind turbine applications where converters interface variable frequency and variable voltage generators to the utility grid, bi-directional power flow capability is needed through this AC/DC conversion stage. In this case, the insulated-gate bipolar transistors (IGBTs) are connected anti-parallel with the diodes and switched synchronously with the natural diode conduction timing.

## 1.2 The Source of Harmonic Distortion in Power Electronics

A linear converter load would draw sinusoidal currents that contain only the fundamental frequency of the grid voltage and would not contain any harmonics of that frequency. Because of the nonlinear conduction sequence of diode rectifiers, the currents being drawn from the converter are nonlinear in nature and contain many harmonics. Harmonic currents do not draw any real power from the utility power system, and have several deleterious effects on power system quality. These effects include [1, 2]:

- Excessive power loss and overheating of transmission lines, transformers, and generators, causing these system elements to be over-designed and de-rated.
- Harmonic currents can overload the shunt capacitors used in the power system for voltage support, and can also excited resonance between these shunt capacitors and the line inductance connecting them through transmission lines causing heating and overload failure.
- The utility voltage itself can become distorted if the harmonic currents are coming from a large load, negatively impacting other linear loads in the power system.

## 1.3 Proposed Standards

Industry standards for allowable harmonic distortion listed in Table 1.1 have been established under IEEE-519-1992 and IEC61000, which outlines recommended guidelines for

harmonic distortion of current. The guidelines are not designed for individual equipment specifications, but more for the harmonics observed at the point of common coupling (PCC) where many electrical loads are aggregated and tied to the grid at a common location, such as a large industrial load. Total harmonic distortion (THD) is the ratio of the root-mean-square (RMS) of the harmonic content  $I_{Lh}$  to the RMS value of the fundamental component  $I_{L1}$ , expressed as a percentage of the fundamental. The term used in the IEEE-519 specification is total demand distortion (TDD), which is the ratio of the RMS of the harmonic content to the RMS value of the demand load current  $I_L$ . The calculations are often very similar if the fundamental component dominates  $I_L$ :

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + \dots}}{I_1}$$

$$TDD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + I_5^2 + \dots}}{I_L}$$

Maximum Harmonic Current Distortion in Percent of $I_L$						
Individual Harmonic Order (Odd Harmonics)						
$I_{sc}/I_L$	< 11	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	$TDD$
< 20*	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 < 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
*All power generation equipment is limited to these values of current distortion, regardless of actual $I_{sc}/I_L$ .						
where						
$I_{sc}$	= maximum short-circuit current at PCC.					
$I_L$	= maximum demand load current (fundamental frequency component) at PCC.					

Table 1.1: IEEE Std 519-1992: Harmonic Guidelines

## 1.4 How to Overcome Distortion

### 1.4.1 Passive Filters

There are two basic approaches to suppress harmonic distortion in the line currents: passive filters or active filters. Passive filters incorporate inductors and capacitors to form a low impedance circuit to the harmonic currents, allowing only the fundamental component to pass into the utility grid. These are typically custom designed to the harmonic-producing load, and thus can introduce resonant problems if there is a modification in impedance. Passive filters normally require an individual filter tuned to each harmonic frequency, making the filter sensitive to system frequency variations. The passive components are often bulky, heavy and expensive, making it difficult to modify and adapt to the aforementioned system variations.

### 1.4.2 Active Filters

Active power filters use PWM controlled power electronic converters to draw currents from the PCC that are opposite in phase to the harmonic currents drawn by the load, such that the resulting currents into the grid are distortion-free, sinusoidal waveforms. The active filter has the ability to correct for all harmonic simultaneously, with additional control capabilities for power factor correction and unbalanced operating conditions [3]. Active filters can be connected in series or shunt with the PCC, and can take

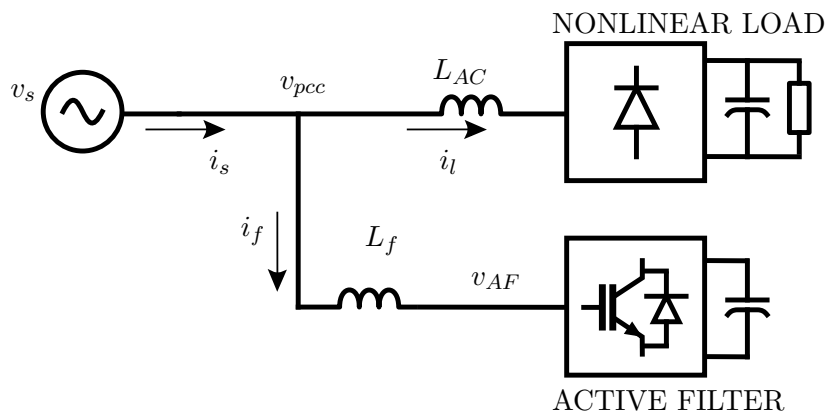


Figure 1.1: System diagram of a pure active filter shunt connected to a nonlinear load, which produces harmonic currents  $i_l$ .

many forms using a purely inductive connection or what is called a hybrid combinations of inductors and capacitors [4]. This paper will focus on the shunt-connected pure active filter, using a single inductor to bridge the converter with the PCC as shown in the system diagram of Fig. 1.1. The converter will be of the voltage-source inverter type, using a capacitor as the DC voltage source for switching the voltage across the filter inductor, generating inductor currents that cancel harmonics from the nonlinear load.

Chapter 2 introduces the details of conventional active power filters. The typical circuit topology is discussed and analyzed, and the methods for characterizing the system as a linear control problem are covered. The basic principles for controlling the active filter currents are described, and some drawbacks to conventional active filters are noted. Chapter 3 will introduce the proposed active power filter topology, which uses a novel circuit configuration and switching strategy to decrease power losses. Chapter 4 provides simulation results to confirm the theory of operation of the proposed active power filter. Chapter 5 will confirm the operation of the system in hardware test results. Chapter 6 summarizes and concludes the thesis.

## Chapter 2

# Conventional Active Power Filters for Harmonic Current Correction

The detailed circuit for a conventional active power filter is shown in Fig. 2.1 . The nonlinear load current  $i_l$  is generated by an adjustable speed drive, with a dc-bus generated by a diode bridge rectifier. The active power filter (APF) consists of a single DC capacitor, six bi-directional switches to form the two-level three-phase power electronic inverter, and a single inductor connecting each leg of the inverter to an input phase. The active filter structure is a voltage source inverter (VSI), which is switched at a constant switching frequency to generate a compensating voltage  $v_{AF}$  on each phase. The voltage induces the compensating currents  $i_{fa}$ ,  $i_{fb}$ , and  $i_{fc}$  to flow through the filter inductors  $L_{fa}$ ,  $L_{fb}$ , and  $L_{fc}$ . Each of the harmonic load currents  $i_{la}$ ,  $i_{lb}$ , and  $i_{lc}$  can be considered to be a superposition of two major current components: the fundamental frequency component  $i_{l1}$  and the harmonic component  $i_{lh}$ . If each phase's filter inductor can be controlled to draw current equal to  $-i_{lh}$  for its own phase, the resulting per-phase currents at the source will be:

$$i_{sa} = i_{la} + i_{fa} = (i_{la1} + i_{lha}) - i_{lha} = i_{la1} \quad (2.1)$$

$$i_{sb} = i_{lb} + i_{fb} = (i_{lb1} + i_{lhb}) - i_{lhb} = i_{lb1} \quad (2.2)$$

$$i_{sc} = i_{lc} + i_{fc} = (i_{lc1} + i_{lhc}) - i_{lhc} = i_{lc1} \quad (2.3)$$

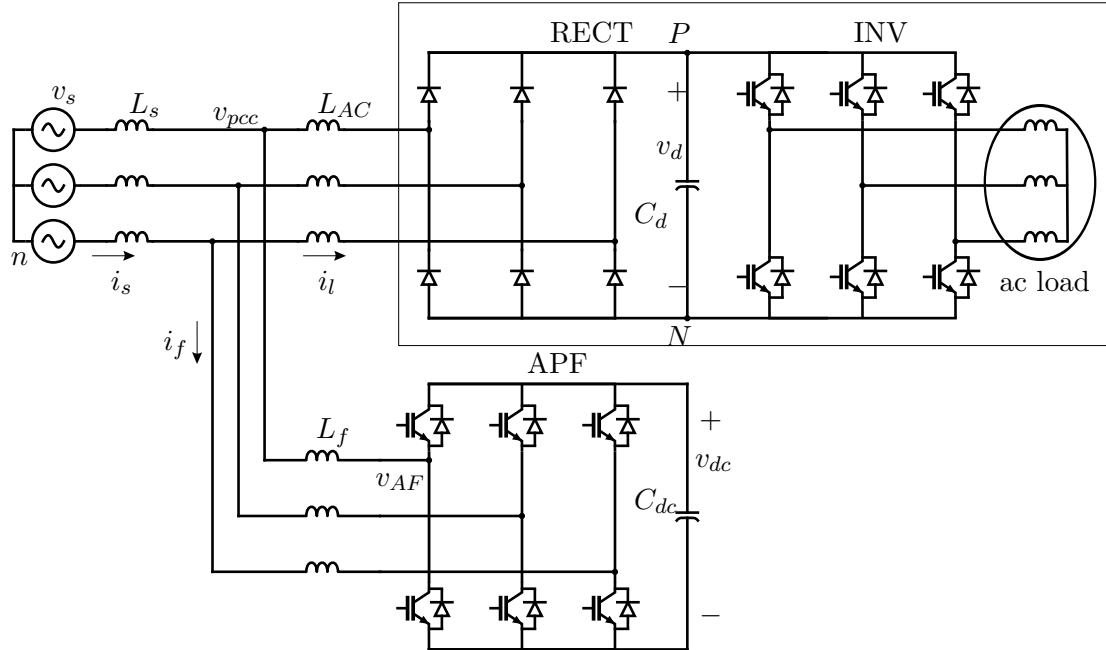


Figure 2.1: Conventional active power filter

In order to extract the desired filter currents to achieve this result, the following steps must be taken:

- Measure the current being drawn by the load  $i_l$ .
- Extract the harmonic currents  $i_{lh}$  from the measured signal.
- Generate the appropriate voltage at the active filter  $v_{AF}$  such that the filter current  $i_f$  is equal to  $-i_{lh}$ .

## 2.1 Control Theory

The controller that generates the switching signals operates on a microcontroller or FPGA platform. The control architecture uses cascade feedback control as shown in Fig. 2.2, where the current controller operates in an inner loop designed at a higher bandwidth frequency than the outer control loop, which regulates the DC voltage on the capacitor.

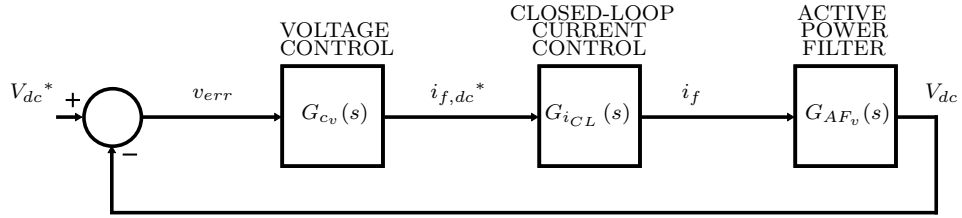


Figure 2.2: Cascade feedback control block diagram

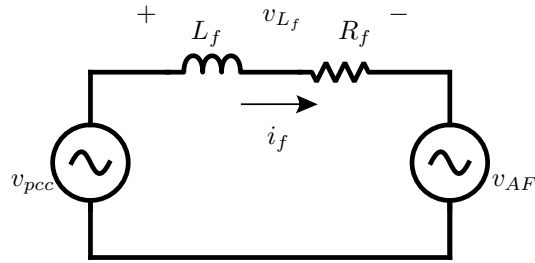


Figure 2.3: Plant system to be controlled: an inductor with a series resistance

In linear control theory, typically a “plant” transfer function is considered as the system that is to be controlled. When controlling the current in a VSI in an active power filter, the system to be controlled can be modeled as an inductor with a series resistance as depicted in the single-line diagram of Fig. 2.3. Using the Laplace variable  $s$ , an equation can be written in the frequency domain describing the current through this inductor as:

$$i_f = \frac{v_{L_f}}{R_f + sL_f} = \frac{v_{PCC} - v_{AF}}{R_f + sL_f} \quad (2.4)$$

with variables as follows:

- $L_f$ : filter inductor
- $R_f$ : series resistance of  $L_f$
- $i_f$ : current through  $L_f$
- $v_{L_f}$ : voltage across  $L_f$
- $v_{PCC}$ : voltage at the point of common coupling (PCC)
- $v_{AF}$ : pole voltage of active filter



A reference signal  $i_f^*$  is generated and compared against the measured current  $i_f$  to generate an error signal  $i_{f,error}$ . The error signal is passed through a PI controller system which will calculate the required voltage needed at the active filter pole voltage  $v_{AF}$  to minimize the error.

### 2.1.1 Current Controller

The bandwidth of the current controller is desired to be high enough to control the most significant harmonic frequencies, but is generally kept ten times lower than the switching frequency of the active filter. In this case, we will consider a switching frequency of 10kHz to make the topology applicable to higher power levels, so the target controller bandwidth is 1kHz. This is done because applying linear control methods requires the system to be linearized around a steady state operating point, and the switching IGBT converters can be considered to be linear below this frequency. The switching frequency of the converter is kept low in order for the topology to be suitable for higher power devices and to minimize switching power losses, which increase proportionally with frequency.

When designing the PI gain values for the current control loop to set the controller bandwidth, it is important to include any filter stages or sampling delays into the stability study of the controller. Most notably, when sampling analog signals from current sensors or voltage sensors, it is common to place an analog low-pass filter before the analog-to-digital sampling phase in order to avoid aliasing errors. It is also convenient to filter the high frequency 10kHz switching signal from the measured currents with this low pass filter, since you don't want the controller to react to these high frequency disturbances. Because of this later requirement, the LPF transfer function can become a significant contributor to the closed-loop performance and bandwidth of the controller, and cannot be ignored when determining controller stability conditions. The full current control system is shown in Fig. 2.4.

### Filter Current Detection

In order to derive the reference filter current  $i_f^*$ , the load current  $i_l$  is first measured and transformed into a  $dq$  reference frame, rotating at the synchronous frequency of the utility voltage. The angle of this rotation is measured using a phase-locked loop

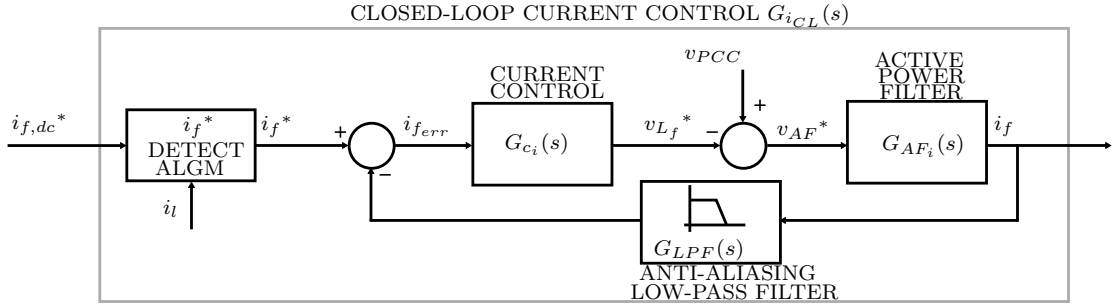


Figure 2.4: Closed loop system for the current controller. Includes algorithm for detecting  $i_f^*$ , control system  $G_{c_i}(s)$ , feedforward term  $v_{PCC}$ , and low-pass filter  $G_{LPF}(s)$  to keep the measured filter current  $i_f$  from having aliasing from the sampling process, along with keeping switching currents out of the control signal.

(PLL) to keep the  $dq$  reference frame synchronized with the utility phase and frequency. If the three load currents are transformed into this rotating  $dq$  frame, the fundamental frequency of the load current is represented as DC components of  $i_{ldq}$ , while the harmonic components  $i_{lh}$  are contained in the AC content of  $i_{ldq}$ . These components can be isolated using digital IIR filters, where a high-pass filter (HPF) would capture the harmonic waveform and the low-pass filter (LPF) would capture the fundamental component of  $i_l$ , which will be called the source current reference  $i_s^*$ . The filter current reference  $i_f^*$  as depicted in 2.5 is then calculated by subtraction:

$$i_f^* = i_s^* - i_l = -i_{lh}$$

Ideally,  $i_f^*$  could be derived by directly taking the output of a high-pass filtered signal which captures the harmonics of the load, but low-order IIR filters have some inherent nonlinear phase delay which can corrupt the correct detection of the harmonic waveform. The DC value of the  $dq$ -currents can be captured by the LPF without the consequence of phase distortion, since it does not vary with time in steady state. There would, however, be a penalty in the dynamic performance under step load changes since the DC tracking would be slowed by the LPF. This paper will use the low-pass filter method followed by subtraction, to favor the steady state performance improvement. There are also several other methods to detect the harmonic waveform, including Fourier

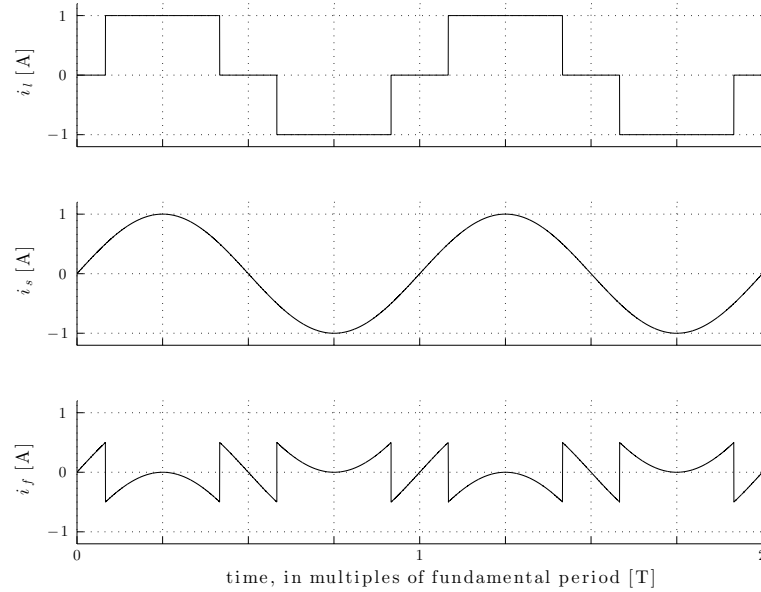


Figure 2.5: Example of ideal load current  $i_l$ , source current  $i_s$ , and filter current  $i_f$ . It can be observed from the graphs that  $i_f = i_s - i_l$ .

analysis and using multiple reference frames for each harmonic [5]

If harmonic correction is the only goal for the active power filter, then only the AC components of the  $d$  and  $q$ -axis load currents  $i_{ld}$  and  $i_{lq}$  are retained for the reference filter current  $i_f^*$ . In this case, the DC components represent a sinusoidal wave at the fundamental frequency with a power factor angle dependent on the amount of DC  $q$ -axis current. If power factor control was also required in the control objective, then the DC value of the  $q$ -axis current could be set to any value to control the power factor angle.

### 2.1.2 Feedforward Signal

A feedforward term must be added after the current controller that will add the voltage at the point of common coupling  $v_{PCC}$  to the control signal, depicted in Fig. 2.4. This is because the voltage that is required to appear at the active filter  $v_{AF}$  needs to track  $v_{PCC}$  closely; the inductor current depends on the difference of these voltages, and the controller is meant to stabilize small-signal errors around the steady-state operating

point. By including this term, the current controllability is improved since the linear PI controller no longer has to include the superposition of this waveform with the control signal and can respond more on the error disturbances in the filter current  $i_f$ . In conventional active power filters, this feedforward term is simply the phase voltage of the voltage source  $v_s$ .

### 2.1.3 Voltage Controller

The outer control loop is designed with a lower controller bandwidth than the inner loop—normally ten times less. This feedback loop regulates the DC voltage appearing across the capacitor without any additional power supply, by controlling a small amount of current from the utility source. The set point for the dc voltage is determined by the maximum current time derivative demanded by the harmonic load currents, in order to allow the active filter to adequately supply enough voltage across the filter inductors to match these harmonics.

The output of the DC voltage controller will be added to the reference value for  $i_{fd}^*$  to regulate the voltage and minimize error. This is because a small amount of real,  $d$ -axis current is required to maintain this capacitor voltage constant [4]. The full system diagram for the  $i_f^*$  detection algorithm is shown in Fig. 2.6.

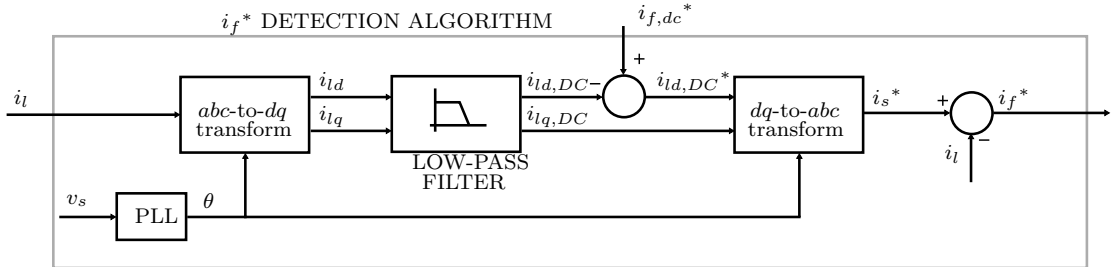


Figure 2.6: Detection algorithm for desired filter current  $i_f^*$ . The load current  $i_l$  is sensed and transformed into the  $dq$  domain rotating at the angle  $\theta$  of the input voltage. The fundamental component is extracted, added with the  $d$ -axis requirements to regulate the DC voltage, and subtracted by the load current  $i_l$  to derive the reference filter current  $i_f^*$ .

## 2.2 Drawbacks of Conventional Active Filters

Traditional active filters discussed thus far have two distinct disadvantages. The first is the use of an external high-voltage DC capacitor as the storage element and voltage source for the inverter. This capacitor is required to be large enough to inject the harmonic currents into the source, and these harmonic currents can have a large magnitude if the converter is operating at high power. The DC voltage rating of the capacitor is also determined by the operating power level, and imposes further size constraints.

The second disadvantage is the additional hardware of six switches used for the inverter, and the associated switching losses incurred by the devices. Power is lost during each switching transition of the IGBTs, and the overall power loss per switch and for the entire six-switch VSI can be estimated by the following equations:

$$P_{loss,sw} = \frac{1}{2}V_d i_{sw}(t_{on} + t_{off})f_s \quad (2.5)$$

$$\begin{aligned} P_{loss,VSI} &= 6 \cdot P_{loss,sw} \\ &= 3V_d i_{sw}(t_{on} + t_{off})f_s \end{aligned} \quad (2.6)$$

with variables defined as:

- $P_{loss,sw}$ : average switching power loss in a single IGBT
- $P_{loss,VSI}$ : average switching power loss in a VSI containing six IGBTs
- $V_d$ : DC-bus voltage of active power filter
- $i_{sw}$ : instantaneous current of active filter switch at switching transition
- $t_{on}$ : rise time of IGBT to turn ON
- $t_{off}$ : fall time of IGBT to turn OFF
- $f_s$ : switching frequency

The control of current distortion in order to maintain distortion limits below what is specified in Table 1.1 is an important consideration, and the additional costs associated with these two disadvantages are justified by the benefits of low harmonic distortion on the utility line. However, this paper suggests an alternative method to active filtering that addresses these shortcomings.

## Chapter 3

# Proposed Minimally-Switched Active Power Filter

The active filter topology presented here is shown in Fig. 3.1 in the context of an adjustable speed drive system for an inductive load. The drive is an AC-to-AC matrix converter-based topology with 12 unidirectional switches, as was proposed in [6], which eliminates energy storage components in the DC bus link. The converters are bridged with a virtual DC-link that has a fluctuating voltage, hence the converter is given the name direct-link drive. The active filter utilizes another 3-phase two-level VSI to draw compensating harmonic current from the supply, canceling the harmonic content drawn by the load.

The voltage at the direct-link  $v_d$  is generated by the front-end converter, which is conducting at line-switched intervals to behave like a diode bridge rectifier. The rectifier will conduct the IGBTs such that the positive terminal  $P$  of the  $v_d$  will always be connected to the maximum voltage, while the negative terminal  $N$  will always be connected to the minimum voltage. This voltage  $v_d$  is a fluctuating with an AC component representing the maximum instantaneous line-to-line voltage available from the source.

A clamp circuit consisting of a clamp diode  $D_{cl}$  and clamp capacitor  $C_{cl}$  is used for protection of the direct-link drive. This circuit is necessary in most converter circuits in case the dc current  $i_d$  is interrupted due to dead time in the inverters switching signal, or due to an unintentional disruption in the signals provided by the controller

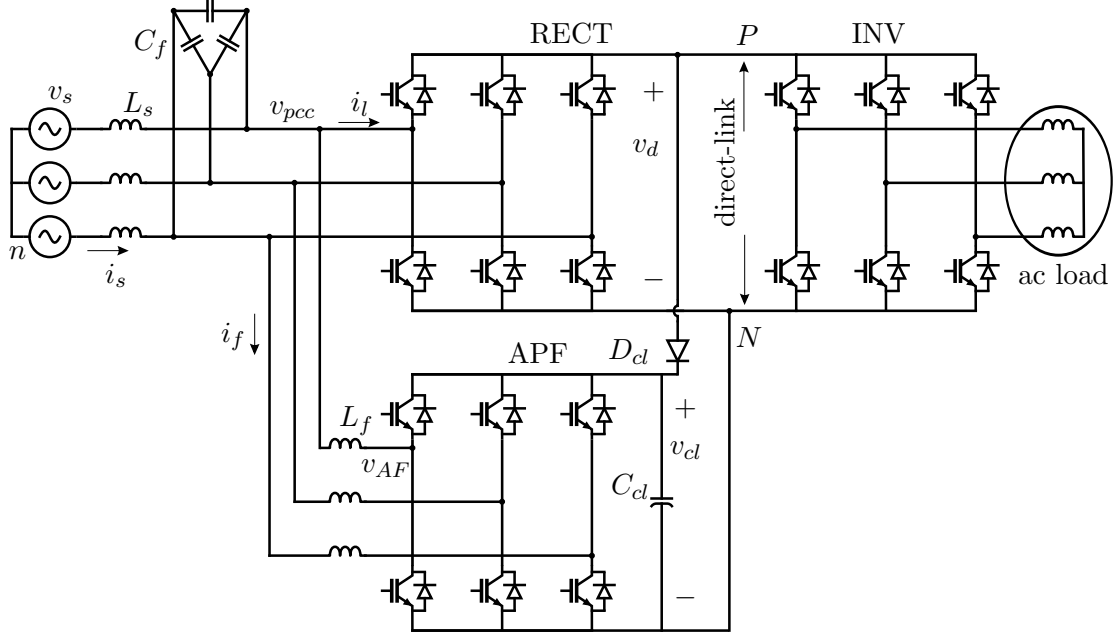


Figure 3.1: Proposed Active Filter Topology

in a fault condition. The clamp circuit provides a path for the currents to flow and reduces harmful voltage spikes that would appear across the devices in such an event, which would otherwise lead to irreparable damage from over-voltage. The active filter will use this clamp capacitor as the voltage source to inject the harmonic currents into the supply.

### 3.1 Operation With Minimal Switching

For proper operation of the active power filter and the direct-link drive, the first control objective is to ensure that the clamp voltage  $v_{cl}$  which appears on  $C_{cl}$  is always higher than the line-line voltage, which will appear at  $v_d$ . This guarantees that the clamp diode  $D_{cl}$  will always be reverse biased under normal operating conditions. The negative terminal of the direct-link  $N$  and thus the negative terminal of  $C_{cl}$  are always connected to the minimum input phase voltage.

As described in [7], consider the case when phase- $c$  voltage is minimum. During this time, the active power filter can effectively be represented as shown in Fig. 3.2. Since

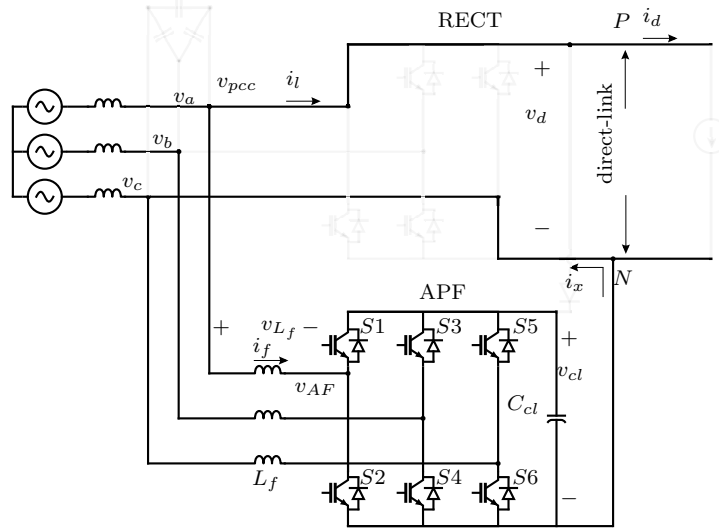


Figure 3.2: Simplified circuit model when phase- $c$  is minimum, ignoring filter capacitors and inactive switches. The maximum phase is arbitrarily chosen as  $a$ , so phase- $b$  is the middle voltage and hence is not connected to the direct link  $v_d$ . It is assumed  $v_d < v_{cl}$ , so the clamp diode  $D_{cl}$  is reverse biased and appears as an open circuit. The inverter is modeled as a current source drawing  $i_d$ .

the negative terminal of the clamp capacitor  $C_{cl}$  is equal to  $v_c$ , the voltages appearing across the filter inductors  $L_{fa}$ ,  $L_{fb}$ , and  $L_{fc}$  can be defined in each switching state as:

$$\begin{aligned}
 v_{L_{fa}} &= \begin{cases} v_{ac} - v_{cl} & \text{if } S1 \text{ is ON} \\ v_{ac} & \text{if } S2 \text{ is ON} \end{cases} \\
 v_{L_{fb}} &= \begin{cases} v_{bc} - v_{cl} & \text{if } S3 \text{ is ON} \\ v_{bc} & \text{if } S4 \text{ is ON} \end{cases} \\
 v_{L_{fc}} &= \begin{cases} -v_{cl} & \text{if } S5 \text{ is ON} \\ 0 & \text{if } S6 \text{ is ON} \end{cases}
 \end{aligned} \tag{3.1}$$

From (3.1), it can be concluded that the inductor voltages  $v_{L_{fa}}$  and  $v_{L_{fb}}$ , corresponding to the phases with the maximum and mid voltages, can take both positive and negative values depending on the switching positions. This is because the phase- $c$  voltage  $v_c$  is the minimum. Thus, the currents through the inductors  $L_{fa}$  and  $L_{fb}$  can be controlled.



Using  $dq$ -extraction and the subtraction method as described in section 2.1.1, let the harmonic currents that are desired to be drawn from the three phases be defined as  $-i_{lha}$ ,  $-i_{lhb}$ , and  $-i_{lhc}$ . Neglecting filter capacitors  $C_f$ ,

$$\begin{aligned} i_{sa} &= i_{la} + i_{fa} \\ i_{sb} &= i_{lb} + i_{fb} \\ i_{sc} &= i_{lc} + i_{fc} \end{aligned} \quad (3.2)$$

So,

$$\begin{aligned} i_{fa}^* &= i_{sa}^* - i_{la} = -i_{lha} \\ i_{fb}^* &= i_{sb}^* - i_{lb} = -i_{lhb} \\ i_{fc}^* &= i_{sc}^* - i_{lc} = -i_{lhc} \end{aligned} \quad (3.3)$$

Assuming the filter currents  $i_{lfa}$  and  $i_{lfb}$  can be controlled to be  $-i_{lha}$  and  $-i_{lhb}$ , consider the situation when the leg of phase- $c$  of the active filter is not switched ( $S6$  is ON). The sum of the active filter currents  $i_{lfa}$  and  $i_{lfb}$  flows through the input phase- $c$ , taking the path from the clamp capacitor negative terminal  $N$  through the lower switch conducting in the rectifier. This is apparent from Fig. 3.3, which also clarifies the path for the current  $i_x = i_{fa} + i_{fb}$ . Thus ideally,

$$\begin{aligned} i_{fa} &= -i_{lha} \\ i_{fb} &= -i_{lhb} \\ i_{fc} &= 0 \\ i_x &= i_{fa} + i_{fb} \end{aligned} \quad (3.4)$$

For a balanced 3-phase system,

$$\begin{aligned} i_{sa} + i_{sb} + i_{sc} &= 0 \\ i_{la} + i_{lb} + i_{lc} &= 0 \end{aligned} \quad (3.5)$$

Thus, using (3.2), (3.4), and (3.5),

$$\begin{aligned} i_{lha} + i_{lhb} + i_{lhc} &= 0 \\ i_x &= i_{lhc} \\ i_{sc} = i_{lc} - i_x &= i_{lc} - i_{lhc} \end{aligned} \quad (3.6)$$

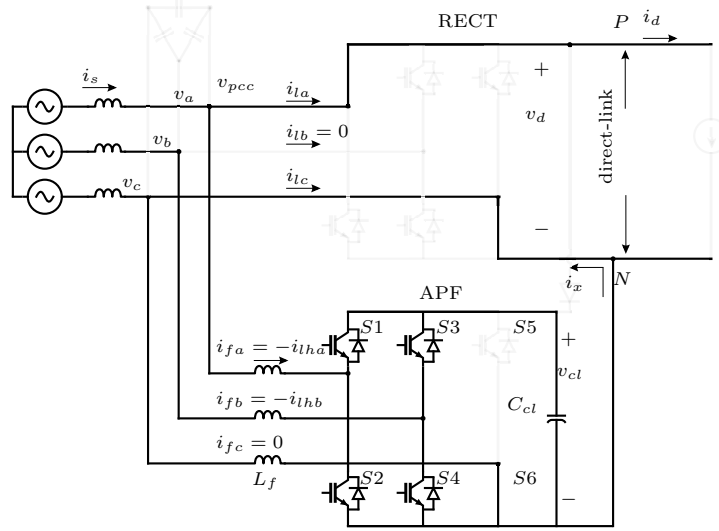


Figure 3.3: Simplified circuit model when the minimum phase- $c$  is minimum and is not switched. The path for  $i_x$  is shown to flow through phase- $c$ , automatically correcting the minimum phase.

From (3.6) it can be seen that if  $i_{lha}$  and  $i_{lhb}$  are compensated for using the active filter, and the leg corresponding to phase- $c$  is not switched, the harmonic current of phase- $c$   $i_{lhc}$  gets automatically compensated.

The objective of harmonic elimination and power factor correction can also be achieved using a conventional active filter with an isolated capacitor as discussed in chapter 2. The novelty of the proposed active filtering mechanism lies in the combination of the active filter with the clamp circuit and still being able to achieve sinusoidal input currents. Also, the switching strategy is such that at any given time, one of the three legs of the active filter is not switched. This leads to an overall reduction in switching losses, so the power loss due to switching is equal to four times the power loss of an individual switch. Using (2.5) the switching loss for the minimally switched active power filter (MSAPF) is

$$\begin{aligned} P_{loss,MSAPF} &= 4 \cdot P_{loss,sw} \\ &= 2V_d i_{sw} (t_{on} + t_{off}) f_s \end{aligned}$$

which is two-thirds of the switching power loss of conventional active power filters (2.6).

## 3.2 Practical Considerations of MSAPF

In order to achieve the active filter operation as described above, there are some practical implementation features that need to be considered with respect to conventional active filters. These considerations need to be addressed with respect to the controller in order for linear control theory to remain effective. In the foregoing discussion of this section, it will be assumed that the period of time described is when phase-*c* is minimum, though the claims are equally valid for any other time when phase-*a* or phase-*b* is minimum with the proper adjustments.

### 3.2.1 Correcting the Current Controller

In the process of deriving the reference filter current  $i_f^*$ , the load current  $i_l$  is sensed and transformed into the  $dq$ -domain, where fundamental component  $i_{l1}$  is represented as dc values and extracted using a low-pass filter. However, when the minimum phase switching strategy is applied and phase-*c* is minimum, the measured current  $i_{lc,measured}$  contains other residual currents besides the load current.

#### Residual Currents in Load Current Measurements

One of the residual currents occurring through the minimum phase path is the exponential discharging of current from  $L_{fc}$ , the filter inductor. This inductor — along with its series resistance  $R_{fc}$  — is essentially being shorted as indicated in Fig. 3.2. The current at the instant phase-*c* is switching from mid to minimum is held and decays with a time constant  $\tau = L_f/R_f$ . The instant phase-*c* becomes minimum is  $\omega_i t = 0$ , and remains the minimum until  $\omega_i t = 2\pi/3$ , where  $\omega_i$  is the frequency of the source voltage in radians per second. With an initial condition  $i_{fc}|_{\omega_i t=0^+}$  to indicate the value of current at the beginning of this period, the current decay can be described mathematically as:

$$i_{fc} = i_{fc}|_{\omega_i t=0^+} \cdot e^{-t \frac{R_f}{L_f}} \quad \text{for all } \omega_i t \in (0, 2\pi/3] \quad (3.7)$$

To characterize this current, the initial condition of the exponential decay can be calculated as follows. Assuming a power factor angle of 0 is required, the source current

$i_{sc}$  should be in phase with the source voltage  $v_{sc}$ . Let the ideal current for  $i_{sc}$  be written in terms of the fundamental component of  $i_{lc}$ :

$$\begin{aligned} i_{sc}^* &= i_{lc1} \\ &= \hat{I}_{l1} \cdot \cos(\omega_i t - 4\pi/3) \end{aligned} \quad (3.8)$$

where  $\hat{I}_{l1}$  is the peak value of the fundamental load current  $i_{lc1}$ . Prior to the minimum phase period there is no current conducting from the rectifier since phase- $c$  is the middle voltage, so the load current  $i_{lc} = 0$ . Therefore at  $\omega_i t = 0^-$ , using (3.3) and (3.8) it can be assumed that  $i_{fc}$  has been controlled to be:

$$\begin{aligned} i_{fc}|_{\omega_i t=0} &= i_{sc}^*|_{\omega_i t=0^-} - i_{lc}|_{\omega_i t=0^-} \\ &= \hat{I}_{l1} \cos(0 - 4\pi/3) - 0 \\ &= -\hat{I}_{l1}/2 \end{aligned} \quad (3.9)$$

Substituting (3.9) into (3.7):

$$i_{fc} = -\frac{\hat{I}_{l1}}{2} \cdot e^{-t\frac{R_f}{L_f}} \quad \text{for all } \omega_i t \in (0, 2\pi/3] \quad (3.10)$$

Along with this discharging current, the measured current into the minimum phase rectifier will sense  $-i_x$ . This currents path follows the negative terminal of the dc-link  $N$ , through the rectifiers lower switch, and to the minimum phase of the source. The negative terminal of the clamp capacitor  $C_{cl}$  shares the point  $N$ , and provides the return path for  $i_{fa}$  and  $i_{fb}$ . Including these paths shown in Fig. 3.4 and and using (3.10),

$$\begin{aligned} i_{la,measured} &= i_{la} \\ i_{lb,measured} &= i_{lb} \\ i_{lc,measured} &= i_{lc} - i_x - i_{fc} \\ &= i_{lc} - i_x + \frac{\hat{I}_{l1}}{2} \cdot e^{-t\frac{R_f}{L_f}} \end{aligned}$$

Also, because of (3.5),

$$\begin{aligned} i_{la,measured} + i_{lb,measured} + i_{lc,measured} &= i_{la} + i_{lb} + i_{lc} - i_x + \frac{\hat{I}_{l1}}{2} \cdot e^{-t\frac{R_f}{L_f}} \\ &= -i_x + \frac{\hat{I}_{l1}}{2} \cdot e^{-t\frac{R_f}{L_f}} \\ &= i_{residual} \end{aligned} \quad (3.11)$$

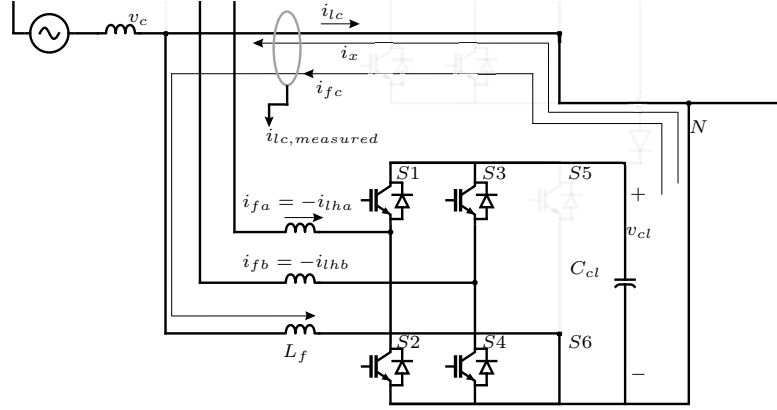


Figure 3.4: Circuit model showing the paths for  $i_x$  and  $i_{fc}$  being included in the measured load current  $i_{lc,measured}$ .

So it is clear that the three-phase currents measured entering the rectifier will have this residual current, which when observed will appear to be unbalanced with a zero-sequence current as indicated by (3.11). Recall the goal is to generate a set of reference currents  $i_s^*$  that is derived from the dc component of the  $dq$  values of the load currents  $i_{ld}$  and  $i_{lq}$ . The filter reference currents  $i_f^*$  are then calculated from these values as detailed in section 2.1.1.

To avoid managing the zero-sequence current being introduced into the controller from these sensed load current signals, the measurements should be compensated to remove  $i_{residual}$ . This is done so the  $dq$  transformation can capture the magnitude and phase of the fundamental component of the rectifier load current as though the residual currents were not there. This keeps the filter detection algorithm simple as in section 2.1.1, where simple IIR filters are used on the  $dq$  variables to extract the fundamental component. This also avoids designing a controller around zero-sequence components. It is important to note that  $i_x = i_{fa} + i_{fb}$ , so  $i_{residual} = i_{fa} + i_{fb} + i_{fc}$  at all times. This compensation can easily be achieved by subtracting the sum of the filter currents from the load current corresponding to the minimum phase.

### Adjusting the Integral Control

During the time when phase- $c$  is minimum, the filter inductor  $L_{fc}$  is not being controlled directly since that inverter leg is not being switched. We have also adjusted the set point for the error signal to be equivalent to a conventional active filter, which would equal  $-i_{lhc}$  during the minimum phase period. It should be noted that mean value  $-i_{lhc}$  is positive during this time, and will integrate to a positive number. The filter current error signal generated will be,

$$\begin{aligned} i_{fc,error} &= i_{fc}^* - i_{fc} \\ &= -i_{lhc} + \frac{\hat{I}_{l1}}{2} \cdot e^{-t \frac{R_f}{L_f}} \quad \text{for all } \omega_i t \in (0, 2\pi/3] \end{aligned}$$

If the integration action in the PI controller is allowed to run and integrate this error signal, it will falsely accumulate a large positive value. Because an integration operation has some “memory” of past input values, this positive error will carry into the control signal when it becomes enabled again as the middle phase. Because of the limitation on controller bandwidth, the integral control cannot recover from this false signal very fast, and would therefore be issuing a false control signal during the mid and max-phase periods. It would take some time before this false control signal settles back to the correct control signal, but is then interrupted again when the phase becomes minimum. Therefore, the integrator must be disabled and forced to hold its previous state during the minimum phase for proper operation. This is the same result as if the error signal  $i_{fc,error} = 0$ .

### Why Not Use a $dq0$ Transformation?

Initially, it seems manageable to allow these zero sequence components to exist in the measured load currents, then transform into the  $dq0$  domain to extract the fundamental components  $i_s^*$  including the imbalance imposed by the 0-component  $i_{l0} = i_{residual}$ . In this case, the calculation of  $i_f^*$  would continue to generate the correct harmonic reference signals for the max and mid phase currents, and should be already aligned with  $i_{fc}$  during the minimum phase in order for  $i_{fc,error} = 0$ .

However, trying to manage this imbalance with the presence of  $i_{l0}$  is cumbersome and ineffective. Applying a 2nd-order IIR filter to  $i_{l0}$  doesn't have the same effect as

filtering the  $dq$ -components since the 0-component is not rotating in the synchronous frame. Therefore, extracting the correct  $i_f^*$  from the  $dq0$  signals is not straightforward. Furthermore, the measured currents have switching signals from the PWM operation of the converters, and any slight mismatch in measurement circuitry will still result in non-zero error for  $i_{fc,error}$ , again leading to accumulation of a false control signal in the integrator.

Entirely ignoring the 0-component will only give false DC values of the  $dq$  components, leading to an inaccurate estimation of the fundamental load current  $i_{l1}$  used for  $i_f^*$ .

To be sure that the minimum phase control signal is not being corrupted by false integrator accumulation due to pre-control correction or parasitic effects from 0-component processing, it is necessary to disable the integrator in all cases mentioned above to maintain best control tracking. This is a simple logic-based task for the FPGA controller. For the reasons listed here, it is computationally more efficient and straightforward to correct for the imbalanced load current measurements before the signal is used in the controller. With the integrator disabled during the minimum phase, the remaining control functionality behaves normally, allowing this minimally-switched active filter to correct for harmonic currents as accurately as conventional active filters.

### 3.2.2 Feedforward Signal for MSAPF

The feedforward term which adds the voltage at the point of common coupling  $v_{PCC}$  to the control signal should be changed when the dc-link negative terminal  $N$  is shared with the negative terminal of the active power filter. Recall from (3.1) the voltages that appear across the inductors are switched with respect to the line-to-minimum voltage of the particular phase of the filter. It is for this reason that the feedforward term for the control signal for any phase should be  $v_{s,ph} - v_{min}$ . For the case when phase- $c$  is minimum, for example, phase- $a$  should have a feedforward signal of  $v_{ac}$  and phase- $b$  should have a feedforward signal of  $v_{bc}$ . Including these terms improves the current controllability of the minimally-switched active filter.

An additional feedforward term is needed before the control signal is processed in a traditional pulse-width modulated converter to generate duty ratio signals for the gate pulses. The method for calculating duty ratios for the pulses is commonly done using

either Sine-PWM or Space-Vector PWM [2]. In each case, the desired pole-voltage of each leg of an inverter is added to a common mode voltage before being compared against the available DC-bus voltage for the modulation. This common mode voltage is used to ensure the full limits of the DC-bus are used symmetrically for positive and negative values of the pole-voltage waveform. For each case, the average common mode voltage is,

$$\bar{v}_{com} = \begin{cases} \frac{v_{cl}}{2} & , \text{ Sine - PWM} \\ \frac{v_{cl}}{2} + \frac{v_{mid}}{2} & , \text{ SV - PWM} \end{cases}$$

where  $v_{mid}$  is the middle of the three voltages generated by the inverter at any time.

The common mode voltage appears on each pole of the inverter, and consequently also biases the DC-bus of the inverter. So for example if Sine-PWM is used on a DC-bus with a voltage of  $V_{cl}$ , the negative terminal is  $-V_{cl}/2$  and the positive terminal is  $+V_{cl}/2$  with respect to the system ground.

Assuming Sine-PWM is used for the proposed active filter topology, it is contradictory to have the negative terminal  $N$  to be equal to  $-V_{cl}/2$ , since it is being latched to the minimum phase at all times through the rectifier. Therefore, the PWM block cannot add an additional common-mode voltage as is traditionally done. This can be accomplished by either neglecting to add this term in the PWM converter calculations, or  $-V_{cl}/2$  can be added as a feedforward term before the PWM block if the PWM algorithm is to remain unchanged.

Another way to consider these additional feedforward terms is that they are re-defining the common mode voltage for the active filter pole voltages, correcting for what the PWM converter is attempting to define for  $v_{com}$ . Put more simply, the common mode voltage that must be added to each phase of the controller signals is:

$$v_{com} = -v_{min} \tag{3.12}$$

so the desired voltage signal at the pole of the MSAPF is:

$$\bar{v}_{AF}^* = \tilde{v}_{AF} + v_{PCC} + v_{com} \tag{3.13}$$



where  $\tilde{v}_{AF}$  is the voltage signal at the output of the PI controller, reflecting the AC small signal disturbance around the steady-state operating point that is dominantly controlling the currents through  $L_f$ . On a per-phase basis when phase- $c$  is minimum, the voltage signals desired at each pole of the MSAPF are:

$$\begin{aligned}\bar{v}_{AF,a}^* &= \tilde{v}_{AF,a} + v_{ac} \\ \bar{v}_{AF,b}^* &= \tilde{v}_{AF,b} + v_{ab} \\ \bar{v}_{AF,c}^* &= \tilde{v}_{AF,c}\end{aligned}\tag{3.14}$$

When these signals are divided by the available DC clamp voltage  $V_{cl}$ , the three-phase duty ratios are calculated:

$$\begin{aligned}d_a &= \frac{\bar{v}_{AF,a}^*}{V_{cl}} = \frac{\tilde{v}_{AF,a}}{V_{cl}} + \frac{v_{ac}}{V_{cl}} \\ d_b &= \frac{\bar{v}_{AF,b}^*}{V_{cl}} = \frac{\tilde{v}_{AF,b}}{V_{cl}} + \frac{v_{bc}}{V_{cl}} \\ d_c &= \frac{\bar{v}_{AF,c}^*}{V_{cl}} = \frac{\tilde{v}_{AF,c}}{V_{cl}}\end{aligned}\tag{3.15}$$

The duty ratio calculated for phase- $c$  is of course ignored, since the active filter switch corresponding to the minimum phase is not switched, and hence cannot be controlled.

## Chapter 4

# Simulation

Simulation results are presented here for the direct-link drive system 3.1 with a PWM inverter driving an inductive load ( $R = 10\Omega, L = 10mH$ ). The model was built in Matlab® using the SimPower® toolbox of Simulink®. Simulation parameters are shown in Table 4.2, along with voltage and current measurements in Table 4.1. An additional damping resistor  $R_s$  needs to be connected in shunt to the source inductor  $L_s$  to dampen the LC resonance formed with the filter capacitors  $C_f$ . The input frequency  $f_i$  and output frequency  $f_o$  are the same. The peak value of the dc-link  $v_d$  is 294 V, so the clamp voltage must be regulated higher than this. The set point is chosen at 400 V.

As shown in Fig. 4.1 and Fig. 4.2, the total demand distortion (TDD) of the source current  $i_{sa}$  improves from 29.47% to 3.01%. The load currents  $i_l$  are measurements of the currents directly entering the rectifier. The filter capacitor  $C_f$  also draws some reactive currents from the source. This is the reason why the currents have a slightly leading

Parameter	Value
$v_{s,ph}$	120V (rms)
$i_{s,ph}$	8.6A (rms)
$v_{o,ph}$	106V (rms)
$i_{o,ph}$	9.7A (rms)
$f_i, f_o$	60Hz

Table 4.1: Voltage and Current

Parameter	Value
$L_s$	$3mH$
$R_s$	$8.8\Omega$
$C_f$	$16.4\mu F$
$L_f$	$1mH$
$C_{cl}$	$10\mu F$

Table 4.2: System Parameters

power factor, which is seen in  $i_{sa}$  superimposed with  $i_{la}$ . If power factor angle control was needed along with harmonic correction, then the filter currents can be adjusted to change this angle. The filter capacitors  $C_f$  also form a 2nd-order passive low pass filter with the source inductance  $L_s$ , which is necessary to filter out the high-frequency switching signals in the current. Since the frequency of these switching signals are high, these passive elements can be very small. Fig. 4.3 shows that the clamp voltage  $v_{cl}$  is being effectively regulated at 400 V. Fig. 4.4 shows the load current  $i_l$  in the  $dq$ -domain. Fig. 4.5 shows the duty ratio for the APF for phase- $a$ .

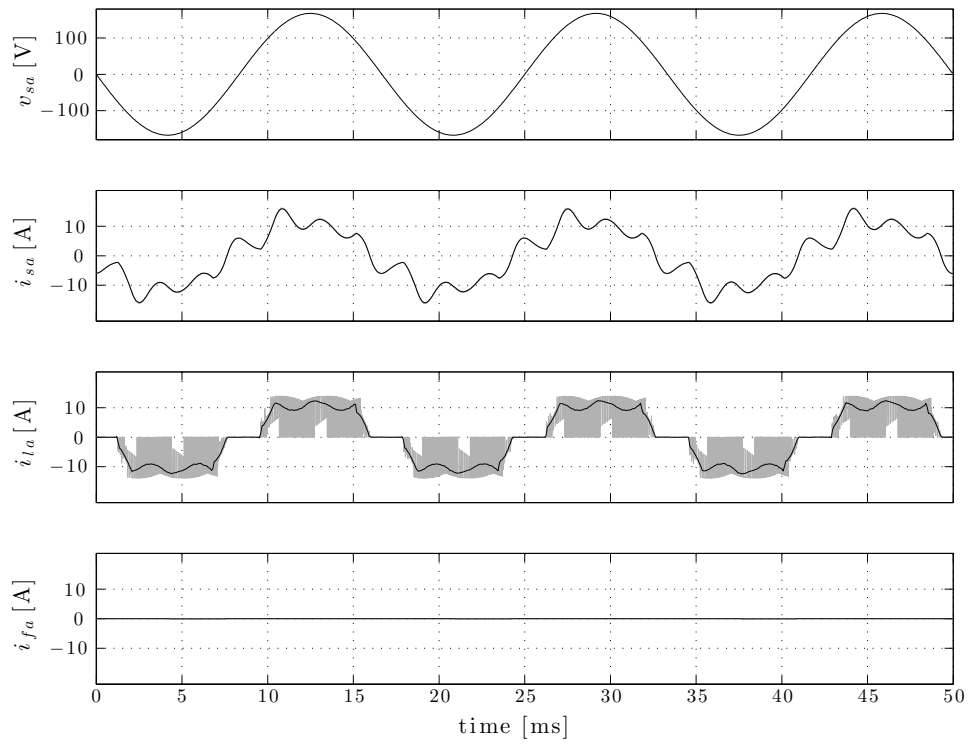


Figure 4.1: Input voltage  $v_{sa}$  along with the source current  $i_{sa}$ , the load current  $i_{la}$ , and the filter current  $i_{fa}$  when active filter is not operating. Signals plotted in gray include switching currents. Signals plotted in black are filtered with an 8th-order lowpass Chebyshev Type I filter at  $f_c = 5$  kHz. TDD of  $i_{sa}$  without APF is 29.47%.

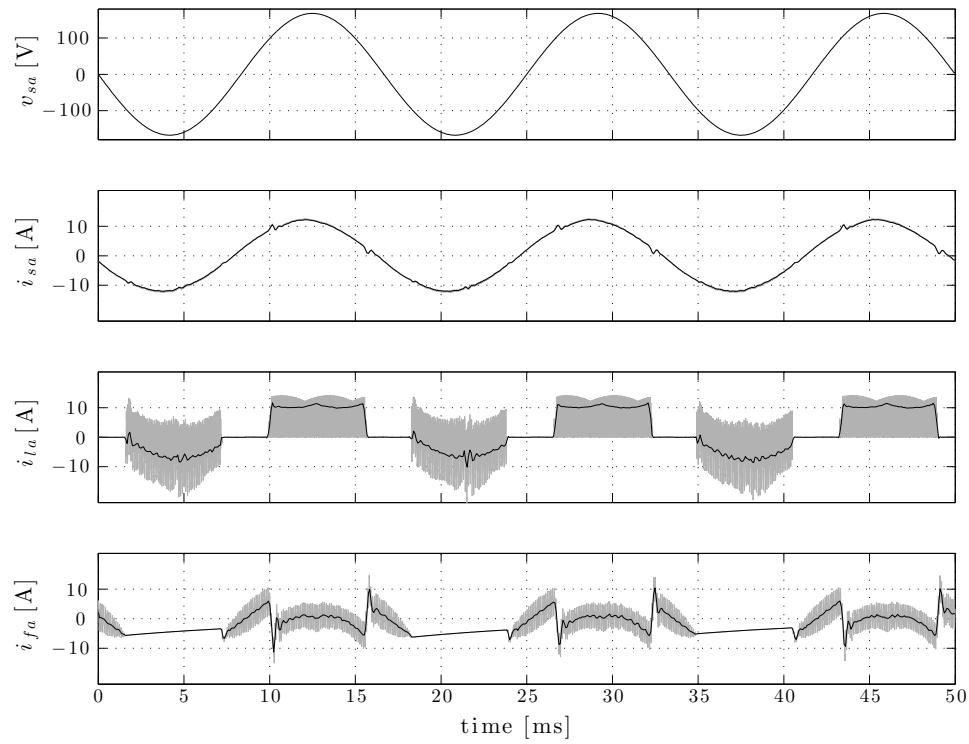


Figure 4.2: Input voltage  $v_{sa}$  along with the source current  $i_{sa}$ , the load current  $i_{la}$ , and the filter current  $i_{fa}$  when active filter is switching. Signals plotted in gray include switching currents. Signals plotted in black are filtered with an 8th-order lowpass Chebyshev Type I filter at  $f_c = 5$  kHz. TDD of  $i_{sa}$  with APF is 3.01%.

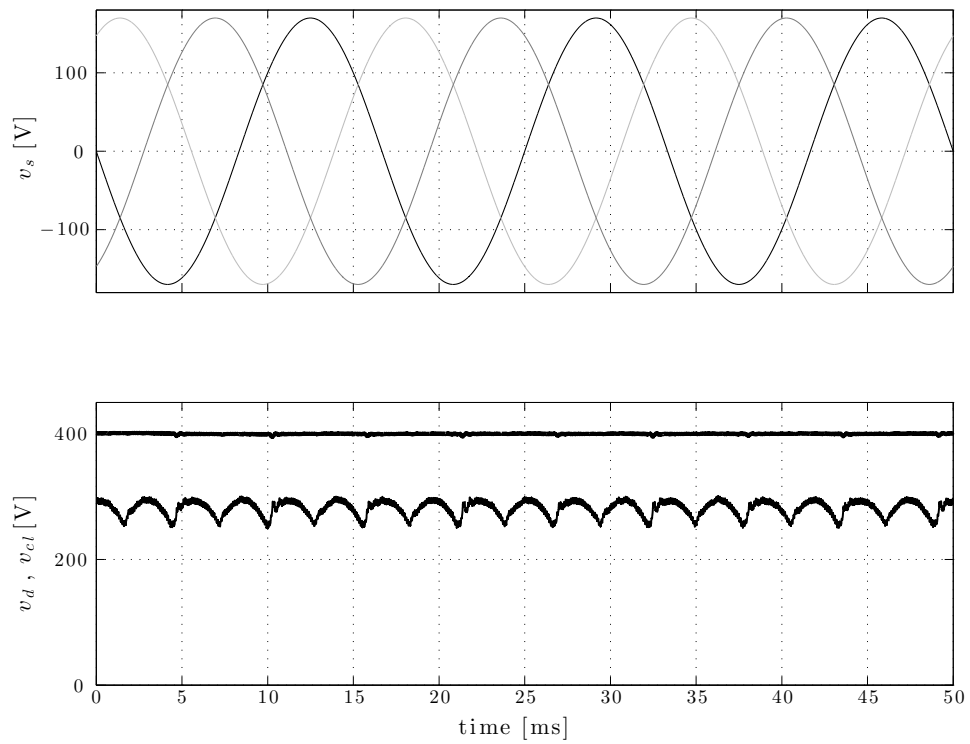


Figure 4.3: Input voltage  $v_{sa}$ ,  $v_{sb}$ , and  $v_{sc}$  along with clamp capacitor voltage  $v_{cl}$  which is regulated to 400 V, and the dc-link voltage  $v_d$  following the maximum instantaneous line-to-line voltage.

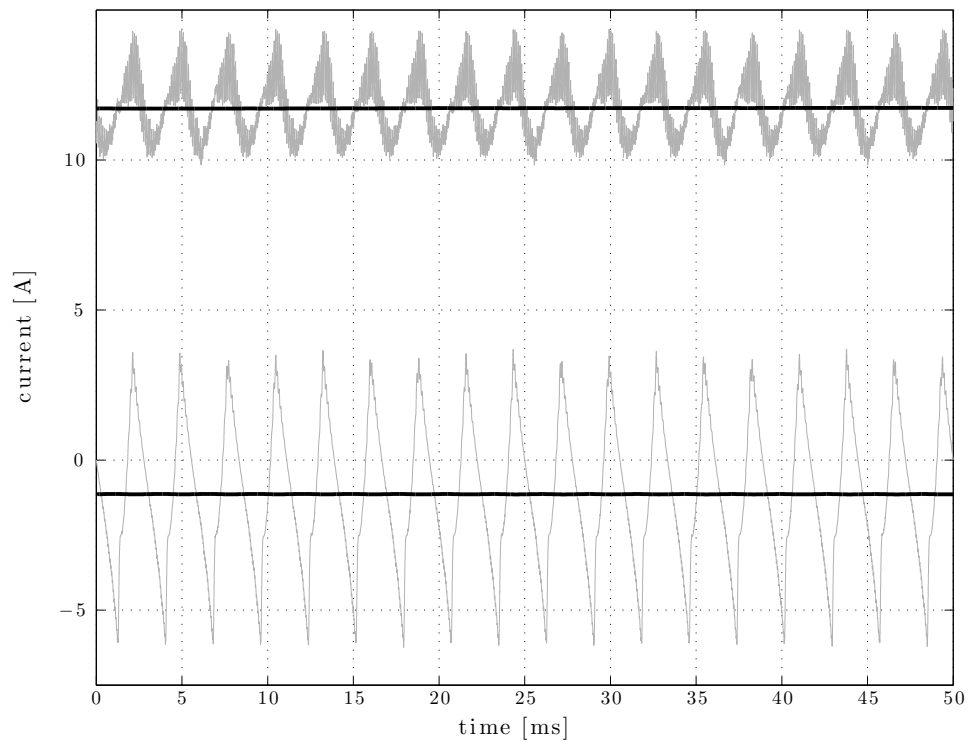


Figure 4.4: Load currents  $i_l$  in the  $dq$ -domain. The top graph shows the  $d$ -axis current  $i_{ld}$  in grey, with the DC value plotted in black. The bottom graph shows the  $q$ -axis current  $i_{lq}$  in grey, with the DC value plotted in black.

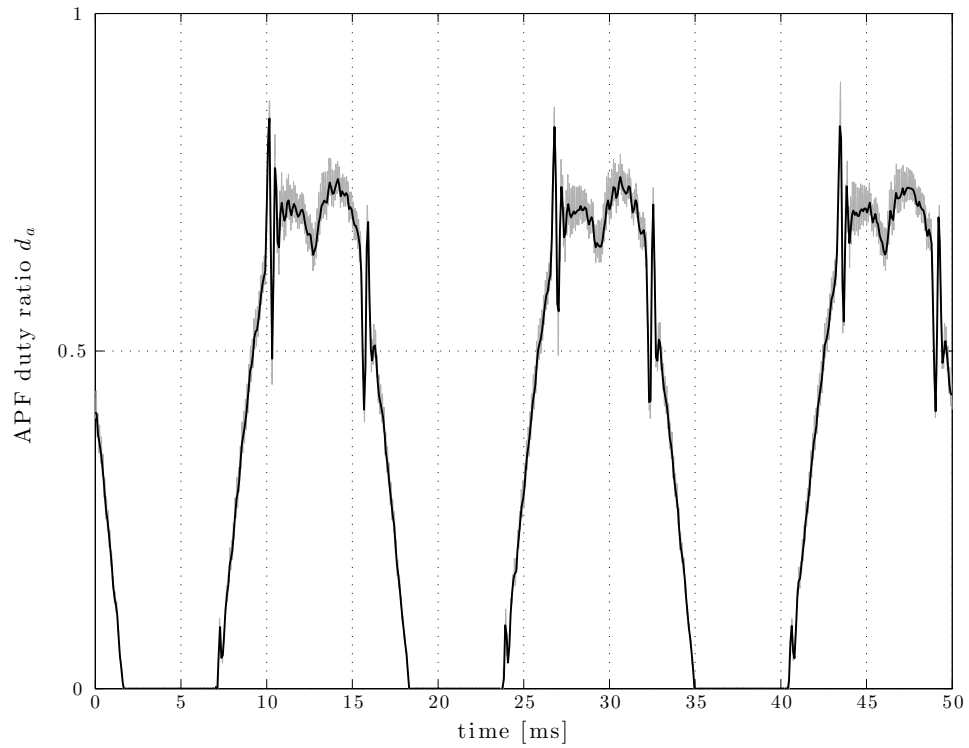


Figure 4.5: Duty ratio signal  $d_a$  for the minimally-switched active power filter. The signal plotted in gray includes switching signals, some of which cannot be avoided in the control signal. The signal plotted in black is filtered with an 8th-order lowpass Chebyshev Type I filter at  $f_c = 5$  kHz.



## Chapter 5

# Experimental Results and Discussion

Experiments were run using Microsemi IGBT power modules APTGT50TA60PG with Concept 6SD106E SCALE gate drivers for the rectifier and inverter stages. The active power filter was built using an integrated power hybrid IC IRAM136-3063B from International Rectifier. The gate signals and control system were coded and implemented on a XILINX Spartan XC3S500E FPGA platform. A photograph of the hardware setup can be seen in Fig. 5.1

The circuit parameters for the hardware tests are the same as the simulation as given in Table 4.2, but with a larger clamp capacitor of  $C_{cl} = 100\mu F$ . The operation of the minimally switched active filter were confirmed at various operating points and load conditions. The voltage and current of the testing conditions are given in Table 5.1 for an RL load and Table 5.2 for a motor load.

Testing was first done on a star-connected inductive RL load ( $R = 16.7\Omega, L = 30mH$ ). At the operating conditions listed above, a reduction in TDD from 27.36% down to 6.82 % was observed. Fig.'s 5.2 - 5.4 show these experimental results. The second set of testing was completed using a GE Energy Saver® NEMA Premium Efficiency 5KS215 induction motor. The motor was coupled to a DC motor used to provide load torque to the machine in order to generate significant load current through the direct link drive system. At the operating conditions listed above, a reduction in TDD from

29.39% down to 7.39 % was observed. Fig.'s 5.5 -5.6 show these experimental results.

## 5.1 Discussion

The harmonic content of each testing condition is given in Table 5.3, showing the amount of distortion in each harmonic bin as a percentage of the load demand current  $I_L$ . The MSAPF shows good control of low order odd harmonics, placing them well below the most strict limits specified in IEEE-519 in Table 1.1. Higher order harmonics are still not within the limits in some operating conditions. This is likely because of the high slew-rate of the rectifier load current  $i_l$  having higher harmonic content than the bandwidth of the controller. The controller bandwidth is limited as discussed in Section 2.1.1, so

Parameter	Value
$v_{s,ph}$	50V (rms)
$i_{s,ph}$	1.5A (rms)
$f_i$	60Hz
$v_{o,ph}$	35.4V (rms)
$i_{o,ph}$	2.1A (rms)
$f_o$	20Hz
$V_{cl}$	250V

Table 5.1: Voltage and Current of RL test

Parameter	Value
$v_{s,ph}$	50V (rms)
$i_{s,ph}$	2.2A (rms)
$f_i$	60Hz
$v_{o,ph}$	35.4V (rms)
$i_{o,ph}$	3.1A (rms)
$f_o$	20Hz
$V_{cl}$	250V

Table 5.2: Voltage and Current of motor test

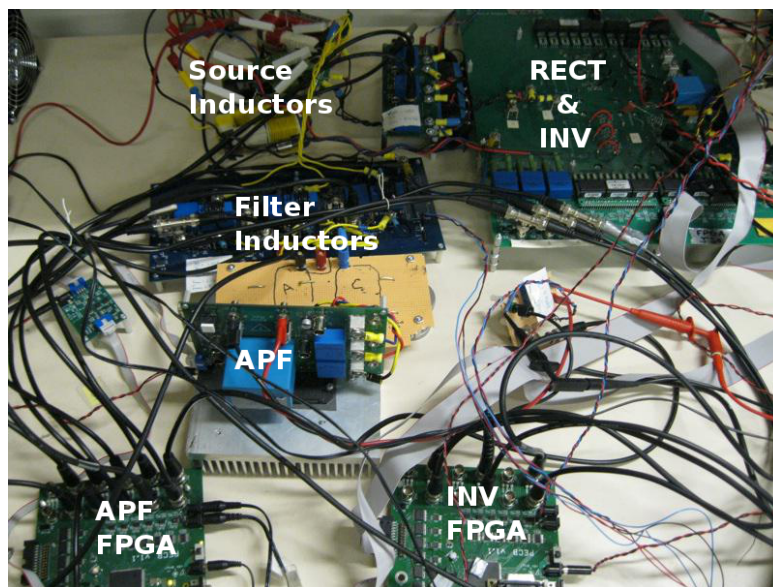


Figure 5.1: Hardware Setup

higher order harmonics are not within the controllable range of the current controller. This may be alleviated by inserting an inductor in the path for  $i_l$  as is done in many conventional active filters [4]. This inductor would limit the slew rate of the current, effectively applying a low-pass filter effect and removing high frequency harmonics with passive components. However, this would increase the number of passive components and would require an additional capacitor at the rectifier to keep the switching currents from generating large voltage spikes across the IGBT devices.

Another interesting observation is that the MSAPF is successfully controlling odd order harmonics to be lower than the most strict harmonic requirements. However, some even order harmonics are generated which are highly undesirable on their own and become a significant contributor to the TDD calculation. For example, the odd order harmonics present in motor test alone have a specific TDD of 3.92%, though when including even order harmonics the total TDD is 7.39%. Even order harmonics in a signal have the effect of asymmetric wave shapes, meaning the source current  $i_s$  is not completely symmetric. Though this is not ideal, the result is not too surprising since the essence of the MSAPF is that the lower portion of the wave (during the minimum phase period) is not being actively switched, and being corrected indirectly through the

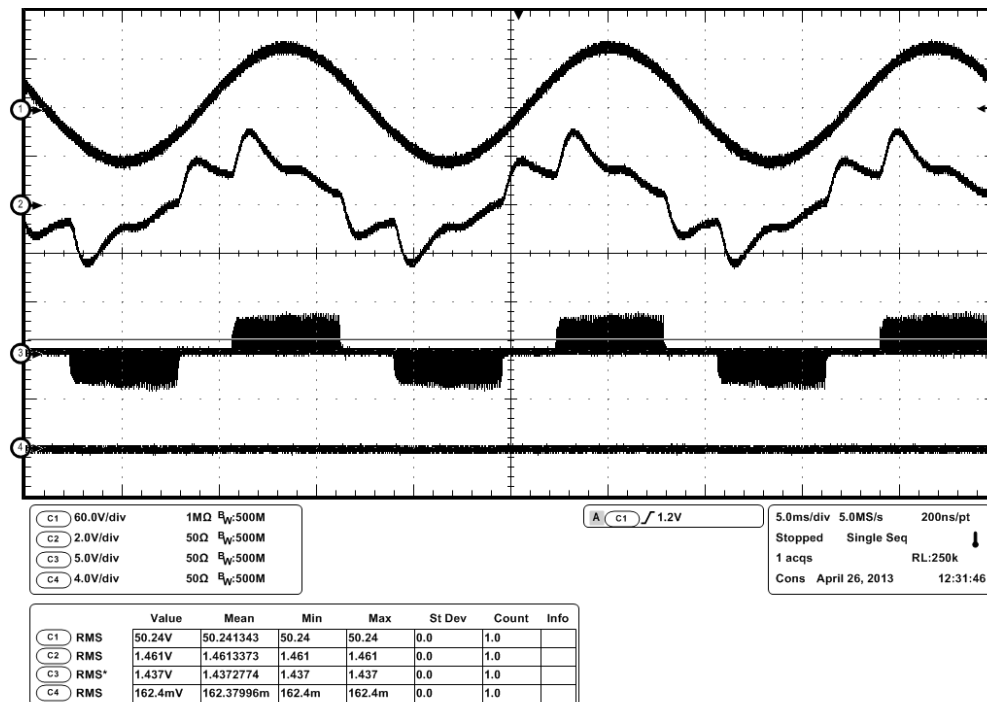


Figure 5.2: Experimental results of direct link drive system without active filtering, using an RL load. Plots 1-4 are  $v_{sa}$ ,  $i_{sa}$ ,  $i_{la}$ , and  $i_{fa}$  respectively. TDD = 27.36 %.

maximum and middle phase control signals. Identifying the precise cause and solution to the presence of even-order harmonics is a topic of further research.

Lower device ratings may be achieved if this topology is constructed using a Hybrid Active Filter, incorporating some series passive elements to filter some of the lowest harmonic frequencies [8]. This effectively reduces the DC-voltage requirements of the VSI, lowering the device ratings of the IGBT switches. However, when using the clamp capacitor as the voltage source, the requirement to keep the clamp voltage higher than the DC link voltage would not allow a lower voltage rating, which is one of the primary benefits of hybrid active filters.

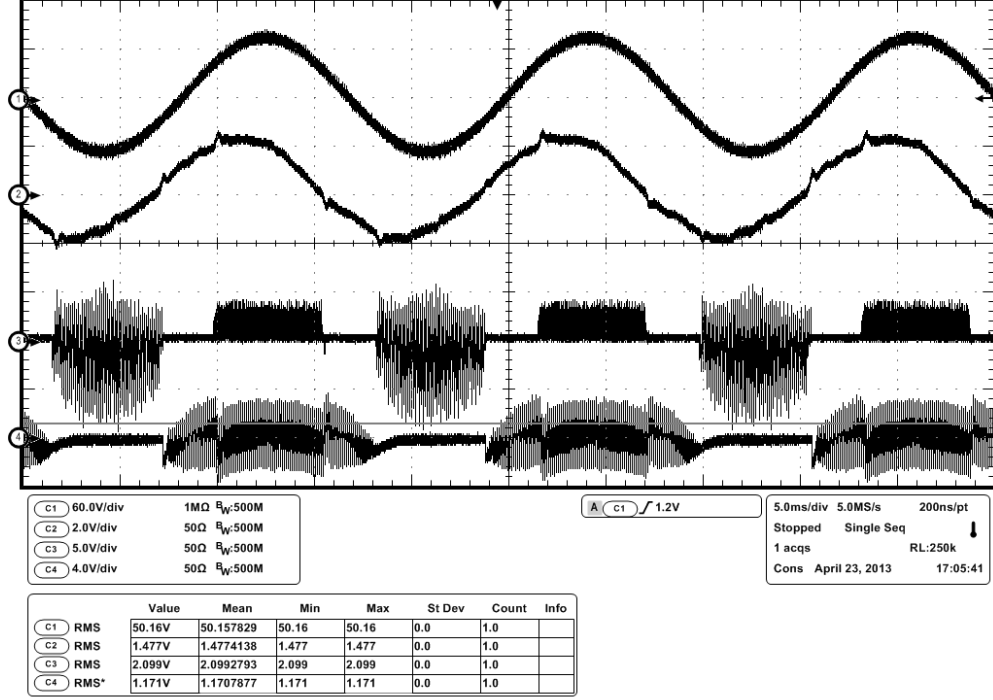


Figure 5.3: Experimental results of direct link drive system with minimally switched active filtering, using an RL load. Plots 1-4 are  $v_{sa}$ ,  $i_{sa}$ ,  $i_{la}$ , and  $i_{fa}$  respectively.  $TDD = 6.82\%$ . Note that during the minimum cycle of  $v_{sa}$ ,  $i_{fa}$  is not switched and the measured load current  $i_{la}$  has residual currents superimposed.

Harmonic Current Distortion in Percent of $I_L$							
Individual Harmonic Order (Odd Harmonics)							
Load	APF	$< 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	$TDD$
RL	OFF	26.4	6.7	2.6	1.3	0.4	27.4
RL	ON	3.3	2.1	1.8	2.2	1.4	6.8
IM	OFF	28.7	5.7	1.5	0.5	0.3	29.4
IM	ON	2.8	1.7	1.3	1.5	0.9	7.4

Table 5.3: Harmonic results of experimental data.

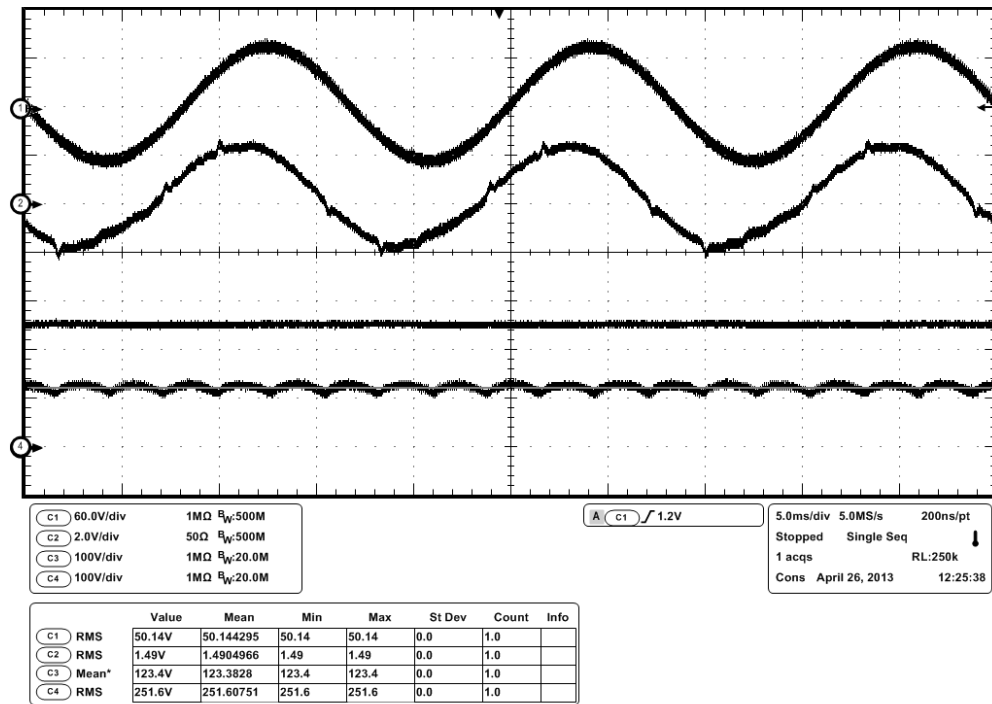


Figure 5.4: Experimental results of direct link drive system with minimally switched active filtering, using an RL load. Plots 1-4 are  $v_{sa}$ ,  $i_{sa}$ ,  $v_d$ , and  $v_{cl}$  respectively. The clamp voltage  $v_{cl}$  is seen to be controlled to 250V.

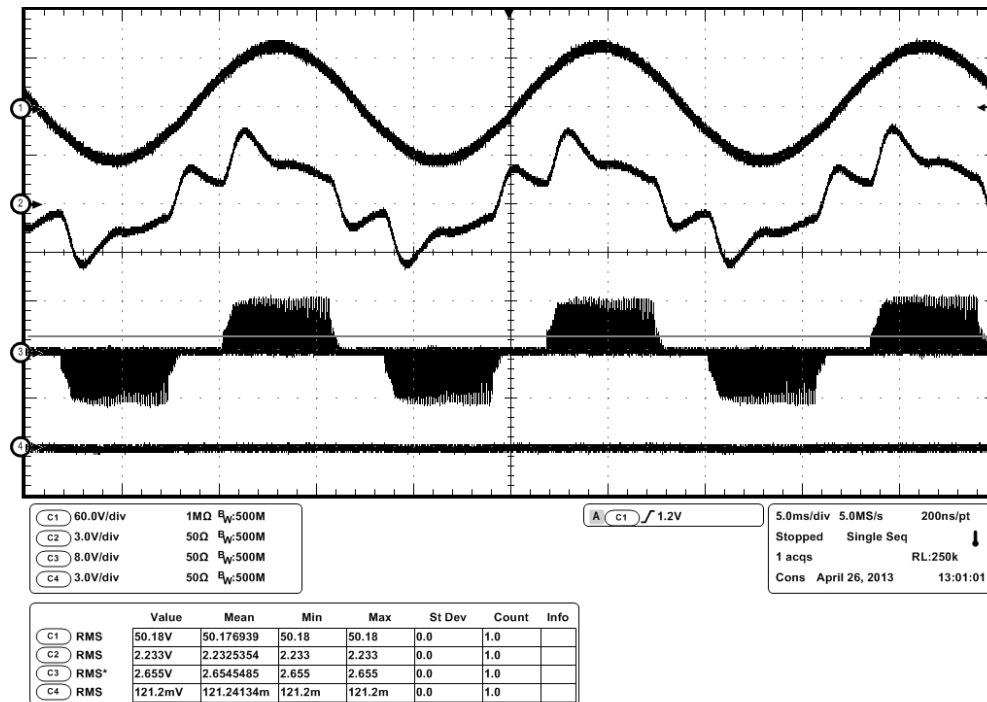


Figure 5.5: Experimental results of direct link drive system without active filtering, using a motor load. Plots 1-4 are  $v_{sa}$ ,  $i_{sa}$ ,  $i_{la}$ , and  $i_{fa}$  respectively. TDD = 29.39 %.

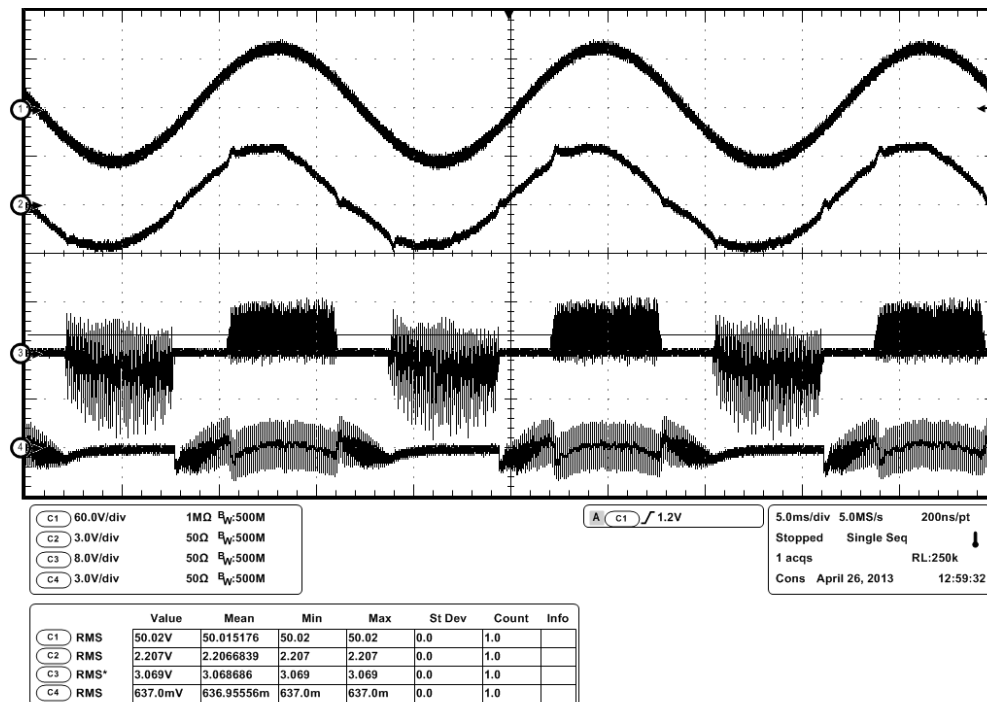


Figure 5.6: Experimental results of direct link drive system with minimally switched active filtering, using a motor load. Plots 1-4 are  $v_{sa}$ ,  $i_{sa}$ ,  $i_{la}$ , and  $i_{fa}$  respectively.  $TDD = 7.39\%$ . Note that during the minimum cycle of  $v_{sa}$ ,  $i_{fa}$  is not switched and the measured load current  $i_{la}$  has residual currents superimposed.



## Chapter 6

# Conclusion

This thesis has covered some of the fundamental issues of harmonic distortion generated by common power electronic converters. It has been shown that the deleterious effects of this distortion can be mitigated by the use of active power filters, which are controlled in a closed-loop feedback system to correct for unwanted harmonics. Conventional active filters are well understood and gaining popularity due to reduced device costs and availability.

The proposed minimally-switched active power filter using the clamp capacitor has shown to have improvements in efficiency as compared to conventional active power filters. Some of the highlights of the new topology include:

- A PWM inverter controlled with linear PI control, using a constant switching frequency.
- Reduced switching losses from IGBT switching transitions.
- Reduced components, utilizing a common DC capacitor shared from the clamp circuit on the dc-link of the direct-link drive system.

Simulation testing and experimental results confirm the viability of this active filter topology. This can have many applications in AC/DC converters, motor drive systems, or any other converter that uses a front end converter operated as a rectifier bridge which generates square-wave currents. One particularly promising application is in the use of open-end winding drive systems for AC machines [9]. In these drive systems,

improvements are seen in superior voltage gain performance and common mode voltage rejection, though the input currents are not controlled and thus have large harmonic distortion. Using such open-end winding drive systems, coupled with this minimally-switched active power filter, provide an elegant all-around solution for a drive system in any motor drive or wind-generation application utilizing such AC machines.

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