Printed Electrolyte-Gated Transistors and Circuits for Flexible Electronics

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To my mother, father and husband.

Abstract

Printed electronics has broad potential applications due to its low fabrication cost, compatibility with flexible substrates, and its suitability for applications where large footprints are required. However, the supply voltages of printed circuits are high in general due to limitations of both the electronic properties of printable materials and the coarse dimensions of printed transistors. This thesis aims to demonstrate low-voltage operation of printed circuits by employing a printable electrolyte, a so-called ion gel, with very large specific capacitance (on the order of $\mu F/cm^2$) as the gate insulator. Ion gels are composites formed by the self-assembly of triblock copolymers, e.g. poly(styrene-b-methyl methacrylate-b-styrene) (PS-PMMA-PS), in an ionic liquid, e.g. 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide ([EMI][TFSA]). These ion gels and other functional materials, such as semiconductors and conductive polymers were fabricated by aerosol jet printing to form electrolyte-gated transistors (EGTs) and circuits on plastic substrates. This thesis demonstrates that these printed devices can achieve low-voltage operation, fast switching speed, remarkable operational stability, and can realize electronic functions of logic gates, capacitor, electrochromic device, etc.

To explore the trade-off between supply voltage and switching speed, this thesis studied EGTs consisted of high capacitance ion gel and high mobility carbon nanotubes (CNTs), which together enable the fast switching speed at low voltages. The CNT EGTs were ambipolar and could be used to make complimentary-like inverters and circuits. Five-stage ring oscillators printed on flexible substrate achieved above 2 kHz frequency,

corresponding to less than 50 μs delay time. The impact of key parameters on delay times were studied, including the EGT channel length, ionic conductivity of the ion gel, parasitic capacitance and resistance. With these understandings, the architecture of EGT was optimized, and ring oscillators with stage delay as short as 1.2 μs time was successfully demonstrated at voltages < 3 V. These results represent a significant improvement in the performance of printed electronics. Fabrication and characterization of inverters and NAND gates, device operational stability and power consumption were also discussed.

To demonstrate integration of EGTs, a flexible circuit with 23 EGTs, 12 capacitors, 20 resistors and an electrochromic (EC) display pixel operates at a voltage as low as 1 V was fabricated on plastic substrates. All of the key components were aerosol jet printed from liquid inks, such as the ion gel, poly (3-hexylthiophene) (P3HT), a semiconductor, and the conductive polymer, poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS). Characteristics and operation mechanisms of each device were discussed respectively. The circuit operated continuously for 100 min with no degradation. Overall, this thesis demonstrates that high reproducibility of device fabrication is possible and that EGTs may be used to achieve conventional electronic function at low voltage on plastics.

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Chapter 1 Introduction

1.1 Motivation

Microelectronics based on silicon crystals and compound semiconductors has had significant impacts on technology over the last half century. The circuit performance and integration density continuously increase due to the scale-down of device dimensions. However, challenges remain in certain areas, e.g., the integration of electronics onto flexible plastic, paper, or metal substrates. Envisioned applications of flexible electronics include roll-up displays, wearable energy-harvesting system, electronic sensors for robots (e-skins), sensors for biological system (bionic ears), etc. Fabrication of conventional electronics, which usually requires high temperatures up to several hundreds of degrees (ion implantation, contact annealing, etc.), is incompatible with most flexible substrates. Furthermore, many process steps in conventional semiconductor industry are intrinsically difficult to be adapted to large-area fabrications, as required for the large area displays, such as photolithography and vacuum deposition processes.

Amorphous silicon was first studied to address these challenges, especially for the large-area applications, but the process temperatures are still relatively high (> 200 °C) and not compatible with most plastic substrates. Some groups have demonstrated flexible circuits based on very thin silicon stripes transferred to flexible substrates using state-of-art fabrication techniques (transfer printing or pick-and-place methods),[1] and these Si based circuits benefit from superior electronic properties.

Organic materials, including semiconducting, insulating and conductive materials, have received intensive attention because they are naturally flexible and compatible with low-temperature, low-cost (solution processable) fabrication. Over the last few decades, organic thin film transistor (OTFT) backplane of active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diodes (AMOLEDs) were reported by many research groups and companies.[2-4] OTFTs fabricated on flexible substrates were also demonstrated in applications such as e-skins, large area sensors, disposable sensor tapes, radio-frequency identification (RFID) tags, and smart objects.[5-15] The technologies used in these flexible electronics are still mostly conventional evaporation and photolithography. Although they are adaptable to flexible substrates, low-cost and large area fabrication is still challenging.

An alternative option for achieving flexible electronics is to employ graphic arts methods such as flexographic, gravure or ink jet printing to pattern metallic, semiconducting, and insulating inks onto foils and paper.[16-21] Liquid phase printing offers the potential for high throughput roll-to-roll (R2R) or sheet-to-sheet processing of electronics on large area substrates. In addition, additive printing from functional liquid inks is promising for cost-effective electronics, such as disposable or portable applications. For example, a flexible, all printed, 1-bit RFID tag was demonstrated recently by mass-printing techniques with estimated cost of 3 cents.[9]

Of the many technical challenges facing printed electronics, one of the most fundamental is the trade-off between supply voltage and operating speed, which is not only limited by the intrinsic material properties, but also the device architecture and

dimensions. Organic semiconductors generally have relatively low mobilities compared to conventional semiconductors, and transistors based on which often require operation voltage > 10 V. The printed transistors require even higher voltage (tens of volts), due to the limitations of printing resolution and large source-to-drain channel. The large voltages are not practical for many potential applications of flexible electronics where power will be supplied by thin film batteries or radio-frequency fields. Meanwhile, the operation speed of the printed circuit is also much lower. The typical delay time in organic circuits is on the order of 10 μs, while in printed circuits is generally around ms.

A barrier to low voltage printed electronics is the low capacitance of many printed gate dielectrics (i.e., the printed gate dielectric layers are too thick and their dielectric constants are too small), which necessitates larger gate voltages to switch the transistors. Many groups explored different strategies to address this issue, including using dielectrics with high κ, very thin dielectric layer (such as self-assembled monolayer), and electrolyte, and successfully reduced the operational voltages.[22-27] Another direction to improve the performance of printed circuits is to employ high mobility semiconductors. Some groups are investigating transfer printing[1,28-32] or jet printing[9,33-38] of high mobility semiconductors, e.g., silicon, oxides, nanowires, graphene and carbon nanotubes (CNTs), and these efforts have the potential to produce low voltage circuits operating at high speed.

This thesis combines both strategies, by employing high mobility carbon nanotubes and high capacitance electrolyte ion gel, and demonstrates printed, flexible circuits which

achieve both low supply voltage and high speed. Both CNT and ion gel were patterned by aerosol jet printing of liquid inks. Ion gel-gated CNT thin film transistors (TFTs) with 50 μm channel lengths display ambipolar transport with both electron and hole mobilities > 20 cm^2/Vs; these devices form the basis of printed inverters, NAND gates, and ring oscillators on both polyimide and SiO_2 substrates. Five-stage ring oscillators achieve frequencies > 2 kHz at supply voltages of 2.5 V, corresponding to stage delay times of 50 μs. The data was first reported on ACS Nano, 2011, which represented a substantial improvement for printed circuitry fabricated from functional liquid inks.

In order to understand the limitations of the operation speed in electrolyte-gated transistors and circuits, and further improve the circuit performance, the impacts of device architecture and materials properties are studied. The inverter delay time decreases as the channel length scaling down. And the ionic conductivities of ion gel also have a strong effect on the delay time. The higher the ionic conductivity the gel has, the faster the transistor can switch. With these understandings, an 83 kHz ring oscillator (with stage delay time ~ 1.2 μs) is successfully demonstrated, based on transistors with 5 μm channel length. The result is published in Nano Letters, 2013. With further optimization of device architecture, achieving 1 MHz printed ring oscillators is possible.

Furthermore, this thesis explores the applications of electrolyte-gated devices. The printed electrolyte-gated polymer OTFTs has been demonstrated by our group previously.[24,25] With similar materials and architecture, electrolyte-gated capacitors and electrochromic (EC) display pixels are fabricated by printing as well. All of components

are printed on a PET substrate to form a driving circuit integrated with EC display. Characteristics of each component are studied. The circuit can operate at a voltage as low as 1 V, and output a large current which is high enough to switch the mm^2 size EC display pixel. The novelty of this work lies in (1) the use of aerosol jet printing to produce a functional circuit containing 68 individual devices (e.g., transistors, capacitors, resistors, etc.) with good reproducibilities, (2) the integration of a printed EC pixel onto the same substrate using the same printing methodology, and (3) the very low voltage operation of the complete assembly.

1.2 Review of the Thesis

Chapter 2 introduces the theories of charge carrier transport in organic semiconductors, the architecture and operation mechanism of organic thin film transistors. In addition, the operation mechanism and characteristics of electrolyte-gated transistors (EGTs) are discussed. Applications of electrolytes in flexible electronics are reviewed.

Chapter 3 briefly introduces the structure and electronic properties of carbon nanotubes, as well as the common growth and fabrication methods. The electronic devices based on the carbon nanotubes are reviewed additionally.

Chapter 4 focuses on the fabrication of flexible and printed electronics. First, common methods of fabricating flexible transistors and circuits are introduced. The printing methods are reviewed in details in an individual section. The last section summarizes the circuit performances of organic circuits and printed circuits, i.e. the delay time vs. supply

voltage, which is one of the major focuses of this thesis. Research in complementary circuits and other applications, such as displays and RFIDs, are also reviewed.

Chapter 5 shows the study on printed, flexible circuits based on electrolyte-gated CNT transistors. Following with the introduction of fabrication method and characteristics of transistors, the performances of digital circuits, including inverters, NAND gate, and ring oscillators are discussed. The parasitic capacitance and operation stability of the circuits are studied in addition. These results have been published as "Printed, Sub-3V Digital Circuits on Plastic from Aqueous Carbon Nanotube Inks", M. Ha, Y. Xia, A. A. Green, W. Zhang, M. J. Renn, C. H. Kim, M. C. Hersam and C. D. Frisbie, *ACS Nano*, 4, 8, 4388-4395.

Chapter 6 discusses the factors that affect the speed of the electrolyte-gated CNT circuits, and how to further improve the circuit performance. The effects of scaling down the transistor dimension and electrode dimension are demonstrated. The output characteristics of inverter based on the ambipolar transistors are discussed. The stage delay time of inverters are characterized with various channel lengths, and the ionic conductivities of electrolytes. Ring oscillators with delay time less than 5 μs were demonstrated. These results have been published as "Aerosol Jet Printed, Low Voltage, Electrolyte Gated Carbon Nanotube Ring Oscillators with Sub-5 μs Stage Delays", M. Ha, J. T. Seo, P. L. Prabhumirashi, W. Zhang, M. L. Geier, M. J. Renn, C. H. Kim, M. C. Hersam, and C. D. Frisbie, *Nano Letters*, 13, 3, 954–960 (2013)

Chapter 7 summarizes the studies on applications of electrolyte-gated devices, including transistors, capacitors and EC displays. Characteristics of each component are discussed respectively. All components are integrated on a PET substrate and can switch a mm^2 size EC pixel at 1 V. The circuit performance and stability are discussed. These results are in preparation for submission as "Aerosol Jet Printed, 1-Volt Drive Circuit on Plastic with Integrated Electrochromic Pixel".

Chapter 8 discusses the future research directions of printed circuits. The power consumption issue of ambipolar circuits is discussed, with proposals of how to reduce the power consumption and some preliminary data. In addition, other applications of printed devices are discussed. In particular, a memory array based on printed capacitors based on electrolyte and polymer semiconductors is demonstrated, which results have been published as "A 1V printed organic DRAM cell based on ion-gel gated transistors with a sub-10nW-per-cell Refresh Power", W. Zhang, M. Ha, D. Braga, M. J. Renn, C. D. Frisbie and C. H. Kim, *Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, *2011 IEEE International*, 326-328, (2011)

Chapter 2 Organic Thin Film Transistors and Applications

The organic semiconductors include carbon-based small molecules and polymers. Studies of these materials date back to early 20th century,[39] and the distinct electronic and optical properties of organic molecules attracted many researchers since then.[40-42] In 1977, the discovery of the charge transport in conjugated polymers opened up new research directions in this field. Alan Heeger, Hideki Shirakawa, Alan McDiarmid were awarded the Nobel Prize in Chemistry, 2000, for this work.[43] Organic materials also offer vast opportunities of tuning their electronic and optical properties by molecular engineering. In addition, they are naturally flexible and compatible to solution process or low-temperature fabrication, which makes them very attractive candidates for flexible electronics. Many promising progress has been demonstrated in flexible electronics over the past decades.

This chapter starts with introducing the charge carrier transport theories in organic semiconductors. Then, the architecture and operation mechanism of the organic field effect transistor (OFET), the basic building block of organic circuits, is discussed. In addition, a unique type of transistors, electrolyte-gated transistor (EGT) is also discussed.

2.1 Charge Transport in Organic Semiconductors

Due to the large size of the molecule and long intermolecular distance in organic semiconductors, the forces between molecules are weaker than the covalent bonds in inorganic semiconductors. In organic semiconductors, the conduction bands are narrower, the charge transfer is not as efficient, thus the charge carrier mobility is lower. For example, the hole mobility of rubrene single crystal can be up to 20 cm^2/Vs,[44] which is among the highest mobilities of organic semiconductors. However, this is still orders of magnitude lower than the mobility of typical doped silicon which is around 10^3 cm^2/Vs. To understand this difference, this section discusses the theories of charge transport in organic semiconductors. The formation of energy levels, the concept of band-like transport, polarons and phonon-assisted hopping, the nearest-neighbor hopping and variable range hopping (VRH) models are reviewed.

2.1.1 HOMO and LUMO Energy Levels

Conjugated organic semiconductors are compounds consisting of sp^2 hybridized carbon atoms. The hybridization of orbitals $2s$, $2p_x$ and $2p_y$ creates three σ bonds, which link a carbon atom to its neighbors. The remaining $2p_z$ orbital forms a π bond. The π orbitals lie above and below the plane of carbon atoms and have significantly less overlap than the σ orbitals. Figure 2.1 shows the atomic π orbital (left), the lowest energy of π molecular orbitals (right above), and delocalized π orbitals (right bottom) of a benzene molecule. The positive and negative signs represent the two phases of the π orbital. Since

the π bond is weaker than σ bond, the delocalized π electrons can transport in these π states. The conjugated organic materials thus can be conductive or semiconducting.

Using the linear combination of atomic orbitals (LCAO) theory, one can calculate the wavefunction of the π-electron in bonding and anti-bonding states, respectively. The bonding states have lower energy than the anti-bonding states, therefore they are energetically favored. In organic materials, the bonding and anti-bonding states are referred as highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). The HOMO and LUMO levels of an isolated ethylene molecule are shown in Figure 2.2 (left). When two ethylene molecules are brought to each other in a cofacial configuration, the LUMO level and the HOMO level will split due to the interactions between states Figure 2.2 (middle). A large number of ethylene molecules stacking closely will result further splitting and eventually create the LUMO and HOMO band, as shown in Figure 2.2 (right).

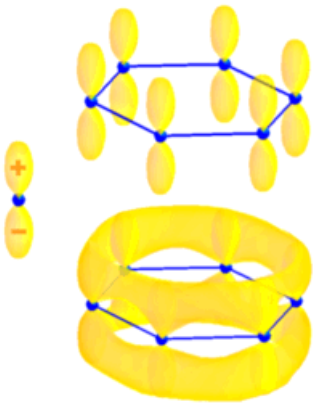

Figure 2.1 A schematic of σ and π Bonds. The blue lines are σ bonds and the yellow clouds are π bonds.

The width of the splitting energy levels is in proportion to the transfer integrals:

$$t = \sum_i \int \varphi^* (r_i) H_{0i} \varphi(r_0) dV \quad (2.1)$$

where φ is the wavefunction of an electron, and H is the Hamiltonian which describes the electron-lattice interaction. Equation 2.1 indicates a strong electron-lattice interaction will result in large transfer integrals, thus wider bands. For example, in silicon crystal, the strong covalent bonds lead to a band width of approximately 12 eV. However, the intermolecular force in organic materials is much weaker and the width of energy bands in organic semiconductors is only around 1 eV.

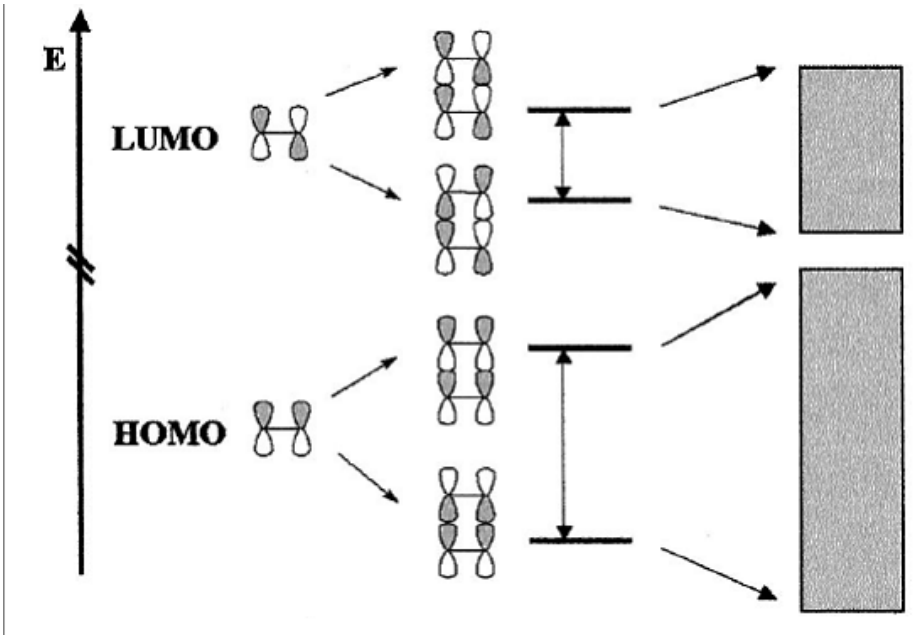

Figure 2.2 The bonding-antibonding interaction between the HOMO and LUMO levels.[45]

2.1.2 Electron-lattice Interaction and Polarons

The transport mechanism is usually divided into two regimes: band-like and hopping transport. Generally, the electron-lattice coupling strength determines which mechanism is dominant. A quantitative analysis suggested by Kao and Hwang compares the electron relaxation time τ, the intermolecular vibration period τ_{vl} and the intramolecular vibration period τ_{vn}.[46] The vibration periods are typically 10^{-12} s for intermolecular modes and 10^{-14} s for intramolecular modes. If $\tau < \tau_{vn} < \tau_{vl}$, that means the electron motion is rapid enough so that both vibrations can be ignored or treated as a perturbation. Thus, the electron can be considered as delocalized, traveling through the lattice as a wave, shown in Figure 2.3, corresponding to the band transport in section 2.1.3.

The second case is $\tau_{vn} < \tau < \tau_{vl}$, which indicates that the intramolecular vibration is faster than the electron motion. In this case, the electron stays on a lattice site long enough that the molecules have enough time to relax to a new equilibrium position. This leads to the formation of a *polaron*. If the spatial extension of a polaron is large compared to the lattice constant, the polarization of the lattice can be treated as a continuum.[47,48] This is *Fröhlich polaron*, which refers to the long range interactions. If the polaron has the size on the order of the lattice constant, it is called *Holstein polaron*, which refers to the short range interactions.[49]

The idea of the transport of small polarons was proposed by Yamashita and Kurosawa in 1950s,[50] and developed by Holstein and Emin[49,51,52] to describe the conduction of the

materials with low mobilities. Silinsh and Capek discussed in details about the polarization in organic solids.[53]

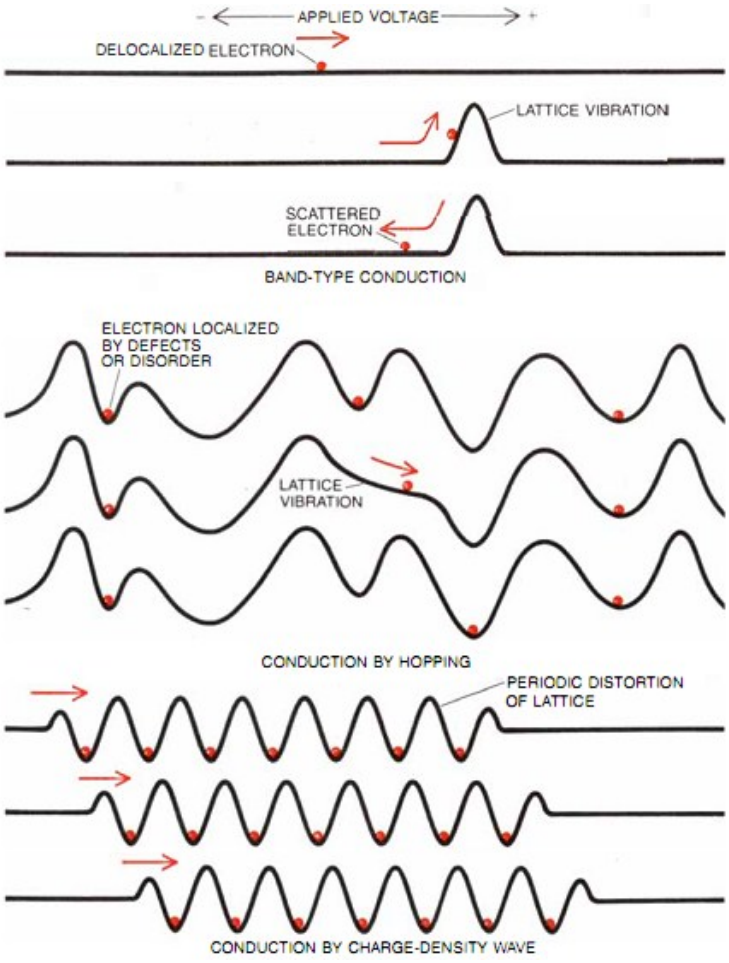

Figure 2.3 Band and Hopping Transport. [54]

Figure 2.4 illustrated the formation of electric dipoles caused by a positive charge trapped in a molecule.[55] Due to the Coulomb effect, the π-electrons of the surrounding lattice sites are attracted toward the center site where the positive charge sits. The polaron can also include a lattice deformation effect if the interaction is strong. Since the lattice

relaxation is faster than the electron's motion, one can consider the hole hopping in a way that the heavy polaron jumps with it, which requires a large activation energy and usually involves the emission and absorption of multiple phonons. The nature of phonon-assisted process is shown in Figure 2.3 schematically.

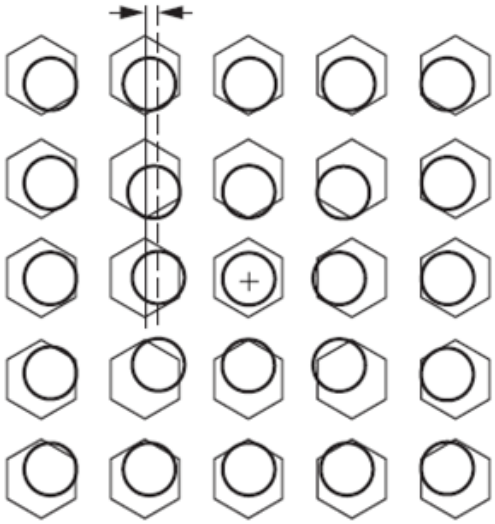

Figure 2.4 A schematic of positive charge induced polaron.[55]

2.1.3 Models of Charge Carrier Transport: Band vs. Hopping

Band Transport. In solid state physics, band theory has been well established and employed to explain various materials properties, especially the electronic properties. Atoms in a highly pure crystalline material (bulk) have long range order of the lattice structure. The periodic lattice forms periodic potential wells due to the Coulomb interaction between electrons and ions, in which electrons are only allowed to have certain states.[56] An electron wavepacket is *allowed* to propagate inside the bands, and

forbidden in the band gaps. Energy bands and band gaps can be explained quantitatively by solving the time independent Schrödinger equation.

An energy band gap on the order of electron volts gives the semiconductor material an electrical conductivity between those of metal and insulator. In semiconductors, the intrinsic conductivity and carrier concentrations are mostly controlled by the energy gap, E_g/k_BT. A smaller energy gap will induce higher concentration of intrinsic carriers and higher conductivity.[57] The material property of optical absorption usually gives the value of the energy gap. The threshold of continuous optical absorption at frequency of ω_g determines the band gap $E_g = \hbar\omega_g$. Another way to characterize the energy gap experimentally is to measure the temperature dependence of the conductivity or of the concentration of the carrier density in the intrinsic range, which can be obtained by the Hall Effect measurement.

The highest energy band filled with electrons at the absolute zero temperature is called valence band (HOMO); the energy band lies upon the valence band, where excited electrons can transport, is called conduction band (LUMO). At a finite temperature above absolute zero, electrons can be excited by a thermal activation energy and jump into the conduction band. The empty states they leave behind are called holes, carrying positive charges. Both electrons and holes are able to move under an applied electric bias thus create a current. Figure 2.5 shows the allowed electron states calculated by using Kronig-Penney model.

The value of the current generated by the external electric field (**E**) depends on how fast the carriers can move. The carrier's drift velocity can be written as $v_d=\mu E$, where μ is the carrier mobility, indicating the velocity of electron's motion under unit electric field. This is an important parameter to characterize the performance of many semiconductor devices. As mentioned in pervious sections, the covalent bond in inorganic semiconductors has stronger bonding interactions, leading to a larger bandwidth, while the weak Van der Waals force dominating in organic materials yields smaller bandwidth.

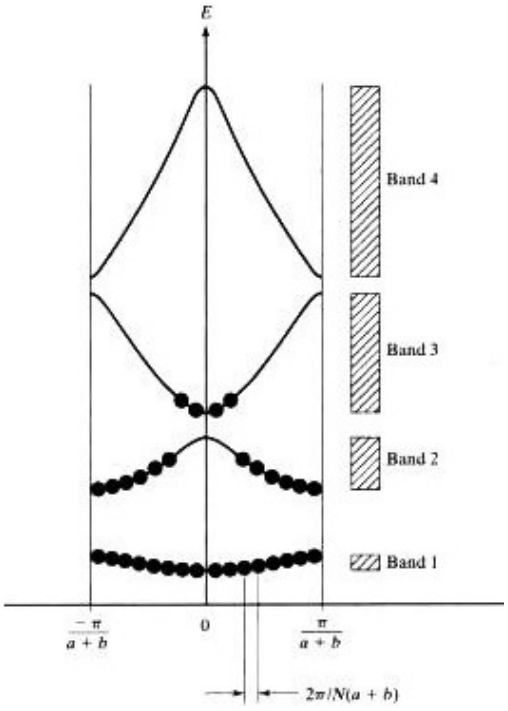

Figure 2.5 Energy band and band gap. A reduced-zone band structure of allowed E-k states in a 1-D crystal with N atoms (Kronig-Penney model).[56]

Miller-Abrahams Hopping. When the bonding interactions are so weak that the electrons may not be considered as delocalized, the band model does not apply. In this

case, the charge carrier has to transport in a thermally activated hopping behavior.[58,59] Miller-Abrahams hopping model, which is also called *nearest-neighbor* hopping, assumes that the localization is strong so the overlap of the electrons wavefunctions fall rapidly with distance. Thus the electron can only jump to the nearest state in space.[60] Mott defined the rate at which the wavefunction on a single well fell off with the distance as exp(-2αr), where $\alpha=\sqrt{2mE}/\hbar$ is the inverse localization length of the wavefunction. The nearest-neighbor hopping happens when $\alpha R_0 \gg 1$, where R_0 is the average distance to a nearest neighbor site. Then the hopping probability per unit time is:

$$p \sim \exp\left(-2\alpha R - \frac{E \pm eRF}{kT}\right) \tag{2.2}$$

where R is the hopping distance, E is the activation energy, F is the applied electric field, k is the Boltzmann's constant, and T is the absolute temperature in degree K. For weak electric field, $eRF \ll$ kT. Thus the mobility of the nearest-neighbor hopping has the temperature dependence which turns out to be an Arrhenius-like relation:

$$\mu = \mu_0 \exp(-E/kT) \tag{2.3}$$

where μ_0 is the prefactor, $E \sim 1/R_0^3 N(E_F)$, is usually on the order of 0.1 eVs in organic amorphous semiconductors. The mobility will decrease with decreasing temperature, which is distinct from the band-like transport behavior.

Mott Variable Range Hopping (VRH). If αR_0 is comparable or less than unity, the overlap of the wavefunction is not limited within the nearest neighbors. At 1968, Mott was the first to point out that, as the temperature decreases, the hopping distance R increases and the thermal activation energy decreases.[61,62] The electron tends to hop to a

state that is energetically favorable, even this requires it to hop over a long spatial distance. Considering a system with localized states near the Fermi level, as shown in Figure 2.6, as the temperature decreases, the two relevant states at which the hopping takes place are limited in a narrower band, with width proportional to T. Therefore the available states are separated further apart, forcing the electron to hop via a longer distance. This is called Mott variable range hopping (VRH) model. The term *variable range* emphasizes that the hopping distance is not confined to the nearest-neighbors.

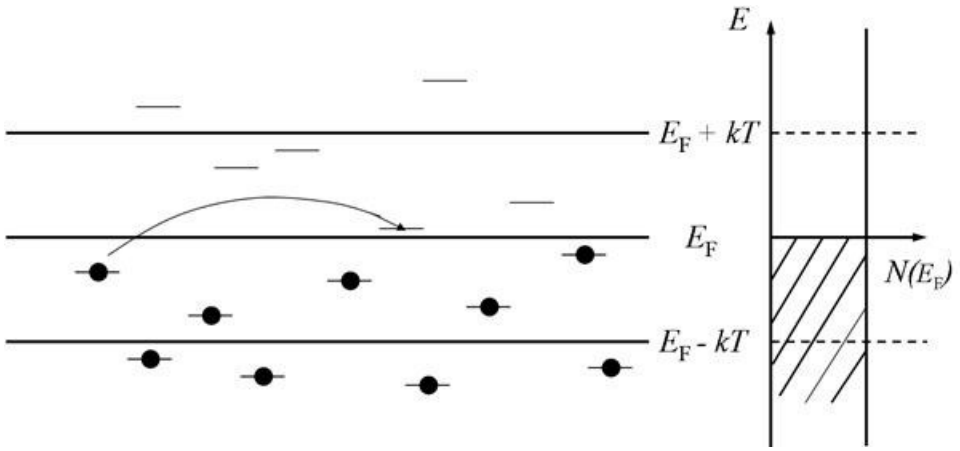

Figure 2.6 Mott variable range hopping. The density of sates near the Fermi level is shown on the right, and the shadow part indicates the occupied states.

Multiple Trapping and Release Model. The multiple trap and release model is a transport mechanism combining the band-like transport with the hopping process. The carriers still travel in a continuous energy band, however, the diffusive transport is limited by shallow traps which lie in the band gap. A trapped carrier has to be thermally activated in order to hop back into the band, and the carrier is easily to be *retrapped* by another trap state. The traps can be structural or chemical in nature, such as vacancies,

positional disorderness, dangling bonds and impurities. The initial model was developed for amorphous silicon film,[59] which gave the result similar to the hopping process due to its thermal activation nature

$$\mu(T) \propto \mu_0 \exp[(E_C - E)/kT] \quad (2.4)$$

where μ_0 is the trap-free mobility, E is the energy of traps. Horowitz *el al.* extended this model to organic materials and considered the gate voltage dependence,[63] and obtain a mobility as a function of V_G and temperature

$$\mu = \mu_0 \frac{N_C}{N_{t0}} \left(\frac{C_i V_G}{q N_{t0}}\right)^{\frac{T_C - T}{T}} \quad (2.5)$$

where μ_0 is the trap-free mobility, N_C is the DOS in the transport band, N_{t0} is the total surface density of traps.

2.2 Organic Thin Film Transistors (OTFTs)

2.2.1 Operation Mechanism

Thin film transistor (TFT) utilizes a capacitively coupled gate dielectric layer to control the current flowing through the semiconductor layer. Four common architectures are shown in Figure 2.7. The basic architecture of TFT includes three electrodes (gate, source and drain), an insulating layer serving as the gate dielectric, and a semiconductor layer transporting charge carriers. TFTs generally have two different geometries, top contacts and bottom contacts. The operation mechanisms are the same for both geometries, although the device performances may be different. For instance, contact resistances are usually larger in (a) & (d). Also, the insulating layer can be fabricated

either on top of the device, which is called top-gate transistor, or on the bottom, which is called bottom-gate transistor.

The gate electrodes and the insulating layer work as a valve, which can control the number of charge carriers in the semiconductor layer. Most OTFTs are based on intrinsic organic semiconductors, meaning that the mobile charge carriers must be injected from electrodes. Theoretically, the gate bias can induce both electrons and holes in the semiconductor layer, which will lead to an ambipolar operation. However, unipolar, especially the p-type transport is often seen in OTFTs.[64]

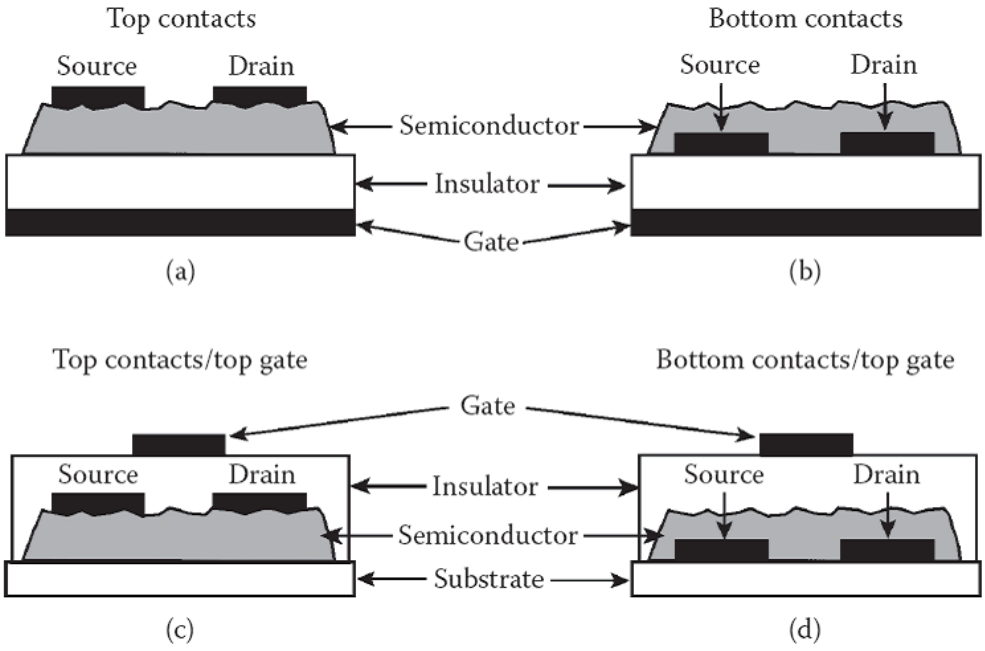

Figure 2.7 Architectures of thin film transistors. (a) top contacts with bottom gate electrode, (b) bottom contacts with bottom gate, (c) top contacts with top gate and (d) bottom contacts with top gate.[55]

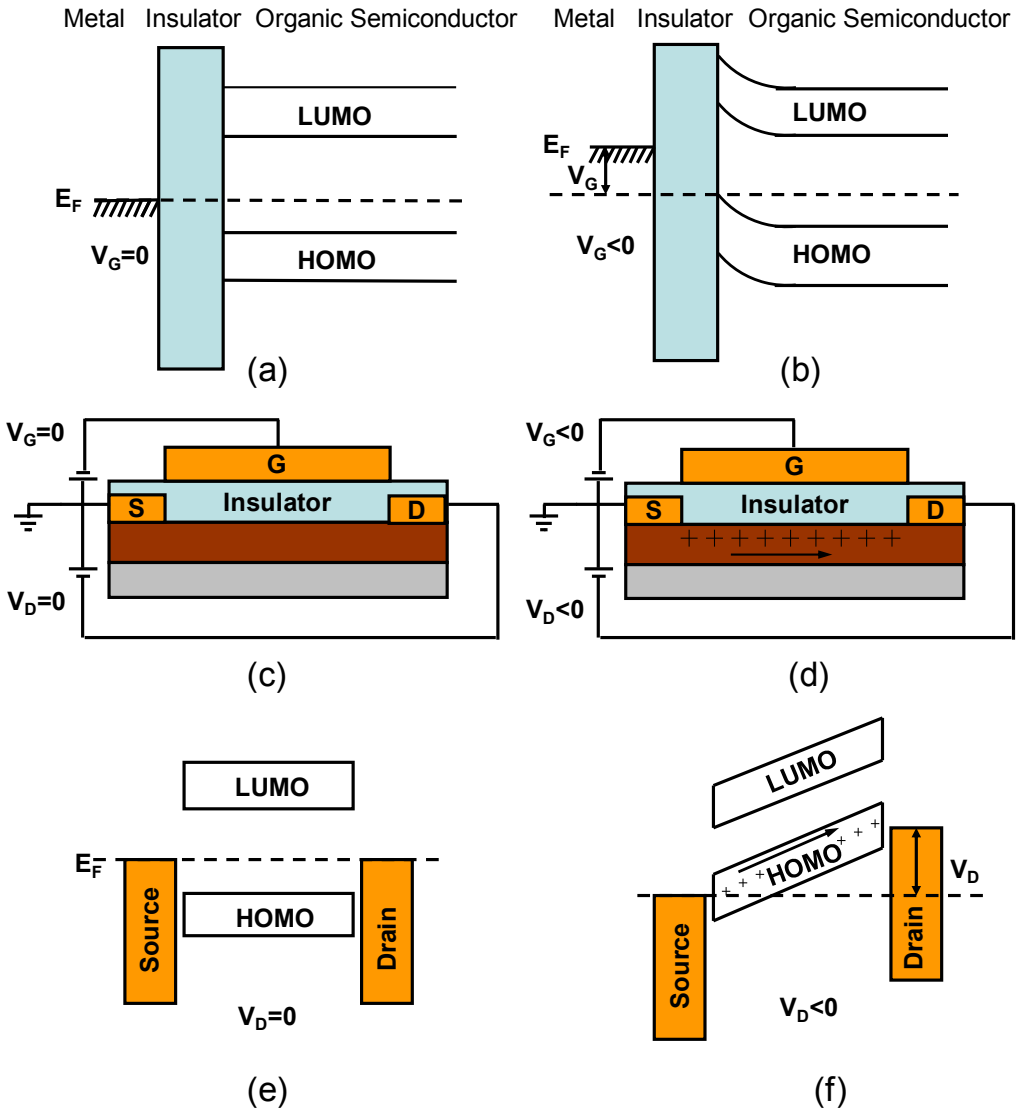

Figure 2.8 Operation mechanism of p-type OTFT. (a) & (b), band diagram of MIS structure with zero gate bias ($V_G = 0$), and a negative bias ($V_G < 0$), respectively. (c) Schematic of a OTFT with zero gate bias applied, and (d) with negative gate bias. (e) Band diagram of the metal contacts and the semiconductor, with zero V_G and V_D, and (f) with a negative drain bias.

The operation mechanism of OTFT is explained based on p-type transistor as an example. A small negative gate bias will induce localized positive charges in

semiconductor at the insulator-semiconductor interface. These localized charges start to fill the deep traps in the energy gap, which energy level is separated from the top of the HOMO level by more than a few k_BT. As the bias getting more negative and more traps are filled, the Fermi level, which is initially located between the HOMO and LUMO level, moves closer to the HOMO band, as shown in Figure 2.8 (b). As soon as (E_F-E_{HOMO}) becomes comparable to k_BT, electrons can be thermally excited from the band into the empty localized states, thus the holes are generated. Therefore, a p-channel is formed at the insulator-semiconductor interface, as shown in Figure 2.8 (d). A negative V_D allows the holes to be injected from the source contact, flowing across the channel, and extracted from the drain contact. The conductance of the semiconductor becomes several orders of magnitude larger when the device is turned ON by the gate bias. As the gate bias getting more negative, the current flowing across the channel increases due to the increasing number of charge carriers. Additionally, Figure 2.8 (e) and (f) show the Fermi level is elevated at the drain side by the source-drain bias, which is the driving force of carriers flowing across the channel.

2.2.2 Characteristics of OTFT

The performance of a transistor is usually characterized by the transfer and output characteristics. Tuning the longitudinal electric field by varying the gate bias will change the transverse drain current, which is shown as a typical transfer curve in Figure 2.9 (a). On the other hand, with constant gate voltage, varying the drain bias also changes the drain current, which is the output curve, as shown in Figure 2.9 (b).

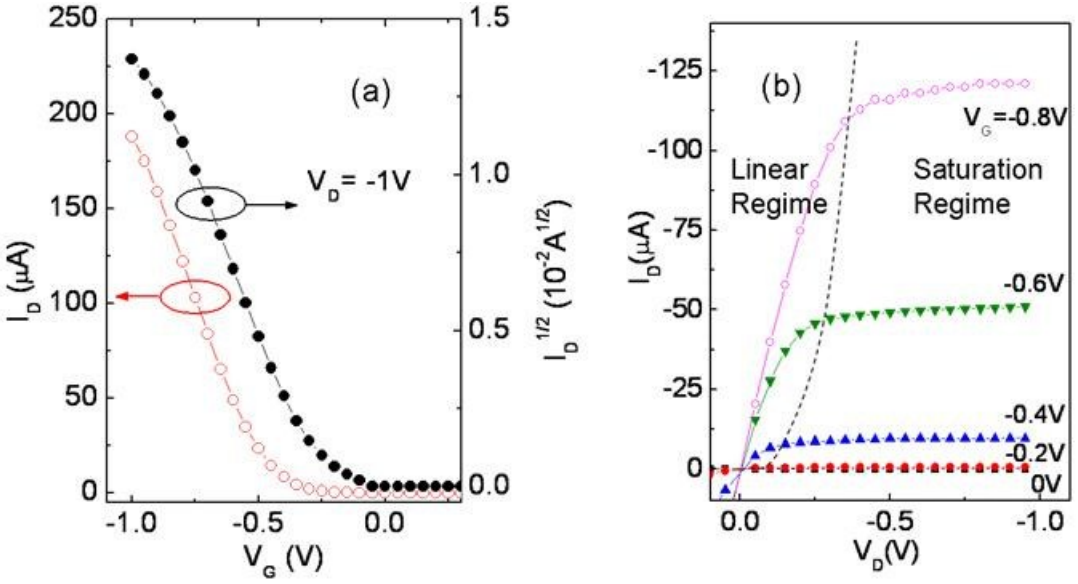

Figure 2.9 Transfer and output characteristics of an OTFT. (a), transfer curves. The left axis is I_D, and the right axis is $\sqrt{I_D}$. (b), output characteristics with various V_G, the linear and saturation regimes are separated by the dashed line.

The characteristics of typical field effect transistor have been well explained in standard semiconductor device textbook.[65,66] In *linear regime*, where the drain voltage (V_D) is small enough compared to the gate voltage (V_G), the drain current (I_D) increases linearly to the charge carrier density, which also linearly depends on the gate bias. The *I-V* behavior obeys:

$$I_{D,Lin} = \frac{W}{L}\mu_{lin}C_i\left[(V_G - V_{th}) - \frac{V_D}{2}\right]V_D \qquad (2.6)$$

where W is the channel width, L is the channel length, μ_{in} is defined as the linear mobility, C_i is the sheet capacitance of the dielectrics, V_G, V_D are the gate and drain bias, respectively, V_{th} is the threshold voltage. V_{th}, as mentioned in previous section, is the voltage needed to induce enough charges to fill the deep traps and surface states in the

semiconductor. From the linear plot of I_D-V_G curve, V_{th} can be extracted when the extension line of I_D crosses the one of off-current.

If V_D is larger than (V_G - V_{th}), the latitudinal electric field becomes comparable to or larger than the longitudinal electric field, which results in the non-uniform carrier density along the channel. Close to drain electrode, the carrier density falls to zero, which is called the *pinch-off* region. As the drain voltage increases, the pinch-off region expands. The resistivity of the pinch-off regime is large due to the low carrier density and low mobility. Therefore, most of the drain voltage drops at this regime. At this stage, the current no longer increase as V_D, which is called the *saturation regime*, as shown in Figure 2.9 (b). The real bias drop on the channel is now approximately equal to the gate voltage, then Eqn. 2.6 becomes

$$I_{D,sat} = \frac{W}{2L}\mu_{sat}C_i(V_G - V_{th})^2 \tag{2.7}$$

where μ_{sat} is the saturation mobility. From Eqn 2.6, the linear mobility can be obtained from the channel transconductance (g_m):

$$g_m = \frac{\partial I_{D,lin}}{\partial V_G}|_{V_D} = \frac{W}{L}\mu_{lin}C_iV_D \tag{2.8}$$

and the saturation mobility can be extracted from the slope of $\sqrt{I_{D,sat}}$ versus V_G :

$$\frac{\partial\sqrt{I_{D,sat}}}{\partial V_G} = \sqrt{\frac{W}{2L}\mu_{sat}C_i} \tag{2.9}$$

This assumes that the mobility is a constant with V_G, which is not always true in experiments. The observed mobility can either increase with V_G, due to the contact

resistance dominating when V_G is small, or decrease with V_G since the distribution of trap density might increase exponentially as the Fermi level approaching the HOMO level.

2.3 Electrolyte-Gated Transistors (EGTs)

The low mobilities in organic semiconductors are the major limitations of the output current and switching frequency of OTFTs. One of the strategies to improve the device performance is to induce more charge carriers in channel by increasing the capacitance of gate dielectric layer. Some researchers employed ultra-thin dielectric layer (including self-assemble monolayer) and high-κ materials.[23,67-69] An intriguing direction is to use the electrolyte as the dielectric layer, which is ionically conducting and electronically insulating. This section discusses the operation mechanisms of electrolyte-gated transistors (EGTs) and their applications.

2.3.1 Introduction of Electrolyte

Using electrolyte as the gate dielectric material is not new in this area. The first Ge transistor was demonstrated with the presence of aqueous electrolyte solutions.[70] The study of EGTs dates back to Wrighton's work in 1980s, who intensively studied the electrochemical doping of semiconducting polymers using electrolytes.[71-75] Many research groups now utilize electrolyte as a dielectric layer gating various type of semiconducting materials to fabricate transistors or study the carrier transport phenomena.[76-79]

Although the early studies in this area are often based on electrolyte in liquid phase, the solid state electrolyte is more applicable in electronics applications. The conventional solid state electrolyte is acquired by dissolving inorganic salts in soft polymers. For example, lithium salts $LiClO_4$ dissolved in poly(ethylene oxide) (PEO) (Figure 2.10), was used to gate various semiconductors, including organic single crystals, small molecules, polymers and carbon nanotubes.[79-83] In this electrolyte, the PEO polymer chain is flexible so that the Li^+ cation can move along the chain due to the interaction between the cation and oxygen.

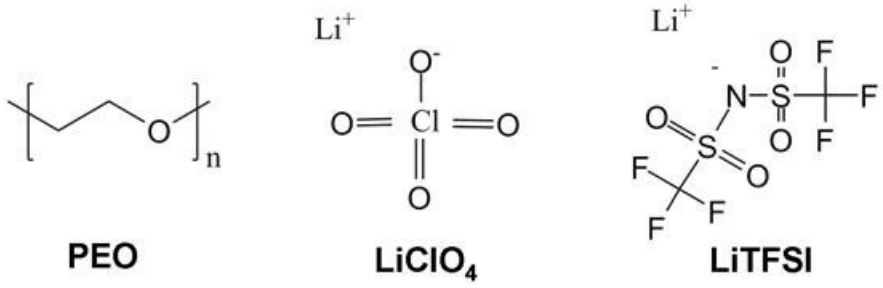

Figure 2.10 Chemical structure of solid polymer electrolyte.

Ionic liquids are a type of organic salts which appear to be liquid at room temperature. They have many exceptional advantages from application prospective, e.g., unmeasurable vaporpressure, great chemical and thermal stability, and high ionic conductivity.[84,85] In order to make it compatible to circuits and other electronic devices, ionic liquids can be dissolved in cross-linked polymers to enhance its mechanical property. For example, the gelation of a typical ionic liquid, [BMIM][PF_6] dissolving in a block-copolymer, PS-PEO-PS can be achieved at a fraction as low as 5 wt%.[86] The polystryrene (PS) is

insoluble in the ionic liquids, and PEO block is soluble. The triblock copolymer forms a physical cross-linked network which gives mechanical support of the ion gel. Typical ionic liquids and polymers for ion gel are shown in Figure 2.11.

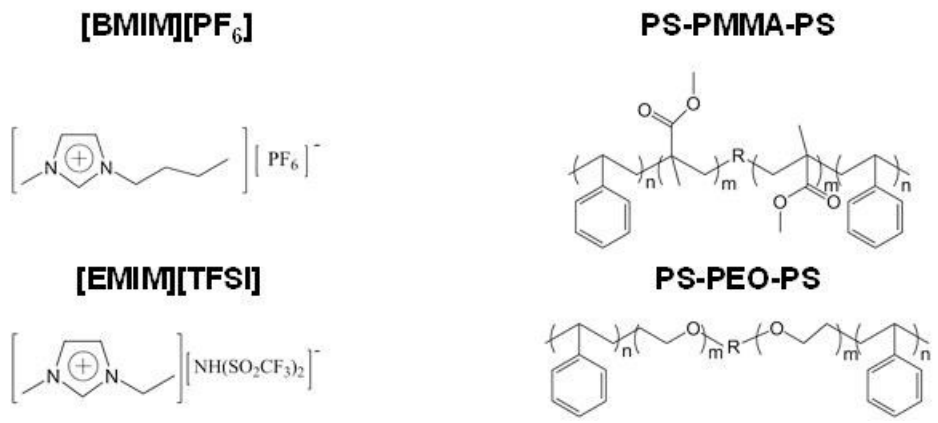

Figure 2.11 Chemical structures of common ionic liquids and polymers for ion gel.

In ion gels, cations and anions of the ionic liquids can migrate easily due to the low melting temperatures of ionic liquids and high ionic conductivities. Ion gel has higher ion mobility (10^{-3} cm/S) compared to the PEO-based electrolyte (10^{-4} – 10^{-5} cm/S), which enhances the transistor working frequency.[87]

Another interesting type of electrolytes, polyelectrolytes, was demonstrated by Berggren's group.[27,88] The polymers contain polyanions which are not mobile, and small cations/protons which are mobile. Using this type of electrolyte, the 3-dimensional ion penetration in EGTs can be largely reduced (details of operation mechanism are in section 2.3.2).

2.3.2 Operation Mechanisms of EGTs

The architecture of EGT is very similar to the OTFTs discussed in previous section, except the dielectric layer is replaced by an ionic conducting electrolyte layer, as shown in Figure 2.12 (a). The electrolyte layer contains dissociated cations and anions, which can migrate under the external electric field.

When a voltage difference is applied between the electrolyte and the semiconductor, the ions in electrolyte will be driven towards the electrode/electrolyte and electrolyte/semiconductor interfaces. If the semiconductor layer is ion-impermeable, the ions will form a Helmholtz layer at one side of the interface, and charge carriers in the semiconductor will accumulate at the other side, together they form an electric double layer. Since the thickness of the EDL is usually around 1 nm, it has a much larger capacitance (on the order of 10 $\mu F/cm^2$) than traditional dielectrics.[89,90] Another electric double layer is also formed at the gate/electrolyte interface. Both EDLs contribute to the total gate capacitance. By the analogy to two capacitance in series, total capacitance of the electrolyte dielectric layer is $1/C=1/C_1+1/C_2$. With impermeable semiconductors, the EGTs are also sometime named as electrical double layer transistors (EDLTs).

On the other hand, with ion permeable semiconductors, such as polymers, the ions can migrate into the semiconductor layer. The EGTs thus operate under the same mechanism of electrochemical transistors (ECTs), as shown in Figure 2.12 (b) right panel. In electrochemical transistors, ions in electrolyte are repelled from the gate electrode, diffusing into the semiconductor film. By chemically reacting with semiconductor

molecules, ions induce charge carriers in the semiconductor layer. The current of an electrochemical transistor depends on the doping level, which is also controlled by the gate voltage. The ECT switches on and off upon the reversible doping and de-doping processes.

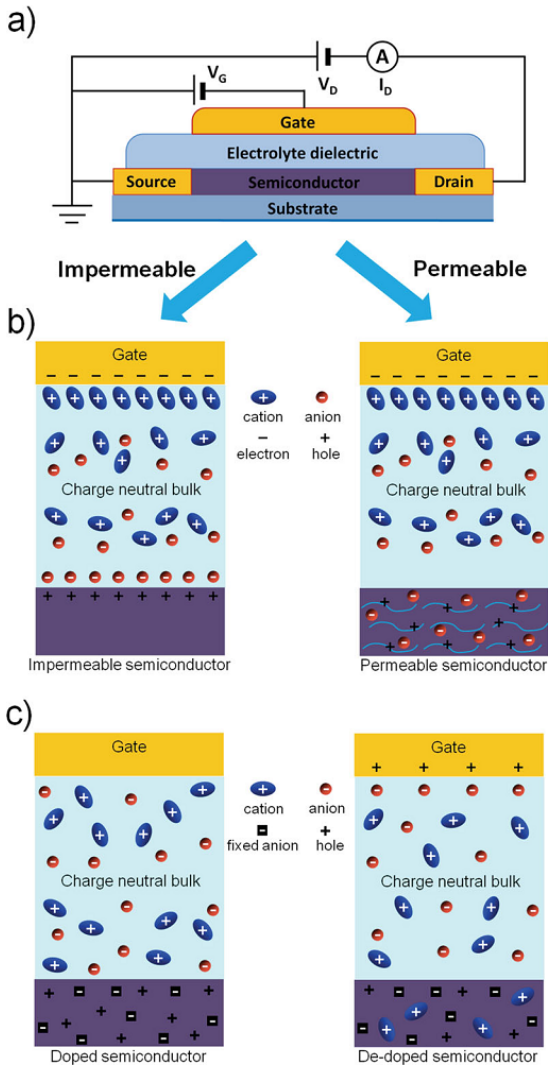

Figure 2.12 Operation mechanism of EGT. (a) architecture of a typical EGT. (b) carrier accumulation mode of an EGT with ion impermeable and permeable semiconductors. (c) depletion mode of EGT without and with a gate voltage.[91]

It is worthwhile noting that because the ions are physically driven across the interface, the frequency of switching the transistor is often limited. In fact, it has been shown that, in ion gels, the operation frequency determines which mechanism is dominant in a transistor. EDL dominates at high frequency (>1 kHz) while electrochemical doping happens at lower frequencies.[92]

2.3.3 Applications of EGTs.

One important advantage of employing electrolyte is to induce a large number of carriers in the semiconductor. The sheet carrier density in EGTs can be orders of magnitude larger than SiO_2.[93,94] Because the charge transport in organic semiconductors is sensitive to the carrier density, the ability to tune the carrier density in several orders of magnitude opens a lot of possibilities, such as metallic state transition,[94,95] superconductor transition,[93] and negative transconductance[77,96], etc. In addition, the electrolyte gating can reduce the contact resistance at the source/drain electrodes, which might contribute to some observations of ambipolar transport.[97] From the application prospective, the electrolytes are competitive in flexible electronics since they are also inherently solution processable, printable and flexible.[98] This section reviews some relative works in this area.

Berggren's group reported a series studies based on electrochemically doping in poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate), PEDOT:PSS, including printed bi-stable electrochemical transistors and all organic current rectifiers.[99,100] Based on the electrolyte gated transistors, they also demonstrated inverters, NAND and NOR logic

gates, as well as the ring oscillators (shown in Figure 2.13 a).[26] The stage delay time of the ring oscillator is 10 s, which is relatively long even compared to organic circuits (more discussions are in chapter 4). This is expected since the electrochemical doping is a relatively slow process. In addition, an all organic, printed humidity sensor was also demonstrated based on the electrochemical doping of PEDOT:PSS (Figure 2.13 b).

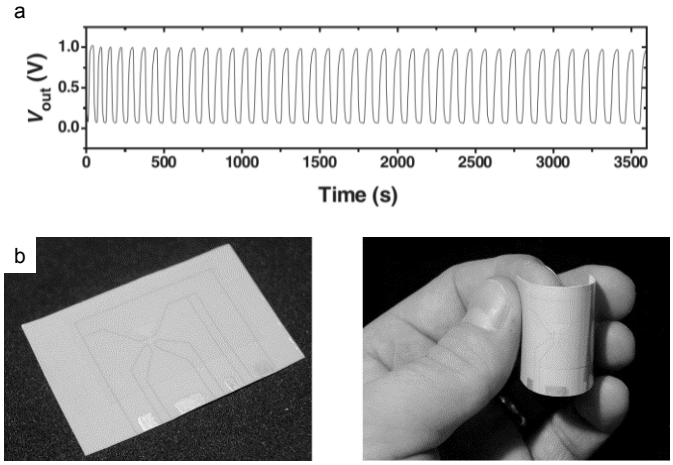

Figure 2.13 Printed electrochemical circuits and sensors.(a) output performance of a printed ring oscillator based on PEDOT:PSS.[26] (b) printed flexible sensor.[101]

Our group reported a printable electrolyte, ion gel, and its applications in printed, flexible electronics in 2008.[24] The ion gel is based on ionic liquid, [EMIM][TFSI], and block-polymer, PS-PMMA-PS. The first report studied EGTs based on various semiconducting polymers, including P3HT, PQT-12, and F8T2. The transistors operate at 1 – 5 V, with mobilities from 0.6 – 2 cm^2/Vs. The transistors showed very good reproducibility, ambient storage stability, and decent operation stability. Continued with the first report, printed and flexible digital circuits based on same EGTs were

demonstrated, including transistor loaded inverters, ring oscillators, NAND gate, SR LATCH and D-flipflop.[25] The transistor loaded ring oscillators showed a frequency as high as 120 Hz at 3 V, corresponding to a delay time < 1 ms (shown in Figure 2.14). The high ion conductivity of ion gel lead to the fast switching ring oscillator in this work.

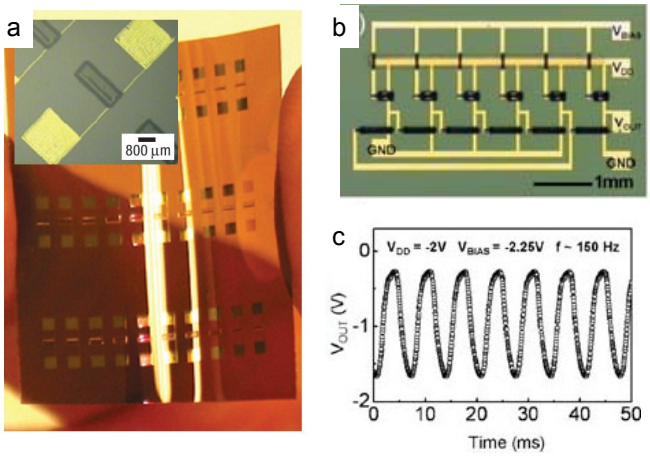

Figure 2.14 Printed ion gel gated transistors and circuits. (a) printed ion gel gated transistor array on polyimide substrate.[24] (b) printed transistor-loaded ring oscillators. (c) the output performance of the ring oscillator.[25]

The work in this thesis is a continued study of above researches. Chapter 5 and 6 focus on how to further improve the circuit performance and speed. Chapter 7 demonstrates more applications of electrolyte gated devices.

2.3.4 Electrochromic (EC) Displays.

The EC display is an interesting application of electrolyte gated devices. They are simple to produce and can provide a full gamut of colors. In addition, they also can be integrated into a spectrum of products ranging from smart windows and mirrors to simple

packaging displays.[102,103] Several groups have demonstrated active matrix control of flexible electrochromic displays.[15,104,105] For instance, Berggren et al. demonstrated a matrix of PEDOT:PSS electrochromic display cells by printing. Each cell consists of two lateral electrodes both made of PEDOT:PSS. A layer of electrolyte covers both electrodes. With a voltage difference between the two electrodes, the positively biased one will be oxidized more and turn into transparent state due to the polaron formation; the negatively biased one will be reduced and turn into dark blue color, as shown in Figure 2.15. Each cell is addressed by an electrochemical PEDOT:PSS transistor.

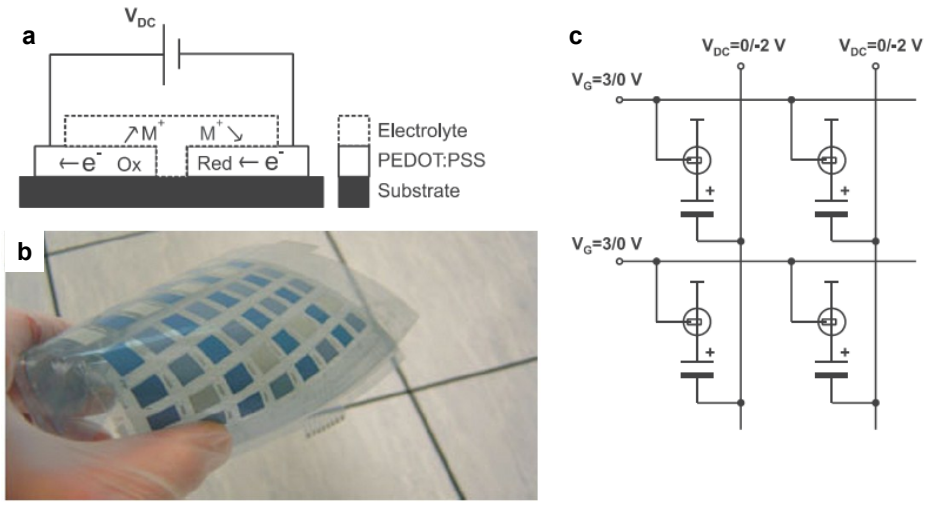

Figure 2.15 Active matrix of printed electrochromic displays. (a) cross-section of a lateral EC display cell. (b) a printed 5x5 display matrix. (c) a scheme of a 2x2 active display matrix.[15]

Chapter 3 Carbon Nanotube Transistors and Applications

3.1 Introduction

As discussed in previous chapters, using printable, high capacitance electrolyte can enable the low voltage operation of printed transistors and circuits. In order to achieve fast switching frequency, a printable, high mobility semiconductor is also important. Carbon nanotube (CNT) is found to be one of the attractive candidates for flexible electronics, due to its high mobility, high mechanical strength, and compatibility with flexible and printable electronics. This chapter discusses the fundamental characteristics of carbon nanotubes and their applications. The structure and growth methods of CNTs, the deposition and purification techniques of single wall nanotubes are reviewed. And the electronic properties of individual CNT and CNT network will be discussed respectively. Finally, the electronic applications based on CNTs are reviewed.

3.2 Structures and Characteristics of Carbon Nanotubes

Carbon nanotubes (CNTs), since the first discovery by Lijima in 1991, various applications have been proposed, such as RF devices, digital logic circuits, interconnects, and conductive sheets. [106-109] The unique one dimensional structure of CNT leads to its distinguishable properties and attracts intensive interests not only on applications, but also the fundamental research in solid state physics, quantum electronics, materials science, and other areas. This section reviews the structure of the carbon-based nano-materials, such as grapheme, C60, and CNT, as well as the fabrication methods of CNTs.

3.2.1 Structures of Carbon Nanotubes

The CNT can be imagined as a seamless cylinder rolled from a sheet of graphene, which is a single layer of sp^2-bonded carbon atoms in honeycomb arrangement. Graphene is recently found can be easily produced by mechanical exfoliation of natural graphite,[110] which is an important discovery awarded with 2010 Nobel Prize in Physics,[111] leading to today's intense study and understanding of the electronic properties of graphene. Besides CNT, another important state of material, fullerene (C_{60}) is also an interesting electronic material, which can be thought of based on the graphene structure. Figure 3.1 shows the atomic structure of graphene, graphite, CNT and C_{60}.[112] Generally, graphite is considered as a 3-dimensional structure as a bulk material, graphene is a 2-dimensional, CNT and C_{60} are 1-dimensional and 0-dimensional, respectively. Graphene and C60 also have been studied intensively due to their remarkably properties, which are out of the scope of this thesis.

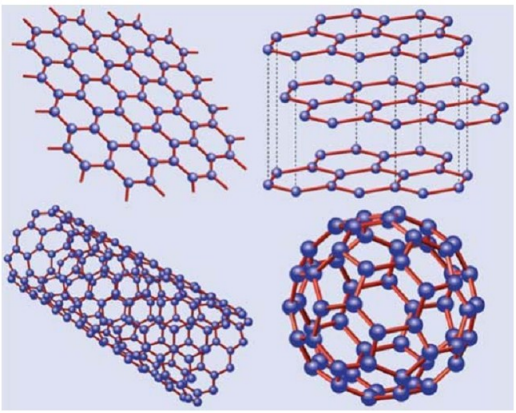

Figure 3.1 Atomic structure of graphene, graphite, carbon nanotube and Fullerene (C60). [112]

The electronic properties of CNT are closely related to graphene's, which will be discussed in the following section. In addition, CNT is sensitive to the tube diameter and chirality (specified by two indices (n, m) based on the wrapping angle of the graphene sheet). Slight difference in these parameters can vary the electronic characteristics of CNTs from semiconducting to metallic, shown both by experiments[113] and theoretic predictions[114-116]. Figure 3.2 shows the relation between the structure of CNT and the wrapping angle.[117] There are two atoms in the graphene unit cell, which are shown Figure 3.2 (a) as A and B. The basis vectors of graphene lattice are $\boldsymbol{a}_1$ = a (√3, 0) and $\boldsymbol{a}_2$ = a (√3/2, 3/2), where a = 0.142 nm is the length of carbon-carbon bond. When cutting a graphene strip to form a CNT, the direction can be defined as vector $\boldsymbol{C}$=n$\boldsymbol{a}_1$+m$\boldsymbol{a}_2$, from which the CNT's chirality can be referred as (n, m). The radius of CNT can be obtained as:

$$R = \frac{C}{2\pi} = \left(\frac{\sqrt{3}}{2\pi}\right) a\sqrt{n^2 + m^2 + nm} \qquad (3.1)$$

The CNTs shown in Figure 3.2 are examples of zigzag nanotube (n, 0), armchair nanotube (n, n), and chiral nanotube (n, m). Figure 3.2 (d) shows the carbon bonds in carbon nanotubes. Three of the four carbon electrons are bonded to its three nearest neighbors by sp^2 bonding, in a manner similar to graphene. The fourth electron is a π orbital perpendicular to the cylindrical surface.

When CNT was discovered at the first time[106], it was made of several layers of graphene layers regularly spaced by 0.34 nm, the same as in conventional graphite materials. These are multiwall nanotubes (MWNTs). The MWNTs usually have

diameters from a few nanometers to several hundreds of nanometers, and the length can be over several microns. The single-wall nanotube (SWNTs) which is made of a single graphene sheet was synthesized soon after the discovery of MWNTs.[118] The SWNTs have small diameters which are on the order of nanometers. The small diameter and the perfect periodic crystalline atomic structure make the SWNT ideal system to study the 1-D electron transport behavior, and attractive material for nanoelectronics. The following sections discuss the electronic properties and applications of SWNTs.

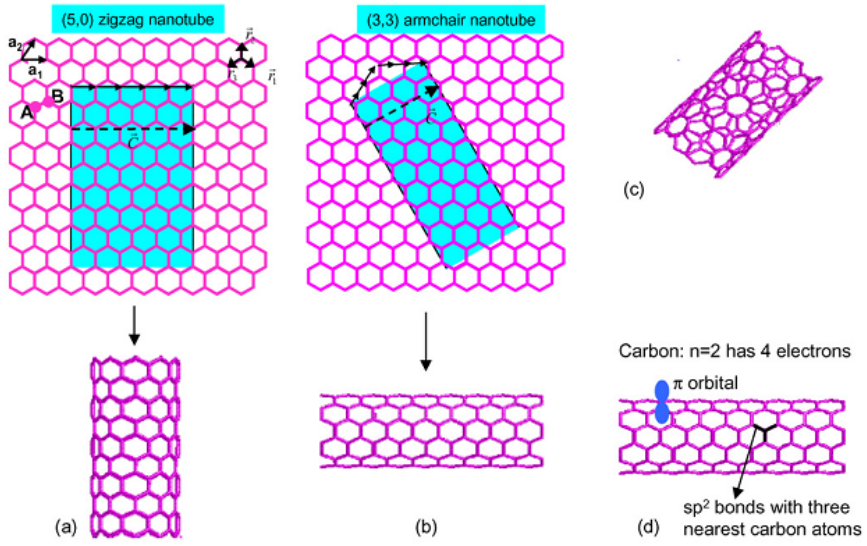

Figure 3.2 Structure of CNTs. (a) a zigzag (*n*, 0) nanotube. (b) creation of a (*n*, *n*) armchair nanotube. (c) a (*n*, *m*) chiral nanotube. (d) the bonding structure of a nanotube.

3.2.2 Electronic Properties of Carbon Nanotubes

As discussed above, the carbon nanotubes can be considered as a graphene sheet rolled over, and the direction of the rolling process is described by a pair of integers (*n*, *m*).

Along the length of the nanotubes, electron motion is free therefore $k_{\parallel}$ is a continuous variable. On the other hand, along the circumference of the nanotube, $k_{\perp}$ is quantized due to the limited number of atoms and periodic boundary conditions. Thus,

$$C \cdot k_{\perp} = C_x k_x + C_y k_y = 2\pi\upsilon, \quad (3.2)$$

where $\boldsymbol{C}=n\boldsymbol{a}_1+m\boldsymbol{a}_2$, is the circumference of a (n, m) nanotube as shown in Figure 3.2, and υ is a non-zero integer. Equation 3.2 sets the allowed relation between k_x and k_y defining lines in the (k_x, k_y) plane. As shown in Figure 3.3, each individual line slices the two dimensional band structure of graphene, generating a one dimensional energy band. The positions of the lines are determined by the value of C_x, C_y and υ, giving rise to the semiconducting and metallic nanotubes. If the lines pass through the Dirac points of the graphene, as shown in the right panel of Figure 3.3, the energy band gap will be zero, therefore the nanotube is metallic. On the other hand, if the lines of quantized wavevectors do not cross the Dirac points, the nanotube will become semiconducting and the band gap is determined by the two lines which are closer to the Dirac points, as shown in the left panel.

The CNT is metallic only when the lines described by Equation 3.2 passes the Dirac points. Therefore, the condition becomes,

$$|n - m| = 3l, \quad (3.3)$$

where l is an integer. CNTs for which the condition does not hold are semiconducting. This condition is the reason why nanotubes that are naturally grown contain 33% metallic nanotubes.

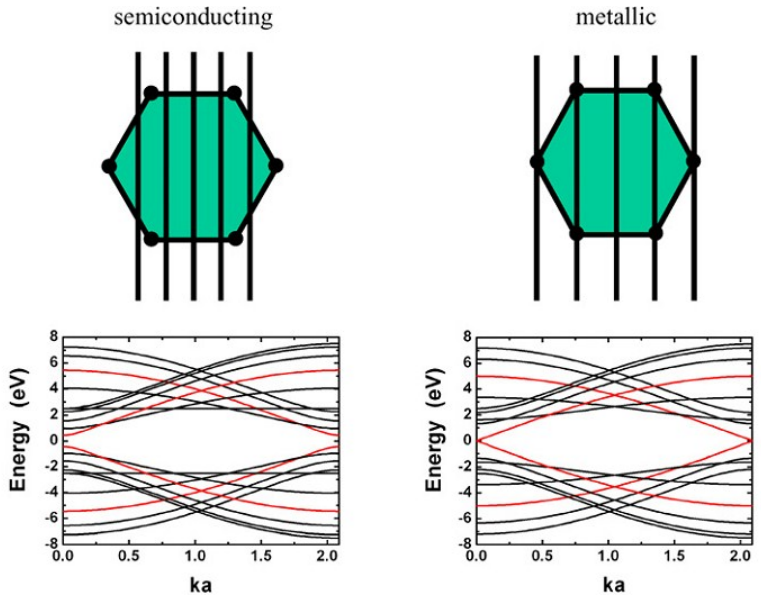

Figure 3.3 Metallic and semiconducting CNTs. Illustration of allowed wavevector lines leading to semiconductor and metallic CNTs and examples of bandstructrures for semiconducting and metallic zigzag CNTs.

When $|n-m| = 3l \pm 1$, the nanotubes are semiconducting, and the band gap is determined by the distance of the two lines which are closer to the Dirac points. Therefore, $e^{ik\cdot C} = \pm e^{i2\pi/3}$, and one can solve the dispersion relation at the Fermi level based on the tight-binding model. The energy gap for a semiconducting nanotube is then

$$E_g = \frac{2\pi a\gamma}{\sqrt{3}|C|} = \frac{2a\gamma}{\sqrt{3}d}, \tag{3.4}$$

where $d = |C|/\pi$, is the diameter of the nanotube. It can be seen the energy gap of semiconducting nanotube decreases as the inverse of its diameter, as shown in Figure 3.4. One can imagine for infinite large diameter, the nanotube has zero band gap since it represents the entire graphene sheet.

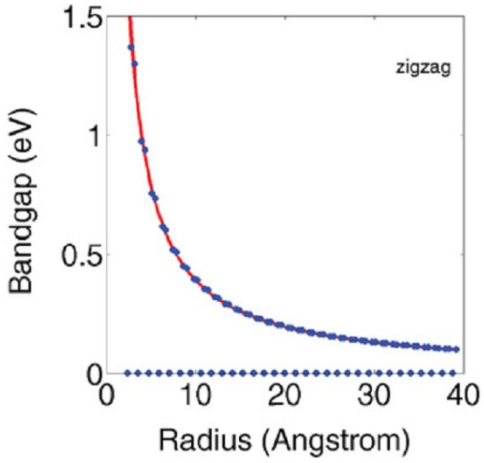

Figure 3.4 Band gap versus radius for zigzag CNTs.

3.2.3 Deposition of Carbon Nanotubes

Overall speaking, the ideal fabrication methods should provide good control in terms of the key parameters of the thin film. Particularly for CNTs thin films, these parameters may include film density (or coverage), ratio of m-CNTs and s-CNTs, alignment, distributions of lengths and diameters of nanotubes, etc. It is also important to be compatible with large-area, low-cost processing, or maybe on flexible substrates for some applications. This section reviews some of the approaches which have demonstrated successes in certain directions.

In order to deposit the CNTs at desired locations on substrate, many techniques have been developed. Usually, it can be divided into categories as "grow-in-place" and "solution-based". The "**grow-in-place**" technique usually involves the synthesis of nanotubes and deposition on substrate simultaneously. The most commonly used and intensively studied synthesis methods of CNTs are chemical vapor deposition (CVD) and

laser ablation. Typically, CVD growth of CNTs gives good control of film density or coverage, as well as the film morphology and nanotube alignment. Growth parameters can be adjusted to tune properties of the CNTs. For example, species of feed gas, concentration of catalytic nano-particles influence the film density.[119-122] There are studies showed that the size and composition of catalyst may affect the diameters and chiralities of the CNTs.[123,124] In addition, the average tube length depends on the growth temperature, gas pressure, and growth time.[125,126] Some examples are shown in Figure 3.5 (a) – (c). Besides the control over the network parameters, some methods also demonstrate the ability of achieving alignment and patterning of the CNTs. Figure 3.5 (d) – (h) showed some examples of aligned CNT networks. The techniques which have been demonstrated include CVD growth with electrical field,[127,128] CVD growth with a laminar feed gas flow,[129-131] growth on substrates with regular atomic steps,[132,133] or patterned catalyst particles.[134] Combining multiple steps of alignment control, the CNT can be even grown in complex morphology (example in Figure 3.5 (i)).[135-138] Despite the capability of fabricating high quality CNT film, CVD growth is not very compatible to low temperature, large area fabrication.

The "**solution-based**" methods, on the other hand, are more suitable to low-temperature, large-area, and cost-effective fabrications of electronics, and thus more attractive to many applications. The methods generally involve the formation of a stable solution suspension of CNTs, and a reproducible way to deposit the CNTs onto substrate from the solution. Due to the strong tube-to-tube interactions of CNTs, to achieve a stable suspension usually requires using surfactant wrapping around the nanotubes. This step

often requires high-power ultrasonication which could reduce the average lengths of CNTs and affect the electrical properties. Furthermore, the presence of the organic surfactant may influence the electronic properties of CNTs due to the complex surface chemistry.

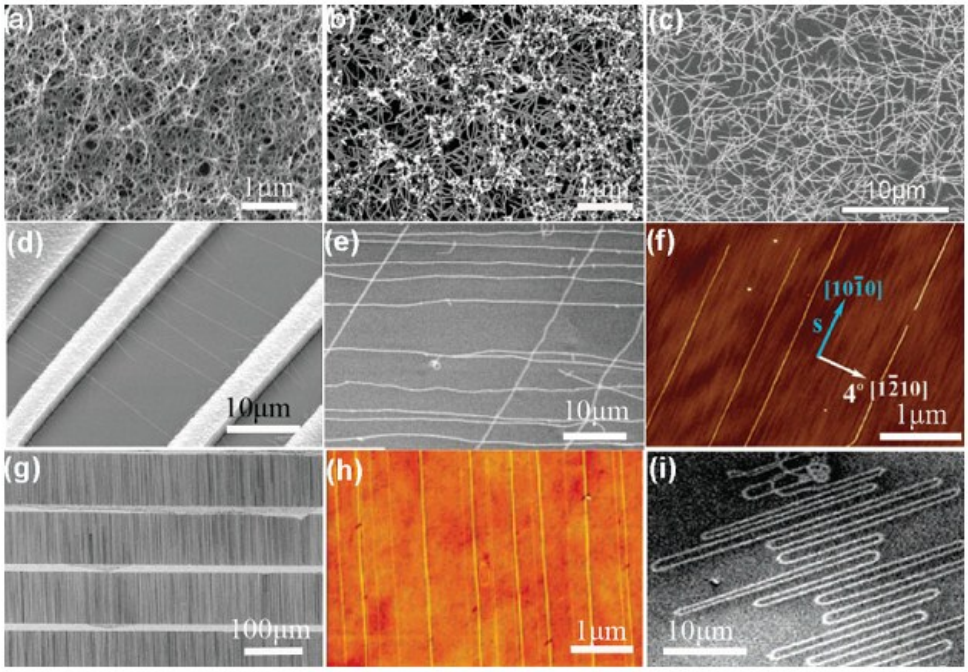

Figure 3.5 SEM/AFM images of CNT films grown by various methods. (a) and (b), CNT films grown by CVD. (c) A CNT film deposited from a suspension in methanol. (d) An aligned array of CNTs grown by CVD with an applied electric field between microelectrodes (bright). (e) Crossbar array of CNTs formed by a two-step flow-alignment growth process. (f) CNT array grown on a miscut sapphire substrate. (g) and (h) Patterned CNT films grown by CVD. (i) Self-organized nanotube serpentines formed due to the combined alignment effects from the quartz substrate and gas flow.[29]

As to how to remove the solvent and fabricate the CNTs onto the desired substrates, there are many different techniques. Early demonstrations by Snow *et al.* showed random

CNT networks can be achieved by as-grown CNTs solutions, with the mobility about 10 – 100 cm^2/Vs, and ON/OFF ratio of 10 – 100.[139-141] Other techniques which can reproducibly achieve random networks include drop-casting,[142-144] spin-coating,[145,146] dip-coating,[147] quasi-Langmuir–Blodgett[148] and Langmuir–Blodgett deposition.[149] These solution-based methods not only share the advantages such as compatibility to large area and room temperature deposition, but also have limitations such as the sensitivity to the substrate surface energy or surface chemistry, alignment, presence of the CNTs bundles, variations of the network morphology and densities, and so on. A technique with controlled flocculation (cF) process demonstrated the ability of controlling the location of CNT deposition, as well as the film density and alignment.[150,151] Other efforts trying to address the alignment of the network include gas-flow cell method,[152] and coating the substrate with functional molecules,[144,147] deposition assisted by electrical or magnetic field,[153-158] and other methods such as deposition based on the liquid-crystalline behavior of CNTs.[159]

Transfer printing is another class of methods which can be combined with some of the above solution-based fabrication methods.[150,151,160] Vacuum filtration method was demonstrated by Grüner and colleagues.[161] The diluted CNT solution is vacuum-filtered through a porous membrane, and the nanotubes were trapped on the surface of membrane, forming a thin film. The advantages of this method are the high throughput (in a few seconds), precise control over the film density by controlling the filtered solution volume, and homogenous film morphology due to the fast evaporation of solvent and minimum tube flocculation. However, it may require additional transfer steps in

order to accommodate different substrates.[162] This method is useful for the applications such as transparent conductance films due to the ability of achieving high density CNT networks under fast speed.[163] It has been successfully demonstrated that spin-coating, drop-casting, dip-coating, ink-jet printing, and aerosol jet printing based on CNTs solutions can fabricate the CNTs films on various type of substrates (examples are shown in Figure 3.6).

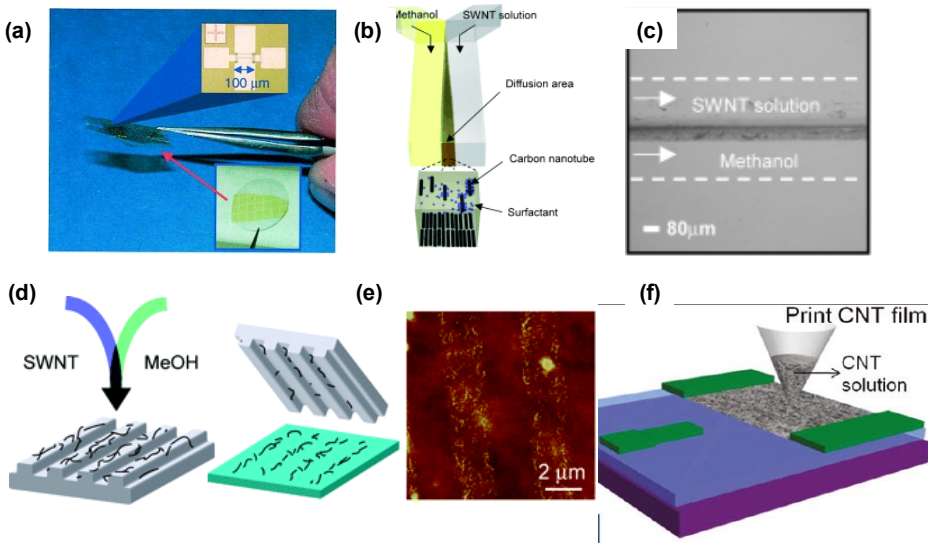

Figure 3.6 Deposition methods of CNTs. (a) drop-casting of CNT thin film.[140] (b) and (c), the schematic of Langmuir–Blodgett deposition and SEM images of CNT film.[151] (d) and (e), transfer printing of CNT stripes. (f) jet printing of CNT solution.[164]

There are several advantages of the solution-based deposition. For example, the post-growth purification techniques have shown some success in controlling the CNT diameters and chirality, which will directly benefit the thin film quality deposited from purified solutions. In addition, several methods, especially printing techniques, can offer very well control in patterning of the thin film, which is critical to electronic applications.

However, the remaining challenge is the alignment of the nanotubes. Perfectly aligned nanotubes network may be desired in low-resistance transparent electrodes applications, but its effect on electronics based on semiconducting CNTs thin films is not yet clear.

3.2.4 Purification of CNTs

As mentioned above, the as-grown CNTs contain m-CNTs and s-CNTs. The m-CNTs are useful to transparent electrodes and sensor applications, and the s-CNTs are good candidates for semiconductor electronics. Therefore, in most of the applications, it is critical to separate these two kinds of the CNTs to achieve the best device performance. The differences in electrical, chemical and optical properties make it possible to separate the two kinds of CNTs. Some level of control during growth has been achieved,[165,166] however, the post-synthesis purification methods seem to be more promising.

Electrical breakdown is a method usually used on CNTs TFTs based on a mixture of m-CNTs and s-CNTs. The CNTs are in "OFF" state under gate bias, and a bias between the source and drain electrodes will induce current through the metallic nanotube paths, thus selectively burned these paths. This technique can increase the ON/OFF ratio up to 10^5, without reducing the ON current substantially. The challenge of this method is to implement it on large scale wafer or complex circuit design.

Another type of purification methods which has been extensively studied is ***flow-based sorting***, including electrophoresis, chromatography and ultracentrifugation based methods.[167-172] The CNTs are suspended in solutions, wrapping with surfactant, charged polymers or DNAs, as shown in Figure 3.7 (a) and (d). The m-CNTs and s-CNTs will

have different packing density of the CNT-polymer complexes, thus the separation by ion-exchange chromatography or ultracentrifugation is possible. The > 99% semiconducting or metallic nanotube enriched solution has been achieved in many research labs,[173,174] also commercial available.[175] With ultracentrifugation, the buoyant density is influenced not only by the type of CNTs, but also the chirality, diameter and length, depending on the nature of the surfactant and functionalization chemistries, as illustrated in Figure 3.7 (b) and (c).[173,176] Zheng and colleagues demonstrated that 20 DNA molecules each can bind with specific CNT (n, m) with specific affinity.[177] CNTs can also be sorted by length with DNAs[178] and amino acids[179,180]. With continuing research and effort, it can be anticipated that the purification of CNTs can eventually provide monodisperse CNT solutions with selective electronic or other properties. This will significantly benefit the fundamental research of CNTs properties. The major challenges then remain are the cost, yield and reproducibility of the CNTs purification, especially for industry applications.

Another difference between the m-CNTs and s-CNTs is the chemical reactivity, which makes another separation strategy possible, ***wet etching***. This is because the m-CNTs and s-CNTs have different density of states near the Fermi level, which leads to different stability in chemical reactions.[181-183] Experiments and calculations show m-CNTs are more chemically reactive than s-CNTs. For example, with certain concentration, diazonium can selectively react with only m-CNTs and render them insulating, without affecting the s-CNTs.[181,184] This method can also be used after deposition, and the TFT achieved 10^5 ON/OFF ratio.[185]

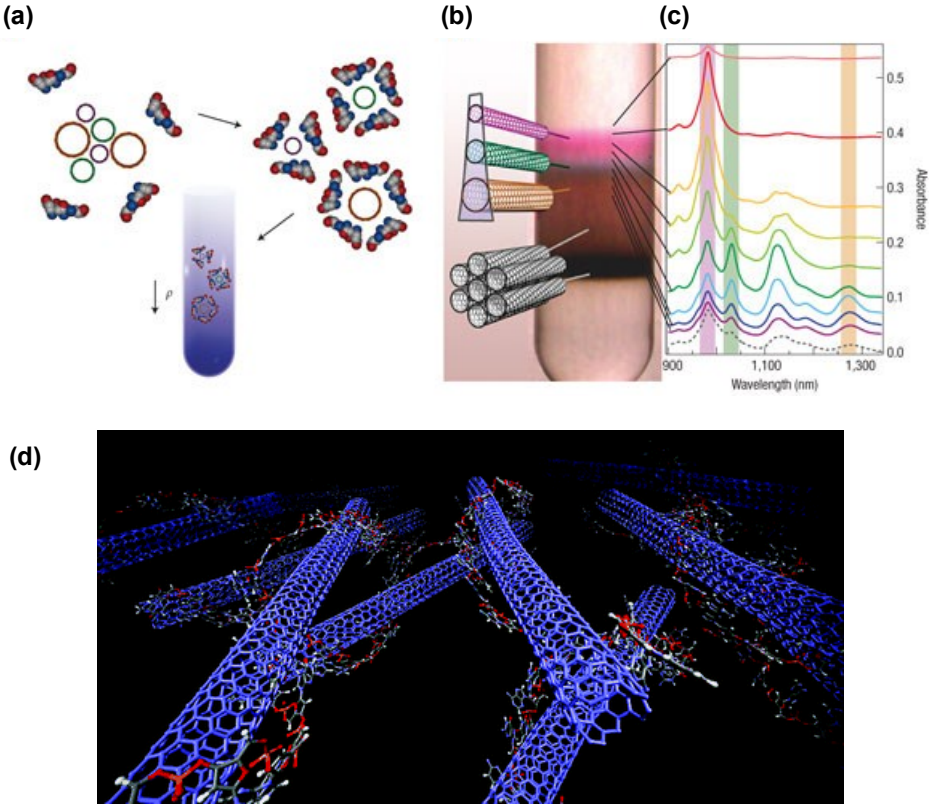

Figure 3.7 Suspension and purifications of CNTs. (a) schematic of surfactant wrapping the CNTs and sorting based on density (ρ). (b) and (c) optical image and absorption spectra of CNTs/Sodium Cholate (SC) suspension after density gradient ultracentrifugation (DGU).[173] (d) schematic of DNA-wrapped CNT network.[178]

3.2.5 CNT Network

The previous discussion of band structures and electronic properties are based on single nanotube. When the CNTs form a network, the electronic properties will become difficult to explore because of various parameters. For example, in a network contains both semiconducting and metallic nanotubes, which is generally true for all cases, there will be a mixture of chirality and electrical characteristics depending on the percentage of the purity. The CNTs network contains metallic and semiconducting nanotubes. The

metallic nanotubes can be modeled as always "on", with a constant resistance. The semiconducting nanotubes can be modeled as either "on" or "off" depending on the gate bias. Early work simulates the conductivity of CNTs network based on percolation theory, assuming the sample is infinite and the tube-tube conductance is perfect.[186] Alam and colleagues took into account the sample size and the finite tube-tube conductance ($0.1\ e^2/h$)[186,187] In addition, the distribution of nanotube lengths and diameters, nanotube-nanotube junctions, network density and the level of alignment all affect the network characteristics. In terms of the device performances, there are additional parameters to consider, such as the ratio between channel length and nanotube lengths, the nanotube-electrode contact resistances, quantum capacitance (especially in FETs), etc. Given so many variables, the current work in electronics based on CNT networks are mostly based on experimental and phenomenological studies.

3.3 Electronic Devices Based on CNTs

Many interesting and attractive applications based on CNTs have been demonstrated or studied in the past decades. The unique electronic, mechanical, and chemical properties of CNTs, such as high mobility, high tensile strength and elastic modulus, large surface area, etc., continuously drive increasing attentions. This section reviews some of the applications based on CNTs electronic properties.

As mentioned above, the electron mobility in CNTs is much higher than conventional semiconductor, such as silicon, which makes CNTs an attractive semiconductor material. Furthermore, the CNTs have been demonstrated with good compatibility of flexible

electronics, in which area most materials suffer the low mobilities. Figure 3.8 illustrates how the CNT mobility compared to organic semiconductors. Single CNT is an ideal candidate for semiconductor electronics, with high ON/OFF ratio (10^6) and mobility (10,000 cm^2/Vs). CNT networks possess lower mobilities compared to single nanotubes, yet much higher than organic semiconductors and amorphous silicon and compatibility to flexible applications. The ON/OFF ratio of CNT network depends on level of purification, fabrication methods, device parameters, etc.

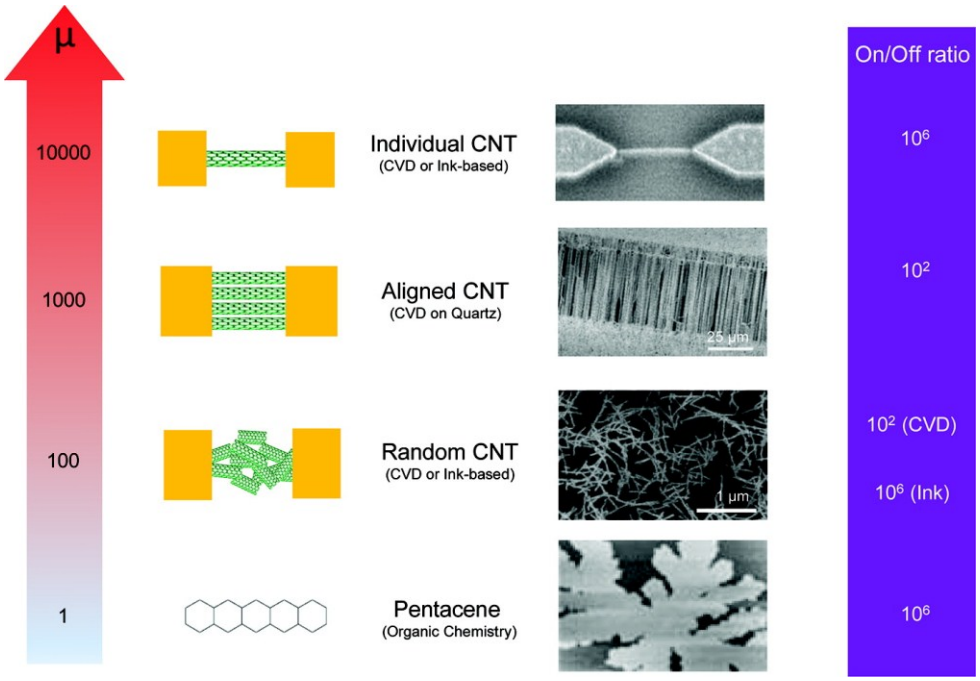

Figure 3.8 Mobility and ON/OFF ratio trend and comparisons for nano-transistors.[188]

3.3.1 Thin Film Transistors Based on CNTs

The first field-effect transistors (FETs) based on CNTs were reported by Dekker and Avouris at 1998.[189,190] Typically, CNTs are grown on top of dielectrics (such as SiO_2),

making contact to metal source/drain electrodes (such as Au, Pt). The CNTs can be tuned from the insulating state to conductive state by the gate bias. Charge carriers can then be injected into the nanotube through source electrode and conduct electric current. As shown in Figure 3.9, the negative gate bias may flatten the valence band of the nanotube and switch the nanotube into conductive state (in this case, for holes), and the positive gate bias bends the band more and deplete the holes which switch the nanotube to the insulating state.

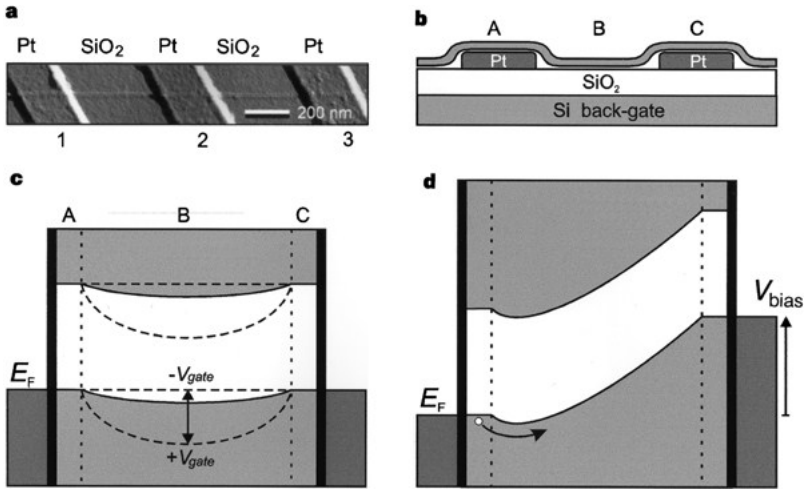

Figure 3.9 FETs based on CNTs. (a) AFM, (b) schematic of the thin film transistor based on CNTs. (c) band diagram of the gating effect of the transistors. (d) effect of drain bias on suppressing the contact barrier.[189]

Although the characteristics of CNT FETs can be explained and modeled by the band theory in conventional MOSFETs, there are a number of differences between the CNT FETs and conventional MOSFETs. First of all, the CNT FETs operate mostly under accumulation mode not depletion mode. The charge carriers are injected from the source

electrode. Since the energy band gap of semi-CNTs are small, the CNT FETs often behave as ambipolar FETs, as shown in Figure 3.10, as long as the contact barrier at both source and drain electrodes are low. For some applications, ambipolar transistors have their own advantages, while some other applications may prefer unipolar transportation. The type of transportation is affected by the chemical doping of the CNTs,[191-193] the Fermi level of contact metals,[194-196] the dielectric materials,[82,197,198] etc.

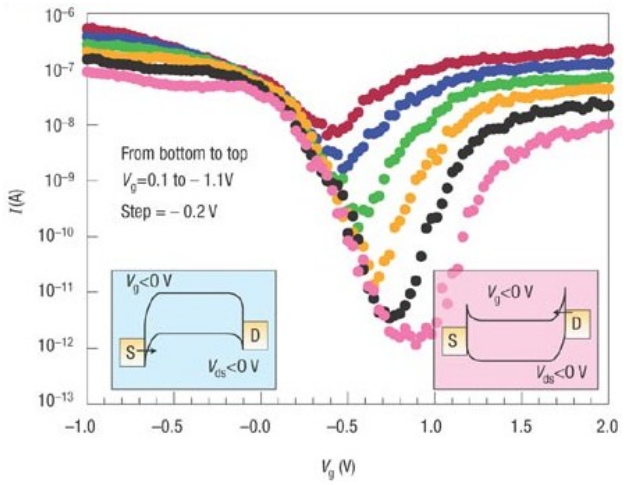

Figure 3.10 Ambipolar transportation of FET based on CNTs. Left inset shows the p-type transportation (hole) under negative gate bias. Right inset shows the n-type transportation (electron) under positive gate bias.[108]

In CNT FETs, the quantum capacitance C_Q, which is the capacitance related to the density of states, is small (~10^{-10} F/m).[199] In conventional MOSFETs, the gate capacitance, C_G, is smaller than C_Q. Therefore, the gate capacitance is the dominant factor controlling the band diagram of semiconductor layer. However, in some CNT

transistors (scaled down or using high dielectric constant materials), $C_Q \sim C_G$, or even $C_Q < C_G$, hence the quantum capacitance may become dominant.

3.3.2 Scaling of CNT FETs

Due to the quasi 1-D structure of CNTs, the scaling effect of the CNT transistors is different from conventional MOSFET. In conventional devices, the key performance parameters, e.g., mobility, is usually independent of the dimensions of the semiconductor layer. However, in CNT FETs, the average length of nanotubes, ratio of nanotube length to channel length, density, purity, and alignment may all play a role in mobility and ON/OFF ratio. Some study in CVD grown, aligned CNT network, shows that the mobility increases with the channel length, which might include the contact resistance effect.[200] There are also other reports about the scaling effects of channel length on mobility, suggesting the dependence may be weak.[201-204] Currently, the channel length dependence of mobility is not fully understood theoretically.

The coverage density of CNT networks has a strong impact on the mobility and ON/OFF ratio, especially on the as-grown CNT networks grown by CVD. For unpurified CNTs, due to the presence of metallic nanotubes, when the m-CNTs are below the percolation threshold while the s-CNTs are above the percolation threshold, the network may achieve the optimum ON/OFF ratio.[28,205] Sangwan and colleagues found, using Monte Carlo simulation, the ON/OFF ratio had a transition around 0.2 ~ 0.3 CNTs/μm^2.[205] For purified CNTs, the ratio of m-CNTs is much lower (up to 2 orders) than unpurified CNTs, which will be below the percolation threshold in most of the

networks. The dependence of the ON/OFF ratio on purified network density was studied by a couple of groups.[201,206] The density dependence of purified network is less significant than unpurified one,[188] which could be due to the purification, the difference of nanotube length and chemistry.

In general, the higher density of the network, the higher the mobility and lower the ON/OFF ratio will be. Burke et al. summarized the mobility and ON/OFF ratio in the CNT networks in their review paper based on all recent studies, as shown in Figure 3.11.[188] The network based on unpurified CNTs (red and green) lines showed a clear transition due to the high ratio of metallic nanotubes, while the purified network showed similar but smoother trend. This plot illustrated the relationship between the ON/OFF ratio and mobility in CNT networks. Despite the CNT properties (length, chirality, and diameter), fabrication methods, device architecture, etc., are different from one research group to another, the trend is clear. Additionally, the purified CNT networks showed improved mobility and ON/OFF ratio. It worth to note that, currently the studies seemed to be phenomenologically, however, a roadmap for practical applications may be established with further fundamental studies.

One of the attractive advantages of CNT based electronics is their potential on flexible, transparent electronic applications.[207] Transparent, conductive CNTs film can be fabricated by vacuum transfer method on wafer scale.[163] Rogers group also demonstrate bendable TFT arrays patterned by transfer printing (a dry printing technique), with effective mobility up to 30 cm^2/Vs.[122] In addition to these, the transparent conductive CNT film also provides potential application in optical electronics, such as organic light

emitting diode (OLED) and organic photo-voltaic devices (OPV), since CNT is a good contact material to organic semiconductors.[208] In Chapter 7, a printed transparent CNT thin film functions as a good contact electrode to the electrochromic devices.

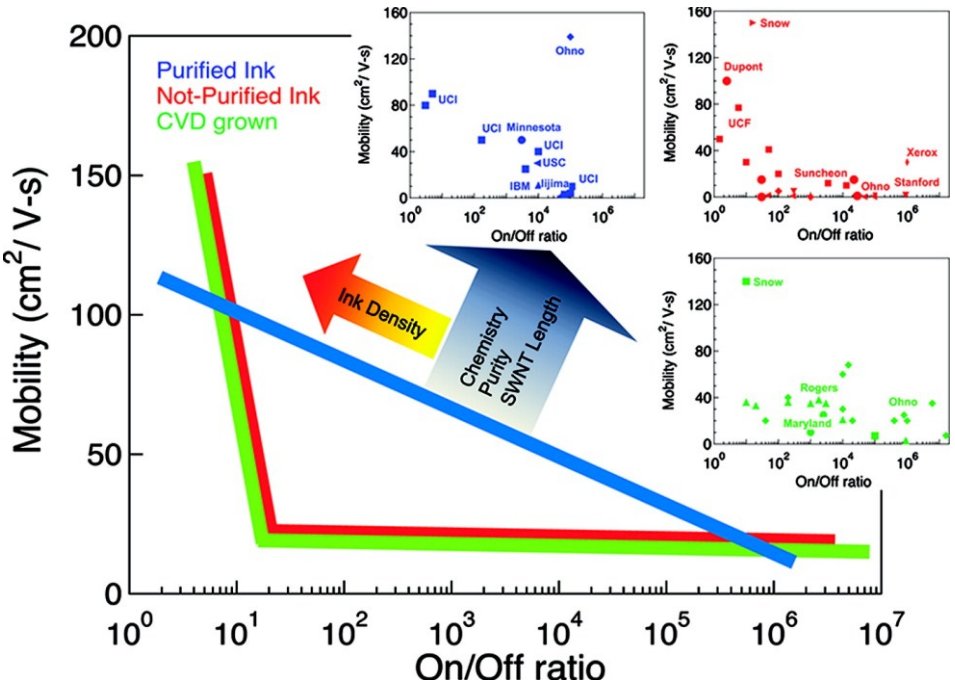

Figure 3.11 Mobility and ON/OFF ratio of CNT network. Solid blue line is for purified inks, red and green lines are for unpurified inks and as-grown networks. The data points of each method are shown in the insets.

3.3.3 CNT Circuits and Other Applications

Thanks to the high mobility, CNTs have been considered as a good candidate of next generation semiconductor electronics. In the area of high frequency applications, Avouris and colleagues demonstrated a 5-stage CMOS ring oscillator based on a single CNT in 2006, which achieved 52 MHz frequency (Figure 3.12).[194] The ring oscillator used an 18μm long s-CNT as the semiconductor, Al_2O_3 as dielectric, and Pd as the gate of n-FET,

Al as the gate of p-FET. Each stage includes one n-FET and one p-FET to form a CMOS inverter.

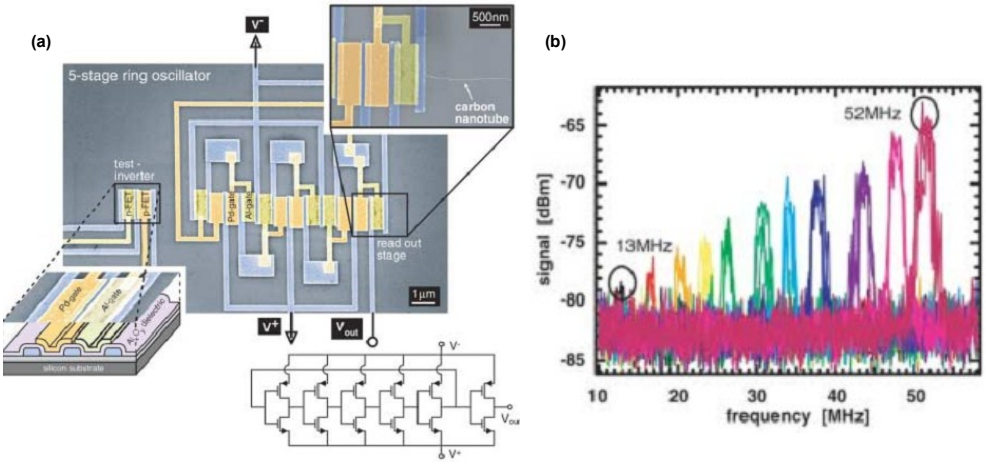

Figure 3.12 A 5-stage ring oscillator fabricated on a single CNT. (a) SEM image of the 5 stages of CMOS inverters. (b) Voltage-dependent frequency spectra.[194]

Dai's group also demonstrate thin film transistors (TFTs) and digital circuits based on individual CNTs. [209] CNTs were CVD grown on substrate which was pre-patterned with bottom W gate electrode, molybdenum source and drain electrodes, and catalyst. The grown CNT bridged through the source and drain electrodes and formed semiconducting transistors (~70% of the transistor array). The TFTs are p-type as fabricated, but can be turned into n-type with desorbing of oxygen in vacuum. By wire bonding several transistors together, the team achieved NOR, OR, NAND and AND logic gates. The three-stage ring oscillator showed 220 Hz frequency and 0.75ms stage delay time. There are a few disadvantages of circuits based on individual CNT. First of all, the fabrication process requires many challenging steps which are unlikely to be compatible with low-

cost, flexible electronics. In addition, the variation from device to device is too large to applications. This is mainly due to the distribution of as-grown CNTs, such as diameters, length, chirality, types, etc. Therefore, this type of devices may be a great platform to study the CNTs properties, but not necessarily a promising direction of CNT applications. This brings to the attention the electronics devices based on arrays of CNTs.

RF devices: Application in radio frequency (RF) devices is one of the advantages of CNTs due to their high intrinsic mobility (~10^4 cm^2/Vs), small capacitance (~100 aF/mm), and nanometer-thick channel. The aligned CNT arrays grown on quartz substrate showed most promising performance. The cut-off frequency for TFTs can be up to 10 GHz, with low density CNT film (5 CNT/μm).[210] RF power amplifiers which can be integrated with a functional analog electronic system have also been explored.[211] The CNT TFTs achieved >1 power gain in very-high-frequency range. Another component of analog RF system, oscillators, achieved 500 MHz with devices based on CNTs.[212]

Gas sensors: CNT consists only with surface atoms, which makes it extremely sensitive to surface environment, such as the chemistry change. These changes can be reflected by the electronic property of CNTs, and be sensed by resistors, transistors or capacitors based on CNTs. CNT array is usually used in sensor devices in order to enhance the signal to noise ratio and achieve the reproducible performance. A simple chem-resistor can be used to detect the presence of certain toxic gas in ppb level.[213] With gas molecules absorbed to the surface defect points, the apparent resistance of CNT will change which is due to the charge transfer between the absorbed molecules and the

valence band of CNTs.[214] The stronger electron donating or withdrawing capability the molecules have, the larger change of CNT resistance will be. However, there are two major drawbacks of CNT gas sensors. First, the specificity is low, since many molecules can be absorbed and result in similar effect. Certain type of functionalization can be helpful.[215,216] Second, the recovery process is usually slow due to the slow desorbing process. Using TFT type of device can speed up this process by applying gate voltage.[213]

Biosensors: CNTs have been demonstrated with good potentials in biosensor area. As previously mentioned, charged large molecules, such as DNAs and proteins, can bind to the surface of SWTN, and alter the conductance of CNT thin films. Similar as the gas sensors, CNT can be fabricated as resistors or transistors to provide a label-free detection of bio molecules.[217,218] The detection limit can achieve picomolar- or even femtomolar-level.[219,220] By pre-coating the device with some antigens, selective detection is also possible.[219]

Chapter 4 Printed and Flexible Circuits and Applications

4.1 Introduction

Any material can be flexible when its thickness comes down to a certain scale. The concept of flexible electronics started decades ago, when the solar cell devices based on single crystal silicon scaled down to ~ 100 μm and exhibited the flexibility to be assembled on plastic substrates.[221] Later on, the hydrogenated amorphous silicon (a-Si:H), which can be deposited at low temperatures, enabled the direct fabrication of solar cells on flexible substrates.[222] Since 1980s, the roll-to-roll fabrication of a-Si:H on flexible metal foil and plastic substrate has been introduced and widely used in industry.[223] Flexible thin film transistors (TFTs) and circuits also date back to 1960s,[224] and developed wide applications including the backplanes for active-matrix liquid-crystal display (AMLCD), flexible LCD, and flexible organic light-emitting diode (OLED) display.

This chapter reviews the fabrication techniques of flexible transistors, circuits and their applications, with a specific focus on the printed electronics. In addition, the recent progresses on flexible electronics are also reviewed, such as the circuit performance, demonstration of complementary circuits, and applications in large area display, RFID tags, etc.

4.2 Fabrication of Flexible Circuits

There are different levels of flexibility in flexible electronics, including bendable, conformally shaped, elastic/stretchable, roll-to-roll manufacturable, etc. Over the decades of researches, flexible electronics have been demonstrated based on inorganic materials, such as a-Si, compound semiconductors, and nano-materials, as well as organic materials, such as small molecules and polymers. These materials can be directly grown on the flexible substrates, assembled after, or fabricated directly by solution-based processes. This section briefly reviews the experimental works of the flexible electronics based on various fabrication methods.

4.2.1 Deposition Methods from Gas-phase

The direct growth fabrication methods are similar as in the conventional semiconductor industry, such as the chemical vapor deposition (CVD) approaches. The challenge of this type of techniques is the trade-off between the process temperatures and the semiconductor film qualities.[225] With the limits of process temperatures not exceeding the glass transition temperature of the polymer-based substrates, the thin films usually could not achieve large scale of crystallinity. In addition, many steps of the growth process and following fabrication processes do not easily scale to the large areas.

Inorganic semiconductors: Amorphous silicon is a semiconducting material most widely employed in the large area applications, by far. Typically, high-quality a-Si films require relative high temperature (> 250 °C) during deposition, but low-temperature processes are demonstrated.[226-228] For example, TFTs fabricated on PET substrate by RF-

PECVD at temperatures < 100 °C showed mobilities around 0.4 cm^2/Vs and ON/OFF ratio > 10^5.[229] The qualities of the a-Si:H films fabricated under low temperatures can be significantly improved by post-deposition processes which transform them into poly-crystalline silicon films, including solid-phase crystallization, excimer-laser annealing, or sequential lateral solidification.[230] These process can lead to large-grain films and good performance, such as TFTs with mobilities >60 cm^2/Vs after annealing at 650 °C.[231]

In addition, compound semiconductors can also be deposited at low temperatures onto flexible substrates, by radiofrequency magnetron sputtering and pulsed-laser deposition. For example, ZnO films deposited on flexible polyimide substrate by pulsed-laser deposition were demonstrated,[232] although the transistors based on ZnO were mostly studied on glass substrates.[233] Hosono's group demonstrated TFTs based on amorphous In-Ga-Zn-O films and achieved mobilities > 6 cm^2/Vs.

Organic semiconductors: Although the electrical performance is lower than crystalline silicon, organic small molecules and polymers are attractive alternatives for flexible electronics, due to their mechanical flexibility and compatibility to low temperature process. The major challenge of organic semiconductors is the lower mobility (detail discussions are in section 2.1), however, many promising results have been demonstrated in the last decades.

Single crystal small molecules can be grown from solution, or physical vapor transport (PVT) method. The single crystal materials can achieve relative high mobilities, e.g., the mobility of Rubrene single crystal can achieve up to 20 cm^2/Vs.[44] Fabrication of transistors based on these materials is usually difficult to apply on integrated circuits.

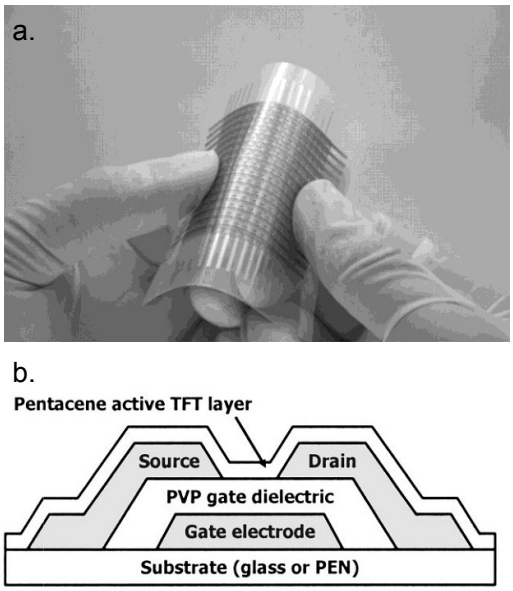

Figure 4.1 Flexible OTFTs based on Pentacene. (a) an array of OTFTs fabricated on polyimide substrate.[234] (b) the scheme of typical flexible transistor with evaporated Pentacene.[235]

Thermal evaporation of organic small molecules is a method compatible to conventional photolithography. Kane et al. reported Pentacene OTFTs and circuits fabricated on polyester film.[236] The Pentacene was deposited by thermal evaporation at about 60 °C, achieved mobility 0.03 – 0.45 cm^2/Vs. The operation voltage range is 20 V. With yield of 65%, they were able to fabricate digital circuits including frequency divider, differential amplifier, and ring oscillator. Klauk et al. later compared the performance of Pentacene OTFT and ring oscillators fabricated both on glass and polyethylene naphthalate (PEN) film.[235] Due to the higher roughness of PEN substrate, the trap density of Pentacene might be higher and resulted in slightly lower mobility (0.3 cm^2/Vs on PEN, 0.7 cm^2/Vs on glass), higher threshold voltage and subthreshold swing. Someya et al. reported OTFTs on large area (8 × 8 cm^2) polyimide substrate, where all of

materials are soft except the electrodes.[234] Examples are shown in Figure 4.1. The Pentacene layer is deposited in the vacuum sublimation system, and can achieve mobility higher than 1 cm^2/Vs, which is comparable to amorphous silicon. However, the OTFTs require large bias voltage (~ 100 V).

4.2.2 Transfer-printing

Transfer-printing is a type of "dry printing" methods that assembles the high quality semiconductor materials to avoid the incompatibility between the growth methods and flexible substrates. For example, high performance single-crystalline silicon wafers can be patterned into microstructures semiconductors, and then transferred to flexible substrates or other substrates and fabricate circuits based on them. Roger's group first demonstrate this in 2004 and reported following studies.[1,237-240] Fist, the silicon wafer is patterned and etched by reactive ion etching into thin strips, which can be then released and transferred to flexible substrate by PDMS stamps, as shown in Figure 4.2. The transistors achieved mobilities of 500 cm^2/Vs, and ring oscillators showed MHz frequency (Figure 4.3). With the same concept, other compound semiconductors can be also fabricated.[241] Transfer printing minimizes the thermal exposure to flexible substrates, thus good circuit performance can be achieved at low temperatures. However, there might be some limitations of the substrates since the transfer process requires the surface energy to be different between the carrying media and substrate surface. In addition, the cost might be a bottle neck since complex photolithography processes are involved.

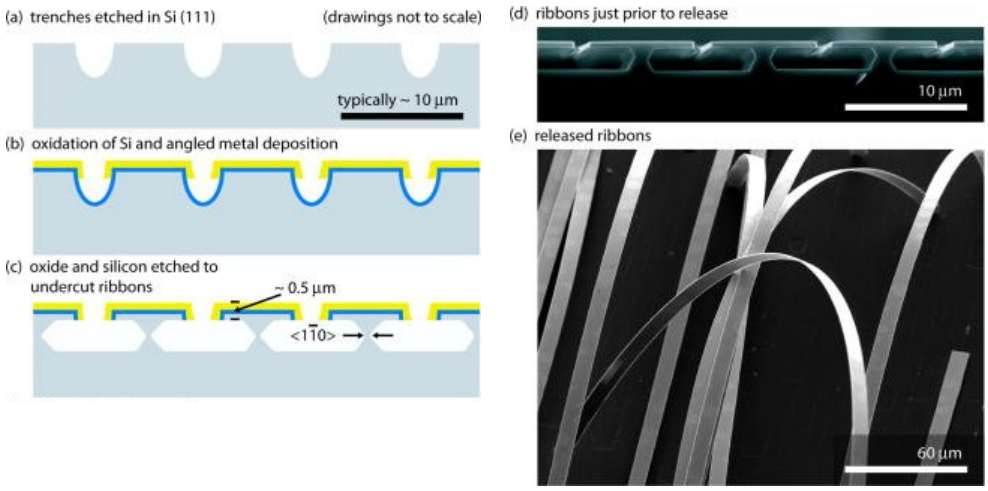

Figure 4.2 Schematic process flow of single-crystal silicon ribbon fabrication. (a) plasma etch. (b) passivation of the sidewalls. (c) undercut of the Si ribbons. (d) Cross-sectional SEM image of partially undercut ribbons. (e) Released, flexible ribbons.[242]

In addition, nanowires or other nanostructures of semiconductors can also be synthesized and then transfer print onto flexible substrates. The work on circuits by transfer printing of carbon nanotubes is reviewed in section 3.2.2.

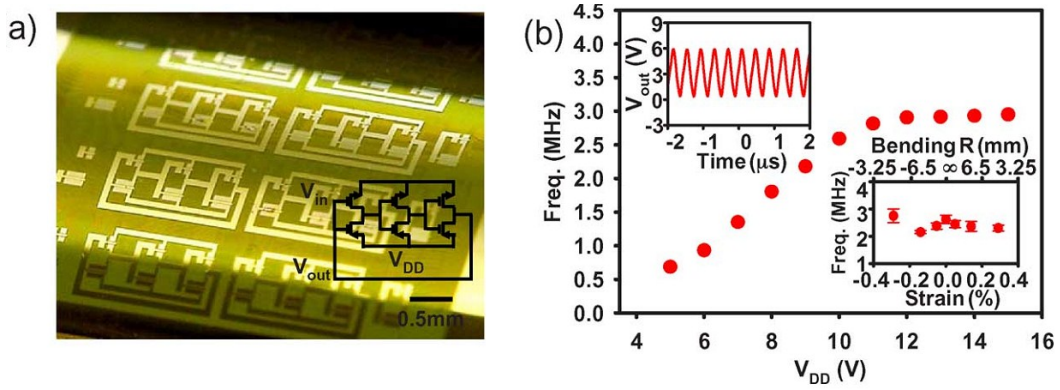

Figure 4.3 Ring oscillators based on ribbon of silicons. (a) image of an array of ring oscillators patterned on flexible substrate. (b) output performance of ring oscillators.[240]

4.2.3 Deposition Methods from Liquid-phase

Previous sections review the fabrication methods which mostly based on gas phase, such as evaporation, sputtering, CVD, etc. Another attractive route to achieve flexible electronics is the solution-based processes, such as spin-coating, drop-casting, and additive printing. The printing process will be discussed in details in section 4.3 since it is a major focus of this thesis.

The solution-based process is cost-effective, low temperature, and easy to scale up to large areas. Almost any materials that can be prepared in solutions or suspensions, such as polymers, small molecules, and nanostructures of materials, are solution processable. The first all-polymer OTFT integrated on plastic substrate is reported by Philips Research Labs in 1998.[243] The transistors were fabricated by spin coating of electrically active precursors on polyimide foil and patterned by exposure of UV light through masks. The p-type transistors with 2 μm channel length and 2 mm channel width achieved mobility of 2×10^{-4} cm^2/Vs. The authors were also able to demonstrate a 15-bit code generator integrated of 326 transistors.

Small molecules (or precursors) and oligomers can be dissolved and then deposited on substrates by drop-casting or spin-coating.[244] For example, many interesting Pentacene derivatives and precursors have been studied and demonstrated solution-processable, with hole mobilities as high as 1 cm^2/Vs.[245,246]

Solution processed films are often considered to have relative lower quality due to the variation of thickness (especially dielectrics), roughness, morphology, etc. Many

researches try to address these challenges and improve the device performance. For instance, it appeared that the grain boundary orientation in drop-casted small molecules thin film has modulation of carrier transport,[247] hence controlling the crystallinity of the semiconductor film can further improve the device performance.[248] The interactions between semiconductor and dielectric layers are also intensively studied.[249]

It is often challenging to pattern the organic films in the solution-based depositions. In addition to the photochemical patterning described above,[243] some studies employ hybrid structures, e.g., organic semiconductors together with inorganic conductive and dielectric layers which can be patterned by standard photolithography, and define the organic layers by etch masks and plasma etching.[250,251] Soft lithography using prepatterned elastomeric materials, such as PDMS, to transfer micrometer or nanometer scale structures, has been demonstrated in fabricating OTFTs.[252-254]

4.3 Printing Techniques for Electronics

Printing is fast-speed, low-cost, and additive technique for flexible electronics. The conventional paper printing is widely used every day, with printing speed up to 100 km/h. The methods of printing electronic materials share the same concepts of printing, but are more sophistic than that. In conventional newspaper printing, the "printing quality" usually refers to resolution and registration of pigment dots. There are a lot more to consider when printing functional electronics. Electronic devices consist of multiple layers, and each has its own specifications of "quality". For example, conductive layer need to be continuous and low-resistance; dielectric layers require uniform thickness

without pinholes; and semiconductor layers may require more control over film thickness, morphology and alignment for optimized performance.

Traditional printing techniques include Gravure, flexography, offset, and screen printing, which all can be used in Roll-to-Roll (R2R) process. Digital printing techniques, such as ink-jet printing and aerosol jet printing are also well developed in flexible circuitry fabrications. The key parameters of common printing techniques are compared in Table 4.1. Details of these printing techniques are described below.

Printing technique	Print resolution [μm]	Print speed [m min^{-1}]	Wet film thickness [μm]	Ink viscosity [mPa s]
Flexo	30–75	50–500	0.5–8	50–500
Gravure	20–75	20–1000	0.1–5	50–200
Offset	20–50	15–1000	0.5–2	20 000–100 000
Screen	50–100	10–100	3–100	500–50 000
Inkjet	20–50	1–100	0.3–20	1–40

Table 4.1 Comparison of common printing techniques. [255]

Flexographic printing. In flex printing, a flexible plate carried the printing patterns is attached to a cylinder. The plate is usually patterned by photolithography in the way that the image area is raised above the non-image areas. The plate surface is inked when in contact with an anilox cylinder surface which is previously inked. And the pattern is finally transferred to substrate by the plate cylinder (Figure 4.4 a). Flex printing is used in printing conductive materials, OTFTs, and organic circuits.[17,256-258]

Gravure printing. Gravure printing, also known as rotogravure printing, is one of the most widely used printing techniques for flexible electronics, include organic solar cells, organic light-emitting diodes, and OTFTs.[257-261] As shown in Figure 4.4 b, the gravure cylinder picks up the inks from fountain when it rolls. A doctor blade removes the excess ink from the cylinder surface before it is in contact with the substrate, which is sandwiched in between the impression roller and the gravure cylinder. The patterns, which are engraved on the gravure cylinder by lithography or chemical etching, are printed on the substrate.

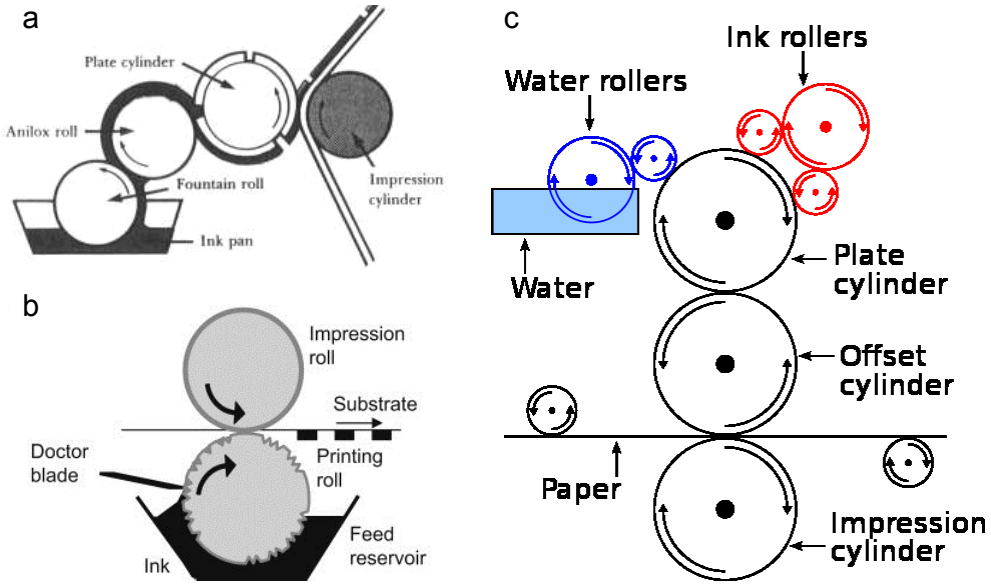

Figure 4.4 Common printing process. (a) Flexographic printing,[262] (b) Gravure printing, [259] (c) Offset printing,[263]

Offset printing. Offset printing is a common printing technique but there are some limitations for printed electronics. This technique employs several cylinders to transfer the ink so the ink can be evenly distributed. The resolution and printing quality of this

technique can be good since the rubber offset cylinder can make a conformal contact to the substrate, as shown in Figure 4.4 (c). This technique is a fast-speed and low-cost printing method, but the demonstration in printed electronics is rare.[264,265]

Screen printing. Screen printing is often used as a flat printing technique, but is adaptable to R2R process. Typically, a high viscosity ink is dragged across the surface of a mesh screen and squeezed through the patterned pores onto the substrate. The printing resolution and quality depends on the ink viscosity and pores density. Screen printing can print relatively thick layers, which is an advantage for conductive layers.[260,266]

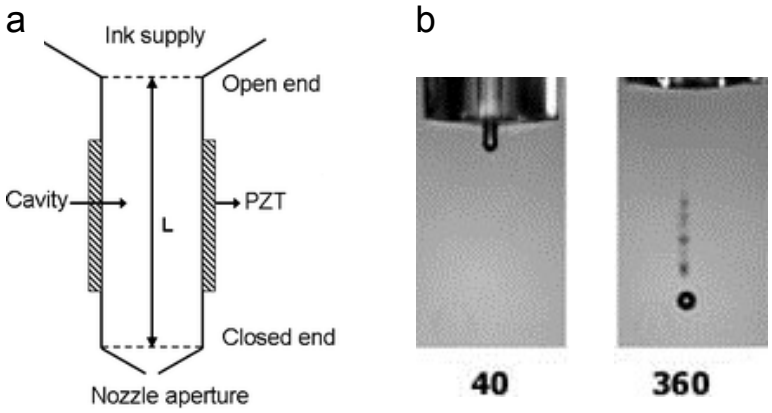

Figure 4.5 Ink-jet printing mechanism. (a) Typical printhead of ink-jet printer. (b) Pictures of a droplet ejecting from the printhead, after 40 μs and 360 μs after the voltage pulse, respectively.[267]

Ink-jet printing. Ink-jet printing has been intensively studied in the area of printed electronics recently, and its application in printed solar cells, antennas, and OTFTs are demonstrated.[267-270] It typically employs the low viscosity inks and piezoelectric drop-on-demand printhead, as shown in Figure 4.5. When a voltage is applied to the piezoelectric

actuator, a sudden volume change in the capillary pushes a droplet of ink out of the nozzle. The surface energy of the droplet, the friction of ambient air, and the voltage applied all affect the speed of the droplets. The major advantage of the ink-jet printing is the low-cost, and digital programmable printing patterns. On the other hand, the ink viscosity, printing speed, and the evaporation kinetics of printed inks often result in complicate interactions, and affect the printing resolution and quality.[271,272]

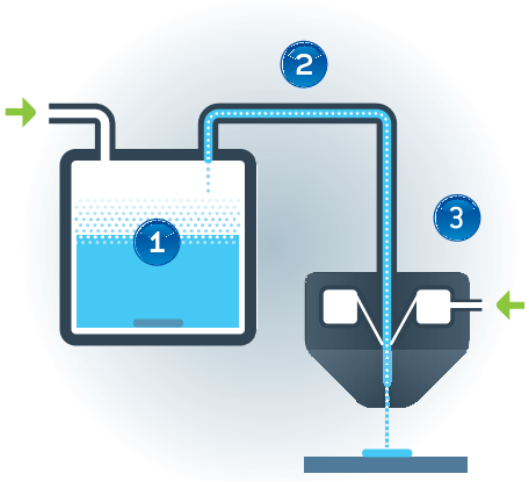

Figure 4.6 Scheme of aerosol jet printing. 1. liquid ink is atomized and a dense aerosol is created. 2. The aerosol is transported to print head by a carrier gas. 3. Aerosol is focused by a sheath gas and pushed out with a high velocity.[273]

Aerosol jet printing. Aerosol jet printing is also an additive digital printing technique which has been demonstrated in functional printing recently. Instead of the liquid ink itself, it prints a dense aerosol which is created from liquid inks. The aerosol is transported to the print head by a carrier gas and focused by a sheath gas at the head. The droplets, which dimensions are between 1~5 μm, are then pushed out with a high velocity

and deposited on the substrate, as shown in Figure 4.6. The printing mechanism of aerosol jet printing is different than ink jet, where the aerosol is carried by a gas flow. This brings several advantages: 1), printing speed can very high (200 mm/s). 2), the standing distance between the head and substrate can be several millimeters, since the distortion from the ambient air is negligible. 3), the focus sheath gas provides the flexibility of printing line width. In addition, aerosol jet printing can accommodate a wide range of ink viscosities.

4.4 Performance and Applications of Flexible and Printed Circuits

4.4.1 Operation Speed of Flexible and Printed Circuits

Clock frequency is one of the key performance parameters in electronics, which indicates how fast the circuits can operate. Ring oscillator, a series of inverters, is used to generate a spontaneous oscillating signal (Figure 4.7). The time it takes for a signal to pass through one inverter stage is usually referred as stage delay time, which is given as $t_D=1/2Nf$, where N is the number of stages, and f is the output frequency. This time constant is often considered as a benchmark of circuit speed, which reflects limitations of both intrinsic materials properties and device architectures.

Figure 4.8. summarizes the stage delay time of ring oscillators acquired from non-printed (evaporated, spin-coated, etc.) organic circuits, printed organic circuits, and printed circuits based on non-organic materials, displayed as a function of supply voltage. Although the data summarized here are not all demonstrated with flexible substrates, these studies are potentially adaptable for flexible applications.

Organic semiconductors, which are good candidates to be used in flexible electronics, have relatively low mobilities compared to conventional semiconductors. For non-printed organic circuits, delay times less than 10 μs have been obtained only with 10 V or greater supply biases,[274-282] and the delay times for circuits operating at battery voltages are above 30 μs.[22,23,283-285] Printed organic circuits are generally much slower (with ms delay time) and require high supply voltages (tens of volts),[9,264,286-288] which are further limited by the printing resolution due to large source-to-drain channel. Some groups are investigating transfer printing[1,28-32] or jet printing[9,33-38] of high mobility semiconductors, e.g., silicon, oxides, nanowires, graphene and carbon nanotubes (CNTs), and these efforts have the potential to produce low voltage circuits operating at high speed.

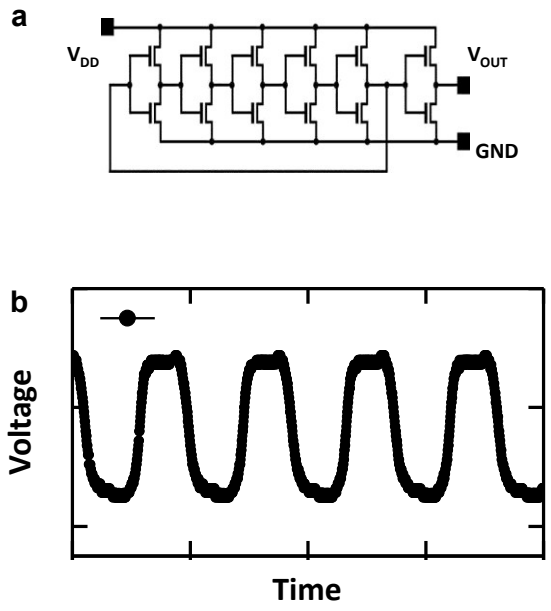

Figure 4.7 Circuit diagram of a typical ring oscillator and its output.

The large voltages are not practical for many potential applications of flexible electronics where power will be supplied by thin film batteries or radio-frequency fields. Very recently, unipolar, p-type electrolyte-gated ring oscillator circuits have been demonstrated that indeed operate at very low supply voltages (brown symbols), but the shortest delay times were 200 μs for devices with rather short (2.5 μm) channel lengths.[25,289] Thus, a major challenge for printed electronics is to develop inks and printing methodologies that allow shorter delay times at low supply voltages, *i.e.*, to move further into the pink shaded region of Figure 4.8.

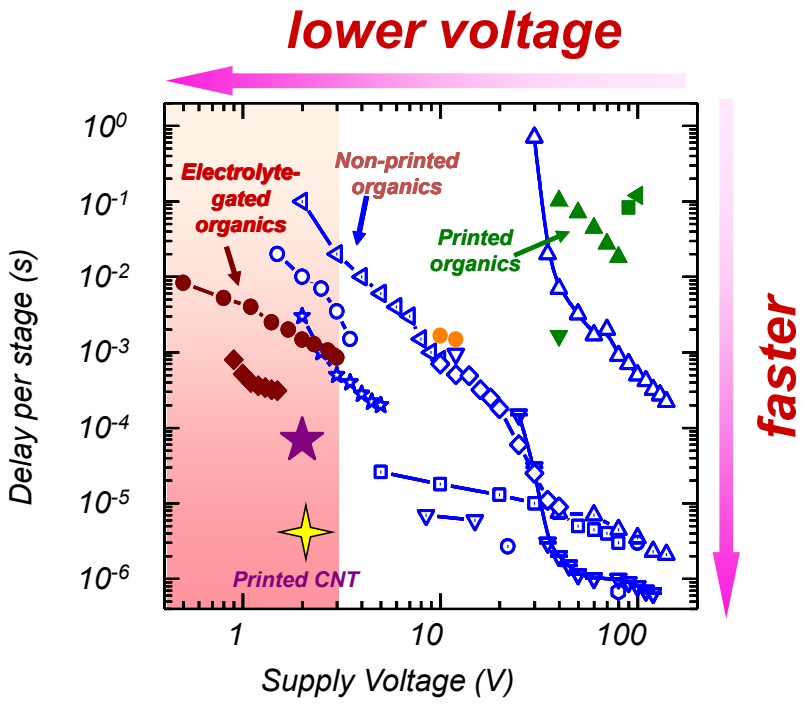

Figure 4.8 Stage delay time of ring oscillators. Blue open symbols represent the non-printed organic ring oscillators; green solid symbols represent the printed ring oscillators; orange symbols are from printed carbon nanotube ring oscillators; brown solid symbols are electrolyte-gated organic ring oscillators. The two star symbols are from the work in this thesis (discussed in chapter 4 and 5, respectively).

4.4.2 Complimentary Circuits: Low Power Operation

The majority of the printed organic transistors and circuits are unipolar, which means only one type of charge carriers transports across the channel. In principle, both electrons and holes should be able to transport in intrinsic organic semiconductors, however, in most organic semiconductors, hole mobility is much higher than electron mobility. The n-type transportation in OTFTs has typically suffered from materials degradation or insufficient operational stability. Therefore, the majority reported printed circuits are based on p-type channels. The unipolar circuits not only have higher circuit complexity, but also much higher power consumption. Complementary circuits, a concept from CMOS silicon circuits, which consists both p- and n-type channels, can truly achieve low power circuits for portable, disposable, and light-weight applications.

Klauk et al. demonstrated a series study on low-voltage, low-power organic complementary circuits. [23,67,275] They employed a low-leakage gate dielectric layer which is a self-assembled monolayer (SAM), and enabled the transistor operation at 1.5 – 3 V. And they fabricated complimentary inverters and ring oscillators with two air-stable organic semiconductor materials for both p-type and n-type transport. Although the devices were demonstrated on glass substrate, the process may also be applied on flexible substrate.

Facchetti et al. demonstrated solution-processed complementary circuits on flexible substrate, based on the air-stable, n-type small molecules developed by Polyera Corp.[290] The spin-coated and drop-casted semiconductor film showed mobilities between 10^{-2} –

10^{-3} cm2/Vs. the complementary ring oscillator showed large output swing, with 75 Hz frequency. They also demonstrated complementary inverters based on a n-type polymer by gravure printing and ink-jet printing.[17] Some groups also studied ink-jet printed, complementary ring oscillators based on polymers.[291]

4.4.3 Other Applications: Displays, RFID, and Sensors

The research on flexible circuits has been motivated due to many promising applications which cannot be easily realized by conventional electronics. The three major applications of flexible circuits are flexible display, large area sensors, and RFID tags.

Display. The most compelling application for flexible circuits is the active matrix displays, including active matrix liquid crystal displays (AMLCDs), active matrix electrophoretic displays, active matrix electrochemical displays, active matrix organic light-emitting diodes (AMOLEDs), etc. The active matrix display requires each display pixel to be driven individually, therefore, it is more costly than passive display.

The first OTFT display was reported in 2001, which was a 16x16 electrophoretic display driven by pentacene TFTs on PET substrate.[292] After that, many groups demonstrated using organic OTFTs as the backplane of flexible displays, including a 10'' electrophoretic display on PET substrate from Plastic Logic, and a 15'' color AMLCD on glass from Samsung.[2,3] OLEDs can also be driven with OTFTs since the voltage is compatible. Using OTFT to drive single pixel of OLEDs was reported in 1998,[293] followed by demonstrations of display matrix on glass substrates.[294,295] In 2005, a 48×48 AMLED displays driven by OTFTs are demonstrated on PET substrate.[4] Recently, our

group reported using printed electrolyte-gated transistors to drive single pixel of OLED, which demonstrated the performance of printed OTFTs is also good for OLED display.[296] Another interesting example of flexible displays is the flexible electrochromic (EC) displays. Several groups have demonstrated active matrix control of flexible electrochromic displays.[15,104,105] The work has been reviewed in details in chapter 2.

RFID. Radio frequency identification (RFID) is a very popular application of flexible electronics. Low-cost, disposable, and low-voltage RFID can replace the optical barcode system which is widely used in supply chain and other areas. RFID based on silicon chips are relatively expensive (>20 cent) for many low cost items, the desired price for printed RFIDs is lower than 1 cent. Heremans et al. demonstrated 128-bit flexible RFID tags based on pentacene by evaporation (Figure 4.9a).[6,297] de Leeuw et al. also presented a 64-bit tag with 1938 pentacene OTFTs on polyimide substrate.[298]

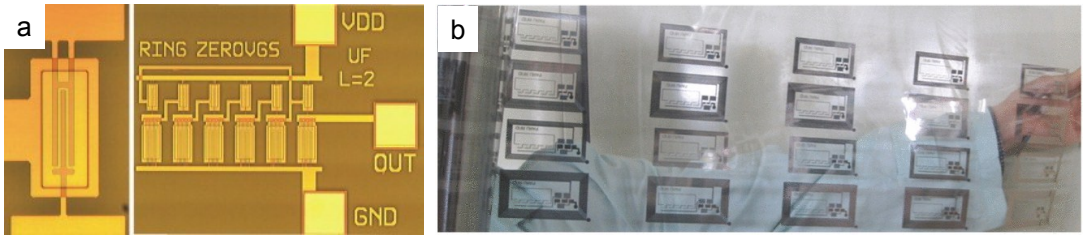

Figure 4.9 Flexible RFID tags. (a) Flexible RFID tag based on evaporated pentacene.[297] (b) all-printed 1-bit RFID tags.[9]

The first all-printed RFID tag is reported by Jung et al., combined gravure, ink-jet, and pad printing techniques, with estimated cost of 3 cents (Figure 4.9b).[9] The transistor and circuits are based on ink-jet printed single-wall carbon nanotubes, which exhibit

mobilities of 5 cm^2/Vs and 60 Hz frequency. Although this is only a 1-bit tag, it does demonstrate the possibilities of achieving low-cost, RFID tags by mass-printing techniques.

Sensors. Someya et al. first demonstrated the concept of integrating the flexible OTFTs to sensor arrays and realized the e-skin for next generation robots. The OTFTs based on evaporated pentacene achieved mobilities around 1 cm^2/Vs. They were fabricated on flexible substrate as an active matrix and integrated with pressure and thermal sensors, and provided 2D pressure/temperature reading.[7,299] Using similar technique, they also reported a 72×72 flexible image sensor array, by coupling the active matrix of OTFTs with organic p-n photodiodes (Figure 4.10 left).[300] Although above circuits were still fabricated with conventional clean room facilities, they represent the next generation of flexible electronics applications.[5]

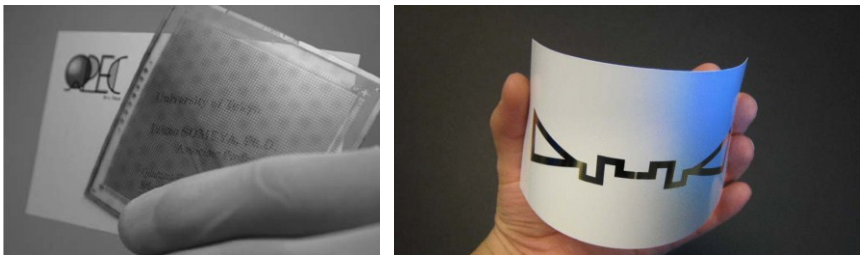

Figure 4.10 Flexible sensors. Left panel: an active matrix of organic image sensors.[300] Right panel: a printed humidity sensor diode integrated with RFID tags. [301]

Many organic materials themselves are good candidates for gas, chemical, humidity sensors, since their electronic properties strongly depend on the environment change. Many research groups have demonstrated printed humidity and temperature sensors on

flexible substrates. Integrated with RFID tag, the sensors can transfer the readings wirelessly (Figure 4.10 right).[301,302]

Chapter 5 Printed Flexible Electrolyte-gated CNT Transistors and Digital Circuits*

5.1 Introduction

Semiconducting carbon nanotubes are known to exhibit very high intrinsic mobilities (~ 100,000 cm^2/Vs)[303] and consequently can be incorporated in high frequency (short delay time) devices.[194] Yet the difficulties associated with circuit fabrication based on single CNTs have hindered their wide application. To overcome this, CNT thin films deposited from solution or by dry transfer printing process have become attractive alternatives.[9,143,202,304-307] Combining printable high capacitance dielectrics with printable high mobility semiconductors could potentially solve these problems.

This chapter demonstrates the fast, flexible digital circuits based on semiconducting carbon nanotube (CNT) networks and high capacitance ion gel gate dielectrics, which were patterned by jet printing of liquid inks. Electrolyte-gated transistors (EGTs) based on CNTs with 50 μm channel lengths display ambipolar transport with electron and hole mobilities > 20 cm^2/Vs; these devices form the basis of printed inverters, NAND gates, and ring oscillators on both polyimide and SiO_2 substrates. The combination of high purity, high mobility semiconducting CNT networks and high capacitance ion gel dielectrics affords the fastest and lowest voltage jet printed electronic circuits up to date

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of this thesis. Chapter 6 will discuss how to further improve the circuit performance by optimizing device architecture.

5.2 Printed Electrolyte-gated Ambipolar CNT EGTs

In this section, printed EGTs based on a high performance aqueous CNT ink in which 98% of the tubes are semiconducting (*i.e.*, the fraction of metallic tubes is ~2%)[173] are demonstrated and discussed. The high purity ink, synthesized by Prof. Hersam's group in Northwestern University, ensures that good ON/OFF current ratios are achieved easily for printed CNT transistors without subsequent processing or chemical treatment to eliminate metallic tubes. Furthermore, the printed CNT networks are intrinsically ambipolar, and exhibit effective mobilities of both holes and electrons in the range of 20-50 cm^2/Vs depending on the printing conditions. The mobilities are comparable to or better than that of CNT networks fabricated by other methods.[9,38,143,198,202,305-308] Ambipolar operation in turn allows fabrication of complementary-like logic circuits,[274,308-310] which is desirable from a circuit design perspective. Another key to achieving low voltage CNT EGTs is the use of a high capacitance gel electrolyte dielectric that discussed previously.

5.2.1 Device Architecture

Figure 5.1 (a) shows the device structure and the printing process. The EGT channels were 50 μm in length and 500 μm in width as defined by lift-off Au electrodes prefabricated on plastic or SiO_2/Si substrates. The CNT channel and subsequent layers

were printed sequentially using aerosol jet printing.[24] A photomicrograph of a completed CNT EGT on polyimide is shown in Figure 5.1 (b). From the atomic force microscopy (AFM) topographic image in Figure 5.1 (c), it is evident that the printed CNTs formed a distributed random network. The coverage of nanotubes can be tuned by varying the concentration of the aqueous CNT ink and printing speed. An apparent surface coverage of ~30% CNTs, as assessed by AFM, was found yield optimized ON/OFF current ratios in the resulting EGTs.

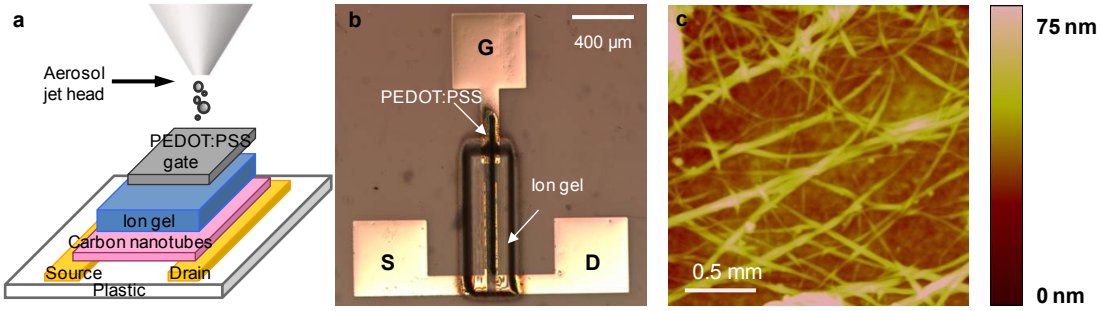

Figure 5.1 Device architecture of printed ion gel-gated CNT transistors. (a), Schematic sketch of aerosol jet printing of a CNT EGT. (b), Optical image of a printed ion gel gated CNT EGT on polyimide substrate. (c), AFM topography image of the printed CNT network on polyimide.

After printing the CNT layer, the high capacitance ion gel dielectric ink was printed over the channel. Evaporation of the ethyl acetate solvent resulted in an ionically conducting, electronically insulating gel electrolyte with an elastic modulus of ~10 kPa. To finish the device, a layer of conducting polymer poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (PEDOT:PSS) was printed on top of the gel to form the gate

electrode. All materials were printed by a commercial available aerosol jet printing technique described in section 4.3.

5.2.2 CNT EGT Performance

The electrical properties of printed CNT transistors were tested in vacuum (10^{-6} Torr). Clear ambipolar behavior can be seen from the transfer curves shown in Figure 5.2 (a). The ON/OFF current ratio is above 10^4 at $V_D = -0.1$ V for this device with a subthreshold swing of 130 mV/decade. The effective mobilities of holes and electrons are 30 and 20 $cm^2/V \cdot s$, respectively, for an estimated 10 $\mu F/cm^2$ gate sheet capacitance.[24] It should be noted, however, that the quantum capacitance of carbon nanotubes (10^{-10} F/m)[199] is on the order of several $\mu F/cm^2$ if the CNT coverage is ~ 50%. For CNT EGTs gated with a high capacitance dielectric such as the ion gel, the quantum capacitance may be smaller than the dielectric capacitance; if this is the case, the quantum capacitance will dominate and thus the effective mobilities will be larger than our estimation.

The typical output characteristics ($I_D - V_D$) as shown in Figure 5.2 (b) also indicate ambipolar behavior. For $V_G > 0.6$ V the output characteristics show clear linear and saturation regimes typical of n-type (electron) transport. For $V_G < 0.6$ V, the transistor exhibits p-type transport in which holes are injected from the drain electrode. The ambipolar behavior of the CNT networks indicates the injection of both electrons and holes is facile from the high work function Au source and drain contacts, which may result from enhancement of the electric fields at the electrode/CNT interfaces due to the presence of electrolyte.[82,198,311]

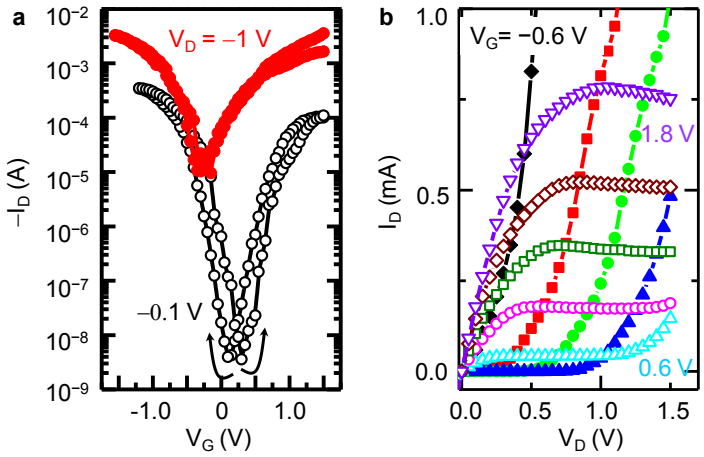

Figure 5.2 Electrical characterization of ion gel gated CNT EGTs showing ambipolar transport. (a), The transfer characteristics of an EGT printed on polyimide substrate, at $V_D = -1$ V (Red solid circles), and at $V_D = -0.1$ V (black open circles). (b), The output characteristics showing both n- (open symbols) and p-type transport (solid symbols), at $V_G = -0.6$ V to 1.8 V, with 0.3 V steps.

5.2.3 Reproducibility of Printed CNT EGTs

Table 5.1 displays the statistics for key device parameters (ON/OFF current ratio, mobility, conductance, and threshold voltage) based on 28 printed CNT EGTs on polyimide substrates, as well as 50 CNT EGTs printed on SiO_2 substrates.

The transistors had either high (~60%) or low (~30%) CNT coverages as determined by the printing conditions. Film coverage refers to the tube density as assessed by AFM. On plastic substrates, the results for high coverage films and low coverage films are reported separately to demonstrate how the network density affects the transistor performance. The general observation is that the ON/OFF current ratio is significantly greater for low density films than for high density films, presumably because of the presence of metallic CNT impurities that raise the OFF current.[139] With a low network

density, a metallic CNT "short" is less likely. Likewise, the mobility appears larger for the high density CNT film, which again may reflect the influence of metallic impurities that effectively shorten the channel.

		I_{ON}/I_{OFF}	μ (cm^2/Vs)	g (ms/mm)	V_{TH} (V)
high density films on polyimide substrate	hole transport	$(2.7 \pm 0.9) \times 10^3$	31 ± 9	5 ± 1	–0.62 ± 0.03
	electron transport	$(1.8 \pm 0.7) \times 10^3$	17 ± 3	7 ± 1	0.50 ± 0.08
low density films on polyimide substrate	hole transport	$(3 \pm 2) \times 10^5$	9 ± 4	1.3 ± 0,6	–0.53± 0.04
	electron transport	$(2 \pm 1) \times 10^5$	3 ± 1	1.1 ± 0.5	0.66 ± 0.08
high density films on SiO_2 substrate	hole transport	3×10^3	50 ± 17	7 ± 4	–0.5 ± 0.1
	electron transport	3×10^3	40 ± 15	8 ± 4	0.8 ± 0.1

Table 5.1 Key parameters of transistors printed on flexible polyimide and on SiO_2 substrates.*

* Results on polyimide are reported for high density (~60% network coverage) and low density (~30% coverage) CNT films. The high density film data are based on 11 EGTs and the low CNT density film results are based on 17 EGTs. For SiO_2 substrates the data are based on 50 EGTs. All the values are acquired with $V_D = -0.1$ V. The ON/OFF current ratios (I_{ON}/I_{OFF}), mobilities ($\mu=(dI_D/dV_G)(1/C_sV_D)(L/W)$), and the normalized conductances ($g = I_D/V_DW$) are obtained at $V_G \sim 1$ V (holes) and $V_G \sim +1.5$ V (electrons).

Figure 5.3 and Figure 5.4 demonstrate the reproducibility of printed CNT EGTs on polyimide (11 devices with high coverage CNT films and 17 devices with low coverage CNT films) and SiO_2 substrates (50 devices with high coverage CNT films), respectively.

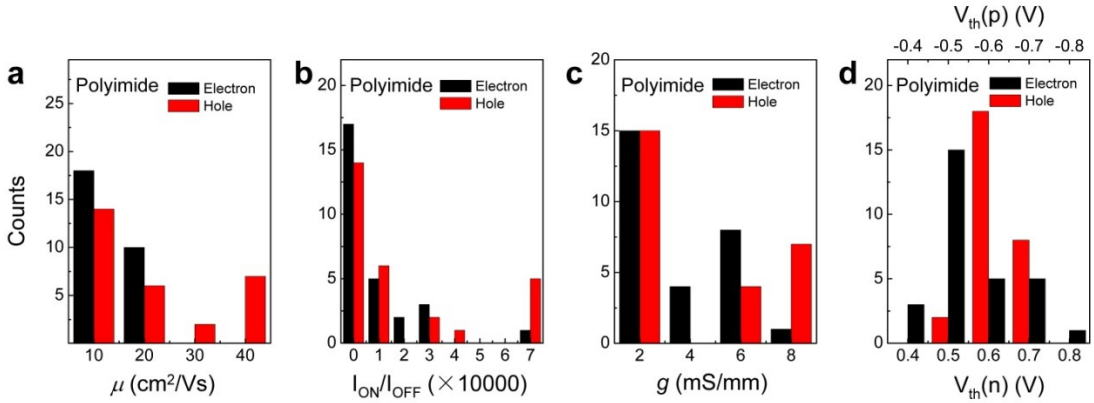

Figure 5.3 Distribution of the key parameters of printed ambipolar CNT EGTs on polyimide substrates. (a), the mobility. (b), the ON/OFF current ratio. (c), the ON state conductance. (d), the threshold voltage. The n-type (electron) transport is shown in black, and p-type (hole) is shown in red, respectively.

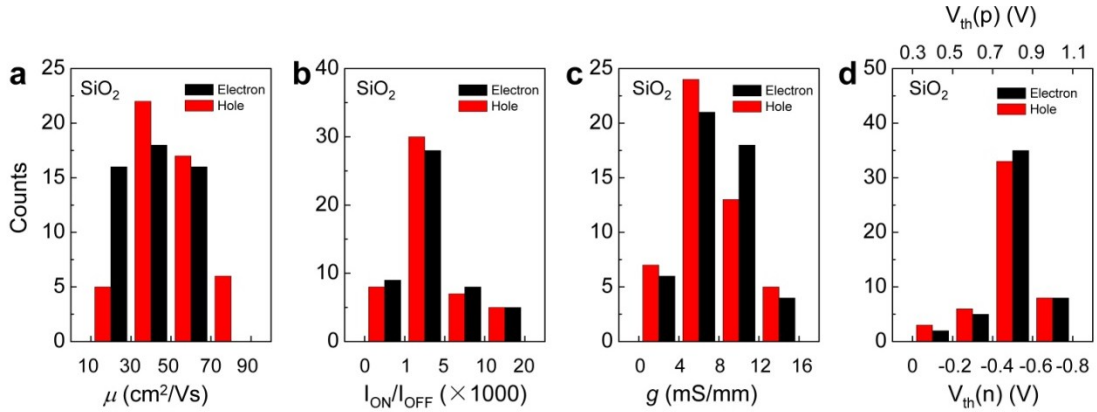

Figure 5.4 Distribution of the key parameters of the printed ambipolar CNT EGTs on SiO_2 substrates. (a), the mobility. (b), the ON/OFF current ratio. (c), the ON state conductance. (d), the threshold voltage. The n-type (electron) transport is shown in black, and p-type (hole) is shown in red, respectively.

5.3 Inverters Based on Printed CNT EGTs

5.3.1 Electrical Characterizations

Realization of ambipolar CNT EGTs allows the development of complementary-like, digital printed circuits.[308,312] The most basic circuit unit, the inverter, can be achieved by combining two identical ambipolar transistors together, as shown in the inset of Figure 5.5 (a). At a given supply (V_{DD}) and input voltage (V_{IN}), transistors ***a*** and ***b*** will work under different bias conditions. When V_{IN} is "low" (*e.g.* 0 V), transistor ***a*** operates in a strong p-type regime (lower resistance) while the transistor ***b*** works in a weak p-type regime (higher resistance). Thus the output voltage (V_{OUT}) will be "high" (close to V_{DD}). On the other hand, when V_{IN} is "high" (*e.g.* 1.5 V), transistor ***a*** operates in a weak n-type regime and transistor ***b*** works in a strong n-type regime, such that V_{OUT} is low. The ambipolar nature of CNT EGTs means that the switching mechanism of CNT inverters is different from the classic silicon complementary (CMOS) inverter in which only one of the two transistors turns ON and the other remains in the OFF state. It is therefore better to describe the CNT inverters as "complementary-like" instead of "complementary".[275]

The input-output voltage characteristics of a typical printed CNT inverter on polyimide (Figure 5.5 a) demonstrate that the output swing reached 1.2 V (80% V_{DD}) for V_{DD}= 1.5 V. The inverter switched sharply at the threshold voltage and achieved a gain as high as 58 (Figure 5.5 b), which is higher than that of previously reported inverters based on CNT films[200,307,308] and other printed organic semiconductors. The hysteresis between the forward and backward sweeps is likely related to hysteresis in the EGT transfer curve

(Figure 5.2). Figure 5.5c and d show the dynamic responses of inverters printed on polyimide and SiO_2 substrates, respectively. For a 1 kHz input square-wave signal, the output swing reached ~ 1 V for V_{DD} = 1.5 V for inverters on polyimide and SiO_2.

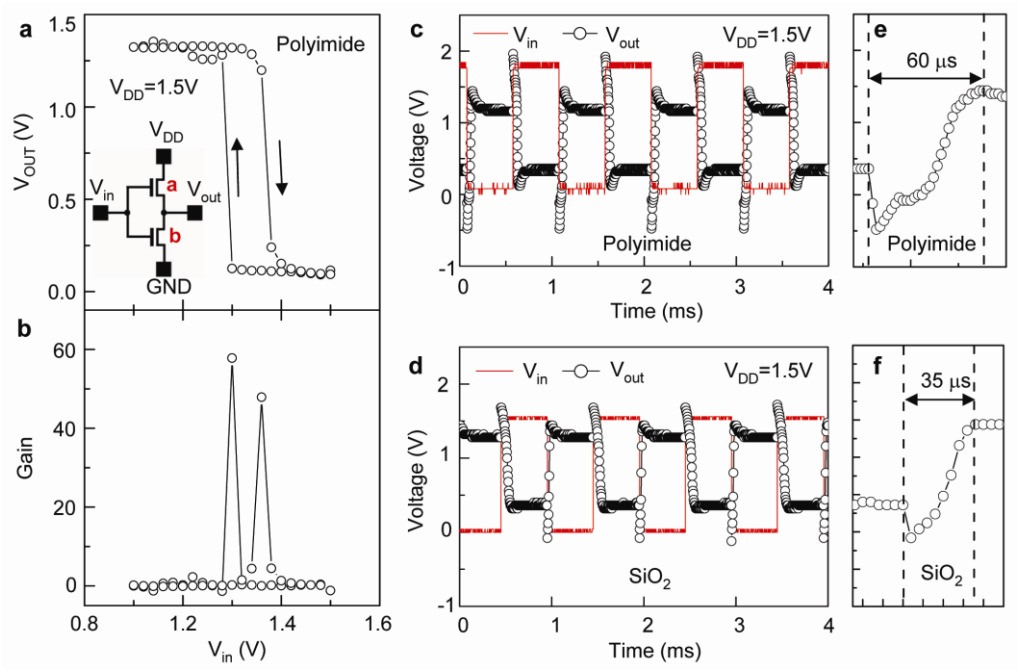

Figure 5.5 Electrical characterization of printed complementary-like inverters based on ambipolar ion gel gated CNT transistors. (a), The input-output characteristics of a CNT inverter printed on polyimide substrate. The inset shows the circuit diagram of the inverter based on two identical ambipolar CNT EGTs. (b), the maximum inverter gain is 58 at V_{DD} = 1.5 V. (c), Dynamic response of an inverter on polyimide substrate acquired with V_{DD} = 1.5 V. The output voltage (open circles) tracks the 1 kHz square signal (red) which ranges from 0 V to 1.8 V. (d), an inverter printed on SiO_2 substrate, where input voltage ranges from 0 V to 1.6 V, with V_{DD} = 1.5 V. The rising time of the inverter is 60 µs on polyimide substrate (e) and 35 µs on SiO_2 substrate (f).

The rise time of the inverter on plastic is 60 µs (Figure 5.5 e), while on SiO_2 it is 35 µs (Figure 5.5f). The overshoot peaks in Figure 5.5 c and d, which may limit the highest working frequency of CNT inverters, derive from parasitic (or "overlap") capacitance.

Parasitic capacitance is a particularly important issue for electrolyte-gated transistors because the capacitance of electrolytes is so large.[24,25] Its origin is the capacitive coupling of the gate to source and drain electrodes which causes momentary current spikes when the voltage on the gate electrode is switched suddenly. To reduce these effects, the electrolyte/metal interfacial capacitance must be minimized.

Figure 5.6 demonstrates that the inverters printed on polyimide substrates can track up to 5 kHz input signal, while the inverters on SiO_2 can track up to 50 kHz. The inverter on polyimide (Figure 5.6 a) exhibits higher overshooting peaks, indicating larger *RC* time constant. This is due to parasitic capacitance associated with rougher electrodes on polyimide, which will be discussed in the following section.

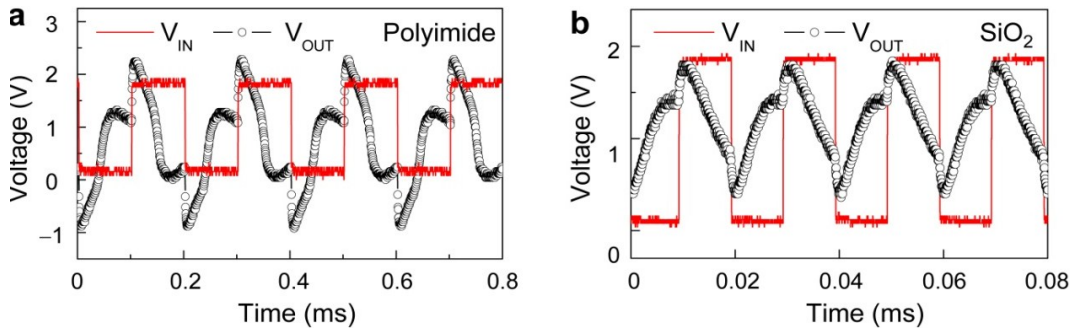

Figure 5.6 Dynamic responses of the CNT inverters. (a), the output signal (black open circles) of an inverter printed on polyimide substrate tracks up to the 5 kHz input signal (red), with V_{DD} = 1.5 V. (b), the output signal (black open circles) of an inverter printed on SiO_2 substrate tracks up to the 50 kHz input signal (red), with V_{DD} = 1.5 V.

5.3.2 Operational Stability of Printed CNT Inverters

The operational stability of the printed CNT inverter at 100 Hz input frequency is shown in Figure 5.7. After 10 min of operation, the output voltage did not detectably

decrease as shown in Figure 5.7 a, but the transfer (I_D - V_G) characteristics of the individual EGTs revealed a 10-fold decrease of both the ON and OFF currents, reflecting an overall resistance increase (Figure 5.7 c). From the enlarged falling time plot (Figure 5.7 b), it can be seen that the switching time increases slightly which is likely due to the increased RC time constant associated with metallic tube burnout, as discussed previously.

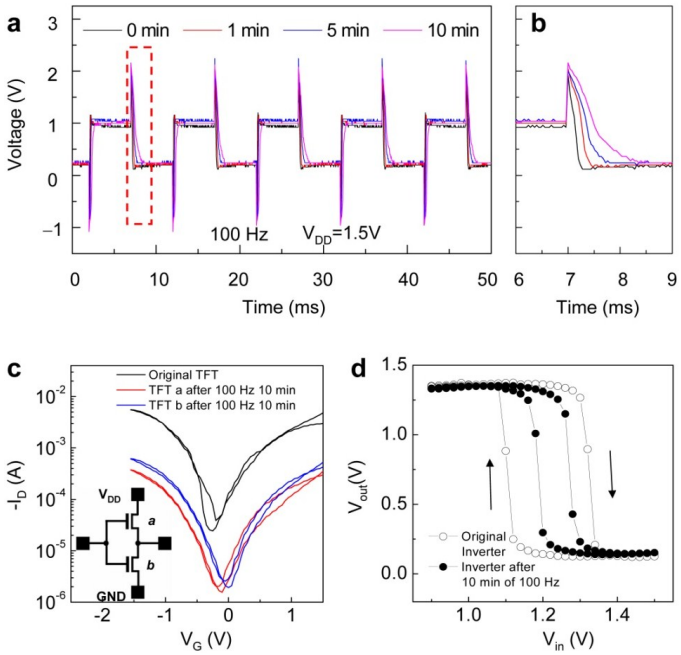

Figure 5.7 Stability of the printed CNT inverter on polyimide substrate. (a), dynamic response of an inverter at 100 Hz with continuous operation for 10 min. (b), enlarged view of the falling edge. (c), the transfer curves of the EGTs measured before the continuous operation and after, with V_D = –0.1 V. The inset shows the circuit diagram of the inverter. (d), the input-output voltage characteristics of the inverter before continuous and after.

Figure 5.7 d shows that the output voltage swing remains about the same. The hysteresis in the output voltage characteristic seems to decrease with time, likely due to

the smaller hysteresis in the transfer curve. The consequences of the increased device resistance are not evident in the inverter operating at 100 Hz but do appear in the output of ring oscillators, which will be discussed in following sections.

5.4 Ring Oscillator

5.4.1 Electrical Characterizations

Figure 5.8 a and b display the optical micrographs and circuit layout of a 5-stage, printed CNT EGT ring oscillator. As soon as the supply voltage V_{DD} reached a critical value (~0.5 –1 V), spontaneous oscillation of the output signal commenced, as observed in Figure 5.8 c. The oscillation frequency is 2.3 kHz and 1.9 kHz on SiO_2 and polyimide substrates, respectively. There is some signal distortion for the oscillator on plastic because of parasitic capacitance. The parasitic capacitance is estimated to be 22% of the total capacitance (see section 5.5), and is more pronounced for oscillators on polyimide because the substrates and thus the metal electrodes are rougher, meaning there is more contact area associated with the metal/electrolyte interfaces. The self-assembled monolayer (SAM) coatings were used on the Au source and drain electrodes to minimize capacitance effects. It is clear that thiol SAMs (either hexadecane thiol or anthracene thiol) improve the ring oscillator output and thus these SAMs were used to treat electrodes in all of the devices discussed in this chapter.

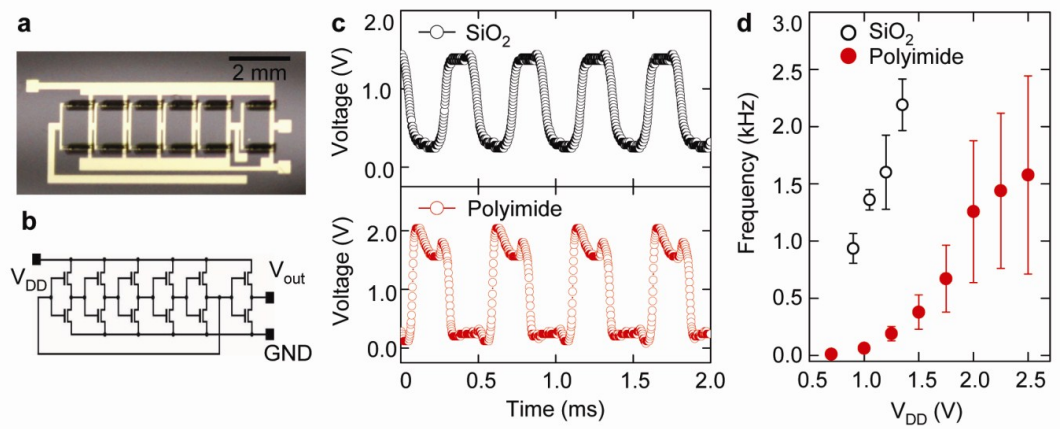

Figure 5.8 Five-stage ion gel gated complementary-like CNT ring oscillator with output buffer. (a), photomicrograph of a printed ring oscillator on polyimide substrate. (b), circuit diagram of the device. (c), upper panel shows the output characteristics of a device printed on SiO_2 substrate with 2.3 kHz oscillation frequency at V_{DD} = 1.5 V; lower panel shows the response of a device printed on polyimide substrate with 1.9 kHz oscillation frequency at V_{DD} = 2.5 V. (d), output frequency as a function of V_{DD} of devices on polyimide (red solid circles) and SiO_2 (black open circles). Error bars represent one standard deviation.

On both plastic and SiO_2 substrates, the output frequencies increase with V_{DD}, as expected, Figure 5.8 d. However, the oscillation frequency of ring oscillators on plastic is generally lower than on SiO_2. This is likely due to the somewhat lower mobility (Table 5.1) and the higher parasitic capacitance, which both can increase the *RC* time constant of the individual stages. The best devices on plastic and SiO_2 achieved frequencies above 2 kHz at 2.5 V supply voltage. The delay time for a single stage of the oscillator, $t_D=1/2Nf$ where N is the number of stages and f is the frequency, is 53 μs for the fastest device on plastic and 42 μs for the fastest on SiO_2. These stage delays are a significant improvement over previous reports in printed electronics.

5.4.2 Operational Stability of Printed CNT Ring Oscillators

The time stability of the ring oscillators on plastic were also tested, as shown in Figure 5.9. After 30 min of continuous operation, the output frequency decreased by 90% for ring oscillators on polyimide. The decrease of the oscillating frequency can be explained by the 10-fold increase in resistance of the individual stages as was observed in our investigation of discrete inverters (Figure 5.7). Probably the cause for the resistance increase is 'burn out' of metallic tube shorts in the network. Higher purity CNT inks may mitigate this issue and enhance stability. The time stability of CNT ring oscillator circuits is currently an ongoing area of investigation.

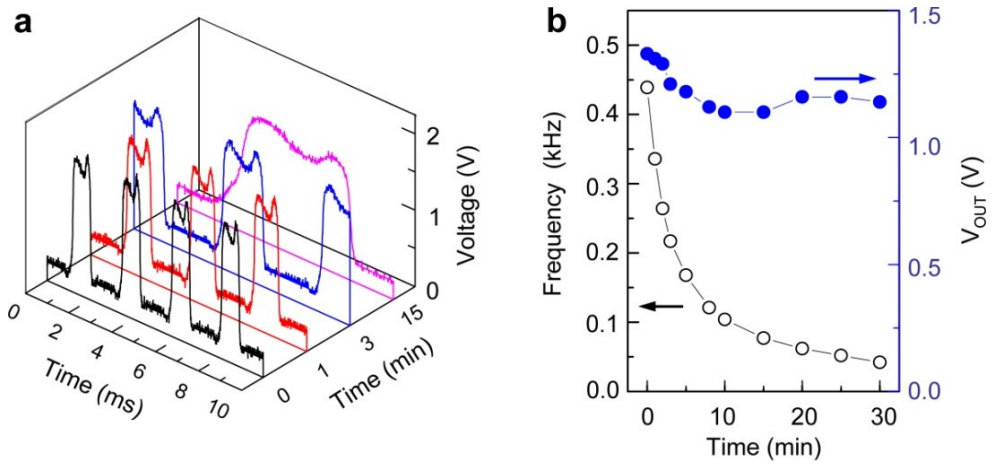

Figure 5.9 Time stability of a CNT ring oscillator printed on polyimide substrate. (a), The output voltage as a function of operation time, with continuous operation at V_{DD} = 1.5 V. (b), The output frequency and the output voltage swing as a function of operation time.

5.5 Parasitic Capacitance

5.5.1 Estimation of Parasitic Capacitance and Parasitic Resistance

The parasitic capacitance in printed CNT circuits (*e.g.*, ring oscillators) can be estimated by the strength of the coupling peaks. From Figure 5.10 b, ΔV (the height of the peak) is 0.24 V, and the V_{OUT} (output voltage swing) is 1.36 V. Figure 5.10 d demonstrates the equivalent circuit which is used to estimate the parasitic (C_p) and channel capacitance (C_c). In this simplified model, it is assumed that only one of the two transistors is ON at each stage of the ring oscillator. The resistance $R=V_{DD}/I$=12 kΩ, where V_{DD} is 2.5 V, and I is 0.15 mA, the average current of the inverter around the transition region (see Figure 5.10 c). When the voltage switches at point A with amplitude V_{OUT}, point B will exhibit a sudden voltage change ΔV due to the coupling of the parasitic capacitance, and this voltage will also charge or discharge the next stage, the total capacitance of which is represented by a channel capacitance and a parasitic capacitance, as shown in Figure 5.10 d. Thus, from the conservation of charge at points A and B,

$$Q = C_p V_{OUT} = (C_p + C_p + C_c)\Delta V \tag{5.1}$$

Thus, using ΔV and V_{OUT} from Figure 5.10 b, C_p/C_c = 0.28. On the other hand, the total capacitance of each stage, $C_p + C_c$, can be estimated by the signal delay time of a single stage (t=1/2Nf), *i.e.* 50 μs for this CNT inverter,

$$t_{delay} = \ln 2 \times RC_{total} = 50 \times 10^{-6} s \tag{5.2}$$

Thus, for each CNT EGT where R = 12 kΩ, C_{total} is estimated to be 5.8 nF, and C_p and C_c are 1.3 nF and 4.5 nF, respectively. Parasitic capacitance is about 22% of the total capacitance.

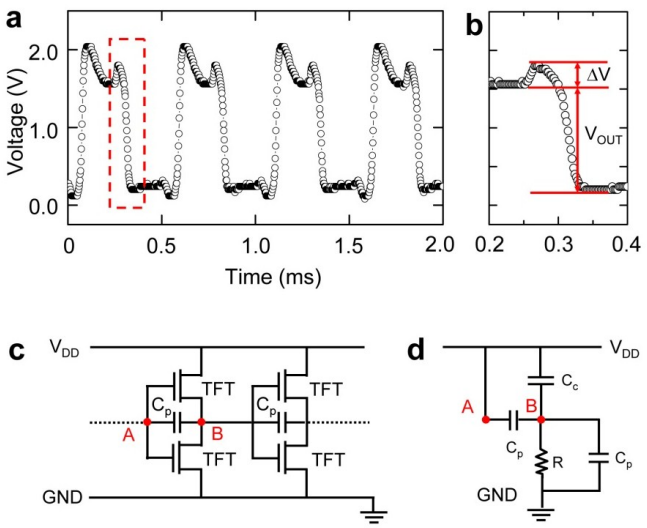

Figure 5.10 Estimation of the parasitic capacitance. (a), The output signal of a printed 5-stage CNT ring oscillator on polyimide. V_{DD} = 2.5 V. (b), the overshooting peak caused by the parasitic capacitance at the falling edge. ΔV is the height of the peak, and V_{OUT} is the output voltage of the ring oscillator. (c), The circuit diagram of two stages in the ring oscillator. C_p represents the parasitic capacitance between the gate electrode and the source and drain electrodes. (d), the equivalent RC circuit of c, where R is the resistance of one EGT between source and drain, C_c is the dielectric capacitance of the CNT channel.

The parasitic resistance is majorly induced by the resistances of the gate electrodes. The average resistance measured for the 500 μm PEDOT:PSS gate electrode is about 200 Ω. Therefore, the effect of parasitic resistance can be estimated by R_{para}/R_{total} = 200/12000 ≈ 1. 7%.

5.5.2 Reduction of Parasitic Capacitance

The parasitic capacitance represents the capacitance at the interface between the ion gel dielectric and the Au surfaces of the source and drain electrodes. One way to reduce this capacitance is to increase the distance between the ions and the Au surface. A self-assembled monolayers (SAMs) of molecules (e.g. anthracene thiol) is used here to coat the Au surfaces. Figure 5.11 demonstrates that the SAM treatment reduces the signal distortion in the output voltage of printed CNT ring oscillators on SiO_2 substrates.

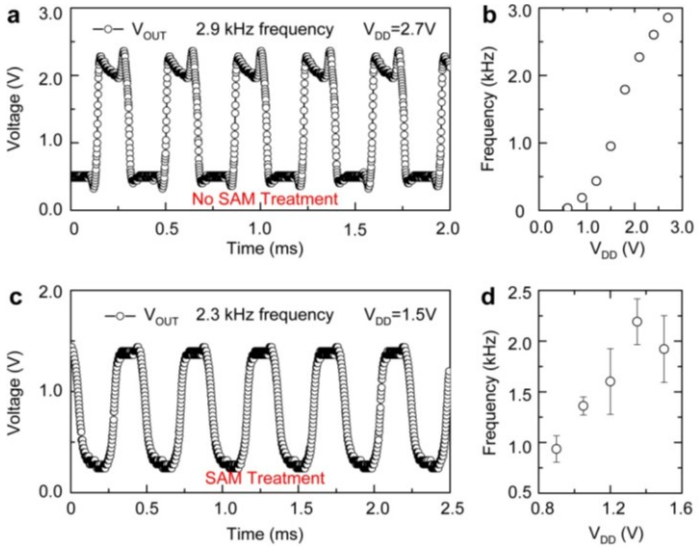

Figure 5.11 Reduction of the parasitic capacitance. (a), The output signal (V_{DD} = 2.7 V) of a ring oscillator printed on SiO_2 substrate, *with no SAM treatment*, shows larger parasitic peaks. (b), The frequency as a function of V_{DD} of inverters with no SAM treatment. (c), The output signal (V_{DD} = 1.5 V) of a ring oscillator printed on SiO_2 substrate, *with SAM treatment* (e.g., anthracene thiol shown in this figure), shows smaller parasitic peaks. (d), The frequency as a function of V_{DD}. Error bars represent one standard deviation.

In considering switching speed, it is important to bear in mind that other "parasitic" parameters may exist in printed circuits that can increase signal propagation delays. One

important example is parasitic capacitance, e.g. capacitance between the gate and the source/drain electrodes. Parasitic capacitance may be a particularly challenging problem in printed electronics where precision patterning is challenging and electrode roughnesses may be high. These factors will add to the overall *RC* time constants. Figure 5.12 shows the comparison of the surface roughness between liftoff Au electrode and printed Au electrode, both fabricated on Si/SiO_2 substrate. It is clear that the printed electrode has much higher surface roughness, which may cause higher parasitic capacitance.

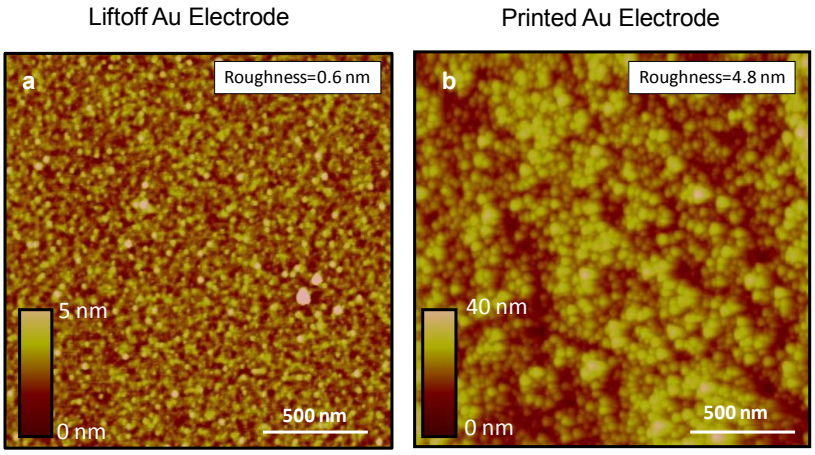

Figure 5.12 AFM images of Au electrodes. (a), liftoff Au electrode. (b), printed Au electrode. The RMS roughness over 2×2 μm^2 area of (a) is 0.6 nm, and (b) is 4.8 nm.

5.6 NAND Gate Based on Printed CNT Transistors

Printed CNT NAND logic gates were also demonstrated on plastic substrates. Figure 5.13 displays an array of printed NAND gates on polyimide. Each NAND gate has two EGTs in parallel (labeled ***a*** and ***b*** in Figure 5.13 b) and two transistors in series (***c*** and ***d***) and only registers low when two input voltages (V_A and V_B) are both high. As discussed

above, the ambipolar EGTs cannot be completely turned OFF, which usually leads to an output voltage swing smaller than conventional complementary circuits[308]. Here the widths of ***c*** and ***d*** (the "pull-down" transistors) are designated to be four times larger than transistors ***a*** and ***b*** to balance the network strength. In this way, the output swing is maximized and the rising and falling times are equalized. NAND gates printed on plastic can respond to two input voltages at 100 Hz as shown in Figure 5.13 c. It can be seen from Figure 5.13 d that for devices on the SiO_2 substrates, the peaks in the output signal caused by parasitic capacitances are much smaller compared with those on plastic substrates, which leads to higher working frequency (1 kHz).

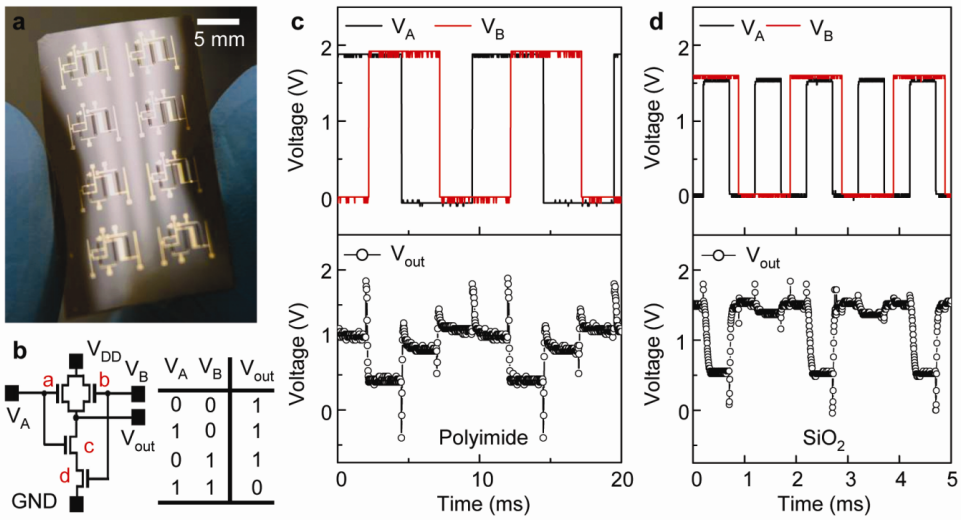

Figure 5.13 NAND logic gate based on ion gel gated printed CNT transistors. (a), Printed CNT NAND gate array on flexible polyimide substrate. (b), Circuit diagram and logic sequence of the NAND gate. (c), Dynamic response of the device printed on polyimide substrate showing proper NAND logic at 100 Hz, V_{DD} = 1.5 V. Black and red lines are input voltages V_A and V_B, and the output voltage (black open circles) registers "low" only when V_A and V_B are both "high". (d), Dynamic response of the device printed on SiO_2 substrate showing proper NAND logic at 1 kHz, V_{DD} = 1.5 V.

5.7 Conclusions

In summary, the combination of high mobility, ambipolar semiconducting CNT networks and high capacitance ion gel dielectrics affords printed digital circuits that operate at sub-3V supply voltages with 40-60 μs signal delays. These results represent a significant improvement for printed circuits processed from liquid inks.

The speed of the printed CNT ring oscillators is promising for printed electronics applications, and there is considerable potential for improvement. It is worthwhile noting that the channel lengths of the devices used here are relatively long at 50 μm. Based on the carrier mobility of the CNT network, one can initially estimate the delay time from $t = \pi L(L+2dL)/\mu V_{DD}$, where L is the channel length (50 μm), dL is the overlapping width between source and drain to the gate electrode (10 μm). The resistance R of the ion gel depends on the film thickness and therefore thinner printed ion gel layers will result in shorter switching times (smaller RCs). The gel layer thickness in the devices reported here is on the order of 10 μm; decreasing that to 1 μm would result in a 10-fold decrease in the RC time constant, potentially allowing switching in the 0.1 MHz regime (stage delays between 10^{-6} and 10^{-5} s).

The following chapter will discuss how these parameters affect the speed of the CNT circuit, and demonstrate optimization of the device architecture to achieve faster printed circuits.

Chapter 6 Printed Fast Electrolyte-gated CNT Ring Oscillators*

6.1 Introduction:

The previous chapter demonstrates the feasibility of fabricating fast, flexible digital circuits based on printed EGTs that pair a high mobility semiconductor layer based on semiconducting CNTs with a high capacitance, printable electrolyte as the gate insulator. The CNT layer has high electron and hole mobilities for fast switching and the printable high capacitance gel electrolyte affords low voltage operation. Using these materials, printed 5-stage ring oscillators operating at 2 kHz with a 3 V supply were presented, which corresponded to a delay of 50 μs per stage. At the time when this work is reported, these performance metrics represented a near record value for printed circuits. Following this initial demonstration, Ohno and colleagues subsequently fabricated ring oscillators with 12 μs stage delay at 4 V supply, using transfer printing of the CNT semiconductor layer and evaporated dielectric and metal layers,[28] thus suggesting the possibility of further improvements.

This chapter focuses on understanding the factors which affects the frequency of ring oscillators, such as channel length, ion conductivity in ion gel, parasitic resistance and capacitance, etc. Inverter switching times, *t*, were systematically characterized as a

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function of transistor channel length and ionic conductivity of the gel dielectric, demonstrating that both the semiconductor and the ion gel play a role in switching speed.

And in the last, printed 5-stage ring oscillators are demonstrated with >20 kHz operating frequencies and stage delays < 5 μs at supply voltages below 3 V, which is an order of magnitude reduction in switching times. The improvements were achieved by employing high mobility semiconducting CNTs, controlling the thickness of the ion gel gate dielectric, reducing the channel lengths, and minimizing parasitic capacitances and resistances. The fastest ring oscillator achieved 1.2 μs delay time at 2 V supply. These results are the fastest low voltage switching speeds in printed electronics reported to date and the speeds are sufficient for many high value applications including video display backplanes. Additionally, by systematically examining device metrics as a function of EGT architecture, this work provides a clear roadmap for future performance enhancements.

6.2 Printed CNT EGTs and Inverters

6.2.1 Printed CNT EGTs with Reduced Channel Lengths

As discussed in the end of chapter 5, the switching speed of transistors are directly affected by the channel length and the width of the source/drain electrodes. As in typical FETs, scaling down the channel length increases the switching speed. Additionally, in EGTs, less overlap between source/drain electrodes and electrolyte reduces the parasitic

capacitance. Therefore, in this chapter, the transistors are fabricated with narrower electrodes (~ 2 μm) and shorter channel lengths compared to previous chapter.

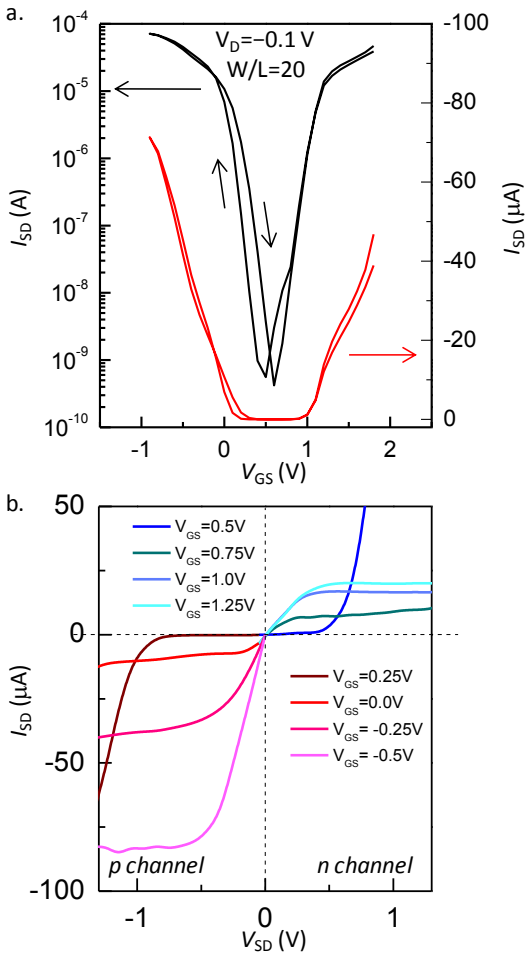

Figure 6.1 Performance of ion gel gated ambipolar CNT EGTs. (a), Transfer characteristics (b), The output characteristics.

Similarly to previous results, with electrolyte gating, CNTs can perform as both p-type and n-type semiconductors, as indicated in the EGT transfer curve shown in Figure 6.1 a. As printed, the CNT network is slightly p-doped. With a negative V_{GS} (gate to source

voltage), the anions in the ion gel migrate to the ion gel/CNT interface, which enhances the p-doping of the CNTs and increases the hole conductivity. On the other hand, a small positive V_{GS} induces cations at the gel/CNT interface, extracting holes from nanotubes and eliminating the p-type transport. Continuing to apply more positive V_{GS} causes injection of electrons into the nanotubes and enhances the electron conductivity. The high capacitance ion gel decreases the width of the contact barriers between Au and the conduction and valence bands of the CNTs, making the injection of both electrons and holes easier.[97] Therefore, the ion gel gated CNT EGTs are ambipolar transistors.

In EGTs based on CNT networks, there is always a trade-off between the mobilities and ON/OFF current ratio. The mobilities generally increase with the network coverage,[28,34] while the ON/OFF current ratio decreases with the CNT network coverage.[139,188] High mobility is the key to achieve fast switching speed, while high ON/OFF current ratio is important for low power consumption and high output voltage swing. In CNT EGTs, the CNT network is immersed in an ionic matrix, where the conformal gel/CNT interface provides a 3-dimensional gating effect. Additionally, high purity SWCNTs that contain > 99% semiconducting nanotubes in order to reduce shorting and screening by metallic tubes.[173] Therefore, even with the CNT coverage much higher than the percolation limit, the printed CNT EGTs are able to achieve high ON/OFF ratios at short channel lengths, i.e., 10^5 with $V_D = -0.1$ V and L = 10 μm, as shown in Figure 6.1 a. The effective mobilities of the electrons and holes are about 20 cm^2/Vs, estimated from the linear fit of the I_D-V_{GS} transfer curve and average channel

capacitance of ~ 2 μF/cm^2 (see discussions of Figure 6.8). The effective mobility here is estimated based on the channel dimensions, not accounting for the actual CNT network coverage, i.e., the number of nanotubes per area.

Figure 6.1 b displays the typical output characteristics of the ambipolar CNT EGTs. With V_{GS} < 0.5 V, p-type transport dominates (red curves). The source – drain current, I_D, increases with the drain bias, V_{SD}, and shows clear linear and saturation regimes. With V_{GS} = 0.25 V, the EGT is in the OFF-state as a typical p-type transistor when a small V_{SD} is applied. Note here the increase of I_D (tail of the curve) at more negative V_{SD} is due to electron injection. The electron injection also contributes to the slight slope of the saturation currents. With V_{GS} >0.25 V, the EGT shows n-type transport (blue curves) and similar performance as the p side.

6.2.2 Transistor Performance with Various V_D

As shown in Figure 6.2, as the drain bias V_D increases, the transistor transfer characteristics change. The OFF current increases with V_D while the ON/OFF ratio decreases. This is attributed to the ambipolar nature of the CNT EGT. Due to the narrow band gap of CNT, both types of carriers, i.e., electrons and holes, can be easily injected in. Under large drain bias, e.g., −1 V, even with very small V_{GS} 0.2 V, the large V_{GD} will start to induce electrons from the drain electrode, therefore, I_D starts to increase as the V_{GS} goes more positive than 0.2 V, before the p-type conductance turned off. Therefore, with larger drain bias, the transistor always shows higher OFF current.

On the other hand, the OFF voltage (the point with lowest current) shifts to the left when the negative V_D increases. Due to the same mechanism discussed above, the threshold voltages of both *p* and *n* conductance change as the drain bias changes, and result in the OFF point shift. Similarly, if V_D increases to positive side, the transistor OFF voltage will shift to right. This will lead to the trip voltage shift in inverters as discussed in Figure 6.3 a.

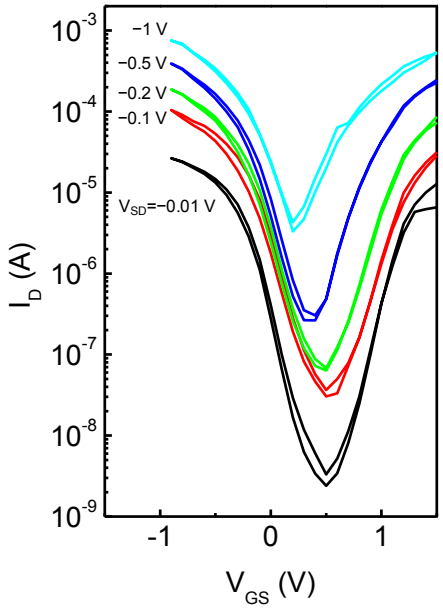

Figure 6.2 Transfer curves of an CNT EGT with various drain biases, from −0.01 V to −1 V. The transistor has channel length of 10 μm, channel width of 500 μm. Ion gel is based on ionic liquid [EMI][TCB].

6.2.3 Printed CNT Inverters with Reduced Channel Lengths

Inverters were fabricated with two identical ambipolar CNT EGTs. As shown in the inset of Figure 6.3 a, the gate electrodes of both CNT EGTs were connected to the input.

Transistor ***a*** functions more like a p-type EGT, while transistor ***b*** more like a n-type device. When input voltage (V_{IN}) is "low", i.e., 0 V, transistor ***b*** operates in the ON-state and transistor ***a*** in the quasi-OFF state (since there is no real OFF state for ambipolar EGTs), leading to a "high" output voltage (V_{OUT}), i.e., V_{DD} (1 V), and vice versa. The transfer characteristics of a typical ion gel-gated CNT inverter are shown in Figure 6.3 a with V_{DD}= 1 V (red curve). V_{OUT} switches between 0 and 1 V, with the trip voltage around 0.5 ~ 0.7 V, and an average gain of 20. The hysteresis between the forward and backward sweeps is likely related to hysteresis in the EGT transfer curve.

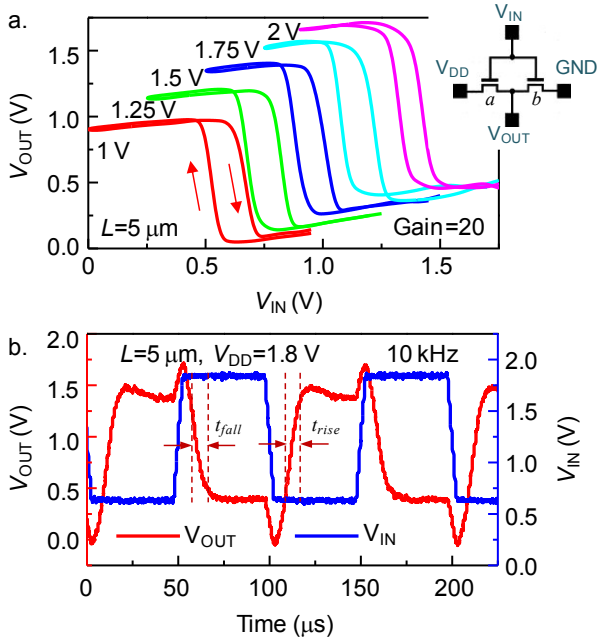

Figure 6.3 Performance of an ion gel gated CNT inverter. (a), The output characteristics of a CNT inverter with different V_{DD} biases. The inverter gain at 2 V is 20. (b), Dynamic response of a CNT inverter to a 10 kHz input signal. The rising and falling time of the input signal is ramped by 5% of the period.

As discussed in last chapter, inverters based on ambipolar EGTs the channel may not be turned OFF completely,[34,275,308,309,313] which effectively results in a static current. Hence, V_{OUT} may not be pulled all the way to V_{DD} or ground. With V_{DD} = 1 V, the output swing is about 95% V_{DD}, which indicates the presence of a small static current. As V_{DD} increases (transfer curves shown in color in Figure 6.1 a), the transistor OFF current increases due to the higher drain bias (see discussions in section 6.2.2), hence the output swing decreases, e.g. about 65% V_{DD} at V_{DD} = 2 V. The inverter trip voltage shifts with V_{DD}, which is due to the transistor OFF voltage changing with V_D.

The dynamic response of a printed inverter with channel length of 5 μm was measured at 10 kHz and V_{DD} =1.8 V. As shown in Figure 6.3 b, V_{OUT} (red) followed V_{IN} (blue). To better represent the circumstances in ring oscillators, the inverter was tested with an identical load inverter, and a square wave signal with ramping time of 5% of the period was used as input voltage. The fall and rise time (t_{fall} and t_{rise}) of V_{OUT} indicates how fast the inverter can switch, which directly affects the stage delay in a ring oscillator. The spikes in the output signal likely result from parasitic capacitance at the ion gel/Au electrode interfaces, and the abrupt change of the input voltage, as discussed previously.[34] Here, t_{fall} and t_{rise} are estimated excluding the spikes. For example, t_{fall} is estimated from the duration of V_{OUT} switching from high to low at the falling edge, as shown in Figure 6.3 b. The switching time, $t = (t_{fall} + t_{rise})/2$, is used to characterize the speed of the inverters, in order to qualitatively understand the limits of delay time in a ring oscillator. It is noteworthy that the inverter switching time does not equal the ring oscillator stage

delay time. In fact, in a ring oscillator, the first inverter only has to switch its output to the trip voltage to trigger the second inverter switching. Therefore, t_{fall} and t_{rise} may be longer than the stage delay time in ring oscillators.

6.2.4 Switching Time of Inverters

In a conventional MOSFET, i.e., $I_D \sim \mu C_i(W/L)(V_G-V_{TH})^2$, where W and L are the channel width and length, μ is the CNT mobility, C_i is the sheet capacitance of the dielectric, and V_G and V_{TH} are gate and threshold voltages, respectively. Assuming $V_G-V_{TH} \approx V_{DD}$, the RC time constant can be estimated as $t \sim (V_{DD}/I_D)(C_iWL) \sim L^2/(\mu V_{DD})$. This indicates that, in an inverter in which channel resistance dominates, the switching time increases as L^2. However, as shown in Figure 6.4 a, there are other factors in the system that affect the switching time.

The left panel of Figure 6.4 a exhibits two inverters in series, representing two consecutive stages in a ring oscillator. The switching time of the inverter is the time required for V_B (the voltage at point B) to flip, after V_A (the voltage at point A) flips. The simplified equivalent RC circuit is illustrated in the right panel, where $R_{channel}$ is the channel resistance, R_{gate} is resistance of the gate electrode, R_{gel} is the bulk resistance of the ion gel dielectric, and C_{gel} is the ion gel capacitance. Importantly, the charging and discharging time of each stage is controlled by the total RC time constant. The parameters contribution to the RC time constant are discussed below.

The gate resistance R_{gate} may not be ignored when estimating the RC time (for more details, see discussions in section 6.4), because the gate electrode material, PEDOT:PSS,

has orders of magnitude lower conductivity than a typical metal. In this work, the gate electrodes were scaled to match the channel width, but were fixed in length (50 μm) and thickness (1 μm). Consequently, the gate resistance of the inverters was independent of channel length, and scaled with channel width as $R_{gate} \sim \rho W$, where ρ is the resistivity of PEDOT:PSS.

Likewise, the bulk ion gel resistance R_{gel} may not be discounted. The printed gel area scaled with both channel dimensions, such that $R_{gel} = H/(\sigma WL)$, where σ is the ionic conductivity, H is the ion gel thickness. With thickness fixed, $R_{gel} \sim (WL)^{-1}$. Considering all three contributions, the total RC time of the inverter scales with length as $t_{switch} \sim (R_{channel}+R_{gate}+R_{gel})C_{gel} \sim (LW^{-1}+ W+ WL^{-1})(WL) \sim L^2+W^2L^1+L^0$. Figure 6.4 b displays the measured inverter switching times as a function of EGT channel length keeping the channel width constant (100 μm). [EMI][TCB] ion gel with a thickness of 1.2 μm was printed as the dielectric layer. Each data point represents the average and standard deviation of switching times measured from 5 inverters, at $V_{DD} = 1.8$ V. As expected, the switching time increases with channel length, and the data are well fit by $t_{switch} = a_1 + a_2L + a_3L^2$, a polynomial which follows from the discussion above. The a_2L term represents the contribution of gate electrode, and a_3L^2 represents the channel dependence. Interestingly, the contribution of $R_{gel}C_{gel}$ to the total RC time constant has no L dependence, as can be seen from the scaling relationships above.

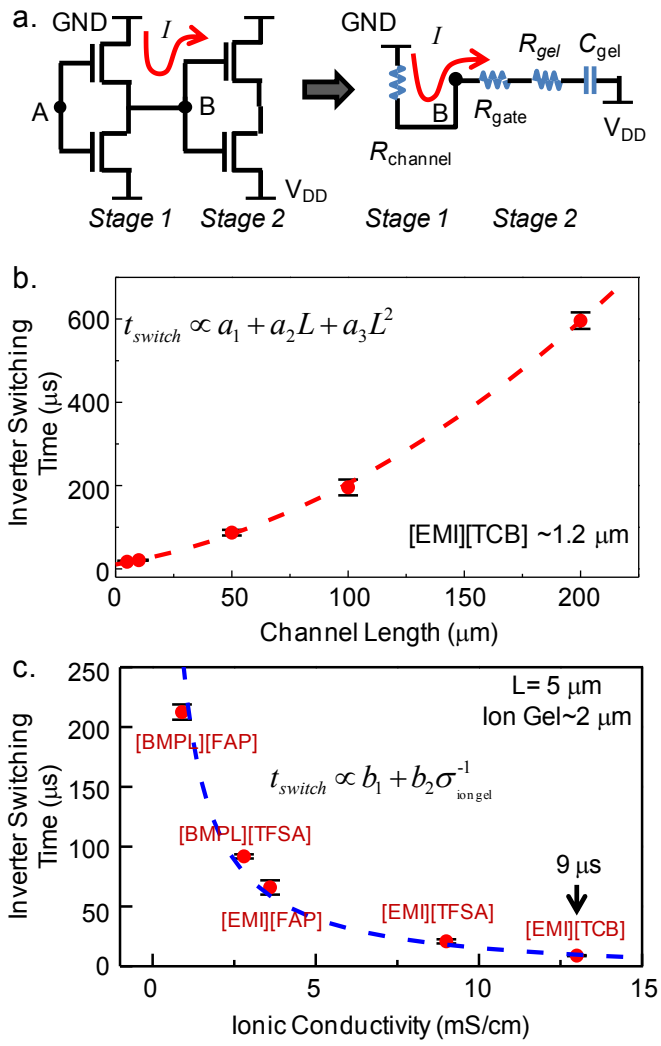

Figure 6.4 Parameters affecting the frequency and switching time of the CNT inverters. (a), The circuit diagram and equivalent circuit of two consecutive inverter stages. (b), Inverter delay time as a function of EGT channel length (W=100 μm). The thickness of [EMI][TCB] ion gel is 1.2 μm, with ionic conductivity of 13 mS/cm. Fitting curve (red dashed line) shows t_{delay}~L+L^2. (c), Inverter delay time as a function of ion conductivities in ion gels. L=5 μm, and ion gel thickness is 2.3±0.3 μm. Fitting curve (dashed line) shows t_{delay}~σ^{-1}.

However, R_{gel}, and thus the switching time, does depend on the ionic conductivity of the gel and on the printed gel layer thickness. The dependence of t on ionic conductivity

is shown in Figure 6.4 c. Five different ion gels each containing 10 wt% polymer and 90 wt% ionic liquid were employed. The low weight percentage of polymer content ensured the ion conductivity is close to the pure ionic liquid.[86,314] The ionic liquids 1-ethyl-3-methylimidazolium tetracyanoborate ([EMI][TCB]), 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide ([EMI][TFSA]), 1-ethyl-3-methylimidazolium tris(pentafluoroethyl)trifluorophosphate ([EMI][FAP]), 1-Butyl-3-methylimidazolium tris(pentafluoroethyl) trifluorophosphate ([BMPL][FAP]), and 1-Butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)amide ([BMPL][TFSA]) have ionic conductivities varying from 0.9 mS/cm to 13 mS/cm. As shown in Figure 6.4 c, as the ionic conductivity increases, the inverter switching time decreases from 210 μs to 9 μs; the times were measured with devices having ~ 2 μm ion gel thickness and 5 μm source-drain channel lengths. Each data point shows the average and standard deviation of 3 inverters. As expected, the switching time scales as σ^{-1}, and $t_{switch} = b_1 + b_2\sigma^{-1}$ (blue dashed line) fits the data well. This indicates that in ion gel-gated EGTs, higher ionic conductivity, i.e., faster ion motion, can lead to faster switching of the transistors.

Figure 6.4 b and c exhibit the contributions of the EGT channel and ion gel bulk resistance to the inverter switching time. Of course, the quantitative scaling relationships may vary if other circuit parameters change. For example, with ultra-thin, high conductivity ion gels (i.e., small R_{gel}), or very conductive gate electrodes (i.e., small R_{gate}), the channel resistance alone will dominate the total RC time. Then the switching time will simply scale as L^2. It is nevertheless clear that scaling down the transistor

dimensions and reducing the ion gel thickness[315] or enhancing its ionic conductivity should further improve the switching speed.

6.3 Ring Oscillator Performance with Optimized Circuit Parameters

As discussed above, short channel length, high ionic conductivity and thinner ion gel can lead to shortest switching time of ion gel-gated CNT inverters. In general, the fast the inverter can switch, the higher frequency of ring oscillator will have. Therefore, fast 5-stage ring oscillators were fabricated with L= 5 ~ 10 μm, ion gel thickness 1 ~ 2 μm, and ion gel based on ionic liquid [EMI][TCB] which ionic conductivity is among the highest (~ 13 mS/cm).

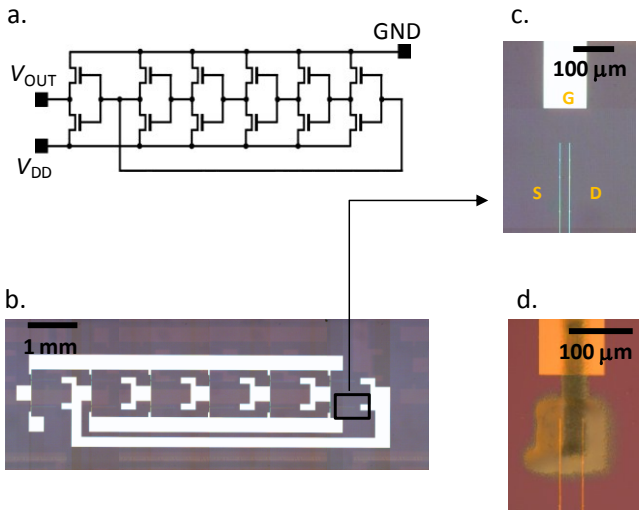

Figure 6.5 Circuit diagram and optical images of ring oscillator. (a) The circuit diagram of 5-stage ring oscillator. Each stage consists 2 identical CNT EGTs. (b) The optical image of Au electrodes and interconnections patterned on Si/SiO_2 substrate. (c) A zoom-in view of the channel area of one EGT, with 2 μm wide source and drain electrodes. (d) Optical image of a completed CNT EGT with printed CNT, ion gel and PEDOT:PSS layers.

As illustrated in the circuit diagram of Figure 6.5 a, the printed ring oscillator consisted of 5 inverter stages and a buffer stage, where each stage employed two identical ion gel-gated ambipolar CNT EGTs. The channel dimensions were defined by 2 μm-wide Au source/drain electrodes, which were pre-patterned on a Si/SiO_2 substrate by photolithography. The layout of patterned Au electrodes on the Si/SiO_2 substrate is shown in Figure 6.5 b, and an expanded view of one EGT is shown in Figure 6.5 c. The fabrication of EGTs are similar as introduced in previous chapter, except the ion gel is based on ionic liquids such as 1-ethyl-3-methylimidazolium tetracyanoborate ([EMI][TCB]) and a structuring triblock copolymer, poly(styrene-b-methyl methacrylate-b-styrene) (PS-PMMA-PS).

The photomicrograph of a completed CNT EGT is shown in Figure 6.5 d. Importantly, by using narrow source and drain electrodes, the parasitic capacitance between the gate and the source and drain is reduced and hence the parasitic peaks in the ring oscillator output signals are significantly attenuated compared to the work demonstrated in chapter 5.

With improved device architecture, Figure 6.6 a displays the output signal generated by a representative (but not the fastest) 5-stage ring oscillator, with transistors having 10 μm channel lengths and 100 μm channel widths. At supply voltage V_{DD} as low as 2 V, the output frequency of the circuit was 22 kHz, which is about 1 order of magnitude faster than our previous report.[34] The output frequency, f, increased from 13 kHz to 25 kHz as V_{DD} increased from 1.5 V to 2.6 V, shown in Figure 6.6 b (red solid circles). The stage

delay time (blue open circles), t, was estimated from $t = 1/(2Nf)$, where $N = 5$ is the number of stages in the ring oscillator. At $V_{DD} = 2.6$ V, the shortest stage delay time for this oscillator was 4 µs.

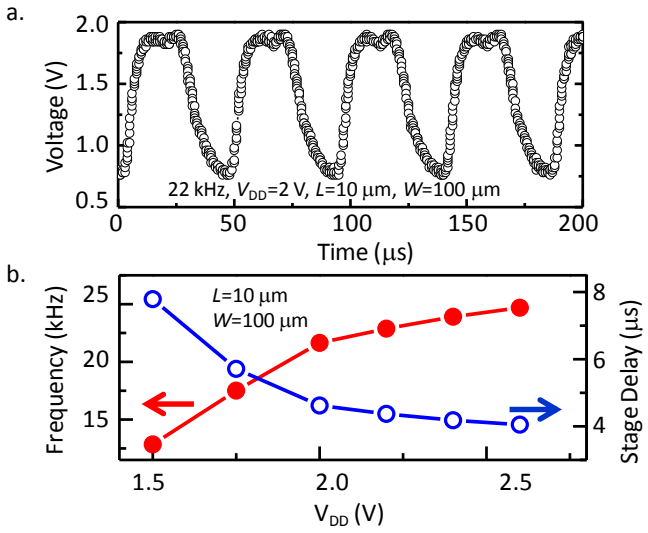

Figure 6.6 Circuit performance of fast printed 5 stage ring oscillator. (a) The output characteristic of an ring oscillator with L=10 µm, W=100 µm, at 2 V supply voltage (V_{DD}). The output frequency is 22 kHz. (b) The frequency and stage delay time as a function of V_{DD}.

In addition, the ring oscillator with channel length down to 5 µm in similar architecture was demonstrated, which is expected to have higher frequency as discussed in section 6.3. Figure 6.7 demonstrates a 83 kHz output signal generated by a 5-stage printed ring oscillator at $V_{DD} = 2.2$ V, with a stage delay time of 1.2 µs. The CNT EGTs have channel length of 5 µm, channel width of 100 µm, and [EMI][TCB] ion gel of 1.2 µm in thickness. However, the output swing of ring oscillator is only 0.8 V (36% V_{DD}), which is likely due to the higher off current when channel length is too short. This effect

is note-worthy when considering the further optimization of electronics based on the CNT EGTs.

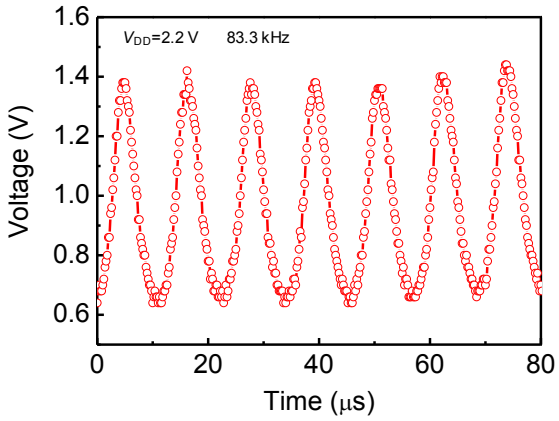

Figure 6.7 Fast printed ion gel-gated CNT ring oscillator with 83 kHz output frequency, at VDD=2.2 V.

6.4 Parasitic Resistance of Printed Gate Electrode

PEDOT:PSS is one of the most conductive polymer used in flexible and printed electronics. However, the PEDOT:PSS conductivity (500~1000 S/cm) is orders of magnitude lower than metal. In order to understand the effects of using the PEDOT:PSS as gate electrode in printed circuits, the capacitance-frequency (C-*f*) characteristics of the Au/ion gel/Au capacitor, and PEDOT:PSS/ion gel/Au capacitor were compared in Figure 6.8. The Au/ion gel/Au capacitor was fabricated by printing the [EMI][TCB] ion gel on pre-patterned Au electrode, and followed by laminating a 1 mm × 2 mm Si/SiO_2 substrate coated with Au thin film on top.[315] The top Au electrode was biased by a 10 mV AC signal superimposed on a DC voltage, while the bottom Au electrode was grounded. The device structure is shown as the inset of Figure 6.8 a. The sheet capacitance, which is

about 2 μF/cm^2, has a weak dependence on the frequency from 100 Hz to 100 kHz as shown in Figure 6.8 a. This indicates the formation of electrical double layer in this capacitor structure can follow well up to 100 kHz, i.e., the *RC* time is smaller 10 μs. In addition, the capacitance does not change with various voltage biases.

On the other hand, a PEDOT:PSS/ion gel/Au capacitor was measured for comparison. A 5 mm×2.5 mm capacitor was fabricated by printing the [EMI][TCB] ion gel on pre-patterned Au electrode, and followed by printing a thin film of PEDOT:PSS. The structure is shown as the inset of Figure 6.8 b. The voltage bias was applied on the PEDOT:PSS electrode, while the bottom Au electrode was grounded. At 0 V (black curve), the capacitance shows a plateau of about 2 μF/cm^2 at the frequencies < 10^4 Hz, and starts to decrease when f > 10^4 Hz. The plateau region indicates the formation of electrical double layer at the ion gel interfaces, which is similar to that in the Au/ion gel/Au capacitor as discussed in the previous section. When the frequency is larger than the RC time constant of the capacitor, the charging and discharging of the capacitor is limited by the bias frequency, and the electric double layer cannot be completely established within a signal period. Effectively, the capacitance decreases at higher frequencies. The difference between Figure 6.8 a and b is that PEDOT:PSS electrode has higher resistance compared to the Au electrode, which limits the charging current of the capacitor and increases the *RC* time.

In addition, the resistance of PEDOT:PSS gate electrode is a function of gate voltage. At negative voltage bias, e.g., −1 V (blue curve), the characteristics of capacitance > 1

kHz remains the same as above. However, with positive bias, +1 V, the high frequency capacitance decreases, leading to a slower capacitance response to frequency. This is attributed to the higher resistance of oxidized PEDOT:PSS under positive bias. It is worthwhile to note that, with a non-zero bias, the capacitance increases at lower frequency range due to ion diffusion into the polymer electrode (supercapacitance).

In conclusion, when using the PEDOT:PSS as electrodes, the effect of its resistance should not be ignored. In comparison with a metal electrode, PEDOT:PSS has higher resistance and an obvious dependence on voltage, which plays an important role in circuit RC time constant. The conductance of the PEDOT:PSS electrode, or other printed electrodes needs to be considered while optimizing the speed of printed circuits.

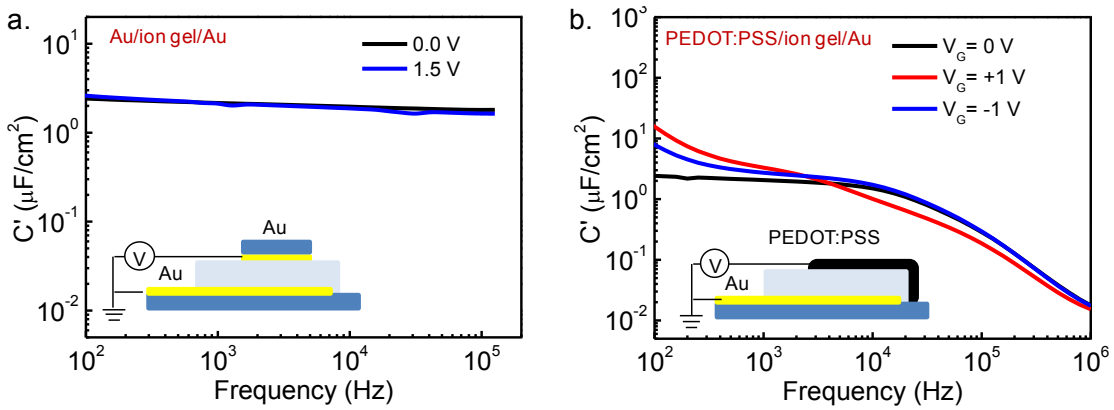

Figure 6.8 Effects of electrode material on frequency response of printed capacitor. (a). The capacitance-frequency characteristics of Au/ion gel/Au capacitor. (b). The capacitance-frequency characteristics of PEDOT:PSS/ion gel/Au capacitor.

6.5 Conclusions

In conclusion, 5-stage ion gel gated CNT ring oscillators can achieve fast frequencies > 20 kHz, corresponding to stage delay times < 5 μs at supply voltages below 3 V. These are the fastest printed circuits reported to date operating at low voltages. The switching times of the inverter stages are affected by the resistances of the semiconductor channel, gate electrode, and ion gel layer, as well as the gate capacitance and they increase with channel length and decrease with ion gel conductivity, following straightforward scaling arguments.

It can be anticipated that further decreases in the transistor dimensions, reducing the ion gel thickness,[315] and enhancing the ion gel ionic conductivity should improve the switching speed. It is instructive to consider quantitatively what delay times can be achieved. The resistance of each series element of the 10 μm channel length EGTs is estimated to be: $R_{channel} = V_D/I_D \approx 0.1$ V/100 μA = 1 kΩ; $R_{gel} = H/(\sigma WL) \approx 1$ μm/(10 mS/cm ×10 μm×100 μm) = 1 kΩ; $R_{gate} \approx 1$ kΩ . That is, for the shorter 10 μm channels have been investigated in this study, the resistances of the three elements are comparable. In order to achieve 1 MHz frequency operation, a factor of ~5 reduction in overall RC time constant is necessary, as what have been shown here that 5 μs switching times are readily achievable with 10 μm long channels. The gate resistance can be reduced by using high conductivity, printable material, such as metallic CNTs, or by scaling down the channel width (length of the gate electrode). Lower gel resistance requires electrolyte with higher ionic conductivity, or a thinner gel layer. A five-fold reduction implies a gel

thickness of 200 nm, which is clearly feasible. There are several strategies that can lead to lower channel resistance. One is to increase the CNT network coverage, which will increase the effective mobility. Alternatively, scaling down the channel length will also lead to lower channel resistance, and to decreased channel capacitance. An L=4 μm channel will have approximately 5 times smaller RC constant than the sub-5 μs value that have been achieved here, for example. Thus, making all of the changes described here should allow 1 μs delay times, or 1 MHz operating frequencies, to be obtained.

Finally, in considering switching speed, it is important to bear in mind that other "parasitic" parameters may exist in printed circuits that can increase signal propagation delays. One important example is parasitic capacitance, e.g. capacitance between the gate and the source/drain electrodes. Parasitic capacitance may be a particularly challenging problem in printed electronics where precision patterning is challenging and electrode roughnesses may be high. These factors will add to the overall *RC* time constants.

Chapter 7 Printed Flexible Circuit with Integrated Electrochromic Pixel*

7.1 Introduction

Printing of organic integrated circuits (OICs) consisting of both active and passive electronic components (e.g., transistors and diodes vs. resistors and capacitors) is a desirable goal and also a substantial challenge for the field of organic electronics. However, to date the quantity and complexity of OICs fabricated by printing of electronically functional inks is far below that of OICs produced by conventional photolithographic methods as discussed in previous chapters. This is primarily because liquid-phase printing of OICs involves a range of materials engineering issues that have yet to be satisfactorily addressed, including multi-layer registration, spatial resolution, and materials/process compatibility.

This chapter demonstrates a printed low voltage flexible circuit which is fully integrated with a large (2 mm x 2 mm) printed polymer electrochromic pixel. In order to control large drive currents at low voltages, a combination that is necessary for driving an EC pixel, electrolyte gated transistor (EGT) technology was employed for the transistors. EGTs produce large drive currents at low supply biases by virtue of an ultra-high capacitance electrolyte gate insulator layer that allows large charge densities to be induced in the EGT channels.[24,27,87,289] The completed circuit generates a 2 V output signal to switch the color of the printed electrochromic pixel reversibly. The circuit has

* This work is under preparation for submission. Ha, M., Zhang, W., Braga, D., Renn, M. J., Kim, C. H., Frisbie, C. D., Aerosol jet printed, 1-Volt drive circuit on plastic with integrated electrochromic pixel.

remarkably good operational stability with essentially no degradation in performance over 100 min of continuous operation. The key elements, e.g. EGTs, capacitors and EC pixels, are designed to use similar materials and structures, which significantly simplifies the printing process and enhances the reproducibility of the devices.

It is important to note that EC displays based on electrochromic π-conjugated polymers currently represent a very active field of research.[317-319] An outstanding problem for EC displays has generally been their slow switching speeds (on the order of seconds) which are the result of relatively low ionic fluxes into or out of the electrochromic polymers upon voltage changes.[320] By using high conductivity ion gels in printed EC pixels, it is demonstrated here efficient switching at 1 Hz, which is faster than most current demonstrations in the literature. The possibility of much faster switching on the order of 100 Hz is also discussed.

7.2 Device Fabrication and Characterization

This section introduces the design and fabrication method of the circuit, and the characteristics of each key element, including the electrolyte-gated transistors (EGTs), capacitors, electrochromic (EC) pixels, and resistors.

7.2.1 Circuit Diagram and Design

OICs were fabricated on transparent, flexible PET substrates using the aerosol jet printing technique that has been described in chapter 2. The dimensions of the circuit elements were defined by Au contacts pre-patterned by photolithography. The functional

materials were all printed. These materials included P3HT, the ion gel based on [EMI][TFSA] and a matrix of the triblock copolymer PS-PMMA-PS, PEDOT:PSS, metallic carbon nanotubes (*m*-CNTs), PMMA and Ag.

Figure 7.1 illustrates the design of the entire circuit, which is composed of 23 EGTs, 12 capacitors, 20 resistors and 9 crossovers. The three main components of the circuit, are the pulse generator, pixel driver, and electrochromic display pixel. By applying an input signal, the pulse generator, which includes 4 inverter chains and 3 NAND gates, will generate two pulses. The input signal can be triggered by a function generator, or by a switch connected to V_{DD}. There are 3 stages of inverters in each chain. When the input signal passes through an inverter stage, the pulse is flipped and delayed. The delay time (t_{delay}) is a function of the *RC* time constant of the inverter. The more stages the signal has passed, the more delay it has compared to the original input. NAND 1 combines the signals after chain 1 and chain 2 (as labeled in Figure 7.1 b), and outputs a pulse signal, the width of which is determined by the time difference between outputs of chain 1 and chain 2. The pulse width is determined by $n \times t_{delay}$, where n is the number of stages in each inverter chain. This eliminates the effect of the input width, e.g. the duration of pressing the switch, on the circuit output signal. Chain 3 and chain 4 generate a second pulse signal in the same way, which is delayed in time compared to the first pulse. The two separate pulses enter NAND 3 and leave as two pulses in sequence. Simply increasing the number of inverter chains and NAND gates can increase the number of pulses, i.e., 6 chains and 4 NANDs can generate 3 pulses and switch the display 3 times.

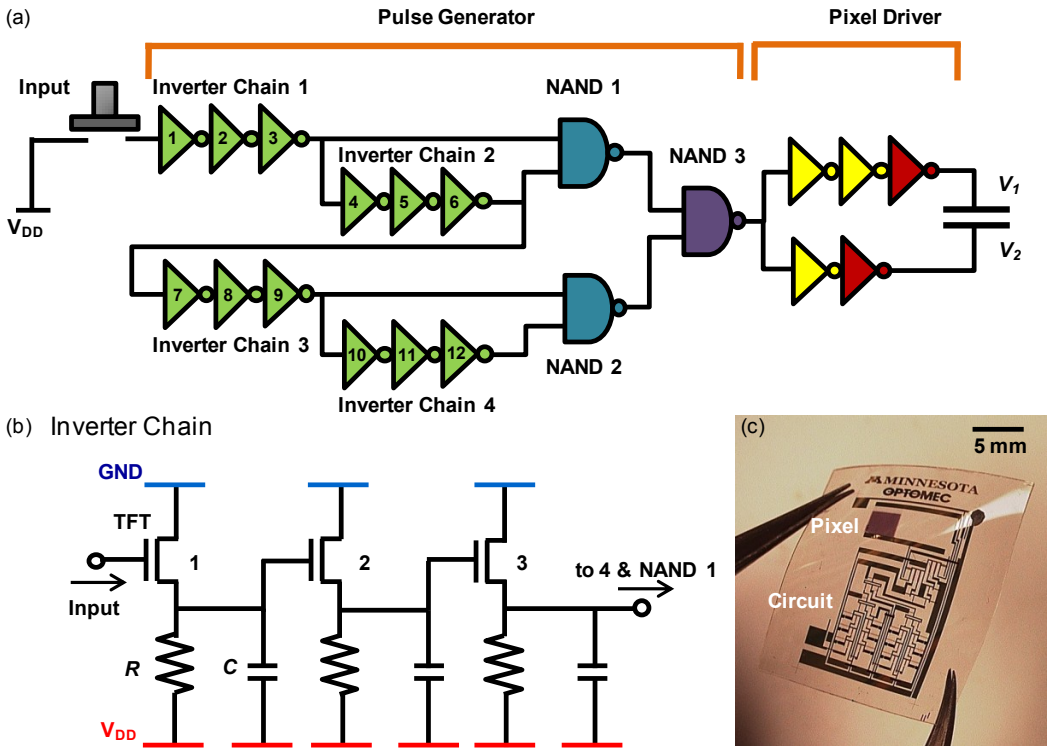

Figure 7.1 Printed, flexible circuit and electrochromic pixel based on ion gel and P3HT. (a) Diagram of the driving circuit. (b) Circuit layout of single inverter chain. (c) Optical photo of the printed circuit with a 2.5×2.5mm^2 electrochromic display pixel on a flexible PET substrate.

Before the pulses going into the EC pixel (represented by a capacitor in Figure 7.1a), the pixel driver modulates the shape of pulses and boosts the current to drive the pixel more efficiently. The output splits into two opposite signals V_1 and V_2 after the driver, because the pixel requires that the drive bias has both polarities (+1 V and -1 V).

Figure 7.1 b shows the component level of the first inverter chain, i.e., inverter stage 1 to stage 3. A typical p-MOS inverter includes an EGT and a load resistor, *R*, which are in series between ground and V_{DD}. The input signal enters the gate electrode of the EGT, and the output leaves from the node between the EGT and load resistor. In this

demonstration, an extra capacitor, C, is added between the V_{OUT} of the inverter and V_{DD}. The capacitor influences the charging and discharging time, i.e., the RC time of each stage. By controlling the size of the capacitance, the inverter stage delay time, t_{delay}, can be easily adjusted, and thus the width of the output pulses. The load resistors in the circuit have systematically decreasing resistance across individual delay chains. This gradient in resistance improves pulse shape and reduces the power consumption. The optical image of the drive circuit (2.5 cm× 2 cm) with an electrochromic display (2.5 mm× 2.5 mm) printed on PET substrate is shown in Figure 7.1 c. The architecture and characteristics of each key element of the circuit are discussed in following sections.

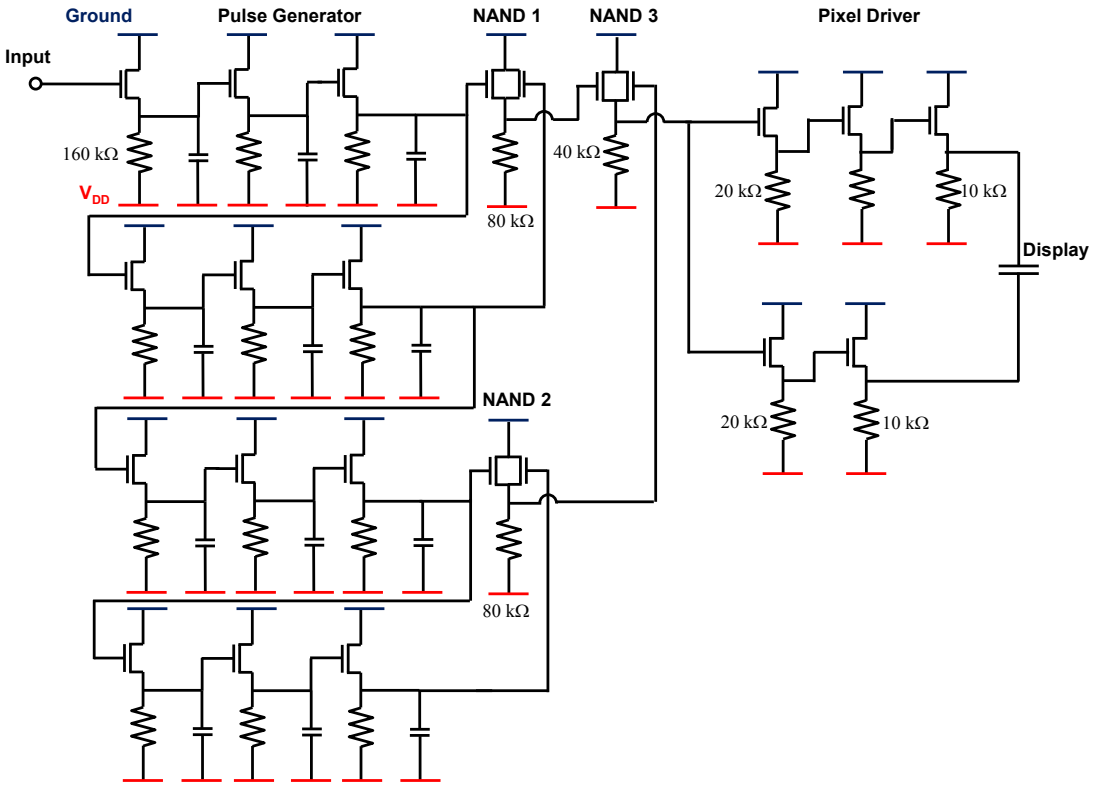

Figure 7.2 Diagram of printed circuit.

The detailed circuit diagram of the full circuit is shown in Figure 7.2. The printed circuit consists of three elements, a pulse generator, a pixel driver, and a display pixel. Except for the last stage of the pixel driver, the EGTs are 25 μm in length and 500 μm in width. To boost the output current, the last stage of the pixel driver employs an EGT with 25 μm in length and 2000 μm in width. The load resistor varies from 160 kΩ to 10 kΩ. The sizes of resistors in each stage are carefully chosen to balance the power consumption, switching speed, signal swing and shape. For example, large resistors in pulse generator ensure low power consumption, and small resistors in pixel driver can provide higher output current. The capacitance of load capacitors can be tuned by the thickness of the P3HT layer. Printed circuit outputs two consecutive pulses to switch the color of printed electrochromic pixel. The resistors and capacitors together control the switching frequency of the EC pixel.

7.2.2 Printed EGTs

The printed P3HT EGTs in the drive circuit have channel lengths L= 25 μm and widths W = 500 μm, except for the EGTs in the last stage of the pixel driver with channel width of 2000 μm to ensure high output current. Figure 7.3 a left panel displays the stacked structure of an ion gel gated P3HT EGT. Source and drain electrodes and the circuit interconnects were pre-patterned on the PET substrate. The printing sequence was P3HT semiconductor, ion gel gate insulator, followed by PEDOT:PSS which served as the gate electrode. The operating mechanism of EGTs is shown in the lower panel. Under

negative gate bias, $[TFSA]^-$ anions migrate to the ion gel/P3HT interface, where electrochemical oxidation of P3HT polymer chains occurs. This switches the P3HT from insulating (OFF state) to conductive (p-type ON state) and increases the drain current (I_D) of the EGT by 5 orders of magnitude (Figure 7.3 b). In electrolyte gated devices, it is important to consider penetration of ions into the semiconductor if it is permeable. In this case, P3HT is permeable to the ionic liquid [EMI][TFSA] and thus electrochemical oxidation (hole doping) of the entire thickness of P3HT can occur if there is sufficient time for electrochemical reaction and ion diffusion. Therefore, EGTs allow three dimensional gating of ion-permeable semiconductors, and this in turn means very high drive currents are possible. Importantly, the electrochemical oxidation process is reversible, so that the device may be cycled between the ON and OFF states repeatedly. At the ion gel/PEDOT:PSS interface, $[EMI]^+$ cations can also penetrate into the conductive polymer layer under negative bias, providing enough gate capacitance such that the total series capacitance of the PEDOT/gel/P3HT stack remains very high.[93,321]

The electronic characteristics of the EGT were measured in an N_2 environment and are shown in Figure 7.3 b and c. The transfer curve in Figure 7.3 a was acquired with the gate voltage (V_G) sweeping from 0.8 V to −1.2 V and back, at 75 mV/s. The p-channel EGT turned on at $V_G \approx 0$ V, at $V_D = -0.1$ V (drain voltage) and the ON/OFF ratio was above 10^5. Since all the devices were printed in ambient air, during printing the P3HT film was likely doped with oxygen. This resulted in slight p-doping of the P3HT layer and caused the V_{th} to shift to positively.[322,323] This air doping effect can lead to a non-desirable leakage current at 0 V in the circuit. The printed devices were stored in rough vacuum (>

10^{-3} Torr) at room temperature for 2 days, in order to de-oxygenate the P3HT. Ideally, printing in inert environment could eliminate this problem.

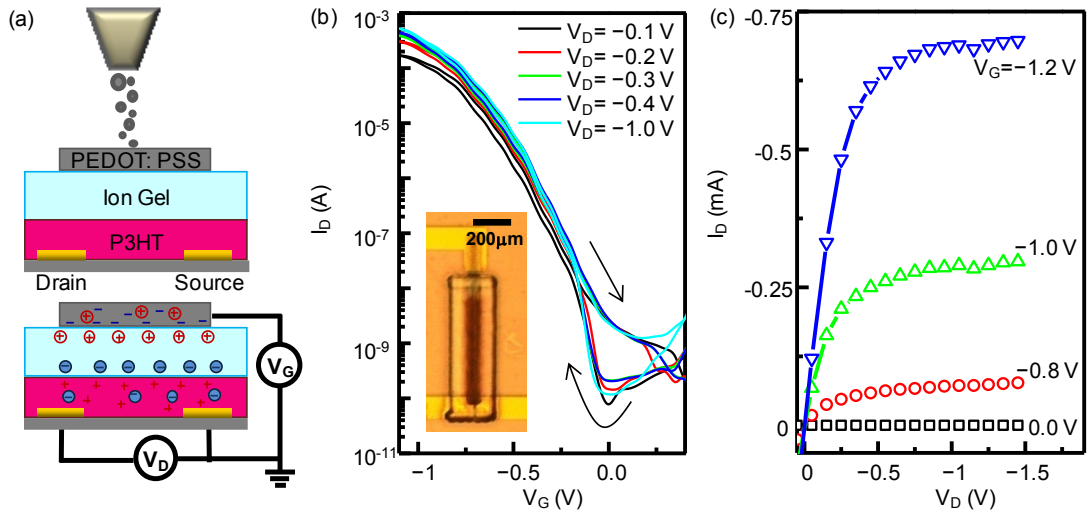

Figure 7.3 Printed ion gel gated P3HT EGTs. (a) The stacked layer structure of a printed EGT. Lower panel illustrates the bias condition as the EGT in on- state. (b) Transfer characteristics of a typical printed EGT. (c) Output characteristics of a typical EGT.

The transfer I-V curves were also carefully measured with different V_D bias, from −0.1 V to −1 V. The ON current increased with V_D, while the turn-on voltage had weak dependence on V_D, as expected. The output curve in Figure 7.3 b shows clear linear and saturation regimes. In saturation regime, the drain current increases slightly with drain bias, which may be due to the non-uniform space profile of ions under large drain bias. The photomicrograph of a printed EGT is shown in the inset of Figure 7.3 b.

The transfer curve shows that the hysteresis between the forward and backward sweep is small, indicating that ion diffusion is not limiting at V_G sweep rates of 75 mV/s. Actually, it has been shown previously that P3HT EGTs can easily work at speeds of

several hundred Hz.[25] With a close look at the OFF-state current, one can see the drain current in forward sweep is about 1 order of magnitude lower than the backward sweep, which appears like a hysteresis. However, the mechanism of the hysteresis is the different sources of the OFF-state currents in the forward and reverse sweep. The origin of the OFF current in forward sweep is the transient current through the ion gel electrolyte. It can be seen from the inset of Figure 7.3 b, a small part of the source and drain electrodes are exposed to ion gel electrolyte. This interface effectively acts as a parasitic capacitor (C_P). When V_G is sweeping, there is a small charging or discharging current due to this parasitic capacitor, and the current can be estimated by $I=C_P \times dV_G/dt$, where dV_G/dt is the sweeping speed of V_G. For the metal/ion gel interface, C_P is about 10 μF/cm^2.[87] Given the area of C_P is about 200×100 μm^2, and the sweep rate is 75 mV/s, the transient current is estimated to be 1.5×10^{-10} A, which matches with the experimental data in Figure 7.3 b. This current can be reduced by optimizing the architecture, in particular minimizing the ion gel/source and ion gel/drain overlaps. As to the backward sweep, the dominant factor influencing the OFF current is the number of carriers remaining in the trap states in the semiconductor. These traps are shallow enough so that the carriers can be extracted by a slightly positive V_G, *e.g.* >0.5 V. The OFF current of the consecutive forward sweep will not be affected. Both forward and backward OFF currents are independent on V_D bias, indicating the static current through the ion gel electrolyte is very small.

7.2.3 Printed Capacitors

As mentioned above, the total delay time, $n \times t_{delay}$, in a single delay chain determines the width of the output pulse. The number of stages n is not flexible once the circuit design is fixed. t_{delay} is a function of R and C, where R is determined by the load resistor, and C is the capacitance of transistor. Neither of these two factors can be tuned freely in a typical circuit.[25] To solve this problem, an extra load capacitor is added in each stage of the inverter, which can be independently varied without affecting the inverter's parameters. The larger the capacitor is, the longer it takes to charge and discharge, thus longer t_{delays} can be achieved.

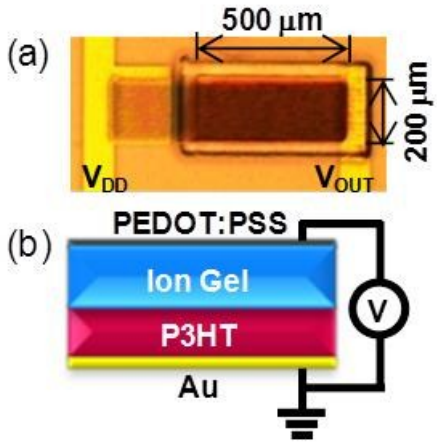

Figure 7.4 Printed ion gel/P3HT capacitors. (a) A photomicrograph and (b) cross section of the printed capacitor.

Figure 7.4 a shows the photomicrograph of a capacitor (500 μm × 200 μm), which dimension is defined by the bottom Au electrode. The cross-sectional view of the capacitor is illustrated in Figure 7.4 b, where the P3HT and the ion gel serve as the

semiconductor and dielectric layer, respectively. The top electrode PEDOT:PSS connects to V_{DD}. The structure of the ion gel/P3HT capacitor is similar to a metal-insulator-semiconductor (MIS) capacitor. Depending on the relative bias between the top and bottom electrodes of the capacitor, P3HT can be electrochemically oxidized or re-reduced, which is equivalent to the charging and discharging process of conventional MIS capacitors. With thicker P3HT films, there is larger electrochemical charging capacity, and thus higher capacitance can be achieved.

The capacitance is measured as a function of bias frequency in Figure 7.5 a. A DC bias (0 V) superimposed with a 10 mV AC bias was applied to the PEDOT:PSS electrode. Without the P3HT layer, the capacitor, which is only an ion gel layer sandwiched in between the PEDOT:PSS and Au electrodes, displayed *C-f* behavior typical of a double-layer capacitor (black curve).[87] Capacitance exhibited a plateau of ~ 3 $\mu F/cm^2$ at $f < 10^5$ Hz. The large capacitance may result from a combination of electrical double layer (EDL) formation at the Au/gel and PEDOT/gel interfaces. It may also reflect redox processes in the PEDOT (so-called 'pseudo-capacitance'). By adding 200 nm P3HT layer into the capacitor, the capacitance at lower frequencies ($<10^4$ Hz) was significantly enhanced (red curve). The capacitance boost appeared to be a strong function of the bias frequency, because the lower frequencies allow electrochemical oxidation to occur whereas high frequencies do not. The thickness of P3HT layer has more impact at the capacitance in low frequency regime. For instance, at 50 Hz, the capacitor with 200 nm P3HT exhibits 50 $\mu F/cm^2$, and the one with 300 nm P3HT

displays 80 μF/cm^2(green curve). For $f > 10^5$ Hz, capacitance decreased because EDL formation and redox reaction was suppressed. At the highest frequencies, only the bulk polarization of the ion gel contributes to the capacitance, which gives a capacitance that is orders of magnitude smaller than EDL and pseudo-capacitance. In these two regimes, because of the suppression of diffusion, P3HT thickness has no effect on the capacitance.

Figure 7.5 b shows the capacitance-voltage (*C*-*V*) characteristic of a capacitor with 200 nm P3HT. With $V > -0.3$ V, the capacitance is small and weakly dependent on *V*. As the applied bias sweeps to more negative voltage, holes are injected into P3HT, and the capacitance starts to increase. Comparing *C*-*V* under different frequency, it can be seen that the capacitance goes up with lower frequency, consistent with discussions above. The capacitance at 10 Hz, −1.5 V is about 200 μF/cm^2. The integrated circuits demonstrated in this report majorly works in ≤1 Hz frequemcy.

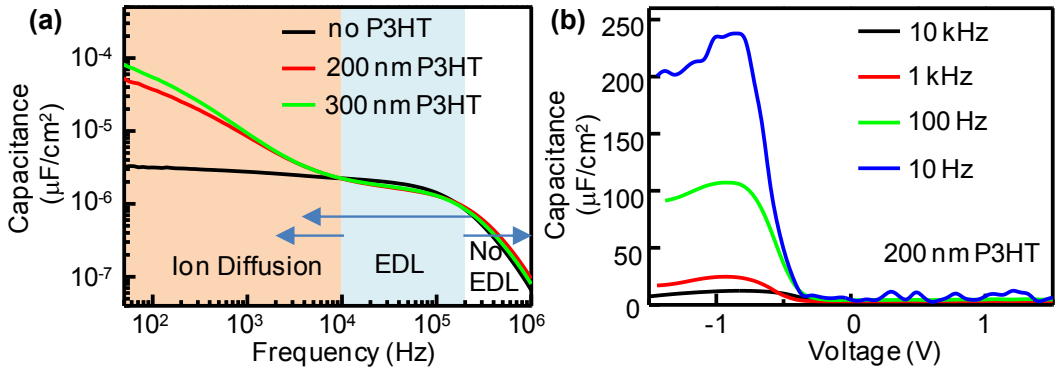

Figure 7.5 Electrical characteristics of printed capacitor. (a) Capacitance-frequency (*C*-*F*) characteristics of printed capacitors, comparing no P3HT layer (black), P3HT layer of 200 nm (red) and 300 nm (green) in thickness, respectively. (b) Capacitance-voltage (*C*-*V*) characteristics of the printed capacitor.

The quasi-static capacitance measured by displacement current is illustrated in Figure 7.6. The charging and discharging current was measured when voltage was swept in 2.86V/s from 1.5V to -1.5V and backward. The 200 nm P3HT capacitor (red curve) showed much higher current comparing to the capacitor without P3HT (black curve). Integration of the shadow area gives a capacitance difference of 520 μF/cm^2. Since the whole sweep takes about 1 s, this capacitance value can be considered similar as under 1 Hz bias.

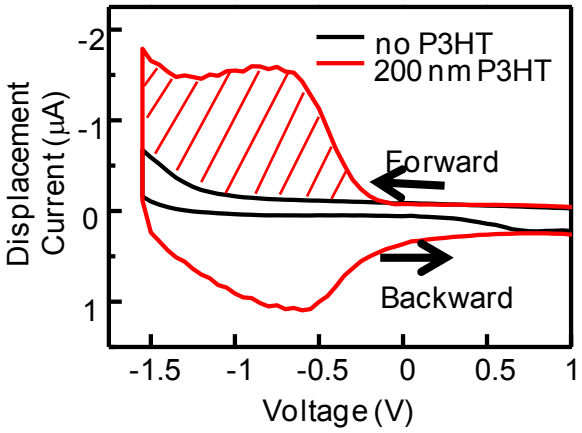

Figure 7.6 Displacement current of capacitors with and without P3HT layer. By integrating the shaded area, the effective capacitance is estimated to be 500 μF/cm^2. Voltage is swept at 2.86 V/s.

When the circuit is operating, neither voltage nor frequency is static, which means the real capacitance is changing with time. In order to characterize the effective capacitance of the ion gel-gated P3HT capacitor in the drive circuit, and its impact on the average delay time, t_{delay} was measured as a function of P3HT thickness and shown in Figure 7.7 a. t_{delay}, was measured from the time difference between the rising edges of two

consecutive odd or even inverter stages. Each data point of t_{delay} shown in Figure 7.7 a was averaged based on 12 inverters, where the EGTs and load resistors were the same. t_{delay} for P3HT=0 nm was acquired from the inverter without load capacitors. The P3HT layer thicknesses were varied from 156 nm to 944 nm in the load capacitors, which resulted in t_{delay} increasing from 0.3 s to 1.1 s. The change of t_{delay} showed a transition from linear to a saturation regime around 400 nm. The thickness of the P3HT layer in capacitors can be designed based on desired delay time and pulse width.

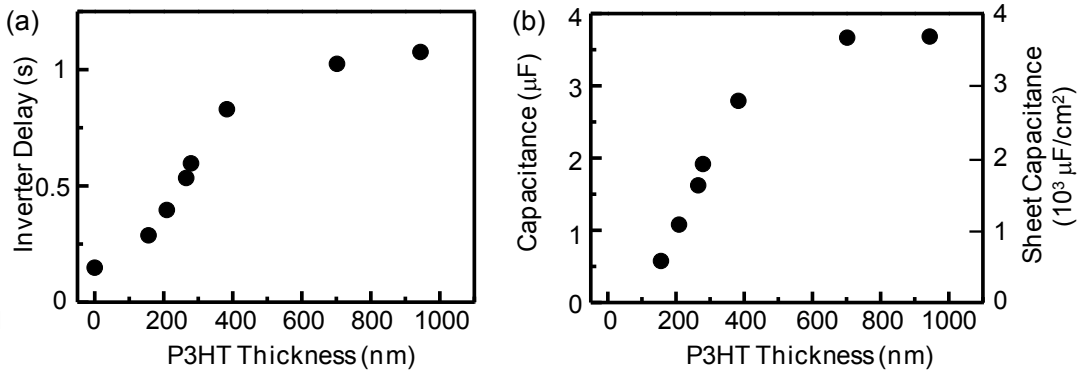

Figure 7.7 Impact on delay time and effective capacitance of printed capacitors. (a) Delay time of the inverters with loaded capacitors. (b) Effective capacitance of the load capacitor estimated from delay time as a function of P3HT thickness. Estimation is based on t=ln2×RC.

It is worth noting that t_{delay} in Figure 7.7 a may not be quantitatively compared to the time constant of *C-F* measurement in Figure 7.5 a, since the charging current in Figure 7.7 a is limited by the inverter EGT, and the current in Figure 7.5 a is limited by the impedance of the impedance analyzer. Figure 7.5 b shows the effective capacitance of the capacitor is up to 3.7 μF at 944 nm, corresponding to a sheet capacitance of 3700 μF/cm^2.

The effective capacitance is estimated based on $t_{delay}(x\ \text{nm}) - t_{delay}(0\ \text{nm}) = Ln2 \times RC$, where R=160 kΩ is the resistance of the load resistor in the inverter chains.

The ion gel/P3HT capacitor is characterized by several different measurements. All measurements demonstrate the capacitance is a function of the P3HT thickness. It is noteworthy that, unlike a conventional MIS capacitor, the capacitance does not depend on the thickness of ion gel (dielectric). The capacitance of ion gel/P3HT capacitor depends on P3HT thickness, bias voltage and frequency. Thicker P3HT, higher bias, and lower frequency lead to larger capacitance.

7.2.4 Printed EC Pixel

The conjugated polymers PEDOT:PSS and P3HT are also known to be electrochromic materials with good chemical stability.[15,104,324] PEDOT:PSS is blue in the pristine or semi-oxidized state, and transparent when further oxidized (fully conducting). P3HT has a red-purple color in the neutral state and is a translucent blue when oxidized. This section shows a bi-color printed electrochromic pixel based on the ion gel, P3HT and PEDOT:PSS. The structure is very similar as the capacitor discussed in previous section, except the bottom Au electrode is replaced by a transparent printed metallic CNTs thin film. The PEDOT:PSS layer also serves as the second electrode due to its large conductance (up to 1000 S/cm). The device switches from reddish purple to blue reversibly.

Figure 7.8 illustrates the change of the UV-visible absorption spectra of a stand-alone EC pixel under various voltage biases. The spectra were acquired in ambient air. The EC

Pixel was illuminated with light at fixed wavelengths and the transmitted intensity was measured. The bottom metallic CNT electrode was grounded and the bias voltage was applied on the PEDOT:PSS layer at 1.5 V, 0 V, and −1 V, respectively. At 0 V (purple curve), the spectrum shows two broad absorption peaks of the EC pixel: one at the green wavelength region (around 530 nm), and the other one at the red to infrared region (a broad absorption around 850 nm). The positions of the two peaks are close to the reported absorption spectra of the pristine P3HT and PEDOT:PSS, respectively.[15,325,326] At positive bias, with $[TFSA]^-$ anions diffusing in, the PEDOT:PSS layer was further oxidized compared to the 0 V condition. The absorption of the red wavelength was largely suppressed (pink curve), and PEDOT:PSS turned into transparent state. On the other side of the electrolyte, P3HT was further reduced compared to 0 V. Since the P3HT is slightly p-doped with air exposure, a slightly positive bias brings the P3HT to pristine state (similar as the "OFF state" as in EGTs). As a result, the stronger green absorption (around 530 nm) can be seen comparing to 0 V. The EC pixel appeared to be purple-red at 1.5 V, as shown in the left image in Figure 7.8.

At negative bias, PEDOT:PSS was reduced, and P3HT was oxidized. The EC pixel absorbed more at the red wavelength, and less at green wavelength, hence the EC pixel showed a blue color at −1 V, as shown in the right image of Figure 7.8. The transmitted light intensity is measured and subtracted by the background and normalized to the highest peak. The change of the spectra represents the change in bulk of P3HT and PEDOT:PSS polymer layers, which again illustrated the 3D ion diffusion and is consistent with the discussions in EGT and capacitor section.

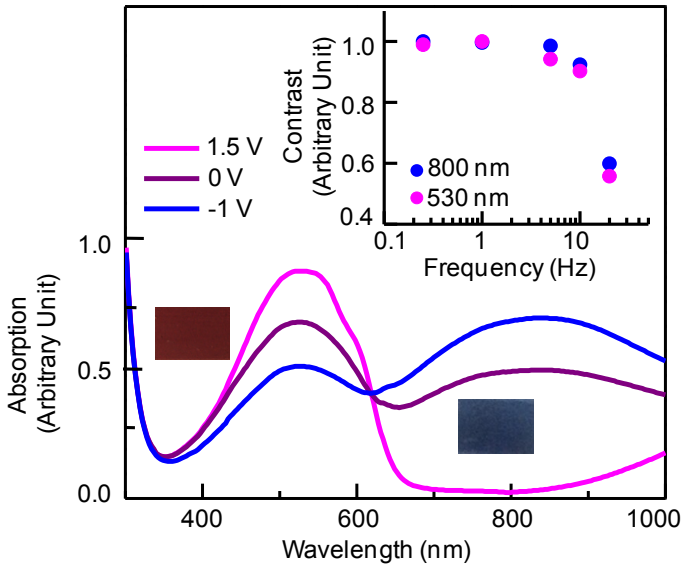

Figure 7.8 Printed EC pixel. UV-vis absorption spectra of printed pixel under various voltage biases is shown. The inset shows the color contrast of the pixel as a function of bias frequency.

The ion gel contains only 20 wt% of triblock copolymers, thus the ion motion is weakly affected by the polymer chains and can potentially enhance the switching speed of the pixel. To measure the dynamic response of the printed EC pixel, the *m*-CNT electrode was grounded, while a square wave signal with controlled frequency was applied to the PEDOT:PSS electrode of the pixel. A laser was set to 530 nm and 800 nm, and the transmitted light intensity was transformed to voltage signal. The voltage modulation on the transmission at 1 Hz is shown in Figure 7.9. Pink curve illustrates the change of the transmission at 530 nm (reflecting the change of P3HT absorption), which reached the maximum at $V = -1.5$ V and minimum at $V = 1.5$ V. The transmission at 800 nm (reflecting the change of PEDOT:PSS absorption), shown in the blue curve, was also modulated by voltage but in the counter direction of P3HT curve. The transmitted signal

followed the modulating voltage signal, indicating the EC pixel can fully switch color at 1 Hz. The unit of transmission was subtracted by the background and normalized to the highest peak. Note here the way the transmission modulated by the bias is in the opposite direction comparing the absorption spectrum in Figure 7.8.

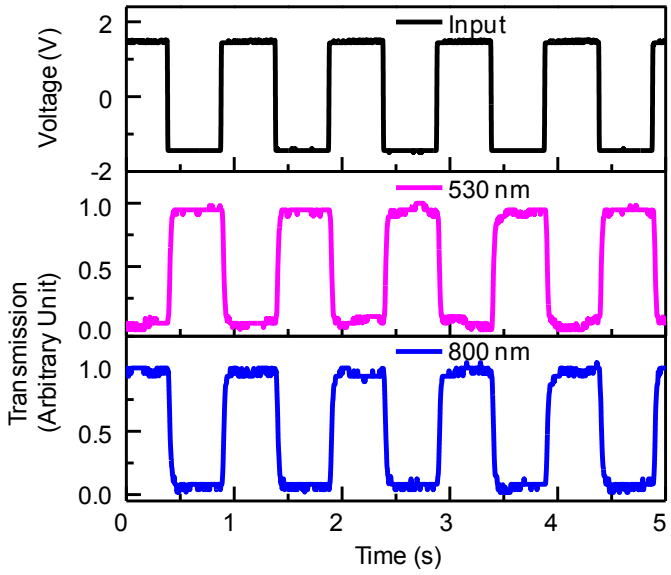

Figure 7.9 Dynamic optical response of the printed EC pixel under 1 Hz bias.

In addition, the color contrast was measured as a function of the bias frequency, shown in the inset of the Figure 7.8a. At each wavelength, the intensity change of the transmitted light was measured at various voltage frequencies (0.25 Hz – 20 Hz), and normalized to the change at 0.25 Hz. The EC pixel remained full contrast up to 5 Hz, and the contrast started to decrease above 10 Hz. When operating at 20 Hz, the pixel remained 60% contrast. Comparing to EGT and capacitors, the EC pixel seems to be "slower". This is because the color contrast is more sensitive to the ion diffusion depth.

Full color contrast requires the electrochromic layer to be completed doped with ions. At higher frequencies, the diffusion depth of ions is limited, thus only part of the film changes color and results in the lower color contrast. On the contrary, ion diffusion in ion gel gated EGT is an enhancement to the current and capacitance, but not a requirement of the functionality. Therefore, those devices can function at a frequency up to kHz. However, there is room for further optimization of switching speed of printed EC pixel, including device architecture, electrochromic film thickness, electrode conductivity, etc.

7.2.5 Printed Resistors and Crossovers

In p-MOS logic circuit, the load resistor controls the output swing and trip point of an inverter. The load resistors in inverter chains are large enough (160 kΩ) to provide enough delay time and reduce the power consumption. Resistors in NAND 1 and 2 are 80 kΩ, and in NAND 3 is 40 kΩ. The pixel driver employs 20 kΩ and 10 kΩ (last stage), respectively. There are two advantages of using this gradient profile of resistance design. First, it gradually regulates the shape of the falling and rising edge of each stage, so that the last stage outputs a high current and square wave to drive the pixel (see discussion in section 7.3). Meanwhile, it minimizes the power of the whole circuit. As demonstrated in the inset of Figure 7.10 a, a strip of PEDOT:PSS is printed between two patterned Au contacts which fixed the length of the resistor. The resistance depends on the thickness and width of the PEDOT:PSS strip, and can be controlled by the printing speed and number of loops. Figure 7.10 a shows the I-V characteristics of a typical resistor in NAND 1 and 2, and the nice linear characteristic indicates ohmic contact between the

printed PEDOT:PSS stripe and Au pads. A crossover, similar to the via in silicon circuitry, connects two wires without shorting to others. As shown in the inset of Figure 7.10 b, a PMMA thin film was printed as a cover for the two vertical Au lines, and a silver line was printed on top connecting the two horizontal Au lines. The crossovers should be much smaller in resistance compared to other elements in the circuit to avoid undesired voltage drops. Therefore, silver was employed due to its high conductance. The resistance of the silver line was ~ 8 Ω, as assessed from the I-V curve shown in Figure 7.10 b.

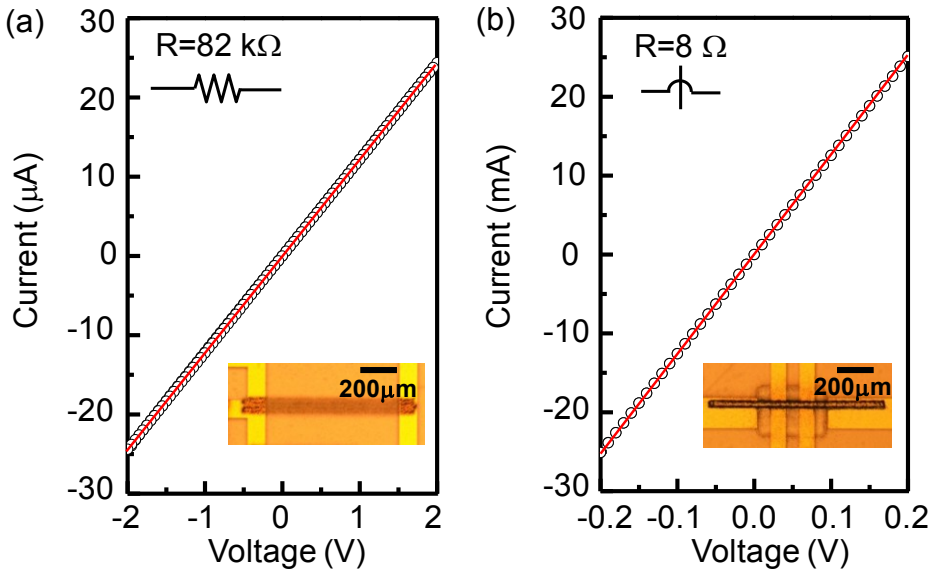

Figure 7.10 I-V characteristics of printed resistor and crossovers. (a) The I-V curve of a printed PEDOT:PSS resistor (red open circle), which serves as a load resistor in the NAND 1 or NAND 2. The resistance estimated from the slope is ~ 82 kΩ. (b) The I-V curve of a printed crossover (red open circle), which resistance is estimated to be 8 Ω based on the slope. Inset shows that a thin film of PMMA is printed on top of two vertical Au lines as an insulator, and a silver line is printed on top of the PMMA connecting the two horizontal lines.

7.3 Printed Circuit Performance

Pulse generator consists of 12 stages of inverters. When signal passing through a stage of inverter, it is flipped and delayed. Figure 7.11 (a) illustrates the function of an inverter, measured in an inverter with a load resistor of 160 kΩ, without the load capacitor, at V_{DD}= −1 V. When input is 0 V, the inverter outputs −1 V, while the input sweeps to −1 V, output is flipped to 0 V.

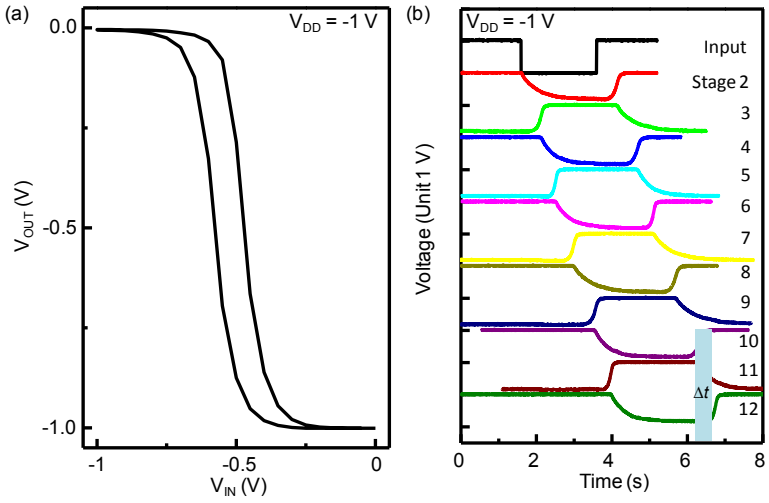

Figure 7.11 Inverter and signal flow in delay chains. (a) The input-output characteristics of a printed ion gel inverter at V_{DD}= −1 V. (b) Voltage signal in inverter chains.

Each stage delays the signal in time due to the *RC* time of the inverter. Figure 7.11 (b) shows the output voltage signal as a function of time from stage 2 to 12, after triggered by the input (black). It can be seen the even stages and odd stages have opposite pulses, also the rising and falling edges of the signals are not symmetric. This is because at the rising edge, the dominant current is the on-state current of the EGT, about mA. While at

the falling edge, the dominant current is from the load resistor (V_{DD}/R_{load}), about 10 μA. The larger current leads to shorter charging time and fast switching edge. Hence the falling edge is always slower than the rising edge in inverter chains.

In typical silicon circuits, the delay time of an inverter is measured from the middle of input rising edge, to the middle of the output falling edge. In this case, the asymmetry edges introduce the inaccuracy in such measurement. Thus the average delay time of the inverter is measured between the two rising edges of consecutive odd stages or even stages. As an example, the time difference (Δt) between stage 10 and stage 12 is shown in shaded area in Figure 7.11 (b). Stage 11 and stage 12 both contribute to Δt, hence $\Delta t = 2 \times t_{delay,}$ where t_{delay} is the average delay time of an inverter.

Another issue raised by the asymmetric rising and falling edges is the total delay time of the odd and even inverter chains are different, although all chains have 3 stage of inverters. Since the falling time is much longer than the rising time, therefore, the major contribution to the total delay time of an inverter chain comes from the falling edges. In even inverter chain, e.g. chain 2, from stage 4 to 6, there are two falling edges and one rising edge, while in odd chain, e.g. chain 3, from stage 7 to 9, there are only one falling edge and two rising edges, as shown in Figure 7.11 (b). This means the total delay time of odd chains are smaller than the even chains.

When all the signals are combined by NAND 3, the differences of the delay time can be seen clearly. Figure 7.12 demonstrates the effect discussed above. NAND 3 outputs two consecutive pulses, and the width of the pulse is not determined by the input, but the

delay time from chain 1 – 4, as illustrated by the dashed lines. Clearly, t_1 and t_3 are shorter comparing to t_2 and t_4. To solve this problem, the capacitors in odd inverter chains are doubled to compensate the difference. An alternative solution could be adding two more stages in odd chains.

NAND 3 employs load resistor of 40 kΩ. The small load resistance decreases the falling time of the output. Therefore, the pink curve shows more symmetric rising and falling edges. The gradient change profile of the load resistors from inverter chains, NANDs, to drivers, regulates the shape of the output signal. At the final stage, the output is modulated as a well defined square wave function as shown in Figure 7.13.

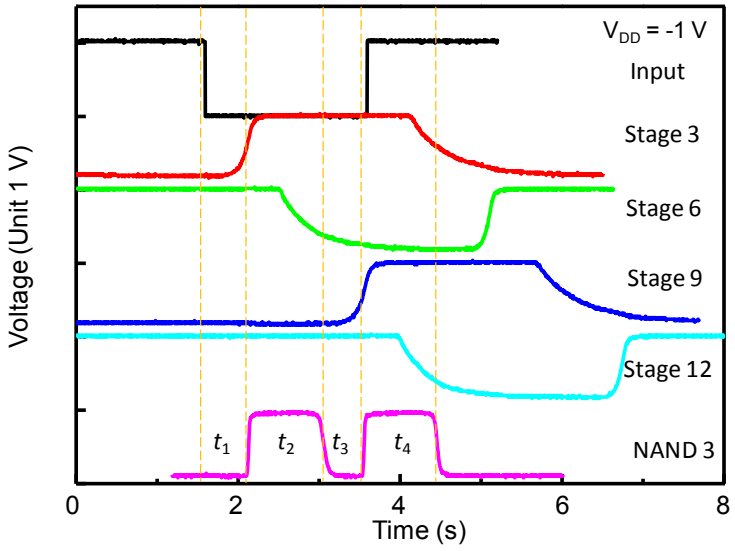

Figure 7.12 Output of NAND 3.

Integrating all the key elements together, an EC pixel driver circuit generating two pulses to switch the pixel color is demonstrated. Since the pixel requires both polarities to switch it, two outputs are designed in opposite waveform, as shown in Figure 7.13. With

an input trigger (black), the outputs showed uniformly shaped square waves with opposite signs, where t_1 to t_4 are the delay times from inverter chains 1 to 4. The evenly distributed outputs demonstrate good control in the printing process as well as the modulation and circuit design.

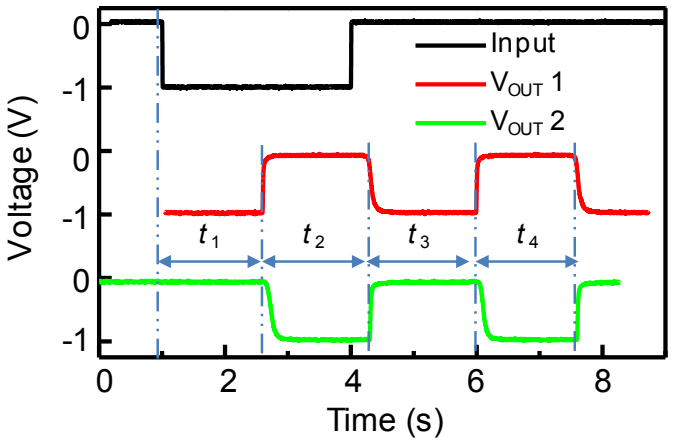

Figure 7.13 The output performance of the printed circuit.

Output 1 and output 2 (as labeled in Figure 7.1 b) are connected to the PEDOT:PSS electrode and *m*-CNT electrode of the pixel, respectively. When V_{OUT} 1= 0 V and V_{OUT} 2 = −1 V, the pixel is effectively under 1 V bias and displays a reddish purple color. With V_{OUT} 1= −1 V and V_{OUT} 2 = 0 V there is an effective bias of −1 V which switches the pixel to blue. The color of the display pixel switched twice upon every input pulse. The drive pulse widths were designed to be 2 s (0.5 Hz), in order to reach the maximized color contrast of the pixel.

Efficient switching of large EC pixels requires very large charge, hence high output current is the key to achieving fast switching and high color contrast. The printed circuit

was tested with EC pixels of different sizes, from 1 mm^2 to 6 mm^2. A magnified view of one pulse is shown in Figure 7.14. The 1 mm^2 and 2 mm^2 pixels had no obvious effects on the output signal, while the 6 mm^2 one slightly slowed down the falling edge of the signal, indicating it takes longer time to switch larger pixel. In essence, the pixel functions the same way as a load capacitor does, i.e., the capacitance and charging time increases proportional to the area. To retain the same performance, the driving current should be proportional to the pixel size. Some simple strategies can be employed in the circuit design if larger size pixels are desired, such as increasing the EGT channel W/L ratio and decreasing the resistance of the load resistors in the driving unit.

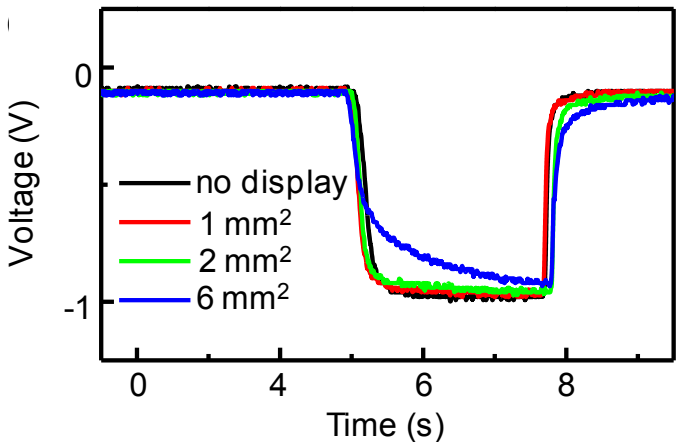

Figure 7.14 Capacity of the driving circuit. Pixel in 1 mm^2 and 2 mm^2 can be driven without affecting the circuit outputs. Pixel in 6 mm^2 deforms the output waveform slightly due to the long charging time.

A good operational stability of the printed circuit was demonstrated. A circuit without a load pixel was tested for 100 minutes in N_2 continuously, with $V_{DD} = -1$ V and an input pulse every 10 s. Output 1 was recorded every 10 minutes, from 0 to 100 min, as shown

in Figure 7.15. The output signal showed excellent stability over 100 min, 600 cycles, with no degradation in amplitude and only minor shift in position.

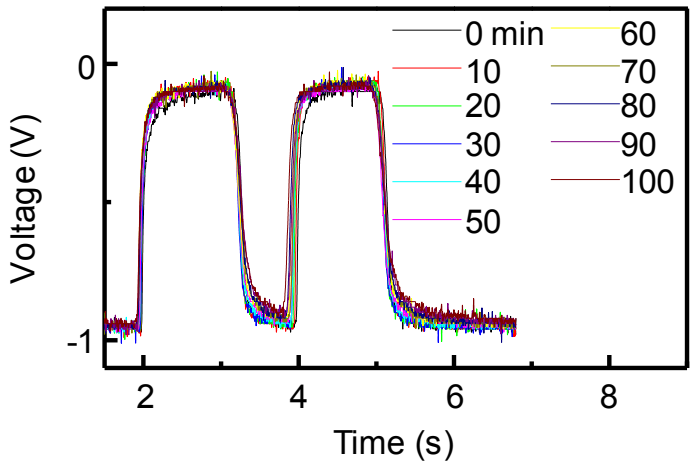

Figure 7.15 Operational stability of printed circuit. V_{OUT} 1 was tested continuously for 100 minutes, 600 cycles continuously, in N_2, showing no degradation in output swing, only slightly shifting in time.

7.4 Conclusions

In summary, all key components of the drive circuitry, namely resistors, capacitors, and transistors, were aerosol jet printed onto a plastic foil; metallic electrodes and interconnects were the only components pre-patterned on the plastic by conventional photolithography. The large milliamp drive currents necessary to switch a 4 mm^2 EC pixel were controlled by printed EGTs that incorporate printable ion gels for the gate insulator layers and P3HT for the semiconductor channels. Upon application of a low voltage input pulse, the circuit switches the printed EC pixel ON (red) and OFF (blue) two times in approximately 4 seconds. The high capacitance ensures the high output

current of EGTs (>1 mA), the high capacitance of ion gel-gated P3HT capacitors (> 100 $\mu F/cm^2$), as well as the fast switching speed of the display pixels (up to 20 Hz). The key elements, EGTs, capacitors and pixels are all based on P3HT, ion gel, and PEDOT:PSS, in similar layered structure and can be fabricated in simple printing process. The good control of printing process and reliable device performance ensure the using of conventional software on circuit design and simulations. The printed circuit drives the display to full contrast at 1 V supply voltage, and showed good stability up to 600 cycles, which demonstrate a great potential of the printed electronics in low voltage, portable applications. This is the most sophisticated circuit reported to date based on EGTs and it also demonstrates that complex materials integration can be achieved with a simple printing process.

Chapter 8 Future Research

Chapter 5-7 summarize the experimental work of electrolyte-gated transistors (EGTs), circuits and their applications in printed circuits. This chapter discusses the remaining challenges and opportunities for future research.

8.1 Power Consumption of Printed Circuits*

When considering the applications in portable electronics, low supply voltage, as what has been discussed extensively in previous chapters, is a key factor in circuit design. In addition to it, low power consumption is also strongly desired. Both low voltage and low power need to be achieved in order for the electronics to be compatible with flexible batteries and light weight applications. In conventional silicon technology, complementary metal-oxide-semiconductor (CMOS) circuits can achieve much lower power consumption compared to n channel (i.e., NMOS) or p channel (i.e., PMOS) only circuits. CMOS consists of both n channel and p channel MOSFETs. At any moment of the steady state, one FET of the pair is in the OFF state, therefore, very little static power is consumed. The power consumption only occurs during the switching status. On the other hand, NMOS (or PMOS) only logic circuits are implemented by FETs and resistors. There is a high static current goes through the resistor even when the transistor is in OFF state, which results in a high static power consumption. Besides the lower power, CMOS

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also offers higher density of logic functions and higher noise margin. Hence, CMOS circuit is the most used circuit in VLSI (very-large-scale integration) chips.

In printed circuitry, complementary circuit remains challenging. A major challenge is the material and processing of n type semiconductors. Organic n type materials are rare and usually sensitive to oxygen and water.[328] These make the high performance n channel transistors very difficult to fabricate. Intensive studies are trying to understand the reasons behind the differences of p type and n type organic semiconductors, the design rules of the high performance, stable n type semiconductors, the synthesis and fabrication of materials and devices.[274,277,309,329] However, this is still an area needed a breakthrough.

As what have been demonstrated in previous chapters, semiconducting CNT is a great candidate of fast, low voltage, printable circuits, however, it is worth noting that the power consumption in this type of circuits may not be an advantage. Using ambipolar transistors, the printed CNT circuit has unique characteristics. Unlike the PMOS or NMOS circuits, the ambipolar circuit has no resistor which leads to a fixed static current. However, the ambipolar circuit also cannot achieve the power consumption as low as CMOS circuit, since the transistor may not be turned OFF due to its nature.

The modeling of the power consumption of CNT ring oscillators is collaborated with Prof. Chris. H. Kim group. The ambipolar CNT EGT is modeled as an NMOS and a PMOS transistor connected in parallel, with the same channel length (50 μm) and width (500 μm). The Hspice Level 3 silicon empirical model was used, and the model parameters were adjusted to fit the data. From Figure 8.1, it can be seen that the model

fits the experimental I_D-V_G data well. The mobilities of the NMOS and PMOS transistors are set to be 20 and 80 cm^2/Vs, and the threshold voltages are set at 0.72 and -0.3 V, respectively. With this compact model, the inverter behavior was verified through simulation, and optimization of inverter design is possible.

Figure 8.1 c and d demonstrate that the model can be employed to understand the switching mechanism of ambipolar CNT inverters. The current of the inverter shows a minimum around the transition point, which means the ambipolar inverter operates differently than a conventional CMOS inverter in which current is peaked at the transition voltage. Figure 8.1 d shows the currents of the n- and p- channels in our model, as a function of V_{IN}. With V_{IN} close to V_{DD} (1.5 V), the current from the n-channel of EGT a (blue straight line) is higher than that of the p-channel (red straight line), indicating EGT a works in the n-type regime. For the same reason (dashed lines), EGT b also works as n-type. Similarly, when V_{IN} is close to ground (0 V), both transistors a and b will work in p-type mode. A key point is that the bias conditions for the two EGTs are different; therefore, the functionality of the inverter can be realized. However, only within a small voltage regime around the transition point ($V_{IN} \sim 1$ V) does the ambipolar inverter work similarly to a classic complementary inverter, where EGT a is p-type and EGT b is n-type.

Since the two transistors are both in the ON state, the static power dissipation in ambipolar inverters is expected to be higher than in CMOS circuits. It can be estimated, $P_{static} = IV_{DD}$ as the average of power consumed at V_{IN} = 1.5 V and 0 V. The currents at

1.5 V and 0 V are 0.2 mA and 2 mA (not shown), respectively, with V_{DD} = 1.5 V. Therefore, average P_{static} is about 1.6 mW.

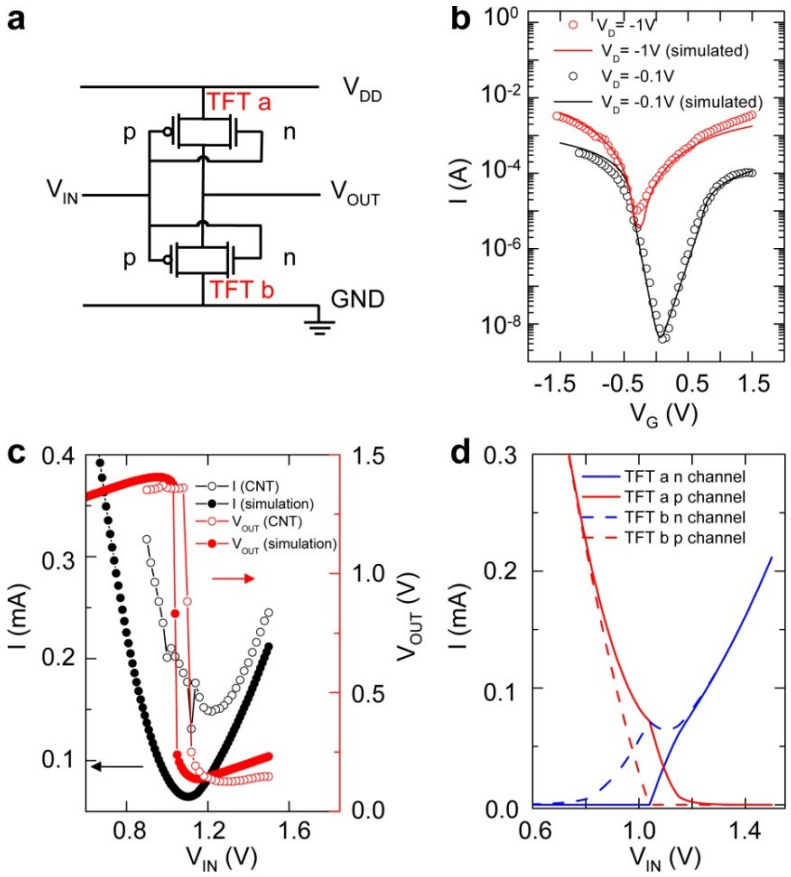

Figure 8.1 The simulations of the ambipolar CNT EGTs and inverters. (a), The equivalent circuit which is used to simulate the CNT inverters. Each CNT EGT is modeled as a p- and an n-channel in parallel. (b), The transfer curves of the simulated and experimental ambipolar CNT EGT. Open circles show the experimental results, with V_D= –0.1 V (black) and -1 V (red); straight lines show the simulated curves, with V_D= –0.1 V (black) and -1 V (red). (c), The drain currents of a printed CNT inverter from experiments (black open circles) and simulation (black solid circles), and the output voltage characteristics from experiments (red open circles) and simulation (red solid circles), respectively. V_{DD}=1.5 V. (d), Simulated currents of the p channel of EGT a (red straight line), n channel of EGT a (blue straight line), p channel of EGT b (red dashed line), and n channel of EGT b (blue dashed line).

The dynamic power dissipation per stage of the CNT ring oscillator can be estimated as $P_{dynamic} = CV_{DD}^2 f$ = 50 μW, where C is the total capacitance calculated below (Figure 5.10) as 4 nF, V_{DD} is 2.5V and f is 1.9 kHz, as shown in Figure 5.8c. Note that for the ambipolar CNT ring oscillator $P_{dynamic} < P_{static}$, which is the opposite of the situation for conventional complementary ring oscillators.

Based on above analysis, it is clear why ambipolar circuit may have high power consumptions. However, semiconducting CNT still has incredible merits of printable electronics, such as the very high mobility, chemistry stability and the compatibility to air processing. Here, a few strategies are proposed for the further improvements in considerations of power consumptions.

8.1.1 Modification of the Electrolyte Material.

The ion gel electrolyte employed in this thesis is based on ionic liquids which have high ionic conductivities for both cations and anions. Berggren's group demonstrated polyelectrolyte materials consists of cations and anions with different sizes, where only smaller ions are mobile. By selecting appropriate polyelectrolyte, the printed CNT transistor may behave as n-type transistor if only cations in the polyelectrolyte are mobile, or p-type if anions are mobile. A true CMOS circuit can be achieved by implementing two kinds of electrolyte into the circuits, without any changes to the semiconducting material. Hence, both the high performance of circuit and low power are possible.

8.1.2 Modification of Semiconducting CNTs.

Although the semiconducting CNTs are intrinsic ambipolar, the band gap of the CNTs are actually tunable, thus the characteristics of p-type and n-type transport. As introduced in Chapter 3, the band gap of CNTs is inversely related to the nanotube diameters (Figure 3.4). Smaller diameters lead to higher energy gap, which means the difference between electron and hole transport energy levels is larger. In other words, the threshold voltages for electrons and holes move further apart, as in Figure 8.2. With smaller diameter (black curve), the ON and OFF current of the transistor remains the same as larger diameter nanotubes (red curve), but the OFF regime is wider. This may help to reduce the static current in ambipolar circuits. This strategy is relatively easy since the selection based on nanotubes diameter is possible as discussed in Chapter 3.

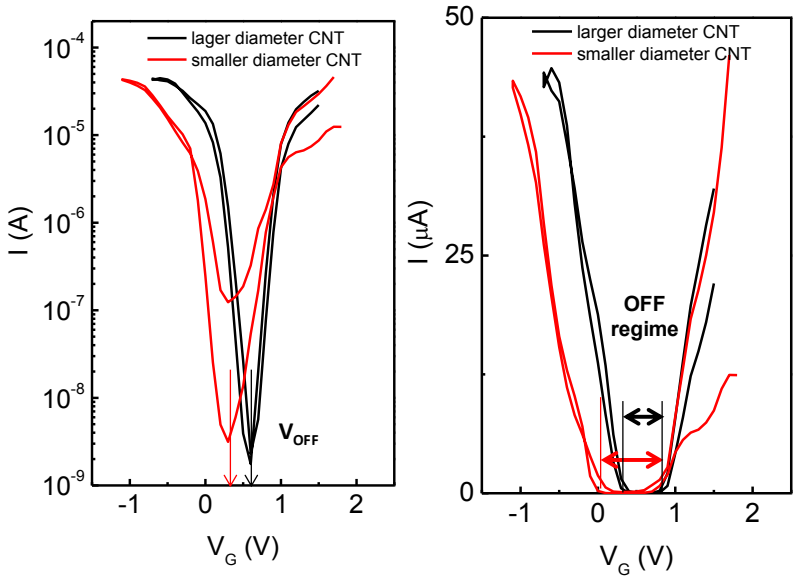

Figure 8.2 Transfer characteristics of transistors based on CNTs with different diameters. Left panel is in semi-log scale, and right panel in linear scale.

Other options remains open, including doping the intrinsic semiconducting CNTs to be p-type and n-type, making more sophisticate circuit design to compensate the undesired static current, etc., but they may lead to topics beyond optimizing the device architecture and will not be discussed in details.

8.2 Capacitor with Large Capacitance and Its Applications

Ion gel provides large surface capacitances because of the formation of the electric double layer. As discussed in previous chapters and in literatures, ion gel gated transistors (based on CNTs, organic crystals, polymers, etc.) were demonstrated with low voltage, enhanced mobilities or ON/OFF ratios, thanks to the high sheet capacitance. In fact, the capacitance itself may lead to interesting researches and applications.

Chapter 7 shows the ion gel capacitors can be integrated into the driving circuit of the electrochromic pixel. Besides the application in logic circuits, large capacitor is also attractive in areas such as batteries and storage. Collaborating with Prof. Kim, we have demonstrated a dynamic random-access memory (DRAM) array based on printed ion gel-gated transistors, which is briefly described as following.[12]

The individual DRAM cell consists of three printed ion gel-gated transistors. The circuit diagram is shown in Figure 8.3 (a). Although there is only single type of transistors in this type of circuit, which is commonly referred as gain cells, the static current can be ignored. The major challenge of the gain cells is the "retention time" (the duration of information can be stored without refreshing) is typically low, e.g., ~ 100 μs in modern silicon technology. In this design, an ion gel-gated transistor is used as the

"storage" EGT, and other two are "write" and "read" EGT, respectively. The information, i.e., charges carriers, can be stored because of the capacitance of the "storage" EGT. Since the static current is low, and the capacitance of ion gel-gated transistor is very large, the information can be sustained for a long duration of time. As illustrated in (c), in a 8x8 DRAM array, majority of the cells can achieve the retention time longer than 60s, which is a large improvement comparing to conventional silicon DRAM.

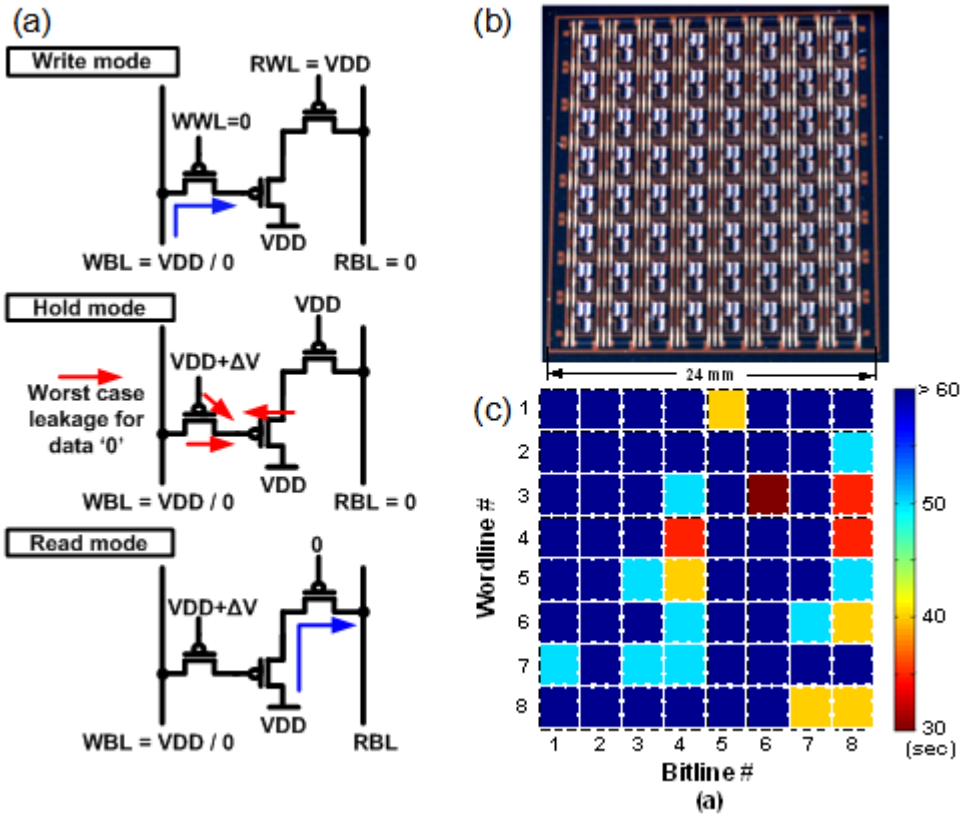

Figure 8.3 A 8x8 DRAM array based on printed ion gel-gated transistors.[12]

With 1.3 V driving voltage, 100% cells can achieve > 60 seconds retention time. The DRAM cells can respond to 20 ms writing time, and showed robust read and write with a

supply voltage down to 0.8 V. In addition, the static power consumption of this circuit is only about 10 nW, which is orders of magnitude lower than the organic SRAM.

Both the capacitors in the pixel driving circuit and DRAM rely on the large capacitance ion gel offers. As discussed in chapter 7, the presence of the polymer layer, e.g., P3HT and PEDOT:PSS, can significantly enhance the capacitance, due to the ion diffusion. Therefore, engineering of the device architecture based on this diffusion should easily lead to a further boost of the capacitance. For example, making the polymer layer more porous can result in larger surface area and help the ion diffusion. Such methods have been studied in other areas such as the heterojunction photovoltaic devices, or nanostructure design in lithium batteries, etc.

The chemical stability of such devices may need to investigate. Electrochemical doping devices are often observed with degradation due to repeating oxidation and reduction. Appropriate selection of materials may minimize the issues.

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