Power Electronic Transformers for AC-AC and AC-DC Conversion with Reduced Number of Switches

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Gysler Fatima Castelino

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Dedication

To my family near and far, my friends and my teachers.

Abstract

Power Electronic Transformers (PETs) operating at frequencies well above the grid frequency have advantages of reduced size and weight as compared to their grid frequency counterparts. They have been proposed for future distribution systems as well as for use in adjustable speed drives where space and weight are at a premium. Power Electronic Transformers are especially attractive to the Navy in power converters for propulsion, radar, lighting and other needs in submarines and ships where the size, cost and weight of power electronic converters needs to be low. Furthermore, these high power density converters have been proposed for harnessing wind energy, especially offshore wind resources.

In this research, a novel reduced-switch Power Electronic Transformer is proposed for three-phase power conversion (three-phase AC to AC as well as three-phase AC to DC). The goal of this project is to reduce the weight and size of the power converter by replacing the low-frequency transformers with high-frequency transformers (HFTs). The novelty of these proposed topologies is that they have only two controlled switches on the primary side of the high-frequency transformers. Additionally, these switches operate at 50% duty ratio, hence they are easy to control. Pulse Width Modulation (PWM) control is only necessary in the converters on the secondary side of the HFT. The modulation strategies proposed in this work achieve nearly Zero Current Switching (ZCS) for these two primary switches.

In the proposed three-phase AC to AC Power Electronic Transformer, a Matrix Converter (MC) is employed on the secondary side of the transformer. Matrix converter with nine four-quadrant switches is a 'more-silicon' and nearly capacitor-less solution for AC to AC conversion. This single-stage AC-AC converter without any electrolytic capacitors translates to higher reliability and efficiency. High-frequency transformers have finite leakage inductance, hence, any switching in the primary or secondary of the transformer requires commutation of the transformer inductive currents. This problem of leakage energy commutation and the required protection are studied in detail in this thesis. Other features of this converter are bi-directional power flow and power factor correction.

The second Power Electronic Transformer is proposed for three-phase AC to DC power conversion. This converter operates on the Dual Active Bridge (DAB) principle wherein the transformer leakage inductance is used for power transfer. Hence, this converter does not suffer from problems associated with leakage energy commutation and additional snubber circuits are not required for this converter. The proposed modulation provides the advantages of unity power factor on the AC side, galvanic isolation and bi-directional power flow capability.

Both these PETs have been analyzed and simulated. Laboratory prototypes have been built and tested to verify the advantages of the proposed PETs.

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Chapter 1

Introduction

Power transformers are building-blocks of our power grid. They are indispensable because they provide voltage transformation that enables power transmission and galvanic isolation for protection. However, these power transformers suffer from some potential limitations: 1) heavy weight because of the size of magnetics 2) use of mineral oils that are not environmentally friendly and 3) sensitivity to harmonics [2]. The size of a transformer depends on its operating frequency, saturation flux density of the core material and the thermal considerations of the core and winding. Operating a transformer at frequencies above the grid frequency has been shown to have advantages of lower weight and higher power density. The use of magnetic materials such as FINEMET with high saturation flux density further reduces the size and weight of High-frequency Transformers (HFTs) [3].

With the help of power electronics, bulky line frequency (50Hz, 60Hz) transformers can be replaced with compact high-frequency transformers. This concept of Power Electronic Transformer (PET) was first introduced by McMurray in 1968 [1]. It has been explored by many researchers and is also called Solid-State Transformer (SST) [4] and Intelligent Universal Transformer. The key properties of PETs are high-frequency isolation along with voltage transformation, voltage regulation, bi-directional power flow capability and in some PETs, reactive power control can be achieved. The definition of PETs has extended to AC to DC conversion as well. The classification of Power Electronic Transformers (PET) is given in Fig. 1.1.

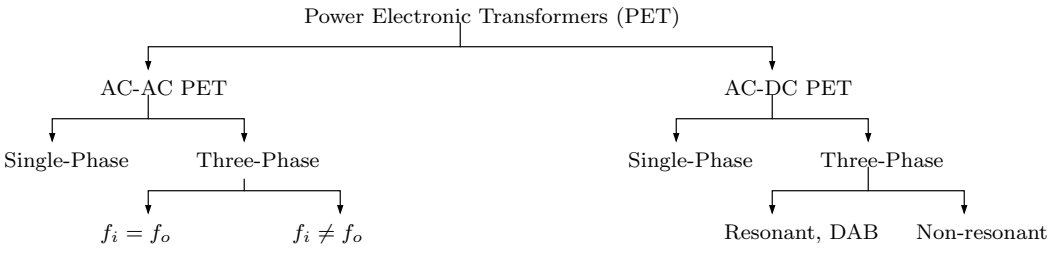


Figure 1.1: Classification of Power Electronic Transformers

PETs require a large number of power semiconductor devices. However, rapid advances in power electronic device technology have made available devices that have high voltage and current ratings with good switching characteristics as well as the ability to perform better at high temperatures [5]. This has played an important role in renewing interest in PETs.

In this chapter, an application of PETs for wind energy and for Plug-in Hybrid Vehicles is described followed by a summary of the state-of-the-art PETs for three-phase AC-AC and AC-DC power conversion.

1.1 Example applications for PETs

Distributed generation in the form of renewable energy resources has increased many-fold in the past decade and it is predicted to increase even more in the years to come. Power electronics provide the enabling technology to connect these variable distributed resources to the power grid that operates at a constant frequency (50Hz, 60Hz). The variability of renewable resources make storage an important element of the modern power grid. Storage can be achieved using batteries, fuel cells, flywheels and recently even plug-in hybrid electric vehicles have been suggested for energy storage. Here as well, PETs can provide an interface with bi-directional power flow capabilities for charging and discharging storage elements.

1.1.1 Power Electronic Transformers for harnessing wind energy

PETs are especially attractive in wind energy generation systems [6]. In conventional on-shore wind turbines, the low-frequency (60Hz) transformers are situated at the base

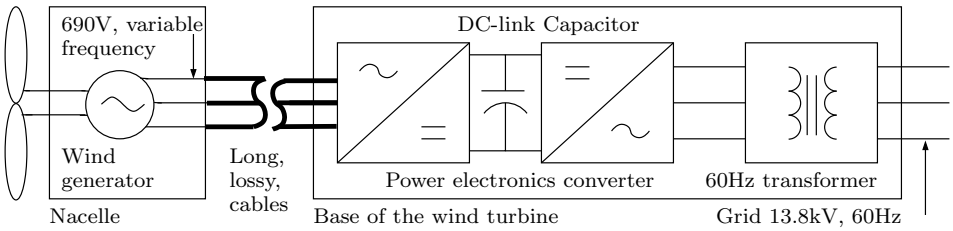


Figure 1.2: Conventional wind turbine systems

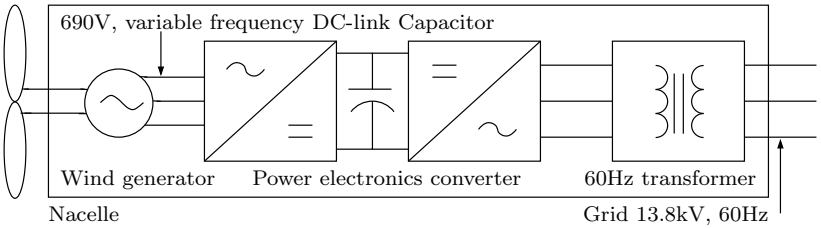


Figure 1.3: Wind turbine systems with low-frequency transformer in the nacelle

of the turbine as shown in Fig. 1.2. Bulky cables carry high currents (kilo-amperes) from the nacelle to the foot of the tower, these cables are costly and also result in high conduction losses. The low-frequency transformers weigh approximately 7-10 tons (2MW, 60Hz). Recently, in off-shore wind turbines, the bulky low-frequency transformers are situated in the nacelle itself as shown in Fig. 1.3 (Vestas V90), this leads to increased cost of infrastructure. These low-frequency transformers can be replaced by high-frequency transformers with the help of power electronics as shown in Fig. 1.4. This would translate to a reduction not only in the cost of infrastructure and copper but also power loss.

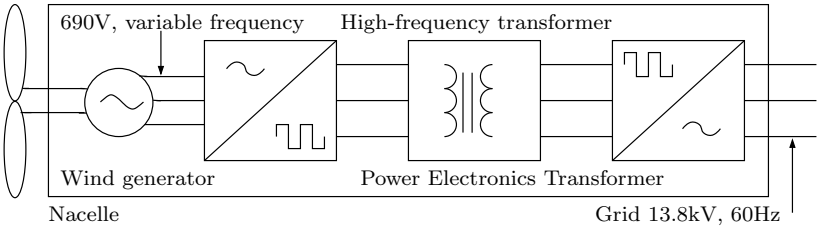


Figure 1.4: Proposed Power Electronic Transformer for wind turbine

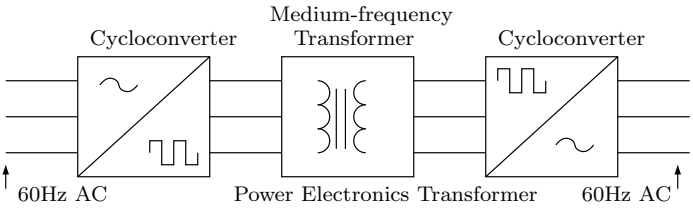


Figure 1.5: First Power Electronic Transformer [1]

1.1.2 Power Electronic Transformers in PHEVs

Rising gasoline prices and a growing concern about pollution due to the use of fossil fuels have led to the development of Hybrid Vehicles, Electric Vehicles and Plug-in Hybrid Electric Vehicles (PHEVs). PHEVs have the ability to charge the on-board battery pack from the grid or an external power source. Vehicle-to-grid (V2G) is a key storage technology proposed for PHEVs wherein a bi-directional AC-DC converter can be used to provide charging and discharging functionality between the battery and the grid [7]. A PHEV with V2G capability can be charged during off-peak hours at night when the grid is under utilized. It can then be connected to the grid as a distributed resource to provide storage that can be used as standby power for a home, spinning reserves for the grid or for peak load shaving [8–10].

1.2 Three-phase AC-AC Power Electronic Transformers

AC-AC PETs that have either medium frequency transformers or high-frequency transformers are divided into two groups, depending on the input and output frequency, f_i and f_o respectively. The first group has applications in replacing distribution transformers with power electronic transformers where the input and output voltages are at the same frequency [2]. The advantages of doing this are in reducing the size of the transformer, while at the same time obtaining voltage regulation, power flow control, fault current limitation and other features [11–13]. The PET proposed by [1] is shown in Fig. 1.5. In this single-stage power converter, the input voltage is chopped to high frequency using a primary side static converter and a secondary side converter is then used to convert these high frequency voltages to variable magnitude output voltages.

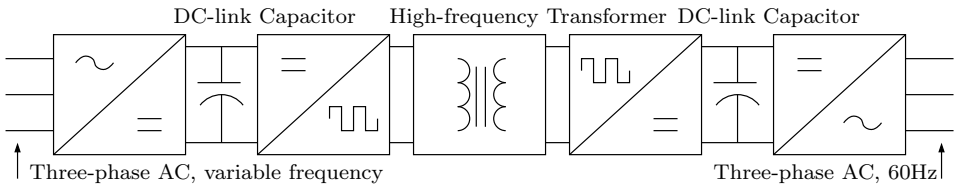


Figure 1.6: Multi-stage Power Electronic Transformer

Voltage regulation is achieved by introducing a phase shift between the input and output converter pulses. Other single-stage Power Electronic Transformers (PETs) have been proposed as distribution transformers in [4, 11, 14–18]. As the switches have finite turn-on and off times, during any switching transition, the current flowing through the inductive leakage inductance of the transformer requires a path to flow. Hence, this converter requires no storage except during switching intervals when the leakage energy of the transformer flows through a protective clamp circuit.

The second group of PETs are proposed for variable frequency drive applications. PETs used as adjustable speed drives make efficient systems because of their inherent regenerative capabilities [19]. These converters are highly suitable for applications in ships, submarines and aircrafts. Such PETs may also find applications in the micro-grids where power flow can be controlled even with a frequency disturbance in the micro-grid [20].

The primary switches in [1] are required to block the entire primary voltage and the secondary switches are required to be rated for the secondary side load currents. This will increase the switch stress as well as cost of the power electronic devices. Hence, multi-level multi-stage PETs have been proposed in [21–26]. Typically, the first stage provides power factor correction and rectification. The following DC-DC converter stage provides high frequency isolation and voltage transformation. The last stage converts the DC voltage to low frequency AC. One drawback is that these converters use DC-link capacitors that are unreliable under thermal stress and hence reduce the overall reliability of the system. Besides, advances in high voltage/high current power electronic devices such as SiC with good switching characteristics, low conduction loss and ability to perform at high temperatures have refocused the interest in single stage power conversion for variable frequency AC-AC converters [5].

Matrix Converters (MC) are a more silicon solution to direct AC-AC conversion. Matrix converters have inherent properties of 1) bi-directional power flow 2) variable frequency and voltage generation 3) active and reactive power control 4) single-stage power conversion. These properties make matrix converters suitable for application in PETs. PETs based on direct modulation [27–29] and indirect modulation [30–32] of matrix converters have been proposed. However, they have a number of switches on the high-voltage side. State-of the art MC based PETs are discussed in Chapter 2.

A High Frequency Transformer (HFT) linked three-phase AC-AC system with only two switches on the high-voltage side was proposed in [6,33–37]. This topology combines the advantages of both matrix converters as well as high frequency transformers. The advantages of this converter are 1) single-stage power conversion, 2) galvanic isolation, 3) power factor control 4) 0.5 modulation index with least number of switching transitions and ZCS for the primary switches. This configuration will be the focus of the first half of this thesis.

1.3 Three-phase AC-DC Power Electronic Transformer

Single-stage isolated AC-DC converters that use cycloconverters are proposed in [38–40]. They have bi-directional power flow capabilities making them suitable for motor drive application for regenerative braking and battery charging/discharging in PHEVs. Protective clamp circuits will be required for these converters because they have finite transformer leakage inductance. This leakage energy commutation limits the switching frequency of these converters [38]. The switching frequency is also limited by the device stress, and switching losses. Converters having soft-switching characteristics, [11, 41–43](multistage) and [44–48](single-stage) are being explored so that they can be operated at higher frequency consequently reducing the size of the transformer and filter.

AC-DC converters with bi-directional capabilities have been proposed in applications for battery charging/discharging in plug-in hybrid vehicles [48], propulsion systems, UPS systems [49], DC grid in ships [50] just to name a few. Bi-directional power transfer between two AC voltages connected by an inductor can be achieved by introducing a phase shift between the two voltages. In Dual Active Bridge (DAB) converters, this phase shift is introduced at high-frequency. This is done either in the DC-DC converter

stage or in single-stage AC-DC converters. An advantage being, the transformer leakage inductance is used for power transfer and clamp circuits are no longer required for commutation of the transformer leakage inductance currents. Additionally, these converters have soft-switching characteristics under certain operating conditions [51, 52]. More details on DAB based power converters is covered in Chapter 4. A discussion of current state-of-the-art soft-switched three-phase AC-DC PETs is given in Chapter 5.

In the second half of this thesis, a single-phase and three-phase bi-directional, HFT isolated, single-stage, DAB-based, AC-DC converter are analyzed. These converters have only two controlled switches on the AC-side. The transformers provide isolation and their leakage inductance is used for power transfer. This topology combines all the advantages of a HFT based system and a DAB-based system. Ideally, no clamp circuit is required for this converter.

1.4 Contributions of this thesis

The two main contributions of this thesis are analysis, design and implementation of laboratory prototypes of 1) a novel AC-AC Matrix converter based PET 2) a novel single-phase and three-phase AC-DC PET based on DAB principle. Both these converters employ high-frequency transformers in push-pull configuration. They have the same primary circuit with the purpose of converting three-phase line voltages to high-frequency AC voltages. The secondary side converter transforms these high-frequency voltages to either to three-phase variable magnitude and frequency AC voltages or DC voltage. These converters have features of single-stage power conversion, bi-directional power flow capabilities and power factor correction.

The problems associated with the finite transformer leakage inductance of the AC-AC PET have been thoroughly studied. A modulation strategy is proposed that eliminates the primary clamp circuitry for the primary side converter. The single-phase and three-phase AC-DC converters proposed in this research use the transformer leakage inductance to enable power transfer, hence they do not suffer from the drawbacks of increased loss and voltage distortions associated with clamp circuits.

1.5 Organization of this thesis

This thesis is organized into four main chapters, the first two focus on a PET for AC-AC conversion and the next two on PET for AC-DC conversion. A brief description of each chapter is given below.

- Chapter 1 introduces the goals pursued in this thesis.
- Chapter 2 introduces a PET with reduced number of switches for AC-AC power conversion. This chapter presents an analysis of the protective snubber circuits (clamp circuits) requirements on the primary side. A new modulation technique is proposed in order to reduce the protection requirements in the source side. This topology with the proposed modulation technique is analyzed and simulated. The experimental results of this converter are presented.
- Chapter 3 provides a detailed analysis of the power loss incurred in the clamp circuit along with a method to design the clamp components. The entire circuit is simulated along with non-ideal leakage inductance and the presented simulation results are compared with the analytical predictions. The effects of dead-time commutation and four-step commutation are compared in this chapter. The experimental results are presented.
- Chapter 4 proposes a control method for a single-phase AC-DC PET based on Dual Active Bridge principle. The converter is thoroughly analyzed by first assuming it to be a DC-DC converter in a push-pull topology and then extending the results to analyze an AC-DC converter. The conclusions of the analysis are confirmed by simulations. The experimental results for this converter are presented.
- Chapter 5 proposes a modulation technique based on the Dual Active Bridge principle for a single-stage three-phase AC-DC PET with only two active switches on the AC-side. This converter is analyzed in detail. The experimental results are presented.
- Chapter 6 summarizes and concludes the thesis.

Chapter 2

AC-AC Power Electronic Transformer: Topology and Modulation

2.1 Introduction

Matrix converter based three-phase AC-AC power electronic converters have inherent bi-directional energy flow capability, power factor correction and single stage power conversion without any storage elements (capacitors and inductors are required only for filtering and protection). High-frequency transformers (HFT) provide galvanic isolation along with voltage transformation. A major advantage being their small size as compared to line frequency transformers. HFT linked matrix converter based three-phase AC-AC systems, combine the advantages of the matrix converter and the HFT [53]. A summary of the state-of-the-art matrix converter based Power Electronic Transformers is given in this introduction.

A PET based on indirect modulation of the matrix converter proposed by [30] uses two three-phase to single-phase matrix converters linked by a high-frequency transformer. Hence, this topology has 12 switches on the high-voltage side. A PET that uses a three winding transformer instead of the two winding transformer of [30] is proposed in [31]. The operating principle for the primary converter is the same as that of [30],

however, due to availability of three levels on the secondary side, common-mode voltage elimination can be achieved in this converter. Another PET, based on indirect modulation of matrix converter that has four wire outputs that is better suited for operation under unbalanced operation is proposed in [32]. A PET based on direct modulation of MC is presented in [27]. It uses two MC on the primary side, has a voltage transformation ratio of up to $1.5 \times \sqrt{3}/2$ and has zero common-mode voltages in the output voltages. However, it has 36 switches on the high voltage side and $18 \times 3 = 54$ switches in all.

The High-frequency transformer (HFT) link in PETs have finite leakage inductance, hence any change in the switching state of the input or output side converter of the PET needs commutation of leakage energy. Commutation of leakage energy using clamp circuits leads to power loss, voltage distortion and requires higher voltage blocking capabilities for the devices in the converter [54]. Some of the problems associated with the commutation of leakage energy can be solved by source-based commutation [29]. Source based commutation is a technique where the primary switches are modulated in a smart way such that the the input voltages instead of clamp circuits are used for commutation purposes. A topology that uses lossless source based commutation technique is proposed in [28]. It uses two matrix converters on the primary side and six bi-directional switches on the secondary side. Another variation of [30] has been proposed in which source based commutation is possible [55]. Although source based commutation is lossless, these PETs have many switches on the high-voltage side and they use very precise and complicated switching strategies.

The High-Frequency Transformer linked AC-AC system shown in Fig. 2.1 with only two switches on the high-voltage (primary) side was proposed and analyzed in [6,33–37]. Source based commutation is not possible in this topology, hence, a clamp or a snubber circuit is used on both sides of the transformer for safe commutation of leakage currents.

This chapter presents a comprehensive analysis of the primary (input) clamp circuit of the proposed PET in Fig. 2.1 and the resulting limitations. A modulation strategy for the secondary (output) side matrix converter has been proposed in order to obviate the need for an input clamp circuit. The advantages of the PET and the proposed modulation strategy are 1) single-stage power conversion, 2) galvanic isolation, 3) power factor control 4) 0.5 modulation index with least number of switching transitions and

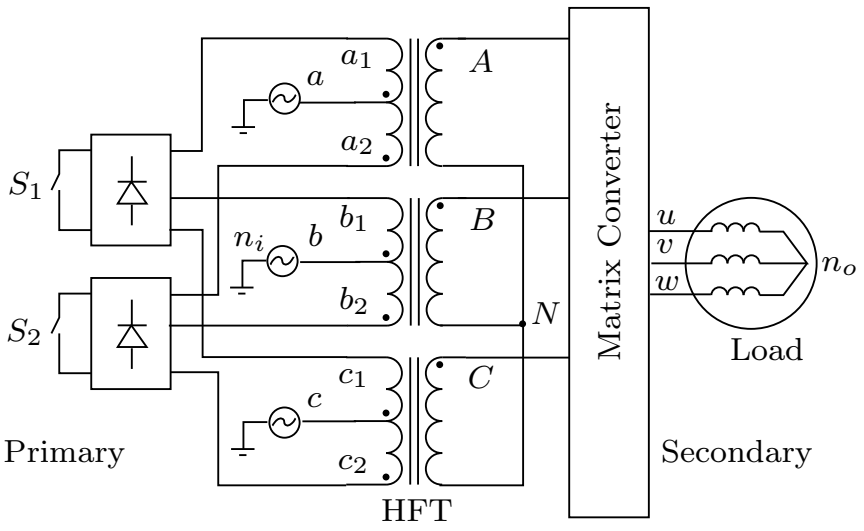


Figure 2.1: Proposed AC-AC PET topology

Zero Current Switching (ZCS) for the primary switches. Experimental results on a laboratory prototype confirm the advantages of the proposed modulation strategy.

2.2 PET topology and modulation strategy

In this topology, the input three-phase balanced AC voltages are applied to a bank of three single-phase transformers as shown in Fig. 2.1. S_1 and S_2 on the primary side are switched in a complimentary fashion with 50% duty cycle. When switch S_1 is on, terminals a_1, b_1 and c_1 are shorted and the upper half of the primary windings conduct. Similarly, when S_2 is on, terminals a_2, b_2 and c_2 are shorted and power is transferred through the lower halves of the primary windings. The voltage across each secondary winding is a chopped version of the corresponding input line to neutral voltage. In the secondary side of the transformers, a matrix converter is employed in order to generate adjustable magnitude and frequency AC waveforms. The Matrix converter is modulated using rotating vectors as described in [33] and [6] to obtain a modulation index of upto 0.5 and 0.866 respectively. During each switching transition of S_1 and S_2 (T_1 and T_2 as shown in Fig. 2.2), power flow is transferred from one half of the primary windings to the other. Due to the presence of leakage inductances L_1 and L_2 (Fig. 2.3) in the

primary windings of the transformer, this transition is not instantaneous, and a snubber or clamp circuit is required for the commutation of the primary leakage energy. In Fig. 2.3, diodes d_{11}, d_{22} and the clamp capacitor C_l form the required clamp circuit. As both the transitions (T_1 and T_2) of S_1 and S_2 are symmetrical, here, a detailed analysis of T_1 is presented. During T_1 and T_2, the output matrix converter is not switched. The secondary side matrix converter with three-phase balanced load can be modeled as three-phase balanced current sources ($i_A = I_A$, $i_B = I_B$ and $i_C = I_C$). Without any loss of generality, it is assumed that I_A is positive, while I_B and I_C are negative. Just before T_1, the currents i_{a_1}, i_{b_1} and i_{c_1} are equal to I_A, I_B and I_C respectively and i_{a_2}, i_{b_2} and i_{c_2} are all zero. The diodes, d_{a_1}, d_{b_2} and d_{c_2} are conducting to provide a path for these currents to flow through S_1. At T_1, when S_1 is switched off, the currents i_{a_1}, i_{b_1} and i_{c_1} cannot change instantaneously, this forces diode d_{11} to come into conduction and current starts flowing through the capacitor C_l. In order to simplify the analysis, it is assumed that the two halves of the primary winding and the secondary winding have equal number of turns and L_1=L_2=L. Neglecting the magnetizing current, application of Amperes' law results in (2.1). In Fig. 2.3, two conducting loops can be traced involving upper halves of the primary windings. The KVL equations for these two loops are given by (2.2) and (2.3). By (2.1), if i_{a_1} reduces, the diode d'_{a_2} will turn on and the lower winding of phase-a will start conducting. Similarly, for a desired change in currents i_{b_1} and i_{c_1}, diodes, d'_{b_1} and d'_{c_1} will start conducting. Switch S_2 provides a path for these currents to flow. The KVL equations for the two conducting loops with the lower halves of the primary windings are give by (2.4) and (2.5). In a balanced three-phase system, with a floating neutral point, the three line to neutral values must sum to zero hence we obtain (2.6).

$$\begin{aligned} i_{a_1} - i_{a_2} - i_A &= 0 \\ i_{b_1} - i_{b_2} - i_B &= 0 \\ i_{c_1} - i_{c_2} - i_C &= 0 \end{aligned} \tag{2.1}$$

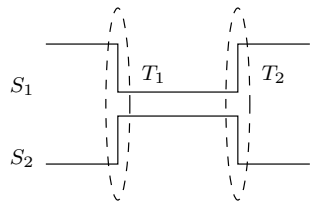


Figure 2.2: Switching pulses for S_1 and S_2

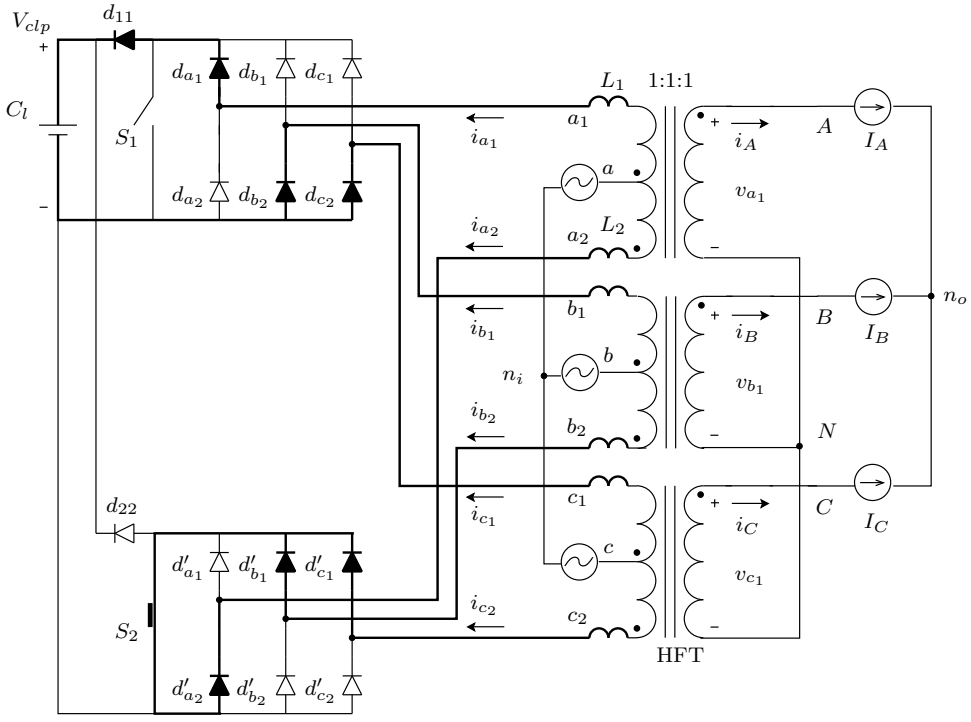


Figure 2.3: Primary clamp circuit analysis

$$v_a - v_{a_1} - L\frac{d}{dt}i_{a_1} - V_{clp} + L\frac{d}{dt}i_{c_1} + v_{c_1} - v_c = 0 \tag{2.2}$$

$$v_a - v_{a_1} - L\frac{d}{dt}i_{a_1} - V_{clp} + L\frac{d}{dt}i_{b_1} + v_{b_1} - v_b = 0 \tag{2.3}$$

$$v_c + v_{c_1} - L\frac{d}{dt}i_{c_2} + L\frac{d}{dt}i_{a_2} - v_{a_1} - v_a = 0 \tag{2.4}$$

$$v_b + v_{b_1} - L\frac{d}{dt}i_{b_2} + L\frac{d}{dt}i_{a_2} - v_{a_1} - v_a = 0 \tag{2.5}$$

$$v_{a_1} + v_{b_1} + v_{c_1} = 0 \tag{2.6}$$

There are nine equations (2.1) to (2.6), involving six unknown rates of change of primary current and three unknown induced voltages in the transformer windings. The slope of the primary side currents are given by (2.7)- (2.9).

$$\frac{d}{dt}i_{a_1} = \frac{d}{dt}i_{a_2} = \frac{3v_a - V_{clp}}{3L} \tag{2.7}$$

$$\frac{d}{dt}i_{b_1} = \frac{d}{dt}i_{b_2} = \frac{6v_b + V_{clp}}{6L} \tag{2.8}$$

$$\frac{d}{dt}i_{c_1} = \frac{d}{dt}i_{c_2} = \frac{6v_c + V_{clp}}{6L} \tag{2.9}$$

When the switch S_1 is switched off and S_2 is switched on, the currents in the transformer are changing according to equations (2.7)-(2.9). When one of the three currents reaches zero, in the winding set connected to S_1 and the corresponding winding current connected to S_2 gets set to its desired value, the currents in the remaining phases, continue to flow at different rates. In the following analysis, let us assume that i_{b_1} goes to zero and i_{b_2} becomes I_B while, i_{a_1} and i_{c_1} are still positive and negative respectively. The network is changed because the branch containing diodes d_{b_1} and d_{b_2} has no current flowing through them and can be considered as an open circuit. All the equations remain the same as in the previous analysis except equation (2.3) is no longer valid, and the currents i_{b_1} and i_{b_2} do not change. In this stage, the slope of the currents, are given by (2.10)-(2.12).

$$\frac{d}{dt}i_{a_1} = \frac{d}{dt}i_{a_2} = \frac{2v_a - 2v_c - V_{clp}}{4L} \tag{2.10}$$

$$\frac{d}{dt}i_{b_1} = \frac{d}{dt}i_{b_2} = 0 \tag{2.11}$$

$$\frac{d}{dt}i_{c_1} = \frac{d}{dt}i_{c_2} = -\frac{2v_a - 2v_c - V_{clp}}{4L} \tag{2.12}$$

If the voltage across the clamp circuit capacitance (V_{clp}) is greater than 6 times the peak of the input line-neutral voltage (V_{ln_i}), all the primary currents during commutation will change in the desired direction. For example, in this case, i_{a_1} being positive, before T_1, should reduce to zero during commutation. Similarly, i_{a_2} should reduce to $-I_A$. This condition also ensures that once the primary currents reach their desired values, the commutation ends naturally. For example, once i_{a_1} reaches zero it remains there. The primary snubber circuit is operational only two times during one switching period, the average current that flows through the clamp circuit per cycle is equal to the sum of the average value of i_{a_1} during T_1. For this case, the average clamp power loss is given by (2.13).

$$P_{pri} = \frac{1}{2} f_s L V_{clp} \left[\frac{3I_B^2}{6v_b + V_{clp}} - \frac{(I_A - I_C)^2}{2v_a - 2v_c - V_{clp}} \right] \tag{2.13}$$

From this analysis, the following points are evident 1) for the proper operation of the clamp circuit, V_{clp} has to be maintained greater than six times the line to neutral voltage. 2) From Fig. 2.3, when d_{11} conducts, the switch, S_1 has to block the voltage across the clamp circuit. 3) During the commutation, undesirable voltages are applied to the load, this leads to distortion in the output voltage and eventually in the output currents. 4) This commutation process also results in power loss given by (2.13). A new modulation method is presented in the following section that overcomes these drawbacks.

2.3 A PWM technique to eliminate the input clamp circuit

The output side matrix converter synthesizes the high-frequency output waveform of the transformer into adjustable frequency and amplitude pulse width modulated (PWM) voltages at terminals u, v and w. When a zero vector is applied in the matrix converter, the secondary currents i_A, i_B and i_C become zero with the help of the secondary side clamp circuit. Then, S_1 and S_2 can be safely switched without the primary side snubber circuit. The input line to neutral voltages and the secondary side voltages are given by

(2.14) and (2.15) respectively; where, $k = 0$ when S_1 is on and $k = 1$ when S_2 is on.

$$\begin{aligned} v_{an_i} &= V_i \cos(\omega_i t) \\ v_{bn_i} &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_{cn_i} &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{2.14}$$

$$\begin{aligned} v_{AB} &= (-1)^k v_{ab} \\ v_{BC} &= (-1)^k v_{bc} \\ v_{CA} &= (-1)^k v_{ca} \end{aligned} \tag{2.15}$$

In a matrix converter, there are 27 unique switching states. Six of these switching states generate synchronously rotating space vectors [56]. These vectors result in zero common-mode voltage at the load terminals [57]. The output voltage space vector is defined by (2.16). Depending on the direction of rotation, these synchronously rotating vectors are further divided into two groups, counter-clockwise (CCW) and clockwise (CW). The three CCW rotating vectors $\vec{V_1}$, $\vec{V_3}$ and $\vec{V_5}$ marked in Fig. 2.4 are obtained when $k = 0$ and terminals $\{u, v, w\}$ are connected to terminals $\{A, B, C\}$, $\{C, A, B\}$ and $\{B, C, A\}$ respectively which are marked in Fig. 2.1. For the same switching states, when $k = 1$, we obtain $\vec{V_4}$, $\vec{V_6}$ and $\vec{V_2}$ respectively. Similarly, the space vectors rotating in clockwise direction are shown in Fig. 2.5. Thus, every switching cycle, the average output voltage vector is synthesized using these six vectors (CCW or CW). These six vectors, divide the complex plane into six symmetrical sectors (marked in Fig. 2.4 and 2.5). At any instant of time, the reference voltage vector (defined by (2.17)) will be in a particular sector. This reference voltage vector is generated on an average over one T_s using the two vectors forming that sector. For example, if $\overline{V}_{ref}$ lies in the first sector, vectors $\vec{V_1}$ and $\vec{V_2}$ are used, such that $\overline{V}_{ref} = d_1\vec{V_1} + d_2\vec{V_2}$, where d_1 and d_2 (given by (2.18)) are the fraction of time for which vectors $\vec{V_1}$ and $\vec{V_2}$ are applied respectively. The values of d_1 and d_2 are constrained to 0.5 because $\vec{V_1}$ and $\vec{V_2}$ are available for maximum 50% of the time. Hence, if only the two adjacent space vectors are used, the maximum modulation index, m is limited to 0.5. In [6], three adjacent voltage vectors are used to

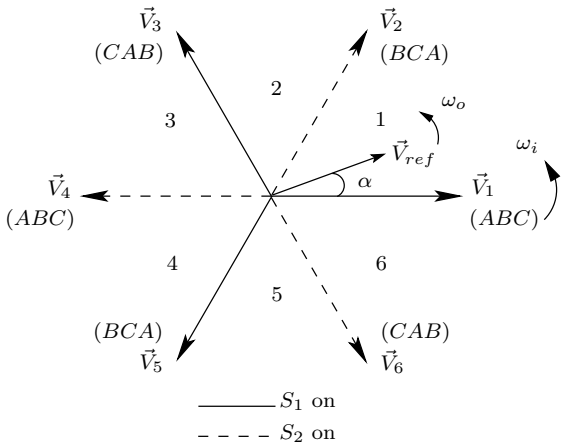


Figure 2.4: CCW rotating vectors

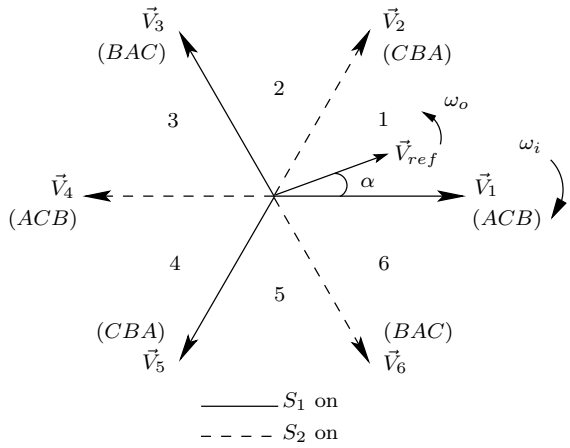


Figure 2.5: CW rotating vectors

obtain a modulation index of 0.75 at the cost of additional switching.

$$\vec{V_o} = v_{un_o} + v_{vn_o}e^{j\frac{2\pi}{3}} + v_{wn_o}e^{-j\frac{2\pi}{3}} \tag{2.16}$$

$$\begin{aligned}
\overline{V}_{ref} &= \overline{V}_o = \overline{v}_{un_o} + \overline{v}_{vn_o}e^{j\frac{2\pi}{3}} + \overline{v}_{wn_o}e^{-j\frac{2\pi}{3}} \\
\overline{v}_{un_o} &= V_o\cos\left(\omega_o t + \phi\right) \\
\overline{v}_{vn_o} &= V_o\cos\left(\omega_o t + \phi - \frac{2\pi}{3}\right) \\
\overline{v}_{wn_o} &= V_o\cos\left(\omega_o t + \phi + \frac{2\pi}{3}\right)
\end{aligned} \tag{2.17}$$

The switching pulses for one cycle are shown in Fig. 2.6. The duty ratios d_1 and d_2 are compared with a triangular carrier waveform, V_{tri} to generate pulses p_{V_1} and p_{V_2}. V_{tri} has a peak value of 0.5 and its frequency is two times the frequency of S_1 and S_2. In sector one, $\vec{V_1}$ is available when S_1 is on, therefore, p_{V_1} is high in the first half of the cycle and p_{V_2} in the second half. Zero vectors are applied in the remaining time. p_z is the switching pulse for the zero vector. In each half cycle, the active vectors are buffered by zero vectors on either side.

Ignoring the effects of the input filter, if only CCW vectors are used for modulation, the grid power factor will equal the load power factor. If only CW vectors are used for modulation, the power angle of the PET will have the same magnitude as of the load

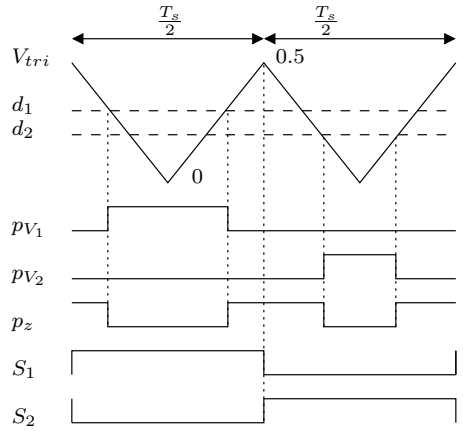


Figure 2.6: Switching pulses for new modulation technique

Table 2.1: Simulation parameters

V_i, V_o, V_{clp}	100V, 30V, 600 V
ω_i, ω_o	$2\pi 60$ rad/sec, $2\pi 60$ rad/sec
Output power	1kW
Load pf.	0.8
L	12 μH

but of opposite sign. If CCW and CW rotating vectors are used for an equal duration of time, unity power factor is obtained on the primary side of the PET [58]. The input power factor can further be varied by changing the reference voltage vector for CCW and CW vectors [57].

$$\begin{aligned} d_1 &= m\frac{2}{\sqrt{3}}\sin\left(\frac{\pi}{3}-\alpha\right) \\ d_2 &= m\frac{2}{\sqrt{3}}\sin(\alpha) \\ m &= \frac{V_o}{V_i} \end{aligned} \tag{2.18}$$

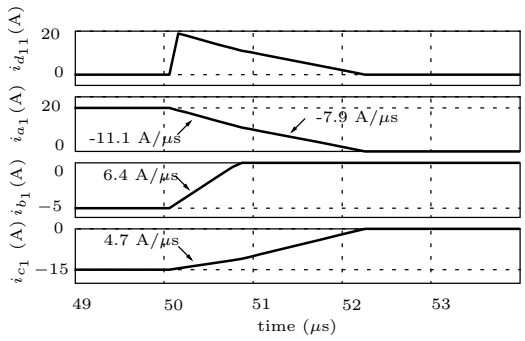


Figure 2.7: Simulation result: input clamp circuit analysis

2.4 Simulation results

The circuit in Fig. 2.3 is simulated in SABER®. The leakage inductance value is chosen to be 12μH, and V_{clp} is kept at 700V. The instantaneous line to neutral voltages are set as follows $v_{an_i} = 100V$, $v_{bn_i} = -40V$ and $v_{cn_i} = -60V$. The secondary side current sources I_A, I_B and I_C are set to 20A, -5A and -15A respectively. In Fig. 2.7 switch S_1 is turned off at 50μs (transition T_1). The currents i_{a_1}, i_{b_1} and i_{c_1} go to zero following the analytically predicted slopes. The current that flows into the clamp circuit is $i_{d_{11}}$, as expected it is the same as i_{a_1}.

A 1kW three-phase AC-AC PET is simulated with the proposed modulation technique. The parameters used in the simulation are listed in Table 2.1. Fig. 2.8(a) shows the input line to neutral voltage waveform with the corresponding filtered line current. This confirms input power factor correction. Fig. 2.8 (b) provides the sinusoidal output load current. The peak of this current is slightly lower than its analytically predicted value. This is due to the voltage loss resulting from the use of a secondary clamp circuit. From Fig. 2.9, it is observed that the currents through the primary side switches are zero when S_1 and S_2 are switched.

2.5 Experimental setup

The experimental setup is shown in Fig. 2.11. Schematically it is represented in Fig. 2.10. All the power electronic devices are controlled using a single Xilinx XC3S500E FPGA. The primary switches, S_1 and S_2 are given pulses at 50% duty at 10kHz. The PWM

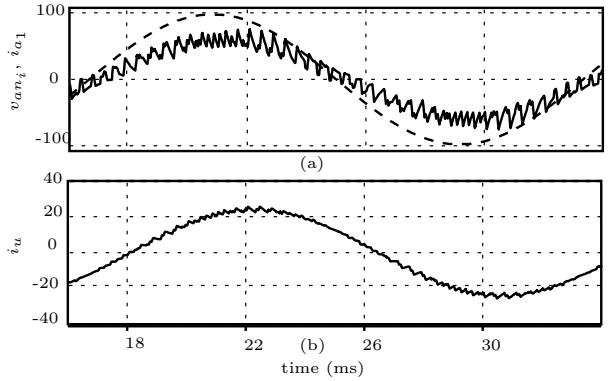


Figure 2.8: Simulation result: Three-phase AC-AC HFT using proposed modulation method (a) input voltage (1V/div) and input current (0.1A/div) (b) output current (1A/div)

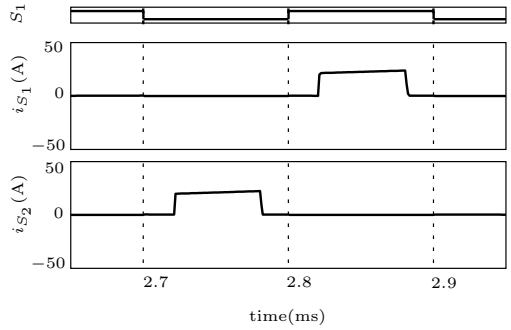


Figure 2.9: Simulation result: Switching pulse and currents through switch S_1 and S_2

Table 2.2: Experimental setup: parameters

V_i, V_o	$80\sqrt{2}$V (SVM) ; $40\sqrt{2}$V(CBM) , 44.46V(SVM); 22.23V (CBM)
ω_i ,ω_o ,f_s	$2\pi60$, $2\pi25$(SVM); $2\pi50$(CBM), 10kHz
R , L	5.5Ω , 30mH
Transformer turns ratio	1:1:1
L_{filter}, C_{filter} , R_{filter}	0.5mH, 20μF(star), 2Ω

pulses for all the switches are generated after the input voltages v_{ab} and v_{ac} are sensed. In order to perform four-step commutation in the MC, two other ADCs sense the output currents i_u and i_v. When the current direction is accurately known, four-step commutation is performed else dead-time commutation is performed. A comparison of four-step and dead-time commutation for this topology is in Chapter 3.

In this chapter, the experimental results are provided for modulation of the matrix converter using Carrier Based Modulation (CBM) [58] and Space Vector Modulation (SVM) [35] that is proposed in this chapter. The experimental parameters for these two modulation strategies are in Table 2.2.

The details of the hardware setup are in Appendix B. The details on FPGA implementation for carrier based modulation and space vector modulation are in Appendix D.

The high-frequency transformers are wound on ferrite cores. These transformers are designed according to the area-product method and have leakage inductance in the range of 15μH and magnetizing inductance of 50mH. The details of the transformer design are in the Appendix C.

The input filter is designed to filter out the high-frequency switching currents at the input of the PET. It is composed of $L_f = 0.5$mH and $C_f = 20\mu$F with a resistance of $R_f = 2\Omega$ in parallel with L_f to damp out the LC resonant frequency of the filter.

2.5.1 Transformer voltages

The primary and secondary voltages of the high-frequency transformer, v_{ab} and v_{AB} respectively are shown in Fig. 2.12. It can be seen that the 60Hz low-frequency input voltages are chopped to high-frequency AC voltages at 10kHz. During the dead-time (t_{dt}) between the switch S_1 and S_2, the primary clamp circuit voltage appears across

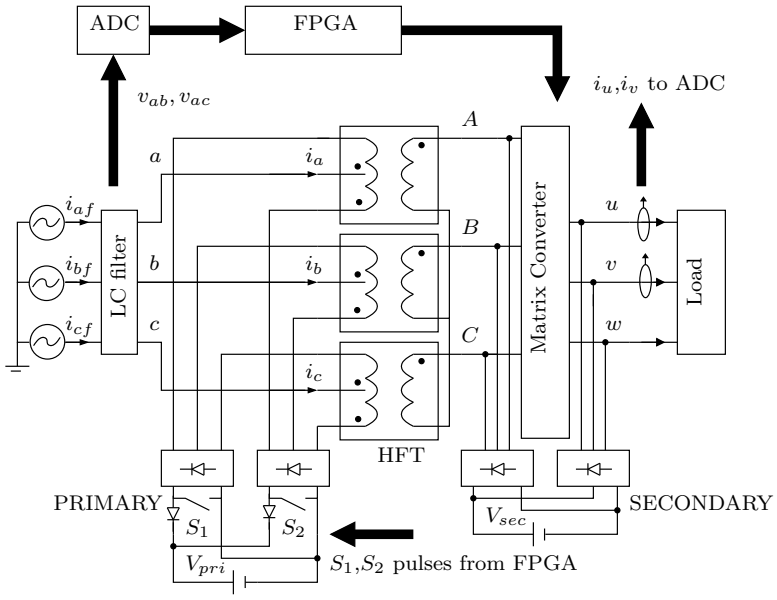


Figure 2.10: Experimental setup

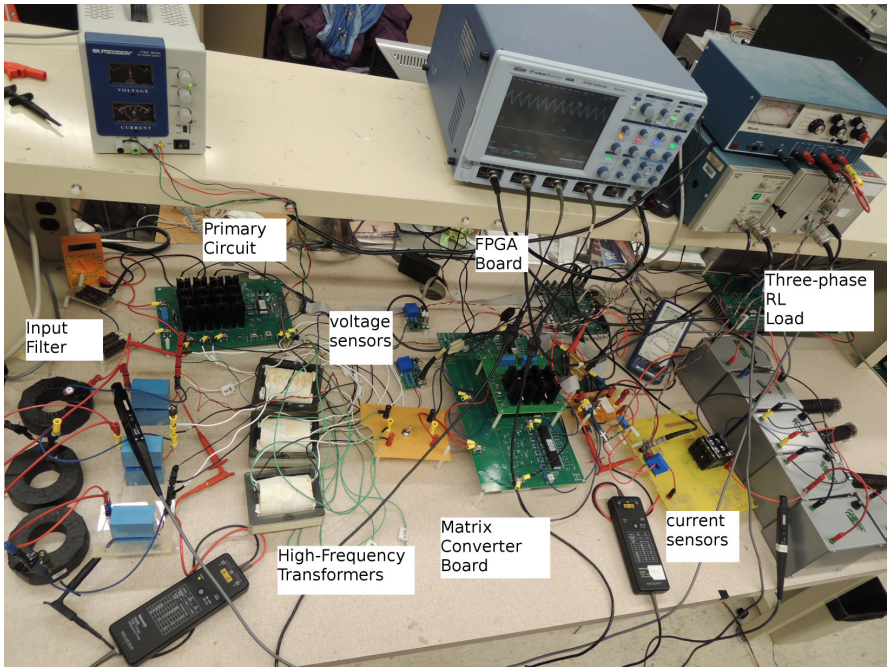


Figure 2.11: Experimental setup for PET for AC to AC power conversion

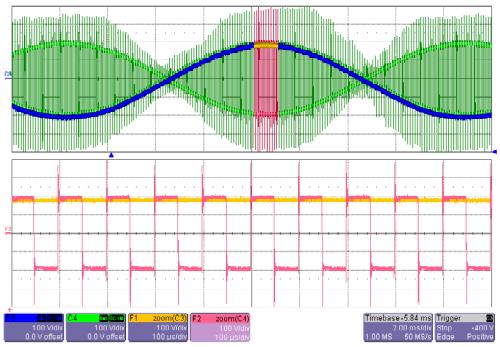


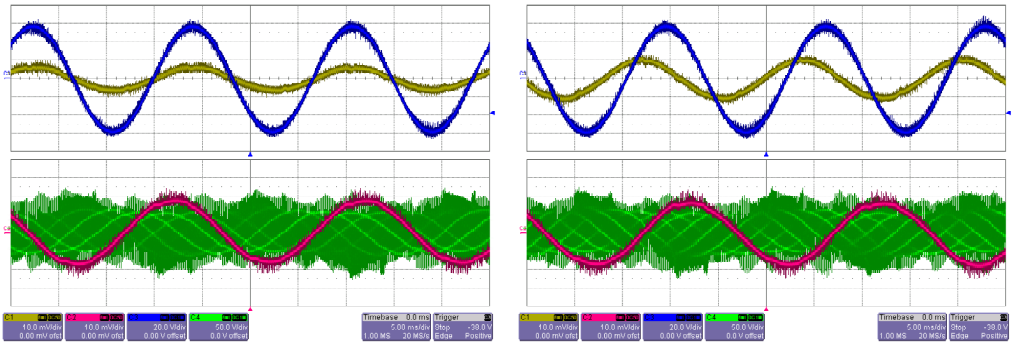
Figure 2.12: Transformer primary v_{ab} (C3: 100V/div) and secondary voltage v_{AB} (C4:100V/div) (top) along with their zoomed waveform at 100μs/div (bottom).

the transformer windings and a spike in voltage is observed. This clamp circuit is a passive RC circuit that needs to be maintained at least two times the line to neutral voltage, during the dead-time, the clamp circuit draws power from the input to support this voltage.

2.6 Experimental results: Carrier based modulation

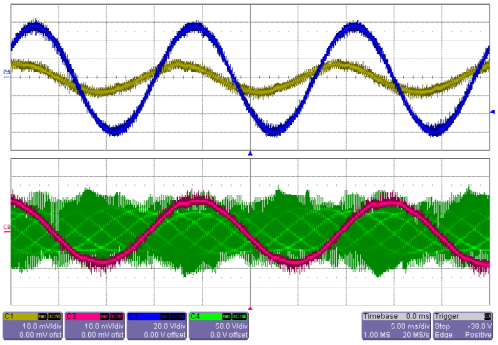
Carrier based modulation is implemented for the following three cases 1) Using only CCW rotating vectors 2) using only CW vectors and 3) using CCW and CW vectors for equal duration of time. The results shown in Fig. 2.13 are taken at $V_i = 40\sqrt{2}$V, $V_o = 22.23V$ with $\omega_i = 2\pi 60$, $\omega_o = 2\pi 50$, $f_s = 10kHz$. The RL load for all these cases is the same and equals 5.5 Ω and 30mH. The output current for all these cases is 1.19A. The experimental results are summarized in Table. 2.3. It can be seen that the input power factor can be varied by changing the vectors used for modulation.

The transformer currents for phase-a are in Fig. 2.14. The upper winding conducts when S_1 is high and the lower winding conducts when S_1 is off. The currents have three distinct sections that correspond to the three vectors applied to the matrix converter. The currents are not zero at the transition of S_1 hence the primary side switches are not ZCS.



(a) CCW vectors only

(b) CW vectors only



(c) CCW+CW vectors

Figure 2.13: Experimental results for carrier based modulation: (top) Filtered input current i_{af} (C1:1A/div) and voltage v_{an} (C3:20V/div) for phase-a; (bottom) output current i_u (C2:1A/div) and voltage v_{un_o} (50V/div) for phase-u when (a) CCW, (b) CW and (c) CCW and CW vectors are used for equal duration of time.

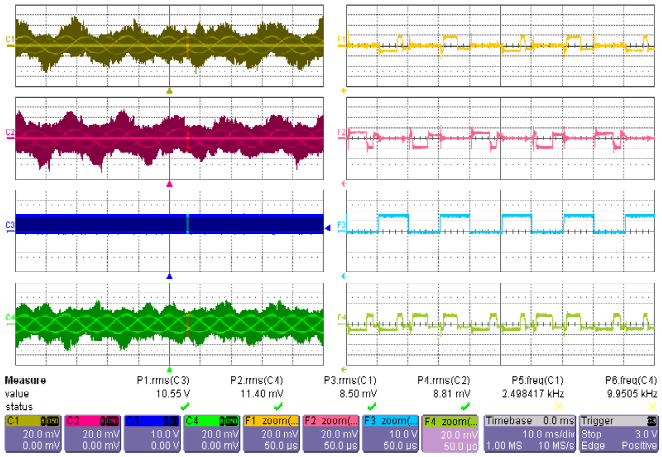


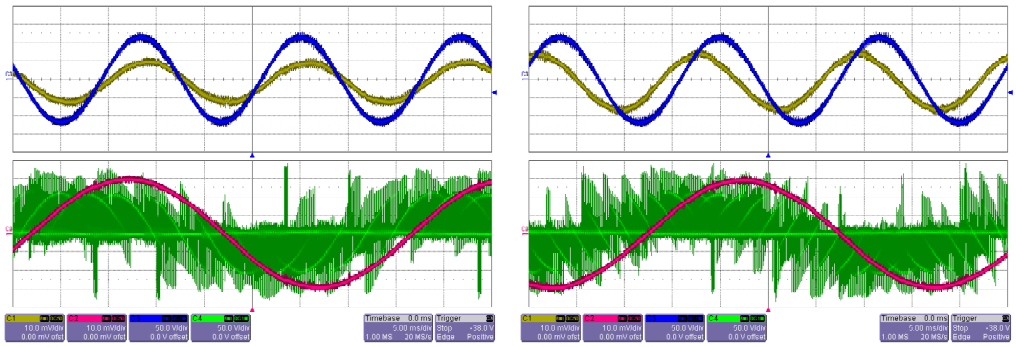
Figure 2.14: (left) Transformer currents for phase-a i_{a1}, i_{a2}, i_A (C1,C2, C4 : 2A/div) and switching pulse for S_1; (right) zoomed waveforms at (50μs/div).

2.7 Experimental results: Space vector modulation

The modulation for the PET is done for three cases 1) using CCW rotating vectors only, 2) using CW vectors only and 3) using CCW and CW vectors for equal duration of time. The experimental parameters of the PET are listed in Table 2.2. In all three cases, the output voltages at 25Hz are supplied to an RL load of 5.5Ω and 30mH. As the input voltages and load are balanced-three-phase, it is sufficient to analyze the results of a single phase only. The waveforms for filtered current (i_{af}), phase-a voltage (v_{an_i}) as well as output current (i_u) and output voltage (v_{un_o}) for these three cases are in Fig. 2.15. In all these cases, the output current i_u has an RMS value of 4.11A. But the input current depends on the vectors used for modulation.

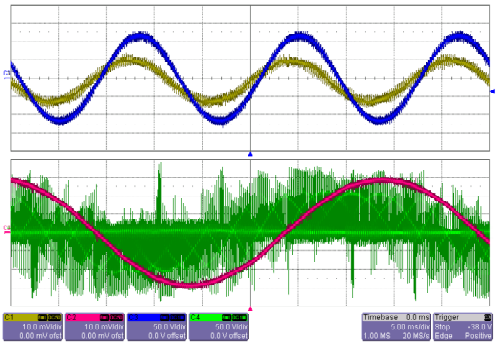
Table 2.3: Experimental results: Carrier based modulation

	I_{af}(A)RMS	P_{in}(Watt)	Q_{in}(VA)	θ(deg)
CCW	0.44	17.92	3.58	-11.29
CW	0.74	17.72	-24.92	54.59
CCW+CW	0.53	18.10	-12.95	35.57



(a) CCW vectors only

(b) CW vectors only



(c) CCW+CW vectors

Figure 2.15: Experimental results for space vector modulation: (top) Input current i_{af} (C1:2A/div) and voltage v_{an} (C3:50V/div) for phase-a; (bottom) output current i_u (C2:2A/div) and voltage v_{uno} (50V/div) for phase u. (a) CCW, (b) CW and (c) CCW and CW vectors are used for equal duration of time.

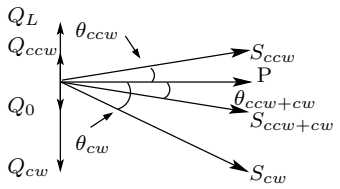


Figure 2.16: Real and reactive power of the PET

2.7.1 Power factor control

The reactive power drawn from the source can be divided into two parts; Power to the input filter (Q_{filter}) and power of the matrix converter. As the transformer magnetizing currents are balanced at high-frequency of 10kHz, it does not contribute to the reactive power at the fundamental of $60Hz$. When CCW vectors are used, the input reactive power is the same as the load reactive power in addition to Q_{filter} (2.19). When CW vectors are used, in addition to Q_{filter}, the input reactive power is equal in magnitude to the load reactive power but opposite in sign (2.20). For these cases, at a certain input voltage, and output load, the voltage drop across the filter inductor L_f is approximately the same and very small. Hence, it can be assumed that $Q_{filter} = Q_0$. When CCW and CW vectors are used for equal duration of time, the net input reactive power is Q_{filter} (2.21). The power diagram for the active and reactive power of this PET with an inductive load of $Q_L = V_o I_o \sin(\rho)$ where ρ is the load angle is in Fig. 2.16. In this experiment, $Q_L = 79.6$VA and $Q_0 = -44.8$VA. The active power consumed by the PET remains the same in all three cases, but the reactive power changes as shown in Table 2.4.

$$Q_{ccw} = Q_{filter} + Q_L \tag{2.19}$$

$$Q_{cw} = Q_{filter} - Q_L \tag{2.20}$$

$$\frac{Q_{ccw} + Q_{cw}}{2} = Q_0 \tag{2.21}$$

Table 2.4: Power factor control

	I_{af} (A)RMS	P_{in} (Watt)	Q_{in} (VA)	θ (deg)
CCW	1.59	123.92	41.55	-18.54
CW	2.17	122.59	-131.17	46.94
CCW+CW	1.66	124.11	-58.62	25.28

$$\cos(\theta_{ccw}) = \frac{P}{\sqrt{P^2 + (Q_0 + Q_L)^2}} \tag{2.22}$$

$$\cos(\theta_{cw}) = \frac{P}{\sqrt{P^2 + (Q_0 - Q_L)^2}} \tag{2.23}$$

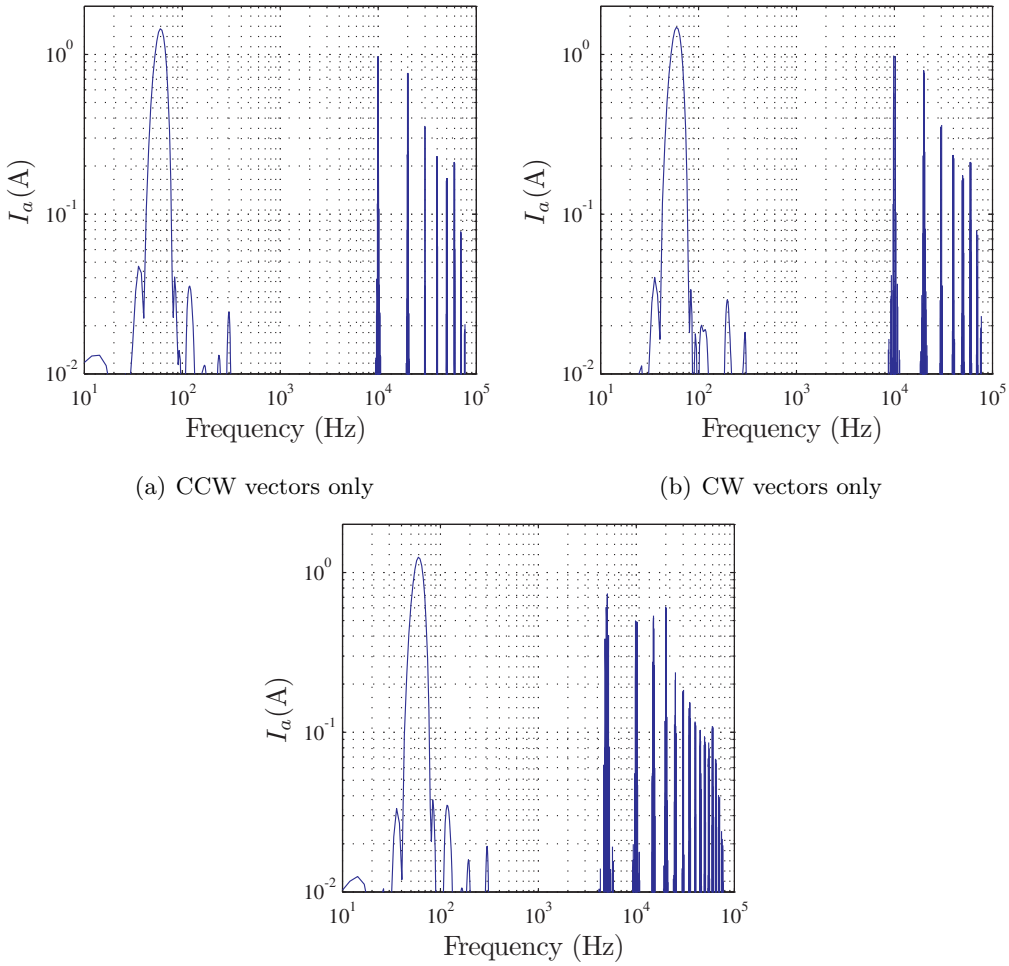
$$\cos(\theta_{ccw+cw}) = \frac{P}{\sqrt{P^2 + Q_0^2}} \tag{2.24}$$

The input power factor for the three cases is given by (2.22)- (2.24). The input side power angle is most leading when only CW (θ_{cw} analytical 45.42^0, observed 46.94^0) vectors are used for modulation. It is most lagging when only CCW vectors (θ_{ccw} analytical -15.85^0, observed -18.54^0) are used for modulation. It is concluded that by use of CCW and CW vectors in varying proportions, the reactive power drawn by the PET can be varied up to a value that depends on the load reactive power. The slight discrepancy is due to the simplifying assumption that the reactive power drawn by the filter inductor is approximately the same for all three cases.

2.7.2 Fourier analysis of input currents

The Fourier spectrum of the input current of the PET for phase-a as shown in Fig. 2.17 are plotted by running an FFT with a hann window on the discrete current data that is collected from the scope. The signal is first filtered and decimated to remove any high-frequency components beyond 80kHz and reduce the sample rate for easier processing.

When either CCW vector or CW vectors are employed, the input current has harmonics at the fundamental as well as at the switching frequency of 10kHz as shown in Fig. 2.17(a) and Fig. 2.17(b). When CCW+CW vectors are used, a 5kHz component is observed in the input current waveform as shown in Fig. 2.17(c). The CCW and CW vectors are used for a duration of 100μs each, hence, the average current vector is synthesized over 200μs. The fundamental component of i_a at 60Hz when only CCW



(a) CCW vectors only

(b) CW vectors only

(c) CCW+CW vectors

Figure 2.17: Fourier spectrum of input current for phase-a

and only CW vectors are used is 1.48A RMS and when CCW and CW vectors are used for equal duration of time, the input current is scaled by $\cos(\rho)$ and equals 1.25A RMS.

In order to calculate the Total Waveform Distortion (TWD) given by (2.25), the fundamental component is calculated by running a DTFT at the fundamental frequency to calculate I_{f1}. The value of I_{rms} is calculated from the discrete data. The TWD for the filtered input currents when CCW vectors are applied is 7.85%, when CW vectors are applied it is 8.37% and when CCW+CW vectors are used it is 13.94%.

$$TWD = \frac{\sqrt{I_{rms}^2 - I_{f1}^2}}{I_{f1}} \tag{2.25}$$

2.7.3 Soft-switching of primary converter

The currents through transformer winding 1 and 2 for phase- a (i_{a1}, i_{a2}) and the corresponding secondary side current (i_A) are shown in Fig. 2.18(a). The currents through the secondary windings of the transformers, i_A, i_B and i_C are shown in Fig. 2.18(b). It can be seen that when a zero vector is applied in the MC, the transformer secondary currents become zero. Hence, ZCS is achieved in S_1 and S_2.

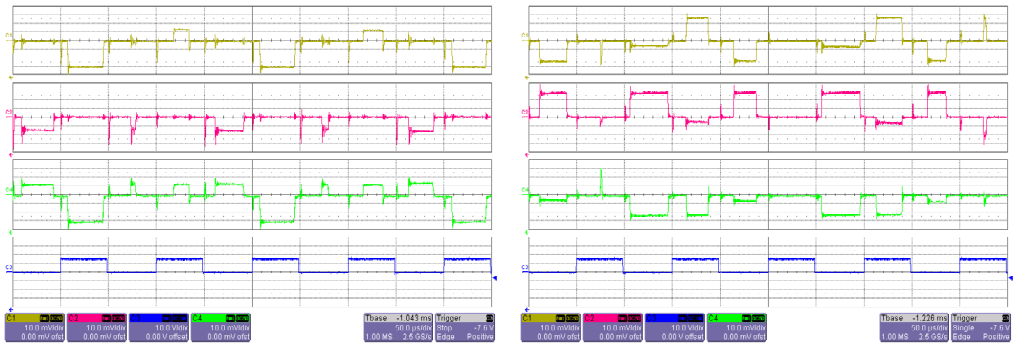
There is a spike of current during the dead-time (1.5μsec) between the transitions of S_1 and S_2, power is supplied to the primary clamp circuit which is there for protection purposes only and is not activated during normal operations.

2.7.4 Output current and voltage

The output currents for phase u and v as well as the line to line voltages are shown in Fig. 2.19. The input current in Fig. 2.19(a), 2.19(c) and 2.19(e) has additional ripple because the input LC filter is not damped. There are spikes in the output line-line voltages when four-step commutation is suspended and dead-time commutation is implemented.

2.7.5 Extended power factor control

With the use of a combination of CW or CCW vectors, the power factor control of the PET is limited by the load power angle (ρ). Hence, a method proposed in [57] for open-end winding drives is applied in this PET where power factor control out of this



(a) (b) CCW vectors only

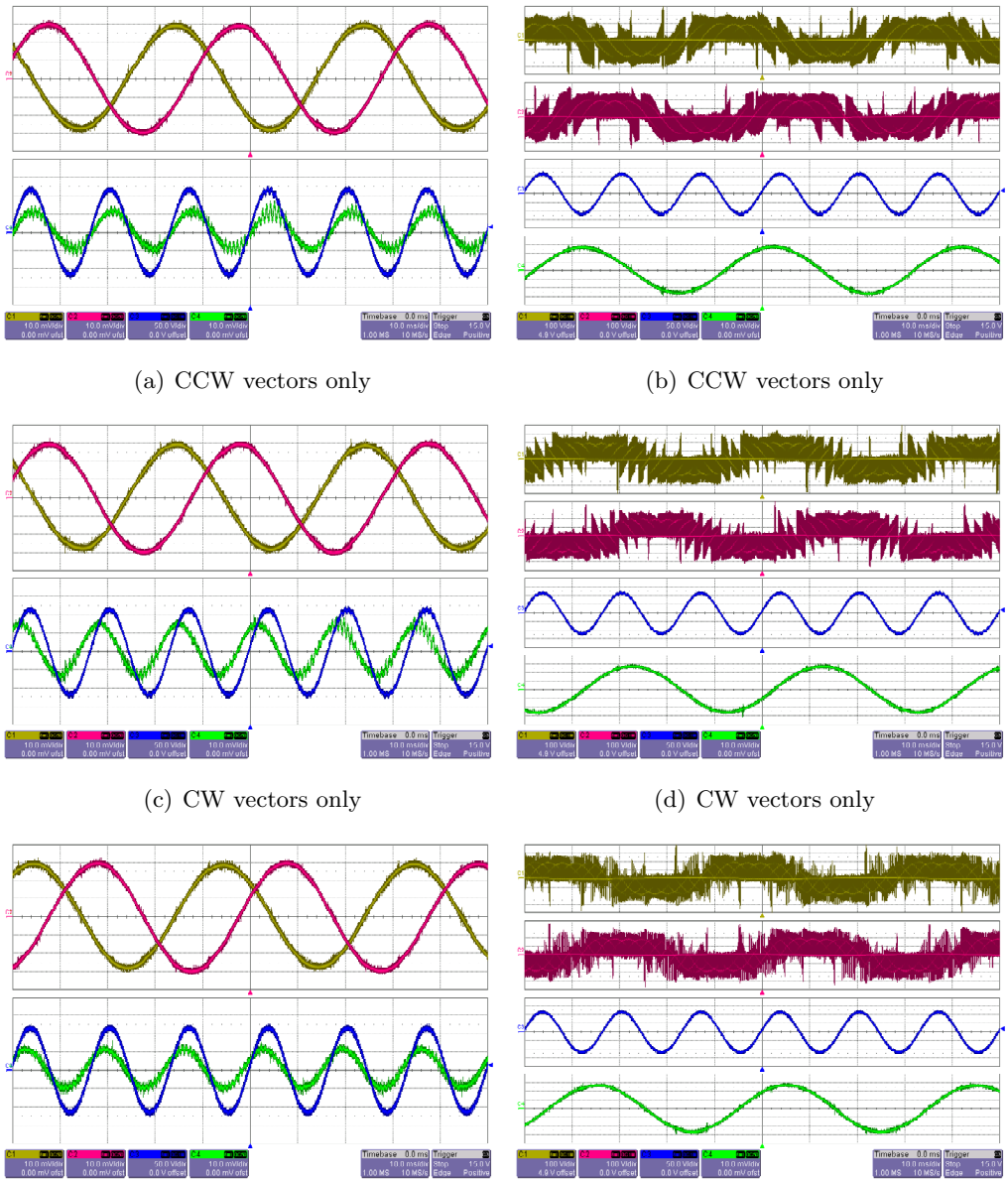
Figure 2.18: Left: Transformer currents for phase-a i_{a1}, i_{a2}, i_A (C1,C2,C4:2A/div) and switching pulses for S_1 (C3: 10V/div); Right: transformer secondary currents i_A, i_B, i_C (C1,C2,C4:2A/div) and switching pulses for S_1 (C3:10V/div).

range is possible at the cost of modulation index. This method is briefly described and analyzed for the proposed PET in this section.

Extended power factor control can be demonstrated by the three cases shown in Fig. 2.20, where the vector $\vec{V}_{ccw}$ and $\vec{V}_{cw}$ are generated using CCW and CW vectors respectively and $|\vec{V}_{ccw}| = |\vec{V}_{cw}| = |\vec{V}_o|$. a) CCW and CW vectors generate the same reference voltage of $\vec{V}_o \cos\beta$ for equal duration of time. b) The reference for the CCW vector is $\vec{V}_o\angle -\beta$ and for the CW vectors the reference voltage is $\vec{V}_o\angle\beta$. c) The reference for the CCW vector is $\vec{V}_o\angle\beta$ and for the CW vectors the reference voltage is $\vec{V}_o\angle -\beta$. In an average sense, the equivalent output voltage in all three cases is the same and equals $V_o^* = \vec{V}_o \cos\beta$. As the load is constant and inductive in nature with a load angle of ρ. In these cases, the current vector is equal to $I\angle\rho$. The equations for input reactive power for Case b is in (2.26). $Q_{ccw\beta}$ and $Q_{cw\beta}$ are the reactive powers due to the CCW and CW vectors at angle β and $-\beta$ respectively. Q_β is the net reactive power of the PET for Case b. The input reactive power for Case c can be calculated in a similar way.

$$\begin{aligned} Q_{ccw\beta} &= Q_0 + V_o^* I \sin(\rho - \beta) \\ Q_{cw\beta} &= Q_0 - V_o^* I \sin(\rho + \beta) \\ Q_\beta &= Q_0 + \frac{1}{2}\left[V_o^* I \sin(\rho - \beta) - V_o^* I \sin(\rho + \beta)\right] \end{aligned} \tag{2.26}$$

The experimental confirmation of variable power factor compensation is proved by



(a) CCW vectors only

(b) CCW vectors only

(c) CW vectors only

(d) CW vectors only

(e) CCW+CW vectors

(f) CCW+CW vectors only

Figure 2.19: Left: (top) Output currents i_u, i_v (C1, C2:2A/div); (bottom) input voltage and current v_{an} (C3:50V/div) and i_{af} (C4:2A/div) for phase-a. Right: (top) Output voltages between phase v_{uv} and v_{vw}; (bottom) input voltage for phase-a (50V/div) and output current for phase-u at 2A/div.

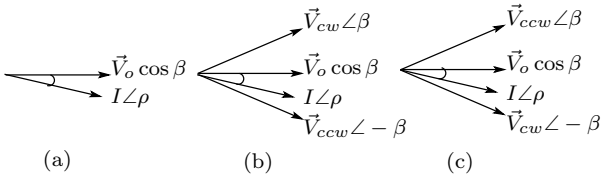


Figure 2.20: Extended power factor control

Table 2.5: Extended power factor control

	I_{af} (A)RMS	P_{in} (Watt)	Q_{in} (VA)	θ (deg)
Case a	0.58	22.38	-28.56	51.91
Case b	0.78	21.88	-44.04	63.58
Case c	0.43	22.95	-13.83	31.07

running the three cases described above for $V_i = 60\sqrt{2}, V_o = 33.35$V, 50Hz and $\beta = 48^0$. The load is a resistor of 5.5Ω and inductor of $30mH$. The waveforms are in Fig. 2.21 and the results are compiled in Table 2.5. As predicted, the values of $P_{in} = 22$Watt for these three cases is the same however the values for Q_{in} is different, with Case b (expected -45.06VA observed -44.04VA) having the most leading power factor and Case c (expected -12.81VA observed -13.83VA) having the most lagging power factor.

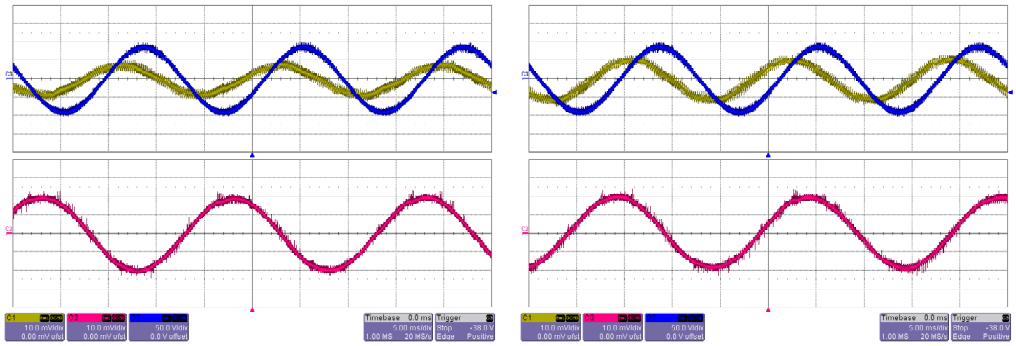
The experimental values of input reactive power for different values of β are compared with the expected values in Fig. 2.22. It can be seen that they match closely.

2.7.6 Variable frequency generation

The output voltages in Fig. 2.15 are at 25Hz and the output voltages in Fig. 2.21 are at 50Hz. Hence, variable frequency and magnitude output voltages can be generated using this PET.

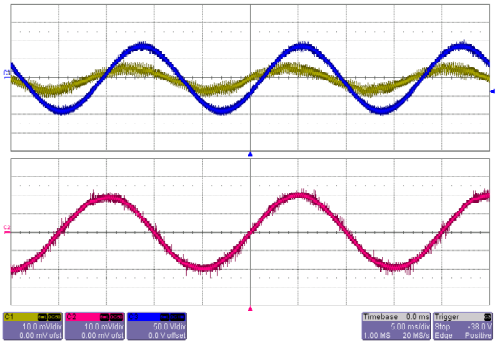
2.8 Conclusions and future work

In this chapter a novel power electronic transformer is presented that has the following features,



(a) Case a

(b) Case b



(c) Case c

Figure 2.21: Extended power-factor control: (top) Filtered input current i_{af} (C1:1A/div) and voltage for phase-a v_{an} (C3:50V/div); (bottom) output current i_u (C2:1A/div)

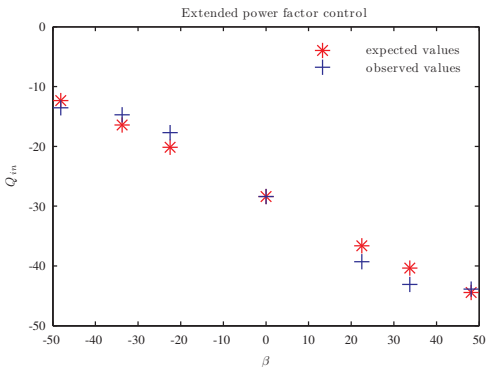


Figure 2.22: Power factor variation for different values of β

- Single-stage power conversion with galvanic isolation and bi-directional power flow capability.
- Variable frequency and amplitude pulse width modulated voltage generation.
- Power factor control at the input.
- Zero current switching (ZCS) for the input side converter.
- Compact size and easy control technique that can be implemented in a single FPGA.

The simulation/hardware results verify that variable frequency and voltage generation is possible in this PET. CCW and CW rotating vectors can be used in varying proportions to achieve control over the reactive power at the input of this PET. The experimental prototype has been tested extensively and the experimental results match the analytical predictions. The experimental results show that, with the new modulation technique, ZCS is achieved for the primary switches, S_1 and S_2. This is an improvement over carrier based modulation. Although, the proposed solution eliminates the primary clamp circuit, the secondary clamp circuit is still necessary. The secondary clamp circuit analysis is done in Chapter 3.

2.8.1 Future work

- When CBM is used in the secondary side MC, the common-mode voltages at terminals $\{u, v, w\}$ is nearly zero. When SVM is used, since zero vectors are applied in the matrix converter, switching common-mode voltages are present at terminals $\{u, v, w\}$. Common-mode voltage elimination can be obtained by operating this PET as an open-ended drive.
- The TWD of the filtered currents is high in this PET. Optimal filter design is required to obtain better TWD.

Note: Parts of this chapter have been reprinted from [35] ©2010 IEEE

Chapter 3

AC-AC Power Electronic Transformer: Clamp Circuit Analysis

3.1 Introduction

The Matrix converter based Power Electronic Transformer discussed in Chapter 2 is a single-stage solution with features of bi-directional power flow capabilities, galvanic isolation and power factor control. Theoretically, this PET provides single-stage power conversion and obviates the need for any storage elements. However, any switching transition in the load side converter causes over voltages due to the presence of finite leakage inductances in the windings of the high-frequency transformer. A clamp circuit as shown in Fig. 3.1 is needed for commutation of this leakage energy and to protect the power electronic devices.

This chapter presents a detailed analysis of secondary side leakage energy commutation for the reduced-switch topology in Fig. 3.1 with respect to the modulation method proposed in Chapter 2. The power losses associated with the clamp circuit operation, the commutation time required and the voltage loss incurred are analytically calculated and checked with simulation. The analysis developed in this chapter is quite general and is applicable to analysis of the clamp circuit in other MC based PETs such as topology

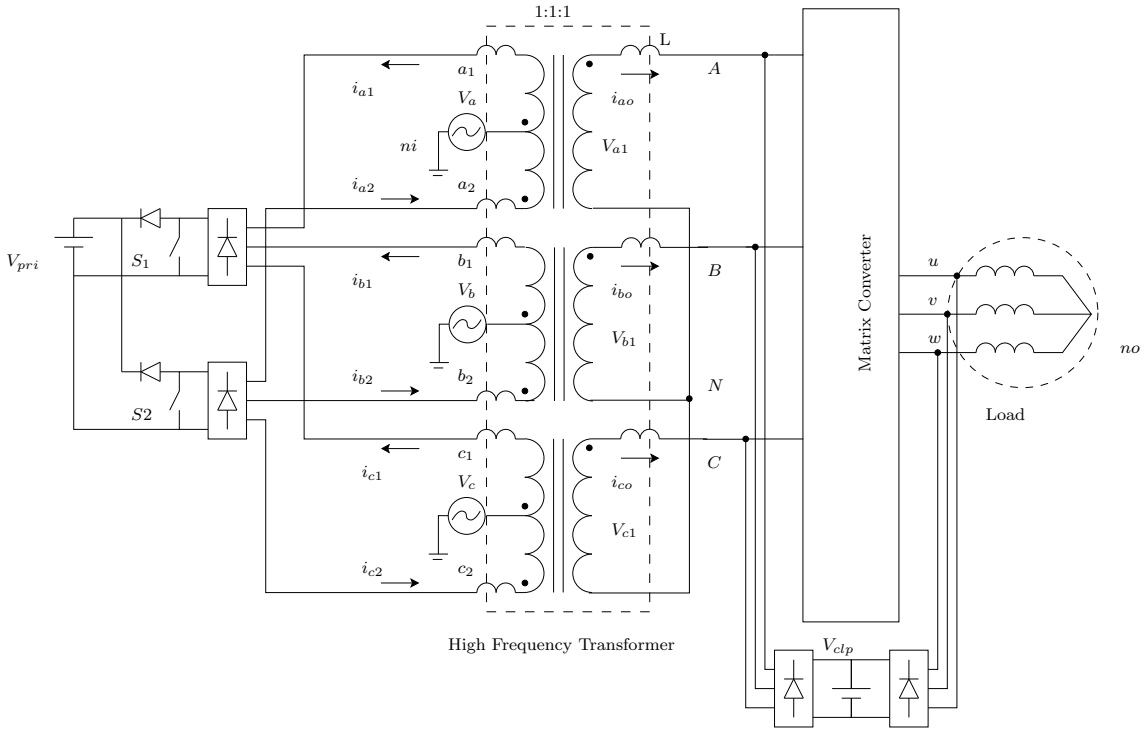


Figure 3.1: Topology with non-idealities

B2 and B3 in [53].

Four-step commutation has been proposed for matrix converters where the input is a voltage port and the output a current port [59]. However, in some MC based PETs, the input as well as the output ports have inductance. A comparison of dead-time commutation and four-step commutation for the MC based PET in Fig. 3.1 is presented in section 3.6.

3.2 Introduction of the secondary clamp circuit

In the Chapter 2, a high-frequency transformer isolated adjustable speed drive was introduced and a new modulation strategy was proposed for it. The switching pulses for this PET are show in Fig. 3.2. When a zero vector is applied in the matrix converter, the output currents free-wheel through the matrix converter and the transformer currents

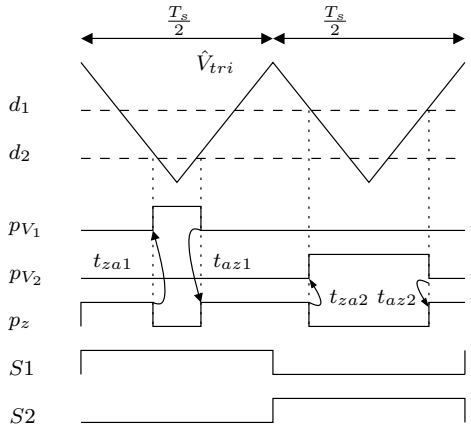


Figure 3.2: Switching pulses

are brought to zero with the help of the secondary side clamp circuit, hence S_1 and S_2 are soft switched (ZCS) and the primary clamp circuit is no longer necessary.

Whenever there is a change in switching state of the matrix converter, the currents through the finite leakage inductances of the transformer are interrupted and the secondary clamp circuit provides a path for these currents to flow. The clamp circuit is operational four times each switching cycle, for two zero vector to active vector transitions (t_{za1}, t_{za2}) and remaining two for active vector to zero vector transitions (t_{az1}, t_{az2}). In this chapter, the clamp circuit refers to the secondary side clamp circuit. This secondary clamp circuit consists of a diode bridge connected to a capacitor. The power extracted from the clamp circuit can be supplied to the auxiliary control circuits. For simplicity here, the clamp capacitor is replaced by a DC voltage source of magnitude V_{clp}. The diodes in the clamp circuit are considered to be fast acting so they come into conduction almost instantaneously.

3.3 Clamp circuit analysis

In this analysis, the turns ratio of the three winding transformers are assumed to be unity, and the leakage inductance of each winding is L. Also, the commutation time intervals are small compared with the switching period. The input three-phase balanced voltages have a peak value of V_i and a frequency of ω_i rad/sec and are given by (3.1).

Neglecting the switching ripple, the output current can be represented by (3.2), where, I_o is the peak value of output current and ω_o is the frequency in rad/sec.

$$\begin{aligned} v_a(t) &= V_i \cos(\omega_i t) \\ v_b(t) &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_c(t) &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \tag{3.1}$$

$$\begin{aligned} i_u(t) &= I_o \cos(\omega_o t - \phi) \\ i_v(t) &= I_o \cos\left(\omega_o t - \frac{2\pi}{3} - \phi\right) \\ i_w(t) &= I_o \cos\left(\omega_o t + \frac{2\pi}{3} - \phi\right) \end{aligned} \tag{3.2}$$

In this section the operation of the secondary clamp circuit is analyzed for 1) an active to zero vector transition and 2) a zero to active vector transition. Depending on the polarity of output currents, each of these transitions has two special cases, a) when two out of three currents are positive and b) when two out of three-phase currents are negative. Hence, each transition is studied when $\omega_o t$ is between $-\pi/6$ and $\pi/6$ and when $\omega_o t$ is between $\pi/6$ and $\pi/2$ (assuming $\phi = 0$). The analysis for these commutation intervals when S_2 is on, are the same as for the commutation intervals when S_1 is on, except that the input voltage polarities are reversed, hence, the analysis when S_1 is on is sufficient.

As the switching frequency is much higher than the fundamental frequency, in one switching cycle, the output currents and the input phase voltages can be considered to be DC. The output phase currents are assumed to be constant current sources of values I_u, I_v and I_w. As synchronously rotating vector are used in the modulation, each output terminal of the matrix converter is connected to a unique input terminal, leading to six possible combinations. When an active vector is applied, for generality, the input voltage connected to phase u, v and w are denoted by v_u, v_v and v_w respectively. For a given choice of output currents, the power loss and commutation time depends on the input voltage. This dependence can be observed by plotting the clamp power loss or the commutation time required for all combinations of input voltages. In the last part of this section, the voltage loss incurred due to operation of clamp circuit is calculated.

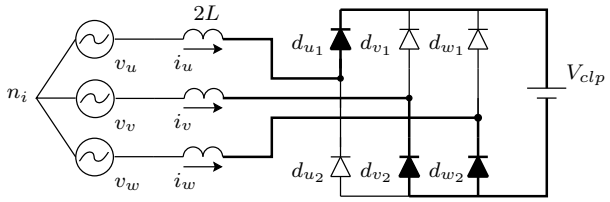


Figure 3.3: Active vector to zero vector equivalent circuit

3.3.1 Active to zero vector transition

When a zero vector is applied in the matrix converter, the output currents free-wheel through the matrix converter and the clamp circuit will provide a path for the leakage currents to flow. Without loss of generality, let us analyze the case when S_1 is on and a zero vector is applied (t_{az1}). Neglecting the magnetizing current, the transformer can be represented by its series leakage inductance ($2L$) only. Say i_u is positive and i_v and i_w are negative (i.e $-\pi/6 \leq \omega_o t \leq \pi/6$). The instantaneous values of phase currents i_u, i_v and i_w when the zero vector is applied are denoted by I_u, I_v and I_w respectively. The positive direction of current in phase u forces diode d_{u_1} to conduct. Similarly, diodes d_{v_2} and d_{w_2} will conduct. The equivalent circuit when the clamp circuit is operational is drawn in Fig. 3.3. The KVL equation for the loop containing v_u, $2L$, d_{u_1}, V_{clp}, d_{v_2}, $2L$ and v_v is given by (3.3). Similarly, the KVL loop containing v_u, $2L$, d_{u_1}, V_{clp}, d_{w_2}, $2L$ and v_w is given by (3.4). The KCL equation for currents at node n_i results in (3.5).

$$v_u - 2L\frac{d}{dt}i_u - V_{clp} + 2L\frac{d}{dt}i_v - v_v = 0 \tag{3.3}$$

$$v_u - 2L\frac{d}{dt}i_u - V_{clp} + 2L\frac{d}{dt}i_w - v_w = 0 \tag{3.4}$$

$$\frac{d}{dt}i_u + \frac{d}{dt}i_v + \frac{d}{dt}i_w = 0 \tag{3.5}$$

The above three equations can be solved to obtain the rate of change of phase currents (3.6) - (3.8)

$$\frac{d}{dt}i_u = \frac{3v_u - 2V_{clp}}{6L} \tag{3.6}$$

$$\frac{d}{dt}i_v = \frac{3v_v + V_{clp}}{6L} \tag{3.7}$$

$$\frac{d}{dt}i_w = \frac{3v_w + V_{clp}}{6L} \tag{3.8}$$

The currents i_u, i_v and i_w are flowing with rates defined by equations (3.6) - (3.8). Depending on the values of t_v and t_w from Table 3.1, either i_v or i_w will become zero amperes. In this case, let current i_v reaches zero amperes first. Diode d_{v_2} will stop conducting and equation (3.3) is no longer involved. Solving for the new rate of change of currents, to obtain (3.9).

$$\frac{d}{dt}i_u = -\frac{d}{dt}i_w = \frac{v_u - v_w - V_{clp}}{4L} \tag{3.9}$$

Once the initial value of current as well as rate of change of currents is known, the total time required (t_{ct}) for all the phase currents to become zero can be calculated. For this case, the current that flows into the clamp circuit is the same as i_u. The power loss in the clamp circuit can be calculated by (3.10), where $< i_u >_{t_{ct}}$ is the average value of current i_u during the commutation interval t_{ct}. The clamp circuit power loss for the case when i_w reaches zero before i_v can be found by interchanging I_v with I_w and v_v with v_w in (3.10).

$$\begin{aligned} P_{Clamp} &= V_{clp} < i_u >_{t_{ct}} \\ &= \frac{V_{clp} f_s L}{2}\left[-\frac{(I_u - I_w)^2}{v_u - v_w - V_{clp}} + \frac{3I_v^2}{3v_v + V_{clp}}\right] \end{aligned} \tag{3.10}$$

A similar analysis is done when S_1 is on and i_u and i_v are positive and i_w is negative ($\pi/6 \leq \omega_o t \leq \pi/2$). The power loss for interval t_{za1} when i_v reaches zero first is given in (3.11).

$$\begin{aligned} P_{Clamp} &= V_{clp} < i_w >_{t_{ct}} \\ &= \frac{V_{clp} f_s L}{2}\left[-\frac{(I_u - I_w)^2}{v_u - v_w - V_{clp}} + \frac{3I_v^2}{-3v_v + V_{clp}}\right] \end{aligned} \tag{3.11}$$

From the above analysis, it is clear that as long as the clamp capacitor voltage is maintained higher than three times the peak line to neutral voltage, the currents will change in the desired manner. If one of the currents reach zero, the other two currents flow at a different rate and eventually become zero. The power loss in the clamp circuit is proportional to switching frequency, leakage inductance and the instantaneous values of phase currents and voltages. The value of V_{clp} is selected to be $5 \times V_i$. For selected values of output currents, the the per unit power loss is plotted as $\omega_i t$ is varied from

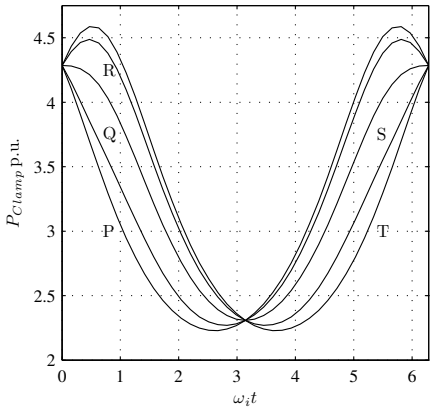


Figure 3.4: Active to zero vector $\omega_o t$(rads)= $-\frac{\pi}{6}$ (P), $-\frac{\pi}{12}$ (Q) , 0 (R), $\frac{\pi}{12}$ (S) and $\frac{\pi}{6}$ (T)

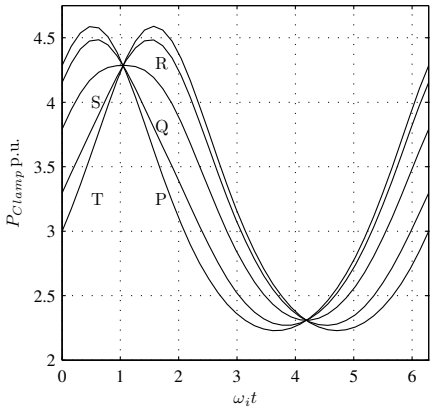


Figure 3.5: Active to zero vector $\omega_o t$(rads) = $\frac{\pi}{6}$ (P) , $\frac{\pi}{4}$ (Q), $\frac{\pi}{3}$ (R), $\frac{5\pi}{12}$ (S) and $\frac{\pi}{2}$ (T)

Table 3.1: Commutation time (active to zero, S_1 on)

Output currents	time	Total time (t_{ct})
$-\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{6}$	$t_v = -\frac{6LI_v}{3v_v+V_{clp}}$ $t_w = -\frac{6LI_w}{3v_w+V_{clp}}$	$= -2L\frac{(I_u-I_w)}{v_u-v_w-V_{clp}}$for $t_v \leq t_w$ $= -2L\frac{(I_u-I_v)}{v_u-v_v-V_{clp}}$otherwise
$\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{2}$	$t_v = -\frac{6LI_v}{3v_v-V_{clp}}$ $t_u = -\frac{6LI_u}{3v_u-V_{clp}}$	$= -2L\frac{(I_u-I_w)}{v_u-v_w-V_{clp}}$for $t_v \leq t_u$ $= -2L\frac{(I_v-I_w)}{v_v-v_w-V_{clp}}$otherwise

0 to 2π in Fig. 3.4 and Fig. 3.5. One per unit value is equal to $0.5LI_o^2 f_s$ Watts. It is observed that the power loss for the case when $-\pi/6 \leq \omega_o t \leq \pi/6$ is bound between the curves corresponding to $\omega_o t = -\pi/6$ and $\omega_o t = \pi/6$. When $\pi/6 \leq \omega_o t \leq \pi/2$, the clamp power loss is bounded by the power loss curves corresponding to $\omega_o t = \pi/6$ and $\omega_o t = \pi/2$. From the graph, the peak value of power that goes into the clamp circuit is 4.6 per unit and the minimum value is 2.2 per unit.

Table 3.1 lists the commutation time for an active to zero vector transition for different cases of output currents. The per unit time required is plotted in Fig. 3.6 for five selected values for output current for different combinations of input voltages. The maximum commutation required is equal to 1.06 p.u., where one p.u. equals LI_o/V_i.

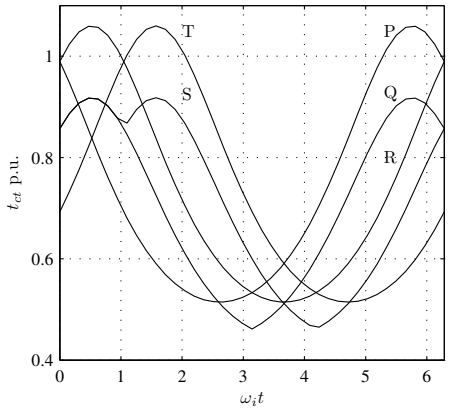


Figure 3.6: Commutation time required: Active to zero vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), 0 (Q) , $\frac{\pi}{6}$ (R), $\frac{\pi}{3}$ (S) and $\frac{\pi}{2}$ (T)

3.3.2 Zero vector to active vector transition

A similar analysis is done for the transition from a zero vector to an active vector when switch S_1 is on (t_{za1}). Consider the currents in the transformer windings are zero, when an active vector is applied in the matrix converter such that phase u, v and w are connected to phase voltages v_u, v_v and v_w respectively. In one switching cycle, the output currents can be assumed to be constant and are given by I_u, I_v and I_w for phase u, v and w respectively. The clamp circuit is active until the transformer currents match the value of the output currents. For the case when current I_u is positive and I_v and I_w are negative ($\pi/6 \leq \omega_o t \leq \pi/6$), diode d_{u_2}, d_{v_1} and d_{w_1} will begin to conduct. The equivalent circuit is drawn in Fig. 3.7. The KVL equations for the two loops in this circuit are given by (3.12) and (3.13). The KCL equation at node n_i is given by (3.14).

$$v_v - 2L\frac{d}{dt}i_v - V_{clp} + 2L\frac{d}{dt}i_u - v_u = 0 \tag{3.12}$$

$$v_w - 2L\frac{d}{dt}i_w - V_{clp} + 2L\frac{d}{dt}i_u - v_u = 0 \tag{3.13}$$

$$\frac{d}{dt}i_u + \frac{d}{dt}i_v + \frac{d}{dt}i_w = 0 \tag{3.14}$$

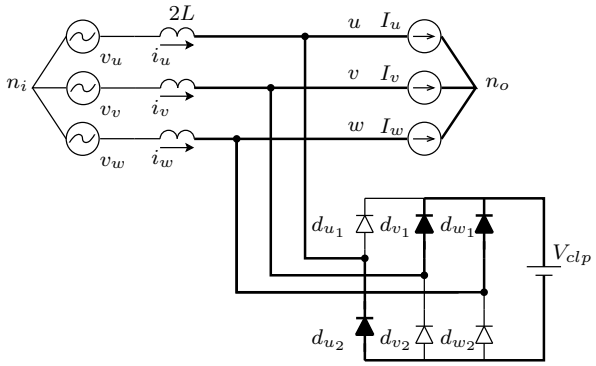


Figure 3.7: Zero vector to active vector equivalent circuit

The three equations and three unknowns (3.12) - (3.14) can be solved to obtain the rate of change of currents given by (3.15) - (3.17).

$$\frac{d}{dt}i_u = \frac{3v_u + 2V_{clp}}{6L} \tag{3.15}$$

$$\frac{d}{dt}i_v = \frac{3v_v - V_{clp}}{6L} \tag{3.16}$$

$$\frac{d}{dt}i_w = \frac{3v_w - V_{clp}}{6L} \tag{3.17}$$

The phase currents i_u, i_v and i_w currents flow at the rates defined above until the time one of them reaches the output value. If i_v equals I_v, then, diode d_{v_1} ceases to conduct and i_u and i_w will change at rates given by (3.18).

$$\frac{d}{dt}i_u = -\frac{d}{dt}i_w = \frac{v_u - v_w + V_{clp}}{4L} \tag{3.18}$$

During the commutation interval, the difference between the inductor current and output current flows into the the clamp circuit. The associated clamp power loss is given by (3.19). When I_u and I_v are positive and I_w is negative ($\pi/6 \leq \omega_o t \leq \pi/2$), the clamp power loss is given by (3.20).

$$\begin{aligned} P_{Clamp} &= V_{clp}(I_u - < i_u >_{t_{ct}}) \\ &= \frac{V_{clp} f_s L}{2}\left[\frac{(I_u - I_w)^2}{v_u - v_w + V_{clp}} - \frac{3I_v^2}{3v_v - V_{clp}}\right] \end{aligned} \tag{3.19}$$

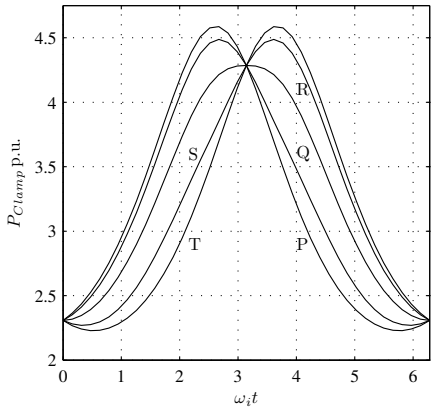


Figure 3.8: Zero to active vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), $-\frac{\pi}{12}$ (Q) , 0 (R), $\frac{\pi}{12}$ (S) and $\frac{\pi}{6}$ (T)

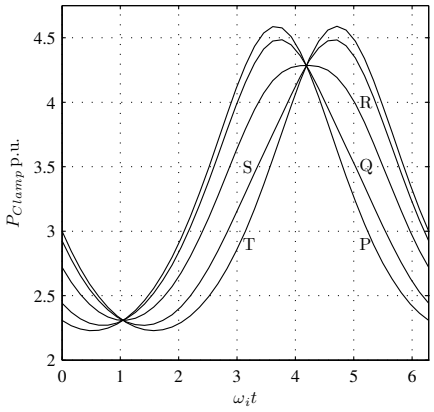


Figure 3.9: Zero to active vector $\omega_o t$ (rads) = $\frac{\pi}{6}$ (P) , $\frac{\pi}{4}$ (Q), $\frac{\pi}{3}$ (R), $\frac{5\pi}{12}$ (S) and $\frac{\pi}{2}$ (T)

Table 3.2: Commutation time for zero to active vector with S_1 on)

Transition	time	Total time (t_{ct})
$-\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{6}$	$t_v = \frac{6LI_v}{3v_v - V_{clp}}$ $t_w = \frac{6LI_w}{3v_w - V_{clp}}$	$= 2L\frac{(I_u - I_w)}{v_u - v_w + V_{clp}}$for $t_v \leq t_w$ $= 2L\frac{(I_u - I_v)}{v_u - v_v + V_{clp}}$otherwise
$\frac{\pi}{6} \leq \omega_o t \leq \frac{\pi}{2}$	$t_v = \frac{6LI_v}{3v_v + V_{clp}}$ $t_u = \frac{6LI_u}{3v_u + V_{clp}}$	$= 2L\frac{(I_u - I_w)}{v_u - v_w + V_{clp}}$for $t_v \leq t_u$ $= 2L\frac{(I_v - I_w)}{v_v - v_w + V_{clp}}$otherwise

$$\begin{aligned} P_{Clamp} &= V_{clp}(I_w - < i_w >_{t_{ct}}) \\ &= \frac{V_{clp} f_s L}{2}\left[\frac{(I_u - I_w)^2}{v_u - v_w + V_{clp}} + \frac{3I_v^2}{3v_v + V_{clp}}\right] \end{aligned} \tag{3.20}$$

The value of V_{clp} is selected to be $5 \times V_i$. The per unit power loss curves for certain values of output current as $\omega_o t$ is varied from 0 to 2π are plotted in Fig. 3.8 and Fig. 3.9. Here again the maximum and minimum clamp power loss is equal to 4.6 and 2.2 p.u. respectively. Table 3.2 lists the commutation time required for a zero to active vector transition. As before, the commutation time required in per unit as a function of input voltage is plotted in Fig. 3.10. The worst case commutation time required is $1.06LI_o/V_i$ sec. There is some output voltage distortion associated with the clamp

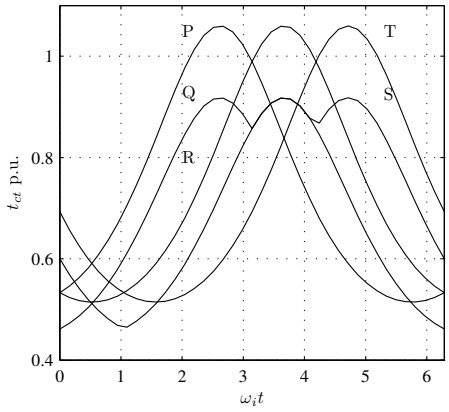


Figure 3.10: Commutation time required: Zero to active vector $\omega_o t$ (rads)= $-\frac{\pi}{6}$ (P), 0 (Q) , $\frac{\pi}{6}$ (R), $\frac{\pi}{3}$ (S) and $\frac{\pi}{2}$ (T)

circuit operation. During an active to zero vector transition, the clamp circuit voltage does not appear across the load. A voltage loss or distortion occurs only during a zero to active vector transitions. In a worst case situation, the clamp circuit may apply $\pm\frac{2}{3}V_{clp}$ across the output line-neutral of a particular phase for the longest commutation time.

3.4 Simulation results

3.4.1 Intervals t_{az1} and t_{za1}

The circuit in Fig. 3.1 is simulated in SABER®for one switching cycle. The input voltages and output currents are DC sources of magnitudes listed in Table 3.3. Fig. 3.11 is the plot of currents i_u, i_v and i_w when a zero vector is applied and S_1 is on. The phase currents for the zero to active vector transition when S_1 is on are shown in Fig. 3.12. The simulated values for the slope of the current coincide with the calculated values. The clamp circuit power loss during a zero to active vector transition when S_2 is on (t_{za2}) is equal to the power loss for an active to zero transition when S_1 is on (t_{az1}) and it is equal to 44 Watt by calculation. The clamp circuit power loss for the transition t_{az2} equals that of t_{za1} equal to 25.74 Watts. The values for commutation time required as well as total clamp power loss in one switching cycle are listed in 3.4. The calculated values match the simulated values very closely.

Table 3.3: Simulation parameters

v_u, v_v,v_w	100 ,-40,-60 V
I_u, I_v , I_w	20, -5,-15 A
V_{clp}	600 V
L	50μ H
Turns ratio	1:1:1

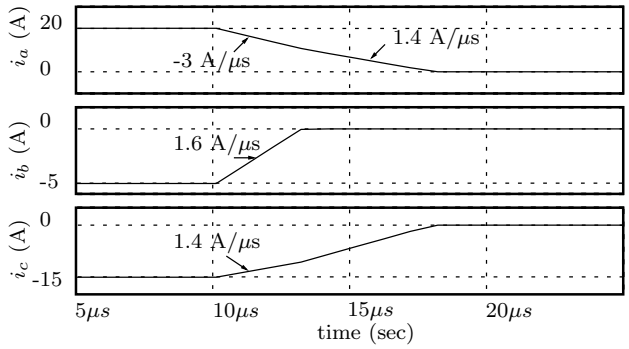


Figure 3.11: Active to zero vector simulation results (t_{az1})

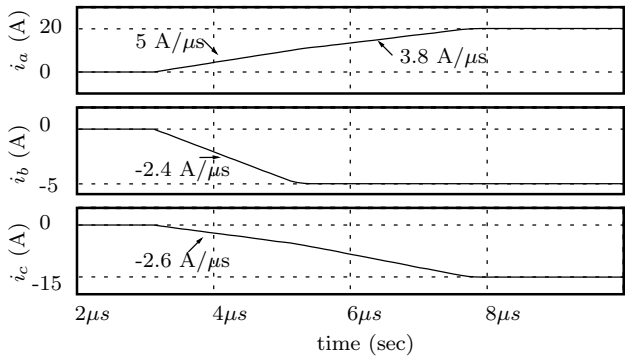


Figure 3.12: Zero to active vector simulation results (t_{za1})

Table 3.4: Simulation results

Value	Simulation	Calculation
P_{clamp}	135.5 W	139.4 W
$t_{az1} = t_{za2}$	8.05μ sec	7.95μsec
$t_{za1} = t_{az2}$	4.62μ sec	4.61μ sec

Table 3.5: Simulation parameters: Three-phase system

V_i, V_o, V_{clp}	100V, 30V, 500V
ω_i, ω_o	$2\pi 60$ rad/sec, $2\pi 60$ rad/sec
Output power	1kW
Load pf.	0.8
L	12 μH

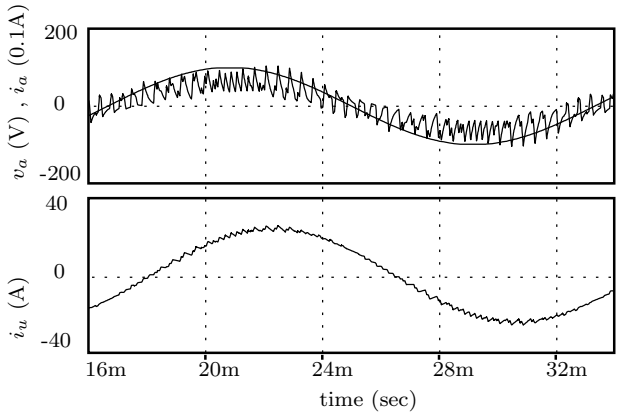


Figure 3.13: Three-phase AC-AC PET(1kW, 0.8 pf)

3.4.2 Three-phase AC-AC case for same frequency

A 1kW three-phase AC-AC system in Fig. 3.1 is simulated with the parameters listed in Table 3.5. Where V_i and V_o are the peak values of input and output balanced three-phase voltages respectively. The matrix converter is controlled using the technique described in section 2.2. Using this method, unity power factor is obtained on the primary side. The input voltage and filtered input current for phase a and current for phase u are plotted in Fig. 3.13. The worst case clamp power loss according to the analysis is 81.154 W (8.12 %) and the least clamp power loss is 17.68 W (1.768 %). The clamp power loss from simulation equals 79.89 W (7.99 %). The peak output voltage from simulation is 26.22 Watts, that corresponds to a voltage loss of 3.78 V. This is below the worst prediction of 10.27 V for voltage loss.

3.4.3 Three-phase variable frequency AC

The same 1kW system is simulated for a reference output voltage of 30V, 120 Hz. The output current and filtered input current along with input voltage for one phase are plotted in Fig. 3.14. The simulated values of power loss and voltage loss are within the calculated limits.

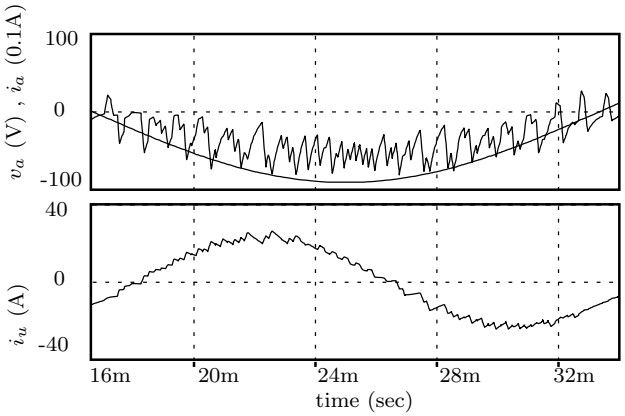


Figure 3.14: 1kW, 0.8 pf, three-phase variable frequency 60Hz - 120Hz

3.5 Experimental results

The experimental setup shown in Fig. 3.15 can be used to test the active vector to zero vector transition as well as the zero vector to active vector transition. The matrix converter is switched between vectors (ABC) and (AAA). Pulses p_1 and p_2 in Fig. 3.15 are generated in the FPGA and have a frequency of $f_s = 1000Hz$ and 50% duty. A dead-time (t_{dt}) of 1.5μ sec is introduced between the pulses p_1 and p_2. Switches S_{Av}, S_{Aw} are provided pulses p_1 and switches S_{Bv}, S_{Cw} are provided pulses p_2. S_{Au} is provided pulses $p_1||p_2$. The input voltages are supplied by two regulated DC supplies connected in series. By changing the DC voltages, two distinct sectors can be observed, one when two out of three-phase currents are positive and the other when only one phase current is positive. The f are in Table. 3.6. The inductance is made larger than in a high-frequency transformer so as to better observe the transitions. The clamp voltage V_{clp1} is set to 80V using a regulated DC supply.

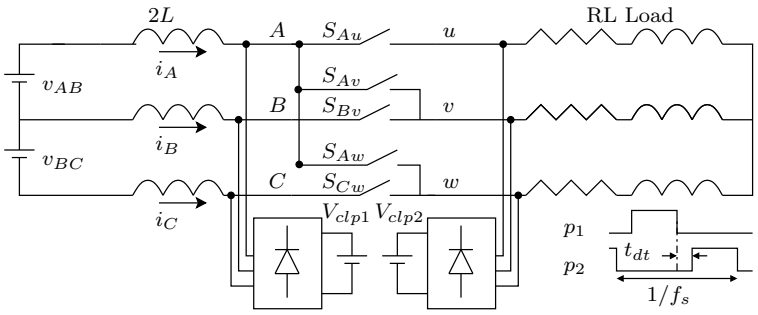


Figure 3.15: Experimental setup for active to zero vector transition

Table 3.6: Experimental setup: Parameters

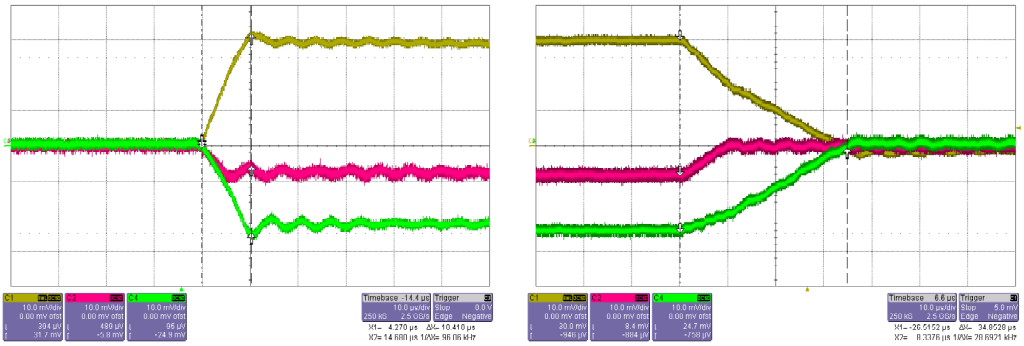
V_{AB}, V_{BC}	33V, 10V(Sector 1); 10V, 33V(Sector 2)
f_s	1kHz
RL Load	6.6Ω, 51.3mH
2L	500μH
V_{clp1}	80V

The currents through the input inductance, i_A, i_B and i_C are measured and compared with simulation in PLECS®. The simulation and experimental results in Sector 1 are in Fig. 3.16. The simulation and experimental results when the current is in Sector 2 are in Fig. 3.17. These results for a zero vector to active vector transition for Sector 1 and 2 are summarized in Table. 3.7. The simulation and hardware results for an active vector to zero vector transition are in Table. 3.8.

It can be seen that the transition times and the currents from the experimental setup and the simulation concur. A dead-time is implemented when switching from one vector to another, hence the load side clamp circuit, V_{clp2} is active every switching transition to conduct the load currents.

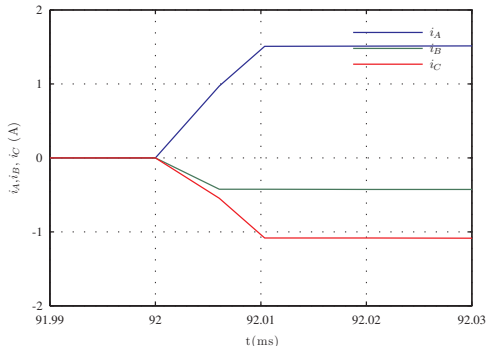
3.6 Comparison of dead-time commutation and four-step commutation

In this chapter, the commutation of transformer leakage inductance currents has been discussed. For an active vector to zero vector transition, this analysis assumes that a

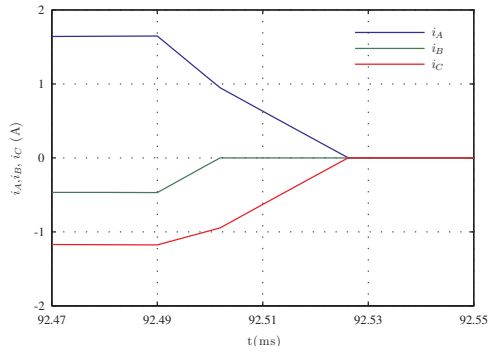


(a) Zero to active vector (10μs/div)

(b) Active to zero vector (10μs/div)



(c) Zero to active vector (10μs/div)

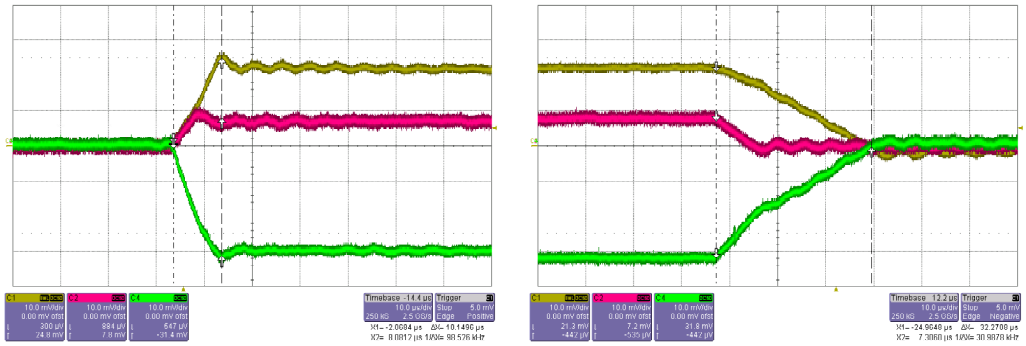


(d) Active to zero vector (20μs/div)

Figure 3.16: Zero to active vector transition in Sector 1 (a) hardware (0.5A/div) (c) simulation; Active to zero vector transition in Sector 1 (b) hardware(0.5A/div) (d) simulation.

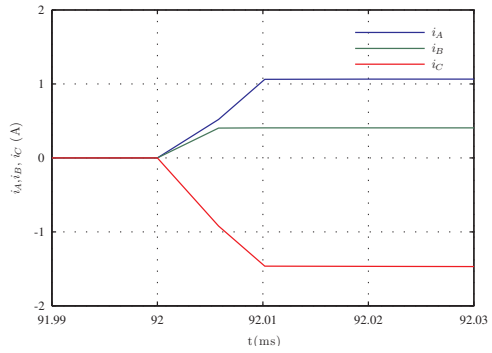
Table 3.7: Experimental results: Zero to active vector transition

	Sector 1		Sector 2	
Parameter	Hardware	Simulation	Hardware	Simulation
i_A (A)	1.5	1.51	1.24	1.08
i_B (A)	-0.4	-0.43	0.39	0.43
i_C (A)	-1.1	-1.08	-1.57	-1.51
t_1 (μs)	6.66	6.07	4.97	6.07
$t_1 + t_2$ (μs)	10.41	10.36	10.14	10.36

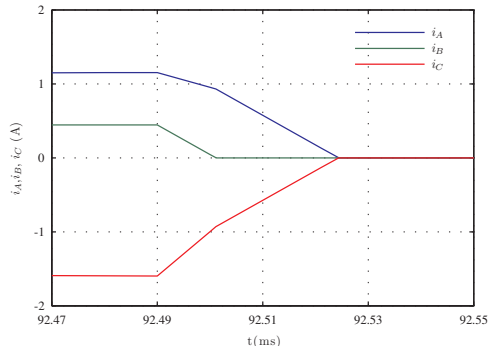


(a) Zero to active vector (10μs/div)

(b) Active to zero vector (10μs/div)



(c) Zero to active vector (10μs/div)



(d) Active to zero vector (20μs/div)

Figure 3.17: Zero to active vector transition in Sector 2 (a) hardware (0.5A/div) (c) simulation; Active to zero vector transition in Sector 2 (b) hardware(0.5A/div) (d) simulation.

Table 3.8: Experimental results: Active to zero vector transition

	Sector 1		Sector 2	
Parameter	Hardware	Simulation	Hardware	Simulation
i_A (A)	1.5	1.65	1.07	1.17
i_B (A)	-0.42	-0.47	0.36	0.47
i_C (A)	-1.235	-1.18	-1.59	-1.65
t_1 (μs)	11.439	11.91	9.63	11.91
$t_1 + t_2$ (μs)	34.85	36.18	32.27	36.18

zero vector has been applied in the matrix converter. For a zero vector to active vector transition, it assumes that the active vector has been applied in the converter. However, power electronic devices have finite turn-on and turn-off times, hence commutation of switches in the matrix converter needs to be considered.

In Matrix converters, commutation of switches is done either using dead-time or four-step commutation. Four-step commutation is a well known method for commutation of four-quadrant switches in a matrix converter when the input is a voltage port and the output a current port [59]. In [15] four-step commutation is implemented in a PET that satisfies this condition. The input as well as output ports of the MC in Fig. 3.1 are inductive in nature. A comparison of dead-time commutation and four-step commutation for the MC based PET in Fig. 3.1 for Carrier Based Modulation as well as Space Vector Modulation is presented in this section.

3.6.1 Simulation results

In order to analyze the benefits of four-step commutation, the circuit in Fig. 3.18 is simulated in PLECS®for three transitions: active vector (ABC) to active vector (BCA), active vector (ABC) to zero vector (AAA) and zero vector (AAA) to active vector (ABC) transition. The input phase voltages V_{AB} and V_{BC} are set to 30V and 40V respectively. The inductors $2L = 15\mu H$ represent the equivalent leakage inductance of the high-frequency transformer. The output currents are set to 10A, 5A and -15A for phase u, v, and w respectively. The four steps of the commutation process occur at time 4, 6, 8 and 10 μs. For dead-time commutation, t_{dt} lasts from 4 μs to 10 μs. Consider the transition from vector (ABC) to (BCA) as shown in Fig. 3.19(a) and 3.19(b). The blue, green and red waveforms are for phase a, b and c respectively. If dead-time commutation is implemented, the input side clamp (i_{a1}, i_{b1}, i_{c1}) circuit is operational for the time required to commutate the currents to zero at the start of the dead-time. As shown in Fig. 3.19(a), the output side clamp circuit (i_{a2}, i_{b2}, i_{c2}) is operational for the entire dead-time t_{dt} in addition to the time required to commutate the currents once (BCA) is applied in the converter. If four-step commutation is implemented, when the correct switch in the incoming branch is turned on, the phase currents commutate naturally if the voltage polarity is correct. When the outgoing branch is completely turned off at 8μs, the remaining currents commutate and reach their desired values. Clamp currents

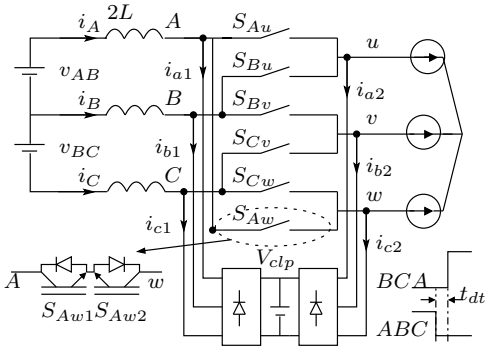


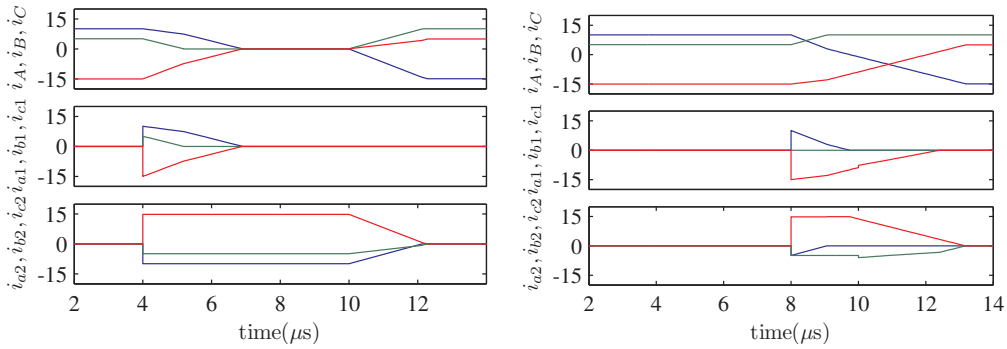
Figure 3.18: Simulation circuit for a transition from (ABC) to (BCA)

flow for an interval (t_{com}) to help with the commutation process as shown in Fig. 3.19(b). The value of t_{com} is a function of $2L, V_{clp}$ and input voltages. The simulation results for an active vector (ABC) to zero vector (AAA) transition as well as for a zero vector (AAA) to active vector (ABC) transition for dead-time and four-step commutation are given in Fig. 3.19(c), 3.19(e) and 3.19(d), 3.19(f) respectively.

During the dead-time, all the load current flows through the output clamp circuit. Hence the clamp voltage, V_{clp} appears across the load voltage terminals. This leads to a reduction in the output voltages seen by the load as well as voltage distortion. The maximum clamp voltage seen between any two phases is $\pm V_{clp}$. This voltage appears 4 times every switching cycle when SVM is used and 6 times when CBM is used. Neglecting the voltage loss associated with t_{com}, the maximum loss in line to line output voltage due to a dead-time of t_{dt} for a switching frequency of f_s is $4t_{dt}f_sV_{clp}$ V per phase when SVM is used and $6t_{dt}f_sV_{clp}$ V when carrier-based modulation is used (worst case with 6 vectors transitions each cycle). It is concluded that dead-time commutation will lead to excessive loss in output voltage, voltage distortion, as well as power loss.

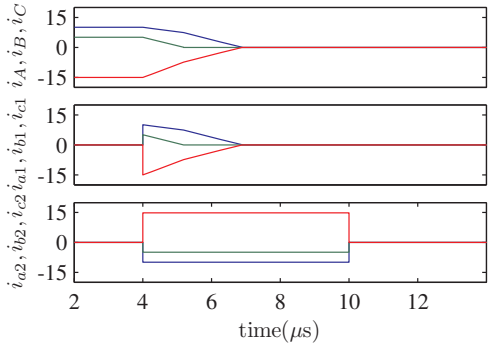
3.6.2 Experimental results

The parameters for the experimental results are listed in Table 3.9. The experimental results when CCW and CW vectors are used for equal duration when CBM is employed with dead-time and four-step commutation are in Fig. 3.20(a) and 3.20(b) respectively. The experimental results when SVM is employed with dead-time commutation and four-step commutation are in Fig. 3.20(c) and 3.20(d) respectively.

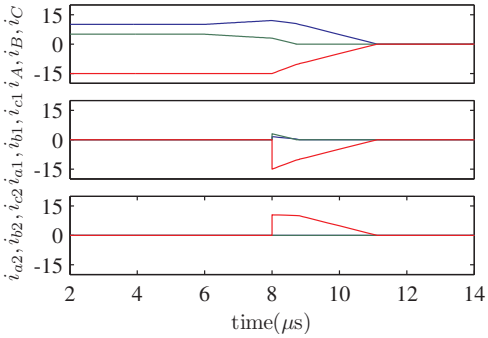


(a) Active vector to active vector

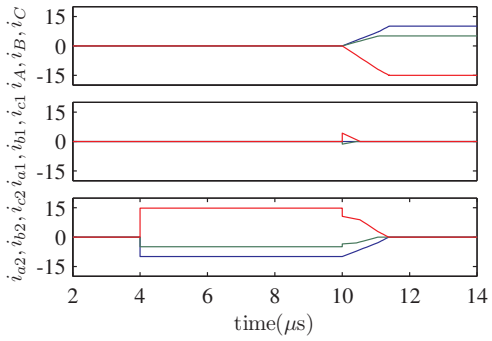
(b) Active vector to active vector



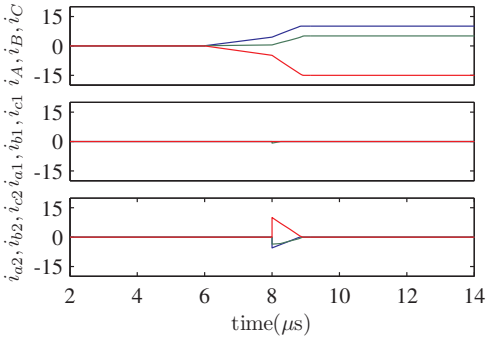
(c) Active vector to zero vector



(d) Active vector to zero vector

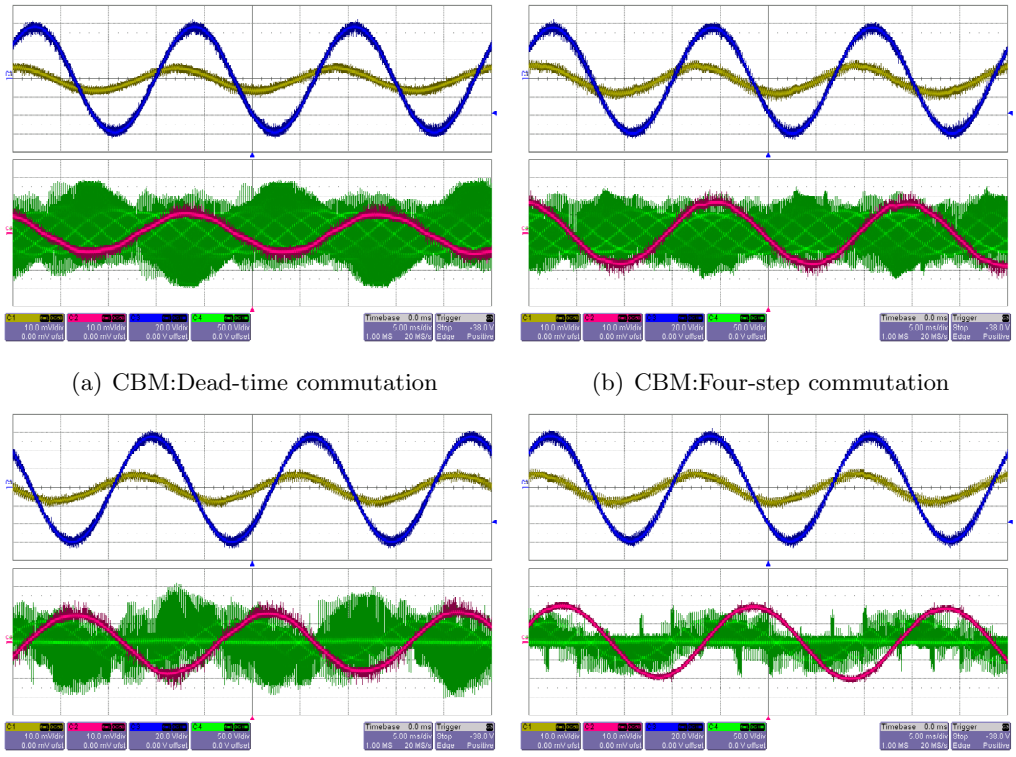


(e) Zero vector to active vector



(f) Zero vector to active vector

Figure 3.19: Comparison of dead-time and four-step commutation: with (a), (c), (e) dead-time commutation; (b), (d), (f) four-step commutation.



(a) CBM:Dead-time commutation

(b) CBM:Four-step commutation

(c) SVM:Dead-time commutation

(d) SVM:Four-step commutation

Figure 3.20: Experimental results using CCW and CW vectors for equal duration: Carrier based modulation with (a) dead-time and (b) four-step commutation; Space Vector Modulation with (c) dead-time and (d) four-step commutation. (top) Input voltage v_{an_i} (C3: 50V/div) and current i_{af} (C1:1A/div); (bottom) output voltage v_{un_o}(C4:50V/div) and current i_u (C2:1A/div), time (5ms/div).

Table 3.9: Experimental parameters: Comparison of commutation techniques

V_i, V_o	$40\sqrt{2}$V , 22.23V
ω_i ,ω_o ,f_s	2π60 rad/s, 2π50 rad/s, 10kHz
R, L , L_f, C_f	5.5Ω , 25mH , 0.5mH, 20μF(star)

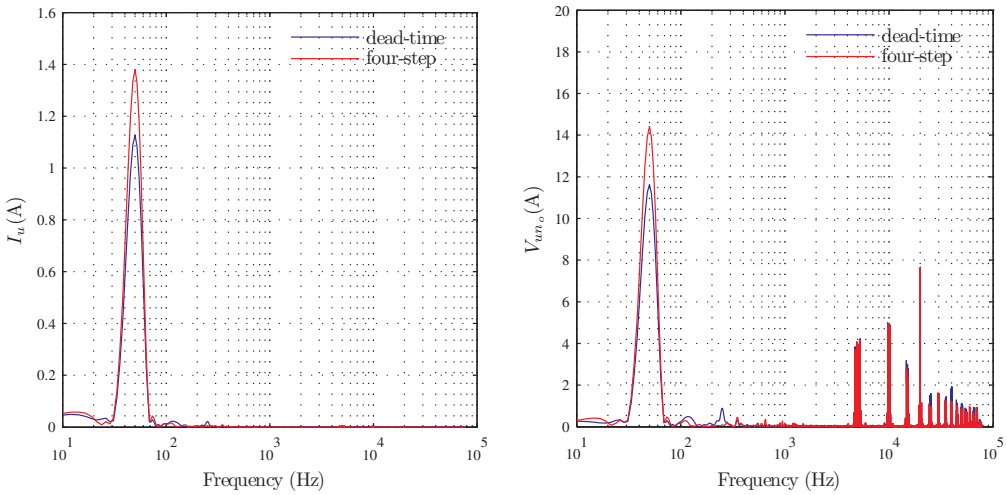
When the load is not connected, the fundamental component of output line-neutral voltage is 16.03V. When the PET is loaded, the observed line-neutral voltages are listed in Table. 3.10. When dead-time commutation is employed the worst case voltage loss expected when CBM is used is 11.4V for a clamp voltage of around 190V. The observed voltage loss is less than that and equals 8.4V. When SVM is employed, the worst case expected voltage loss is 7.6V and the observed loss is 4.5V. The maximum voltage is observed when SVM is applied with four-step commutation. As four-step commutation is suspended when the current direction is not accurately known, there is some voltage loss of 1.65V associated with it. At higher currents, four-step commutation is possible for a higher percentage of time, leading to better voltage profiles. When four-step commutation is used with carrier based modulation, there is a voltage loss of 3.67V. This is because there are six switching transitions as compared to four switching transitions per cycle when SVM is used.

The Fourier spectrum of the output current for phase u for SVM is in Fig. 3.21(a). It is observed that the component of output current at the fundamental frequency is higher for four-step commutation (1.38A) as compared to dead-time commutation (1.12A) when SVM is used. The Total Waveform Distortion (TWD) is given by (3.21). The TWD for I_u when dead-time commutation is used is 5.61% and when four-step commutation is used is 4.4%. The Fourier spectrum of the output voltage, v_{un_o} is in Fig. 3.21(b). It is observed that the fundamental component of the output voltage is higher when four-step commutation is used. The output voltage contains harmonics at the fundamental frequency, at 5kHz (because CCW and CW vectors are used) as well as harmonics at the switching frequency of 10kHz. In conclusion, four-step commutation leads to better output TWD, lesser power loss in the clamp circuit and consequently better efficiency.

$$TWD = \frac{\sqrt{I_{rms}^2 - I_{f1}^2}}{I_{f1}} \tag{3.21}$$

Table 3.10: Comparison of modulation and commutation

	CBM dead-time	CBM four-step	SVM dead-time	SVM four-step
V_{un_o} RMS (V)	7.60	12.36	11.53	14.38
I_u RMS (A)	0.74	1.19	1.12	1.38
TWD i_u %	6.75	4.83	5.61	4.40



(a) I_u (SVM)

(b) V_{un_o} (SVM)

Figure 3.21: Fourier spectrum of output current and voltage

3.7 Conclusions

In this chapter, the secondary side clamp circuit requirement is studied and a detailed analysis of its operation is done. The lower and upper limit of power loss associated with the leakage energy commutation using a clamp circuit is calculated and these values concur with the simulated values. The following conclusions can be drawn,

1. The secondary clamp voltage must be greater than three times the peak line to neutral voltage.

2. The clamp circuit is operational every time the load side converter is switched.

3. For $V_{clp} = 5 \times V_i$, the power loss associated with it is between $4.46 f_s L I_o^2$ and

$9.18 f_s L I_o^2$ Watts.

4. For $V_{clp} = 5 \times V_i$, the maximum time required for commutation can be upto $1.06 \times LI_o/V_i$ sec .

5. Zero to active vector transitions and dead-time in the load side converter lead to distortion in the output voltage waveform.

6. This research proves that even though the MC has leakage inductance on the input port, four-step commutation instead of dead-time commutation leads to better voltage profile and consequently better output currents. It also leads to improved efficiency of the PET.

The results of this analysis can be used to design the resistive and capacitive components for the clamp circuit. This analysis is very general and can be further extended to the clamp circuit operation in any other relevant topologies.

Note: Parts of this chapter have been reprinted from [36] ©2010 IEEE and [60]

Chapter 4

Single-Phase AC-DC Power Electronic Transformer

The switching frequency in high-frequency transformer (HFT) isolated AD-DC converters is limited by the device stress, switching losses and commutation time for leakage energy. Hence, converters having soft-switching characteristics are being explored.

Dual Active Bridge Converters (DABC) are a class of high-frequency transformer-isolated converters that have inherent qualities of soft switching, low device stress, small filter requirements and use of the HFT inductance for power transfer. These make them suitable for applications requiring high power density. DABC was introduced for DC-DC power conversion in [51, 52]; In this converter, two square-wave voltages are phase shift modulated (PSM) to control the power flow across the leakage inductance of the transformer. When the input and output voltages are not the same value, the soft switching range of PSM DABC is limited. New modulations methods, where one or both the converters are duty-ratio modulated (PWM) were proposed to extend this soft switching range [61]. These PWM techniques can be categorized into inner mode, outer mode, Trapezoidal and Triangular current modulation [62–67]. Triangular current mode modulation is used when the input and output voltages are not equal; this strategy results in maximum ZVS/ZCS at the cost of high RMS currents [68]. In trapezoidal current modulation, low RMS currents are obtained in the transformer and higher power transfer is possible compared to triangular current modulation. Triangular current

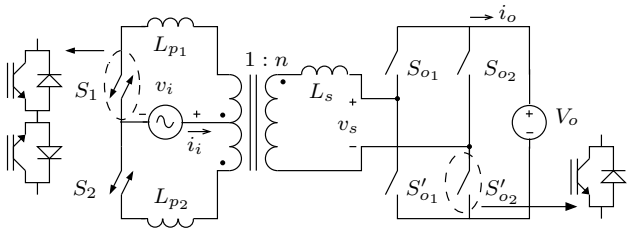


Figure 4.1: Single-phase AC-DC PET

mode modulation is a special case of the 'inner mode' of operation. The 'inner mode' of operation is characterized by limiting the PWM pulses of the high voltage side converter to be contained within those of the low voltage side converter. It is possible to obtain ZCS in the low voltage side converter in this mode of operation. Single-phase AC-DC converters based on DAB principle have been proposed in [69–72].

In this chapter, a control method for a single-phase AC-DC converter (PET) (shown in Fig. 4.1) that is based on the 'inner mode' DAB principle is proposed that simultaneously has the following features: a) galvanic isolation, b) bi-directional power flow, c) ZCS for the primary side switches and ZVS turn-on for the secondary side switches, d) linear power relationship for easy control implementation, e) unity power factor under open-loop control and f) single-stage power conversion. In order to analyze the single-phase AC-DC converter, first, the 'inner mode' of operation for a DC-DC DABC with the primary switches in push-pull topology is analyzed in section 4.1.1. This analysis is extended to single-phase AC-DC converter in section 4.1.2. In section 4.2, the simulation results in SABER®are compared with the theoretical analysis. The experimental results for the DC-DC converter and single-phase AC-DC converter are compared with the simulation results in section 4.4 and 4.5 respectively.

4.1 Topology and modulation

An AC-DC Dual Active Bridge Converter (DABC) with the primary side in push-pull configuration is shown in Fig. 4.1. An AC voltage source $v_i = \hat{V}_i \sin(\omega t)$, where $\omega = 2\pi f$ is connected to the primary of a three-winding high-frequency transformer and a DC voltage source V_o is connected to the secondary of the high-frequency transformer through a H-bridge inverter. The turns-ratio of one half of the primary winding to the

secondary winding of the transformer is $1:n$. In the following analysis, it is assumed that $V_o \geq n\hat{V_i}$. The leakage inductances of the two primary windings are L_{p_1} and L_{p_2} and that of the secondary winding is L_s. The primary side switches S_1 and S_2 are four-quadrant. They are switched at 50% duty-ratio in a complementary way at a switching frequency of $f_s(=\frac{1}{T_s})$. If the leakage inductance of the two primary windings are identical, $L_{p_1} = L_{p_2} = L_p$, and the magnetizing current is neglected, the equivalent circuit of the converter system seen from the secondary side of the transformer is shown in Fig. 4.2 where, $L = n^2L_p + L_s$. The voltage v_p is $+nv_i$ when S_1 is on and is $-nv_i$ when S_2 is on. In one switching cycle, the net volt-sec applied to the transformer is zero; thus, the flux in the transformer core is balanced in the modulation technique described below. The secondary side switches S'_{o_1} and S'_{o_2} are switched complementary to S_{o_1} and S_{o_2} respectively. The voltage v_s can be controlled to be $+V_o$, $-V_o$ or 0.

4.1.1 Analysis of DC-DC converter

In a DC-DC DABC, the input voltage in Fig. 4.1 is constant at V_i. The switches S_1 and S_2 can be two-quadrant. The secondary side converter is pulse-width modulated with a duty-ratio given by (4.1). A phase shift of $\delta\frac{T_s}{2}$ is introduced between the voltages v_p and v_s to obtain power transfer (Fig.4.3 (a)). In the 'inner mode' of operation, the absolute value of δ is limited by (4.2) [67]. This modulation technique ensures that the average voltage applied across the inductor is zero every $T_s/2$ and the switches S_1 and S_2 are switched at zero current, thus reducing the switching losses considerably. An added advantage being a snubber circuit is no longer necessary for these switches. The inductor current i_L, i_o and i_i are shown in Fig. 4.3 (c), (d) and (e) respectively.

$$d = \frac{nV_i}{V_o} \tag{4.1}$$

$$0 \leq |\delta| \leq (1-d)\frac{1}{2} \tag{4.2}$$

Each half cycle $(T_s/2)$ is divided into three time intervals, t_1, t_2 and t_3 given by (4.3). The current in the inductor during these time intervals is given by, (4.4),(4.5) and (4.6). Solving equations (4.1)- (4.6), the values of I_0 and I_3 equal zero (eq. (4.7)).

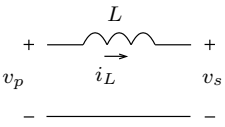


Figure 4.2: Equivalent circuit of single-phase AC-DC converter

$$t_1 = \frac{T_s}{4} + \delta\frac{T_s}{2} - d\frac{T_s}{4}$$
$$t_2 = d\frac{T_s}{2}$$
$$t_3 = \frac{T_s}{2} - t_1 - t_2 \tag{4.3}$$
$$I_1 = I_0 + \frac{nV_i}{L}t_1 \tag{4.4}$$
$$I_2 = I_1 + \frac{(nV_i - V_o)}{L}t_2 \tag{4.5}$$
$$I_3 = I_2 + \frac{nV_i}{L}t_3 \tag{4.6}$$
$$I_0 = I_3 = 0 \tag{4.7}$$

The secondary side converter can be modulated by two switching strategies; in the first case (Fig. 4.3 (a)), the zero voltage is applied by turning on S'_{o_1} and S'_{o_2}. In the second method (Fig. 4.3 (b)), the zero voltage is applied either by S_{o_1} and S_{o_2} or by S'_{o_1} and S'_{o_2}; this method has an advantage that the secondary side pulses are square wave. A dead-time is introduced between the transition of switches in the same leg. The switches in the secondary side turn on under ZVS condition as anti-parallel diodes are conducting when these switches are turned on. This condition is true for any direction of power flow. The voltage, current and power bases are selected as (4.8). The average power supplied is calculated to be (4.10). A maximum power of 0.233 pu can be transferred using this converter when $d = 2/3$. Due to the constraints on phase shift δ, the power transferred in the inner mode of operation is lesser than a PSM

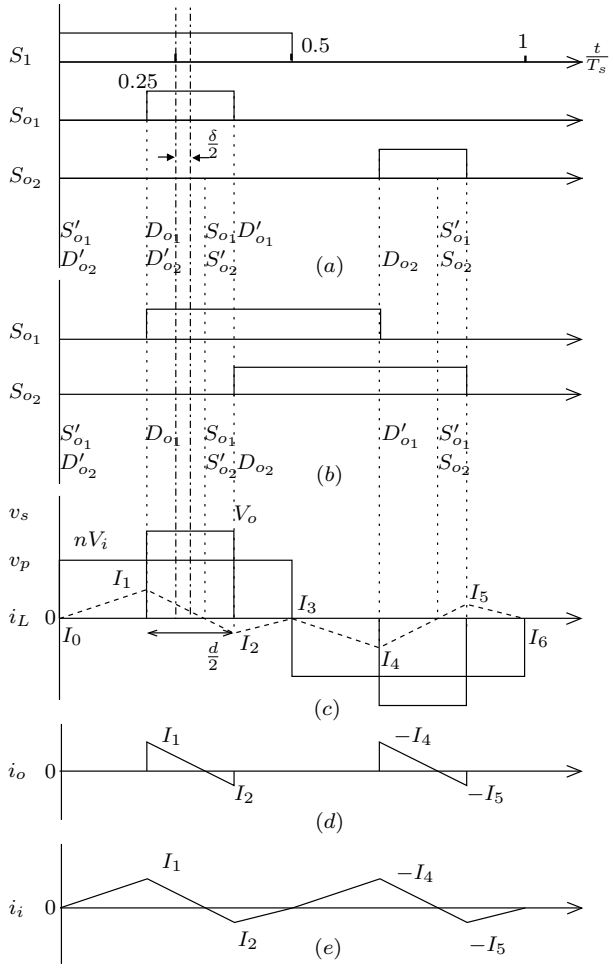


Figure 4.3: Switching waveforms for DC-DC converter

DABC [51](0.523 pu at d=2/3).

$$\left.\begin{aligned} V_{base} &= V_o \\ I_{base} &= \frac{V_o}{2\pi f_s L} \\ P_{base} &= \frac{V_o^2}{2\pi f_s L} \end{aligned}\right\} \tag{4.8}$$

$$P_o = \left(V_o \frac{2}{T_s}\right)\left(\frac{I_1 + I_2}{2}\right) t_2 \tag{4.9}$$

$$\begin{aligned} P_{io} &= \delta d \frac{n V_i V_o}{2 L f_s} = \delta d^2 \frac{V_o^2}{2 L f_s} \\ &= \delta d^2 \pi \qquad \cdots \text{in pu} \end{aligned} \tag{4.10}$$

The per-unit (pu) RMS currents in the transformer are calculated to be (4.11) and (4.12). The primary and secondary RMS voltages are calculated in (4.13) and (4.14) respectively. Using these values the transformer per-unit VA can be calculated as (4.15). The per-unit values of P_t are plotted as a function of P_{io} in Fig. 4.4. A transformer per-unit VA of $P_t = 0.299$pu is required to transfer the maximum power of 0.233pu, which corresponds to a transformer utilization (P_{io}/P_t) of 0.779, This is higher than the transformer utilization (0.636) for maximum power transfer at the diode bridge boundary for topology B in [51].

$$\overline{I}_{L_s} = K\sqrt{(1 - 2d + d^2 + 12\delta^2)d^2} \tag{4.11}$$

$$\text{where,} \qquad K = \frac{2\pi}{4\sqrt{3}}$$

$$\overline{I}_{L_{p_1}} = \overline{I}_{L_{p_2}} = \frac{\overline{I}_{L_s}}{\sqrt{2}} \tag{4.12}$$

$$\overline{V}_p = \frac{d}{\sqrt{2}} \tag{4.13}$$

$$\overline{V}_s = \sqrt{d} \tag{4.14}$$

$$\begin{aligned} P_t &= \frac{1}{2}[2\overline{V}_p \overline{I}_{L_p} + \overline{V}_s \overline{I}_{L_s}] \\ &= \frac{1}{2}(d + \sqrt{d})\overline{I}_{L_s} \end{aligned} \tag{4.15}$$

The size of the DC-side filter capacitor is a function of the RMS ripple current through it. The per-unit value of the RMS ripple current through the DC capacitor, $\overline{I}_{rpl}$ is given

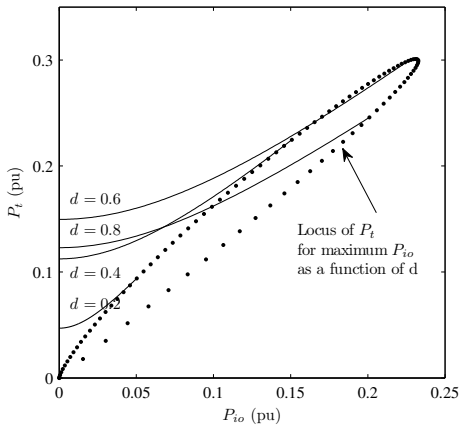


Figure 4.4: DC-DC Converter: P_t Vs P_{io}

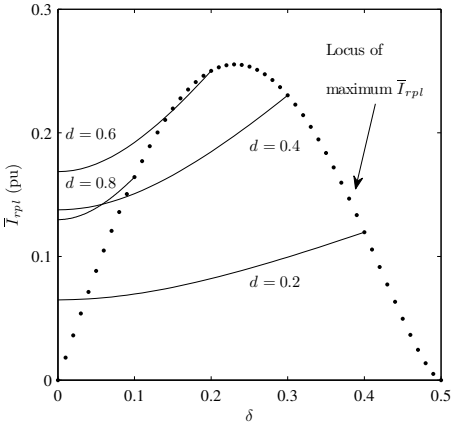


Figure 4.5: DC-DC Converter: $\overline{I}_{rpl}$ Vs δ

by (4.17). In Fig. 4.5, the worst case ripple equals 0.256 pu at δ of 0.23 (d=0.54).

$$\overline{I}_o = K\sqrt{(1 - 2d + d^2 + 12\delta^2)d^3} \tag{4.16}$$

$$\overline{I}_{rpl} = K\sqrt{(1 - 2d + d^2 + 12\delta^2(1 - d))d^3} \tag{4.17}$$

4.1.2 Analysis of single-phase AC-DC converter

Consider a single-phase phase AC-DC converter in Fig. 4.1. As $f_s \gg f$, in one switching cycle, the input voltage can be approximated as a DC voltage. In the positive half cycle, the ZCS conditions for the primary side switches are satisfied when the output side converter is modulated with a duty ratio of (4.18). In the negative half cycle, the pulses for S_{o_1} and S_{o_2} are interchanged. The duty ratio d of the secondary side converter varies with time, hence the maximum value of δ also varies with time (4.19). Selecting a constant value of δ ensures unity power factor on the AC side. For a given value of

m, $|\delta|$ is constrained by (4.20).

$$d(t) = m|\sin(\omega t)| \qquad \cdots \; m = \frac{n\hat{V}_i}{V_o} \tag{4.18}$$

$$0 \leq |\delta| \leq \frac{1}{2}(1 - d(t)) \tag{4.19}$$

$$0 \leq |\delta| \leq \frac{1}{2}(1 - m) \tag{4.20}$$

The instantaneous power transferred (4.21) is obtained by replacing V_i and d in (4.10) by $\hat{V}_i \sin(\omega t)$ and (4.18) respectively. From the definition of input power, the switching-cycle averaged input current ($\tilde{i}_i(t)$) can be calculated as (4.22). Under open-loop control, the switching-cycle averaged input current is in phase with the input voltage and unity power factor is obtained. The average power, P_{avg} is calculated by integrating the instantaneous power over one fundamental cycle of the input voltage. The following inferences are made about P_{avg}: 1) The power flow has a linear relationship to δ this simplifies the control strategy where power flow can be bi-directional by changing the sign of δ. 2) As m increases, the range of δ reduces. 3) No power can be transferred when $V_o = n\hat{V}_i$. 4) The locus of maximum power that can be transferred is plotted by the dotted curve in Fig. 4.6. The maximum value of P_{avg} (0.116 pu) occurs when $m = 2/3$.

$$P(t) = \frac{\delta n^2 \hat{V}_i^{\,2}}{2Lf_s} \sin^2(\omega t) \tag{4.21}$$

$$\tilde{i}_i(t) = \frac{P(t)}{V_i(t)} = \frac{\delta n^2 \hat{V}_i}{2Lf_s} \sin(\omega t) \tag{4.22}$$

$$P_{avg} = \frac{1}{2\pi} \int_0^{2\pi} P(\omega t) d(\omega t) \tag{4.23}$$

$$\begin{aligned} P_{avg} &= \delta n^2 \frac{\hat{V}_i^{\,2}}{4Lf_s} = \delta m^2 \frac{V_o^2}{4Lf_s} \\ &= \frac{1}{2}\delta m^2 \pi \qquad \cdots \text{in pu} \end{aligned} \tag{4.24}$$

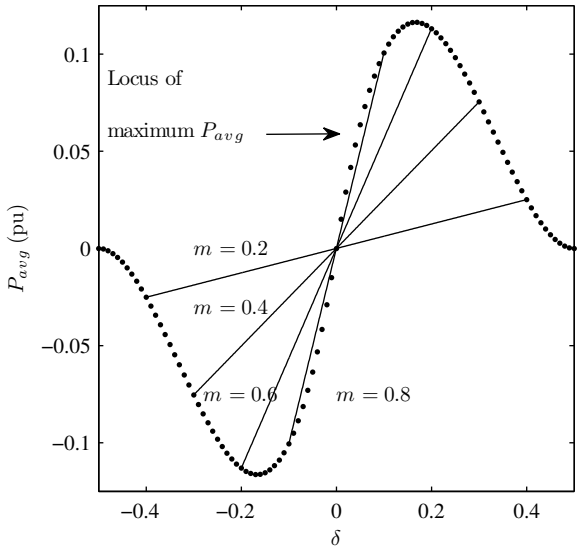


Figure 4.6: AC-DC Converter: P_{avg} Vs δ

$$\overline{I}_{L_s} = K'm\sqrt{9m^2\pi - 64m + 12\pi(1 + 12\delta^2)} \tag{4.25}$$

where, $K' = 0.1044$

$$\overline{I}_{L_{p_1}} = \overline{I}_{L_{p_2}} = \frac{\overline{I}_{L_s}}{\sqrt{2}} \tag{4.26}$$

$$\overline{V}_p = \frac{m}{2} \tag{4.27}$$

$$\overline{V}_s = \sqrt{\frac{2m}{\pi}} \tag{4.28}$$

$$\begin{aligned} P_t &= \frac{1}{2}[2\overline{V}_p\overline{I}_{L_p} + \overline{V}_s\overline{I}_{L_s}] \\ &= \frac{1}{2}\left(\frac{m}{\sqrt{2}} + \sqrt{\frac{2m}{\pi}}\right)\overline{I}_{L_s} \end{aligned} \tag{4.29}$$

The RMS currents in the transformer windings over one switching period are a function of $d(t)$ and are given by (4.11) and (4.12). The equation for the RMS currents through the transformer windings over one cycle of the input voltage (given by (4.25) and (4.26)) can be found by integrating the the square of (4.11) and (4.12) and determining root of the mean. The RMS values for the primary and secondary voltages are given by (4.27) and (4.28) respectively. The transformer per-unit VA rating is calculated by

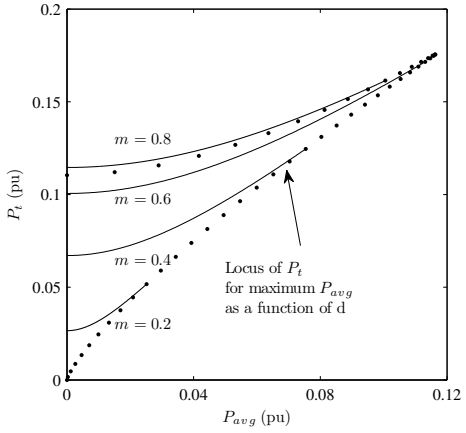


Figure 4.7: AC-DC Converter: P_t Vs P_{avg}

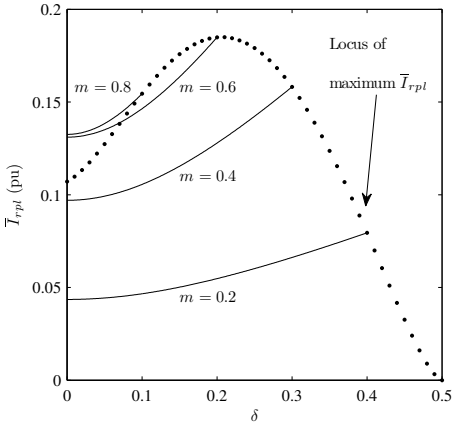


Figure 4.8: AC-DC Converter: $\overline{I}_{rpl}$ Vs δ

(4.29). The per-unit values of P_t are plotted as a function of P_{avg} in Fig. 4.7. The dotted curve marks the locus of maximum VA for the transformer for different values of P_{avg}. To transfer the maximum power (0.116 pu), the transformer VA required is 0.176, resulting in a transformer utilization of 0.663. This is the maximum utilization of the transformer. The RMS values for i_o and ripple current in the dc-capacitor given by (4.30) and (4.31) are calculated from (4.16) and (4.17) respectively. The per-unit values of the dc-capacitor current ripple is plotted for selected values of m as a function of δ in Fig. 4.8. The maximum value for $\overline{I}_{rpl}$ (0.185 pu) occurs when δ is 0.21(m=0.58) at a power transfer of 0.111 pu.

$$\overline{I}_o = K'' \sqrt{m^3(64m^2 - 45m\pi + 80(1 + 12\delta^2))} \tag{4.30}$$

$$\overline{I}_{rpl} = K'' \sqrt{m^3(64m^2 - 45m\pi - 270\pi\delta^2 m + 80 + 960\delta^2)} \tag{4.31}$$

where, $K'' = 0.0661$

4.2 Simulation results

The DC-DC converter in Fig. 4.1 is simulated in SABER®. The converter parameters are listed in Table 4.1. The waveforms for the current through S_1 and S_2 as well

Table 4.1: Simulation parameters

$V_i = \hat{V}_i$, V_o	40V, 200V
f_s ,f	5kHz , 60Hz
$L_{p_1} = L_{p_2} = L_s$	50μH
turns-ratio	1:1:1
δ	0.1

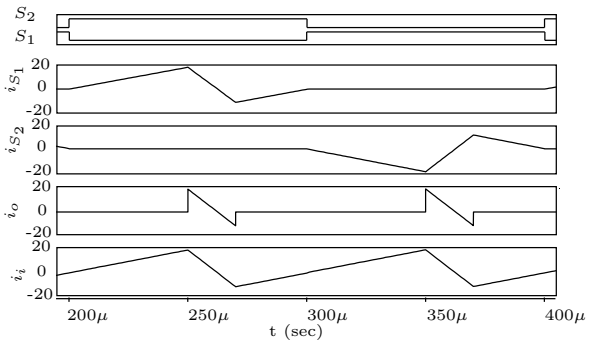


Figure 4.9: Simulation result: DC-DC converter

as the input and output currents are shown in Fig. 4.9. As these currents are zero at the transition of S_1 or S_2, zero switching for primary switches is confirmed. A single-phase AC-DC converter having parameters listed in Table 4.1 is also simulated in SABER®. In Fig. 4.10, the input voltage and filtered input current are in phase with each other, indicating that a unity power factor of operation is obtained. The calculated and simulated values for P_{io}, $\overline{I}_i$, $\overline{I}_o$ and $\overline{I}_{rpl}$ for both DC-DC and AC-DC converters match closely as listed in Table 4.2.

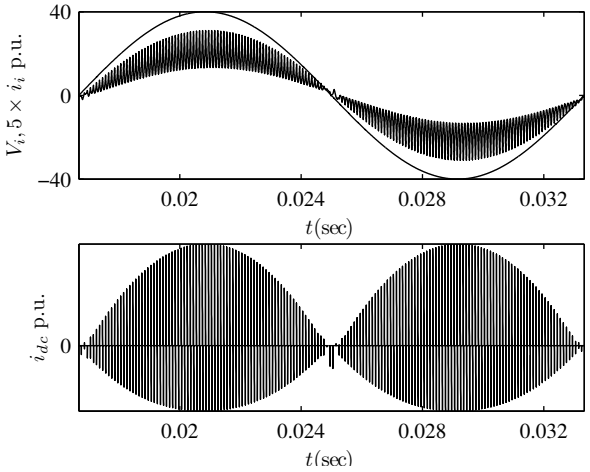


Figure 4.10: Simulation result: Single-phase AC-DC

Table 4.2: Comparison of simulation and analytical values

Parameter	Simulation (DC-DC)	Calculation (DC-DC)	Simulation (AC-DC)	Calculation (AC-DC)
P_{io}	158.81 W	160 W	79.51 W	80 W
$\overline{I}_i$(RMS)	10.12 A	10.06 A	7.27 A	7.35 A
$\overline{I}_o$(RMS)	4.53 A	4.50 A	2.96 A	3.01 A
$\overline{I}_{rpl}$(RMS)	4.46 A	4.43 A	2.93 A	2.97A

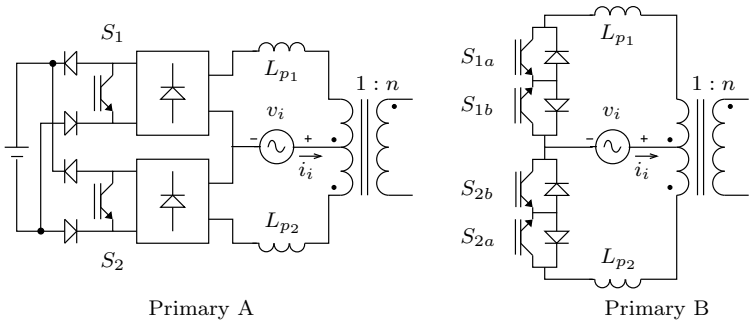


Figure 4.11: Primary side converter in push-pull topology

4.3 Experimental setup

In this AC-DC PET, the primary side switches need to be four-quadrant. It can be constructed in two distinct ways: 1) Primary A: Using a diode bridge and one controlled switch as shown in Fig. 4.11(a). 2) Primary B: Using common-emitter or common-collector four-quadrant switches shown in Fig. 4.11(b). Both these cases are identical in the ideal-case and the primary switches are switched at zero current. However, a real circuit has device drops, conduction loss, dead-times etc. and the current may not cross zero at the switch transitions. Hence, a clamp circuit will be required for Primary A.

In Primary B, source based commutation will be possible. Consider the positive half cycle of v_i, switches S_{1b} and S_{2b} are kept on and S_{1a} and S_{2a} are modulated at 50% duty ratio at high-frequency. Consider the input voltage is in the positive half cycle, and winding 1 was conducting when S_{1a} is turned off and there is a dead-time between before switch S_{2a} is turned on. If the current in the transformer winding is slightly positive, the diode in the lower winding, d_{2a} and S_{2b} will conduct the current and S_{2a} will have ZVS turn-on. If the current is slightly negative, the diode in upper winding, d_{1a} and S_{1b} will be conducting so that S_{1a} as well as S_{2a} will be ZCS. There is no need to sense the direction of the current for the modulation of these primary side switches only the polarity of the voltage is necessary. In the negative half cycle, switches S_{1a} and S_{2a} are kept on and S_{1b} and S_{2b} are modulated at 50% duty ratio at high-frequency. A comparison of Primary A and Primary B is given below.

- **Switching Loss** In Primary A, the primary switches may not attain ZCS. In

Primary B, in each switching transition, one of the switches achieves either ZVS or ZCS. Also, only 2 switches are modulated at high frequency, the other two are modulated at line frequency at the zero crossing on the line voltage, where the switching loss is low.

- **Conduction Loss**: In Primary A, the primary switch has two diodes and one switch, while in Primary B, the path is only one diode and one switch. Hence conduction losses are less.

- **Gate Driver**: In Primary A, only two gate drive circuits are required. In Primary B, four gate drive circuits are required however since common-emitter configuration is used, the number of isolated power supplies required for these gate drivers is only two.

In this chapter, Primary A configuration is used to test the DC-DC converter and the single-phase AC-DC converter. The schematic for the experimental setup is in Fig. 4.12. The picture of the experimental setup is in Fig. 4.13. L_f, C_f are the input filter for this converter. v_{pps} is the programmable power supply for the single-phase AC-DC converter and a regulated DC power supply is used for the DC-DC converter. R_i and R_o are load resistors that are used to sink the power. Additional inductance is added on the secondary side of the transformer to limit the amount of power transferred. The details of the experimental setup are in Appendix B. The PWM pulses for all the power semiconductor devices are generated using an FPGA. The details of FPGA implementation are in Appendix E.1.

4.4 Experimental results: DC-DC converter

The experimental parameters are listed in Table. 4.3. The magnitude of V_o is set to 100V and V_i is varied to obtain different values of d. The converter is run for different values of d and δ and the results are summarized in Fig. 4.14(a) for positive values of δ and in Fig. 4.14(b) for negative values of δ. The input and output currents, i_i and i_o respectively that are marked in Fig. 4.12 are measured using a current probe and the average values of input power $P_i = v_i \times i_i$ and output power $P_o = v_o \times -i_o$ are calculated from the scope data. The expected power P_{io} equals $\delta d^2 \frac{V_o^2}{2Lf_s}$ from (4.10).

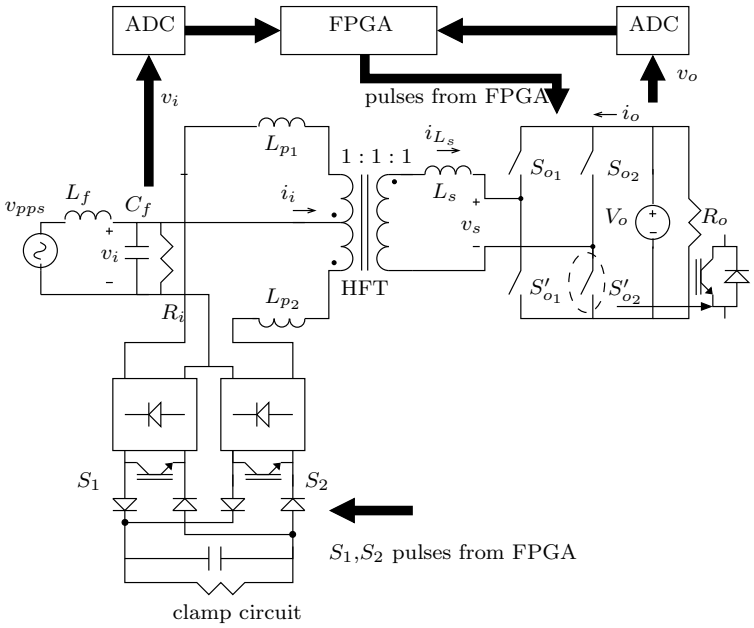


Figure 4.12: Single-phase AC-DC PET: Schematic of experimental setup

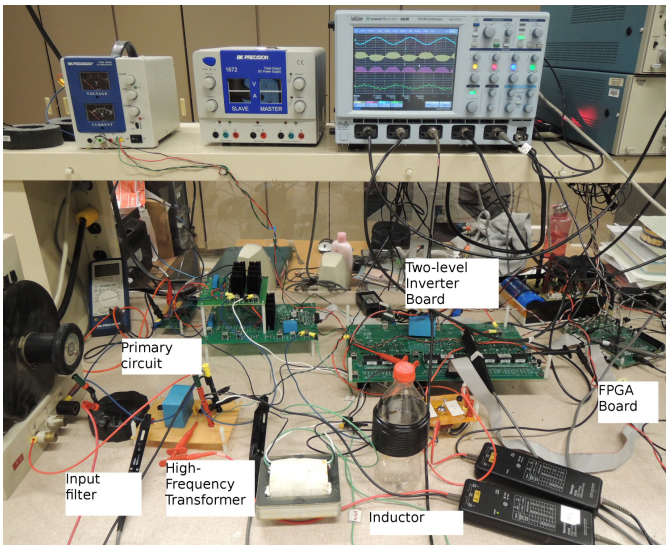
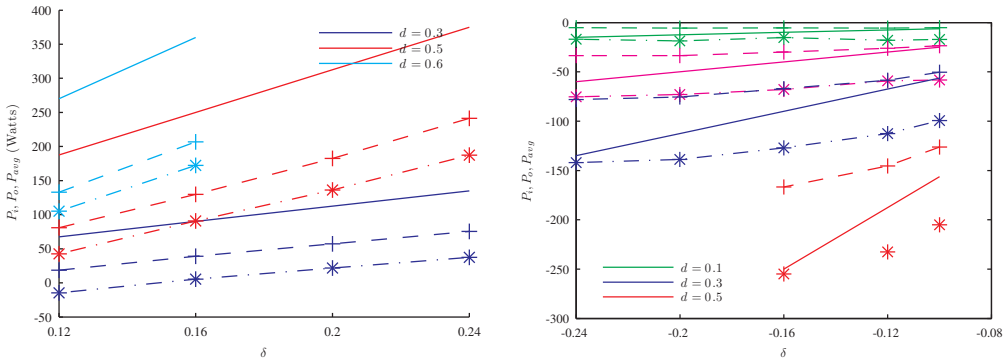


Figure 4.13: Experimental setup for DC-DC and single-phase AC-DC conversion

Table 4.3: Experimental parameters for DC-DC and single-phase AC-DC converter

V_o	100V
f_s ,f	10kHz , 60Hz
L_s	80μH
turns-ratio	1:1:1



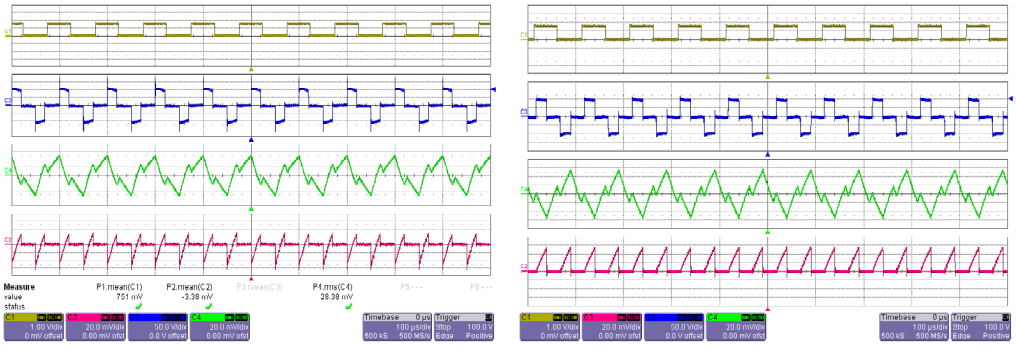
(a) δ is positive

(b) δ is negative

Figure 4.14: DC-DC converter: Expected power P_{io}, input power P_i(-+) and output power P_o(-.*) for different values of d and δ

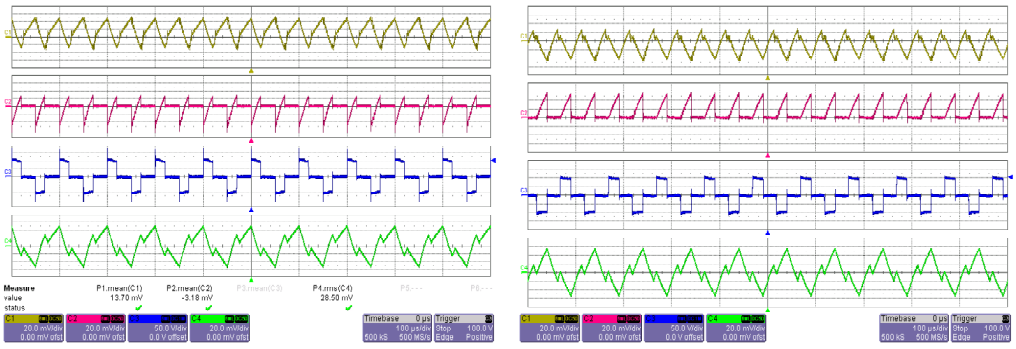
Bi-directional power flow capability of this converter has been demonstrated. For positive values of δ power flows from v_i to v_o and vice versa for negative δ. It is observed that for positive direction of power flow, P_i is higher than P_o and the opposite is true for negative power flow. This is because of the losses in the circuit.

The operating point with $V_i = 40$V and $\delta = \pm 0.2$ is selected for further study. The switching pulse for S_1 and the converter voltage v_s are shown in Fig. 4.15. For $\delta = 0.2$, v_s is shifted to the right with respect to the pulses for S_1. For $\delta = -0.2$, v_s is shifted to the left with respect to the pulses for S_1. The input and output currents as well as the inductor current are in Fig. 4.16. The currents through S_1 and S_2, are shown in Fig. 4.17. At the transition of S_1 and S_2 the currents through these switches are small but they are not ZCS.



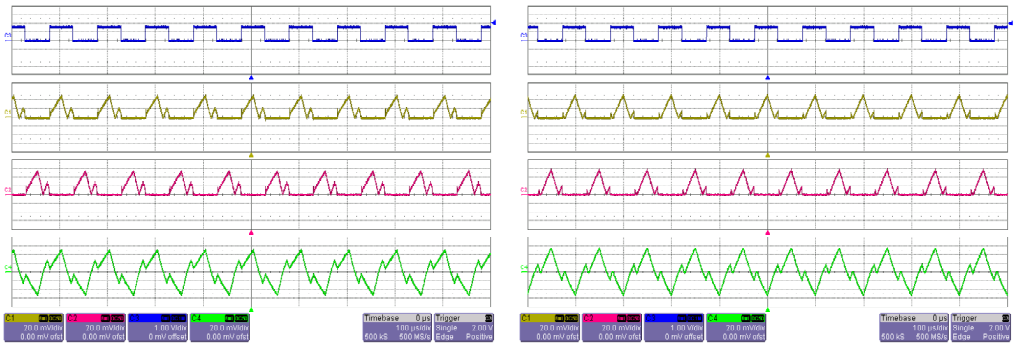
(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.15: DC-DC converter: (top to bottom) FPGA pulse for S_1 (C1:1V/div), voltage v_s (C3:50V/div) inductor current i_{L_s} (C4:4A/div) and output current i_o (C2:4A/div); time at 100μs/div.



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.16: DC-DC converter: (top to bottom) Input and output currents i_i (C1:4A/div) and i_o (C2:4A/div), voltage v_s (C3:50V/div) and inductor current i_{L_s} (C4:4A/div); time at 100μs/div.



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.17: DC-DC converter: (top to bottom) FPGA pulse for S_1 (C3:1V/div), Primary switch currents i_{S_1} (C1: 4A/div) and i_{S_2} (C2: 4A/div) and inductor current i_{L_s} (C4:4A/div); time at 100μs/div.

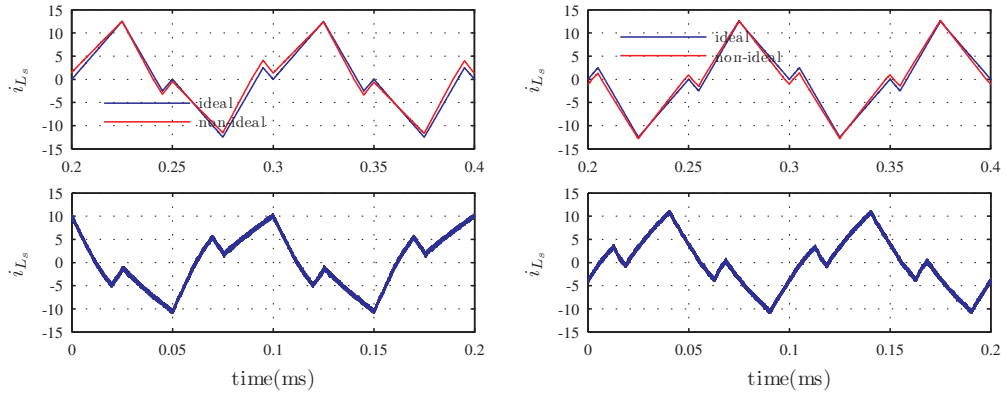
4.4.1 Effects of non-idealities in the circuit

In this topology, power flow is obtained by phase shifting the voltages across the effective leakage inductance of the transformer. This causes a change in the average value of the input and output currents. Power electronic devices have a finite resistance and voltage drop associated with them. Also, additional resistance/inductance is present in any circuit due to circuit layout. These non-idealities cause the converter currents and power flow to deviate from the ideal case. The converter is simulated in PLECS®for a non-ideal case with diode voltage drop of 2.5V, and IGBT device drop of 1.7V and a resistance of 1Ω in series with the inductance of the transformer (L_s). These simulation results are compared with an ideal case as well as with the hardware results in Fig. 4.18 and Fig. 4.19. The results are compiled in Table 4.4.

The input and output voltage are assumed to be constant during a switching interval. However, this is not true as there is a ripple in the capacitor voltages. This causes additional error that may not result in ZCS of S_1 and S_2.

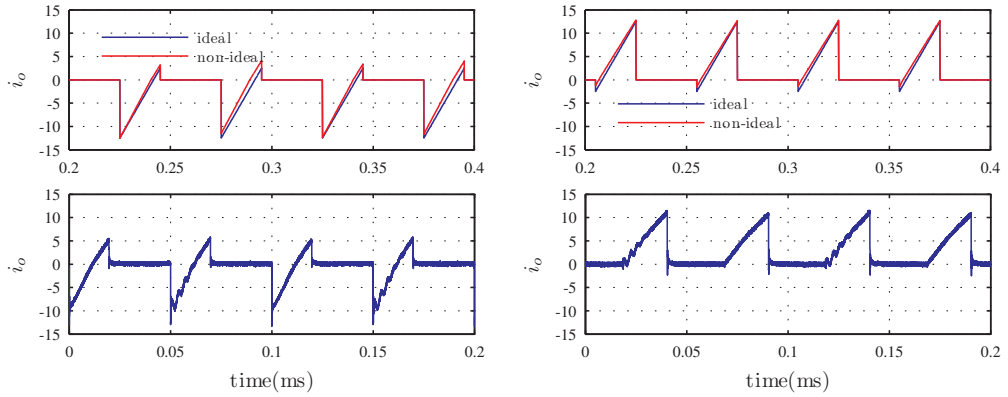
The converter is controlled using an FPGA. The voltage sensors have some offset associated with them which causes an error in the calculated duty ratio d. Additionally, the devices have finite turn-on and turn-off times. This leads to an error in δ.

A dead-time is introduced between the upper and lower switches of the two level converter. During the dead-time the diodes form a path for the inductor current to



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.18: DC-DC converter: Comparison of simulation (top) and experimental (bottom) results of inductor current (i_{L_s}).



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.19: DC-DC converter: Comparison of simulation (top) and experimental (bottom) results of DC current (i_o).

Table 4.4: Experimental results: DC-DC converter

	$\delta = 0.2$			$\delta = -0.2$		
	ideal	non-ideal	experimental	ideal	non-ideal	experiment
P_o (W)	154.41	114.51	63.65	-212.21	-245.57	-252.56
$\bar{I}_{L_s}$ (A)	6.34	6.38	5.70	6.39	6.61	5.51
$\bar{I}_o$ (A)	3.74	3.37	3.04	4.30	4.61	4.33

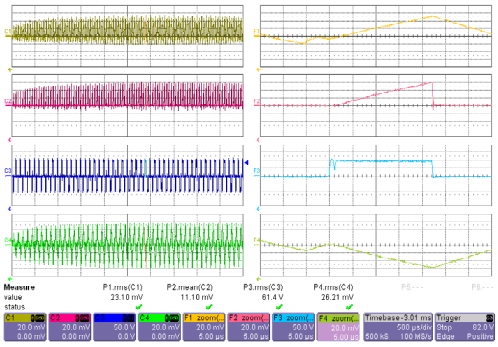
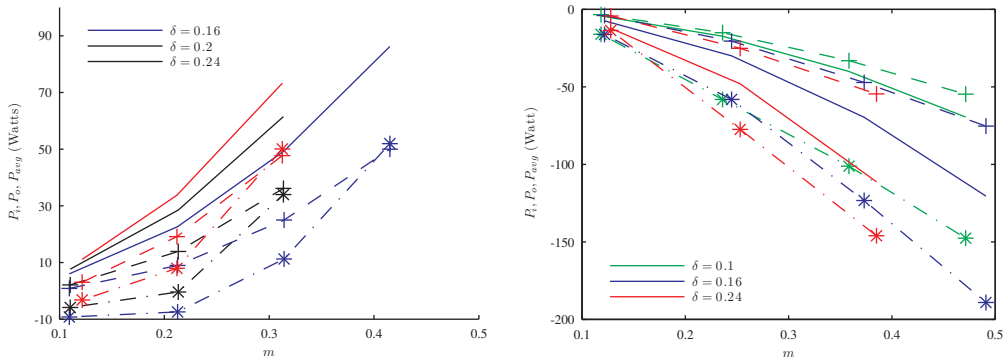


Figure 4.20: DC-DC converter: Effect of dead-time Input and output currents (top to bottom) i_i (C1:4A/div) and i_o (C2:4A/div), converter voltage v_s (C3:50V/div) and inductor current i_{L_s} (C4:4A/div); (left) time at 500μs/div and (right) time at 5μs/div.

flow. Fig. 4.20 shows the inductor current, and the converter voltage, v_s. The inductor current is slightly positive when switch S'_{o1} is turned off, hence, diode d_{o1} comes into conduction and the voltage $v_s = 100$V. This causes the inductor current to reduce to zero. Once the current reaches zero, v_s the depends on the voltage balanced by the device capacitances. When S_{o1} is turned on, the voltage $v_s = 100$V. Hence a glitch is observed in the voltage v_s.

4.5 Experimental results: Single-phase AC-DC converter

The experimental parameters are listed in Table. 4.3. The magnitude of V_o is set to 100V and $\hat{V}_i$ is varied to obtain different values of m. The converter is run for different values



(a) δ is positive

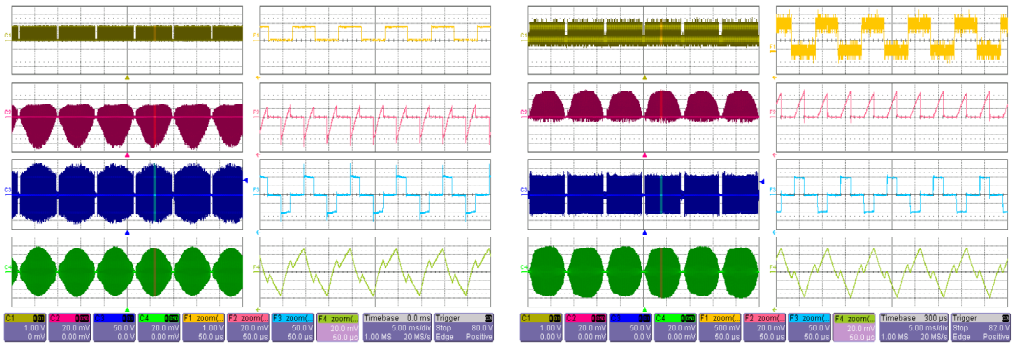
(b) δ is negative

Figure 4.21: Single-phase AC-DC converter: Expected power P_{avg}, input power P_i(-+) and output power P_o(-.*) for different values of m and δ.

of m and δ. The average input power, $P_i = v_i \times i_i$ and output power, $P_o = v_o \times -i_o$ are calculated from the scope data. The expected power P_{avg} equals $\delta m^2 \frac{V_o^2}{4Lf_s}$ from (4.24). The results are summarized in Fig. 4.21(a) for positive values of δ and in Fig. 4.21(b) for negative values of δ.

Bi-directional power flow capability of this converter has been demonstrated. It is observed that for positive direction of power flow, P_i is higher than P_o and the opposite is true for negative power flow. This is because of the losses in the circuit. The power flow in the converter has a quadratic relationship with respect to d and almost linear relationship with respect to δ.

In order to observe the switching waveforms of the converter $\hat{V}_i = 30\sqrt{2}$ and δ is selected to be ± 0.2. The pulses for S_1 along with the phase shifted secondary side voltage, v_s are shown in Fig. 4.22. For $\delta = +0.2$, v_s is shifted to the right with respect to S_1. For $\delta = -0.2$, v_s is shifted to the left with respect to S_1. The input and output currents as well as the inductor current can be observed in Fig. 4.23. The current i_o in Fig 4.23(a) has a negative average value indicating power flow is from the AC to DC side. i_o has a positive average value in Fig 4.23(b) indicating power flow from the DC to AC side. The input voltage v_i along with the filtered input current, i_{L_f} are shown in Fig. 4.24. There is a phase shift between v_i and i_{L_f} because of the input filter. It can be seen that the non filtered converter current, i_i is in phase with the input voltage for



(a) $\delta = 0.2$ (b) $\delta = -0.2$

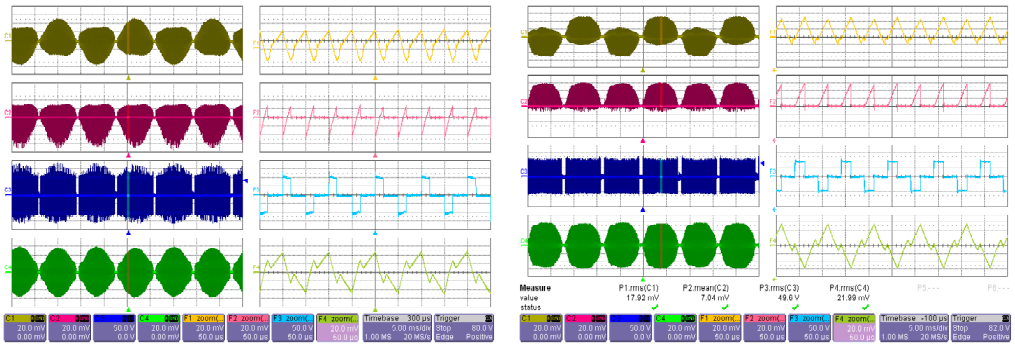
Figure 4.22: Single-phase AC-DC converter: (top to bottom) FPGA pulse for S_1 (C1:1V/div), output current i_o (C2:4A/div), v_s (C3:50V/div) and inductor current i_{L_s} (C4:4A/div); (left) time at 5ms/div and (right) time at 50μs/div.

a positive δ and it is 180^0 out of phase with respect to v_i for a negative δ. The currents through switch S_1 and S_2 are shown in Fig. 4.25. When S_1 is on, the current through it equals the inductor current i_{L_s}. When S_1 is off, $i_{S_2} = i_{L_s}$. The Fourier spectrum of the input current, i_i when $\delta = 0.2$ and $\delta = -0.2$ are in Fig. 4.26(a) and Fig. 4.26(c) respectively. This current has harmonics at the fundamental of 60Hz (f) and at 20kHz ($2 \times f_s$). The dc value of the output current has been removed and the Fourier transform of the resultant waveform when $\delta = 0.2$ and $\delta = -0.2$ are in Fig. 4.26(b) and Fig. 4.26(d) respectively. This current has components at 120Hz ($2 \times f$) and at 20kHz ($2 \times f_s$).

4.5.1 Effects of non-idealities in the circuit

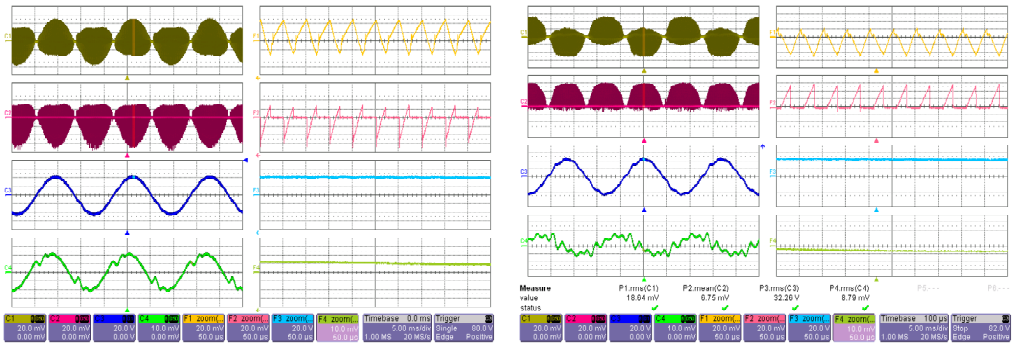
It is observed that the power transferred in the experimental prototype is different from the expected values. The analysis in section 4.4.1 is true for this single-phase AC to DC converter as well. A simulation with device voltage drops is run in PLECS®and the simulation and experimental results for the input current, inductor current and output current are compared in Fig. 4.27, Fig. 4.28 and Fig. 4.29 respectively. The results of this comparison are compiled in Table. 4.5.

From Fig. 4.27, it is observed that the input voltage, v_i has a large ripple content at the switching frequency. In the ideal analysis, it is assumed that v_i has a constant value during a switching interval. However, in the experimental case, the input voltage



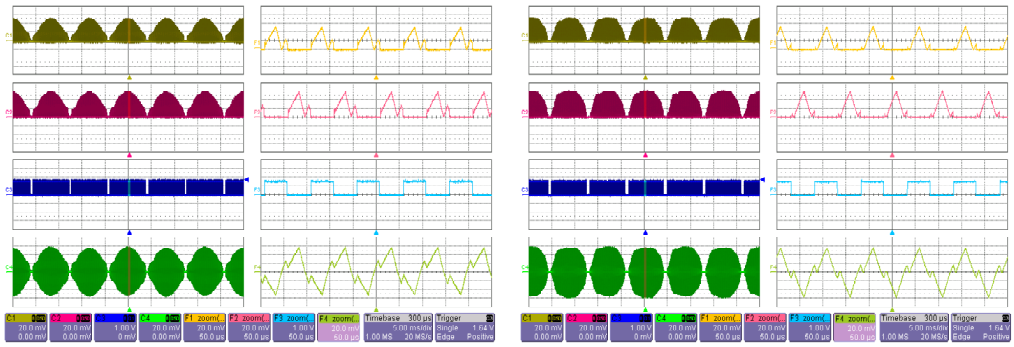
(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.23: Single-phase AC-DC converter: (top to bottom) Input and output current i_i (C1:4A/div) and i_o (C2:4A/div), v_s (C3:50V/div) and inductor current i_{L_s} (C4:4A/div); (left) time at 5ms/div and (right) time at 50μs/div.



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.24: Single-phase AC-DC converter: (top to bottom) Input and output current i_i (C1:4A/div) and i_o (C2:4A/div), input voltage v_i (C3:50V/div) and filtered input current i_{L_f} (C4:4A/div); (left) time at 5ms/div and (right) time at 50μs/div.



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.25: Single-phase AC-DC converter: (top to bottom) Currents through the primary switches i_{S_1}, i_{S_2} (C1,C2:4A/div), FPGA pulse for S_1 (C3:1V/div) and inductor current i_{L_s} (C4:4A/div); (left) time at 5ms/div and (right) time at 50μs/div.

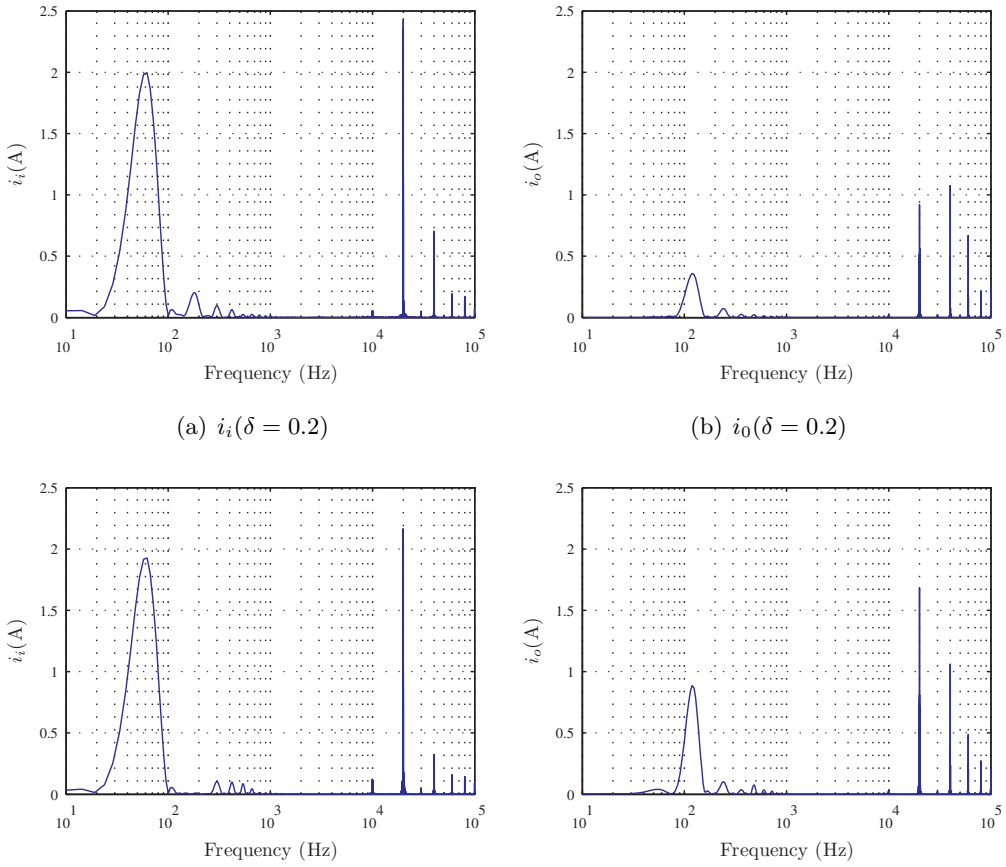
Table 4.5: Experimental results: Single-phase AC-DC converter

	$\delta = 0.2$			$\delta = -0.2$		
	ideal	non-ideal	experimental	ideal	non-ideal	experiment
P_o	62.08	26.20	29.78	-185.67	-188.18	-141.25
$\bar{I}_{L_s}$	5.39	5.35	4.47	5.42	5.20	4.43
$\bar{I}_o$	2.94	2.73	2.27	3.96	3.90	3.17

has some ripple it because of the ripple in the input current. This ripple in v_i has two effects; 1) In a switching interval, P_{io} given by (4.10) is proportional to the square of V_i, hence any perturbation in V_i will result in a change in the power transferred. 2) V_i is sensed only once every switching cycle. The duty ratio for the secondary side converter are calculated using this sensed input voltage. Hence, the applied duty ratio may not result in ZCS of the primary switches.

4.6 Conclusions and future work

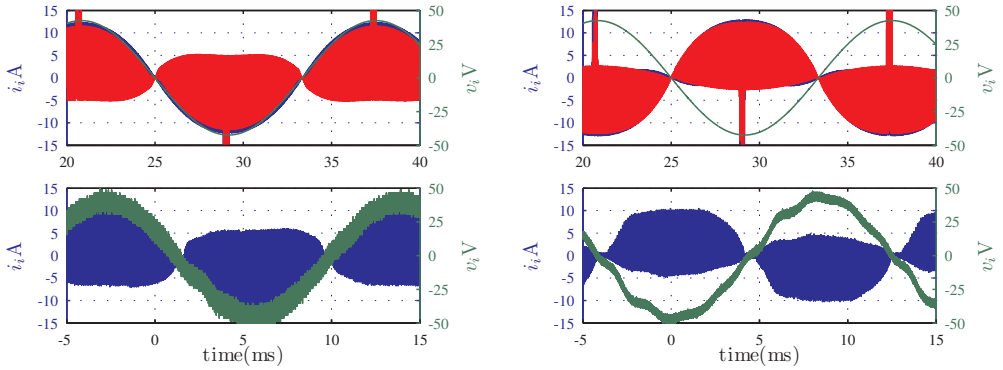
In this chapter, a modulation technique for a DAB-based single-phase AC-DC PET is proposed that results in several beneficial features simultaneously. The salient features



(a) $i_i(\delta = 0.2)$ (b) $i_0(\delta = 0.2)$

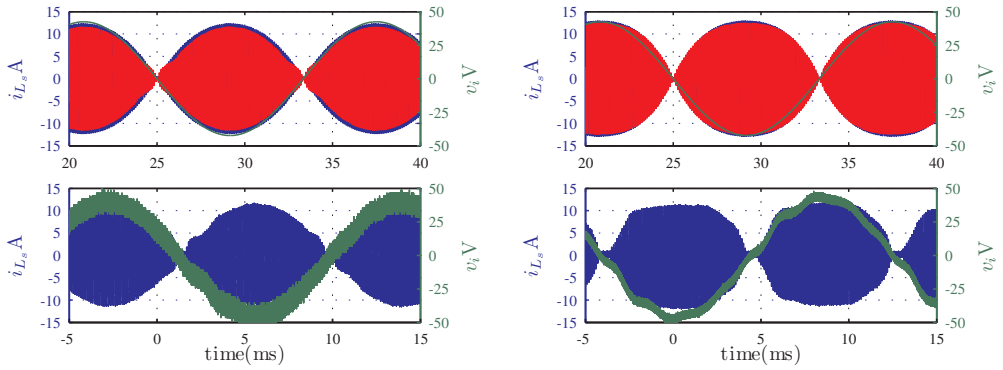
(c) $i_i(\delta = -0.2)$ (d) $i_o(\delta = -0.2)$

Figure 4.26: Single-phase AC-DC converter: Fourier spectrum of input and output currents



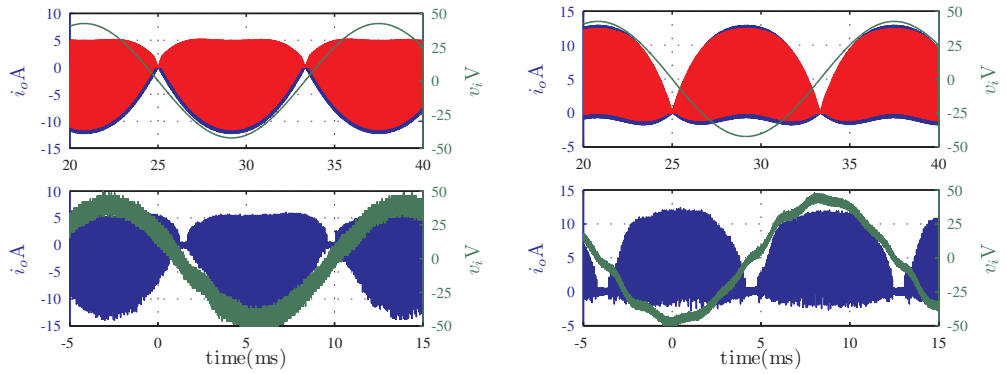
(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.27: AC-DC converter: Comparison of simulation (top) and experimental (bottom) results of input current (i_i).



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.28: AC-DC converter: Comparison of simulation (top) and experimental (bottom) results of inductor current (i_{L_s}).



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 4.29: AC-DC converter: Comparison of simulation (top) and experimental (bottom) results of DC current (i_o).

are single-stage power conversion, bi-directional power flow, open-loop unity power factor of operation, soft switching and high power density.

This single-stage power conversion with high-frequency transformer isolation is an improvement over conventional multi-stage AC-DC converters with bulky low frequency transformers. The bi-directional property of this converter makes is especially attractive for distributed DC storage. The linear relationship between power and δ makes it easy to control.

By operating in the 'inner mode' with constant phase shift, open-loop unity power factor is obtained on the AC-side. Nearly Zero Current Switching (ZCS) on the low voltage (high-current) side will lead to reduction in switching losses and improved efficiency. The switching frequency can also be increased, thus reducing the size of the magnetic components considerably. However, this potential reduction in size needs to be evaluated in light of higher RMS currents that result to achieve ZCS.

The input current has harmonics at twice the switching frequency. This translates to a small size of filter on the AC side. The DC side current has a low frequency harmonic at twice the input fundamental frequency. Hence, a bigger filter capacitor is required for the DC side of this converter.

The converters for DC-DC power conversion and single-phase AC-DC power conversion have been tested extensively in simulation. Experimental prototypes have been

built and tested. The device voltage drops, clamp circuit, dead-time, device turn-on and turn-off delays, sensing delays, ripple in input and output capacitor voltage are reasons for discrepancy in the experimental and the simulation results. The IGBTs used in the secondary side converter are rated for 1200V, 50A. Hence, the device non-idealities are significant at lower voltages, this leads to lower efficiency of the converter.

4.6.1 Future work

- Interleaving of the PET can be beneficial for reducing the ripple currents seen by the input and output side capacitors.
- Optimizing the filter design and the converter design to reduce the effects of parasitics on the operation of this PET.

Note: Parts of this chapter have been reprinted from [73] ©2012 IEEE
Part of this work has been done in collaboration with Nathan and Kaushik .

Chapter 5

Three-phase AC-DC Power Electronic Transformer

High-frequency transformer isolated three-phase AC-DC converters with soft-switching features are discussed in this section. A typical multi-stage AC-DC converter with an active front-end for power factor correction (PFC) and a soft-switched DC-DC Dual Active Bridge converter to provided high-frequency isolation and regulated output voltage is shown in Fig. 5.1 [11, 41–43, 74, 75]. These two stages are coupled using a capacitor. Such multi-stage power conversion systems may require more than one controller, have more power electronic devices, lower efficiency and reduced reliability. The DC capacitors are further known to be unreliable especially under thermal stress. Therefore, there has been an increasing interest in single-stage converters for AC-DC power conversion.

Single-stage, HFT isolated, three-phase AC-DC converters with soft-switching (ZVS or ZCS) have been proposed in [45–47, 76]. These converters do not operate on the DAB principle, however they achieve single stage power conversion with ZVS/ZCS of

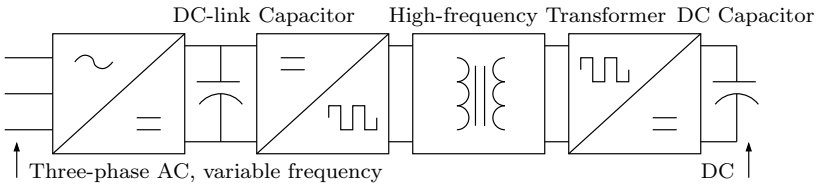


Figure 5.1: Multi-stage Power Electronic Transformer for AC to DC conversion

the switches. These converters however, lack bi-directional functionality.

Single-stage bi-directional converters that are soft-switched are proposed in [44] (resonant) and [48] (DAB). The converter in [48] is based on the DAB principle discussed in Chapter 4. It has features of ZCS and open loop power factor correction; however, the converters in [44, 48] require six four-quadrant switches on the AC side.

In this chapter, a three-phase bi-directional, HFT isolated, single-stage, DAB-based, AC-DC PET shown in Fig. 5.2 is analyzed. This converter has only two active switches on the AC-side. The transformers provide isolation and their leakage inductance is used for power transfer based on the DAB principle. This topology combines all the advantages of a HFT based system and a DAB-based system. Ideally, no clamp circuit is required for this converter. In Section 5.1, the topology and modulation technique are introduced. In Section 5.2, the converter is analyzed. In section 5.3, the analytical results are compared with the simulation results. In Section 5.4, closed-loop control of this converter is discussed. In Section 5.5, the experimental results on a laboratory prototype are presented.

5.1 Topology and modulation technique

The three-phase AC-DC PET is shown in Fig. 5.2. Balanced three-phase AC voltages given by (5.1) are applied to a bank of three three-winding transformers. The turns-ratio of one half of the primary winding to the secondary winding is $1 : n$. The secondary side of the transformer is connected to a DC voltage source, V_{dc} through a two-level converter. In this topology, $V_{dc} > \sqrt{3}n\hat{V}_i$. All the switches on the DC side are two-quadrant. Each switch on the AC side is realized using a three-phase diode bridge and a single one-quadrant switch. S_1 and S_2 are switched in a complementary way, with 50% duty at a switching frequency $f_s \left(= \frac{1}{T_s}\right)$ where, $f_s \gg f$. Hence high-frequency AC voltages are applied to the transformer. Assuming the leakage inductance of the two primary windings are identical ($L_{p_1} = L_{p_2} = L_p$) and the magnetizing inductance is neglected, the primary side circuit and HFT referred to the secondary side can be represented by three balanced voltages v'_x (where, x denotes a, b or c phase) with equivalent transformer leakage inductances in series with it. v'_x is $+nv_x$ when S_1 is on and $-nv_x$ when S_2 is on. The per-phase equivalent leakage inductance referred to the

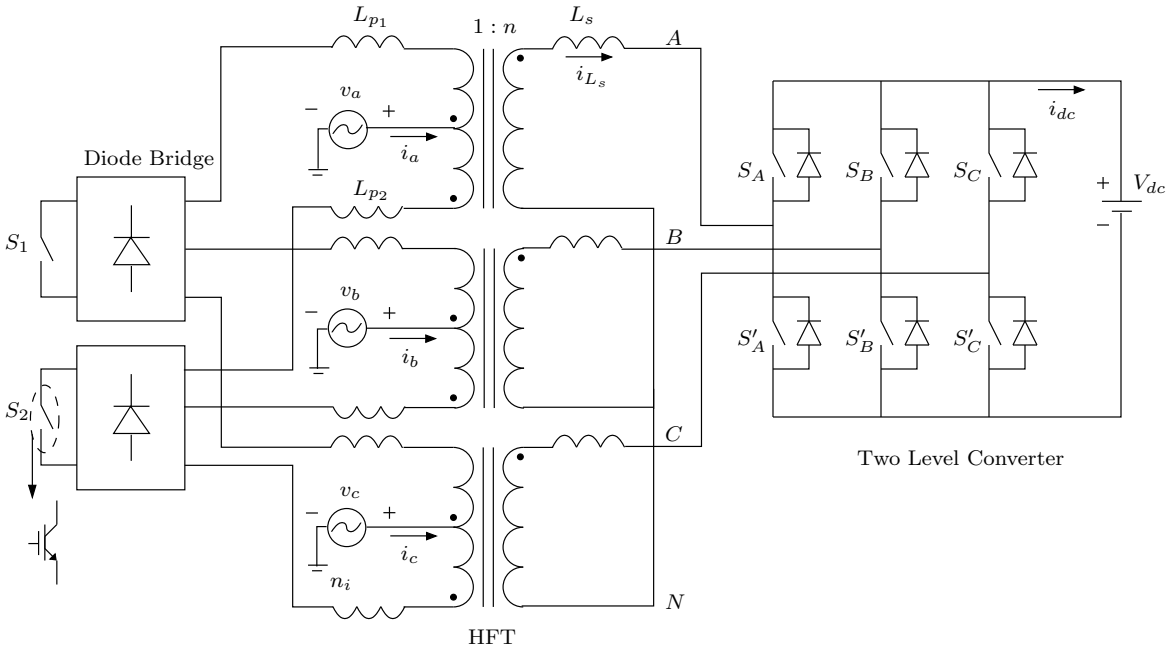


Figure 5.2: Three-phase AC-DC converter (PET): Topology

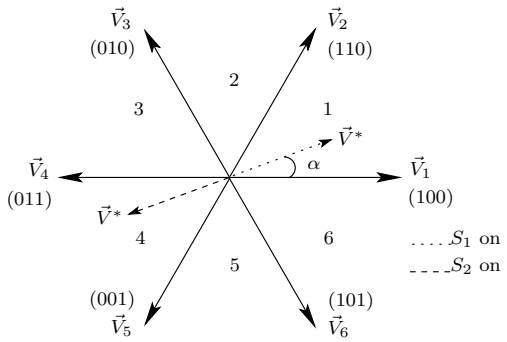


Figure 5.3: Two-level converter space vectors

secondary side is given by $L_{eq} = n^2 L_p + L_s$. The two-level converter is pulse-width modulated (PWM) to satisfy the following three conditions. 1) Over every $\frac{T_s}{2}$, the average voltage applied across each transformer equivalent leakage inductance must be zero. 2) The PWM voltages generated by the two-level converter are phase shifted with respect to the voltages on the secondary side of the transformer; hence, power is transferred by the Dual Active Bridge principle. 3) In this modulation, the phase shift that can be applied is limited such that at any point, the converter can be viewed to be in 'inner mode' of operation. In order to satisfy the first criterion, the duty ratios for the two-level converter are calculated using conventional Space Vector Modulation (SVM). The voltage space-vector diagram for a two-level converter is in Fig. 5.3. In this example, when S_1 is on, the input voltage space vector, $\vec{V}^*$ given by (5.2) is in sector 1 and when S_2 is on, it is 180^0 out of phase, in sector 4. The duty ratios for vectors $\vec{V}_1$ and $\vec{V}_2$ are given by d_1 and d_2 respectively in (5.3). As the effective voltage applied across L_{eq} is zero every $\frac{T_s}{2}$ the phase currents of the transformer go to zero at the transition from S_1 to S_2 and vice-versa. Hence, Zero Current Switching (ZCS) is

achieved for these switches.

$$v_a(t) = \hat{V}_i \cos(\omega t)$$
$$v_b(t) = \hat{V}_i \cos\left(\omega t - \frac{2\pi}{3}\right)$$
$$v_c(t) = \hat{V}_i \cos\left(\omega t - \frac{4\pi}{3}\right) \qquad \cdots \text{Where, } \omega = 2\pi f \tag{5.1}$$
$$\vec{V}_i(t) = \vec{V}^*(t) = v'_a(t) + v'_b(t)e^{j\frac{2\pi}{3}} + v'_c(t)e^{j\frac{4\pi}{3}} \tag{5.2}$$
$$d_1 = \sqrt{3}d\sin\left(\frac{\pi}{3} - \alpha\right)$$
$$d_2 = \sqrt{3}d\sin(\alpha) \quad \cdots \text{Where, } d = \frac{n\hat{V}_i}{V_{dc}} \tag{5.3}$$
$$|\delta| \leq \frac{1}{2}\left(1 - \sqrt{3}d\right) \quad \text{Hence, } d_{max} = \frac{1}{\sqrt{3}} \tag{5.4}$$

Without loss of generality, the converter waveforms are analyzed when $\vec{V}^*$ is in sector 1 and S_1 is on. The secondary side equivalent transformer voltage for phase-a, v'_a and the two-level converter output voltage for phase-a, v_{AN} are shown in Fig. 5.4(a). A phase shift $\delta\frac{T_s}{2}$ is introduced between the primary and secondary PWM voltages of the transformer in order to obtain power transfer and v_{AN} is symmetric with respect to the phase shift $\frac{T_s}{4} + \delta\frac{T_s}{2}$. According to the third condition, the PWM pulses for the two-level inverter must be contained within $\frac{T_s}{2}$; thus, δ is limited by (5.4). When S_1 is on, v_{AN} is 0, $\frac{2}{3}V_{dc}$, $\frac{1}{3}V_{dc}$ when vectors $\vec{V_0}$, $\vec{V_1}$ and $\vec{V_2}$ are applied respectively. The current through L_{eq} for phase-a is shown in Fig. 5.4(b). As the average value of v_{AN} equals the average value of v'_a over each half cycle, $I_{a_0} = I_{a_5} = 0$. This is true for phase-b and phase-c as well. When vector $\vec{V_0}$ is applied, the DC current, i_{dc} (Fig.5.4 (c)) is zero. When vector $\vec{V_1}$ is applied, $i_{dc} = i_{L_{eq},a}$ and when vector $\vec{V_2}$ is applied, $i_{dc} = i_{L_{eq},a} + i_{L_{eq},b}$. In order to analyze the currents, voltages and power the per-unit (pu) base values on the secondary side are chosen to be (5.5). The currents $i_{L_{eq},a}$ and i_{dc} are assumed to be piecewise linear over the switching cycle; hence, per-unit switching-cycle-average phase currents as well as the DC current of the converter can be calculated to be (5.6) and (5.7) respectively. It is clear from (5.6), if δ is a constant, unity power-factor is obtained on the AC side. The average power per switching cycle, P_{io} is given by (5.8). The power transferred is directly proportional to δ. The locus of the power that can be transferred for different values of d as a function of δ is plotted in Fig. 5.5. Maximum

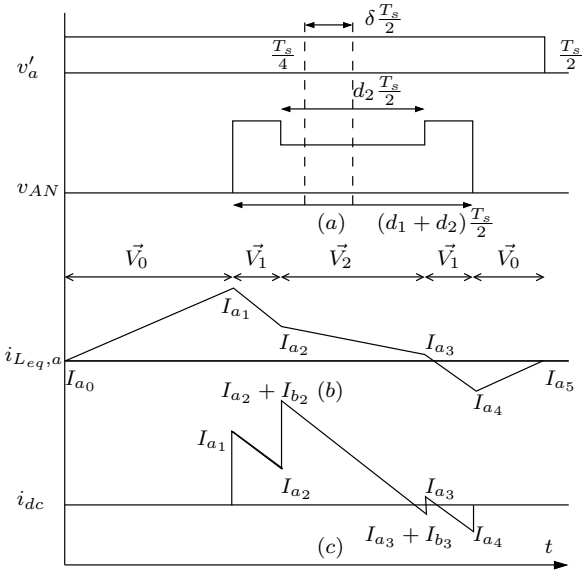


Figure 5.4: Switching waveforms

power can be transferred (0.1164pu) when d is 0.3849 ($\frac{2}{3\sqrt{3}}$). When δ is positive, power is transferred from the AC side to the DC side, when δ is negative, the power transfer is in the opposite direction.

$$\left.\begin{aligned} V_{base} &= V_{dc} \\ I_{base} &= \frac{V_{dc}}{2\pi f_s L_{eq}} \\ P_{base} &= \frac{V_{dc}^2}{2\pi f_s L_{eq}} \end{aligned}\right\} \tag{5.5}$$

$$\begin{aligned} \tilde{i_a} &= \pi d\delta\cos(\omega t) \\ \tilde{i_b} &= \pi d\delta\cos(\omega t - \frac{2\pi}{3}) \\ \tilde{i_c} &= \pi d\delta\cos(\omega t - \frac{4\pi}{3}) \end{aligned} \tag{5.6}$$

$$\tilde{i}_{dc} = 1.5\pi d^2\delta \tag{5.7}$$

$$\begin{aligned} P_{io} &= \frac{3d^2V_{dc}^2\delta}{4L_{eq}f_s} \\ &= \frac{3d^2\pi\delta}{2}pu \end{aligned} \tag{5.8}$$

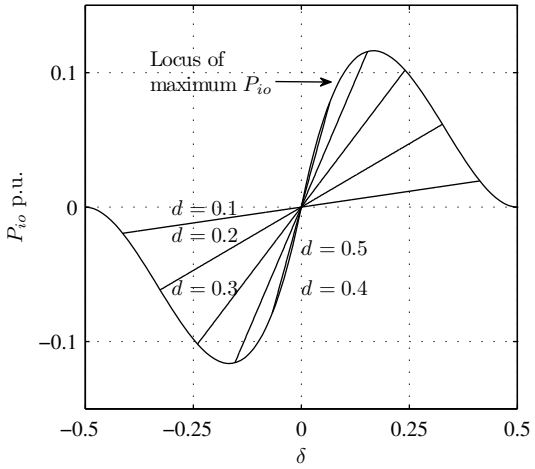


Figure 5.5: Three-phase AC-DC: P_{io} Vs δ

5.2 Analysis

Every $\frac{T_s}{2}$, the reference voltage space vector, $\vec{V}^*$ is constructed using the two adjacent vectors that make up the sector along with zero vectors. If the zero vector is selected to be 0(000) in all sectors, the vector sequence 0-1-2-1-0 in odd sectors and 0-2-1-2-0 in even sectors will result in minimum number of switch transitions. If 7(111) is selected as the zero vector for all sectors, then switching sequence 7-2-1-2-7 in odd sectors and 7-1-2-1-7 in even sectors will result in minimum number of switch transitions. If the switching sequence is held constant, the zero vector that needs to be applied will change depending on the sector. This will lead to a switching from (111) to (000) every $\frac{T_s}{2}$ because, at that instant, the input voltage reference always switches from an odd sector to even sector or vice-versa. Since $f_s >> f$, in one switching interval, the input AC-voltages can be assumed to be constant, thus the slope of the currents in Fig. 5.4(b), (c) will be linear. The RMS value for the piece-wise linear DC current calculated over $\frac{T_s}{2}$ is denoted by $\overline{I}_{Ts/2}$, it is a function of voltages, d, α and δ. The value of $\overline{I}_{Ts/2}$ is calculated in all 6 sectors for switching sequence 0-1-2-1-0 and 0-2-1-2-0. The RMS current over a sector j, $\overline{I}_j$ is calculated by (5.9). It can be shown that it is sufficient to calculate the value of

$\overline{I}_j$ in sector 1 and 2 only. Further, the RMS value over the low frequency fundamental is calculated by (5.10). A similar analysis is done for the transformer currents. The choice of switching sequence does not affect the RMS values for the currents and they all result in unity-power factor on the AC-side.

$$\overline{I}_j = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \overline{I}_{Ts/2}^2 \,\mathrm{d}\alpha} \qquad j \in \{1, 2..6\} \tag{5.9}$$

$$\overline{I}_{1/f} = \sqrt{\frac{1}{6}\sum_{j=1}^{6} \overline{I}_j^2} \tag{5.10}$$

The RMS value of the DC-current $\overline{I}_{dc}$ of this converter in per-unit is given by (5.11). The size of the DC-capacitor is a function of the RMS ripple current content of i_{dc}. This RMS ripple current in the DC capacitor, $\overline{I}_{rpl}$ is calculated by subtracting the DC component from $\overline{I}_{dc}$. The values of $\overline{I}_{rpl}$ given by (5.12) are plotted for different values of d as a function of δ in Fig. 5.6. For a certain value of d, the ripple content in the DC capacitor increases as the absolute value of phase shift, $|\delta|$ increases. The maximum value of $\overline{I}_{rpl}$ is 0.137pu when $d = 0.322$.

$$\begin{aligned}\overline{I}_{dc} &= K_2[(\sqrt{3}\left(9d(-45+358d) + 40\left(29+360\delta^2\right)\right) \\ &\quad - 1890d\pi)\pi d^3]^{\frac{1}{2}} \qquad \text{Where, } K_2 = 0.013 \end{aligned} \tag{5.11}$$

$$\begin{aligned}\overline{I}_{rpl} &= K_2[(\sqrt{3}(9d(-45+358d) + 40(29+360\delta^2)) \\ &\quad - 270d(7+48\delta^2)\pi)\pi d^3]^{\frac{1}{2}} \end{aligned} \tag{5.12}$$

$$\begin{aligned}\overline{I}_{L_{eq}} &= K_1[(-560\sqrt{3}d + 27d^2(3\sqrt{3}+8\pi) \\ &\quad + 96(\pi + 12\delta^2\pi))\pi d^2]^{\frac{1}{2}} \qquad \text{Where, } K_1 = 0.021 \end{aligned} \tag{5.13}$$

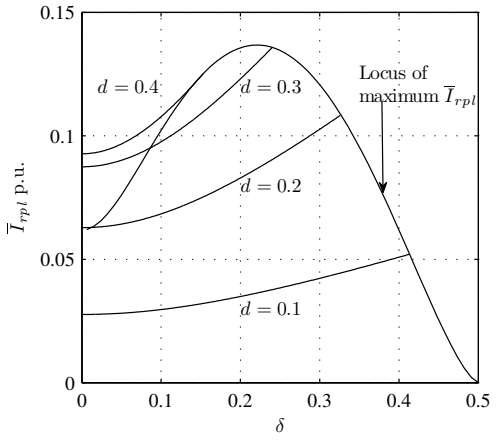


Figure 5.6: Three-phase AC-DC: $\overline{I}_{rpl}$ Vs δ

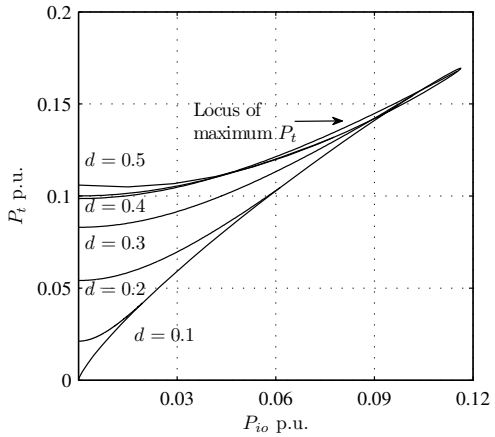


Figure 5.7: Three-phase AC-DC: P_t Vs P_{io}

$$\overline{V}_p = d/2 \qquad \overline{V}_s = \sqrt{\frac{2d}{\sqrt{3}\pi}} \tag{5.14}$$

$$\overline{I}_{L_p} = \frac{\overline{I}_{L_s}}{\sqrt{2}} \qquad \overline{I}_{L_s} = \overline{I}_{L_{eq}} \tag{5.15}$$

$$\begin{aligned} P_t &= \frac{3}{2}\left[2\overline{V}_p\overline{I}_{L_p} + \overline{V}_s\overline{I}_{L_s}\right] \\ &= \frac{3}{2}\left(\frac{d}{\sqrt{2}} + \sqrt{\frac{2d}{\sqrt{3}\pi}}\right)\overline{I}_{L_s} \end{aligned} \tag{5.16}$$

The size of the high-frequency transformer is related to its VA rating which is given by P_t in (5.16). Hence, it is important to determine the RMS voltages and currents applied to the high-frequency transformer. The RMS value of $i_{L_{eq}}$ in per-unit as a function of d and δ is given by (5.13). The voltages generated by the two-level converter are applied at the secondary side of the HFT. Since the switching duty ratios as well as the DC voltage is known, the RMS voltages applied to the secondary side of the transformer, $\overline{V}_s$ can be calculated in the same way as the RMS analysis for the currents. The transformer primary and secondary winding RMS voltages $\overline{V}_p$ and $\overline{V}_s$ are given by (5.14). As each primary winding conducts only for 50% of the time, $\overline{I}_{L_p}$ is given by (5.15). P_t is plotted

Table 5.1: Simulation and experimental parameters for three-phase AC-DC converter

$\hat{V}_i$	$20\sqrt{2}$V
V_{dc}	100V
f_s , f	10kHz , 60Hz
L_s	80μH
turns-ratio	1:1:1
δ	$\pm$0.2

as a function of P_{io} for different values of d in Fig. 5.7. The transformer utilization factor (TUF) is defined as $\frac{P_{io}}{P_t}$. The highest value of TUF 68.8% is obtained for a power transfer of 0.116pu with $d = 0.399$. One drawback of this converter is that, when δ equals zero, the power transfer is zero, however there are RMS currents in the transformer. The worst case occurs when $d = 0.577$ and $P_t = 0.106$pu.

5.3 Simulation results

The converter in Fig. 5.2 is simulated in PLECS®. All the switches and diodes in the circuit are considered to be ideal. The simulation parameters are listed in Table 5.1. The input current and voltage for phase-a (i_a, v_{an_i}) and the DC current (i_{dc}) are plotted for $\delta = 0.2$ and $\delta = -0.2$ in Fig. 5.8 and 5.9 respectively. It can be seen that bi-directional power flow is possible by changing the direction of phase shift, δ. The input currents have harmonics at twice the switching frequency and the output current has harmonics at six times the fundamental frequency in addition to harmonics at twice the switching frequency. The switching pulses for switch S_1, the currents through the AC-side switches and the DC current are shown for a few switching cycles in Fig.5.10 and 5.11. It is observed that the switches S_1 and S_2 are switched at zero current.

The RMS values for transformer currents as well as DC current are measured for $\delta = \pm 0.2$, these values are compared with their analytical formulas in Table 5.2.

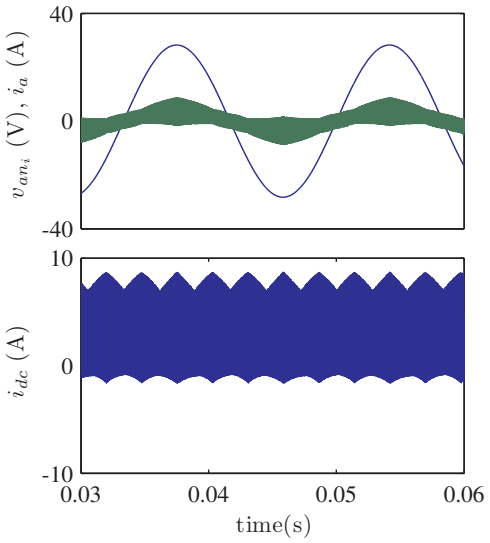


Figure 5.8: $\delta = 0.2$

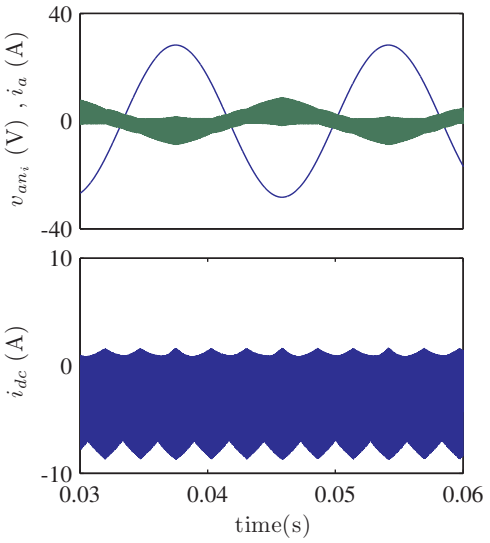


Figure 5.9: $\delta = -0.2$

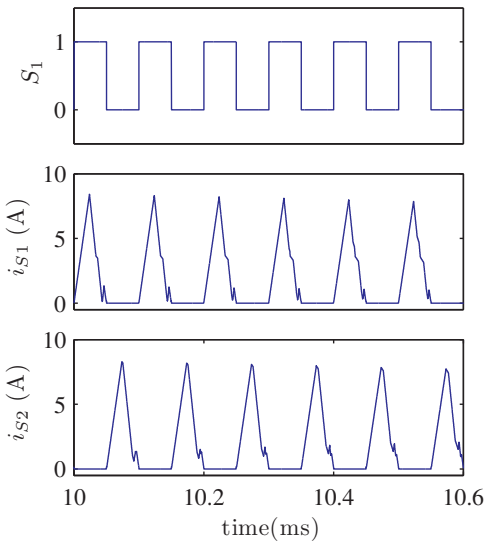


Figure 5.10: $\delta = 0.2$

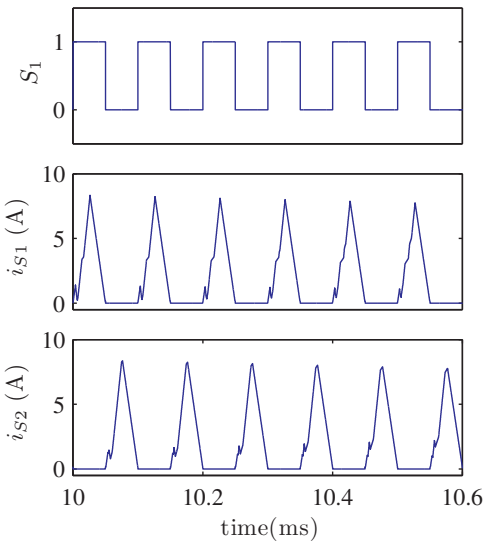


Figure 5.11: $\delta = -0.2$

Table 5.2: Analytical and simulated values

	Analytical	Simulation (δ=0.2)	Simulation (δ=-0.2)
P_{dc} (Watt)	150.00	145.76	-149.14
$\overline{I}_x$ (A)	3.20	3.16	3.16
$\overline{I}_{dc}$ (A)	2.77	2.73	2.77
$\overline{I}_{rpl}$ (A)	2.33	2.31	2.34

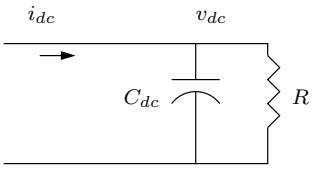


Figure 5.12: DC load

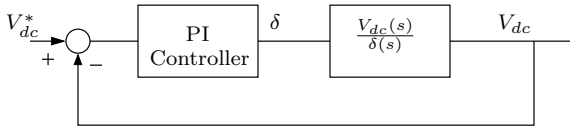


Figure 5.13: Control loop

5.4 Closed-loop control of three-phase AC-DC converter

In this section a controller is designed so as to regulate the DC voltage of the converter in Fig. 5.2. In this converter, the power transfer is directly proportional to the phase-shift δ and the equation for power transfer is given by (5.17). The DC side of the converter can be represented by the load capacitor and some load resistance R as shown in Fig. 5.12. R can be either positive or negative depending on the direction of power flow. The output DC current and DC voltage are related by (5.18). The controller can be designed by linearizing the circuit about an operating point. If there is a perturbation $\tilde{\delta}$ around the operating point δ, there is a perturbation in P, V_{dc} and I_{dc} which are represented by $\tilde{p}$, $\tilde{v_{dc}}$ and $\tilde{i_{dc}}$ respectively. The resulting perturbed power equation is given by (5.19). Neglecting the terms for $\tilde{v_{dc}}\tilde{i_{dc}}$, the resulting equation in frequency domain is given by (5.20). The transfer function relating V_{dc} and δ is in (5.21).

The control loop for the plant is shown in Fig. 5.13. A Proportional-Integral(PI)

Table 5.3: Simulation parameters: Closed-loop control

$\hat{V}_i$, V_{dc}	70V, 300V
f_i, f_s	60Hz, 10kHz
C_{dc}, L_{eq}	500μF, 100μH

controller is designed for an operating point given in Table. 5.3. The cross-over frequency for the control is selected to be 50Hz.

$$P = V_{dc}I_{dc} = \frac{3\hat{V}_i^2\delta}{4L_{eq}f_s} \tag{5.17}$$

$$I_{dc}(s) = \frac{V_{dc}(s)(RCs+1)}{R} \tag{5.18}$$

$$P + \tilde{\tilde{p}} = (V_{dc} + \tilde{\tilde{v_{dc}}}) * (I_{dc} + \tilde{\tilde{i_{dc}}})$$

$$\tilde{\tilde{p}} = V_{dc}\tilde{\tilde{i_{dc}}} + I_{dc}\tilde{\tilde{v_{dc}}} \tag{5.19}$$

$$\frac{3\hat{V}_i^2\delta(s)}{4L_{eq}f_s} = V_{dc}\left[\frac{(RCs+1)V_{dc}(s)}{R}\right] + I_{dc}V_{dc}(s) \tag{5.20}$$

$$G_{ps}(s) = \frac{V_{dc}(s)}{\delta(s)} = \frac{3\hat{V}_i^2}{4L_{eq}f_s}\frac{1}{\left[\frac{V_{dc}(RCs+1)}{R} + I_{dc}\right]} \tag{5.21}$$

The converter is simulated in using PLECS blockset in MATLAB®/Simulink® environment. The response of the controller to a step change in the reference value of V_{dc} from 300V to 330V at $\frac{2}{f_i}$s is in Fig. 5.14. The load resistance is changed at $\frac{7}{f_i}$s from R to $\frac{2}{3}R$ and it is seen that after an initial perturbation, the voltage is being controlled to the reference value. In order to study the controller response for bi-directional power flow, the output is represented as a current source that changes value so that the converter switches from feeding power to drawing power from the AC side at $6/f_i$s. The DC voltage reference is set to 300V during this time. The DC voltage and currents are shown in Fig. 5.15, The unfiltered input voltage and current for phase-a are given in Fig. 5.16. It is clear that the input current is 180^0 out of phase before $3/f_i$s and in phase with it after that, hence unity power factor is obtained as well as bi-directional power flow is possible under voltage control.

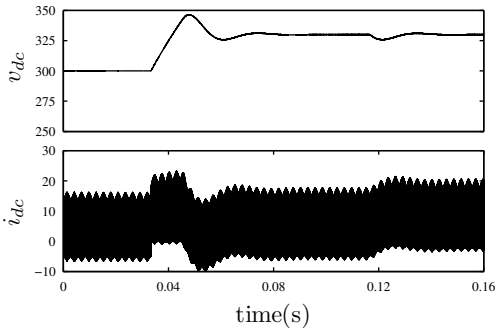


Figure 5.14: Voltage controller response

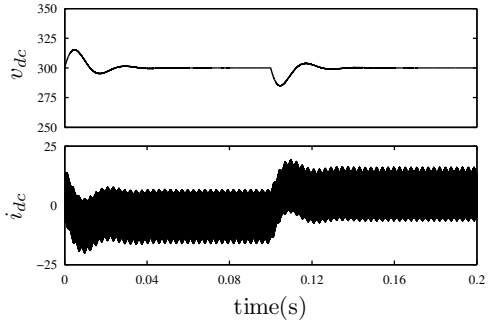


Figure 5.15: DC voltage and currents

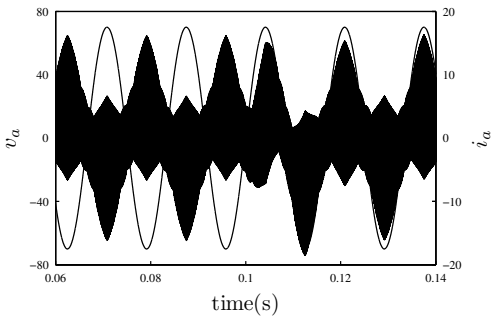


Figure 5.16: AC current and voltage

5.5 Experimental results

The schematic of the experimental setup for the three-phase AC-DC converter is shown in Fig. 5.17. A photograph of the experimental setup is in Fig. 5.18. The three winding transformer are wound of ferrite cores. These transformers have unity turns-ratio, leakage inductance of approximately 15μH and magnetizing inductance of 50mH. The leakage inductance of the transformer is very small, hence, in order to limit the power flow in this converter, additional inductors, L_A, L_B and L_C are connected on the secondary side of the transformers as shown in Fig.5.17. Since programmable power supplies are used in this experiment, the resistors R_i and R_{dc} are included to sink the power that is transferred by this AC-DC converter. An LC (L_f=0.5mH, C_f=20μF) filter is used on the AC side. A clamp circuit composed of a resistor and capacitor is present on the AC side. It provides a path for currents to flow during the dead-time between switches S_1 and S_2. More details on the experimental setup are in Appendix B. The input voltages, v_{ab}, v_{ac} and v_{dc} are sampled at 10kHz using 12-bit ADCs. Using these sensed voltages, the FPGA computes the duty ratios and generates PWM pulses for all the power electronic switches. The details of the FPGA implementation are in Appendix E.2.

The converter is tested at different values of d and δ for parameters listed in Table. 5.1. The magnitude of V_o for all these cases is 100V and $\hat{V}_i$ is varied to obtain different values of d. In order to compare the analytical values and experimental values, it is assumed that the DC voltage, V_{dc} is constant at 100V. The RMS value of the input voltage for phase-a ($\overline{V}_a$) is calculated from the scope data. The value of $d = \frac{\sqrt{2}\times\overline{V}_a}{V_{dc}}$. The average input power for phase-a is calculated by taking the average of the instantaneous product of the input voltage and unfiltered input current. The average value of the DC current is given by I_{dc}. The output power, $P_{dc} = V_{dc} \times -I_{dc}$. The results are summarized in Fig. 5.19(a) for positive values of δ and in Fig. 5.19(b) for negative values of δ. There is some error in the expected power, P_{io} (5.8) and the measured AC and DC power. This is mainly due to the parasitics such as device voltage drops, resistance and dead-time. An operating point with $V_{dc} = 100V$, $\hat{V}_i = 20\sqrt{2}$ and $\delta = 0.2$ and $\delta = -0.2$ is selected for further study. The filtered and unfiltered input current for phase-a for these two cases are in Fig. 5.20. For a positive δ, the input current for phase-a is in phase with the input voltage. Hence, unity power factor is obtained. When

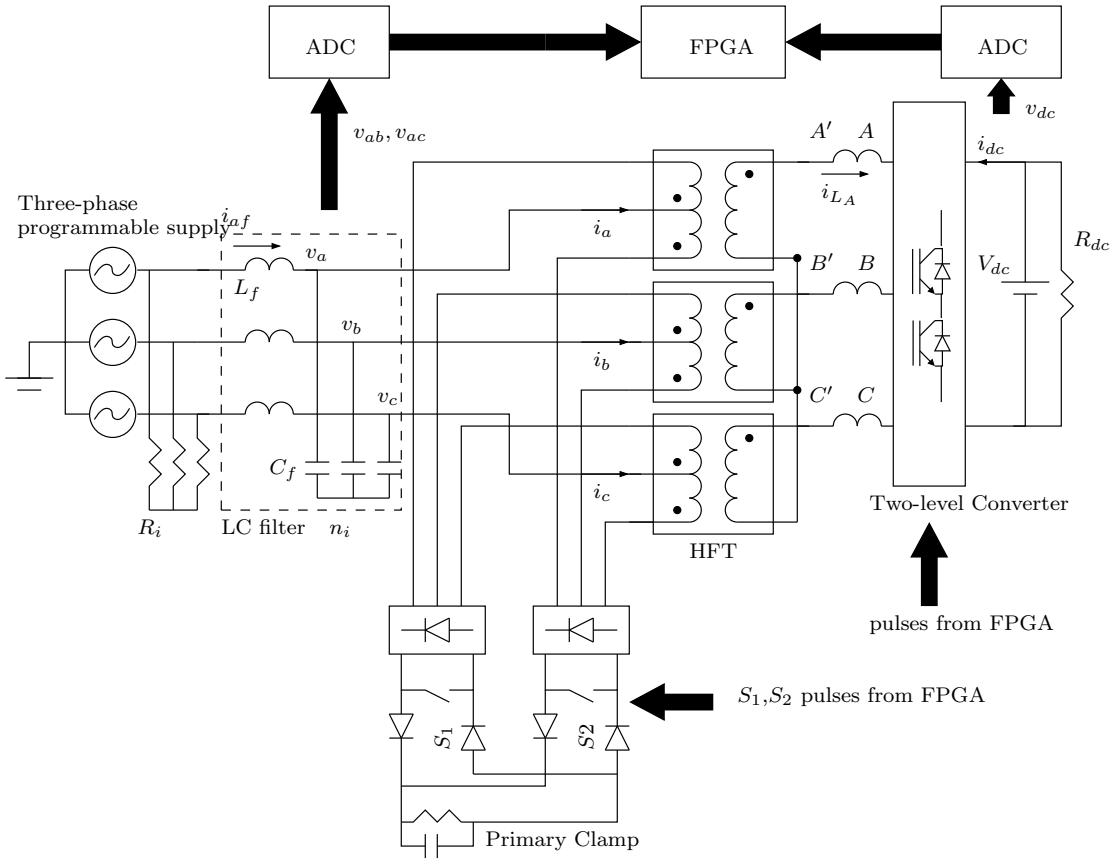


Figure 5.17: Schematic of experimental setup

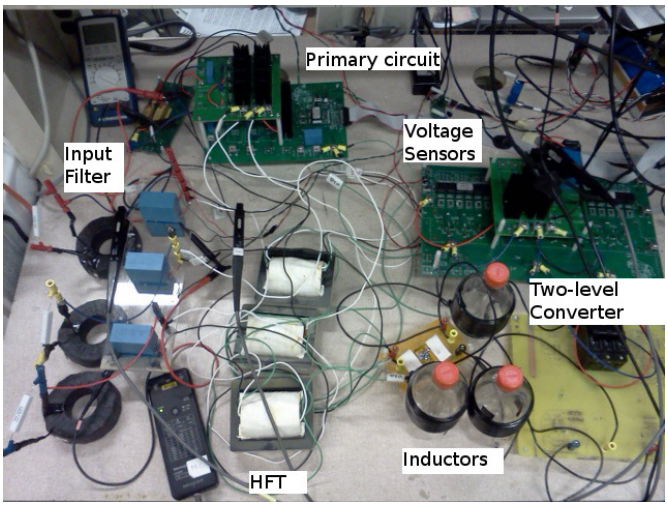
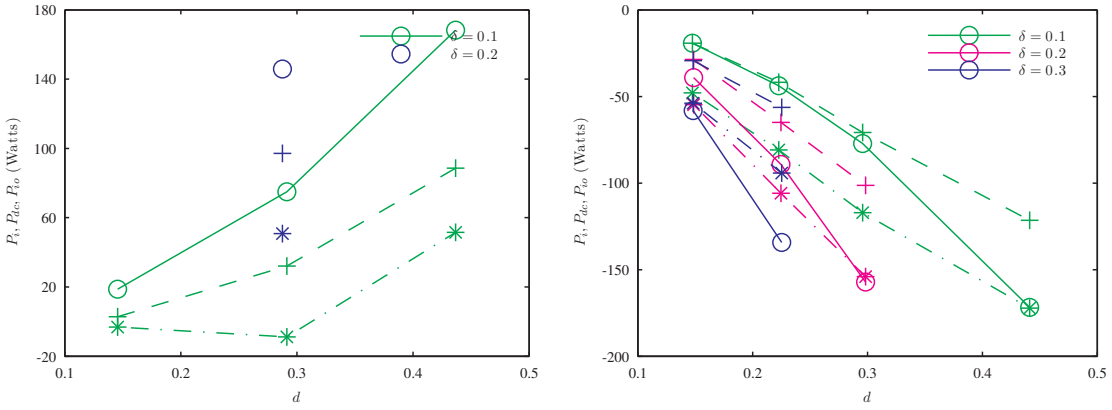


Figure 5.18: Photograph of experimental setup



(a) δ is positive

(b) δ is negative

Figure 5.19: Three-phase AC-DC converter: Expected power P_{io}(-o), input power P_i(-+) and output power P_{dc}(-.*) for different values of d and δ

Table 5.4: Experimental and analytical results of P_{io}

	P_i (Watt)	P_{dc} (Watt)	P_{io} (Watt) (Analytical)
$\delta = 0.2$	102.72	-54.42	154.37
$\delta = -0.2$	-101.28	154.39	-161.76

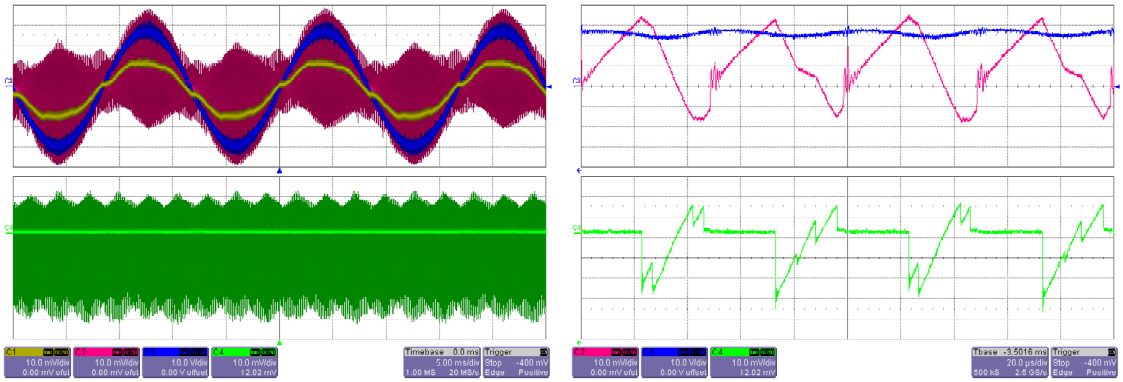
Table 5.5: Experimental and analytical results of RMS currents

	$\overline{I}_{L_{eq}}$(experiment)	$\overline{I}_{L_{eq}}$(analytical)	$\overline{I}_{dc}$(experiment)	$\overline{I}_{dc}$(analytical)
$\delta = 0.2$	2.84A	3.23A	2.08A	2.82A
$\delta = -0.2$	2.60A	3.29A	2.69A	2.90A

δ is negative, the input currents are 180^0 out of phase with the input voltage. Hence, power is flowing from DC to AC side. The average value of the DC current is positive when power flow is from the DC to AC side and it is negative for a positive value of δ. The experimental and analytical powers at the input and output of this converter are summarized in Table 5.4. The transformer secondary voltage and the converter voltage are shown in Fig. 5.21. For a positive δ, the two-level converter voltages are shifted to the right with respect to the high-frequency voltages on the secondary side of the transformer. When δ is negative, the two-level converter voltages are shifted to the left. The currents through the primary switches S_1 and S_2 are in Fig. 5.22. The switches, S_1 and S_2 are not critically switched at zero current. This is because of device voltage drops, circuit resistance, dead-time as well as discrepancy in duty ratio calculations. However, it must be noted that the current at the instant of switching is very small.

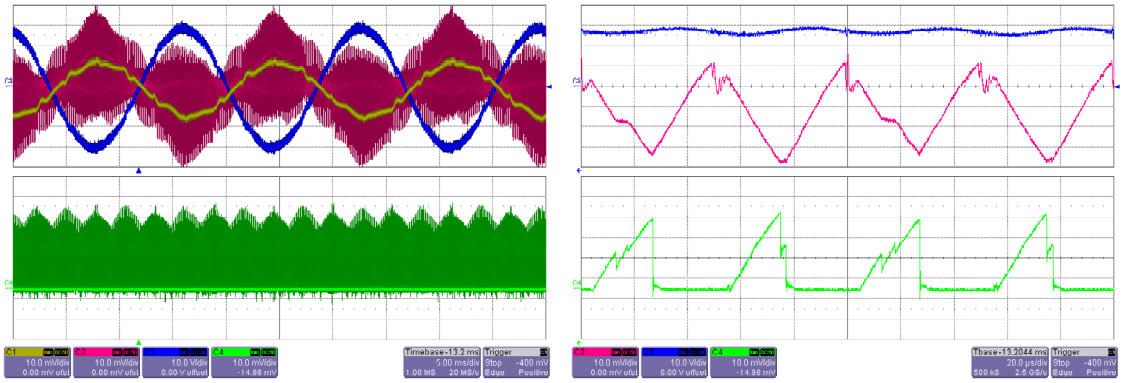
The RMS currents from the experimental data are compared with the analytical values in Table 5.5.

The Fourier spectrum of the unfiltered input current, i_a when $\delta = 0.2$ and $\delta = -0.2$ are in Fig. 5.23(a) and Fig. 5.23(c) respectively. This current has harmonics at the fundamental of 60Hz and at 20kHz ($2 \times f_s$). The DC value of the output current has been removed and the Fourier transform of the resultant waveform when $\delta = 0.2$ and $\delta = -0.2$ are in Fig. 5.23(b) and Fig. 5.23(d) respectively. This current has components at 120Hz ($2 \times f_i$), 360Hz ($6 \times f_i$) and at 20kHz ($2 \times f_s$).



(a) $\delta = 0.2$ (5ms/div)

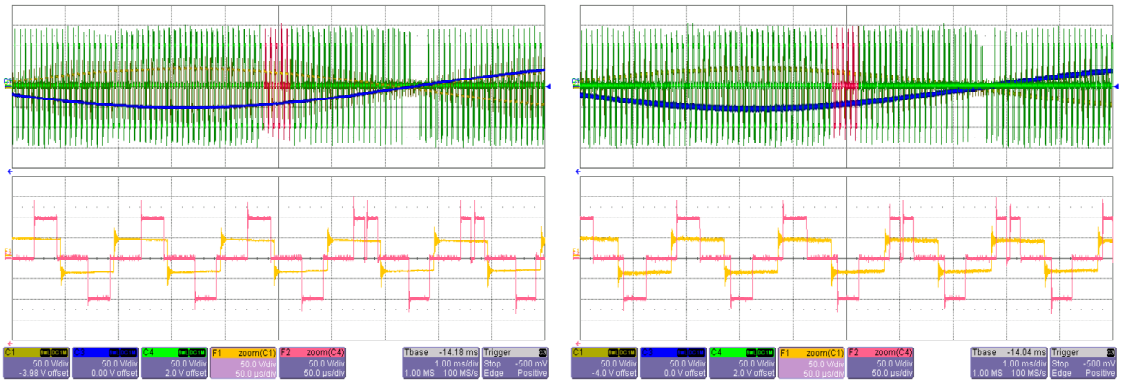
(b) i_a and i_{dc} for $\delta = 0.2$ (20μs/div)



(c) $\delta = -0.2$ (5ms/div)

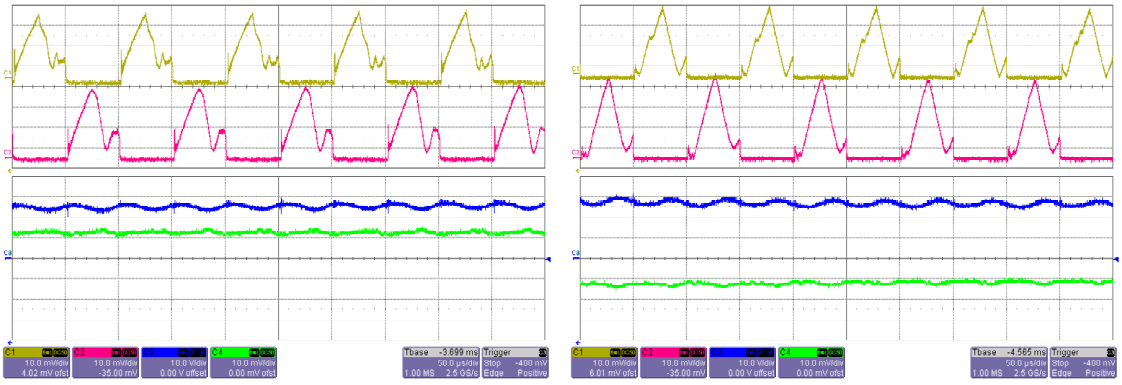
(d) i_a and i_{dc} for $\delta = -0.2$ (20μs/div)

Figure 5.20: Left: (top) Filtered input current i_{af} and the converter AC current i_a (2A/div) for phase-a along with the input voltage v_{an_i} (10V/div); (bottom) DC current i_{dc} (2A/div) time is 5ms/div. Right: zoomed in waveforms at 20 μs/div



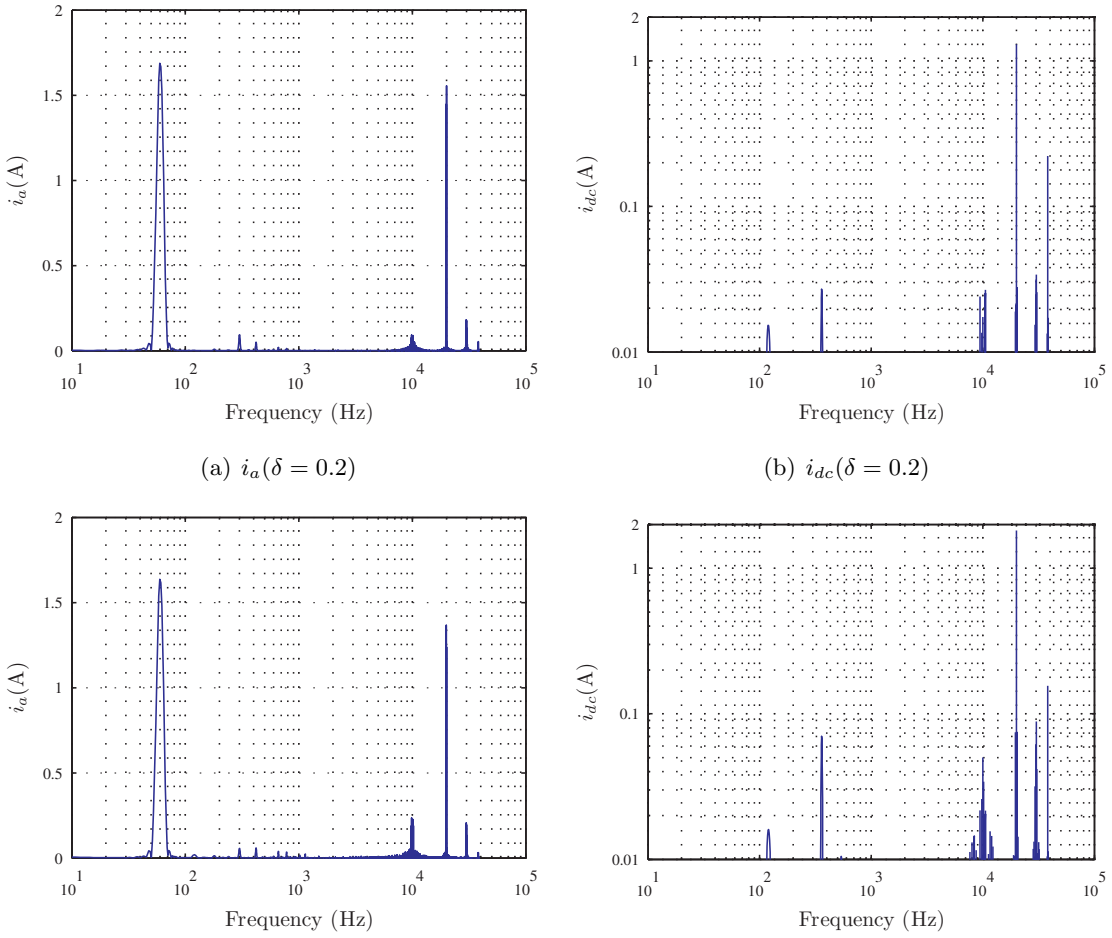
(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 5.21: Open circuit voltages: (top) Input voltage v_{ab}, transformer secondary voltage $v_{A'B'}$ and output voltage of the converter between phase A and B (50V/div). (bottom) Zoomed in section of $v_{A'B'}$ and v_{AB} at 50 μs/div



(a) $\delta = 0.2$ (b) $\delta = -0.2$

Figure 5.22: (top) Primary switch currents i_{S_1}, i_{S_2} (2A/div); (bottom) input voltage v_{an_i} and the filtered input current i_{L_f} for phase-a at 50μs/div.



(a) $i_a(\delta = 0.2)$ (b) $i_{dc}(\delta = 0.2)$

(c) $i_a(\delta = -0.2)$ (d) $i_{dc}(\delta = -0.2)$

Figure 5.23: Fourier spectrum of input and output currents

5.6 Conclusions and future work

In this research, a single-stage three-phase AC-DC PET with only two active switches on the AC-side has been analyzed in detail. This topology has all the benefits of a high-frequency transformer system:- voltage transformation ratio, isolation along with high power density. The DAB-based control provides all the benefits of DAB-converters:- soft switching, use of the transformer leakage inductance for energy transfer and compact size. The currents in this converter have high ripple percentage, however this ripple content is at $2 \times f_s$; hence, the size of the filters will be small. The high RMS values for the transformer have to be considered against the benefit of soft-switching.

In an ideal case, the switches S_1 and S_2 are ZCS therefore a clamp circuit is not required for these switches. This is not the case when the device voltage drops and circuit parasitics are taken into account. Hence, a clamp circuit is required on the primary side for the switches S_1 and S_2. It should be noted that the current through the switches is very small at the switching instant.

The power transfer for this converter is directly proportional to the phase shift δ. Bi-directional power flow is possible by changing the sign of δ. The design of the voltage controller for this converter is given in this chapter. The simulation results show that the DC voltage can be regulated under small load disturbances.

An experimental prototype of this converter has been built and tested and the experimental results verify the advantages of this converter topology.

5.6.1 Future Work

- The operation of this converter under unbalanced voltages or as a single phase converter.

Note: Parts of this chapter have been reprinted from [77] ©2012 IEEE Part of this work has been done in collaboration with Kaushik.

Chapter 6

Conclusion

In this research, PETs have been proposed for single-stage AC to AC and AC to DC power conversion with bi-directional power flow capabilities. The novelty of these converters is that they require only two controlled power electronic switches on the primary side. These primary switches operate at a constant frequency and at 50% duty ratio making them easy to control.

The features of the power electronic transformer for AC-AC conversion are listed below,

- Single-stage power conversion with high-frequency transformer isolation and bi-directional power flow capability.
- Variable frequency and amplitude pulse width modulated voltage generation.
- Variable power factor correction.
- Zero current switching (ZCS) for the primary side converter switches.
- Compact size and easy control technique that can be implemented on a single FPGA.

The features of the power electronic transformer for AC-DC conversion are summarized below,

- Single-stage power conversion with high-frequency transformer isolation and bi-directional power flow capability.

- Linear power relationship for easy control implementation.
- Unity power factor under open-loop control.

These two PETs without any intermediate storage capacitors and with their use of a high-frequency transformer link provide an efficient, reliable and high-power density solution for AC to AC and AC to DC power conversion.

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Appendix A

Acronyms

PET	Power Electronic Transformer
HFT	High-Frequency Transformer
PWM	Pulse Width Modulation
MC	Matrix Converter
PHEVs	Plug-in Hybrid Electric Vehicles
PSM	Phase Shift Modulation
DAB	Dual Active Bridge
CCW	Counter-Clockwise synchronously rotating vectors used for modulation
CW	Clockwise synchronously rotating vectors used for modulation
CCW+CW	Counter-Clockwise rotating vectors used for modulation for one cycle(T_s) and Clockwise vectors used for modulation in the next cycle
RMS	Root mean square
THD	Total Harmonic Distortion
TWD	Total Waveform Distortion
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Appendix B

Experimental Setup

B.1 Matrix converter board

The matrix converter (MC) is composed of Microsemi APTGF50TDU120PG IGBT modules that are rated for 1200V and 50A. Each module contains six IGBTs connected in common-emitter configuration as shown in Fig. B.1. A picture of the MC board is in Fig. B.2.

B.1.1 Clamp circuits

Three clamp circuits are part of the AC-AC PET setup. The primary clamp (V_{pri} in Fig. 2.10) provides a path for the transformer currents to flow during the dead-time between switches S_1 and S_2. Additionally, it provides protection in case of a fault in the switching of S_1 or S_2. The voltage of this clamp circuit is greater than $2\sqrt{3}\hat{V}_{an_i}$ so that it does not come into the circuit under normal operation. Clamp circuits are present at the input and output terminal of the matrix converter and are necessary for commutation of currents when the MC is switched. They are also required for protection during a fault in the MC. The diodes in the clamp circuit are fast acting diodes (IXYS DSEE30-12A) rated for 600V and 30A. These clamp circuits are terminated in an RC network with C=47μF and R depending on the operating point.

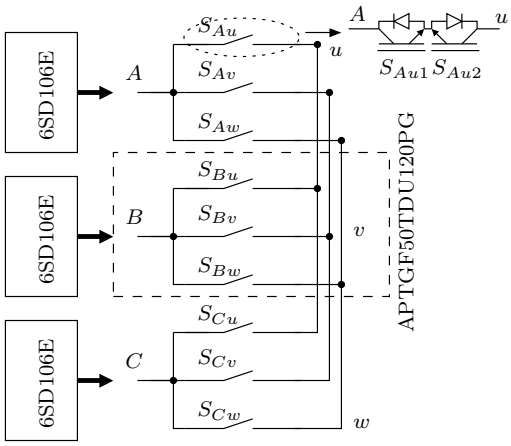


Figure B.1: Matrix converter board schematic

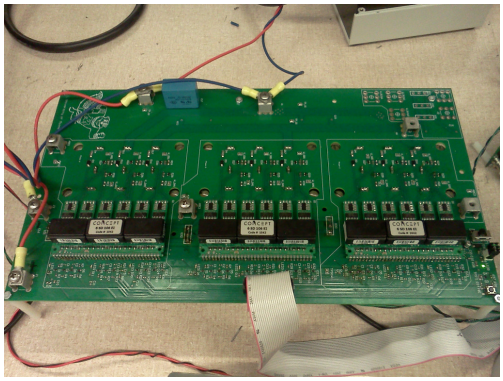


Figure B.2: Matrix converter board

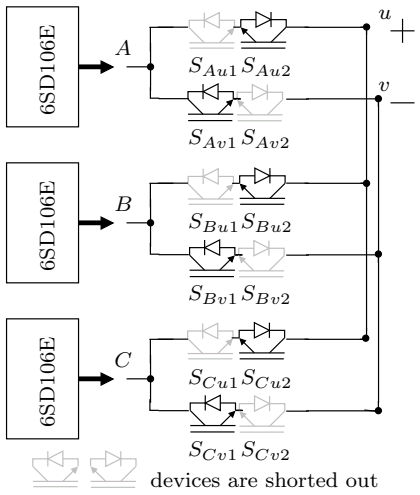


Figure B.3: Matrix converter board configured as a two-level inverter

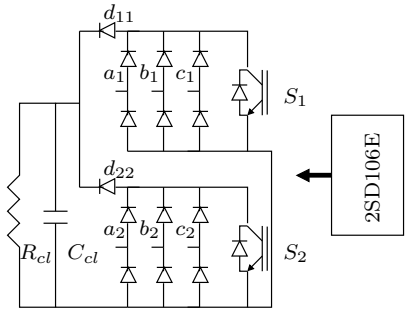


Figure B.4: Primary circuit: PET for AC-AC conversion

B.2 Two-level converter

The two-level converter is configured from the matrix converter board as shown in Fig. B.3. Some of the IGBTs switches have been shorted out to reduce the device voltage drop associated with these devices in the conduction path.

B.3 Primary circuit

1. AC-AC PET: The primary side circuit for this converter is in Fig. B.4. The primary side switches need to block a maximum voltage of $2\sqrt{3}\hat{V}_{an_i}$. SiC diodes

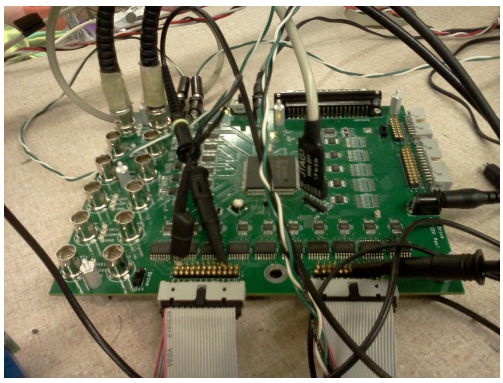


Figure B.5: FPGA control board

from CREE (C3D10065A) rated for 650V and 10A are used in the primary side diode bridges to provide benefits of zero reverse recovery current. The switches S_1 and S_2 are IXGH30N120B3 that are rated for 1200V, 30A.

2. AC-DC PETs: The diode bridges in the primary circuit are composed of (IXYS DSEE30-12A) devices. CREE (C3D10065A) diodes are used for the clamp diodes (d_{11} and d_{22}). The switches S_1 and S_2 are IXGH30N120B3 that are rated for 1200V, 30A.

B.4 Gate driver

Concept 6-pack SCALE driver 6SD106E was used in the design for the matrix converter and, 2SD 106A is used for the two switches on the primary side. All of the drivers are run independently from the FPGA control board.

B.5 Sensing and control

1. FPGA control Board: A Xilinx XC3S200E board that was developed at the University of Minnesota is used for the control of the IGBTs (Fig. B.5). The board has on-board 12-bit ADCs for sensing voltages.

2. Sensor Boards: Voltage sensor board is designed that uses an LEM sensor: LV 25-P. The output of the sensor board is conditioned using an analog sallen-key

filter. This board can also be used as a current sensor using LEM LA55-P current sensor.

Appendix C

Transformer Design

The three-phase three winding transformer shown in Fig. C.1 is designed in this section for the three-phase AC-AC PET in Fig. 2.1 driving a 1kW load at 0.8 power factor. The design is done for the operating conditions in Table. C.1. the three-winding transformers are designed according to the area product method. Faraday's law given by (C.1) results

Table C.1: AC-AC PET operating conditions

V_{in} (rms)	120 V
V_{out} (rms) ,	42.42 V
P_{total} (3 phases)	1000 W
$P_{1\phi}$	333.33 W
f_s	5 kHz
Turns ratio	1:1:1
pf	0.8

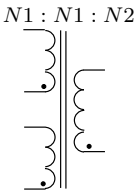


Figure C.1: Three-winding transformer

in two design constraints given by (C.2) and (C.3). The values of B_{max} depends on the material and the value of core cross section area, A_c depends on the core used. Since a ferrite core is selected, $B_{max} = 5000$ gauss (0.5T) . The turns ratio is selected to be 1:1:1, hence $N_1 = N_2$. The number of windings and the size of the conductors are constrained by the window area and the thermal considerations of the windings (C.4).

$$E = N\frac{d}{dt}\phi \tag{C.1}$$

$$\hat{V_p} = K_f N_1 B_{max} A_c f_s \tag{C.2}$$

$$\hat{V_s} = K_f N_2 B_{max} A_c f_s \tag{C.3}$$

$$A_w K_w J = N_1 I_{pri_1(rms)} + N_1 I_{pri_2(rms)} + N_2 I_{sec(rms)} \tag{C.4}$$

For this three winding transformer, $I^2_{pri_1(rms)} + I^2_{pri_2(rms)} = nI^2_{sec(rms)}$. Depending on the matrix converter switching, the primary windings may or may not carry the same RMS currents. In this design it is assumed that the primary winding currents are equal, $I_{pri_1(rms)} = I_{pri_2(rms)} = n\frac{I_{sec(rms)}}{\sqrt{2}}$ where, $n = N_2/N_1$. The area product is given by (C.5). Due to modulation of the matrix converter, the transformer secondary RMS current is given by (C.6), where, $\hat{I_o}$ is the peak of the output current. The transformer design parameters are given in Table C.2. The designed transformer is in Table C.3. Thanks to Hirel Systems for winding the three transformers in Fig. C.2.

$$A_w A_c = \frac{n\hat{V_{in}}}{K_f B_{max} f K_w J}[\sqrt{2}+1]I_{sec(rms)} \tag{C.5}$$

$$I_{sec(rms)} = \frac{0.866}{\sqrt{2}}\hat{I_o} \tag{C.6}$$

The transformers are characterized using an LCR meter, the leakage inductance for these transformers is approximately 15μH and the magnetizing inductance is around 50mH.

Table C.2: Transformer design parameters

$P_{1\phi}$	333.33 W
$\hat{I_o}$	13.99A
$I_{sec(rms)}$	8.505 A
f_s	5 kH
Turns ratio	1:1:1
B	0.000015 $V-s/cm^2$
K_w winding factor	0.3
K_f square wave excitation	4
J	300 A/cm^2

Table C.3: Designed transformer

Core	MAG INC 0P49928EC
A_c	6.92 cm^2
A_w	21.223 cm^2
A_p	146.86316 cm^4
$N_1 = N_2$	82 (2*AWG 17)

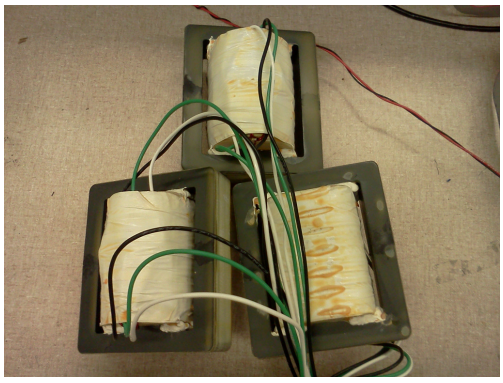


Figure C.2: Picture of the three three-winding transformers

Appendix D

FPGA Code for AC-AC Power Electronic Transformer

The MC based PET is controlled using a Xilinx XC3S500 FPGA. The FPGA algorithm in Fig. D.1 is written in Verilog HDL using Xilinx ISE 12.3. The pulses for S_1 and S_2 are at 10kHz and nearly 50% duty with a dead-time of 1.5μs between the transition of S_1 and S_2. The input voltages between phase a and b and phase a and c are sensed using LV25 hall effect sensors. These sensed voltages are discretized using a 12-bit ADC and are given by V_{ab} and V_{ac} respectively. Vxi and Vyi in (D.1) and (D.2) are intermediate values that depend on the type of vector used for modulation. The input voltages are transformed into a stationary reference frame (abc $\rightarrow \alpha\beta$). The resulting stationary frame voltages are $V_{\alpha i}$ and $V_{\beta i}$. The $\alpha\beta$ voltage references for the output voltages are $V_{\alpha o}$ and $V_{\beta o}$ respectively and are generated inside the FPGA using CORDIC 12-bit sine and cosine generator.

$$Vxi = V_{ab} + V_{ac} \tag{D.1}$$

$$Vyi = \begin{cases} -V_{ab} + V_{ac} & \text{for CCW vectors} \\ V_{ab} - V_{ac} & \text{for CW vectors} \end{cases} \tag{D.2}$$

$$V_{\alpha i} = Vxi/2 \qquad V_{\beta i} = (\sqrt{3}/2) \times Vyi \tag{D.3}$$

$$|V_i|\angle\theta_i = V_{\alpha i} + jV_{\beta i} \quad |V_o|\angle\theta_o = V_{\alpha o} + jV_{\beta o} \tag{D.4}$$

When CCW rotating vectors are used, the input voltage vector in the stationary

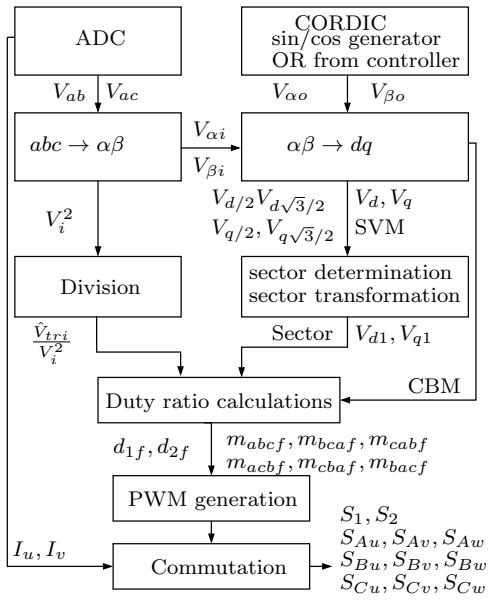


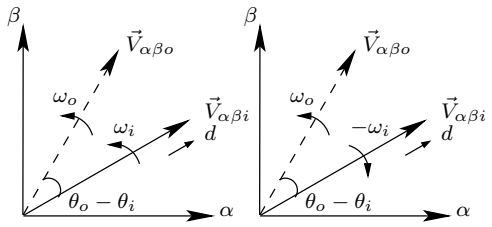
Figure D.1: FPGA algorithm: AC-AC PET

reference frame rotates in the the same direction as the output voltage vector as shown in Fig. D.2(a). When CW vectors are used, the input and output voltage vectors rotate in opposite directions as shown in Fig. D.2(b). The d-axis is aligned with $V_{\alpha i}$ as shown in Fig. D.2(a) and the output voltage is transformed into this reference frame. The d-axis component of the output reference voltage is the projection of $V_{\alpha\beta o}$ on $V_{\alpha\beta i}$ i.e. $|V_{\alpha\beta o}|\cos(\theta_o - \theta_i)$ and the q-axis component of the output reference voltage is the the quadrature component i.e. $|V_{\alpha\beta o}|\sin(\theta_o - \theta_i)$. In order to optimize the number of multiplications and divisions, the calculations are done using $\cos(\theta)$ and $\sin(\theta)$ scaled by K. There is only one division operation (D.9) every switching cycle to calculate the inverse of V_i^2.

$$\theta = \theta_o - \theta_i, \qquad K = |V_o||V_i| \tag{D.5}$$

$$V_d = K\cos(\theta) = V_{\alpha o} \times V_{\alpha i} + V_{\beta o} \times V_{\beta i} \tag{D.6}$$

$$V_q = K\sin(\theta) = V_{\beta o} \times V_{\alpha i} - V_{\alpha o} \times V_{\beta i} \tag{D.7}$$



(a) CCW vectors (b) CW vectors

Figure D.2: Stationary reference frame

$$V_i^2 = (1/2^2)Vxi \times Vxi + (3/2^2)Vyi \times Vyi \tag{D.8}$$

$$V_{inv} = \hat{V}_{tri}/V_i^2 \tag{D.9}$$

$$V_{d/2} = V_d/2 \qquad V_{d\sqrt{3}/2} = \sqrt{3}V_d/2 \tag{D.10}$$

$$V_{q/2} = V_q/2 \qquad V_{q\sqrt{3}/2} = \sqrt{3}V_q/2 \tag{D.11}$$

D.1 Carrier Based Modulation

The modulation indices for the 6 synchronously rotating vectors when S_1 is on are given by (D.12)–(D.14); where, $\theta_i = \theta_i + \pi$ when S_2 is on. Instead of determining the angle and then performing sine and cosine operations, trigonometric identities are used to reduce the number of computations significantly, leading to saving of space in the FPGA. (D.17)–(D.18) are used in the computation of the modulation indices for CCW vectors. When S_2 is on, the magnitudes of Vxi and Vyi are the same as when S_1 is on but the sign is opposite. Hence in (D.17)–(D.18), $k = 0$ when S_1 is on and $k = 1$ when S_2 is on. V_{inv} is unaffected by the sign of Vxi and Vyi; hence, it needs to be computed only once every switching cycle. The same equations are valid for modulation indices

for CW vectors.

$$m_{ABC}, m_{ACB} = 1/3 + (2m/3)\cos(\theta) \tag{D.12}$$

$$m_{CAB}, m_{BAC} = 1/3 + (2m/3)\cos(\theta - 2\pi/3) \tag{D.13}$$

$$m_{BCA}, m_{CBA} = 1/3 + (2m/3)\cos(\theta - 4\pi/3) \tag{D.14}$$

$$\theta_{ccw} = \theta_o - \theta_i \quad \theta_{cw} = \theta_o + \theta_i \tag{D.15}$$

$$m = |V_o|/|V_i| \tag{D.16}$$

$$m_{abcf}, m_{acbf} = V_{tri} + (-1^k)2V_{inv}V_d \tag{D.17}$$

$$m_{bcaf}, m_{cbaf} = V_{tri} + (-1^k)2V_{inv}(-V_{d/2} - V_{q\sqrt{3}/2}) \tag{D.18}$$

$$m_{cabf}, m_{bacf} = V_{tri} + (-1^k)2V_{inv}(-V_{d/2} + V_{q\sqrt{3}/2}) \tag{D.19}$$

Since, the modulation indices are scaled by $3V_{tri}$, the sawtooth carrier wave will have a peak value of $3V_{tri}$. Every $T_s/2$, the sequence of vectors applied is (ABC), (BCA) and (CAB) when CCW vectors are employed and (ACB), (CBA) and (BAC) when CW vectors are employed. These switching pulses are routed to the appropriate switches and either four-step commutation or dead-time commutation is performed. Carrier-based FPGA implementation can also be used in a MC by setting $k = 0$. The total of fifteen 18-bit multipliers were used in this implementation.

D.2 Space Vector Modulation

The duty-ratios for SVM are calculated only after the sector is correctly determined. Using the dq-components, the sector of operation is determined according to Fig. D.3. Once the sector is known, using trigonometric identities, the V_{d1}, V_{q1} values are transformed into the first sector according to Table D.1. The values of $V_{d/2}, V_{q/2}, V_{d\sqrt{3}/2}$ and $V_{q\sqrt{3}/2}$ that are given by (D.10)–(D.11) are calculated only once every switching cycle. V_{tri} in (D.9) is the peak of the triangular wave that the duty ratios d_{1f} and d_{2f} (D.21)–(D.20) are compared with to generate the PWM pulses for the appropriate active vector. For 120 switching cycles, vector (AAA) is selected as the zero vector for the next 120 cycles (BBB) is selected and the following 120 cycles (CCC) is used. Depending on the sector and kind of vector (clockwise or counter-clockwise) to be applied, these switching

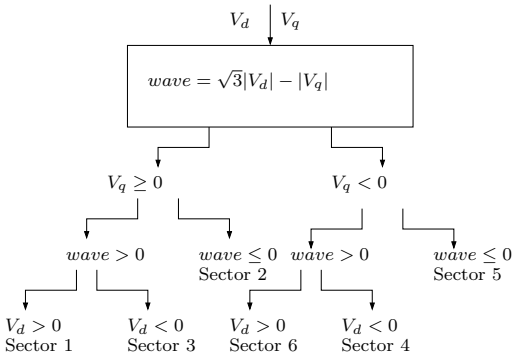


Figure D.3: SVM: Sector Determination

pulses are routed appropriately. All multiplications and divisions by 2 are performed by shift operations. The FPGA implementation uses sixteen 18-bit multipliers in the FPGA.

Table D.1: Sector Transformation

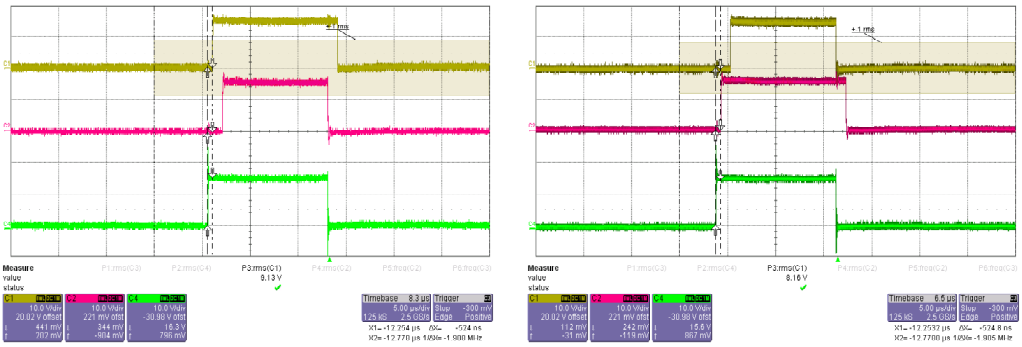
Sector	V_{d1}	V_{q1}
1	V_d	V_q
2	$V_{d/2} + V_{q\sqrt{3}/2}$	$V_{q/2} - V_{d\sqrt{3}/2}$
3	$-V_{d/2} + V_{q\sqrt{3}/2}$	$-V_{q/2} - V_{d\sqrt{3}/2}$
4	$-V_d$	$-V_q$
5	$-V_{d/2} - V_{q\sqrt{3}/2}$	$-V_{q/2} + V_{d\sqrt{3}/2}$
6	$V_{d/2} - V_{q\sqrt{3}/2}$	$V_{q/2} + V_{d\sqrt{3}/2}$

$$d_{2f} = V_{inv} \times V_{q1} \times (\sin \pi/3)^{-}1 \tag{D.20}$$

$$d_{1f} = V_{inv} \times V_{d1} - d_{2f}/2 \tag{D.21}$$

D.3 Commutation

The commutation of switches is done either using dead-time commutation or four-step commutation. The currents for phase u and phase v are sensed at 100kHz using sensors LA55-P. The current for phase w is determined from phase u and v currents. If the direction of phase currents are accurately known, four-step commutation is performed



(a) $i_u \geq 0$ (b) $i_u < 0$

Figure D.4: Four-step commutation pulses: C1: S_{Au1}; C2:S_{Au2}; C4: ideal pulse

else dead-time commutation is performed. In this code, the dead-time (t_{dt}) is set to 1.5μs. The time for each step in four-step commutation is 500ns. The gate pulses for four-step commutation of S_{Au1} and S_{Au2} are shown in Fig. D.4. Thanks to Rohit Baranwal for the verilog state-machine for four-step commutation.

Note: Parts of this chapter have been reprinted from [60]

Appendix E

FPGA Code for AC-DC Power Electronic Transformer

The single-phase and three-phase AC-DC PETs are controlled using a Xilinx XC3S500E FPGA. In entire switching algorithm is written in Verilog HDL.

E.1 Single-phase AC-DC Power Electronic Transformer

The input and output voltages, V_i and V_o are sensed using LV-25 voltage sensors and their values discretized by 12-bit ADCs. The ADCs sample these voltages at 10kHz.

The pulses for S_1 and S_2 are at 10kHz and nearly 50% duty with a dead-time of 1.5μs between the transition of S_1 and S_2. Xilinx CORE Generator division block is used to perform a 16-bit division on V_o. The inverse of V_o is multiplied with the input to generate a duty ratio given by (E.2). A saw-tooth carrier wave counts from 0 to V_{saw} every 50μs as shown in Fig. E.1. This sawtooth waveform is compared with the duty ratio to generate phase shifted PWM pulses. Depending on the polarity of the input voltage, the pulses are routed to the appropriate switches. A dead-time of 1.5μs is introduced between the switching pulses of the switches in the same leg of the secondary side converter. The modulation is suspended in this converter for the following cases : 1) If $V_{dc} < V_i$ 2) If the phase shift is too high $\frac{V_{saw}}{2} - \frac{d}{2} + \delta \leq 0$ or if $\frac{V_{saw}}{2} + \frac{d}{2} + \delta > V_{saw}$.

3) If d is too small.

$$V_{inv} = \frac{V_{saw}}{V_o} \tag{E.1}$$

$$d = V_{inv} \times V_i \tag{E.2}$$

$$\tag{E.3}$$

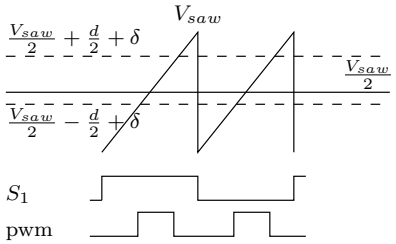


Figure E.1: FPGA implementation: Single-phase AC-DC PET

E.2 Three-phase AC-DC Power Electronic Transformer

A brief description of the algorithm shown in Fig. E.2 is given in this section.

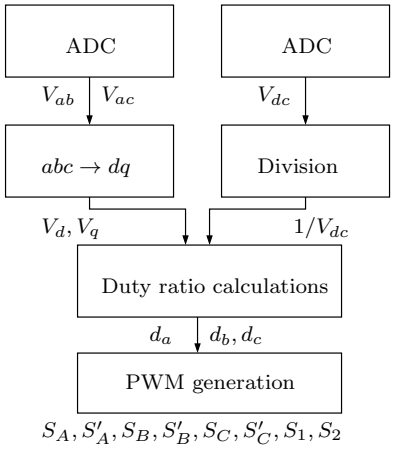


Figure E.2: FPGA algorithm: Three-phase AC-DC PET

The input voltages, V_{ab}, V_{ac} and V_{dc} are sampled at 10kHz using 12-bit ADCs. The division, V_{saw}/V_{dc} is done using Xilinx CORE Generator 16 bit division.

The input AC voltages V_{ab} and V_{ac} are converted to dq-stationary reference frame using (E.4)- (E.6). The values of $V_{d/2}, V_{q/2}, V_{d\sqrt{3}/2}$ and $V_{q\sqrt{3}/2}$ that are given by (D.10)–(D.11) are calculated only once every switching cycle. The sector can be determined by checking the sign of *wave* (E.7) , V_d and V_q as shown in Fig. D.3. Just as in the AC-AC SVM implementation, the values of of V_d and V_q are transformed into Sector 1 and are given by Table. D.1.

$$Vxi = V_{ab} + V_{ac} \tag{E.4}$$

$$Vyi = -V_{ab} + V_{ac} \tag{E.5}$$

$$V_d = \frac{Vxi}{2} \qquad V_q = \frac{\sqrt{3}}{2} \times Vyi \tag{E.6}$$

$$\begin{aligned} wave &= \sqrt{3}|V_d| - |V_q| \\ &= \frac{\sqrt{3}}{2}(|Vxi| - |Vyi|) \end{aligned} \tag{E.7}$$

In each sector, once V_{d1} and V_{q1} are known, the duty ratios for the adjacent vectors can be calculated using (D.20) and (D.21). The duty ratios are routed to the PWM block where the the phase-shifted PWM pulses for the switches are generated as shown in Fig. E.1. A dead-time of 1.5μs is introduced between the switching transitions in an inverter leg. Depending on the sector and switching state of the primary side switches S_1 and S_2, these PWM pulses are routed to the correct switches.

The selected FPGA has twenty dedicated 18-bit hardware multipliers. In this code only six hardware multipliers are used.