CMOS CIRCUITS FOR MULTI-ANTENNA COMMUNICATION SYSTEMS

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SATWIK PATNAIK

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Dedicated to my parents,

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Sujata Patnaik,

and my sister,

Satroopa Patnaik.

Abstract

Multi-antenna systems allow for higher communication rates without substantial increase in hardware and power. This has led to significant interest in incorporating multi-antenna communication into upcoming wireless standards, like the 802.11n.

This thesis focuses on CMOS circuits and architectures for multi-antenna wireless communication systems. Specifically, we will propose solutions for a special class of multi-antenna systems called phased-array systems. The most important circuit block in a phased-array system is the phase-shifter. Traditional phased-array systems, mostly military radars, used external ferrite phase-shifters for microwave applications, which were wide-band, almost noiseless, highly linear and had high power-handling capability, but were bulky. Commercial wireless systems rely on portability and low-power, with the result that CMOS is the technology of choice and most products are fully integrated on a single-chip. On-chip CMOS phase-shifters have not been able to match the performance of ferrite phase-shifters. Consequently, CMOS-based phased-array systems have relied on a modified architecture known as the LO-phase shifting architecture to deliver comparable performance. In this work, we first present two novel schemes for the phase-generation network for the LO-phase-shifting architecture, based on a phenomenon called injection-locking. The injection-locked oscillator (ILO) is used as a phase-shifter. The two schemes are integrated into a dual-mode architecture for a phased-array receiver providing us with the advantages of both. The prototype, operating at 2.4-GHz, is fabricated in a 0.13-μm CMOS technology. It requires lower power and area compared to previous state-of-the-art designs. Measurement results from this prototype show excellent agreement with the theoretical performance predicted for the phased-array receiver. Both architectures have also been extended to two-dimensional

phased-array systems.

A majority of the commercial phased-array applications are focused on the mm-wave regime. We have verified that our architecture can operate at these frequencies as well. A 24-GHz two-channel CMOS phased-array receiver has been designed and fabricated in 0.13-μm BiCMOS technology. In this architecture, the injection-locked oscillator not only acts as a phase-shifter and buffer, but also as a frequency tripler. Because of this multi-functionality of the ILO, the overall area and power of this receiver are better than other state-of-the-art designs. Since the LO distribution network now operates at one-third the LO frequency, it allows for further power savings in the distribution network.

Finally, a beam-forming receiver based on the Fast-Fourier Transform (FFT) is presented. In this architecture, the beam-forming operations are performed in the base-band processing section. Owing to a low-power FFT architecture and the inherent properties of the FFT, multiple beams can be created at closely-spaced frequencies. This allows the use of narrow-band transmitter and receiver architectures for the RF section. A two-channel receiver based on this architecture has been designed in a 65-nm CMOS process.

In addition, to these different receiver architectures, a novel 24-GHz UWB-LNA is presented. The LNA, which has been integrated as part of a UWB receiver, is presented in this thesis. However, the overall UWB receiver design is not presented here.

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Chapter 1

Introduction

The wireless market has seen explosive growth in terms of the number of wireless devices in common use today. What is astounding is that this has mostly come about only in the last two decades. Counting the number of cellular phones alone (4.6 billion against a world population of 6.8 billion, as of 2009), gives us an idea of the potential of wireless devices in day-to-day life. And their demand is only going to increase in the future. The primary reason behind this, is the ability to integrate them in CMOS technology.

1.1 Wireless Communications

Although the field of wireless communication came into existence at the advent of the 19th century, it was heavily restricted in use for commercial purposes. Television receivers and AM radios were the only wireless communication devices for civilian applications till the widespread use of cellular phones began in the early 1980s. Today, there are multiple wireless standards being used in day-to-day life. Table 1.1 lists some of these current and future communication standards for commercial applications, along with their corresponding data rate, frequency of operation and coverage range.

Table 1.1: Comparison of a few commercial wireless communication standards

Commercial name	Standard	Theoretical data rates	Max Range	Frequency (GHz)
Bluetooth	IEEE 802.15.1	2Mb/s	100m	2.4
Zigbee	IEEE 802.15.4	250Kb/s	10m	2.4
WiFi	IEEE 802.11a	54Mb/s	30m	5.5
WiFi	IEEE 802.11g	54Mb/s	100m	2.4
WiFi	IEEE 802.11n	300Mb/s	30m	2.4/5.5
WiMAX	IEEE 802.16a	70Mb/s	50km	2.5/3.5/5.8
mm-wave WPAN (proposed)	IEEE 802.15.3c	10Gb/s	10m	57-64

Wireless communication is also of considerable interest for military applications. In fact, most of the wireless communication technologies and techniques in civilian use today such as spread-spectrum, frequency hopping, global positioning, etc. were initially developed for and used by the military for many decades. The two world wars fueled active research in wireless radios for detection and ranging, resulting in RADARs, and stealth wireless communication technologies (such as spread-spectrum). Many of these technologies were declassified by the Federal Communications Commission (FCC) in the 1970s and 1980s, and were immediately adopted for civilian applications.

1.2 CMOS Technology

The semiconductor industry has witnessed unprecedented growth in the last three decades. In order to increase functionality, speed and capacity, and reduce power and area, silicon technology has constantly evolved. The de-facto standard for semiconductor technology is the feature size for the gate length in a complementary metal-oxide semiconductor (CMOS) transistor. Market pressures from the microprocessor and memory industry, aided by Moore's law, have forced scaling of the feature sizes down to the nanometer regime.

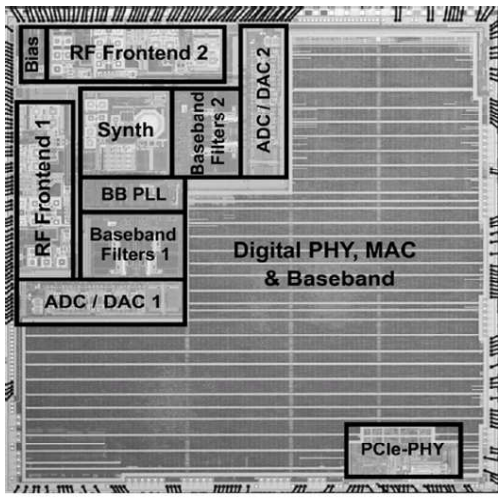


Figure 1.1: Die micrograph of an 802.11n radio [1]; majority of the area occupied by digital section (70%)

From the point of view of digital circuits, reducing feature-size has few cons and mostly only benefits its design. However, for analog-circuits, reducing feature-size creates a *mixed bag*. On the one hand, it reduces parasitic capacitance and improves the transconductance, resulting in higher cut-off frequencies (f_T) for devices and circuits. It also reduces the area occupied by analog circuits and improves matching (when compared to a similar-sized device in an older technology). On the other hand, it reduces the gain offered by a single transistor, making the design of analog high-gain amplifiers difficult. Further, to combat sub-micron effects such as drain-induced barrier lowering and sub-threshold leakage, the doping of the silicon substrate is increased compared to previous technology. This reduces the isolation offered by the substrate, compared to previous technologies and increases high-frequency signal leakage. Especially, in mixed-signal circuits, leakage from the digital section severely affects the analog/RF section. Further, with the lowering of supply voltages, the power handling capability of the transistors is greatly reduced.

Most modern radios for wireless communications integrate the RF and analog section

with the digital processing section on a single chip. The advantage of doing so, other than reduced cost, is the ability to finely calibrate analog mismatches and imperfections with relatively *free* digital solutions. As illustrated by the die micrograph of an 802.11n transceiver from Atheros Communications [1] in Fig. 1.1, majority of the area is occupied by the digital processing section in a modern wireless transceiver. As a result, most radios are implemented in the newest CMOS technologies, that are most attractive to digital circuits.

Until the last decade, RF and microwave circuits were almost exclusively designed in III-V technologies such as GaAs or InP, because of their higher transistor f_Ts and power handling capability. Radios designed in these technologies were expensive and limited to military use. However, CMOS and BiCMOS technologies have caught up with these exotic technologies and in fact, have been predicted to supersede III-V semiconductor devices in terms of transistor speed in the coming years. Fig. 1.2 plots the f_T of a transistor in a given technology, as projected by the International Technology Roadmap for Semiconductors (ITRS) in 2009 [2]. This has also attracted the military community with a greater interest in increasing the share of silicon-based technologies in military radios. With the f_T and f_{max} of CMOS technologies going beyond 200GHz, it has become the technology of choice for radio integration for use in newer mm-wave wireless standards. Consequently, CMOS-based technologies have been used for all prototypes described in this dissertation.

1.3 Organization

This dissertation focuses on the design of CMOS-based circuits for high-speed RF/mm-wave wireless communication. The architectures and circuits introduced in this work are specifically geared towards beamforming in wireless communications. Measurement results from two prototypes based on the proposed architectures verify their performance.

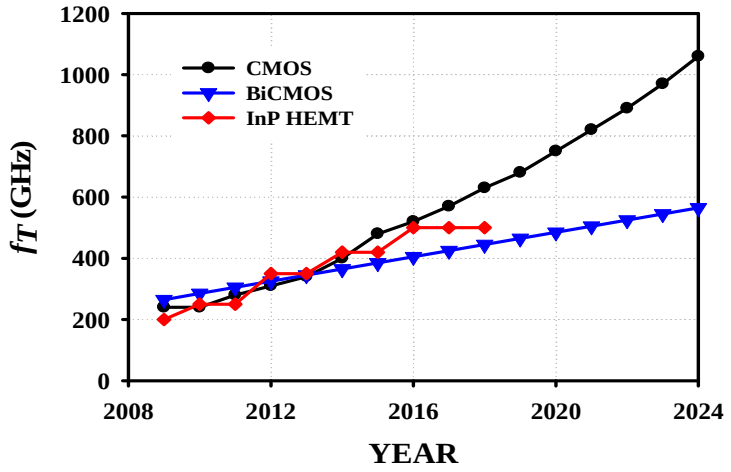


Figure 1.2: Speeds available from silicon technologies (CMOS and BiCMOS) compared to III-V, according to ITRS'09

Two additional prototypes have been presently submitted for fabrication.

Chapter 2 introduces the fundamentals of RF transmitters, receivers and frequency synthesizers. Here we also discuss the concept of multi-antenna communication, its advantages and disadvantages, with a special emphasis on phased-arrays. Next, the basic architectures for phased-array transmitters and/or receivers are briefly explained.

Chapter 3 discusses the phenomenon of injection-locking in LC-oscillators. This is important because injection-locked LC-oscillators form the basis of the next three chapters. In this chapter, different mathematical models which portray the transient process of locking in the LC-oscillator are explained. The most widely used model for the injection-locked oscillator - Adler's model - is extended to quadrature injection-locked oscillators.

Chapter 4 focuses on the application of injection-locked oscillators to phased-arrays. First, it presents an overview of previous architectures for phased-arrays utilizing injection-locking. Next, it proposes two schemes for phase-pattern generation. Finally, these schemes are translated into two receiver architectures.

In Chapter 5, a receiver is described which integrates the two receiver architectures into a dual-mode architecture. The chapter covers the circuit design and architecture details. Measurement results from a fabricated prototype validate the operation and feasibility of the receiver.

Phased-arrays are being targeted for milli-meter wave wireless communication. Chapter 6 extends the proposed receiver architecture to mm-waves and allows for additional power savings by running the LO distribution at one-third of the RF frequency. Measurements results from a prototype receiver verify the design.

Chapter 7 proposes a new scheme to achieve multiple beamforming for radar applications. The concept of fast-fourier transform is harnessed to separate individual frequencies into bins and separate bin-level processing is used to achieve independent beam control. A two-channel receiver based on this architecture is presented and the design is currently under fabrication.

Chapter 8 presents an ultra-wideband low-noise amplifier (LNA) operating around 24GHz. The amplifier uses transformers for impedance matching as well as for output driving. The LNA is presently being fabricated as a part of an ultra-wideband receiver.

Chapter 9 concludes this thesis and highlights the important contributions of the work in the field of RF circuit and architectures for multi-antenna wireless communication.

Chapter 2

Background

A wireless communication or ranging system consists of a transmitter and a receiver. The transmitter (TX) as the name suggests transmits the signal and the receiver (RX) receives and decodes the signal. Most wireless communication systems consist of both the transmitter and the receiver, which often share the antenna. The combination of the transmitter and the receiver is called a transceiver. The channel between the TX and the RX can be a combination of dielectric media, a majority of which is usually free space. The type of environment in which the TX and RX operate dictates many of the design constraints of their various constituent blocks. We explain the basic concepts and circuit blocks, which constitute the TX and RX, in the next three sections. Then we discuss multi-antenna communication, with an emphasis on phased-arrays.

2.1 Transmitter

The TX of a wireless system delivers signal power to the antenna which transmits it into free-space. A TX, as shown in Fig. 2.1, consists of the base-band (BB) section, the frequency synthesizer, the up-conversion mixer and the power-amplifier. The frequency

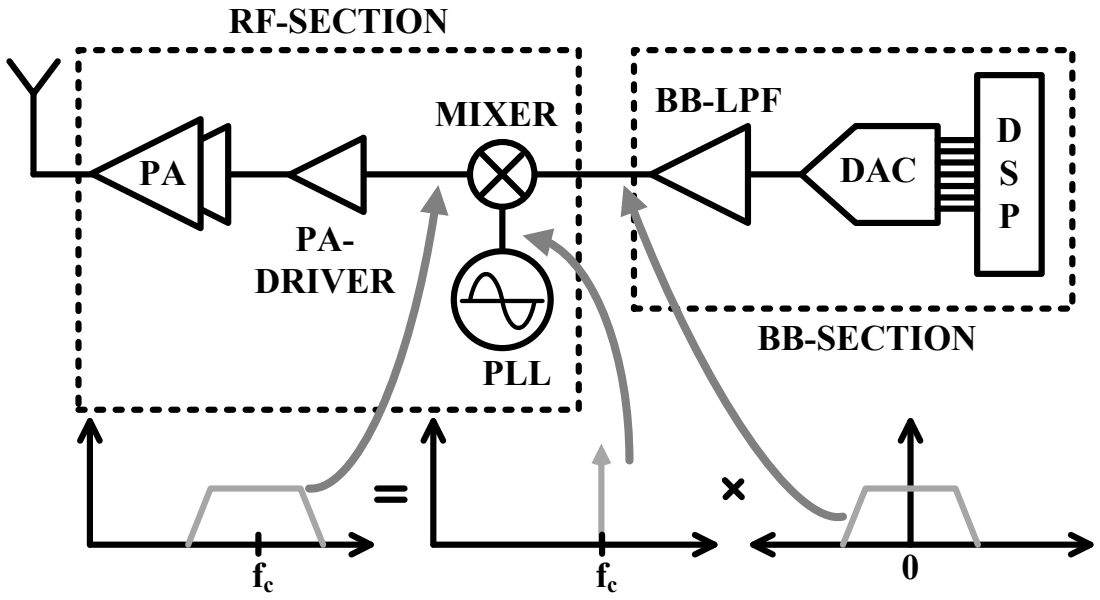


Figure 2.1: A basic transmitter architecture

synthesizer, the up-conversion mixer and the power amplifier form the RF section of the receiver.

The base-band processing section consists of the digital sub-section, the digital-to-analog converter (DAC) and the analog sub-section. The digital sub-section of the transmitter performs the signal or symbol generation. The DAC converts the digital bits into analog waveform. The analog sub-section amplifies the analog output of the DAC. In some architectures, the baseband section also consists of an intermediate frequency (IF) section, in which the baseband analog waveform is up-converted to an IF, which is much lower than the intended carrier frequency.

The frequency synthesizer generates the carrier signal on which the analog waveform or data rides. The frequency synthesizer usually consists of a phase-locked loop (PLL), which shall be discussed in more detail in Section 2.3. In the case of the transceiver, the frequency synthesizer section is shared between the TX and the RX.

The up-conversion mixer translates the baseband (or IF) signal to the carrier frequency, as shown in Fig. 2.1. The mixer multiplies the carrier frequency signal to the input baseband (or IF) signal to perform this translation. This signal is then driven into the antenna using a power amplifier (PA). The PA is the most critical block of the transmitter. It needs to deliver a significant amount of power to the antenna, ranging from a few hundred milliwatts (+15-20dBm as in the case of wireless local-area networks or WLANs) to a few watts (+30-35dBm in case of cellular phones). Since the efficiency of PAs is far from ideal, the unused power is dissipated thermally and results in heating issues. Consequently, in many applications, the PA is off-chip. Also, the technology of choice for the high-power PAs is usually III-V, owing to their higher power handling capability. CMOS-based PAs have proven to deliver up to a few watts of power [3, 4]. Sub-watt-level CMOS PAs are routinely integrated into the transceiver for short-range wireless applications, such as wireless LAN. But due to lower efficiencies of watt-level CMOS PAs compared to their III-V-based counterparts, integrating them on-chip is certainly non-trivial. The signals out of the up-conversion mixer are shaped to ensure that they meet the FCC spectral mask conditions at the output of the PA/antenna. Since the signal level at the output of the PA is usually high, linearity of the PA becomes paramount. Any non-linearity in the PA creates harmonics and IM3 signals, in addition to the fundamental signal band. This can result in the output signal not meeting the FCC spectral mask conditions. Hence, the PA linearity also places a stringent constraint in its design.

2.2 Receiver

The basic receiver architecture is shown in Fig. 2.2. It consists of the low-noise amplifier (LNA), down-conversion mixer, the frequency synthesizer and the baseband section. In the case of a receiver, the LNA, mixer, frequency synthesizer and any blocks between

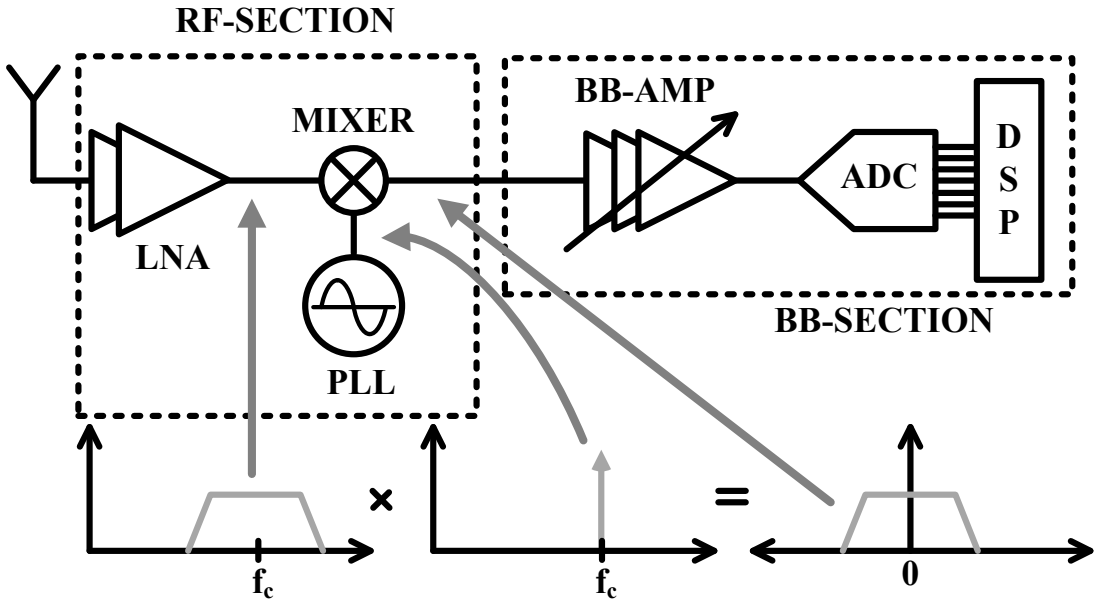


Figure 2.2: A basic receiver architecture

the LNA and the mixer form the RF section. The baseband section comprises of the baseband amplifier(s), the analog-to-digital converter (ADC) and the digital signal processing section.

In the case of the RX, the signal received at the antenna is extremely low in power. At the same time, the antenna also receives background noise, which results in a finite signal-to-noise ratio (SNR) at the antenna itself. The LNA amplifies this RF signal along with the received noise within its bandwidth. However, any circuit block exhibits its own device noise. This deteriorates the SNR at the output of each block. The LNA ensures that the additional circuit noise being added at the beginning of the receiver is minimal. The signal is then mixed down to an IF or baseband depending upon the architecture of the RX. Since this action can cause the image frequency to also mix down the IF or baseband, an image-reject filter may be inserted between the LNA and the mixer to filter out the image-frequency band.

The IF or baseband signal is then amplified and processed by the baseband section.

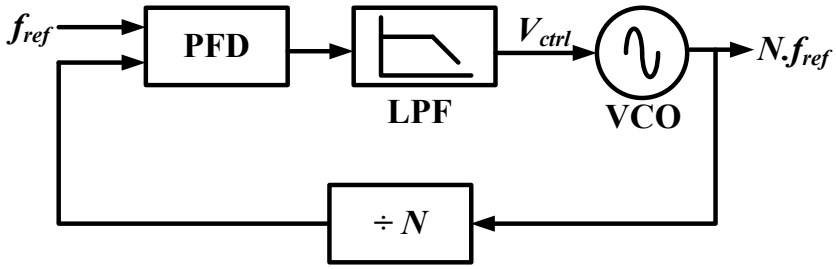


Figure 2.3: PLL block diagram

Since amplifiers in the RF domain are expensive in terms of power, most of the signal amplification is done at the baseband level. The signal received at the antenna can vary in strength depending upon the distance from the TX, which is transmitting it. Hence, the gain from the LNA input to the ADC needs to be programmable, so as to increase it when signal is low and vice-versa. This is achieved by designing various stages in the RF and the baseband analog section to be of variable gain.

The ADC design in the baseband section is critical since it has to operate under stringent specifications for linearity, (added) noise, dynamic range and power. The DSP in this baseband section is also more intensive than in the case of the transmitter, since this section performs multiple operations, *viz.*, equalization, complex (very high-order) filtering, symbol detection and estimation.

2.3 Frequency Synthesizer and the VCO

Frequency synthesizer is most commonly realized by using a phase-locked loop or PLL. A PLL synchronizes the output signal, voltage controlled oscillator (VCO) signal here, to the phase (and frequency) of a reference. A VCO as a stand-alone frequency generator suffers from problems of frequency drift and degraded phase noise. Synchronizing it to a stable reference eliminates these problems and synthesizes a pure frequency tone.

Fig. 2.3 shows the basic block diagram of a PLL. A PLL comprises three critical

blocks: a phase detector, a low-pass filter and a VCO. The phase detector (PD) compares the phases of the reference signal and the VCO output and generates a voltage proportional to their difference. This voltage is low-pass filtered to eliminate any ripple and is provided as a control voltage (V_{ctrl}) to the VCO. The VCO then produces an output frequency proportional to the control voltage. In the case there is a phase mismatch at the input, the frequency of the VCO is altered in a direction that reduces this phase error. When a steady-state is reached, the average frequencies of the input reference and VCO are exactly equal, and depending on the DC loop gain of the PLL, a finite phase error may remain to maintain the VCO at the altered frequency.

In the case of frequency multiplication, a (programmable) divider is included in the loop. Here the phase of the divided VCO output is compared against the reference frequency and imposes the condition $f_{ref} = \frac{f_{out}}{N}$ where N is the divide ratio. The simplicity of the integer-N PLL architectures makes them a popular choice in monolithic implementation. The primary drawback in these is that the output frequency can only be changed in the steps of f_{ref}. If smaller frequency steps are required, the reference frequency should be made really small. This heavily constrains the loop bandwidth as it is chosen to be a fraction of f_{ref} because of stability issues. The presence of spurs mandates a smaller bandwidth. Narrow loop bandwidths result in long acquisition and settling times. In applications where very small frequency steps are required, a fractional-N divider is often used. In fractional-N frequency synthesizers, *fractional* multiples of the reference frequency can be synthesized. This allows the use of larger reference frequency and therefore wider loop-bandwidths for a required frequency resolution.

Linear model for PLL

PLL systems are inherently nonlinear due to the nonlinear phase detector in the loop. In steady state however, when the loop is in lock, the PLL can be approximated as an

LTI system. In the locked state, the input-output phase error is small and the phase detector is assumed to operate in the linear region. The linear model for the PLL is shown in Fig. 2.4.

The input to the linearized system is the phase of the reference frequency. The PD generates a voltage directly proportional to this difference phase, given by

$$V_{PD} = K_{PD}\Delta\phi \tag{2.1}$$

where K_{PD} is the PD gain and $\Delta\phi$ is the input phase difference. The loop-filter is represented by the transfer function $G(s)$. Since phase is the integral of frequency, the transfer function from the input of the VCO (V_{ctrl}) to output (ϕ_{out}) is that of an integrator as shown by the transfer function in (2.2).

$$\phi_{out} = \frac{K_{VCO}}{s}V_{ctrl} \tag{2.2}$$

The open-loop transfer function is given by

$$H_{ol}(s) = \frac{K_{PD}K_{VCO}G(s)}{Ns} \tag{2.3}$$

The closed-loop transfer function of the PLL is then given by equation

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{K_{PD}K_{VCO}G(s)}{s + \frac{K_{PD}K_{VCO}G(s)}{N}} \tag{2.4}$$

The order of the polynomial in the denominator of the closed-loop transfer function (2.4) is called the order of the PLL. In the case of (2.4), the loop-filter order determines the overall order. On the other hand, the number of integrators in the loop is called the type of the PLL. Since the VCO acts as an integrator, a PLL is at least of Type-I. If the loop-filter contributes additional integrators, the type of the PLL increases. Most common PLLs are Type-II. The order of a PLL is always greater then the type of the PLL i.e, a Type-II PLL is at least second order.

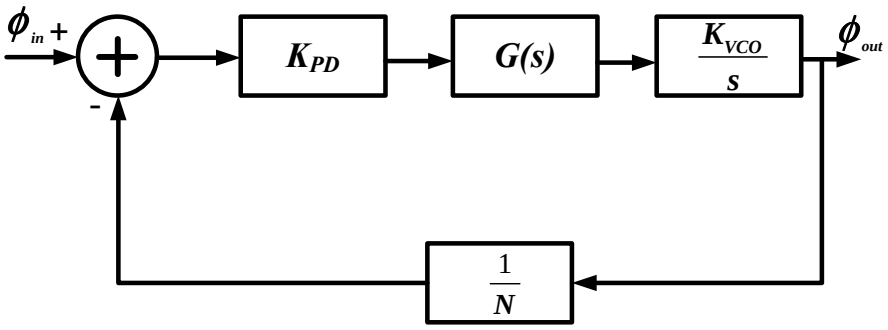


Figure 2.4: A linearized model for the PLL

2.3.1 Phase noise in a PLL

Using the linear model developed, the phase noise contributions of all the noise sources in the loop can be determined. The two major sources are the VCO and the reference noise. The closed-loop response to the reference noise is the same as (2.4). It is a low-pass transfer function with the loop 3-dB frequency. Within the bandwidth, the reference noise is amplified by the division ration N.

The phase noise of the VCO can be modeled as an additive noise (ϕ_{VCO}). Assuming ϕ_{in} and ϕ_{VCO} are uncorrelated, the transfer function for the VCO noise can be shown as

$$\frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{sN}{sN + K_{PD}K_{VCO}G(s)} \tag{2.5}$$

This is a high-pass transfer function which means that the negative feedback suppresses the slow varying VCO signals at the output phase. The high frequency phase noise from the VCO is not suppressed and increasing the PLL loop bandwidth lowers the VCO phase noise contribution.

2.3.2 Charge-pump PLL

The most popular implementation of a modern day Type-II PLL uses a charge pump phase/frequency detector as shown in Fig. 2.5. It consists of a two switches that are designed to deliver or remove charge from the loop filter under the control of the phase frequency detector (PFD) discussed below. The PFD outputs turn the switches $S1$ and $S2$ on and off, controlling the up and down currents that add to or subtract from the charge on the capacitor.

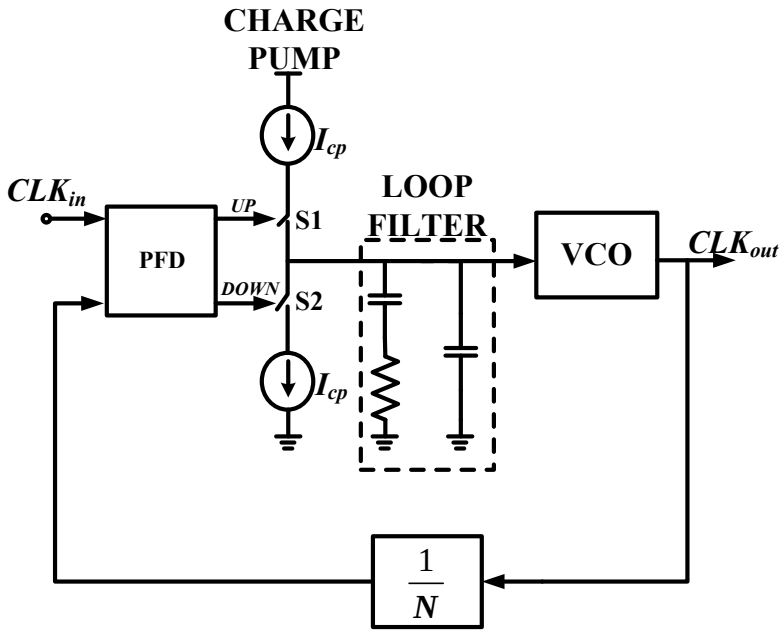


Figure 2.5: Charge pump PLL

Phase/frequency detector: Traditional PDs suffer from a small linear (and even monotonic) range and more seriously, harmonic locking. Alternatively, a phase/frequency detector (PFD) can be used. A PFD is a sequential circuit that can discriminate between both frequency and phase between its two inputs. A particular implementation of PFD is shown in Fig. 2.6. If the frequency at input A (ω_A) if greater than that at

B (ω_B), then Q_A produces positive pulses while Q_B remains zero. If $\omega_A = \omega_B$ then depending on the phase difference between A and B either Q_A or Q_B produces positive pulses. Ideally the two outputs are not high simultaneously. This is the distinction between the PFD and XOR or latch-based phase detectors which always produce complementary outputs. The delay elements shown in Fig. 2.6 are used to mitigate the effects of dead-zone which reduces the loop gain when the phase error is very small. The transfer characteristics of the PFD discussed are shown in Fig. 2.7.

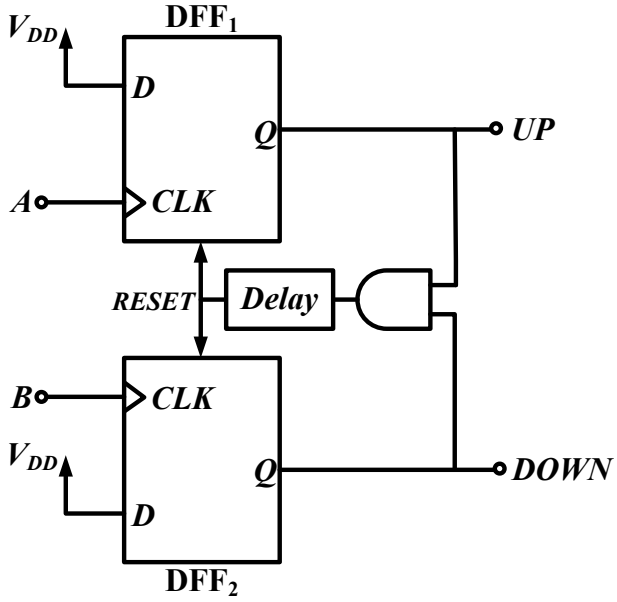


Figure 2.6: An example phase frequency detector circuit

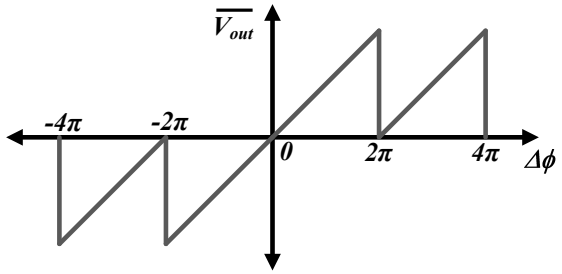


Figure 2.7: PFD transfer characteristics

For the CPPLL shown in Fig. 2.5, the individual transfer functions can be expressed as follows:

$$K_{PD} = \frac{I_{CP}}{2\pi} \tag{2.6}$$

$$G(s) = \frac{1+sRC_1}{s(C_1+C_2+sRC_1C_2)} \tag{2.7}$$

$$\approx \frac{1+sRC_1}{sC_1} \tag{2.8}$$

The capacitor C_2 is added to the loop to provide ripple suppression on the control voltage. In the equation above for $G(s)$, C_2 is small and without incurring a lot of error it is ignored to simplify the understanding. Using these expressions, the closed-loop transfer function is given by (2.9).

$$H(s) = \frac{\frac{K_{PD}}{N}K_{VCO}R(s+\frac{1}{RC_1})}{s^2+\frac{sK_{PD}K_{VCO}R}{N}+\frac{K_{PD}K_{VCO}}{NC_1}} \tag{2.9}$$

Comparing with a general second-order system, the natural frequency and damping factor are given as follows:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC_1}} \tag{2.10}$$

$$\zeta = \frac{R}{2}\sqrt{\frac{K_{PD}K_{VCO}C_1}{N}} \tag{2.11}$$

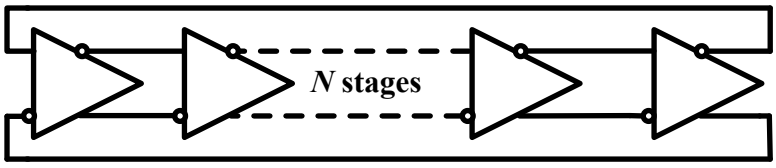
$$H(s) = \frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\omega_n\zeta s+\omega_n^2} \tag{2.12}$$

Since there are two integrators in the loop (one from the VCO and the second from the filter), the CP-PLL shown here is a Type-II PLL. The order of the loop as seen from (2.9) is also two (Note: if C_2 is not ignored, it's a third-order loop). If the loop filter resistor (R) is not used, the loop transfer function contains two poles at DC and no zeros which makes it unstable. Therefore a stable Type-II PLL must have at least one zero.

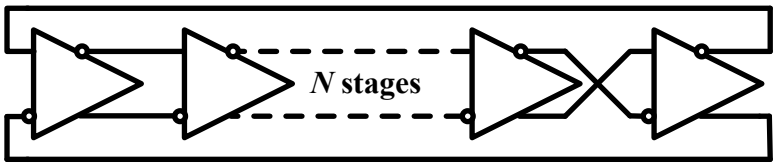
Types of Oscillators

An oscillator functions on the principle of $2N\pi$ ($N = 0, 1, 2...$) overall phase around a feedback loop with a gain greater than unity at a particular frequency (Barkhausen's criteria). As a result, any noise at that frequency (frequency of oscillation, say ω_0) is amplified through a positive feedback mechanism until the non-linearities in the system limit it to a particular amplitude (amplitude of oscillation, say A). In this section, we will discuss two main categories of VCOs used within PLLs: ring oscillators and LC oscillators. While in a ring oscillator, a net phase of 360° is obtained around the loop through the use of inverters or inverting amplifiers connected in a ring, in an LC oscillator, the net phase is zero at the resonance frequency of an inductor-capacitor (LC) tank.

Ring oscillators Ring oscillators are constructed by connecting a series of inverter or amplifier blocks in a ring as shown in Fig. 2.8.



(a) For odd values of N



(b) For even N

Figure 2.8: Construction of ring oscillators

The inverters/amplifiers need to provide a 180° phase shift at frequencies of interest requiring an odd number of stages if the individual stages are single ended. If differential

stages are available, even number of stages can be used used with one flipped differential connection (Fig. 2.8(b)). Additionally, at some frequency ω_0, the additional frequency-dependent phase from each stage adds up to 180°, thus providing a net 360° phase shift around the entire loop. If the overall gain at this frequency, ω_0 is greater than unity, then the positive feedback causes the circuit to oscillate at this frequency.

Ring oscillators have the advantage of being fully compatible with standard digital CMOS technology. The on-chip area consumption is small and relatively large tuning ranges can be achieved. However, the phase noise of these oscillators is traditionally higher than that obtained in LC oscillators.

LC-oscillators LC-oscillators function on the principle that an inductor (L) and a capacitor (C) connected in parallel offer an infinite impedance and zero phase shift at the frequency of resonance. However, a real LC-tank, due to its non-idealities, provides a finite real impedance at the resonance frequency. Sustained oscillations are produced at the resonance frequency by connecting a parallel negative resistance to cancel out the loss in the tank, and provide a net positive loop gain for the oscillator to start up. The negative resistance is usually realized by appropriately connected active devices as shown in Fig. 2.9. Depending on the configuration in which transistors are connected, different kinds of oscillators can be constructed.

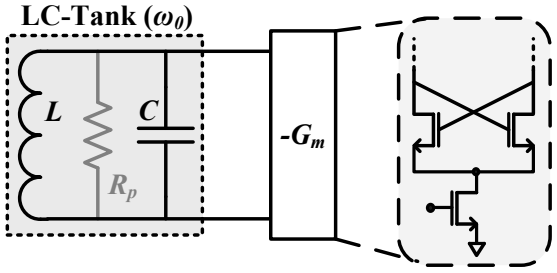


Figure 2.9: Conceptual construction of an LC oscillator

On-chip inductors and high performance capacitors often need special processes and

are not readily available in digital CMOS technologies. Also, they consume large area, especially for lower frequencies of operation. However, due to the higher quality factor (Q) of the LC-tank, LC-oscillators offer a relatively improved phase noise performance.

Phase noise

Any random fluctuations in the output phase of a synthesized frequency is characterized using phase noise. Noise in oscillators can produce fluctuations in both amplitude and phase of the output signal. Usually the amplitude noise is less important as it can be eliminated using limiters if required. A periodic oscillator output can be represented as $V(t) = Acos(\omega_0 t + \phi_n(t))$ where $\phi_n(t)$ represents random excess phase and is called "phase noise".

Phase noise is expressed as a function of the offset frequency from the center frequency of the generated carrier. The magnitude of the power spectral density (PSD) at the given frequency offset is compared to the carrier power to give the single side-band (SSB) phase noise. The mathematical definition is shown in (2.13).

$$L(\Delta\omega) = \frac{S(\omega_0 + \Delta\omega)}{\int_{-\infty}^{\infty} S(\omega) d\omega} \qquad (\Delta\omega > 0) \tag{2.13}$$

The spectrum of the oscillator as a function of the offset frequency is shown in Fig. 2.10. As shown in the figure, there are three distinct regions. The $\frac{1}{f^2}$ region is formed by the shaped thermal noise from different devices by the oscillator frequency domain response. The $\frac{1}{f^3}$ region is a manifestation of the up-converted flicker noise from the active devices and is seen close to the carrier frequency. At offset frequencies far from the center frequency, ω_0, white thermal noise of the devices dominate.

Oscillator phase noise analysis has been traditionally challenging. Here we discuss two main phase noise models popularly used for analysis.

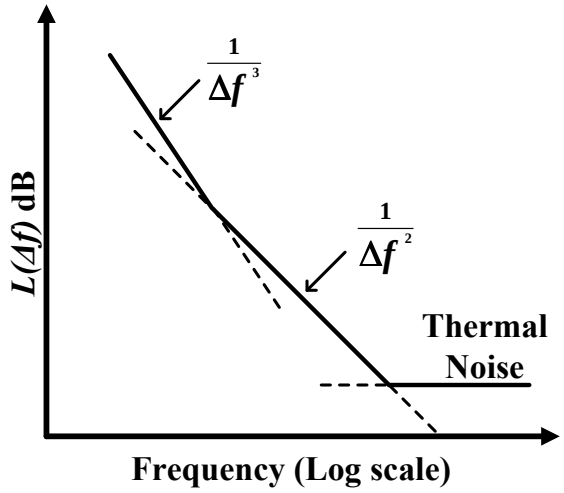


Figure 2.10: An example diagrammatic phase noise spectrum

Linear model: In 1966, D. B. Leeson presented a heuristic model of the oscillator spectrum in terms of the power, quality factor, absolute temperature, frequency, and frequency offset [5].

Although no formal proof was originally presented, one way to approximately derive Leeson's model would be to use the oscillator's frequency domain response to effectively shape the noise generated by the devices [6]. The result of such an analysis is given in (2.14).

$$L(\Delta\omega) = \frac{2FkT}{P_s}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{2.14}$$

where k is boltzman constant, T is temperature, P_s is output power, Q is quality factor, $\Delta\omega$ is frequency offset and F is called the excess noise factor used by Leeson to model the excess noise from the active devices.

Despite the intuitive nature and simplicity of Leeson's model, it suffers from some limitations. The excess factor, F, cannot be calculated without using measurement data to fit the model. Additionally, according to Leeson, the $\frac{1}{(\Delta f)^3}$ region coincides with the

flicker noise corner. However, in reality, this is not necessarily the case [7].

Ring oscillator: Linear phase noise model Ring oscillators have become very popular for frequency synthesis in monolithic CMOS designs. However, since Leeson's model is based on the Q of the resonator tank, ring oscillators could not be analyzed in a similar fashion. In 1996, B. Razavi proposed a definition of inductor-less VCOs that could be used in Leeson's equation to predict their phase noise [8]. The theory can thus be used to mathematically describe the phase noise of ring oscillators as given in (2.15)

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\phi}{d\omega}\right)^2} \tag{2.15}$$

where A and ϕ are the gain and the phase of the open-loop transfer function shown in Fig. 2.11. Note, this definition of Q only applies to a prediction of phase noise and does not represent a storage of energy per cycle, *i.e.*, it does not match the classical definition of Q for a circuit [9].

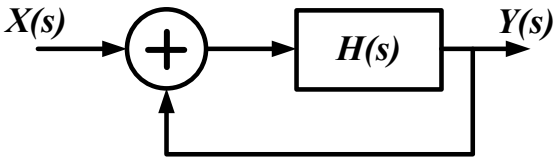


Figure 2.11: Linear model of an oscillator

The definition captures the sensitivity of the open-loop transfer function to circuit parameter variations. A larger Q, therefore, ensures a larger phase deviation with slight perturbations, and consequently, a larger feedback bringing the oscillation frequency back to ω_0. This definition also holds for LC-oscillators, and therefore, can be used as a general definition of Q. However, one should note that for ring oscillators the Q factor does not describe the ratio of active energy to energy loss per cycle.

Linear Time-variant model In 1998, A. Hajimiri and T. Lee introduced the impulse sensitivity function (ISF), symbolized as Γ to capture the cyclostationary nature of the impact of device noise on phase noise [7]. The fundamental observation is that if a noise current impulse affects the circuit during the oscillator's zero crossing, all the noise is converted into a phase disturbance. On the contrary, if a noise current impulse affects the circuit at its peak output voltage, all the noise gets converted into amplitude noise and the phase is not affected. Based on this the ISF is computed for each time instant, τ, within a time period. The ISF can then be expanded in a Fourier series given by:

$$\Gamma(\omega_0) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n cos(n\omega_0\tau + \theta_n) \tag{2.16}$$

where c_n represents the amount of noise contributed around the frequency $n\omega_0$ where $n = 0, 1, 2, \ldots$.

The phase noise expression in the single sideband case is then given by

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \frac{\overline{i_n^2}/\Delta f}{2\Delta\omega^2} \tag{2.17}$$

where $\overline{i_n^2}/\Delta f$ is the PSD of the circuit thermal noise and q_{max} is the maximum charge displacement across the capacitor on that node.

2.4 Multi-Antenna Communication

To meet the ever-increasing demands for higher data-rates in wireless communication, modern wireless standards are moving to multi-antenna architectures. Shannon's theorem states that for a given bandwidth, the maximum data-rate (in bits per second or bps) possible is given by:

$$C = B \cdot \log_{10}(1 + SNR) \tag{2.18}$$

where C is the maximum data rate or *capacity*, B is the bandwidth used in the communication and SNR is the signal-to-noise ratio (in absolute value).

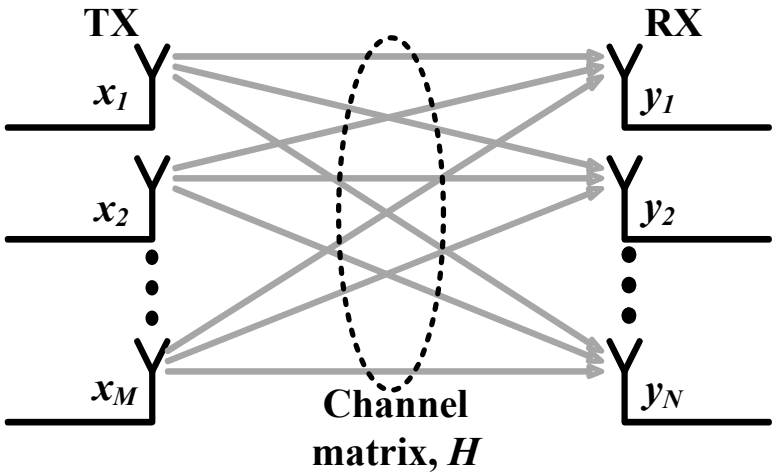


Figure 2.12: MIMO communication

However, Shannon's capacity is only defined for a single links. If there are multiple independent and co-existent links, they can use the same bandwidth and increase the capacity by the factor equal to the number of independent links. This forms the basis for multi-antenna communication. Consider a scenario of M antennas at the transmitter and N antennas at the receiver, as shown in Fig. 2.12.

Each transmit antenna creates a link with each receive antenna, which is characterized by a complex gain. Consider the i-th transmit antenna linking to the j-th receive antenna with a complex gain h_{ji}, with received noise n_j . Thus, the entire communication between the transmit and receive antennas can be characterized as follows [10]:

$$y_j = h_{ji}x_i + n_j \qquad \text{or} \qquad \underline{y} = H\underline{x} + \underline{n} \tag{2.19}$$

where

$$\underline{y} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_N \end{bmatrix} \qquad H = \begin{bmatrix} h_{11} & h_{12} & \dots & h_{1M} \\ h_{21} & h_{22} & \dots & h_{2M} \\ \vdots & \vdots & \ddots & \vdots \\ h_{N1} & h_{N2} & \dots & h_{NM} \end{bmatrix} \qquad \underline{x} = \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_M \end{bmatrix} \qquad \underline{n} = \begin{bmatrix} n_1 \\ n_2 \\ \vdots \\ n_N \end{bmatrix} \tag{2.20}$$

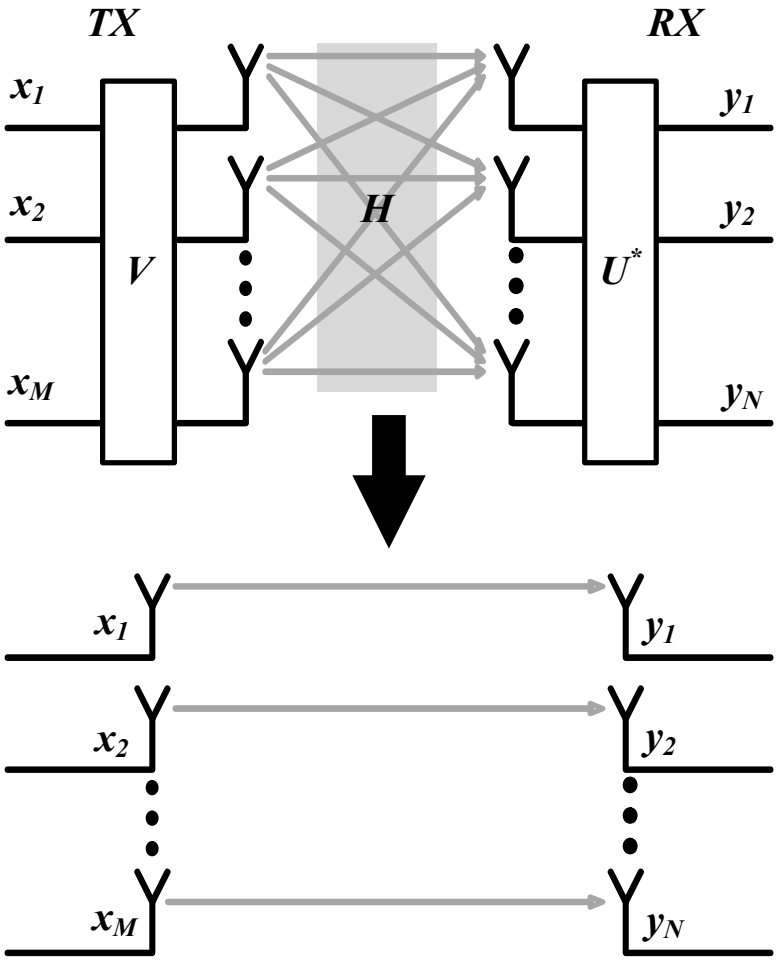


Figure 2.13: $\min\{M, N\}$-fold increase in communication capacity through MIMO

Expressing this communication as the multiple-input multiple-output (MIMO) system, allows the use of a simple linear algebra technique known as singular value decomposition (SVD). By using the SVD, the channel matrix $\boldsymbol{H}$ can be factorized into three matrices $\boldsymbol{U}$, $\boldsymbol{\Sigma}$ and $\boldsymbol{V}$, such that the following hold true.

$$\boldsymbol{H} = \boldsymbol{U}\boldsymbol{\Sigma}\boldsymbol{V}^* \qquad \boldsymbol{V}^*\boldsymbol{V} = \boldsymbol{I}_{\boldsymbol{M}\times\boldsymbol{M}} \qquad \boldsymbol{U}^*\boldsymbol{U} = \boldsymbol{I}_{\boldsymbol{N}\times\boldsymbol{N}} \tag{2.21}$$

The $\boldsymbol{N} \times \boldsymbol{M}$ matrix $\boldsymbol{\Sigma}$ is a diagonal matrix.

If the dataset $\underline{\boldsymbol{x}}$ (refer to (2.19)) was coded using the matrix $\boldsymbol{V}$ to generate $\underline{\boldsymbol{x'}}$ which

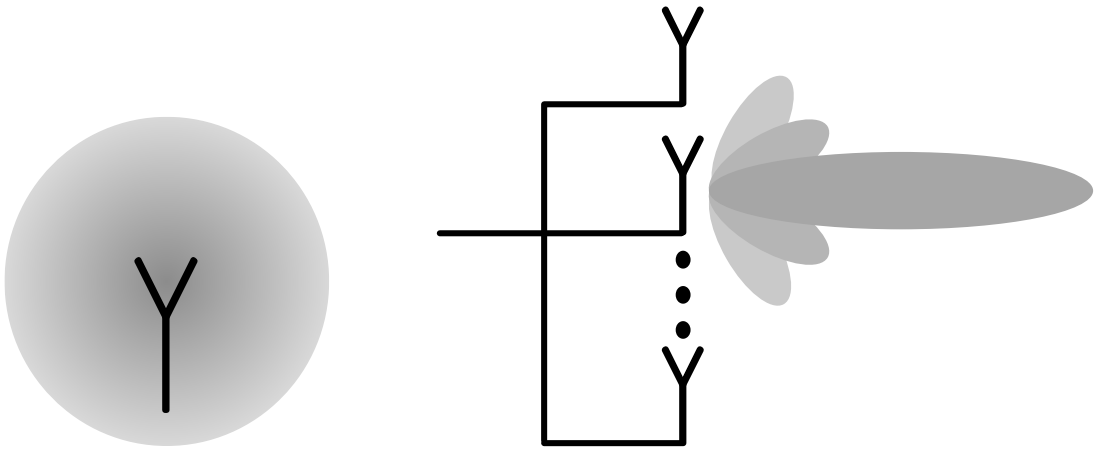
is then transmitted, and the received dataset is decoded using the matrix $\boldsymbol{U^*}$, then $\mathbf{min\{}\boldsymbol{M,N}\mathbf{\}}$ independent channels can be achieved. This incremental factor in the channel capacity is called the *multiplexing* gain of the MIMO system.

$$\underline{\boldsymbol{x'}} = \boldsymbol{V}\underline{\boldsymbol{x}} \Rightarrow \underline{\boldsymbol{y'}} = \boldsymbol{H}\underline{\boldsymbol{x'}} + \underline{\boldsymbol{n}} = \boldsymbol{U\Sigma}\underbrace{\boldsymbol{V^*}(\boldsymbol{V}}_{=\boldsymbol{I}}\underline{\boldsymbol{x}}) + \underline{\boldsymbol{n}}$$

$$\Rightarrow \underline{\boldsymbol{y}} = \boldsymbol{U^*}\underline{\boldsymbol{y'}} = \underbrace{\boldsymbol{U^*U}}_{=\boldsymbol{I}}\boldsymbol{\Sigma}\underline{\boldsymbol{x}} + \boldsymbol{U^*}\underline{\boldsymbol{n}} = \boldsymbol{\Sigma}\underline{\boldsymbol{x}} + \underline{\boldsymbol{n'}} \tag{2.22}$$

Each symbol in the dataset $\underline{\boldsymbol{x}}$ is independently transmitted and received in this scheme (Fig. 2.13). Since the noise is assumed to be random and the decoding matrix multiplication is a linear operation, its distribution or color (frequency content) remain unaffected.

From a theoretical standpoint, the above transmit-receive scheme can potentially allow an $\boldsymbol{n}$-fold increase in data-rates. However, there is one important assumption that has been made during this derivation: the transmitter and receiver *know* the channel (*i.e.*, channel matrix $\boldsymbol{H}$). This is not true for most wireless communication systems and networks. For example, a user talking over the cellular phone and moving in a automobile causes a constant change in the wireless channel characteristics between the phone and the wireless base station. In a MIMO system, the transceivers on both the phone and the base station will have to constantly update the channel matrix, compute the SVD and use it in the encoding and decoding of signals. This is a non-trivial task. Further, estimation of the channel matrix itself requires training (or pilot) symbols. If the channel characteristics changes frequently, then training symbols would use up most of the communication period. This is undesirable in high data-rate systems, which is the principal application of MIMO communication.



(a) Single isotropic antenna (b) Equi-spaced array of isotropic antennas

Figure 2.14: Single antenna versus multiple antennas transmitting the same signal

2.5 Phased-Arrays

In theory, traditional multiple-input multiple-output (MIMO) systems increase the communication bandwidth by a factor of $\boldsymbol{N}$, where $\boldsymbol{N}$ is the minimum of the number of transmit and receive antennas [10]. But in real-time systems, in order to achieve this theoretical increase, complex MIMO algorithms need to be implemented in the digital signal processor. Also, these systems are plagued by dynamic range requirements of the analog-to-digital converters. Phased-arrays are a subset of MIMO systems that forgo these stringent requirements.

2.5.1 Concept of the Phased-Array

The basic principle of phased-array was developed during World War II and was revolutionized in the 1950's and 1960's towards their application in military radars and radio astronomy [11]. A single *isotropic* antenna radiates equally in all directions

(Fig. 2.14(a)). The radiation pattern can be expressed mathematically as

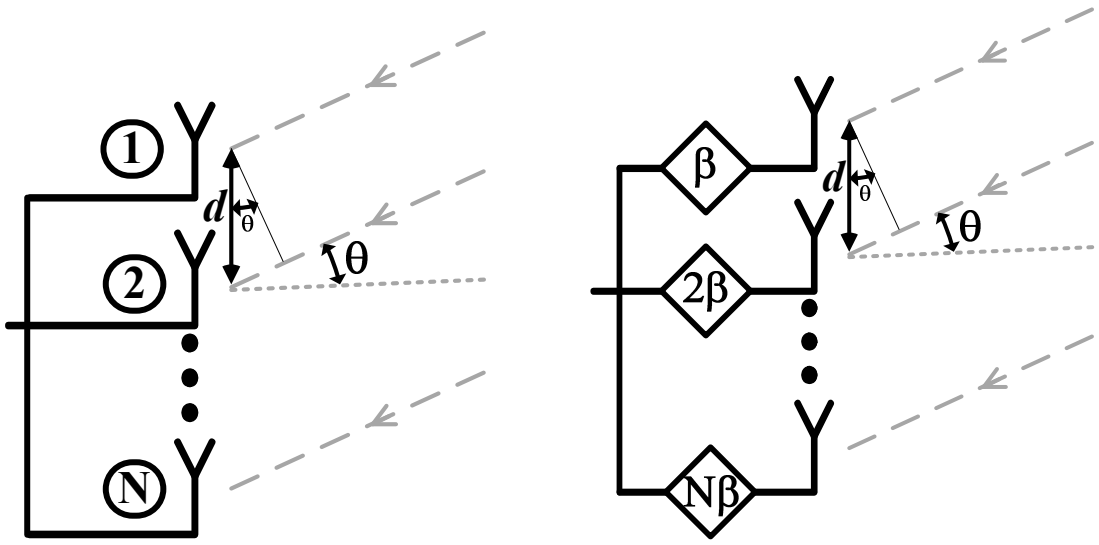
$$f(r) \propto \frac{e^{-jkr}}{r^2} \qquad k = \frac{2\pi}{\lambda} \tag{2.23}$$

where k is the wave number, r is the radial distance from the antenna and λ is its wavelength. Now, if we consider an equi-spaced array of isotropic antennas which are fed the same signal, the effective beam formed is as shown in Fig. 2.14(b). Since each of these antennas radiate the same signal, at a sufficiently far distance, the radiation from each of the antennas can be assumed to be parallel and equal in strength. At any such point, assume that the angle from the *broadside* direction is θ (as shown in Fig. 2.15(a)). The effective signal can be calculated as the vector sum of the signals transmitted by each antenna. Since radiation from all the antennas is approximately parallel, the vector sum reduces to a simple summation of all the signals.

$$f_{total}(r,\theta) \propto \frac{A}{r^2} \sum_{i=1}^{n} e^{-jk(r+(i-1)d\sin\theta)} \Rightarrow |f_{total}(\theta)| \propto \left| \frac{\sin\left(\frac{Nkd\sin\theta}{2}\right)}{\sin\left(\frac{kd\sin\theta}{2}\right)} \right| \tag{2.24}$$

The radial pattern described by (2.24) is similar to a *sinc* function ($\sin(x)/x$). When this function is plotted in the polar coordinate system, the pattern is similar to the one depicted in Fig. 2.14(b). The maximum power is transmitted (or received) in the broadside ($\theta = 0$) direction. The signal strength (power) in this direction is N^2 times the power transmitted by each antenna. Further, there are multiple sidelobes with signal strength tapering away from the broadside direction. The number of sidelobes depends on the number of antennas in the array. The sidelobes are separated by null (zero power) directions. These nulls can be effectively harnessed to block interferers and signal jammers.

The N^2 improvement in the transmitted signal power results in an SNR improvement by the same factor. Since the same (phase-shifted) signal is transmitted through all the antennas, the multiplexing gain of a true MIMO system is lost. The SNR improvement increases the channel capacity, but the relationship is logarithmic in nature.



(a) Antenna-array (b) Phased-array

Figure 2.15: Beamforming in the antenna array versus the phased-array

Hence, as N increases, the capacity improves, but the relative increment in capacity diminishes. The beamwidth also decreases when $\boldsymbol{N}$ is increased [11]. This reduces the interference caused by the radiation to any neighboring radios, not in the principal beam direction.

$$\boldsymbol{C = B\log[1 + N^2 \times SNR]} \tag{2.25}$$

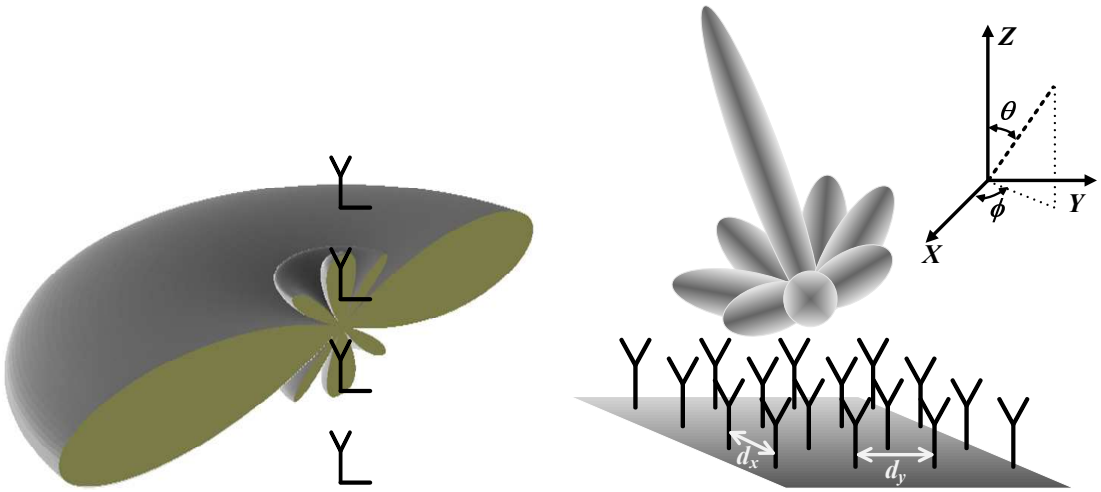
Next, if a progressive phase-shift is applied to the antennas as shown in Fig. 2.15(b), the effective beam pattern can be derived as

$$\boldsymbol{|f_{total}(\beta,\theta)| \propto \left|\frac{\sin\left(\frac{N(\beta - kd\sin\theta)}{2}\right)}{\sin\left(\frac{\beta - kd\sin\theta}{2}\right)}\right|} \tag{2.26}$$

According to (2.26), adding the progressive phase-shift moves the principal beam to an angle $\boldsymbol{\theta_0}$ given by

$$\boldsymbol{\theta_0 = \sin^{-1}\left(\frac{\beta}{kd}\right)} \tag{2.27}$$

The polar $\boldsymbol{sinc}$ pattern of the beam still remains and the sidelobes and nulls only change



(a) 3D view (cross-section) of radiation in linear array

(b) 2-D phased-array

Figure 2.16: Beamforming in the linear array versus the planar or 2D phased-array

directions.

If the antennas are equispaced along a line, the array is called a linear array. The three-dimensional beam-pattern of a linear array is depicted in Fig. 2.16(a). The linear array can focus the beam in any given direction along the elevation, but along the azimuth, the radiation is *impartial*. To generate a more focussed beam or *pencil* beam, as it is known, the antenna can be laid out in a 2-D matrix (as shown in Fig. 2.16(b)). The characteristics of the beam from a 2-D phased array are similar to the beam from the linear-array. The signal strength in the principal beam is $\boldsymbol{N_x^2 N_y^2}$ times the power transmitted by each antenna, where $\boldsymbol{N_x}$ and $\boldsymbol{N_y}$ are the number of elements in the $\boldsymbol{x}$ and $\boldsymbol{y}$ directions, respectively, of the antenna array. In a linear array, the progressive phase-shift (of $\boldsymbol{\beta}$) is one-dimensional. In the 2-D case, two angular constants, $\boldsymbol{\beta_x}$ and $\boldsymbol{\beta_y}$ need to be defined (not shown in the figure to reduce complexity) along the $\boldsymbol{x}$ and $\boldsymbol{y}$-axes, respectively. In this case, the principal beam direction is characterized by $(\boldsymbol{\theta_0}, \boldsymbol{\phi_0})$

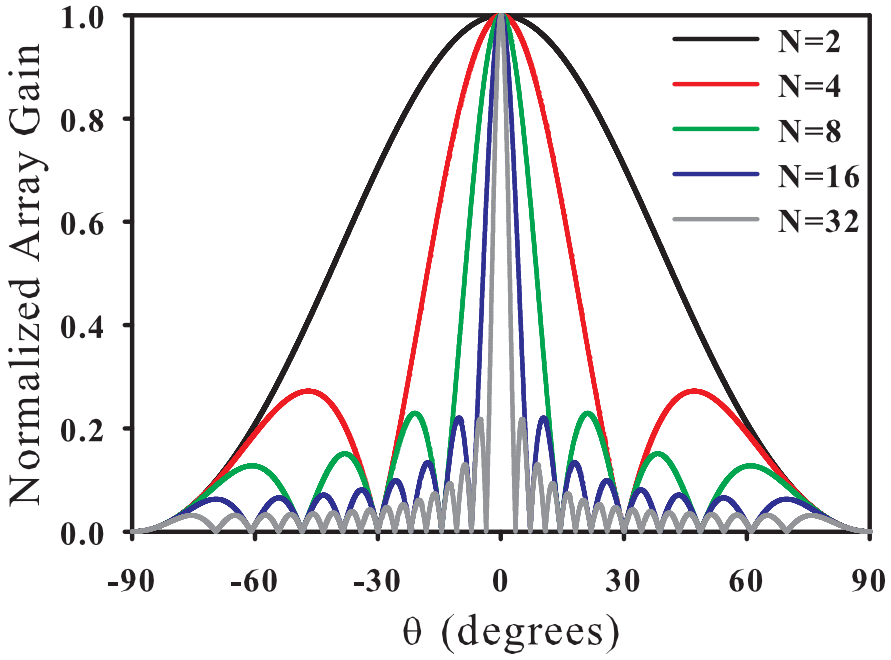


Figure 2.17: Radiation pattern for an antenna-array as a function of N (for $\boldsymbol{d = \lambda/2}$)

which satisfy the following relations [11]:

$$\boldsymbol{\theta_0 = \sin^{-1}\left(\frac{1}{k}\sqrt{\left(\frac{\beta_y}{d_y}\right)^2 + \left(\frac{\beta_x}{d_x}\right)^2}\right)} \qquad \boldsymbol{\phi_0 = \tan^{-1}\left(\frac{\beta_y}{\beta_x}\right)\left(\frac{d_x}{d_y}\right)} \tag{2.28}$$

The phase-shift $\boldsymbol{\beta}$'s are generated in the transmitter (or receiver) section. Since these phase-shifts are generated electronically, phased-arrays are also widely known an electronically scanned arrays (ESAs).

2.5.2 Applications of Phased Arrays

Phased-arrays have been used by the military for radar and long-range communication applications for last five decades. To date, phased-arrays remain as one of the most attractive architectures for radar design because of their various advantages. Significant advances have been made with respect to the capability of phased-array radars

(a) 3D view (Multiple applications of phased-array in a radar

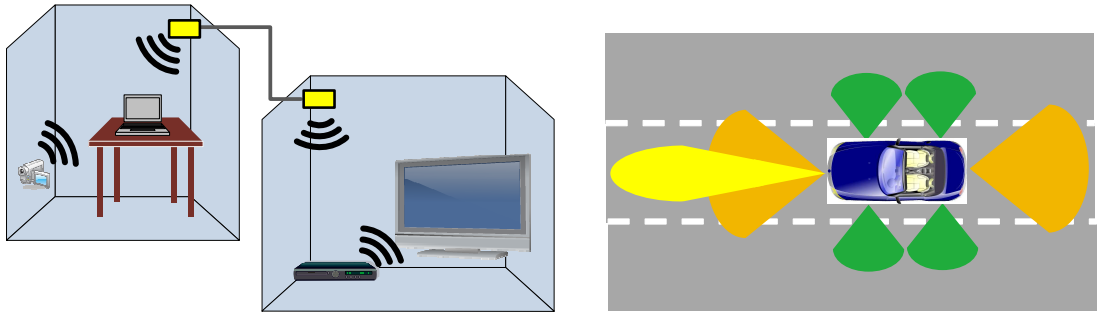
(b) AN-SPY1 Radar used in ships (source: http://www.navy.mil)

Figure 2.18: Military applications of phased-array

since their inception. For example, modern radar are capable of generating multiple concurrent beams for different applications like surveillance, projectile guidance, detection and tracking (Fig. 2.18(a)). Military communication radios and radars operate at various frequencies, most notably in the S-band (2-4GHz), X-band (8-12GHz) and Q-band (40-60GHz).

Until recently, phased-array technology was almost exclusively used for military applications, satellite communication and radio-astronomy. Recently, phased-arrays have gained considerable attention as a viable solution for communication in the millimeter-wave (mm-wave) bands for consumer applications. The Federal Communications Commission (FCC) has opened frequency bands around 24GHz and 60GHz for industrial, scientific and medical (ISM) applications, with a band of 7GHz allocated around 60GHz center frequency for unlicensed devices [12]. Further, certain frequencies in the W-band (75-110GHz) have also been dedicated to automotive anti-collision radars and passive imaging applications [13, 14].

Atmospheric absorption causes significant attenuation of electromagnetic signals at



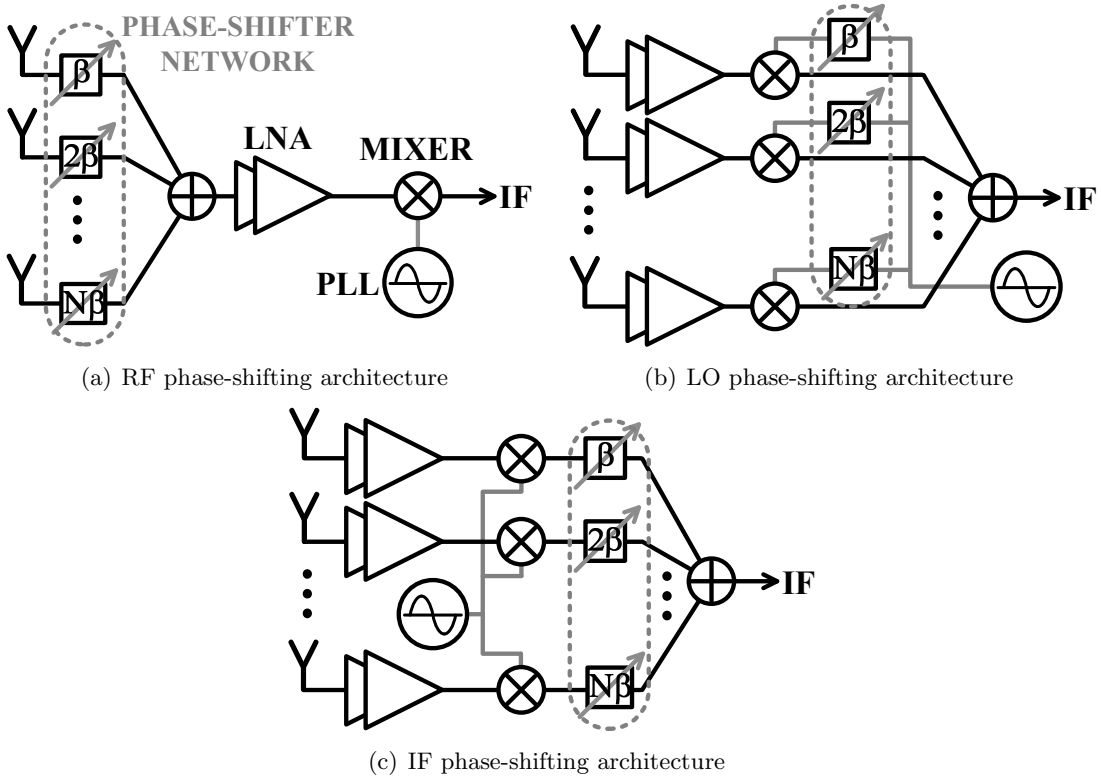
(a) 60GHz Wireless Personal Area Network (WPAN) (b) Anti-collision radars in automobiles

Figure 2.19: Military applications of phased-array

24GHz and 60GHz. Especially at 60GHz, the attenuation factor (20dB/km) is significantly higher than that in the neighboring bands (0.1-1dB/km). Consequently, these bands are not suitable for radar or long-range communication applications. Ultra-widebands have been allocated around these frequencies for ISM and unlicensed applications, respectively. The 60GHz band (57-64GHz) is especially attractive for in-home networking to connect multiple devices through a single high-data rate wireless network [15]. However, even for these short distances, the power output available from silicon-based transmitters is limited at such high frequencies. In order to increase the effective radiated power to overcome this limitation, phased-arrays have been proposed as a possible solution.

2.5.3 Phased-Array TX/RX Architectures

Phased-array technique is based on the progressive phase-shift operation required to point the resultant beam from an array of antennas in the desired direction. In the case of a transmitter, the phase-shift is introduced electronically to the RF signal being driven into the antenna array. In the case of a receiver, the phase-shift is electronically canceled from the RF signals being received by the antenna array. Consequently, the electronic phase-shifter forms the most critical block in the phased-array.



(a) RF phase-shifting architecture

(b) LO phase-shifting architecture

(c) IF phase-shifting architecture

Figure 2.20: Phased-array architecture categories (shown for only the receiver)

Depending upon the placement of the phase-shifter in the transmitter or receiver phased-array architectures can be broadly classified into three categories: RF phase-shifting, LO-phase-shifting and IF-phase-shifting (or baseband-phase-shifting). These are illustrated in Fig. 2.20 for a receiver. Each of them can be applied to the case of a transmitter. In the RF phase-shifting architecture, the phase-shifter is placed in the RF path, either before or after the LNA (or PA, in the case of a TX) depending upon the implementation. This is the traditional architecture that has been widely used in military radars and satellite communication radios. The radio design in these systems is modular in nature and each block is implemented as a monolithic microwave integrated circuit (MMIC) or individual modules. The phase-shifter, in particular needs to satisfy

stringent constraints on linearity, noise figure, power handling capability, operation bandwidth and phase-shift accuracy. The only flexibility in the design is the size of the phase-shifter. Consequently, ferrite phase-shifters are often used as they satisfy all of the aforementioned requirements. A typical ferrite phase-shifter is illustrated in Fig. 2.21(a).

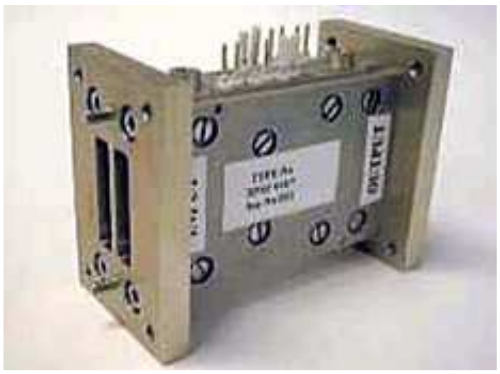
There are many advantages of using the RF phase-shifting architecture over the other two categories. In the RF phase-shifting receiver, the signal combining is done early in the receiver. Consequently any jammers or interferers in the null directions are canceled before they are processed by the RF and IF/baseband sections. Since these circuits consist of active elements (transistors), their linearity is limited. Any strong interferer around the desired signal can create unwanted intermodulation frequencies [16]. By canceling the jamming and interfering signals early, the architecture effectively *shields* the stages ahead. Further, as illustrated in Fig. 2.20, the component count in the RF phase-shifting architecture is lower than the other two. This avoids the mismatch issues for the various RF and baseband blocks, except for the phase-shifter.

In the LO phase-shifting architecture, the phase-shifter is placed in the local-oscillator (LO) path, *i.e.*, between the frequency synthesizer and the mixer(s). The mixer in the RF section multiplies the input signal with the LO signal to upconvert or downconvert the input frequency. In this operation, any phase-shift at the input automatically transfers to the output.

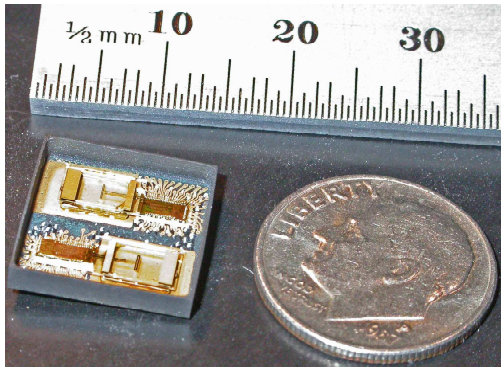
$$\text{TX:} \quad \cos(\omega_{LO}t + \beta) \times \sin(\omega_{BB}t) = \sin(\omega_{RF}t + \beta) \qquad \omega_{RF} = \omega_{LO} + \omega_{BB}$$

$$\text{RX:} \quad \cos(\omega_{LO}t + \beta) \times \sin(\omega_{RF}t + \beta) = \sin(\omega_{BB}t)$$

where ω_{LO}, ω_{RF} and ω_{BB} are the LO, RF and baseband frequencies, respectively. The equations above only express the frequency components remaining after relevant filtering operations. The RF phase-shifting architecture may require the phase-shifter to



(a) X-band ferrite phase shifter (WR75 connector: 19mm x 9.53mm) (source: http://www.meslmicrowave.com)



(b) Integrated 60GHz communication radios (source: http://domino.watson.ibm.com)

Figure 2.21: Comparison of the size of a module in a phased-array for military/satellite applications and an integrated radio implementation preferred for consumer wireless applications

operate over a wideband signal, depending upon the application. One of the important advantages of the LO phase-shifting architecture is that the phase-shifter operates on the LO signal which is inherently very narrow-band in nature (ideally a single tone). This allows for the design of low-power phase-shifters. Also, the phase-shifter no longer affects the noise figure or linearity of the receiver chain. However, multiple channels of the RF section are used before the signal combiner. Consequently, the architecture suffers from mismatch and inter-channel leakage issues, in addition to increased power dissipation from the RF section. This also places a stringent constraint on the linearity of the RF section, since any interfering signal from the null direction (which is canceled in the signal combiner) is processed by the RF section and the generated intermodulation terms remain even after signal combining. In spite of these issues, silicon-based (CMOS or BiCMOS) phased-array transmitters and receivers have widely adopted the LO phase-shifting architecture [12, 17–24]. The primary reason behind this is the ease of phase-shifter design for the LO signal. Novel circuit topologies for wideband RF phase-shifting

have been demonstrated in silicon [25–28]. But they have been unable to match the performance of discrete ferrite phase-shifters.

Baseband/IF phase-shifting architecture employs the phase-shifter in the IF or baseband section. The *beamforming* can be done either in the analog [29] or in the digital domain [30]. The RF section linearity issue plaguing the LO phase-shifting architecture becomes worse in this case, since all the blocks (including the ADC, if the beamforming is done in the digital subsection) before the signal combiner are affected by it. With respect to noise figure, the phase-shifter does not need to meet any stringent requirements because the gain of the previous stages would mitigate its effect to a large extent. However, due to the same reason, its linearity strongly affects the overall system linearity. In spite of these issues, IF beamforming presents a very effective techique to generate multiple independent concurrent beams from the same phased-array, as will be discussed in Chapter 7.

2.5.4 Isolation between channels

MIMO transceivers (including phased-arrays) consist of multiple transmit and receive channels. For consumer wireless applications, the entire transceiver is integrated on a single silicon IC. Naturally, there is cross-talk between these channels. The cross-talk can be linear or non-linear in nature [31]. Linear cross-talk can be canceled in a true MIMO scheme. However, in a phased-array, any form of cross-talk only deteriorates the beam-forming performance. Fig. 2.22 shows this change in beam caused by cross-talk between channels. It should be observed that the principal beam characteristics are hardly affected by cross-talk (as long as it is low enough). However, the nulls are most sensitive to cross-talk. Nulls are created by complete destructive combination of phase-shifted signals. In radars, beams are engineered to direct the main lobe in a certain direction whereas the nulls are directed at jammers and interferers. Cross-talk can move

the null from its original direction. For example, in Fig. 2.22, the ideal beam creates nulls in the $\pm 90^{\circ}$ direction. However, in the presence of cross-talk, this null shifts to 82.5°. Further, if a jammer is present at $\boldsymbol{\theta} = 90^{\circ}$, in the ideal case, its signal would be completely attenuated. However, under the influence of cross-talk, the attenuation (normalized) reduces to approximately 35dB. In such a case, a strong jamming signal can easily saturate the radar front-end. The calculations for Fig. 2.22 only take nearest neighbors' interaction into account. Also, the improvement of suppression in the nulls in the presence of cross-talk illustrated in the plot is an artifact of the resolution used on the $\boldsymbol{x}$-axis. Cross-talk from other channels can cause additional random shifts in null direction(s). Therefore, in the case of military radars working in hostile environments, cross-talk can severely affect the performance of the radar against jammers and interferers. On the other hand, for consumer wireless applications, the isolation constraint among channels is not so stringent.

In silicon ICs, there are three principal mechanisms of cross-talk: through power supply, through the substrate, and through inductors and transformers (magnetic coupling). Power supply noise can be suppressed by placing on-chip de-coupling capacitors. The continuous scaling of CMOS technology to achieve better digital circuit performance has resulted in silicon substrates being heavily doped to combat short-channel effects in MOS transistors. This has increased the conductivity of the silicon substrate and degraded its isolation properties. Substrate cross-talk is one of the most important forms of signal leakage in modern CMOS RF and mixed-signal circuits. Substrate cross-talk at RF frequencies can be minimized by using guard rings around each channel [32]. By using pattern-ground shield (PGS) [33] and/or deep-trench isolation structures below the inductors and enclosing their individual areas with ground-to-substrate contacts, inter-inductor cross-talk and noise coupling through the substrate can be suppressed [34]. Further, cross-talk can also occur through common ground and power supply lines for

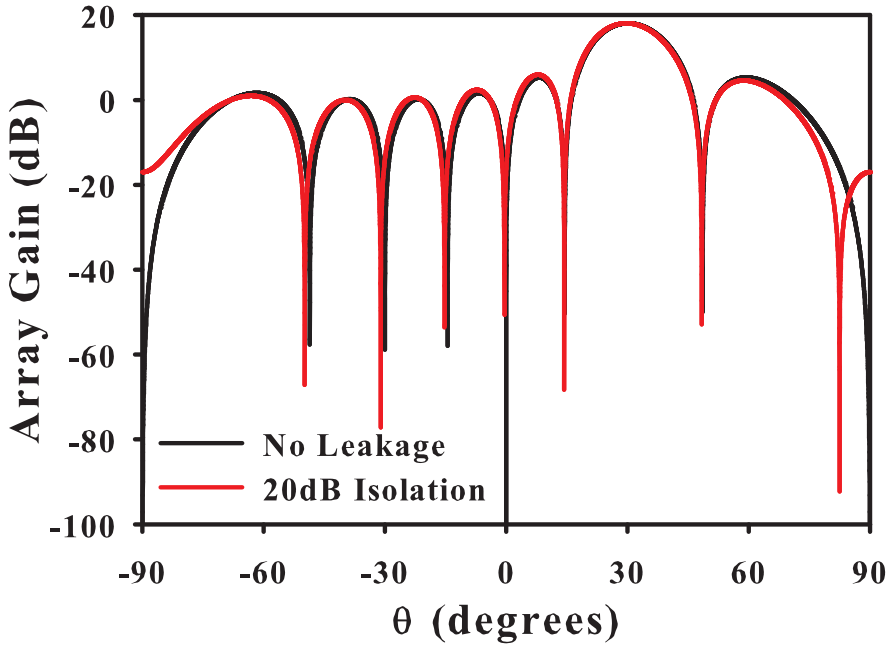


Figure 2.22: Effect of cross-talk on the radiation pattern (eight-element array beam directed at 30°)

different transmit/receive channels. By separating these for each of the channels, better channel-to-channel isolation has been reported [35].

Most high-speed circuits and RFICs use inductors, transmission lines and transformers for high frequency and/or broadband operations. With multiple inductor/transfomer coils or unshielded transmission lines placed in close proximity, some of the magnetic field lines from one block can pass through the other block(s) and cause magnetic coupling of signals. The transmission line coupling can be suppressed by using slow-wave coplanar waveguide structures [36]. The magnetic field lines of inductor/transformer can be curtailed by placing metal shields, extending from the bottom to the the top metal layers. But this solution also poses additional area requirements. A novel way to suppress magnetic coupling from these coils is to adopt a *twisted* or *clover*-shaped

topology for the inductor instead of the standard coil topology [37]. The most important advantage of this topology is that it restricts almost all of the field lines within the inductor area. This is a natural effect arising from the inductor geometry. Thus, magnetic coupling is significantly mitigated.

Finally, 3D-SOI CMOS technology offers another solution to achieve high channel-to-channel isolation. 3D-SOI technology allows for the use of electromagnetic structures such as Faraday cages [38] which are very effective at isolating channels. However, 3D technologies are still currently under development.

2.6 Previous Silicon-Based Phased Arrays

Recent years have seen significant interest from academia and industry to implement phased-arrays in silicon for consumer mm-wave wireless applications. In this section, we chronologically review the state-of-the-art phase-generation techniques and architectures for phased-array transceivers in silicon, reported in recent literature.

One of the first fully-integrated silicon-based phased-array receivers was presented in [17, 39]. A ring-oscillator can create multiple equi-spaced phases for a single output frequency. The number of available phases is equal to the number of elements in the ring. In [17,39], the 24GHz eight-channel phased-array receiver adopts a two-step heterodyne architecture and the LO phase-shifting is performed in the first down-conversion. An 8-stage 19.2GHz differential ring-oscillator is locked to an external reference, through a PLL (Fig. 2.23). The 16 phases (or 8 differential phase pairs) are multiplexed to the mixer LO inputs. This phase-generation scheme relies on the extensive LO signal distribution of all possible phases to each of the eight channels. This extensive LO routing draws significant amount of power and large area for the symmetric layout of transmission lines. The phase generation from the ring-oscillator is accurate, but the phases possible and hence, the possible directions for the principal beam are fixed.

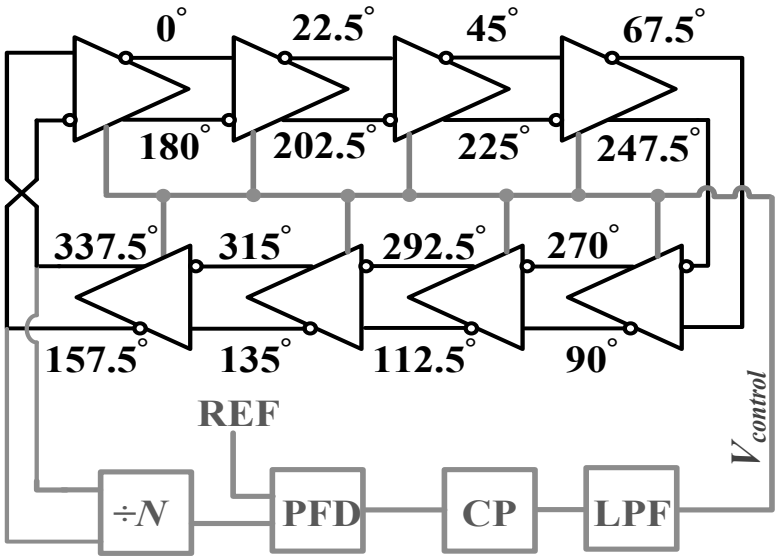


Figure 2.23: Ring-oscillator outputs generate the required progressive phase-shift pattern

This doesn't allow for arbitrary phase-shift patterns for beam engineering. A similar generation approach is adopted for a phased-array transmitter in [40].

Low-power phased-array systems can be designed by reducing the number of constituent blocks in the transceiver, which is one of the advantages of RF phase-shifting architectures. One of the proposed techniques to achieve RF phase-shifting using active circuits in silicon [25] is called *cartesian combining*. The deduction of the architecture from complex mixing is shown in Fig. 2.24. The effective mixing action can be mathematically expressed as:

$$\begin{aligned} x(t) \times e^{j(\omega_{LO}t+\phi)} &= x(t) \times e^{j\omega_{LO}t} \underbrace{(\cos\phi + j\sin\phi)}_{A_r + jA_i} \\ = \quad & [\{x(t)\cdot A_r\} \times \cos(\omega_{LO}t) - \{x(t)\cdot A_i\} \times \sin(\omega_{LO}t)] \\ + \quad & j\,[\{x(t)\cdot A_i\} \times \cos(\omega_{LO}t) + \{x(t)\cdot A_r\} \sin(\omega_{LO}t)] \end{aligned} \tag{2.29}$$

The architecture provides a simple and effective approach for controlled RF phase-generation. However, the beamforming occurs after the downconversion. This increases

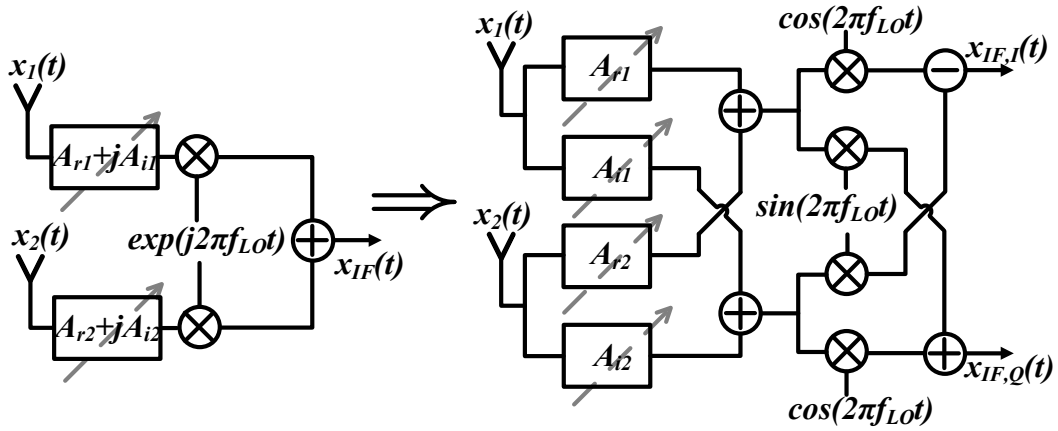


Figure 2.24: Cartesian combining technique for beamforming

the linearity constraints on the LNA, the mixer and any other RF blocks between these two circuits. The architecture uses variable-gain amplifiers (VGAs) in the RF path, which affect the linearity and noise figure of the RF chain directly. In addition, VGAs draw significant power.

At RF and mm-wave frequencies, ring-oscillators draw significantly larger amounts of power than negative-g_m LC-oscillators. Additionally, the phase noise of ring-oscillators is worse than the negative-g_m LC-oscillators. Hence, LC-oscillators are often used in many RF and mm-wave radio implementations. In such a case, multi-phase outputs cannot be expected from the oscillator. However, a simpler form of cartesian combining, known as *vector modulation*, expressed as

$$A_s \sin(\omega_{LO}t) + A_c \cos(\omega_{LO}t) = \sqrt{A_s^2 + A_c^2}\sin(\omega_{LO}t + \alpha) \qquad \text{where } \tan\alpha = \frac{A_c}{A_s} \tag{2.30}$$

can be used on quadrature LO signals to generate the desired phase-shift as shown in Fig. 2.25. This LO phase-shifting approach avoids placing VGAs in the RF path. A 77GHz transceiver for automotive radar based on this architecture is presented in [18,19]. It is also adopted for a 60GHz receiver described in [21].

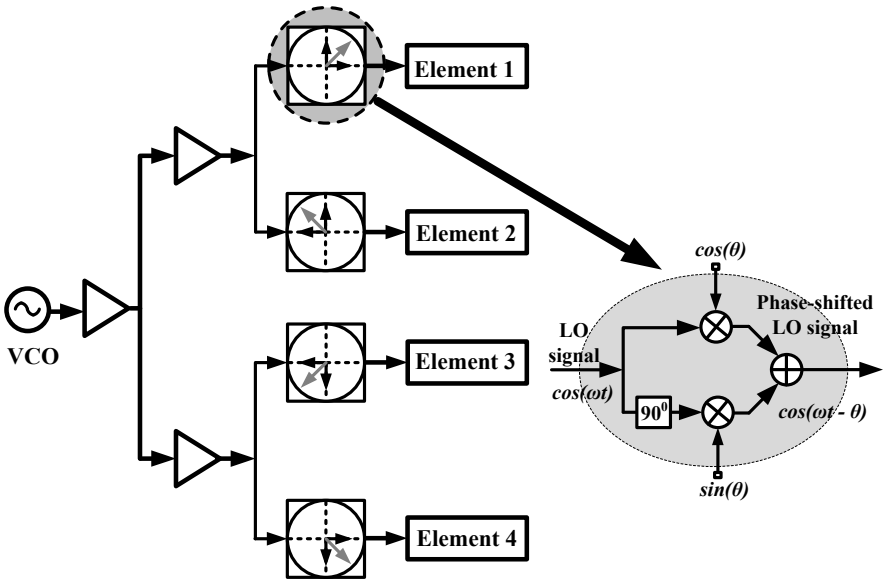


Figure 2.25: Pushing the cartesian combining to the LO

The ring-oscillator based PLL generates multiple fixed phases. However, if a variable phase-shifter were placed in the ring, then the progressive phase-pattern generated can be tuned. When a phase is applied in the loop, it is compensated for by the oscillator stages, by a shift in the frequency to ensure that the phase around the loop is 360°. Simultaneously, the PLL would ensure that the ring-oscillator remains locked to the reference frequency. Consequently, the control voltage for the oscillator changes. The basic architecture of the variable-phase ring-oscillator PLL (VPRO-PLL) used in the transceiver in [20] is depicted in Fig. 2.26. The transceiver, designed for 24GHz automotive radar applications, uses the VPRO-PLL for multiple functions - frequency synthesis, phase-generation and mixing. During transmit, applying the modulation signal to the control voltage of the PLL generates a frequency modulated and phase-shifted set of signals at the outputs. On the other hand, during the receive operation, the VPRO-PLL is injection-locked to the incoming signal from the antenna array. This phase-shifted set of injection signals pull the ring-oscillator. But the PLL tries to lock the oscillator back

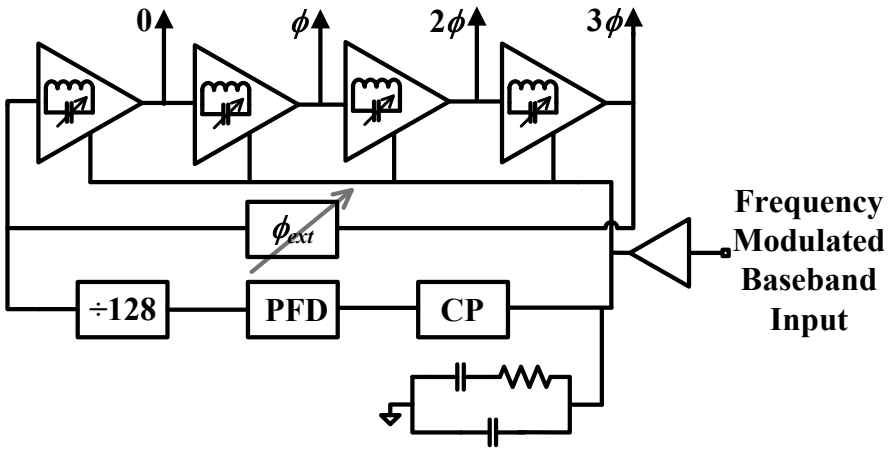


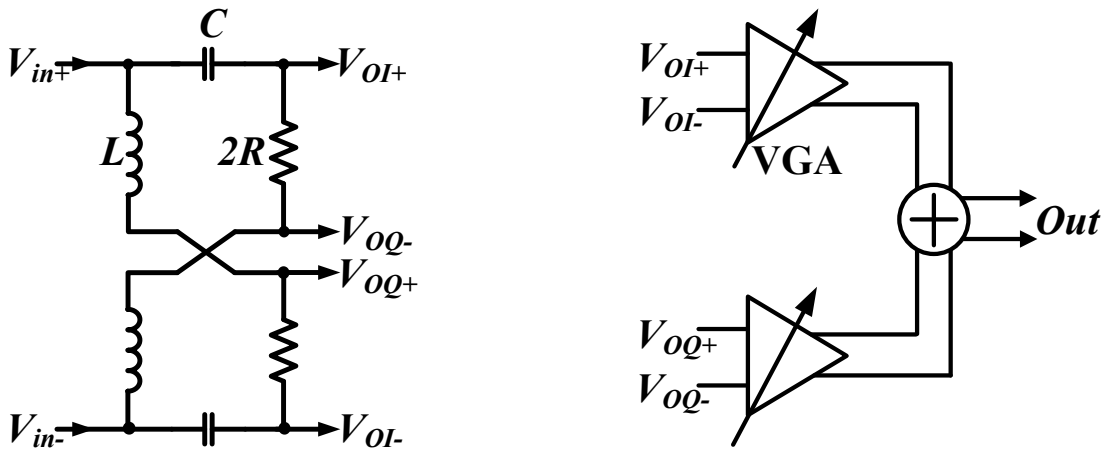
Figure 2.26: Variable Phase Ring-Oscillator (VPRO) architecture for phase generation

to its reference. Since the received input signal is frequency-modulated, this *tug-of-war* between the injection signals and the PLL generates the baseband signal on the PLL control voltage, which can be tapped out for signal processing. This multi-functional aspect of the VPRO-PLL results in significant reduction in the overall power consumption of the transceiver.

The architecture, however, suffers from some drawbacks. First, the architecture is based on a ring-oscillator which draws significant amount of power at mm-wave frequencies. Second, the architecture is not easily scalable to a large number of elements, since this requires more number of stages in the ring-oscillator, which in turn reduces its frequency of operation. The authors propose to overcome this drawback by designing ring oscillators which have a total loop phase equal to a non-unity integer multiple of 360°. Finally, the phase-shift possible through this architecture is limited, when the PLL operates at the fundamental frequency. This is because the maximum phase-shift possible from a circuit is 360°.

$$\phi = \frac{2k\pi - \phi_{ext}}{N} \qquad k \in \mathbf{Z} \tag{2.31}$$

Consequently, the maximum value for ϕ is 90° (assuming $k = 0$ and the case of



(a) QAF Structure (b) Vector Modulation

Figure 2.27: Quadrature All-pass Filter (QAF) with vector modulation to create wideband RF phase-shifting

$\boldsymbol{N = 4}$), thereby restricting the beam angle $\boldsymbol{\theta}$ between $-30°$ and $+30°$ for half-wavelength antenna spacing. The authors overcome this issue by designing the PLL at half the RF frequency and then employing frequency doublers for final frequency generation [41]. The frequency doubling operation doubles the output phase, thereby covering the entire required phase range of $-180°$ to $+180°$.

The architecture presented in [25] attains RF phase-shifting but relies on the LO quadrature for this. Consequently, the beamforming occurs in the IF/baseband. One of the first true RF phase-shifting architectures in silicon is described in [27]. The architecture performs cartesian combining, but without the assistance of the quadrature LO. Quadrature versions of the incoming RF signal are generated using a passive quadrature all-pass filter (QAF), which is depicted in Fig. 2.27. The filter achieves accurate quadrature generation of the RF signal over a very wideband (8-18GHz and 18-26GHz), resulting in wideband RF beamforming. From Fig. 2.27, the phase difference between

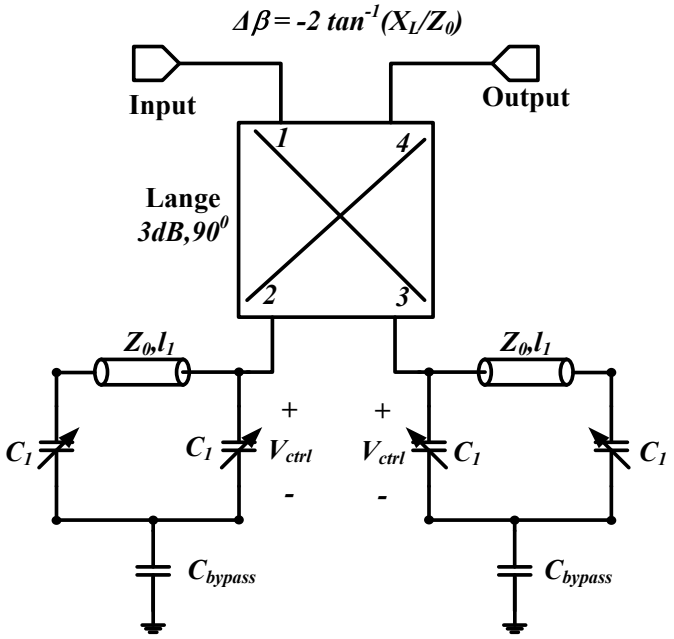


Figure 2.28: Reflective-Type Phase-Shifter for RF phase-shifting with modified loads

quadrature outputs can be expressed as

$$\angle V_{OI} - \angle V_{OQ} = 2\cot^{-1}\left[\frac{1}{2}\left(\frac{\omega_0}{\omega} + \frac{\omega}{\omega_0}\right)\right] \tag{2.32}$$

At the resonant frequency ω_0 ($1/\sqrt{LC}$), the phase difference is exactly equal to 90°. Additionally, the amplitude is the same for both V_{OI} and V_{OQ} at all frequencies. However, VGAs used to create the phase-shift affect the linearity and the noise figure of the RF chain. The authors propose using a high-gain low-NF LNA at the input of the phase-shifter to set the NF of the entire receiver. However, this would severely deteriorate the linearity of this receiver.

Another type of RF phase-shifter, which is widely used, is the reflective-type phase-shifter (RTPS). This phase-shifter relies on the phase of the reflection coefficient created on a transmission line terminated by a purely reactive load. The reflection coefficient for a transmission line terminated with a reactive impedance at the load end is given

by [42]

$$\boldsymbol{\Gamma = \frac{jX - Z_0}{jX + Z_0} \Rightarrow |\Gamma| = 1 \;\&\; \angle\Gamma = -180 - 2\tan^{-1}\frac{X}{Z_0}} \tag{2.33}$$

However, since the forward and reflected waves ride on the same line, a directional or hybrid coupler is placed in front of the reflective load, as shown in Fig. 2.28. The RTPS uses passive blocks and hence, exhibits low power, low NF and excellent linearity. However, since the topology uses transmission lines and/or reactive elements such as capacitors and inductors, it consumes significant area. In addition, the topology attenuates the input signal, which is undesirable in the RF path of a receiver. Further, the limited tuning range of MOS and hyper-abrupt junction varactors in silicon technology, results in a limited phase range. Multiple RTPS structures can be cascaded to achieve the full range of 360°, but this also increases the signal attenuation. To increase the phase range of a single RTPS, a modified reactive load is designed and implemented in [28] for 60GHz applications, as illustrated in Fig. 2.28.

At mm-wave frequencies, LO distribution is an important concern. Especially in the case of the LO phase-shifting architecture, the LO needs to be distributed to all the channels and requires an extensive network of transmission lines and buffers. Further, PLLs running at mm-wave frequencies draw significant power [43] unless the pre-scalar network consists of injection-locked frequency dividers [44,45]. To reduce this power, the LO can be distributed at a lower frequency and local frequency multipliers can be used. Such a scheme is adopted in [46]. In this work, a 2×2 60GHz phased-array transmitter is designed with LO distributed at one-third the RF frequency. The LO is locally tripled in frequency using an injection-locked two-stage ring-oscillator [47] for each of the four channels, as illustrated in Fig. 2.29. Additionally, a common block phase-shifts and quadruples the input frequency of 5GHz ($\boldsymbol{LO_{inj}}$) to the 20GHz injection signal. As described in Fig. 2.16(b) and (2.28), two angles need to be defined to steer the beam in the desired direction. These angles - $\boldsymbol{\beta_x}$ and $\boldsymbol{\beta_y}$ - are depicted in Fig. 2.29. Since each

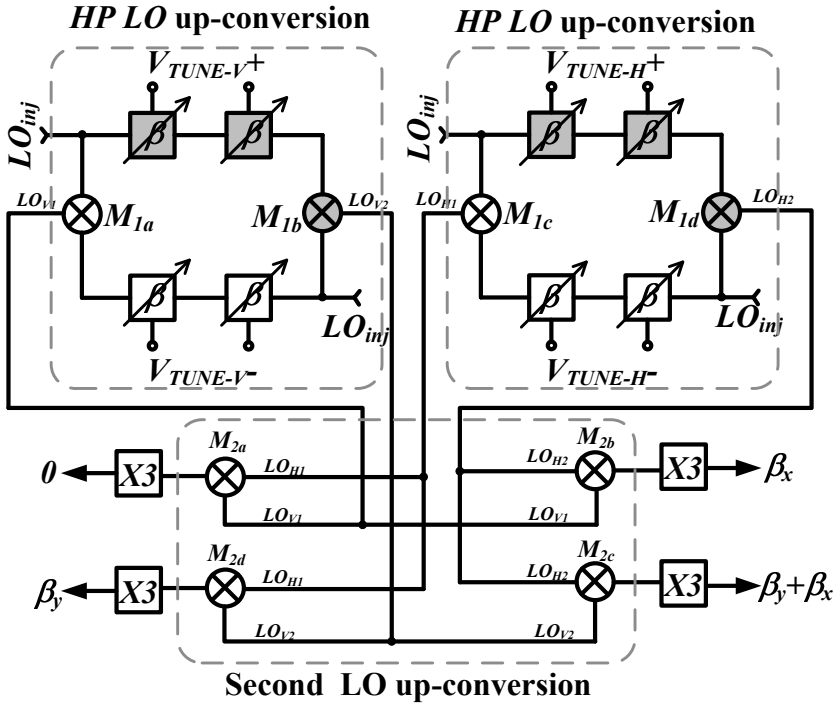


Figure 2.29: Phase-generation and frequency multiplication for a 2×2 60GHz TX

channel requires the full range of 360° at 60GHz, the 5GHz phase-shifters only need to attain a phase range of 30°. This scheme relaxes the specifications for the phase-shifter. However, at the same time any error in phase generation is amplified by 12×. Further power savings can be attained by combining the phase-shifting and frequency tripling operations as is performed in our architecture presented in [24] and explained in Chapter 6.

The unlicensed band for 60GHz wireless communication spans 7GHz (57-64GHz). Consequently, the baseband signal is ultra-wideband. To shield the phase-shifter from the effects of parasitics at mm-wave frequencies, beamforming is performed in the baseband section in [29]. The architecture performs vector modulation of the baseband quadrature signals, to generate phase-shifted outputs, as shown in Fig. 2.30. The VGAs used in the architecture, operate in baseband and hence, draw lower power than their

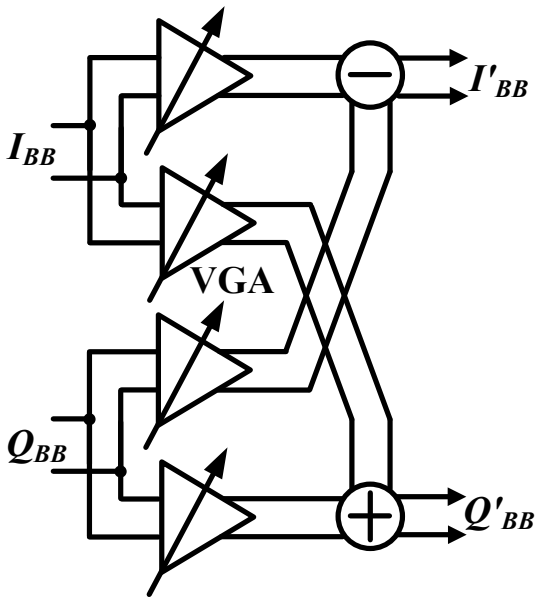


Figure 2.30: Baseband beamforming for 60GHz applications

mm-wave equivalent. And the noise figure of the VGA is suppressed by the gain from the RF stages. However, the linearity requirement becomes more stringent. Another flexibility of baseband beamforming that is not exploited by this architecture is multiple independently steerable beamforming. Such an architecture based on the Fast-Fourier Transform space(FFT) is presented in Chapter 7.

2.7 Summary

In this chapter, we have explained the RF transmitter, receiver and frequency synthesizer, and the functions performed by their constituent blocks. We then discuss the concept of multi-antenna communication with emphasis on phased-arrays. Finally, we elaborate on various architectures for the phased-array and briefly describe the phase-generation schemes used in recent state-of-the-art phased-array transmitters and/or receivers in silicon.

Chapter 3

Injection Locking in LC-Oscillators

Oscillators can be found in various fields, *viz.* electronics, optics, mechanical structures and chemical systems. In electronics, oscillators form the basis of frequency synthesis in wired and wireless communication architectures and clocks in CPUs. In optics, lasers are the equivalent of oscillators and a clock pendulum is an ideal example of a mechanical oscillator. In chemistry, a combination of certain chemicals can be produce *oscillations*, *i.e.*, a reaction which creates a second combination of chemicals, which in turn react to reproduce the original combination of chemicals [48]. In this chapter, we discuss a phenomenon of injection locking of oscillators, with specific emphasis on injection-locking of electronic LC-oscillators. Injection locking forms the basis of the phased-array receiver architectures presented in the next three chapters.

3.1 Injection Locking: Introduction

Injection locking is a phenomenon whereby an oscillatory system is locked to an external signal of frequency close to the natural frequency of the system. The first observations of injection-locking have been reported since 19th century [49]. The oscillator system shifts its oscillation frequency from its natural frequency to the injection frequency. However, this phenomenon occurs only if the injection frequency is within the *lock range* of the oscillator. This range depends on the strength of the injection signal being applied and the quality factor of the oscillator core. The detailed mathematical models are presented in the next section.

External synchronization of oscillators by injection locking has been studied extensively and many of their critical asymptotic properties, such as phase noise and lock range, have been well understood [49–51]. Once locked, the injection-locked oscillator (ILO) behaves like a first-order phase-locked loop (PLL), which under appropriate locking conditions, has a large loop bandwidth and good phase noise properties [49, 50]. Many applications of ILOs exploit these interesting asymptotic properties. For example, in [52] ILOs are used as low power dividers, while in [53] they are designed for precision quadrature generation. Injection-locking also forms the basis of the quadrature VCO (QVCO) which shall be discussed in Section 3.3.

More recently, ILOs have been applied for WiMedia-standard-compliant quadrature frequency synthesizers [54–56] which are constrained by extremely fast hop-time requirements, in clock recovery [57, 58] and de-skewing circuits [59], and in frequency multipliers [47]. ILOs have also been used as phase-shifters in beam-forming applications which form a part of this thesis and is discussed in the next three chapters.

3.2 Mathematical Modeling

The mathematical analysis of injection-locking was first described by R. Adler in his seminal paper in 1948 [50]. The analysis describes a non-linear differential equation which portrays the frequency transient from the oscillator's resonant frequency to the final steady-state injection frequency. The simple and intuitive equation provides for an analytical solution which can be effectively used to predict various interesting aspects of injection-locking [60, 61]. However, Adler's model assumes low injection signal strength, constant signal amplitude and phase symmetry of the tank impedance around the resonant frequency.

Adler's model was modified by Paciorek [62] to accommodate higher injection signal strengths. Due to renewed interest in injection locking, in recent years, many new and improved models have emerged [63, 64], which place reduced constraints on the ILO. However, many of these models do not provide closed-form solutions for the transient differential equation and hence, are not easy for analysis.

3.2.1 Adler's Model

An LC-oscillator can be modeled around its center frequency, $\boldsymbol{\omega_0}$, as a parallel RLC-tank with a parallel negative transconductance cell, denoted by $\boldsymbol{G_m}$. Considering an injection signal of strength $\boldsymbol{I_{inj}}$ and frequency $\boldsymbol{\omega_{inj}}$, the overall injection-locked LC-oscillator can be well-described by Fig. 3.1. $\boldsymbol{I_{osc}}$ is the current flowing through the oscillator and $\boldsymbol{I_T}$ is the vector sum of the injection and oscillator current, as depicted in the figure.

By applying phasor analysis on the currents, we can derive the following equation [50] based on the sine law for triangles:

$$\frac{\sin \phi(t)}{I_{osc}} = \frac{\sin \psi(t)}{I_{inj}} \tag{3.1}$$

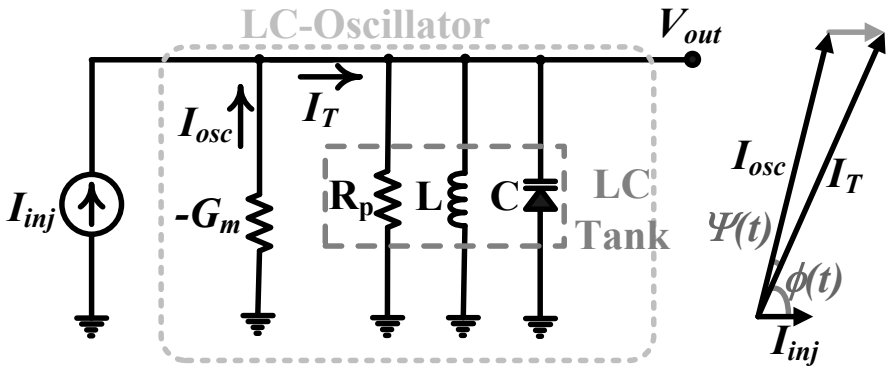


Figure 3.1: Simplified model of an injection-locked LC-oscillator

where $\boldsymbol{\phi(t)}$ is the angle of the $\boldsymbol{I_{osc}}$ with respect to $\boldsymbol{I_{inj}}$ and $\boldsymbol{\psi(t)}$ is the angle between the $\boldsymbol{I_{osc}}$ and $\boldsymbol{I_T}$. Adler's model places a constraint of low relative injection signal strength, $\boldsymbol{I_{inj} \ll I_{osc}}$, which implies that $\boldsymbol{\psi(t)}$ is a very small angle ($\boldsymbol{\ll 1}$) and hence (3.1) is a valid approximation. Also, applying the approximation $\boldsymbol{\sin \psi(t) \approx \psi(t)}$, (3.1) can now be modified as

$$\psi(t) = \frac{I_{inj}}{I_{osc}} \sin \phi(t) \tag{3.2}$$

Since $\boldsymbol{I_{osc}}$ and $\boldsymbol{V_{out}}$ are related by $\boldsymbol{-G_m}$, and $\boldsymbol{V_{out}}$ is created by $\boldsymbol{I_T}$ flowing into the RLC-tank (impedance$=$ $\boldsymbol{Z_{tank}}$), these relationships can be expressed

$$I_{osc} = -(-G_m) \times V_{out} \qquad V_{out} = Z_{tank} \times I_T \tag{3.3}$$

which implies that $\boldsymbol{I_{out}}$ and $\boldsymbol{V_{out}}$ are in phase, and $\boldsymbol{I_T}$ and $\boldsymbol{V_{out}}$ are separated by the phase of the tank ($\boldsymbol{\psi(t) = \angle Z_{tank}}$). It should be noted here that $\boldsymbol{G_m}$ is the large signal transconductance.

The phase of the tank impedance around its resonant frequency can be linearized and assumed to be symmetric (invoking the symmetry condition of the RLC-tank around $\boldsymbol{\omega_0}$ stated earlier) and expressed as

$$\tan \psi(t) = \frac{2Q}{\omega_0}\{\omega_0 - \omega(t)\} \approx \psi(t) \tag{3.4}$$

where $\boldsymbol{Q}$ is the quality factor of the RLC-tank. Combining (3.2) and (3.4),

$$\boldsymbol{\omega(t) = \omega_0 - \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}\sin\phi(t)} \tag{3.5}$$

Subtracting $\boldsymbol{\omega_{inj}}$ from both sides and applying the relation $\boldsymbol{d\phi(t)/dt = \omega(t) - \omega_{inj}}$, we obtain the final version of Adler's equation.

$$\boldsymbol{\frac{d\phi(t)}{dt} = \omega_0 - \omega_{inj} - \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)\sin\phi(t)} \tag{3.6}$$

When the ILO reaches steady-state, *i.e.*, it is locked, the phase settles to a constant value implying $\boldsymbol{d\phi(t)/dt = 0}$. Applying this condition yields the steady-state phase, $\boldsymbol{\phi_{ss}}$

$$\boldsymbol{\phi_{ss} = \sin^{-1}\left(\frac{\omega_0 - \omega_{inj}}{\frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}}\right)} \tag{3.7}$$

The quantity in the denominator is the lock-range ($\boldsymbol{\omega_L}$) of the ILO. If the injection frequency is within the lock-range, the oscillator locks to it.

$$\boldsymbol{\omega_L = \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)} \tag{3.8}$$

At the two edges of the of the lock-range $\boldsymbol{\phi_{ss} = \pm\pi/2}$ Adler's equation is a differential equation of $\boldsymbol{\phi(t)}$ with respect to time $\boldsymbol{t}$. The solution can be: $\boldsymbol{\phi}$ as a function of $\boldsymbol{t}$, or $\boldsymbol{t}$ as a function of $\boldsymbol{\phi}$. The two solutions [50, 60] are

$$\boldsymbol{\phi(t) = 2\tan^{-1}\left[\left(\frac{\omega_L}{\omega_0 - \omega_{inj}}\right) - \left(\frac{\omega_B}{\omega_0 - \omega_{inj}}\right) \times \tanh\left(\frac{\omega_B(t - t_0)}{2}\right)\right]} \tag{3.9}$$

$$\boldsymbol{t = \frac{1}{\omega_B}\ln\left|\left(\frac{\tan\left(\frac{\phi(t)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(0)}{2}\right) - \cot\left(\frac{\phi_{ss}}{2}\right)}\right)\left(\frac{\tan\left(\frac{\phi(0)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}{\tan\left(\frac{\phi(t)}{2}\right) - \tan\left(\frac{\phi_{ss}}{2}\right)}\right)\right|} \tag{3.10}$$

where

$$\boldsymbol{\omega_B = \sqrt{\omega_L^2 - (\omega_0 - \omega_{inj})^2}}$$

and $\boldsymbol{t_0}$ is an integration constant which can take up complex values under certain conditions. These solutions portray the exponential settling behavior of the phase $\boldsymbol{\phi(t)}$. Each

of these solutions present its own advantages and disadvantages. Equation (3.9) can be used to analyze the phase settling and its time derivative yields the frequency settling. On the other hand, (3.10) can be used to deduce the factors which affect the lock-time of the ILO. This equation provides valuable insights for the design of fast-hopping ILOs, as described in [54, 65].

3.2.2 Paciorek's Model

The same phasor analysis as used by Adler to derive the non-linear differential equation (3.6), was used by Paciorek [62] to derive the modified equation which allows for higher injection signal strengths. The sine law equation of (3.1) without approximation, is

$$\frac{\sin\{\phi(t)-\psi(t)\}}{I_{osc}} = \frac{\sin\psi(t)}{I_{inj}} \Rightarrow \tan\psi(t) = \frac{I_{inj}\sin\phi(t)}{I_{osc}+I_{inj}\cos\phi(t)} \tag{3.11}$$

Applying (3.4), the above equation can be modified into Paciorek's differential equation

$$\frac{d\phi}{dt} = \omega_0 - \omega_{inj} - \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)\frac{\sin\phi(t)}{1+(I_{inj}/I_{osc})\cos\phi(t)} \tag{3.12}$$

The lock-range for Paciorek's model can be derived by maximizing $\sin\phi(t)/[1+(I_{inj}/I_{osc})\cos\phi(t)]$ for all values of $\phi(t)$. The lock-range is derived to be

$$\omega_L = \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)\frac{1}{\sqrt{1-(\frac{I_{inj}}{I_{osc}})^2}} \tag{3.13}$$

Paciorek's equation can be solved into an closed-form expression [62].

$$\begin{aligned} B(1+K^2)t \;&= \frac{1}{\sqrt{1+K^2\left(1-\frac{1}{C^2}\right)}}\ln\left[\frac{\frac{C\sqrt{1+K^2}+K\sin u+C\sqrt{1+K^2\left(1-\frac{1}{C^2}\right)}\cos u}{K+C\sqrt{1+K^2}\sin u}}{\frac{C\sqrt{1+K^2}+K\sin u_0+C\sqrt{1+K^2\left(1-\frac{1}{C^2}\right)}\cos u_0}{K+C\sqrt{1+K^2}\sin u_0}}\right] \\ &\quad + Ck(u-u_0) - C.\ln\left[\frac{K+C\sqrt{1+K^2}\sin u}{K+C\sqrt{1+K^2}\sin u_0}\right] \end{aligned} \tag{3.14}$$

where

$$B = \frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right) \qquad C = \left(\frac{I_{inj}}{I_{osc}}\right) \qquad K = \frac{\omega_0-\omega_{inj}}{\frac{\omega_0}{2Q}}$$

$$\theta = \tan^{-1} K \qquad u = \phi - \theta$$

The steady-state phase can be derived as

$$\phi_{ss} = \sin^{-1}\left(\frac{2Q}{\omega_0}\frac{I_{osc}}{I_{inj}}\frac{\omega_0 - \omega_{inj}}{\sqrt{1+K^2}}\right) + \sin^{-1}\left(\frac{2Q}{\omega_0}\frac{\omega_0 - \omega_{inj}}{\sqrt{1+K^2}}\right) \tag{3.15}$$

Although Paciorek's equation provides a more accurate potrayal of for the ILO transient behavior, the solution to the differential equation is extremely hard to analyze. Consequently, Adler's model is widely used for ILO analysis.

3.2.3 Other Models

The models proposed by Adler and Paciorek assume symmetric RLC loads and the linearity of tank impedance phase around its 3-dB bandwidth (ω_0/Q). However, in CMOS processes the achieved inductor Q's are relatively low, especially for custom inductors designed in digital CMOS processes. Further, an on-chip tank is modeled as a capacitance C in parallel with the series combination of R and L. In such cases, the above mentioned models fail to predict the asymmetry of the lock-range around the resonant frequency. The model proposed in [64] provides a better estimate of the transient behavior. This model, however, is not conducive to a closed-form solution and numerical computation techniques need to be applied for analysis.

3.3 Injection Locking of Quadrature Oscillators

The concept of two coupled oscillators oscillating in quadrature was first reported in the 1930's [66] and its first on-chip CMOS implementation was reported in 1996 [66]. When two oscillators are coupled in feedback, in addition to Barkhausen's loop criteria for each individual oscillator, the phase criterion for the feedback loop also needs to be satisfied. Fig. 3.2 shows the feedback loop structure used to construct a quadrature

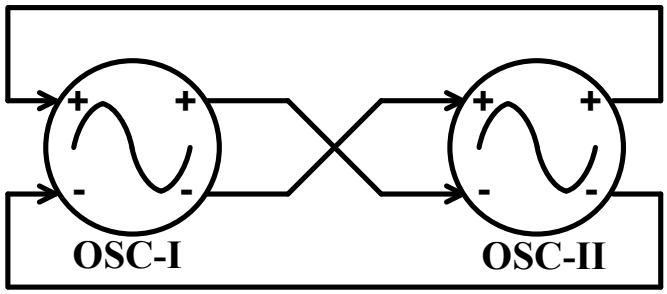


Figure 3.2: Feedback structure of the QVCO

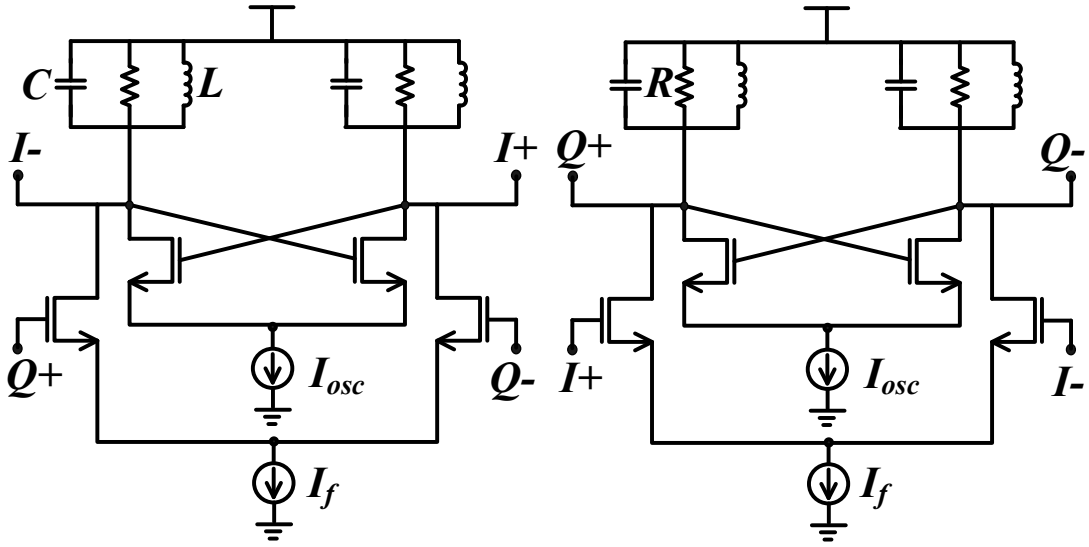


Figure 3.3: Quadrature VCO

voltage-controlled oscillator or QVCO. Coupling between the oscillators can be introduced as a current or voltage) by a zero-phase or π-phase coupling network. Since the overall loop needs to have zero or $\mathbf{2\pi}$ phase-shift and a phase-shift of π is already introduced by the feedback loop structure, the effective outputs of the two oscillators operate with a phase-shift of $\boldsymbol{\pi/2}$ or $\boldsymbol{-\pi/2}$.

3.3.1 The Quadrature Oscillator

Consider the QVCO shown in Fig. 3.3. A simplified figure and the phasor diagram of the QVCO are shown in Fig. 3.4. The phasor diagram in Fig. 3.4(b) represents the orientation of various signals in steady-state. By applying the zero (or $\boldsymbol{2\pi}$) phase condition on the loop, we arrive at the requirement for the two oscillators to lock in quadrature:

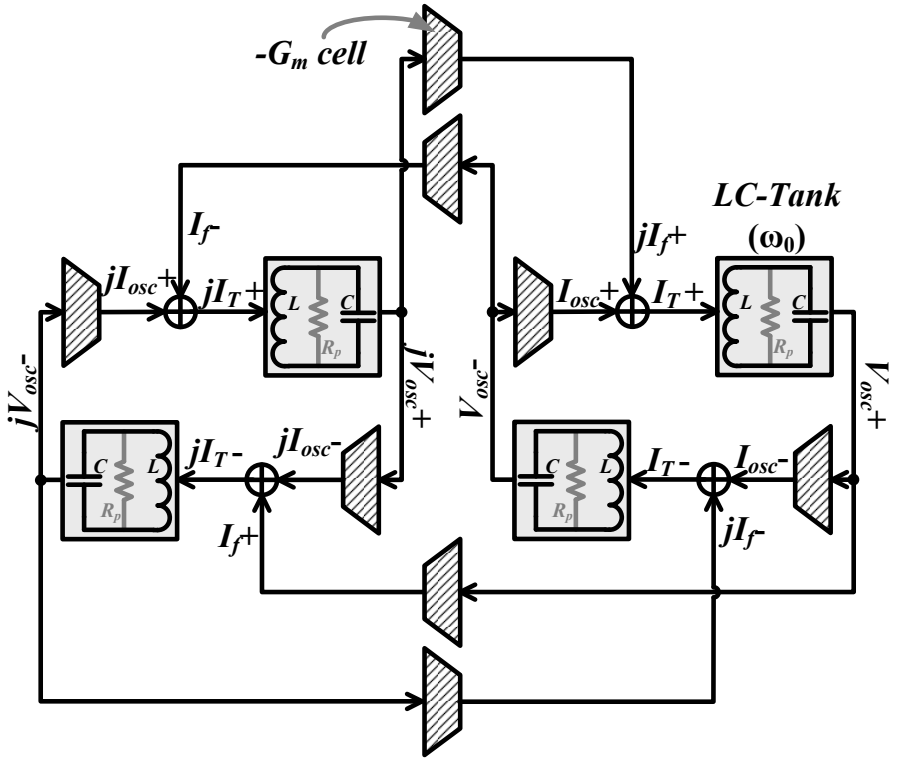
$$\boldsymbol{\phi_{ss} + \psi_{ss} = \pm\frac{\pi}{2}} \tag{3.16}$$

The '$\pm$' denotes that one of the two oscillators could lead or lag the other by $\boldsymbol{\pi/2}$ or 90°. Under ideal conditions of parallel RLC model for the tank and perfect matching between the two oscillators, either of the two states are possible. However, due to the asymmetry of an on-chip LC-tank around its center frequency and the mismatch between oscillators, the QVCO settles to one of the states [67]. For the case depicted in Fig. 3.4, $\boldsymbol{\phi_{ss} + \psi_{ss} = \pi/2}$. This condition requires the QVCO to shift its frequency $\boldsymbol{\omega_{QVCO}}$, such that $\boldsymbol{\omega_{QVCO} < \omega_0}$. This phenomenon can be viewed as two oscillators trying to injection-lock to each other and settling to a *mutually agreeable* frequency. Continuing from (3.16), $\boldsymbol{\omega_{QVCO}}$ can be determined as follows:

$$\boldsymbol{\psi_{ss} = \pm\frac{\pi}{2} - \phi_{ss} \Rightarrow \pm\frac{2Q}{\omega_0}(\omega_0 - \omega_{QVCO}) = \cot(\phi_{ss}) = \frac{I_f}{I_{osc}}}$$

$$\boldsymbol{\Rightarrow \omega_{QVCO} = \omega_0 \pm \frac{\omega_0}{2Q}\left(\frac{I_f}{I_{osc}}\right)} \tag{3.17}$$

This implies that each oscillator of the QVCO is pushed to the same edge (either higher or lower) of the lock-range. This is intuitive, since the output of each block of the QVCO is phase-shifted with respect to the feedback signal by $\pm$90°, at the edge of lock-range.

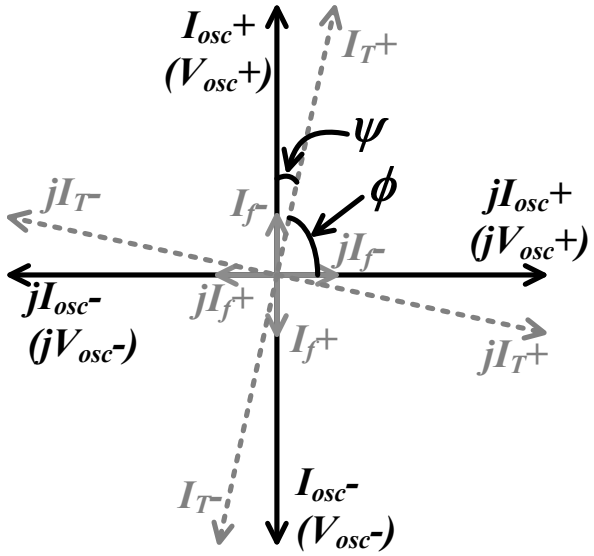


(a) QVCO block diagram

Figure 3.4: Simplified diagram and phasor representation of QVCO

3.3.2 Adler-like Model

The QVCO output spectrum still behaves like an open-loop system, since both the oscillators in the QVCO are open-loop. In order to stabilize it, the QVCO has to be locked to a low-noise reference either through a phase-locked loop (PLL) [68] or through injection-locking [53]. A particular scheme for injection locking the QVCO is shown in Fig. 3.5 and its block diagram is shown in Fig. 3.6(a). The principal idea is to lock the two oscillators of the QVCO to a pair of quadrature injection signals. This adds a set of four additional current vectors to the phasor diagram in Fig. 3.4(b). To simplify the understanding of the phasor mechanics, only one set of phasors of the quadrature signals is shown in Fig. 3.6(b).



(b) QVCO phasor interpretation

Figure 3.4: Simplified diagram and phasor representation of QVCO

By taking into account the two assumptions stated while deriving Adler's equation for an ILO, we derive the Adler's equivalent equation for a QILO. In the following derivation, we also assume that $|\boldsymbol{I_{inj}} \pm| = |j\boldsymbol{I_{inj}} \pm| = \boldsymbol{I_{inj}}$ and the same is true for $\boldsymbol{I_{osc}}$, $\boldsymbol{I_T}$, $\boldsymbol{I_f}$ and $\boldsymbol{I_r}$. Applying the sine-law for triangles to this case, we arrive at

$$\frac{\mathbf{sin}\{\psi(t)\}}{\boldsymbol{I_r}} = \frac{\mathbf{sin}\{\phi(t) - \beta(t)\}}{\boldsymbol{I_{osc}}} \tag{3.18}$$

And the angle between $\boldsymbol{I_{inj}}$ and $\boldsymbol{I_f}$ vectors is $\boldsymbol{2\pi - 3\pi/2 - \phi(t) - \psi(t) = \pi/2 - \phi(t) - \psi(t)}$. This adds two more relations:

$$\boldsymbol{I_r}\,\mathbf{cos}\{-\beta(t)\} = \boldsymbol{I_{inj}} + \boldsymbol{I_f}\,\mathbf{sin}\{\phi(t) + \psi(t)\} \tag{3.19}$$

$$\boldsymbol{I_r}\,\mathbf{sin}\{-\beta(t)\} = \boldsymbol{I_f}\,\mathbf{cos}\{\phi(t) + \psi(t)\} \tag{3.20}$$

Substituting (3.19) and (3.20) into (3.18), gives

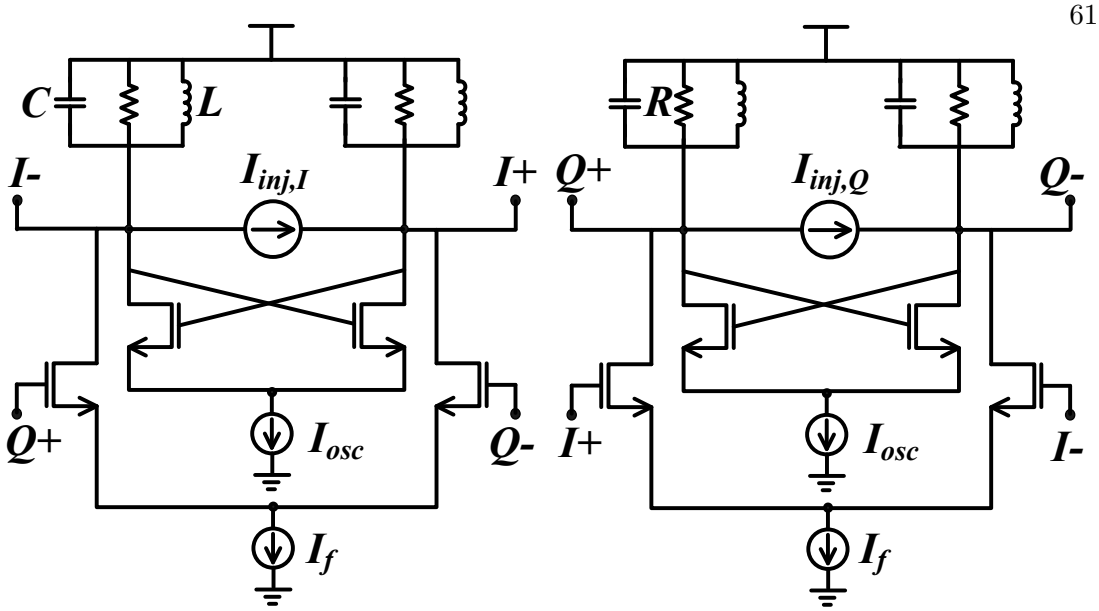


Figure 3.5: Injection locked quadrature VCO (QILO)

$$\begin{aligned}\sin\{\psi(t)\} &= \frac{\sin\{\phi(t)\}[I_{inj} + I_f \sin\{\phi(t)+\psi(t)\}]}{I_{osc}} \\ &\quad + \frac{\cos\{\phi(t)\}[I_f \cos\{\phi(t)+\psi(t)\}]}{I_{osc}} \\ &= \frac{I_{inj}}{I_{osc}} \sin\{\phi(t)\} + \frac{I_f}{I_{osc}} \cos\{\psi(t)\} \end{aligned} \tag{3.21}$$

Assuming the small-injection approximation ($\sin\{\psi(t)\} = \psi(t)$, $\cos\{\psi(t)\} = 1$) and substituting (3.4), (3.21) can be reduced to

$$\begin{aligned}\frac{d\phi(t)}{dt} &= \underbrace{\left(\omega_0 - \frac{\omega_0}{2Q}\frac{I_f}{I_{osc}}\right)}_{\approx \omega_{QVCO}} - \omega_{inj} - \underbrace{\frac{\omega_0}{2Q}\left(\frac{I_{inj}}{I_{osc}}\right)}_{= \omega_L} \sin\{\phi(t)\} \\ \Rightarrow \frac{d\phi(t)}{dt} &\approx (\omega_{QVCO} - \omega_{inj}) - \omega_L \sin\{\phi(t)\} \end{aligned} \tag{3.22}$$

The quantity, ω_L, can be defined as the single-sided lock-range of the QILO around the center frequency of the QVCO, ω_{QVCO}. Equation (3.22) is the same form as Adler's equation. Hence, the solutions (3.9, 3.10) to the non-linear differential equation can be

extended to the QILO. Also, the theories/predictions on ILO presented in [60] can be applied to the QILO.

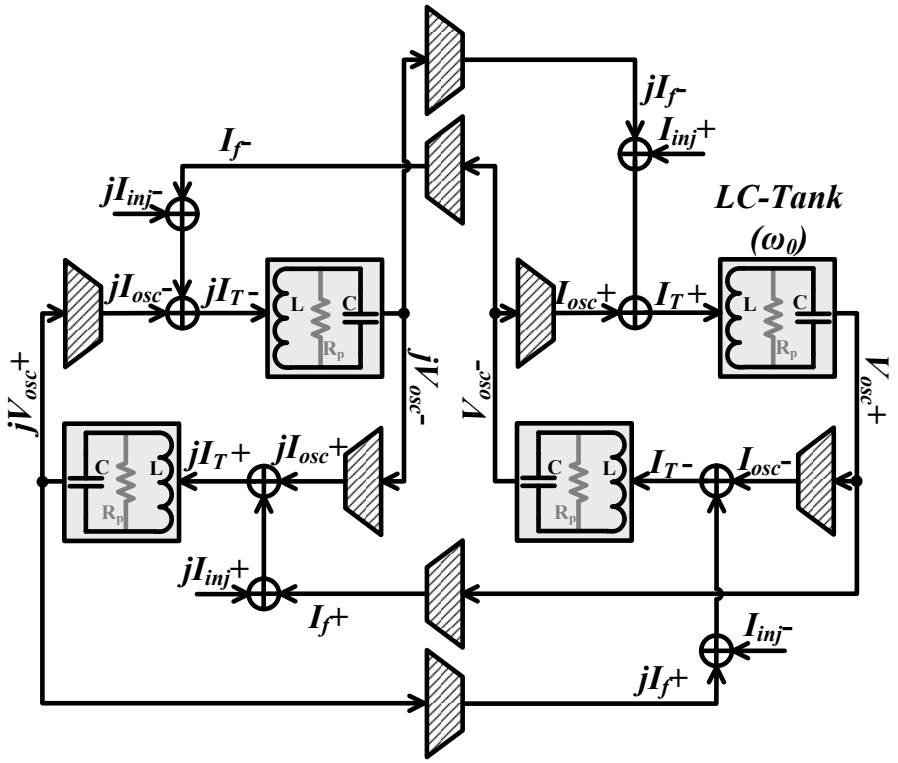
The steady-state phase, ϕ_{ss}, for the QILO is given by

$$\phi_{ss} = \sin^{-1}\left(\frac{\omega_{QVCO} - \omega_{inj}}{\omega_L}\right) \tag{3.23}$$

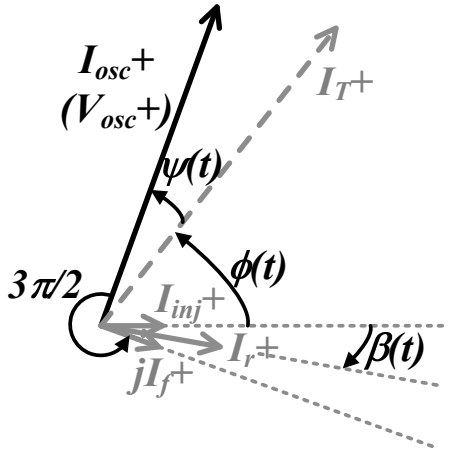
As in the case of an ILO, this model can also be extended to larger injection signal strengths (Paciorek-like model).

3.4 Summary

In this chapter, we discussed the basic theory of injection-locking and the mathematical models proposed to portray its transient behavior. We then discussed the steady-state behavior of a quadrature VCO and presented the Adler-like model which describes the transient during injection-locking of the QVCO to an external signal. The concepts developed in this chapter will be used to develop the ILO as a phase-shifter in the next chapter.



(a) QILO block diagram



(b) QILO phasor interpretation

Figure 3.6: QILO simplified diagram and phasor representation

Chapter 4

Beamforming using Injection Locking

Injection-locking has been used to a limited extent in phased-arrays, previously. There have been some efforts in the last three decades [69–71]. The basic concept underlying these different schemes is that the output of an injection-locked oscillator (ILO) is phase-shifted with respect to the injection signal. However, depending upon the ILO array design, the phase-generation capabilities of these different schemes vary. We will briefly discuss the work presented in [69], [70] and [71] in the following section. Following that, we propose two schemes developed in our work and compare them. Finally, we extend these ideas to 2D beamforming and quadrature ILOs.

4.1 Previous work with ILOs in Phased Arrays

One of the first attempts to use injection-locking for phase-generation is proposed in [69]. In this architecture, an array of LC-oscillators are injection-locked to a common injection signal. The injection signal frequency (ω_{inj}) is four times the fundamental output

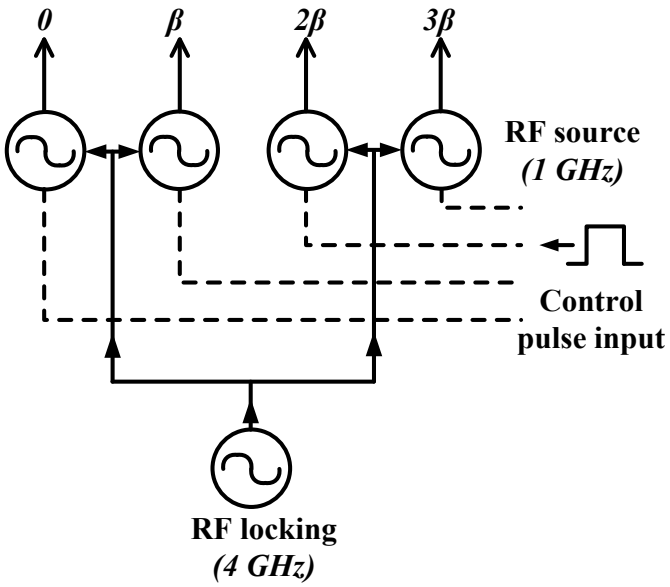


Figure 4.1: n-th harmonic locking used for phase-generation in steps of $2\pi/n$

frequency of the oscillator array, resulting in harmonic injection-locking. In order to achieve lock, the oscillator's resonant frequency ω_0 should be close to the fundamental component ($\omega_{inj}/4$). This is similar in operation to injection-locked frequency dividers (ILFDs) [52]. The basic architecture used in [69] is depicted in Fig. 4.1. Consider any set of two ILOs locked to the RF source. In order to generate the required phase-shift in the first ILO, pulsed signals are used on the DC bias of that oscillator to change its resonant frequency sufficiently, so that it goes out of lock. The duration of this pulse is accurately controlled to one period of the injection signal ($2\pi/\omega_{inj}$). Once the pulse duration ends, the DC bias of the oscillator is pulled back to its original value and locking is quickly restored. However, due to the pulse duration, the first ILO output is now phase-shifted with respect to the second ILO by $\pi/2$. The sign of the phase-shift can be controlled by the polarity of the pulse applied to the DC bias. The architecture provides an effective method for phase-generation and was one of the first attempts at digital phase-shifting. However, the phase-steps that are possible are multiples of $2\pi/n$, if the injection signal

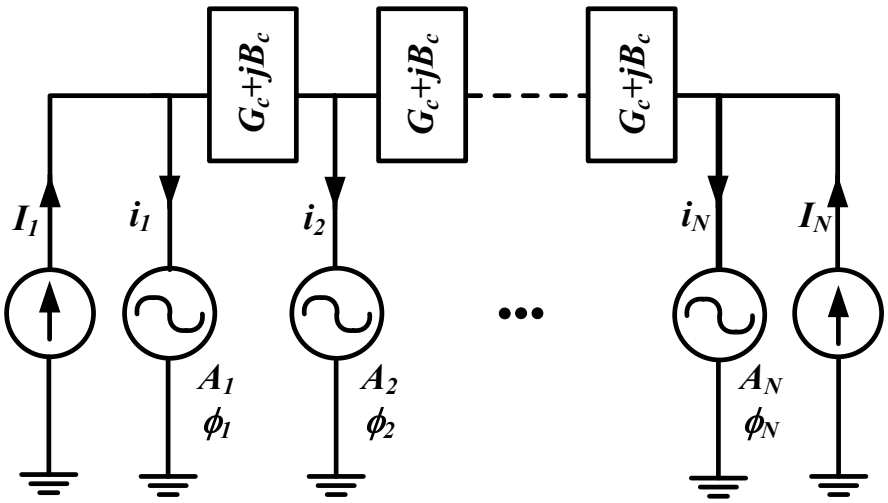


Figure 4.2: Inter-injection-locked array of oscillators with phase-shifted injection at the two ends

is the n-th harmonic of the fundamental signal. For small phase-resolution requirements, the injection signal frequency becomes prohibitively large. Consequently, this technique is not well-suited for integrated mm-wave applications.

The techniques proposed in [70] and [71], use an array of inter-injection-locked oscillators to generate the progressive phase-shift pattern required for beamforming. In an inter-injection locked array of oscillators, each oscillator tries to lock its two neighboring oscillators. Since the coupling between oscillators is bi-directional, the Adler's analysis cannot be used to describe the locking behavior of the array. In [70], bi-directional passive coupling networks is placed in between every pair of adjacent oscillators, as illustrated in Fig. 4.2. By applying a phase-shifted pair of signals to the end oscillators, a progressive pattern of phase-shifts can be created at the oscillator outputs. For an array of N similar oscillators, the phase difference between adjacent oscillators is ϕ/N, where ϕ is the phase-difference between the injected signals at the two ends. This restricts the maximum phase shift possible in this configuration. In addition, it requires a phase-shifted pair of signals with variable phase-shift for beamsteering. To overcome these

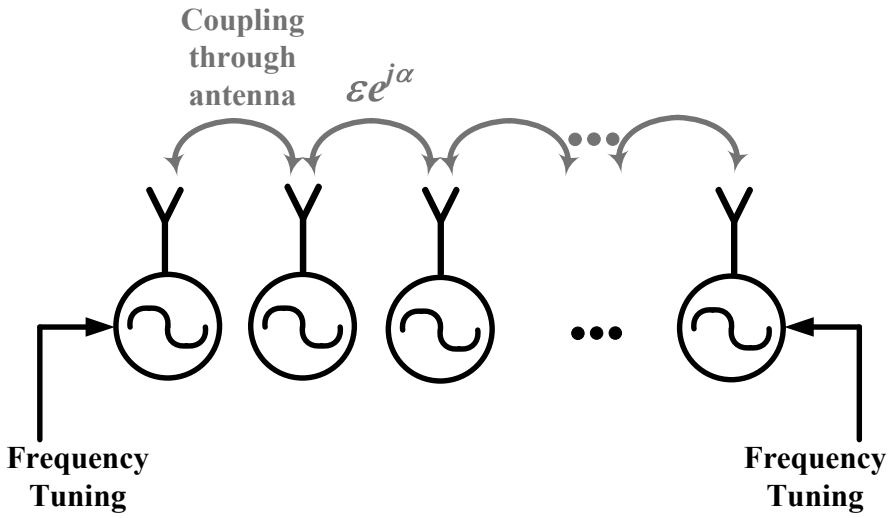


Figure 4.3: Inter-injection-locked array of oscillators with end-element tuning

limitations, [71] proposes a different technique to achieve the progressive phase-shift in an inter-injection-locked array.

A coupled array of oscillators mutually settle to a frequency. This can be viewed as an extension of the QVCO discussed in Chapter 3. In the work presented in [71], a progressive pattern of phase-shifts can be obtained by tuning the frequency of the end elements alone. If a consecutive element phase difference of $\boldsymbol{\beta}$ is desired from an N-element coupled oscillator array (Fig. 4.3) at frequency $\boldsymbol{\omega_f}$, the free-running frequency of the $\boldsymbol{i}$-th oscillator ($\boldsymbol{\omega_i}$) should be tuned to

$$\omega_i = \begin{cases} \omega_f \left[1 + (\epsilon/2Q)\sin(\beta + \alpha)\right] & \text{for } i = 1 \\ \omega_f \left[1 + 2(\epsilon/2Q)\cos\beta\sin\alpha\right] & \text{for } 1 < i < N \\ \omega_f \left[1 - (\epsilon/2Q)\sin(\beta - \alpha)\right] & \text{for } i = N \end{cases} \tag{4.1}$$

where $\boldsymbol{Q}$ is the quality factor of the oscillator tank, and $\boldsymbol{\epsilon}$ and $\boldsymbol{\alpha}$ are the magnitude and phase of the coupling coefficient between adjacent oscillators respectively. If the

coupling coefficient, is real (α =0 or 180°), the (4.1) takes a simpler form.

$$\omega_i = \begin{cases} \omega_f \left[1 + (\epsilon/2Q) \sin\beta\right] & \text{for } i = 1 \\ \omega_f & \text{for } 1 < i < N \\ \omega_f \left[1 - (\epsilon/2Q) \sin\beta\right] & \text{for } i = N \end{cases} \tag{4.2}$$

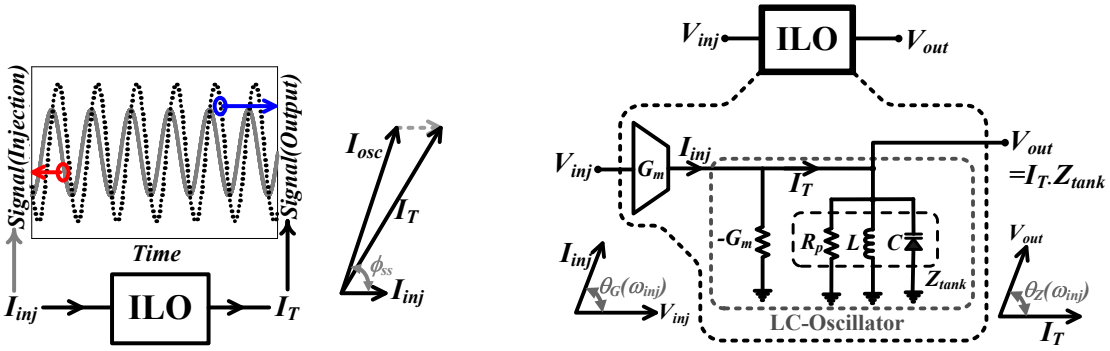
Thus, the final frequency of the oscillator array is equal to the frequency of the inner elements. By tuning end-elements in opposite directions ($\omega_1 > \omega_f$ and $\omega_N < \omega_f$ or vice-versa), the beam can be steered to either side of the broadside direction. However, the stability analysis shows that the oscillator array is stable only for β values between $-90°$ and $+90°$. Hence, for the half-wavelength spacing antenna array ($d = \lambda/2$), the beamsteering is restricted to $\pm 30°$ around the broadside direction. Further, the coupling mechanism of the array is through the antennas. Hence, the coupling coefficient is very small. Consequently, the lock-range of each individual oscillator is restricted and extremely accurate frequency tuning is required to steer the beam. In integrated implementations, in the presence of mismatch, the oscillator array may not be able to settle to a common frequency.

We propose a modified scheme to use the ILO as a phase-shifter, but with the major improvement in the phase-shift mechanism. It allows for accurate phase control and the entire range for β from $-180°$ to $+180°$. We propose two techniques for progressive phased-generation based on this scheme.

4.2 Two Proposed Techniques for Phase Generation

For ease of understanding, we will briefly re-visit the basic concepts of Adler's theory. When the ILO reaches steady-state, the phase difference $\phi(t)$, between the output and the injection signal attains a constant value, defined by ϕ_{ss}, expressed as

$$\phi_{ss} = \sin^{-1}\left(\frac{\omega_0 - \omega_{inj}}{\omega_L}\right) \tag{4.3}$$



(a) Current-Input Current-Output (b) Voltage-Input Voltage-Output

Figure 4.4: ILO as a phase-generation block (the amplitudes in the plot are not to scale)

where ω_0 and ω_{inj} are the oscillator's resonant frequency and injection frequency, respectively. And the quantity ω_L is the lock-range of the ILO. The steady-state frequency of the ILO is equal to ω_{inj}. So under relevant conditions, the ILO can be viewed as a buffer block whose input (injection) and output frequencies are the same, and the input-to-output phase difference is given by (4.3). Also, this phase difference can be varied by changing either ω_L or ω_0. By independently varying both these quantities, the phase-generation scheme can be made very flexible. ω_L can be varied by changing I_{inj} and ω_0 can be controlled using a voltage-controlled oscillator (VCO) as the oscillator core. For simplicity, in our architecture, we have chosen to only control ω_0. An important point to remember is that varying ω_0 also changes ω_L.

For our ILO design, the injection signal is an RF voltage signal. And the local-oscillator (LO) input to a mixer is also voltage-based. The models for ILO presented in Chapter 3, assume the signal is in the form of a current. So the ILO model needs to be modified from a current-input current-output block to a voltage-input voltage-output block as shown in Fig. 4.4. From Fig. 4.4(a) and (4.3), we can approximate that for low injection levels [50],

$$\angle I_{osc} - \angle I_{inj} \approx \angle I_T - \angle I_{inj} = \phi_{ss}(\omega_0) \tag{4.4}$$

And from Fig. 4.4(b) and (4.4), it can be deduced that

$$\angle \boldsymbol{V_{out}} - \angle \boldsymbol{V_{inj}} \approx \boldsymbol{\phi_{ss}(\omega_0) + \theta_Z(\omega_{inj}) - \theta_G(\omega_{inj})} \tag{4.5}$$

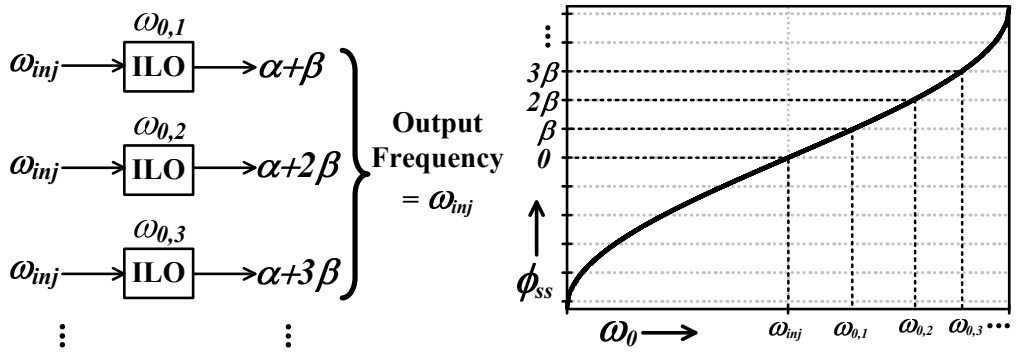
where $\boldsymbol{\theta_G(\omega_{inj})}$ is the phase difference between the voltage injection signal, $\boldsymbol{V_{inj}}$, and the output current signal, $\boldsymbol{I_{inj}}$, from the $\boldsymbol{G_m}$ cell when the injection frequency is $\boldsymbol{\omega_{inj}}$, and $\boldsymbol{\theta_Z(\omega_{inj})}$ is the phase difference between the total current flowing through the tank $\boldsymbol{I_T = I_{osc} + I_{inj}}$ (as shown in Fig. 4.4) and the output of the ILO. Since the injection frequency is a constant, so are $\boldsymbol{\theta_Z(\omega_{inj})}$ and $\boldsymbol{\theta_G(\omega_{inj})}$. In a phased array system, the phase-shift pattern applied are in arithmetic progression - $\boldsymbol{\alpha + \beta}$, $\boldsymbol{\alpha + 2\beta}$, $\boldsymbol{\alpha + 3\beta}$, $\boldsymbol{\ldots}$ - where $\boldsymbol{\alpha}$ is a constant and $\boldsymbol{\beta}$ is the progressive phase-shift [11]. For our case, we can define $\boldsymbol{\alpha = \theta_Z(\omega_{inj}) - \theta_G(\omega_{inj})}$. And the progressive $\boldsymbol{\beta}$-component can be obtained by varying $\boldsymbol{\omega_0}$ to different values - $\boldsymbol{\omega_{0,1}}$, $\boldsymbol{\omega_{0,2}}$, $\boldsymbol{\omega_{0,3}}$, ...- so that

$$\boldsymbol{\beta = \phi_{ss}(\omega_{0,1}),\ 2\beta = \phi_{ss}(\omega_{0,2}),\ 3\beta = \phi_{ss}(\omega_{0,3}),\ \ldots}$$

as shown in Fig. 4.5. Two important considerations here are - (a) the phase-frequency relationship is non-linear, and (b) $\boldsymbol{\phi_{ss}}$ lies in the interval $\boldsymbol{[-90°, 90°]}$. Due to their non-linear relationship, precise phase resolution requires accurate frequency control. In order to support the entire phase range of $\boldsymbol{360°}$, an additional $\boldsymbol{180°}$ of phase can be achieved by selectively inter-changing the terminals in a differential ILO implementation. We will now discuss the two proposed architectures - (a) fully-flexible and (b) meander-line.

4.2.1 Fully-Flexible Architecture

The fully-flexible architecture is derived from the concept presented in Fig. 4.5(a). A common injection signal is applied to an array of ILOs. By individually tuning their resonant frequencies, the required phase-pattern can be achieved (Fig. 4.6(a)). In many radar applications, specific phase- and amplitude-patterns are required in order to generate lower side-lobes and/or generate nulls in certain directions (directions of jammers



(a) Phase generation (b) Phase-frequency mapping (for $\boldsymbol{\alpha = 0}$)

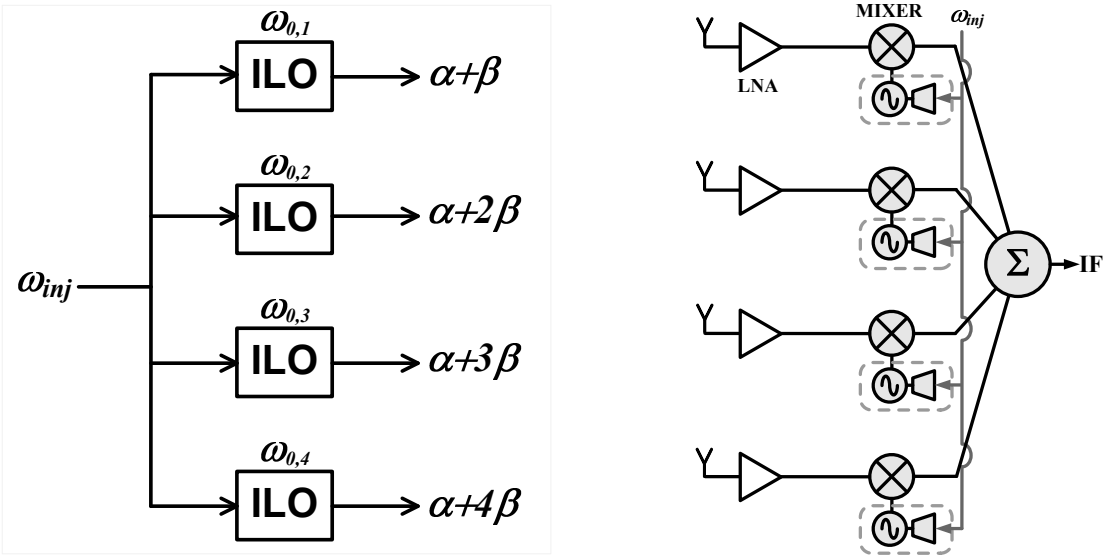
Figure 4.5: Generating phase patterns using ILOs - non-linear relationship between phase $(\boldsymbol{\phi_{ss}})$ and resonant frequency $(\boldsymbol{\omega_0})$ requires accurate control over $\boldsymbol{\omega_0}$

or interferers). The fully-flexible architecture can be easily configured to generate the required phase-pattern. In addition, to generate the desired amplitude pattern, an RF or IF VGA can be placed in the signal path. The basic schematic of the fully-flexible architecture is shown in Fig. 4.6(b).

This architecture can be easily extended to 2-D phased-array systems. Two important considerations, however, are - (a) symmetric distribution of the injection signal, and (b) a look-up table (LUT) to store the phase-frequency relationship for accurate phase control. The first issue can be tackled by approaches similar to clock-tree distribution solutions. The second requires the use of digitally-controlled oscillator (DCO) or a digital-to-analog converter (DAC) controlled varactor load. This would allow the use of a digital LUT that can be easily implemented as a small shift-register-based memory.

4.2.2 Meander-Line Architecture

When locked, the input and output frequencies of an ILO are the same, with a phase-shift. This phenomenon can be exploited to derive a second scheme for phase-generation. As depicted in Fig. 4.7(a), a cascade of ILOs can be easily programmed to generate the



(a) Independent Phase Control

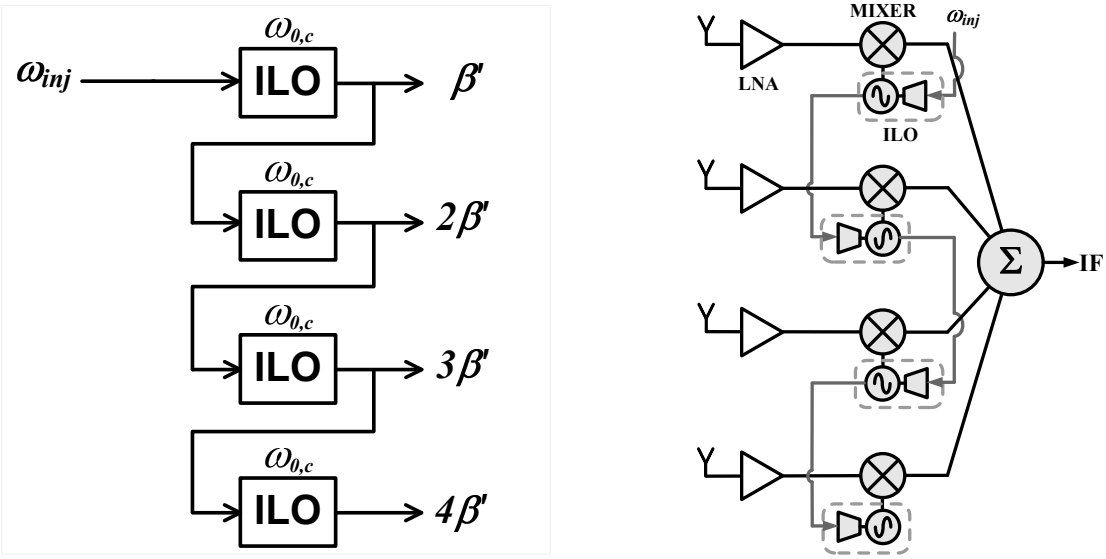
(b) Fully flexible architecture

Figure 4.6: Fully flexible architecture derived from independent phase control scheme arithmetically-progressive phase-shift pattern. By tuning each ILO to the same resonant frequency $(\omega_{0,c})$, a constant phase-shift (β') can be automatically obtained. Then the cascade scheme generates the desired phase-pattern. From (4.5), the constant (β') can be expressed as

$$\beta' = \phi_{ss}(\omega_0) + \theta_Z(\omega_{inj}) - \theta_G(\omega_{inj}) \tag{4.6}$$

The corresponding receiver architecture is shown in Fig. 4.7(b). The injection signal traverses through this architecture in a meandering form. Hence, the architecture has been named the *meander-line* architecture.

With respect to layout for LO distribution, the architecture only needs the length of each section of the meander-line and the drive strength of the LO buffers to be matched across channels. Further, the power of the external injection signal need not be matched to the LO buffer output power. This is because the first ILO output acts as a reference and all the subsequent ILOs are driven by the previous ILO's buffer. When operating in interference-rich environments, radars need to be able to create



(a) Cascade Phase Control

(b) Meander-line Architecture

Figure 4.7: Meander-line architecture derived from the cascade phase control scheme

nulls in desired directions. This requires non-uniform phase-patterns (unlike the pattern shown in Figs. 4.6(a) and 4.7(a)). Generating such patterns becomes more arduous in the meander-line architecture, because phase of each element gets added to the next element.

The most important advantage of an ILO versus other phase-shifting techniques is that it requires lower power to operate at RF and mm-wave frequencies. In fact, ILOs can be designed at frequencies close to the f_T of the CMOS process. This is because ILOs are regenerative blocks. ILOs are also more robust to mismatch because their operation depends on physically large components like inductors and capacitors. Further, most of the previous techniques discussed in the Chapter 2, only allow fixed phase-shifts. However, in an ILO, the phase-shifting can be made continuous by the use of varactors for frequency tuning, thereby allowing the beam to be seamlessly steered.

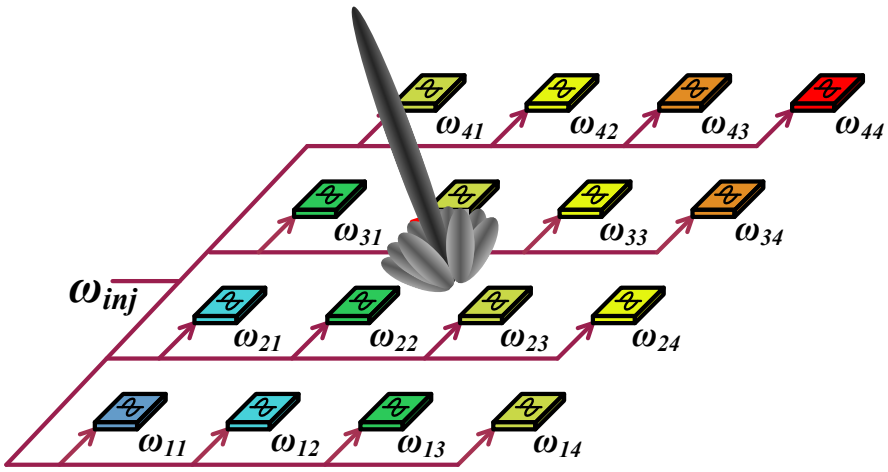


Figure 4.8: Fully-flexible architecture extended to 2D phased-array

4.3 Extensions of Proposed Architectures

4.3.1 To 2D Phased Arrays

Most phased-array radars are designed as a two-dimensional matrix, as illustrated in Fig. 2.16(b). The phase generation matrix $\boldsymbol{\Theta}$ corresponding to the 2D array is

$$\boldsymbol{\Theta} = \begin{pmatrix} \vdots & \vdots & \vdots & \iddots \\ \boldsymbol{\alpha + 2\beta_y} & \boldsymbol{\alpha + 2\beta_y + \beta_x} & \boldsymbol{\alpha + 2\beta_y + 2\beta_x} & \dots \\ \boldsymbol{\alpha + \beta_y} & \boldsymbol{\alpha + \beta_y + \beta_x} & \boldsymbol{\alpha + \beta_y + 2\beta_x} & \dots \\ \boldsymbol{\alpha} & \boldsymbol{\alpha + \beta_x} & \boldsymbol{\alpha + 2\beta_x} & \dots \end{pmatrix}$$

where $\boldsymbol{\alpha}$ is the constant part of phase-shift caused in every phase-generation block, and $\boldsymbol{\beta_x}$ and $\boldsymbol{\beta_y}$ are the horizontal and vertical polarization phase shifts.

In the fully-flexible architecture, the LO is distributed symmetrically to all the channels. So the same concept can be applied to a 2D array. The individual channel frequency for the (i, j)-th element in the array (Fig. 4.8) can be computed as

$$\omega_{ij} = \omega_{inj} - \omega_L \sin(\alpha + i\beta_x + j\beta_y) \tag{4.7}$$

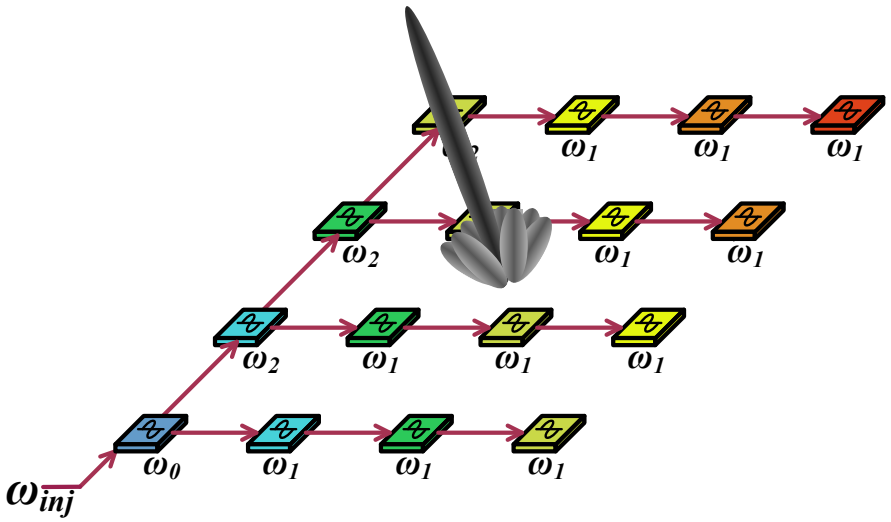


Figure 4.9: One possible configuration for 2D meander-line architecture

The fully-flexible architecture for a 2D array also suffers from similar drawbacks as its linear array equivalent - extensive symmetric LO routing, and LUT requirement for each channel phase shift. These drawbacks are partially alleviated by the meander-line architecture. The cascaded ILO scheme in the meander-line architecture can be extended to a 2D array as shown in Fig. 4.9. In fact, an alternative configuration illustrated in Fig. 4.10 also provides the same phase-pattern. Only two frequencies need to be defined to setup the 2D progressive phase-pattern - $\boldsymbol{\omega_1}$ and $\boldsymbol{\omega_2}$ - as illustrated in the two figures.

$$\boldsymbol{\omega_1 = \omega_{inj} - \omega_L \sin \beta_x} \qquad \boldsymbol{\omega_2 = \omega_{inj} - \omega_L \sin \beta_y} \tag{4.8}$$

Both configurations are similar in terms of layout complexity and frequency tuning requirements. Similar to the meander line architecture for a linear array, the resonant frequency tuning and the external injection signal strength for the first element (1,1) do not affect the array performance.

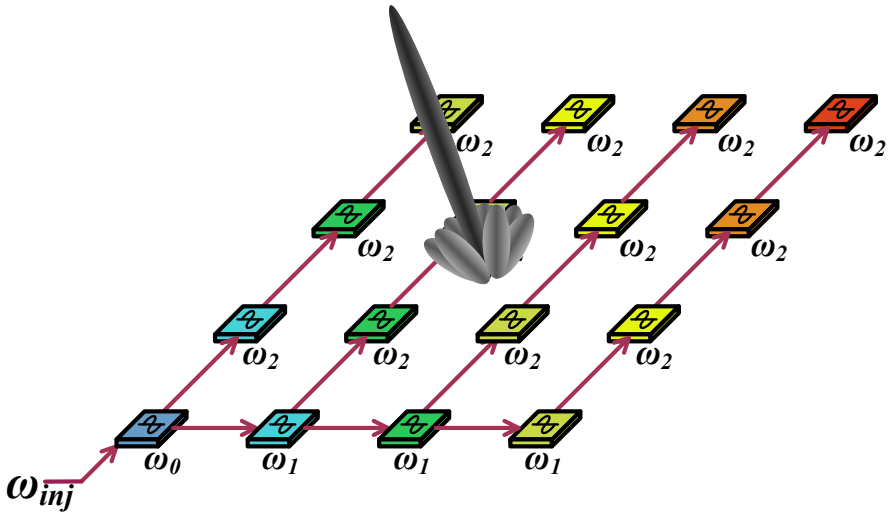


Figure 4.10: Alternative configuration for 2D meander-line architecture

4.3.2 Beamforming using the QILO

Many of the modern radio architectures require quadrature LO signals to support complex signal processing. Quadrature LO signals are also used in image-rejection receiver architectures [72]. The two phase-generation schemes discussed in this chapter do not provide quadrature LO outputs. However, from the mathematical analysis of quadrature injection-locked LC-oscillators (QILO), described in Chapter 3, the proposed architectures can be extended to QILOs, to generate quadrature phase-shifted outputs. Only few previous designs [25, 29, 47] presented have directly generated phase-shifted quadrature output signals. For a QILO, the quadrature outputs are phase-shifted with respect to their incoming signals by ϕ_{ss} similar to an ILO.

$$\phi_{ss} = \sin^{-1}\left(\frac{\omega_{QVCO} - \omega_{inj}}{\omega_L}\right) \tag{4.9}$$

By varying the ω_{QVCO}, which in turn varies linearly with ω_0, different phase-shifts can be produced and similar to the proposed architectures, the entire phase range of $-180°$ to $+180°$ can be achieved. It should be noted that the QILO requires quadrature input

signals if the injection is at fundamental frequency. The QILO phase-shifts the injection signal pair and corrects any quadrature error between them. However, if the injection frequency is at the second harmonic, the injection signals can be differential [56].

4.4 Summary

The aim of this chapter was to present techniques based on injection-locking to be applied for phase-generation. First, we have discussed previous work related to the application of ILOs in phased-arrays. The advantages and their drawbacks are highlighted. Due to the acute requirements of these designs, they are not well-suited for implementation in CMOS/BiCMOS technologies. Then, we present our proposed architectures - fully-flexible and meander-line - which overcome many of the drawbacks of previous state-of-the-art and can be integrated in silicon. Finally, we propose extensions of these architectures to 2D phased-arrays and quadrature generation.

Chapter 5

Dual-Mode Phased-Array Receiver

Two different architectures for phased-arrays based on ILOs were presented in the last chapter. In this chapter, we discuss the silicon implementation of the two architectures. In addition, the two architectures have been integrated into a unique dual-mode architecture. The 2.4GHz four-channel receiver prototype was designed and fabricated in a 0.13-μm CMOS process [23]. In the next two sections, we present the architecture and the circuit design which are followed by measurement results from a prototype IC.

5.1 Dual-Mode Architecture

A dual-mode architecture comprising of both - fully-flexible and meander-line, gives rise to a more versatile architecture. It supports the generic phase-patterns (arithmetic progression of phase) as well as arbitrary phase-patterns (nulls and peak in arbitrarily chosen directions) required in military radars. The difference between the two architectures lies in the source of the injection-signal. The dual-mode architecture can be

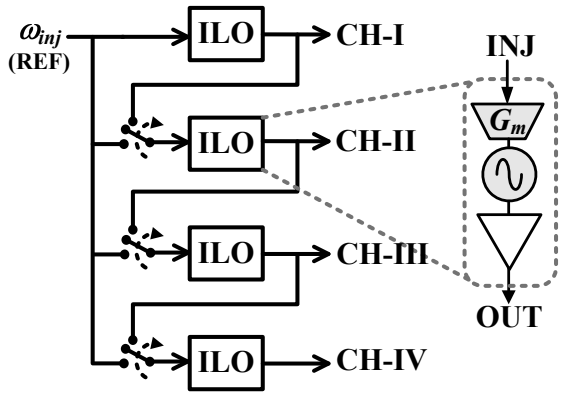


Figure 5.1: Phase-generation block of the dual-mode architecture

realized by using a scheme that allows the system to switch the injection source for all of the channels of a phased-array, as is illustrated in Fig. 5.1. In this scheme, the injection signal paths are symmetric for the meander-line architecure. However, for the fully-flexible architecture, a dummy always-ON switch needs to be placed in the injection path of the first ILO to ensure the symmetric injection signal strength.

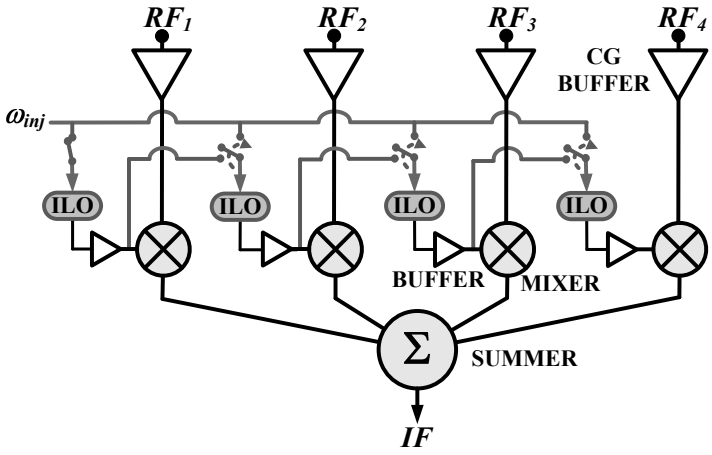


Figure 5.2: Dual-mode architecture implemented in a 0.13-μm CMOS

The complete system architecture is shown in Fig. 5.2 which depicts a four-channel phased-array receiver. Each channel consists of an RF input impedance matching buffer,

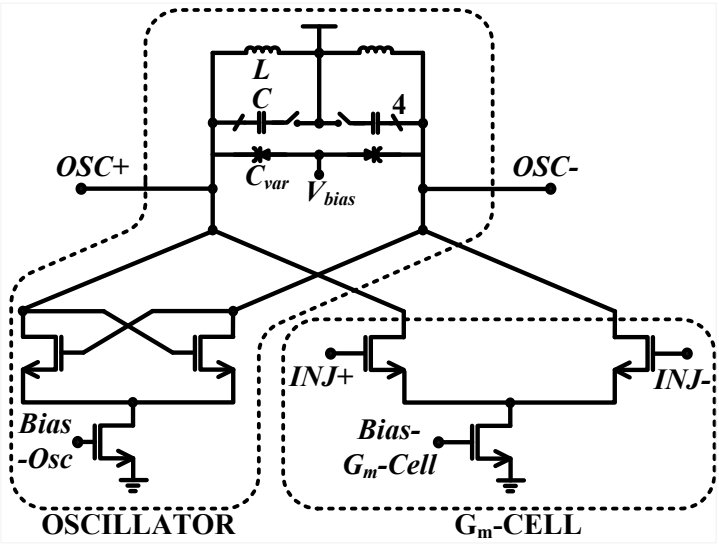


Figure 5.3: Circuit diagram for the ILO

a double-balanced mixer, an ILO acting as the phase-shifter and a CML buffer. A common signal summation circuit adds all the phase-aligned IF signals and drives the outputs off-chip. A digital register section is used for storing digital bits for each individual oscillator tuning, signal flipping (additional 180°) and architecture switch (fully-flexible or meander-line).

5.2 Circuit Considerations

5.2.1 ILO Design

The ILO is the most critical block as it functions as an amplifier as well as the phase generator. From the design point of view, the resonator needs to have a wide tuning-range, in order to combat process variations. The ILO should also exhibit a large lock-range ($\boldsymbol{\omega_L}$), so that any deviations or errors in $\boldsymbol{\omega_0}$ from its ideal value results in a minimal phase error.

The ILO schematic is shown in Fig. 5.3. It consists of a VCO-DCO hybrid, which

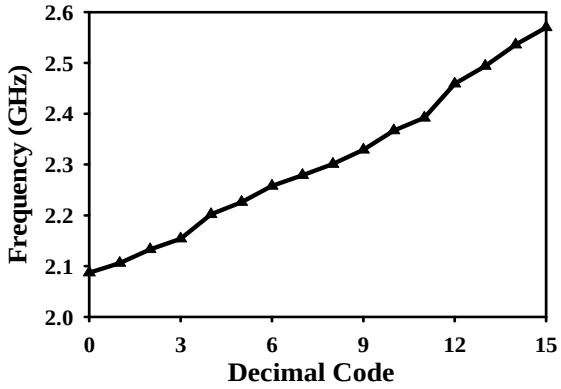


Figure 5.4: Simulated tuning range with coarse (digital control)

features 4-bit digital switched capacitor control and a single-varactor analog control. The digital control is used for coarse tuning of the resonant frequency. A set of four binary weighted capacitors are used for this purpose. Analog MOS varactor control is used for fine tuning. The simulated frequency tuning range obtained from the coarse control alone is plotted in Fig. 5.3. Using the varactor control increases the frequency range and the tuning range improves to 2.03-2.7 GHz.

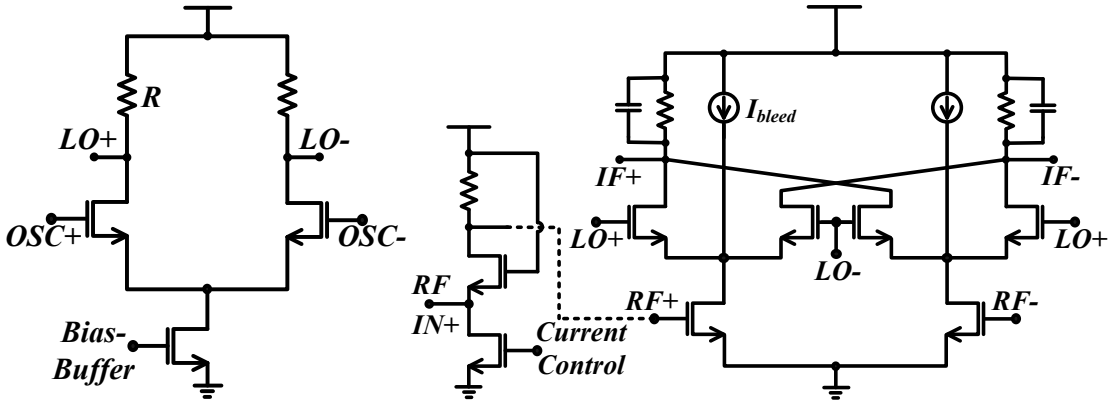
In order to ensure the validity of Adler's theory [50], the ratio of $\boldsymbol{I_{inj}/I_{osc}}$ was chosen to be approximately 0.38. According to the lock-range expressed by Paciorek [62]

$$\omega_L = \left(\frac{\omega_0}{2Q}\right) \frac{\frac{I_{inj}}{I_{osc}}}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} = \left(\frac{\omega_0}{2Q}\right) \times 0.4108 \approx \left(\frac{\omega_0}{2Q}\right)\left(\frac{I_{inj}}{I_{osc}}\right)$$

the difference between the large-signal and small-signal injection approximation is about 8%. Since this is a deterministic error, it is calibrated out during the measurement phase.

5.2.2 CML Buffer, Mixer and Summer

The ILO buffers the injected signal, which has a sinusoidal output. The mixer gain improves marginally when the sinusoid input at the LO port is replaced by a square-wave input. So a current-mode logic (CML) buffer is introduced after the ILO. The



(a) CML Buffer (b) Gilbert-cell mixer with g_m enhancement

Figure 5.5: Schematics for phase-shifted LO generation

CML circuit schematic is shown in Fig. 5.5(a) The buffer also drives the subsequent ILOs in the meander-line architecture and shields the driving ILO(s) from any reverse leakage effects.

The down-conversion mixer is implemented as a standard double-balanced Gilbert-cell mixer (Fig. 5.5(b)). In order to obtain more transconductance, extra DC current ($\boldsymbol{I_{bleed}}$) is introduced to the RF-input transistors. The mixer provides a gain of +12 dB. The mixer load is designed for a low-pass response with a bandwidth of 20 MHz. The external RF input is matched to 50-$\boldsymbol{\Omega}$ impedance by a common-gate buffer. The impedance of the input node is matched by tuning the current of the input transistor. Such a impedance-matching buffer is also used in the injection-signal path.

The four-channel summer, depicted in Fig. 5.6, combines the IF signals. The IF signals are converted to currents by a differential pair. The resistive load combines the currents from the four differential pairs and produces an output voltage signal. Any phase-shift introduced in the $\boldsymbol{V}$-to-$\boldsymbol{I}$-to-$\boldsymbol{V}$ conversion process is common to all the channels and does not affect the combining process.

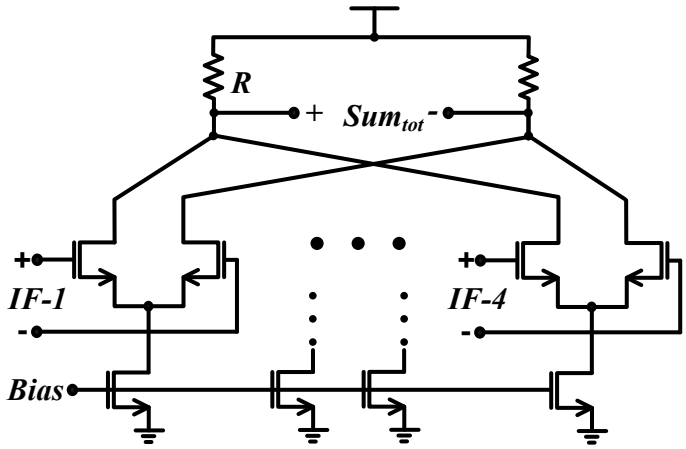


Figure 5.6: Four-channel summer

5.3 Measurement Results

The dual-mode receiver was fabricated in UMC's 0.13-μm CMOS process. The four-channel receiver core draws only 42mW of power (10.5mW/channel) from a 1.55V power supply and occupies 1.2-mm $\times$ 1.2-mm of active area. This is the lowest power phased-array receiver reported in recent literature by approximately 50%. The use of differential inductors can further improve the performance, and reduce the active area of the receiver.

The prototype die is packaged into a quad-flat no-lead (QFN) package, in order to ensure good RF performance (low lead inductance and capacitance). Due to pin limitation in the IC, individual oscillator outputs are not driven out of the chip. Hence, the oscillator frequency is measured from the leakage signal on the corresponding RF channel. Each oscillator has a continuous tuning range between 1.9-2.8GHz with the help of a switched capacitor array and a varactor. The excellent matching between channels in the digital frequency-tuning characteristics is depicted in Fig. 5.7. The middle region shows a smaller frequency step than others. This is probably due to the binary layout of the capacitor bank, which can cause mismatch. By using thermometer

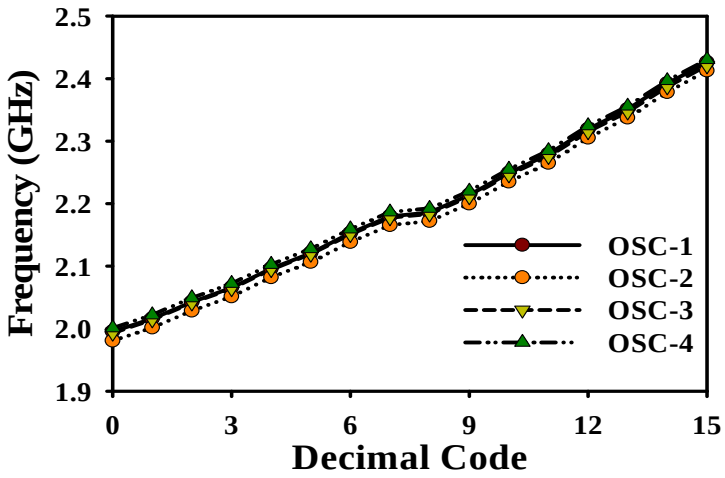
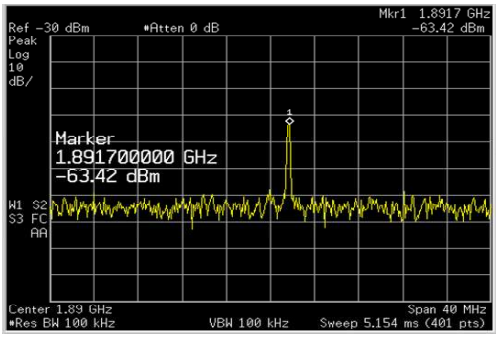
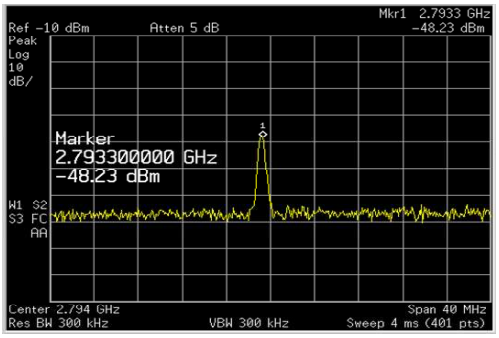


Figure 5.7: Measured free-running digital tuning range for oscillators in the four channels

coding, we can reduce the capacitor bank mismatch. The maximum frequency difference between any two oscillators is only 20MHz (less than 1% mismatch). Further, three different ICs are measured and the worst-case mismatch in frequency seen across all three dies is about 52 MHz (approximately 2% mismatch). With minimal calibration via varactor tuning, the slight mismatch in the oscillator frequencies can be eliminated. Fig. 5.8 shows the minimum and maximum frequencies achievable through varactor tuning, measured on a spectrum analyzer.



(a) Minimum frequency



(b) Maximum frequency

Figure 5.8: Minimum and maximum oscillator frequencies obtaining by varactor tuning

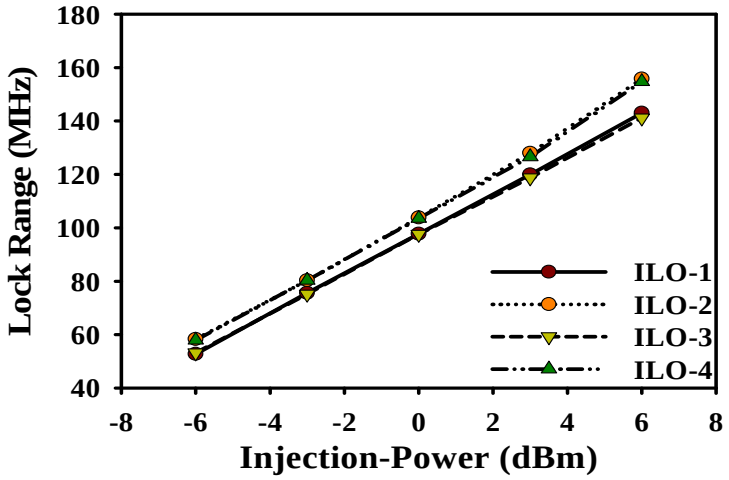


Figure 5.9: Measured lock-range of ILOs in the four channels for $\omega_0 \approx 2.4$GHz

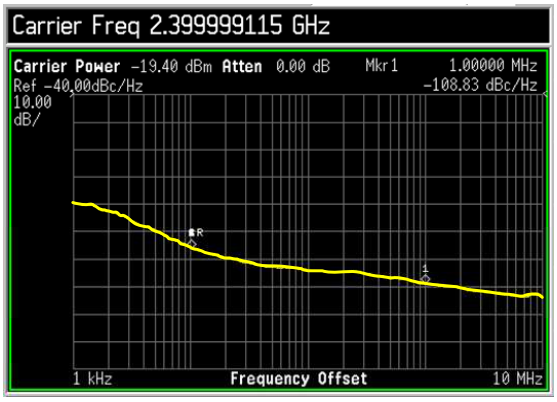


Figure 5.10: Phase noise of the ILO locked at 2.4GHz

Next, the ILO lock-range is characterized for all the four channels. Fig. 5.9 plots the measured results. The worst-case mismatch in the lock-range is about 20MHz. Since the free-running frequencies exhibit less than 1% mismatch, it implies that this lock-range difference is a result of mismatch in the G_m cells injecting current into the oscillator. For phase noise measurement, the LO signal leakage from the RF port is amplified using an external power amplifier. The phase noise of the ILO locked to 2.4GHz, measured on a spectrum analyzer, is plotted in Fig. 5.10. At 1MHz offset from the carrier frequency,

the phase noise is approximately −109dBc/Hz. The measured gain of the mixer and summer is approximately 11.5dB, after de-embedding the cable losses and balun transfer ratios. The RF input of each mixer and the injection port is matched to 50Ω using a common-gate buffer. The input matching characteristics (S_{11}) for one of the channels and the injection port are shown in Fig. 5.11.

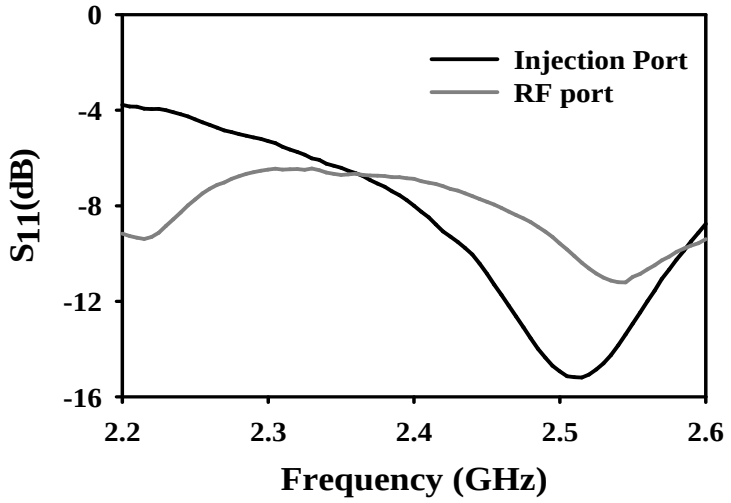


Figure 5.11: Measured input matching measured around 2.4GHz

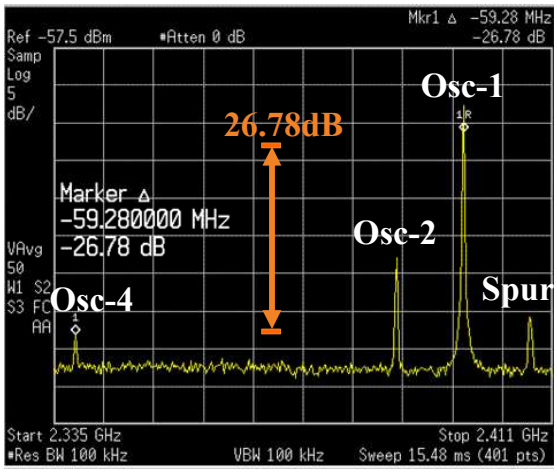


Figure 5.12: Measured on-chip channel-to-channel isolation

Although no specific isolation structures were used to separate the four-channels, on-chip isolation is observed to be better than 26dB. In order to estimate it, all four oscillators are turned ON and set to different frequencies around 2.4GHz. Fig. 5.12 plots the measured signal on RF channel-1 from a spectrum analyzer. As depicted, the oscillator in channel-1 exhibits the strongest leakage. However, since the channel-1 transmission line on PCB is very close that of channel-2, without any ground isolation between them, the LO leakage from channel-2 also leaks into channel-1 and pulls its oscillator, thereby creating the spur illustrated in Fig. 5.12. The true channel-to-channel worst-case isolation is between channels 1 and 4 and is measured at 26.78dB. Leakage from channel-3, which is farthest from channel-1 is below the noise floor. Of the four RF receiver channels designed, one of the channels showed less than the required individual gain and has not been included in our results. Investigation of this issue revealed that this gain reduction can be attributed to the mixer and summer connection for channel-4. The other three channels show individual gains which are $\pm$1dB of each other. The maximum total measured gain of the three-channel receiver is approximately 20dB. The received signal improvement due to the three channel phased array architecture is measured to be about 8.5dB, which is close to the ideal value of 9.5dB.

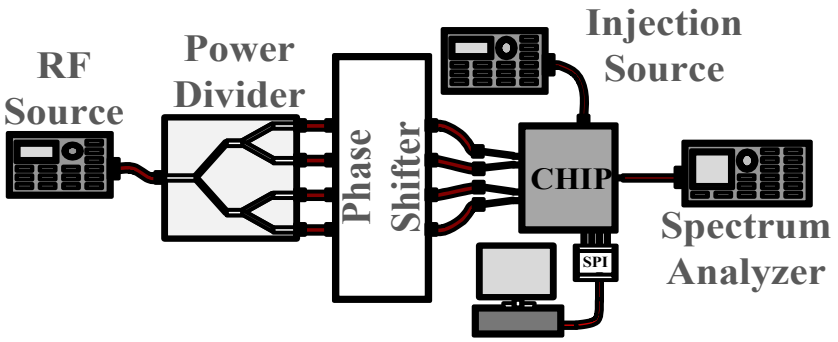


Figure 5.13: Experimental setup for radiation pattern measurement

To measure the array radiation pattern, the effect of a receiver antenna array feed

Table 5.1: Summary of measurement results

Receiver Performance		
Receiver Gain	2-channel	17dB
	3-channel	20dB
Signal Improvement	2-channel	6dB
	3-channel	8.5dB
RF Frequency		2.4GHz
IF Frequency		8MHz
IF Amplitude Mismatch		±1dB
Suppression in Nulls		16-25dB
Power Dissipation		
LO Core		2.67mW (×4)
LO Buffer + G_m-cell		4.26mW (×4)
Downconversion mixer		2.56mW (×4)
Summer		4.15mW
Total Power) w/o bias & 50Ω matching circuits)		**42.11mW 10.5mW/channel**

network is mimicked using RF phase-shifters and a 1:4 Wilkinson power divider. The experimental setup used is depicted in Fig. 5.13. The RF phase-shifters and power divider have been implemented using microstrip transmission lines of FR4 substrate. The IF frequency is set at 8MHz. Table 5.1 summarizes the measurement results from the chip and Fig. 5.14 shows the die micrograph. Fig. 5.15 illustrates the measured and theoretical two-channel and three-channel radiation patterns for both the architectures. The synthesized beams are in excellent agreement with theoretical predictions. The signal rejection achieved in the null directions varies from 16dB to 25dB. The variation is more for the fully-flexible architecture, which is probably due to the mismatch in the individual ILO conditions, resulting in higher amplitude mismatch. The antenna spacing for all these cases is assumed to be half the wavelength corresponding to the RF frequency.

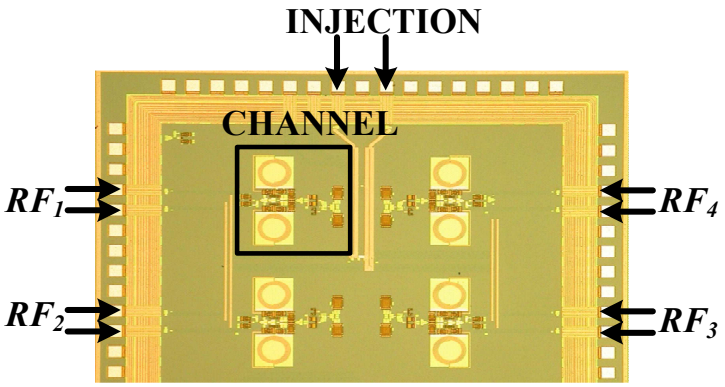
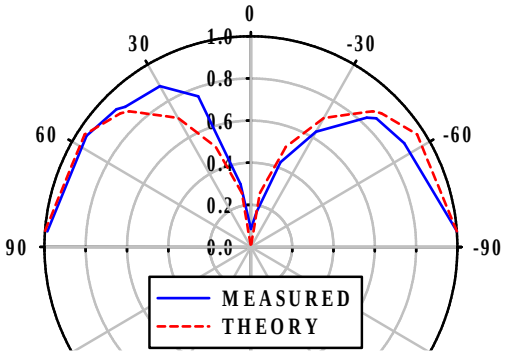


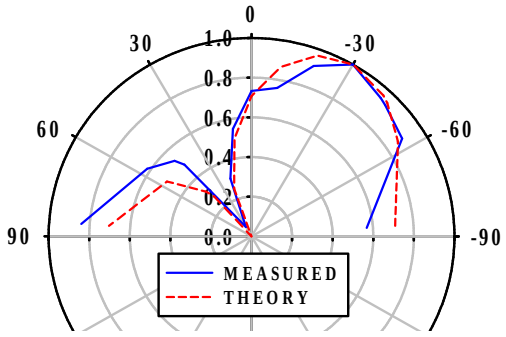
Figure 5.14: Micrograph of receiver IC

5.4 Summary

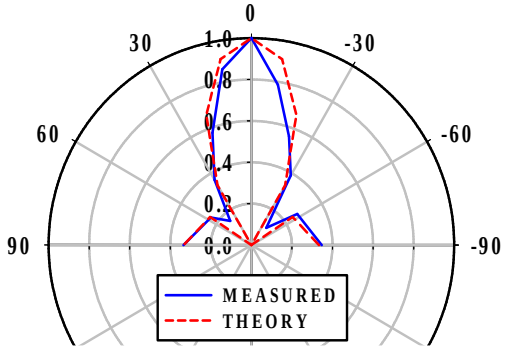
In this chapter, we introduced a dual-mode architecture for a phased-array receiver. The architecture integrated the fully-flexible and the meander-line architectures into the two modes of operation. The phase-generation schemes can be extended to the case of a transmitter. The architecture used injection-locking in both modes to generate phase-shifts and hence was able to operate at low power. The active area of the receiver is comparable to previous state-of-the-art. At the same time, it should be noted that using differential inductors in the ILO could further reduce the active area, as is proven in our next effort. The power consumption of the receiver is lower than previous state-of-the-art by approximately 2X. The architecture poses no constraint in terms of expansion to large arrays for radar applications or extension to mm-wave frequencies. The measured beamforming by the receiver closely matches theoretical predictions and proves the operation and feasibility of the design.



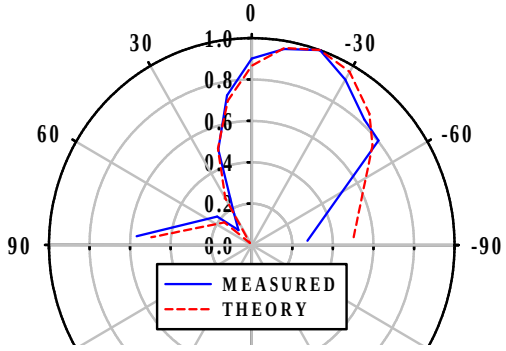
(a) 2-channel beam at 90° (Fully-flexible)



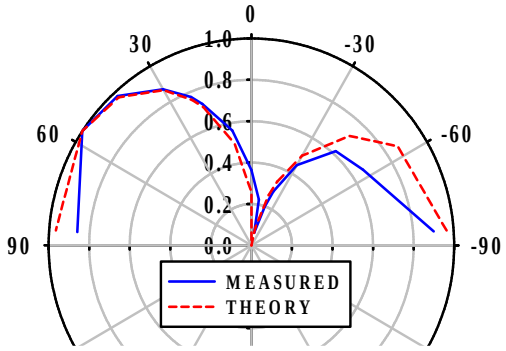
(b) 2-channel beam at −30° (Fully-flexible)



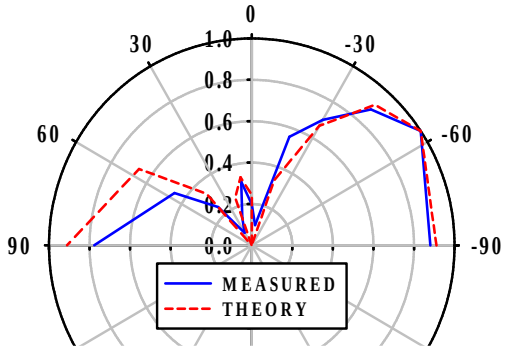
(c) 3-channel beam at 0° (Fully-flexible)



(d) 2-channel beam at −20° (Meander-line)



(e) 2-channel beam at 60° (Meander-line)



(f) 3-channel beam at −60° (Meander-line)

Figure 5.15: Synthesized radiation patterns for two architectures

Chapter 6

24GHz Phased-Array Receiver Prototype

The concept of using injection-locking in an LO-phase-shifting architecture in silicon was presented in the last chapter. Next, we aim to prove that ILOs can be used as low-power phase-shifters at mm-wave frequencies. We present a 24GHz phased-array receiver front-end, which uses the ILO for multiple purposes - phase-shifting, buffering and frequency tripling. The next section describes the two-channel receiver architecture. Section 6.2 explains multi-functionality aspect of the ILOs in the receiver. Sections 6.3 discusses the design of the various circuit blocks. Measurement results from a CMOS prototype, fabricated in a 0.13-μm BiCMOS process, are presented in Section 6.4.

6.1 Receiver Architecture

The fully-flexible architecture has been adopted in the designed receiver. The basic block diagram of the receiver is shown in Fig. 6.1. Each channel of the receiver consists

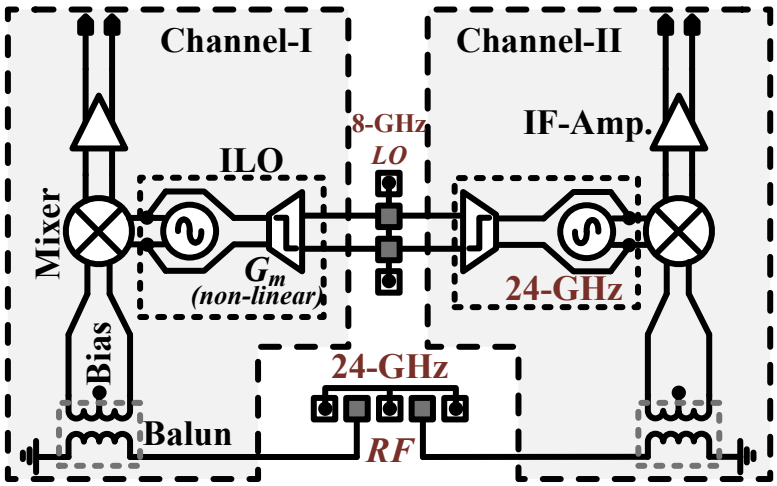


Figure 6.1: Proposed phased-array receiver

of a balun to convert the single-ended RF input to differential outputs, a downconversion mixer, an IF amplifier and the ILO. The RF signals are applied into the IC through probe-pads. The ILO operates as a phase-shifter as well as a frequency tripler. Consequently, the LO signal injected into the IC is at 8GHz.

6.2 Multi-functional ILO

The performance of the ILO as a phase-shifter has been proposed and proven in the last two chapters. In this work, we first extend the ILO design to mm-wave frequency. In order to achieve lock, the injection-signal to an ILO only needs to possess a frequency component that is within the ILO lock-range. All other components are suppressed by the LC-tank characteristics [56]. For example, a square-wave may be used to lock an ILO to any odd-harmonic of the square wave as illustrated in Fig. 6.2. This is called sub-harmonic injection-locking.

In a transceiver, frequency synthesis and LO distribution consume a significant amount of power [73]. Especially, in the LO-phase-shifting or baseband/IF phase-shifting architecture, the LO needs to be distributed to all the channels and can be

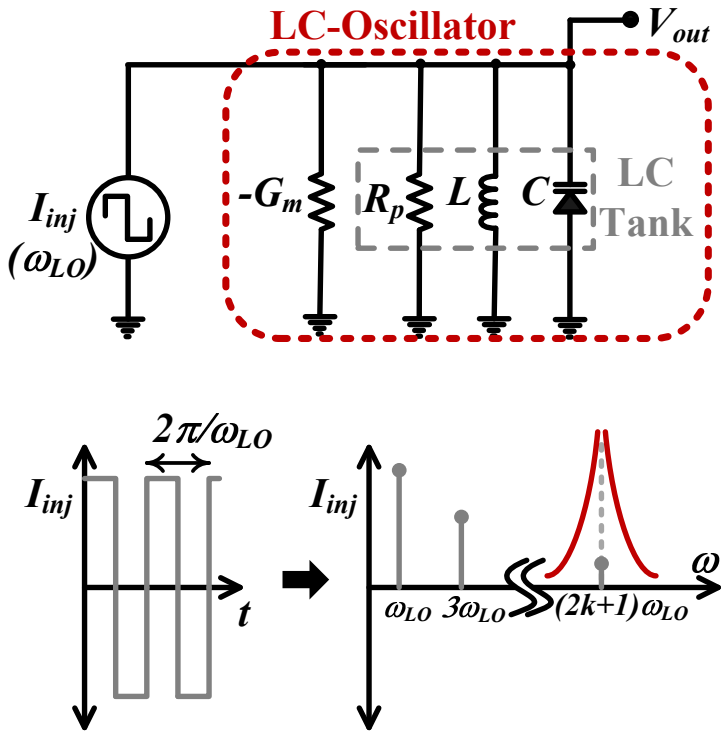


Figure 6.2: Sub-harmonically injection-locked oscillator ($(\boldsymbol{2k+1})\boldsymbol{\omega_{LO}} \approx \boldsymbol{1/\sqrt{LC}}$)

expensive in terms of power, at mm-wave frequencies. The exponential increase in signal losses with frequency [74] has to be compensated with additional buffers. By applying sub-harmonic injection-locking, this power consumption can be greatly reduced [75, 76]. Firstly, the LO-distribution is done at a sub-harmonic frequency and hence, it reduces signal losses. Secondly, with a reduced divider ratio and potential removal of some divider stages, the overall power of the frequency synthesizer (PLL) reduces. In general, a large portion of the PLL power is spent on the initial stages of the dividers. Essentially, the ILO would perform three important functions - frequency multiplication, phase-shifter and signal buffering. All three functions are done utilizing the highly power efficient positive feedback inherent in an LC-based ILO. This multi-functionality allows the receiver to operate at lower power making phased-arrays a viable option for

portable systems.

Sub-harmonic injection-locking reduces the power spent on LO distribution, by reducing the LO frequency. However, there are a number of other system tradeoffs that also need to be considered. Sub-harmonic injection-locking results in the leakage of unwanted harmonics at the ILO output. There is a trade-off between the choice of the sub-harmonic and spurious tones. A lower sub-harmonic ($\boldsymbol{\omega_{ILO}/\omega_{LO}}$) value results in lower number of spurs close to $\boldsymbol{\omega_{ILO}}$ and larger lock-range, but creates a larger leakage tone at $\boldsymbol{\omega_{LO}}$ and increases LO generation and distribution power, and vice-versa. Though these unwanted harmonics are suppressed by the oscillator tank, they can reduce the SNR at the mixer outputs, by noise folding back to the baseband. In order to further mitigate this problem, techniques like pulse-slimming and narrow-band filtering can be utilized [56].

In addition, PLLs operating at mm-wave require a high-division ratio, due to limited crystal frequencies. And, the VCO in the PLL is phase-locked and tracked (updated) at the rate of the reference frequency. At other times, the VCO is effectively open-loop. Hence, by reducing the LO frequency, through sub-harmonic injection-locking, the VCO of the PLL (generating the LO frequency) is updated at a faster rate (relative to the LO frequency).

6.3 Circuit Design

In this section, we describe the various circuit blocks implemented as parts of the receiver. All the circuits are CMOS-only implementations.

6.3.1 ILO

The oscillator core of the ILO is realized as a negative-$\boldsymbol{g_m}$ LC-oscillator. The LC-tank resonant frequency is tuned by a hyper-abrupt junction diode-varactor to allow for linear

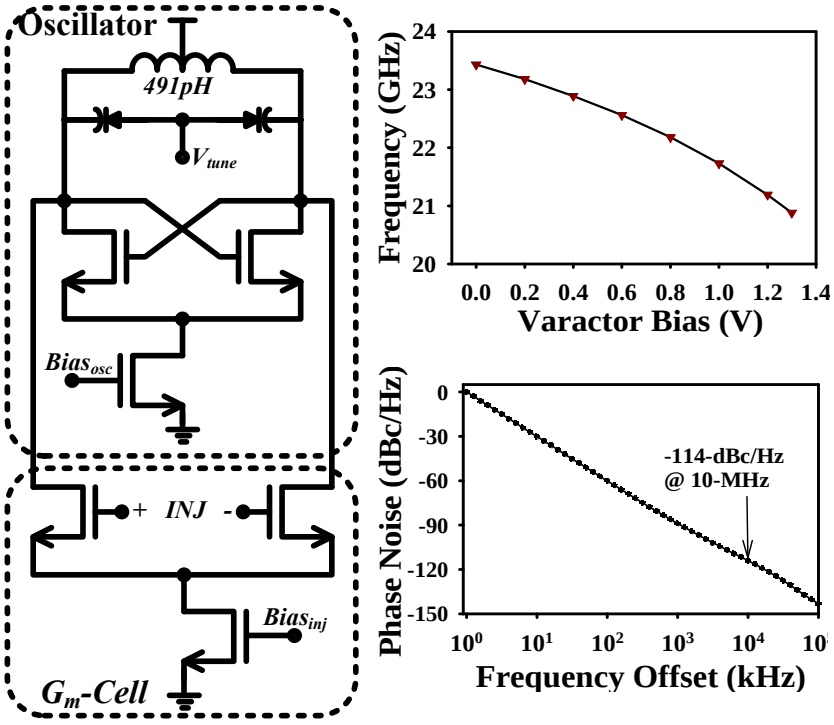


Figure 6.3: Schematic of the injection-locked oscillator and simulated results of oscillator under free-running conditions

tuning. The oscillator is designed for a tuning range between 20.9 and 23.4GHz. The simulated phase-noise at the highest frequency at a 10MHz offset was -114dBc/Hz.

The pMOS-nMOS cross-coupled pair gives the best phase noise performance and swing [77] in an LC-oscillator, but the parasitic capacitance in the output node is prohibitively large. And although pMOS-based cross-coupled transistors offer better flicker noise performance, their lower f_T results in higher power requirements. Under these considerations, the negative-g_m cell is chosen to be nMOS-only. The use of a symmetric octagonal inductor results in better phase noise performance and lower area.

An external G_m-cell is used to inject the required frequency into the oscillator. The differential pair is designed to completely swing the tail current from one arm to the other for a 0-dBm differential injection signal. This non-linearity of the G_m cell creates

odd harmonics of the injection frequency, out of which the oscillator is locked onto the third harmonic. And phase-shift is controlled through the varactor tuning voltage. Although not implemented in this design, digital control can be achieved either by controlling the tuning voltage through a high-resolution digital-to-analog converter, or through digitally-switched capacitor bank.

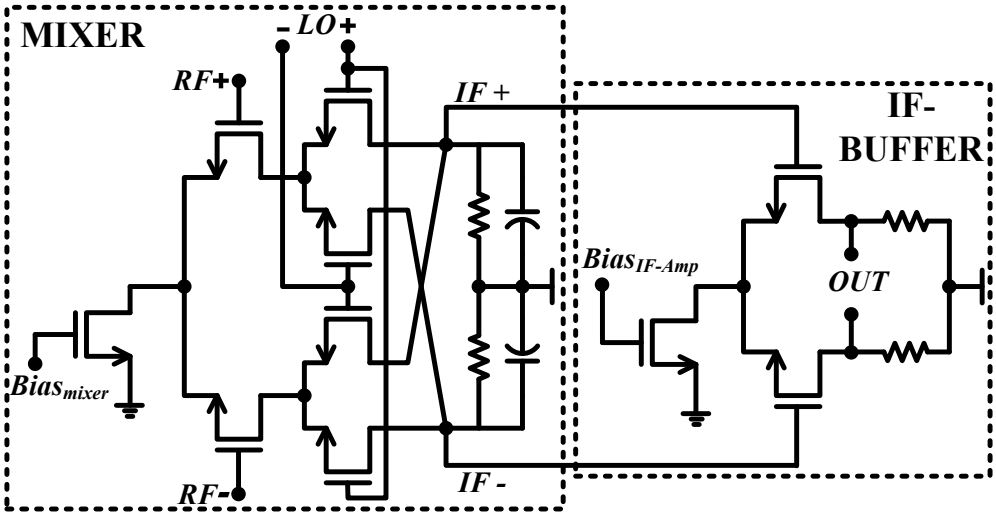


Figure 6.4: Mixer and IF buffer schematics

6.3.2 Mixer & IF Buffer

For the down-conversion mixer, the double-balanced Gilbert cell topology is chosen over the passive-mixer topology, because the passive-mixer requires a larger local oscillator signal for optimum performance. The output load of the mixer is designed for a bandwidth of 150-MHz. The mixer is preceded by a current-mode logic (CML) buffer at the LO-port. This buffer is used to convert the sinusoidal output from the ILO into an approximate square-wave signal, to improve the mixer gain. It also reduces any LO amplitude mismatch caused at the ILO output due to frequency tuning (for phase generation). Due to the RF-input transistors operating so close to their f_T (70-80GHz),

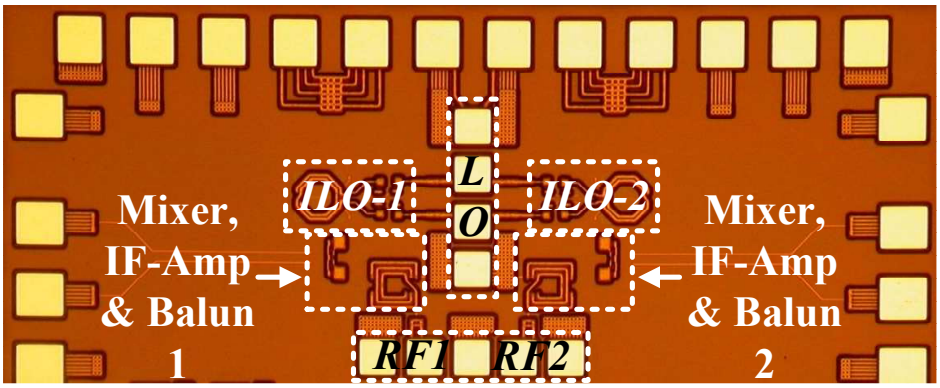


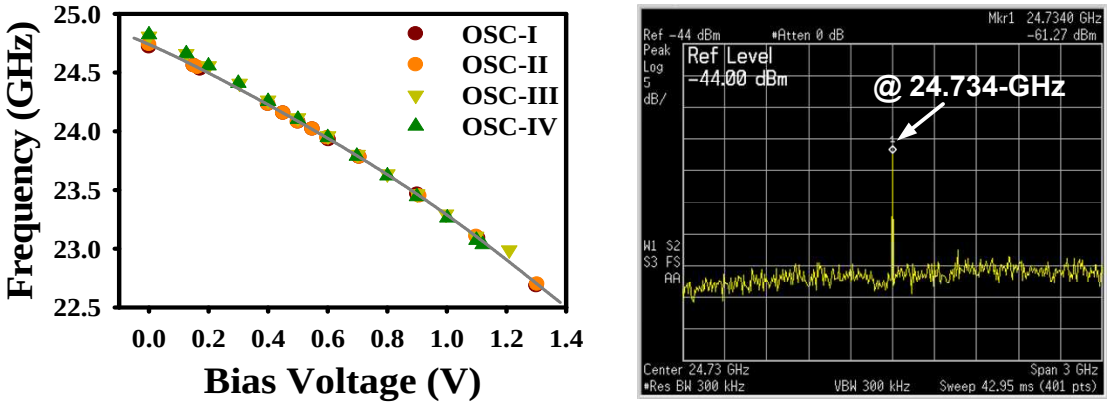
Figure 6.5: Die micrograph of the CMOS prototype fabricated in 130-nm SiGe BiCMOS technology

the overall mixer conversion gain is 2-dB. An IF buffer drives the output.

6.4 Measurement Results

The circuit is fabricated in the 0.13-μm SiGe IBM BiCMOS process, but the design is CMOS-only. The die micrograph of the prototype is shown in Fig. 6.5. The active area occupied (excluding pads and ESD structures) is 0.23sq. mm. The two-channel receiver draws 16mA of current from a 1.5V power supply, excluding biasing circuits. Each phase-shifter (ILO and CML buffer) consumes about 6mA.

Individual channels of a phased-array receiver need to have excellent matching, for optimum performance. In order to evaluate the matching performance, two prototypes are measured for free-running frequency tuning range. All four oscillators (two on each prototype) exhibit a tuning range between 22.7 and 24.74GHz. The frequencies for the oscillators are measured by looking at the carrier frequency leakage at the RF-port of the mixer. Fig. 6.6 shows the tuning range of the two oscillators and the highest frequency measured on the spectrum analyzer for one oscillator. The two oscillators show excellent matching with the worst case frequency mismatch of about 20MHz. In



(a) Frequency tuning

(b) Highest frequency (24.73GHz)

Figure 6.6: Measured oscillator free-running frequency characteristics

order to measure phase-noise, the oscillator signal is downconverted to an IF of 94MHz. One of the oscillators (Oscillator-I) free-running at 24GHz exhibits a phase noise of -106dBc/Hz at a 10MHz offset. The $\mathbf{1/f^2}$ nature of the free-running oscillator is clearly observed at higher frequency offsets in Fig. 6.7. The 8GHz microwave source exhibits a phase noise of -126dBc/Hz at a 10MHz offset. When one of the oscillators (Oscillator-I) is injection-locked to this signal, the measured phase noise of the downconverted signal is -116dBc/Hz at a 10MHz offset (Fig. 6.7), which matches well with the value predicted from the signal source phase noise (-126dBc/Hz + 9.5dB = -116.5dBc/Hz). Also, the in-band phase-noise behavior of the ILO closely follows the signal source (PLL behavior), albeit with a loop-bandwidth increment (Fig. 6.7).

The measurement setup is shown in Fig. 6.8. The rat-race hybrid converts the single-ended 8GHz signal from the microwave source into a pair of differential signals with approximately 1dB loss (apart from the usual 3dB due to power splitting). A mm-wave source is used to generate the RF input to the mixer. The signal is power-split into two - equal in phase and magnitude, which are fed to the two channels through

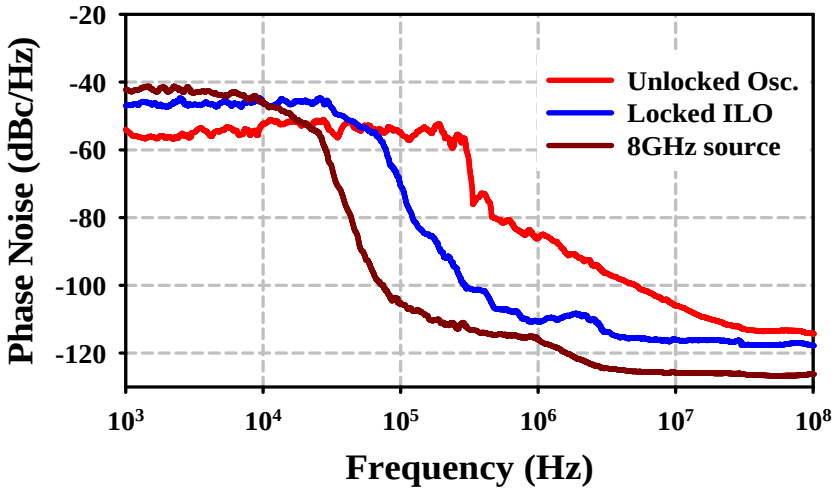


Figure 6.7: Phase-noise measured for the 8GHz signal source, unlocked oscillator and locked ILO

RF probes. The IF is measured on a digital storage oscilloscope (DSO) sampling at 5-GSa/s. For impedance matching before the RF balun on each channel, a 50$\boldsymbol{\Omega}$ resistance is connected between the RF input and ground. The measured $\boldsymbol{S_{11}}$ on a vector network analyzer is shown in Fig. 6.9.

As discussed earlier, tuning the natural frequency of the VCO in the ILO results in a phase-shift between the injected and output signal. However, this tuning needs to be done within the lock-range. Hence, lock-range estimation is an important step in the measurement and calibration of the system. The injection signal is strong enough to ensure complete switching of the tail current in the $\boldsymbol{G_m}$-cell (Fig. 6.3). Hence, the lock-range can be varied by changing the tail-current transistor bias of the $\boldsymbol{G_m}$-cell. The double-sided lock-range of the ILO is set to 242-MHz by setting the appropriate $\boldsymbol{G_m}$-cell tail bias ($\boldsymbol{(I_{inj}/I_{osc}) \approx 0.075}$ at 24.372-GHz). This lock-range is sufficient for the requisite phase-generation in our prototype. For more flexibility, this lock-range should be further enhanced. This can be done by applying a square wave to the $\boldsymbol{G_m}$-cell, instead of a sinusoid. Simulation results show that the lock range more than doubles

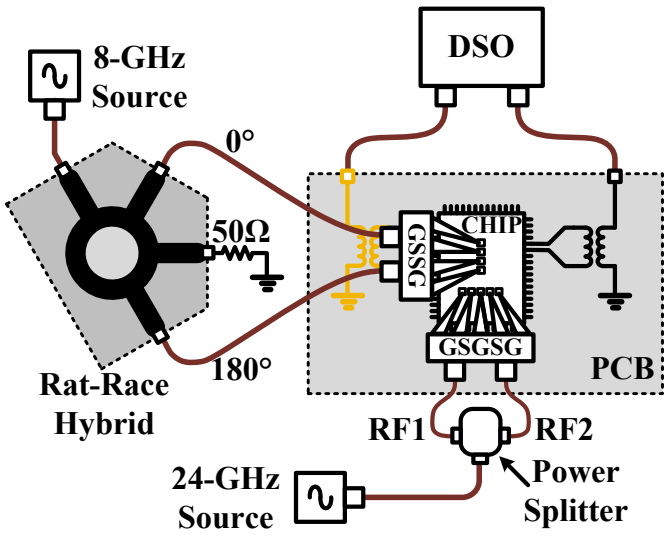


Figure 6.8: Measurement setup used to evaluate beamforming performance of the RX

using this modifications.

Traditionally, in a phased-array receiver, the phase-shifter cancels the phase-shift produced by the antenna-array. However, for simplicity of measurement, RF signals are aligned and the LO-phase-shifts are measured at the IF. Fig. 6.10 illustrates the various phase-shifts that are measured on the oscilloscope. The worst-case amplitude mismatch and phase error are approximately 1.5-dB and 4°, respectively. After de-embedding signal losses from cables and insertion losses from power-divider, balun and RF probes, the mixer-IF-buffer combination shows approximately 0-dB gain. The corresponding beam patterns are depicted in Fig. 6.11. Table 6.1 summarizes the measurement results from the chip.

The accuracy of the phase-shift in a phased-array dictates the quality of beam nulls in the radiation pattern. So for higher rejection from null directions, high phase-accuracy is essential. For each of the phase-shift waveforms, the ILO center frequency ($\boldsymbol{\omega_0}$) is tuned using the varactor bias. An external trim potentiometer ensures fine frequency resolution to achieve accurate phase-shifts. It should be mentioned that in a full-system

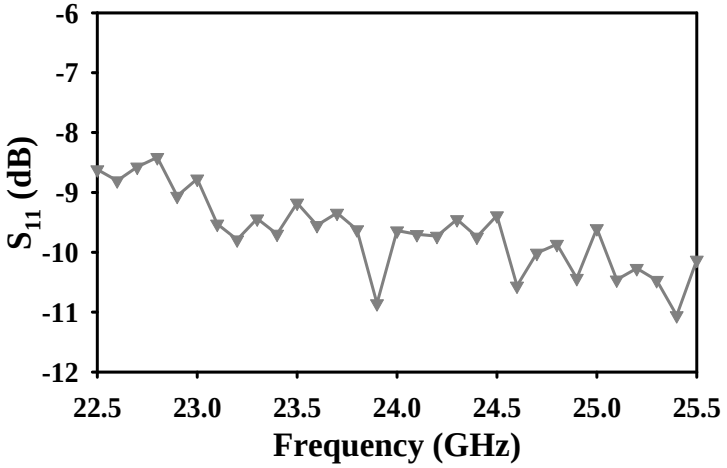
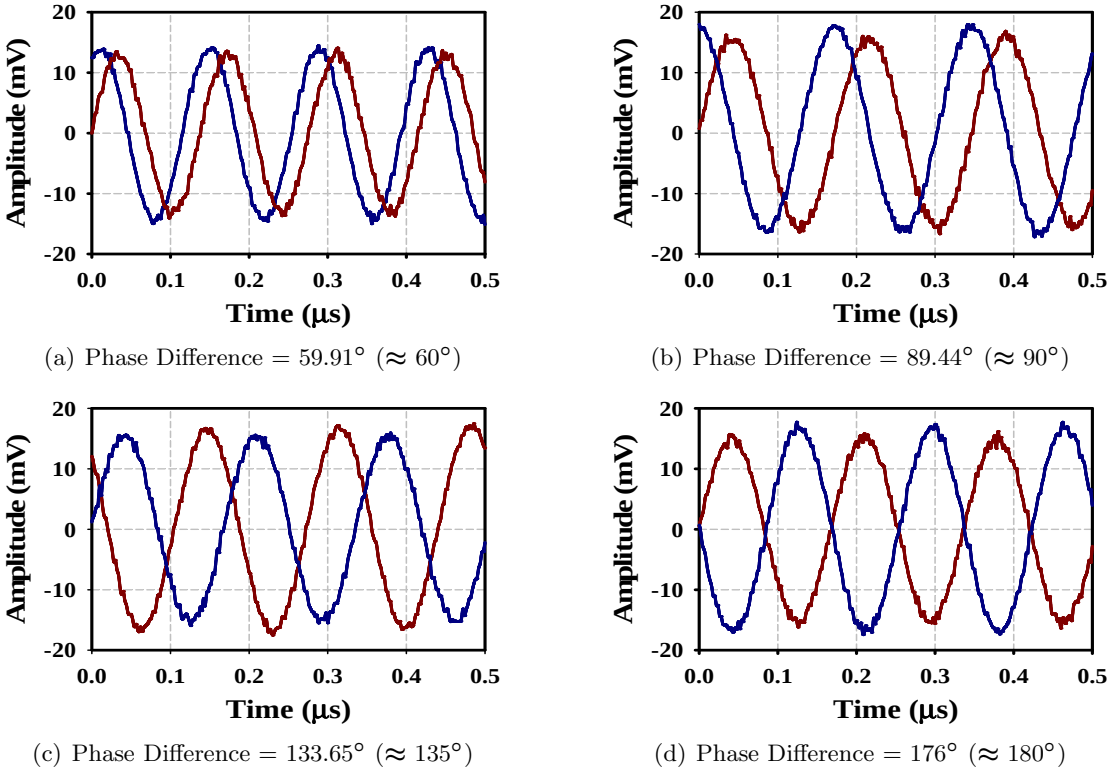


Figure 6.9: Impedance matching at one of the RF inputs measured on a network analyzer

implementation, a high-resolution digital-to-analog converter (DAC) can be used for varactor bias for accurate control of frequency (and consequently, phase), or a hybrid VCO-DCO [23] could be used, where digital bits are used for coarse control and DAC-controlled varactor bias *fine-tunes* the frequency.

6.5 Summary

This chapter presented a low-power 24GHz phased-array receiver architecture that is based on sub-harmonic injection-locking. It has proved that ILOs can operate at mm-wave frequencies as versatile phase-shifters. The ILO is the principal block in the receiver performs multiple functions, which has resulted in the low power consumption of the receiver. To the author's knowledge, the power consumption per channel (12mW) for this receiver is one of the lowest reported in recent literature. Also, the receiver occupied an active area of only 0.23sq. mm. The reduction in LO-frequency requirement for the receiver allowed for simpler LO distribution networks. The two channels of the receiver



(a) Phase Difference = 59.91° (≈ 60°)

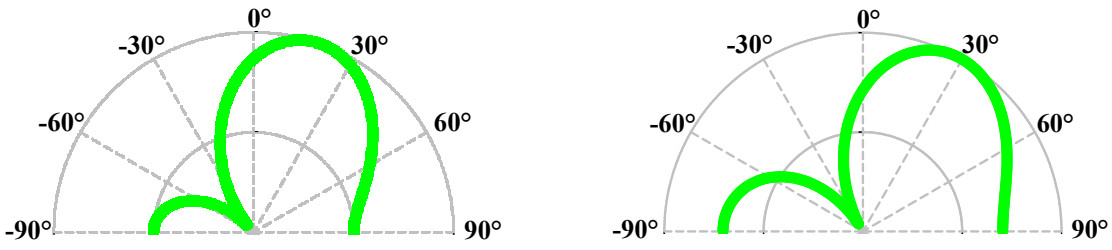
(b) Phase Difference = 89.44° (≈ 90°)

(c) Phase Difference = 133.65° (≈ 135°)

(d) Phase Difference = 176° (≈ 180°)

Figure 6.10: Different phase-shifts measured at IF outputs

exhibited a gain error of approximately 1.5dB with no calibration and a worst-case (best-case) phase error of 4° (0.1°), with minimal (manual) calibration. Finally, techniques to improve the flexibility of the phase-shifter were also discussed.



(a) $\theta \approx 20°$ (b) $\theta \approx 30°$

Figure 6.11: Radiation patterns, corresponding to phase-shifts of 60° and 90°

Table 6.1: Summary of measurement results

Receiver Performance	
RF Frequency	24GHz
Input LO Frequency	8GHz
IF Amplitude Mismatch	1.5dB (max.)
Suppression on Nulls	24-27dB
Phase Noise @10MHz offset	-117dBc/Hz
Power Dissipation	
LO Core + G_m-cell + CML Buffer	9mW ($\times 2$)
Mixer + IF Amplifier	3mW ($\times 2$)
Total Power (excluding bias)	24mW (12mW/ch.)

Chapter 7

Beam-forming using the Fast-Fourier Transform

Phase-generation techniques discussed in the previous chapters have limited the number of beams to one. In this chapter, we propose a technique to achieve multiple independently steerable beams from a single array. Section 7.1 discusses previous approaches to generating multiple beams from an antenna array. Section 7.2 proposes a new architecture to generate concurrent multiple independently steerable beams from a linear or 2D array, based on the fast Fourier transform (FFT) and Section 7.3 elaborates on a two-channel prototype receiver designed in a 65nm CMOS process and currently in fabrication.

7.1 Generating multiple beams in a phased-array

Multiple beams can be created in a linear or 2D phased-array by partitioning the array into sub-arrays. As portrayed in Fig. 7.1, an $\boldsymbol{M \cdot N}$-element array is split into $\boldsymbol{M}$ independent sub-arrays, each consisting of $\boldsymbol{N}$ antennas. The beam from each sub-array

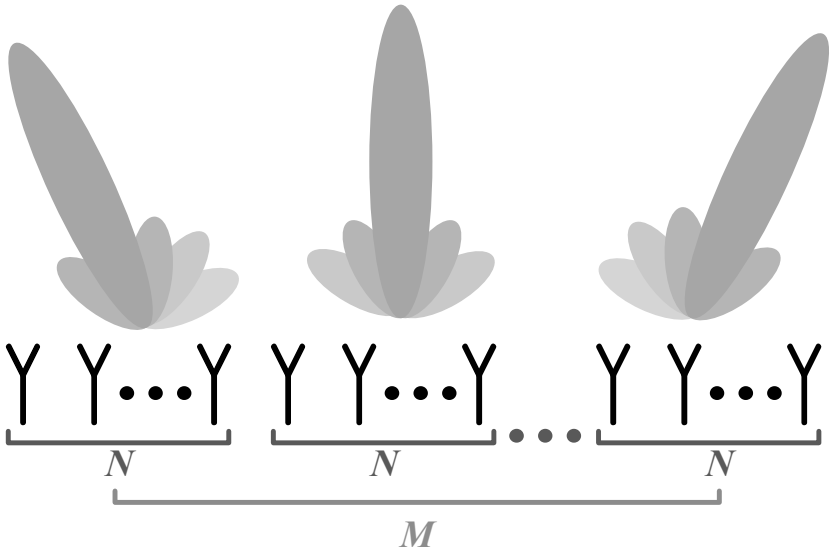


Figure 7.1: *Sub-arraying* to create multiple independently steerable beams

is concurrent (with beams from other sub-arrays) and can be independently steered. However, this reduces the effectiveness of beamforming, since the array gain per beam reduces.

One of the first attempts at creating multiple beams using a single antenna array in silicon was presented in [26]. However, the bi-directional approach fixes the angle of one beam with respect to the other, and hence, is not independently steerable. Another approach to creating multiple beams that is proposed in [22] allows for four concurrent independent beams at two widely spaced frequencies - a pair of beams per frequency. Each pair of beams consists of the vertical polarization and the horizontal polarization. A major disadvantage of this architecture is its scalability. To increase the number of independent beams, the number of widely spaced frequencies has to increase. This results in more number of components per frequency band and larger LO distribution networks, increasing the power consumption of the system.

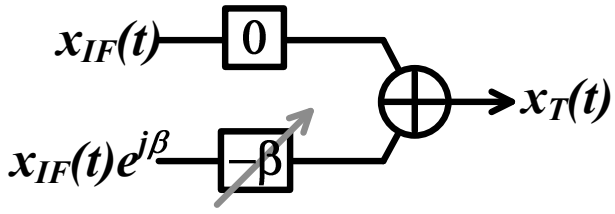


Figure 7.2: IF/baseband section of a two-channel receiver

7.2 Multiple beamforming using the FFT

In baseband/IF beamforming, the phase-shifting operation is done in the baseband/IF section. Consider a two-channel IF beamforming receiver, as illustrated in Fig. 7.2. Only the IF phase-shifting and signal combining components are depicted. Here $\boldsymbol{x_{IF}(t)}$ represents the complex IF signal of channel-1. If channel-2 signal is phase-shifted by $\boldsymbol{\beta}$, then the signal for channel-2 is $\boldsymbol{x_{IF}(t)e^{j\beta}}$. The signal combining can be expressed as:

$$\boldsymbol{x_T(t) = x_{IF}(t) + x_{IF}(t)e^{j\beta}e^{-j\beta} = 2x_{IF}(t)} \tag{7.1}$$

If we consider this operation in the frequency domain, then assuming $\boldsymbol{\mathfrak{F}\{x_T(t)\} = X_T(\omega)}$ and $\boldsymbol{\mathfrak{F}\{x_{IF}(t)\} = X_{IF}(\omega)}$, we see that

$$\boldsymbol{X_T(\omega) = X_{IF}(\omega) + X_{IF}(\omega)e^{j\beta}e^{-j\beta} = 2X_{IF}(\omega)} \tag{7.2}$$

Hence, the phase-shift in time domain is carried on to the frequency domain. Further, the vector phase rotation technique [25] can also be performed in the frequency domain. Quadrature IF signals are created by multiplying quadrature LO signals to the same RF signal.

7.2.1 Applying the Fast-Fourier Transform

Vector phase-rotation can be used to phase-shift IF signals. But the vector phase-rotation operates on the entire IF signal. If the IF signal could be *split* into different

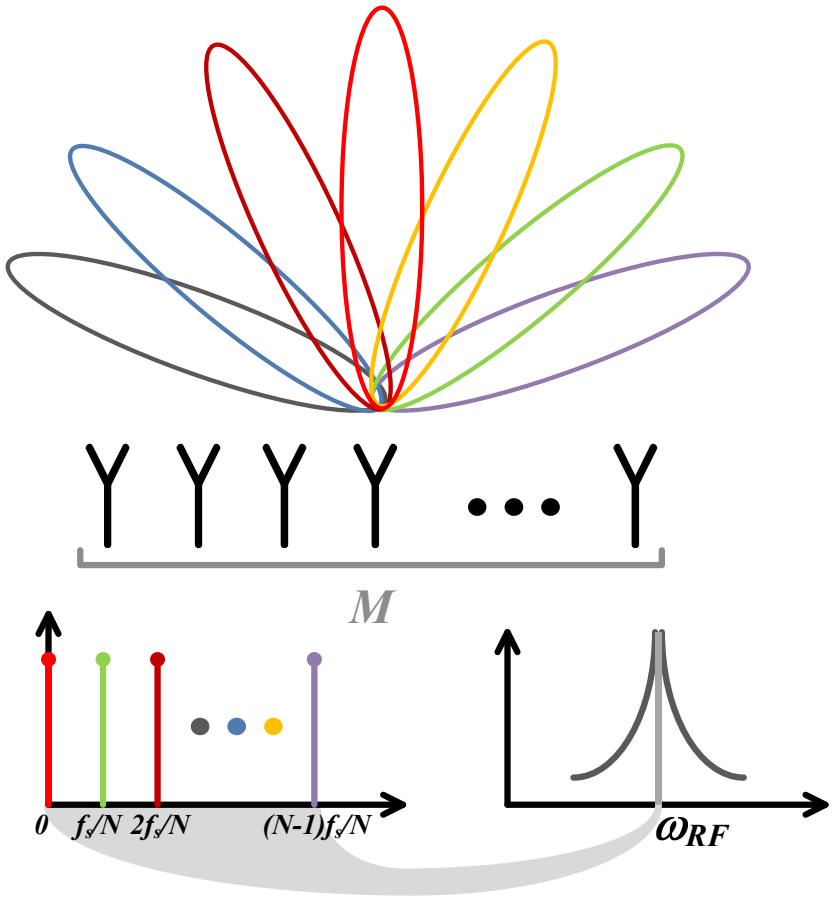


Figure 7.3: N independent beams by using FFT

frequencies or bands, then vector phase-rotation on each tone or band could result in multiple beams. The fast-Fourier transform or FFT can be used for this purpose. N samples of the IF signal taken at a sampling frequency of f_s, create N frequency bins given by - 0, f_s/N, $2f_s/N$, ..., $(N-1)f_s/N$. If the received quadrature IF signal is made up of tones which exactly overlap on these bins, the IF can be effectively split into independent frequency channels by the FFT operation.

The N outputs of the FFT represent the signal strength and phase on their corresponding bins. These bins can be independently phase-rotated. Thus for the two-channel case depicted in Fig. 7.2, performing an N-point FFT on each of the channels results in N-bins for each channel. These N-bins can be independently phase-shifted and combined, resulting in N independently steerable beams at N frequencies.

There are numerous advantages of this technique. First, it does not reduce the array-gain like sub-arraying. Second, the hardware increment is in the size of the FFT computation and the individual IF section for vector phase rotation and combining. This has a smaller power overhead than having separate RF and IF channels for individual beam processing. Also, this architecture can be used for narrowband systems. The frequency bins depend on the sampling frequency f_s. By ensuring that f_s is within the bandwidth of the receiver, N beams can be independently received, as illustrated in Fig. 7.3.

The same beamforming scheme can also be extended to the transmitter. In fact, by ensuring that all the N bins point to the same direction, beam-forming can be achieved for Orthogonal Frequency Division Multiplexed (OFDM) signals [10]. Creating N beams also allows for significant frequency diversity which is effective in combating frequency-selective fading.

7.3 Receiver Architecture

A two-channel 8GHz receiver is implemented in the IBM's 65nm CMOS process. Fig. 7.4 shows the block-level schematic of the receiver. The RF section consists of an 8GHz balun and quadrature downconversion mixers. The two channel inputs are applied to the chip through GSGSG probes. Each balun drives two mixers (in-phase and quadrature). Each downconversion mixer consists of a Gilbert cell, with current bleeding for g_m enhancement (topology used previously in Chapter 5, Fig. 5.5(b)). The mixer achieves

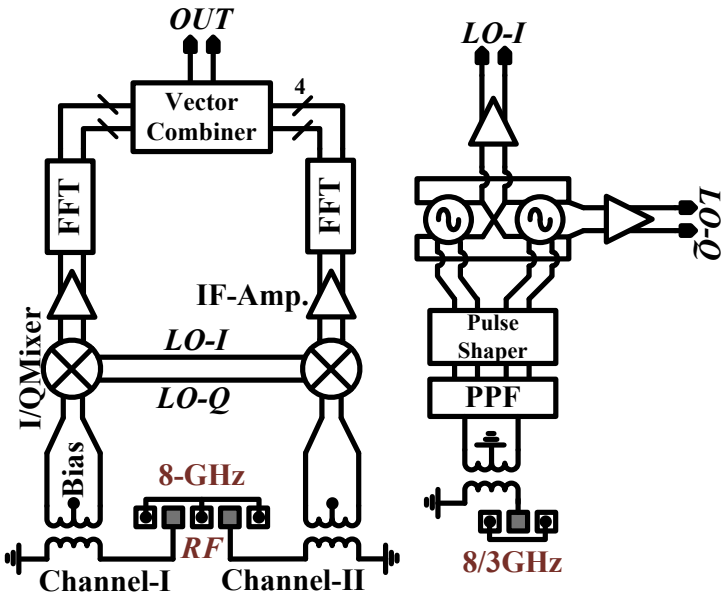


Figure 7.4: Two-channel receiver architecture using FFT

a voltage gain of 8dB. A source follower buffers the individual IF outputs and drives FFT processing core.

The FFT processing core computes a 4-point FFT. It consists of a sampling stage and switched capacitor computation section. The sampling stage consists of four samplers, which take contiguous samples. If (x_0, x_1, x_2, x_3) are the four samples, their FFT can be expressed as:

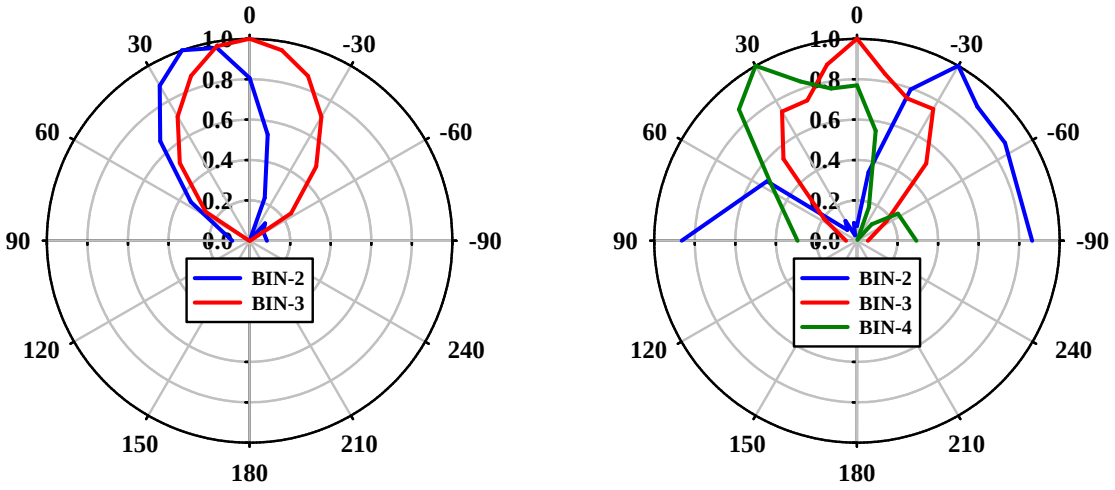
$$X_k = x_0 + x_1 e^{-j\frac{\pi k}{2}} + x_2 e^{-j\pi k} + x_3 e^{-j\frac{3\pi k}{2}} \qquad 0 \leq k \leq 3 \tag{7.3}$$

For our case of 4-point FFT, all the coefficients result in either ± 1 or $\pm j$. These computations can be easily performed by reversal of differential and/or quadrature signals. Once these computations are completed, the summation operation is achieved through averaging of all the samples stored on the capacitors. For higher-point FFTs, more involved computation circuits need to be employed.

The 4-point FFT results in four bins implying that four beams can be independently

created. However, since the first bin is at zero frequency or DC, any offset in the baseband circuits before the FFT stage can significantly affect the performance of this bin. Hence, the DC bin is not used in our architecture for signal combining. Therefore, an $\boldsymbol{N}$-point FFT can create $\boldsymbol{N-1}$ independent beams.

The vector combiner performs phase-cancelation and signal combining for the phased-array receiver. The two FFT engine's output bins, as depicted in Fig. 7.4, are the input to the vector combiner. For this proof-of-concept design, only three possible configurations of phase-shift within the vector combiner, have been designed - 0° and ±90°. Consequently, for a half-wavelength-spaced antenna array, the beam can be at broadside or ±30° around the broadside. Synthesized beam patterns obtained from simulations are shown in Fig. 7.5. It shows two concurrent and three concurrent beam configurations. Other angles can also be created by using non-unity magnitude coefficients.



(a) Two concurrent beams

(b) Three concurrent beams

Figure 7.5: Synthesized beam patterns for the designed two-channel receiver

The quadrature LO signals for the quadrature mixers are generated from a QILO.

The QILO performs frequency multiplication, in addition to, quadrature reinforcement [76]. An injection frequency of one-third the required LO frequency is applied through GSG probes. The balun converts the signal to differential outputs and the poly-phase-filter (PPF) subsequently converts the differential injection signal to quadrature differential injection signals. These quadrature signals are converted to square-wave and pulse-slimmed to reduce the content of the fundamental injection frequency [56]. The series QVCO core, similar to that adopted in [56, 78] is used. The QVCO draws approximately 6mA of current from a 1.2V power supply and uses 3-bits of binary capacitor banks for frequency tuning. The tuning range achieved is from 6.5 to 9GHz. CML buffers convert the sinusoidal output to approximate square waves and draw a combined current of 12mA.

7.4 Summary

We have proposed a novel architecture for multi-beamforming. It can essentially be classified under baseband beamforming. The architecture provides significant advantages over previous state-of-the-art for multi-beam generation phased-array architectures. A prototype is presently in fabrication in IBM's 65nm CMOS process. The functionality of multi-beamforming is verified through simulations. The layout of the prototype is illustrated in Fig. 7.6.

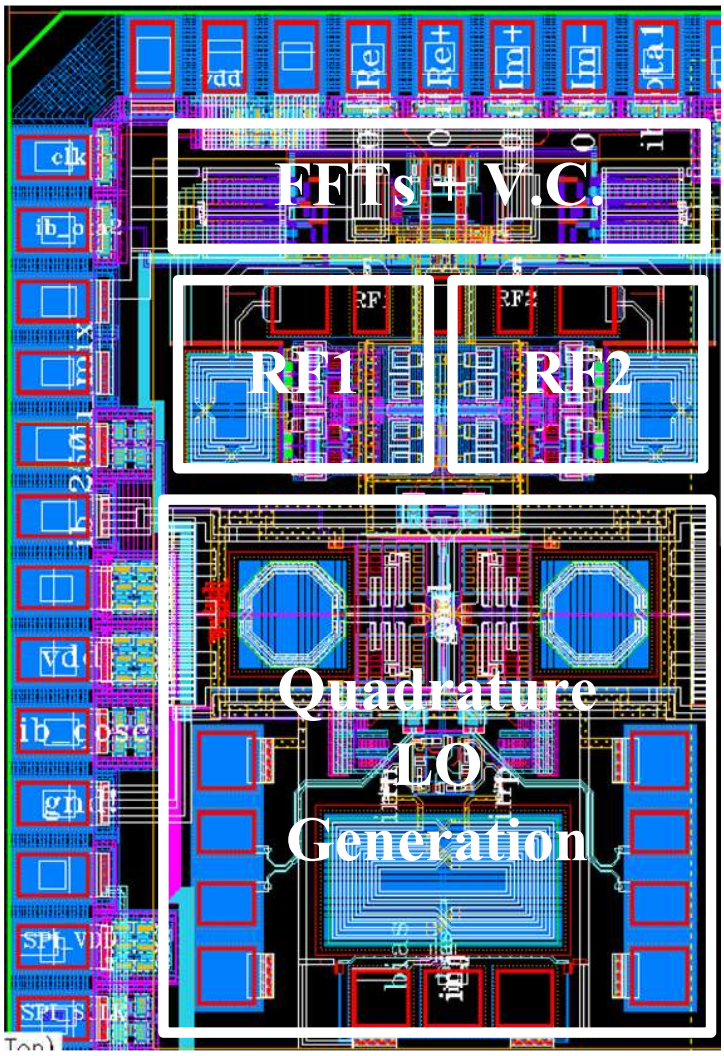


Figure 7.6: Layout of the two-channel receiver

Chapter 8

Other Work: 24-GHz UWB LNA

According to Shannon's theorem, the channel data-rates are directly proportional to the consumed frequency bandwidth. To support gigabit data rates over wireless networks, a large bandwidth is required. Ultra-wide bands (UWB) have been opened by the FCC centered around RF and mm-wave frequencies for high-data rate applications. Most RF blocks use LC-tuned circuits for narrowband operation. However, narrow-band circuits are not suitable for transceivers operating in these UWB frequencies. In this chapter, we present an ultra-wideband LNA designed around a center frequency of 24GHz. The LNA operates over a bandwidth of 21-25GHz and is part of a receiver, implemented in a 0.13-μm CMOS process and currently in fabrication. Section 8.1 describes the input matching technique used in the LNA. The two-stage design is explained in Section 8.2 and simulation results are presented in Section 8.3.

8.1 Wideband Input Matching

The LNA amplifies a signal without introducing significant noise at the output. At the same time, since most antennas are located far away (electrically) from the receiver,

transmission lines are used to connect the antenna to the LNA. Naturally, the LNA's input needs to be impedance matched to the transmission line's characteristic impedance. Inductive degeneration is the most widely used technique for impedance matching in LNAs. However, the need to place an additional large inductor at the gate of the LNA input transistor, in this technique, results in a narrowband impedance match [9].

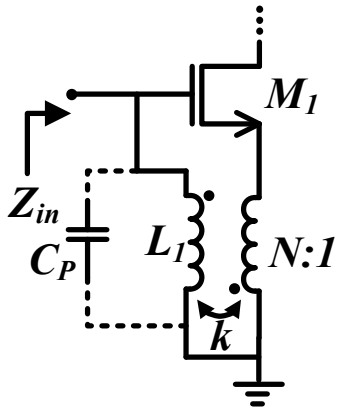


Figure 8.1: Transformer feed-back input matching

One of the simplest techniques to achieve wideband matching is through the use of a transformer [79]. A transformer-feedback input, as shown in Fig. 8.1, results in an input admittance ($\boldsymbol{Y_{in}}$) given by

$$\boldsymbol{Y_{in} = \frac{1}{Z_{in}} = kN(1+kN)g_m + j \cdot \left[(1+kN)^2 \omega C_{gs} - \frac{1}{\omega L_1}\right]} \tag{8.1}$$

where $\boldsymbol{g_m}$ and $\boldsymbol{C_{gs}}$ are the transconductance and gate-to-source parasitic capacitance of the input transistor $\boldsymbol{M_1}$. The imaginary part in (8.1) is primarily inductive for nominal values of the turns ratio, $\boldsymbol{N}$. Hence, by placing a capacitor $\boldsymbol{C_p}$ in parallel to the transformer, as shown in Fig. 8.1, the inductive portion of $\boldsymbol{Y_{in}}$ can be neutralized, resulting in a real impedance of

$$\boldsymbol{Z_0 = \frac{1}{kN(1+kN)g_m}} \tag{8.2}$$

The pad capacitance in an IC can be used as C_p. The matching is wideband because of the wideband response of a transformer and the low-Q of the reactive elements used in the matching. Further, the transconductance of the overall input section consisting of the transistor and the transformer is enhanced to $g_m(1 + kN)$.

8.2 LNA Design

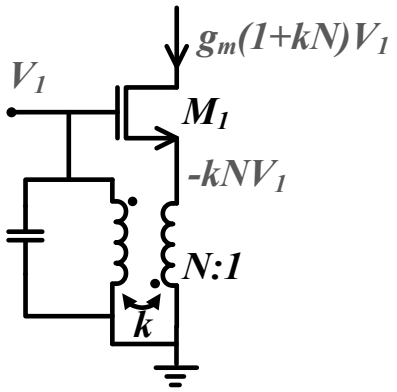


Figure 8.2: Increasing the transconductance of the input section

The design requirement for the LNA is to operate in the range of 21-25GHz and provide a voltage gain of approximately 10dB over the entire bandwidth. It is designed in the IBM's 0.13-μm CMOS process. The most important step in the design of this LNA is the choice of the transformer. Hence, a 1:1 transformer is designed using the top two thick metals. By stacking the metals one on top of the other, the coupling factor is set at 0.65. For a turns ratio of 1:1, the required g_m from the input transistor for 50Ω matching is about 17.5mS. When the low resonant impedance (R_p) of parallel LC-tanks at mm-wave frequencies is considered, the required g_m of the input transistor, in spite of the transconductance improvement, does not provide enough gain. A multi-stage design can be used to boost the gain. However, the number of reactive elements in the circuit also increases with number of stages, increasing the area of the LNA.

On the other hand, if additional transconductance can be added to the input without disturbing the input matching, the gain can be increased without any area penalty. It should be observed that the drain current (flowing into the drain) of the input transistor is in phase with the input gate voltage, in spite of the transformer feedback. This is explained in Fig. 8.2. Hence, adding another transistor parallel to $\boldsymbol{M_1}$, $\boldsymbol{M_1'}$ with its source connected to ground can improve the overall transconductance to the desired value (corresponding to the required gain). It also, however, directly increases the noise figure of the LNA, unlike a multi-stage design. Hence, the trade-off is between area and noise figure, of which we choose the former due to area constraints on the design. A cascode transistor on top of the input transistor pair mitigates the Miller effect of drain-to-gate capacitance of the input transistor and provides better reverse isolation.

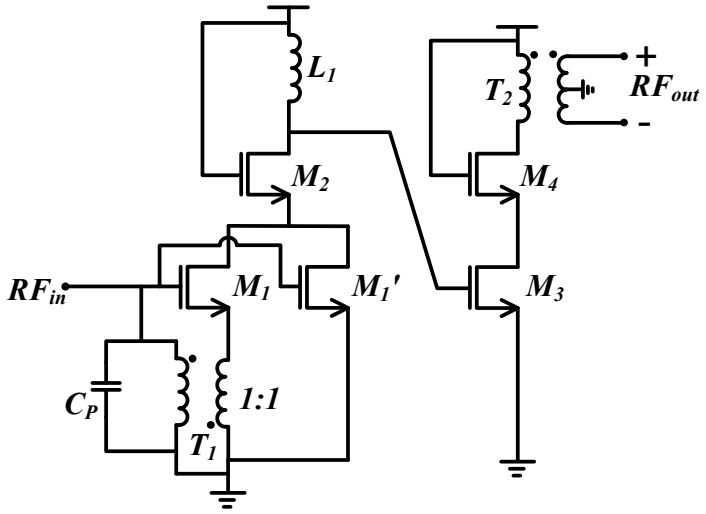
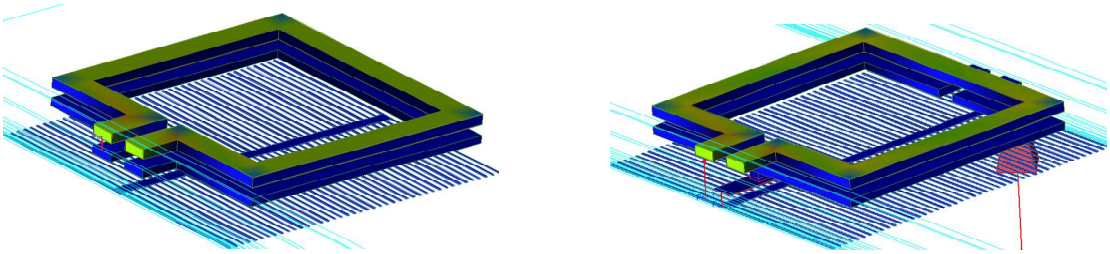


Figure 8.3: Two-stage LNA

To meet the gain requirement of >10dB, the LNA is split into two stages as depicted in Fig. 8.3. The first-stage provides gain for the lower-end of the bandwidth. The inductance $\boldsymbol{L_1}$ is set to 255pH such that it resonates out the parasitic capacitance at

the output node of the first-stage, at a frequency of approximately 21GHz. The second-stage has a balun as the load. The balun drives a set of four mixers (two channels each consisting of $\boldsymbol{I}$ and $\boldsymbol{Q}$ mixers). The second-stage is also a single-ended cascode amplifier.

The two transformers $\boldsymbol{T_1}$ and $\boldsymbol{T_2}$ used in the design are shown in Fig. 8.4. Both these transformers have been custom-designed and analyzed in an EM simulation tool. The extracted S-parameters were used in Cadence Spectre environment for the simulation of the LNA.



(a) Input matching transformer $\boldsymbol{T_1}$ (b) Output balun $\boldsymbol{T_2}$

Figure 8.4: Transformer coils used in tha LNA

8.3 Simulation Results

The two-stage UWB LNA has been designed in the IBM's 0.13-$\boldsymbol{\mu}$m CMOS process and is currently in fabrication, as part of a 24GHz UWB receiver. The layout of the LNA is depicted in Fig. 8.5. Simulations show that the total power dissipation is about 9mW from a 1.2V supply.

The two transformers, $\boldsymbol{T_1}$ and $\boldsymbol{T_2}$, are simulated in Agilent's Momentum environment. In Cadence Spectre environment, the extracted S-parameters are used for $\boldsymbol{n}$-port network definition. Since the transformers are in a 1:1 ratio, their coupling factor, $\boldsymbol{k}$, is plotted in Fig. 8.6, along with the phase-difference between the output and the input.

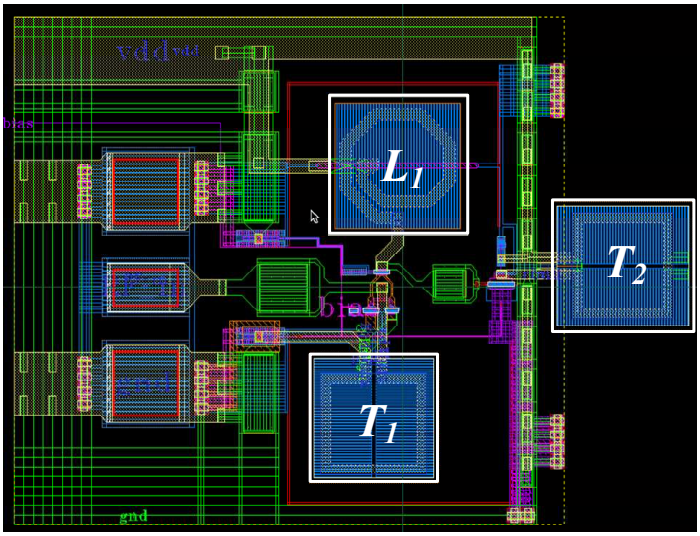
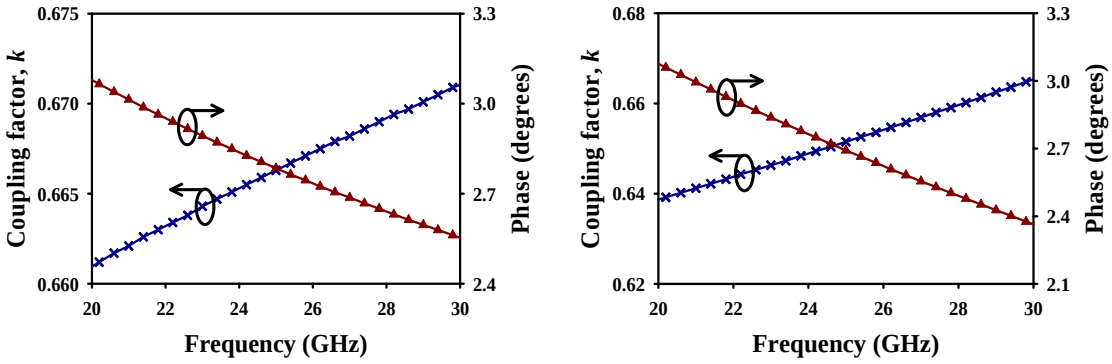


Figure 8.5: Layout of the two-stage LNA

For the balun, the phase-error between the differential ports is less than 0.5°. The coupling factor for both the transformers ranges between 0.64 and 0.68, which is close to the maximum coupling possible at these frequencies considering the design rule check (DRC) limitations of their layout.



(a) Coupling characteristics of T_1 (b) Coupling characteristics of T_2

Figure 8.6: Transformer characteristics simulated in Agilent Momentum

As depicted in Fig. 8.5, the single-ended RF input was applied through GSG probe pads. The probe-pad capacitance to ground and the gate capacitance of M_1' compensate

for the required C_p for resonance. The simulated input matching and noise figure for the LNA over a frequency range from 20-30GHz is shown in Fig. 8.7. The input matching is better than 10dB over the entire band, which highlights the broadband nature of the matching technique. The noise figure of the LNA in the required band of 21-25GHz is between 6.2-6.6dB. The relatively high NF is attributed to the frequency of operation, which is close to one-third the f_T of the nMOS input transistor.

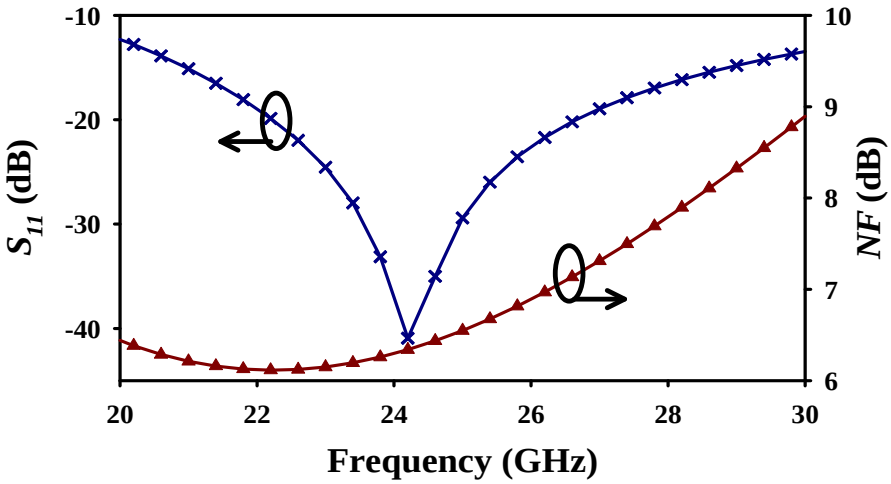


Figure 8.7: RF characteristics of the LNA: S_{11} and NF

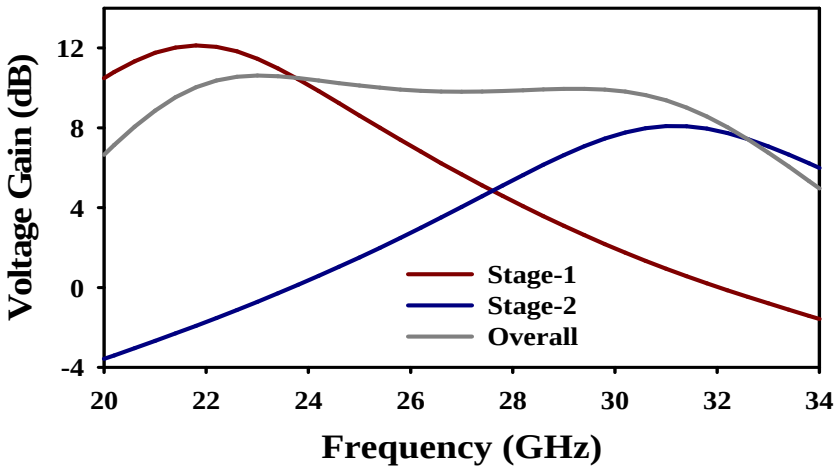


Figure 8.8: Stage-level and overall gain of the LNA

The voltage gain of the two stages of the LNA along with the overall gain is plotted in Fig. 8.8. The LNA's output is not matched. Hence, only the voltage gain is measured. The 3dB bandwidth of the LNA ranges from 20.5GHz to 32.5GHz. These simulations include the load of four downconversion mixers. The LNA's higher edge of the bandwidth has been over-designed to ensure proper operation even in the case of significant parasitic capacitance due to routing in the layout, which cannot be accurately accounted for without extensive EM simulations.

8.4 Summary

An ultra-wideband 24GHz LNA topology is presented with simulation results. It is implemented in a 0.13-μm CMOS technology and is presently in fabrication. The two-stage LNA draws 9mW of power from a 1.2V supply and achieves 10dB of gain with a 3dB bandwidth of more than 10GHz. It uses a transformer feedback network for wideband input matching and achieves an average noise figure of 6.5dB over the required frequency range of 21-25GHz.

Chapter 9

Conclusions & Contributions

Multi-antenna and ultra-wideband-based solutions are likely to be the only possible means to meet the ever-increasing demands for higher throughput over wireless networks. This thesis has discussed circuits and architectures, which can be employed in these solutions. The primary goal in the design of the proposed circuits and architectures is to advance the state-of-the-art by allowing for lower power with minimal compromise in other performance metrics. The most important advantage of lower power dissipation is that these techniques can be used to realize high-data wireless portable systems, which invariably run on a power budget.

Two new architectures for progressive/arbitrary phase-generation have been introduced - fully-flexible and meander-line, based on the injection-locking of LC-oscillators. A dual-mode receiver, integrating the two architectures, is designed and fabricated in a 0.13-μm CMOS process. Measurement results verify the architecture's beamforming capabilities, which are in excellent agreement with theoretical estimates. This proves the feasibility of our concept architecture. The overall power consumption of the four-channel receiver is 50% less than previous state-of-the-art design and proves the advantages that ILOs bring to beamforming transceivers.

The LO distribution network in any transceiver consumes a significant portion of its power. The situation grows worse for LO-phase-shifting architectures. Hence, the fully-flexible architecture based on injection-locking is improved by allowing the ILO to perform multiple functions, including frequency tripling. This lowers the LO frequency requirement to one-third of the original frequency, which reduces the power budget for LO distribution and the frequency synthesizer for the LO. A CMOS prototype implemented in a 0.13-μm BiCMOS process, is used to verify the capability of the ILO to perform these multiple functions simultaneously.

The requirements of military radars differ from those of commercial portable applications. Military radars are used for target detection and tracking, projectile guidance and long-range surveillance. Multiple beams are required to cater to these different applications individually. Multiple beams may also be dedicated to each application to improve their performance. Sub-arraying is widely used to achieve this. However, it is a sub-optimal solution since it breaks the array into smaller groups and consequently, reduces the array gain factor. It also limits the number of independent beams that can be created. This can significantly affect the range of operation of radars. We propose a new novel technique to generate multiple beams without sacrificing on performance. It uses the fast-Fourier transform (FFT) to separate individual beams into equally spaced frequency bins and allows for their individual processing. The advantage of this technique is that it does not reduce array gain. Additionally, it decouples the number of beams from the number of antennas, making it a highly scalable solution. A two-channel X-band phased-array implementation in 65-nm CMOS is presently in fabrication. The proof-of-concept prototype uses a four-point FFT to create three independent beams.

We have also presented an ultra-wideband low-noise amplifier (LNA) design, which is applicable to both high-data rate commercial applications and military radars. A 24GHz prototype has been implemented in a 0.13-μm CMOS process. It is implemented as part

of an ultra-wideband receiver and is presently in fabrication. Simulations show that the LNA achieves 10.5dB of voltage gain over a 3dB bandwidth of more than 10GHz, while drawing 9mW of power. As the circuit operates close to the cut-off frequency of transistors in 0.13-μm CMOS technology, it exhibits an average noise figure of 6.5dB. This can be expected to significantly reduce when the circuit is implemented in more advanced CMOS technologies, making it an excellent LNA solution.

In addition to the presented circuits and architectures, this thesis also discusses avenues for future work. The proposed fully-flexible and meander-line architectures have been extended to 2D phased arrays. The theory of quadrature ILO proves that they can be used in the place of ILOs, to create phase-shifts and quadrature LO outputs. Finally, the FFT-based architecture may also be used for beamforming in OFDM-based transceivers.

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