Matrix Converter fed Power Electronic Transformer with enhanced features

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Dedication

To my parents and to my guru - His Holiness Sri Sri Ravi Shankar

Abstract

Power transformers are an integral part of power systems. In many applications, like wind energy conversion and electric ship, the large weight and volume of present 60 Hz power transformer is a limitation. The size of transformers can be reduced by replacing the power transformers with high frequency transformers. For use of high frequency transformer in power systems, first the low frequency voltages are converted to high frequency by a power electronic converter and then it is stepped up or down by the high frequency transformer and finally the high frequency voltage is converter to low frequency by a second power electronic converter. The whole system is termed as power electronic transformer (PET).

Matrix converter(MC) based power electronic transformers are the focus of this doctoral research. Direct AC to AC conversion using matrix converters have the major advantage of absence of storage capacitors over AC-DC-AC based conversion systems. A matrix converter based PET with open ended primary is described in this thesis. It has the salient features of controllable output voltage frequency, controllable input power factor, bi-directional power flow, zero common mode voltage and voltage transfer ratio of 1.5. The described PET is analyzed and simulation results are presented.

Commutation of current in the leakage inductance is one of the challenges in the matrix converter based PET. The effect on voltage regulation due to increase in leakage inductance is studied using extensive simulation. An alternative path is needed for change of direction of current during commutation time. One of the ways to provide alternative path is use of clamp circuits. But use of clamp circuits lead to energy loss unless efficient energy recovery systems are designed.

A source based commutation method is proposed to eliminate the use of clamp circuits. Depending on the direction of current in the HF transformer, the matrix converters on primary side of the transformer are switched such that natural commutation takes place in the leakage inductances. The overall efficiency of the PET is significantly improved.

The commutation time is dependent on the value of leakage inductance. So, higher the leakage inductance, larger the commutation time and therefore, lower is the switching frequency. The nano-crystalline materials used for making HF transformers have very low core losses at very high frequencies as compared to 60 Hz power transformers. Also, power devices made of SiC devices are available which can operate at very high switching frequencies with very low switching losses. Therefore, leakage inductance is the only factor that limits the switching frequency. To solve the above mentioned problem, three novel PET topologies are proposed in which the switching frequency is independent of the value of leakage inductance. The first one is sinusoidal input output three phase HF transformer. It has a three phase low pass filter and a matrix converter on both primary and secondary side of the HF transformer. Three square wave voltages at switching frequency, phase shifted by 120° are produced by the primary side MC. The square wave voltages are filtered by the primary side filter to give three sine waves at high frequency shifted by 120°. The switched currents at the input of secondary side MC are filtered by the secondary side low pass filter. The HF transformer works like a three phase power transformer.

The second topology proposed is sinusoidal input output three winding HF transformer. In this topology, the supply voltages are first converted to square wave voltage at high frequency by a three phase to single phase MC and then filtered to a sine wave by a low pass filter connected to primary of the HF transformer. Two opposite sine voltages at high frequency are produced by the three winding transformer, on the secondary side, which is further connected to two capacitors. The switched currents on the input of MC, connected to load, are filtered by these two capacitors. The transformer again sees sinusoidal voltages and currents as in the first topology. Zero common mode voltage is achieved in this topology by use of a modified pulse density modulation(PDM) strategy proposed.

The third one proposed is sinusoidal current HF transformer. Unlike the first two, it does not has a filter on the primary side. A high frequency square wave voltage is produced by a three phase to single phase MC. A MC is connected between the secondary terminals and the load. PDM is used for secondary side MC. A low pass filter is formed with the transformer by connecting a capacitor at the secondary terminals. Both, the switched currents at input of secondary side MC and the square wave voltages across

the primary windings are filtered by the low pass filter. Thus, only sinusoidal currents flow through the HF transformer.

In all the above three mentioned topologies, the leakage inductance is used to form the low pass filter, minimizing the amount of reactive elements required. As these low pass filters are required to filter very high frequency voltages, the size of reactive elements are reduced. For the sinusoidal current HF transformer only one additional capacitor is needed. Also because of use of PDM, zero voltage switching is possible for the sinusoidal three winding and sinusoidal current transformers.

All the proposed topologies are analyzed and simulated in MATLAB/ SIMULINK environment and the simulation results are presented. Mathematical model for filter design is provided. A laboratory prototype is built for sinusoidal current HF transformer and the experimental results are presented.

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Chapter 1

Introduction

Transformers are one of the most essential parts of a power system. However, present transformers of 60Hz are very bulky and occupy a large space. Large volume and weight of transformers are a limitation for several applications like off-shore wind power generation [5] and electric ships [6], [7]. Also, the transportation, replacement and maintenance time for present power transformers is high due to large weight and volume.

Transformer core size reduces with frequency. Higher the frequency smaller is the size of transformer core. So, high frequency (HF) transformers provide a solution for the problem of large volume and weight of $60Hz$ transformers.

In this chapter, a power electronic transformer (PET), its advantages and limitations are described. The applications of PET are discussed. Present proposals for PET are based on AC to DC and then DC to AC conversion systems [8–17]. Direct AC to AC conversion is an alternative for PET.

Matrix converter based high frequency transformers are the main motivation of this doctoral research. The problem of leakage inductance in PET has been addressed by proposing several novel topologies described in this thesis.

1.1 Power Electronic Transformer

A power electronic transformer is a system comprising of power electronic converters and a high frequency transformer. Fig. 1.1 shows a PET. The $60Hz$ low frequency

supply is converted to high frequency by a power electronic converter. The high frequency transformer steps or steps down the high frequency voltage. The voltage at the secondary of HF transformer is converted to low frequency by a power electronic converter.

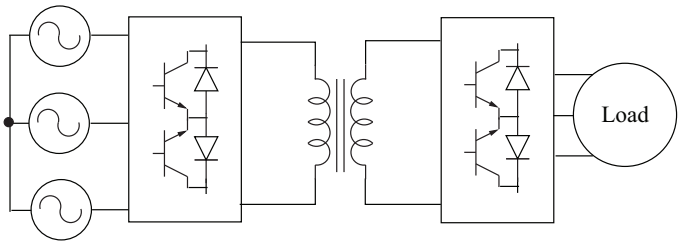

Figure 1.1: Power electronic transformer

The core of HF transformer is made up of nano-crystalline material. One of the nano-crystalline materials is FINEMET which is a promising material in terms of reducing core loss. Table 1.1 shows a comparison of a power transformer at $60Hz$ and a $20kHz$ HF power transformer. Fig. 1.2 shows a pictorial comparison of size. It can be seen from table 1.1 that for comparable ratings, the core loss of FINEMET built HF transformer is approximately $\frac{1}{11}$th of the core loss of $60Hz$ power transformer and the size of HF transformer is approximately $\frac{1}{150}$th of that of $60Hz$ power transformer.

Table 1.1: Comparison of $60Hz$ power transformer and $20kHz$ HF power transformer [2]

	60Hz Power transformer	HF transformer
Voltage and frequency rating	100kV, 60Hz	140kV, 20kHz
Current rating	20Amp RMS	20Amp RMS
Power	2MW	1MW
Weight	35 Tons	450 lbs
Loss	Approx. 35 KW	Approx. 3 KW at 2MW

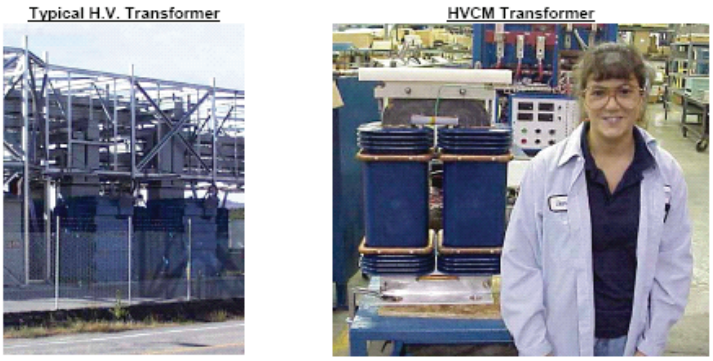

Figure 1.2: Comparison of size of 60Hz and 20kHz HF transformer [2]

Fig. 1.3 shows the plot of increase in core loss with frequency for three different types of FINEMET. The plot of fig. 1.3 is provided by the manufacturer of nano-crystalline material HITACHI [3].

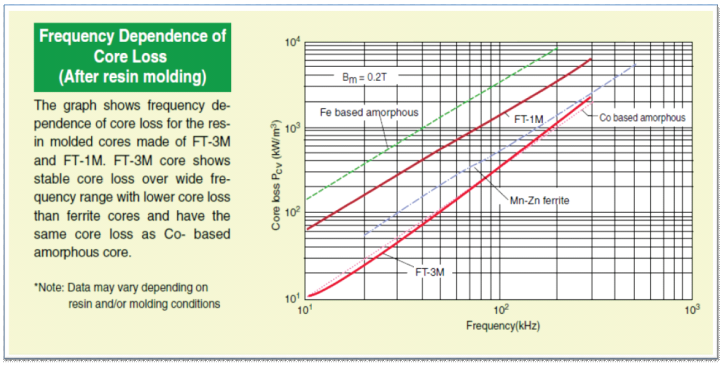

Figure 1.3: Core loss vs frequency plot of FINEMET [3]

From fig. 1.3 it is clear that the core loss of nano-crystalline materials is less as compared to $60Hz$ transformers even at very high frequencies such as $100kHz$. The data provided starts at a minimum frequency of $10kHz$. Thus, the potential use of HF transformers is at very high frequencies, which is a desirable characteristics since higher the frequency smaller is the weight and volume of the transformer.

1.2 Power electronic converters for HF transformers

Present proposals for PET are based on AC to DC and DC to AC conversion. One such conversion system is shown in fig. 1.4. $60Hz$ AC is converted to DC and DC is converted to HF AC on the primary side of the HF transformer. The HF AC at secondary side of the transformer is converted to DC and then to low frequency AC. The major limitations of the AC-DC-AC system are:

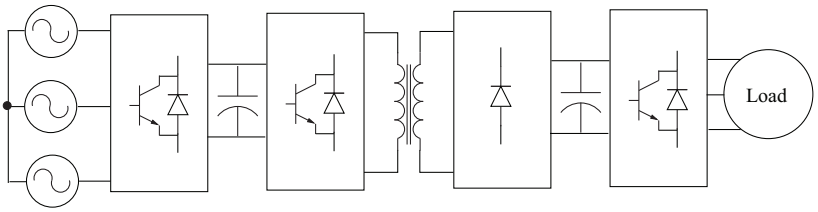

Figure 1.4: Power electronic transformer with AC-DC-AC converters

1. Need of bulky storage capacitors. The storage capacitors occupy large space, add to the volume of the total PET, reduce the reliability of the system and are susceptible to poor performance and failure at high temperatures.

2. Large reactive elements are needed at the input side of the AC-DC-AC based topologies which further increase the weight and volume of PET.

An alternative to AC-DC-AC conversion is direct AC-AC conversion using matrix converter (MC) based topologies [18–24]. A review of matrix converters is available in [25, 26]. The advantages of matrix converter based PET over AC-DC-AC conversion system are:

1. Removal of large storage capacitors, thus reducing weight and volume and increasing reliability.

2. Possibility of zero common mode voltage by use of rotating space vectors in the modulation scheme and by other novel modulation schemes described in chapter 6.

However in matrix converter based PET, the commutation of current in leakage inductance of HF transformers is a limitation.

1.3 Applications of PET

Following are some of the application areas where PET are needed.

1. Wind power generation - The present wind power generation system is shown in fig 1.5. Power generation takes place at $690V$, $60Hz$ and the bulky $60Hz$ transformers are placed at the bottom the the tower. Low voltage (LV) cables at $690V$ are brought to the bottom of 50 to $60m$ long towers. As LV cables are much thicker then high voltage (HV) cables, huge amount of cable management is needed which is a limitation of present wind generation system.

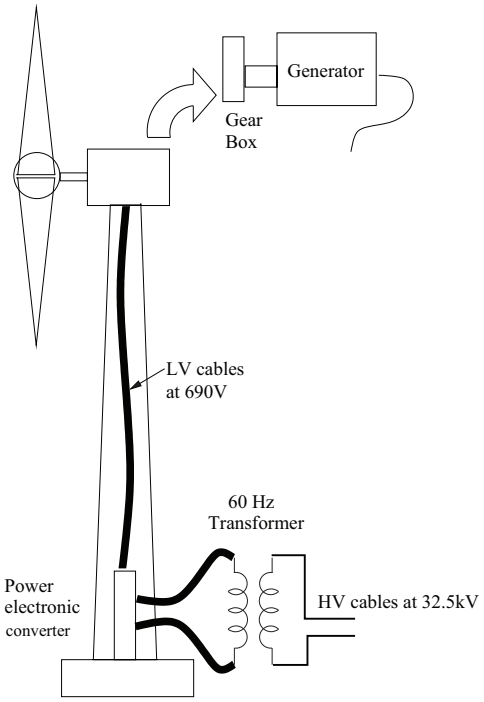

Figure 1.5: Present wind power generation system

Fig. 1.6 shows a wind power generation system based on matrix converters and high frequency transformers. Because of small size of HF transformers, it can be put at the nacelle, and therefore voltage can be stepped up in the nacelle. So HV cables at $2.5kV$, which are much thinner then $690V$ LV cables, need to be brought

down, reducing great amount of cable.

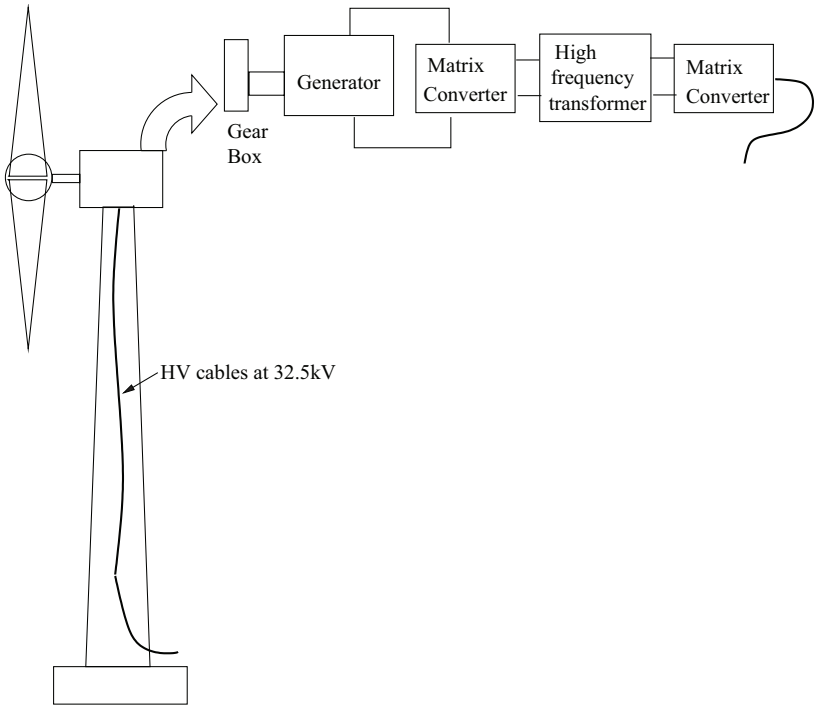

Figure 1.6: Wind power generation system based on MC and HF transformer

2. Marine applications - In electric ship applications, large volume and weight of $60Hz$ power transformers is a major limitation. Therefore, HF transformers can be used to step down voltage from $11kV$ to $690V$ [6, 7].

3. Power systems - PET can be used to replace the current $60Hz$ power transformers and is a research area for micro grids. The frequency at input and output of PET are independent. As PET are much smaller in size, they can be easily transported, replaced and back up PET can be kept in any power station. These are not possible with present power transformers.

1.4 Scope of this thesis

A matrix converter based power electronic transformer with open ended primary is described in this thesis. It has the salient features of elimination of large storage capacitors, voltage transfer ratio of 1.5, controllable input power factor, zero common mode voltage, bi-directional power flow and controllable output frequency.

When a direct AC to AC converter is connected to the secondary of a transformer, switched currents flow in the secondary winding of the transformer. Because of the leakage inductance of the transformer, the direction of current in the transformer cannot change instantaneously. An alternative path is needed for the commutation of current in the leakage inductance.

The time needed for the switched current to change its direction is termed as commutation time. It is dependent on the value of leakage inductance. And therefore, the switching frequency is limited by the value of leakage inductance. The following solutions are investigated in this thesis to solve the problem of commutation of current because of leakage inductance.

1. Use of clamp circuit - The current can be commutated with the help of a clamp circuit connected at the secondary of the transformer. But it leads to power loss and drop in voltage regulation.

2. Source based commutation - A source based commutation method has been proposed for the matrix converter based PET with open ended primary. It eliminates the requirement of clamp circuit and therefore power loss.

3. Family of sinusoidal HF transformer - The above two solutions provide an alternative path to the current during commutation. But the commutation time and therefore, the switching frequency is limited by the value of leakage inductance. But as seen in fig. 1.3 the nano-crystalline materials are capable of working at very high frequencies with low core loss. With the advancement in semiconductor technology, SiC devices are also available which can operate the power converters at high frequencies with low switching losses [27]. The following three novel sinusoidal HF transformer based PET are proposed, in this thesis, in which the

switching frequency is independent of the value of leakage inductance. And therefore, these can be used at very high frequencies.

(a) Sinusoidal input output three phase HF transformer

(b) Sinusoidal input output three winding HF transformer

(c) Sinusoidal current HF transformer

In all the above PET, the leakage inductance is used to form a filter by adding a capacitor at the secondary of the HF transformer.

All the above mentioned commutation methods and topologies are analyzed and simulated. The experimental results are presented for sinusoidal current HF transformer.

1.5 Contribution of this thesis

Following are the contributions of this thesis.

1. Detailed analysis and simulation of matrix converter based PET with open ended primary.
2. Study of effect of leakage inductance on voltage regulation of PET.
3. A novel source based commutation method for matrix converter based PET with open ended primary, its analysis and simulation results.
4. A novel sinusoidal input output three phase HF transformer, its filter design procedure and simulation results.
5. A novel sinusoidal input output three winding HF transformer with zero common mode voltage and simulation results.
6. A novel pulse density modulation scheme for the sinusoidal input output three winding HF transformer.
7. A novel sinusoidal current HF transformer, its filter design procedure, simulation and experimental results.

1.6 Organization of the thesis

Chapter 1 introduces power electronic transformers and its applications. The advantages of matrix converter based PET are explained and problems are discussed. Chapter 2 presents the matrix converter based PET with open ended primary. The modulation method is explained and simulation results are presented.

Chapter 3 discusses the problem of leakage inductance and its effects on PET. Source based commutation method is explained in chapter 4. Simulation results are also provided.

Chapter 5 introduces the sinusoidal input output three phase HF transformer. Filter design procedure is discussed and simulation results are presented. Chapter 6 presents the sinusoidal input output three winding HF transformer with zero common mode voltage. The PET is simulated with the novel modulation scheme and results are provided. Chapter 7 explains in detail the sinusoidal current HF transformer. The PET is simulated and also verified with hardware implementation. The simulation results are presented in chapter . Chapter 8 explains in detail the hardware implementation of the sinusoidal current HF transformer and also provides the experimental results. Chapter 8 concludes the thesis.

A detailed mathematical analysis of input filter design of matrix converters is provided in appendix A. Two step and four step commutation control, used for the commutation control of matrix converters, is explained in appendix B. Appendix C provides the verilog program used for the hardware implementation of sinusoidal current HF transformer.

1.7 Conclusion

The context of the thesis is established in this chapter. Power electronic transformer is introduced and its applications are explained. The advantages of matrix converter based PET are explained. The problem of leakage inductance in PET is introduced. The scope and contribution of this thesis are presented.

Chapter 2

Matrix converter fed power electronic transformer with open ended primary

A matrix converter fed PET with open ended primary is introduced in this chapter [21]. The space vector pulse width modulation (SVPWM) used to control the PET is explained. Due to open ended primary, 1.5 voltage transfer ratio is attained as compared to 0.866 from single matrix converter. Zero common mode voltage is achieved in the described PET by use of only rotating space vectors. Control of input power factor is explained. The described topology is simulated in MATLAB/SIMULINK environment and the simulation results are presented.

2.1 Circuit description

A power electronic transformer based on matrix converters with open ended primary is proposed in [21]. The circuit is described with the help of fig. 2.1 . The open ended primary of the transformer is fed from two power converters MC1 and MC2. These two converters are matrix converters with three bi-directional switches removed, one from each leg. The secondary of the transformer is connected to a third matrix converter MC3.

The three phase supply voltage at low frequency is first converter to high frequency by MC1 and MC2. Thus, the transformer sees only high frequency voltages. The high frequency voltages are stepped up or down by the transformer. These voltages are then converted to low frequency by MC3. MC1, MC2 and MC3 are switched in synchronization such that flux balance is maintained in the transformer and voltage and frequency can be controlled at the output of MC3.

A clamp circuit is connected at the input of MC3. The need and operation of the clamp circuit is explained in chapter 3.

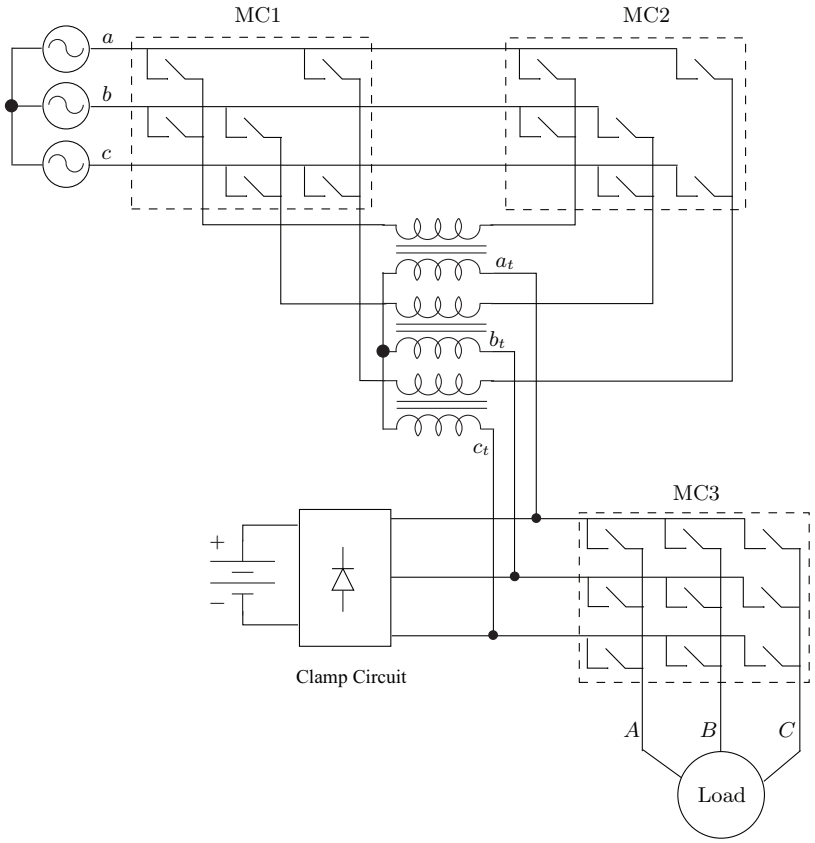

Figure 2.1: Matrix converter driven high frequency transformer

2.2 Synthesis and control of voltage across transformer

The supply voltages v_a, v_b and v_c can be written as

$$\begin{aligned} v_a &= \frac{2}{3}V_m cos(\omega_i t) \\ v_b &= \frac{2}{3}V_m cos(\omega_i t - \frac{2\pi}{3}) \\ v_c &= \frac{2}{3}V_m cos(\omega_i t + \frac{2\pi}{3}) \end{aligned} \tag{2.1}$$

where $\frac{2}{3}V_m$ and ω_i are the amplitude and frequency of the supply voltages respectively. The space vector that can be formed at the output of any thee phase to three phase converter can be written as

$$v_{123} = v_1 + v_2 e^{j\frac{2\pi}{3}} + v_3 e^{j\frac{4\pi}{3}} \tag{2.2}$$

where v_1, v_2 and v_3 are the voltages at the output of matrix converter.

There are 27 possible switching combinations in a matrix converter [28]. Out of these 27, 6 switching combinations produce rotating space vectors with zero common mode voltages [29]. Three out of these 6 are produced by anti-clockwise rotating vectors and three are produced by clockwise rotating vectors. Fig. 2.2 shows the three anti-clockwise rotating vectors that can be produced across the output of a matrix converter. The anti-clockwise reference vectors and the 180° phase shifted vectors are shown together in fig. 2.3.

Similarly, fig. 2.4 shows the three clockwise rotating vectors that can be produced across the output of a matrix converter. The clockwise reference vectors and the 180° phase shifted vectors are shown together in fig. 2.5.

Out of the three anti-clockwise rotating space vectors, only space vectors v_{abc} and v_{bca} can be produced by MC1 and MC2 (as these are not full matrix converters). MC1 and MC2 are switched such that when space vector v_{abc} is produced at output of MC1, then space vector v_{bca} is produced at output of MC2 and vice versa. Thus, the voltage obtained across the open ended primary winding is the difference of voltages v_{abc} and v_{bca} and vice versa. Or in other words it the addition of voltages v_{abc} and 180° phase shifted vector of v_{bca} and vice versa. The opposite space vectors are represented as $v_{a'b'c'}$ and $v_{b'c'a'}$. The space vector diagram of voltage obtained across the open ended primary winding is shown in fig. 2.6.

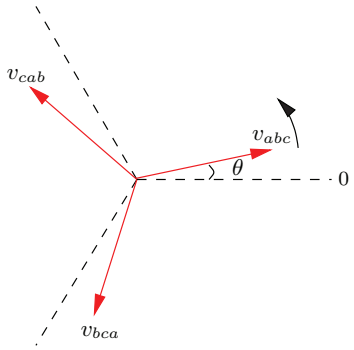

Figure 2.2: Anti-clockwise reference vectors

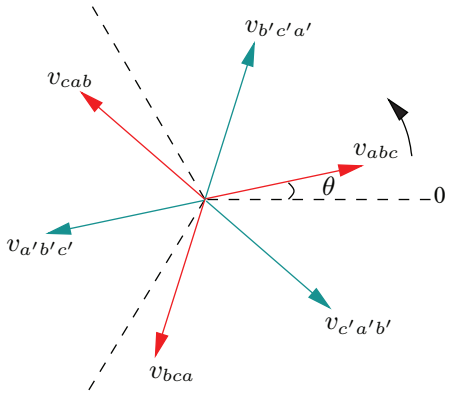

Figure 2.3: Anti-clockwise reference vectors and the opposite vectors

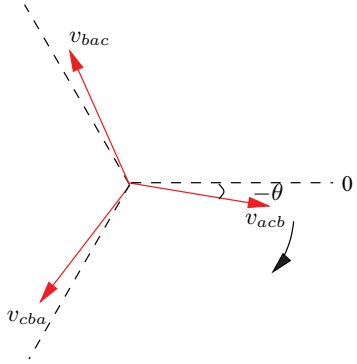

Figure 2.4: Clockwise reference vectors

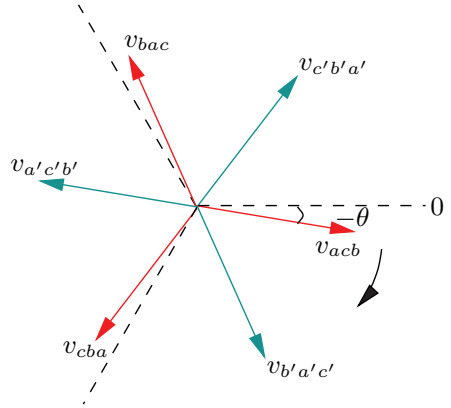

Figure 2.5: Clockwise reference vectors and the opposite vectors

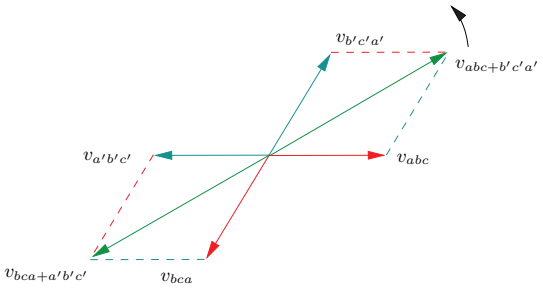

Figure 2.6: Anti-clockwise vectors applied to transformer

As is clear from fig. 2.6, two 180° phase shifted voltages are obtained across the primary windings. By switching these opposite voltages for equal switching time periods, the flux balance is maintained in the high frequency transformer.

To obtain zero voltage across the primary winding, both MC1 and MC2 are switched to provide either space vectors v_{abc} or v_{bca} at their output.

2.3 Synthesis and control of output voltage

The voltage at the secondary terminal of the HF transformer or at the input of MC3 is represented as v_{a_t}, v_{b_t} and v_{c_t}. The synthesis of output voltage of MC3 can be explained with the following example.

Table 2.1: Anti-clockwise vectors

MC1	MC2	MC3	Output
v_{abc}	v_{bca}	$v_{a_tb_tc_t}$	$v_{abc+b'c'a'}$
v_{bca}	v_{abc}	$v_{a_tb_tc_t}$	$v_{bca+a'b'c'}$
v_{abc}	v_{bca}	$v_{c_ta_tb_t}$	$v_{cab+a'b'c'}$
v_{bca}	v_{abc}	$v_{c_ta_tb_t}$	$v_{abc+c'a'b'}$
v_{abc}	v_{bca}	$v_{b_tc_ta_t}$	$v_{bca+c'a'b'}$
v_{bca}	v_{abc}	$v_{b_tc_ta_t}$	$v_{cab+b'c'a'}$

Suppose the space voltage vector at the terminals of open ended primary winding, by switching of MC1 and MC2, be v_{abc} or v_{bca}. So, the voltage at the terminals of primary winding are v_{ab}, v_{bc} and v_{ca}.

MC3 can be switched to produce clockwise or anti-clockwise vectors with respect to $v_{a_tb_tc_t}$. Suppose MC3 is switched to obtain anti-clockwise vector $v_{b_tc_ta_t}$. So, the voltage that appears at the output of MC3 is v_{bc}, v_{ca} and v_{ab}. The space vector produced by v_{bc}, v_{ca} and v_{ab} can be represented as a combination of space vectors v_{bca} and $v_{a'b'c'}$.

All other space vector combinations resulting from switching of MC1, MC2 and MC3, using anti-clockwise rotating vectors, are tabulated in table 2.1. The space vector diagram is shown in fig. 2.7.

The output voltages are synthesized from the space vectors shown in fig. 2.7 using space vector pulse width modulation. As can be seen from table 2.1, any two adjacent vectors in fig. 2.7 are obtained by switching combinations in MC1 and MC2, which produce 180° phase shifted voltages across the high frequency transformer. Therefore, to maintain flux balance in the HF transformer, any two adjacent vectors need to be applied for equal time periods.

The output voltage control can be explained with fig.2.8 and the following example.

The inscribed circle is divided in six sectors. At any instant, suppose the output space vector lies in sector no. 1. And suppose to produce this voltage, vectors marked as v_{11} and v_{12} need to be applied for T_1 and T_2 time intervals respectively. Vectors v_{11} and v_{12} are average vectors of vectors $v_{cab+b'c'a'}$ and $v_{abc+b'c'a'}$ and vectors $v_{abc+b'c'a'}$

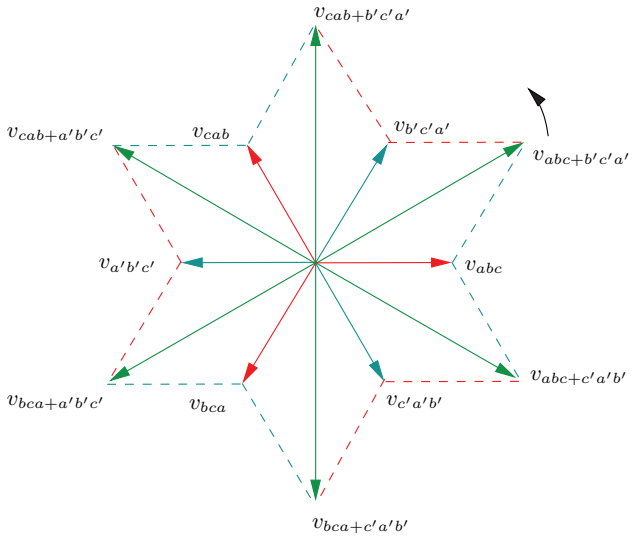

Figure 2.7: Output vector from anticlockwise rotating vectors

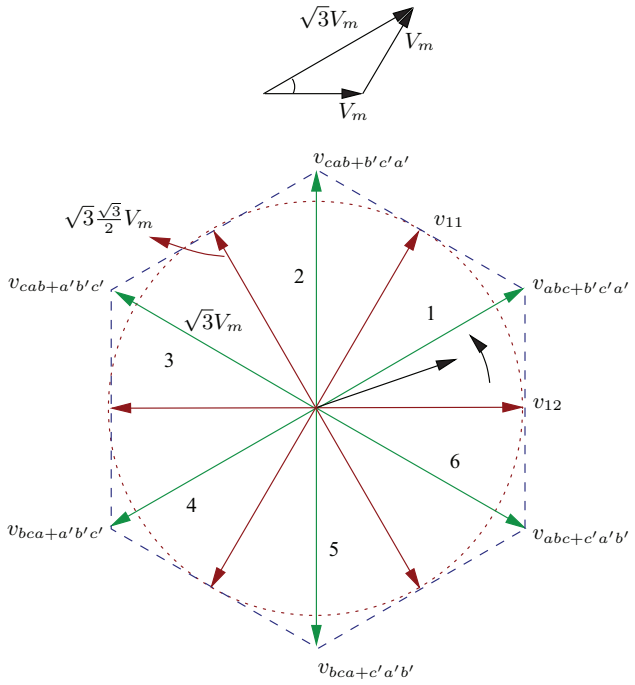

Figure 2.8: Diagram to illustrate maximum voltage transfer ratio

and $v_{abc+c'a'b'}$ respectively.

So, applying vector $v_{cab+b'c'a'}$ for $\frac{T_1}{2}$, vector $v_{abc+b'c'a'}$ for $\frac{T_1+T_2}{2}$ and vector $v_{abc+c'a'b'}$ for $\frac{T_2}{2}$ is equal to applying vector v_{11} for T_1 and vector v_{12} for T_2 intervals. Zero vector is applied for $T_0 = T_s - (T_1 + T_2)$ interval, where T_s is the switching time period.

The maximum voltage transfer ratio can be explained with help of fig. 2.8. It is clearly seen from fig. 2.8 the maximum magnitude of space vector obtainable is $\sqrt{3}X\frac{\sqrt{3}}{2} = 1.5$.

2.4 Synthesis output voltage from clockwise rotating vectors

The above section explained the synthesis of output voltage with anti-clockwise rotating vectors. The same output voltage can be synthesized with clockwise rotating vectors. Table 2.2 shows the vectors needed at MC1, MC2 and MC3 to produce clockwise rotating vectors at output. It is clear from table 2.2 that the switching vectors needed for MC1 and MC2 remain the same as in table 2.1. Clockwise vectors are used only for switching MC3. The synthesis of vector diagrams with clockwise rotating vectors is shown in fig 2.9.

Table 2.2: Clockwise vectors

MC1	MC2	MC3	Output
v_{abc}	v_{bca}	$v_{a_tc_tb_t}$	$v_{acb+b'a'c'}$
v_{bca}	v_{abc}	$v_{a_tc_tb_t}$	$v_{bac+a'c'b'}$
v_{abc}	v_{bca}	$v_{b_ta_tc_t}$	$v_{bac+c'b'a'}$
v_{bca}	v_{abc}	$v_{b_ta_tc_t}$	$v_{cba+b'a'c'}$
v_{abc}	v_{bca}	$v_{c_tb_ta_t}$	$v_{cba+a'c'b'}$
v_{bca}	v_{abc}	$v_{c_tb_ta_t}$	$v_{acb+c'b'a'}$

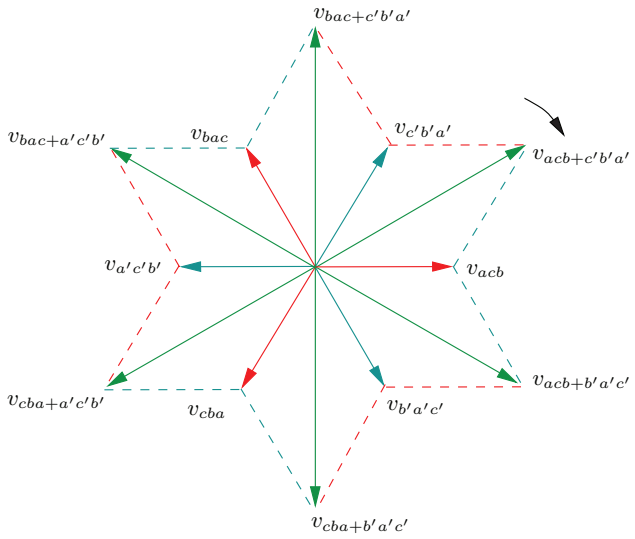

Figure 2.9: Output vector from clockwise rotating vectors

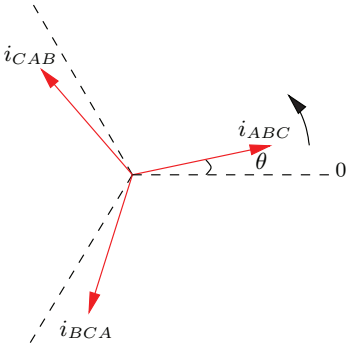

Figure 2.10: Anti-clockwise reference vectors at input

2.5 Input power factor control

Fig. 2.10 shows the anti-clockwise rotating current vectors. The anti-clockwise reference current vectors and the 180° phase shifted current vectors are shown together in fig. 2.11.

Similarly, fig. 2.12 shows the clockwise rotating current vectors. The clockwise

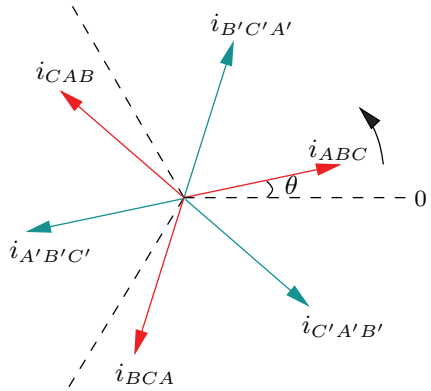

Figure 2.11: Anti-clockwise reference vectors and the opposite vectors at input

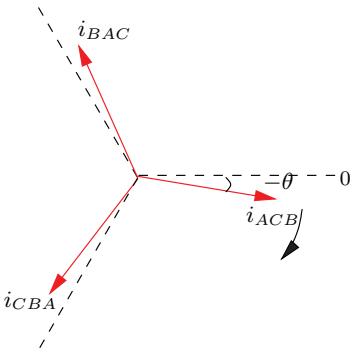

Figure 2.12: Clockwise reference vectors at input

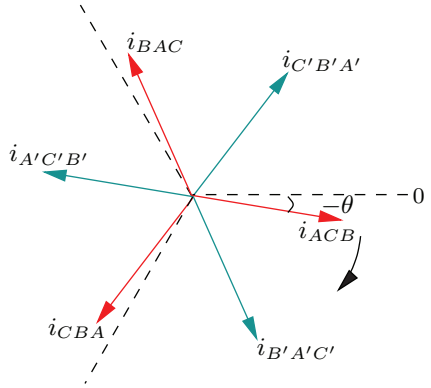

Figure 2.13: Clockwise reference vectors and the opposite vectors at input

reference current vectors and the 180° phase shifted current vectors are shown together in fig. 2.13.

Table 2.3 shows the input current, with respect to the transformer current, that flows because of the switching of MC1 and MC2. The current flowing in the transformer winding is assumed as I_{a_t}, I_{b_t} and I_{c_t}. As the input current is the difference of currents in two phases of the transformer windings, it can be represented as the addition of current vector $I_{a_tb_tc_t}$ and 180° phase shifted current vector of $I_{c_ta_tb_t}$ or current vector $I_{c_ta_tb_t}$ and 180° phase shifted current vector of $I_{a_tb_tc_t}$.

Table 2.4 shows the transformer currents, with respect to the output currents I_A, I_B and I_C, for anti-clockwise and clockwise switching of matrix converter MC3. The current space vectors formed at the input of the PET because of anti-clockwise switching of MC3 are listed in table 2.5. Fig. 2.14 shows the corresponding vector diagram. Similarly, the current space vectors formed at the input of the PET because of clockwise switching of MC3 are listed in table 2.6. Fig. 2.15 shows the corresponding vector diagram.

Table 2.3: Input currents

MC1	MC2	I_a	I_b	I_c
v_{abc}	v_{bca}	$I_{a_t} - I_{c_t}$	$I_{b_t} - I_{a_t}$	$I_{c_t} - I_{b_t}$
v_{bca}	v_{abc}	$I_{c_t} - I_{a_t}$	$I_{a_t} - I_{b_t}$	$I_{b_t} - I_{c_t}$

Suppose the output voltages of the PET are given by

$$\begin{aligned} v_A &= V_{om}cos(\omega_o t) \\ v_B &= V_{om}cos(\omega_o t - \frac{2\pi}{3}) \\ v_C &= V_{om}cos(\omega_o t + \frac{2\pi}{3}) \end{aligned} \tag{2.3}$$

where V_{om} and ω_o are amplitude of output voltage and output frequency respectively. Corresponding to equations 2.3 the output voltage space vector is given by

$$v_{ABC} = V_{ABC}e^{j\omega_o t} \tag{2.4}$$

Table 2.4: Transformer currents

MC3	I_{a_t}	I_{b_t}	I_{c_t}
$v_{a_tb_tc_t}$	I_A	I_B	I_C
$v_{b_tc_ta_t}$	I_C	I_A	I_B
$v_{c_ta_tb_t}$	I_B	I_C	I_A
$v_{a_tc_tb_t}$	I_A	I_C	I_B
$v_{b_ta_tc_t}$	I_B	I_A	I_C
$v_{c_tb_ta_t}$	I_C	I_B	I_A

Table 2.5: Input for anti-clockwise rotating vectors

MC1	MC2	MC3	Input
v_{abc}	v_{bca}	$v_{a_tb_tc_t}$	$i_{ABC+C'A'B'}$
v_{bca}	v_{abc}	$v_{a_tb_tc_t}$	$i_{CAB+A'B'C'}$
v_{abc}	v_{bca}	$v_{c_ta_tb_t}$	$i_{BCA+A'B'C'}$
v_{bca}	v_{abc}	$v_{c_ta_tb_t}$	$i_{ABC+B'C'A'}$
v_{abc}	v_{bca}	$v_{b_tc_ta_t}$	$i_{CAB+B'C'A'}$
v_{bca}	v_{abc}	$v_{b_tc_ta_t}$	$i_{BCA+C'A'B'}$

Table 2.6: Input for clockwise rotating vectors

MC1	MC2	MC3	Input
v_{abc}	v_{bca}	$v_{a_tc_tb_t}$	$i_{ACB+B'A'C'}$
v_{bca}	v_{abc}	$v_{a_tc_tb_t}$	$i_{BAC+A'C'B'}$
v_{abc}	v_{bca}	$v_{b_ta_tc_t}$	$i_{BAC+C'B'A'}$
v_{bca}	v_{abc}	$v_{b_ta_tc_t}$	$i_{CBA+B'A'C'}$
v_{abc}	v_{bca}	$v_{c_tb_ta_t}$	$i_{CBA+A'C'B'}$
v_{bca}	v_{abc}	$v_{c_tb_ta_t}$	$i_{ACB+C'B'A'}$

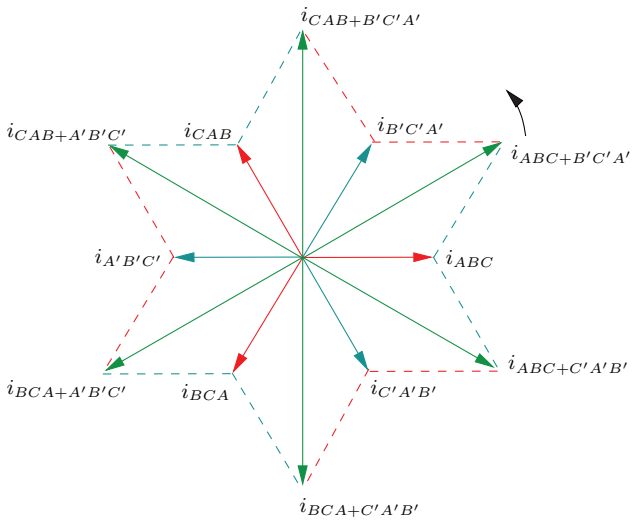

Figure 2.14: Input current vector from anticlockwise rotating vectors

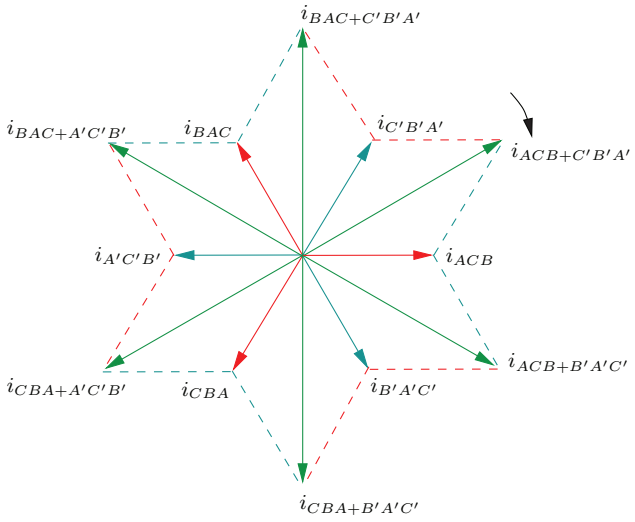

Figure 2.15: Input current vector from clockwise rotating vectors

where, V_{ABC} is the magnitude of the output voltage space vector. The exact magnitudes of space vectors have been neglected in the following analysis for simplicity. Similarly, the input voltage space vector can be written as

$$v_{abc} = V_{abc}e^{j\omega_i t} \tag{2.5}$$

The synthesis of average output voltage space vector from input voltage space vector, using anti-clockwise rotating vectors, can be represented by a space vector equation

$$V_{ABC}e^{j\omega_o t} = V_{abc}e^{j\omega_i t}R_{SVM_{anti}}e^{j(\omega_o-\omega_i)t} \tag{2.6}$$

where $R_{SVM_{anti}}$ is the magnitude of the average space vector modulated(SVM) vector. Please note that the $R_{SVM_{anti}}$ is equivalent to the voltage transfer ratio. The output currents can be given by

$$\begin{aligned} i_{oA} &= I_{om}cos(\omega_o t - \phi) \\ i_{oB} &= I_{om}cos(\omega_o t - \phi - \frac{2\pi}{3}) \\ i_{oC} &= I_{om}cos(\omega_o t - \phi + \frac{2\pi}{3}) \end{aligned} \tag{2.7}$$

where I_{om} is the amplitude of output current. Corresponding to equations 2.7 the output voltage space vector is given by

$$i_{ABC} = I_{ABC}e^{j(\omega_o t-\phi)} \tag{2.8}$$

where I_{ABC} is the magnitude of the output current space vector and ϕ is the load power factor angle. Using equation 2.6 and 2.8, the average input current space vector is given by

$$\begin{aligned} i_{abc} &= I_{ABC}e^{j(\omega_o t-\phi)}R_{SVM_{anti}}e^{-j(\omega_o-\omega_i)t} \\ &= I_{abc}e^{j(\omega_i t-\phi)} \end{aligned} \tag{2.9}$$

where I_{abc} is the magnitude of the input current space vector. From equation 2.9 it can be seen that when the output voltage is synthesized using anti-clockwise rotating vectors, the input power factor is the same as the load power factor i.e. a lagging power factor.

Using clockwise rotating vectors, the average output voltage space vector can be written as

$$V_{ABC}e^{j\omega_o t} = V_{abc}e^{-j\omega_i t}R_{SVM_{clock}}e^{j(\omega_o+\omega_i)t} \tag{2.10}$$

where $R_{SVM_{clock}}$ is the voltage transfer ratio. Using equation 2.10 and 2.8, the average input current space vector is given by

$$\begin{aligned} i_{abc} &= I_{ABC}e^{j(\omega_o t-\phi)}R_{SVM_{clock}}e^{-j(\omega_o+\omega_i)t} \\ &= I_{abc}e^{-j(\omega_i t+\phi)} \end{aligned} \tag{2.11}$$

Thus, using clockwise rotating vectors, the input power factor is the equal and opposite of the load power factor i.e. a leading power factor. Input power factor can be controlled by using both anti-clockwise rotating vectors and clockwise rotating vectors. This can be explained with fig. 2.16 and fig. 2.17. Suppose the input power factor angle to be achieved with power factor control is ρ. For one switching time period, the output voltage vector with angle $\theta-\rho$ is synthesized using anti-clockwise rotating vectors, where $\theta = \omega_o t$. For the next switching time period, the output voltage vector with angle $\theta+\rho$ is synthesized using clockwise rotating vectors. Thus the average angle over the two switching time periods is zero for the output voltage vector.

For the anti-clockwise rotating vector, the angle of input current vector obtained is $\theta+\phi+\rho$ and for clockwise rotating vector, the angle of input current vector obtained is $\theta-\phi+\rho$, here $\theta = \omega_i t$. Therefore, the average input power factor angle is controlled to ρ and is independent of load power factor angle.

2.6 Simulation results

The above described topology has been simulated in MATLAB/ SIMULINK environment for a supply voltage of $120V$, $60Hz$ and RL load of 10Ω and $10mH$. A 1:1 high frequency transformer with zero leakage inductance has been used. Fig. 2.18 shows the simulation results for output voltage with voltage transfer ratio 1.0 and output frequency of $50Hz$ using anti-clockwise rotating vectors. The simulation results show the output voltage, output current, the supply voltage and supply current for one of the phases. To determine the load power factor, the average output voltage is also shown as filtered voltage. It can be seen in fig. 2.18 that the input current power factor is equal

to the load power factor. Fig. 2.19 shows the simulation results the for output voltage with voltage transfer ratio 1.0 and output frequency of $50Hz$ using clockwise rotating vectors. In fig. 2.19 the input current power factor angle is leading by the same value as the load power factor. Fig. 2.20 shows the simulation results for the output voltage with voltage transfer ratio 1.0 and output frequency of $50Hz$ using both anti-clockwise rotating and clockwise rotating vectors for unity power factor.

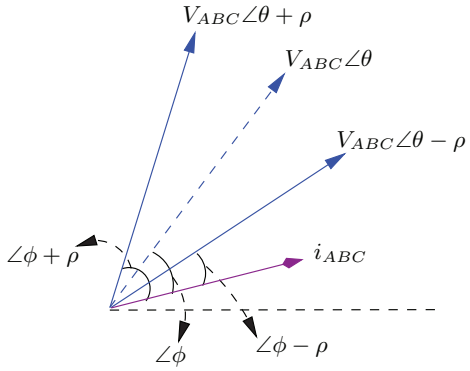

Figure 2.16: Average voltage vector using both anti-clockwise and clockwise rotating vectors

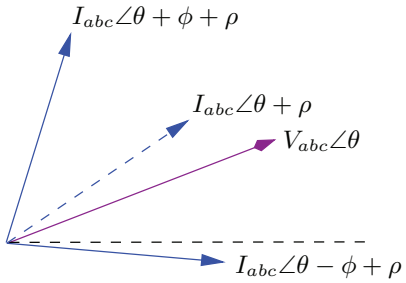

Figure 2.17: Average input current vector using both anti-clockwise and clockwise rotating vectors

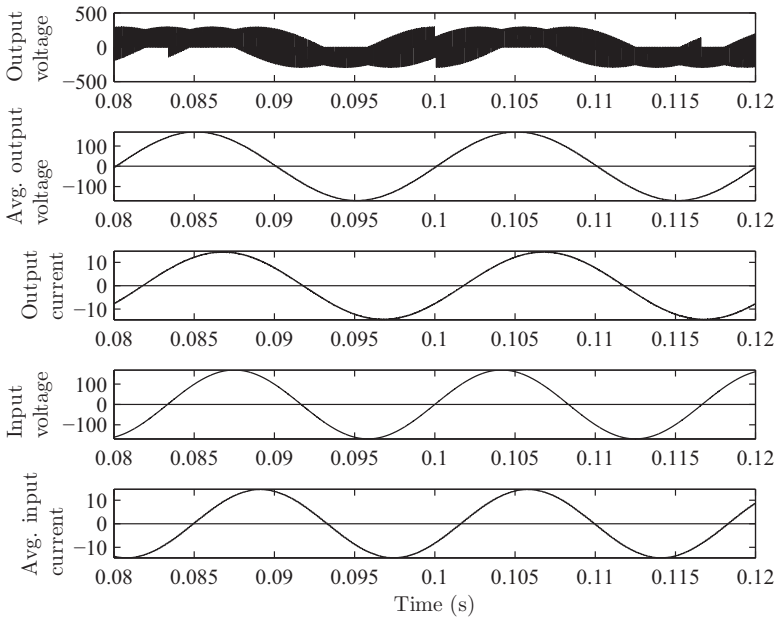

Figure 2.18: 50 Hz output voltage for anti-clockwise vector rotation

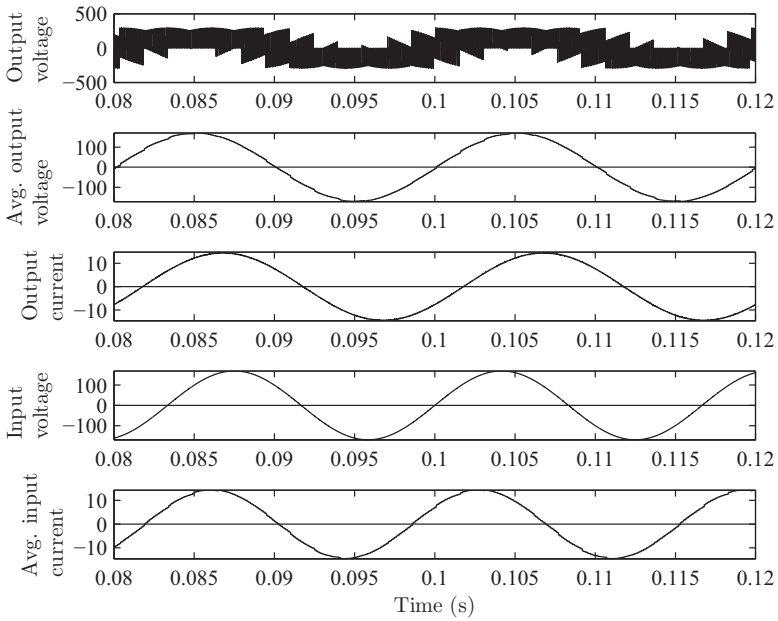

Figure 2.19: 50 Hz output voltage for clockwise vector rotation

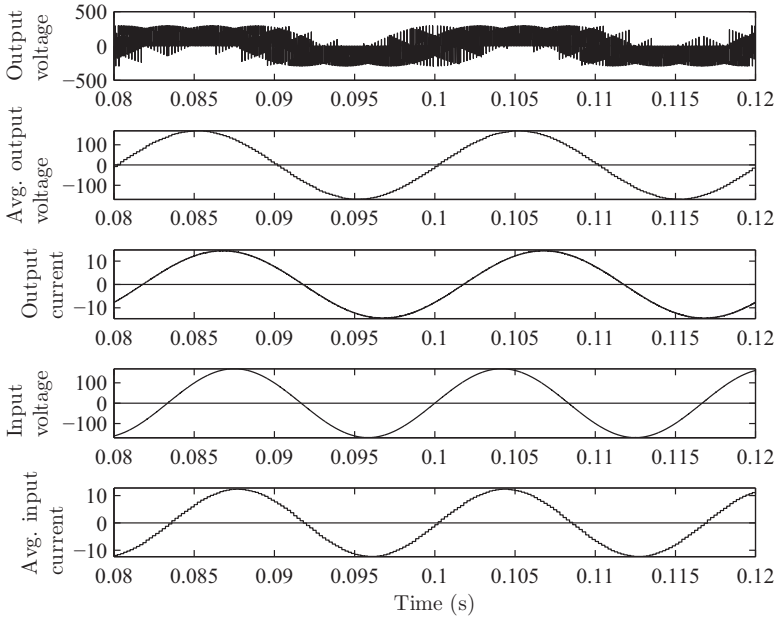

Figure 2.20: 50 Hz output voltage for power factor control

2.7 Conclusion

A matrix converter fed PET with open ended primary is described. Space vector pulse width modulation is used for the control of PET. Controllable output voltage and frequency, voltage transfer ratio of 1.5, controllable input power factor, bi-directional power flow, zero common mode voltage and absence of bulky storage capacitors are the salient features of the described PET. Open ended primary with one MC at each end leads to voltage transfer ratio of 1.5. Rotating space vectors are used to obtain zero common mode voltage. Input power factor is controlled by use of both clockwise and anti-clockwise rotating vectors.

Chapter 3

Problem of leakage inductance

The non-idealities such as leakage inductance of the transformer have a significant effect on the performance of PET. The effect of leakage inductance on the regulation of the output voltage of PET is studied in this chapter. The MC based PET with open ended primary, described in the previous chapter; with a clamp circuit connected at secondary terminals is used for the study. The major aspects studied are the change in output voltage of the PET with switching frequency and leakage inductance. The simulation study has been carried out in SIMULINK and the results have been presented.

3.1 Effect of Leakage

The problem of leakage inductance in HF transformers can be explained as follows. As explained in chapter 2, a high frequency switched voltage appears across the transformer. Simulation results of the volatge across primary and secondary winding of the transformer is shown in fig. 3.2. Since the three matrix converters are switched simultaneously, a high frequency switched current flows through the transformer primary and secondary. The current flowing through the secondary of the transformer is shown in fig. 3.3. A practical transformer has a definite leakage inductance. Therefore, the current cannot change instantaneously in the transformer.

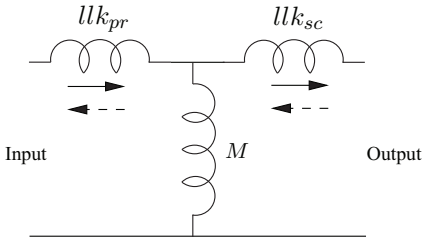

Figure 3.1: Transfomer with leakage inductance

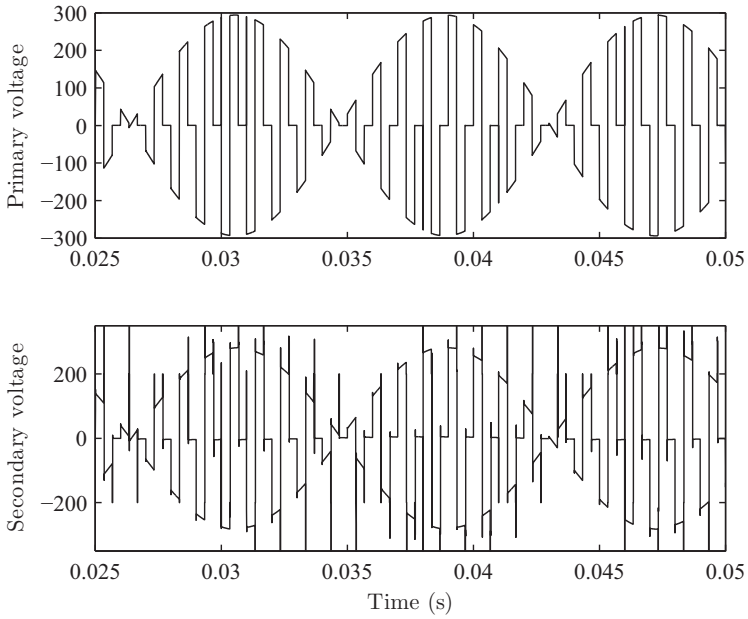

Figure 3.2: Primary and secondary voltage of transformer

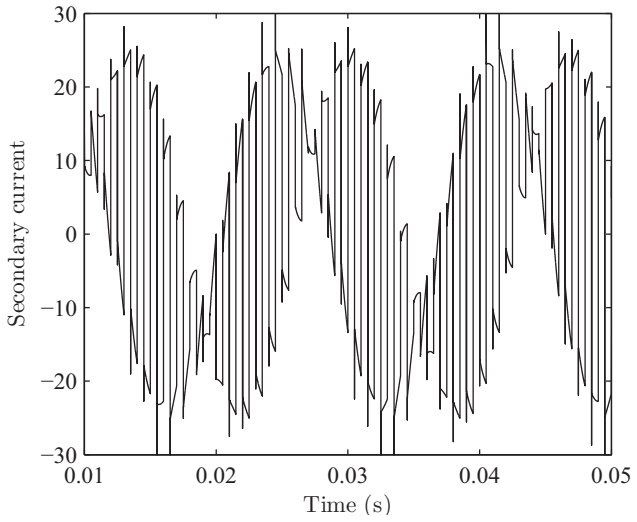

Figure 3.3: Current flowing through secondary of the transformer

The leakage inductance in the transformers creates a commutation delay in the primary side to secondary side voltage transfer (fig. 3.1). At high frequency, the transformer leakage impedance is proportional to $f(llk_{pr} + n^2 llk_{sc})$, where f is frequency of excitation, llk_{pr}, llk_{sc} are primary leakage and secondary leakage inductances respectively and n is the primary to secondary turns ratio. The input voltage to the transformer is a square wave in the switching interval. There is a finite commutation period, during which the direction of current changes from positive (solid) to negative (dotted) as shown in fig. 3.1. During the commutation interval, entire input voltage drops across the leakage. The difference in the load current and secondary leakage current flows to the clamp circuit, thus producing power loss.

3.2 Simulation Results

The overall scheme is simulated in a MATLAB/SIMULINK environment and the output regulation at transformer primary and secondary is observed. The topology shown in fig. 2.1 is simulated for $120V$, $60Hz$ source voltage, 1:1 transformer with magnetizing inductance $10mH$ and 2% leakage inductance, RL load of 10Ω and $10mH$, switching frequency $5kHz$, voltage transfer ratio of 1.5 and output voltage frequency $60Hz$. Fig.

3.4 shows the effect of leakage on the output of MC3. The secondary voltage is distorted during the positive to negative transition. During this period the secondary current flows through the clamp circuit. Fig. 3.5 shows this effect. It may be noted that while the primary voltage has transited, the secondary voltage is clamped to the clamp voltage. There is finite clamp current during transition and the input current in the primary is ramping up during the same period. As the value of leakage inductance is increased, the effect of leakage also increases, affecting the magnitude of the output voltage. Also, as the switching frequency is increased, the leakage reactance and frequency of occurrence of commutation delay period increases, affecting the magnitude of output voltage. The simulation is run for different values of switching frequency and leakage inductance. Fig. 3.6 shows the change in regulation with increase in leakage inductance of transformer for $5kHz$ switching frequency. And fig. 3.7 shows the change in regulation with increase in switching frequency for 2% leakage inductance. As the switching frequency of transformer or the leakage is increased, the secondary voltage drops.

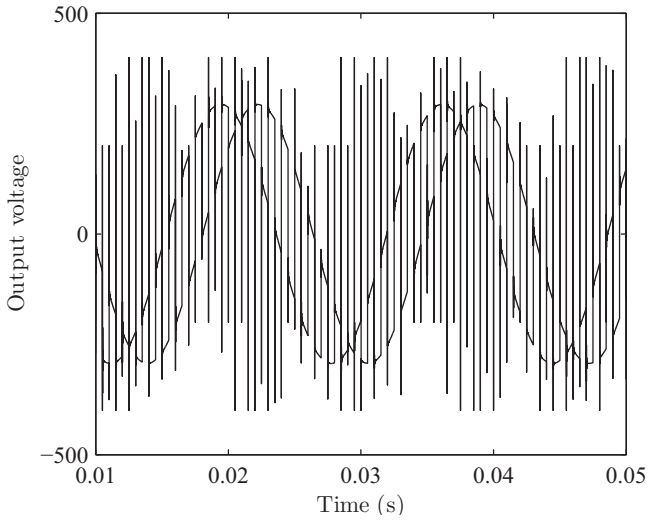

Figure 3.4: Output voltage

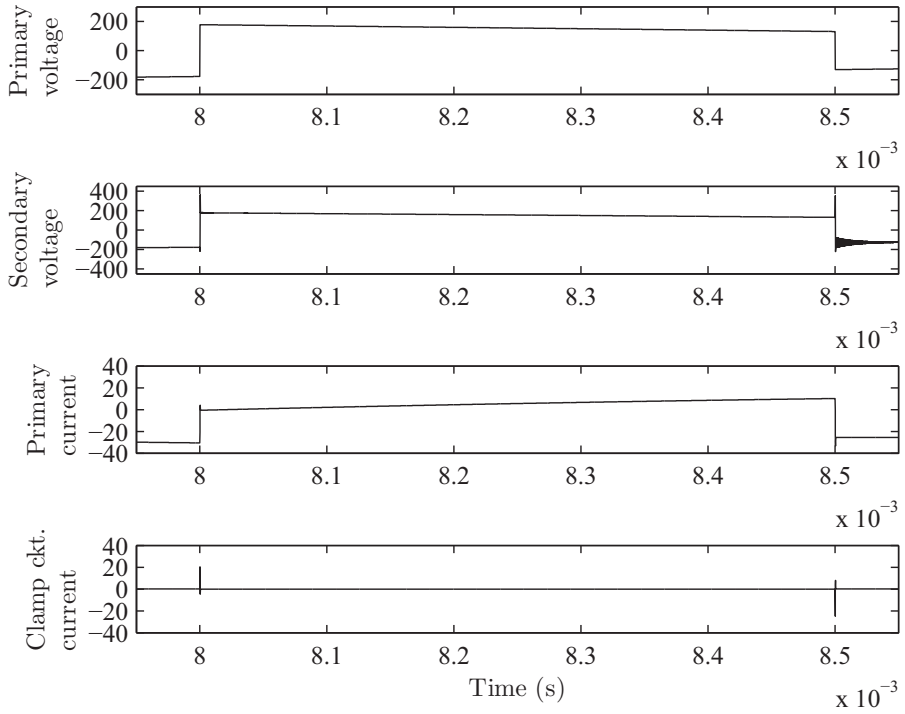

Figure 3.5: Primary volatge, secondary voltage, primary current, clamp circuit current

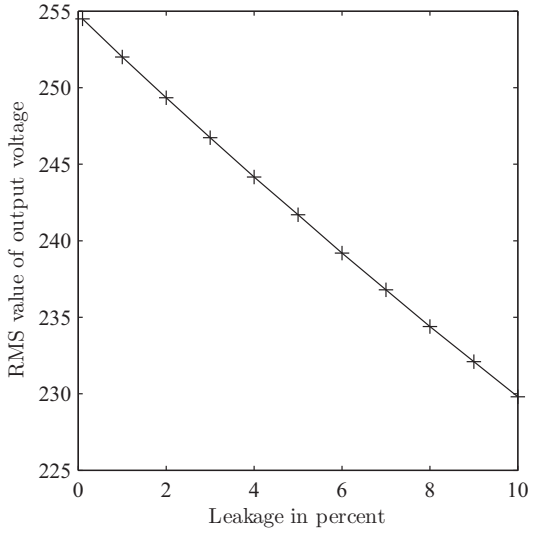

Figure 3.6: Decrease in output voltage with increase in leakage

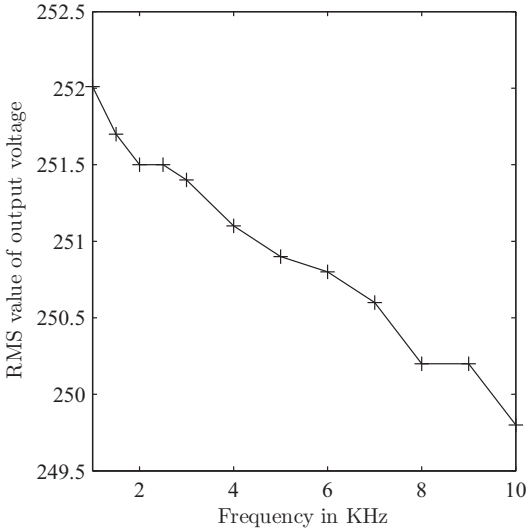

Figure 3.7: Decrease in output voltage with increase in frequency

3.3 Conclusion

The current in the leakage inductance of a transformer cannot change instantaneously. An alternative path can be provided during commutation time by clamp circuit. Use of clamp circuit reduces the voltage regulation and efficiency. The output voltage drops with increase in leakage inductance or switching frequency. Thus, the leakage inductance of high frequency transformer plays a significant role in the output voltage regulation and overall efficiency of the system. Hence, it is desirable to design high frequency transformers with minimum leakage inductance.

Note: This chapter is reproduced from my IEEE publication [30]. I acknowledge the contributions of Krushna K. Mohapatra as co-author in this publication.

Chapter 4

Source Based Commutation

Leakage inductance is one of the important factors which affect the performance of the converter proposed in [21]. Use of clamp circuit for current commutation in leakage inductance requires an energy recovery circuit. This chapter proposes a source based commutation method by which use of clamp circuit is minimized. The proposed source based commutation is simulated in SIMULINK.

4.1 Principle of source based commutation

The basic principle of source based commutation can be explained with the help of fig. 4.1, fig. 4.2 and fig. 4.3. Fig. 4.1 shows a two phase to single phase matrix converter with two controllable input voltages $V1$ and $V2$. The source inductance L_{lk} represents the leakage inductance of the high frequency transformer. Fig. 4.2 shows the state diagram for the source based commutation from SW1 to SW2. For the direction of current, as shown in fig. 4.1, IGBT SA1 was conducting. When a commutation is required from SW1 to SW2, both IGBTs SA1 and SA2 are gated i.e. the matrix converter goes into the 1010 state as shown in fig. 4.2. Now, if $V2 > V1$ then commutation of current from SA1 to SA2 will occur. The time of commutation is decided by the value of leakage inductance, the value of current and difference between $V2$ and $V1$. So, for source based commutation the correct voltage inequality has to be provided by $V1$ and $V2$.

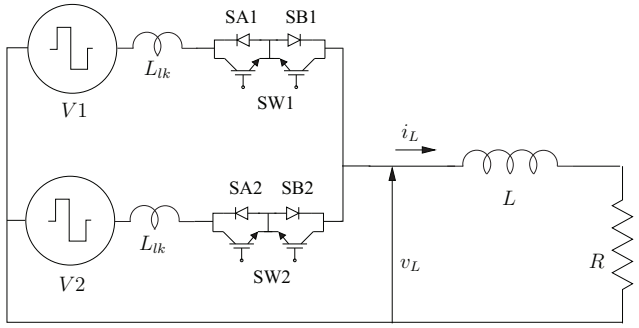

Figure 4.1: Two phase to single phase matrix converter with source inductance

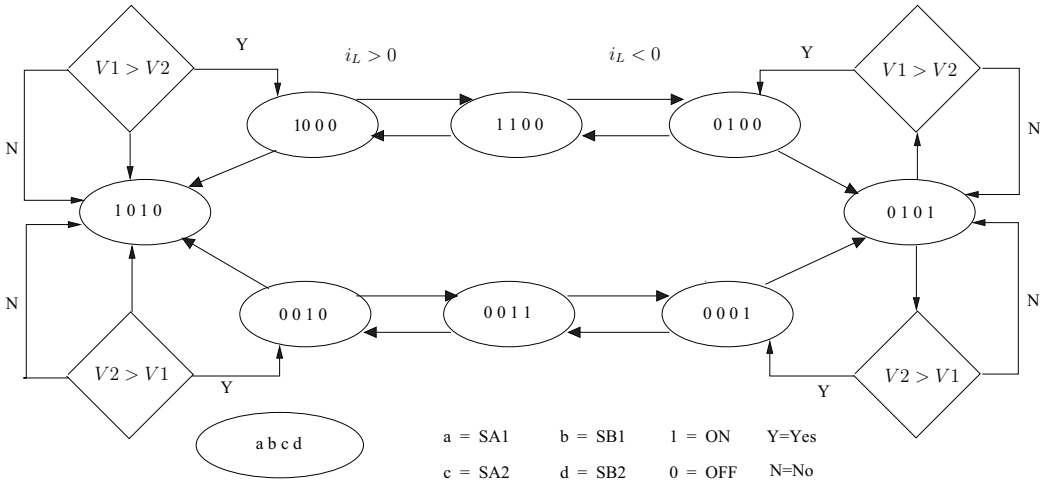

Figure 4.2: State diagram for source based commutation of a two phase to single phase matrix converter

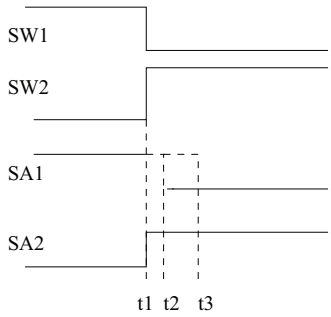

Figure 4.3: Commutation from SW1 to SW2

As shown in fig. 4.2, whenever a commutation is required from SW1 to SW2, the matrix converter goes into 1010 or 0101 states depending on the direction of the current. At this point the voltage inequality condition provided by $V1$ and $V2$ is checked. fig. 4.3 shows the details of switching when a commutation from SW1 to SW2 is required and the direction of current is as shown in fig. 4.1. At time instant $t1$, SA2 is turned ON. At $t1$ if $V2 > V1$ then a timer is activated and SA1 is turned OFF after the timer period, shown as time instant $t2$ in fig. 4.3. But, at $t1$ if $V2 < V1$ then SA1 remains ON till $V1$ and $V2$ change such that $V2 > V1$. When $V2 > V1$ is obtained, then a timer is activated and SA2 turns OFF at time instant $t3$. The timer provides a pulse suitable for commutation. During the interval the timer is ON, the matrix converter remains in the 1010 or 0101 state. After the commutation is over, the matrix converter is switched to the final state.

The principle explained above can be extended to a three phase to three phase matrix converter as follows. Table 4.1 shows the voltage inequality conditions required for source based commutation, depending on the directions of current in a three phase balanced load and the change of switching in MC3. As shown in fig. 4.4, a three phase supply can be divided into six zones based on the voltage inequality satisfied by that zone. Therefore, at any time instant one out of the six voltage inequalities are provided by MC1 and MC2.

Table 4.1: Voltage inequalities for source based commutation

MC3 switching	i_{LA}	i_{LB}	i_{LC}	Voltage inequality required
$v_{a_tb_tc_t}$ to $v_{b_tc_ta_t}$	+	+	-	$V_c > V_b > V_a$
	+	-	+	$V_b > V_a > V_c$
	-	+	+	$V_a > V_c > V_b$
	-	-	+	$V_a > V_b > V_c$
	-	+	-	$V_c > V_a > V_b$
	+	-	-	$V_b > V_c > V_a$
$v_{b_tc_ta_t}$ to $v_{c_ta_tb_t}$	+	+	-	$V_a > V_c > V_b$
	+	-	+	$V_c > V_b > V_a$
	-	+	+	$V_b > V_a > V_c$
	-	-	+	$V_b > V_c > V_a$
	-	+	-	$V_a > V_b > V_c$
	+	-	-	$V_c > V_a > V_b$
$v_{c_ta_tb_t}$ to $v_{a_tb_tc_t}$	+	+	-	$V_b > V_a > V_c$
	+	-	+	$V_a > V_c > V_b$
	-	+	+	$V_c > V_b > V_a$
	-	-	+	$V_c > V_a > V_b$
	-	+	-	$V_b > V_c > V_a$
	+	-	-	$V_a > V_b > V_c$

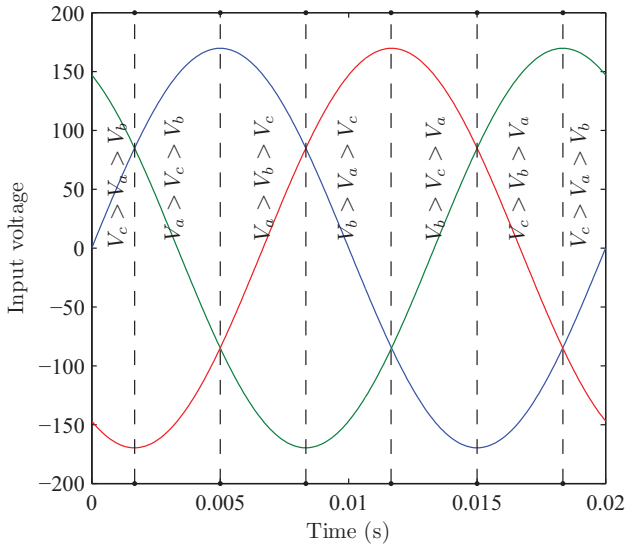

Figure 4.4: Six voltage inequality conditions in three sine waves

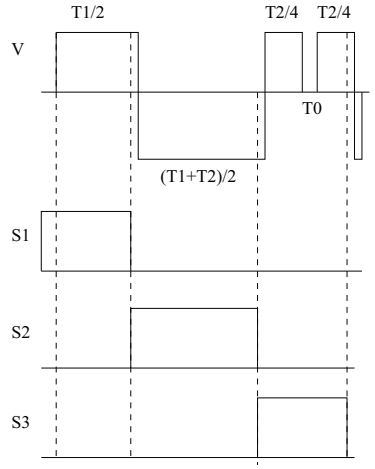

Figure 4.5: Voltage across one winding of transformer and the three modulation pulses of MC3

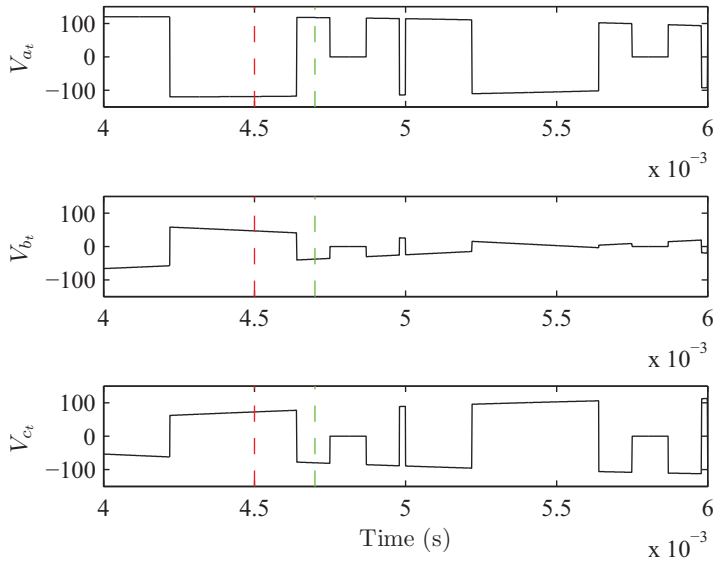

Figure 4.6: Voltage across primary winding of transformer

As explained in [30] and [21], the high frequency voltage obtained from MC1 and MC2 is such that the volt second balance is maintained in the transformer. Therefore, alternating voltages with 180^o phase shifts are applied in one switching time period. This indicates that if at any time instant a given voltage inequality was satisfied, the opposite voltage inequality is satisfied after MC1 and MC2 are switched. For example, in fig. 4.6 at time $0.0045s$ (shown by red dashed line), $V_c > V_b > V_a$. After switching MC1 and MC2, at time $0.0047s$ (shown by green dashed line), $V_a > V_b > V_c$ i.e. the opposite voltage inequality is satisfied. Therefore, a source based commutation can be obtained by shifting the switching time instants of MC1 and MC2 ahead of the switching time instants of MC3 as shown in fig. 4.5.

The commutation in three phase to three phase matrix converter can be explained with fig. 4.3, fig. 4.7, fig. 4.8, fig. 4.9 and fig. 4.10. Suppose the values of load currents i_{LA}, i_{LB} and i_{LC} before commutation i.e. before time instant $t1$, are $+5$, $+7$ and -12 respectively and a switching from v_{abc} to v_{bca} is required. This is shown in fig. 4.7. The switches which are not conducting before $t1$ are not shown in fig. 4.7 for clarity. The current in leakage inductances L_{lka}, L_{lkb} and L_{lkc} are $+5$, $+7$ and -12 respectively. At

time instant $t1$, S_{bA1}, S_{cB1}, S_{aC2} are turned ON. This is shown in fig. 4.8.

From table 4.1 the voltage inequality required for commutation is $V_c > V_b > V_a$. Suppose MC1 and MC2 provides a voltage inequality $V_b > V_c > V_a$, so out of the three required inequalities two inequalities $V_b > V_a$ and $V_c > V_a$ are available. Therefore, the diodes of S_{bA1} and S_{aC2} will get forward biased. So, the currents in S_{aA1} and S_{cC2} become zero after a commutation time interval. The diode of S_{cB1} remains reverse biased. Therefore, the current in S_{bB1} continues to be +7. The currents in leakage inductances L_{lka}, L_{lkb} and L_{lkc} change from +5, +7 and −12 to −12, +12 and 0 respectively. At time instant $t2$, S_{aA1} and S_{cC2} are switched OFF. This is shown in fig. 4.9.

After time $t2$, MC1 and MC2 are switched. So the voltage inequality provided by MC1 and MC2 becomes $V_a > V_c > V_b$. Now, the third inequality required for source based commutation $V_c > V_b$ is also satisfied. The diode of S_{cB1} gets forward biased. The current in S_{bB1} becomes zero after the commutation time interval. S_{bB1} is turned OFF at time instant $t3$. The currents in leakage inductances L_{lka}, L_{lkb} and L_{lkc} change from −12, +12 and 0 to −12, +5 and +7 respectively. This is shown in fig. 4.10.

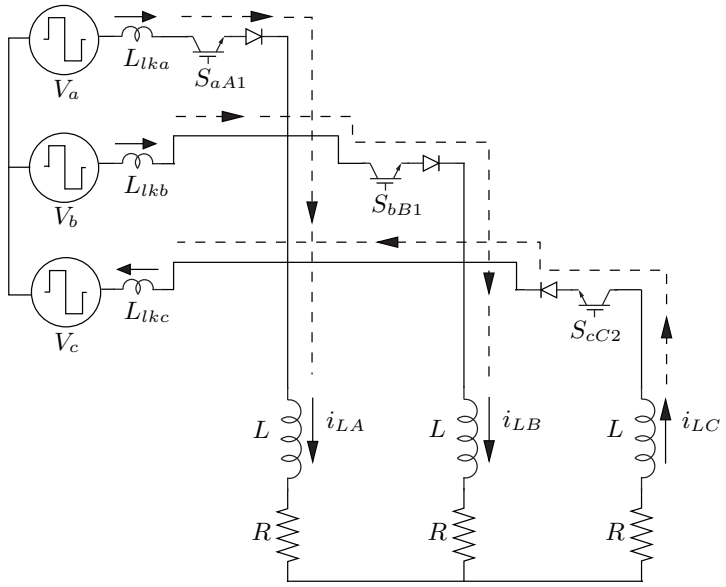

Figure 4.7: MC3 before time instant $t1$

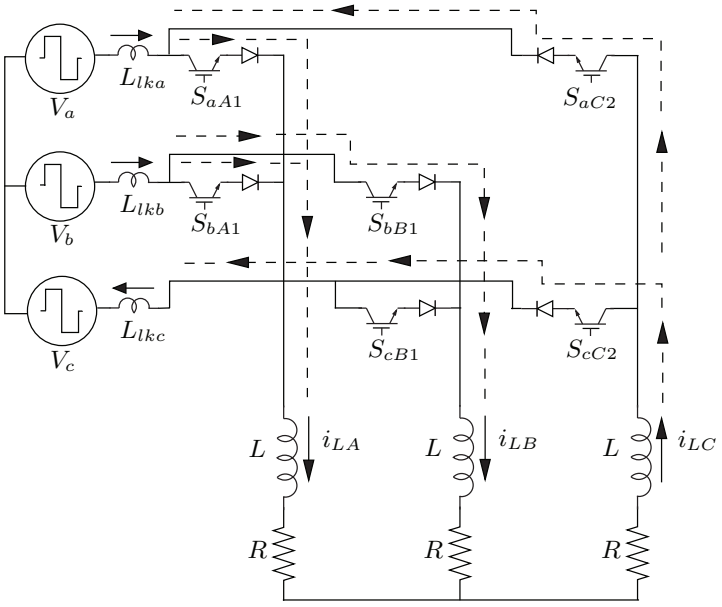

Figure 4.8: MC3 at time instant $t1$

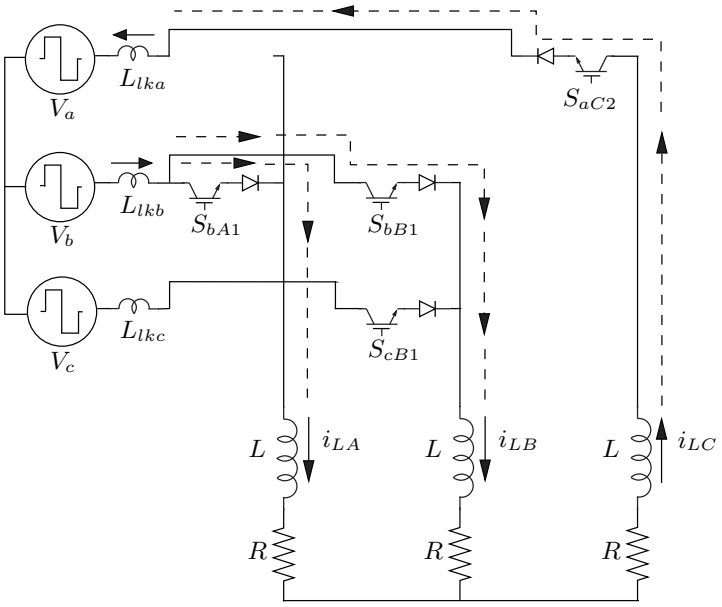

Figure 4.9: MC3 at time instant $t2$

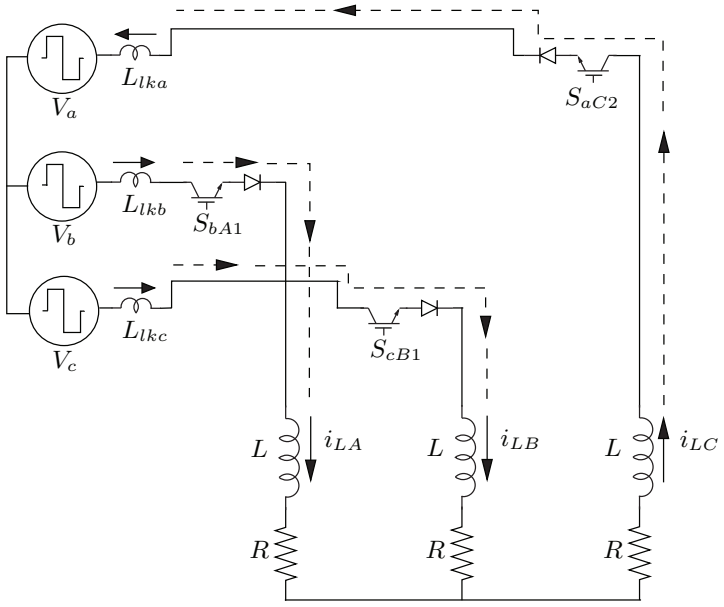

Figure 4.10: MC3 at time instant $t3$

Thus, a clamp circuit is not required for the current commutation in leakage inductance. When the difference in voltage between two phases becomes very small, the time interval needed for commutation becomes very large. At this stage the clamp circuit is used to achieve a fast commutation.

4.2 Simulation Results

The proposed source based commutation method has been verified by simulation in SIMULINK/MATLAB. Simulation results with source based commutation are shown in fig. 4.13 and fig. 4.14. Fig. 4.11 shows the voltage across the secondary winding of the high frequency transformer without source based commutation i.e. only using clamp circuit. Fig. 4.12 shows the voltage and current at output of MC3 using clamp circuit. In fig. 4.11, during every commutation interval the voltage across the secondary winding is the clamp circuit voltage, whereas in fig. 4.13, the clamp circuit voltage appears during commutation interval, only when the difference between input voltages of MC3 becomes very small. Comparison of fig. 4.11 and fig. 4.13 indicates a significant reduction in

power loss. Fig. 4.14 shows the voltage and current at output of MC3.

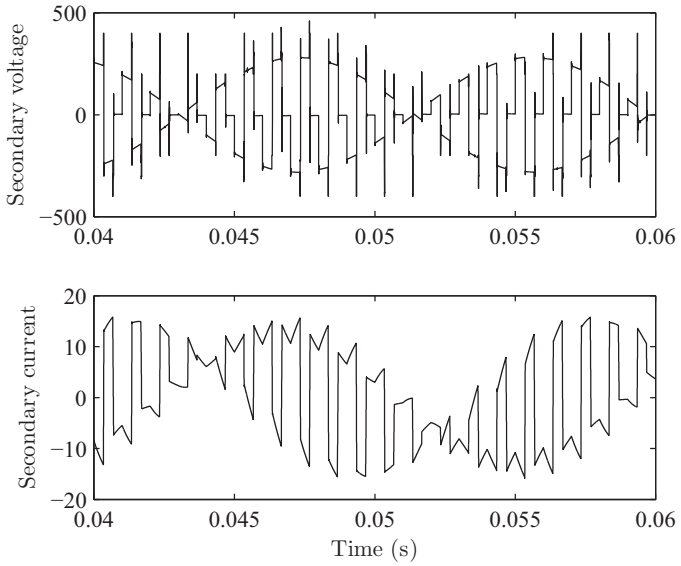

Figure 4.11: Voltage across secondary with clamp circuit

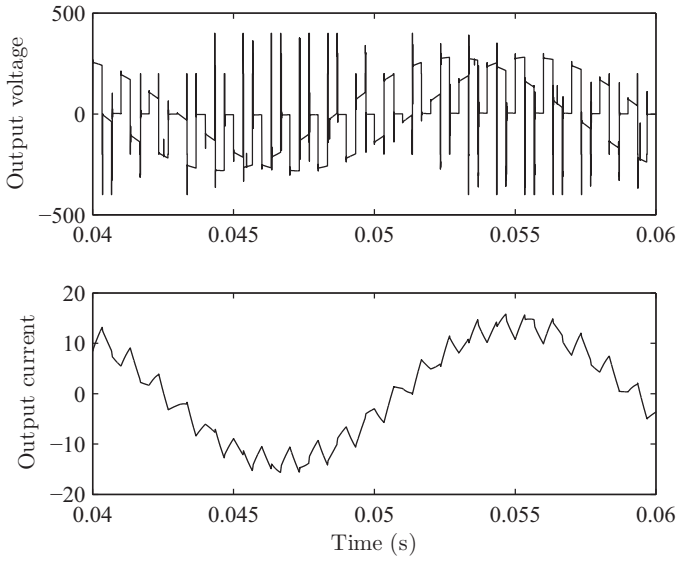

Figure 4.12: Output voltage and current with clamp circuit

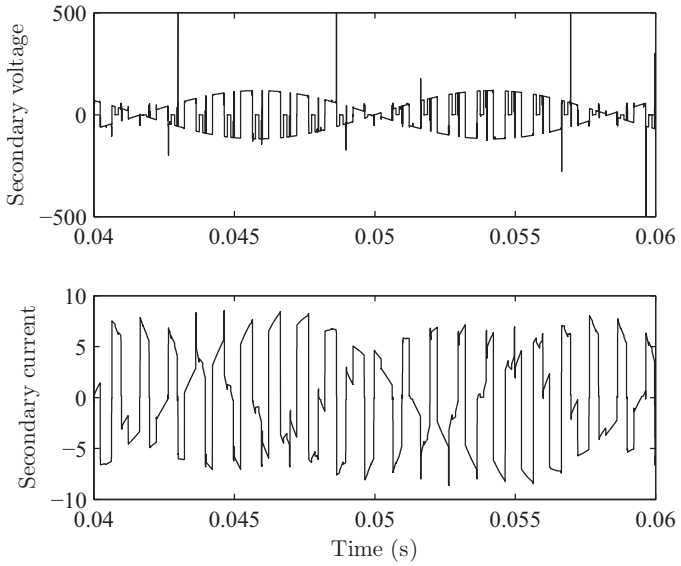

Figure 4.13: Voltage across secondary winding and current with source based commutation

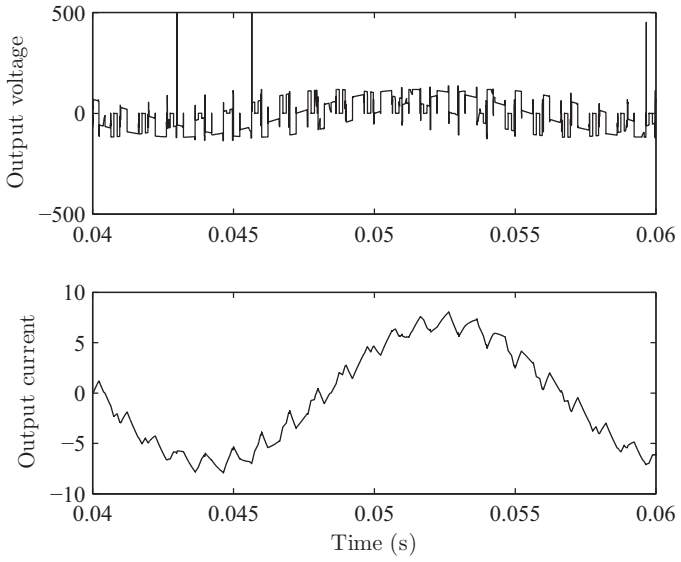

Figure 4.14: Output voltage and current with source based commutation

4.3 Conclusion

A source based commutation method for a high frequency transformer controlled through matrix converter is proposed. Current commutation in leakage inductance of high frequency transformer with clamp circuit leads to power loss and requires an energy recovery circuit. The source based commutation minimizes the use of clamp circuit significantly and thus increases overall efficiency of the system.

Note: This chapter is reproduced from my IEEE publication [31]. I acknowledge the contributions of Krushna K. Mohapatra and Kaushik Basu as co-authors in this publication.

Chapter 5

Sinusoidal input output three phase HF transformer

This chapter proposes a matrix converter fed, sinusoidal input output high frequency transformer. As explained in chapter 3, current in the leakage inductance of the transformer, cannot change instantaneously, current commutation is needed. The current in leakage inductance is commutated either by using clamp circuits or by source based commutation. The switching frequency is limited by the value of leakage inductance in both these methods.

With increase in switching frequency size of high frequency transformers reduce. The core of high frequency transformers are usually made with nanocrystaline materials. These nanocrystaline materials are capable of operating at very high frequencies with low core losses [3]. With the advancement in semiconductor technology, SiC devices are also available which can operate the power converters at high frequencies with low switching losses [27, 32–35]. Therefore, switching frequency is only limited by the value of leakage inductance.

The switching frequency of power electronic transformer, proposed in this chapter, is independent of the value of leakage inductance. The transformer sees sinusoidal voltages and currents, at high frequency, on both primary side and secondary side. This is achieved by low pass filters on both primary side and secondary side of the transformer.

5.1 Circuit description and basic principle

The proposed topology is shown in fig. 5.1. The supply voltage at $60Hz$ is converted to high frequency switched voltages by matrix converter MC1. The three output voltages of MC1, V_{sw-a}, V_{sw-b}, V_{sw-c} are square wave voltages phase shifted by 120° at $20kHz$ and are shown in fig. 5.2. These voltages are filtered by three low pass filters, connected in delta, to the primary of the high frequency transformer. Because of filter action, three sinusoidal voltages, V_{sin-a}, V_{sin-b}, V_{sin-c}, phase shifted by 120° at $20kHz$, are obtained at the primary terminals of the high frequency transformer.

The secondary of the high frequency transformer is connected to three capacitors C_{fs}. The leakage inductance of the transformer and the capacitors C_{fs} form the secondary side low pass filter. The switching frequency harmonics present in the input current of the matrix converter, MC2, are filtered by the secondary side low pass filter. Therefore, the transformer sees sinusoidal currents I_{x-a}, I_{x-b}, I_{x-c}. Since V_{sin-a}, V_{sin-b}, V_{sin-c} and I_{x-a}, I_{x-b}, I_{x-c} are sinusoidal, V_{f-a}, V_{f-b}, V_{f-c} are also sinusoidal, and are phase shifted by 120° at $20kHz$. These 120° phase shifted voltages are finally converted to low frequency by the matrix converter MC2. MC2 works like a cycloconverter.

The low pass filter operation is based on the fourier series of a square wave voltage waveform. A square wave contains only odd harmonics. The low pass filter, filters the third and higher order harmonics. The frequency of sine wave voltages V_{sin-a}, V_{sin-b}, V_{sin-c} is equal to the switching frequency of MC1.

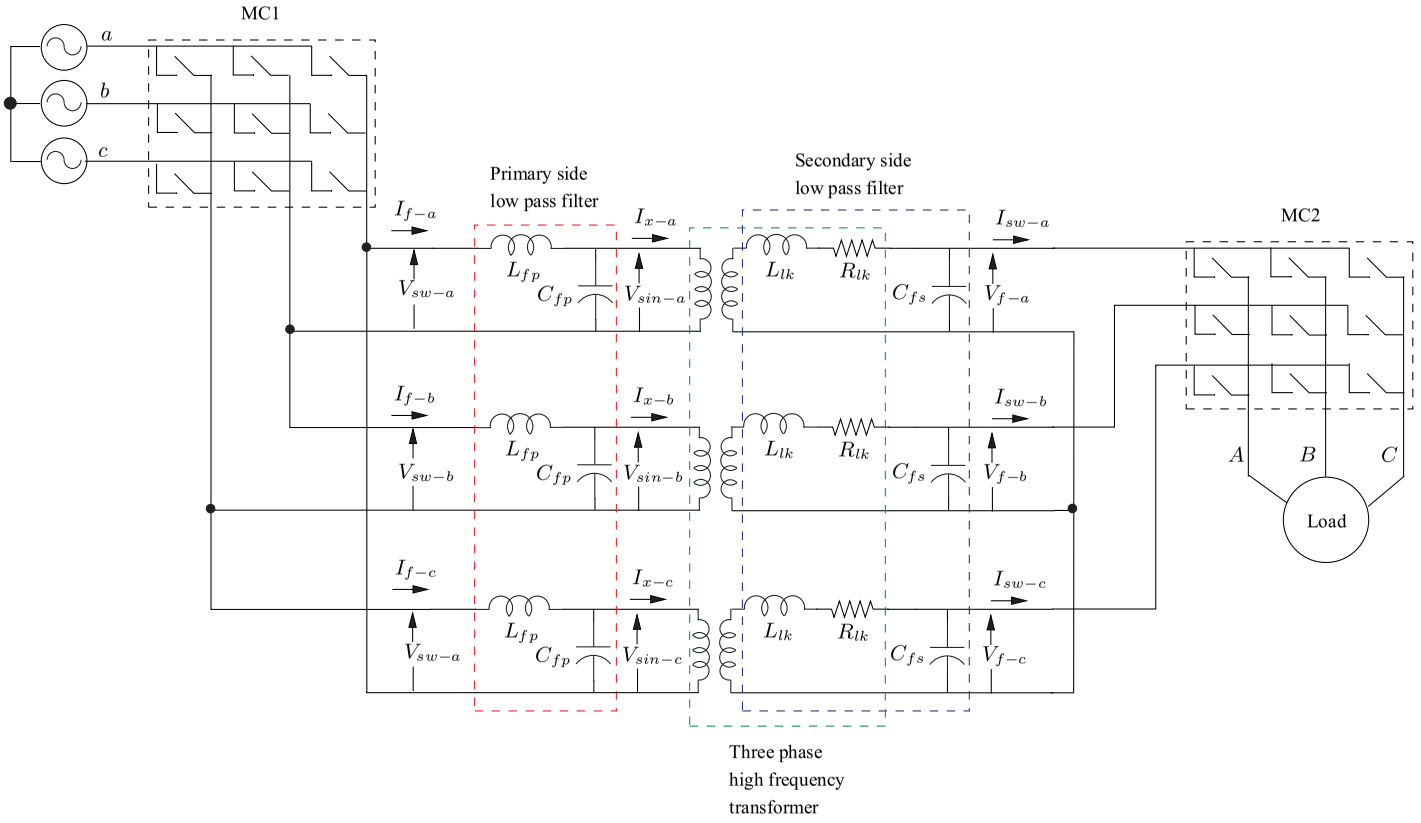

Figure 5.1: Matrix converter fed sinusoidal input output high frequency transformer

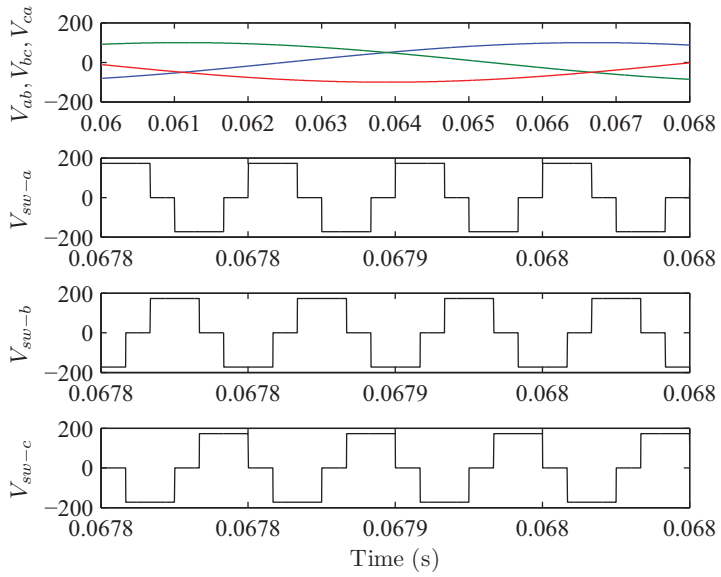

Figure 5.2: Supply voltage and output voltage of MC1

5.2 Filter design

Filter design is the most important part of the proposed converter. To design the filter a mathematical model is developed and is shown in figure 5.3. The mathematical model is based on the voltage and current equations for the two filters. In fig. 5.3, R_{fp} is the series resistance of the inductance L_{fp}.

As is seen in fig. 5.3, the design of the two filters is not independent of each other. Depending on the switching frequency, first the cut off frequencies of primary side filter and secondary side filter are decided. The two cut off frequencies need not be same. On secondary side value of C_{fs} is decided according to the value of transformer leakage inductance L_{lk} and cut off frequency. As is seen from the bode plots there will be amplification in current because of secondary side filter. So, accordingly the values of L_{fp} and C_{fp} are decided to compensate for the amplification in current and proper filtering of voltage.

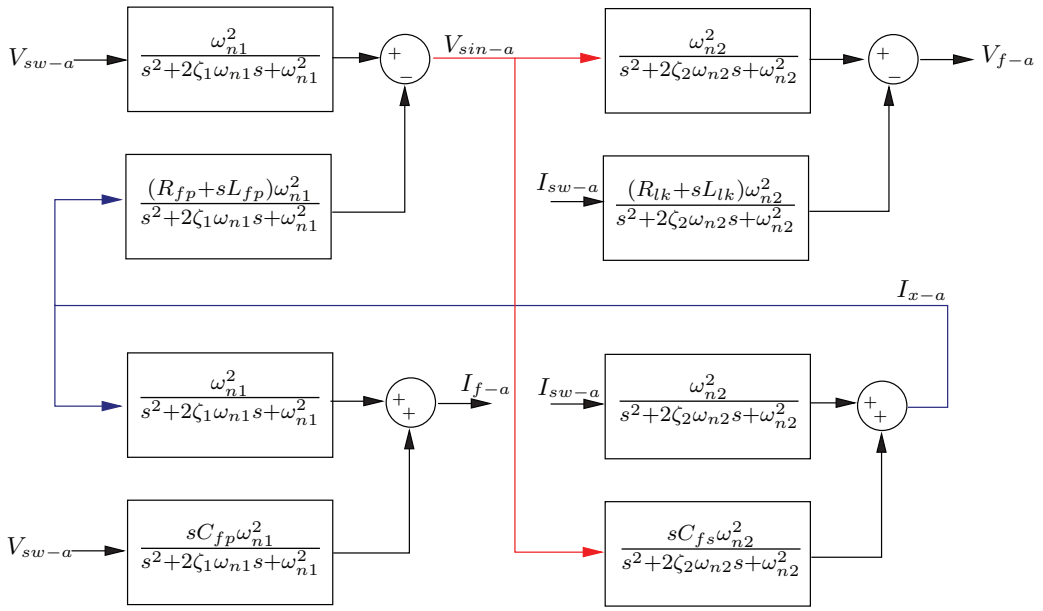

Figure 5.3: Mathematical model for filter design of the two low pass filters

5.3 Simulation results

The proposed topology has been simulated in MATLAB/ SIMULINK environment for a supply voltage of $100V$, $60Hz$ and RL load of 10Ω and $10mH$. The high frequency transformer used is $1200\backslash1200V$, $18kVA$, $20kHz$. The primary side values of filter inductance and capacitance are $200\mu H$ and $0.1\mu F$ respectively. The secondary side value of filter capacitance is $0.1\mu F$ and the value of leakage inductance of HF transformer is $100\mu H$. The simulation results are shown in figure 5.4, 5.5, 5.6, 5.7. Figure 5.4 shows the primary sides filter voltages and currents. Figure 5.5 shows the transformer voltages and currents. It can be seen from figure 5.5 that the transformer voltages and currents are sinusoids at $20kHz$. Figure 5.6 shows the input voltage and input current of the secondary side matrix converter. Figure 5.7 shows the load voltage and the load current.

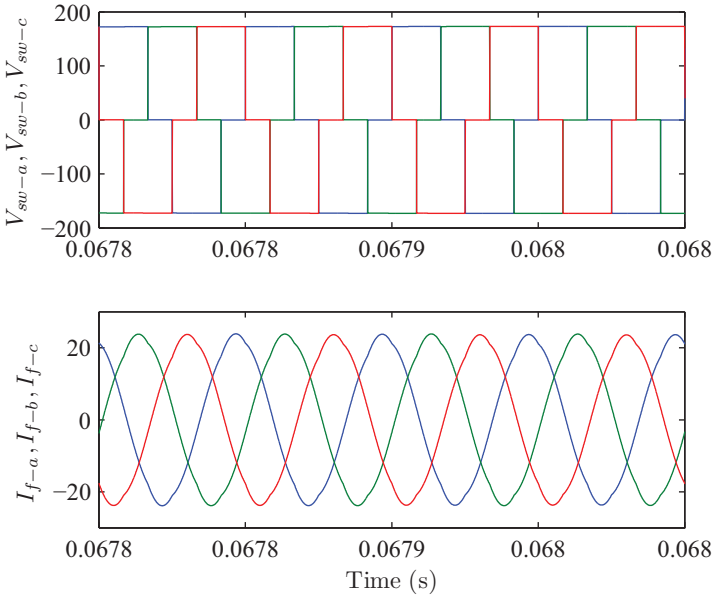

Figure 5.4: Primary side filter voltages and currents

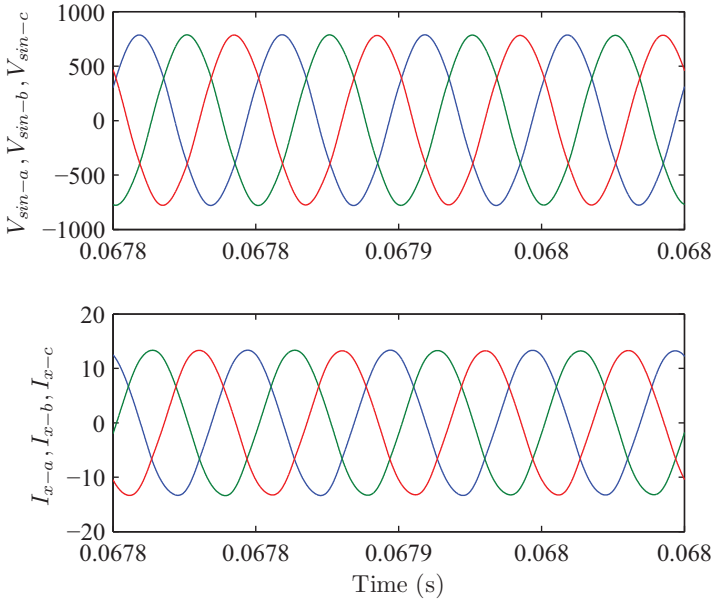

Figure 5.5: Transformer primary voltages and currents

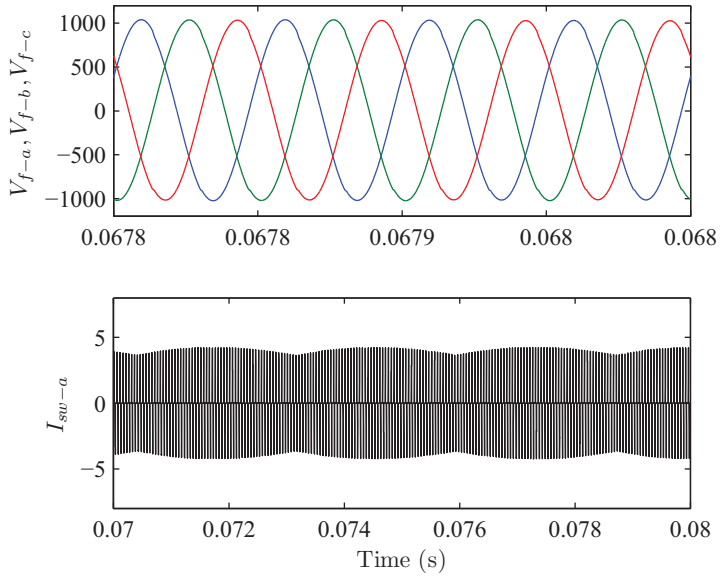

Figure 5.6: Transformer secondary voltages and input current of MC2

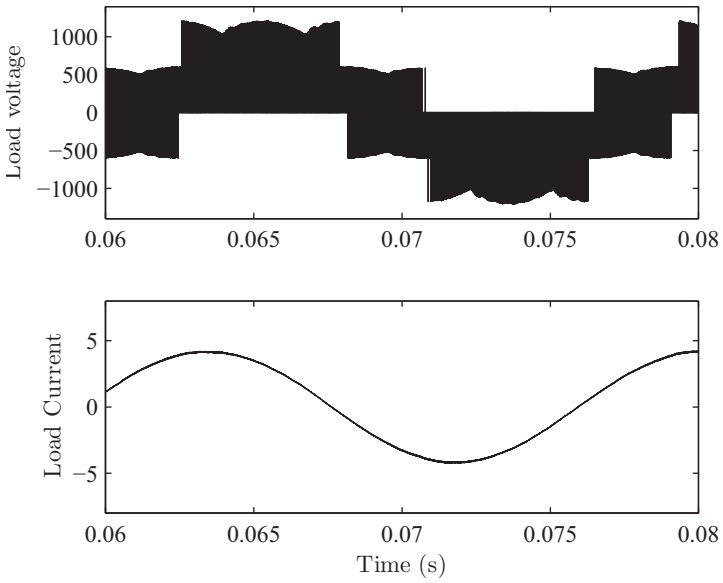

Figure 5.7: Load voltage and current

5.4 Conclusion

A matrix converter-fed sinusoidal input output high frequency transformer has been proposed. The switching frequencies of power electronic transformers are limited by the value of leakage inductance. The proposed topology makes the switching frequency, independent of the value of leakage inductance. Since the series resistance and leakage inductance of the high frequency transformer, is used to form the low pass filter, the number of reactive elements required is reduced. The values of reactive elements required are small, because of high switching frequency.

Note: This chapter is reproduced from my GCMS publication [36].

Chapter 6

Sinusoidal input output three winding HF transformer

This chapter proposes a matrix converter fed, sinusoidal input output three winding high frequency transformer. A single phase three winding transformer is used in the proposed topology. The primary side of the transformer is connected to a low pass filter, and a three phase to single phase matrix converter. The two secondary windings of the transformer are connected to two low pass filters, and a three phase to three phase matrix converter. Because of the low pass filters, the transformer sees high frequency sinusoidal voltages and currents.

A novel pulse density modulation scheme is proposed for matrix converters. The modulation scheme is used in the matrix converter connected to secondary of the transformer.

Zero common mode voltage is achieved with the proposed power electronic transformer. The switching frequency of power electronic transformer, proposed in this chapter, is independent of the value of leakage inductance.

A mathematical model is developed to design the two low pass filters. The proposed power electronic transformer is simulated in MATLAB/SIMULINK environment and results are presented.

6.1 Circuit description and basic principle

The proposed topology is shown in fig. 6.1. The supply voltage at $60Hz$ is converted to high frequency switched voltages by matrix converter MC1. MC1 converts the low frequency supply voltages to high frequency switched voltage, V_{switch}. V_{switch} is filtered by a low pass filter, connected to the primary of the high frequency transformer.

The primary side low pass filter operation is based on the fourier series of a square wave voltage waveform. The fourier series of a square wave is given by

$$v_t = \frac{4}{\pi}\sum_{k=1}^{\inf}\frac{sin(2k-1)2\pi ft}{(2k-1)} \tag{6.1}$$
$$= \frac{4}{\pi}\left[sin(2\pi ft) + \frac{1}{3}sin(6\pi ft) + \frac{1}{5}sin(10\pi ft)\right]$$

So, a square wave contains only odd harmonics. The low pass filter, filters the third and higher order harmonics. Thus, the primary of the transformer sees a high frequency sinusoidal voltage V_p. The frequency of V_p is equal to the switching frequency of MC1.

As shown in fig. 6.1 the power electronic transformer is a single phase three winding transformer. The two windings, of the secondary, are connected to two low pass filters. The leakage inductance of the transformer can be used to form the two low pass filters. Two 180° phase shifted, sinusoidal voltages V_{sf1}, V_{sf2}, at high frequency, are obtained at the output of the two low pass filters.

The two low pass filters are connected to a three phase to three phase matrix converter, MC2. The three inputs of MC2 are denoted by a', b', c' and three outputs are denoted by A, B, C. The three phase voltages at the input of MC2 are $V_{a'N}$, $V_{b'N}$, $V_{c'N}$ and are equal to V_{sf1}, 0 and V_{sf2} respectively. $V_{a'N}$, $V_{b'N}$, $V_{c'N}$ are converted to low frequency voltages by MC2. The modulation strategy proposed for MC2 is explained in section 6.2. The two low pass filters, on the secondary side, filter the switching frequency harmonics present in the input current of MC2. Whereas, the low pass filter, connected to primary of the transformer, filters the harmonics present in V_{switch}. Therefore, the high frequency transformer sees sinusoidal voltages and currents, on both primary and secondary side.

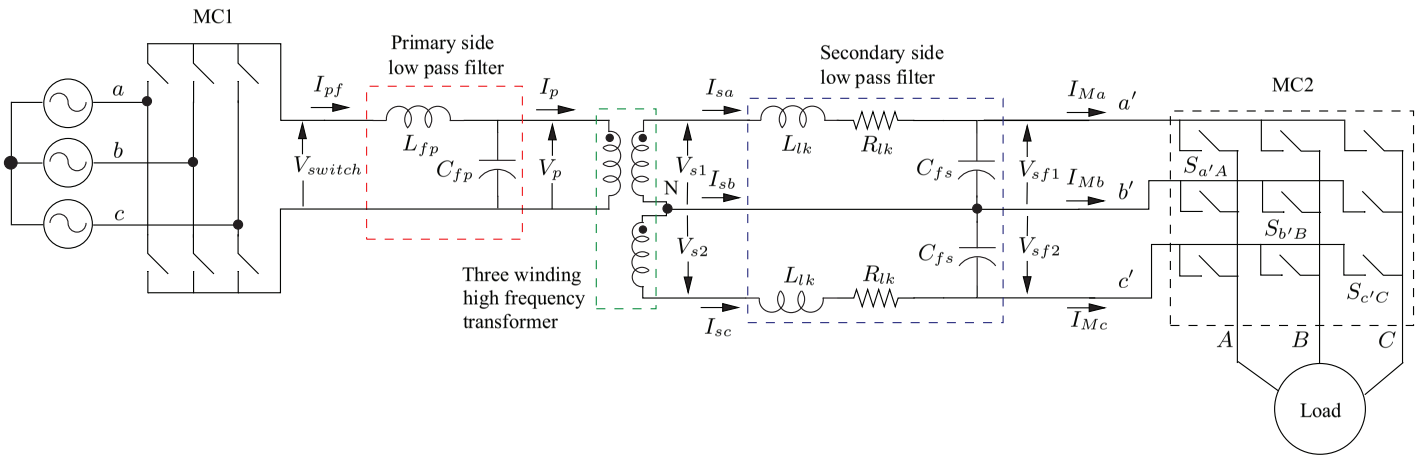

Figure 6.1: Matrix converter fed sinusoidal input output three winding high frequency transformer

6.2 Modulation methods

The modulation methods used for primary side and secondary side converters are described below.

6.2.1 Modulation of Primary side converter

The line to line supply voltages and the switched voltage V_{switch} of MC1 are shown in Fig. 6.2. The maximum of the three line to line voltages is determined by the modulation algorithm. The following example explains the algorithm. Let at any instant V_{ab} is maximum positive. MC1 is switched so that V_{switch} is equal to V_{ab} for $\frac{T_s}{2}$ interval and equal to V_{ba} for next $\frac{T_s}{2}$ interval, where T_s is the switching time period. Therefore, square wave voltage V_{switch}, at switching frequency, is obtained at the output of MC1.

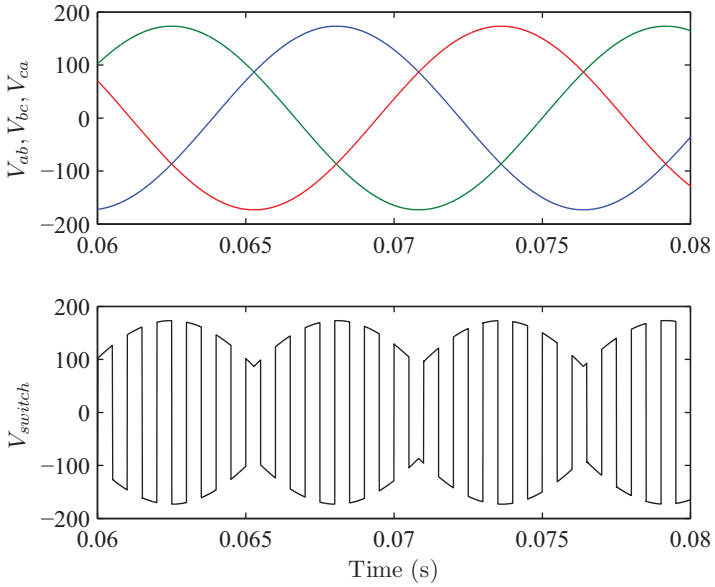

Figure 6.2: Supply voltages and output voltage of MC1

6.2.2 Modulation of Secondary side converter

A novel pulse density modulation (PDM) scheme is proposed for three phase to three phase matrix converter. The modulation scheme can be explained with the help of block

diagram shown in fig. 6.3. M_{AB}, M_{BC}, M_{CA} are the reference voltages at low frequency and V_{AB}, V_{BC}, V_{CA} are the line to line voltages at the output of MC2. The error of reference voltages and output voltages are integrated. The three errors, so obtained, are compared. Based on the comparison of error values, different priority numbers are given to the output phases. The output phase which has the largest error is given priority no. 1 and which has the smallest error is given priority no. 3. Depending on the priority no. and the sign of voltage V_{sf}, the gate pulse for bi-directional switches are generated. Table 6.1 shows the switch to be turned ON, in any phase, depending on the priority no. of that phase and the sign of V_{sf1}.

Unlike the PDM explained in [37] and [38], which is used for single phase AC link to three phase systems, the proposed PDM scheme is suitable for any three phase to three phase high frequency AC link system. Also, in the above explained PDM, MC2 is switched at every zero crossing of the high frequency sine wave. So, MC2 operates at ZVS and has zero switching losses.

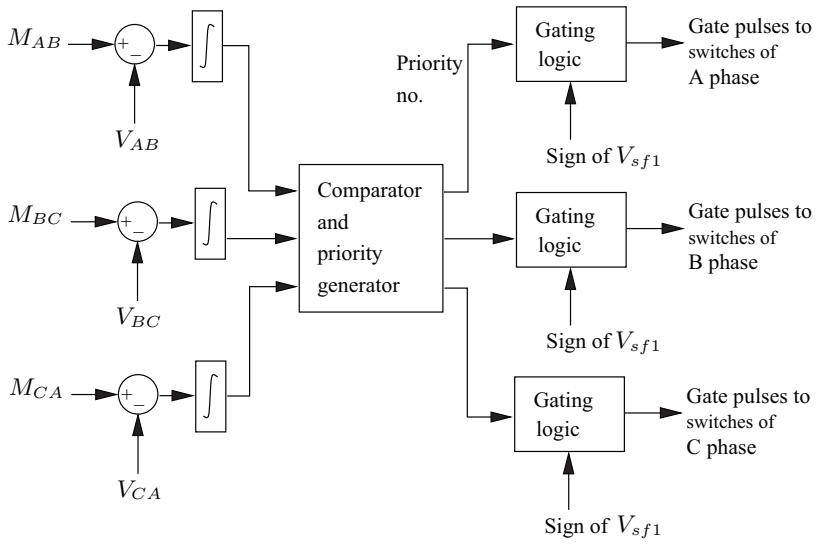

Figure 6.3: Block diagram of modulation of MC2

Table 6.1: Switching combinations in MC2 using PDM

Priority No.	Sign of V_{sf1}	Switch to turn ON ($j = A, B, C$)
1	+	$S_{a'j}$
2	+	$S_{b'j}$
3	+	$S_{c'j}$
1	−	$S_{c'j}$
2	−	$S_{b'j}$
3	−	$S_{a'j}$

6.3 Common mode voltage

The common mode voltage for the proposed power electronic transformer is defined in equation 6.2 as

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3} \tag{6.2}$$

From table 6.1 it can be observed that, the PDM explained in section 6.2.2, uses only six switching combinations: $S_{a'A}$, $S_{b'B}$, $S_{c'C}$; $S_{a'A}$, $S_{c'B}$, $S_{b'C}$; $S_{b'A}$,$S_{a'B}$, $S_{c'C}$; $S_{b'A}$,$S_{c'B}$, $S_{a'C}$; $S_{c'A}$,$S_{a'B}$, $S_{b'C}$ and $S_{c'A}$,$S_{b'B}$, $S_{a'C}$. So, at any instant, no two output phases are connected to the same input phase of MC2. Therefore, at any instant of time, the sum of input phase voltages is equal to common mode voltage.

As explained in section 6.1, the input voltages of MC2 are $V_{a'N}$, $V_{b'N}$, $V_{c'N}$ and are equal to V_{sf1}, 0 and V_{sf2} respectively. Since, V_{sf1} and V_{sf2} are 180° phase shifted, therefore, the sum of input voltages of MC2 is equal to zero. Thus, zero common mode voltage in achieved in MC2.

6.4 Filter design

Filter design is the most important part of the proposed converter. To design the filter a mathematical model is developed.

The equations for the secondary side filter are given by

$$V_{s1}(s) - V_{sf1}(s) = (R_{lk} + sL_{lk})I_{sa}(s) \tag{6.3}$$

$$I_{sa}(s) = I_{Ma}(s) + sC_{fs}V_{sf1}(s) \tag{6.4}$$

Solving these equations, we obtain

$$I_{sa}(s) = \frac{I_{Ma}(s)}{1 + sC_{fs}R_{lk} + s^2L_{lk}C_{fs}} + \frac{sC_{fs}V_{s1}(s)}{1 + sC_{fs}R_{lk} + s^2L_{lk}C_{fs}} \tag{6.5}$$

$$V_{sf1}(s) = \frac{V_{s1}(s)}{1 + sC_{fs}R_{lk} + s^2L_{lk}C_{fs}} - \frac{(R_{lk} + sL_{lk})I_{Ma}(s)}{1 + sC_{fs}R_{lk} + s^2L_{lk}C_{fs}} \tag{6.6}$$

Substituting, $\omega_{n2} = \frac{1}{\sqrt{L_{lk}C_{fs}}}$ and $\zeta_2 = \frac{R_{lk}}{2}\sqrt{\frac{C_{fs}}{L_{lk}}}$, we get

$$I_{sa}(s) = \frac{\omega_{n2}^2 I_{Ma}(s)}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} + \frac{sC_{fs}\omega_{n2}^2 V_{s1}(s)}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} \tag{6.7}$$

$$I_{sa}(s) = T_s(s)I_{Ma}(s) + T_{svi}(s)V_{s1}(s) \tag{6.8}$$

$$V_{sf1}(s) = \frac{\omega_{n2}^2 V_{s1}(s)}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} - \frac{(R_{lk} + sL_{lk})\omega_{n2}^2 I_{Ma}(s)}{s^2 + 2\zeta_2\omega_{n2}s + \omega_{n2}^2} \tag{6.9}$$

$$V_{sf1}(s) = T_s(s)V_{s1}(s) - T_{siv}(s)I_{Ma}(s) \tag{6.10}$$

Similarly, equations are obtained for the primary side and are given below.

$$I_{pf}(s) = \frac{\omega_{n1}^2 I_p(s)}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} + \frac{sC_{fp}\omega_{n1}^2 V_{switch}(s)}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} \tag{6.11}$$

$$I_{pf}(s) = T_p(s)I_p(s) + T_{pvi}(s)V_{switch}(s) \tag{6.12}$$

$$V_p(s) = \frac{\omega_{n1}^2 V_{switch}(s)}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} - \frac{(R_{ps} + sL_{fp})\omega_{n1}^2 I_p(s)}{s^2 + 2\zeta_1\omega_{n1}s + \omega_{n1}^2} \tag{6.13}$$

$$V_p(s) = T_p(s)V_{switch}(s) - T_{piv}(s)I_p(s) \tag{6.14}$$

where, $\omega_{n1} = \frac{1}{\sqrt{L_{fp}C_{fp}}}$ and $\zeta_1 = \frac{R_{ps}}{2}\sqrt{\frac{C_{fp}}{L_{fp}}}$ and R_{ps} is the effective series resistance of the filter inductor L_{fp}.

From the above equations it can be seen that, to design the low pass filters, on the two sides of the transformer, the transfer functions, $T_s(s)$, $T_{svi}(s)$, $T_{siv}(s)$ and $T_p(s)$, $T_{pvi}(s)$, $T_{piv}(s)$ are to be designed. These two sets of transfer functions are similar. So, only design of one set of transfer function is discussed in this paper. $T_s(s)$ is the familiar second order transfer function. To design $T_s(s)$, first the cut off frequency need to be selected depending on the switching frequency. Cut off frequency should be higher than the switching frequency. The reason for this choice is explained in section 6.1. Depending on the value of leakage inductance of the high frequency transformer, the value of capacitance for the filter can be decided. The bode plot of $T_s(s)$, $T_{svi}(s)$, $T_{siv}(s)$ are shown in fig. 6.4. From the bode plots it can be seen that $T_{svi}(s)$, $T_{siv}(s)$ produce amplification in voltage and current. So value of capacitor chosen should be such that the minimum amplification is obtained.

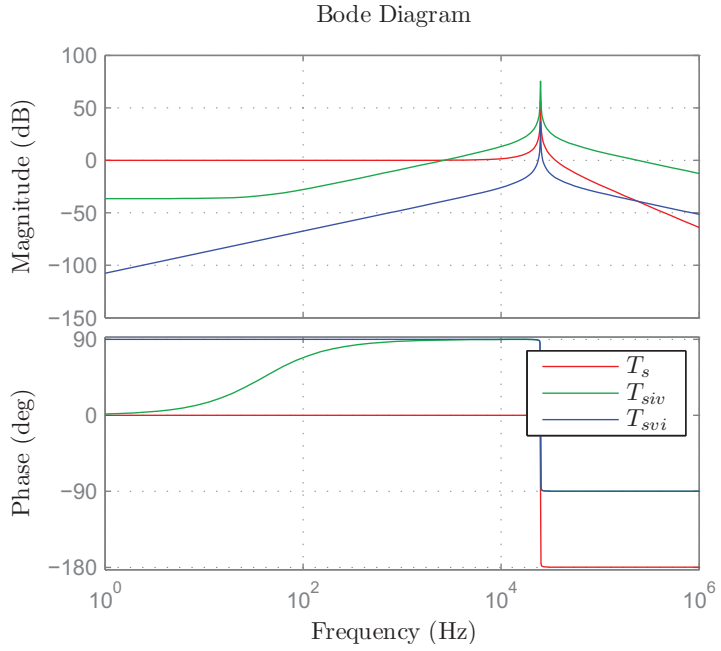

Figure 6.4: Bode plot of $T_s(s)$, $T_{svi}(s)$, $T_{siv}(s)$

6.5 Simulation results

The proposed topology has been simulated in MATLAB/ SIMULINK environment for a supply voltage of $100V$, $60Hz$ and RL load of 20Ω and $50mH$. The high frequency transformer used is $400V\backslash 400V\backslash 400V$, $10kVA$, $20kHz$. The value of series resistance and leakage inductance used for the transformer are $10m\Omega$ and $50\mu H$ respectively. The primary side low pass filter is designed for cut off frequency of $25kHz$ and capacitance C_{pf} equal to $2.026\mu F$. The secondary side low pass filters are designed for cut off frequency of $25kHz$ and capacitance C_{pf} equal to $0.675\mu F$.

Fig. 6.5 shows the input voltage and current of primary side filter, V_{switch} and I_{pf}. Fig. 6.6 shows the transformer primary voltage and current, V_p and I_p. Fig. 8 shows the transformer secondary voltage and current, V_{s1}, V_{s2}, I_{sa}, I_{sb}, I_{sc}. It can be seen from fig. 6.6 and fig. 6.7 that the transformer voltage and current are sinusoidal. Fig. 6.8 shows the input voltage and current of matrix converter V_{sf1}, V_{sf2}, I_{Ma}. The simulation results show that V_{sf1} and V_{sf2} are phase shifted by 180°. The load voltage and current are shown in fig. 6.9. Fig. 6.10 shows the common mode voltage V_{CM}, defined in section 6.3. Fig. 6.2 shows that the common mode voltage is zero.

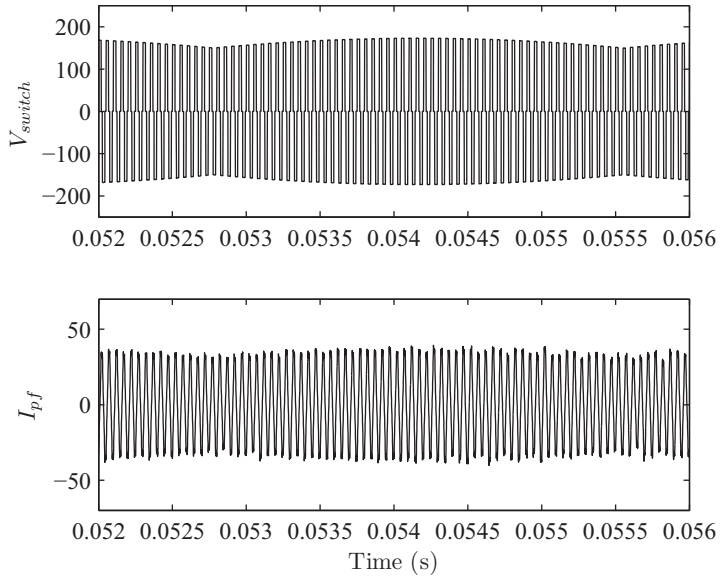

Figure 6.5: Input voltage and current of primary side filter

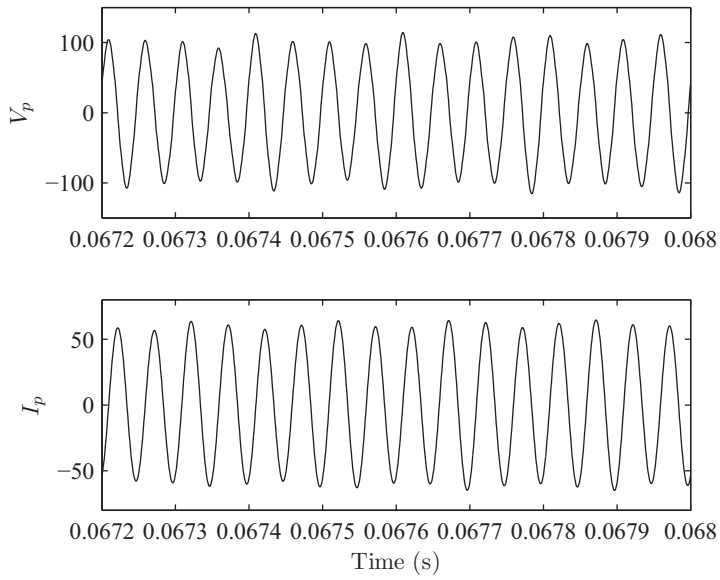

Figure 6.6: Transformer primary voltage and current

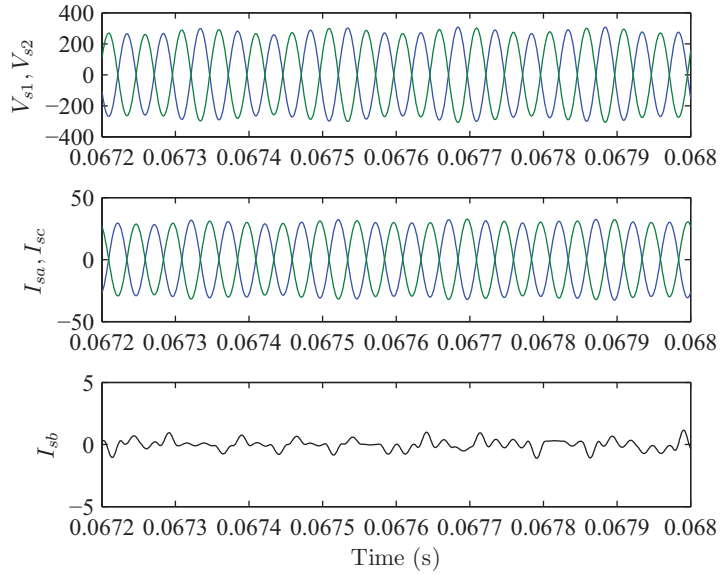

Figure 6.7: Transformer secondary voltage and current

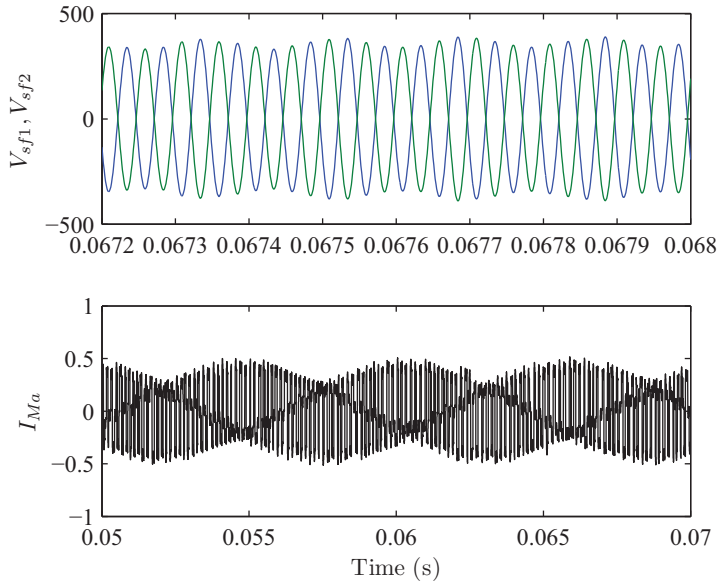

Figure 6.8: Input voltage and current of matrix converter

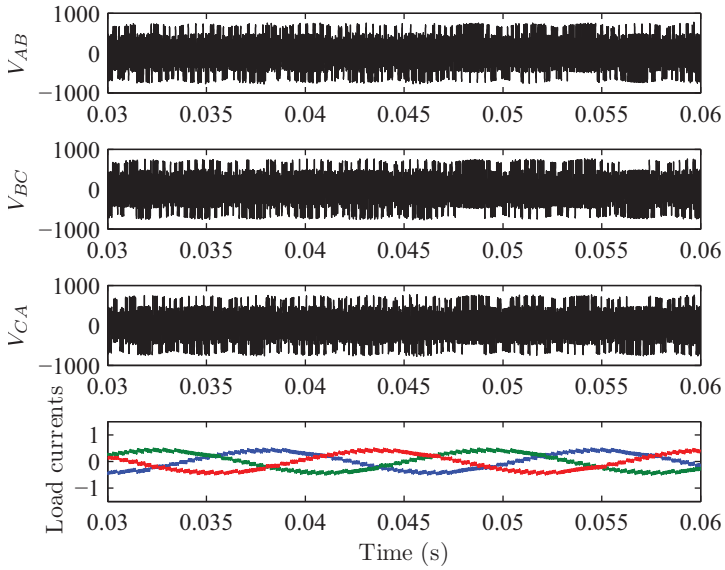

Figure 6.9: Load voltages and currents

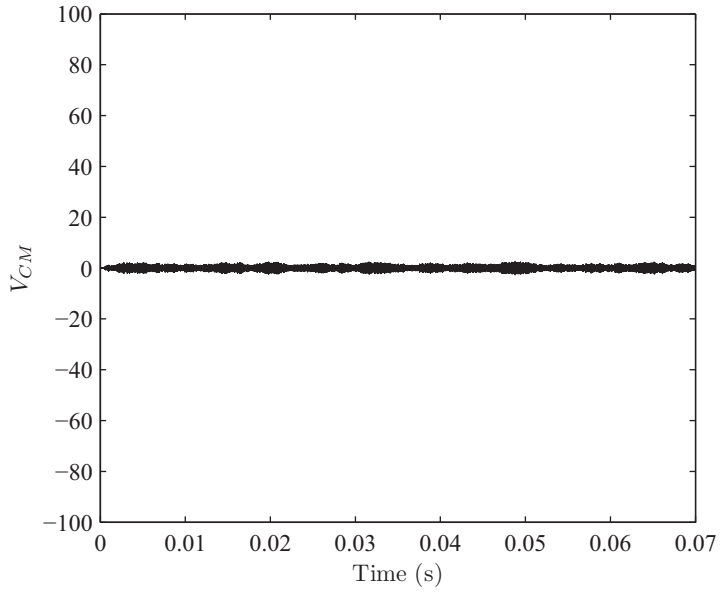

Figure 6.10: Common mode voltage

6.6 Conclusion

A matrix converter-fed sinusoidal input output three winding high frequency transformer has been proposed. In high frequency transformer, the value of leakage inductance puts a limit on the switching frequency. In the proposed topology the switching frequency is not limited by the value of leakage inductance. The series resistance and leakage inductance of the high frequency transformer are used to form the low pass filter. This reduces the number of reactive elements required. Because of high switching frequency, the values of reactive elements required are small.

By the use of single phase three winding transformer, two 180° phase shifted voltages are obtained. These two voltages and the novel pulse density modulation scheme, proposed for matrix converters, give zero common mode voltage. In addition, zero switching losses are obtained, in the secondary side matrix converter, by use of pulse density modulation.

Note: This chapter is reproduced from my IEEE publication [39].

Chapter 7

Sinusoidal current HF transformer

A power electronic converter, with sinusoidal currents in high frequency transformer, is proposed in this chapter. As in chapter 5 and chapter 6, the switching frequency of power electronic transformer, proposed in this chapter, is again independent of the value of leakage inductance. This is achieved with the help of a low pass filter, formed by connecting a capacitor across the secondary.

High frequency switched voltage, is produced across the primary of the transformer. Sinusoidal voltage at high frequency is obtained at secondary side because of filter action.

A matrix converter is connected to the secondary of the transformer. The switched currents at the input of the matrix converter are filtered by the capacitor. Thus, sinusoidal currents flow in the high frequency transformer.

Modulation strategies for the two matrix converters at the two sides of the transformer are explained. A mathematical model is developed to design the low pass filter. The proposed transformer is simulated in MATLAB/SIMULINK and results are provided.

The proposed converter is also tested for unbalanced load and the simulation results are presented.

7.1 Circuit description and basic principle

The proposed topology is shown in Fig. 7.1. The primary of the high frequency transformer is connected to a three phase to single phase matrix converter. The three phase to single phase matrix converter, MC1 converts the low frequency supply voltages to high frequency switched voltage V_{switch}. A capacitor C_f is connected to the secondary of the high frequency transformer. The high frequency transformer with the capacitor forms a low pass filter. The output of the filter is connected to a single phase to three phase matrix converter, MC2. The output of the single phase to three phase matrix converter, MC2 is connected to a three phase load.

The low pass filter operation is based on the fourier series of a square wave voltage waveform as explained in chapter 6.

So, a square wave contains only odd harmonics. The low pass filter, filters the third and higher order harmonics. Therefore, the switched voltage V_{switch} is filtered to a sine wave voltage V_{filter}, by the low pass filter. The frequency of sine wave voltage V_{filter} is equal to the switching frequency of MC1. V_{filter} is then converted to low frequency voltages by MC2.

The input current of MC2 is a switched current I_{switch}. I_{switch} is also filtered by the low pass filter. The filtered current, I_{filter} is nearly sinusoidal. The equivalent circuit is shown in Fig. 7.2. The low pass filter filters the switched voltage V_{switch}, at its input and the switched currents I_{switch}, at its output and, gives filtered voltage V_{filter}, at its output and filtered current I_{filter}, at its input. Thus, the primary and secondary windings of the high frequency transformer see a nearly sinusoidal current and, the problem of current commutation in leakage inductance, due to switched currents at the input of MC2, is eliminated.

Unlike the resonant converters proposed in [37] and [38], the topology proposed in this paper is based on low pass filter operation. In addition, it uses the transformer series resistance and leakage inductance at the primary and secondary side. Only one additional reactive element C_f is needed. This is unlike the converters proposed in [37] and [38], which use tank circuits on both primary and secondary side of the transformer.

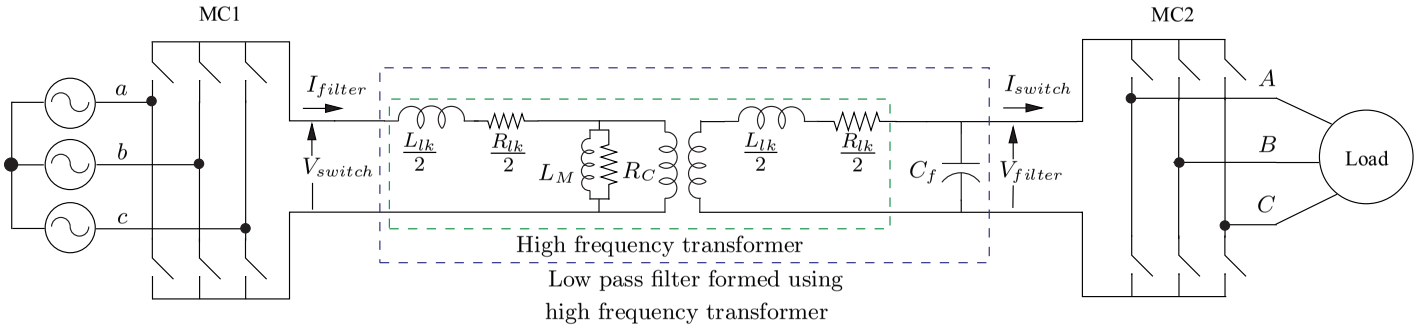

Figure 7.1: Power electronic converter with sinusoidal currents in high frequency transformer

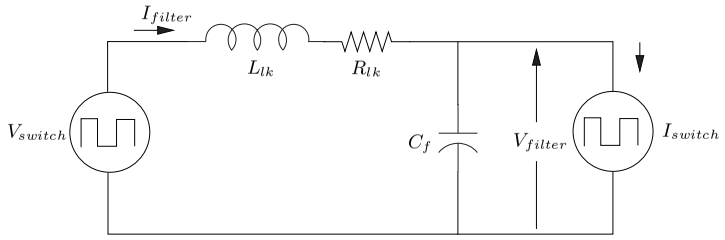

Figure 7.2: Equivalent circuit

7.2 Modulation methods

The modulation methods used for primary side and secondary side converters are described below.

7.2.1 Modulation of Primary side converter

The modulation of the primary side converter is the same as that of the modulation of primary side converter of sinusoidal input output three winding transformer, explained in section 6.2.1.

7.2.2 Modulation of Secondary side converter

Since the input voltage to MC2, is a sine wave at switching frequency, pulse density modulation [37] is used for obtaining low frequency voltages at the output of MC2. Fig. 7.3 shows the pulse density modulation scheme [37]. M_{AB}, M_{BC}, M_{CA} are the reference voltages at low frequency and V_{AB}, V_{BC}, V_{CA} are the output line to line voltages of MC2. The error of reference voltage and output voltage is integrated. A digital logic decides the gating pulse for the switch, depending on the sign of, integration of error, V_{filter} and V_{AB}, V_{BC}, V_{CA} for each phase.

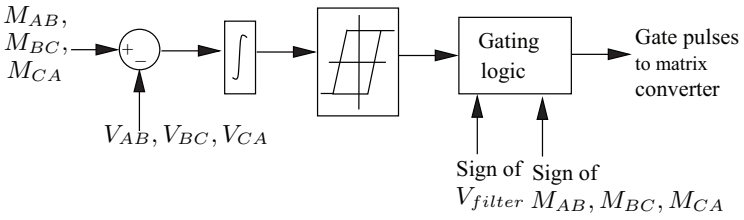

Figure 7.3: Pulse density modulation

7.3 Filter design

Filter design is the most important part of the proposed converter. To design the filter a mathematical model is developed. The primary side series resistance and leakage inductance is referred to the secondary side, and the magnetizing inductance and core

loss resistance is neglected, for simplicity in analysis. The total series resistance and leakage inductance referred to secondary side is R_{lk} and L_{lk} respectively. The equations for V_{filter} , I_{filter}, V_{switch} and I_{switch} is given by

$$V_{filter}(s) = V_{switch}(s) - (R_{lk} + sL_{lk})I_{filter}(s) \tag{7.1}$$

$$I_{filter}(s) = sC_f V_{filter}(s) - I_{switch}(s) \tag{7.2}$$

The above equations can be written further as

$$V_{filter}(s) = \frac{V_{switch}(s)}{1 + sC_f R_{lk} + s^2 L_{lk} C_f} - \frac{(R_{lk} + sL_{lk})I_{switch}(s)}{1 + sC_f R_{lk} + s^2 L_{lk} C_f} \tag{7.3}$$

$$= H_{basic}(s)V_{switch}(s) - H_{vf}(s)I_{switch}(s) \tag{7.4}$$

$$I_{filter}(s) = \frac{I_{switch}(s)}{1 + sC_f R_{lk} + s^2 L_{lk} C_f} + \frac{sC_f V_{switch}(s)}{1 + sC_f R_{lk} + s^2 L_{lk} C_f} \tag{7.5}$$

$$= H_{basic}(s)I_{switch}(s) + H_{if}(s)V_{switch}(s) \tag{7.6}$$

Substituting

$$\omega_n = \frac{1}{\sqrt{L_{lk}C_f}} \text{ and } \zeta = \frac{R_{lk}}{2}\sqrt{\frac{C_f}{L_{lk}}} \tag{7.7}$$

equations (7.4) and (7.6) become the familiar second order transfer functions. Based on these equations a mathematical model is developed for the filter design and is shown in fig. 7.4.

From fig. 7.4 it is clear that the three transfer functions $H_{basic}(s)$, $H_{vf}(s)$ and $H_{if}(s)$ affect the filter design. The values of L_{lk} and C_f not only decide the cut off frequency, ω_n and damping factor, ζ, but also the gain for the transfer functions $H_{vf}(s)$ and $H_{if}(s)$. The bode plots for $H_{basic}(s)$, $H_{vf}(s)$ and $H_{if}(s)$ are shown in fig. 6.4 for a cut off frequency of $30kHz$. Since the values of R_{lk} and L_{lk} are obtained from transformer parameters, C_f is decided by ω_n and ζ is calculated from (7.7).

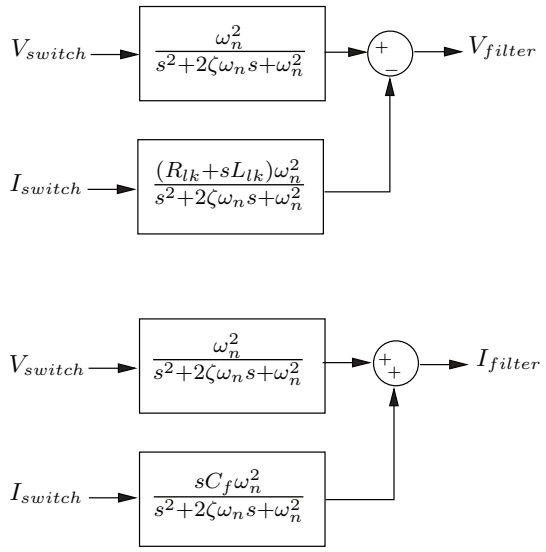

Figure 7.4: Mathematical model of low pass filter

7.4 Simulation results

The proposed topology has been simulated in MATLAB/ SIMULINK environment for a supply voltage of $100V$, $60Hz$ and RL load of 20Ω and $100mH$. The high frequency transformer used is $120\backslash120V$, $5kVA$. The simulation is performed at two switching frequencies of $20kHz$ and $100kHz$. The value of series resistance and leakage inductance used for the transformer are $10m\Omega$ and $200\mu H$. The cut off frequencies chosen are $15kHz$ and $90kHz$ for switching frequencies of $20kHz$ and $100kHz$ respectively. The C_f values after filter design are $0.56\mu F$ and $15.6nF$ for $20kHz$ and $100kHz$ respectively. Therefore, the value of capacitor needed for filter, is small.

Fig. 7.5, 7.6 and 7.7 show V_{switch}, I_{filter}, V_{filter}, I_{switch}, the line to line load voltages V_{AB}, V_{BC}, V_{CA} and the three phase load currents respectively, for switching frequency of 20kHz. Fig. 7.8, 7.9 and 7.10 show V_{switch}, I_{filter}, V_{filter}, I_{switch}, the line to line load voltages V_{AB}, V_{BC}, V_{CA} and the three phase load currents respectively, for switching frequency of $100kHz$. From the simulation results it can be seen that, V_{filter} and I_{filter} are nearly sinusoidal.

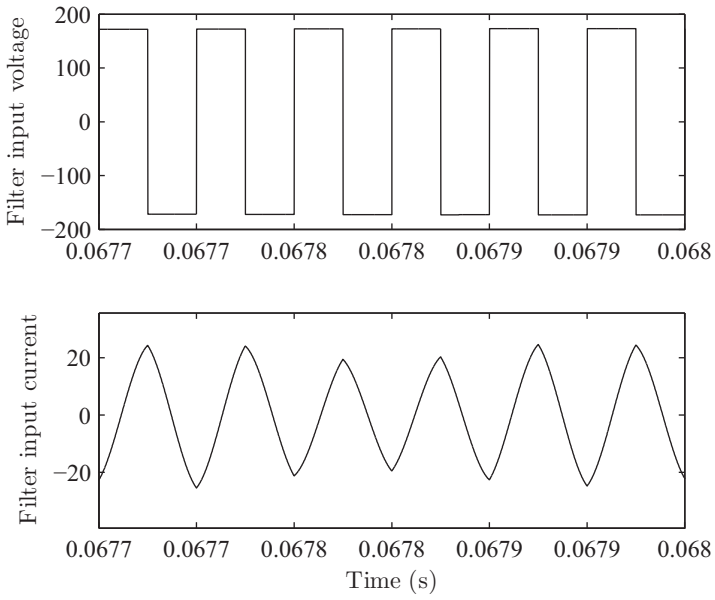

Figure 7.5: Input voltage and current of filter at 20kHz

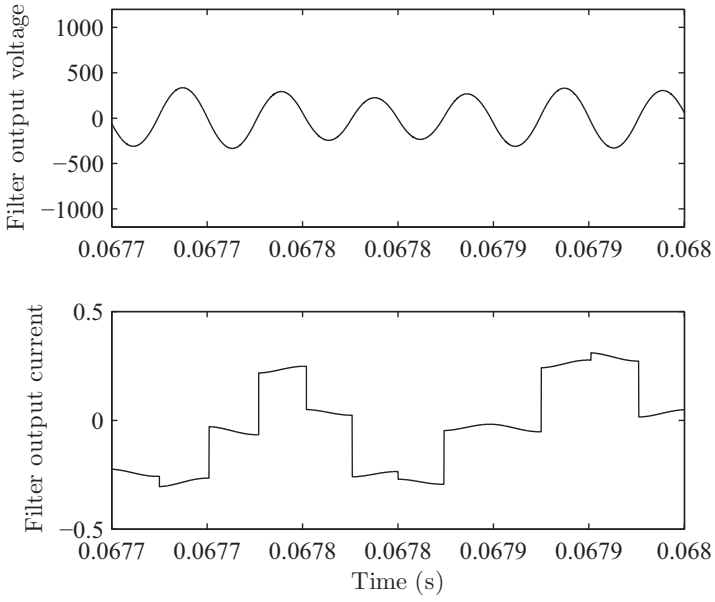

Figure 7.6: Output voltage and current of filter at 20kHz

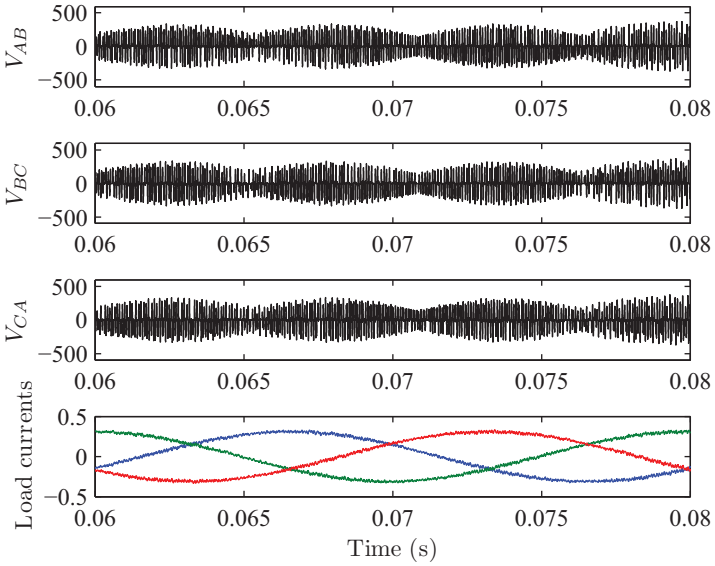

Figure 7.7: Load voltage and current at 20kHz

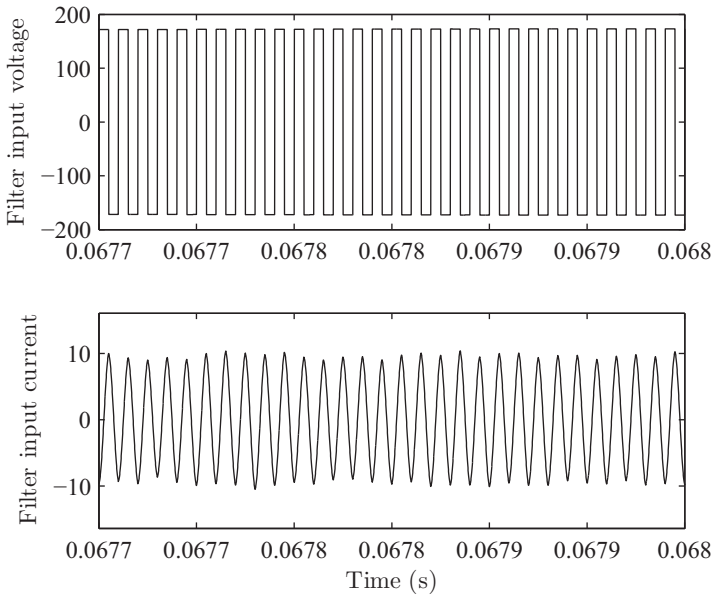

Figure 7.8: Input voltage and current of filter at 100kHz

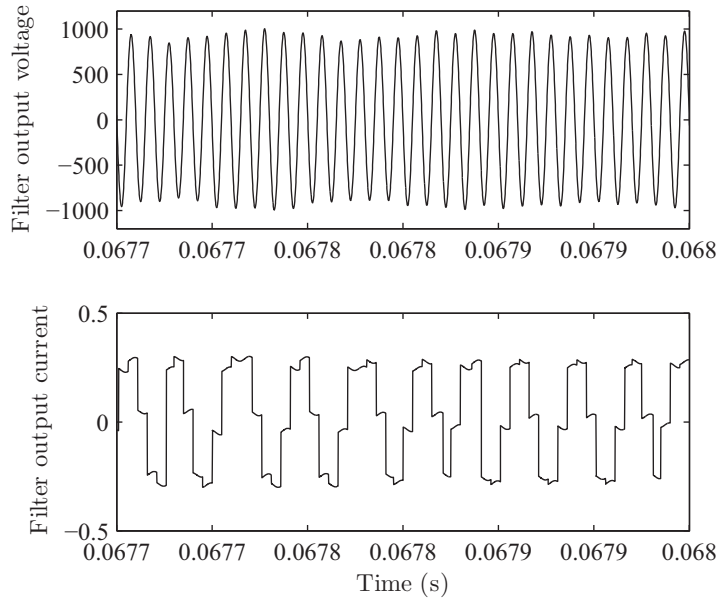

Figure 7.9: Output voltage and current of filter at 100kHz

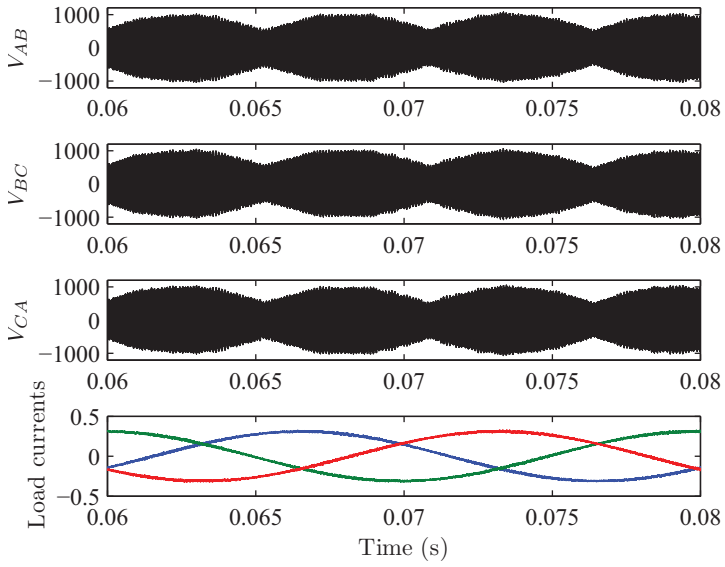

Figure 7.10: Load voltage and current at 100kHz

7.5 Sinusoidal current high frequency transformer with unbalanced load

The sinusoidal current high frequency transformer is tested with unbalanced load. Two phases of the output of MC2 are connected to a RL load of 10Ω and $10mH$ and one phase is connected to a RL load of 1Ω and $1mH$. A HF transformer at $20kHz$ is used. Fig. 7.11 shows the voltage across the transformer primary winding, secondary winding and transformer current. Fig. 7.12 and fig. 7.13 show the output line to line voltages across the load and the load currents for unbalanced condition. From fig. 7.11 and fig. 7.12, it can be seen that the transformer voltages and load voltages remain unaffected by the unbalanced load.

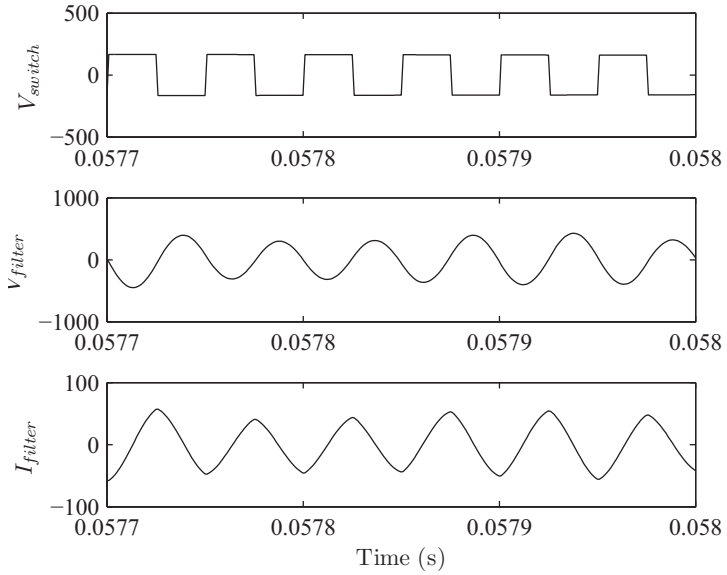

Figure 7.11: Transformer primary voltage, secondary voltage and transformer current for unbalanced load at 20kHz

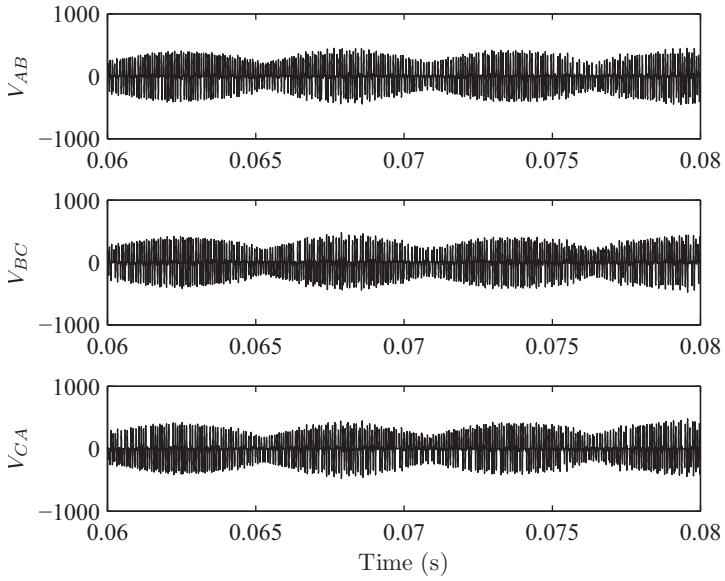

Figure 7.12: Output voltages for unbalanced load

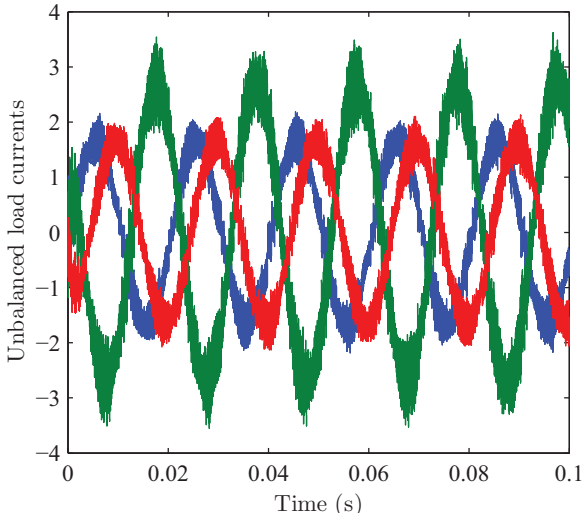

Figure 7.13: Unbalanced load current at 20kHz

7.6 Conclusion

A solid state converter with sinusoidal currents in high frequency transformer is proposed. The switching frequency of high frequency transformer is limited by the value of leakage inductance. The proposed topology makes the switching frequency, independent of the value of leakage inductance. Also, there is no energy loss because of leakage inductance. Since the series resistance and leakage inductance of the high frequency transformer, is used to form the low pass filter, only one additional reactive element i.e. a capacitor is needed. The value of capacitance required is small, because of high switching frequency. The proposed PET is able to take unbalanced load with negligible change in output voltage..

Note: Part of this chapter is reproduced from my IEEE publication [40].

Chapter 8

Implementation of sinusoidal current HF transformer

A $0.5kW$ laboratory prototype of sinusoidal current high frequency transformer is built and experimentally verified. Experiments are performed with RL load of 10Ω and $22.5mH$. The details of the hardware developed for the prototype are provided. The control algorithm programmed in verilog is described. The inferences of the experimental results obtained are discussed.

8.0.1 Implementation of hardware

The implementation block diagram of the sinusoidal current high frequency transformer is shown in fig 8.1 and the laboratory prototype is shown in fig 8.2. The three phase power, required for the experimental setup, is taken from a programmable AC power supply. Integrated bidirectional modules of $600V$, $75A$ APTGT75TDU60PG are used to realize both the primary side and secondary power converters. Diode bridge clamp circuits are used for over voltage protection of power devices for both primary and secondary side matrix converters. Integrated diodes $1000V$, $30A$ APT30D100BHB, 100Ω external clamp resistors and $2.2\mu F$ capacitors are used to form the clamp circuits. The clamp is initially charged from a DC power supply. Integrated driver modules 6SD601E are used as driver circuits for the power converters. Damping resistors of 1.4Ω is used at primary side of the high frequency transformer.

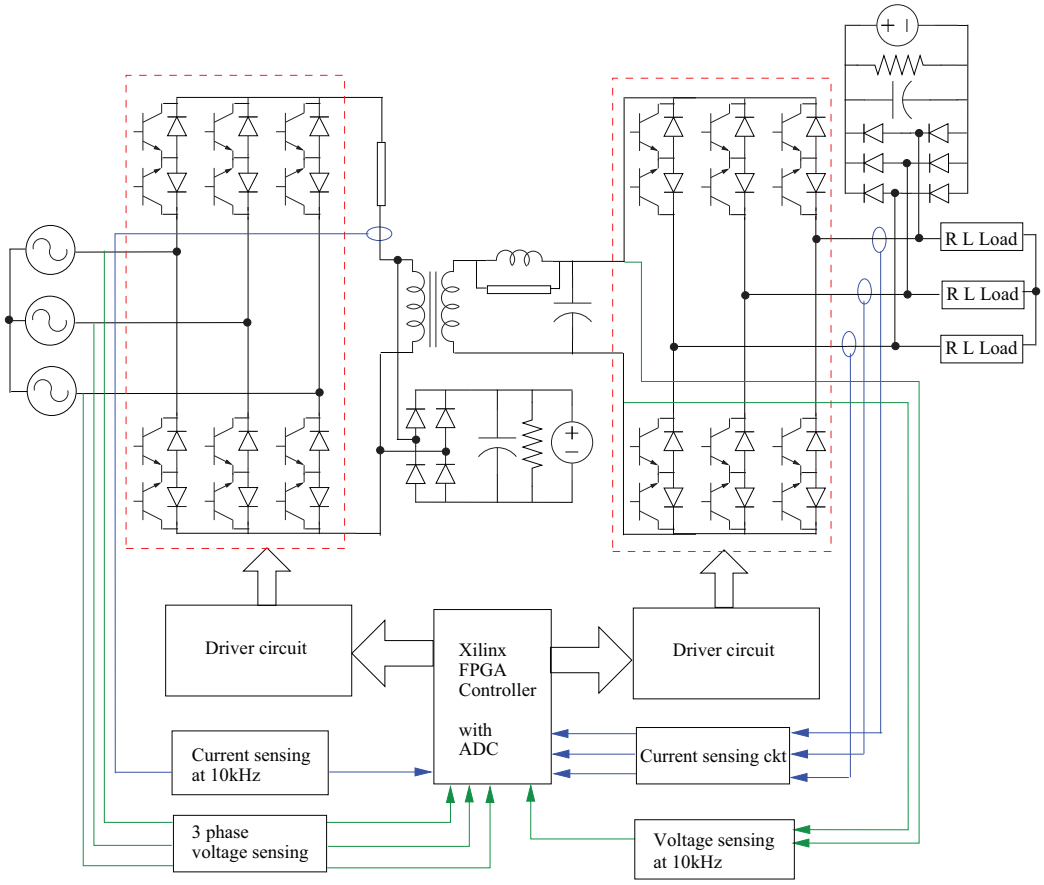

Figure 8.1: Implementation diagram of sinsoidal current HF transformer

A $100V \backslash 100V$, $2kVA$, $10kHz$ ferrite core HF transformer, shown in fig. 8.3, is used for the experiments. The transformer parameters are provided in table 8.1. The leakage inductance of the transformer is measured with the help of a LCR meter by shorting the secondary terminals.

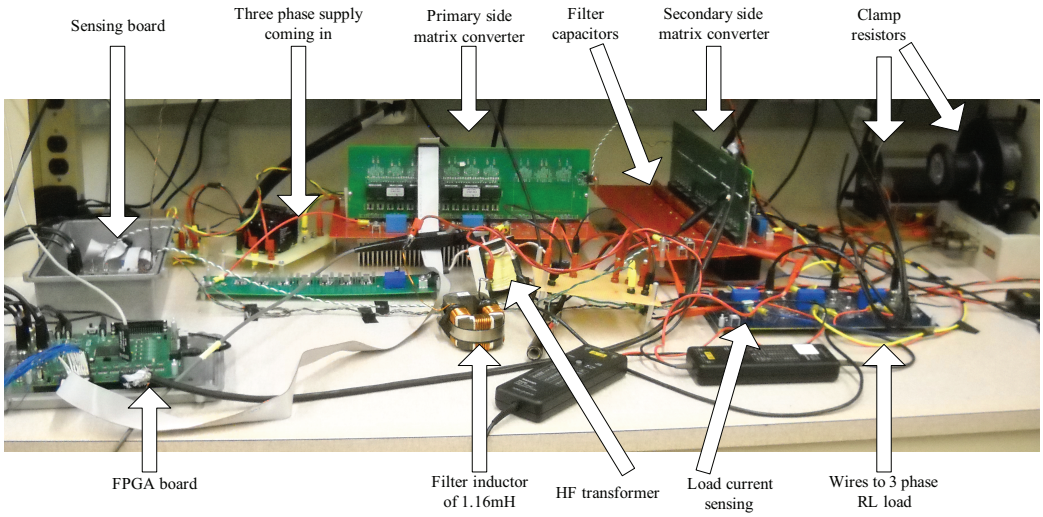

Figure 8.2: Laboratory prototype of sinusoidal current HF transformer

Table 8.1: Transformer parameters

Parameter	Value
Voltage rating	$100V$ peak
Current rating	$20A$
Turns ratio	1:1
Frequency	$10kHz$
Magnetizing inductance	$3.98mH$
Core resistance	–
Leakage inductance	$15\mu H$
Series resistance	$30m\Omega$

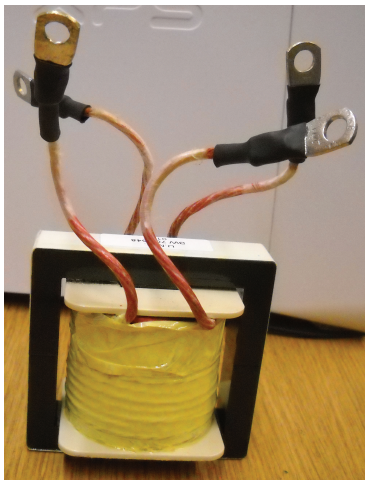

Figure 8.3: HF transformer

Since the leakage inductance of the HF transformer used is very small, to prove the advantage of the proposed topology at high leakage inductances, an additional inductance of $1.16mH$ is connected at the secondary of the transformer. An extra damping resistor of 100Ω is connected across the inductor in the secondary side of the HF transformer. Capacitor of value $0.47\mu F$ is used to form the low pass filter with the $1.16mH$ inductor and transformer. Special film capacitors QXK2J474KTPTZH ($0.47\mu F$, $630VDC$, $250VAC$) which can take high voltages at $10kHz$ frequency are used for the filter. The driver signals at $15V$ are obtained from a Xilinx XC3S500E FPGA control board. This control board can accept 12 analog input signals (AD7367-5) at $\pm 10V$ and 10 digital inputs at $5V$ or $3.3V$ and output 60 digital signals at $15V$. The Xilinx FPGA board is shown in fig 8.4.

LEM sensors LA 55-P are used for sensing load currents at the output of the secondary side matrix converter. The current signals sensed are passed through a salen key low pass filter to reject high frequency noise. The current sensing circuit takes a power supply voltage of $\pm 15V$. The gains are adjusted to give voltages in range of $\pm 10V$. The high frequency sinusoidal voltage at $10kHz$ are sensed using a differential amplifier. The differential amplifier used gives a maximum delay of $18\mu s$ at $10kHz$. The design of very high speed differential amplifier is important for the proper implementation of pulse density modulation method. The three phase line to line supply voltages are sensed

using differential amplifiers. LEM sensor LA25-P is used for sensing currents at $10kHz$ in the primary winding of the transformer. Again, in both these sensing circuits the power supply voltage is at $\pm 15V$ and the gains are scaled to output in range of $\pm 10V$. The analog output signals of all the above mentioned sensing circuits are given to the Xilinx FPGA control board. The sensor board developed shown in fig. 8.5.

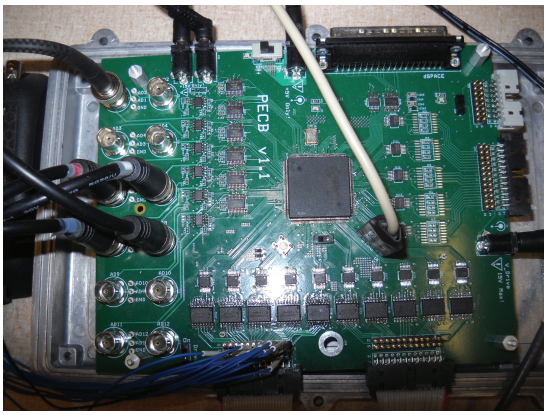

Figure 8.4: Xilinx FPGA board

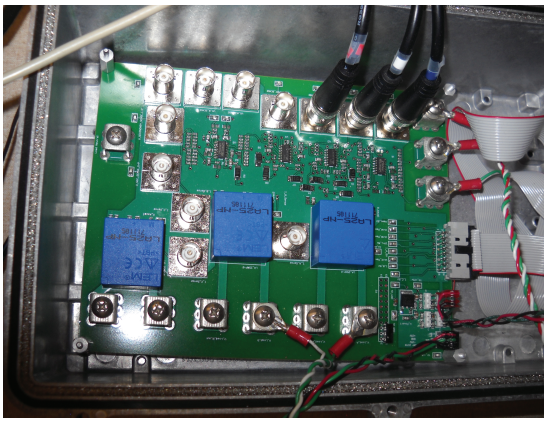

Figure 8.5: Sensor board

8.0.2 Implementation of control algorithm

The control algorithm needed to generate to the driver pulses of the two matrix converters can be explained with help of fig. 8.6 and fig. 8.7 . Fig. 8.6 shows the block diagram of Verilog code written in Xilinx ISE to generate the pulses to control the primary side matrix converter. The clock frequency used for all the Verilog modules is $50MHz$. The Verilog code has six modules and they are explained as follows:

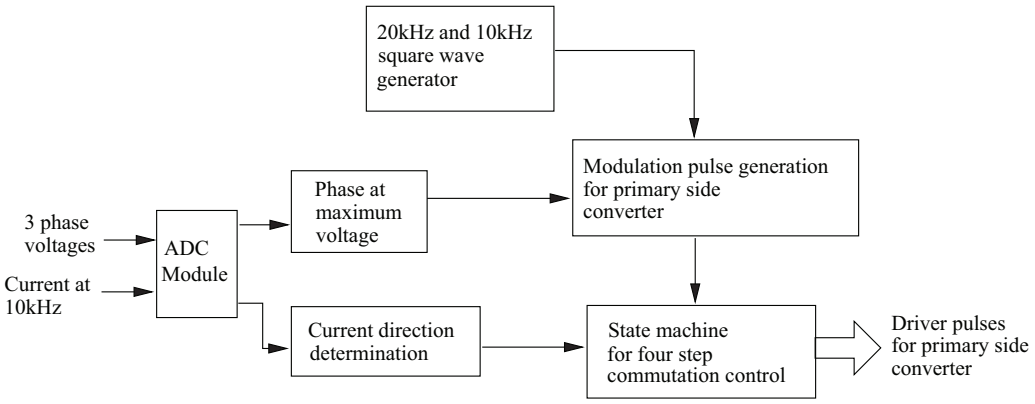

Figure 8.6: Block diagram of primary side verilog control

1. ADC module - The three phase line to line supply voltages and the current in the primary winding of the transformer, measured with the voltage and current sensing circuits, are read by the ADC on the FPGA board. A Verilog module is synthesized for the A\D conversion and to read the data from the ADC. This module has two instants one reads the two out of the three phase voltages and second reads the third phase voltage and the current in the primary winding.

2. Phase at maximum voltage This module compares the three line to line voltages and determines which of the three phase voltages is maximum and outputs logic 01 if V_{ab} is maximum, logic 10 if V_{bc} is maximum and logic 11 if V_{ca} is maximum.

3. $20kHz$ and $10kHz$ square wave generator Two square waves one at $20kHz$ and another at $10kHz$ are generated by this module. The $10kHz$ square wave is needed as the reference switching time period for the primary side matrix converter. The $20kHz$ square wave is in synchronization with the $10kHz$ square wave.

4. Pulse generation for primary side converter This modules takes the $20kHz$ and $10kHz$ square waves as input, and depending on the output of the module - phase at maximum voltage, determines which switch needs to be turned ON and generates the six pulses for the six bi-directional devices of the primary side matrix converter.

5. Current direction determination The direction of current needs to be determined for the commutation control of the matrix converter. Current direction determining module compares the current with zero and gives the output as bit 1 for one direction of current and bit 0 for the opposite direction of current.

6. State machine for four step commutation control A state machine is used for the four step commutation control of the matrix converter. The state machine takes the 6 pulses generated for the primary side converter and the current direction information as the input, and determines the 12 driver pulses for the 12 IGBTs of the primary side matrix converter.

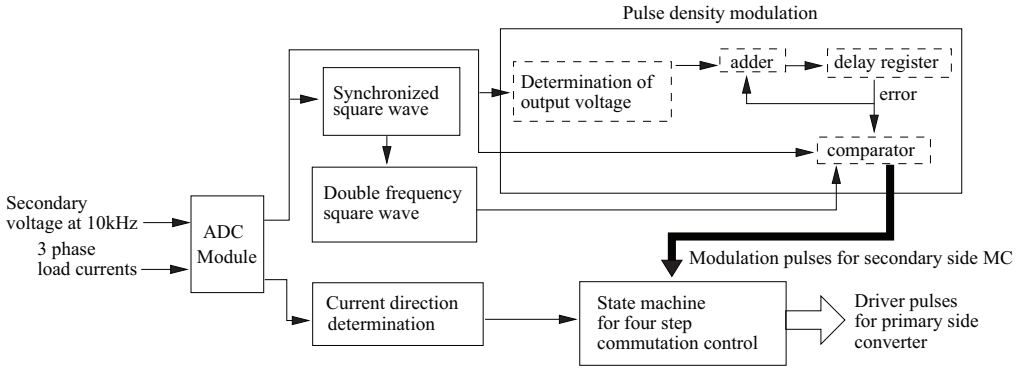

Figure 8.7: Block diagram of secondary side verilog control

Fig. 8.7 shows the block diagram of Verilog code to generate the pulses to control the secondary side matrix converter. As is seen from fig. 8.7 , it also has six modules and are explained below:

1. ADC module The Verilog code for ADC modules does the A/D conversion of the voltage at secondary side of the transformer, v_{filter} and the three phase load

currents sensed. The digital data of v_{filter} and three phase load currents are the output of this module.

2. Synchronized square wave This module generates a square wave at $10kHz$ which is in synchronization with v_{filter} . The square wave is needed to do zero voltage switching in the secondary side matrix converter.

3. Double frequency square wave For pulse density modulation at $10kHz$, a clock is needed which is in synchronization with v_{filter} i.e. at every zero crossing of the voltage a pulse is generated. This is obtained by doubling the frequency of the synchronized square wave at $10kHz$ in the previous module.

4. Pulse density modulation Discrete integration is used for the implementation of pulse density modulation. First the output voltage value, say v_{out}, at each individual phase is determined based on the output of the pulse density block and the value of v_{filter} . Suppose the reference voltage is v_{ref}. At every rising edge of the $50MHz$ clock, the v_{out} is subtracted from v_{ref} and the error is added to the error at the previous clock edge. Or in other words the error is accumulated by adding the current error with the previous error. The accumulated error is stored in a register which acts as a delay block and holds the error for the next clock edge i.e. it stores the previous error. The output of the delay block is compared with zero. For every zero crossing of v_{filter} , and for a positive value of v_{filter}, if the error is positive is positive then the lower bi-directional switch is turned ON otherwise the upper bi-directional switch is turned ON. Similarly, for a negative value of v_{filter}, if the error is positive then the upper bi-directional switch is turned ON otherwise the lower bi-directional switch is turned ON.

5. Current direction determination The current direction determining module is the same as the one described for primary side control with the only difference that the direction of three load currents is determined.

6. State machine for four step commutation control Again, the state machine used works the same way as explained for primary side control.

8.1 Intermediary tests of hardware setup

The two matrix converters on the primary side and on the secondary side of the HF transformer are tested separately, before testing the full sinusoidal current HF transformer. Fig. 8.8 shows the primary side matrix converter. Fig. 8.9 and fig. 8.10 show the expermental results of test of MC1 with RL load of 10Ω and $1mH$ connected to the secondary of the HF transformer. MC1 is first tested with dead time control. Fig. 8.9 shows the voltage across the primary winding of the transformer and the transformer current with dead time. It can be seen that during the dead time the voltage across the primary winding of the transformer is the clamp circuit voltage. Fig. 8.10 shows the experimental results with four step commutation control. It can be seen that the clamp circuit voltage is absent in fig. 8.10.

Fig. 8.11 shows the secondary side matrix converter. MC2 is first tested for a single leg with RL load of 10Ω and $44.5mH$. Pulse density modulation with four step commutation control is used. Supply voltage at $1kHz$ are provided from a programmable power supply. The load current and the output voltage at frequency of $50Hz$ are shown in fig. 8.12. Fig. 8.13 shows the experimental results for test of full MC2 with three phase RL load.

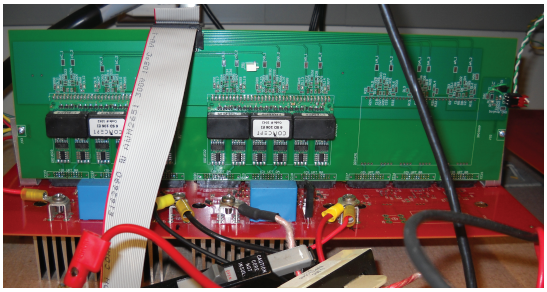

Figure 8.8: Primary side MC

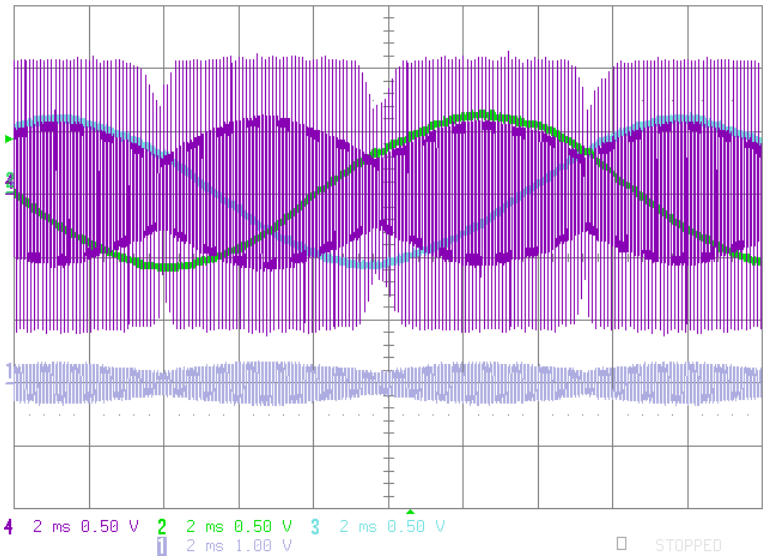

Figure 8.9: MC1 output voltage [50V/div] and transformer current [2.5A/div] with dead time

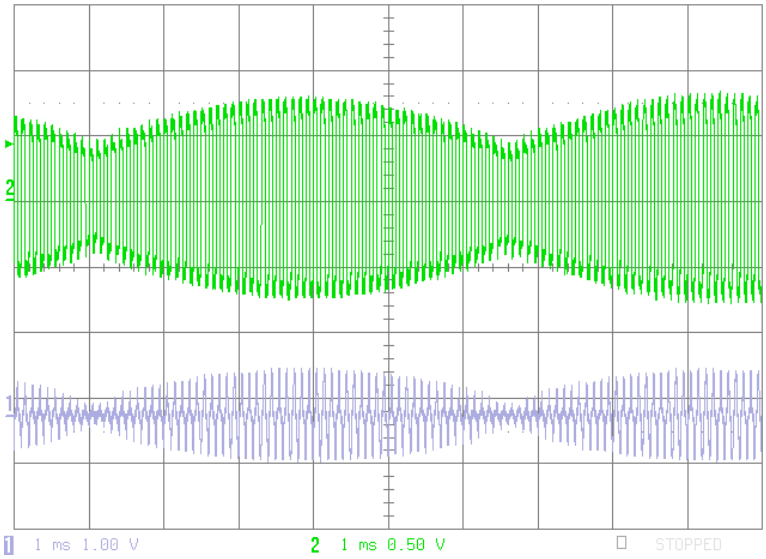

Figure 8.10: MC1 output voltage [50V/div] and transformer current [2.5A/div] with four step commutation control

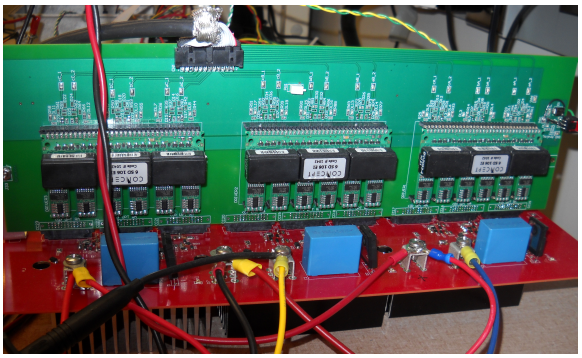

Figure 8.11: Secondary side MC

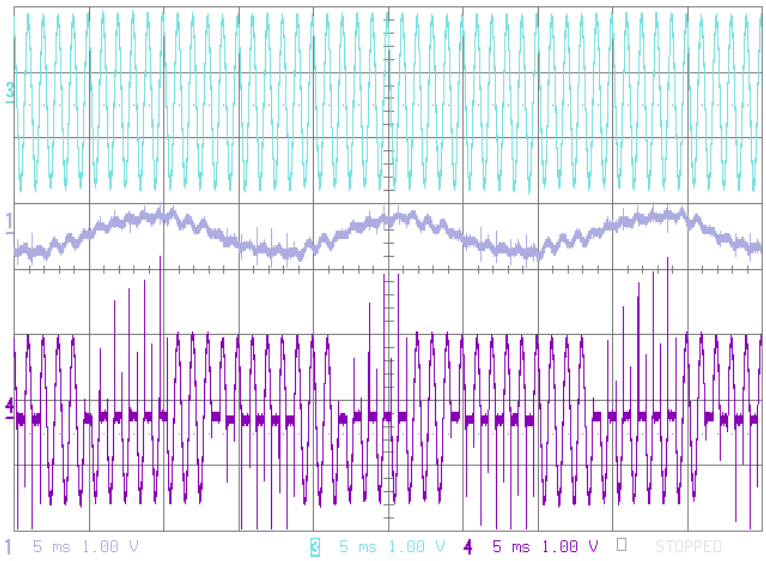

Figure 8.12: Supply voltage[50V/div] at 1kHz, load current [1A/div] and output voltage [50V/div] for MC2

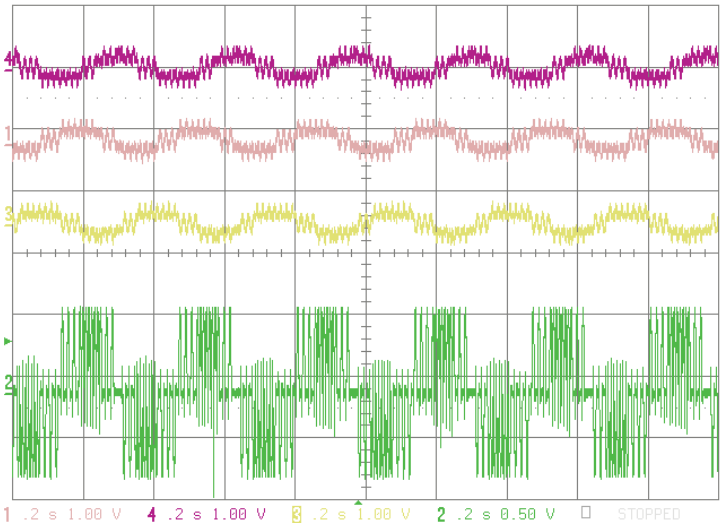

Figure 8.13: Three phase load currents and load voltage for test of MC2 modulation at 1kHz

8.2 Experimental results

Experiments are performed, on the hardware implemented explained above, at a supply voltage of $100V$ peak and 60 Hz frequency and a output frequency of $50Hz$ with a star connected RL load of 10Ω and $22.5mH$. The filter inside the programmable ac supply is used to filter the switched frequency harmonics in supply current, no additional input filter is added for experiments. Fig. 8.14 and fig. 8.15 show the voltage v_{switch} and v_{filter}, obtained at the output of primary side matrix converter and the input voltage of MC2 $10kHz$. Fig. 8.16 and fig. 8.17 show the transformer voltage current and input voltage of MC2, v_{filter} at $10kHz$. Fig. 8.18 shows output voltages across one of the phases of the 3 phase load and the three phase load currents at $50Hz$ for pulse density modulation.

It can be seen from fig. 8.14 that the voltage applied to the primary of the transformer is a square wave voltage at $10kHz$, with its amplitude varying as the envelop of the line to line supply voltages, and the current flowing in the transformer is a sinusoidal current. From fig. 8.15 and fig. 8.17, the voltage at the secondary of the transformer

winding is a sinusoidal voltage although the voltage at the primary of the transformer is a switched square wave. So, the filter formed with the transformer leakage inductance additional inductance of $1.16mH$ and capacitors at the secondary terminals the filters both the switched currents at the input of secondary side matrix converter MC2 and the switched voltage at the primary terminals of the HF transformer. From the output voltage of fig. 8.18 it can be seen that the MC2 is switched very close to zero voltages. Thus, the principle of sinusoidal current HF transformer is experimentally verified. Also as a $1.16mH$ inductance is added to form a low pass filter, it is verified that the switching frequency is independent of the value of leakage inductance of HF power transformers.

As is seen from fig. 8.18, the harmonic profile of load currents obtained is not purely sinusoidal. These experimental results can be improved and sinusoids with good harmonic profile can be obtained by use of very fast ADC and design of differential amplifiers used to sense the voltage v_{filter}. Accurate sensing of v_{filter} and efficient synthesizable verilog codes are important for proper operation of pulse density modulation.

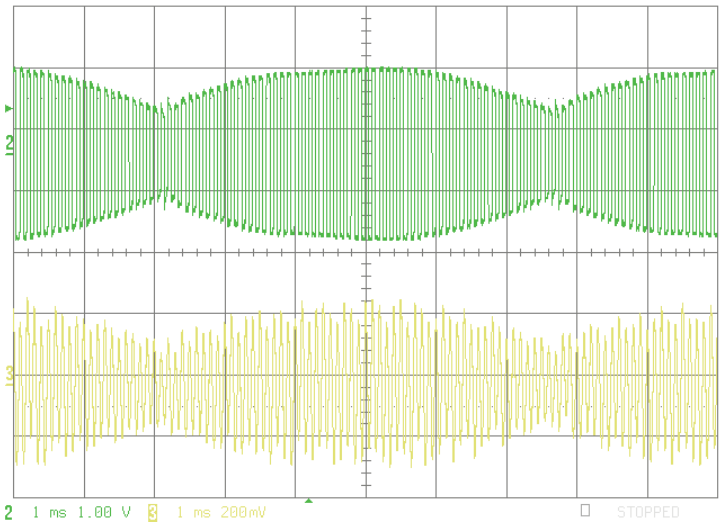

Figure 8.14: Transformer primary voltage [50V/div] and input voltage of MC2 [10V/div] at 10kHz

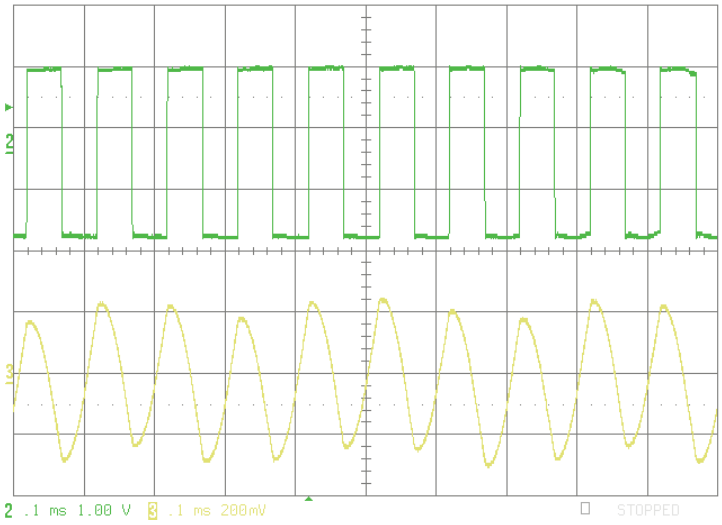

Figure 8.15: Zoomed transformer primary voltage [50V/div] and input voltage of MC2 [10V/div] at 10kHz

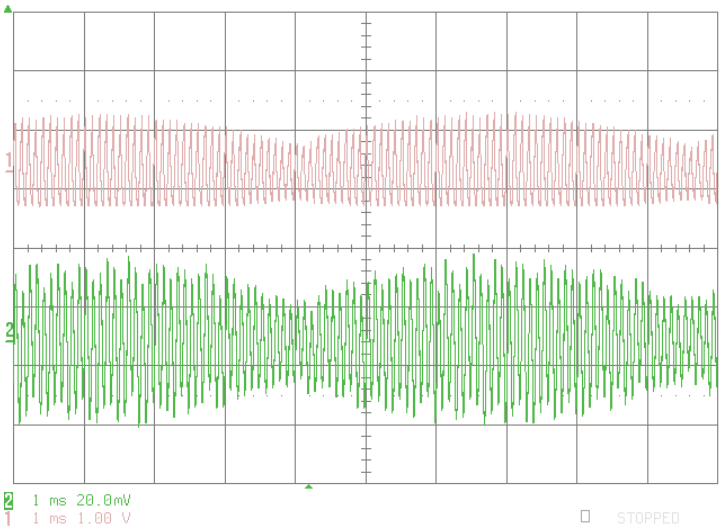

Figure 8.16: Transformer current [2.5A/div] and input voltage of MC2 [10V/div] at 10kHz

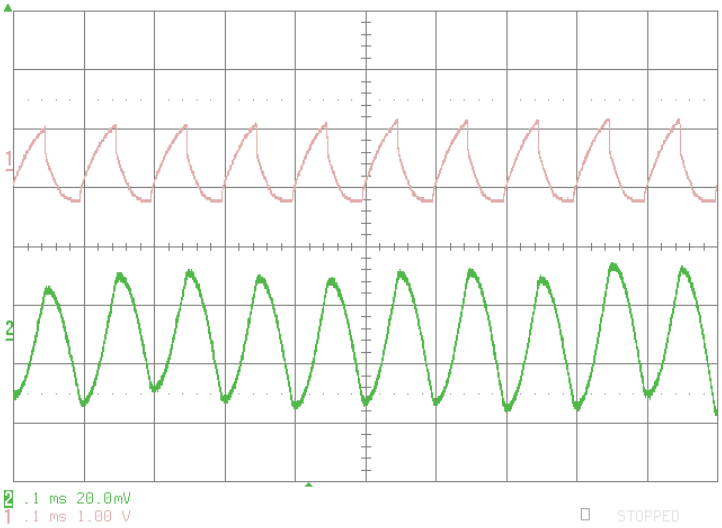

Figure 8.17: Zoomed Transformer current [2.5A/div] and input voltage of MC2 [10V/div] at 10kHz

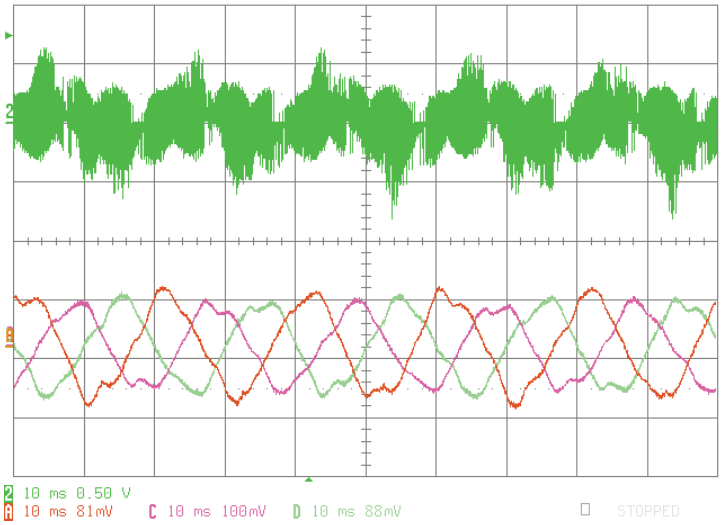

Figure 8.18: Load voltage [25V/div] and three phase load currents [1.5A/div]

8.3 Conclusion

A laboratory prototype of sinusoidal current HF transformer is implemented. The experimental results obtained shows sinusoidal currents flowing in the transformer. So, the sinusoidal current transformer topology gives a solution of problem of leakage inductance in HF transformers.

Chapter 9

Summary and Future work

High frequency transformers provide an alternative for modern 60Hz power transformers, in applications like wind energy conversion and electric ship, where weight and volume of transformers is a limitation. AC-DC-AC based PET has the disadvantage of bulky storage capacitors and large reactive elements for filtering which reduce the reliability, efficiency and increase the weight and volume of overall PET. Direct AC to AC based PET using matrix converters overcome these disadvantages because of absence of storage elements. The scope of matrix converter based PET is explored in this thesis, by first analyzing and simulating a matrix converter based PET with open ended primary and second by addressing the issue of leakage inductance. The problem of leakage inductance in matrix converter based is addressed by proposing a source based commutation method and three novel topologies based on sinusoidal HF transformer. In the sinusoidal HF transformers, the switching frequency is independent of the value of leakage inductance. Some of the important conclusions are discussed in the following sections.

9.1 Matrix converter based PET with open ended primary

A matrix converter based PET with open ended primary is described in chapter 2. It has the salient features of 1.5 voltage transfer ratio, bi-directional power flow, elimination of bulky storage capacitors, controllable output voltage and frequency, controllable input power factor and zero common mode voltage. The use of rotating space vectors of matrix

converters, for the modulation of all three matrix converters, give zero common mode voltage. Common mode voltage is a concern in several drives applications. Zero common mode voltage is not possible in AC-DC-AC based PET. The open ended primary and use of two matrix converters at the primary side, increases the voltage transfer ratio to 1.5 as compared to 0.866 achievable by single matrix converter systems. Also delay in commutation of current due to transformer leakage inductance in primary side is avoided.

9.2 Problem of leakage inductance

The use of matrix converter in the secondary side of the HF transformer, leads to flow of switched current in the HF transformer. The transformer current cannot change instantaneously because of the leakage inductance of the HF transformer. An alternative path needs to be provided for the commutation of current in the leakage inductance. A clamp circuit is connected at the secondary of the transformer to provide this alternative path in the matrix converter based PET discussed in chapter 2. The time needed for the current to change its direction in the transformer winding is termed as commutation time. During the commutation time, the clamp circuit voltage appears at the output of the third matrix converter. This leads to output voltage loss. This effect increases with increase in value of leakage inductance and increase in switching frequency. The drop in voltage regulation with increase in leakage inductance and switching frequency is studied in chapter 3. Also the energy stored in clamp capacitor during commutation time needs to be recovered, otherwise it leads to severe drop in efficiency of the PET. So, clamp circuits can be used only with energy recovery systems.

9.3 Source based commutation

Depending on the direction of the current, the current in the leakage inductances can also be commutated by applying the appropriate voltages from the primary side matrix converters. This is termed as source based commutation method and is explained in chapter 4. This eliminates the need of clamp circuits and therefore, energy recovery circuits and increases the efficiency of the overall PET significantly. Also, as the supply

voltages are applied during the commutation time, the output voltage waveform becomes cleaner.

9.4 Sinusoidal HF transformers

The commutation time is decided by the value of leakage inductance and the maximum of the supply voltage. So, higher the value of leakage inductance, larger is the commutation time period and therefore, lower is the switching frequency. Thus, although the overall efficiency of the PET is improved by source based commutation but the voltage regulation is still affected and the switching frequency is still limited by the value of leakage inductance.

The main idea behind using PET is to reduce size of power transformers. The nanocrystalline materials such as FINEMET used for making HF transformers have very low core losses even at very high operating frequencies of 100kHz. SiC carbide devices are also available which have very low switching losses at very high frequencies. Thus, the switching frequency and therefore, the size of HF transformers is only limited by the value of leakage inductance.

Chapter 5, chapter 6 and chapter 7 proposes three sinusoidal HF transformer based PET where the switching frequency is made independent of the value of leakage inductance. In all these topologies, the leakage inductance is used to form a low pass filter with a capacitor connected at the secondary terminals of the HF transformer. As the low pass filters operate at very high frequencies of 10kHz or above, the size of the reactive elements required becomes very small.

Chapter 5 proposes a sinusoidal input output three phase HF transformer. Chapter 6 proposes a sinusoidal input output three winding HF transformer and Chapter 7 proposes a sinusoidal current HF transformer. In the topologies proposed in chapter 5 and chapter 6, a low pass filter is connected at the primary side of the transformer to convert the HF square wave voltage into a HF sine wave voltage. And capacitors are connected at the secondary side of the transformer to filter the switched input current of the secondary side matrix converter. Thus, the primary side filter filters the switched voltage and the secondary side filter filters the switched current. Hence, the HF transformer sees a sinusoidal voltages and sinusoidal currents at high frequency

on both primary and secondary sides like a 60 Hz power transformer. The switching frequency of the matrix converter is the same as the operating frequency of the HF transformer; therefore, both the capability of high frequency magnetic materials and power devices is utilized.

The topology described in chapter 5 utilizes a three phase transformer, two matrix converters and three phase filter at both primary and secondary sides. Whereas, the topology described in chapter 6 uses a three winding transformer with a three phase to single phase matrix converter on primary side and a matrix converter on secondary side with two capacitors on the secondary terminals. This reduces the switch count and also the no. of reactive elements required for the overall PET proposed in chapter 6. Also zero common mode is achievable with the sinusoidal input output three winding HF transformer.

The sinusoidal current HF transformer proposed in chapter 7 is different from that proposed in chapter 5 and chapter 6. It has a single phase transformer and uses only one capacitor at the terminal of the secondary of the transformer. The transformer sees square wave voltage at primary side and sinusoidal voltage at the secondary side. Sinusoidal currents flow through the transformer. Thus, the filter, formed with the capacitor and leakage inductance, filters both the square wave voltage and switched currents. There is no filter at the primary side of the HF transformer. So, only one additional reactive element is required for the operation of the PET. One of the limitations of the sinusoidal HF based topologies is that the transformer currents become high because of filter action. Good design of filter is very important for the proper operation of these topologies. The switching frequency is unaffected by high values of leakage inductance and is verified with experiments, for sinusoidal current HF transformer.

9.5 Future work

The future scope of this thesis includes the following:

1. Pulse density modulation used for sinusoidal current HF transformer can be modified with space vector pulse density modulation (SVPDM) [41–48]. Use of SVPDM gives more control on the selection of power devices to be switched. Also, the capacitor switched current can be modified which is not possible with PDM.

2. In sinusoidal current HF transformer the transformer voltage changes with change in load. Closed loop control is needed for regulating the voltage for load changes in the output side.

3. As the transformer sees square wave voltage at primary side and sinusoidal voltage at the secondary side, the transformer design for sinusoidal current HF transformer will be different than normal power transformer design. So, the transformer design needs to be explored.

4. For good filter design, the exact equivalent circuit of the HF transformer is needed. The HF transformers have stray capacitances which affect the filter performance and the commutation time in source based commutation. A study of parametric analysis of HF transformers is needed.

5. All the topologies proposed in this thesis can be implemented and compared.

Bibliography

[1] N. Burany. Safe control of four-quadrant switches. In *Industry Applications Society Annual Meeting, 1989., Conference Record of the 1989 IEEE*, pages 1190 –1194 vol.1, oct. 1989.

[2] W. A. Reass, D. M. Baca, and R. F. Gribble. Design and application of polyphase resonant converter modulators. `http://www.aps.anl.gov/News/Conferences/2006/CWHAP06/presentations/Reass.pdf`.

[3] Hitachi. Nanocrystalline soft magnetic material finemet. `http://www.hilltech.com/pdf/hl-fm10-cFinemetIntro.pdf`.

[4] L. Empringham, P.W. Wheeler, and J.C. Clare. Intelligent commutation of matrix converter bi-directional switch cells using novel gate drive techniques. In *Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE*, volume 1, pages 707 –713 vol.1, 1998.

[5] A. Prasai, Jung-Sik Yim, D. Divan, A. Bendre, and Seung-Ki Sul. A new architecture for offshore wind farms. *Power Electronics, IEEE Transactions on*, 23(3):1198 –1204, may 2008.

[6] T. Ericsen. The ship power electronic revolution: Issues and answers. In *Petroleum and Chemical Industry Technical Conference, 2008. PCIC 2008. 55th IEEE*, pages 1 –11, sept. 2008.

[7] T. Ericsen, N. Hingorani, and Y. Khersonsky. Power electronics and future marine electrical systems. *Industry Applications, IEEE Transactions on*, 42(1):155 – 163, jan.-feb. 2006.

[8] H. Iman-Eini, S. Farhangi, J.-L. Schanen, and J. Aime. Design of power electronic transformer based on cascaded h-bridge multilevel converter. In *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on*, pages 877 –882, june 2007.

[9] Chuanhong Zhao, S. Lewdeni-Schmid, J.K. Steinke, M. Weiss, T. Chaudhuri, M. Pellerin, J. Duron, and P. Stefanutti. Design, implementation and performance of a modular power electronic transformer (pet) for railway application. In *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pages 1 –10, 30 2011-sept. 1 2011.

[10] F.N. Mazgar, M.T. Hagh, and E. Babaei. Distribution electronic power transformer with reduced number of power switches. In *Power Electronics and Drive Systems Technology (PEDSTC), 2012 3rd*, pages 324 –329, feb. 2012.

[11] M.R. Banaei and E. Salary. Power quality improvement based on novel power electronic transformer. In *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd*, pages 286 –291, feb. 2011.

[12] Zhibing Wang and Kunshan Yu. The research of power electronic transformer (pet) in smart distribution network. In *Power System Technology (POWERCON), 2010 International Conference on*, pages 1 –7, oct. 2010.

[13] D. Wang, Chengxiong Mao, Jiming Lu, Shu Fan, and Luonan Chen. The research on characteristics of electronic power transformer for distribution system. In *Transmission and Distribution Conference and Exhibition: Asia and Pacific, 2005 IEEE/PES*, pages 1 –5, 2005.

[14] D. Wang, C. Mao, and J. Lu. Modelling of electronic power transformer and its application to power system. *Generation, Transmission Distribution, IET*, 1(6):887 –895, nov. 2007.

[15] E.R. Ronan, S.D. Sudhoff, S.F. Glover, and D.L. Galloway. A power electronic-based distribution transformer. *Power Delivery, IEEE Transactions on*, 17(2):537 –543, apr 2002.

[16] H. Wrede, V. Staudt, and A. Steimel. Design of an electronic power transformer. In *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]*, volume 2, pages 1380 – 1385 vol.2, nov. 2002.

[17] L. Heinemann and G. Mauthe. The universal power electronics based distribution transformer, an unified approach. In *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, volume 2, pages 504 –509 vol.2, 2001.

[18] Jin Ai-juan, Li Hang-tian, and Li Shao-long. A new matrix type three-phase four-wire power electronic transformer. In *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pages 1 –6, june 2006.

[19] H. Mirmousa and M.R. Zolghadri. A novel circuit topology for three-phase four-wire distribution electronic power transformer. In *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on*, pages 1215 –1222, nov. 2007.

[20] M. Kang, P.N. Enjeti, and I.J. Pitel. Analysis and design of electronic transformers for electric power distribution system. *Power Electronics, IEEE Transactions on*, 14(6):1133 –1141, nov 1999.

[21] K.K. Mohapatra and N. Mohan. Matrix converter fed open-ended power electronic transformer for power system application. In *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century, 2008 IEEE*, pages 1 –6, july 2008.

[22] K. Basu, R.K. Gupta, S. Nath, G.F. Castelino, K.K. Mohapatra, and N. Mohan. Research in matrix-converter based three-phase power-electronic transformers. In *Power Electronics Conference (IPEC), 2010 International*, pages 2799 –2803, june 2010.

[23] R.K. Gupta, K.K. Mohapatra, and N. Mohan. A novel three-phase switched multi-winding power electronic transformer. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 2696 –2703, sept. 2009.

[24] K. Basu, A. Somani, K.K. Mohapatra, and N. Mohan. A three-phase ac/ac power electronic transformer-based pwm ac drive with lossless commutation of leakage energy. In *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on*, pages 1693 –1699, june 2010.

[25] J. Rodriguez, M. Rivera, J.W. Kolar, and P.W. Wheeler. A review of control and modulation methods for matrix converters. *Industrial Electronics, IEEE Transactions on*, 59(1):58 –70, jan. 2012.

[26] P.W. Wheeler, J. Rodriguez, J.C. Clare, L. Empringham, and A. Weinstein. Matrix converters: a technology review. *Industrial Electronics, IEEE Transactions on*, 49(2):276 –288, apr 2002.

[27] T. Friedli, S.D. Round, and J.W. Kolar. A 100 khz sic sparse matrix converter. In *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, pages 2148 –2154, june 2007.

[28] L. Huber and D. Borojevic. Space vector modulated three-phase to three-phase matrix converter with input power factor correction. *Industry Applications, IEEE Transactions on*, 31(6):1234 –1246, nov/dec 1995.

[29] K.K. Mohapatra and N. Mohan. Open-end winding induction motor driven with matrix converter for common-mode elimination. In *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, pages 1 –6, dec. 2006.

[30] S. Nath, K.K. Mohapatra, and N. Mohan. Output voltage regulation in matrix converter fed power electronic transformer for power systems application in electric ship. In *Electric Ship Technologies Symposium, 2009. ESTS 2009. IEEE*, pages 203 –206, april 2009.

[31] S. Nath, K.K. Mohapatra, K. Basu, and N. Mohan. Source based commutation in matrix converter fed power electronic transformer for power systems application. In *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on*, pages 1682 –1686, june 2010.

[32] R.J. Callanan, A. Agarwal, A. Burk, M. Das, B. Hull, F. Husna, A. Powell, J. Richmond, Sei-Hyung Ryu, and Qingchun Zhang. Recent progress in sic dmosfets and jbs diodes at cree. In *Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE*, pages 2885 –2890, nov. 2008.

[33] Jun Wang, Xiaohu Zhou, Jun Li, Tiefu Zhao, A.Q. Huang, R. Callanan, F. Husna, and A. Agarwal. 10-kv sic mosfet-based boost converter. *Industry Applications, IEEE Transactions on*, 45(6):2056 –2063, nov.-dec. 2009.

[34] Honggang Sheng, Zheng Chen, F. Wang, and A. Millner. Investigation of 1.2 kv sic mosfet for high frequency high power applications. In *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pages 1572 –1577, feb. 2010.

[35] Gangyao Wang, Xing Huang, Jun Wang, Tiefu Zhao, S. Bhattacharya, and A.Q. Huang. Comparisons of 6.5kv 25a si igbt and 10-kv sic mosfet in solid-state transformer application. In *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pages 100 –104, sept. 2010.

[36] S. Nath and N. Mohan. Sinusoidal input output three phase transformer. In *Grand Challenge in Modeeling and Simulation (GCMS), 2011*, June 2011.

[37] P.K. Sood, T.A. Lipo, and I.G. Hansen. A versatile power converter for high-frequency link systems. *Power Electronics, IEEE Transactions on*, 3(4):383 –390, oct 1988.

[38] P.K. Sood and T.A. Lipo. Power conversion distribution system using a high-frequency ac link. *Industry Applications, IEEE Transactions on*, 24(2):288 –300, mar/apr 1988.

[39] S. Nath and N. Mohan. A matrix converter fed sinusoidal input output three winding high frequency transformer with zero common mode voltage. In *Power Engineering, Energy and Electrical Drives (POWERENG), 2011 International Conference on*, pages 1 –6, may 2011.

[40] S. Nath and N. Mohan. A solid state power converter with sinusoidal currents in high frequency transformer for power system applications. In *Industrial Technology (ICIT), 2011 IEEE International Conference on*, pages 110 –114, march 2011.

[41] B. Jacob and M.R. Baiju. Spread spectrum modulation scheme for two-level inverter using vector quantised space vector-based pulse density modulation. *Electric Power Applications, IET*, 5(7):589 –596, august 2011.

[42] B. Jacob and M.R. Baiju. Vector quantized spread spectrum pulse density modulation for four level inverters. In *Industrial Electronics and Applications (ICIEA), 2011 6th IEEE Conference on*, pages 674 –679, june 2011.

[43] A. Hirota, S. Nagai, and M. Nakaoka. A novel delta-sigma modulated space vector modulation scheme using scalar delta-sigma modulators. In *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, volume 2, pages 485 – 489 vol.2, june 2003.

[44] A. Hirota, S. Nagai, and M. Nakaoka. A simple configuration reducing noise level three-phase sinewave inverter employing delta-sigma modulation scheme. In *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, page 5 pp., march 2006.

[45] A. Hirota, B. Saha, Sang-Pil Mun, and M. Nakaoka. An advanced simple configuration delta-sigma modulation three-phase inverter implementing space voltage vector approach. In *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE*, pages 453 –457, june 2007.

[46] A. Mertens. Performance analysis of three-phase inverters controlled by synchronous delta-modulation systems. *Industry Applications, IEEE Transactions on*, 30(4):1016 –1027, jul/aug 1994.

[47] J. Nieznanski, A. Wojewodka, and R.J. Chrzan. Comparison of vector sigma-delta modulation and space-vector pwm. In *Industrial Electronics Society, 2000. IECON 2000. 26th Annual Confjerence of the IEEE*, volume 2, pages 1322 –1327 vol.2, 2000.

[48] G. Luckjiff and I. Dobson. Hexagonal sigma; delta; modulators in power electronics. *Power Electronics, IEEE Transactions on*, 20(5):1075 – 1083, sept. 2005.

[49] Yashkawa. Matrix converter maturation and future prospects. In *Industrial Electronics, 2009. IECON '09. 35th Annual Conference of IEEE*, pages 4461 –4462, nov. 2009.

[50] I. Yamato and N. Tokunaga. Power loss reduction techniques for three phase high frequency link dc-ac converter. In *Power Electronics Specialists Conference, 1993. PESC '93 Record., 24th Annual IEEE*, pages 663 –668, jun 1993.

[51] S. Figarado, T. Bhattacharya, G. Mondal, and K. Gopakumar. Three-level inverter scheme with reduced power device count for an induction motor drive with common-mode voltage elimination. *Power Electronics, IET*, 1(1):84 –92, march 2008.

[52] R.K. Gupta, K.K. Mohapatra, A. Somani, and N. Mohan. Direct-matrix-converter-based drive for a three-phase open-end-winding ac machine with advanced features. *Industrial Electronics, IEEE Transactions on*, 57(12):4032 –4042, dec. 2010.

[53] Hongwu She, Hua Lin, Xingwei Wang, and Limin Yue. Damped input filter design of matrix converter. In *Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, pages 672 –677, nov. 2009.

[54] P.W. Wheeler, H. Zhang, and D.A. Grant. A theoretical and practical consideration of optimised input filter design for a low loss matrix converter. In *Electromagnetic Compatibility, 1994., Ninth International Conference on*, pages 138 –142, sep 1994.

[55] P. Wheeler and D. Grant. Optimised input filter design and low-loss switching techniques for a practical matrix converter. *Electric Power Applications, IEE Proceedings* -, 144(1):53 –60, jan 1997.

[56] S. Ferreira Pinto and J. Fernando Silva. Input filter design for sliding mode controlled matrix converters. In *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, volume 2, pages 648 –653 vol.2, 2001.

[57] M. hamouda, F. Fnaiech, and K. Al-Haddad. Input filter design for svm dual-bridge matrix converters. In *Industrial Electronics, 2006 IEEE International Symposium on*, volume 2, pages 797 –802, july 2006.

[58] K. Yamada, T. Higuchi, E. Yamamoto, H. Hara, T. Sawa, M.M. Swamy, and T. Kume. Filtering techniques for matrix converters to achieve environmentally harmonious drives. In *Power Electronics and Applications, 2005 European Conference on*, pages 10 pp. –P.10, 0-0 2005.

[59] K. Yamada, T. Higuchi, E. Yamamoto, H. Hara, T. Sawa, M.M. Swamy, and T. Kume. Integrated filters and their combined effects in matrix converter. In *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, volume 2, pages 1406 – 1413 Vol. 2, oct. 2005.

[60] T. Kume, K. Yamada, T. Higuchi, E. Yamamoto, H. Hara, T. Sawa, and M.M. Swamy. Integrated filters and their combined effects in matrix converter. *Industry Applications, IEEE Transactions on*, 43(2):571 –581, march-april 2007.

[61] Furong Liu, C. Klumpner, and F. Blaabjerg. Stability analysis and experimental evaluation of a matrix converter drive system. In *Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE*, volume 3, pages 2059 – 2065 Vol.3, nov. 2003.

[62] D. Casadei, G. Serra, A. Tani, A. Trentin, and L. Zarri. Theoretical and experimental investigation on the stability of matrix converters. *Industrial Electronics, IEEE Transactions on*, 52(5):1409 – 1419, oct. 2005.

[63] D. Casadei, J. Clare, Lee Empringham, G. Serra, A. Tani, A. Trentin, P. Wheeler, and L. Zarri. Large-signal model for the stability analysis of matrix converters. *Industrial Electronics, IEEE Transactions on*, 54(2):939 –950, april 2007.

[64] D. Casadei, G. Serra, and A. Tanl. A general approach for the analysis of the input power quality in matrix converters. In *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, volume 2, pages 1128 –1134 vol.2, jun 1996.

[65] Domenico Casadei, Mirko Ghirelli, Giovanni Serra, Angelo Tani, and Luca Zarri. Theoretical and experimental analysis of the line current in matrix converters. In *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, pages 781 –786, 30 2006-sept. 1 2006.

[66] E. Erdem, Y. Tatar, and S. Su andnter. Effects of input filter on stability of matrix converter using venturini modulation algorithm. In *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on*, pages 1344 –1349, june 2010.

[67] M. Catucci, J. Clare, and P. Wheeler. Predective control strategy for zcs single stage resonant converter. In *IEEE Industrial Electronics, IECON 2006 - 32nd Annual Conference on*, pages 2905 –2910, nov. 2006.

[68] A. Alesina and M.G.B. Venturini. Analysis and design of optimum-amplitude nine-switch direct ac-ac converters. *Power Electronics, IEEE Transactions on*, 4(1):101 –112, jan 1989.

[69] P.W. Wheeler, J.C. Clare, L. Empringharn, M. Bland, and M. Apap. Gate drive level intelligence and current sensing for matrix converter current commutation. *Industrial Electronics, IEEE Transactions on*, 49(2):382 –389, apr 2002.

[70] Robert W. Erickson and Dragan Maksimovic. *Fundamentals of Power Electronics*, chapter 19. Springer, 2nd, edition, 2001.

[71] Ned Mohan, Tore M. Undeland, and William P. Robbins. *Power Electronics: Converters, Applications, and Design*, chapter 9. Wiley, 3rd, edition, 2002.

[72] Marian K. Kazimierczuk and Dariusz Czarkowski. *Resonant Power Converters*. Wiley-IEEE Press, 2nd, edition, 2011.

[73] D.O. Neacsu. Igbt-based cycloconverters built of conventional current source inverter modules. In *Signals, Circuits and Systems, 2003. SCS 2003. International Symposium on*, volume 1, pages 217 –220 vol.1, 0-0 2003.

Appendix A

Matrix converter Input Filter design

A brief review of available literature [53–66] on MC filter design is as follows. The size and cost of LC filters required for matrix converters are investigated in [54], [55]. Filter design for different control method and for different topology of matrix converter are provided in [56], [57]. Integrated input filtering techniques for matrix converter are proposed in [58], [59]. A transfer function based approach to design input filter is adopted in [53]. However, the effect of only switched current of matrix converter, on filter design, is investigated in [53]. So, in present literature, a complete mathematical analysis based on transfer functions, and design procedure of the input filter of MC is not available.

This appendix presents a detailed theoretical analysis of the input filter design of MC. The expression for input impedance of matrix converter, in steady state, has been derived. A mathematical model for filter design, based on second order transfer functions, has been developed. The effect of poles and zeros, in terms of the filter parameters, is explained. Each transfer function is analyzed and its effect on filter performance is investigated. The analysis is proved by simulation in MATLAB/SIMULINK. A filter design procedure is also provided.

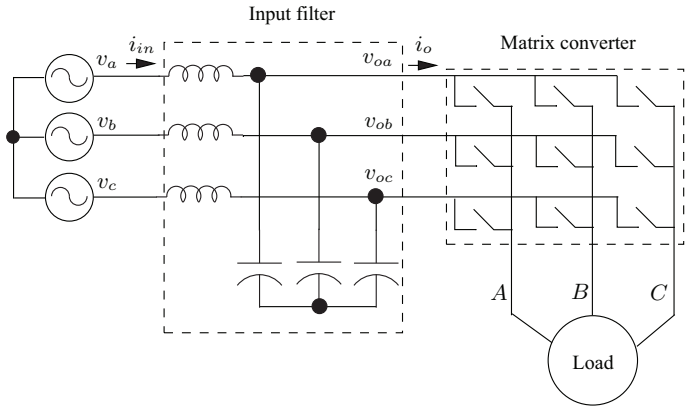

Figure A.1: Matrix converter with input filter

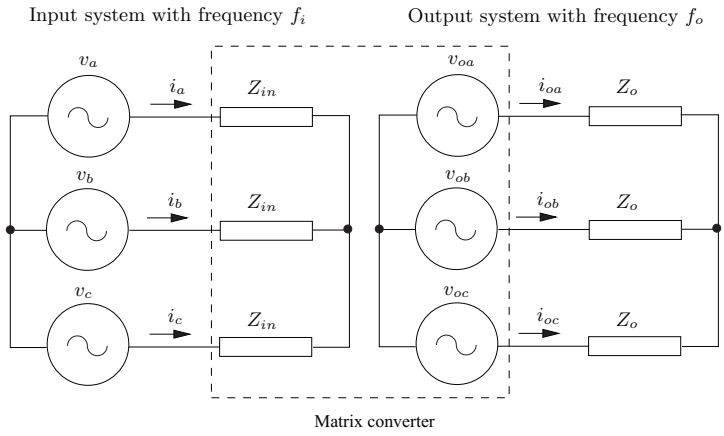

Figure A.2: Matrix converter as two separate systems at steady state

A.1 Input impedance of matrix converter

The design of EMI filters in DC to DC converters use expressions of input impedance. The input impedance of DC to DC converters is obtained by small signal analysis. But a small signal analysis is very complicated for three phase to three phase converters [61–63]. Therefore, steady state analysis is used to obtain an approximate expression

for input impedance of matrix converters. In steady state analysis, the effect of switching frequency harmonics is neglected. A matrix converter with load impedance, Z_o is considered. For the steady state analysis, the matrix converter system is viewed as two separate systems one input system with three voltage sources at frequency i, connected to input impedances Z_{in}, and second output system with three voltage sources at frequency o, connected to output impedance Z_o, shown in fig. A.2.

The steady state analysis is as follows. The input voltage equations are given by,

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = V_{im} \begin{bmatrix} cos(\omega_i t) \\ cos(\omega_i t + \frac{2\pi}{3}) \\ cos(\omega_i t + \frac{4\pi}{3}) \end{bmatrix} = Z_{in} \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{A.1}$$

And the output voltage equations are given by

$$\begin{bmatrix} v_{oa}(t) \\ v_{ob}(t) \\ v_{oc}(t) \end{bmatrix} = V_{im} \begin{bmatrix} cos(\omega_o t) \\ cos(\omega_o t + \frac{2\pi}{3}) \\ cos(\omega_o t + \frac{4\pi}{3}) \end{bmatrix} = Z_{in} \begin{bmatrix} i_{oa}(t) \\ i_{ob}(t) \\ i_{oc}(t) \end{bmatrix} \tag{A.2}$$

Where, q is the voltage transfer ratio and V_{im} is the peak value of input voltage. Equating instantaneous powers on input and output sides, we obtain

$$p_i(t) = p_o(t) \tag{A.3}$$

$$v_a(t)i_a(t) + v_b(t)i_b(t) + v_c(t)i_c(t) = v_{oa}(t)i_{oa}(t) + v_{ob}(t)i_{ob}(t) + v_{oc}(t)i_{oc}(t) \tag{A.4}$$

Substituting from (A.1) for $i_a(t), i_b(t), i_c(t)$ and from (A.2) for $i_{oa}(t), i_{ob}(t), i_{oc}(t)$ in (A.4), we get

$$\frac{{v_a}^2 + {v_b}^2 + {v_c}^2}{Z_{in}} = \frac{{v_{oa}}^2 + {v_{ob}}^2 + {v_{oc}}^2}{Z_o} \tag{A.5}$$

Since sum of square of three 120° shifted sine waves is equal to 1.5, therefore (A.5) can be written as

$$\frac{Z_{in}}{Z_o} = \frac{{v_{im}}^2 1.5}{q^2 {v_{im}}^2 1.5} \tag{A.6}$$

As the loads connected to a matrix converter are highly inductive, neglecting the resistance in Z_o, we obtain

$$Z_{in} = \frac{Z_o}{q^2} = \frac{\omega_o L}{q^2} \tag{A.7}$$

A matrix converter is simulated in MATLAB/SIMULINK, with a star connected R-L load of 10Ω and $10mH$, and supply voltage of $100V$, $60Hz$. To verify (A.7), the simulation is run multiple times, with fixed voltage transfer ratio of 0.4 and varying output frequency. For every simulation, FFT of input current is performed, using power GUI block of SIMULINK. The magnitude, of fundamental, of input current is used to calculate the input impedance ($Z_{in} = V_{im}/I_a$). Using these values, a graph is plotted between Z_{in} and f_o, and is shown in fig. A.3. Similarly, multiple simulations are run for fixed output frequency of $50Hz$ and varying voltage transfer ratio. The graph between Z_{in} and q is shown in fig. A.4. From fig. A.3 and fig. A.4, it can be seen that the input impedance, varies linearly with output frequency, and varies as inverse square with the voltage transfer ratio. Thus, (A.7) is verified.

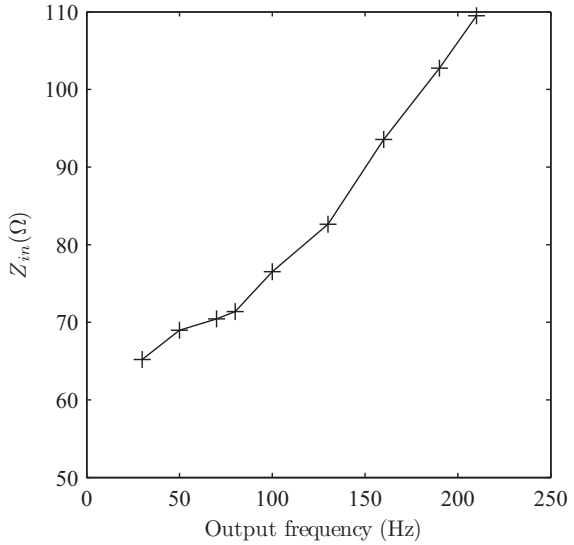

Figure A.3: Input impedance vs output frequency

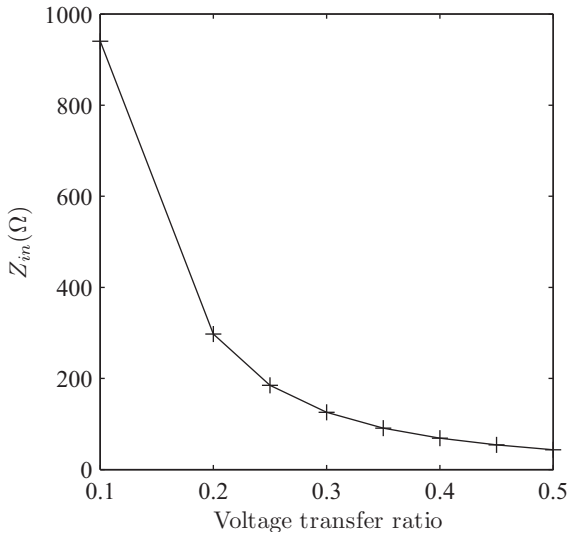

Figure A.4: Input impedance vs voltage transfer ratio

A.2 Mathematical model of input filter

Fig. A.5 shows the equivalent circuit for input filter design. R_l and R_c are the effective series resistance of inductor L and capacitor C respectively.

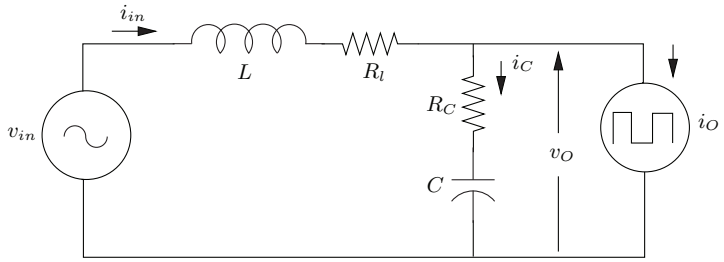

Figure A.5: Equivalent circuit

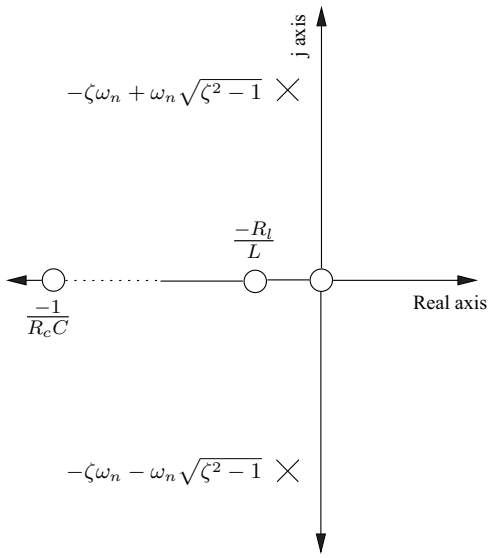

Figure A.6: Poles and zeros of input filter

The voltage and current equations are given by

$$V_{in}(s) - V_o(s) = (R_l + sL)I_{in}(s) \tag{A.8}$$

$$I_c(s) = I_{in}(s) - I_o(s) \tag{A.9}$$

$$V_o(s) = (R_c + \frac{1}{sC})I_c(s) \tag{A.10}$$

Substituting (A.8) and (A.9) in (A.10) and solving, we obtain

$$V_o(s) = \frac{sCR_c + 1}{s^2LC + sC(R_c + R_l) + 1}V_{in}(s) - \frac{s^2R_cLC + s(R_cR_lC + L) + R_l}{s^2LC + sC(R_c + R_l) + 1}I_o(s) \tag{A.11}$$

$$I_{in}(s) = \frac{sC}{s^2LC + sC(R_c + R_l) + 1}V_{in}(s) + \frac{sCR_c + 1}{s^2LC + sC(R_c + R_l) + 1}I_o(s) \tag{A.12}$$

The above equations contain four transfer functions. It can be converted to the familiar second order transfer functions by substituting cut off frequency, $\omega_n = \frac{1}{\sqrt{LC}}$ and damping ratio, $\zeta = \frac{R_c+R_l}{2}\sqrt{\frac{C}{L}}$. So,

$$V_o(s) = \frac{(sCR_c + 1){\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}V_{in}(s) - \frac{R_c(s + \frac{1}{R_cC}(s + \frac{R_l}{L})}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}I_o(s) \tag{A.13}$$

$$V_o(s) = T_{vv}(s)V_{in}(s) - T_{iv}(s)I_o(s) \tag{A.14}$$

$$I_{in}(s) = \frac{sC{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}V_{in}(s) + \frac{(sCR_c + 1){\omega_n}^2)}{s^2 + 2\zeta\omega_n s + {\omega_n}^2}I_o(s) \tag{A.15}$$

$$I_{in}(s) = T_{vi}(s)V_{in}(s) + T_{ii}(s)I_o(s) \tag{A.16}$$

The poles and zeros of the transfer functions are shown in fig. A.6. Since the values of R_l and R_c are very small, the system is marginally stable. The damping can be increased with slightly higher values of R_l and R_c.

A.3 Analysis of filter model

The effect of all four transfer functions is explained as follows.

A.3.1 $T_{vv}(s)$

As is seen from (14), $T_{vv}(s)$ is multiplied to $V_{in}(s)$. Since $V_{in}(s)$ is a sine wave of frequency $60Hz$, the gain of $T_{vv}(s)$ at $60Hz$ is only important. As shown in fig. A.7, the gain of $T_{vv}(s)$ is 1 at $60Hz$. Therefore, $T_{vv}(s)$ has no effect on $V_o(s)$.

A.3.2 $T_{iv}(s)$

Because of transfer function $T_{iv}(s)$, $I_o(s)$ affects $V_o(s)$. The bode plot of $T_{iv}(s)$ is shown in fig. A.8. The gain $T_{iv}(s)$ is very small at all frequencies except near cut off frequencies. Due to high gain of $T_{iv}(s)$, the harmonics present in $I_o(s)$, near cut off frequency, get amplified. This distorts the filter output voltage $V_o(s)$. Usually the effect of $T_{iv}(s)I_o(s)$ is negligible. So, $V_o(s)$ is obtained almost equal to $V_{in}(s)$.

A.3.3 $T_{vi}(s)$

From (16), since $T_{vi}(s)$ is multiplied to $V_{in}(s)$, gain of $T_{vi}(s)$ at $60Hz$ is only important. From the bode plot shown in fig. A.9, the gain at $60Hz$ is negative. In order to have minimum effect of $V_{in}(s)$ on $I_{in}(s)$, the gain of $T_{vi}(s)$ should be very small at $60Hz$. Thus, the effect of $T_{vi}(s)$ is to amplify the filter current $I_{in}(s)$.

Also, from the phase plot in fig. A.9, the current due to $V_{in}(s)$ i.e. $T_{vi}(s)V_{in}(s)$ has a phase shift of 90 deg. Since, the net phase of $I_{in}(s)$ is the sum of phases of fundamental

of $I_o(s)$ and current due to $V_{in}(s)$, the effect of phase of $T_{vi}(s)$ is important in power factor control of matrix converter.

A.3.4 $T_{ii}(s)$

Transfer function $T_{ii}(s)$ is same as $T_{vv}(s)$ and is shown in fig. A.7. $T_{ii}(s)$ has two effects. First, it filters the switching frequency harmonics of $I_o(s)$. And second it amplifies the harmonics of $I_o(s)$ present near cut off frequency. The amplification is due to the high gain of $T_{ii}(s)$ near cut off frequency. So, the cut off frequency should not be a multiple of supply frequency.

Thus, $I_{in}(s)$ contains harmonics near cut off frequency, in addition to fundamental $60Hz$ component of $I_o(s)$. For any value of L and C, it is not possible to remove cut off frequency harmonic components from $I_{in}(s)$. Therefore, the effect of $T_{ii}(s)$ is to distort the filter current $I_{in}(s)$. Unlike $T_{vi}(s)$, $T_{ii}(s)$ does not introduce any phase shift in the $60Hz$ component of $I_o(s)$.

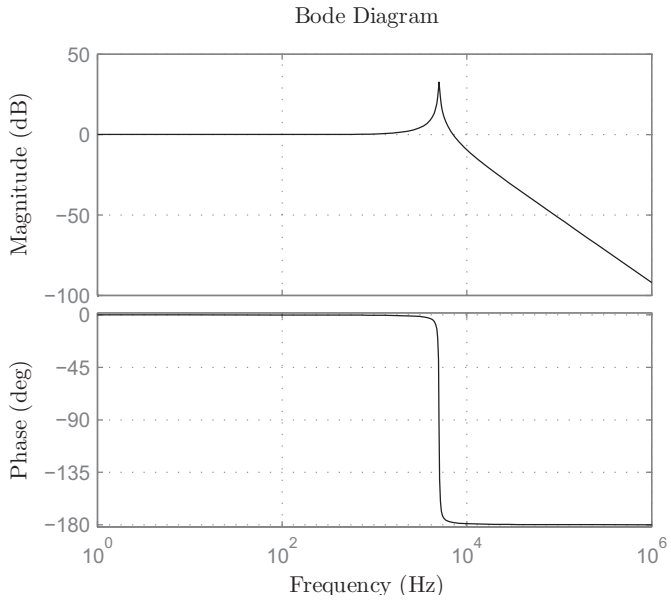

Figure A.7: Bode plot of $T_{vv}(s)$ and $T_{ii}(s)$

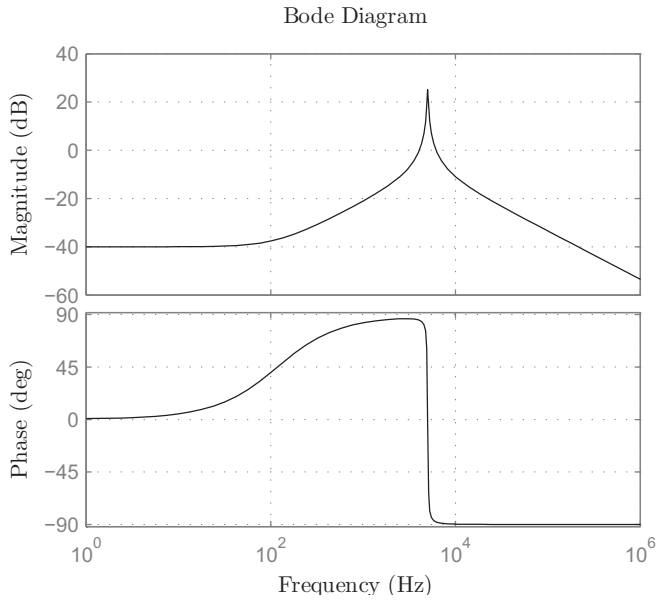

Figure A.8: Bode plot of $T_{iv}(s)$

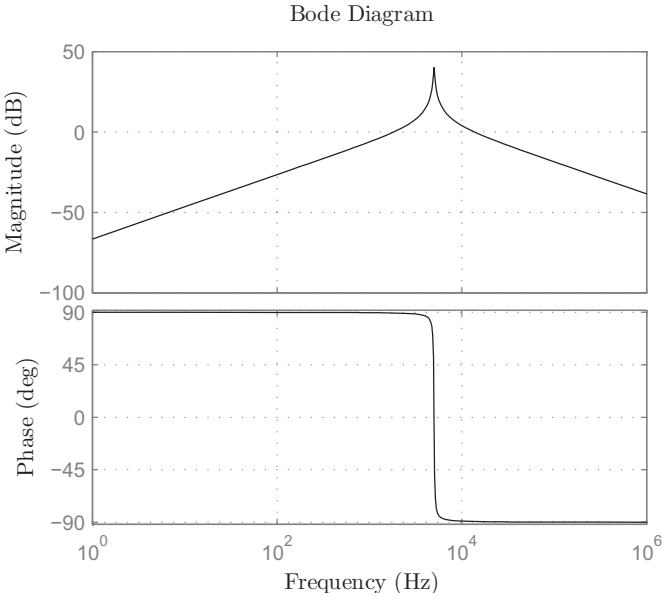

Figure A.9: Bode plot of $T_{vi}(s)$

A.4 Design procedure and simulation results

The effect of various parameters of the input filter is analyzed and the analysis is verified with simulation in MATLAB/SIMULINK. The system shown in fig. 1 is simulated for a R-L load of 10Ω and $10mH$, and supply voltage of $100V$, $60Hz$, using Venturinis modulation method for a switching frequency of $10kHz$. The values of R_l and R_c are taken as 0.01Ω and 0.001Ω respectively. The output frequency used is $60Hz$ and voltage transfer ratio used is 0.4. The load voltage and load current are shown in fig. A.10. The input current of matrix converter, I_o is shown in fig. A.11.

Filter design needs the selection of L and C. From section IV, $T_{vi}(s)$ leads to amplification in $I_{in}(s)$. The value of C is more important than the value of L. So for filter design, proper value of cut off frequency and C need to be chosen. ζ is very small and is decided by R_l and R_c.

The simulation is run multiple times, for filters with cut frequency $3kHz$ and different values of C. The bode plots of $T_{vi}(s)$ are shown in fig. A.12 and the simulation results of input current I_{in} is shown are fig. A.13. From the simulation results it is clearly seen that, as the value of C increases, the amplification in current I_{in} increases.

The reason is explained as follows. The amplification in current is due to the gain of $T_{vi}(s)$ at $60Hz$. Gain of $T_{vi}(s)$ at $60Hz$ is given by,

$$\left|T_{vi}(s)\right| = \left|\frac{sC{\omega_n}^2}{s^2+2\zeta\omega_n s+{\omega_n}^2}\right| = \frac{\omega C{\omega_n}^2}{\sqrt{({\omega_n}^2-\omega^2)^2+(2\zeta\omega_n\omega)^2}} = \frac{C2\pi 60{\omega_n}^2}{\sqrt{({\omega_n}^2-2\pi 60^2)^2+(4\pi 60\zeta\omega_n)^2}} \tag{A.17}$$

From the above expression, $\left|T_{vi}(s)\right|$ is directly proportional to value of C. Thus, increase in value of C will increase the amplification in current I_{in}.

Similarly, the simulation is run multiple times, for filters with value of C equal to $75\mu F$ and different values of cut off frequencies ω_n. The bode plots of $T_{ii}(s)$ are shown in fig. A.14 and the simulation results of input current I_{in} are shown in fig. A.15. From the simulation results it is observed that, as the value of ω_n increases, the distortion or high frequency harmonics in current I_{in} increases.

As explained in section IV, the distortion or high frequency harmonic content in I_{in} is due to high gain of $T_{ii}(s)$ near cut of frequencies. It can be seen in fig. 15 that as ω_n increases, the range of frequencies where gain is greater than 1 increase. (Please note

that frequency is shown on a logarithmic scale in fig. A.14). Thus, increase in value of ω_n will increase the distortion in current I_{in}.

Fig. A.16 shows the supply voltages V_A, V_B, V_C and filter output voltages V_{OA}, V_{OB}, V_{OC}. The filter output voltage follows very closely the supply voltage. Based on the above discussion, design of input filter can be put in two steps

1. Decide the cut off frequency depending on the switching frequency of matrix converter and the permissible amount of high frequency harmonic injection in supply current.

2. Decide the value of C depending on the current limit of the voltage supply and the value of load current.

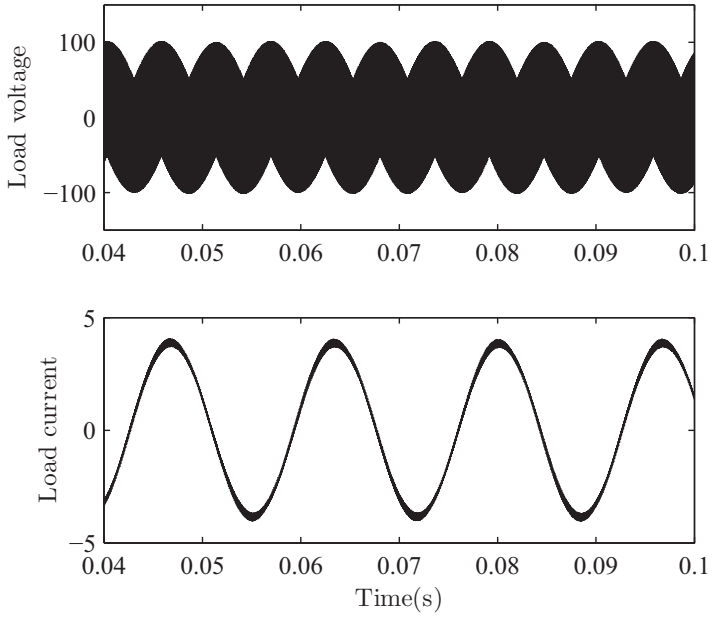

Figure A.10: Load voltage and load current

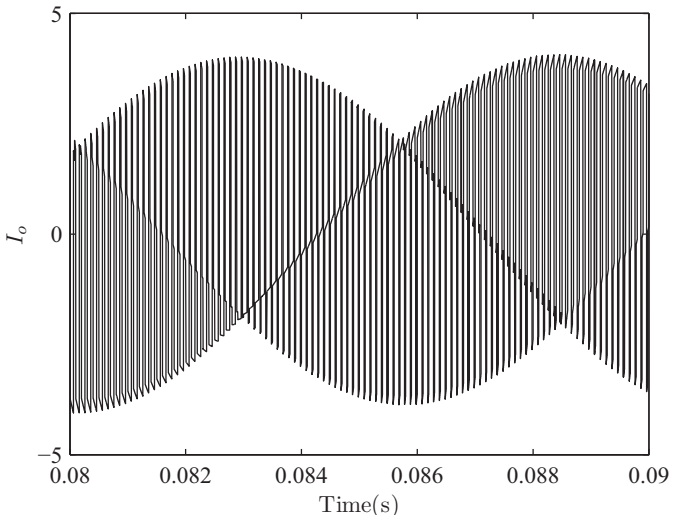

Figure A.11: Input current of matrix converter

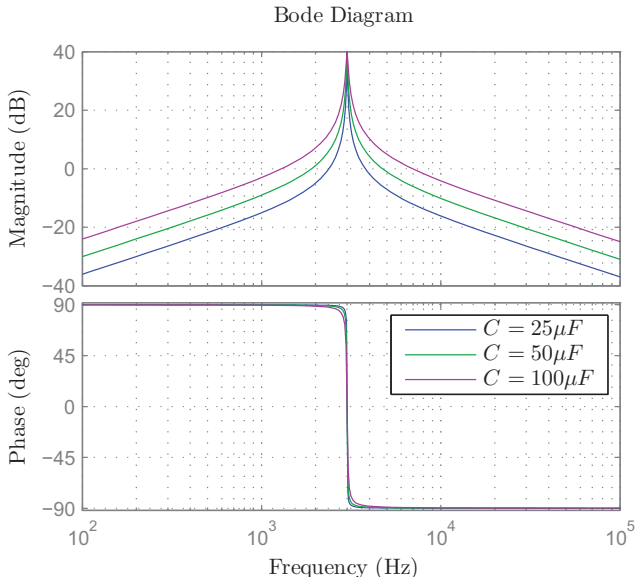

Figure A.12: Bode plots of $T_{vi}(s)$ for different values of C

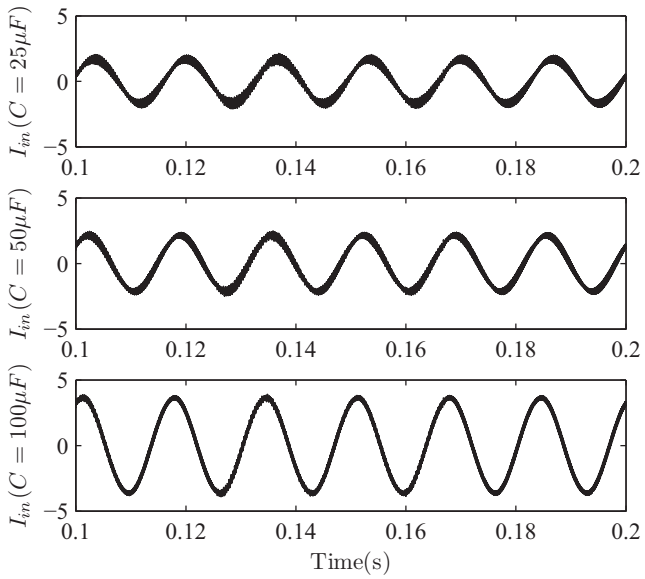

Figure A.13: Filter current for different values of C

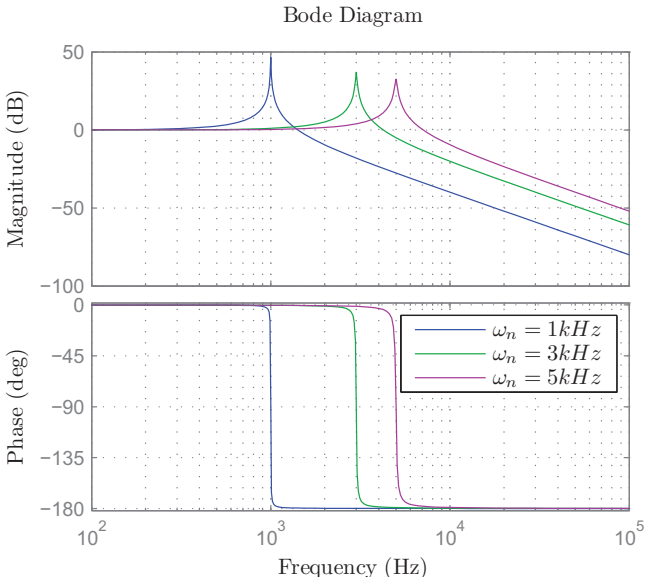

Figure A.14: Bode plots of $T_{ii}(s)$ for different values of cut off frequencies

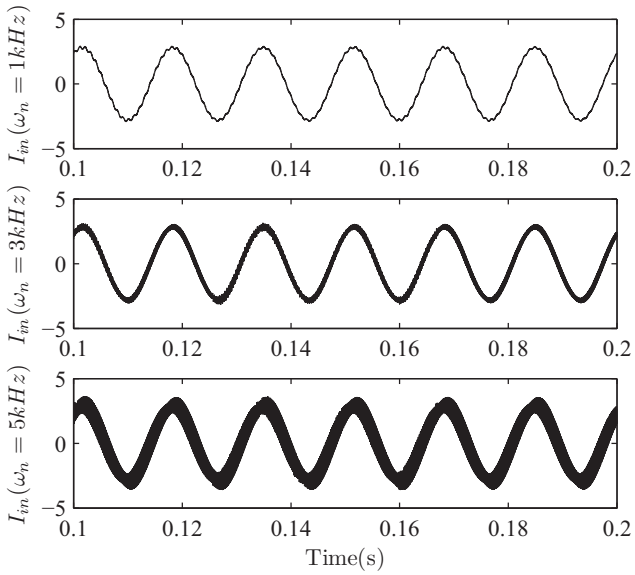

Figure A.15: Filter current for different values of cut off frequencies

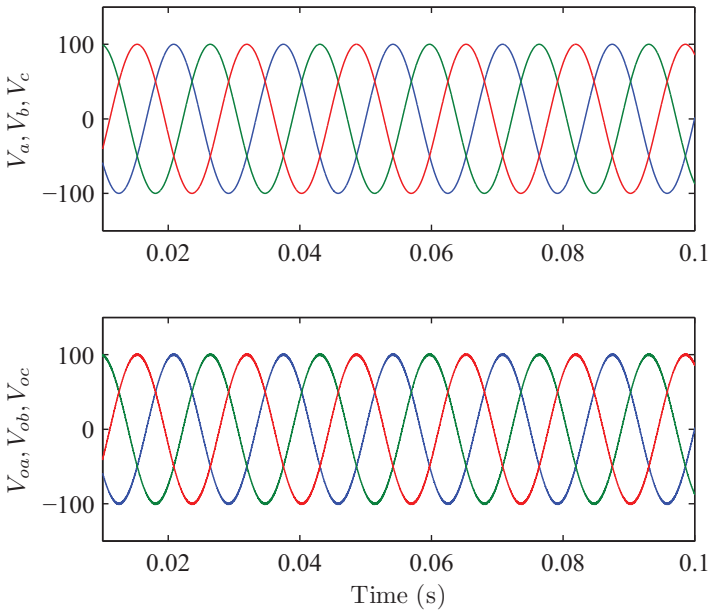

Figure A.16: Supply voltage and filter output voltage

A.5 Conclusion

A mathematical model, based on second order transfer function, is developed for the input filter design of matrix converter. The expression for input impedance of matrix converter is derived. The input impedance is directly proportional to output frequency and inversely proportional to voltage transfer ratio. The filter output voltage is almost equal to supply voltage for any design of input filter. The input current of filter is affected by the supply voltage, in addition to the harmonics present in switched current of matrix converter. The filter is designed in two steps: first deciding the cut off frequency and second deciding the value of filter capacitor.

The value of cut off frequency affects the harmonic content, and the value of capacitor affects the amplification, of input current of filter. The cut off frequency should not be a multiple of supply frequency. The input filter of matrix converter requires small values of inductor and relatively large values of capacitor.

Note: I acknowledge the contributions of Rashmi Prasad in the work presented in this appendix.

Appendix B

Commutation control of Matrix Converters

Commutation of current between bi-directional switches during switching is one of the important problems of matrix converters. The problem of commutation can be explained with help of fig. B.1. Fig. B.1 shows a two phase to single phase matrix converter. There are two basic rules for the operation of matrix converters:

1. 1 No two switches in a leg can be ON simultaneously as it leads to source to source short.

2. Since there is no freewheeling path in a matrix converter, so to avoid opening an inductive circuit, at least one switch in each leg needs to be ON.

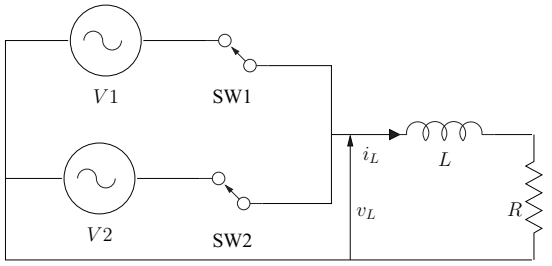

Figure B.1: Simple ckt to explain problem of commutation [1]

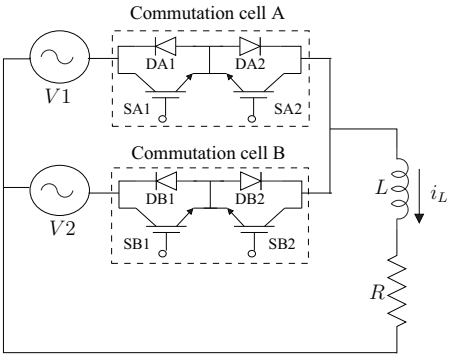

Figure B.2: Two phase to Single phase Matrix Converter

So, in fig. B.1, SW1 and SW2 cannot be OFF simultaneously i.e. a dead time cannot be provided nor SW1 and SW2 can be ON simultaneously i.e. an overlap needs to be avoided. This leads to the problem of commutation in matrix converter.

One of the methods to solve the problem of commutation is based on the direction of current. Fig. B.2 shows a two phase to single phase matrix converter with bi-directional cells A and B. Consider the direction of load current shown in fig. B.2 as positive. Suppose cell A is turned ON, then IGBT SA1 and diode DA2 or IGBT SA2 and diode DA1 conduct depending on the direction of current. So, at any instant, according to the direction of current, only two of the devices in a bi-directional cell are conducting. When a commutation from cellA to cell B is needed, only if SA1 and SB2 or SA2 and SB1 are turned ON simultaneously, it leads to a short circuit fault. Or if all four switches are turned OFF together then an open circuit fault occurs.

Therefore, there are only few switching combinations which are needed to be avoided. Commutation control is based on the elimination of hazardous switching combinations in matrix converter. Table B.1 shows the non-hazardous switching combinations.

Two types of commutation methods are widely used for matrix converters four step and two step. They are described below.

B.1 Four Step Commutation

The four step commutation cab be explained with the timing diagram shown in fig. B.3. Suppose at any instant the direction of current is positive and cell A is conducting. When

Table B.1: Non Hazardous Switching Combinations [1]

No.	SA1	SA2	SB1	SB2	sign of i_L
1.	1	1	0	0	+-
2.	0	0	1	1	+-
3.	1	0	0	0	+
4.	0	1	0	0	-
5.	0	0	1	0	+
6.	0	0	0	1	-
7.	1	0	1	0	+
8.	0	1	0	1	-

a commutation is needed from cell A to cell B, first the IGBT that is not conducting i.e. SA2 is turned OFF. After a short interval IGBT SB1 is turned ON. At this instant no source to source short happens as only positive direction of current flow is possible. When IGBT SB1 is completely ON, SA1 is turned OFF and finally SB2 is turned ON. So the commutation gets completed in four steps and open circuit and short circuit is avoided in all the four steps. The state diagram for four step commutation is showed in fig B.4.

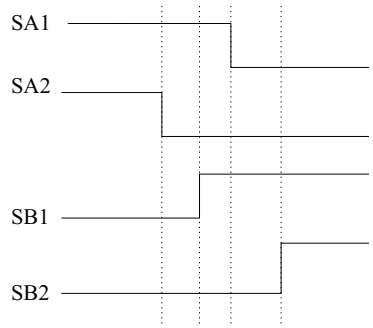

Figure B.3: Timing diagram for Four Step Commutation [4]

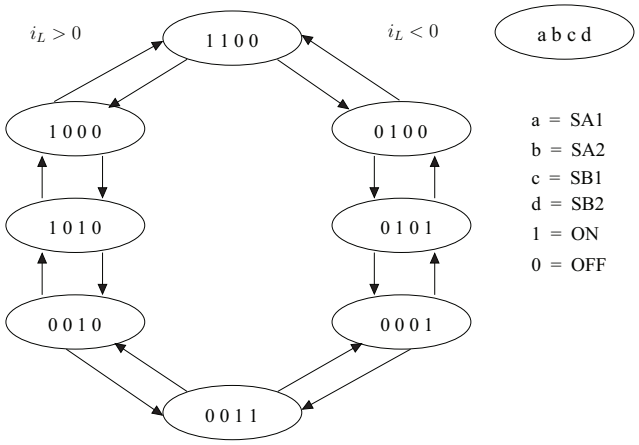

Figure B.4: State diagram for Four Step Commutation [4]

B.2 Two Step Commutation

The two step commutation can be explained with the help of fig. B.5. In two step commutation at any instant, depending on the direction of the current, only one IGBT in a bi-directional cell is turned ON. So, the commutation is possible in two steps as the extra steps of turning OFF and turning ON of two IGBTs are removed.

But when the value of current is very small i.e. near zero crossing, the LEM sensors cannot determine the direction of current properly. So for very low value of current a threshold is decided in which a LEM sensor can give erroneous information of current. When the current enters the threshold region, both the IGBTs in a bi-directional cell are turned ON and no commutation is allowed till the current comes out of the threshold region. This affects the harmonic profile of the current. Since the commutation is performed in two steps matrix converters can be operated with higher switching frequencies with two step commutation.

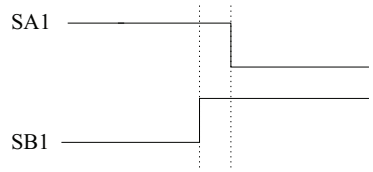

Figure B.5: Timing diagram for Two step Commutation for known Current direction [4]

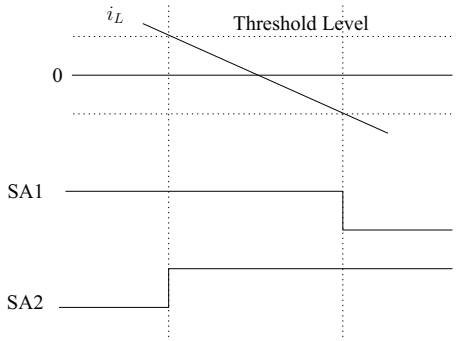

Figure B.6: Current reversal by threshold [4]

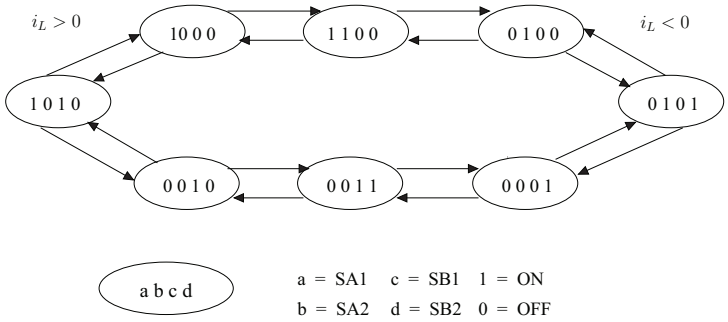

Figure B.7: State diagram for Two Step Commutation with Current Sensing [4]

Appendix C

Verilog Program

The verilog programs used for the experiments of sinusoidal current HF transformer are provided in this appendix. Two different codes are used for the control of secondary side matrix converter. Both of them are shown in a common test bench file. The verilog codes of modules adc_two, adc_one_test_secondary, adc_one_secondary_current_meas are similar to the verilog codes of adc_one_test. Also, the verilog codes of modules four_step2x1 and check_pulse_secondary are similar to the verilog codes of four_step_basic and check_pulse respectively.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
//
// Create Date:    15:36:47 02/27/2012
// Design Name:
// Module Name:    sine_current_HF_tb
//
// Two different types of codes are provided for the secondary side matrix converter.
// The changes to be made in the signal declarations are indicated by comments wherever
necessary.
//
//////////////////////////////////////////////////////////////////////////////////
module sine_current_HF_tb(clk,
DINA3, DINA4, DINB3, DINB4,
CONVST_b3, CONVST_b4,
SCLK3, SCLK4, CS_b3, CS_b4,

SA_up_a_corr, SB_up_a_corr, SC_up_a_corr,
SA_low_a_corr, SB_low_a_corr, SC_low_a_corr,

SA_up_b_corr, SB_up_b_corr, SC_up_b_corr,
SA_low_b_corr, SB_low_b_corr, SC_low_b_corr,

////////////////////////////////////////////////
//Secondary side ports
DINA, DINB, CONVST_b, SCLK, CS_b, //replace with line 35 and 36 for alternative code
//DINA1, DINB1, CONVST_b1, SCLK1, CS_b1,
//DINA2, DINB2, CONVST_b2, SCLK2, CS_b2,

sa1_leg1_corr, sa3_leg1_corr, sb1_leg1_corr, sb3_leg1_corr,
sa1_leg2_corr, sa3_leg2_corr, sb1_leg2_corr, sb3_leg2_corr,
sa1_leg3_corr, sa3_leg3_corr, sb1_leg3_corr, sb3_leg3_corr,

delay_pulse, out_sq, out_dataB,
signal_in

);

input clk;
input DINA3, DINA4;
input DINB3, DINB4;

wire SA_up_a, SB_up_a, SC_up_a, SA_low_a, SB_low_a, SC_low_a;
wire SA_up_b, SB_up_b, SC_up_b, SA_low_b, SB_low_b, SC_low_b;

output SA_up_a_corr, SB_up_a_corr, SC_up_a_corr, SA_low_a_corr, SB_low_a_corr,
SC_low_a_corr;
```

```
output SA_up_b_corr, SB_up_b_corr, SC_up_b_corr, SA_low_b_corr, SB_low_b_corr,
SC_low_b_corr;

output CONVST_b3, CONVST_b4;
output SCLK3, SCLK4;
output CS_b3, CS_b4;
wire curr_dir;

wire SA_up, SB_up, SC_up, SA_low, SB_low, SC_low;

wire out1;
wire [11:0] Vab, Vbc;
wire [11:0] Vca;
wire [1:0] max;
wire clkop;
wire rev_i_dir;

////////////////////////////////////////////////////////////////
//Secondary side definitions
output delay_pulse;

input DINA;
input DINB;
output CONVST_b;
output SCLK;
output CS_b;
output out_sq;

input signal_in;

wire reset;

wire sa1_leg1, sa3_leg1, sb1_leg1, sb3_leg1;
wire sa1_leg2, sa3_leg2, sb1_leg2, sb3_leg2;
wire sa1_leg3, sa3_leg3, sb1_leg3, sb3_leg3;

output sa1_leg1_corr, sa3_leg1_corr, sb1_leg1_corr, sb3_leg1_corr;
output sa1_leg2_corr, sa3_leg2_corr, sb1_leg2_corr, sb3_leg2_corr;
output sa1_leg3_corr, sa3_leg3_corr, sb1_leg3_corr, sb3_leg3_corr;

wire Slow_leg1, Slow_leg2, Slow_leg3;
wire Sup_leg1, Sup_leg2, Sup_leg3;

output out_dataB;
//Add this part for alternative code
/*wire out_dataA, out_dataC;
wire [11:0] Vref_A, Vref_B, Vref_C;
wire Vref_sign_A, Vref_sign_B, Vref_sign_C;
```

```
wire [11:0] DataA;
*/
////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////

assign rev_i_dir = ~curr_dir;

adc_one_test adc1 (
.CLK(clk),
.DINA(DINA3),
.DINB(DINB3),
.CONVST_b(CONVST_b3),
.SCLK(SCLK3),
.CS_b(CS_b3),
.DataA(Vab),
.DataB(Vbc)
);

adc_two adc2 (
.CLK(clk),
.DINA(DINA4),
.DINB(DINB4),
.CONVST_b(CONVST_b4),
.SCLK(SCLK4),
.CS_b(CS_b4),
.DataA(Vca),
.out_dataB(curr_dir)
);

peak_voltage_determine pk_dt(
.clk(clk),
.Vab(Vab),
.Vbc(Vbc),
.Vca(Vca),
.max(max)
);

square_wave sq1( .clk(clk),
.out1(out1),
.clkop(clkop)
);

pulse_determine pulse_dt(
.clkop(clkop),
.sq_wv1(out1),
.max(max),
.SA_up(SA_up), .SB_up(SB_up), .SC_up(SC_up), .SA_low(SA_low), .SB_low(SB_low),
.SC_low(SC_low)
```

```
);

four_step_basic leg1(.SA_a(SA_up_a), .SB_a(SB_up_a), .SC_a(SC_up_a), .SA_b(SA_up_b),
.SB_b(SB_up_b), .SC_b(SC_up_b),
.m1(SA_up), .m2(SB_up), .m3(SC_up),
.i_dir(curr_dir),
.clk(clk)
);

four_step_basic leg2(.SA_a(SA_low_a), .SB_a(SB_low_a), .SC_a(SC_low_a),
.SA_b(SA_low_b), .SB_b(SB_low_b), .SC_b(SC_low_b),
.m1(SA_low), .m2(SB_low), .m3(SC_low),
.i_dir(rev_i_dir),
.clk(clk)
);

check_pulse check_leg1(.sa1(SA_up_a), .sb1(SA_up_b), .sa2(SB_up_a),  .sb2(SB_up_b),
.sa3(SC_up_a), .sb3(SC_up_b),
.sa1_corr(SA_up_a_corr), .sb1_corr(SA_up_b_corr), .sa2_corr(SB_up_a_corr),
.sb2_corr(SB_up_b_corr), .sa3_corr(SC_up_a_corr), .sb3_corr(SC_up_b_corr)
);

check_pulse check_leg2(.sa1(SA_low_a), .sb1(SA_low_b), .sa2(SB_low_a),  .sb2(SB_low_b),
.sa3(SC_low_a), .sb3(SC_low_b),
.sa1_corr(SA_low_a_corr), .sb1_corr(SA_low_b_corr), .sa2_corr(SB_low_a_corr),
.sb2_corr(SB_low_b_corr), .sa3_corr(SC_low_a_corr), .sb3_corr(SC_low_b_corr)
);
////////////////////////////////////////////////////////////////////////////////
////////////////////////////////////////////////////////////////////////////////
//Secondary side code
reset_gen rst1(.clk(clk), .signal_in(signal_in), .reset(reset)
);

double_clk uut (
.clk(clk),
.out1(out_sq),
.delay_pulse(delay_pulse),
.reset(reset)
);

////////////////////////////////////////////
adc_one_test_secondary adc3 (
.CLK(clk),
.DINA(DINA),
.DINB(DINB),
.CONVST_b(CONVST_b),
.SCLK(SCLK),
.CS_b(CS_b),
```

```
.out1(out_sq),
.out_dataB(out_dataB),
.reset (reset)
);

PDM_bit_generate_leg1 uut1 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Slow_leg1(Slow_leg1),
.Sup_leg1(Sup_leg1),
.reset(reset)
);

PDM_bit_generate_leg2 uut2 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Slow_leg2(Slow_leg2),
.Sup_leg2(Sup_leg2),
.reset(reset)
);

PDM_bit_generate_leg3 uut3 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Slow_leg3(Slow_leg3),
.Sup_leg3(Sup_leg3),
.reset(reset)
);

dead_time dead_t1(
.pulse(Slow_leg1),
.out_pulse(sa1_leg1),
.clk(clk)
);

dead_time dead_t2(
.pulse(Sup_leg1),
.out_pulse(sa3_leg1),
.clk(clk)
);

dead_time dead_t3(
.pulse(Slow_leg2),
.out_pulse(sa1_leg2),
.clk(clk)
);

dead_time dead_t4(
```

```
.pulse(Sup_leg2),
.out_pulse(sa3_leg2),
.clk(clk)
);

dead_time dead_t5(
.pulse(Slow_leg3),
.out_pulse(sa1_leg3),
.clk(clk)
);

dead_time dead_t6(
.pulse(Sup_leg3),
.out_pulse(sa3_leg3),
.clk(clk)
);

assign sb1_leg1 = sa1_leg1;
assign sb3_leg1 = sa3_leg1;
assign sb1_leg2 = sa1_leg2;
assign sb3_leg2 = sa3_leg2;
assign sb1_leg3 = sa1_leg3;
assign sb3_leg3 = sa3_leg3;
////////////////////////////////////////////////

// Alternative code
// Code from 183 to 261 can be replaced with 264 to 355
/*adc_one_test_secondary adc3 (
.CLK(clk),
.DINA(DINA1),
.DINB(DINB1),
.CONVST_b(CONVST_b1),
.SCLK(SCLK1),
.CS_b(CS_b1),
.out1(out_sq),
.out_dataB(out_dataA),  //current direction
.DataA(DataA),
.reset (reset)
);

adc_one_secondary_current_meas adc4 (
.CLK(clk),
.DINA(DINA2),
.DINB(DINB2),
.CONVST_b(CONVST_b2),
.SCLK(SCLK2),
.CS_b(CS_b2),
.out1(out_dataB),
```

```
.out_dataB(out_dataC),
.reset (reset)
);

sine_wave_generate_leg1 uut1 (
.clk(clk),
.sine_out(Vref_A),
.Vref_sign(Vref_sign_A)

);

sine_wave_generate_leg2 uut2 (
.clk(clk),
.sine_out(Vref_B),
.Vref_sign(Vref_sign_B)
);

sine_wave_generate_leg3 uut3 (
.clk(clk),
.sine_out(Vref_C),
.Vref_sign(Vref_sign_C)

);

add_accumulate add1 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Vref(Vref_A),
.Vmeas(DataA),
.Slow(Slow_leg1),
.Sup(Sup_leg1)
);

add_accumulate add2 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Vref(Vref_B),
.Vmeas(DataA),
.Slow(Slow_leg2),
.Sup(Sup_leg2)
);

add_accumulate add3 (
.clk(clk),
.clk_20kHz(delay_pulse),
.Vref(Vref_C),
.Vmeas(DataA),
.Slow(Slow_leg3),
```

```
.Sup(Sup_leg3)
);

four_step2x1 phaseA(.sa1(sa1_leg1), .sb1(sb1_leg1), .sa2(sa3_leg1), .sb2(sb3_leg1),
.m1(Sup_leg1), .m2(Slow_leg1),
.i_dir(out_dataA),
.clk(clk)
);

four_step2x1 phaseB(.sa1(sa1_leg2), .sb1(sb1_leg2), .sa2(sa3_leg2), .sb2(sb3_leg2),
.m1(Sup_leg2), .m2(Slow_leg2),
.i_dir(out_dataB),
.clk(clk)
);

four_step2x1 phaseC(.sa1(sa1_leg3), .sb1(sb1_leg3), .sa2(sa3_leg3), .sb2(sb3_leg3),
.m1(Sup_leg3), .m2(Slow_leg3),
.i_dir(out_dataC),
.clk(clk)
); */

check_pulse_secondary ch_pl1(.sa1_leg1(sa1_leg1), .sa3_leg1(sa3_leg1), .sb1_leg1(sb1_leg1),
.sb3_leg1(sb3_leg1),
.sa1_leg1_corr(sa1_leg1_corr), .sa3_leg1_corr(sa3_leg1_corr),  .sb1_leg1_corr(sb1_leg1_corr),
.sb3_leg1_corr(sb3_leg1_corr),

.sa1_leg2(sa1_leg2), .sa3_leg2(sa3_leg2), .sb1_leg2(sb1_leg2), .sb3_leg2(sb3_leg2),
.sa1_leg2_corr(sa1_leg2_corr), .sa3_leg2_corr(sa3_leg2_corr), .sb1_leg2_corr(sb1_leg2_corr),
.sb3_leg2_corr(sb3_leg2_corr),

.sa1_leg3(sa1_leg3), .sa3_leg3(sa3_leg3), .sb1_leg3(sb1_leg3), .sb3_leg3(sb3_leg3),
.sa1_leg3_corr(sa1_leg3_corr), .sa3_leg3_corr(sa3_leg3_corr), .sb1_leg3_corr(sb1_leg3_corr),
.sb3_leg3_corr(sb3_leg3_corr)
);

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    15:34:22 01/23/2012
// Design Name:
// Module Name:    adc_one_test
//////////////////////////////////////////////////////////////////////////////////
module adc_one_test(
input CLK,
input DINA,
input DINB,
```

```
output reg CONVST_b=1,
output SCLK,
output reg CS_b=1,
output reg signed [11:0] DataA,
output reg signed [11:0] DataB
 );

integer  count;
reg [1:0] c1=2'b00; // Clock divider
// Counter for 16 falling Sclk edges
reg signed [11:0] SData1=0; // Serial data, received as-is
reg signed [11:0] SData2=0;

assign SCLK=c1[0];

always @(posedge CLK) // clk divide - Target frequency ~ 25 MHz
begin
c1<=c1+1;
end

always @ (negedge SCLK) begin
count <= count + 1;
if(count>=36)
begin // count=250 for 100kHz and =2500 for 10kHz 625 for 40kHz
count<=0;
end

case (count)
// Pulse CONVST low to start ADC conversion on selected channels (SL).
0    : begin
                    CONVST_b <= 1;
                    end

2    : CONVST_b <= 0;

3    : begin
                    CONVST_b <= 1;
                    end

22   : CS_b <= 0;

23   : begin
                    SData1[11]<=DINA;
                    SData2[11]<=DINB;
                    end
24   : begin
                    SData1[10]<=DINA;
                    SData2[10]<=DINB;
```

```
                end
25  : begin
                SData1[9]<=DINA;
                SData2[9]<=DINB;
                end
26  : begin
                SData1[8]<=DINA;
                SData2[8]<=DINB;
                end
27  : begin
                SData1[7]<=DINA;
                SData2[7]<=DINB;
                end
28  : begin
                SData1[6]<=DINA;
                SData2[6]<=DINB;
                end
29  : begin
                SData1[5]<=DINA;
                SData2[5]<=DINB;
                end
30  : begin
                SData1[4]<=DINA;
                SData2[4]<=DINB;
                end
31  : begin
                SData1[3]<=DINA;
                SData2[3]<=DINB;
                end
32  : begin
                SData1[2]<=DINA;
                SData2[2]<=DINB;
                end
33  : begin
                SData1[1]<=DINA;
                SData2[1]<=DINB;
                end
34  : begin
                SData1[0]<=DINA;
                SData2[0]<=DINB;
                end

35  : begin
                DataA<=SData1[11:0];
                DataB<=SData2[11:0];
                CS_b<=1;
                end
// Quiet time is (256 - 223) * 1/(25 Mhz) = 1.3 us.
```

```
endcase
end    //end of always

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    16:36:58 02/28/2012
// Design Name:
// Module Name:    peak_voltage_determine
//////////////////////////////////////////////////////////////////////////////////
module peak_voltage_determine(clk, Vab, Vbc, Vca, max
);

input clk;
input signed [11:0] Vab, Vbc;
input signed [11:0] Vca;
output reg [1:0] max;

always @(posedge clk)
begin
if ((Vab <= Vbc) && (Vab <= Vca))
max = 2'b01;
else if ((Vbc <= Vab) && (Vbc <= Vca))
max = 2'b10;
else if ((Vca <= Vab) && (Vca <= Vbc))
max = 2'b11;
else
max = 2'b00;
end

endmodule

`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    15:17:43 02/27/2012
// Design Name:
// Module Name:    square_wave
//////////////////////////////////////////////////////////////////////////////////
module square_wave(input clk,
output reg out1, clkop
);

integer count;

initial begin
count=0;
```

```
//out = 60'd1152921504606846975;
out1 = 1'd0;
//out2 = 1;
end

always @ (posedge clk) begin
if (count >= 1250)
begin
count=0;
clkop=~clkop;
end

else
count= count+1;
end

always @ (posedge clkop) begin
out1 = ~out1;
//out2 = ~out2;
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    18:16:05 02/28/2012
// Design Name:
// Module Name:    pulse_determine
//////////////////////////////////////////////////////////////////////////////////
module pulse_determine(clkop, sq_wv1, max,
SA_up, SB_up, SC_up, SA_low, SB_low, SC_low
);

input clkop;
input sq_wv1;
input [1:0] max;
output reg SA_up, SB_up, SC_up;
output reg SA_low, SB_low, SC_low;

always @(posedge clkop)
begin
if ((sq_wv1 == 1) && (max == 2'b01))
begin
SA_up <= 1;
SB_up <= 0;
SC_up <= 0;
SA_low <= 0;
```

```
SB_low <= 1;
SC_low <= 0;
end
else if ((sq_wv1 == 1) && (max == 2'b10))
begin
SA_up <= 0;
SB_up <= 1;
SC_up <= 0;
SA_low <= 0;
SB_low <= 0;
SC_low <= 1;
end
else if ((sq_wv1 == 1) && (max == 2'b11))
begin
SA_up <= 0;
SB_up <= 0;
SC_up <= 1;
SA_low <= 1;
SB_low <= 0;
SC_low <= 0;
end
else if ((sq_wv1 == 0) && (max == 2'b01))
begin
SA_up <= 0;
SB_up <= 1;
SC_up <= 0;
SA_low <= 1;
SB_low <= 0;
SC_low <= 0;
end
else if ((sq_wv1 == 0) && (max == 2'b10))
begin
SA_up <= 0;
SB_up <= 0;
SC_up <= 1;
SA_low <= 0;
SB_low <= 1;
SC_low <= 0;
end
else if ((sq_wv1 == 0) && (max == 2'b11))
begin
SA_up <= 1;
SB_up <= 0;
SC_up <= 0;
SA_low <= 0;
SB_low <= 0;
SC_low <= 1;
end
```

```
else
begin
SA_up <= 0;
SB_up <= 0;
SC_up <= 0;
SA_low <= 0;
SB_low <= 0;
SC_low <= 0;
end
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    16:15:10 02/01/2012
// Design Name:
// Module Name:    four_step_basic
//////////////////////////////////////////////////////////////////////////////////
module four_step_basic(SA_a, SB_a, SC_a, SA_b, SB_b, SC_b,
m1, m2, m3,
i_dir,
clk
   );

input i_dir;
input clk ;
input m1, m2, m3;
reg [2:0] in_state;
reg clk_SM;
output reg SA_a, SB_a, SC_a; //SA_low_a, SB_low_a, SC_low_a;
output reg SA_b, SB_b, SC_b; //SA_low_b, SB_low_b, SC_low_b;

integer count;
parameter s1 = 4'b0000 ;
parameter s2 = 4'b0001 ;
parameter s3 = 4'b0010 ;
parameter s1pos = 4'b0011 ;
parameter s1neg = 4'b0100 ;
parameter s2pos = 4'b0101 ;
parameter s2neg = 4'b0110 ;
parameter s3pos = 4'b0111 ;
parameter s3neg = 4'b1000 ;
parameter s12pos = 4'b1001 ;
parameter s12neg = 4'b1010 ;
parameter s23pos = 4'b1011 ;
parameter s23neg = 4'b1100 ;
```

```
parameter s13pos = 4'b1101 ;
parameter s13neg = 4'b1110 ;
reg [3:0] next_state ;

initial
begin
next_state <=s2;
end

always @ (posedge clk)
begin
if (count >= 30) // Set at 1.2us. Can be adjusted.
begin
count=0;
clk_SM=~clk_SM;
end

else
count= count+1;
end

always @ (posedge clk)
begin
 if ((m1 == 1'b1) && (m2 == 1'b0) && (m3 == 1'b0) && (i_dir == 1'b1))
 in_state = 3'b001 ;
 else if ((m1 == 1'b1) && (m2 == 1'b0) && (m3 == 1'b0) && (i_dir == 1'b0))
 in_state = 3'b010 ;
 else if ((m1 == 1'b0) && (m2 == 1'b1) && (m3 == 1'b0) && (i_dir == 1'b1))
 in_state = 3'b011 ;
 else if ((m1 == 1'b0) && (m2 == 1'b1) && (m3 == 1'b0) && (i_dir == 1'b0))
 in_state = 3'b100 ;
 else if ((m1 == 1'b0) && (m2 == 1'b0) && (m3 == 1'b1) && (i_dir == 1'b1))
 in_state = 3'b101 ;
 else if ((m1 == 1'b0) && (m2 == 1'b0) && (m3 == 1'b1) && (i_dir == 1'b0))
 in_state = 3'b110 ;
 else //if ((m1 == 1'b0) && (m2 == 1'b1) && (i_dir == 1'b0))
 in_state = 3'b111 ;

end

always @(posedge clk_SM)
begin

 case(next_state)
s1:
if ((in_state == 3'b011)||(in_state == 3'b101))
        begin
                next_state <= s1pos;
```

```
		end
else if ((in_state == 3'b100)||(in_state == 3'b110))
		begin
			next_state <= s1neg;
		end
else
			next_state <= s1;

s2:
if ((in_state == 3'b001)||(in_state == 3'b101))
		begin
			next_state <= s2pos;
		end
else if ((in_state == 3'b010)||(in_state == 3'b110))
		begin
			next_state <= s2neg;
		end
else
			next_state <= s2;

s3:
if ((in_state == 3'b001)||(in_state == 3'b011))
		begin
			next_state <= s3pos;
		end
else if ((in_state == 3'b010)||(in_state == 3'b100))
		begin
			next_state <= s3neg;
		end
else
			next_state <= s3;

s1pos:
if ((in_state == 3'b001)||(in_state == 3'b010))
		begin
			next_state <= s1;
		end
else if ((in_state == 3'b011)||(in_state == 3'b100))
		begin
			next_state <= s12pos;
		end
else if ((in_state == 3'b101)||(in_state == 3'b110))
		begin
			next_state <= s13pos;
		end
else
			next_state <= s1pos;
```

```
s1neg:
if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s1;
        end
else if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s12neg;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s13neg;
        end
else
                next_state <= s1neg;

s2pos:
if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2;
        end
else if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s12pos;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s23pos;
        end
else
                next_state <= s2pos;

s2neg:
if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2;
        end
else if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s12neg;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s23neg;
        end
else
                next_state <= s2neg;
```

```
s3pos:
if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3;
        end
else if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s23pos;
        end
else if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s13pos;
        end
else
                next_state <= s3pos;

s3neg:
if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3;
        end
else if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s23neg;
        end
else if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s13neg;
        end
else
                next_state <= s3neg;

s12pos:
if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s1pos;
        end
else if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2pos;
        end
else
                next_state <= s12pos;

s12neg:
if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s1neg;
```

```
        end
else if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2neg;
        end
else
                next_state <= s12neg;

s23pos:
if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2pos;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3pos;
        end
else
                next_state <= s23pos;

s23neg:
if ((in_state == 3'b011)||(in_state == 3'b100))
        begin
                next_state <= s2neg;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3neg;
        end
else
                next_state <= s23neg;

s13pos:
if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s1pos;
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3pos;
        end
else
                next_state <= s13pos;

s13neg:
if ((in_state == 3'b001)||(in_state == 3'b010))
        begin
                next_state <= s1neg;
```

```
        end
else if ((in_state == 3'b101)||(in_state == 3'b110))
        begin
                next_state <= s3neg;
        end
else
                next_state <= s13neg;

default: next_state <= s1pos;

endcase

end

always @(posedge clk_SM)
begin

case(next_state)
s1:
begin
SA_a = 1;
SA_b = 1;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end

s2:
begin
SA_a = 0;
SA_b = 0;
SB_a = 1;
SB_b = 1;
SC_a = 0;
SC_b = 0;
end

s3:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 1;
SC_b = 1;
end
```

```
s1pos:
begin
SA_a = 1;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end

s1neg:
begin
SA_a = 0;
SA_b = 1;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end

s2pos:
begin
SA_a = 0;
SA_b = 0;
SB_a = 1;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end

s2neg:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 1;
SC_a = 0;
SC_b = 0;
end

s3pos:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 1;
SC_b = 0;
```

```
end

s3neg:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 1;
end

s12pos:
begin
SA_a = 1;
SA_b = 0;
SB_a = 1;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end

s13pos:
begin
SA_a = 1;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 1;
SC_b = 0;
end

s23pos:
begin
SA_a = 0;
SA_b = 0;
SB_a = 1;
SB_b = 0;
SC_a = 1;
SC_b = 0;
end

s12neg:
begin
SA_a = 0;
SA_b = 1;
SB_a = 0;
SB_b = 1;
```

```
SC_a = 0;
SC_b = 0;
end

s13neg:
begin
SA_a = 0;
SA_b = 1;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 1;
end

s23neg:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 1;
SC_a = 0;
SC_b = 1;
end

default:
begin
SA_a = 0;
SA_b = 0;
SB_a = 0;
SB_b = 0;
SC_a = 0;
SC_b = 0;
end
        endcase
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    17:03:53 03/21/2012
// Design Name:
// Module Name:    check_pulse
//////////////////////////////////////////////////////////////////////////////////
module check_pulse(sa1, sa2, sb1, sb2, sa3, sb3,
sa1_corr, sa2_corr,  sb1_corr, sb2_corr, sa3_corr, sb3_corr
    );
```

```
input sa1, sa2, sb1, sb2, sa3, sb3;
output sa1_corr, sa2_corr, sb1_corr, sb2_corr, sa3_corr, sb3_corr;


assign sa1_corr = (sa1^sb2^sb3)&sa1;
assign sb1_corr = (sb1^sa2^sa3)&sb1;
assign sa2_corr = (sa2^sb1^sb3)&sa2;
assign sb2_corr = (sb2^sa1^sa3)&sb2;
assign sa3_corr = (sa3^sb1^sb2)&sa3;
assign sb3_corr = (sb3^sa1^sa2)&sb3;

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    16:07:56 03/26/2012
// Design Name:
// Module Name:    reset_gen
//////////////////////////////////////////////////////////////////////////////////
module reset_gen(clk, signal_in, reset
);


input clk, signal_in;
output reg reset;
reg reset_sync;

always @(posedge clk or posedge signal_in)
begin
if (signal_in)
  begin
  reset_sync <= 1'b1 ;
  reset <= 1'b1 ;
  end
else
  begin
  reset_sync <= 1'b0 ;
  reset <= reset_sync ;
  end
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
```

```
// Create Date:    14:10:22 02/13/2012
// Design Name:
// Module Name:    double_clk
//////////////////////////////////////////////////////////////////////////////////
module double_clk(clk, out1, delay_pulse, reset
   );

input clk;
input out1;
input reset;
output reg delay_pulse;
reg delay_pulse1;
reg delay_pulse2;
reg [17:0] count1;
reg [17:0] count2;

initial
begin
count1 <= 1;
count2 <= 1;
delay_pulse1 <= 0;
delay_pulse2 <= 0;
end

assign out2 = ~out1;

always @(posedge clk or posedge reset)
begin
if (reset == 1)
delay_pulse <= 0;
else
delay_pulse <= delay_pulse1 | delay_pulse2;
end

always @(posedge clk or posedge reset)
begin
if (reset ==1)
            begin
            count1 <= 1;
            delay_pulse1 <= 0;
            end
else if (out1 == 0)
            begin
            count1 <= 1;
            delay_pulse1 <= 0;
            end
else if ((out1 == 1)&&(count1<=1250))
            begin
```

```
        count1 <= count1 + 1;
        delay_pulse1 <= 1;
        end
else
        delay_pulse1 <= 0;
end

always @(posedge clk or posedge reset)
begin
if (reset ==1)
        begin
        count2 <= 1;
        delay_pulse2 <= 0;
  end
else if (out2 == 0)
        begin
        count2 <= 1;
        delay_pulse2 <= 0;
        end
else if ((out2 == 1)&&(count2<=1250))
        begin
        count2 <= count2 + 1;
        delay_pulse2 <= 1;
        end
else
        delay_pulse2 <= 0;
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    15:09:30 02/07/2012
// Module Name:    PDM_wave_generate
//////////////////////////////////////////////////////////////////////////////////
module PDM_bit_generate_leg1(clk, clk_20kHz, Slow_leg1, Sup_leg1, reset
 );
input reset;
input clk;
input clk_20kHz;
output Slow_leg1;
output Sup_leg1;
reg PDM_bit;
reg [10:0] bit_count;
parameter M=400;

initial
```

```
begin
bit_count=1;
end

always @(posedge clk_20kHz or posedge reset)
begin
if (reset ==1)
        bit_count <= 1;
else if (bit_count>=M)
        begin
        bit_count<=1;
        end
else
        bit_count <= bit_count+1;
end

always @(posedge clk or posedge reset)
begin
if (reset == 1)
PDM_bit <= 0;
else
begin
case(bit_count)
1: PDM_bit <= 1;
2: PDM_bit <= 1;
3: PDM_bit <= 1;
4: PDM_bit <= 1;
/*
.
.
This part of the code is omitted to reduce the length of the print of the code.
It is a long sequence of PDM_bit values.
*/
endcase
end//end else
end

assign Sup_leg1 = PDM_bit;
assign Slow_leg1 =~Sup_leg1;
endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    17:32:56 12/14/2011
// Design Name:
//////////////////////////////////////////////////////////////////////////////////
module dead_time(pulse, out_pulse, clk
```

```
);

input pulse, clk;
integer count;
output reg out_pulse;
reg dead_time_pulse;

initial
begin
count <=0;
end

always@(posedge clk)
begin
if(pulse == 0)
        begin
        dead_time_pulse <= 0;
        count <= 0;
        end
else if((pulse == 1)&& (count>=50))
        begin
        dead_time_pulse <= 0;
//      count <= count + 1;
        end
else
        begin
        dead_time_pulse <= 1;
        count <= count + 1;
        end
end

always@(posedge clk)
begin

begin
if ((dead_time_pulse==1)&&(pulse==1))
out_pulse <= 0;
else if ((dead_time_pulse==0)&&(pulse==0))
out_pulse <= 0;
else if ((dead_time_pulse==0)&&(pulse==1)&&(count>=20))
out_pulse <= 1;
else
out_pulse <= 0;
end

end

endmodule
```

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    15:09:30 02/07/2012
// Design Name:
// Module Name:    sine_wave_generate
//////////////////////////////////////////////////////////////////////////////////
module sine_wave_generate_leg1(clk, sine_out, Vref_sign
 );

input clk;
output reg signed [11:0] sine_out;
output reg Vref_sign;

reg [10:0] theta_i;
reg [11:0] c;

parameter M=2000; //No. of divisions made in 2pi
parameter N=2500; //N=Tref/(Tclk*M)

initial
begin
c=1;
theta_i=1;
end

always @(posedge clk)
begin
if (theta_i>=M)
        begin
        theta_i<=1;
        end
else if (c>=N)
        begin
                c <= 1;
                theta_i <= theta_i+1;
        end
else
        c <= c+1;
end

always @(posedge clk)
begin
case(theta_i)
1: sine_out <= 0;
2: sine_out <= 6;
3: sine_out <= 13;
```

```
4: sine_out <= 19;
5: sine_out <= 26;
/*
.
.
It is a long sequence of sifferent values of sine_out.
This part of the code is emitted to reduce the length of the print of the code.
.
.
*/
1060: sine_out <= -377;
1061: sine_out <= -384;
1062: sine_out <= -390;
1063: sine_out <= -396;
/*
.
.
*/
endcase
end

always @(posedge clk)
begin
if (sine_out >= 0)
        Vref_sign <= 1;
else
        Vref_sign <= 0;
end

endmodule


`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Create Date:    16:17:23 02/07/2012
// Design Name:
// Module Name:    add_accumulate
//////////////////////////////////////////////////////////////////////////////////
module add_accumulate(clk, clk_20kHz, Vref, Vmeas,
Slow, Sup //, Vout, accumulation_error, current_error, prev_error
    );

input clk, clk_20kHz;
input signed [11:0] Vmeas;
input signed [11:0] Vref;

reg signed [24:0] current_error;
reg signed [24:0] prev_error;
```

```
reg signed [24:0] accumulation_error;
reg signed [11:0] Vout;
output reg Slow, Sup;
reg [3:0] count;

//assign Vout <= Sup*Vmeas;
initial
begin
Sup=1;
Slow=0;
accumulation_error=0;
current_error=0;
prev_error=0;
count =0;
end

always @(posedge clk)
begin
count <= count +1;
if (count ==1)
        begin
                //count <= count +1;
                if (Sup == 1)
                Vout <= Vmeas;
                else
                Vout <= 0;
        end
else if (count == 2)
        //count <= count +1;
        current_error <= Vout - Vref;
else if (count==3)
        accumulation_error <= current_error + prev_error;
else if (count ==4)
        begin
        prev_error <= accumulation_error;
        count <= 0;
        end

end

always @(posedge clk_20kHz)
begin
if ((accumulation_error >=0) && (Vmeas >= 0))
        begin
                Slow = 1;
                Sup = 0;
        end
else if ((accumulation_error >=0) && (Vmeas < 0))
```

```
        begin
                Slow = 0;
                Sup = 1;
        end
else if ((accumulation_error <0) && (Vmeas >= 0))
        begin
                Slow = 0;
                Sup = 1;
        end
else //if ((accumulation_error <0) && (Vmeas < 0))
        begin
                Slow = 1;
                Sup = 0;
        end
end

endmodule
```