

DiCAD Design Methodology

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## **Abstract**

This paper presents a method for obtaining a fine tuning range digital controlled oscillator using a digital controlled artificial dielectric. Additionally, a design methodology is also provided in order to provide step-by-step instructions for the design of fine-tuning range digital controlled oscillators using a digital controlled artificial dielectric.

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# 1. Introduction

Phase Lock Loops have been a critical component in communications systems and most recently, All Digital Phase Lock Loops (ADPLL) have been proposed. A critical component to the ADPLL is the Digital Controlled Oscillator (DCO). Design of microwave oscillators poses a difficult challenge due to device parasitics. Recently, in [1] a Digital Controlled Dielectric (DiCAD) was proposed as a coarse tuning method in DCOs. In this work, a fine tuning method is presented along with a design methodology for using the DiCAD as a fine tuning device in DCOs.

## 1.1 PLL

A Phase-Locked Loop (PLL) is a closed loop system used for frequency synthesis, clock recovery, modulation, demodulation and skew compensation. A PLL consists of four main components: a reference signal, a Phase Detector (PD), a controllable oscillator and a loop filter. In many cases, a divider is placed in the feedback path when a higher output frequency is desired. Over the years, several advances have been made in order to improve PLL performance and adapt PLLs for use in varying target applications. One PLL topology that has gained interest over the past few years is the All-Digital-PLL (ADPLL).

## 1.2 ADPLL

All Digital Phase Lock Loops offer a cheaper long-term solution when compared to their analog counterparts. The cost savings arise from the reduction in non-reoccurring

engineering costs through design reuse. Most of the ADPLL is synthesizable thus limiting the amount of custom circuit design required when transitioning to different process nodes or different output frequencies. ADPLLs are ideal for Software Defined Radios because they enable direct phase modulation from the digital domain. This has two important benefits. First, when used in the transmit path, the ADPLL directly modulates the carrier. Second, when operated as part of a receiver direct modulation enables compensation of predicted phase error based on estimated quantization errors. ADPLLs are different from their analog counterpart. Instead of using a phase detector, the ADPLL uses a Time to Digital Converter and the controllable oscillator is a Digital Controlled Oscillator.

### **1.3 DCO**

Digital Controlled Oscillator design poses several challenges particularly in sub-micron CMOS at gigahertz frequencies. The use of transmission lines in oscillator design is preferred because they offer a higher quality factor and demonstrate optimum noise characteristics and temperature stability. However, if one desires a wide tuning range and high linearity, transmission line structures are typically are not a viable solution. However, a Digital Controlled Artificial Dielectric (DiCAD), presented in [1], enables the use of a transmission line structure as a coarse tuning element in a wideband DCO.

### **1.4 Focus of Thesis**

Research into methods for using the DiCAD as a fine-tuning structure to improve

the noise characteristics and temperature stability of frequency synthesizers is the focus of this thesis.

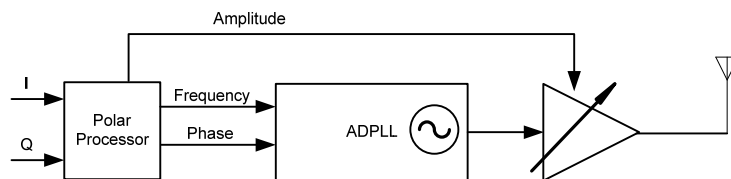
This thesis offers a design methodology for the design of fine-tuning DCOs. This fine-tuning DCO can be used in the design of temperature stable frequency synthesizers exhibiting lower phase noise than other design approaches. Its robust design and digital control make the proposed frequency synthesizer ideal for military software defined radio applications. In addition, the design comes with the added benefit of reducing NRE costs.

## 2. Background

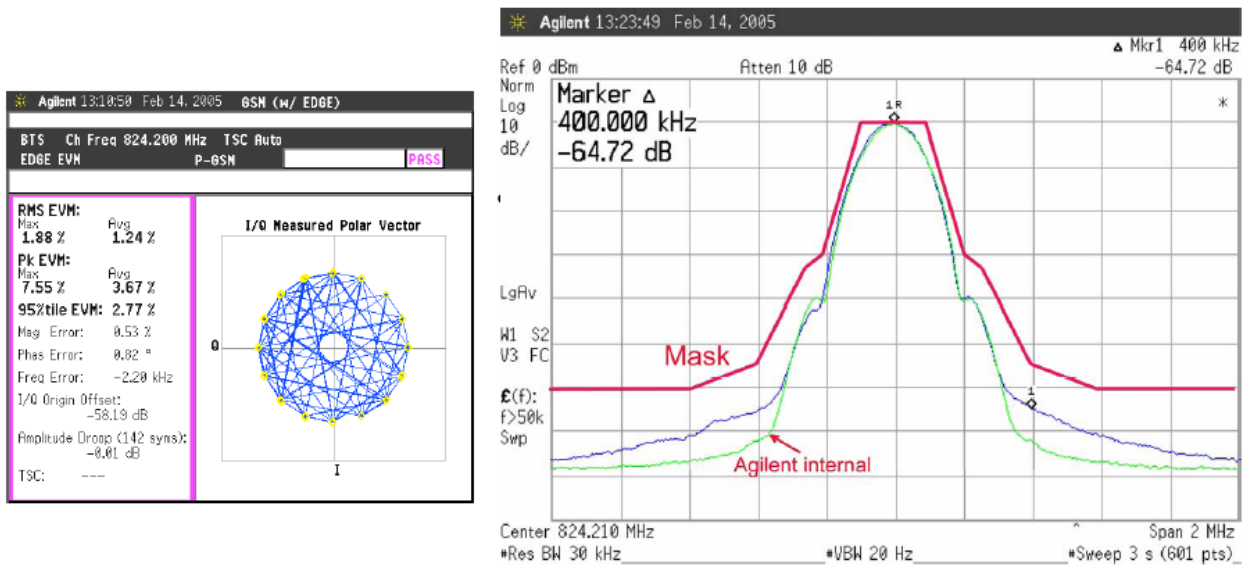
### 2.1 ADPLL and its uses

ADPLL popularity grew out of work funded by Texas Instruments® (TI). The Digital RF Processor (DRP™) project resulted in over 50 patents for its primary researcher Bogdan Staszewski. The ADPLL gives rise to a new type of transmitter called a polar transmitter, shown in figure 2-1. Digital control of the frequency, phase and amplitude can implement Bluetooth extended data rates, EDGE and Wideband CDMA wireless standards. Figure 2-2 shows TI's ability to implement an EDGE transmitter using polar transmitter techniques. The figure shows the transmitter meeting specifications with significant margins.

Phase Lock Loops have been a critical component in communications systems, recently All Digital Phase Lock Loops (ADPLL) have been proposed. A critical component to the ADPLL is the Digital Controlled Oscillator (DCO). Design of microwave oscillators poses a difficult challenge due to device parasitic. Recently, in [1] a Digital Controlled Dielectric (DiCAD) was proposed as a coarse tuning method in DCOs. In this work a fine tuning method is proposed along with a design methodology for using the DiCAD as a fine tuning device in DCOs.



**Figure 2-1:** Digital controlled polar transmitter



**Figure 2-2:** TI's EDGE modulation measured results [2]

In coherent communication systems, a PLL performs timing synchronization. Also in communications systems it is beneficial to perform carrier synchronization in order to undo symbol rotations induced by frequency and phase offsets induced by the channel. Synchronization occurs from obtaining an estimate of the channel offsets followed by the tracking of any changes after estimation. Applied through digital control ADPLLs can enable direct symbol rotation prior to baseband sampling from estimates performed in digital baseband.

With its direct digital control, ADPLLs offer the versatility required in high performance SDR systems. The increase in performance comes from replacing intensive digital baseband software computations with software controllable hardware.

## **2.2 PLL / ADPLL noise**

The design and overall performance of PLLs is mostly concerned with the management of noise sources within the system. Design of a working system involves trading off different design parameters to obtain a desired output phase noise, where the application determines the phase noise requirements. For example, in an RF system oscillator phase noise can result in reciprocal mixing during down conversion. In clock generation and clock recovery circuits, PLL phase noise directly determines the amount of clock jitter present.

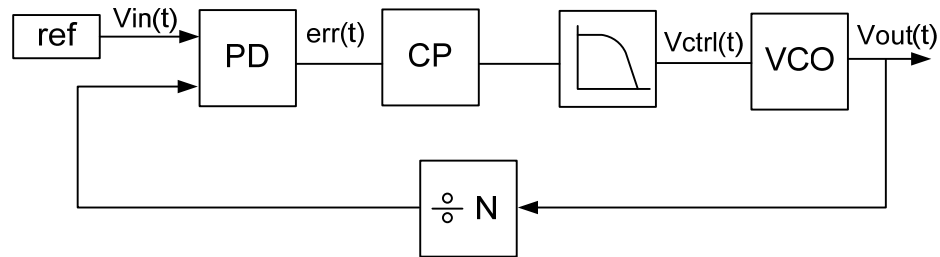
Each sub-component in a PLL system contributes phase noise. Depending on where the component is located, each noise source exhibits its own transfer function and therefore contributes differently to the phase noise at the output.

## **2.3 PLL basics**

Before diving into phase noise contributions it is important to understand how PLLs work and how an ADPLL differs from an analog PLL. Figure 2-3 shows a common PLL configuration. Supplied to the input of a Phase Detector (PD) is a stable reference signal and a divided version of the output signal. The division ratio can be either integer or fractional. The phase detector compares the phase of both signals and produces an error signal at its output. The error signal is then converted to a voltage with a Charge Pump (CP) and capacitor and low-pass filtered with a loop filter. The filtered signal presents a control voltage to a Voltage Controlled Oscillator (VCO). This system essentially forces

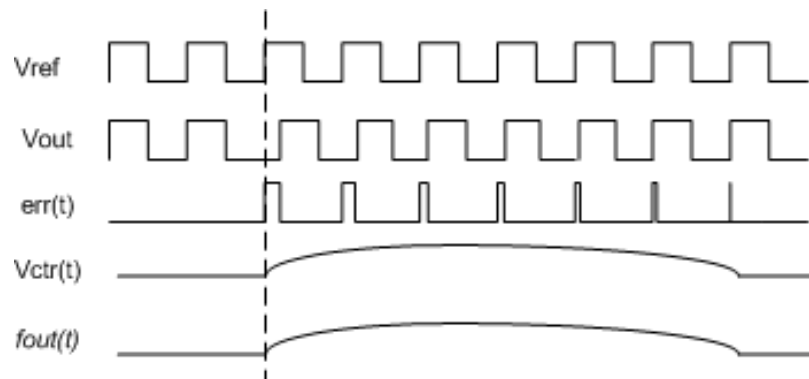


the unstable VCO to produce a stable output frequency.



**Figure 2-3:** Phase-Locked Loop system diagram and governing equations

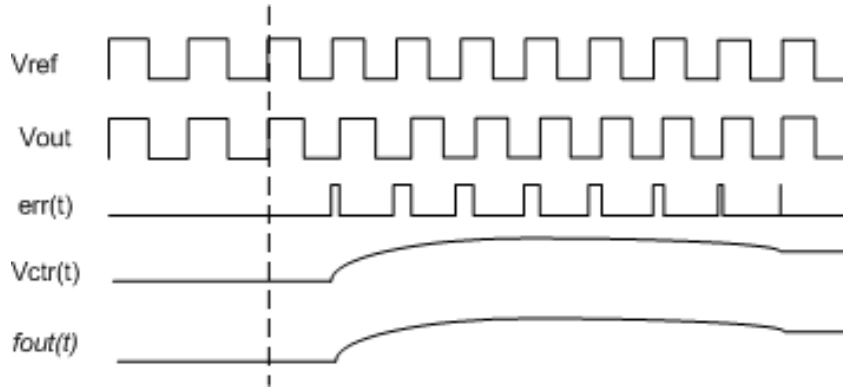
The closed loop system in figure 1 can track changes to both phase and frequency. Figure 2-4 shows the system response to a change in phase. In figure 2-4, the output oscillator lags in phase at the dashed line. This situation is common in VCOs where the oscillator is inherently unstable and tends to drift. When the output phase drifts, the phase detector produces an error signal. The result is a temporary rise in the VCO control voltage, which increases the VCO output frequency until the input and output match in both phase and frequency.



**Figure 2-4:** Loop response to a change in frequency, recreation of figure 15.11 in [3]

In response to a change in frequency, the PLL exhibits the response shown in figure 2-5. This situation is similar to a clock recovery circuit on startup. The VCO is operating at its natural frequency when an embedded clock signal is presented to the PLL as a

reference clock. The reference clock is running faster than the VCO, resulting in phase-detector error signal causing the control voltage at the VCO to increase until the signals are matched in phase and frequency.



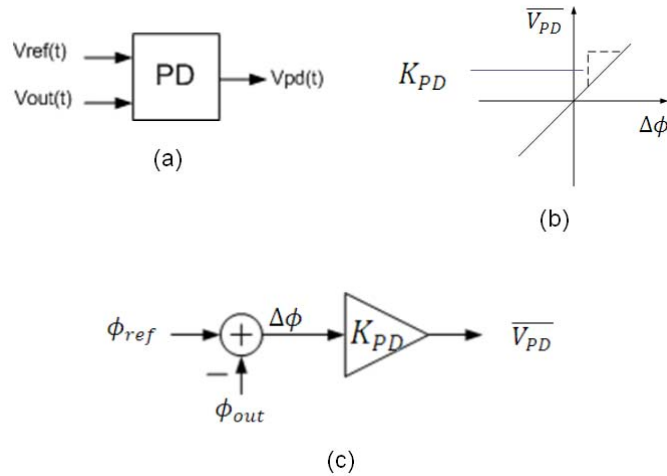
**Figure 2-5:** Loop response to a change in frequency, recreation of figure 15.12 in [3]

## 2.4 PLL Modeling

To properly design a PLL and understand the effects of individual noise sources one needs an appropriate model. Several PLL models exist. There are frequency domain, phase-domain and time domain models. Furthermore, these models can be analyzed using Laplace and z-domain techniques. Since the PLL designer is primarily concerned with phase noise performance. The phase-domain model is most appropriate. If necessary, this model can be converted to other domains when conversion simplifies the design of individual components.

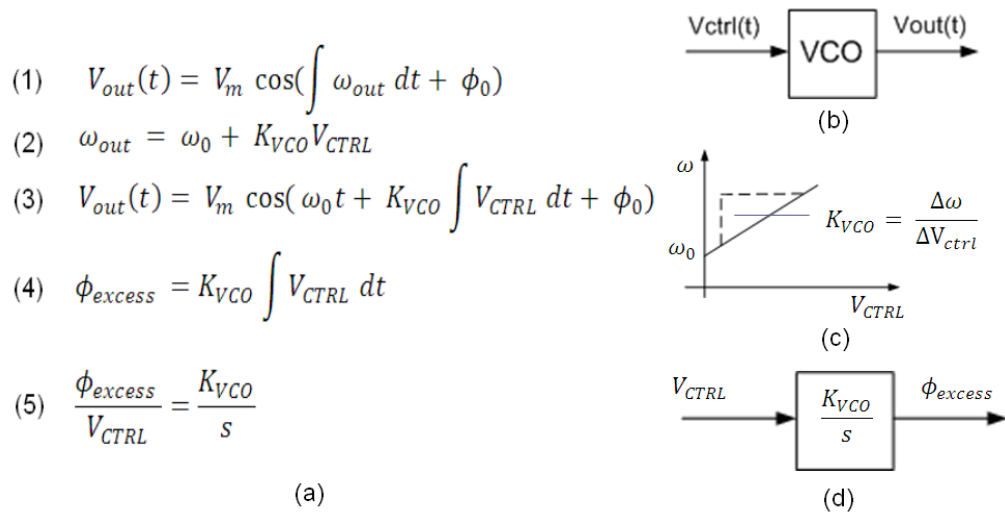
PLL modeling begins with generating phase-domain models for each of the individual components. The phase detector in figure 2-6.a produces an error signal, which is proportional to the phase difference of the two signals presented to its input. This gives rise to a phase detector gain, which is shown in figure 2-6.b. The phase-domain model of

the phase detector is shown in figure 2-6.c.

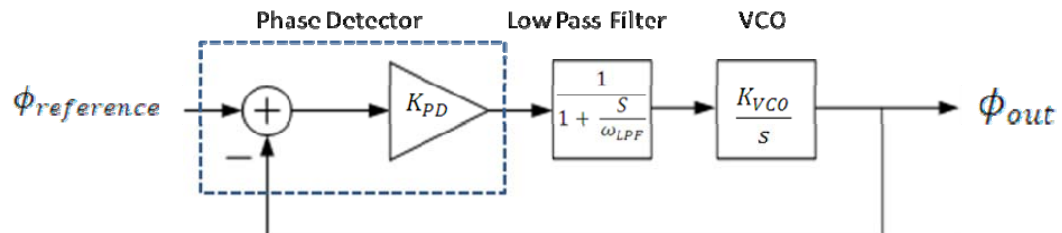


**Figure 2-6:** Phase detector modeling (a) phase detector (b) formation of phase detector gain (c) phase-domain model of phase detector

The charge pump is used to convert the phase error signal into a voltage and has its own gain  $K_{cp}$ . The loop filter is characterized by its own transfer function  $H(\omega)$ . The divider's phase-domain model is simply  $1/N$ . The VCO phase-domain model is more complicated and requires a little bit of math to be developed. Figure 5a shows the math used to arrive at the VCO phase-domain model. Similar to the phase detector, the VCO too has a gain associated with it, except it starts with an offset determined by the VCO natural frequency with no control voltage present. This gain and offset are shown in equation 2. Equations 1-3 in figure 2-7.a define the time-domain transfer function for the VCO of figure 2-7.b. The VCO behaves like an ideal integrator. Integration of the VCO's control voltage over time results in excess phase. Figure 2-7.d shows the resulting phase-domain model of a VCO.



**Figure 2-7:** VCO modeling (a) math used to arrive at phase-domain model (b) VCO (c) VCO gain (d) VCO phase-domain model



**Figure 2-8:** Linear phase-domain model of a PLL.

Figure 2-8 shows the combined linear phase-domain model for a PLL. It has been simplified by removing the charge pump and divider. Open loop and closed loop transfer functions are used to design and analyze the system. The open loop transfer function is used for the design of individual components, where the closed loop transfer function is used to determine stability, closed-loop bandwidth and settling time of the PLL. These transfer functions are shown in figure 2-9.

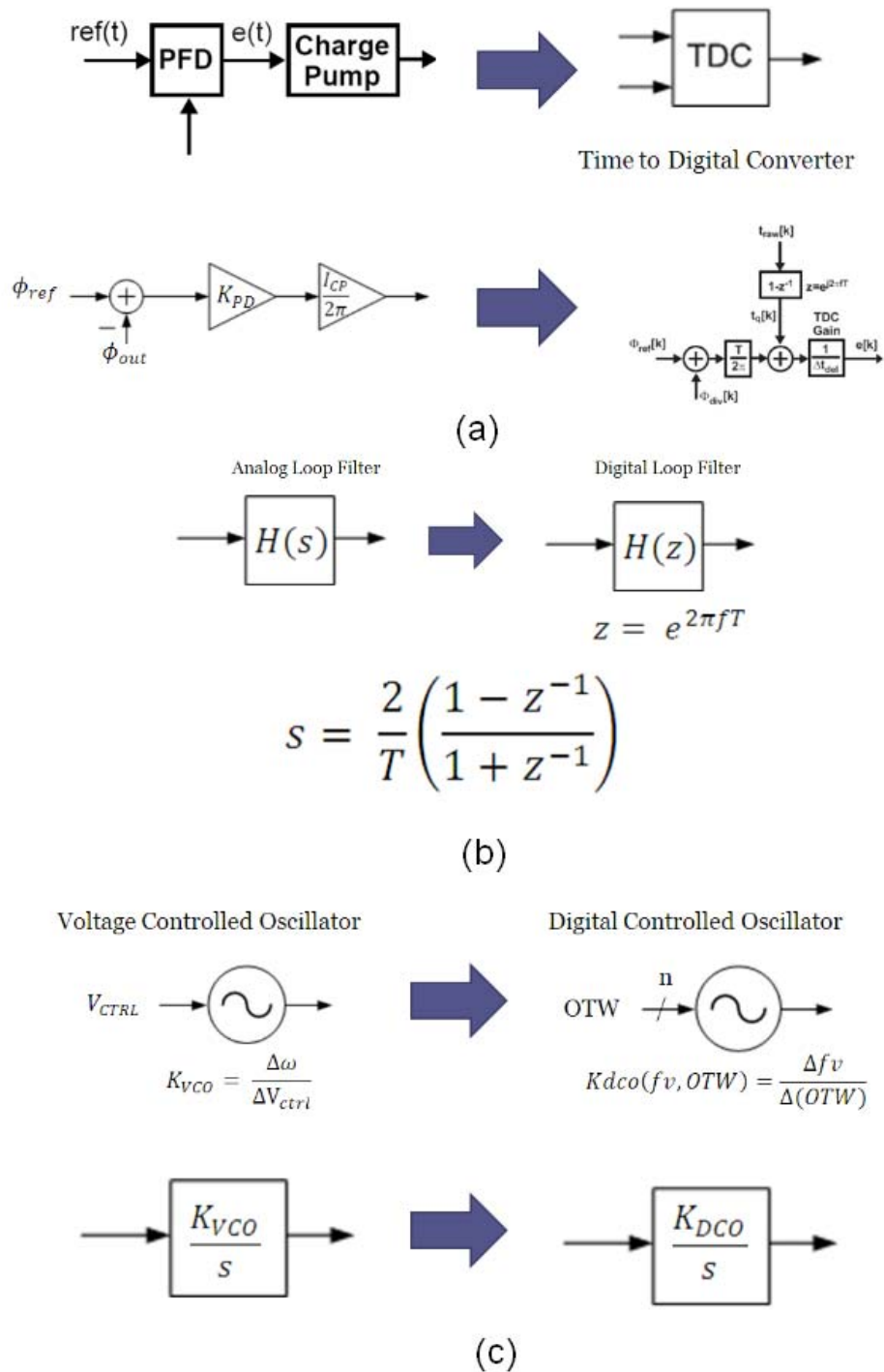
$$H(s)_{open} = \frac{\phi_{out}}{\phi_{ref}} = K_{PD} * \frac{1}{1 + \frac{s}{\omega_{LFF}}} * \frac{K_{VCO}}{s}$$

$$\begin{aligned}
 & \text{(a)} \\
 H(s)_{closed} &= \frac{K_{PD} K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD} K_{VCO}} \\
 & \text{(b)}
 \end{aligned}$$

**Figure 2-9:** (a) open loop transfer function (b) closed loop transfer function.

## 2.5 The transition to an ADPLL

A digital system is described as a system whose circuit boundaries behave in a digital manner. This means the circuit inputs and outputs are characterized by high and low voltage levels. The inputs and outputs transition between these levels and never settle to an intermediate voltage levels. In current PLL designs, the phase detector and divider are already implemented using digital techniques. To arrive at an all-digital solution, the charge pump, loop filter and VCO must be replaced with digital components. The phase detector and charge pump are replaced by a Time to Digital Converter (TDC). The loop filter is replaced with a digital filter using the bilinear transform. Finally, the VCO is replaced with a Digital Controlled Oscillator (DCO). Upon replacement of each component the phase-domain model must be replaced with an appropriate model. Figure 2-10 shows the system level block diagram and phase-domain model transformations just described.



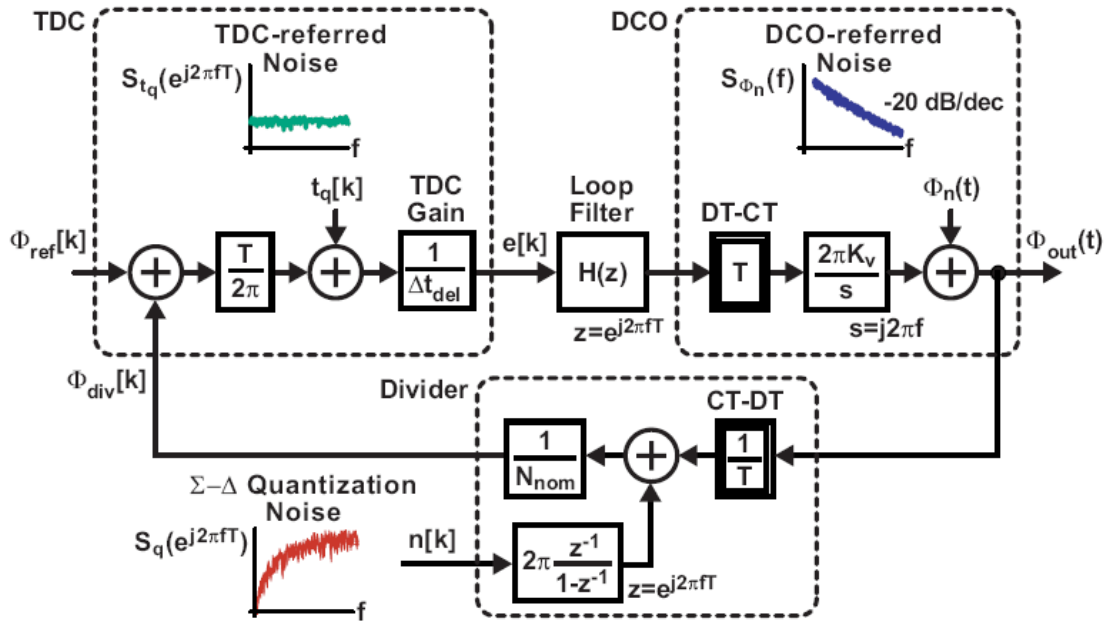
**Figure 2-10:** The transition to ADPLL (a) phase detector and charge pump replaced by TDC (b) loop filter replaced by digital filter through the bilinear transform (c) VCO replaced by DCO

### 3. ADPLL noise

Figure 3-1 shows the phase-domain model for an ADPLL including all noise sources. It too has its own open and closed loop transfer functions they are as follows:

$$A(f) = \frac{1}{\Delta t_{del}} H(e^{j2\pi fT}) T \frac{K_V}{2\pi f} \frac{1}{N} \quad (\text{open loop transfer function})$$

$$G(f) = \frac{A(f)}{1+A(f)} \quad (\text{closed loop transfer function})$$



**Figure 3-1:** Phase domain model of an ADPLL including noise sources, from [4]

#### 3.1 TDC noise

The TDC noise is a flat spectrum resulting from quantization errors and is determined by its resolution, output frequency and the reference frequency. The total TDC quantization noise is represented by the following equation:

$$TDCnoise = \frac{1}{T} |2\pi N|^2 \frac{\Delta t_{del}^2}{12}$$

$$\frac{1}{T} = \text{reference frequency}, \quad N = \frac{\text{output frequency}}{\text{reference frequency}}, \quad \Delta t_{\text{del}} = \text{TDC resolution}$$

When the TDC quantization noise is referred to the output it passes through the closed loop transfer function  $G(f)$ . The result is the TDC noise being low-pass filtered with a DC gain of one.

### 3.2 Divider Noise

In fractional-N PLLs integer divide ratios are periodically alternated. The average divide ratio determines the fractional division ratio. This is required in frequency synthesizers where the tuning step is less than the reference clock frequency. The periodic altering of divider ratios introduces quantization noise. Traditionally sigma-delta modulators randomize the divide signal used for selecting the integer divide ratios. This results in a spectral shaping of the divider quantization noise. The sigma-delta modulator up converts the low frequency noise components of the divider to a higher frequency, which is hopefully beyond the bandwidth of the PLL. The resulting divider phase noise has the shape shown in bottom left of figure 9 and is determined by the order or number of sigma-delta cells used and is governed by the following equation.

$$\mathcal{L}\{f\} = \frac{(2\pi)^2}{12 * F_{ref}} \left( \frac{f}{\frac{F_{ref}}{2\pi}} \right)^{2(m-1)} \text{ in } \left( \frac{\text{rad}^2}{\text{Hz}} \right)$$

### 3.3 DCO noise

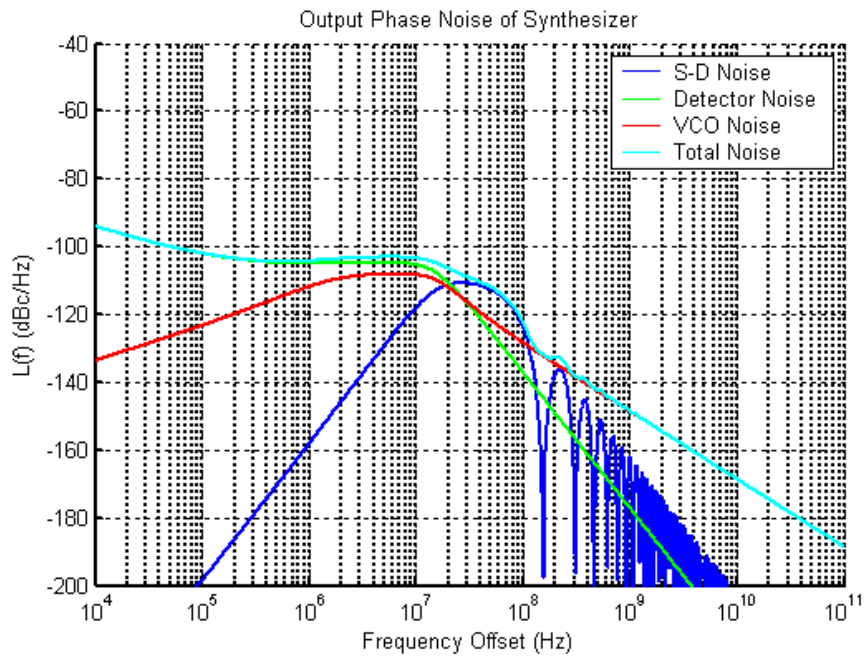
The DCO noise has more analog under the hood than the rest of the components. The DCO consists of thermal and flicker noise components. The actual DCO noise



sources are analyzed in more detail in a later section. The DCO noise sees a  $1 - G(f)$  transfer function which exhibits a high pass behavior.

### 3.4 Combined Phase Noise at output

Figure 3-2 shows the combination of TDC (detector), sigma-delta (S-D), DCO (VCO) and Total phase noises. The figure shows the result after many design iterations to converge on an ADPLL solution with a center output frequency of 26.5 GHz.



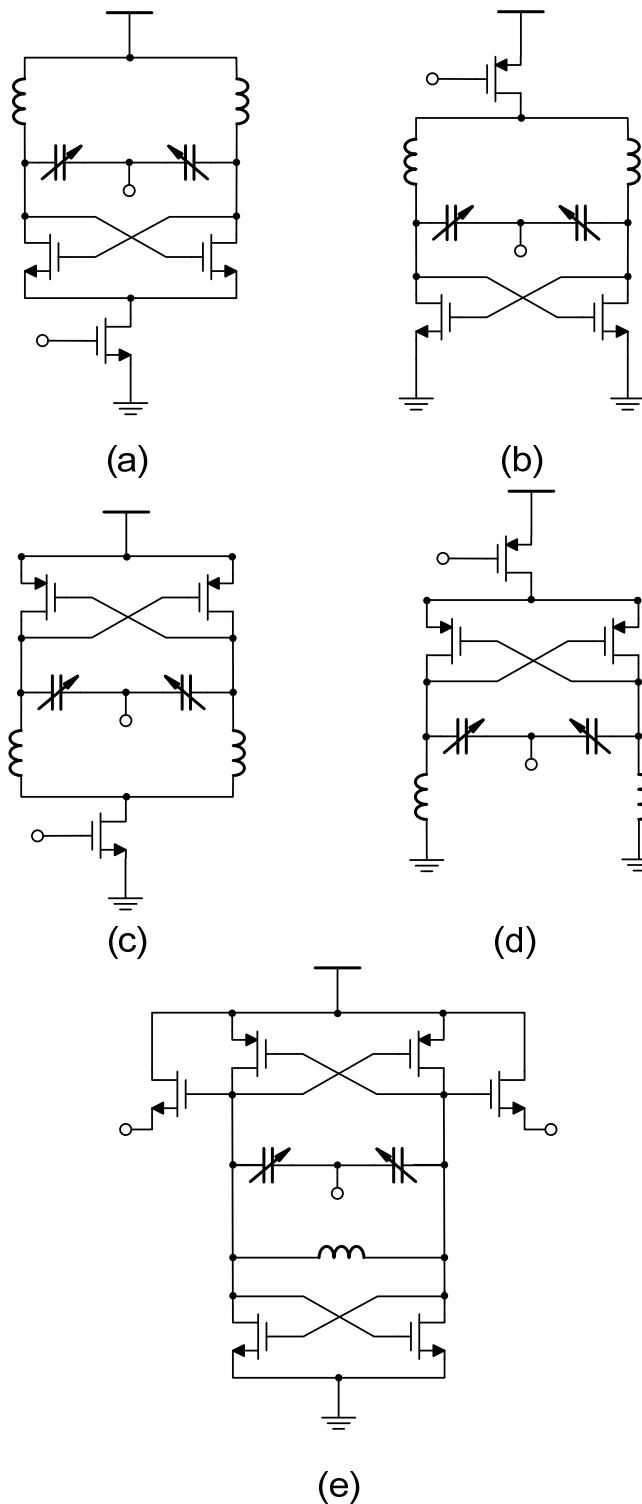
**Figure 3-2:** Total and individual phase noise for a 26.5 GHz ADPLL

## 4. Oscillator Design

Tunable oscillator design consists of choosing a topology, which includes a feedback system, a resonator structure and a tuning method. Each choice has an effect on oscillator performance metrics, such as phase noise and tuning range. A successful design guarantees the oscillator starts up on power up and is stable under steady state conditions.

### 4.1 Topologies

Since the focus of this research involves CMOS design, there really is only one viable oscillator topology, the cross-coupled tank circuit. However, CMOS cross-coupled oscillators can take on several forms. The cross-coupled pair can be implanted using either NMOS or PMOS transistors and the tail current source can be placed on the top or bottom. These configurations can produce four different cross-coupled differential oscillators. Additionally, both PMOS and NMOS transistors can be used producing a fifth topology. All five configurations are shown in figure 4-1. Some papers have claimed PMOS transistors exhibit smaller flicker noise than NMOS transistors, however this is not true in all processes and some researchers claim one should build and test all configurations to determine which configuration delivers the lowest phase noise. A cross-coupled CMOS pair can be analyzed as two out-of-phase identical oscillators with a virtual ground. Additionally, differential oscillator noise can be analyzed as a single-ended negative resistance oscillator where the cross-coupled pair produces the negative resistance required to compensate for losses in the resonator.



**Figure 4-1:** differential cross-coupled CMOS configurations (a) NMOS cross-coupled pair, bottom tail current source (b) NMOS cross-coupled pair, top tail current source (c) PMOS cross-coupled pair, bottom tail current source (d) PMOS cross-coupled pair, top tail current source (e) both NMOS and PMOS cross coupled pair w/ output buffers

## **4.2 Resonator Structures**

A resonant structure is required to set the oscillator output frequency. Resonant structures come in various forms such as, quarter-wave resonators, quartz crystals, Surface Acoustic Wave (SAW) devices and LC tank. Although the LC tank is most common, each resonator structure offers its own benefits and should be considered based on the target application.

Each resonant structure exhibits some losses. In a resonant circuit, the ratio of energy stored vs. energy lost is a measure of the structures quality factor (Q). Some structures have a higher Q than others and often a higher Q represents a lower tuning range.

## **4.3 Tuning Structures**

A variety of devices can be used for tuning the resonator or tank structure. The most common device is a varactor. A varactor is a variable capacitor made out of a semiconductor device. It is a diode whose depletion region can be varied with a bias voltage, thus varying the device's capacitance. In CMOS technologies, a PMOS transistor is used to form the varactor. A PMOS transistor exhibits different capacitance vs. voltage relationships depending on if it is operating in the accumulation, depletion or inversion region. These are all techniques used in voltage controlled oscillators.

Different techniques have been proposed to tune digital controlled oscillators. One

method uses standard varactors controlled by a digital to analog converter [6]. Others [7] have used banks of on-off varactors. Most recently, a Digital Controlled Artificial Dielectric (DiCAD) has been proposed for coarse tuning of DCOs [8]. The DiCAD is discussed in more detail in a later section.

#### **4.4 Phase Noise**

Since phase noise is of importance at the system level, it is important to understand the sources of phase noise in a tunable oscillator. Phase noise is a strong function of the resonator and determined largely by the quality factor or  $Q$  of the tank circuit. Additionally, flicker noise in CMOS transistors can have adverse effects. High capacitance vs. voltage varactor curves can be highly sensitive to voltage fluctuations induced by flicker noise in the tail current source.

The differential oscillator in figure 1e will be used for demonstrating the different sources of phase noise. The circuit can be separated into a model of the tank circuit and a noise generator from the cross-coupled pair as shown in figure 4-2. In the figure,  $L$  represents the tank inductance.  $C$  represents the tank capacitance.  $C_p$  represents the parasitic capacitances of the circuit, including the output buffers and inductor.  $RL$  represents the parasitic resistance of the inductor. Finally,  $R_c$  represents the parasitic resistance of the capacitor in the tank circuit. According to [5], the phase noise of differential oscillators can be determined by looking at singled ended LC tank oscillators using negative resistance. This results in the use of the Lesson equation for thermally

induced phase noise, shown below.

$$L(f_m) = \frac{kTF}{2P_L} \left( \frac{f_0}{Q_L f_m} \right)^2$$

$P_L$  = power dissipated in load resistance

$Q_L$  = resonator quality factor

$$\frac{1}{Q_L} = \frac{1}{Q_{ind}} + \frac{1}{Q_{cap}} \frac{C}{C + C_p}$$

$$Q_{ind} = \frac{R_L}{\omega L} \text{ and } Q_{cap} = \omega C R_C$$

$f_0$  = center frequency

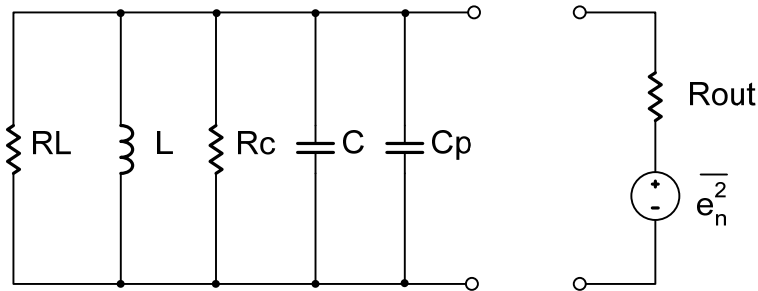
$f_m$  = phase offset

$kT$  = thermal noise

$$F = \frac{R_n}{R_L} = \text{noise factor}$$

$R_n$  = active device equivalent noise resistance

$R_L$  = load resistance



**Figure 4-2:** Separation of cross-coupled pair into tank circuit and noise generator

The Lesson equation shows the contributions to single-side-band phase. Because of the squared term, increasing the Q of the resonant circuit is the highest priority for reducing phase noise.

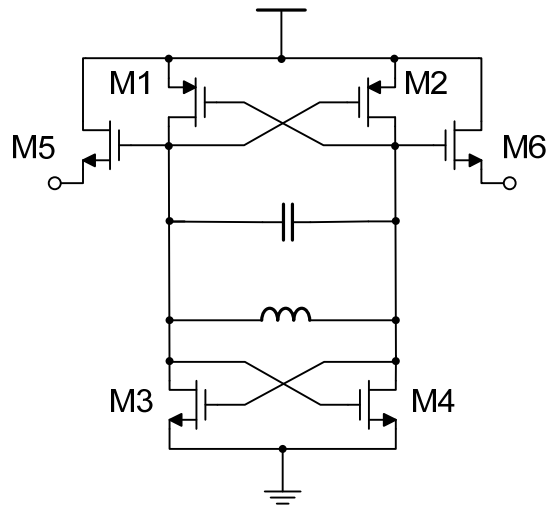
Flicker noise, or 1/f noise, in CMOS circuits results from carrier traps near the silicon / silicon-dioxide interface. A common mistake is to assume PMOS devices exhibit lower flicker noise than NMOS devices, based on historical measurements.

However, flicker noise is process dependent and caused through different interaction at the surface, such as mobility and lattice fluctuations. NMOS flicker noise is associated with fluctuations in the number of carriers, where PMOS flicker noise is mostly related to mobility fluctuations. Flicker noise is given by the following equation.

$$\overline{I_{nd}^2} = \frac{K_f I_d^2 \Delta f}{C_{ox} L W f}$$

$K_f = \text{imperical flicker noise coefficient}$

According to [5], the tail current source, along with its bias circuit, is the biggest contributor of flicker noise in a differential cross-coupled LC oscillator. These flicker noises result in fluctuations in the bias current. This has two different effects. First, consider the oscillator of figure 1a and its common-mode voltage found at the node connecting the sources of the cross-coupled pair. At this node, fluctuations in the bias current lead to fluctuations in the common-mode voltage, which in turn modulates the varactor's bias voltage. The second effect of fluctuating tail current is the result of variations in the oscillator amplitude. This amplitude variation also affects the voltage seen by the varactor. Both of these affects contribute to phase noise.



**Figure 4-3:** Cross-coupled oscillator to be designed

#### 4.5 Oscillator Design

The design of cross-coupled CMOS oscillators is fully developed. Design is based on negative resistance oscillators, with the idea of using a negative resistance device to contribute energy into the system to compensate for losses in the tank or resonator circuit. The following design equations can be used to design the cross-coupled oscillator of figure 4-3 and uses short channel models.



## Circuit Topology Analysis (Short Channel Models)

$R_s$  series loss of inductor

$R_p := (1 + Q^2) \cdot R_s$  parallel loss of resonator

$g_{m_{nmos}} := v_{satn} \cdot c_{ox} \cdot W3$        $g_{m_{pmos}} := v_{satp} \cdot c_{ox} \cdot W1$

$g_{m_{large}} := \frac{-(g_{m_{pmos}} + g_{m_{nmos}})}{2}$

$R_T := \frac{(2 \cdot R_p)}{2 - R_p \cdot (g_{m_{nmos}} + g_{m_{pmos}})}$  equivalent resistance at resonance

$Q_L := \frac{R_p}{\omega \cdot L}$  Q of the inductor

### Start Up conditions

$R_{T_{sw}} := \frac{1}{\left(\frac{1}{R_p}\right) - g_{m_{large}}} < 0$  with stability factor of 2  $g_{m_{large}} \cdot R_p = 2$

### Center Frequency Calculations

$C_{ox3} := c_{ox} \cdot W3 \cdot L3 \cdot scale^2$        $C_{ox1} := c_{ox} \cdot W1 \cdot L1 \cdot scale^2$

$C_{gs3} := \frac{2}{3} \cdot C_{ox3}$        $C_{gs1} := \frac{2}{3} \cdot C_{ox1}$

$C_{gd3} := c_{gd0} \cdot W3$        $C_{gd1} := c_{gd0} \cdot W1$

$C_{db3} := c_{jd3}$        $C_{db1} := c_{jd1}$

$C_{nmos} := 4 \cdot C_{gd3} + C_{gs3} + C_{db3}$

$C_{pmos} := 4 \cdot C_{gd1} + C_{gs1} + C_{db1}$

$C_{tank} := \frac{1}{2} \cdot (C_{nmos} + C_{pmos} + C_L + C)$

$f_0 := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{tank} \cdot C_{tank}}}$

## 5. DiCAD

According to [8], artificial dielectrics were first used to reduce the size of antenna lenses. The authors of [8] also introduced a way to tune transmission line structures using digital techniques through the use of a Digital Controlled Artificial Dielectric (DiCAD). They presented several applications for using DiCAD structures, including a DCO.

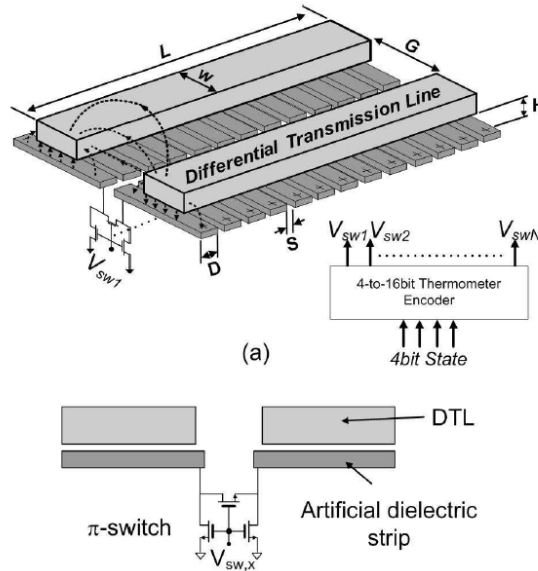
### 5.1 DiCAD basics

Figure 5-1 shows the DiCAD structure presented in [8]. The DiCAD works by placing metal strips underneath a differential transmission line. The effective dielectric under the transmission line obtains a boost when the metal strips are connected. When the strips are connected, the electric field from the differential transmission line orientates the charges in the metal, forming a dipole moment. The formed dipole moment induces a polarization vector, mimicking the molecules in the surrounding dielectric. In a dielectric, the electric flux density,  $D$ , is proportional to the electric field,  $E$ , and the relative permittivity or dielectric constant,  $\epsilon$ , thus  $D = \epsilon E$ . The induced dipole moment is also proportional to the electric field, say  $p = \alpha(\epsilon E)$ . This can be converted into dipole polarization per unit volume by dividing by the volume of the metal strip. The result is added and yields the total electric flux density.

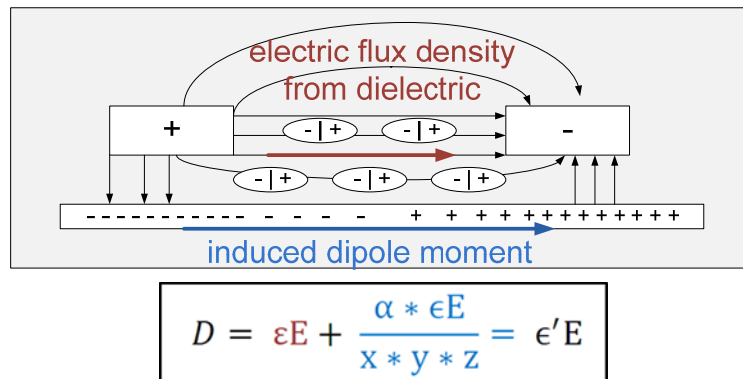
$$D = \epsilon E + \frac{\alpha * \epsilon E}{x * y * z} = \epsilon' E$$

Figure 5-2 is a drawing of the differential transmission line structure along with its

electric fields, the induced dipole moment and the electric flux density from the dielectric.



**Figure 5-1:** DiCAD structure (© IEEE 2009 [8])

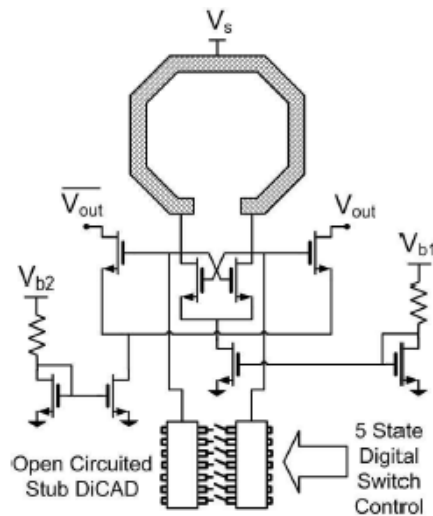


**Figure 5-2:** Diagram of electric field, induced dielectric flux density and dipole moment

Having the ability to control the effective dielectric of the transmission line enables control of the velocity in which a wave propagates down the line. This change in velocity affects the phase delay or S12 parameters of the transmission line and the structure becomes frequency selective. The number of connected metal strips under the

transmission line determines the effective dielectric.

Figure 5-3 shows the DCO implementation presented in [8]. The design has one deficiency in that it exhibits a coarse selection of tuning frequencies. However, the design has great potential because it exhibits lower phase noise than standard LC tank oscillators. The lower phase noise is a result of the higher Q obtained from using the transmission line and lack of varactors which eliminates phase noise contributed from flicker noise in CMOS transistors.



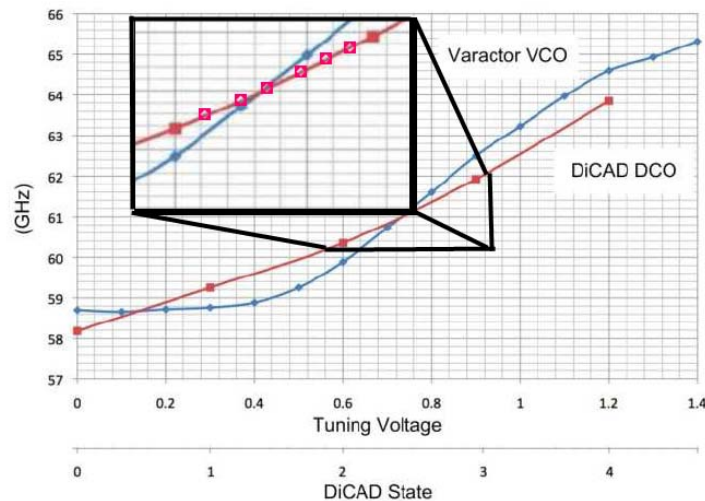
**Figure 5-3:** DiCAD digital controlled oscillator (© IEEE 2009 [8])

## 6. Proposed Fine Tuning range technique

### 6.1 Focus of this work

A coarse tuning range DCO was presented in [8]. The focus of this work is to investigate if a fine-tuning range can be obtained by using the DiCAD structure. The idea is to modulate in time the number of DiCAD metal strips connected. If this work is successful, a DCO for use in an ADPLL will be designed using these techniques.

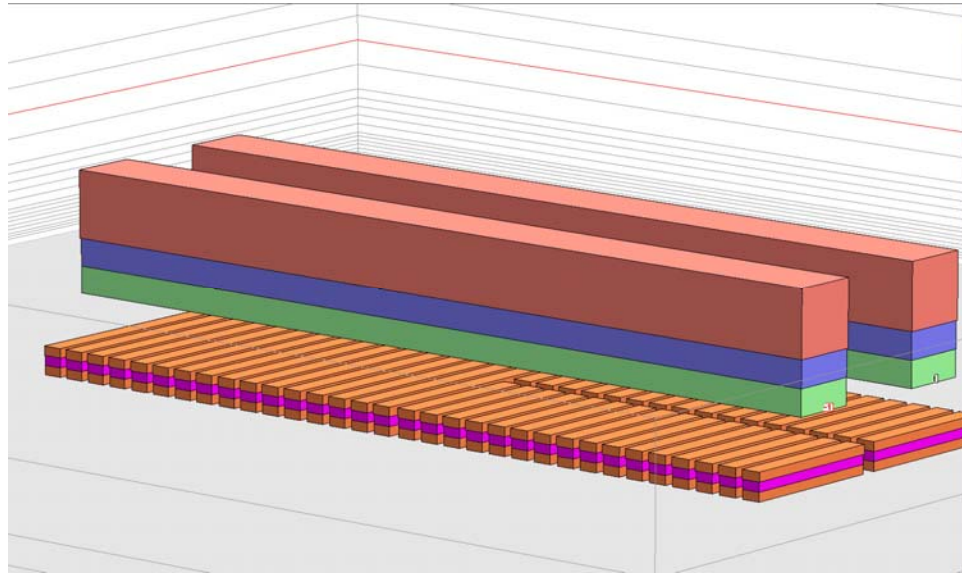
Figure 6-1 shows the comparison of a varactor VCO and a DiCAD DCO. The work of [8] proved the DiCAD controlled oscillator exhibited high tuning linearity compared to the varactor-controlled oscillator. The DCO in [8] obtained tuning steps 1.5 GHz per DiCAD state. This work hopes to reduce the tuning step into smaller steps as shown in figure 6-1.



**Figure 6-1:** Desiring a fine tuning range DiCAD based DCO

## 6.2 DiCAD Analysis

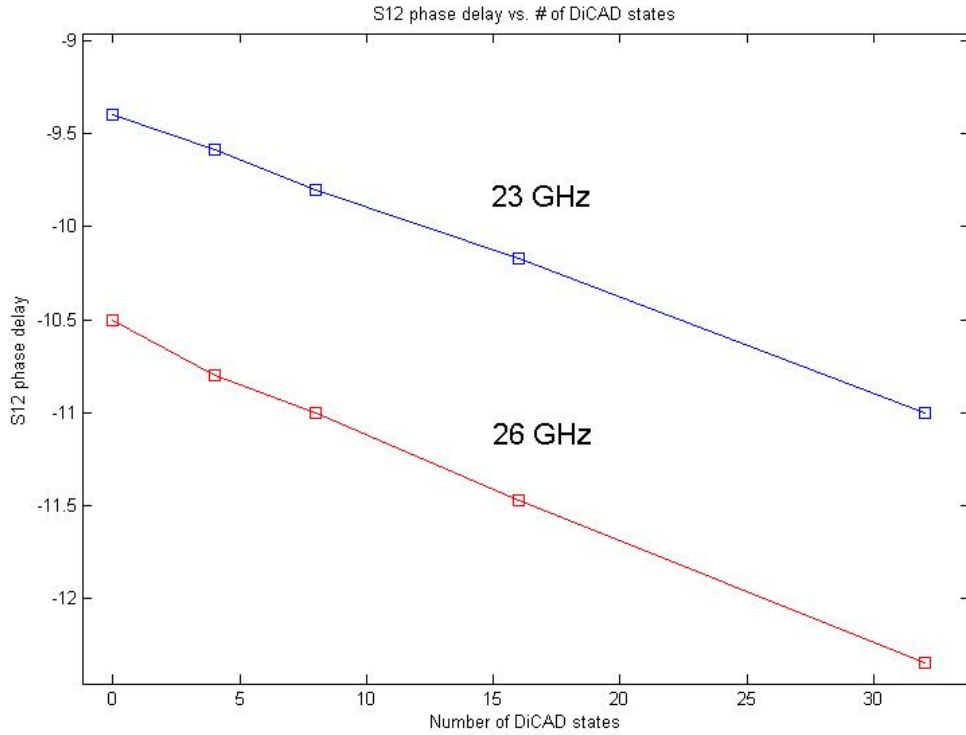
The DiCAD structure was implemented and tested using the FreePDK45nm design kit. The differential transmission line lives in metal layers eight and nine. Where the floating metal strips reside in metal layers six and seven. From [8] it was determined that the spacing between the floating metal strips should be as small as possible. Therefore, this spacing was set to the minimum spacing allowed in metal layer six. The spacing between the differential transmission line (DTL) and width of each individual line determines the characteristic impedance of the DTL. The dielectric constant of the silicon dioxide in the FreePDK45nm kit is 2.5. The addition of floating metal strips under the DTL boosts the dielectric constant. An estimated boost to seven was estimated for initial sizing of the DTL to obtain a characteristic impedance of 23 ohms. An on-line impedance calculator was used for determining the transmission line dimensions. A spacing of 20um and width 10um resulted in a differential characteristic impedance of 23 ohms. An initial test structure, using these dimensions, was created using the FreePDK45nm design rules. Thirty-two floating metal strips were placed under the DTL in attempt to obtain a DCO tuning range of 24.5 – 28.5 GHz. Figure 6-2 shows the 3D plot of the extracted gdsII stream for a structure having 16 of the floating strips connected.



**Figure 6-2:** DiCAD test structure with 16 of 32 metal strips connected.

### **6.3 Simulation of initial test structure**

Five test structures were created each with a different number of metal strips connected. These test structures were imported into Sonnet, which is an electromagnetic (EM) simulator. Successful simulation of the DiCAD test structure required entering the Process Design Kit (PDK) stack-up into the simulator. Table 6.1 shows the dielectric layers used in Sonnet, where table 6.2 shows the metal layers used. Once the stack-up was entered gdsII streams could be imported with ease. Figure 6-3 shows the S12 phase delay vs. number of DiCAD floating strips connected.



**Figure 6-3:** S12 phase delay vs. number of DiCAD states

**Table 6.1:** Sonnet dielectric layers

Layer	Thickness (um)	Mat Name	Erel	Dielectric Loss Tan	Diel Cond (S/m)
0	4	SiO at top	2.5	0	1.00E-12
1	2	SiO at M9	2.5	0	1.00E-12
2	0.82	SiO between M8 & M9	2.5	0	1.00E-12
3	0.8	SiO at M8	2.5	0	1.00E-12
4	0.8	SiO between M7 & M8	2.5	0	1.00E-12
5	0.8	SiO at M7	2.5	0	1.00E-12
6	0.29	SiO between M6 & M7	2.5	0	1.00E-12
7	0.28	SiO at M6	2.5	0	1.00E-12
8	0.28	SiO between M5 & M6	2.5	0	1.00E-12
9	0.29	SiO at M5	2.5	0	1.00E-12
10	0.28	SiO between M4 & M5	2.5	0	1.00E-12
11	0.12	SiO at M4	2.5	0	1.00E-12
12	0.14	SiO between M3 & M4	2.5	0	1.00E-12
13	0.12	SiO at M3	2.5	0	1.00E-12
14	0.14	SiO between M2 & M3	2.5	0	1.00E-12
15	0.12	SiO at M2	2.5	0	1.00E-12
16	0.13	SiO between M1 & M2	2.5	0	1.00E-12
17	0.085	SiO at M1	2.5	0	1.00E-12
18	0.085	SiO at Poly	2.5	0	1.00E-12
19	0.2	substrate	3.9	0	10

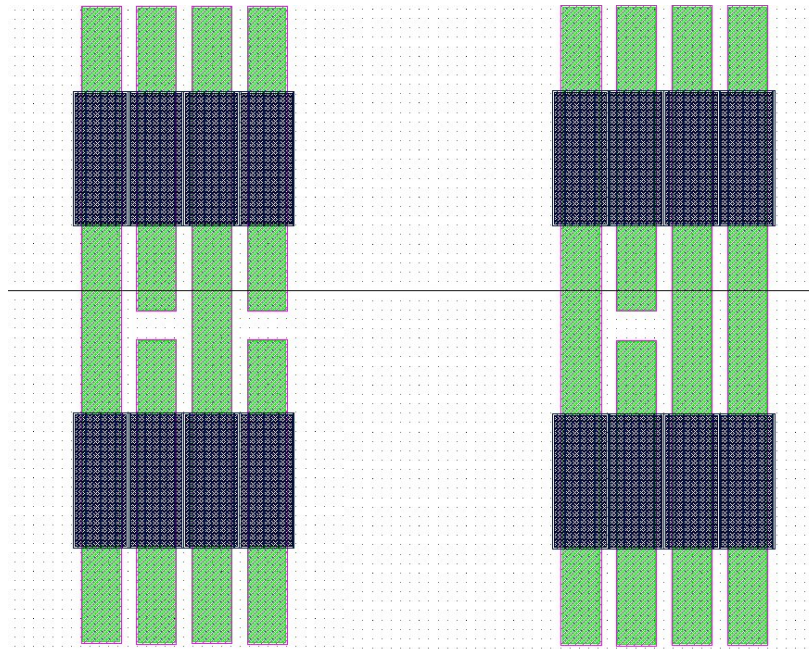


**Table 6.2: Sonnet metal layers**

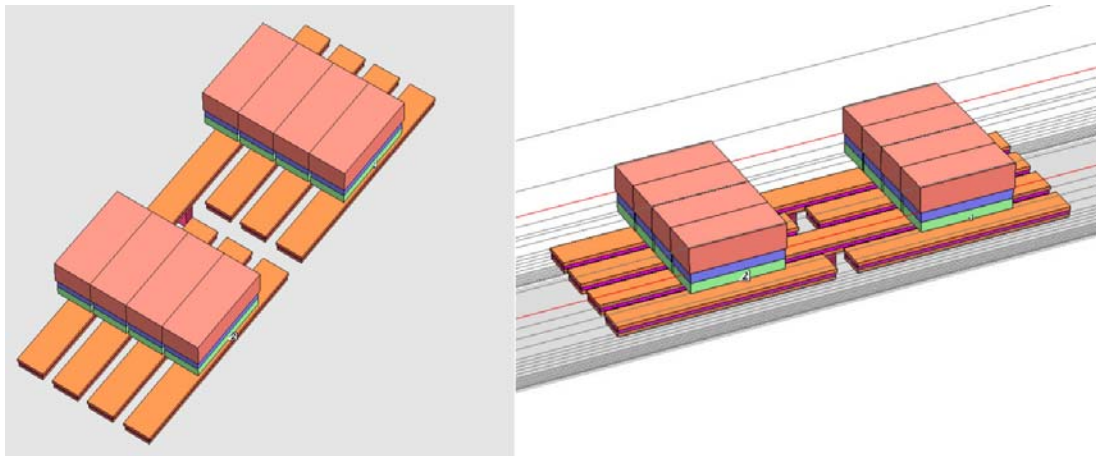
Name	Cond (S/m)	T (um)	Number of Sheets	Model
Metal1	5.80E+07	0.085	2	Thick Metal Type
Metal2	5.80E+07	0.13	2	Thick Metal Type
Metal3	5.80E+07	0.14	2	Thick Metal Type
Metal4	5.80E+07	0.14	2	Thick Metal Type
Metal5	5.80E+07	0.28	2	Thick Metal Type
Metal6	5.80E+07	0.28	2	Thick Metal Type
Metal7	5.80E+07	0.8	2	Thick Metal Type
Metal8	5.80E+07	0.8	2	Thick Metal Type
Metal9	5.80E+07	2	2	Thick Metal Type
via8_9	5.80E+07	0.82	2	Thick Metal Type
via6_7	5.80E+07	0.29	2	Thick Metal Type

#### 6.4 Design of a switchable model

In order to determine if a fine tuning range is obtainable a switchable DiCAD model is required. To accomplish this smaller DiCAD sections were created and simulated using Sonnet. A section size of four was chosen. All states 0/4, 1/4, 2/4, 3/4 and 4/4 were created using the cadence tools and imported into Sonnet. The S-parameters were then extracted using EM simulations. Figure 6-4 shows the 2/4 and 3/4 sections drawn in the Cadence layout tool. Figure 6-5 shows the 1/4 and 2/4 subsections in Sonnet with their connections to ground modeling the actual implementation.



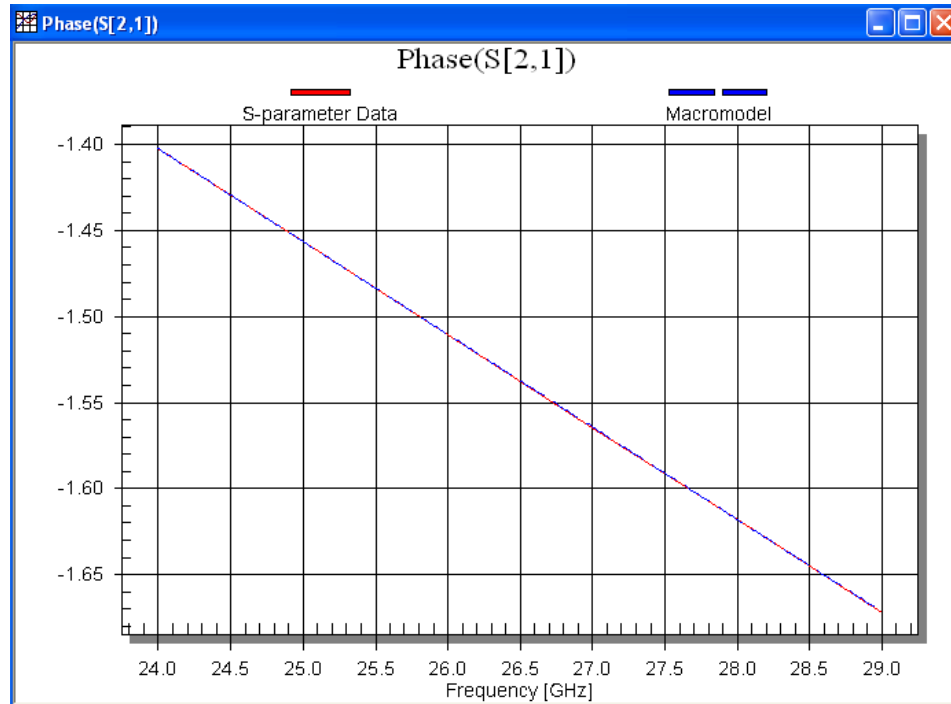
**Figure 6-4:** 2/4 and 3/4 DiCAD subsections



**Figure 6-5:** 1/4 and 2/4 subsections in Sonnet

For each of these subsections, the EM simulation s-parameter results were converted to spice models using a software tool from EM Wonder titled EMtoSpice [10]. Different order models were examined to determine which order yielded the best accuracy. It was determined that an eighth order model had the least amount of error. The eighth order model resulted in a worst case RMS error of 0.000002. The application can

produce plots comparing the S-parameter model to the generated spice model. An example is shown in figure 6-6. The spice models are valid over the frequency range of 24 – 29 GHz.



**Figure 6-6:** S-parameter and Spice model comparison

The different spice models were imported into Agilent ADS to determine the appropriate size inductor and expected tuning range of the resonant structure. The inductor size was chosen for a zero phase delay in the S12 parameters around 26.5 GHz and a DiCAD state of 15 out of 32 floating strips connected. Table 6.3 shows the results from these simulations. With a 1nF inductor the center frequency was 26.5473 GHz, the tuning range was 25.2997 – 28.2407 GHz and with a step size of 73.2 MHz per DiCAD state. These results also reveal the effect on inductor variations. A 10% change in inductance results in a 45% change in resonant frequency. If the inductor value was

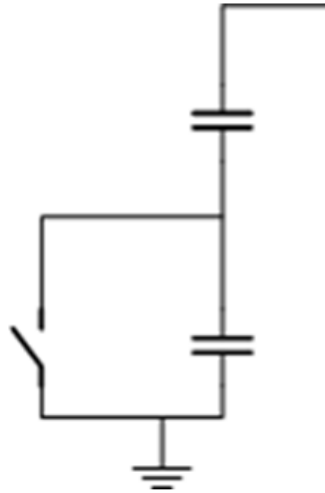
reduced and the length of the DiCAD structure increased the sensitivity to resonant frequency changes for inductor changes would go down. Additionally the tuning range of the inductor / DiCAD resonant circuit would increase. Given the current set up the tuning range is 11%.

**Table 6.3:** Inductor / DiCAD resonant frequencies for different DiCAD states

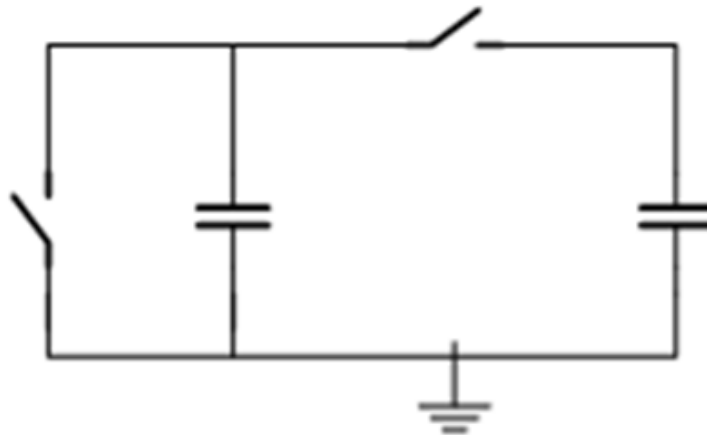
DiCAD state	Inductor		
	0.9 nF	1.0 nF	1.1nF
0/32	>28.5 GHz	28.2407 GHz	26.9516 GHz
15/32	27.9503 GHz	26.5473 GHz	25.337 GHz
16/32	27.8280 GHz	26.4312 GHz	25.2264 GHz
17/32	27.7507 GHz	26.3580 GHz	25.1567 GHz
32/32	26.6348 GHz	25.2997 GHz	< 24.5 GHz

To simulate the modulation of DiCAD states over time a switchable spice model was needed. To simplify the design, 3rd order spice models were created from the 2/4 and 3/4 cell s-parameters. The EMtoSpice software creates models made up of resistors, capacitors and voltage controlled current sources. The combination of voltage controlled current sources and capacitors are used to model the transmission line's inductance. The result is two different situations and both were modeled to simulate the effects of switching the DiCAD. Figure 6-7 shows a switchable transmission line to substrate capacitance. Closing the switch simulates the effect of the DiCAD floating strips being connected together and to ground. The result is the bottom capacitor is shorted to ground, increasing the total capacitance between the transmission line and the substrate. Figure 6-8 shows the capacitors which are connected to the voltage controlled current source. When the DiCAD is connected, the inductance in the transmission line decreases. To model this some of the capacitance is disconnected and shorted out to simulate the loss of

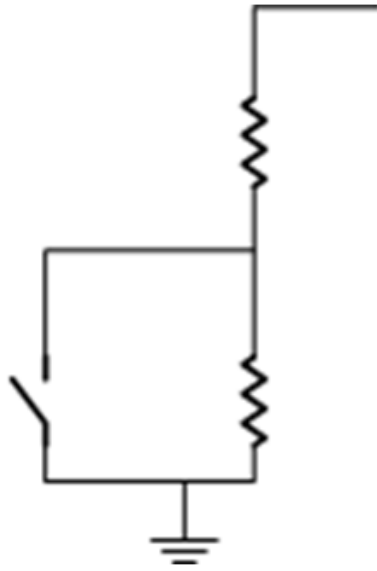
energy which occurs during switching. Switchable resistance values were also created to model the difference in the transmission line losses for the different states. This switchable model can be found in figure 6-9.



**Figure 6-7:** switchable transmission line to substrate capacitance



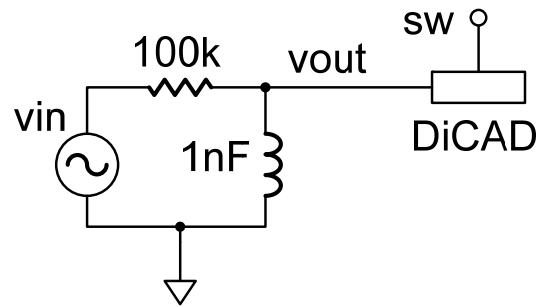
**Figure 6-8:** switchable capacitance simulating a changing in transmission line inductance



**Figure 6-9:** Switchable transmission line losses

### **6.5 Simulation of time varying DiCAD states**

The switchable cell replaced one of the eight subsections and simulations of the s-parameters were ran to compare with the 16/32 and 17/32 simulations results presented in table 6.3. The 16/32 DiCAD state resonant frequency differed by 600 kHz, where the difference in the 17/32 DiCAD state resonant frequency was 300 kHz. Figure 6-10 shows the simulation test setup used for investigating the effects of modulating the DiCAD state. To verify resonance AC simulations were carried out to get an estimate of the expected test circuit resonant frequencies. This was done for the switch being both open and closed. Figure 6-11 shows the results of this simulation. With the switch closed the center frequency was 26.672 GHz, when open it was 26.735 GHz.



**Figure 6-10:** Transient simulation test setup

Next transient simulations ran with the switch in the steady closed and steady open position. This resulted in a resonant frequency of 26.655 GHz when the switch was closed. With the switch open, the transient resonant frequency was 26.718 GHz. The simulation results can be seen in figures 6-12 and 6-13, respectively.

The next step was to investigate the modulation of the switch at different frequencies. A duty cycle of 50% was set and simulated for switching frequencies 500 MHz and 1 GHz. Switching at 500 MHz presented some issues. The resonant frequency shifted in between clock cycles. At switching rates of 1GHz, the drift is small resulting in a steady state resonant frequency. This does not mean that lower clock rates are out. The switching of frequencies in time would result in an average value. However, it would be better to have a single resonant frequency. Figures 6-14 and 6-15 show the drift in phase delay for a 500 MHz switching rate. Figures 6-16 to 6-18 show a close to steady state phase delay of zero during the entire switching period. There is a slight delay around the high to low switching point.

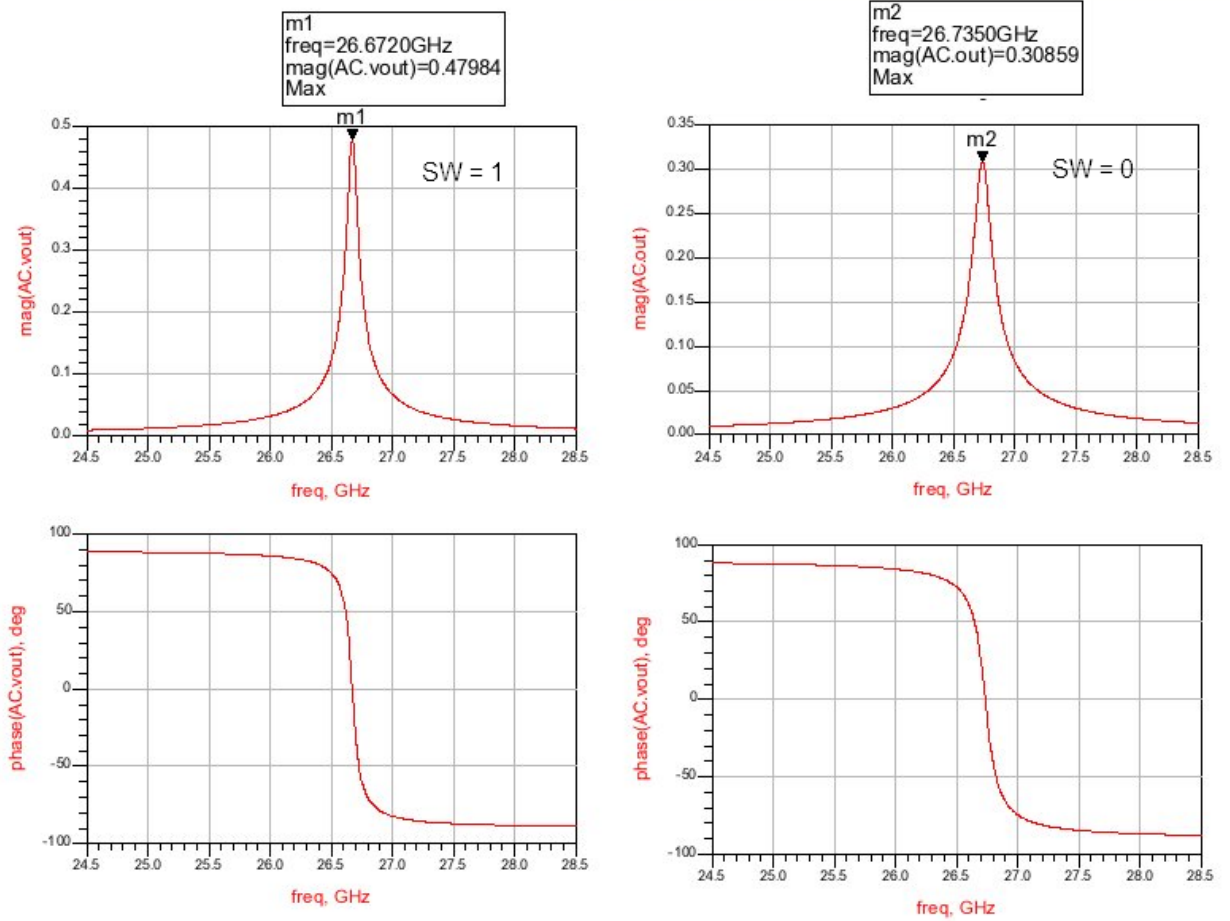
With the switching speed set to 1 GHz the duty cycle was adjusted to see if the

expected fine tuning resolutions could be obtained. Table 6.4 holds the result of this experiment. The largest error was 2.2MHz and the smallest error was 100 kHz.

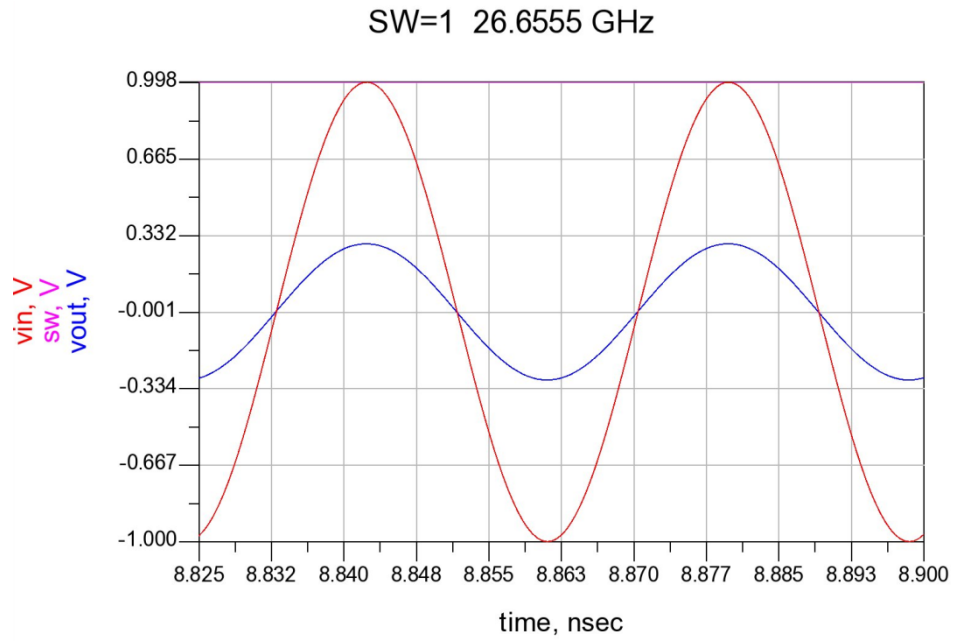
**Table 6.4:** Expected and measured resonant frequencies for varying duty cycles

Duty Cycle	Frequency (GHz)		
	Fo expected	Fo measured	Difference
50.0%	26.6868	26.688	-0.0012
25.0%	26.6711	26.6706	0.0005
12.5%	26.6633	26.6655	-0.0022
6.5%	26.6596	26.6591	0.0005
3.0%	26.6574	26.6575	-0.0001
1.5%	26.6564	26.6565	-0.0001

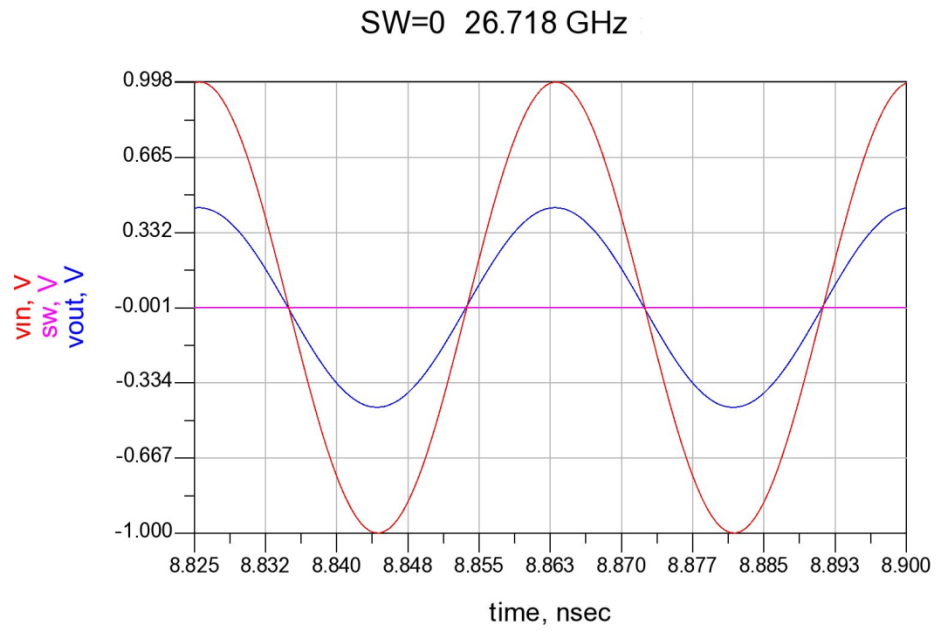




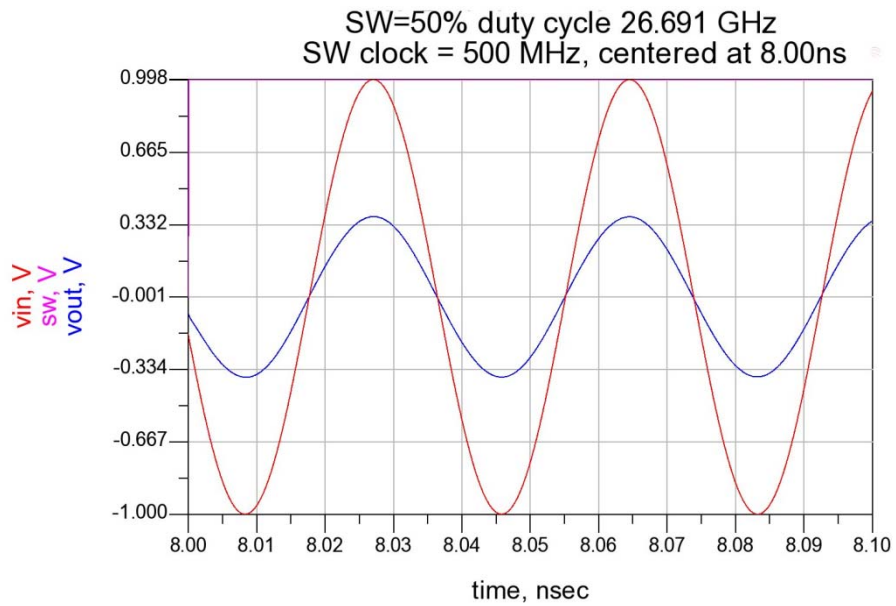
**Figure 6-11:** AC simulation results for switch both high and low



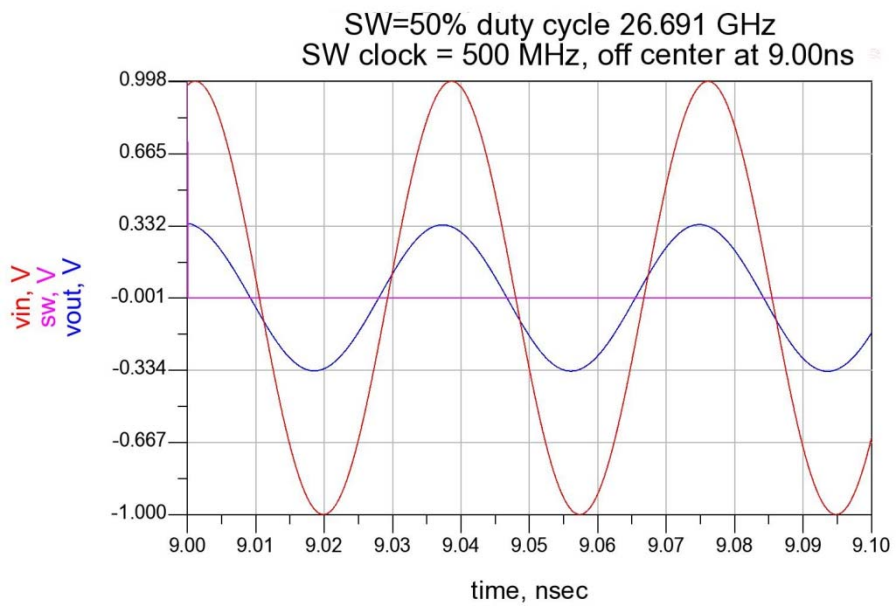
**Figure 6-12:** Transient resonant frequency with switch high



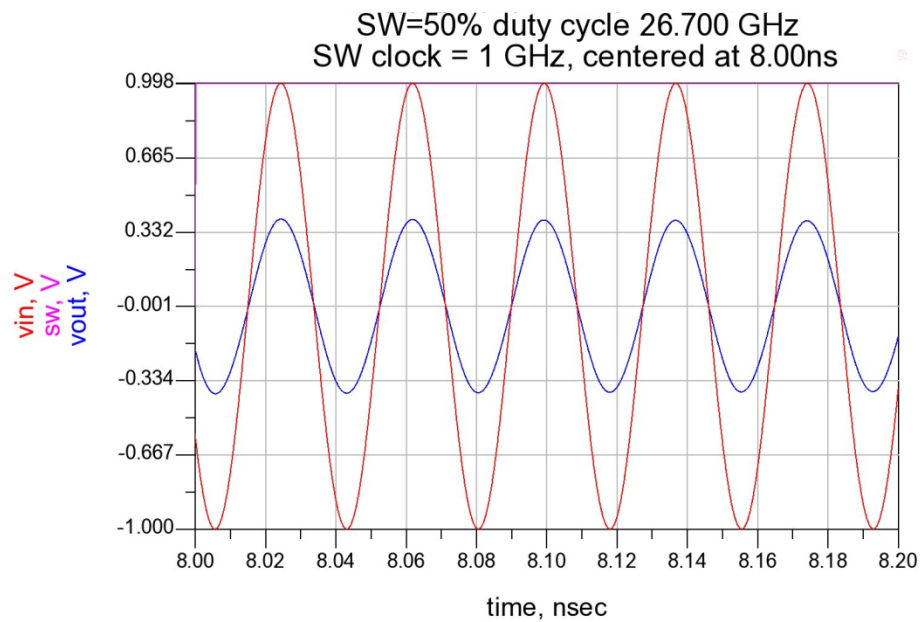
**Figure 6-13:** Transient resonant frequency with switch low



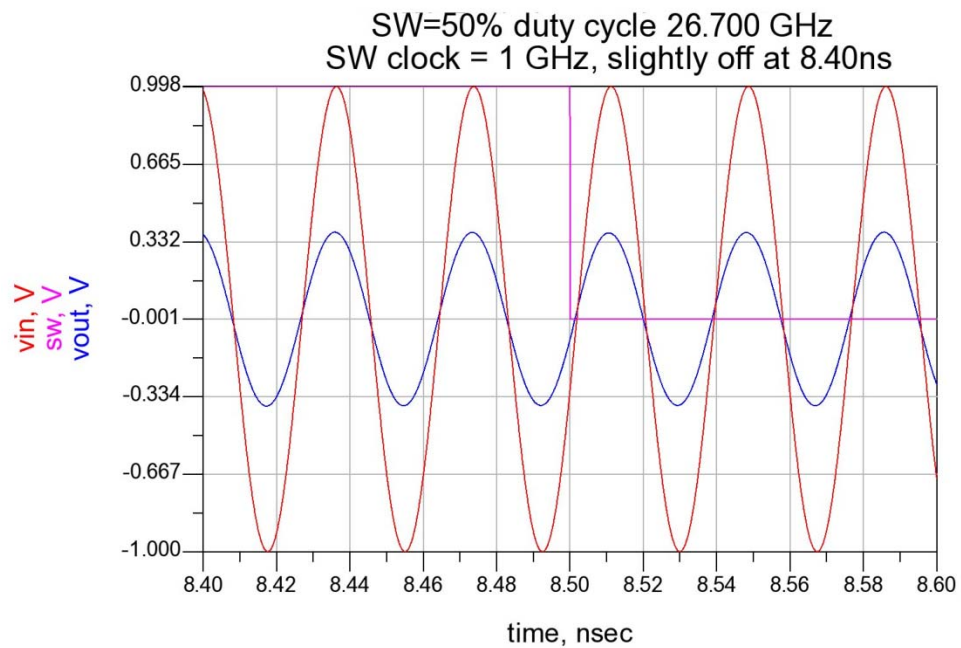
**Figure 6-14:** 500MHz switching rate, phase delay zero w/ switch high



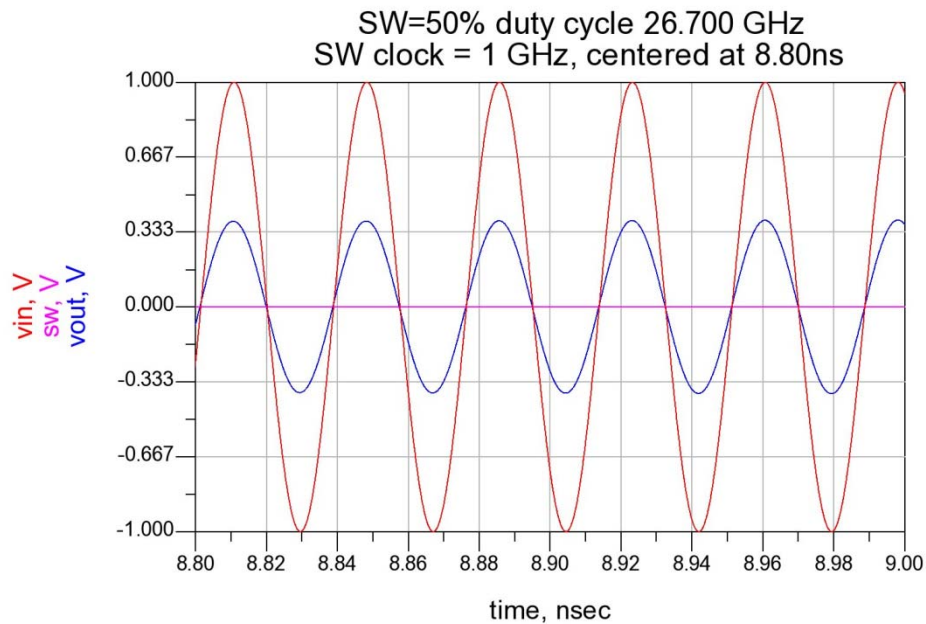
**Figure 6-15:** 500MHz switching rate, phase delay not zero w/ switch low



**Figure 6-16:** 1 GHz switching rate, phase delay zero w/ switch high



**Figure 6-17:** 1 GHz switching rate, slight phase delay at high-to-low switch



**Figure 6-18:** 1 GHz switching rate, phase delay zero w/ switch low

## 6.6 DCO design

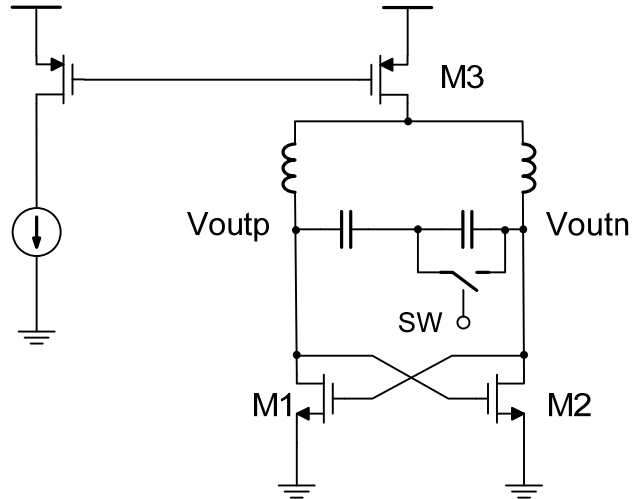
The design of a DiCAD DCO took place in several steps. Earlier the differential DiCAD structure was modeled as a 2-port device. For the DiCAD DCO a switchable 4-port model was required. Also for comparison, a simple cross-coupled DCO was designed to switch between two capacitance values.

## 6.7 Simple Cross-Coupled DCO

Figure 6-19 shows the setup used for analyzing the simple cross-coupled DCO and for comparison with the switchable DiCAD DCO. This is also used to analyze the effect of switching on oscillator stability, oscillator settling and amplitude variations.

Figure 6-20 shows the simulation results of switching the capacitance values at a

clock rate of 500MHz. There is some settling time associated with switching states and some fluctuation in frequency while in each state.



**Figure 6-19:** simple cross-coupled DCO



**Figure 6-20:** simple cross-coupled DCO transient simulation

## 6.8 DCO with switchable DiCAD model

The design of a switchable 4-port model followed a similar process used for the design of the switchable 2-port model. However, some changes were required. In the 2-port model, the EM simulation covered a short range between 24 GHz and 29 GHz. However, for the DCO a more complicated simulation setup was required. For startup and convergence the model need to extrapolate out to DC but still remain accurate within the frequency range of interest, 24-29 GHz. EM simulation was used to extract s-parameters and a forth order spice model was created. A simple text comparison revealed over 150 different circuit components between models, certainly too many to change by hand in a schematic entry program. Instead, a Perl script was used to compare Spectre model files and implement the switchable model. Figure 6-21 shows the Perl script used to created the switchable model.

```
#!/usr/bin/perl -w

my $file0 = "dicad_3_4_11ohm4th.scs";
my $file1 = "dicad_4_4_11ohm4th.scs";
my $output = "dicad_3_4_sw4th.scs";

open dicad_0, "<", $file0 or die "Could not open file: $! \n";
open dicad_1, "<", $file1 or die "Could not open file: $! \n";
open dicad_output, ">", $output;
select dicad_output;

my $lineNumber = 1;
my %dicad_0lines;
my %dicad_1lines;
my $line;
my $numberlines;
my $i;
my ($type, $smaller, $diff, $compName,$net0 , $net1, $val0, $val1);
my ($sw0, $sw1);
my $switch = "relay vt1=300m vt2=800m ropen=1T rclosed=1.00m";

while(<dicad_0>){
    $line = $_;
    chomp($line);
    $dicad_0_lines{$lineNumber++} = $line;
```

```

}
close dicad_0;
$numberlines = $lineNumber;
$lineNumber = 1;

while(<dicad_1>){
    $line = $_;
    chomp($line);
    $dicad_1_lines{$lineNumber++} = $line;
}
close dicad_0;

for ($i=1; $i < $numberlines; $i++) {
    if ($dicad_0_lines{$i} eq $dicad_1_lines{$i}) {
        print "$dicad_0_lines{$i}\n";
    } else {
        $_ = $dicad_0_lines{$i};
        if (/resistor/) {$type = $1};
        if (/capacitor/) {$type = $1};
        if (/vccs/) {$type = $1};
        if (/inductor/) {$type = $1};
        if (/w+/) {$compName = $1};
        if (/=/) {$sval0 = $1};
        if (/^(\w+)/) {$net0 = $1};
        if (/(\w+)\/) {$net1 = $1};
        $_ = $dicad_1_lines{$i};
        if (/=/) {$sval1 = $1};
        if ($sval0 > $sval1) {
            $sw0 = "swn";
            $sw1 = "sw";
            $smaller = $sval1;
            $diff = $sval0 - $sval1;
        } else {
            $sw0 = "sw";
            $sw1 = "swn";
            $smaller = $sval0;
            $diff = $sval1 - $sval0;
        }
        if ($type eq "resistor") {
            print "$compName ($net0 n$i) $type r=$smaller\n";
            print "r$i (n$i $net1) $type r=$diff\n";
            print "w$i (n$i $net1 $sw1 $net1) $switch\n";
        }
        elsif ($type eq "inductor") {
            print "$compName ($net0 n$i) $type l=$smaller\n";
            print "l$i (n$i $net1) $type l=$diff\n";
            print "w$i (n$i $net1 $sw1 $net1) $switch\n";
        }
        elsif ($type eq "capacitor") {
            print "$compName ($net0 $net1) $type c=$smaller\n";
            print "c$i (n$i $net1) $type c=$diff\n";
            print "w$i"."_0 ($net0 n$i $sw0 $net1) $switch\n";
            print "w$i"."_1 (n$i $net1 $sw1 $net1) $switch\n";
        }
    }
}

```



```

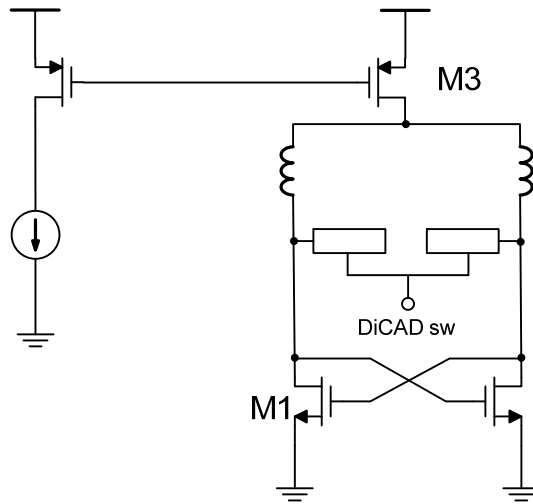
    }
    elsif ($type eq "vccs") {
        print "$compName ($net0 $net1 $net0 $net1) $type
gm=$smaller\n";
        print "G$i (n$i $net1 $net0 $net1) $type gm=$diff\n";
        print "w$i (n$i $net0 $sw0 $net1) $switch\n";
    }
    else {
        die "Error, Found an unrecognized component type";
    }
}
}
}
close dicad_output;

```

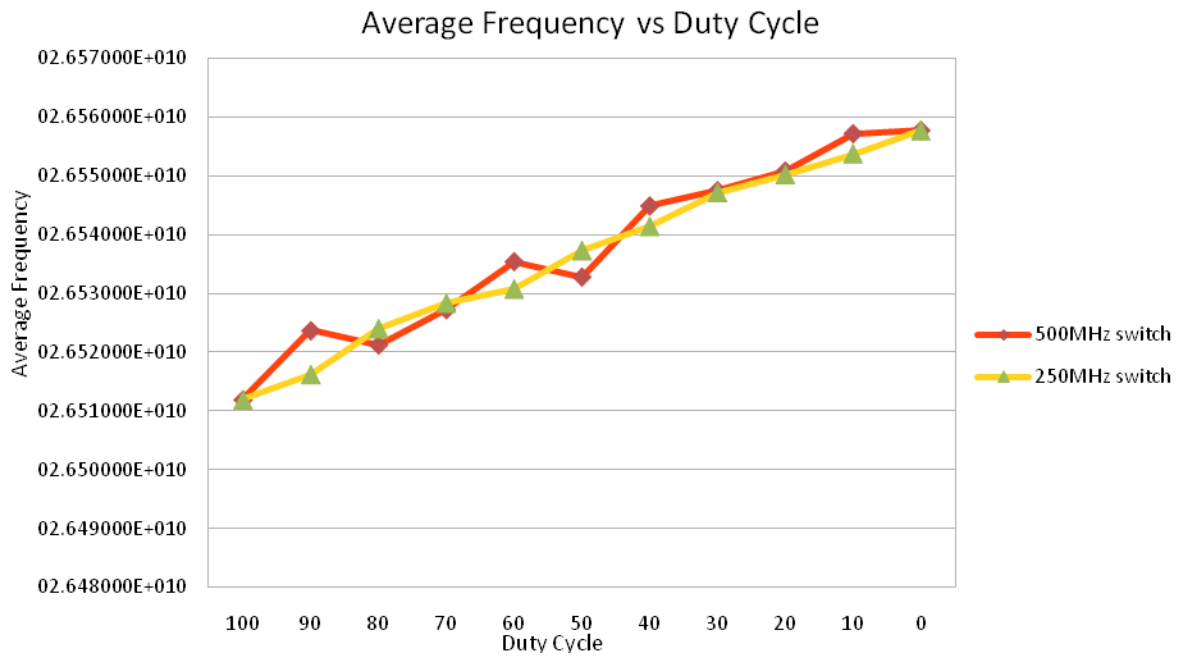
**Figure 6-21:** Perl script used to create a switchable 4-port DiCAD model

## 6.9 Simulation of Switchable DiCAD DCO

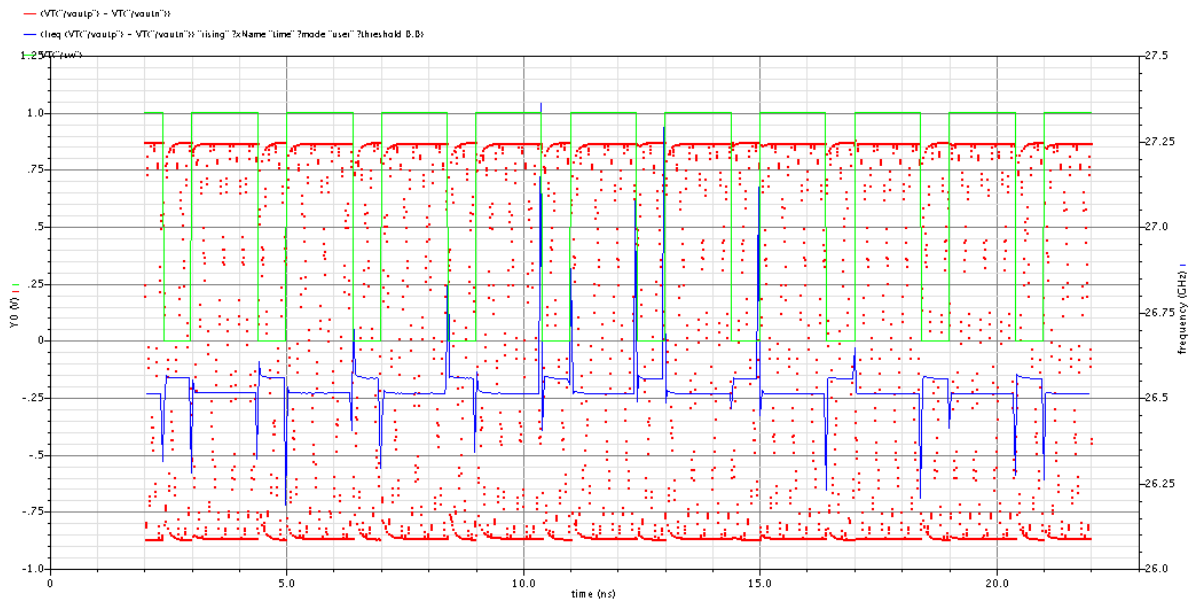
To test for a fine tuning range the circuit of Figure 6-22 was simulated using a switchable DiCAD model which switched between DiCAD states 3/4 and 4/4 along with seven other 3/4 DiCAD cells to make a combined switchable 24-25/32 model. Figure 6-23 shows the linearity of the DCO resonant frequency for different switching speeds. The lower the switching rate the better the linearity. This is because every time the DiCAD is switched the oscillator needs time to settle from the jump in frequency which occurs at the switching time. This can be seen in figure 6-24. The blue line shows the instantaneous frequency.



**Figure 6-22:** transient simulation setup



**Figure 6-23:** average output frequency vs. duty cycle



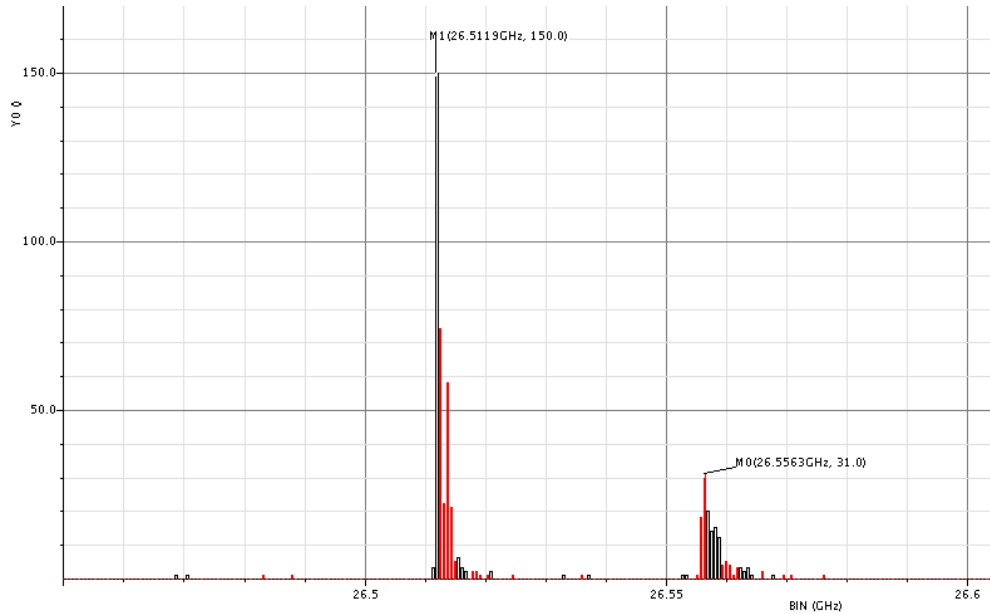
**Figure 6-24:** transient simulation showing large frequency jumps at switching times

## 6.10 Limitation of Fine Resolution Tuning

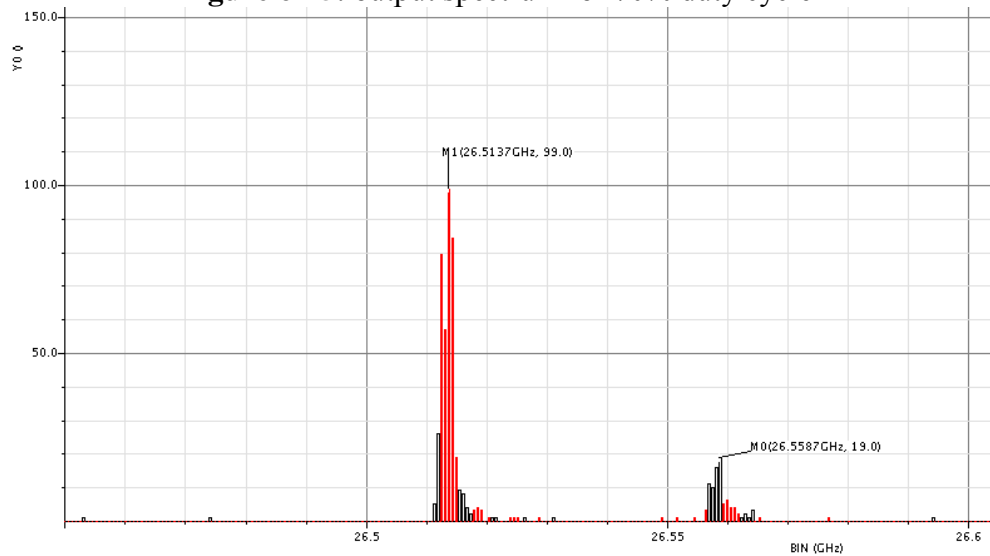
There is a limit to the fine tuning resolution which can be obtained with the DiCAD DCO. This limit is determined by the noise produced from switching the oscillator. As shown in figure 24 there are large jumps in output frequency when the DiCAD is switched. These large jumps appear as noise in the output spectrum and the tuning step needs to result in a change in output spectrum which is higher than this noise. Figure 6-25 and 6-26 shows the output spectrum for duty cycles of 70% and 80%.

Two methods can be used to reduce the noise and improve the resolution of the tuning range. First, sigma delta modulators can break up any periodic occurrences of the large frequency jumps produced during switching. Looking at figure 6-24 it is apparent there is some periodicity induced from the switching rate. Second, by retiming the DiCAD

switching signal to occur when all of the energy is in the inductor the large frequency jumps can be minimized. The finest observable tuning range difference was 1.21 MHz for a change in duty cycle of 5%.

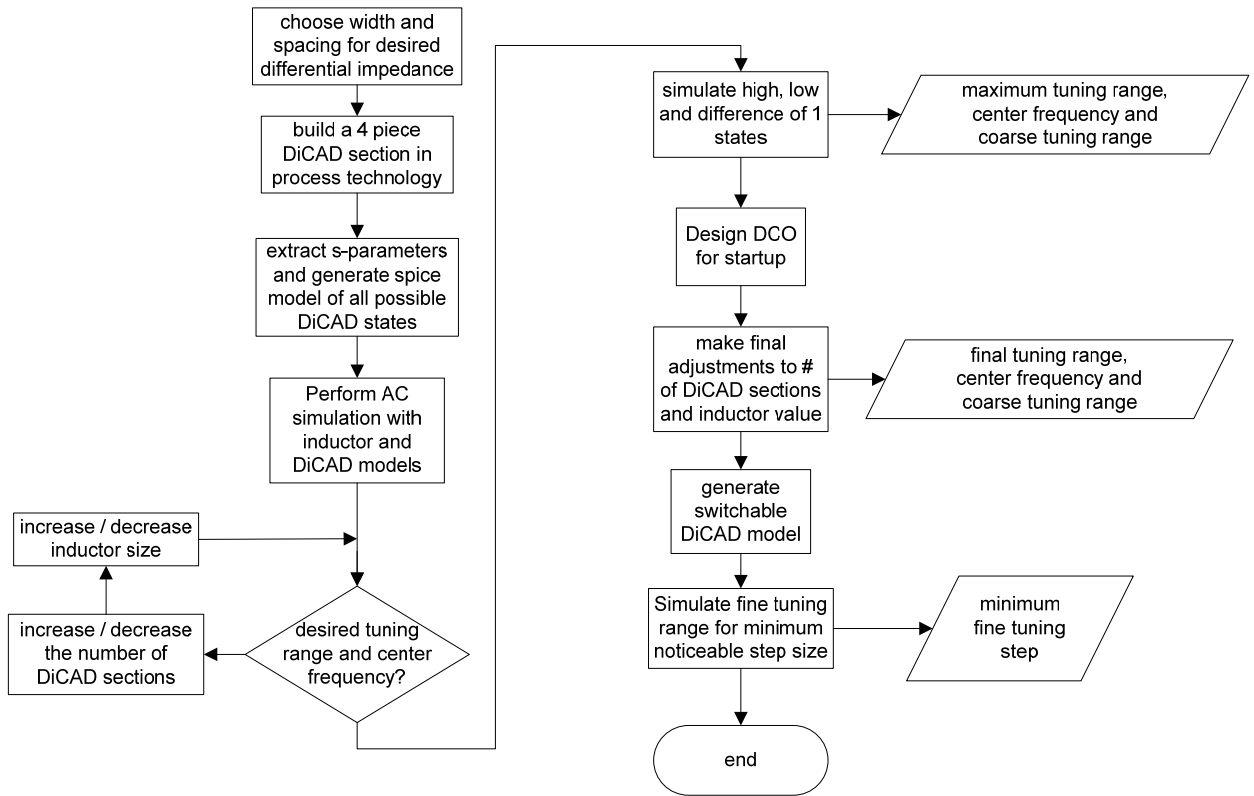


**Figure 6-25:** output spectrum for 70% duty cycle



**Figure 6-26:** output spectrum for 80% duty cycle

## 7. Proposed Design Methodology



**Figure 7-1:** Proposed Design Methodology

Figure 7-1 shows the proposed design methodology, next is a description of all the steps required.

Step 1:

First, choose the desired characteristic impedance for the differential transmission line and determine the appropriate line width and spacing to achieve the desired impedance. The dielectric constant of the silicon oxide should not be used for this calculation. Instead, the characteristic impedance should be multiplied by a factor of 4.

This is because the insertion of floating strips underneath the differential transmission line boosts the effective dielectric constant.

Step 2:

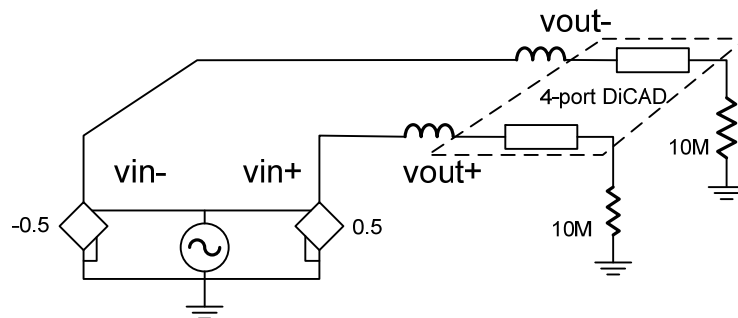
Next, build a four piece section in the process technology. A minimum of a four-piece section should be used to include the effects of neighboring DiCAD sections on each other. All possible DiCAD states should be created and exported as gdsII streams.

Step 3:

Next, perform 4-port EM simulations to extract s-parameters for all possible DiCAD states, from close to DC up two times the highest desired output frequency. Extra frequency points should be added in order to insure high accuracy within and around the desired tuning range. From the touchstone s-parameter files create spice models using EM Wonders EMtoSpice software. Use the smallest order model which obtains the minimum mean-squared-error.

Step 4:

Perform AC simulations using the setup shown in figure 7-2.



**Figure 7-2:** AC test setup for determining center frequency and tuning range

Step 5:

Adjust the number of DiCAD sections and the inductor value to obtain the desired tuning range and center frequency

Step 6:

Simulate with zero DiCAD sections connect and all the sections connected to determine the total maximum tuning range. Simulate two DiCAD states which differ by one connection this determines the maximum coarse tuning step.

Step 7:

Design the DCO so that the oscillator starts up properly and offers good stability.

Step 8:

Make final adjustments to the oscillator to achieve the desired tuning range and center frequency. Because of device parasitic capacitances, additional DiCAD sections may need to be added or the inductor value decreased to obtain the correct tuning range.

Step 9:

Generate the 4-port switchable model using the Perl script. Different order model files offer different stability. The 4th order model was free of voltage controlled current sources and voltage controlled voltage sources and offered the best stability during transient simulation.

Step 10:

Simulate the switchable model to determine what the finest achievable tuning resolution is.

## 8. Conclusion

The DiCAD was presented as a tuning device in digital controlled oscillator. The DiCAD structure was analyzed to see if a fine tuning range could be obtained. A successful fine-tuning range DCO was realized using the DiCAD structure. There is a fundamental limit in the fine tuning range which is based on the noise of the oscillator and noise induced by switching. Furthermore, a design methodology was realized for using the DiCAD in Digital Controlled Oscillators.



## 9. Bibliography

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