Low Voltage Ride-Through Capability for Matrix Converter fed Adjustable-Speed Induction Machine Drives for Industrial and Wind Applications

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Dedication

This dissertation is dedicated to my husband, whose love, support and encouragement made this milestone possible and whose gift of our beautiful daughter Oma, has made our life much more meaningful and joyous. I also dedicate this to my parents, who always supported me in every endeavor. They are the reason I am here at all and made me who I am today.

Abstract

The matrix converter (MC) has been a subject of investigation since 1980, and with the rapid decline in semiconductor cost, better packaging concepts and the improvement in switching characteristics, it is now showing potential to replace the conventional dc link inverter rectifier structures. The MC finds its application wherever bidirectional power flow and controlled voltage and current in AC systems is needed and proves to be superior to its competitors when applied in certain specific environments and circumstances. Wind energy conversion systems (WECS) are also a recent growing research topic where use of MC as power electronic converter is being explored and compared to the performance of conventional voltage source based back-to-back converters. This thesis proposes to address one of the limitations of an MC, which is its ride-through capability. The proposed strategy may help to take matrix converters a step ahead in its struggle for commercialization.

Ride-Through capability of an adjustable-speed drive (ASD) refers to the ability to avoid a system shut-down and thus unwanted delays in drive operation, leading to huge production losses, during short term power interruptions. In the context of wind energy systems, it refers to the grid requirement of the generating systems staying connected to the utility for a defined time during grid faults and disturbances. The ride-through behavior of the system with an MC is a challenging task, because of the absence of storage elements. Due to the direct connection between the grid and the generator/motor drives, any disturbance at the utility grid is immediately reflected on the machine behavior.

The thesis comes up with a novel strategy to enhance the ride-through duration and achieve minimum possible flux deviation in the drive operation, during the voltage sag period, allowing minimum transients during power system restoration. With hysteretic control on the magnitude of motor current, the strategy comprises of keeping the motor continuously operating through a combination of input voltage vector application, aligned in the flux direction and zero vector application, along with discontinuation of MC switches. The strategy has been verified through simulation done in Matlab/Simulink.

The ride-through behavior has been analyzed in integration with a wind energy system and various kinds of under voltage faults studied with different sag magnitudes for industrial applications. Ongoing research is aimed at improving the strategy based on experimental verification using laboratory prototype.

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Chapter 1

Introduction

1.1 Overview- Three phase AC/AC Converters

Several industrial application parts today require ac/ac conversion and hence ac/ac converters are widely used for conversion from the three phase mains source to the three phase output load, e.g. variable speed drives with controllable frequency, amplitude and phase. There are various alternatives for ac/ac converter as illustrated in Fig 1.1, based on a discussion in [1]. The most classic solution is the conventional DC link converter which consists of two converter stages coupled via an energy storage element (inductor or capacitor) in the DC link as shown in Fig 1.2 (a) and (b). The energy storage element helps in the instantaneous decoupling of the two converter stages and hence the input side pulse-width modulated (PWM) rectifier and the output side PWM inverter can be independently controlled.

The other category of ac/ac converters are the Matrix Converters which comprise of an array of four quadrant bi-directional switches, directly connecting the output terminals with the input grid phases without an intermediate storage element. Conventional Direct MC as shown in Fig 1.3 (a) carries out power conversion in a single stage. Alternatively, there exists an Indirect MC, Fig 1.3 (b) which has separate stages for voltage and current conversion like the back-to-back converters but the DC link lacks any storage element.

There are various other existing topological variations of the Matrix Converter (MC) which include the Sparse MC and the Hybrid MC concepts.

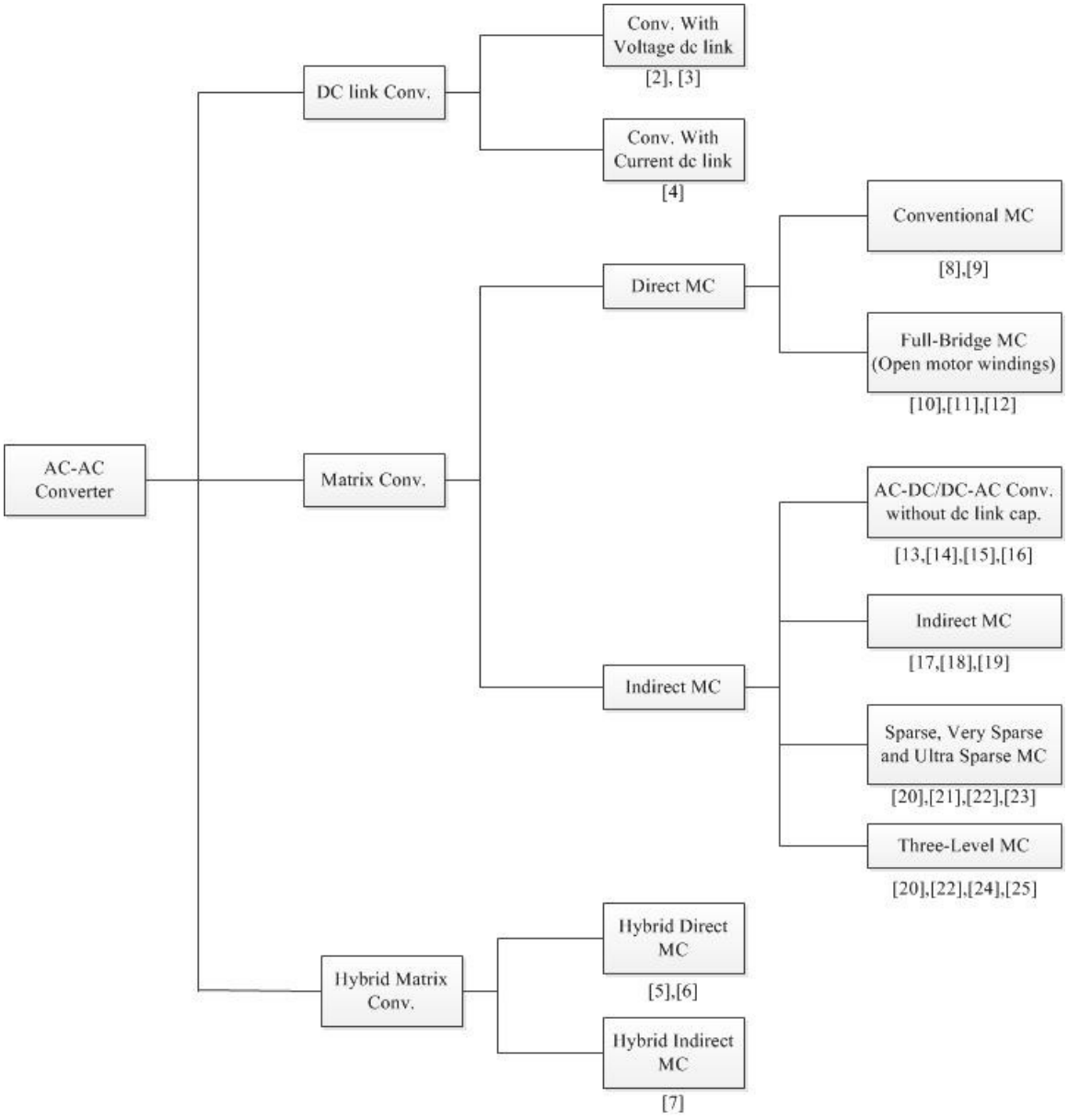
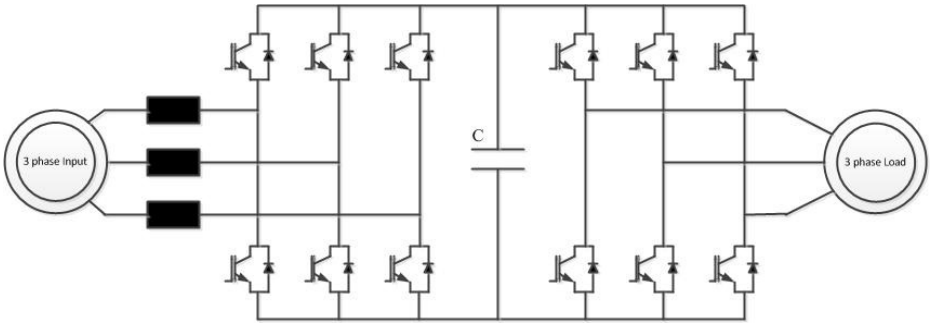
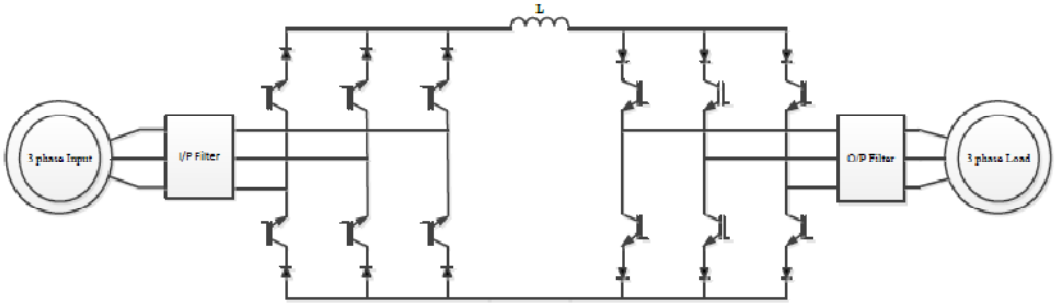


Figure 1.1 Three-phase AC-AC converter circuit categories with references to technical literature [1].

Due to the independence of the voltage form and frequency on the input and output sides, the MC topology holds a promising potential for universal power conversion such as: ac-dc, dc-ac, dc-dc and ac-ac [27].



(a)



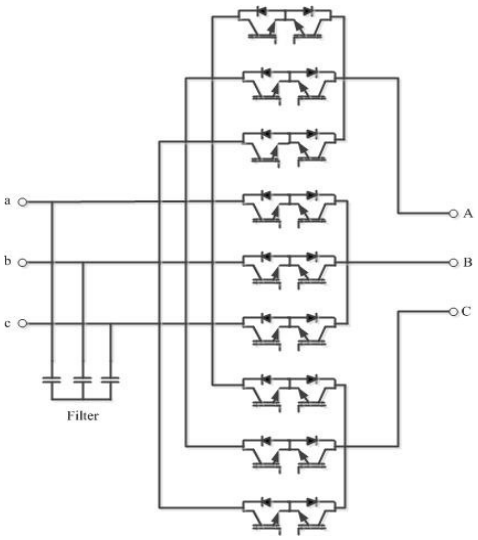
(b)

Figure 1.2 (a) Voltage dc-link converter (b) Current dc-link converter.

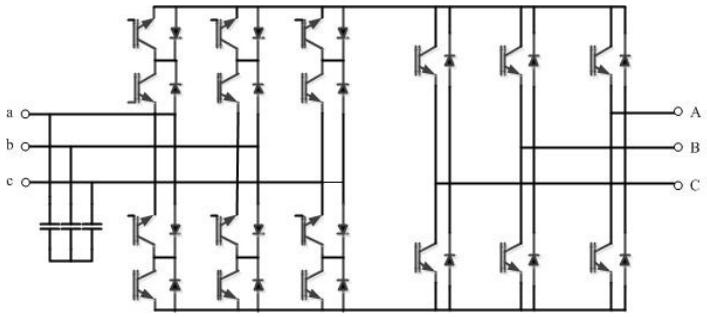
1.2 Research Motivation

Several ac drive applications require use of a compact voltage source converter, with high efficiency and power density, which draws sinusoidal input current at controllable power factor from the input source and provides variable-amplitude, variable-frequency

sinusoidal output voltages. MC's fit this requirement well and hence are becoming increasingly attractive over the years.



(a)



(b)

Fig 1.3 Basic Conventional Matrix Converters (a) Direct Matrix Converter (b) Indirect Matrix Converter.

1.2.1 Advantages of MC over conventional back-to-back PWM VSI

MC's have several advantages over the traditional DC voltage link power frequency converters, which have been well documented in literature [28]–[30]. Some of the important ones are as below:

- An all silicon power module of the MC increases the converter's long term reliability and life as compared to the lifetime-limited large electrolytic capacitors used by the back-to-back converters.
- MC's also show a potential for reduced cost of maintenance, with the innovations in semi-conductor power modules and low power/volume and power/weight ratios and hence they are more suitable for applications where space is a constraint.
- MC's provide sinusoidal input and output waveforms with minimum higher order harmonics generally seen with current commercial inverters.
- They have inherent bi-directional power flow capability with controllable input power factor.
- Last but not the least MC's have minimal energy storage requirements, thus reducing the volume of these converters.

1.2.2 Limitations of MC

Along with the advantages, MC also has certain disadvantages listed as below:

- The maximum input-output voltage transfer ratio of MC's in the linear modulation range is limited to ~ 87%.
- It requires more semiconductor switches due to the absence of existing bi-directional switch, and has complex modulation techniques, for its control.
- Due to absence of intermediate storage elements, MC's are particularly sensitive to voltage disturbances and have no ride-through capabilities.

Recognized as a future concept for adjustable speed drives technology, MC's are still in the realm of a research lab. With a low industrial penetration, the MC is struggling for commercialization, as extensive research continues in an effort to find alternative solutions to its limitations. The lack of fault handling capability is one of its major limitations, which have hindered the practical implementation of this converter for commercial applications.

1.3 Research Objectives

Low voltage ride-through capability during short term power disturbances are a desired characteristic in modern industrial drives. The objectives of this thesis are based on this ride-through limitation of matrix converter. This MC limitation arises due to its lack of energy storage elements which turns out to be both an advantage and a disadvantage.

The primary goal here is to address the issue of input voltage sag handling capability of MC fed adjustable-speed induction machine drives, both for motoring mode and generating mode applications.

With this goal, a strategy to impart limited duration ride-through to the operation of induction drives has been designed. The proposed method requires minimum hardware resources and is able to extend the ride-through duration by a greater amount than the existing ride-through methods with MC's. The simplicity and capability of the proposed method has been demonstrated through simulation in two different commercial applications of the MC. First, for general purpose industrial applications which do not require full power ride-through, and second, for wind energy applications using variable

speed induction generators. The ride-through behavior has been analyzed for various kinds of under voltage faults, balanced and unbalanced, with different sag magnitudes.

1.4 Literature Survey

Matrix Converter has been a topic of research for over two decades now, but the technology is not yet mature enough for a practical industrial implementation. Numerous papers have been published addressing the various issues with MC's by researchers all over the world. Most of the work has been concentrated on modulation algorithms and on practical implementation issues such as device realization and safe current commutation techniques. A brief review of this literature has been presented here for handiness. This section summarizes the modulation techniques, device realization and commutation methods, the input filter issues, protection issues and finally the ride-through capability issues associated with MC's.

1.4.1 Modulation Techniques

As can be seen in Fig 1.3 (a), the Conventional MC consists of an array of nine bidirectional switches which are arranged such that any input line can be connected to any output line at any time. The switch duty cycles are then modulated to generate a desired output waveform on the basis of the demanded output voltage and the input ac supply voltages. Due to the presence of 18 active switches and 27 possible switching combinations for voltage synthesis, several modulation algorithms have been proposed in literature which achieve the desired control objectives. Principally, all modulation schemes create switched voltage or current pulse trains having the same fundamental volt-second or amp-second average as that of the reference waveform. The only difficulty

with these switched waveforms is that they contain unwanted harmonic components which degrade the quality of energy. Hence an optimal modulation strategy would be one which would minimize the input current and output voltage harmonic distortion and also the device power losses. The modulation techniques for MC's can be broadly grouped into carrier based methods and space vector based methods. Under these categories there are several algorithms as shown in Fig 1.4 [31]. The first modulation method was proposed by Venturini [32] based on mathematical formulation though it achieved only 50% voltage. After that, several carrier based methods as well as space vector based methods were developed for MC modulation. The carrier based techniques used either third harmonic injection or variable amplitude carrier whereas the space vector based methods made use of look up tables and complex sector estimation techniques for practical implementation. A comparison of the carrier based methods has been presented recently in [33] for a modulation index within the linear modulation range.

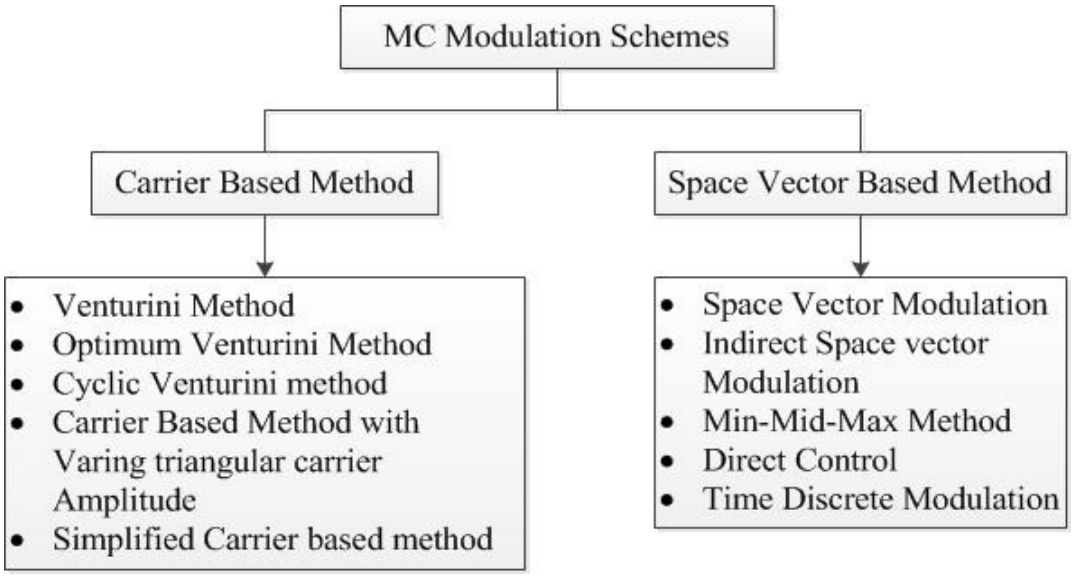


Fig 1.4 Matrix Converter Modulation methods proposed in literature.

1.4.2 Device Realization and Commutation

The first issue with MC starts with the realization of a bidirectional switch. A bidirectional switch is one which can conduct current in either direction and is also capable to block voltage of either polarity [34]. But due to unavailability of a true bidirectional switch, unidirectional devices are suitably combined together to form a switch with bidirectional capability. Fig 1.5 shows different possible bidirectional switch configurations documented in literature [34]-[36].

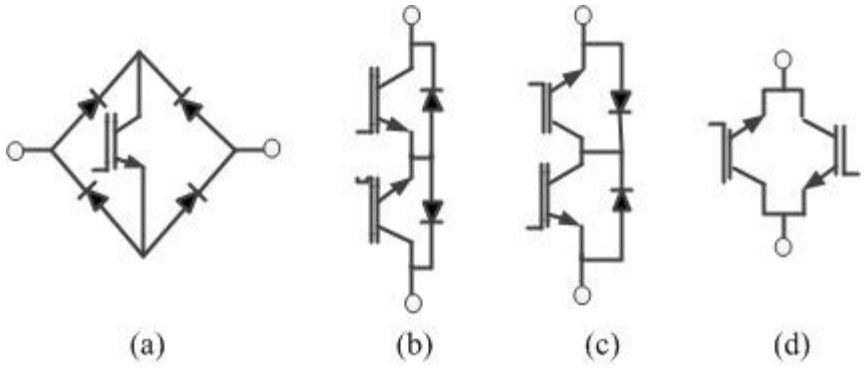


Fig 1.5 Different bi-directional switch configurations (a) Diode Bridge Switch cell (b) Common Emitter IGBT (c) Common Collector IGBT (d) Reverse Blocking IGBT.

Another problem which hindered the MC from being widely used in industrial applications is the commutation problem. The MC is an array of switches, which reveal an absence of passive freewheeling path for the load. For safe commutation, it is desired to prevent any short circuit of input voltage or breaking of load current. This means utmost care has to be taken while developing the timing and synchronization of the switch command signals. Two techniques namely, the two step commutation and the four step commutation have been developed. However these methods depend on the accuracy

of measured output current or input voltage and these may lead to commutation inaccuracies and hence switch failures.

1.4.3 Input Filter Issue

Although the MC is presented as an "all silicon solution", because of the absence of the bulky DC Link capacitors when compared to traditional VSI, yet it is true that MC also requires a minimum set of reactive components represented as the input filter. If viewed from the input supply side, the MC acts like a current source converter and therefore needs an LC filter to minimize harmonics which result in voltage distortions. The issue with input filter design, is that they need to be designed optimally due to the reactive component requirement in an MC which restrict it to small input filters. In other words, use of large reactive components in an MC will make it lose its biggest advantage over traditional DC Link converters. This problem of input filter design has been addressed in quite a few papers [37]-[42] and different configurations have been suggested based on different weights, switching frequencies and modulation strategies. The requirements for the input filter design [43] are as follows:

- To have a lower cut-off frequency as compared to the converter switching frequency.
- Minimum weight, volume and cost for capacitors and inductors.
- Minimum voltage drop due to filter inductance at rated current to avoid reduction in voltage transfer ratio.

In addition a set of considerations for system stability, system efficiency and filter parameter variation also need to be made for an optimized filter design. Hence, coming

up with such an optimized design, is not an easy task and in light of the recent harmonics and EMI reduction standards, it is still an outstanding issue.

1.4.4 Protection Issue

Similar to any other power electronic converter, the MC needs to be protected against over-voltages and over-currents which might damage the semiconductor devices used. These over-voltages might originate due to voltage surge from the AC mains or might be a consequence of switch commutation errors, causing output current interruption. As far as over-currents are concerned, they might arise due to short circuits either at the input side or the output side. To avoid appearance of such destructive over-voltages and over-currents at the MC switches, current freewheeling paths for load de-energization needs to be provided.

Clamp circuit is the common protection scheme for the MC which is operative over all nine bidirectional switches. The clamp circuit comprises of a capacitor connected to all input and output lines through two fast recovery diode bridges as shown in Fig 1.6. Though this clamp circuit protection scheme has the advantage of being very simple and safe in all operating conditions, yet it has some drawback too. First and foremost, it increase the number of semiconductor devices used in the circuit. Secondly, because of the clamp capacitor used, it increases the number of reactive components in the system. Lastly, to optimally design a clamp circuit, the machine equivalent circuit parameters should be known. Another proposed protection scheme has been to use varistors both at the input and output and dissipate any inductive current energy during faulty situations in

these varistors [44]. Nevertheless, the diode clamp is the most widely recognized method of protecting the MC during faults.

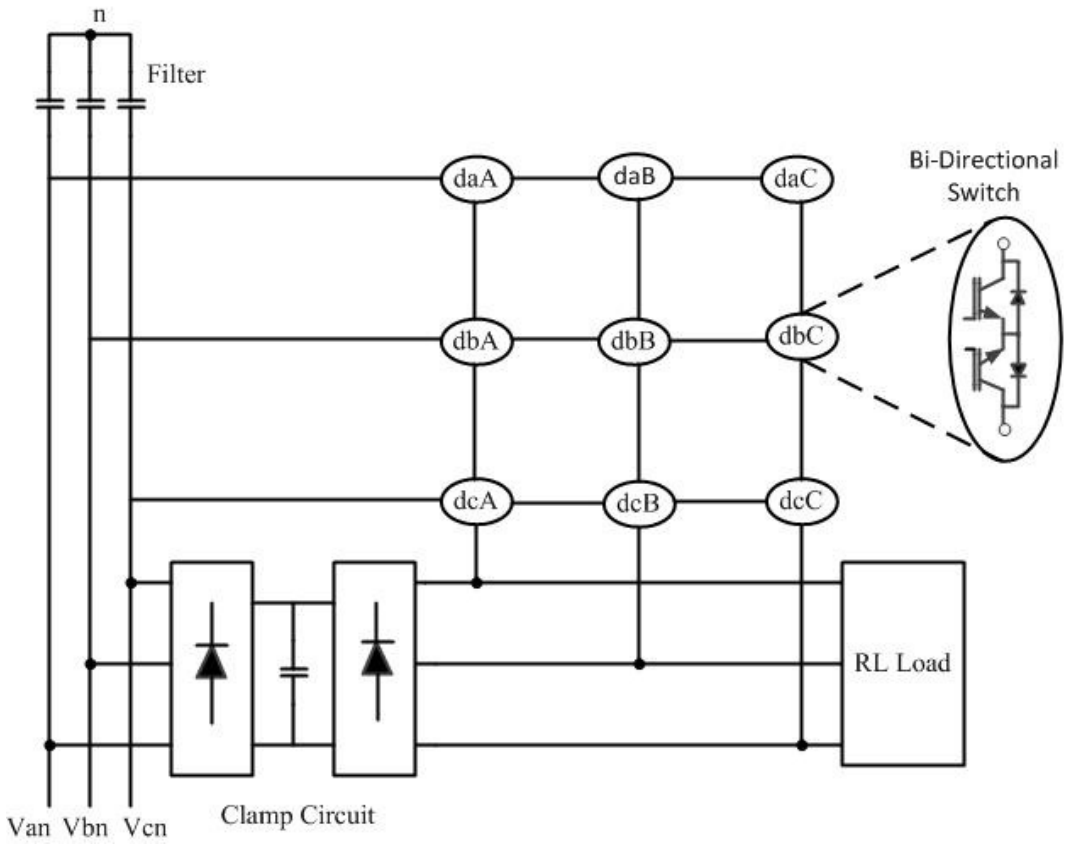


Fig 1.6 Direct Matrix Converter Schematic.

1.4.5 Ride-Through Capabilities

To practically realize a MC for commercial purposes, it needs to have at least limited ride-through capability so that frequent system trips and hence shutdown, can be avoided. The common solution proposed in [45] is very similar to the approach adopted for traditional DC link systems. The strategy consists of isolating the machine from the grid by turning off the switches, and to recover the energy from the load inertia to keep the dc

capacitor voltage in the clamp circuit constant. This capacitor could be connected to the control electronics and hence the controls could be kept alive for limited time. When power system recovers, the controller restarts the drive to its normal operating point.

Another method was proposed in [46], which would help MC fed ASD's to ride-through voltage sags by enforcing constant volts/hertz operation and reduce speed reference if required. Yet another ride-through scheme was proposed in [47], which modified the conventional MC topology by adding extra IGBT switches and a dc link capacitor. A detailed explanation to each of these methods would be given in the later chapters. Despite these proposed methods, there is still lot of scope to improve the ride-through behavior of MC fed variable speed drives, such that it can show a satisfactory performance during commercial implementation of MC's.

1.5 MC Applications

The MC is an attractive converter topology for applications where factors such as elimination of electrolytic capacitors, potential to achieve high power density, reduced size and weight, sinusoidal input and output currents and unity power factor operation are desired. This would include applications ranging from industrial application up to megawatt level, renewable energy applications and also transportation applications. MC applications documented in literature include field oriented control and DTC of motor drives, wind power generation topologies in both squirrel cage induction machine (SCIG) and doubly-fed induction topologies. The MC is also being investigated for use in auxiliary drive system for diesel locomotives [48]. This includes its use in driving traction motors, cooling fan motors, air conditioners and boost compressors. Recently an

increasing number of papers are being reported which are exploring the potential use of MC's in electric aircraft applications [49] and hybrid vehicle applications too [50].

The main hurdles in realizing an industrial MC Drive have been overcome and the first steps towards commercialization have already been taken. Yasakawa Electric built the first commercial MC Drive for low voltage applications like centrifuges, escalators, elevators and test stands and launched it recently in the global market. That being said, MC still has a lot of areas which need to be improved before it can show comparable or superior performance to the conventional VSI's used extensively today.

1.6 Dissertation Outline

This thesis has been organized into seven chapters in the following manner:

Chapter-2 of the thesis presents the ride-through problem in AC Drive applications and its challenges with respect to MC's. It also discusses the specific ride-through requirements by the industrial and renewable energy sector in U.S. The chapter ends by enlisting seven fault scenarios commonly occurring with voltage sags.

Chapter-3 of the thesis gives the mathematical modeling detail of the MC Drive system and then presents the simulation results of the normal mode operation of the MC-Drive followed by the experimental verification.

Chapter-4 presents the proposed ride-through scheme in sufficient detail. The scheme has been simulated for validation. Parametric evaluation of ride-through has been performed followed by the dynamic machine analysis during the short term power disturbance. At the end of the chapter the scheme is compared to the existing MC ride-through schemes.

Chapter-5 presents the MC fed ASD response to the different voltage sag conditions with the proposed ride-through scheme for general purpose industrial applications. The ride-through durations of the system with different load types have also been discussed and simulated.

Chapter-6 develops a wind energy conversion model with MC as the converter and validates the ride-through scheme for such a system based on U.S Grid Interconnection Requirements.

Chapter-7 lists the conclusion and scope for future work.

Experimental setup details have been listed in the Appendix following the chapters.

Chapter 2

Ride-Through in AC Drives

This chapter presents an overview on the ride-through problem associated with AC Drive applications. It then highlights the challenges encountered in handling voltage sags by MC fed ASD's. The chapter also reviews the ride-through requirements, with respect to industrial applications as well as wind power plant applications. Finally, the chapter presents the voltage sag fault scenarios on which the proposed method would be tested in the later chapters.

2.1 Ride-Through Definitions

Many AC Drive applications require the drive to essentially ride-through a short term power disturbance. Ride-through for such applications should meet the specific demand of the application without adversely affecting the process. With numerous application parameters and variation in drive features, to achieve ride-through with acceptable drive performance can be a real challenge.

The term 'Ride-Through' very often has varied meanings for varied applications. In the generic sense, it refers to the capability of maintaining some degree of order and control of the drive operation, during a momentary power disturbance. The different interpretations of ride-through, as discussed in [51] are presented in the sub-sections below:

2.1.1 Power Ride-Through

This category of ride-through is defined as the ability of the drive system to keep the machine controlled and to maintain full speed and torque during a short term power disturbance/loss to the input of the drive. This means, even after an input supply interruption, the drive should continue to deliver full power to the load. In a back-to-back converter, this is done by extracting stored energy from the DC link capacitor and using it to power the drive. Though, it should be remembered that any ride-through energy is subject to the capacitor size. For a Matrix Converter, this kind of ride-through is not possible to attain without any external energy supplying hardware, because of the absence of any internal energy storing component, in this particular converter topology.

Power ride-through is demanded by applications which are process critical like paper and textile mills, for which any speed fluctuation would mean damage to the product and in extreme cases even temporary shutdowns causing huge production losses.

2.1.2 Inertia Ride-Through

This ride-through method requires a load which has a relatively large rotating mass and consequently a large inertia. Here ride-through is achieved by letting the drive operate in regenerative mode. This means that the motor starts acting like a generator and the stored kinetic energy is converted into electrical energy needed for the drive to sustain operation. In this ride-through mode, the drive speed is compromised, to keep the motor modulated and running. In other words, the load is affected here because in order to regenerate, the speed is slowly reduced (output frequency is lowered), and the drive can no longer maintain full power output. The extent of ride-through duration would depend

on the amount of stored kinetic energy in the rotating mass. The benefit of this method is that, the drive has been continuously synchronized to the motor during the power disturbance event, and hence does not need to reconnect to the motor following a power system restoration. This would allow for smooth recovery and minimize any transients in the drive operation.

Inertia ride-through is demanded by applications like fan or pump loads, which do not have continuous full power requirements during short term fault conditions and can afford to lose speed without adversely affecting the process.

2.1.3 Battery Back-Up

This kind of ride-through is needed for true long term fault conditions extending anywhere between minutes to hours. To provide sustained power ride-through for long durations, an external reserve of energy would have to be employed. This could be anything like a simple battery or an uninterruptible power supply, which could provide the AC power needed for the drive to maintain its performance without getting affected by the fault condition. Of course the trade-off here would be the cost involved for the external back-up power reserve. But the benefit would be immense, and the cost would be compensated, if the application demands a continuous supply of power and an unfavorable loss of power can be avoided to meet the demand.

2.1.4 Back-Up Inertia Ride-Through

This ride-through method is used when the application demands sustained power for comparatively longer durations extending to minutes, and where acid batteries cannot be used for back-up power. In these cases, a high inertia flywheel drive is used instead to

provide the energy to the drive for sustained operation. The ride-through duration would again depend on the moment of inertia and speed of the flywheel drive and also on the power consumed by the drive and motor which require continuous operation during the fault event. Since a dedicated flywheel is used, some control over the drive is still maintained and hence the ride-through duration can be optimized in such situations.

2.1.5 Logic Ride-Through

Several applications require the ability to maintain logic functions like communications and memory which means to keep the control electronics running, during a short term fault condition, Unlike power ride-through, logic ride-through requires very low power (mostly what is consumed by the switch mode power supply feeding the control circuits) which can be supplied by the stored energy in the dc link capacitor in case of back-to-back converters and by the clamp circuit capacitor in case of MC fed drives. By keeping the control electronics alive, a graceful and timely recovery from the short term power disturbance event can be attained.

2.2 Ride-Through Challenge with MC Drives

Looking at the above ride-through categories, it can be concluded that for “true power ride-through” , some kind of stored energy is needed in the system, which can safely quickly deliver power to the drive to maintain its operating point, in case of an input power dip/loss. In case of MC’s, as we know there is no significant amount of energy storage, due to the absence of the dc link capacitor. Hence, without adding any external storage, it is not possible to achieve power ride-through with MC’s. This makes ride-

through a challenging issue with MC drives. In this thesis a clamp circuit, which is commonly used for protection purposes, has been used to help in ride-through

2.2.1 Simulation Results

Here, the impact of a symmetrical three-phase sag on the ASDs controlling an induction motor (IM) will be discussed. The basic topology is as shown in Fig 2.1. The induction motor with specification as given in Table 1.1 was assumed to have balanced windings and balanced input voltages from the converter and was simulated using dq analysis. Field orientation control (FOC) is considered. The ASD was modeled in MATLAB/Simulink.

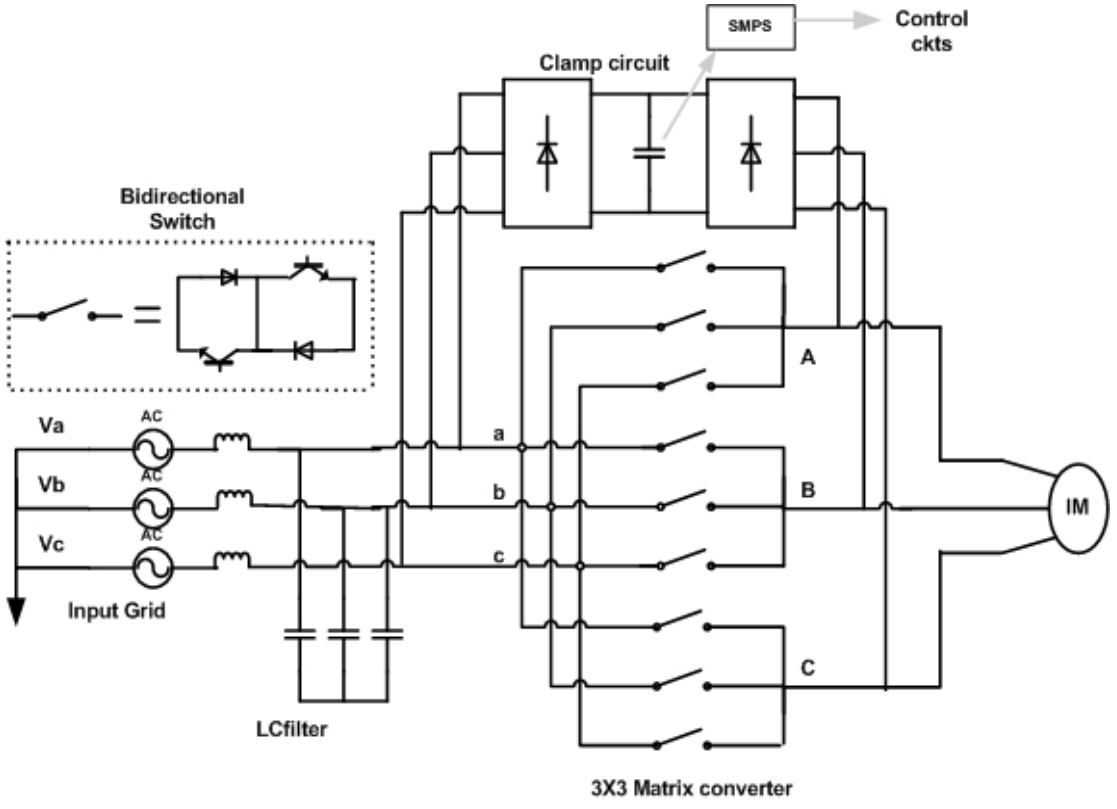


Fig 2.1 Basic MC Drive Topology.

Motor Parameters	Specifications
Power	19KW
$V_{LL,rms}$	250 V
R_r	0.125Ω
R_s	0.19Ω
f_{sw}	15kHz
f_o	60Hz
X_m	13.9Ω
X_{lr}	0.603Ω
X_{ls}	0.641Ω
J	$0.7kgm^2$

Table 2.1 Induction Motor Specifications

A balanced three-phase 25% dip and a zero voltage fault were applied for duration of 150 ms when the system was operating in steady-state at unity input power factor. The stator current waveforms are shown in Fig.2.2 and Fig. 2.3.

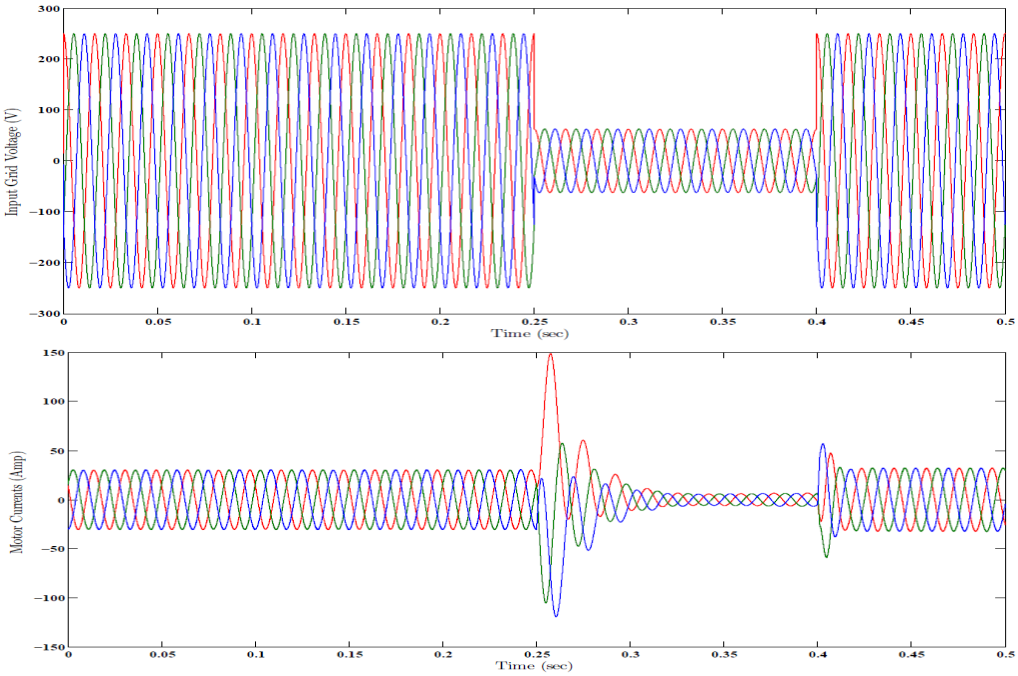


Fig. 2.2 MC Drive Waveforms during 25% voltage dip without ride-through protection (a) Input Grid Voltage (b) Motor over-currents.

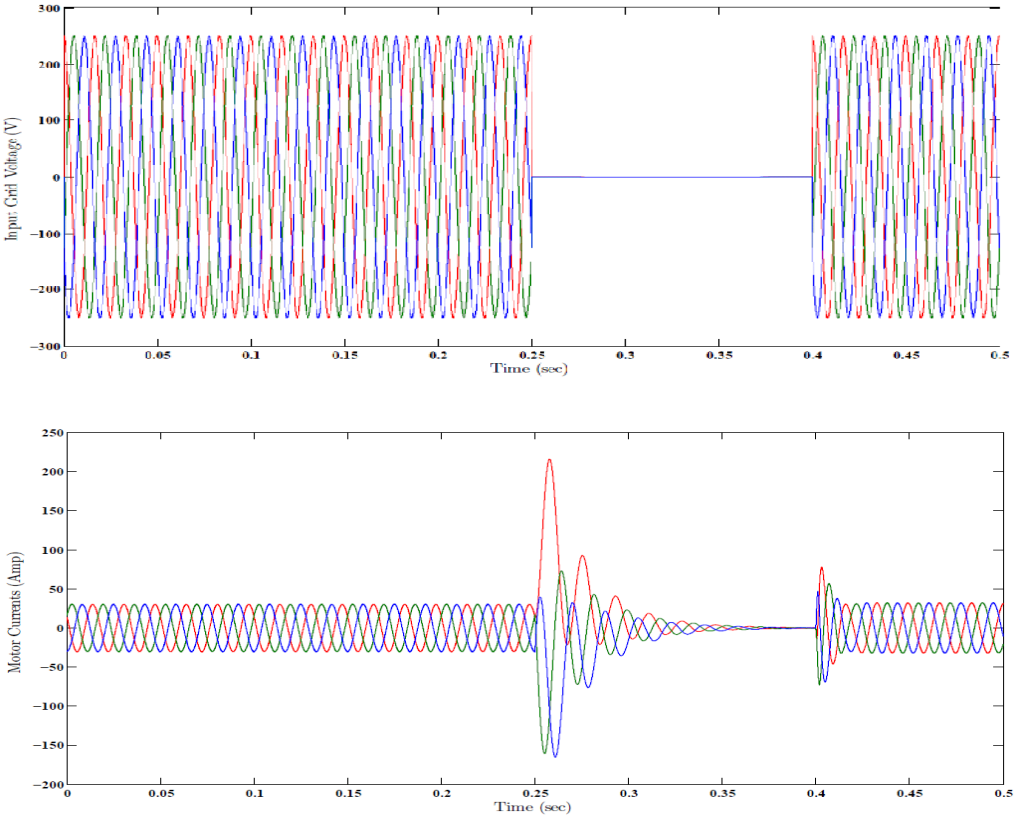


Fig. 2.3 MC Drive Waveforms during zero voltage fault without ride-through protection (a) Input Grid Voltage (b) Three-phase Stator Currents.

As can be seen, a fault at the utility immediately gets reflected on the machine load performance. Over-currents due to sudden imbalance between the reduced voltage at the machine terminals and the back e.m.f leads to over-currents in the system and under voltage in the clamp capacitor voltage. Both these could cause the system to trip leading to a temporary production shutdown interrupting the industrial processes. Hence , there is a great need for enhancing the ride-through capability of the MC Drive systems to keep the machine alive and the clamp capacitor voltage maintained during the fault duration.

The only storage element in the MC Drive systems are the small clamp capacitors, used in the protection circuit to provide a path for load de-energization in case of a switching failure. This leaves us with the option to somehow cleverly manage the energy in the system inertia and the clamp capacitor and achieve "inertia ride-through" and "logic ride-through". This thesis addresses this ride-through issue in MC's and comes up with a novel strategy to keep the motor continuously modulated and hence magnetized and also keep the control electronics alive, assuming they are being fed by a switch mode power supply which takes energy from the clamp capacitor. Thus ride-through is achieved for MC's, which can be suited for applications for which achieving a power ride-through is not required, instead a timely recovery with minimum transients is the essential need.

2.3 Low voltage Sag Ride-Through Requirements

Till the sixties, the consumers of electricity were mostly concerned about the continuity of power supply or in other words the reliability of supply. Nowadays, along with reliability, power quality has also become an equally important concern of the consumers. One of the major reasons for this concern is the widespread use of electronic devices in the industrial environments. As more and more power electronics equipment such as ASD's, are being developed to become more compact, efficient and smaller, they are becoming less tolerant to supply voltage disturbances. Voltage sags are seen as the most important power quality problem due to increased sensitivity of industrial equipment. According to the IEEE Std 1159/95 voltage sag is defined as : *a reduction between 0.1-0.9 p.u. of the voltage and current (on an rms basis) at the power frequency for any*

duration ranging from 0.5 cycles to 1 min [52]. The amplitude would be the remaining voltage value during the sag. IEC terminology is almost the same just that they use the term 'dip' instead of 'sag'. They define voltage dip as: *a sudden voltage reduction at any point in the electrical system lasting from anywhere between half a cycle to few seconds* [53]. Voltage sags may be triggered due to faults at the transmission or distribution levels or due to breaker operation, motor starting causing large inrush currents, transformer energizing, capacitor switching and other such sudden load changes. Sometimes voltage sags are also caused if there is a fault on the nearby feeder, causing voltage drops on other plant feeders. Spurious tripping of ASD's due to protection device sensitivity in response to such voltage sags cost the industries a lot of money for each such unplanned shutdown, in addition to restart charges and penalties of late delivery due to frequent production shutdowns. Therefore it is important to improve the ASD's ability to "ride-through" sags, and hence minimize any losses associated with them [54]-[55].

2.3.1 General Purpose ASD Application Ride-Through Requirements

A number of power quality surveys give us an idea about the characteristics of voltage disturbances, mostly short interruptions and voltage sags, but these are not comparable due to different customer requirements, different applications and hence different definitions. Despite these differences, some general conclusions can be drawn which are as follows:

- Voltage sags are the major cause of disturbances, with a frequency of occurrence between 61% and 87% [56].

- Most of them last for a duration of four to ten cycles and have a voltage magnitude of around 80% [57].
- A majority of the sags are anywhere between 20% and 30% in magnitude and last for a duration of ten cycles or less [58].
- The number of voltage sag events between 70% and 80% are three times more than the number of short term voltage interruptions. Also 35% of the events with duration of 3sec or less, last not more than six cycles [59].
- Among voltage sags, single phase sags are most frequent with a an incidence of approximately 45%, next follows three-phase faults with almost 31% incidence and lastly the two-phase faults with an incidence of nearly 21% [56].

This thesis would be looking at short term voltage dips of sags (single phase, double phase and three phase) ranging anywhere between 0.1 to 0.9 pu and giving a ride-through duration of few cycles to seconds for motoring mode general purpose applications used in the industrial environment. The actual durations would depend on the load parameters and the severity of the sag. Every MC Drive would have its own voltage sag tolerance curve with the proposed ride-through method and depending on that the drives can be analyzed with its suitability to application ride-through needs.

2.3.2 Wind Energy Grid-Code Ride-Through Requirements

Wind energy penetration into power systems has been continuously on the rise in the recent years. The installation of these wind power plants, have now reached important levels where their behavior would have an impact on the transmission system characteristics. Therefore, the grid interconnection codes are being continuously revised

to demand wind power plants to show a behavior more like conventional power plants, in order to maintain power system stability and reliability. These technical regulations vary from country to country. This thesis looks at the US recent grid-code low voltage ride-through (LVRT) requirements, complying to the FERC order 661-A [60] which is illustrated in Fig 2.4 and summarized as below:

- All wind generators are required to stay connected and remain alive during all three phase faults, double phase faults and single phase faults. This means that machine should stay online with no faults and turbine stability issues (no over speed, no instability of machine output current, etc.). Different machines require different controls, hence looking specifically at the variable speed induction generators, it means that the machine needs to maintain magnetization so as soon as the voltage is recovered, the system is ready to pitch the blades back and increase power (power increase rate should be only based on how fast the blades can be pitched).
- The maximum clearing time that a wind plant has to withstand during three phase faults would be 9 cycles, beyond which the plant may disconnect from the transmission system. The normal clearing times during three phase faults would depend on the substation location of the plant.
- There is no requirement for power limitation during fault.
- There is no requirement for reactive power injection during fault or recovery, though during normal operation, reactive power should be between 0.95 leading to 0.95 lagging.

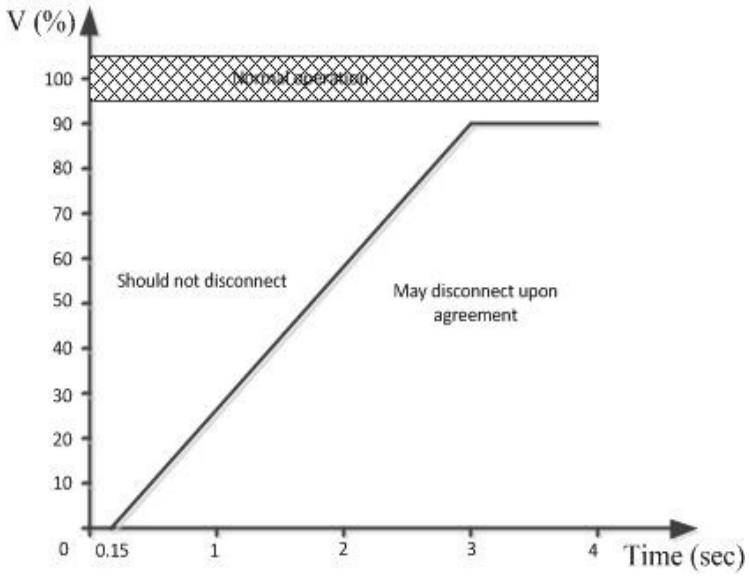
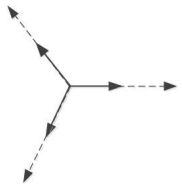
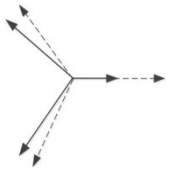
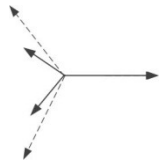
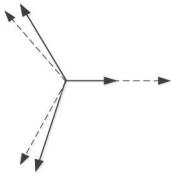
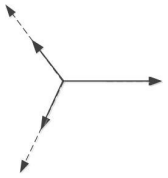


Fig 2.4 LVRT in US-WECC [60].

An important thing to keep in mind is that these codes would continue to be iteratively revised in the coming years by the cumulative efforts of transmission system operators, wind power plant operators and developers, in order to assist the future wind plants to keep the power system stabilized.

2.4 Fault Scenarios

The voltage sags can be grouped into seven types on the basis of ABC classification [61], the phasor diagrams of which with their complex voltages are shown in Table 2.1: the dotted lines are the voltage phasors during pre-fault condition. The solid lines are the voltage phasors during fault. E1 is the pre-fault rms voltage value and V* is the rms value of the residual voltage.

Type	Voltages	Phasors
A	$V_a = V^*$ $V_b = -\frac{1}{2}V^* - \frac{1}{2}jV^*\sqrt{3}$ $V_c = -\frac{1}{2}V^* + \frac{1}{2}jV^*\sqrt{3}$	
B	$V_a = V^*$ $V_b = -\frac{1}{2}E_1 - \frac{1}{2}jE_1\sqrt{3}$ $V_c = -\frac{1}{2}E_1 + \frac{1}{2}jE_1\sqrt{3}$	
C	$V_a = E_1$ $V_b = -\frac{1}{2}E_1 - \frac{1}{2}jV^*\sqrt{3}$ $V_c = -\frac{1}{2}E_1 + \frac{1}{2}jV^*\sqrt{3}$	
D	$V_a = V^*$ $V_b = -\frac{1}{2}V^* - \frac{1}{2}jE_1\sqrt{3}$ $V_c = -\frac{1}{2}V^* + \frac{1}{2}jE_1\sqrt{3}$	
E	$V_a = E_1$ $V_b = -\frac{1}{2}V^* - \frac{1}{2}jV^*\sqrt{3}$ $V_c = -\frac{1}{2}V^* + \frac{1}{2}jV^*\sqrt{3}$	

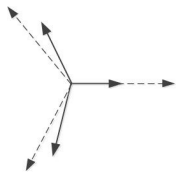
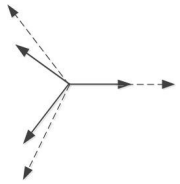
F	$V_a = V^*$ $V_b = -\frac{1}{2}V^* - (\frac{1}{3}E_1 + \frac{1}{6}V^*)j\sqrt{3}$ $V_c = -\frac{1}{2}V^* + (\frac{1}{3}E_1 + \frac{1}{6}V^*)j\sqrt{3}$	
G	$V_a = \frac{2}{3}E_1 + \frac{1}{3}V^*$ $V_b = -\frac{1}{3}E_1 - \frac{1}{6}V^* - \frac{1}{2}jV^*\sqrt{3}$ $V_c = -\frac{1}{3}E_1 - \frac{1}{6}V^* + \frac{1}{2}jV^*\sqrt{3}$	

Table 2.2 Types of Voltage sag faults seen by three phase equipment at the input supply based on ABC classification [61].

For type A sag, all the three phase voltages drop in magnitude by the same amount. For type B and D sag, one phase voltage drops in magnitude while the other two phase voltages only change in phase angle. Such a phase angle difference may be because of difference in X/R ratio between source and feeder or due to unbalance sag transformation to lower voltage levels [62]. For type C sag, two voltage phases drop in magnitude as well as change in phase angle. For type E sag, two voltage phases see a drop only in magnitude. For Type F and G sag, two voltage phases see a drop in magnitude as well as change in phase angle while the third phase voltage sees only a drop in magnitude. For further details on the type of sag, please refer [61]. The thesis simulates the ride-through scheme for MC fed ASD's for all the above seven voltage sag fault scenarios commonly seen by any three phase equipment.

Chapter 3

Mathematical Modeling for the MC Drive System

In this chapter, a vector controlled matrix converter-fed induction motor drive has been simulated. The modulation algorithm which is used to generate the switching signals for the matrix converter power circuit devices gives a unity power factor at the input and is based on the simplified carrier based scheme. The indirect field orientation technique has been implemented in the drive system. The modeling details have been presented below followed by the experimental verification of the simulated results.

3.1 Basic MC Topology

The three-phase MC Drive Scheme as shown in Chapter 2, Fig 2.1 clearly depicts all the different components of this integrated MC fed adjustable-speed drive system. Starting with the converter itself, it has nine four quadrant bidirectional switches which allow for high frequency switching operation. By use of an appropriate modulation scheme, a low frequency output voltage of variable amplitude and frequency can be obtained. If viewed from the input supply side, the MC acts like a current-source converter and therefore requires an LC filter to shape the current. For protection of MC, as already mentioned in Chapter 1, a clamp circuit is used which will be described in detail in the later section. A switched-mode power supply (SMPS) is connected to the clamp capacitor, its stored energy being used to feed the control circuits of the converter. Because one of the advantages of MC is its lower weight due to absence of storage elements, care is taken while designing the passive filter components and the clamp circuit capacitor.

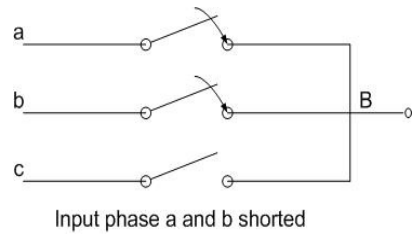
3.1.1 Modulation Scheme

There are two basic switching constraints Fig 3.1, applied for safe operation of matrix converters:

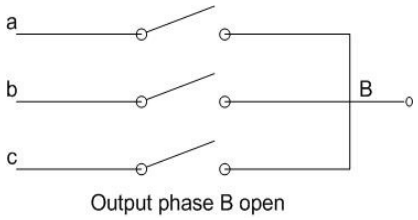
1. Input phases must not be shorted to avoid over-currents due to the inductive nature of the load.

2. Output phases must not be open to avoid over-voltages caused by interruption of the inductive load.

Keeping these two rules in mind, only 27 switching states are permitted with MC operation.



(a)



(b)

Figure 3.1. Switching Rule Violations (a) Input phase short circuit (b) Output phase open circuit.

Various modulation schemes for matrix converters have been described in the literature where few require addition of the harmonics of the output frequency to the modulation

indices and some others require sector information. To avoid complexity and the need for sector information and corresponding look-up tables, the simplified-carrier based modulation scheme [31] has been used for the MC power circuit of the system under study. The following description is taken from [31].

For output voltage synthesis, the duty-ratios of the three switches in each phase are defined as d_{aA}, d_{bA}, d_{cA} for output phase A, d_{aB}, d_{bB}, d_{cB} for output phase B, and d_{aC}, d_{bC}, d_{cC} for output phase C respectively.

- **Input Frequency Elimination**

  The input voltages are

  $$v_a = \hat{V}\cos(\omega t),\ v_b = \hat{V}\cos(\omega t - 2\pi/3),\ v_c = \hat{V}\cos(\omega t - 4\pi/3)$$

  The synthesis for output voltages is done by time-weighting the input voltages by duty-ratios as follows:

  $$v_A = d_{aA}v_a + d_{bA}v_b + d_{cA}v_c$$

  $$v_B = d_{aB}v_a + d_{bB}v_b + d_{cB}v_c$$

  $$v_C = d_{aC}v_a + d_{bC}v_b + d_{cC}v_c \qquad (3.1)$$

  To synthesize the output voltages, independent of input frequency, the duty-ratios are selected such that input voltages are in stationary reference frame and output voltages in synchronous reference frame. The duty-ratios for output phase A, d_{aA}, d_{bA}, d_{cA} are $k_A\cos(\omega t - \rho), k_A\cos(\omega t - 2\pi/3 - \rho), k_A\cos(\omega t - 4\pi/3 - \rho)$.

  Substituting these values in the above equations we get

$$v_A = \frac{3}{2} k_A \hat{V} \cos(\rho)$$

where k_A is the modulation index for output phase A and is defined as $k_A = k\cos(\omega_o t)$ where ω_o is the desired output frequency. Therefore the output voltage in phase A is

$$v_A = \left(\frac{3}{2} k \hat{V} \cos(\rho)\right)\cos(\omega_o t) \tag{3.2}$$

- **Introduction of offset duty-ratios**

Offset duty-ratios are added to the existing duty-ratios so that at any instant the net duty-ratios of the individual switches is always positive. Also, they should be added equally to all the output phases so that they have a null effect on the load. To utilize the input voltage capability to the fullest for maximum output voltage generation, an additional common-mode term equal to $\left[-\{\max(k_A, k_B, k_C) + \min(k_A, k_B, k_C)\}/2\right]$ is added to the duty-ratio of each phase. Thus the new duty-ratios for output phase A are

$$d_a^A = D_a(t) + \left[k_A - \{\max(k_A, k_B, k_C) + \min(k_A, k_B, k_C)\}/2\right] \times \cos(\omega t - \rho)$$

$$d_b^A = D_b(t) + \left[k_A - \{\max(k_A, k_B, k_C) + \min(k_A, k_B, k_C)\}/2\right] \times \cos(\omega t - 2\pi/3 - \rho)$$

$$d_c^A = D_c(t) + \left[k_A - \{\max(k_A, k_B, k_C) + \min(k_A, k_B, k_C)\}/2\right] \times \cos(\omega t - 4\pi/3 - \rho)$$

where (3.3)

$$D_a(t) = \left|0.5\cos(\omega t - \rho)\right|, D_b(t) = \left|0.5\cos(\omega t - 2\pi/3 - \rho)\right|, D_c(t) = \left|0.5\cos(\omega t - 4\pi/3 - \rho)\right|$$

Similarly we can calculate the duty-ratios for the other phases.

- **Input power factor**

  To calculate the input power factor, the input currents are synthesized by time-weighting the output currents by duty-ratios

$$i_a = d_{aA} i_A + d_{aB} i_B + d_{aC} i_C$$

$$i_b = d_{bA} i_A + d_{bB} i_B + d_{bC} i_C$$

$$i_c = d_{cA} i_A + d_{cB} i_B + d_{cC} i_C \qquad (3.4)$$

  Because i_A, i_B, i_C are three-phase balanced quantities, so

  (The common mode terms in d_{aA}, d_{aB}, d_{aC} etc.)$\times (i_A + i_B + i_C) = 0$

  Hence,

$$i_a = (k_A i_A + k_B i_B + k_C i_C)\cos(\omega t - \rho) \qquad (3.5)$$

  Where $k_A i_A + k_B i_B + k_C i_C = \frac{3}{2} k I_o \cos\varphi_o$ with φ_o as the output power factor angle. To have unity input power factor, $\rho = 0$.

  Finally, the switch duty-ratios are compared with a triangular carrier waveform to generate switching signals.

3.1.2 Protection Scheme

For matrix converter protection, clamp circuit has been used. It comprises of two fast recovery diode bridge rectifiers and a capacitor. The input side rectifier is used to clamp the capacitor voltage to the input voltage. The output side rectifier is used to provide a path for current in case of commutation errors or other faulty situations.

3.2 Induction Machine Modeling

The induction machine modeling is done by developing mathematical equations for the dynamic analysis of the machine operation in terms of dq- windings. For further details on the equations, please refer to [70]. I have attempted to use the same notations to provide consistency. Below are the equations used to develop the induction motor model. The subscripts s, r, d, and q refer to stator, rotor, d-axis and q-axis respectively. ω_d is the speed of the stator flux-linkage vector while ω_{dA} is the speed of the dq reference frame relative to the actual physical rotor. L_m refers to the magnetizing inductance. $L_s = L_m + L_{ls}$ and $L_r = L_m + L_{lr}$. L_{ls} and L_{lr} are the stator and rotor leakage inductances and p is the number of poles.

State Equations:

$$\frac{d\lambda_{sd}}{dt} = v_{sd} - R_s i_{sd} + \omega_d \lambda_{sq} \tag{3.6}$$

$$\frac{d\lambda_{sq}}{dt} = v_{sq} - R_s i_{sq} - \omega_d \lambda_{sd} \tag{3.7}$$

$$\frac{d\lambda_{rd}}{dt} = v_{rd} - R_r i_{rd} + \omega_{dA} \lambda_{rq} \tag{3.8}$$

$$\frac{d\lambda_{rq}}{dt} = v_{rq} - R_r i_{rq} - \omega_{dA} \lambda_{rd} \tag{3.9}$$

Supporting Equations:

$$\omega_{dA} = \omega_d - \omega_m \tag{3.10}$$

$$\omega_d = \frac{d}{dt}\theta_{da} \tag{3.11}$$

$$i_{rq} = \frac{\lambda_{sq} - L_s i_{sq}}{L_m} \tag{3.12}$$

$$i_{rd} = \frac{\lambda_{rd} - L_m i_{sd}}{L_r} \tag{3.13}$$

Final Equations:

Rotor (in state space form):

$$\frac{d}{dt}\begin{bmatrix}\lambda_{rd}\\ \lambda_{rq}\end{bmatrix} = \begin{bmatrix}0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}v_{rd}\\ v_{rq}\end{bmatrix} - \omega_{dA}\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\lambda_{rd}\\ \lambda_{rq}\end{bmatrix} + \begin{bmatrix}-R_r & 0\\ 0 & -R_r\end{bmatrix}\begin{bmatrix}i_{rd}\\ i_{rq}\end{bmatrix} \tag{3.14}$$

Stator (in state space form)

$$\frac{d}{dt}\begin{bmatrix}\lambda_{sd}\\ \lambda_{sq}\end{bmatrix} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}v_{sd}\\ v_{sq}\end{bmatrix} - \omega_{d}\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\lambda_{sd}\\ \lambda_{sq}\end{bmatrix} + \begin{bmatrix}-R_s & 0\\ 0 & -R_s\end{bmatrix}\begin{bmatrix}i_{sd}\\ i_{sq}\end{bmatrix} \tag{3.15}$$

Net Electromagnetic Torque on the Rotor:

$$T_{em} = \frac{p}{2}(\lambda_{rq} i_{rd} - \lambda_{rd} i_{rq}) \tag{3.16}$$

3.2.1 Vector Control

Accurate control of speed and position can be accomplished by vector control of induction-motor drives which emulate the performance of dc and brushless-dc motor servo drives. For the decoupling of flux and torque, the d-axis is aligned with the rotor flux-linkage space vector such that the rotor flux linkage in the q-axis is zero. The simplified equations used to model the vector controlled induction motor drives are as below:

State Equations:

$$\frac{d\lambda_{sd}}{dt} = v_{sd} - R_s i_{sd} + \omega_d \lambda_{sq} \tag{3.17}$$

$$\frac{d\lambda_{sq}}{dt} = v_{sq} - R_s i_{sq} - \omega_d \lambda_{sd} \tag{3.18}$$

$$\frac{d\lambda_{rd}}{dt} = -R_r i_{rd} \tag{3.19}$$

$$\frac{d\lambda_{rq}}{dt} = 0 \tag{3.20}$$

Supporting Equations:

$$\omega_{dA} = -\frac{R_r i_{rq}}{\lambda_{rd}} \tag{3.21}$$

$$i_{rq} = -\frac{L_m i_{sq}}{L_r} \tag{3.22}$$

$$i_{rd} = \frac{\lambda_{rd} - L_m i_{sd}}{L_r} \tag{3.23}$$

Final Equations:

Rotor (in state space form):

$$\frac{d}{dt}\begin{bmatrix}\lambda_{rd}\\ 0\end{bmatrix} = \begin{bmatrix}0 & 0\\ 0 & 0\end{bmatrix}\begin{bmatrix}v_{rd}\\ v_{rq}\end{bmatrix} - \omega_{dA}\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\lambda_{rd}\\ 0\end{bmatrix} + \begin{bmatrix}-R_r & 0\\ 0 & -R_r\end{bmatrix}\begin{bmatrix}i_{rd}\\ i_{rq}\end{bmatrix} \tag{3.24}$$

Stator (in state space form)

$$\frac{d}{dt}\begin{bmatrix}\lambda_{sd}\\ \lambda_{sq}\end{bmatrix} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}v_{sd}\\ v_{sq}\end{bmatrix} - \omega_{d}\begin{bmatrix}0 & -1\\ 1 & 0\end{bmatrix}\begin{bmatrix}\lambda_{sd}\\ \lambda_{sq}\end{bmatrix} + \begin{bmatrix}-R_s & 0\\ 0 & -R_s\end{bmatrix}\begin{bmatrix}i_{sd}\\ i_{sq}\end{bmatrix} \tag{3.25}$$

Net Electromagnetic Torque on the Rotor:

$$T_{em} = -\frac{p}{2}\lambda_{rd} i_{rq} \tag{3.26}$$

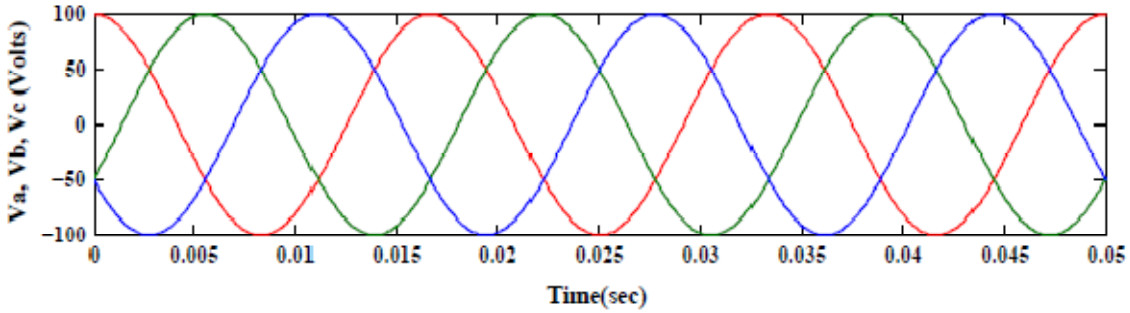
3.3 Simulation Results

A switching model of the MC is built in Matlab® using the Simulink® toolbox. The induction motor model is developed using the machine dynamic equations in the previous section with the specifications as listed in Table 3.1.

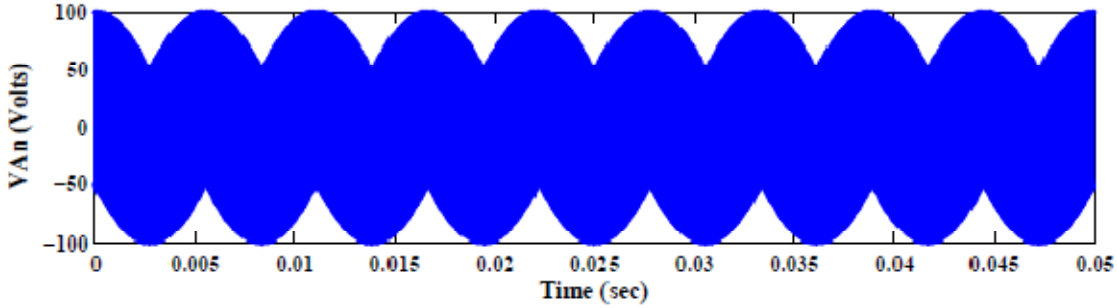
Motor Parameters	Specification
Power	3HP/2.24kW
$V_{LL,rms}$	200 V
R_r	0.55 ohms
R_s	0.9375 ohms
f_{sw}	10kHz
L_m	0.0663H
L_{lr}	0.0022H
L_{ls}	0.0022H
J	0.015kg-m^2

Table 3.1 Induction Motor Specifications

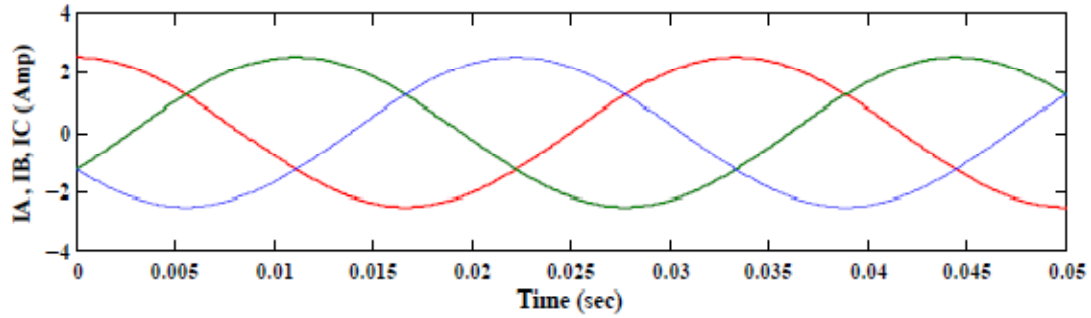
The waveforms of the voltages and currents as plotted are presented in this section.



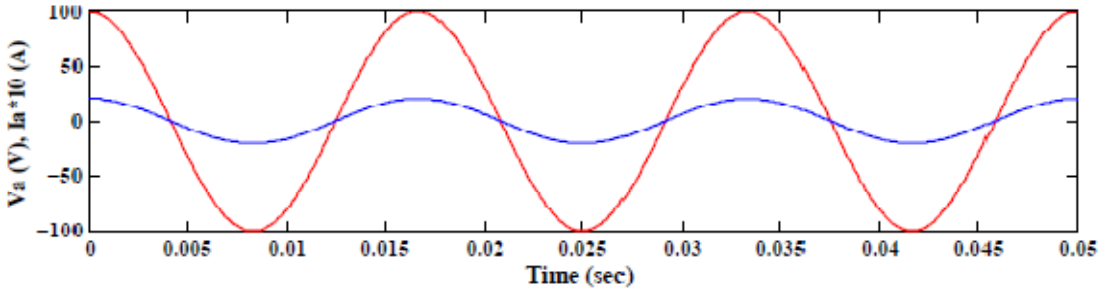
(a) Three-phase Input Grid Voltages



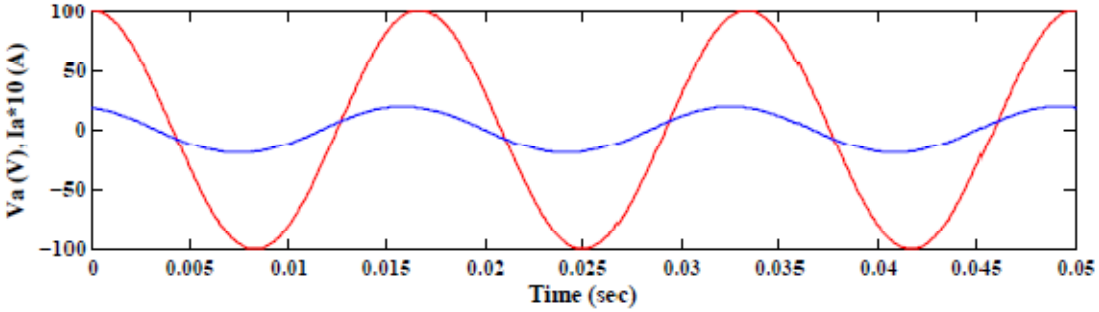
(b) Switched Output Voltage



(c) Three-phase output currents



(d) Grid input voltage and current at UPF



(e) Grid input voltage and current at 18 Deg leading input PF

Fig 3.2 Plots of grid input voltages, switched output voltage, output machine currents and input grid currents.

3.4 Experimental Results

A 5KVA Three-Phase Matrix-Converter-Prototype is realized in hardware which uses a matrix of 18 IGBT switches with a clamp circuit for safe commutation of switches. The control interface is built using a ds1103 dSPACE System which is interfaced with a Xilinx Spartan-3 FPGA board to generate gate signals for IGBT's. Fig. 3.3 shows the block diagram of the experimental setup for testing normal mode operation of MC Drive System. Further details of the prototype are given in Appendix A.

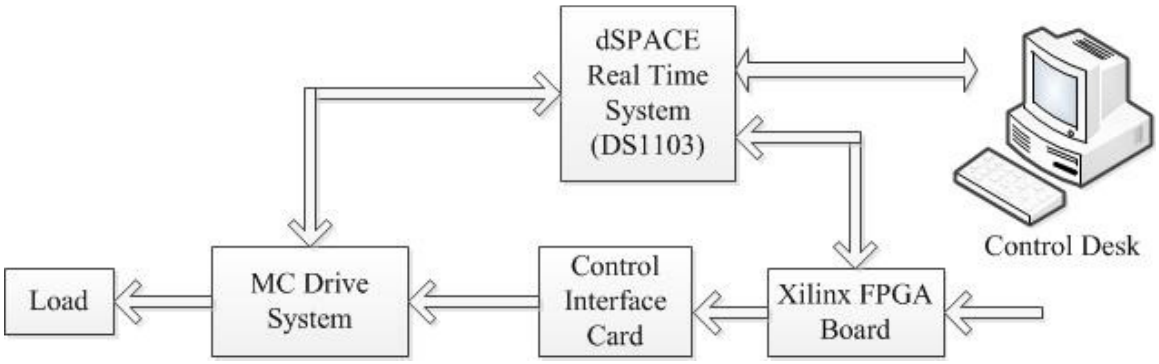


Fig 3.3 Block Diagram of the Experimental Setup.

Fig 3.4 shows the input phase grid voltage (Vin), the input phase grid current (Iin) and the output motor phase current (Iout) waveforms with the motor parameters as listed in Table 3.1. The peak input grid voltage applied is 100V. Fig 3.5 shows the output MC phase voltage (with respect to the input neutral) waveform and the motor phase current waveform which is as expected for the MC system. Fig 3.6-3.7 show the input phase grid voltage, motor phase current and input phase grid current with a leading input power factor and unity power factor respectively. The experimental results are seen to be in agreement with the simulation results.

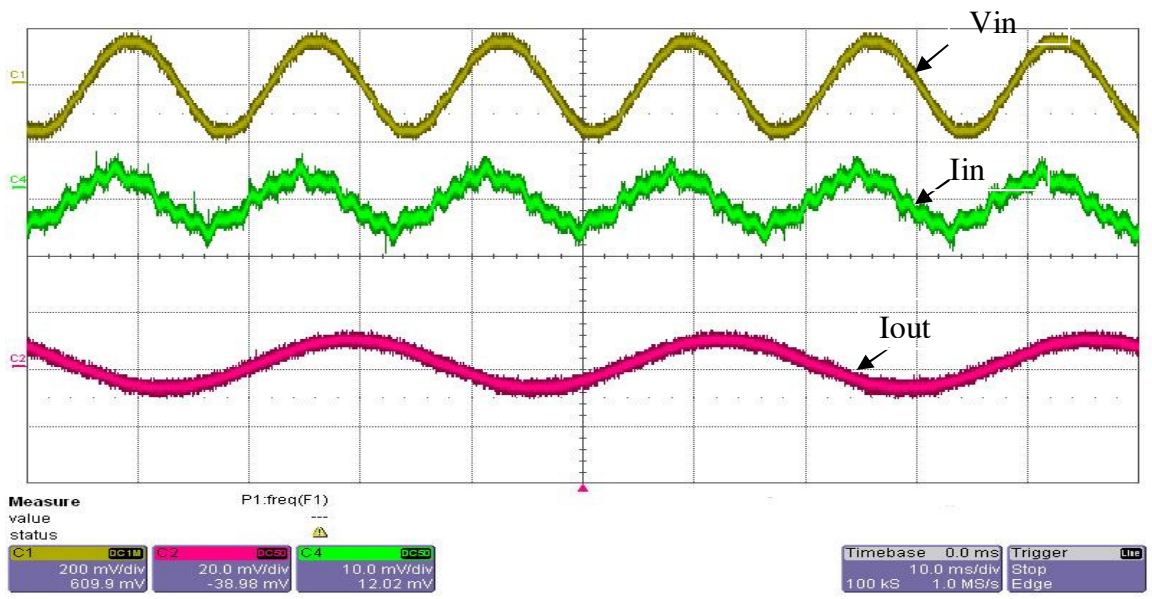


Fig 3.4 Experimental waveforms of the input phase grid voltage (100V/div), input phase grid current (3A/div) and the motor phase current (5A/div).

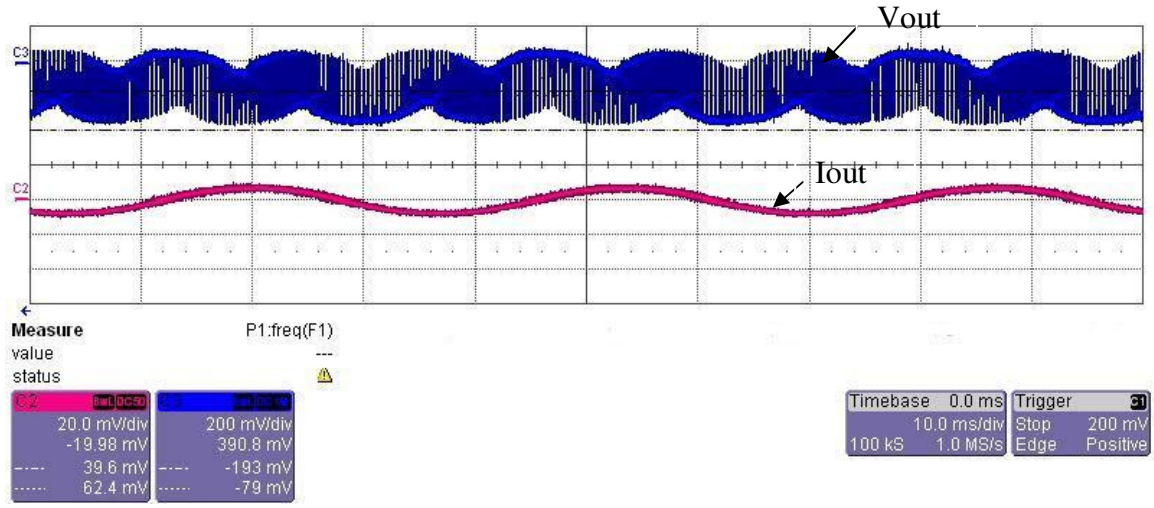


Fig 3.5 Experimental waveforms of the output MC phase voltage [w.r.t. input neutral] (100V/div) and the motor phase current (5A/div).

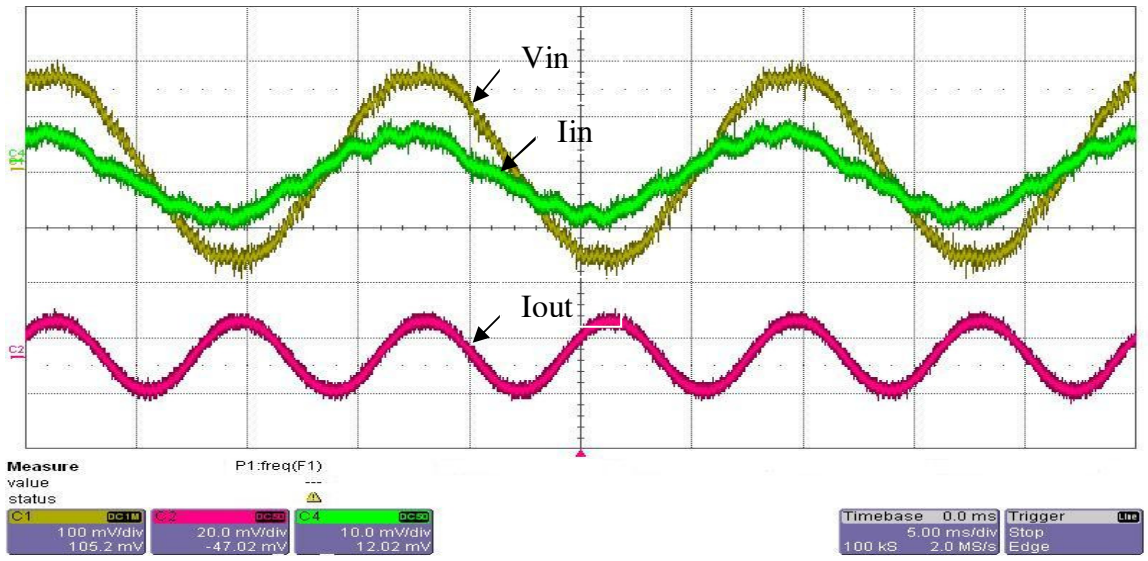


Fig 3.6 Experimental waveforms of the input grid phase voltage (50V/div) and input grid phase current (3A/div) at leading input power factor and the motor phase current (5A/div).

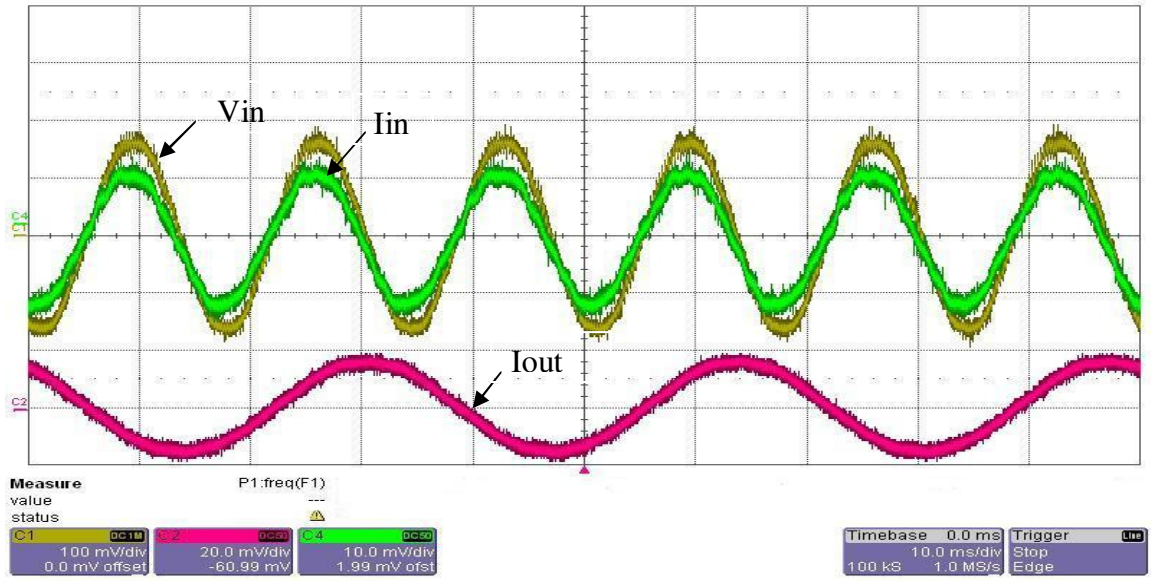


Fig 3.7 Experimental waveforms of the input grid phase voltage (50V/div) and input phase grid current (2A/div) at unity input power factor and the motor phase current (3A/div).

Chapter 4

Ride-Through Strategy for MC fed Induction Drives

This chapter presents the proposed ride-through strategy for MC fed Induction Drives. It first enlists the objectives for the scheme and gives an overall understanding of the scheme in detail. Transient behavior of the induction machine during fault conditions has been mathematically analyzed. The scheme is then verified through simulation of the MC Drive topology and the simulation results compared with the most well known existing scheme for MC ride-through.

4.1 Ride-Through Objectives

4.1.1 For general purpose ASD

- Maintain flux level in machine at the closest possible value to the rated, and keep synchronization between matrix converter and motor, so that recovery time is less with minimum transients.
- Enhance ride through duration.
- Maintain clamp capacitor voltage within limits to supply control circuits.
- Involve minimum hardware modification and hence cost.

4.1.2 For wind power plant

- Maintain current at a desired value and maintain flux level in machine at the closest possible value to the rated, and keep synchronization between

matrix converter and motor, so that recovery time is less with minimum transients.

- Enhance ride through duration to the best possible.
- Maintain clamp capacitor voltage within limits to supply control circuits.
- Eliminate any reactive power supply by the grid during fault thus avoiding further voltage collapse.
- Involve minimum hardware modification and hence cost.

4.2 Proposed Scheme

The main ride-through objective of an MC driven ASD is to maintain current at a desired value and maintain flux in the machine at the closest possible value to the rated. But we are constrained by the drop in grid voltage, due to which we no more have the freedom to give the desired voltage vector at an arbitrary phase and amplitude. The electromagnetic machine dynamics, at any instant, is governed by the available voltage, speed of the rotor and the available flux in the machine. Before ride-through, in normal mode of operation all the quantities balance each other according to the motor model, and maintain certain steady state values. But during ride-through, when voltage at the grid drops by a sag amount, then the balanced steady state is no longer maintained. The system can then show large over-currents, due to low available grid voltages, because the back e.m.f. in the machine is no longer balanced by the available grid side voltage. In order to maintain current level and flux level within limit during ride-through, it is desirable to get additional voltage levels from the clamp circuit. But because clamp circuit allows uncontrolled rectification, therefore the phase and amplitude of voltages applied at the

motor terminals, is no more in our control. This phase and amplitude of the voltage vector will entirely be governed by the phase of the stator current in the machine.

Here we have two options available:

1. All switches of MC are forced to open and machine current is dictated by clamp circuit. Fig 4.1 shows how the clamp circuit voltage will look like with the given machine current per phase.

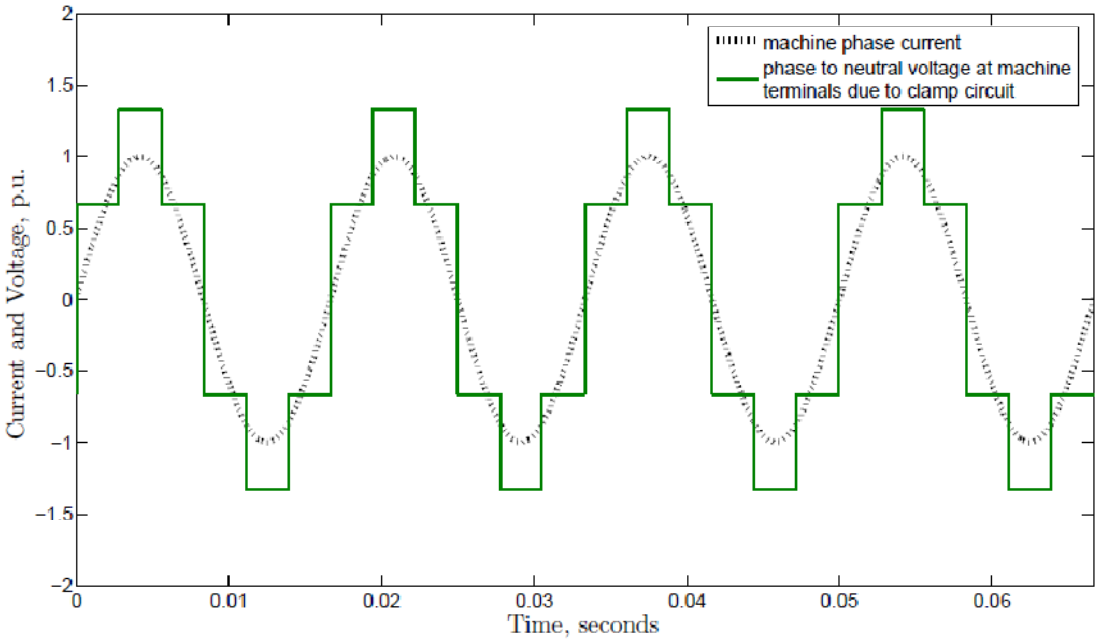


Fig. 4.1: Available Clamp circuit voltage vector according to the machine phase current.

2. In addition to clamp circuit voltage, we should use available grid voltage to control stator flux and stator current to the best possible extent, which has been done in this thesis.Traditionally, switching between the zero vector, which implies short circuiting the motor terminals, and the open state mention in option 1, was used to control the motor currents within a limited range [6].

Unlike the traditional method, our strategy advocates use of the best possible voltages from the grid along with the clamp circuit voltages to control the stator flux and current. During the normal mode, the switching modulation scheme used generates PWM patterns for the matrix converter switches. These then generate the desired voltage at the motor terminals and maintain the continuous operation of the drive. When an input power interruption is detected, the control is transferred from the normal operating mode to the ride-through mode.

During ride-through, the proposed controller uses hysteresis control to maintain the current amplitude from the clamp circuit voltages and voltages available from the grid. To control Imotor in a hysteresis band, as shown in Fig 4.2, we switch between applying the available grid voltage in the flux direction, and the clamp circuit voltage (done by opening all switches). If the resulting motor current vector amplitude goes beyond the desired value, then the voltage vector due to the clamp circuit is applied; and if the motor current vector amplitude is below the desired value, then the available grid side voltage vector is applied.

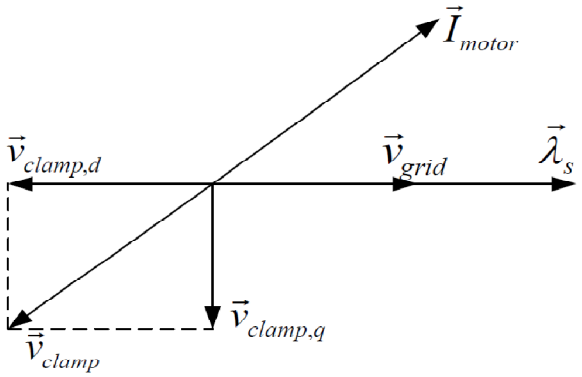


Fig. 4.2 Voltage vectors available from grid and clamp circuit during ride-through mode.

In other words, the ride-through mode operation involves two switching states:

1. Open state, illustrated in Fig 4.3a, where the matrix converter switches are opened, causing the clamp circuit to be connected to the motor. With the clamp circuit voltage higher than the motor back e.m.f., the stator currents would tend to decay.

2. Active voltage vector state, illustrated in Fig 4.3a, where some active voltage is still available to be applied to the motor terminals in a direction which is aligned to the direction of the stator flux, as shown in Fig 4.4 thus minimizing stator flux decay.

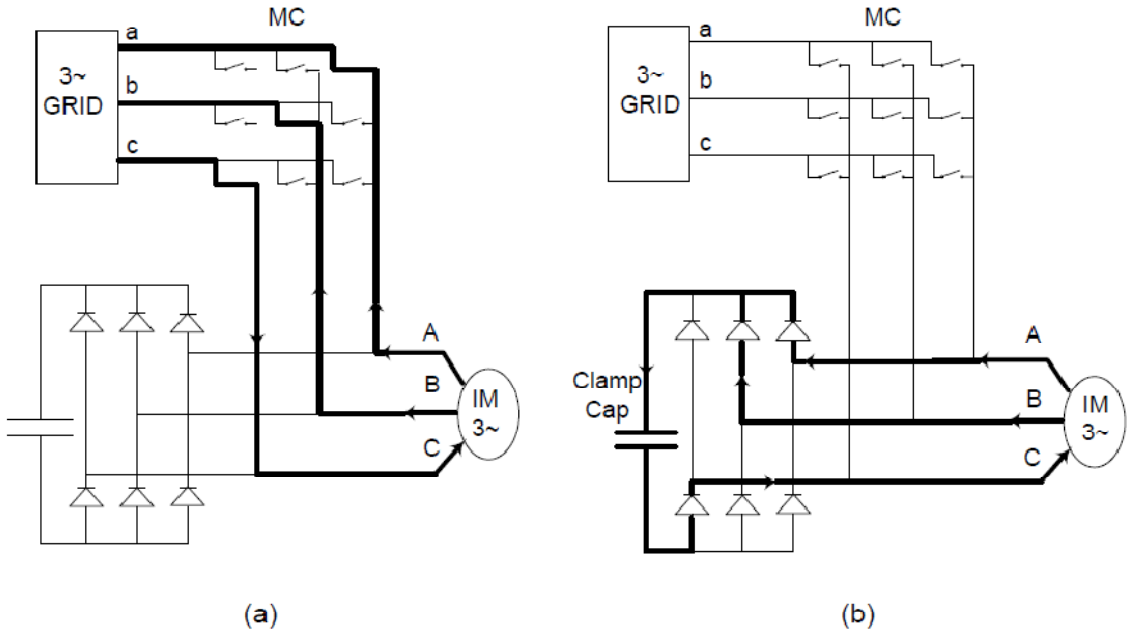


Fig 4.3 Ride-Through Switching States (a) Active Vector Switch State (b) Open Switch State.

By allowing the matrix converter to switch between these two states in the ride-through operation, the stator flux decay is minimized, and hence the ride-through time period is enhanced. Here I have assumed the maximum ride-through time period to be the time when the fault occurs, till the time in which flux decays to 0.1 p.u. or the speed decays to

0.1 p.u.(depending on whichever decays first) Thus limited ride-through capability is achieved by employing the above strategy which works like a boost operation Fig 4.5

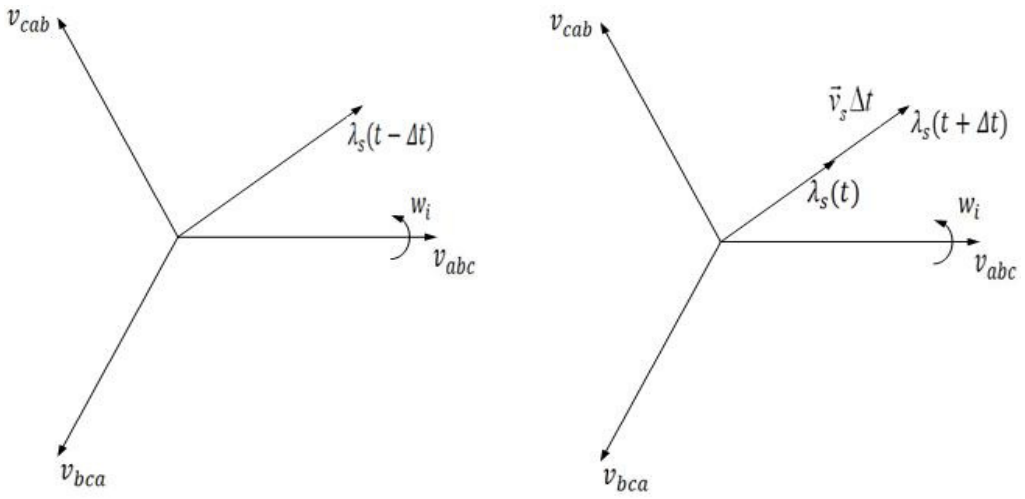


Fig 4.4 Stator flux compensation by voltage vector alignment in ride-through mode. (Flux amplitudes are exaggerated for illustration purposes.)

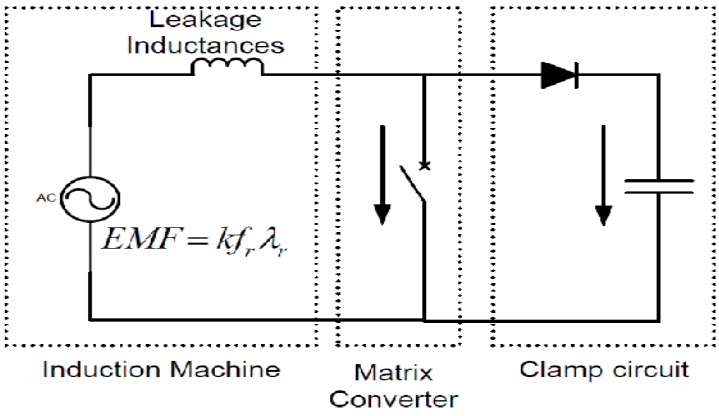


Fig 4.5 Boost operation MC Drive system in ride-through mode.

Another hysteresis block is used to control the flux amplitude in the machine to prevent it from exceeding its rated value; it becomes active only when the flux amplitude tries to exceed its rated value. This flux magnitude determines whether zero vector or the voltage

vector along the flux direction, operated at the maximum modulation range from the MC should be applied.

Fig 4.6 shows the average available grid voltage and clamp circuit voltage during ride-through. The voltage needed by the machine during this time is Vmotor (back emf) which cannot be supplied by grid voltage alone, as can be seen, and hence clamp circuit voltage will also be applied alternately. (Here, we should remember that since clamp voltage vector position cannot be controlled instead is determined by current vector direction, so in some positions it will fail to add additional voltage level at the motor terminals.)

The closer the V_{motor} to the clamp circuit voltage, the more the contribution of clamp circuit vector on an average over a cycle. With decrease in speed, as back e.m.f.

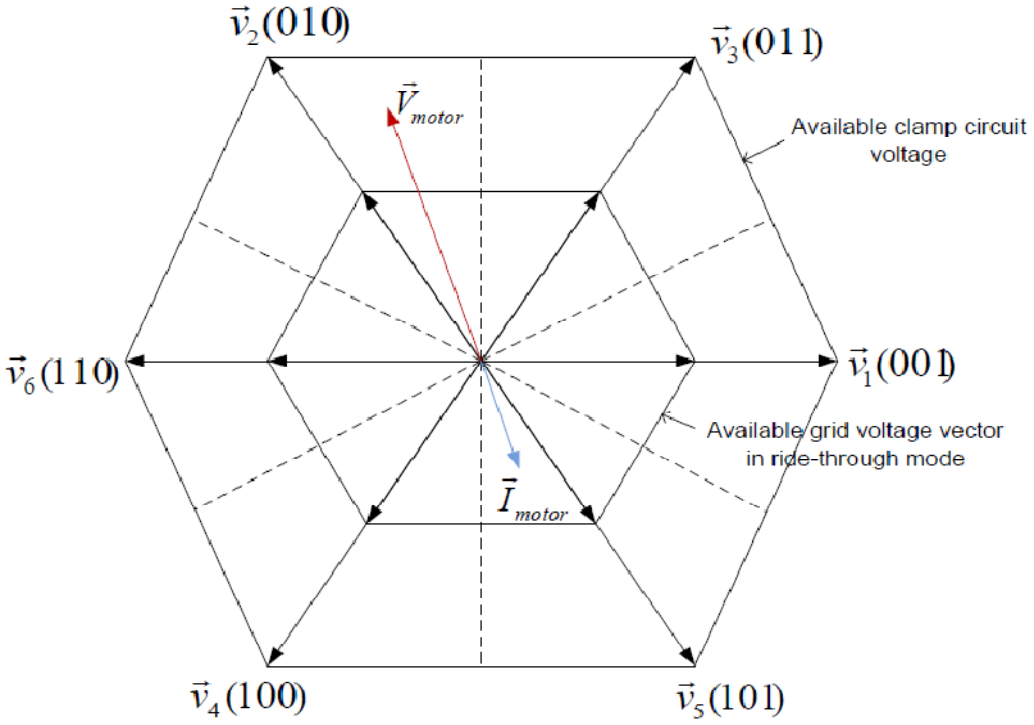


Fig 4.6 Voltage vector selection during ride-through mode depending on the back e.m.f. of the motor.

decreases, voltage needed by the machine decreases. This means that V_{motor} is closer to the grid voltage vector envelope than the clamp circuit voltage vector envelope. Consequently, more grid voltage in the flux direction would be applied than the clamp circuit voltage during low speed. Thus flux may tend to increase during low speed operation of the machine during ride-through.

4.3 Simulation Results

The proposed ride-through strategy was simulated and tested in MATLAB/Simulink. Using the Induction Motor dynamic equations, the motor model was created with the specifications given in Table 2.1. This motor drive system was vector controlled and the initial conditions were calculated from the applied phasor voltages using phasor analysis and the dq equations. The MC and the Clamp circuit were modeled using SimPowerSystem® Toolbox. The whole integrated system has been illustrated as a block diagram in Fig 4.7.

During normal mode operation, the input grid supplies voltages switched by the MC to get the desired output voltages and currents at the motor terminals. The clamp circuit operates only during the dead time (if any) during this mode. The desired control voltages feed the appropriate modulation index to the MC during this time. When suddenly the voltage at the input grid drops below its nominal voltage, sag detect flag gets enabled and the system now starts operating in ride-through mode. During ride-through mode, as explained in the previous section, vector control is no longer into action. Hysteresis control is now used to sustain flux in the machine, and keep it online during the STPI

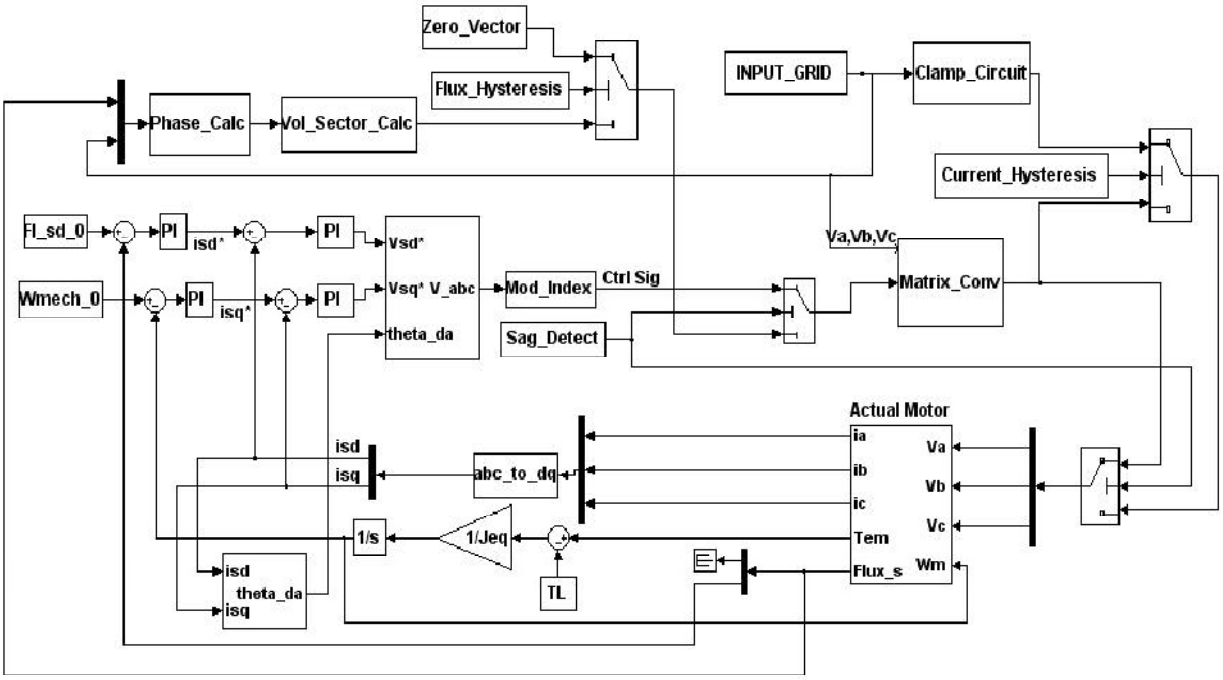


Fig 4.7 Block Diagram for the Simulated Matrix Converter Drive System with Ride-Through Strategy.

period. The stator flux position is estimated, and with the idea of applying voltages in the direction of flux, the voltage sector is determined. Using this information, the MC voltage vector is then appropriately switched to apply the active voltage vector that is available from the grid. The hysteretic current controller and the flux controller together manage to sustain the current and hence the flux in the machine. The alternate switching between the two ride-through states continues during the fault period, till mechanical energy is present in the system, beyond which the stator flux can no longer be sustained. Thus ride-through duration is limited by the system inertia. This control sequence flow is presented in Fig. 4.8 as a flowchart for ease of understanding.

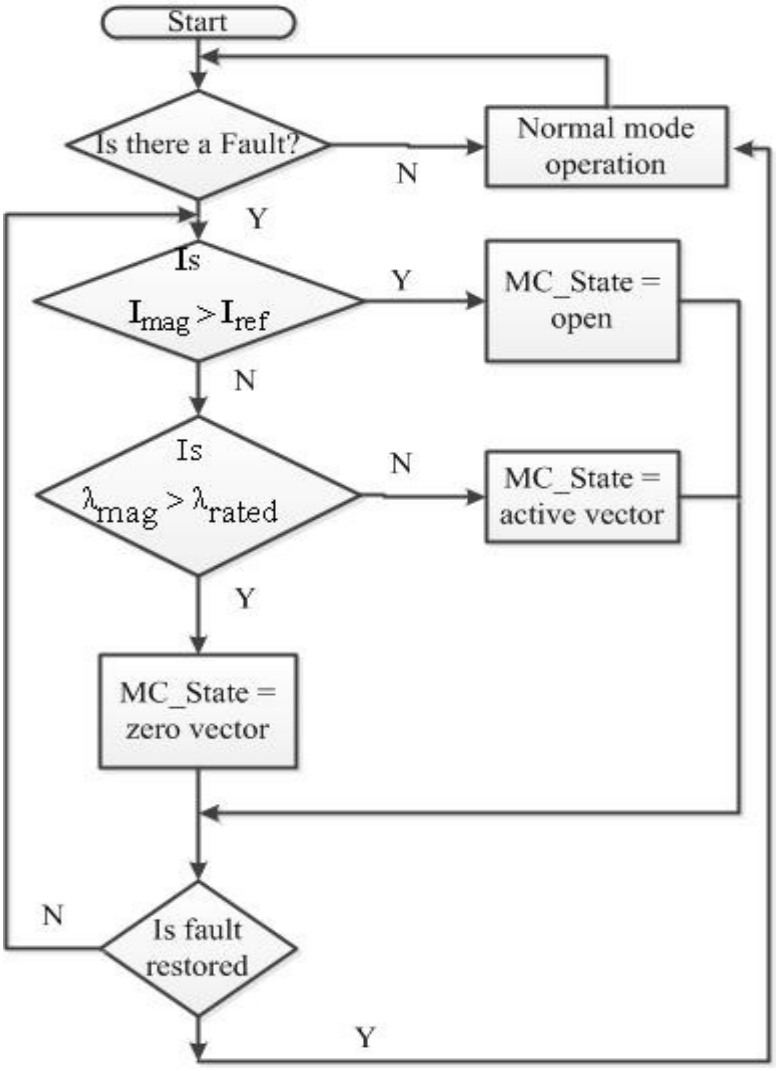


Fig 4.8 Proposed ride-through control flow.

The steady state waveforms of the matrix converter drive in normal mode of operation is shown in Fig 4.9. It shows the input and output side characteristic waveforms when the input grid is normally supplying power to the drive. The available input grid voltages are shown to be around 260V peak. The motor currents and stator flux are seen to be sinusoidally varying with a peak of around 36A and 0.53 Wb-t respectively. The next set of waveforms in Fig 4.10 show the transient response, when the input voltage at the grid

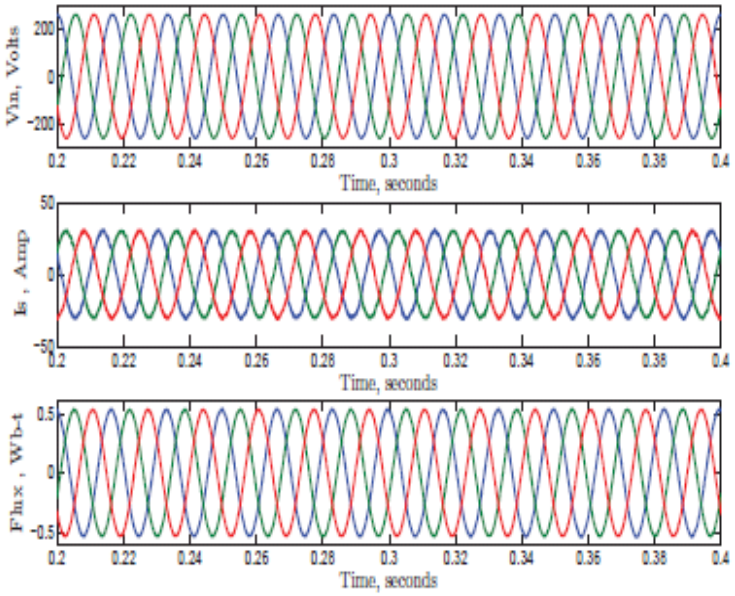


Fig 4.9 Simulation results in normal mode (a) Input Grid Voltage vs. Time (b) Motor currents vs. Time (c) Stator Flux Linkage vs. Time.

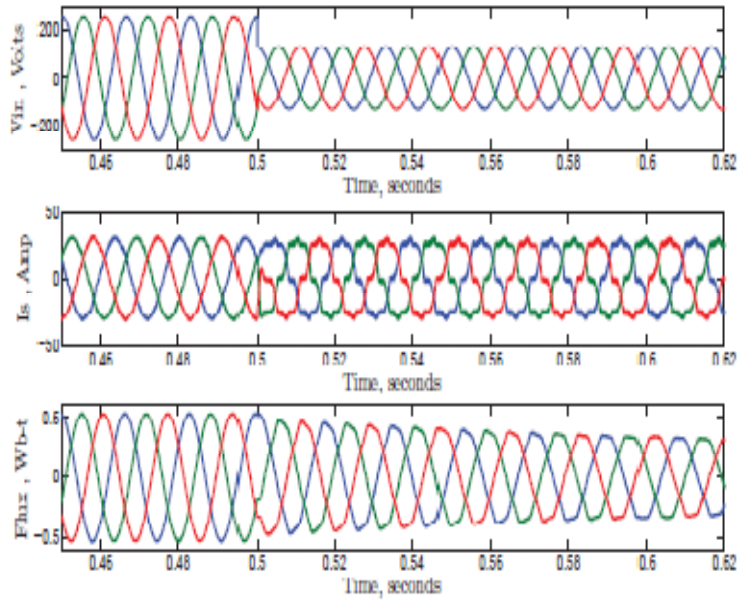


Fig 4.10 Simulation results during transition to ride-through mode (a) Input Grid Voltage vs Time (b) Motor currents vs Time (c)Stator Flux Linkage vs Time.

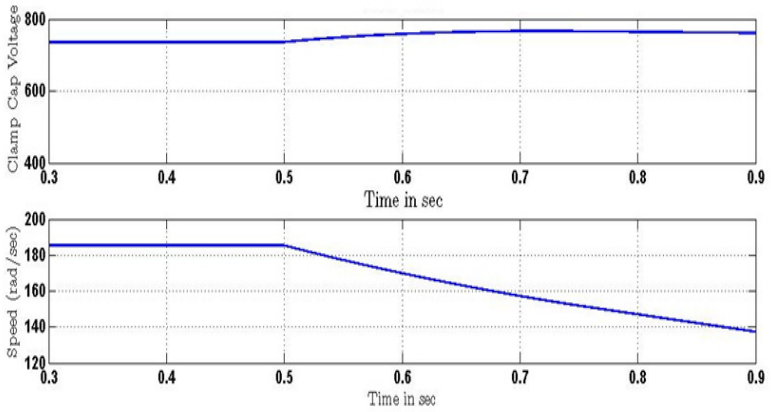


Fig 4.11 During transition to ride-through mode (a) Clamp capacitor voltage vs. Time (b) Motor Speed vs. Time.

suddenly falls down to 50% of its nominal voltage. Waveforms depicted are the voltages, motor currents, and the stator flux .The stator currents and stator flux do not see any overshoots in their response. The currents can be seen to be maintained around the reference rated current magnitude set by the hysteresis controller. The stator flux waveform gradually decreases immediately after the under-voltage fault appears. The clamp capacitor voltage is also seen to be almost maintained as the speed decelerates during ride-through in Fig 4.11. In this case, after the flux has risen to its rated value during ride-through time, the system is recovered. Fig 4.12 show the system recovery instant when the fault is cleared and the voltage at the grid appears suddenly. The current and flux waveforms are seen to come back to their initial operating conditions with minimum transient. Fig 4.13 shows the motor current and flux waveforms for the entire duration of the normal mode operation, transition to ride-through mode, ride-through mode operation and power recovery transition back to normal mode. The flux waveform

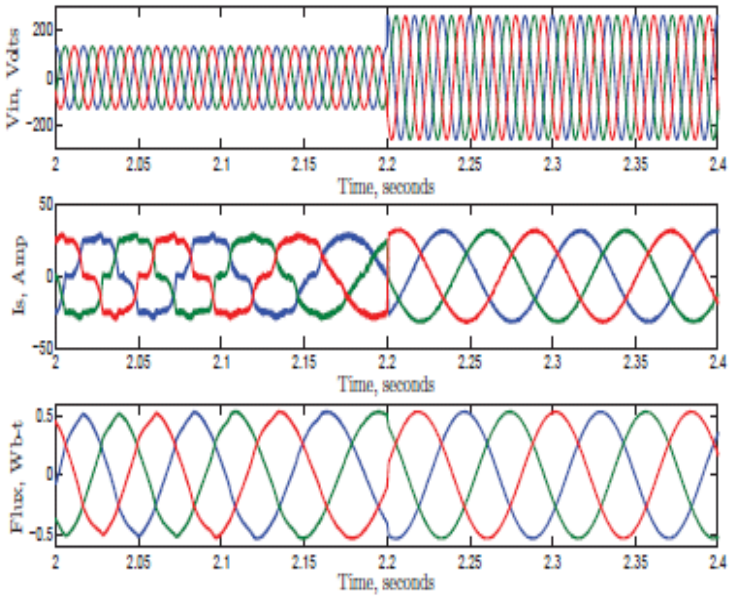


Fig 4.12 Simulation results during system recovery at rated flux (a) Input Grid Voltage vs. Time (b) Motor currents vs. Time (c) Stator Flux Linkage vs. Time.

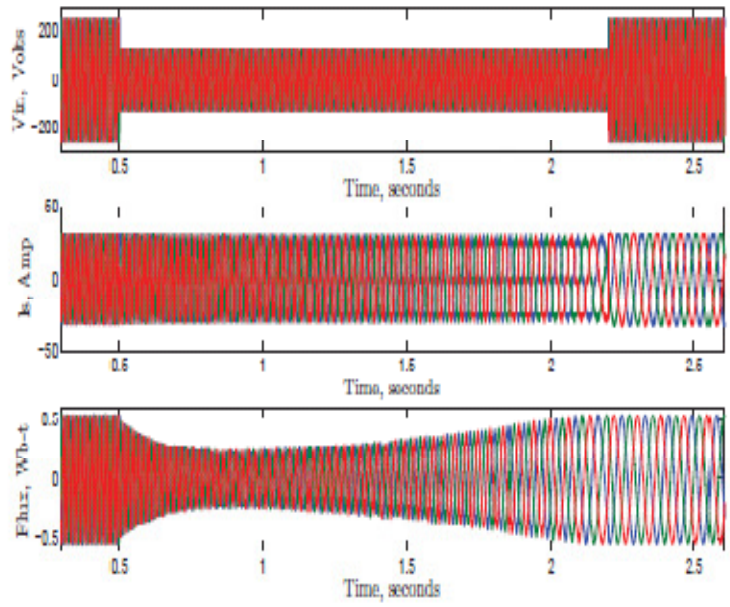


Fig 4.13 Simulation results during ride-through mode (a) Input Grid Voltage vs. Time (b) Motor currents vs. Time (c) Stator Flux Linkage vs. Time.

show how the flux values decrease, and try to sustain at a certain level during the ride-through. But because of the low speeds, its value starts increasing, due to increased stator voltages applied at the motor terminals. Finally the flux reaches the rated value and is sustained at that level, till the entire ride-through duration, which is limited by the system inertia.

These waveforms help investigate the feasibility of applying this strategy to ride through voltage sags of long duration and reduced voltage levels.

4.4 Analysis of Machine Dynamics during Ride-Through

The stator voltage equation in space vector form is given in (1). $\vec{V}_s$ is stator input voltage vector. $\vec{\lambda}_s$ and $\vec{i}_s$ are stator flux-linkage and current vectors respectively. Here the analysis is done in a d – q co-ordinate frame. This frame is oriented along $\vec{\lambda}_s$ (λ_{sq} is zero). If we neglect the stator resistance drop (4.1) results in (4.2) and (4.3). The subscripts s, r, d, and q refers to stator, rotor, d-axis and q-axis respectively. ω_d is the speed of the stator flux-linkage vector. (4.4) provides the flux linkage equation in this frame. L_m refers to the magnetizing inductance. $L_s = L_m + L_{ls}$ and $L_r = L_m + L_{lr}$. L_{ls} and L_{lr} are the stator and rotor leakage inductances. From (4) assuming $L_{ls}, L_{lr} << L_m$ we get (5). (4) also results in (4.6), where $\overline{\sigma} = (\frac{L_s L_r}{L_m^2} - 1)$.

$$\vec{V}_s = R_s \vec{i}_s + \frac{d}{dt}\vec{\lambda}_s \qquad (4.1)$$

$$v_{sd} \approx \frac{d}{dt}\lambda_{sd} \tag{4.2}$$

$$v_{sq} \approx \omega_d \lambda_{sd} \tag{4.3}$$

$$\begin{pmatrix} \lambda_{sd} \\ 0 \\ \lambda_{rd} \\ \lambda_{rq} \end{pmatrix} = \begin{pmatrix} L_s & 0 & L_m & 0 \\ 0 & L_s & 0 & L_m \\ L_m & 0 & L_r & 0 \\ 0 & L_m & 0 & L_r \end{pmatrix} \begin{pmatrix} i_{sd} \\ i_{sq} \\ i_{rd} \\ i_{rq} \end{pmatrix} \tag{4.4}$$

$$i_{sq} \approx -i_{rq} \tag{4.5}$$

$$\lambda_{rq} = -\bar{\sigma} L_m i_{sq} \tag{4.6}$$

The rotor voltage equations in this frame are given in (4.7) and (4.8). ω_m is the mechanical speed of the rotor. Here for simplicity we have assumed a two pole machine. Using equations (4.2) to (4.6) and assuming $\bar{\sigma}$ to be approximately zero, for short intervals of time (small compared to $\frac{\bar{\sigma} L_m}{R_r}$ or rotor leakage impedance time constant) (4.7) and (4.8) result in (4.9) and (4.10). $\tilde{i}_{sq}$ represents the variation in i_{sq}. (4.11) and (4.12) gives an expression for torque and the mechanical equation of the machine respectively. In this analysis, for short intervals of time during ride-through, as the inertia as quite high J, ω_m is assumed to be constant.

$$R_r i_{rd} - (\omega_d - \omega_m)\lambda_{rq} + \frac{d}{dt}\lambda_{rd} = 0 \tag{4.7}$$

$$R_r i_{rq} + (\omega_d - \omega_m)\lambda_{rd} + \frac{d}{dt}\lambda_{rq} = 0 \tag{4.8}$$

$$\bar{\sigma} L_m \frac{d}{dt} i_{sd} \approx v_{sd} \tag{4.9}$$

$$\bar{\sigma} L_m \frac{d}{dt} i_{sq} \approx v_{sq} - \omega_m \lambda_{sd} \tag{4.10}$$

$$T_e = \lambda_{sd} i_{sq} \tag{4.11}$$

$$J \frac{d}{dt} \omega_m = T_e - T_L \tag{4.12}$$

Looking at the mechanical equation of the machine and (4.12), there are four conditions which can exist:

1. $T_e = T_L$ which means the machine is in steady state and there is no decay of ω
2. $T_e > 0$ (but $< T_L$) which means ω would decay slowly. In other words, some small power is being supplied to the machine to keep the machine magnetized.
3. $T_e = 0$ which means because of T_L, ω would decay faster than the previous condition. In other words, since $i_{sq} = 0$, no power is being given to machine nor extracted from machine implying that the machine is completely isolated from the grid.
4. $T_e < 0$ which means ω would decay the fastest because of the combined effect of T_e and T_L. In other words, power is being extracted from the machine.

If we have a voltage dip at the input terminals, one way is to keep the machine isolated from the grid. In other words by keeping $T_e = 0$, and then by using $J \frac{d\omega}{dt} = T_L$ we can find out the maximum ride-through time for the machine for which $\omega > 0$.

But then we have the control electronics which is being fed power from the clamp capacitor to be kept alive during the fault. Hence we try to feed this capacitor with the

requisite load current from the machine. This means that during the ride-through time the machine kinetic energy is being recovered to maintain the voltage of the clamp capacitor and extend logic ride-through. That is, it generates power and feeds i_{sq} current to the capacitor to charge it and compensate for its discharge value due to control electronics. Thus now with $T_e < 0$, ω tends to decay faster but at the same time during active vector state we are giving a minimal power to the machine to keep the motor magnetized. Hence ride-through duration during the voltage sag would now depend on both speed and flux and also the severity of the sag.

4.4.1 Ride-Through Active vector Mode

During the voltage sag condition, the matrix converter is modulated to generate a voltage vector along the direction of $\vec{\lambda}_s$ (4.13). This results in linear increase in stator flux and d-axis component of the stator current (4.14). The stator flux-linkage vector stops rotating i.e. $\omega_d \approx 0$. Minimal power is transferred from the input source to charge the magnetizing current or to maintain the machine flux during ride-through.

$$v_{sd} = V_d^M$$

$$v_{sq} = 0 \tag{4.13}$$

$$\tilde{\lambda}_{sd}(t) = V_d^M t$$

$$\tilde{i}_{sd}(t) = \frac{V_d^M t}{\bar{\sigma} L_m} \tag{4.14}$$

4.4.2 Ride-Through Clamp Circuit Mode

In this mode a three phase diode bridge is connected to the input of the machine. The applied voltage can't be controlled and depends on the magnitude and direction of the input current space vector, but in any case it results in applying a set of voltage to the stator as given in (4.15). This results in a decrease in stator flux linkage, (4.16). This is how the stator flux is maintained. By (4.10) assuming ω_m does not change appreciably during this time we get (4.17). In this interval i_{sq} is negative so the electromagnetically generated torque T_e is also negative. A part of the mechanical energy stored in the rotor inertia is transferred to clamp circuit through the electrical machine. This helps to maintain the clamp capacitor voltage during ride through period so that the control electronics could remain alive and a proper acceleration of the machine to its rated speed is possible in a minimum amount of time without any current transient once the power comes back.

$$\begin{aligned} v_{sd} &= -V_d^R \\ v_{sq} &= -V_q^R \end{aligned} \tag{4.15}$$

$$\tilde{\lambda}_{sd}(t) = -V_d^R t$$

$$\tilde{i}_{sd}(t) = -\frac{V_d^R t}{\bar{\sigma} L_m} \tag{4.16}$$

$$\tilde{i}_{sq}(t) = -\left(\frac{V_q^R + \omega_m \lambda_{sd}}{\bar{\sigma} L_m} \right) t \tag{4.17}$$

4.5 Parametric Evaluation of Ride-Through of MC fed Drives

The major parameters that affect the ride through time are the initial motor flux, the leakage inductances, the rotor time constant (rotor resistance and inductance), the inertia, the load torque and the magnetizing inductances. Since we have used a current controller in our ride-through strategy, the hysteresis band is also a parameter that might affect the motor current ripple and has been investigated too, along with the other parameters as mentioned above [63].

4.5.1 Parametric Analysis

During ride-through mode, if there is no applied voltage to overcome the back e.m.f. of the motor and sustain the current, then that would lead to decay of magnetizing current due to opposing voltage acting upon it, coupled with the voltage drop across the stator resistance. Following this decaying current, the rotor flux decays and its decay time constant would determine the ride-through time period of the vector controlled induction motor drive.

To show the dependence of λ_{rd} on i_{sd} , we have

$$\lambda_{rd} = L_r i_{rd} + L_m i_{sd} \tag{4.18}$$

Substituting for i_{rd} and using τ_r (L_r/R_r), the rotor flux-linkage dynamics expressed in time-domain is as follows:

$$\frac{d}{dt}\lambda_{rd} + \frac{\lambda_{rd}}{\tau_r} = \frac{L_m}{\tau_r} i_{sd} \tag{4.19}$$

Also under vector control in steady state, the torque expression showing a dependence on the q-axis current is as follows:

$$T_e = k i_{sq} \tag{4.20}$$

where $k = \frac{p}{2}\frac{L_m^2}{L_r} i_{sd}^*$

The value for inductances with stator currents determine the magnetizing energy and the motor rotating inertia at a speed determines the kinetic energy in the motor. These together comprise the energy going to the clamp capacitor, a part of which is dissipated in the clamp circuit equivalent resistor. The decay time of the rotor flux (λ_{rd}) depends on the inductance along with the rotor time constant, and the current excitation, i_{sd}. The load torque electro-mechanical equation which depends on the q-axis current, as shown in the equation above, is as follows:

$$P = \frac{dW}{dt} = (T_e - T_L)\omega_m \tag{4.21}$$

When the motor has a higher load torque, its speed will tend to decrease faster compared to the motor with smaller load torque. For smaller load torques, power opposing the rotation would be smaller, hence the motor speed coasts down at a slower rate and thus the motor can continue running for a longer ride-through time. Considering the rotor time-constant parameter τ_r, an increase in the rotor resistance would lead to a corresponding decrease in the rotor time constant. With τ_r decreasing, the rate of decay of rotor flux increases (refer to the rotor-flux linkage dynamic eq. above) and hence the ride-through duration decreases as the rotor flux drops rapidly. The magnetizing inductance and consequently the magnetizing current values also affect the rotor flux. Energy equation during ride-through duration can be written as below:

$$Pt_{rt} = \frac{1}{2} C_{clamp} (V_{final}^2 - V_{initial}^2) + I_{clamp}^2 Rt_{rt}$$

$$= \Delta W_{motor} \text{ where } \Delta W_{motor} = \Delta W_{inertial} + \Delta W_{mag}$$

$$\Delta W_{inertial} = \frac{1}{2} J \omega_m^2$$

$$\Delta W_{mag} = \text{Energy stored in the winding inductances}$$

Ptrt is the energy going into the clamp capacitor circuit during ride-through and R is the load on the clamp capacitor.

For all the parameters mentioned above, it is difficult to decouple the non-linear equations and derive a dependence on ride-through for each parameter separately. That would involve a lot of mathematical derivations and analysis. To avoid that, we could do a simulated analysis for each parameter and then observe each individual parametric trend of dependence on ride-through time and behavior.

Another important parameter, which has not yet been discussed, is the hysteresis band width of the current controller which determines the ride-through profile, although it does not significantly affect the ride-through duration. Because the two ride-through switching states are chosen according to the motor current magnitude, the ripple frequency is not constant and depends highly on the following parameters: the reference current limit chosen to change the switching state, the clamp circuit voltage and the stator time constant (L_s/R_s). The current ripple can be influenced by the choice of current hysteresis controller; in this analysis, an ideal bi-positional controller (also known as "bang bang controller"), is used for the simulations due to a lower frequency of ripple,

though the magnitude is slightly higher. Also the band width selected for the hysteresis controller directly affects the magnitude of current ripple. A narrow band width would mean a lower ripple in the motor current though at the cost of an increased ripple frequency. Thus smoother ride-through profiles could be achieved through appropriate selection of hysteresis band.

4.5.2 Simulation Results

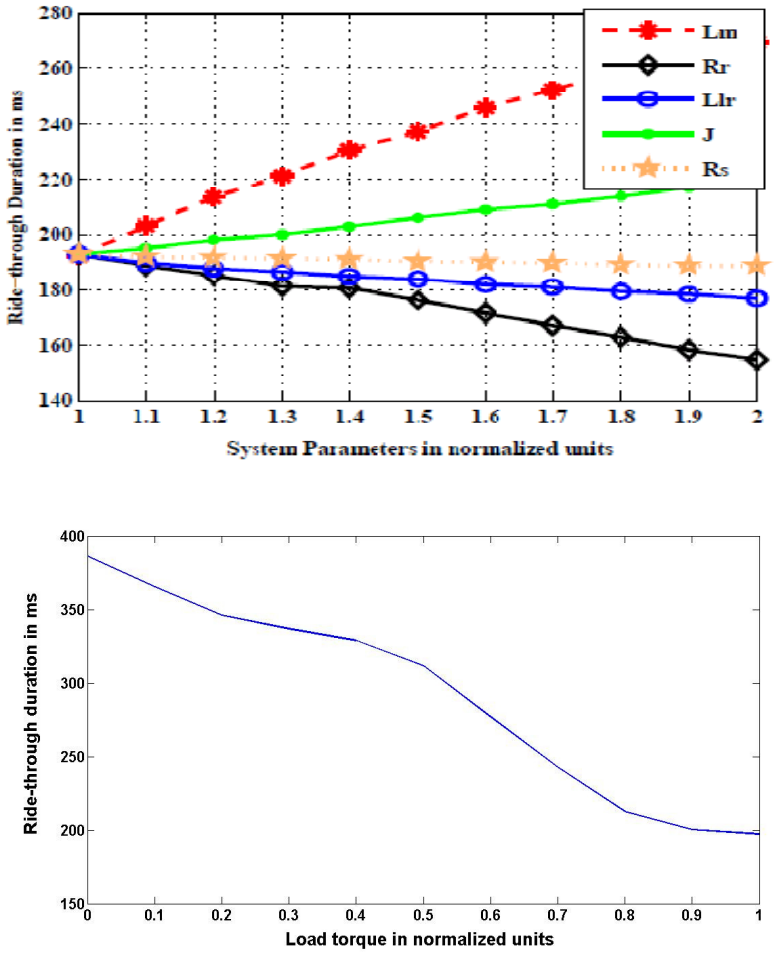


Fig. 4.14 Parametric Plot with ride-through strategy applied (a) Ride-through duration vs. system parameters like L_m(red), R_r(black), R_s(orange), L_{lr}(blue), J(green) (b) Ride-Through duration vs. Load torque.

Once the main simulation was done and the currents and voltages plotted, each of the parameters mentioned in the previous section was taken and varied in a range keeping the others fixed. For each combination of values, the ride-through duration was measured and then the normalized graphs were plotted and analyzed, as shown in Fig 4.14.

After studying the graphs, it can be observed that the most variation in the ride-through duration is due to the magnetizing inductance, rotor resistance and the load torque with the magnitude of current ripple depending on the hysteresis band width. Keeping the speed relatively constant, the magnetizing current was varied via changing magnetizing inductance values and its effect on ride-through duration was observed. The change in inertia does not always affect the ride-through time period because in some cases, by the time speed can show any significant effect, rotor flux has decayed to zero. All the other parameters do not significantly affect the ride-through duration for the matrix converter drive system.

As was expected (explained in the previous section) due to decrease in the load torque , a corresponding significant increase in the ride-through duration is observed. With increasing values of magnetizing inductance, ride-through duration is extended as now the windings can store more magnetic energy and hence can sustain the motor current for a longer time. With changes in rotor resistance, rotor time constant changes, and hence the decay time of the rotor flux is significantly affected, affecting the ride-through duration. Among the most significantly affecting parameters, only load torque and hysteresis band are the ones we have active control on, because the motor parameters are mostly given to us and can only change within experimental variations. With control over

load torque acting on the motor drive system, we can extend the ride-through duration to almost double. By narrowing the band width used for the hysteresis controller that acts as the switch state selector, we can smoothen our ride-through profile due to lowering of the magnitude of motor current ripple. Choice of hysteresis band does not much affect the ride-through duration , as can be seen through the graph ,Fig 4.15 (a).

Hence for designing the minimum clamp capacitance, we can choose to lower the torque (q axis current) to get the maximum value of ride-through duration $(t_{rt} = t_{activevecstate} + t_{clampvecstate})$ and then use the energy equation below to calculate the corresponding clamp capacitance:

$$C_{clamp} = \frac{2\Delta W_{motor}}{(V_{final}^2 - V_{initial}^2) + I_{clamp}^2 R t_{rt}} \tag{4.22}$$

The current ripple can be reduced by taking the narrowest band width, as shown in Fig.4.15 (b), but the narrower the band width the higher would be the ripple frequency.

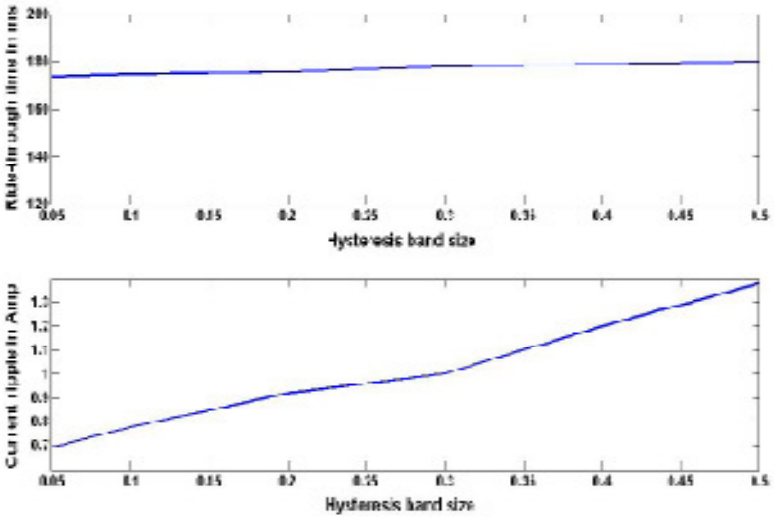


Fig. 4.15 Parametric Plot with ride-through strategy (a) Ride-Through duration vs. Hysteresis band width (b) Current ripple vs. Hysteresis band width.

4.5 Comparison with Existing Scheme

The proposed strategy has the following advantages:

1. It maintains stator flux magnitude longer and keeps the matrix converter synchronized to the motor.

2. It avoids significant over currents in the motor.

3. It involves no hardware modification apart from the clamp circuit which in either case, is used with matrix converters for preventing voltage spikes during commutation errors.

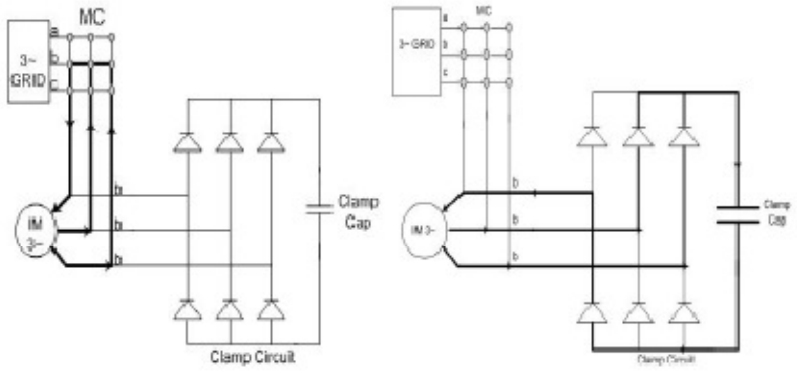
4. It enhances the ride-through duration considerably during the power interruption even for voltage levels as low as 15%.

There are two other ride-through strategies in literature proposed in [64] and [65], which do not use any additional external hardware to achieve ride-through.

1. The first ride-through strategy developed for MC uses an approach similar to the one for conventional back-to-back drives. During an under-voltage fault, the system is forced into the ride-through mode, which permits two switching states in that mode.

- The Zero-vector switching which allows connection of all motor phases to the same input grid phase, as illustrated in Fig 4.16(a). Due to the short circuit of the motor terminals, the stator currents are forced to increase, thereby increasing the magnetic energy in the leakage inductances.
- The Open state where all the matrix converter switches are switched off disconnecting the motor from the grid, as shown in Fig 4.16(b). The interrupted motor currents thus flow through the clamp circuit keeping the capacitor level constant as long as the motor flux does not decay to very low values.

The switching between the two states is controlled by the motor current vector magnitude



(a) (b)

Fig 4.16 Ride-Through Switching states (a) Zero vector state (b) Disconnected state.

Compared to the proposed strategy, the disadvantage of this above scheme is that since the input grid is separated from the motor terminal, the ride-through duration would be the same for all voltage sag percentages (Fig 4.17) as opposed to the new scheme where ride-through durations would differ depending on the sag severity, as depicted by Fig 4.18

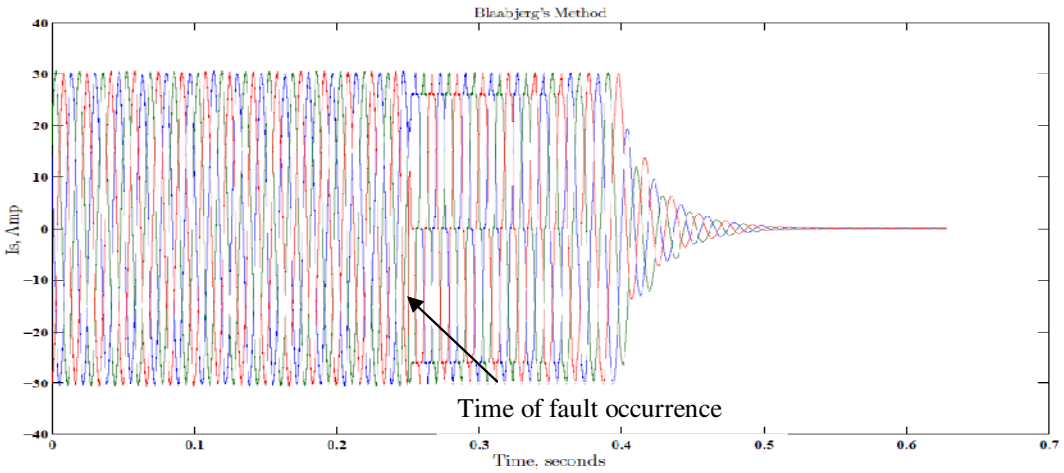


Fig 4.17 Scheme proposed in [45]: Motor current during normal mode and during any percentage voltage sag.

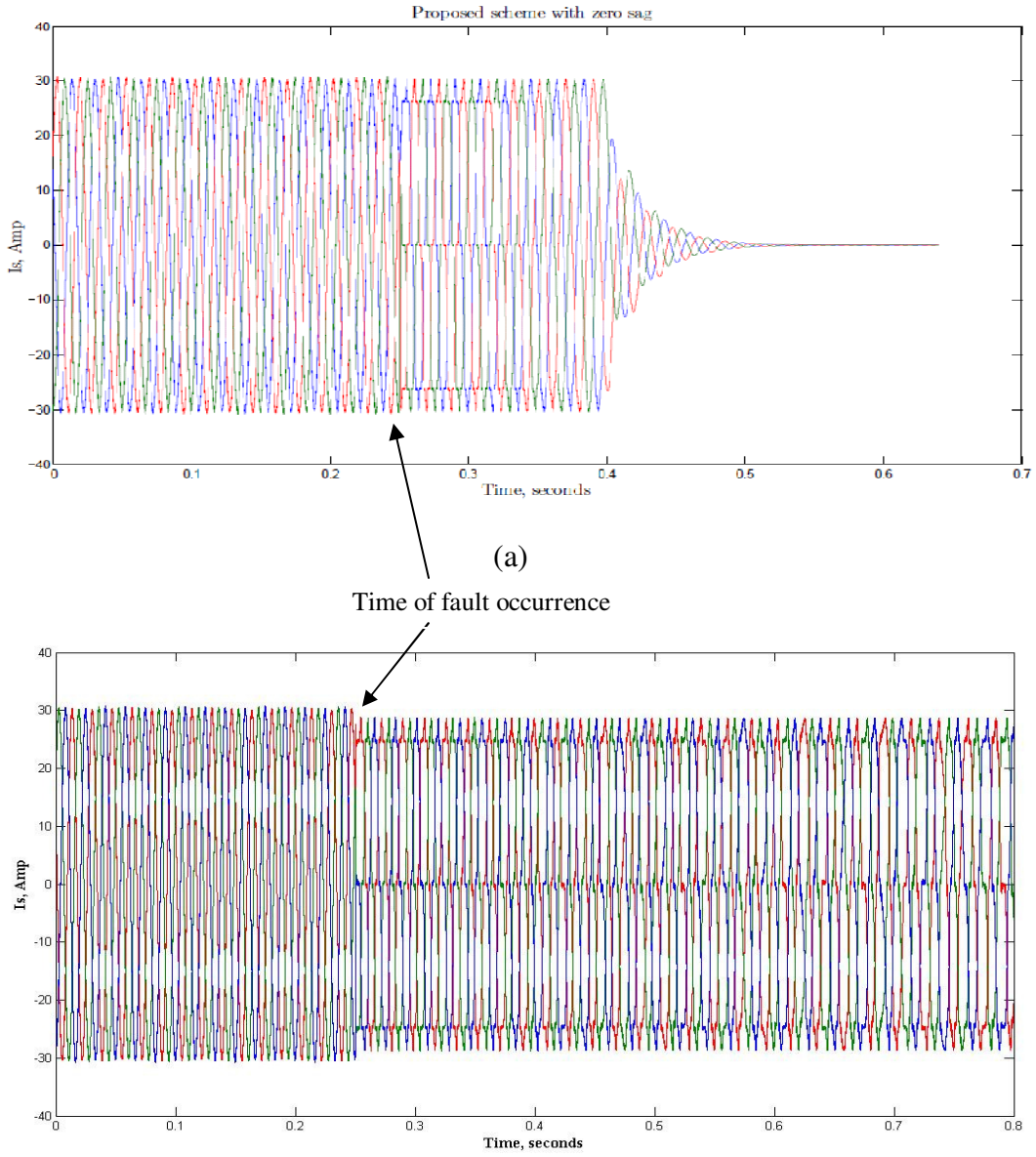


Fig 4.18 Proposed Scheme: Motor current during normal mode and during (a) zero voltage sag (b) 50 percent sag.

2. The next proposed ride-through strategy for MC fed ASD's [46] involved enforcing constant volts/hertz operation through voltage sags with a minimum motor speed reduction. To maintain constant V/f operation, first the modulation index of the MC was

regulated which would counteract the dip in source voltage and secondly, the speed reference was lowered if required.

Compared to the proposed strategy, this strategy does not aim at maintaining the clamp capacitor voltage. It tries to keep the motor continuously running in the motoring mode even during fault. For the proposed strategy, if maintaining the clamp capacitor voltage requirement is absent, then after the speed decelerates to a point where the back emf would balance the residual voltage at the machine terminals during sag condition, the machine could be brought back into motoring mode and continue to operate indefinitely at that quasi-state condition, till the voltage is restored. This would be similar to the above mentioned strategy which lowers the speed reference and keeps the motor magnetized indefinitely till fault is cleared. Also this scheme works best for less severe sags than for more severe ones (0.5pu to 0.1pu)

Chapter 5

Ride-Through Response for MC based General Purpose Industrial Applications

This chapter presents the MC fed ASD response to the different voltage sag scenarios with the proposed ride-through scheme for general purpose industrial applications. It also discusses the response of different load types to this ride-through scheme.

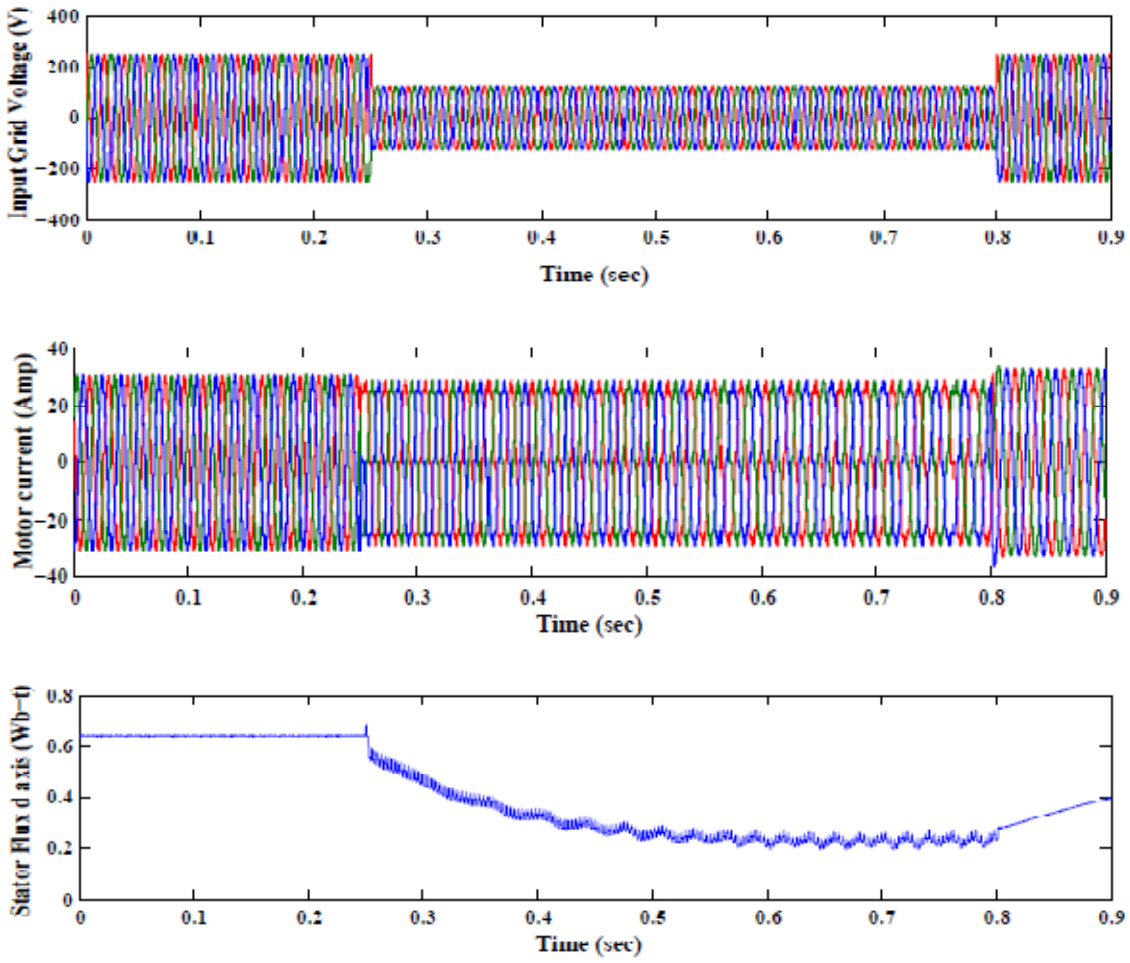
5.1 ASD Response to Different Voltage Sag conditions

The voltage sags observed in transmission and distribution networks generally affect more than one of the voltage phases. Moreover, each of the three phases might perceive a different voltage sag characteristic during a fault. In other words they may see different sag magnitudes and phase angle jumps during the voltage dip power disturbance. Hence, this section aims to verify the proposed strategy with the different fault scenarios (both symmetrical and unsymmetrical faults) as listed in Chapter 2. The dip type was extracted by comparing the RMS voltages of the phase to neutral and the phase to phase voltage with their nominal values. This method was proposed in [68] and is easy to implement.

5.1.1 Type A Voltage sag

This is a three phase symmetrical fault considered one of the worst faults though not that frequent. It shows an equal drop in magnitude for all three phase to neutral voltages. Fig 5.1 shows the waveforms obtained for such a fault at the grid input. The waveforms show that the scheme works with this kind of sag and extends a ride-through duration of

the machine depending on the severity of the sag and other parameters as discussed in Chapter 4. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. The stator flux linkage decelerates to almost one-third the rated value and is sustained at that point through the entire ride-through duration. There is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is restored. Finally the figure shows the ride-through profile of the machine during a three-phase symmetrical fault. According to this profile, the maximum ride-through duration of the machine is around 1.7 sec for a Type A Voltage Sag.



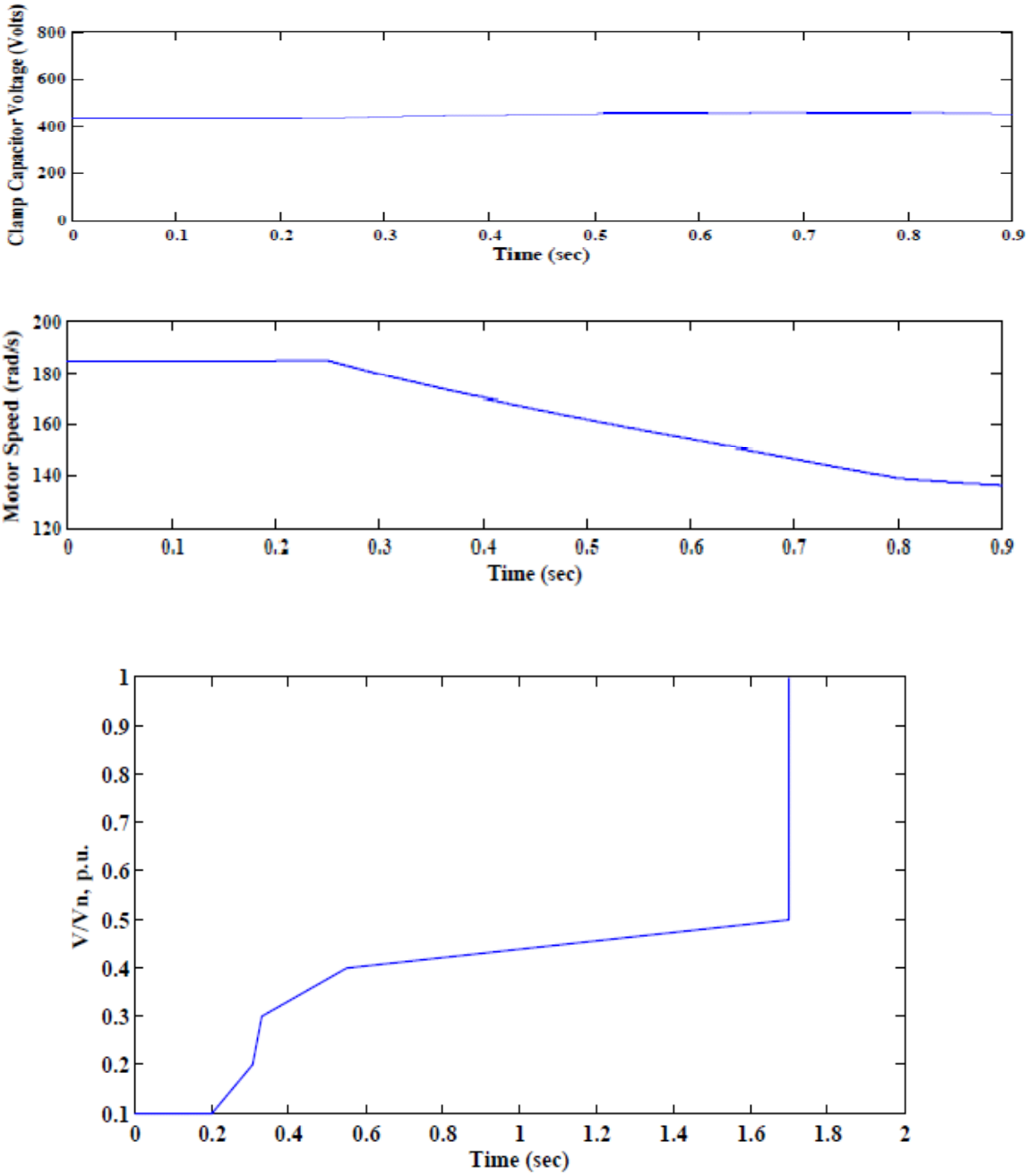
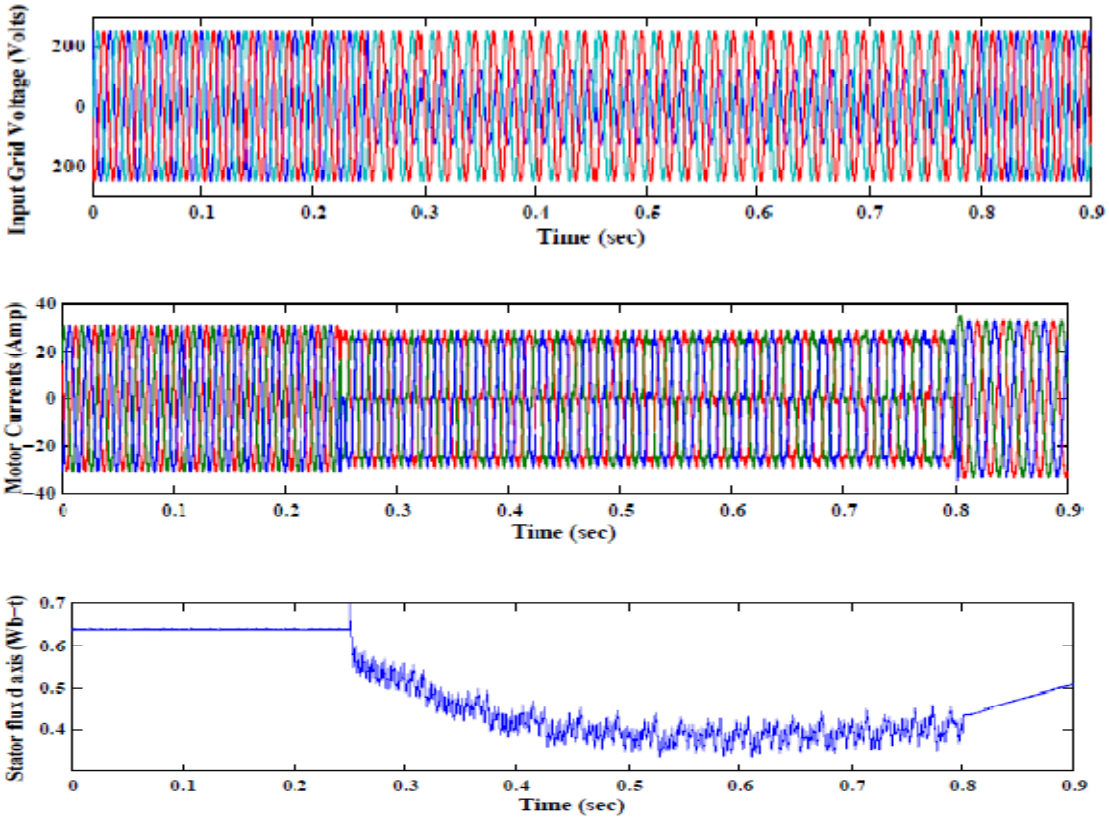


Fig 5.1 ASD Response to Type A Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.2 Type B Voltage sag

Type B Voltage sag shows a phase to ground fault, where there is a drop in one of the phase to neutral voltages while the other two phases show a phase angle jump due to the unbalance of the fault (transformer between the fault location and the load removes the zero sequence component). The waveforms are similar to the three phase sag and hence show that the scheme works with this kind of sag. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. There is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is restored. The maximum ride-through duration of the simulated system for the Type B Voltage Sag is around 2.3 sec as seen by the ride-through profile figure.



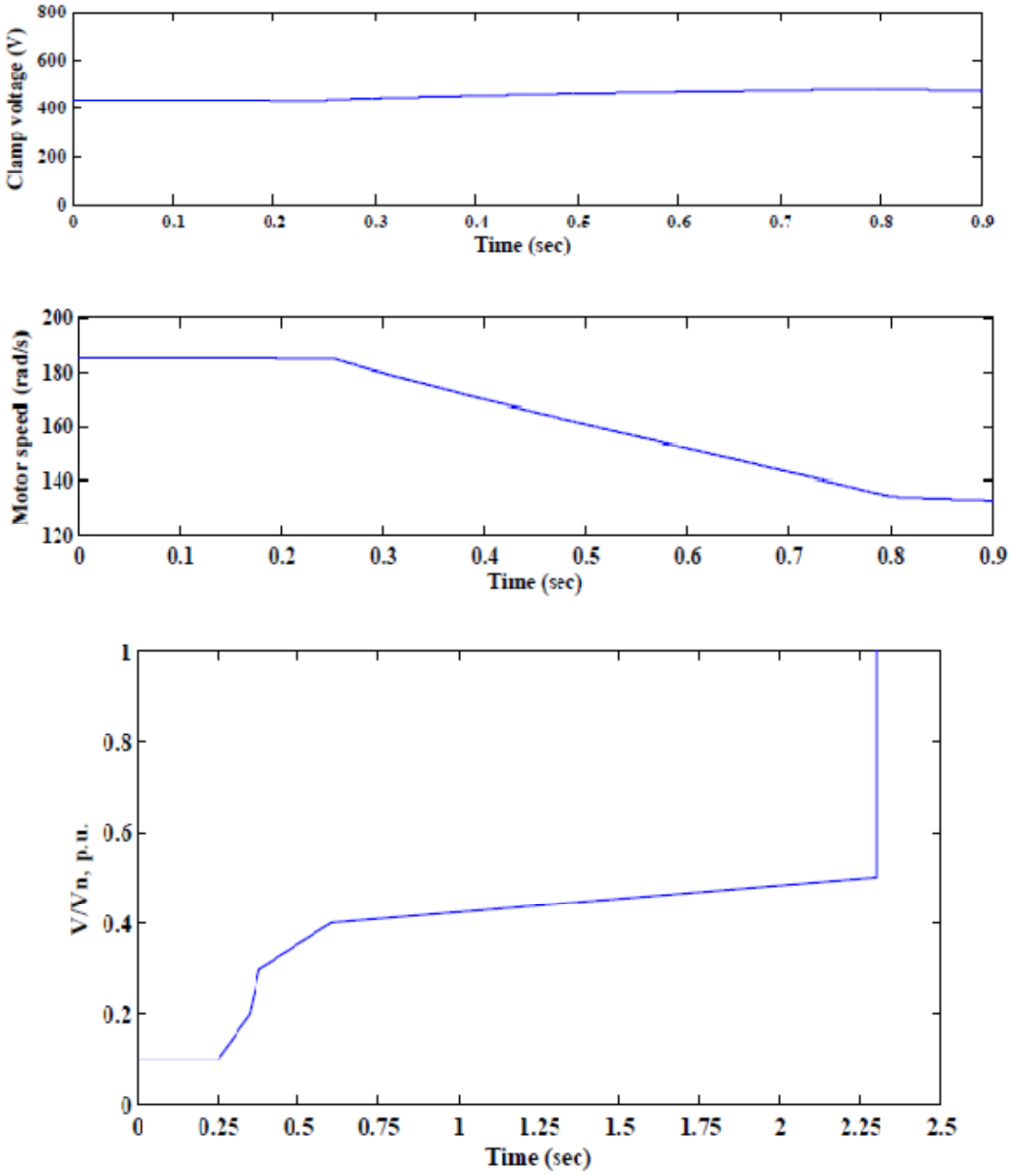
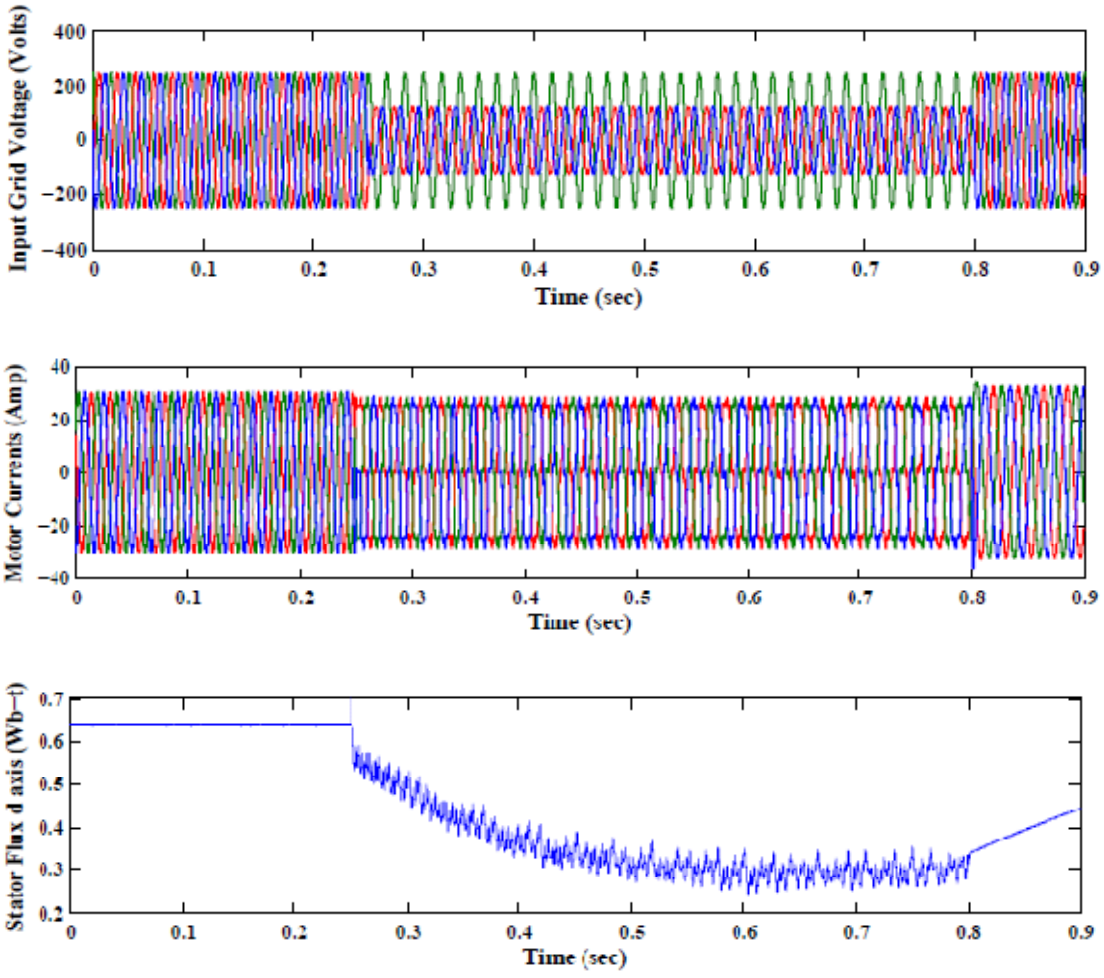


Fig 5.2 ASD Response to Type B Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.3 Type C Voltage sag

A phase to phase fault results in a Type C Voltage sag. There is a voltage drop in two of the phases with a phase angle jump. The output waveforms are almost similar to the Type A, B sags and hence show that the scheme works with this kind of sag. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. There is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is restored. The maximum ride-through duration of the simulated MC Drive system for this type of voltage sag is around 2 sec as seen by the ride-through profile.



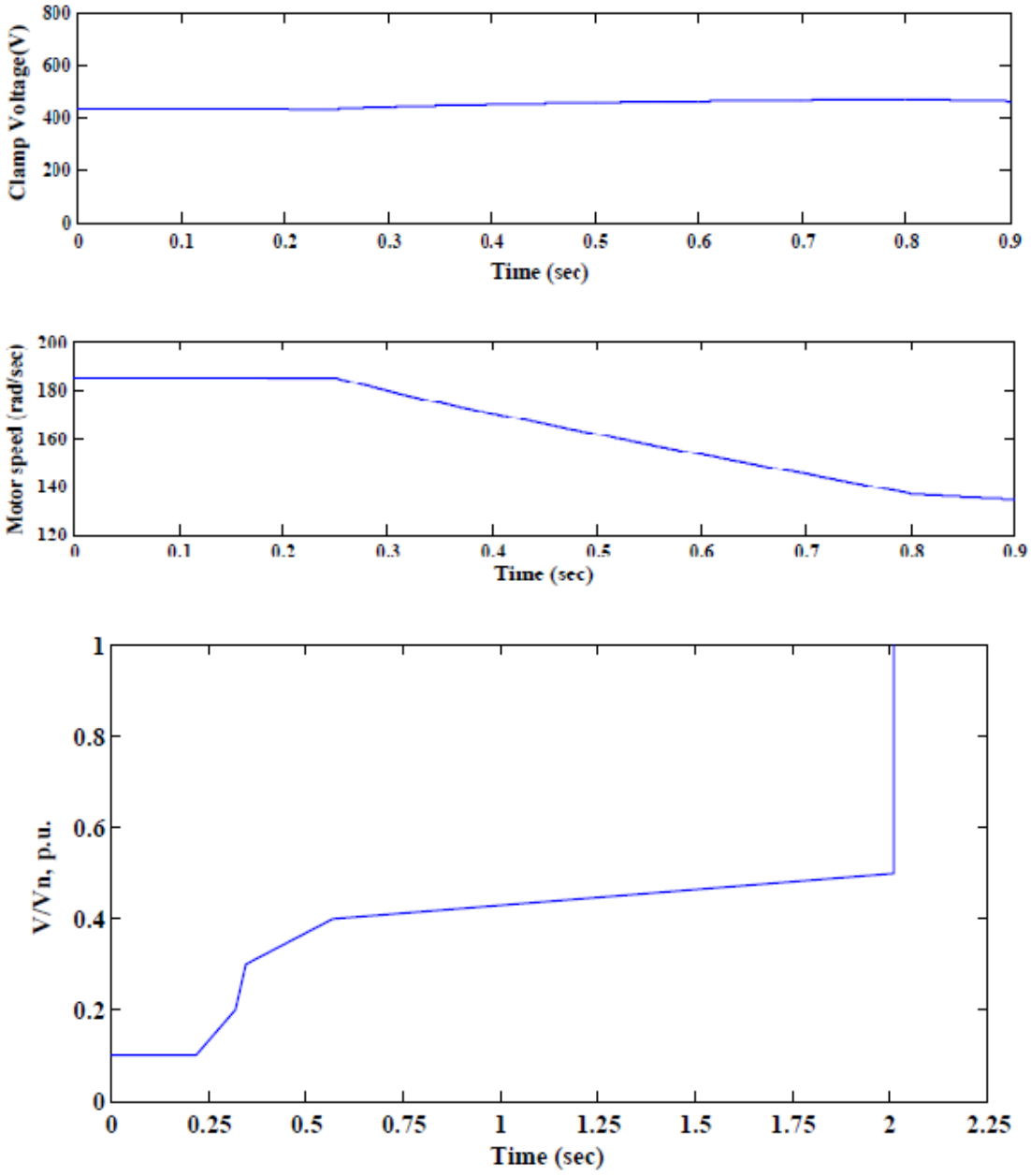
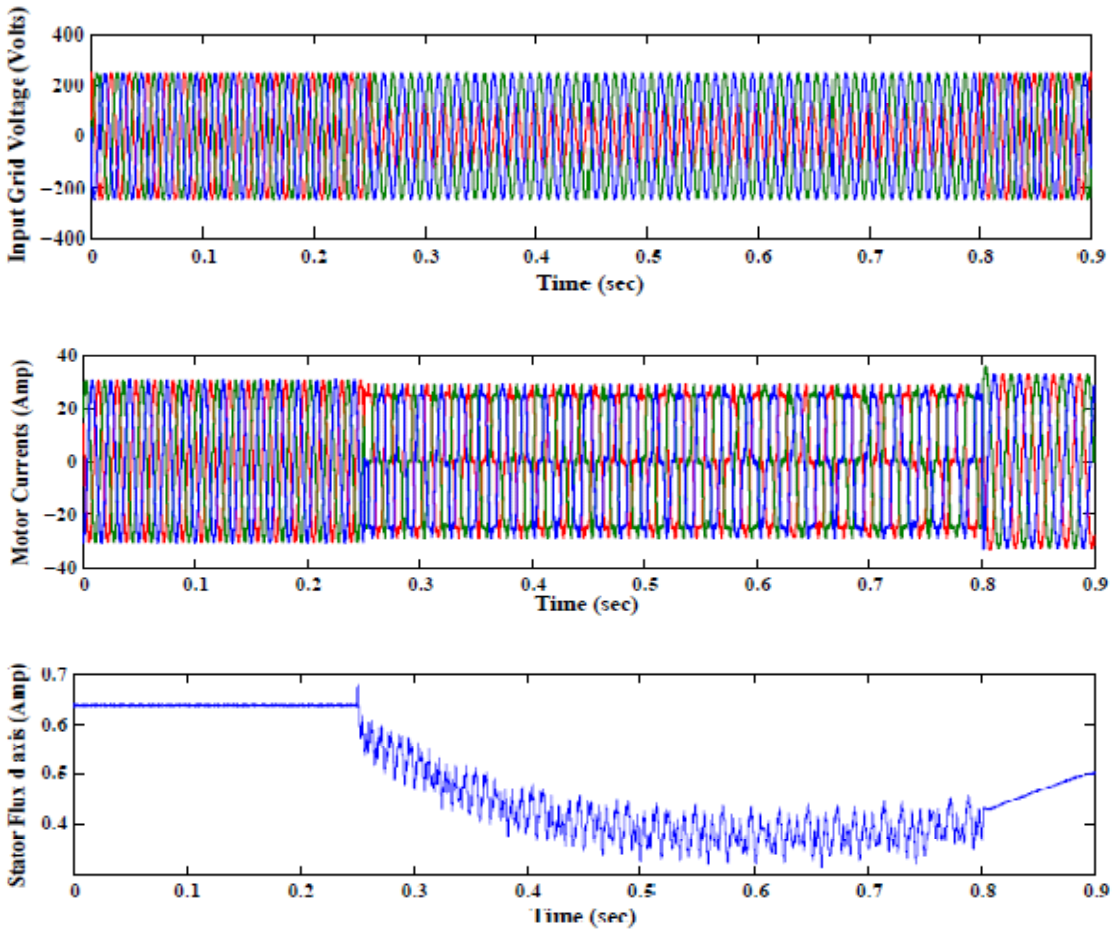


Fig 5.3 ASD Response to Type C Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.4 Type D Voltage sag

A phase to ground fault results in a Type D Voltage sag, similar to Type B sag. There is a drop in one of the phase to neutral voltages while the other two phases show a phase angle jump. The output waveforms show that the scheme works with this kind of sag. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. There is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is restored. The ride-through profile of the system during a Type D Voltage sag shows a maximum ride-through duration of 2.2 sec.



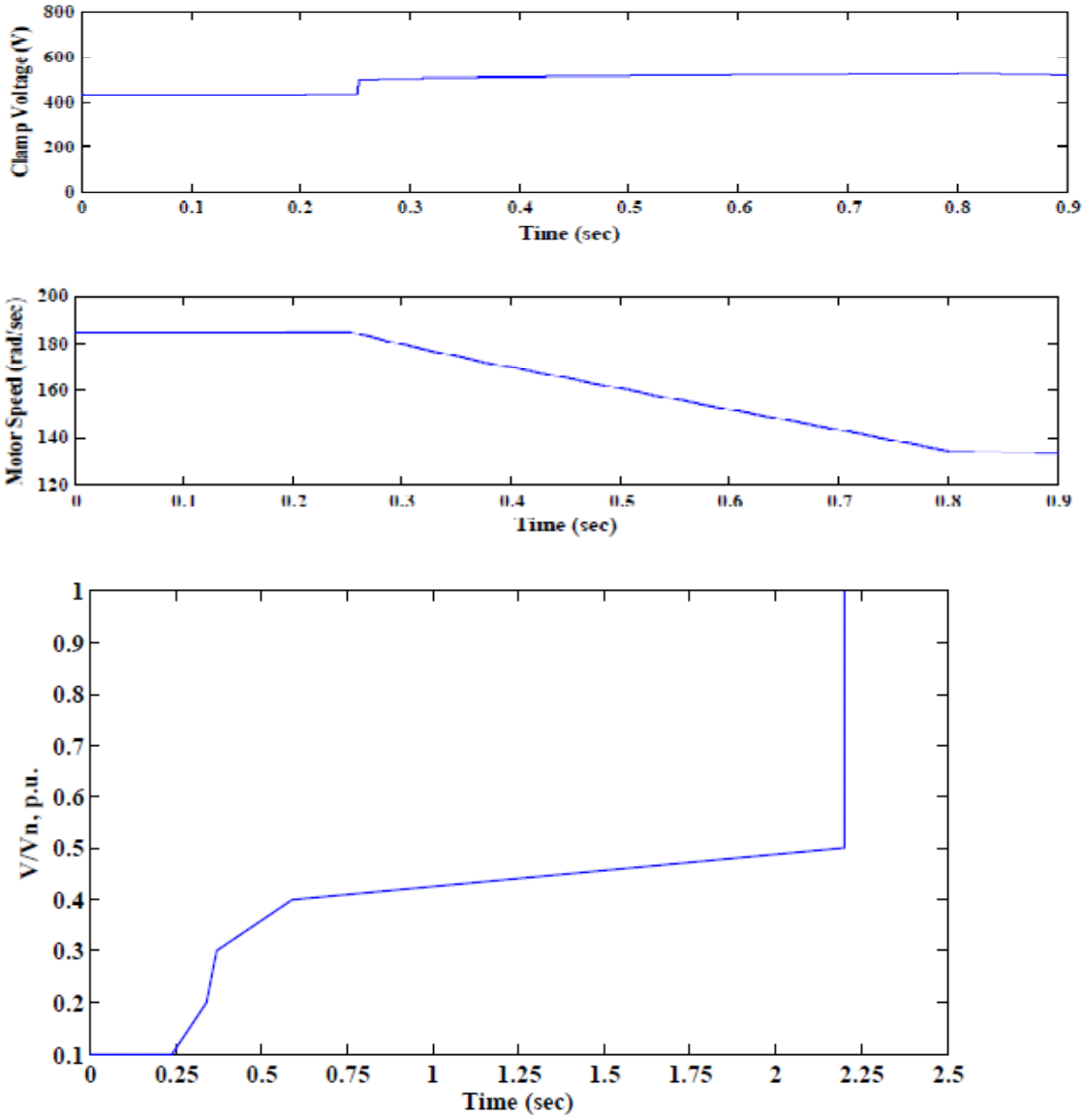
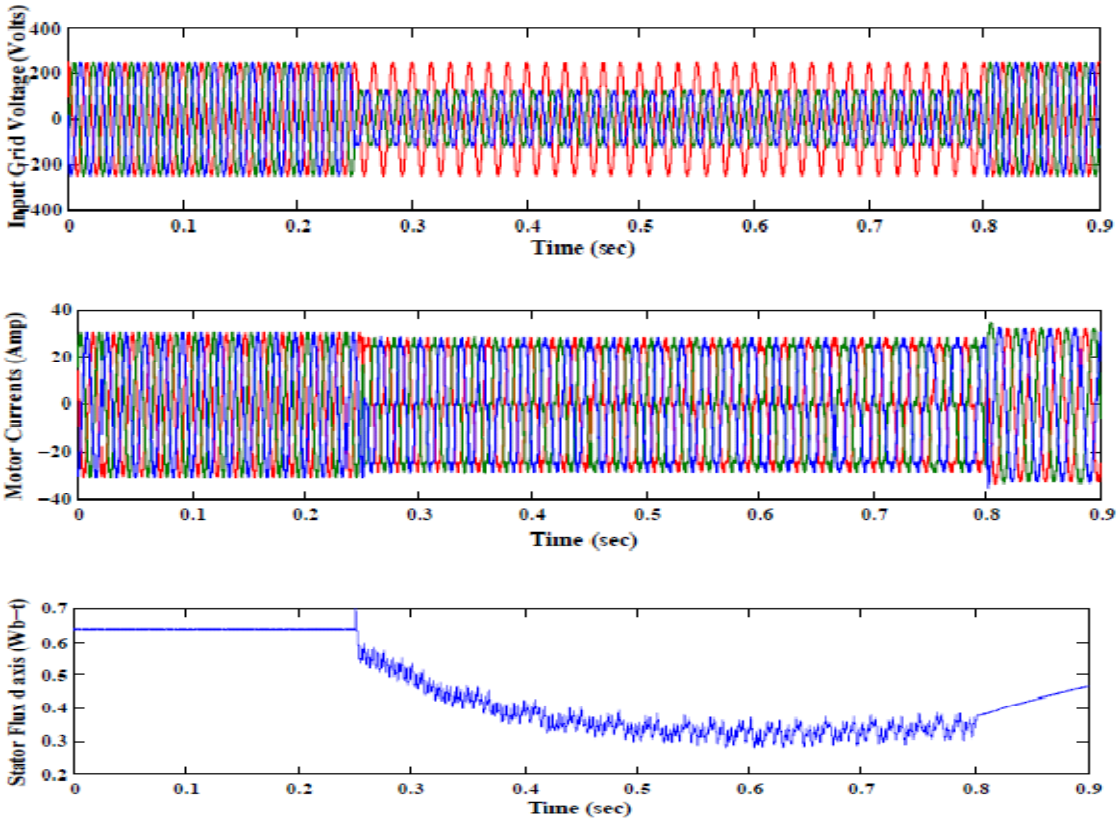


Fig 5.4 ASD Response to Type D Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.5 Type E Voltage sag

A two-phase-to-ground fault results in a Type E voltage sag. There is a drop in two of the phase to neutral voltages while the other phase remains un-sagged. The output waveforms show that the scheme works with this kind of sag. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. The stator flux linkage decelerates to nearly fifty percent and then starts increasing as the flux drop gets compensated through voltage vector alignment. There is a smooth transition from the ride-through mode to the normal mode of operation once the power system gets restored to normal operation. The ride-through profile of the particular MC fed drive shows the maximum ride-through duration during a Type E Voltage Sag to be around 2.12 sec.



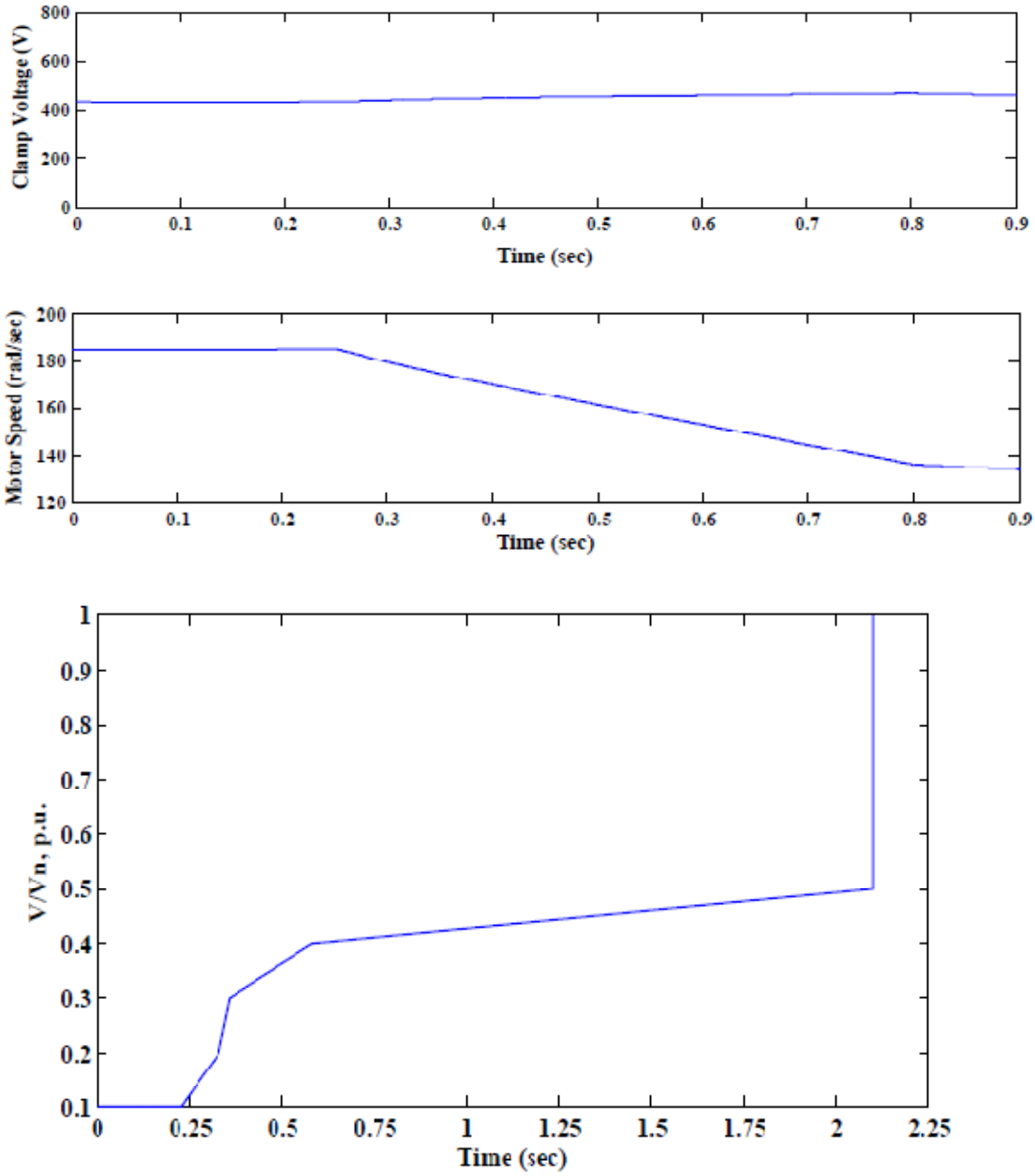
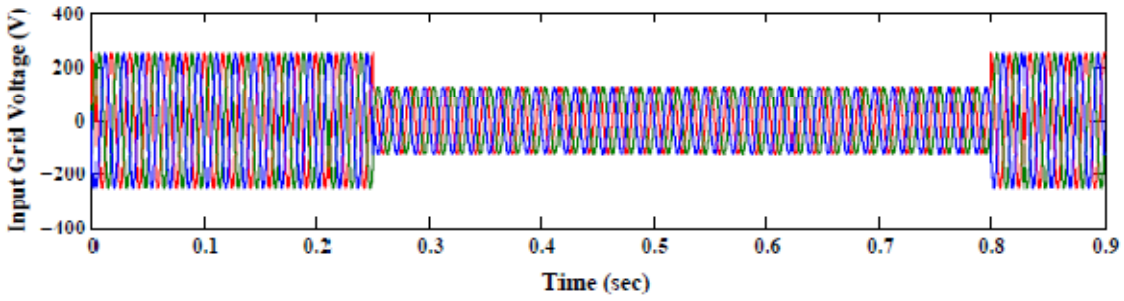
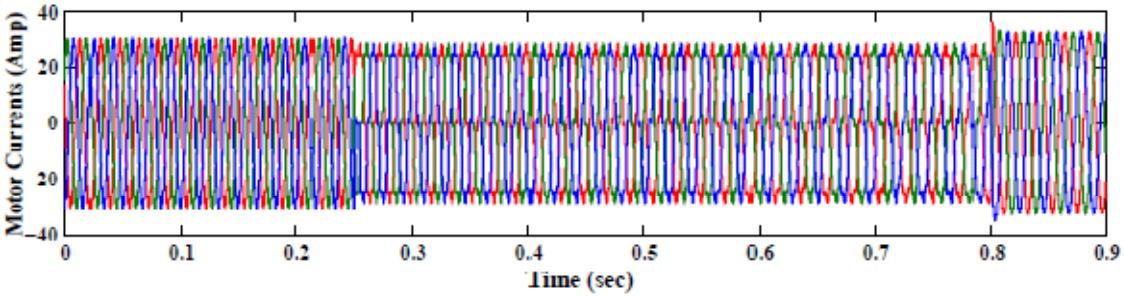


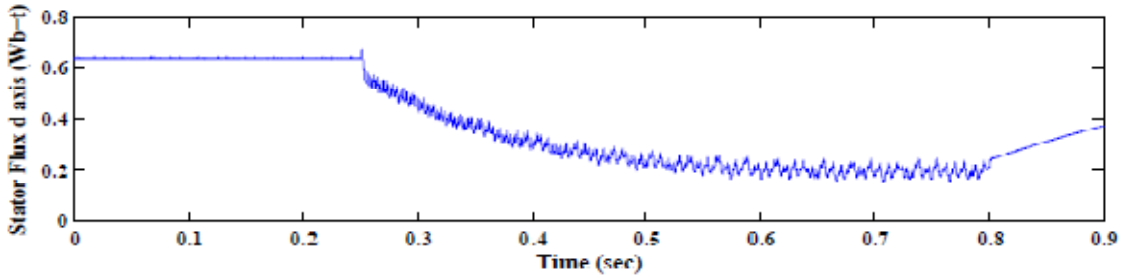
Fig 5.5 ASD Response to Type E Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.6 Type F Voltage sag

A two-phase to ground fault with a phase angle jump results in a Type F Voltage sag. There is a voltage drop in all the three phases while two phases also show phase angle jump. The output waveforms show that the scheme works with this kind of sag and there is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is cleared. The stator flux linkage value decelerates by some amount and then is sustained at a lower value (around one-third of its rated value) for the subsequent ride-through period. The drive ride-through profile shows a maximum ride-through duration of 1.9 sec for a Type F Voltage Sag.







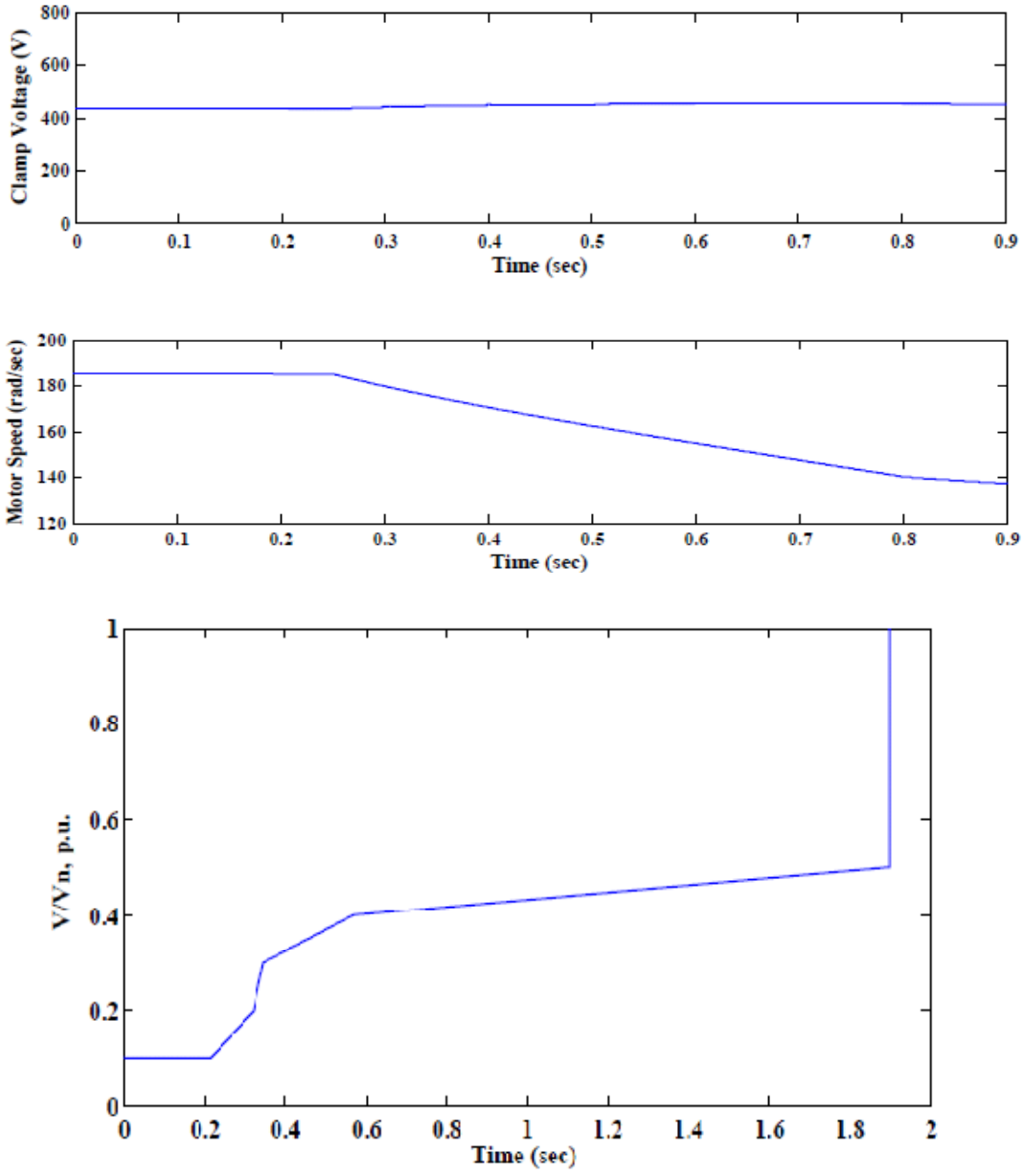
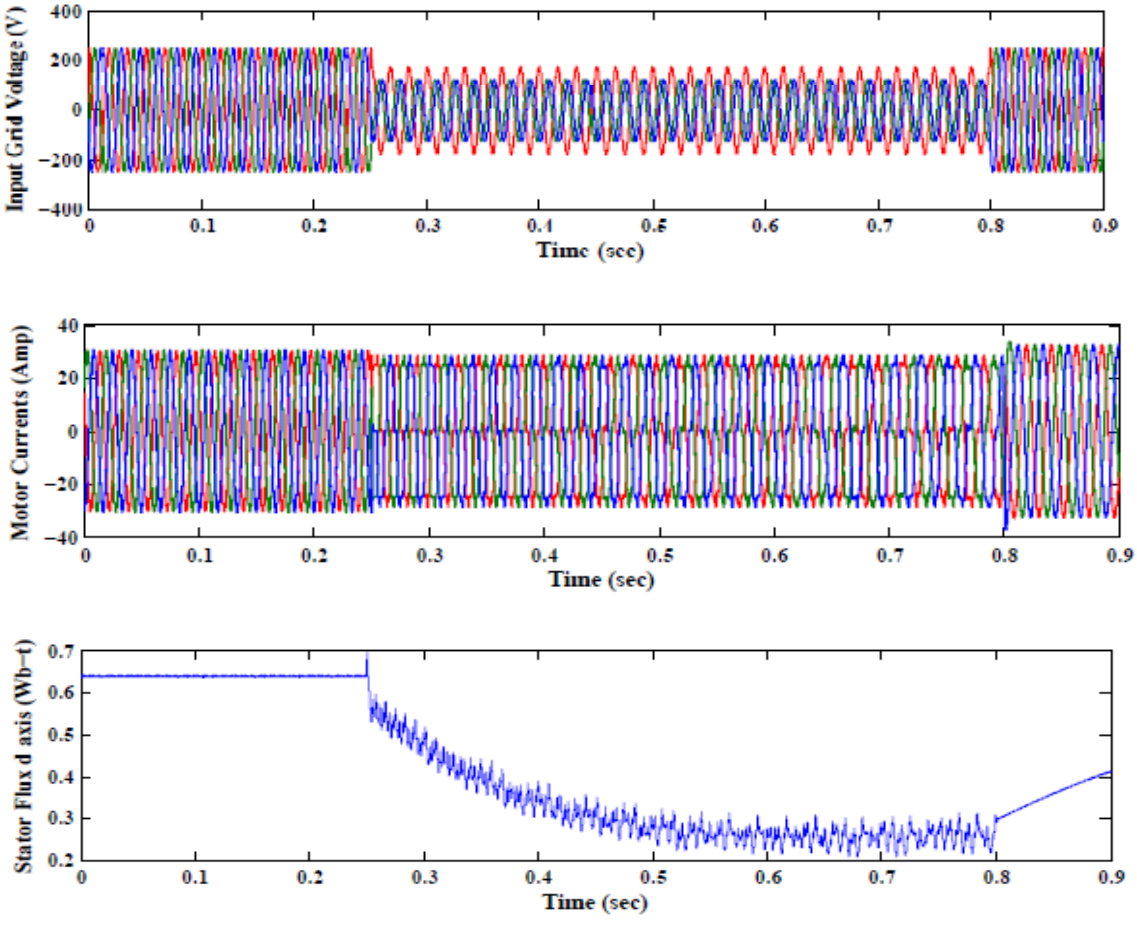


Fig 5.6 ASD Response to Type F Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.1.7 Type G Voltage sag

Type G Voltage sag is caused by a two-phase to ground fault similar to the Type F sag with the only difference being the phase angle jump. The output waveforms for this kind of sag also show that the scheme works with this kind of sag. During the fault as expected, the speed decelerates slowly while the clamp capacitor value is almost maintained without significant over-voltages. There is a smooth transition from the ride-through mode to the normal mode of operation once the fault at the input is restored. The ride-through profile of the machine under a Type G Voltage sag reveals the maximum ride-through duration of 1.75sec for the machine simulated.



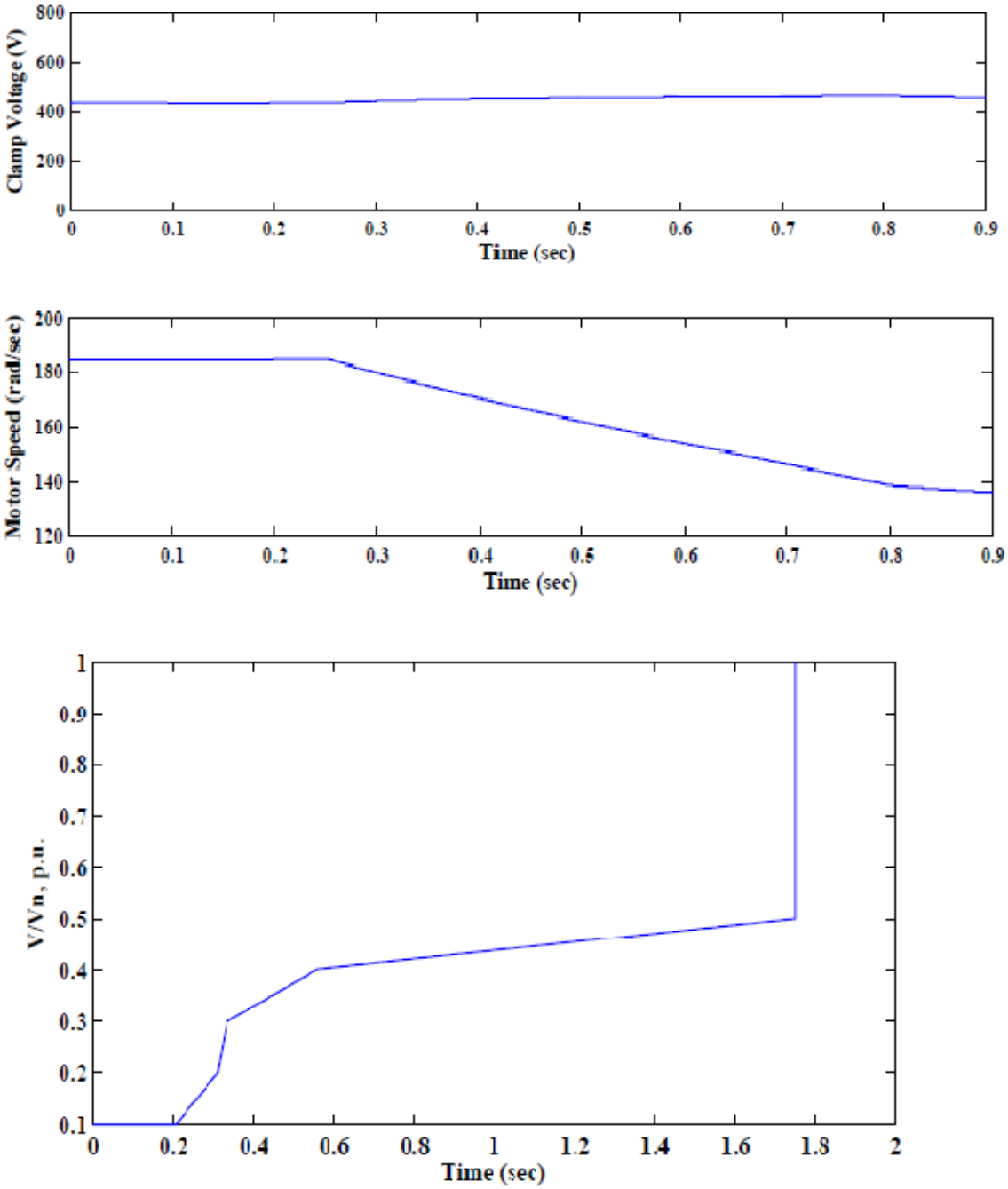


Fig 5.7 ASD Response to Type G Voltage sag for a duration of 550 ms with subsequent voltage restoration (a) Three-phase Input Grid Voltages (b) Three-Phase Motor Currents (c) d-axis component of Stator Flux Linkage (d) Clamp Capacitor Voltage (e) Motor speed (f) Ride through profile with Rated Torque Load.

5.2 ASD Dependence on Load Characteristic

An essential variable has been left out in all our discussion and testing for voltage sag ride-through response of ASD's. ASD response is dependent not only on sag magnitude, sag duration, steady state load torque value, machine inertia and other such parameters but also on the load types. Industrial loads represent any one of the broad categories: constant horsepower load, constant torque load or variable torque loads [66]. For example a plastic extruder might not present the same speed-torque characteristic as a conveyor though they might have the same steady-state value at any particular operating point.

For the steady-state constant torque load type, the load torque is constant over any load speed. A steady-state constant torque load type can be described by $T_L = k$ where T_L is the steady-state load torque and k represents the constant load torque value. Conveyors and extruders are few examples of constant torque load types**.** Fig 5.8 is a graphical representation of a steady-state constant torque load.

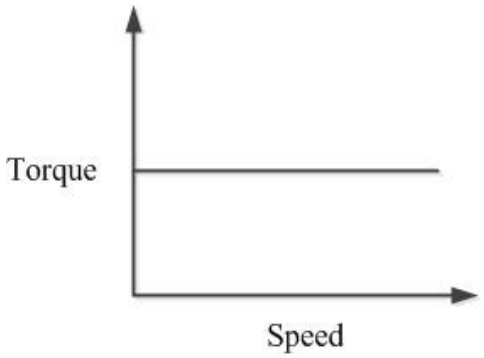


Fig 5.8 Steady State Constant Torque load Type.

For the steady-state constant power load type, the load torque varies **as** the inverse of the speed. Thus, low speeds produce high torque and vice versa. The load power stays constant over the entire speed range of the load. A steady-state constant power load type

is described as $T_L = P_L \omega_m^{-1}$ where P_L is the load power and ω_m is the angular speed of the motor. Traction motors, cranes and lathes are few examples of constant power load types**.** Figure 5.9 is a graphical representation of a steady-state constant power load.

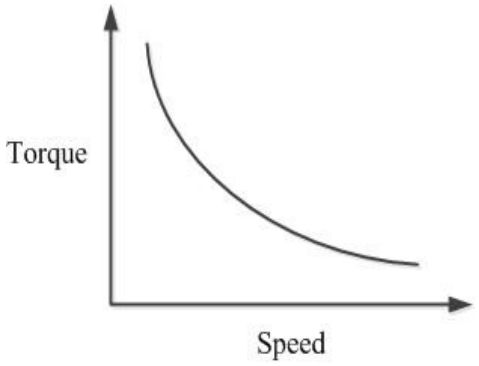


Fig 5.9 Steady State Constant Power Load Type.

For the steady-state variable torque load type (considering quadratic type load here), the load torque changes **as** some function of the speed. A steady-state variable (quadratic) torque load type is described by $T_L = k\omega_m^2$ where k is a constant coefficient associated with the load. Fans, blowers, centrifugal pumps, and compressors are examples of variable torque load **types.** Figure 5.10 is a graphical representation of a steady-state quadratic variable torque load.

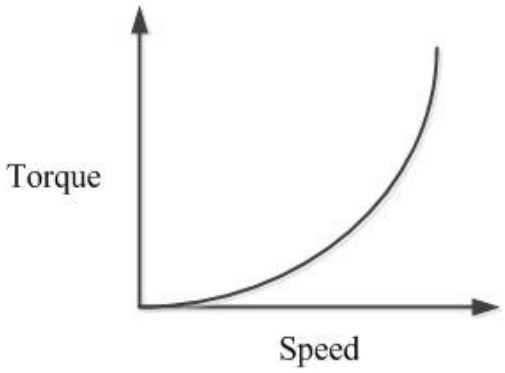


Fig 5.10 Steady State Quadratic Variable Torque Load.

5.2.1 Simulation Results

With the ASD operating in steady state, a balanced three-phase voltage sag of 75% nominal voltage and 250ms duration was applied to the system, as shown in Fig 5.11 .When the voltage sag was applied to the ASD**,** the system speed fell to 1520 rpm for the constant power load type. For the quadratic variable torque load type**,** the system speed only fell to 1560 rpm. The load torque increases **as** the speed decreases for the constant horsepower load type while the load torque decrease **as** the speed decreases for the quadratic variable torque load type. Therefore, the speed reduction under a constant power load is expected to be higher than that of quadratic load. Consequently with different speed drops during the sag, the ride-through duration would also be different as the duration is limited by the speed deceleration, considering all load types have the same inertia.

Comparison between different voltage sag speed responses for different load types in the case of two-phase voltage sags with rated voltage in the third phase for ASD is shown Fig. 5.12. The difference in speed drops of different load types is lesser than for the three –phase sags which means that influence of different load types on ride-through duration is even smaller than in the case of balanced three-phase sags. Fig. 5.13 again shows a very small influence of different load types on ASD ride-through duration in the case of single-phase voltage sags with rated voltage in the two un-sagged phases.

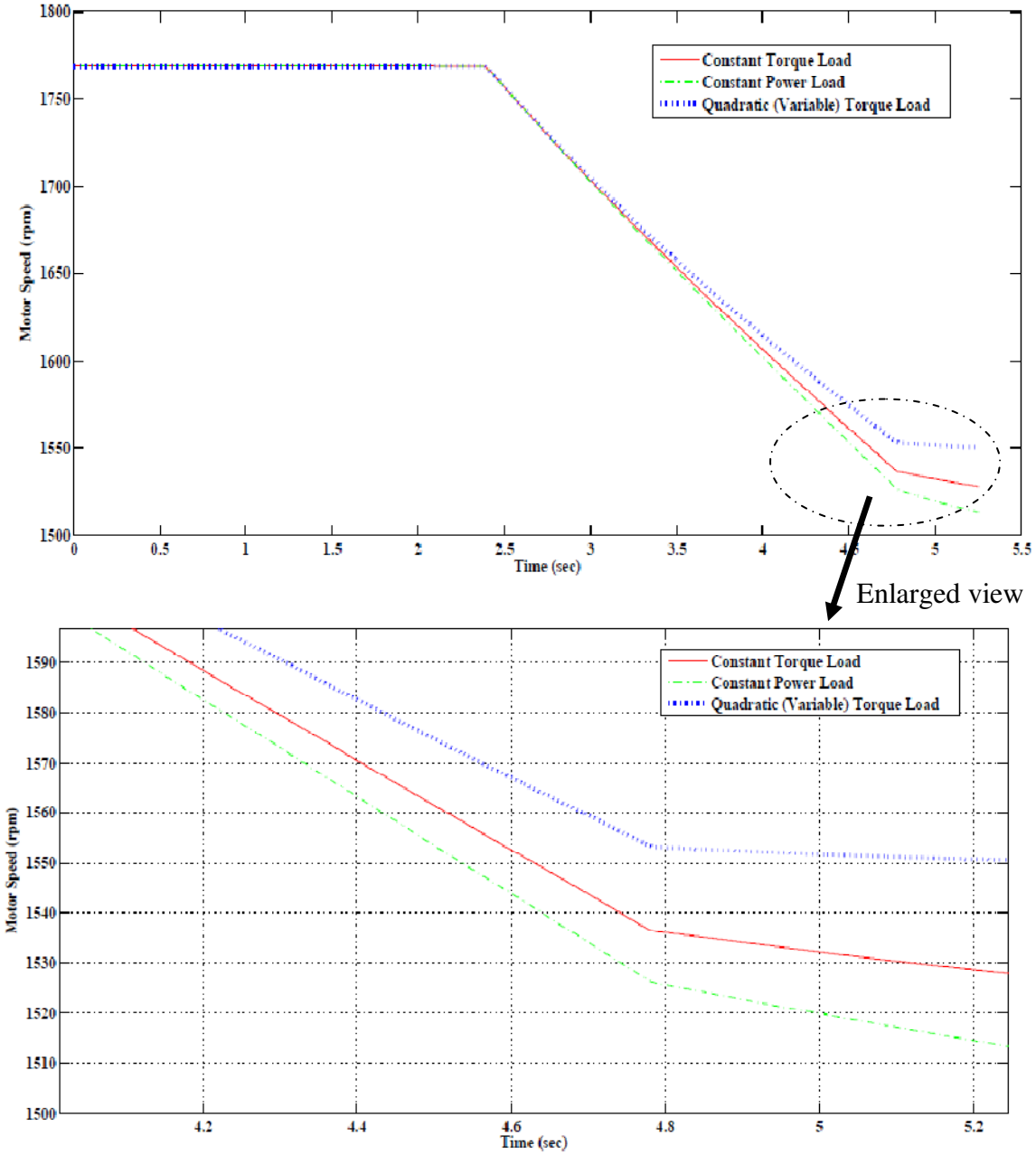


Fig. 5.11. Influence of different load types on ASD speed response to balanced three-phase voltage sags.

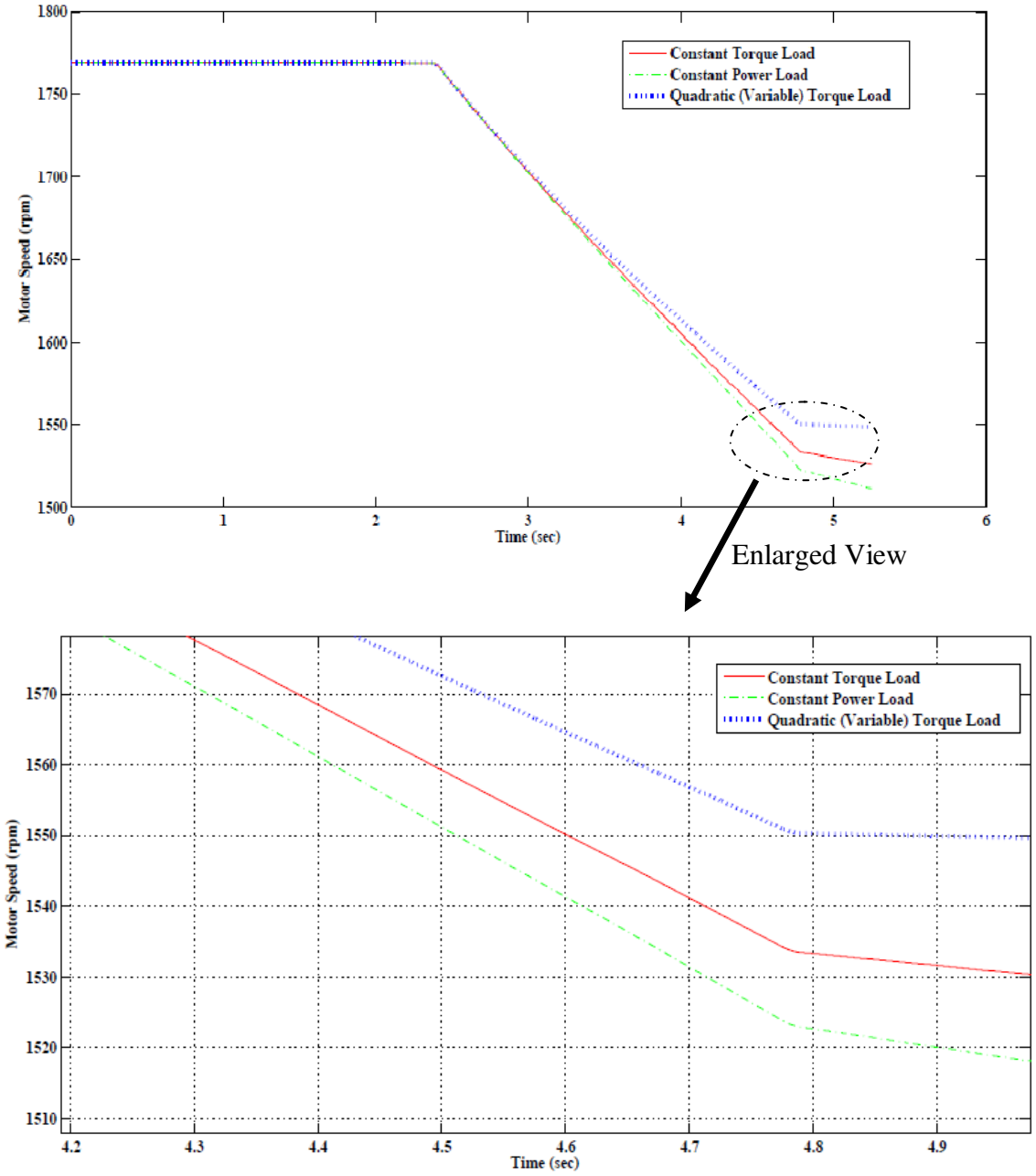


Fig. 5.12. Influence of different load types on ASD speed response to two-phase voltage sags with rated voltage in un-sagged phase.

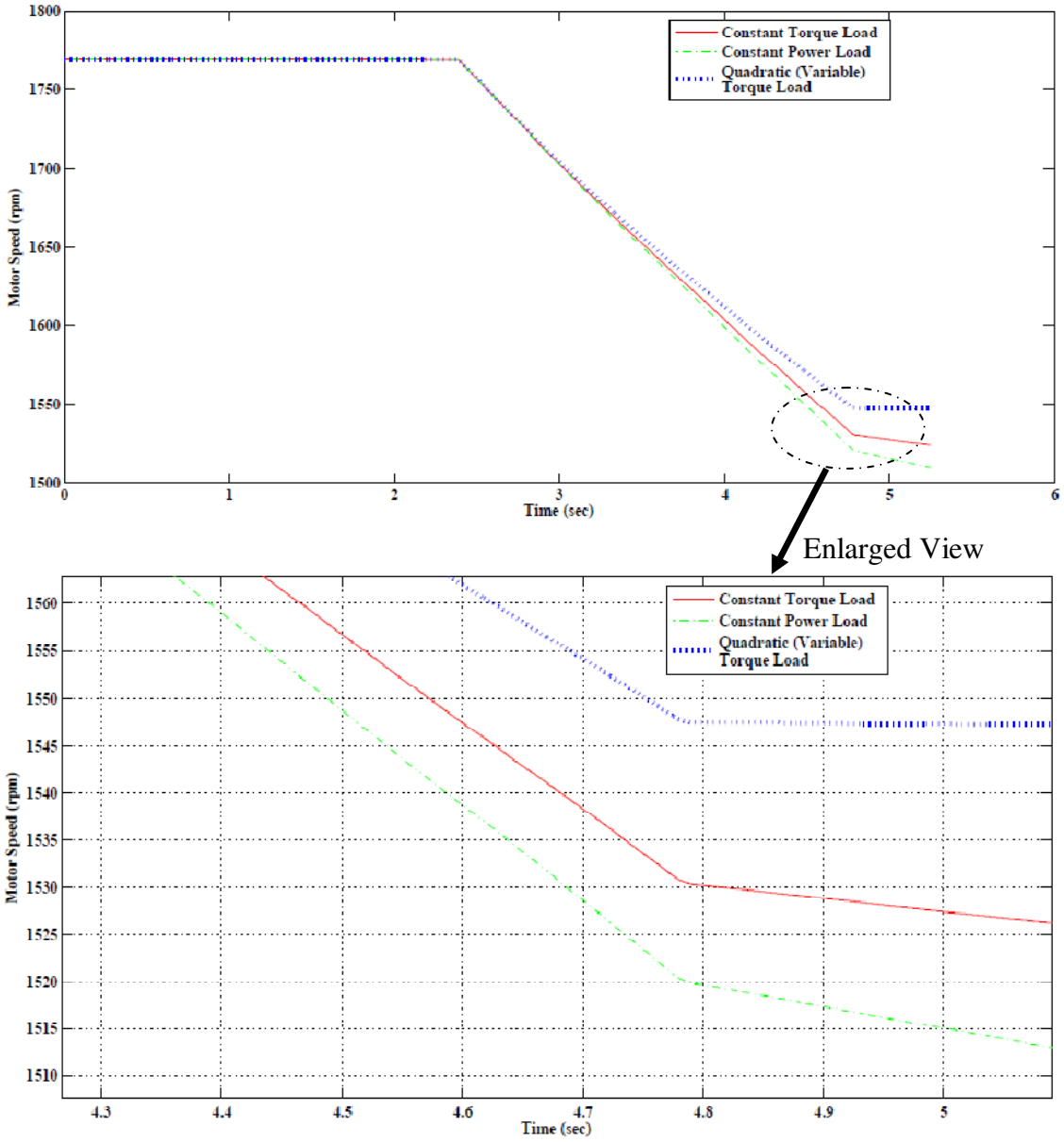


Fig. 5.13. Influence of different load types on ASD speed response to single-phase voltage sags with rated voltage in un-sagged phase.

5.3 Three Phase Fault Ride-Through Duration Evaluation

The waveforms shown in Fig 5.14 and Fig 5.15, show the variation in ride-through duration, with different reference currents, and different percentage of voltage sag (V/Vn

*100). At a particular reference current, the 10%sag has lower ride-through duration as compared to 20% sag and so on. For 50%sag and beyond, the ride-through durations are limited by the mechanical energy of the system. This means that for an infinite inertia machine (hypothetical case), the flux can be sustained for infinite time using this strategy. As the reference currents are lowered the ride-through duration increases, because now, with lower current values in the machine, the torque values decrease due to which speed decreases at a slower rate.

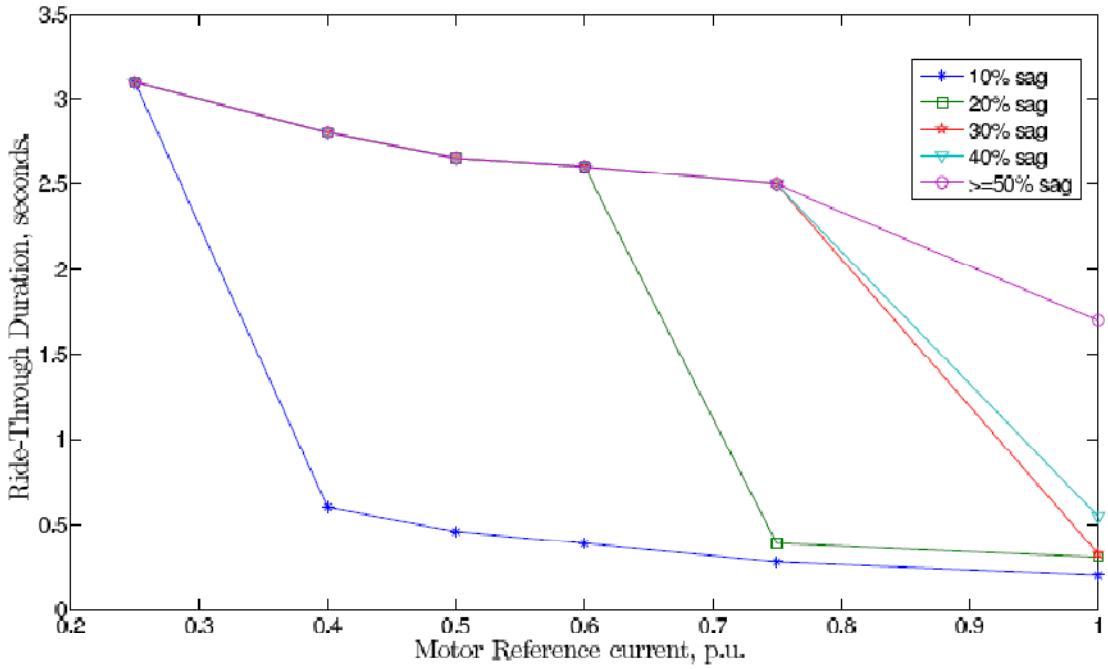


Fig 5.14 Ride-Through Duration Vs. Current Reference at Full Load torque.

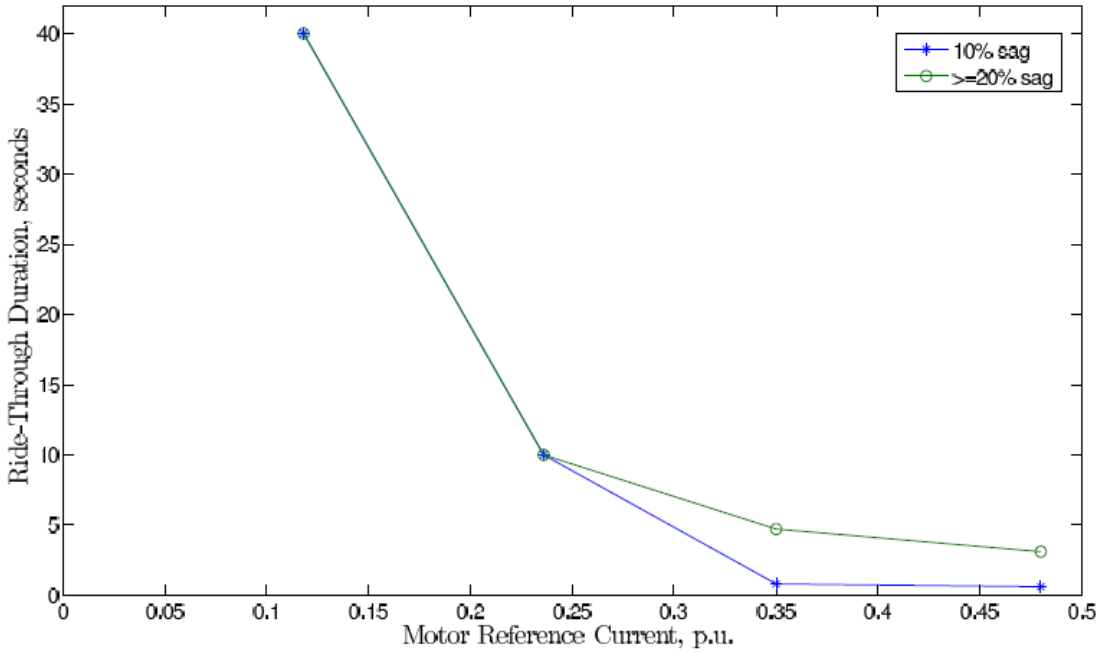


Fig 5.15 Ride-Through Duration Vs. Current Reference at No Load torque.

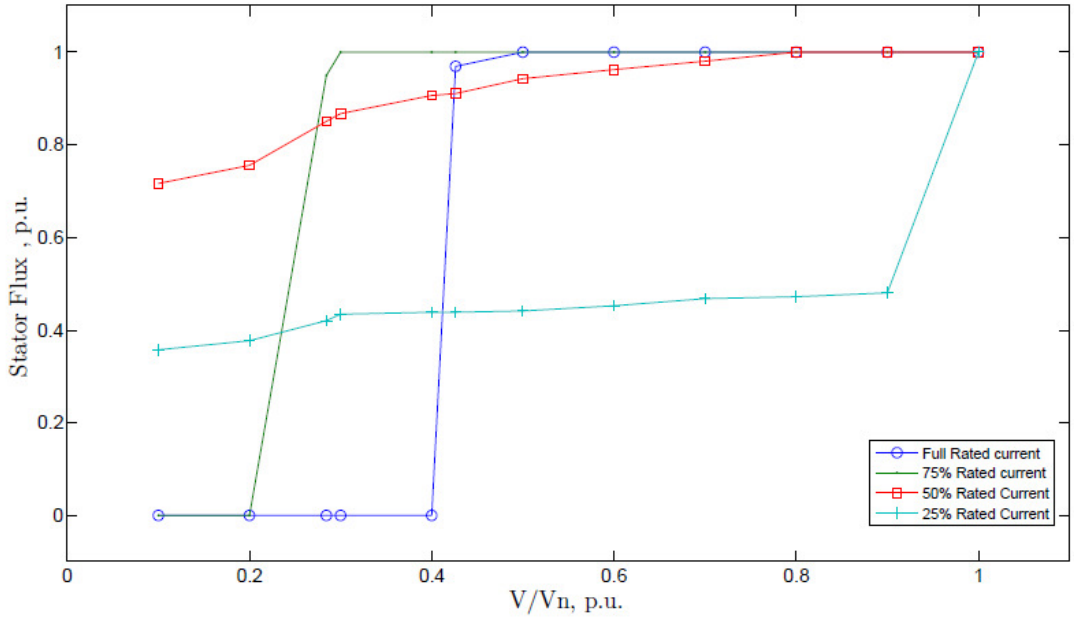


Fig 5.16 Stator Flux Vs. Voltage Sag % at Different Motor Current References.

Fig 5.15 shows a similar waveform but at no load condition. Waveforms of stator flux versus percentage of voltage dip (V/Vn *100) in Fig 5.16, show the flux levels maintained during the ride-through duration for different voltage sags and different values of reference currents. For very low voltage dip values as the reference currents are decreased below the rated, the flux levels are seen to increase, never falling to zero for 50% and 25% reference current values.

5.4 Summarizing the Results

After testing the MC Drive topology with the proposed ride-through scheme subjected to the different faults, it is seen that the scheme works for all the different fault types and sag magnitudes. The voltage profiles for each fault type with different sag magnitudes show that the Type A sag is the worst fault with the smallest ride-through duration, as each of its phases see a dip in voltage as compared to the other faults where only one or two of the phases see a dip. The best fault in terms of ride-through duration is the Type B sag which single phase sag, where only one of the phase to neutral voltages see a voltage dip. So the residual voltage in the system at the machine terminals is more than the other faults. Similar type of sags like Type C and Type F show almost similar ride-through profiles. Altogether, the ride-through profiles for the different faults on the ASD differ by slight amounts and show almost similar results with this scheme.

ASD ride-through response to different load types, with the proposed scheme has also been simulated and reveal that the variable torque load is better as compared to constant power and constant torque load, in terms of speed deceleration and hence ride-through

duration because of the quadratic decrease in torque with a decrease in speed during the voltage sag period. Finally the ride-through durations for different sag magnitudes and different motor currents and rated and no load torques have been simulated to show that with lower current references ride-through durations are increased and that load torque is an important parameter affecting ride-through duration.

Chapter 6

Ride-Through for MC based Wind Energy Conversion System

In this chapter, the proposed ride-through scheme is implemented on a grid-connected wind-energy converter system including a matrix converter and a full power variable speed squirrel cage induction generator. In this new green era, the induction generator, with its simplicity and lower maintenance, appears to be a good solution for renewable energy applications mainly hydro and wind power plants. The matrix converter, an upcoming future power electronic converter technology, is used to interface the induction generator with the grid and control the wind turbine shaft speed.

6.1 Topology/Advantages

Fig. 6.1 illustrates the schematic diagram of the MC wind turbine system. The system consists of the wind turbine rotors, a gearbox, squirrel-cage induction generator, and a matrix converter (MC). MC interfaces the induction generator with the grid and implements a shaft speed control methods to achieve maximum power-point tracking at varying wind velocities. It also performs power factor control at the grid interface and satisfies the Var demand at the induction generator terminals. The aim of the proposed ride-through scheme is to impart a ride-through capability to the wind energy conversion system to assist in meeting the grid code requirement associated with wind plants.

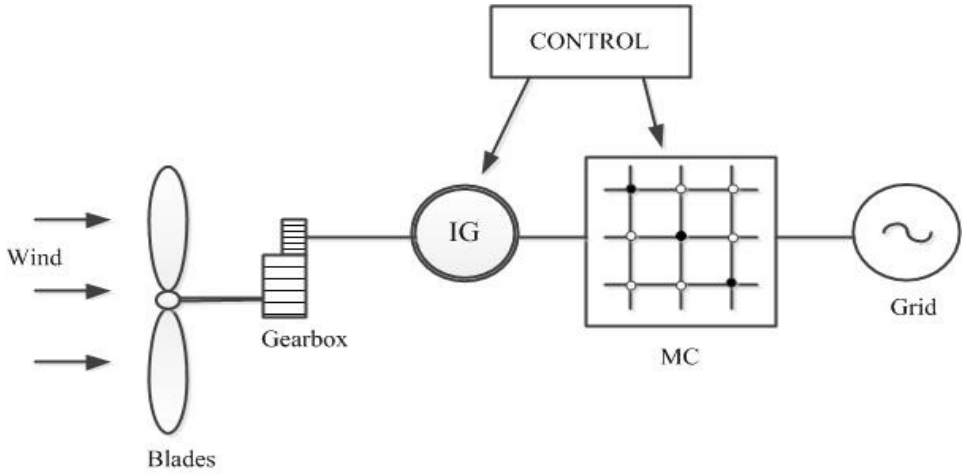


Fig 6.1 Schematic diagram of the wind turbine system.

6.2 Mathematical Modeling of WECS

Different components of the wind power generation system and the interactions among them are illustrated in Fig. 6.2 [68]. The figure shows model blocks for wind speed, the aerodynamic wind turbine, the mechanical part comprising the shaft and gearbox, the electrical generator, the matrix converter, and the utility grid. The system also contains the pitch angle control model which is used to regulate the power output of the turbine generator system.

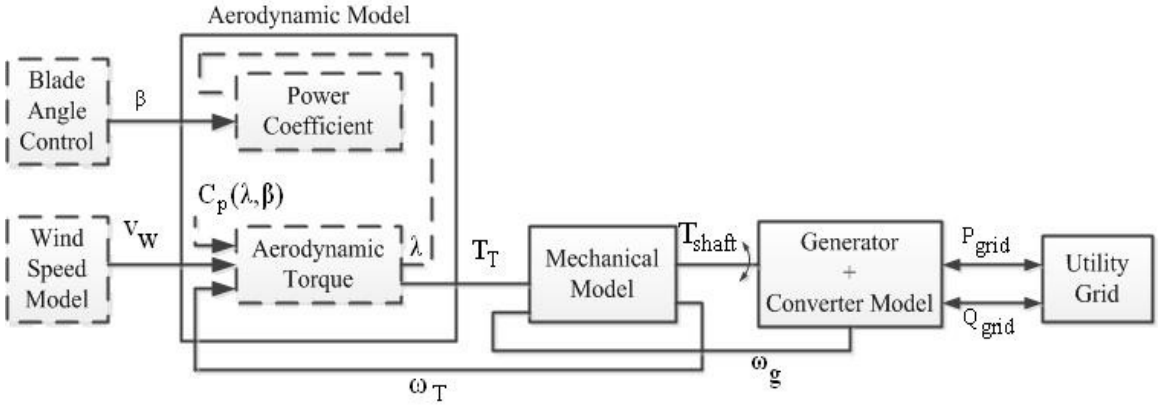


Fig 6.2 Block diagram of the overall wind turbine system model.

The entire wind energy system can be sub divided into following components [69]:

1. Wind Speed model,

2. Wind Turbine model,

3. Shaft and gearbox model,

4. Induction Generator + Power Electronic Converter model

5. Control system model (Pitch Angle Control).

The following sections describe the mathematical modeling of the above wind system components and their SIMULINK implementation.

6.2.1 Wind Model

The model of the wind should be able to simulate the temporal variations of the wind velocity, which consists of gusts and rapid wind speed changes. The wind velocity (Vw) can be written as [70], $V_w = V_{wb} + V_{wg} + V_{wr}$

where,

V_w = Total wind velocity,

V_{wb} = Base wind velocity,

V_{wg} = Gust wind component and

V_{wr} = Ramp wind component.

The base wind speed is a constant and is given by,

V_{wb} = C1; C1 = constant

However in this simulation, since the prime motive is to verify the proposed strategy, hence the wind speed is taken as constant.

6.2.2 Turbine Model

The turbine model represents the power capture by the turbine. The power in the wind (Pw) in an area is given by,

$P_w = \frac{1}{2}\rho A v_w^3$, where v_w is the wind velocity.

However, the turbine captures only a fraction of this power (Pm) which can be expressed as $P_m = P_w \times C_p$ where Cp is a fraction called the power coefficient.

The power coefficient represents a fraction of the power in the wind captured by the turbine and has a theoretical maximum of 0.5926 [71]. The power coefficient can be expressed by a typical empirical formula [69] as

$$C_p = \frac{1}{2}(\gamma - 0.022\beta^2 - 5.6)e^{-0.17\gamma}$$

where β is the pitch angle of the blade in degrees and γ is the tip speed ratio of the turbine, defined as

$$\gamma = \frac{v_w(\text{mph})}{\omega_b(\text{rad/s})} \text{ , } \omega_b = \text{Turbine angular speed}$$

The SIMULINK implementation of the turbine model is shown in Fig. 6.5

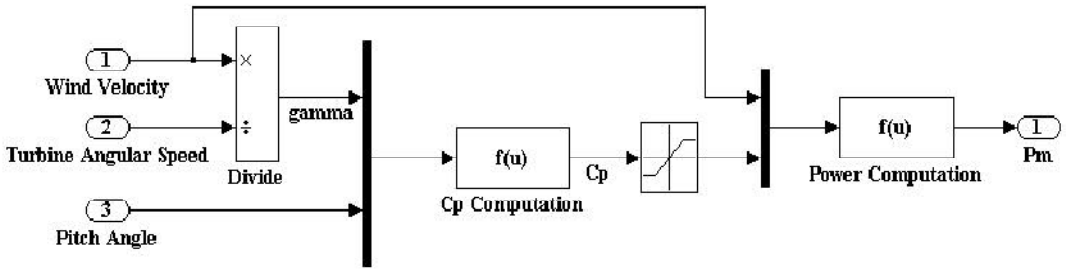


Fig. 6.3 SIMULINK implementation of the wind turbine model.

6.2.3 Standard IG Model

A dq-axis model of a squirrel cage induction generator driven by a variable pitch turbine, similar to the induction motor model as discussed in Chapter 3 and Chapter 4 has been simulated. The stator winding connects directly to the grid while the wind turbine drives the rotor. This external torque that comes from the turbine model, by convention must be negative for power generation. The induction generator converts the power captured by the turbine into electrical power and transmits it to the utility grid via stator. The generator power is limited to its nominal value in case of high and gusty winds through pitch angle control, which we will talk about in the next section.

6.2.4 Pitch control of WTG

The pitch control system is one of the most widely used control techniques to regulate the output power of a wind turbine generator. The method relies on the variation in the power captured by the turbine as the pitch angle of the blades is changed. Hydraulic actuators are used to vary the pitch angle. Normal operation, blade pitch adjustments with rotational speeds are approximately expected at $\beta n = 5$ to 10 °/ S = 0.09 to 0.17 rad/sec

The control system structure used to generate the pitch angle reference is given in Fig. 6.3 [69]. The pitch controller consists of two paths a nonlinear feed forward path, which generates β_o and a linear feedback path, which generates $\Delta\beta$. The feed forward path uses the information about the desired power output, wind velocity and the turbine speed to determine the pitch angle required. The pitch angle as a function of the measured variables is [69] as below:

$$\beta_o = \sqrt{\frac{1}{0.022}}\left[\gamma - 5.6 - \frac{2P_{ref}e^{0.17\gamma}}{P_w}\right]$$

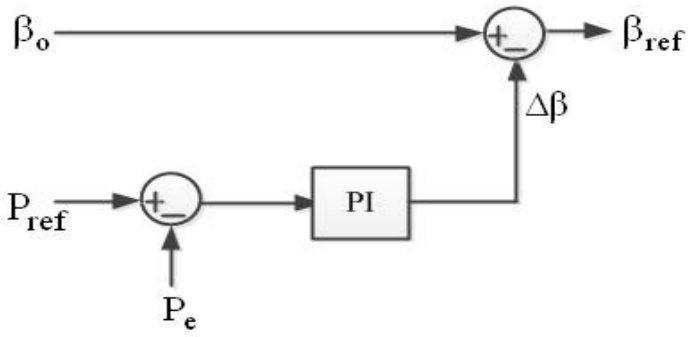


Fig 6.4 Pitch angle reference generator.

However, the feed forward term assumes that all the components are ideal and does not account for the losses in the system. The feedback path compensates for the losses by decreasing the pitch angle, if the output power is less than the desired power, to increase the power captured. The block diagram showing the plant and controller used for generating the step response is shown in Figure 6.4 [69]. The actuator is modeled as an integrator in a feedback loop. The rate limiter limits the rate of change of the pitch angle, as most pitch actuators cannot change the pitch angle more than a particular degrees /sec. The value used for the rate limiter in the simulations is 50 / sec.

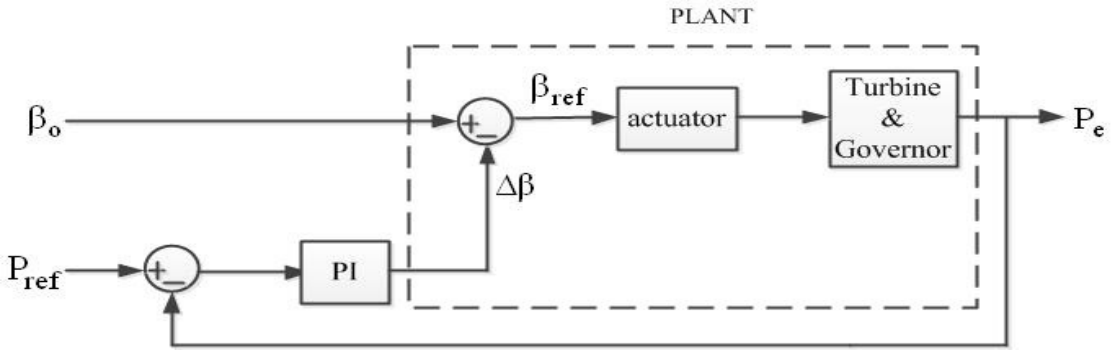


Fig. 6.5 Plant and Controller Definition.

6.3 Challenge with integration of WT into Power system

The disadvantage with the MC's is that during voltage disturbance at the grid, they unlike the state-of-the-art back-to-back topologies, are unable to decouple the input and output and hence show an absence of ride-through capability. This is due to the absence of dc link passive storage components which normally considered as an advantage acts as a disadvantage during fault conditions.

6.4 Ride-Through Operation /Simulation Results

Ride-Through operation results for the WECS System is as below. The induction generator model used is specified in Table 6.1. The results have been taken for a ride-through duration of 3 sec. The system has been subjected to a three phase balanced sag for 3 sec and then the system is recovered to follow normal operation.

Generator Parameters	Specification
Power	1.5MW
$V_{LL,rms}$	480 V
R_r	0.00145 ohms
R_s	0.00085 ohms
f	60Hz
X_m	4.25H
X_{lr}	0.02H
X_{ls}	0.015H

Table 6.1 Induction Generator Specification

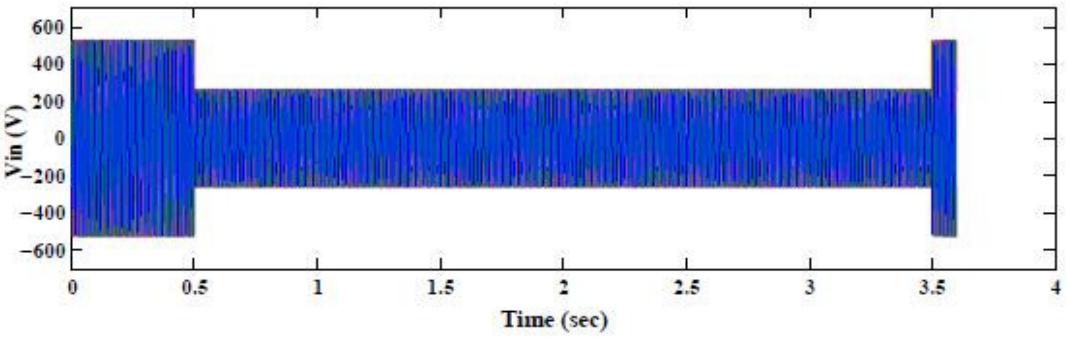


Fig 6.6 Input Three-phase Grid Voltage.

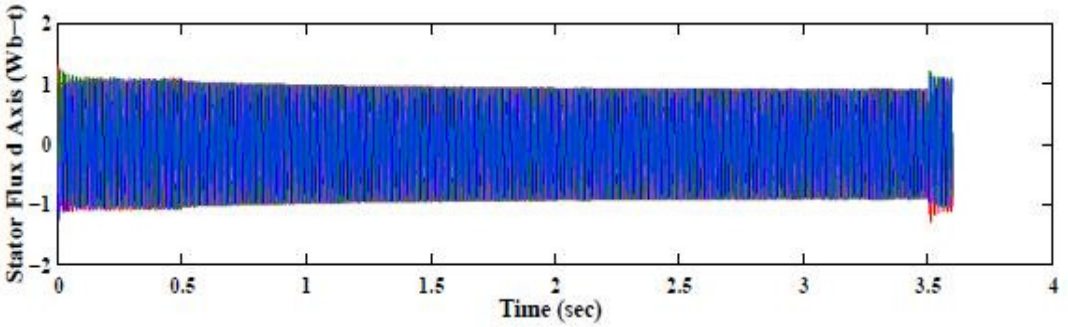


Fig 6.7 Stator Flux d-axis Linkage.

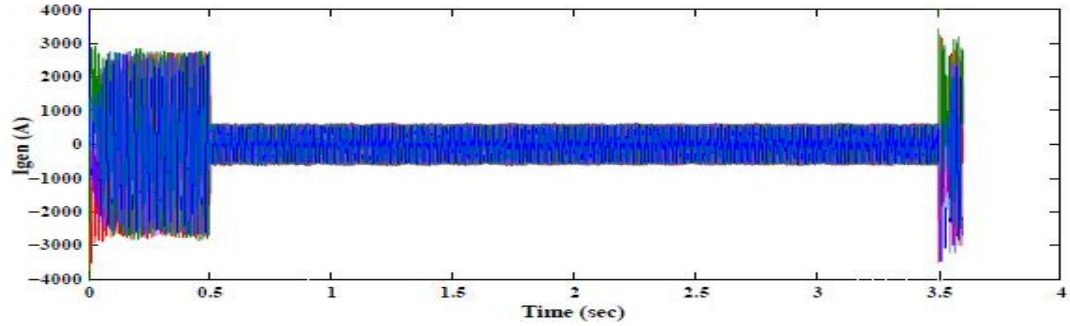


Fig 6.8 Generator Three-phase currents.

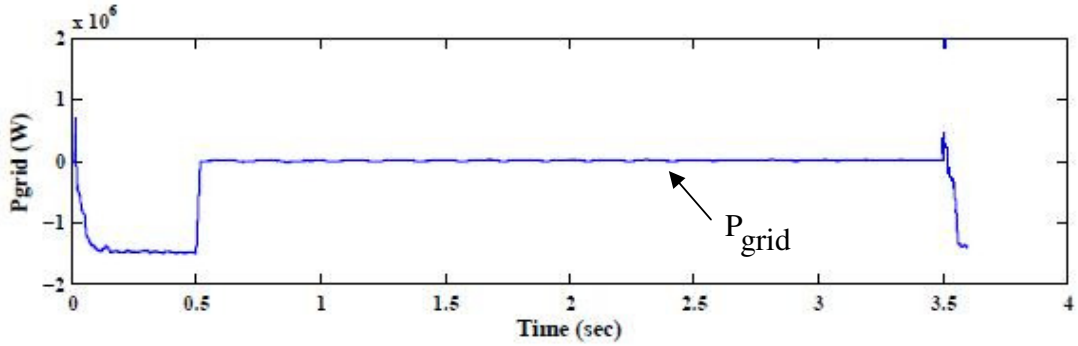


Fig.6.9 Power coming from the input grid.

As can be seen from Fig 6.6-6.9, the system remains connected to the grid for the entire ride-through duration and recovers from the fault without any system transients. Fig 6.6 shows the input grid voltage with a 50% sag occurring at 0.5 sec and then power system recovery at 3.5 sec. The generator currents in Fig 6.8 are seen to be maintained at 20% rated current (desired current picked at random) during the ride-through duration and then coming back to normal operation mode at rated current without any transients. The stator flux waveform in Fig 6.7 shows the flux being sustained for the entire fault period. Though continuously decreasing, it successfully kept the machine alive for a period of 3 sec (max. ride-through period as specified by the WECS requirements, Fig. 2.4). Power curve shown in Fig 6.9 shows a minimal amount of power being pulled from the grid during the low voltage fault duration to charge the magnetizing current and sustain the machine flux during ride-through operation. But the power being transferred is very small and hence does not affect the grid too much. The reactive power curve has not been shown explicitly as input power factor control can be controlled by proper modulation of the converter as seen by the experimental results in Chapter 3.

The above simulation results reveal that the strategy proposed can be used for the wind generation system which uses MC as the power electronic converter. The results are preliminary and a detailed simulation with wind variations and fault variations need to be done for an accurate profiling of particular induction generators for suitability to wind applications with requisite ride-through tolerance.

Chapter 7

Conclusion and Future Work

In this thesis, a novel method of enhancing the ride-through capability of matrix converter fed adjustable speed drive is proposed and verified through simulation. A squirrel cage induction machine has been selected because of two reasons: first because of its low fault handling capability due to its need for continuous external excitation, and second, due to its low-cost, simplicity and robustness, it is in wide commercial use in industrial applications as well as with renewable energy applications. The proposed ride-through scheme has been successfully tested via simulation for two potential MC Drive applications: motoring mode general purpose industrial applications and generating mode wind energy applications.

7.1 Contributions

The focus of this thesis is on three main items

- Developing a low voltage short term ride-through strategy for Matrix Converter fed Adjustable-speed Induction Drives without any external energy storage component or significant hardware modification.
- Verifying through simulation, the ride-through scheme for general purpose industrial applications which can tolerate speed reduction during the short term power disturbance.
- Verifying through simulation, the ride-through scheme for wind energy system, meeting US Grid Interconnection codes.

This research is novel because it proposes a ride-through strategy which enhances the fault handling duration of an MC Drive system as compared to the existing scheme.

Below are the major contributions of the work presented in this thesis:

1. Chapter 4 presents a novel ride-through strategy for MC fed Induction Drives, which keeps the drive system continuously modulated and hence the machine stays magnetized for a longer duration than the existing scheme. It also keeps the control electronics alive, assuming they are being fed by the clamp capacitor whose voltage is maintained.

2. Chapter 4 also presents the analysis of MC fed induction drives during fault conditions. It studies the behavior and comes up with mathematical formulations to explain the dynamic fault condition ride-through behavior of the system. In our existing literature, a detailed mathematical analysis of the ride-through behavior of an MC Drive system is lacking and hence this work will be beneficial. It also comes up with a parametric evaluation of the ride-through for the system.

3. Chapter 5 verifies the ride-through strategy through simulation for a general purpose industrial application by testing on several commonly occurring fault scenarios as described in Chapter 2. It also successfully meets the ride-through objectives as defined in Chapter 4. This strategy is suited for applications for which achieving a power ride-through is not required. Such applications, for example, are slurry mixers, fans etc. which can tolerate a speed reduction without any adverse effect on the process as long as a timely recovery with minimum transients and delay can be made and the control circuits kept alive.

4. Chapter 6 presents a wind energy conversion system based on a variable speed full power induction generator and a matrix converter as the power electronic interface. It tests the proposed ride-through scheme on this system and successfully meets the objectives pertaining to wind applications as defined in Chapter 2.

7.2 Suggestions for future work

To continue and further extend the work presented in this dissertation, a number of areas can be focused on as follows:

- **Experimental Test**

A laboratory prototype of an MC Drive system operating both in motoring and generating modes can be built and tested to verify the validity of the proposed system. Such a prototype is already been started on, comprising of the MC Drive system and the Voltage Sag Emulator system, the details of which are provided in Appendix A.

- **Looking at Permanent magnet generator for wind system**

PM generators are increasingly being used for wind applications. The ride-through capabilities of permanent magnet generators with matrix converters as the power electronic interface can be investigated and the proposed scheme can be modified accordingly.

- **Optimal Clamp Capacitor Design**

Since the reduced passive storage elements, mainly the elimination of bulky capacitors, form the main advantage of matrix converters as compared to back-to-back state-of-the-art topology, hence the design of an optimal clamp capacitor becomes a challenge. As the proposed scheme makes use of clamp capacitor as the storage element for enhancing the

ride-through duration, an optimal design will add to the advantages of the converter by extending the capability of this scheme to work effectively in all fault conditions.

- **Voltage Swells**

Voltage swells are another commonly occurring fault condition in the input power system and hence the ride-through capability of MC based drives for high voltage disturbances are also an important area to look at. This proposed scheme can be modified and validated for voltage swells fault condition in matrix converter based system.

- **Ride-through inherent in the normal operating mode**

The proposed ride-through scheme can be improved to include the ride-through vector as another additional switching vector during the normal modulation scheme. This means the ride-through condition would be inherent in the normal mode of operation and hence would enable a smoother transition and better ride-through profile during fault conditions.

Bibliography:

[1] J. W. Kolar, T. Friedli, F. Krismer, S. D. Round, "The Essence of Three-Phase AC/AC Converter Systems", Proceedings of the 13th Power Electronics and Motion Control Conference (EPE-PEMC'08), Poznan, Poland, pp. 27 – 42, Sept. 1 - 3, 2008.

[2] A. Alesina, M. Venturini, "Analysis and design of optimum-amplitude nine-switch direct AC-AC converters", IEEE Trans. on Pwr. Elect., Vol. 4, No. 1, pp. 101-112, Jan. 1989

[3] I. Takahashi and Y. Itoh, "Electrolytic Capacitor-Less PWM Inverter," in *Proc. IPEC*, Tokyo, Japan, April 2–6, 1990, pp. 131–138.

[4] K. Kuusela, M. Salo, and H. Tuusa, "A Current Source PWM Converter Fed Permanent Magnet Synchronous Motor Drive with Adjustable DC-Link Current," in *Proc. NORPIE*, Aalborg, Denmark, June 15–16, 2000, pp. 54–58.

[5] M. H. Bierhoff and F. W. Fuchs, "Pulse Width Modulation for Current Source Converters – A Detailed Concept," in *Proc. 32nd IEEE IECON*, Paris, France, Nov. 7–10, 2006.

[6] R. W. Erickson and O. A. Al-Naseem, "A New Family of Matrix Converters," in *Proc. 27th IEEE IECON*, Denver, CO, Nov. 29–Dec. 2, 2001, vol. 2, pp. 1515–1520.

[7] C. Klumpner and C. I. Pitic, "Hybrid Matrix Converter Topologies: An Exploration of Benefits," in *Proc. 39th IEEE PESC*, Rhodos, Greece, June 15–19, 2008, pp. 2–8.

[8] C. Klumpner, “Hybrid Direct Power Converters with Increased/Higher than Unity Voltage Transfer Ratio and Improved Robustness against Voltage Supply Disturbances,“ in *Proc. 36th IEEE PESC*, Recife, Brazil, June 12–16, 2005, pp. 2383–2389.

[9] L. Gyugyi, B. R. Pelly, “Static Power Frequency Changers - Theory,Performance, & Application,“ New York: J. Wiley, 1976.

[10] W. I. Popow, “Der zwangskommutierte Direktumrichter mit sinusf ormiger Ausgangsspannung,“ Elektrie 28, no. 4, pp. 194–196,
1974.

[11] K. K. Mohapatra and N. Mohan, “Open-End Winding Induction Motor Driven with Matrix Converter for Common-Mode Elimination,“ in *Proc. PEDES*, New Delhi, India, Dec. 12–15, 2006.

[12] M. Braun and K. Hasse, “A Direct Frequency Changer with Control of Input Reactive Power,“ in *Proc. 3rd IFAC Symp.*, Lausanne, Switzerland, 1983, pp. 187–194.

[13] D. H. Shin, G. H. Cho, and S. B. Park, “Improved PWM Method of Forced Commutated Cycloconverters,“ in *Proc. IEE*, vol. 136, pt. B, no. 3, pp. 121–126, 1989.

[14] P. D. Ziogas, Y. Kang, and V. R. Stefanovic, “Rectifier-Inverter Frequency Changers with Suppressed DC Link Components,“ *IEEE Trans. Ind. Appl.*, vol. IA-22, no. 6, pp. 1027–1036, 1986.

[15] S. Kim, S. K. Sul, and T. A. Lipo, “AC/AC Power Conversion Based on Matrix Converter Topology with Unidirectional Switches,“ *IEEE Trans. Ind. Appl.*, vol. 36, no. 1, pp. 139–145, 2000.

[16] K. G¨opfrich, C. Rebbereh, and L. Sack, “Fundamental Frequency Front End Converter (F3E),“ in *Proc. PCIM*, Nuremberg, Germany, May 20–22, 2003, pp. 59–64.

[17] B. Piepenbreier and L. Sack, “Regenerative Drive Converter with Line Frequency Switched Rectifier and Without DC Link Components,“ in *Proc. 35th IEEE PESC*, Aachen, Germany, June 20–25, 2004, pp. 3917–3923.

[18] J. Holtz and U. Boelkens, “Direct Frequency Converter with Sinusoidal Line Currents for Speed-Variable AC Motors,“ *IEEE Trans. Ind. Electron.*, vol. 36, no. 4, pp. 475–479, 1989.

[19] K. Shinohara, Y. Minari, and T. Irisa, “Analysis and Fundamental Characteristics of Induction Motor Driven by Voltage Source Inverter without DC Link Components (in Japanese),“ *IEEJ Trans.*, vol. 109-D, no. 9, pp. 637–644, 1989.

[20] L. Wei and T. A. Lipo, “A Novel Matrix Converter Topology with Simple Commutation,“ in *Proc. 36th IEEE IAS*, Chicago, IL, Sept. 30–Oct. 4, 2001, vol. 3, pp. 1749–1754.

[21] J. W. Kolar, M. Baumann, F. St¨ogerer, F. Schafmeister, and H. Ertl, “Novel Three-Phase AC-DC-AC Sparse Matrix Converter, Part I - Derivation, Basic Principle of Operation, Space Vector Modulation, Dimensioning, Part II - Experimental Analysis of the Very Sparse Matrix Converter,“ in *Proc. 17th IEEE APEC*, Dallas, TX, March 10–14, 2002, vol. 2, pp. 777–791.

[22] L. Wei, T. A. Lipo, and H. Chan, “Matrix Converter Topologies with Reduced Number of Switches,“ in *Proc. VPEC*, Blacksburg, VA, April 14–18, 2002, pp. 125–130.

[23] F. Schafmeister, “Sparse und Indirekte Matrix Konverter,“ PhD thesis no. 17428, ETH Z¨urich, 2007.

[24] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, “Novel Three-Phase AC-AC Sparse Matrix Converters,“ *Trans. Power Electron.*, vol. 22, no. 5, pp. 1649–1661, 2007.

[25] M. Y. Lee, P. Wheeler, and C. Klumpner, “A New Modulation Method for the Three-Level-Output-Stage Matrix Converter,“ in *Proc. 4th PCC*, Nagoya, Japan, April 2–5, 2007.

[26] C. Klumpner, M. Lee, and P. Wheeler, “A New Three-Level Sparse Indirect Matrix Converter,“ in *Proc. IEEE IECON*, 2006, pp. 1902–1907.

[27] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Hoboken, NJ: John Wiley & Sons, 2003.

[28] P.W Wheeler, J. Rodriguez, J.C. Clare, L. Empringham, A. Weinstein, “Matrix converters: a technology review*”, IEEE Trans. Industrial Electronics*, Vol. 49, Nr. 2, pp. 276 – 288, April 2002.

[29] Marco Matteini, “Control Techniques for Matrix Converter Adjustable Speed Drives”, PhD Thesis, University of Bologna, 2001

[30] S. Burnet, S. Ponnaluri, and R. Teichmann, “Design and Loss Comparison of Matrix Converters and Voltage Source Converters for Modern AC Drives”, *IEEE Trans. Industrial Electronics*, Vol. 49, Nr. 2, pp. 304-314, April 2002.

[31] Satish Thuta, “Simplified control of Matrix Converter and Investigation into its applications”, University of Minnesota, Dec 2007

[32] A. Alesina and M.G.B. Venturini: “Solid State Power Conversion: A Fourier Analysis Approach to Generalized Transformer Synthesis”, IEEE Transactions on Circuits and Systems, Vol. CAS-28, No.4, April 1981, pp. 319 – 330.

[33] Narayanaswamy P.R. Iyer, “Carrier Based Modulation Technique for Three phase Matrix Converters – State of the Art Progress”, IEEE Region8 SIBIRCON, Russia, July11-15, 2010

[34] N. Burany, “Safe Control of Four-Quadrant Switches,” in Conference Records of IEEE/IAS Annual Meeting, 1989, pp. 1190-1194.

[35] C.L. Neft and C.D. Schauder, “Theory and Design of a 30-Hp Matrix Converter”, in Conference Records of IEEE/IAS Annual Meeting, 1988, pp. 934-939.

[36] S. Bernet, T. Matsuo and T.A. Lipo, “A Matrix Converter Using Reverse Blocking NPTIGBT’s and Optimised Pulse Patterns,” Proceedings of IEEE/PESC’96 , Baveno, Italy, June 1996, pp. 107-113.

[37] P. Nielsen, “The matrix converter for an induction motor drive,” Industrial Ph.D. project EF493, ISBN 87-89179-14-5, 296 pages, Aalborg University, Denmark,1996.

[38] L. Huber, D. Borojevic, “Input Filter Design of Forced Commutated Cycloconverters”, Proceedings of 6th Mediterranean Electrotechnical Conference, 1991, vol.2, pp. 1356-1359.

[39] P.W. Wheeler, H. Zhang and D.A. Grant, “A theoretical and practical investigation of switching frequency harmonics in a matrix converter,” Proceedings of UPEC’93, pp. 502-505, 1993.

[40] P.W. Wheeler and D.A. Grant, "Optimised input filter design and low-loss switching techniques for a practical matrix converter," IEE Proceedings of Electric Power Applications, vol. 144, No. 1, pp. 53-60, Jan. 1997.

[41] R.D. Middlebrook, "Input filter considerations in design and application of switching regulators", Conference Records of IEEE/IAS Society Annua l Meeting, 1976, Chicago, pp. 91-107.

[42] R.D. Middlebrook and S.M. Cuk, "Design Techniques for Preventing Input Filter Oscillations in Switched-Mode Regulators", Proceeding of Powercon 5, the Fifth National Solid-State Power Electronics Conference, 1978, pp. 153-168.

[43] C. Klumpner, P. Nielsen, I. Boldea, and F. Blaabjerg, "A new matrix converter-motor (MCM) for industry applications," in Conf. Rec. IEEE-IAS Annu. Meeting, 2000, CD-ROM.

[44] J. Mahlein, M. Braun, "A Matrix Converter without Diode clamped Over-Voltage Protection," Proceedings of IEEE-IPEMC 2000, vol. 2, pp. 817-822, 2000.

[45] C. Klumpner, I. Boldea, and F. Blaabjerg, "Limited ride-through capabilities for direct frequency converters," *IEEE Trans. on Power Electronics*, vol. 16, pp. 837-845, Nov. 2001.

[46] E. P. Wiechmann, R. P Burgos, and J. Rodriguez, "Continuously motor synchronized ride-through capability for matrix-converter adjustable-speed drives," *IEEE Trans. on Industrial Electronics*, vol. 49, pp. 390 –400, April 2002.

[47] H. Cha and P. Enjeti, "A new ride-through approach for matrix converter fed adjustable speed drives", Industrial Applications Conf., pp. 2555-2560, 2002.

[48] Yang Mei, Kai Sun, Daning Zhou, Lipei Huang, and Kouki Matsuse, “Application of Matrix Converter in Auxiliary Drive System for Diesel Locomotives”, IEEE 2005.

[49] P. Wheeler, J. Clare, M Apap, L Empringham, L De Lilo, K J Bradley, C Whitley and G Towers, “Power Supply Loss Ride-Through and Device Voltage Drop Compensation in a Matrix Converter Permanent Magnet Motor Drive for an Aircraft Actuator”, IEEE Power Electronics Specialist Conference, Germany, 2004.

[50] T. F. Podlesak - U. S. Army Research Lab., “Matrix Converters for Hybrid Vehicle Applications”, Future Transportation Technology Conference & Exposition, August 1998.

[51] Rockwell Automation, “AC Drive Ride-Through Techniques”, Technical Paper, May 2002

[52] IEEE Xplore Press, 1995. IEEE recommended practice for monitoring electric power quality.

[53] International Electrotechnical Commission, 1992. IEC TR 61000-2-3 Electromagnetic Compatibility (EMC)-Part 2: Environment-section 3: Description of the environment-radiated and non-network frequency-related conducted phenomena.

[54] M. F. McGranaghan, D. R. Mueller, and M. J. Samotyj, "Voltage sags in industrial systems," *IEEE Trans. on Ind. Appl.*, vol. 29, no. 2, pp. 397-402, March/April 1993.

[55] L. Conrad, K. Little, and C. Grigg, "Predicting and preventing problems associated with remote fault-clearing voltage dips," *IEEE Trans. on Ind. Appl.*, vol. 27, no. 1, pp. 167-172, January/February 1991.

[56] J. C. Gomez, M. M. Morcos, C. Reineri, and G. Campetelli, "Behavior of induction motor due to voltage sags and short interruptions" *IEEE Trans. on Power Delivery.*, vol. 17,no. 2, pp. 434–440, April 2002.

[57] E. W. Gunther and H. Mehta, "A survey of distribution system power quality—Preliminary results," *IEEE Trans. Power Delivery*, vol. 10, pp.322–329, Jan. 1995.

[58] L. Tang, J. Lamoree, M. McGranagham, and H. Mehta, "Distribution system voltage sags: Interaction with motor and drive loads," in *Proc. IEEE Transmiss. Distribut. Conf.*, Chicago, IL, 1994, pp. 1–6.

[59] D. S. Dorr, M. B. Hughes, T. M. Gruzs, R. E. Jurewicz, and J. L. Mc-Claine, "Interpreting recent power quality surveys to define the electrical environment," *IEEE Trans. Industry Applicat.*, vol. 33, pp. 1480–1487, Nov./Dec. 1997.

[60] Order 661 A - Interconnection with Wind Energy, issued by Federal Energy Regulatory Commission (FERC) of United States, Dec 12, 2005.

[61] Bollen, M.H.J and L.D. Zhang (2003), "Different methods of classification of three phase unbalanced voltage dips due to faults." Electric Power Systems Research 66(1): 59-69.

[62] M.H.J. Bollen, P. Wang, N. Jenkins, "Analysis and consequences of the phase jump associated with a voltage sag", *Power Systems Computation Conf.,* Aug 1996, Dresden, Germany.

[63] R. Prasad, K.K. Mohapatra and Ned Mohan, "Parametric Evaluation of Ride-Through Capability of Matrix Converters using Matlab/Simulink", GCMS Conference, June 2009

[64] C. Klumpner, and F. Blaabjerg, "Experimental evaluation of ride-through capabilities for a Matrix Converter under short power interruptions ," *IEEE Trans. Ind. Applicat.*, vol. 49, No. 2, April 2002.

[65] E.P.Wiechmann, R.P.Burgos and J.Rodriguez,"Continuously motor synchronized ride-through capability for matrix converter adjustable speed drives", *IEEE Trans. Ind. Applicat.*, vol. 49, No. 2, June 2002

[66] R Langley, A Mansoor , E. R. Collins, Jr. and R.L. Morgan, "Voltage-Sag Ride-Through Testing of Adjustable-Speed-Drives using a Controllable Dynamic Dynamometer", International Conference on Harmonics and Quality of Power (ICHQP), Athens, Greece, Oct 14-16, 1998.

[67] M.H.J. Bollen, "Algorithms for characterizing three-phase unbalanced voltage dips", IEEE Transactions on Power Delivery, Vol.18, no.3 (July 2003), pp.937-944.

[68] S. Masoud Barakati, "Modeling and Controller Design of a Wind Energy Conversion System Including a Matrix Converter", PhD.Thesis, Univ. of Waterloo, 2008.

[69] Rohit Tirumala, " Simulation Study of Wind Energy Conversion Systems", M.S. Thesis, University of Minnesota, May 2000.

[70] N. Mohan, "Advanced Electric Drives: Analysis, Control and Modeling using Simulink", published by MNPERE, 2001

[71] M.M. El-Wakil, "Power Plant Technology", College Custom Series.

Appendix A

1. Laboratory prototype of Matrix Converter Drive System

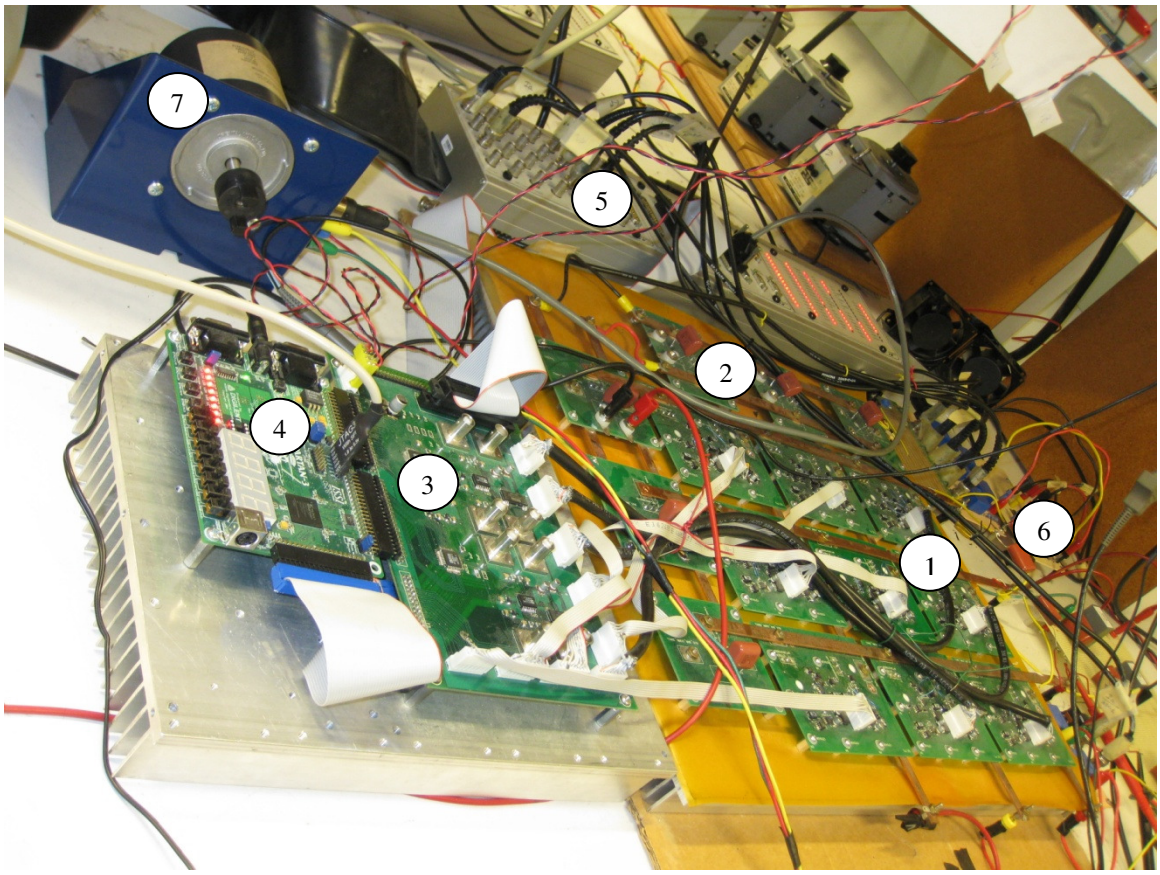


Fig 8.1 View of Hardware MC Prototype

1. 3x3 Matrix Converter
2. Clamp Circuit
3. Gate Driver Control Board
4. FPGA Board
5. Dspace Board
6. Sensor circuits
7. Induction Motor

FPGA Code for the above Lab MC Prototype

```
   1. `timescale 1ps / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company: University of Minnesota
// Engineer: Rashmi Prasad
// Create Date:    05/19/2009
// Design Name:
// Module Name:    interface_board
// Project Name:
// Description: main module
// Revision:
// Revision 0.01 - File Created
//////////////////////////////////////////////////////////////////////////////////
////////////

module interface_board(F_OUT, PW_OUT, RESET, CLK, P_IN, F_IN,
PWM_STOP);

input RESET;            //reset
input CLK;              // clock signal
input [5:0] P_IN;
input [17:0] F_IN;
input PWM_STOP;

output [17:0] PW_OUT;
output [1:0] F_OUT;

wire [5:0] P_SYNC; //synchronized pwm's
wire [17:0] P_OUT;
wire [17:0] PWM_OUT;
wire CLK_DIV;
wire CLK_DT;
wire EN;

clock_divider CLKD(CLK_DIV, CLK, RESET);
Delay_PWM D1(P_SYNC, CLK_DIV, RESET, P_IN);
clock_div_deadtime CLKDT(CLK_DT, CLK, RESET);

//PWM Signals after Dead-Time
DeadTime_Delay PWM1(PWM_OUT[0], CLK_DT, RESET, P_OUT[0]);
DeadTime_Delay PWM2(PWM_OUT[1], CLK_DT, RESET, P_OUT[1]);
DeadTime_Delay PWM3(PWM_OUT[2], CLK_DT, RESET, P_OUT[2]);
DeadTime_Delay PWM4(PWM_OUT[3], CLK_DT, RESET, P_OUT[3]);
DeadTime_Delay PWM5(PWM_OUT[4], CLK_DT, RESET, P_OUT[4]);
DeadTime_Delay PWM6(PWM_OUT[5], CLK_DT, RESET, P_OUT[5]);
DeadTime_Delay PWM7(PWM_OUT[6], CLK_DT, RESET, P_OUT[6]);
```

```
DeadTime_Delay PWM8(PWM_OUT[7], CLK_DT, RESET, P_OUT[7]);
DeadTime_Delay PWM9(PWM_OUT[8], CLK_DT, RESET, P_OUT[8]);
DeadTime_Delay PWM10(PWM_OUT[9], CLK_DT, RESET, P_OUT[9]);
DeadTime_Delay PWM11(PWM_OUT[10], CLK_DT, RESET, P_OUT[10]);
DeadTime_Delay PWM12(PWM_OUT[11], CLK_DT, RESET, P_OUT[11]);
DeadTime_Delay PWM13(PWM_OUT[12], CLK_DT, RESET, P_OUT[12]);
DeadTime_Delay PWM14(PWM_OUT[13], CLK_DT, RESET, P_OUT[13]);
DeadTime_Delay PWM15(PWM_OUT[14], CLK_DT, RESET, P_OUT[14]);
DeadTime_Delay PWM16(PWM_OUT[15], CLK_DT, RESET, P_OUT[15]);
DeadTime_Delay PWM17(PWM_OUT[16], CLK_DT, RESET, P_OUT[16]);
DeadTime_Delay PWM18(PWM_OUT[17], CLK_DT, RESET, P_OUT[17]);


// assign pwm outputs for output phase-A
assign P_OUT[0] = ((~P_IN[0])& (~P_SYNC[1]) & (EN));
assign P_OUT[1] = P_OUT[0];
assign P_OUT[2] = ((~P_IN[0])& (P_SYNC[1]) & (EN));
assign P_OUT[3] = P_OUT[2];
assign P_OUT[4] = ((P_IN[0])& (P_SYNC[1]) & (EN));
assign P_OUT[5] = P_OUT[4];

// assign pwm outputs for output phase-B
assign P_OUT[6] = ((~P_IN[2])& (~P_SYNC[3]) & (EN));
assign P_OUT[7] = P_OUT[6];
assign P_OUT[8] = ((~P_IN[2])& (P_SYNC[3]) & (EN));
assign P_OUT[9] = P_OUT[8];
assign P_OUT[10] = ((P_IN[2])& (P_SYNC[3]) & (EN));
assign P_OUT[11] = P_OUT[10];

// assign pwm outputs for output phase-C
assign P_OUT[12] = ((~P_IN[4])& (~P_SYNC[5]) & (EN));
assign P_OUT[13] = P_OUT[12];
assign P_OUT[14] = ((~P_IN[4])& (P_SYNC[5]) & (EN));
assign P_OUT[15] = P_OUT[14];
assign P_OUT[16] = ((P_IN[4])& (P_SYNC[5]) & (EN));
assign P_OUT[17] = P_OUT[16];

//fault logic

assign F_OUT[0] = ~(F_IN[0] & F_IN[2] & F_IN[3] & F_IN[4] & F_IN[5]);
assign F_OUT[1] = (~(F_IN[6] & F_IN[7] & F_IN[8] & F_IN[9] & F_IN[10] &
F_IN[11]))| (~(F_IN[12] & F_IN[13] & F_IN[14] & F_IN[15] & F_IN[16] &
F_IN[17]));
//assign F_OUT[2] = ~(F_IN[12] & F_IN[13] & F_IN[14] & F_IN[15] &
F_IN[16] & F_IN[17]);
//assign fault = ~(F_OUT[0] | F_OUT[1] | F_OUT[2]);

assign EN = PWM_STOP;
//assign EN = 1'b1;

assign PW_OUT[0] = PWM_OUT[0];
assign PW_OUT[1] = PWM_OUT[1];
assign PW_OUT[2] = PWM_OUT[2];
assign PW_OUT[3] = PWM_OUT[3];
```

```
assign PW_OUT[4] = PWM_OUT[4];
assign PW_OUT[5] = PWM_OUT[5];

assign PW_OUT[6] = PWM_OUT[6];
assign PW_OUT[7] = PWM_OUT[7];
assign PW_OUT[8] = PWM_OUT[8];
assign PW_OUT[9] = PWM_OUT[9];
assign PW_OUT[10] = PWM_OUT[10];
assign PW_OUT[11] = PWM_OUT[11];

assign PW_OUT[12] = PWM_OUT[12];
assign PW_OUT[13] = PWM_OUT[13];
assign PW_OUT[14] = PWM_OUT[14];
assign PW_OUT[15] = PWM_OUT[15];
assign PW_OUT[16] = PWM_OUT[16];
assign PW_OUT[17] = PWM_OUT[17];

endmodule


   2. `timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company:       University of Minnesota
// Engineer: Rashmi Prasad
// Create Date:    05/19/2009
// Design Name:
// Module Name:    clock_div_deadtime
// Project Name:   Delay Circuit for DSPACE PWM Signals
// Description:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
////////////

`define COUNT_DT 2
module clock_div_deadtime(CLK_DT, CLK, RESET);

input CLK;
input RESET;

output CLK_DT;

reg Q;
reg [5:0] count;

always @ (posedge CLK or posedge RESET) begin

if (RESET == 1) begin
      count = 0;
      Q = 0;
```

```
end //if
else if (count == `COUNT_DT) begin
            count = 0;
            Q = ~Q;
end //if
else
      count = count + 1;
end // always

assign CLK_DT = Q;
```

endmodule

```
   3. `timescale 1ps / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company: University of Minnesota
// Engineer: Rashmi Prasad
// Create Date:    05/19/2009
// Design Name:
// Module Name:    clock_divider
// Project Name:   Delay Circuit for DSPACE PWM Signals
// Description:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//////////////////////////////////////////////////////////////////////////////////
////////////

`define COUNTER 16
module clock_divider(CLK_DIV, CLK, RESET);

input CLK;
input RESET;

output CLK_DIV;

reg Q;
reg [4:0] count;

always @ (posedge CLK or posedge RESET) begin

if (RESET == 1) begin
      count = 0;
      Q = 0;
end //if
else if (count == `COUNTER) begin
            count = 0;
            Q = ~Q;
end //if
```

```
else
      count = count + 1;
end // always

assign CLK_DIV = Q;

endmodule


   4. timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company:             University of Minnesota
// Engineer:            Rashmi Prasad
// Create Date:    05/19/2009
// Module Name:    DeadTime_Delay
// Project Name:   Delay Circuit for DSPACE PWM Signals
// Description:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
////////////
`define DELAY_DT 1

module DeadTime_Delay(OUT, CLK, RESET, IN);

input CLK;
input RESET;
input IN;

output OUT;
reg [`DELAY_DT-1 : 0] PWM_D;

always @(posedge CLK) begin

if (RESET == 1) begin
      PWM_D = 0;
end

else
PWM_D = ({IN, PWM_D} >> 1);
end //always

assign OUT = (PWM_D[0] & IN);

endmodule
```

```
   5. `timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company:  University of Minnesota
// Engineer: Rashmi Prasad
// Create Date:    05/19/2009
// Design Name:
// Module Name:    Delay_PWM
// Project Name:  Delay_Dspace
// Description: For synchronizing the signals
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
////////////
module Delay_PWM(PWM_OUT, CLK, RESET, PWM_IN);

input [5:0] PWM_IN;
input CLK;
input RESET;

output [5:0] PWM_OUT;

//reg [5:0] PW_OUT;

shift_reg PWM1(PWM_OUT[1], CLK, RESET, PWM_IN[1]);
shift_reg PWM2(PWM_OUT[3], CLK, RESET, PWM_IN[3]);
shift_reg PWM3(PWM_OUT[5], CLK, RESET, PWM_IN[5]);

/*
always @(posedge CLK) begin

PW_OUT[0] = PWM_IN[0];
PW_OUT[1] = PWM_IN[2];
PW_OUT[2] = PWM_IN[4];

end
*/

assign PWM_OUT[0] = PWM_IN[0];
assign PWM_OUT[2] = PWM_IN[2];
assign PWM_OUT[4] = PWM_IN[4];

endmodule
```

```
   6. `timescale 1ps / 1ps
//////////////////////////////////////////////////////////////////////////////////
////////////
// Company: University of Minnesota
// Engineer: Rashmi Prasad
// Create Date:    05/19/2009
// Design Name:
// Module Name:  shift_reg
// Project Name: Delay_Dspace
// Description:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//////////////////////////////////////////////////////////////////////////////////
////////////

`define DELAY_DTC 137
//`define DELAY_PWM_10K 211 //10KHz Switching Frequency
`define DELAY_PWM_10K 137 //10KHz Switching Frequency for Unbalance
Method-I
`define DELAY_PWM_5K 64  //5KHz Switching Frequency
`define DELAY_PWM_1K 359  //5KHz Switching Frequency

module shift_reg(OUT, CLK, RESET, IN);
input CLK;
input RESET;
input IN;

output OUT;
//reg OUT;

reg [`DELAY_PWM_10K : 0] PWM;

always @(posedge CLK) begin

if (RESET == 1) begin
      PWM = 0;
end
else
      PWM = ({IN, PWM} >> 1);
   //OUT = PWM[0];
end

assign OUT = PWM[0];

endmodule
```

2. Voltage Sag Emulator System

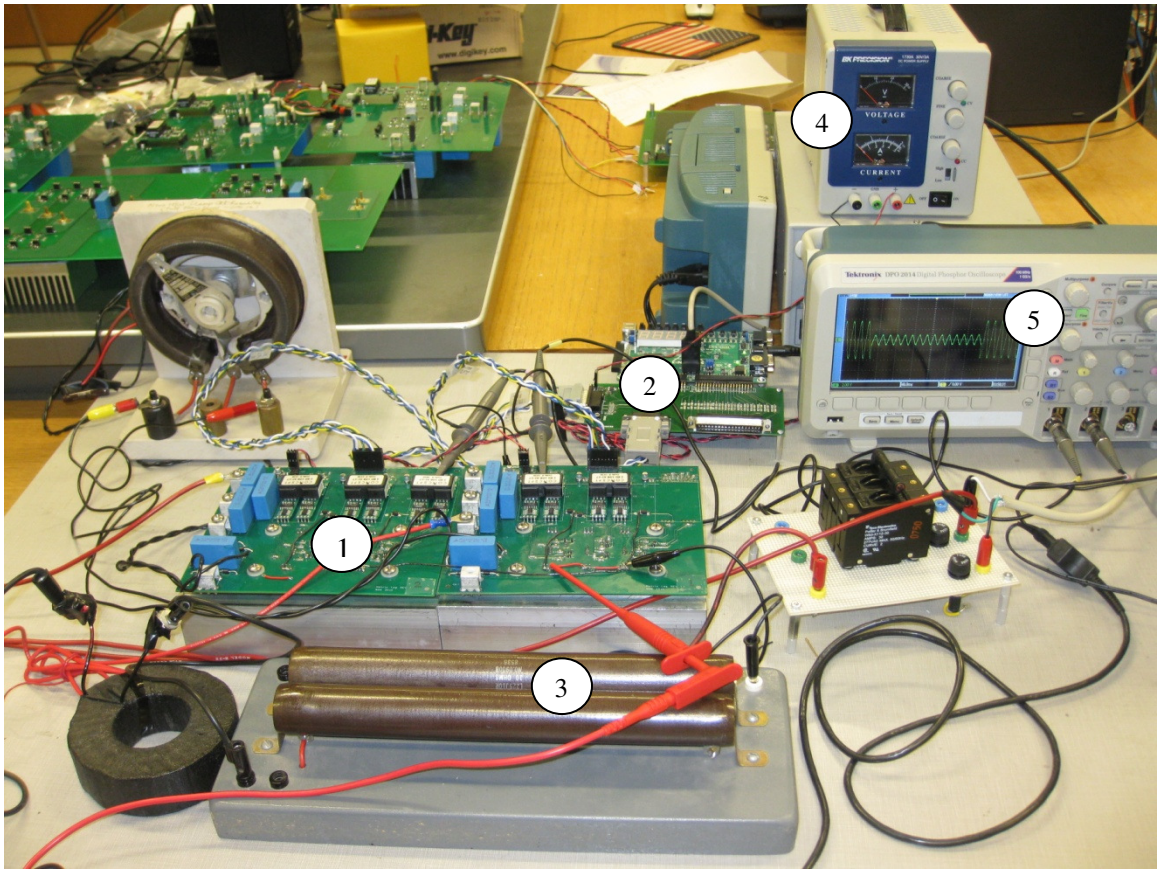


Fig 8.2 Voltage Sag Emulator Hardware Prototype

1. IGBT Switches
2. FPGA + Interface Card
3. R-L Load
4. Power Supply
5. Oscilloscope

This piece of hardware has been built to provide grid disturbances to the MC Drive System. Thus by emulating different kinds of balanced and unbalanced voltage

magnitude sags, it is able to behave like the grid and hence eliminates the need for the purchase of an expensive programmable power supply.

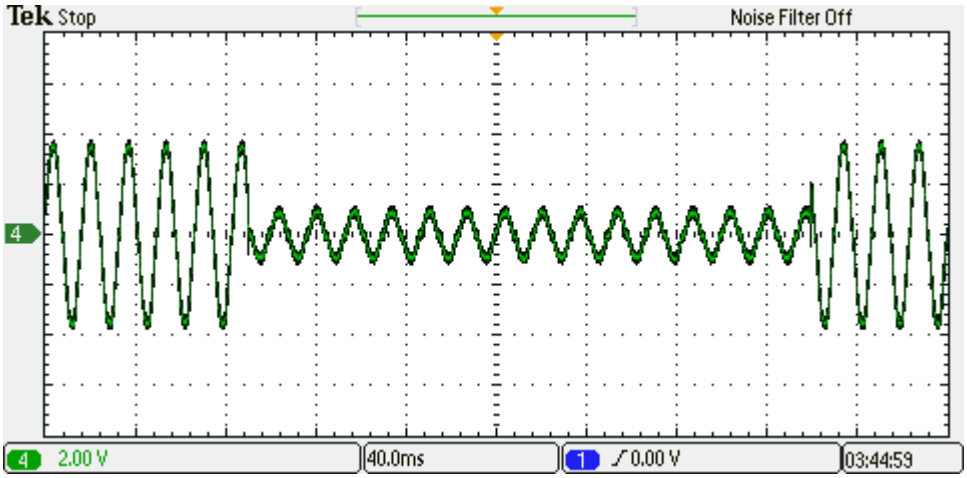


Fig. 8.3 Single Phase Sag Emulated by the above hardware prototype

The above waveform shows one kind of unbalanced sag (single phase sag) seen by the input of the MC drive System.