Development and Evaluation of a Place and Route Flow using Virtuoso-GXL layout tool Suite

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Dedication

This thesis is dedicated to my family and I am thankful to them for their support.

Abstract

In this work, the automatic placement and routing tools from Cadence Virtuoso(R)-GXL layout tool suite have been used to create a flow to allow automatic placement and routing of small to medium sized blocks using schematic or verilog gate-level netlist as input, for aiding the design of testchips. The flow has also been tried on a larger design and timing results are compared with results from a commercial P&R tool-Cadence Encounter(R) Digital Implementation System.

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Introduction

Automatic Place & Route tools are available from different EDA vendors in the semiconductor industry today, and have matured significantly to meet its requirements of design closure. However the infrastructure for setting up these tools, including input files required by them is very complex and requires considerable manual effort before they can be actually deployed on any design. The design of testchip layout is still predominantly manual using Cadence Virtuoso(R)-Layout tool. The idea behind this work is to automate the layout of small logic blocks and their integration in the design of the testchip. The *Custom Digital Placer* and *Chip Assembly Router* from the Cadence Virtuoso(R)-Layout-GXL tool suite can be used to perform automatic placement and routing respectively, using the schematic or gate-level verilog netlist as input to the flow.

1. Placement Flow

The *Virtuoso Custom Digital Placer* can be used to perform a simple row-based placement of standard cell based designs. There are 2 styles of placement available as part of this tool:

Assisted CMOS Placement Style [1]*:* This placement style has different rows for NMOS and PMOS devices, and the number of these rows should be equal.

Assisted Standard-Cell Placement Style [1]: This placement style which has been used for this work, does standard cell based row placement, where standard cells are logic gates with a defined cell height. It also allows placement of bigger blocks which are a multiple of the standard cell height. These 2 placement styles can also be mixed [1].

1.1 Pre-requisites for Assisted Standard-Cell Placement

There are certain steps that need to be followed before running the actual placement tool. These are required to get a relatively clean layout from the placement process. The sequence of steps required is as follows:

- Ensure that individual standard cells are placement ready – this primarily means that they should be able to able to abut with any other cell in the design without violating DRC rules for the technology.
- The width of the VDD/GND power rails needs to trimmed to half the desired width i.e. use a value of 0.12um if the desired power rail width is 0.24u. This is to allow overlap of power rails between adjacent rows as is standard practice in our designs.
- All standard cells in the library should share a uniform orientation – vertical for horizontal placement rows. Make sure that the lower left corner of the standard cell is aligned with the origin in the layout editor window.

- All standard cells need to use standard vdd/gnd symbols to allow proper identification of vdd!/gnd! rails in the flow.
- The standard cells should not have their own PR-boundary layers, as this interferes with proper placement of the cells in rows.

1.2 Generate the initial layout for the cells from schematic

This step involves the invocation of Virtuoso(R)-Layout-GXL from the schematic to be placed, using

Launch->Layout GXL menu.

Use the following Skill command in the main Virtuoso command window in order to preserve the orientation of standard cells that will be generated using the subsequent step

envSetVal("layoutXL" "lxGenerationOrientation" 'string "R0")

The first step is to define standard cells to be used in placement using the

Configure Physical Hierarchy Editing Menu – Launch-> Configure Physical Hierarchy..

The following menu will appear.

Select the *Component Types* option from this menu. In the “Cells” section right-click and create a component type with the “Add Component Type” and name it. Then expand the cells under “No Component Type” and move cells to the newly created component type by selecting all cells and using “Move cells” to the new ‘component type’. In the ‘Attributes’ section for the new “Component type” change the “Component class” to **STDCELL**. Save changes and close this window.

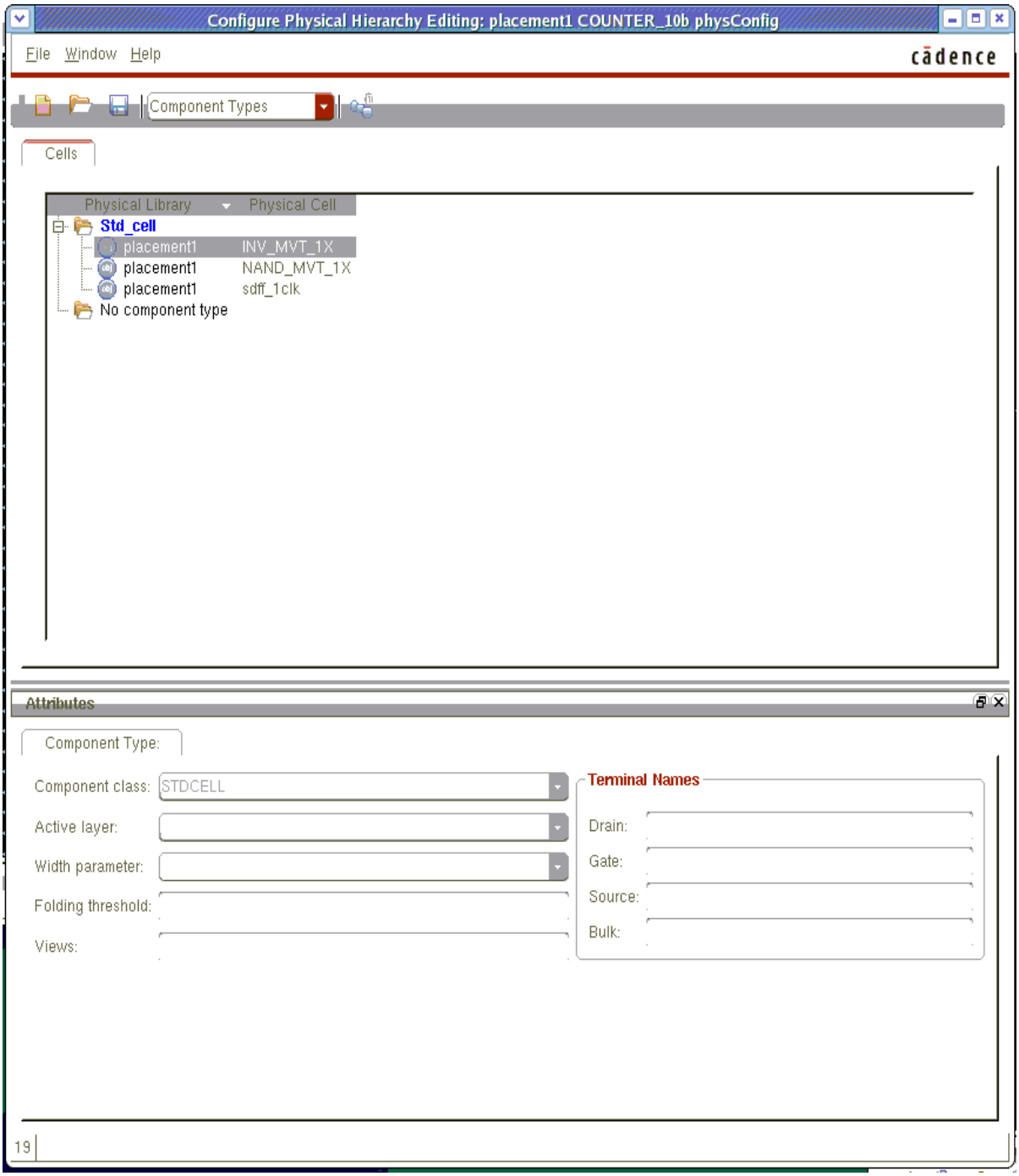


Fig 1. Standard cell Component type addition

Next, click connectivity->Generate->All from source. The following menu appears. The *Boundary Area Estimation* section can be used to define the dimensions or the aspect ratio of the placement region.

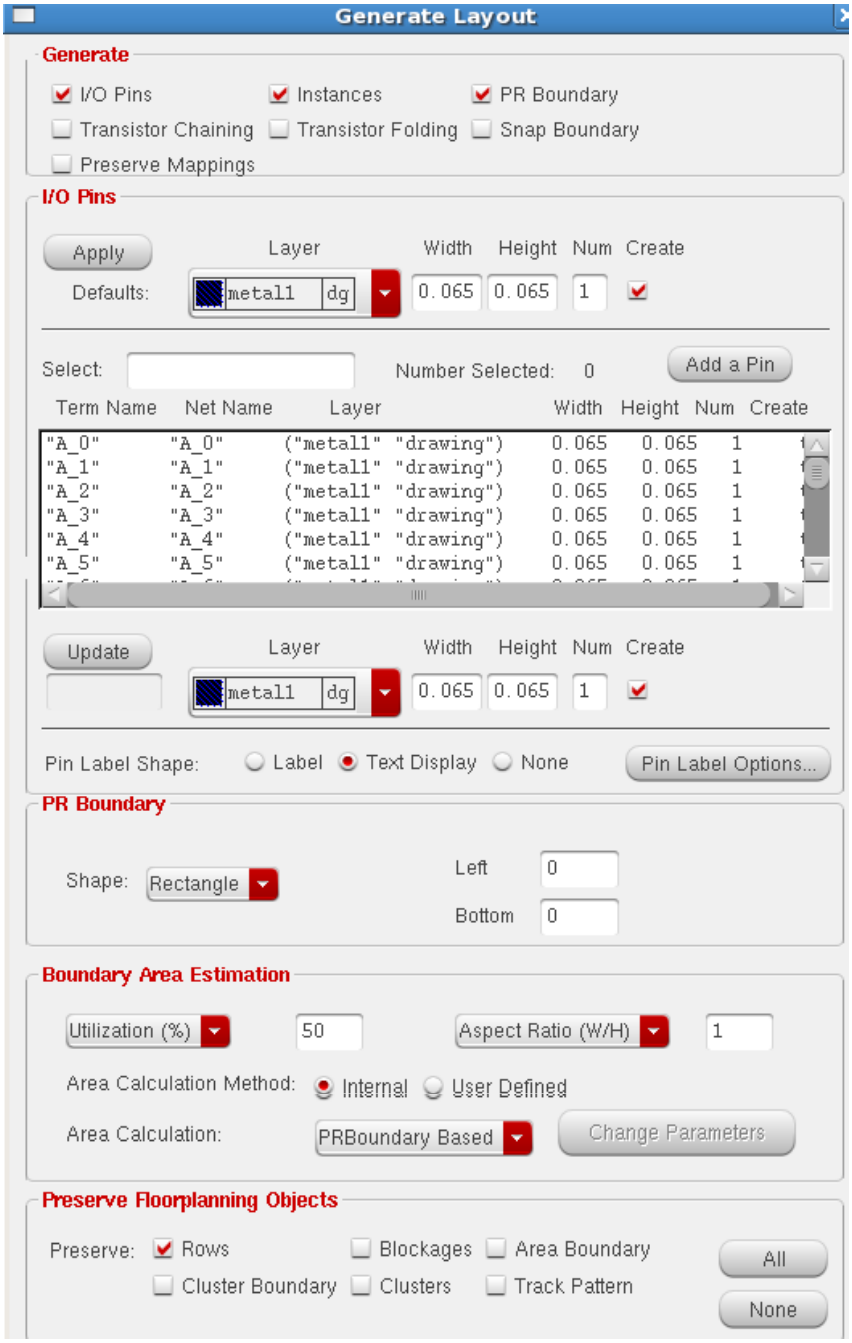


Fig 2. Layout Generation From Schematics – *Generate layout* menu

1.3 Running Virtuoso Custom Digital Placer

The following is a sequence of steps to run the *Virtuoso Custom Digital Placer*:

- Select the “Custom Digital Placer” using the menu->Windows->Assistants-> Task Assistant, and checking on “Custom Digital Placer”. The “Placement Planning” and the “Digital Placer” icons should show up at the bottom of the layout XL window.
- Invoke the “Placement Planning” menu by clicking on the icon. Select the “Assisted Standard-Cell” using the “Style” dropdown menu. There are multiple tabs that need to be configured here to guide placement.
    - In the “Regions” tab, check the “Allow for Pins” to allow pin placement outside the rows and “Allow Rows beyond regions” to allow expansion of rows for initial iterations of placement.
    - In the “Rows” tab set the “Utilization Inside Rows” to 100% to fully utilize row area for cells. Also check the “% Area Covered By Rows” and select “Specify” and set it to 0. This is again to allow overlap of VDD/GND power rails in adjacent rows. We will update the section about “Use Filler Cells” and “Use Substrate Contacts” at a later point, but for now we will add these manually.
    - In the “Rails” tab select the metal layers used for routing the vdd!/gnd! rails(typically metal1). Name the rails as **vdd!** and **gnd!**. Enter the half-width for both rails in the “Width” fields as explained earlier, in order to allow overlap of VDD/GND power rails. Select the G-P-P-G in the “Pattern” field and enter the cell height (centre-centre distance between power rails) in the “Rail To Rail Spacing” field.

- Click on “Calculate Rows” to see the placement rows created by the tool.

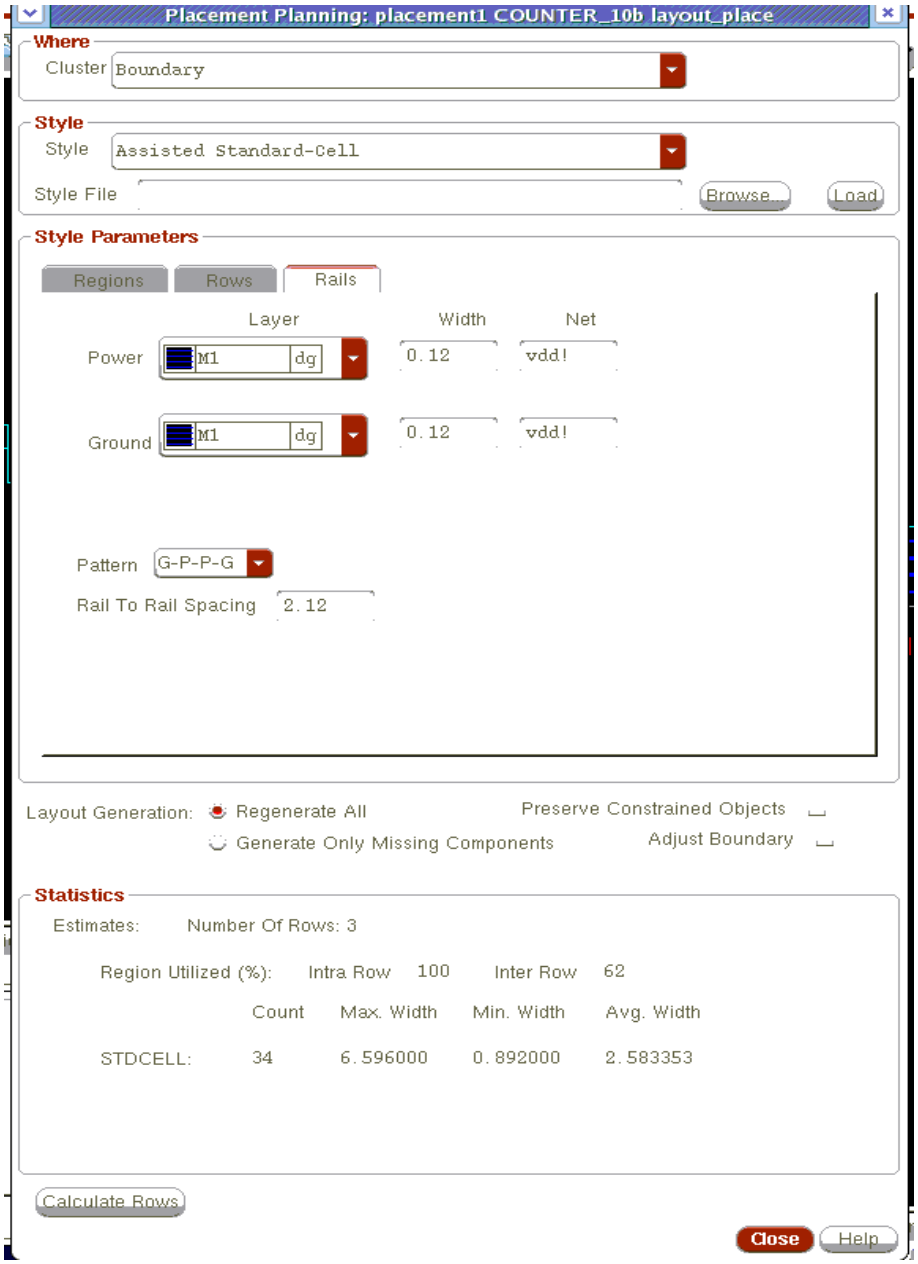


Fig 3. Virtuoso Custom Digital Placer – Placement Planning window

- Invoke the placer by clicking on the “Digital Placer” icon. Check only the following options:
    - Allow Rotation

- Global Placement
- Optimize Placement – you can use different “Runtime” options depending on the size of the design and runtime requirements.
- Do not check any of the “Spacer” options. Click OK to run the placer.

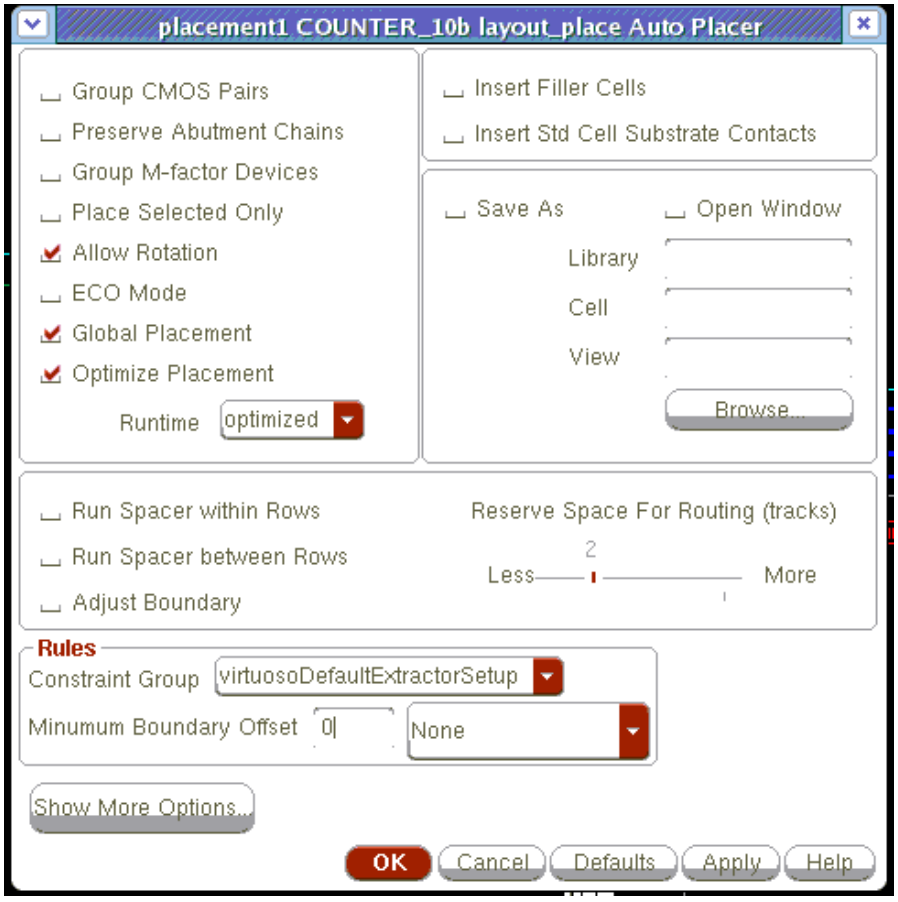


Fig 4. Virtuoso Custom Digital Placer – Auto Placer window

The procedure for hierarchical placement of pre-placed is quite similar to placement for individual blocks. The same pre-requisite steps need to be done on the pre-placed blocks to be placed to form bigger blocks. **Figure 5** shows an example with 2 10-bit counters and a NAND gate after placement.

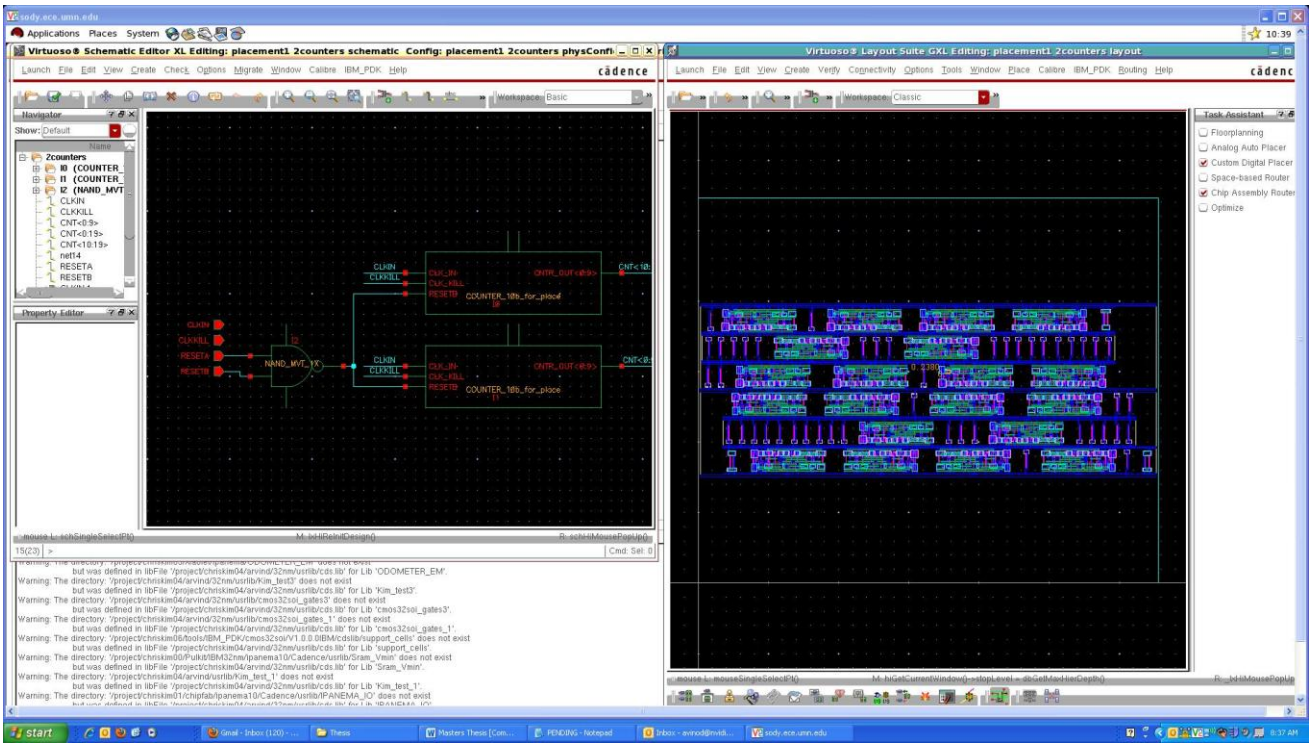


Fig 5. Virtuoso Custom Digital Placer – Hierarchical placement

2. Routing Flow

The *Virtuoso Chip Assembly Route* is the tool used for global and detailed routing in Virtuoso. The sequence of steps for running the router is as follows:

- Select the router using the *Windows->Assistants-> Task Assistant*, and checking on "Chip Assembly Router". The *Start Router* icon should show up at the bottom of the layout XL window. Invoke the router by clicking on the icon.
- Invoke the *Pin Escape* menu using *Autoroute->Pre route->Pin Escape.* The pin_escape command is a preroute command that routes a short wire from a via to a pin [2].
- Next invoke the global router using *Autoroute->Global Route->Global Route.* Run the global router for at least 25 passes on a large design.
- Following this the detailed router is invoked using *Autoroute->Detail Route ->Detail Router.* Run it for a sufficient number of passes in order to get a 100% routed design.
- In order to remove U-shaped notches formed by metal layer for the same net, run *Autoroute->Post Route->Remove Notches*

For smaller blocks it is preferable to have pins in M2 or above since the router finds it difficult to route M1 due to extensive use inside the standard cells.

If pins need to be placed manually they should be un-checked in the *Generate Layout* menu prior to placement, and then routed manually, after running the router to route internal nets.

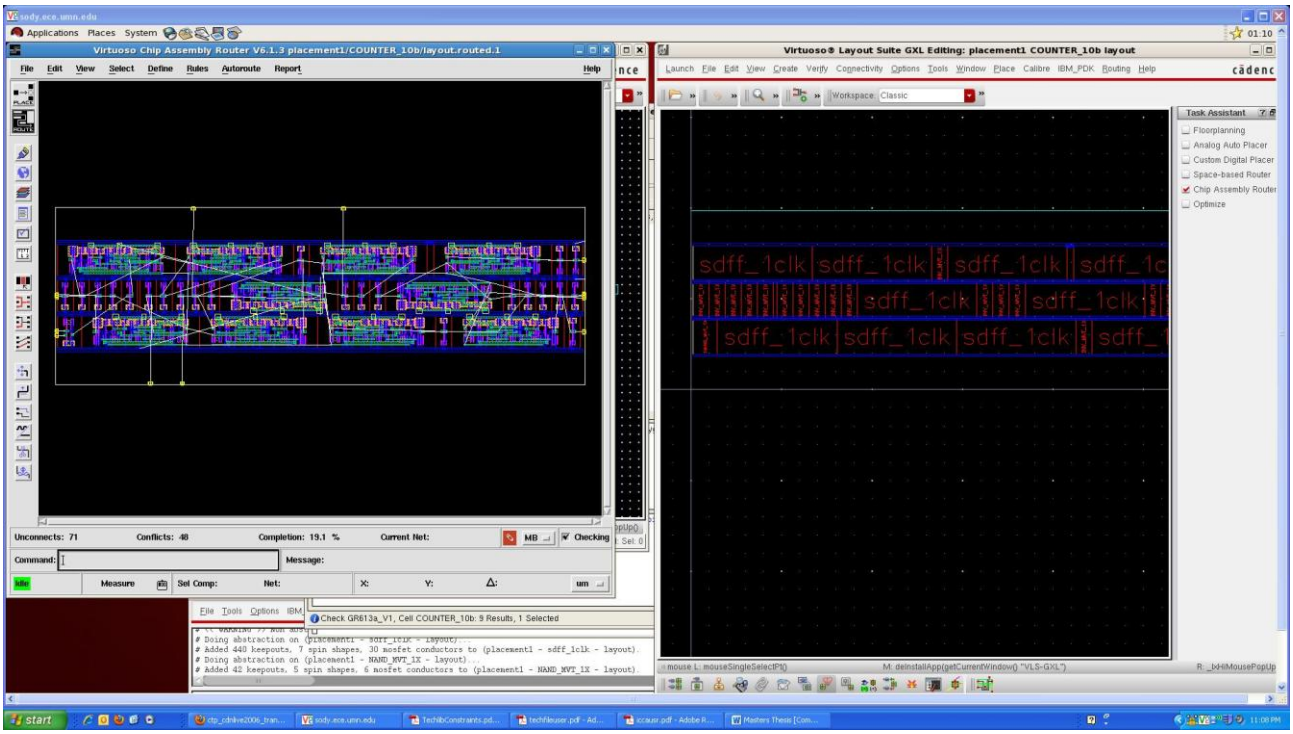


Fig 6. Virtuoso Chip Assembly Router window

2.1 Technology File Modification for Routing

The technology library can be modified to guide the router to improve DRC cleanliness, via placement of the routed design [5][6]. For the Open Access library format (used by Cadence version IC61*), different sections of the technology library database can be dumped using the *Technology Tool Box*, which can be invoked from *Tools->Technology File Manager* from the main Virtuoso command window.

As seen in **Figure 7** different sections of the technology file can be written using the

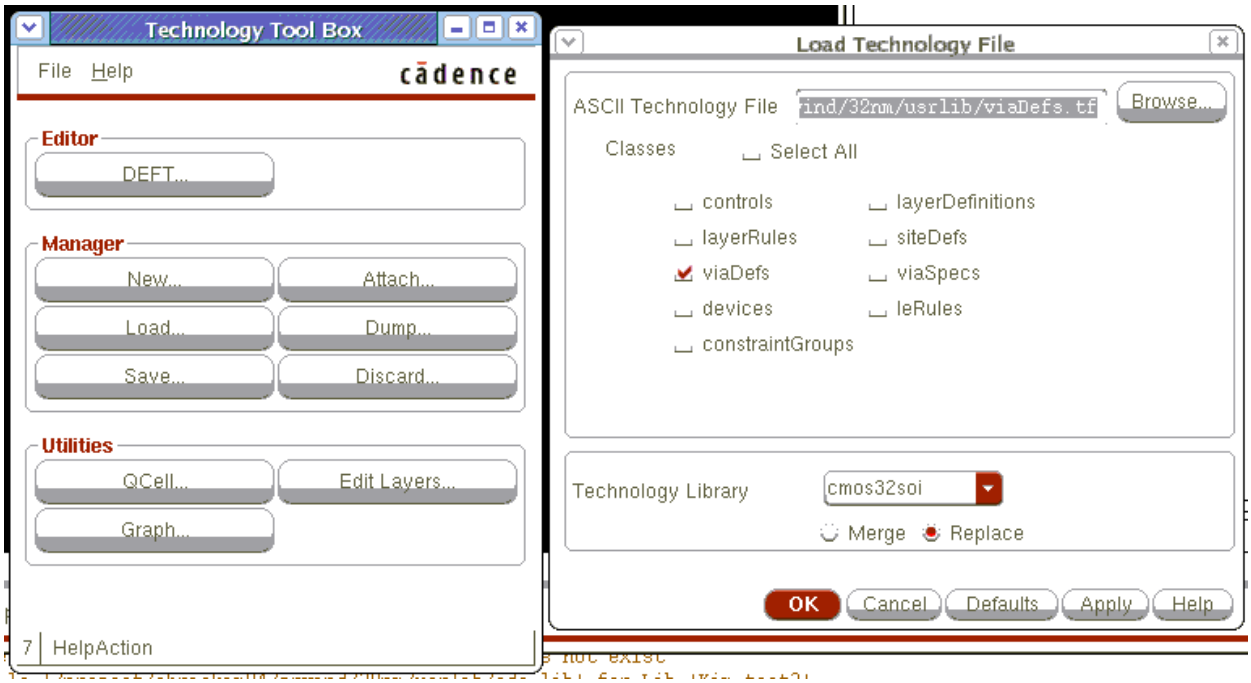


Fig 7. Virtuoso Technology Tool Box – loading changes to technology file

Dump option and loaded selectively into virtual memory using the *Load* option. The technology library for the given PDK should be selected in the *Technology Library* field.

The following is a brief description of different sections of the technology file [6]:

Controls (controls) specify data that can be used throughout the technology file and also specify references to other technology libraries.

Layer definitions (layerDefinitions) define the layers that can be used to define data throughout the technology file or by other technology databases in design sessions.

Layer rules (layerRules) specify layer attributes, such as layer materials, manufacturing grid resolutions, and current densities.

Constraint groups (constraintGroups) specify design constraints.

Site definitions (siteDefs) define scalar site definitions and arrays of scalar site

definitions.

Via definitions (viaDefs) define standard and custom vias.

Via specifications (viaSpecs) define arrays of via definitions.

Devices (devices) define Cadence-predefined MOS and ruleContact devices andmultipart path templates.

The *constraintGroups* section of the technology file can be used to control the following

- The metal layers which get used for routing, by listing the metals used to route in the *validlayer* section:

```
( "virtuosoDefaultSetup" nil
; layer constraints
interconnect(
( validLayers   (M1  M2  M3  M4   ) )
( validVias     (M2_M1 M2_M1_via  M2_M1_viaB  M2_M1_viaC M3_M2 M3_M2_via M3_M2_viaB
M3_M2_viaC M4_M3 M4_M3_via   M4_M3_viaB  ) )
);interconnect
);virtuosoDefaultSetup
```

- Using the *spacingTables* section, spacing between metal routes of the same layer can be controlled based on the width and length of the metal route [6]:

```
constraintGroups(
("foundry"
spacingTables(
;( constraint layer1
; (( index1Definitions index2Defintions) defaultValue)
; ( table) )
;( ------------------------------------------)
( minSpacing "Metal1"
(( "width" nil nil "length" nil nil ) )
(
(0.0 0.0 ) 0.12
(0.0 0.56 ) 0.12
(0.0 1.5 ) 0.12
(0.0 3.0 ) 0.12
(0.1805 1.5 ) 0.18
(0.1805 3.0 ) 0.18
(1.5005 1.5 ) 0.5
 (3.0005 1.5 ) 0.5
(3.0005 3.0 ) 0.9
```

```
)    )
) ;spacingTablesmetal table spacing
```

The *viaDefs* section of the technology file can be used to control the metal enclosure of vias:

```
viaDefs(
 standardViaDefs(
 ;( viaDefName  layer1  layer2  (cutLayer cutWidth cutHeight [resistancePerCut])
 ;   (cutRows   cutCol  (cutSpace))
 ;   (layer1Enc) (layer2Enc)    (layer1Offset)  (layer2Offset)  (origOffset)
 ;   [implant1   (implant1Enc)  [implant2       (implant2Enc) [well/substrate]]])
 ;( ---------------------------------------------------------------------------- )
  ( VSPC_M1            PC         M1               ("CA" 0.04 0.04 0.7)
    (1 1 (0.064 0.064))
    (0.0 0.0)  (0.0 0.0)      (0.0 0.0)      (0.0 0.0)      (0.0 0.0)
  )
  ( VSRX_M1            RX         M1               ("CA" 0.04 0.04)
    (1 1 (0.064 0.064))
    (0.0 0.0)  (0.0 0.0)      (0.0 0.0)      (0.0 0.0)      (0.0 0.0)
  )
  ( VSM1_M2            M1         M2               ("V1" 0.05 0.05)
    (1 1 (0.08 0.08))
    (0.017 0.0)       (0.017 0.0)    (0.0 0.0)      (0.0 0.0)      (0.0 0.0)
  )
 ) ;standardViaDefs
) ;viaDefs
```

Note that these are just a few examples of how the routing process can be controlled using the technology file. Also in order for these changes to take effect the relevant section should be *loaded* using the ***Merge*** option in the *Technology Tool Box.*

Other parameters which are defined in the *foundry* section of the *constraintgroups* which can be useful to control the router are as follows:

```
spacings(
    ( minSpacing              "RX"     0.10 )
    ( minSpacing              "V1"     0.10 )
    ( minSpacing              "PC"     "CA"              0.010 )
    ( minSameNetSpacing       "RX"          0.10 )
    ( minSameNetSpacing       "M1"          0.10 )
    ( minSameNetSpacing       "M2"          0.10 )
    ( minSameNetSpacing       "M3"          0.10 )
    ( minSameNetSpacing       "CA"          "V1"              0.0 )
    ( minSameNetSpacing       "V1"          "V2"              0.0 )
    ( minWidth              "M1"     0.10 )
    ( minWidth              "CA"     0.10 )
    ( minWidth              "V1"     0.10 )
    ( maxWidth              "M1"     2.00 )
    ( minArea               "M1"     0.10 )
    ( minArea               "M2"     0.10 )
    ( minArea               "M3"     0.10 )
    ( minViaSpacing           "V1"   0.10 )
    ( minViaSpacing           "V2"   0.10 )
    ( viaSpacing            "CA"     (3 0.20 0.20) )
    ( viaSpacing            "V1"     (3 0.20 0.20) )
    ( viaSpacing            "V2"     (3 0.20 0.20) )
   ) ;spacings
```

A minimum spacing - *minSameNetspacing* must be maintained between two electrically equivalent shapes (typically, the “notches” in wires that are created by some tools). If this minimum cannot be met, the notch space must be filled [5]. *minSameNetspacing* should be used only when it is less than the MinSpacing.

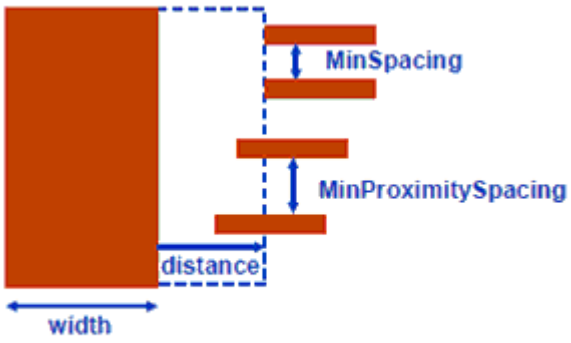


Fig 8.a minSameNetSpacing

Fig 8.b MinProximitySpacing

Proximity rules are used to set perpendicular wire spacing close to wide wires, as shown in **Figure 8.b** [5]. This can be set directly from the router using the following command:

rule layer M1 (proximity on (influence (width 5.0 within 1.0 clear 1.0) (width 7.5 within 2.5 clear 2.5))

Figure 9 shows DRC violations for a 10-bit counter layout, that can be fixed by editing the technology file. **Table 1** provides a summary of the sections of the technology file that need to be changed. Note that these changes may result in a slightly higher area, but that usually is not a major concern for testchips. The tradeoff lies in relatively DRC clean layout from the router.

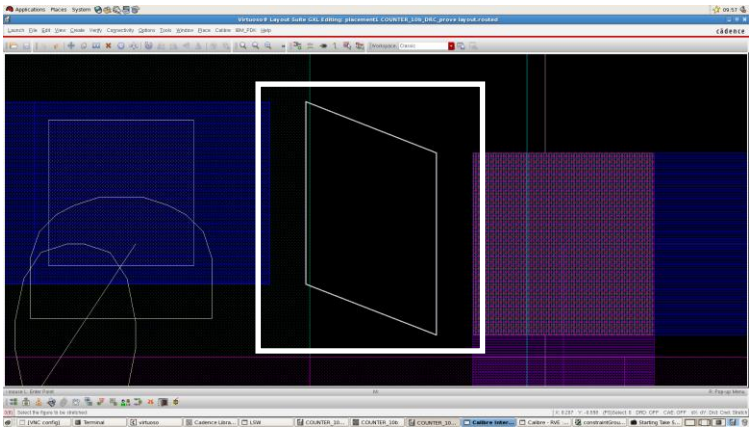


Fig 9.a. Metal1 violating minimum spacing DRC

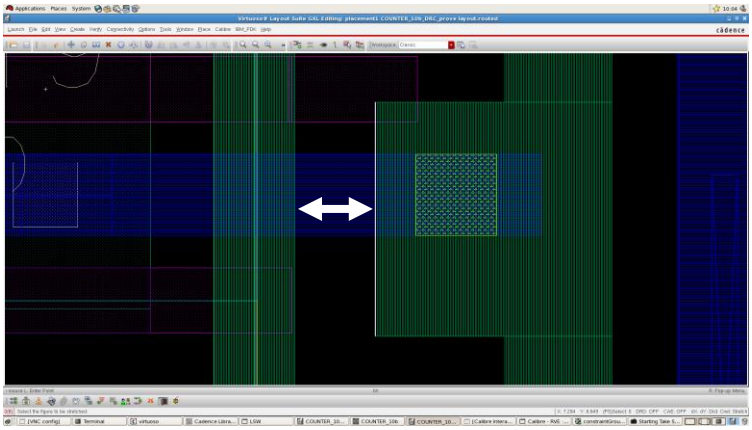


Fig 9.b. Metal2 violating minimum spacing DRC

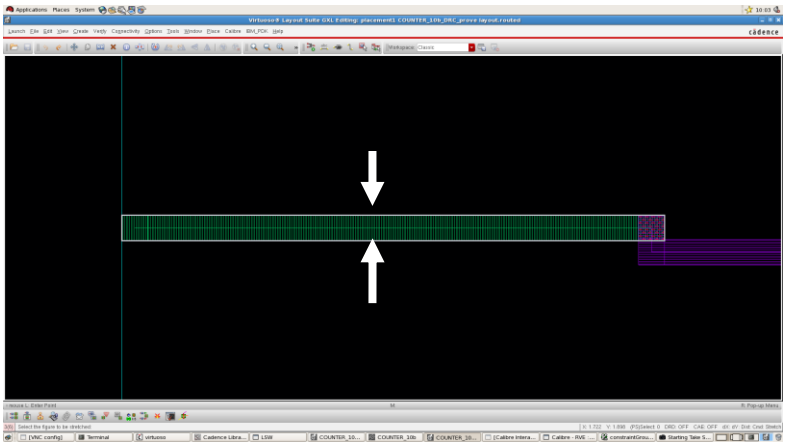


Fig 9.c. Metal violating minimum width DRC in 1 direction

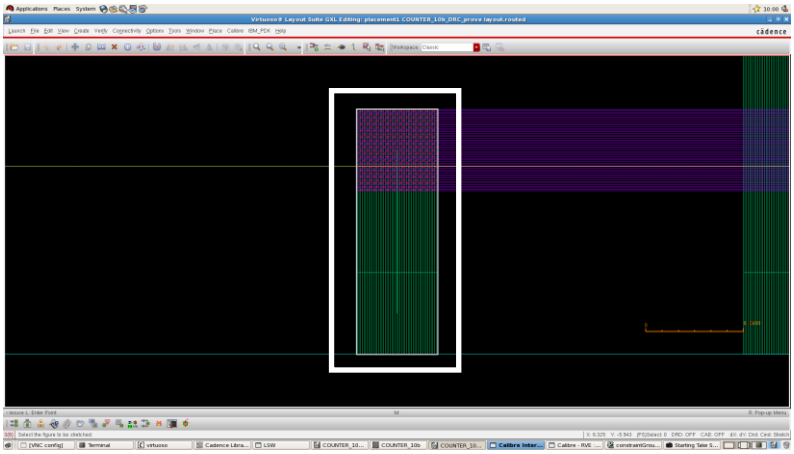


Fig 9.d. Metal violating minimum area DRC

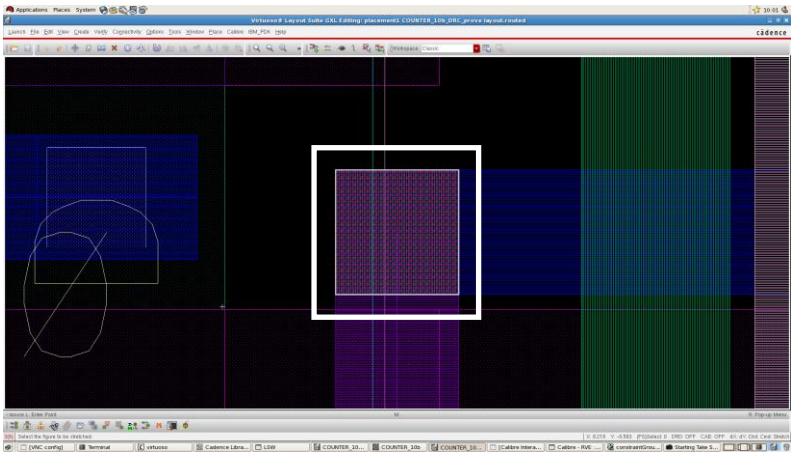


Fig 9.e. No metal enclosure of standard via

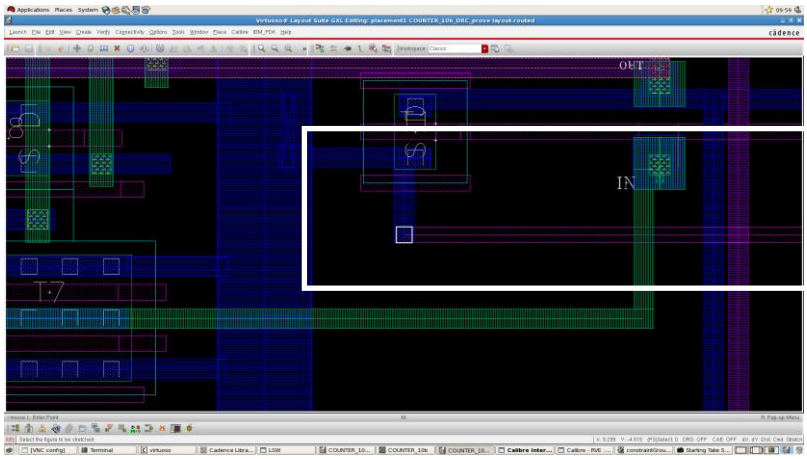


Fig 9.f. Illegal use of POLY for routing

Type of DRC violation	Constraint to be edited	Technology File Section
Setting choice of metal/vias for routing	interconnect((validLayers ()) (validVias ())) ;interconnect	constrainGroups
Layer spacing violations	spacingTables(spacingTables())	constrainGroups – foundry constraints
Minimum layer spacing/width/area	spacings(minSpacing “” minSameNetSpacing “” minWidth “” minArea “”)	constrainGroups – foundry constraints
Metal enclosure of vias	standardViaDefs(;(viaDefName layer1 layer2 (cutLayer cutWidth cutHeight [resistancePerCut]) ; (cutRows cutCol (cutSpace)) ; (layer1Enc) (layer2Enc) (layer1Offset) (layer2Offset) (origOffset) ; [implant1 (implant1Enc) [implant2 (implant2Enc) [well/substrate]]]) ;(----------) ( ))	viaDefs

Table 1. Sections of Technology file to be edited for DRC clean routing

Fig 10. DRC violation from routing

However in spite of all these manipulations to the technology file for running the router, there are still some DRC violations that arise as a result of routing. An example of such a violation is as shown in the **Figure 10** above, where a small corner notch is formed by the routing metals giving rise to violations. For now these violations need to be corrected manually, but there should be an automated solution which needs to come up as part of future work.

Another class of DRC errors still seen were related to the number of via cuts that are placed for wide metal overlap regions. Although the technology filw has a setion – *minNumCut* the tool does not honor these properly.

Virtuoso Custom Digital Placer & Chip Assembly Router were run on a 10-bit counter block with some of the above fixes attempted to obtain a DRC clean layout. The results are shown below in **Figure 11a**. **Figure 11.b** shows the DRC and LVS results for the final layout after some manual edits.

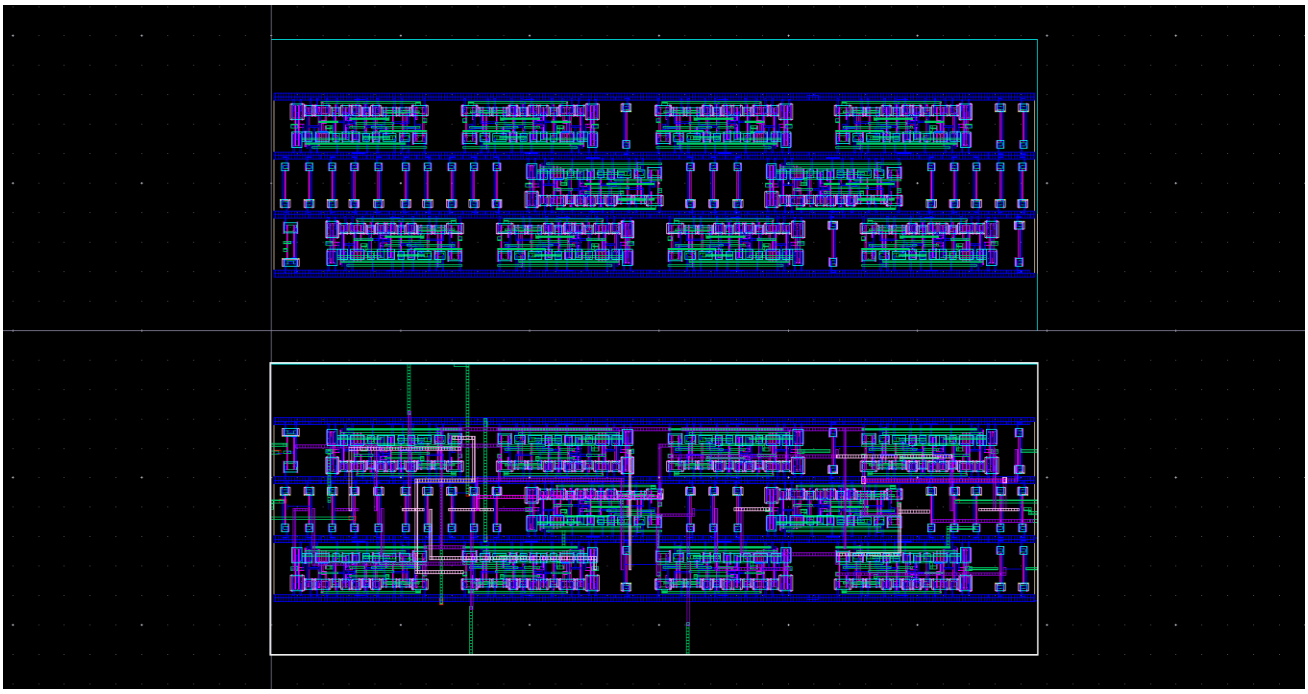


Fig 11.a. Layouts after Placement and Routing

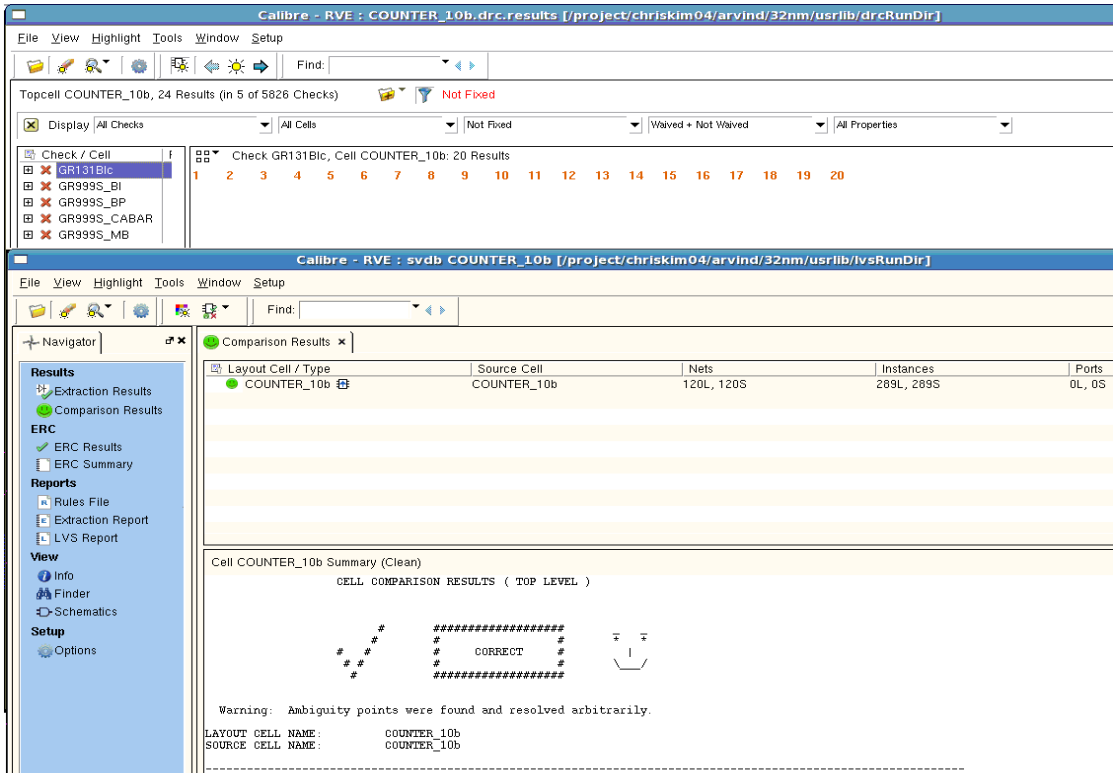


Fig 11.b. DRC and LVS results – DRC errors occur since it is a standalone block

DRC results for 10-bit counter block after technology file modification

In order to get a relatively DRC clean layout from the Virtuoso Chip Assembly Router the following edits were made to the technology files for 32nm and 65nm PDKs:

- Changed metal minimum spacing, minimum area and minimum width requirements of metal layers to adhere to certain DRC violations at the cost of slightly higher layout area.
- Changed metal enclosure of vias for these metal layers - M2/3/4/5/6/7. This was done to to take care of minimum area DRC violations for stacked vias. M1 enclosure of vias was not changed because of higher metal density for M1.
- Selectively change metal enclosure of vias when there are multiple kinds of vias between the same 2 metal layers. For eg. different M2 enclosure for the 3 types of vias to allow the router to choose the via to meet metal spacing & area DRC rule requirements together.
- Changed validlayers to remove poly and other metal layers not desired for routing, to preclude their use for routing.

Figure 12 below shows the improvement in DRC results before and after making edits to the technology file for the 32nm and 65nm PDKs.

As mentioned before the violations that are left after modifying the technology file are to do with the following:

- L-shaped metal noteches
- Minimum number of via cuts for wide metal overlaps

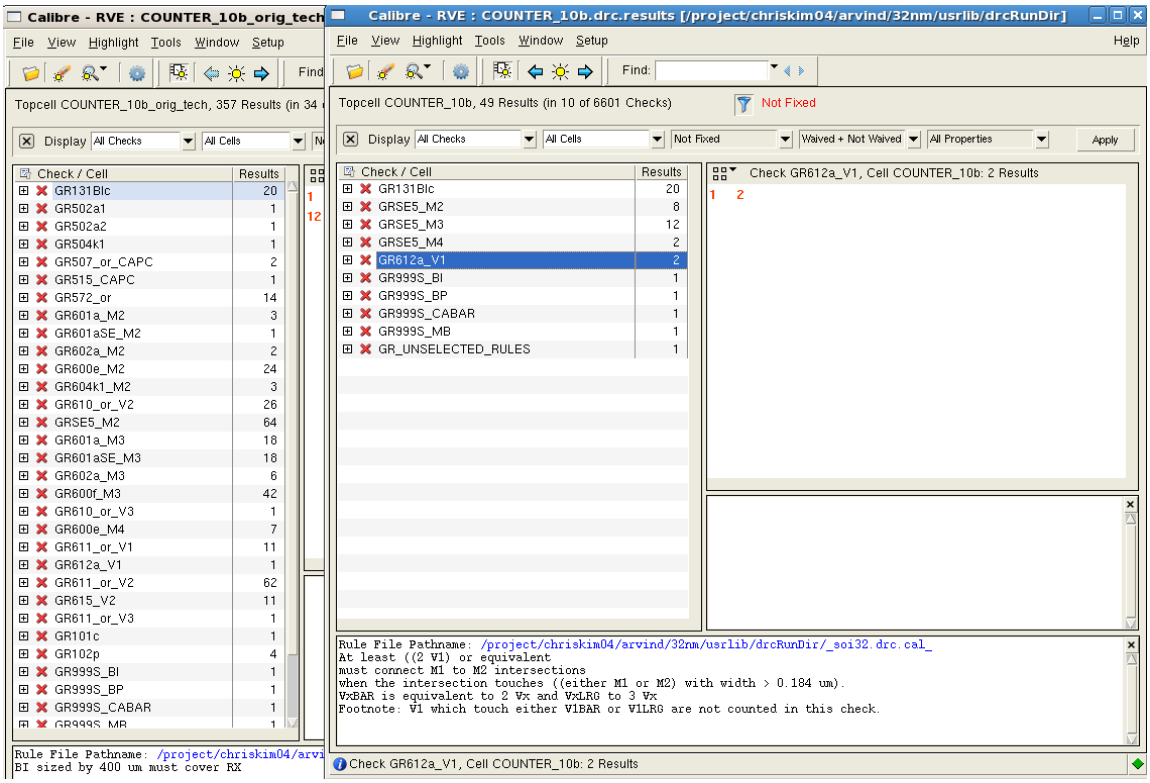


Fig 12.a. 32nm DRC results comparison

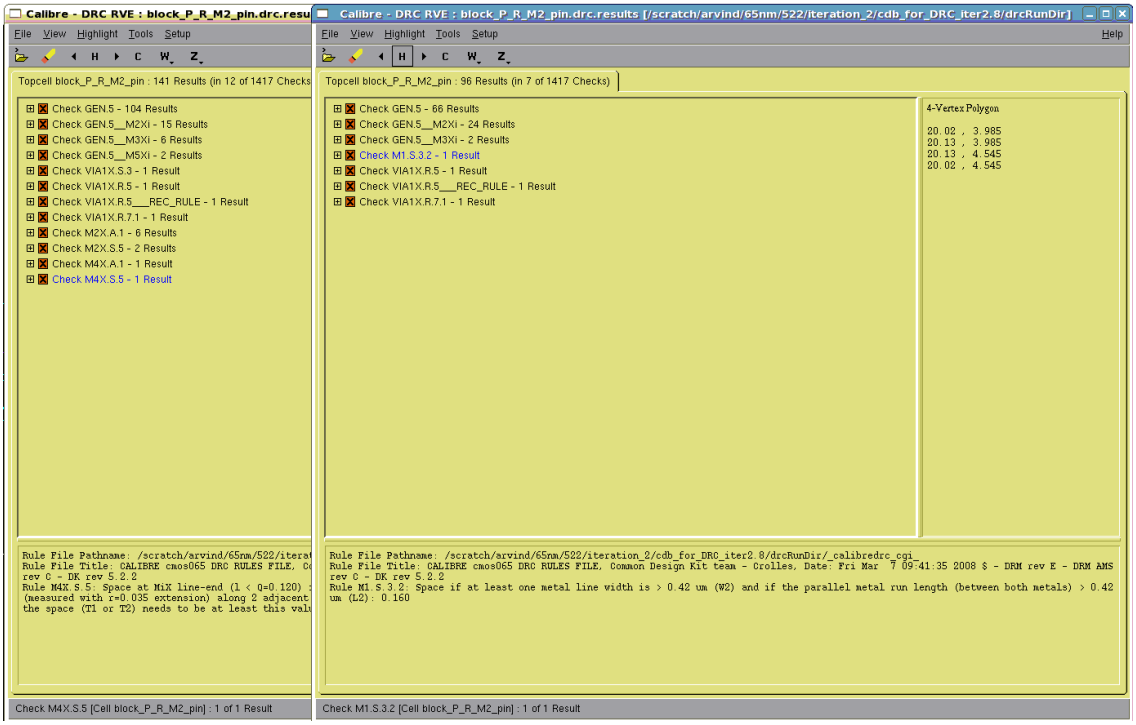


Fig 12.b. 65nm DRC results comparison

3. Timing Comparison between Encounter and Virtuoso-GXL P&R tools

In order to evaluate this flow, *Virtuoso Custom Digital Placer* and *Virtuoso Chip Assembly Router* were run on a larger design and timing results were compared with an industry standard place and route solution – *Cadence Encounter Digital Implementation System XL(R)* [4].

For this run the testcase used was an Advanced Encryption System core – aes_cipher_top - from *http://opencores.org* [7]. This gate-count for this core is 9809. For both the runs the design was attempted to close timing at a clock period of 2.5ns (400 Mhz) using a 65nm PDK from ST Microelectronics. The corners used for this analysis were as follows:

Min corner: Strong process, VDD=1.1V, Temperature= -40C

Max corner: Weak process, VDD=0.9V, Temperature= 125C

3.1 Encounter P&R flow

The gate-level netlist and Synopsys Design Constraints (SDC) file were run through a basic Encounter P&R flow as shown in **Figure 13** below. The flow was run using a 7-metal layer process.

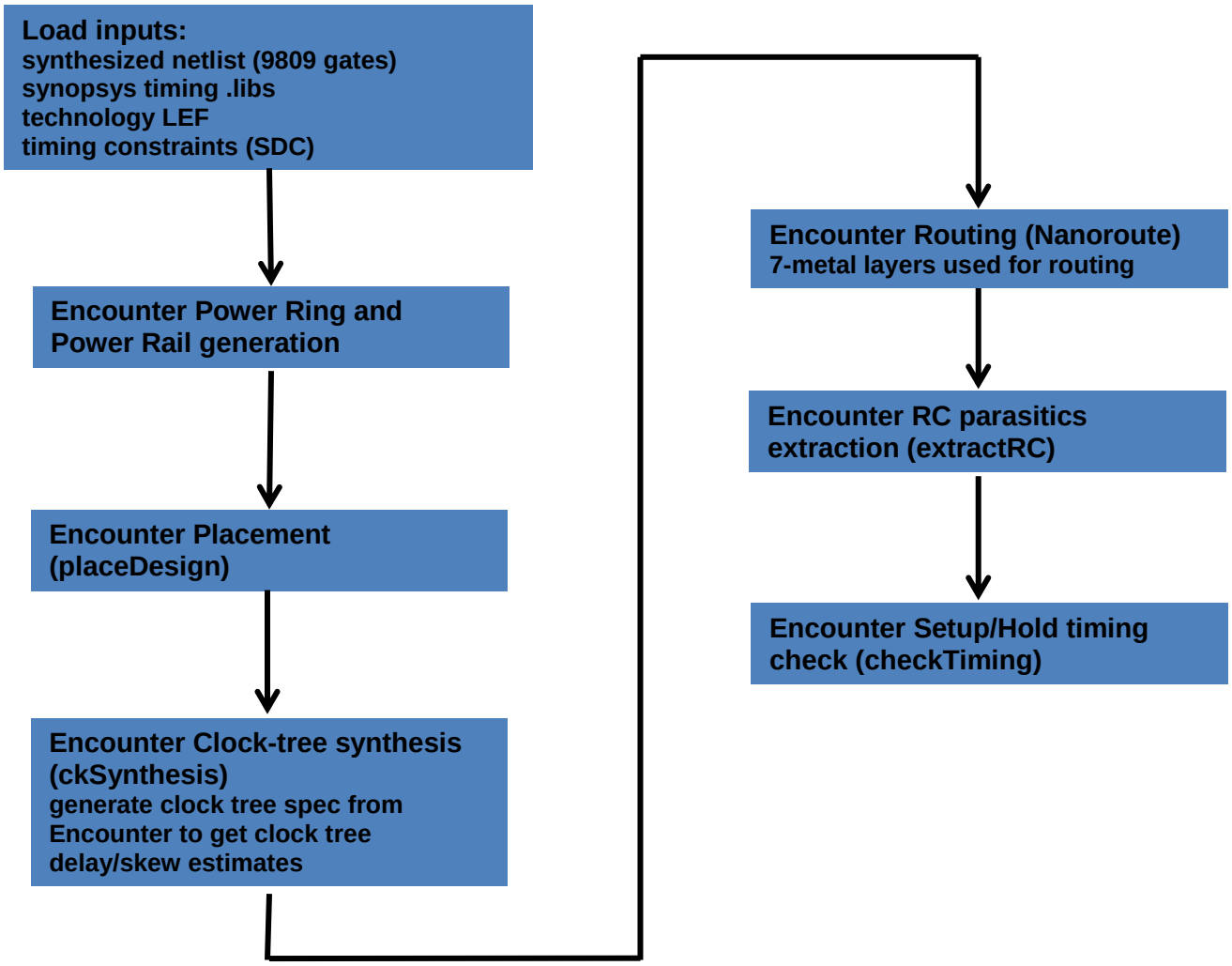


Fig 13. Encounter Place & Route flow

Static timing analysis using worst and best timing corners for setup and hold was performed within Encounter, which revealed 9 paths which violated slack for setup at a clock period of 2.5ns. The worst negative was -0.036ns. Hold timing for the design was closed during this run. The following **Figure 14** shows timing snapshot of the worst setup and hold paths from this run.

```
#####################################################################
# Generated by:     Cadence Encounter 09.11-s084_1
# OS:               Linux x86_64(Host ID sody.ece.umn.edu)
# Generated on:     Mon May  2 12:58:53 2011
# Command:          report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 100 -net -summary >
$rpt_dir/report_timing.post_extract.summary
#####################################################################
+-------------------------------------------------------------------------------------------------------------------------------------------+
|  Path |              Pin |                                  Cause                                  | Slack | Arrival | Required |    Phase | Other Phase |
|   No. |                  |                                                                         |       |         |          |          |             |
|-------+------------------+-------------------------------------------------------------------------+-------+---------+----------+----------+-------------|
|     1 |  \sa32_reg[4] /D ^ | VIOLATED Setup Check with Pin \sa32_reg[4] /CP                        | -0.036 |   2.705 |    2.669 | clk(D)(P) | clk(C)(P) * |
|     2 |  \sa31_reg[1] /D ^ | VIOLATED Setup Check with Pin \sa31_reg[1] /CP                        | -0.032 |   2.739 |    2.708 | clk(D)(P) | clk(C)(P) * |
|     3 |  \sa20_reg[7] /D ^ | VIOLATED Setup Check with Pin \sa20_reg[7] /CP                        | -0.025 |   2.722 |    2.697 | clk(D)(P) | clk(C)(P) * |
|     4 |  \sa20_reg[3] /D ^ | VIOLATED Setup Check with Pin \sa20_reg[3] /CP                        | -0.022 |   2.721 |    2.699 | clk(D)(P) | clk(C)(P) * |
|     5 |  \sa00_reg[1] /D ^ | VIOLATED Setup Check with Pin \sa00_reg[1] /CP                        | -0.020 |   2.769 |    2.749 | clk(D)(P) | clk(C)(P) * |
|     6 |  \sa23_reg[3] /D ^ | VIOLATED Setup Check with Pin \sa23_reg[3] /CP                        | -0.019 |   2.715 |    2.696 | clk(D)(P) | clk(C)(P) * |
|     7 |  \sa23_reg[6] /D ^ | VIOLATED Setup Check with Pin \sa23_reg[6] /CP                        | -0.007 |   2.700 |    2.693 | clk(D)(P) | clk(C)(P) * |
|     8 |  \sa23_reg[1] /D ^ | VIOLATED Setup Check with Pin \sa23_reg[1] /CP                        | -0.004 |   2.703 |    2.699 | clk(D)(P) | clk(C)(P) * |
|     9 |  \sa20_reg[1] /D ^ | VIOLATED Setup Check with Pin \sa20_reg[1] /CP                        | -0.002 |   2.704 |    2.702 | clk(D)(P) | clk(C)(P) * |
|    10 |   \sa32_reg[1] /D ^ | MET Setup Check with Pin \sa32_reg[1] /CP                            |  0.001 |   2.678 |    2.679 | clk(D)(P) | clk(C)(P) * |
|    11 |   \sa00_reg[3] /D ^ | MET Setup Check with Pin \sa00_reg[3] /CP                            |  0.002 |   2.750 |    2.752 | clk(D)(P) | clk(C)(P) * |
|    12 |   \sa20_reg[4] /D ^ | MET Setup Check with Pin \sa20_reg[4] /CP                            |  0.003 |   2.698 |    2.701 | clk(D)(P) | clk(C)(P) * |
|    13 |   \sa23_reg[4] /D ^ | MET Setup Check with Pin \sa23_reg[4] /CP                            |  0.003 |   2.697 |    2.700 | clk(D)(P) | clk(C)(P) * |
|    14 |   \sa00_reg[4] /D ^ | MET Setup Check with Pin \sa00_reg[4] /CP                            |  0.004 |   2.748 |    2.752 | clk(D)(P) | clk(C)(P) * |
|    15 |   \sa31_reg[4] /D ^ | MET Setup Check with Pin \sa31_reg[4] /CP                            |  0.005 |   2.701 |    2.705 | clk(D)(P) | clk(C)(P) * |
```

Fig 14.a. Encounter Worst Setup Timing paths

```
#####################################################################
# Generated by:     Cadence Encounter 09.11-s084_1
# OS:               Linux x86_64(Host ID sody.ece.umn.edu)
# Generated on:     Mon May  2 13:00:43 2011
# Command:          report_timing -format {hpin arc cell delay arrival slew load} -early -max_points 100 -net -summary >
$rpt_dir/report_timing.post_extract.hold.summary
#####################################################################
  +-------------------------------------------------------------------------------------------------------------------------------------------+
  |  Path |              Pin |                                  Cause                                  | Slack | Arrival | Required |    Phase | Other Phase |
  |   No. |                  |                                                                         |       |         |          |          |             |
  |-------+------------------+-------------------------------------------------------------------------+-------+---------+----------+----------+-------------|
  |     1 |          ld_r_reg/D v | MET Hold Check with Pin ld_r_reg/CP                               |  0.121 |   0.406 |    0.286 | clk(D)(P) | clk(C)(P) * |
  |     2 |  \text_in_r_reg[81] /D v | MET Hold Check with Pin \text_in_r_reg[81] /CP                 |  0.126 |   0.402 |    0.275 | clk(D)(P) | clk(C)(P) * |
  |     3 |  \text_in_r_reg[92] /D v | MET Hold Check with Pin \text_in_r_reg[92] /CP                 |  0.128 |   0.402 |    0.274 | clk(D)(P) | clk(C)(P) * |
  |     4 |  \text_in_r_reg[99] /D v | MET Hold Check with Pin \text_in_r_reg[99] /CP                 |  0.130 |   0.401 |    0.270 | clk(D)(P) | clk(C)(P) * |
  |     5 |  \text_in_r_reg[96] /D v | MET Hold Check with Pin \text_in_r_reg[96] /CP                 |  0.131 |   0.401 |    0.270 | clk(D)(P) | clk(C)(P) * |
  |     6 | \text_in_r_reg[118] /D v | MET Hold Check with Pin \text_in_r_reg[118] /CP                |  0.131 |   0.403 |    0.272 | clk(D)(P) | clk(C)(P) * |
  |     7 |  \text_in_r_reg[98] /D v | MET Hold Check with Pin \text_in_r_reg[98] /CP                 |  0.131 |   0.401 |    0.270 | clk(D)(P) | clk(C)(P) * |
  |     8 |  \text_in_r_reg[94] /D v | MET Hold Check with Pin \text_in_r_reg[94] /CP                 |  0.131 |   0.403 |    0.272 | clk(D)(P) | clk(C)(P) * |
  |     9 | \text_in_r_reg[100] /D v | MET Hold Check with Pin \text_in_r_reg[100] /CP                |  0.131 |   0.401 |    0.270 | clk(D)(P) | clk(C)(P) * |
  |    10 | \text_in_r_reg[101] /D v | MET Hold Check with Pin \text_in_r_reg[101] /CP                |  0.131 |   0.401 |    0.270 | clk(D)(P) | clk(C)(P) * |
  |    11 |  \text_in_r_reg[87] /D v | MET Hold Check with Pin \text_in_r_reg[87] /CP                 |  0.132 |   0.405 |    0.273 | clk(D)(P) | clk(C)(P) * |
  |    12 |  \text_in_r_reg[93] /D v | MET Hold Check with Pin \text_in_r_reg[93] /CP                 |  0.132 |   0.405 |    0.273 | clk(D)(P) | clk(C)(P) * |
  |    13 | \text_in_r_reg[102] /D v | MET Hold Check with Pin \text_in_r_reg[102] /CP                |  0.132 |   0.401 |    0.269 | clk(D)(P) | clk(C)(P) * |
  |    14 |  \text_in_r_reg[95] /D v | MET Hold Check with Pin \text_in_r_reg[95] /CP                 |  0.132 |   0.404 |    0.272 | clk(D)(P) | clk(C)(P) * |
  |    15 | \text_in_r_reg[103] /D v | MET Hold Check with Pin \text_in_r_reg[103] /CP                |  0.132 |   0.401 |    0.269 | clk(D)(P) | clk(C)(P) * |
```

Fig 14.b. Encounter Worst Hold Timing paths

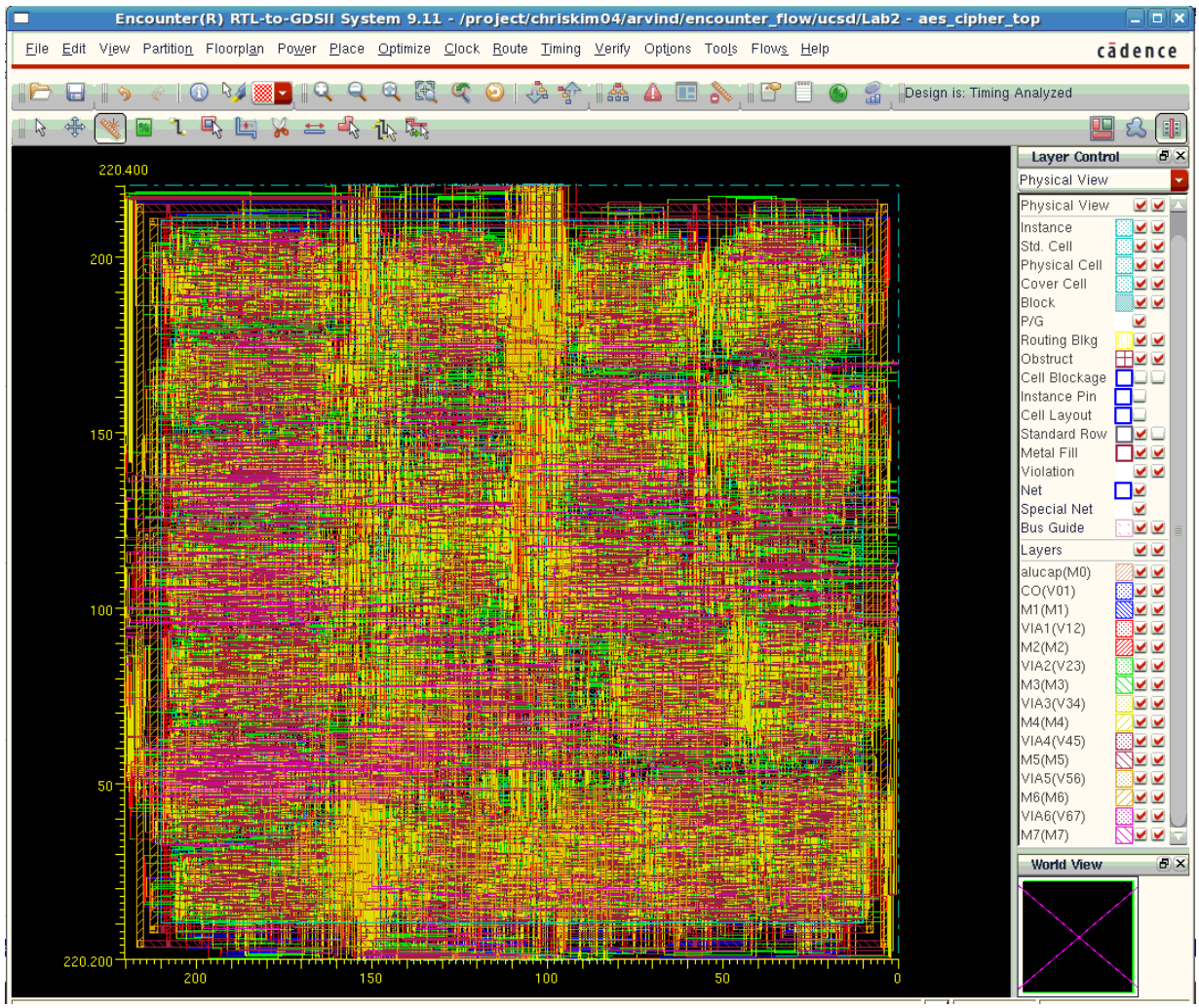


Fig 15. Encounter Place & Route run

3.2 Virtuoso-GXL P&R flow

Next the gate-level netlist were run through a basic Encounter P&R flow as shown in **Figure 15** below. The router was restricted to using 7 metal layers in order to be consistent with the Encounter flow.

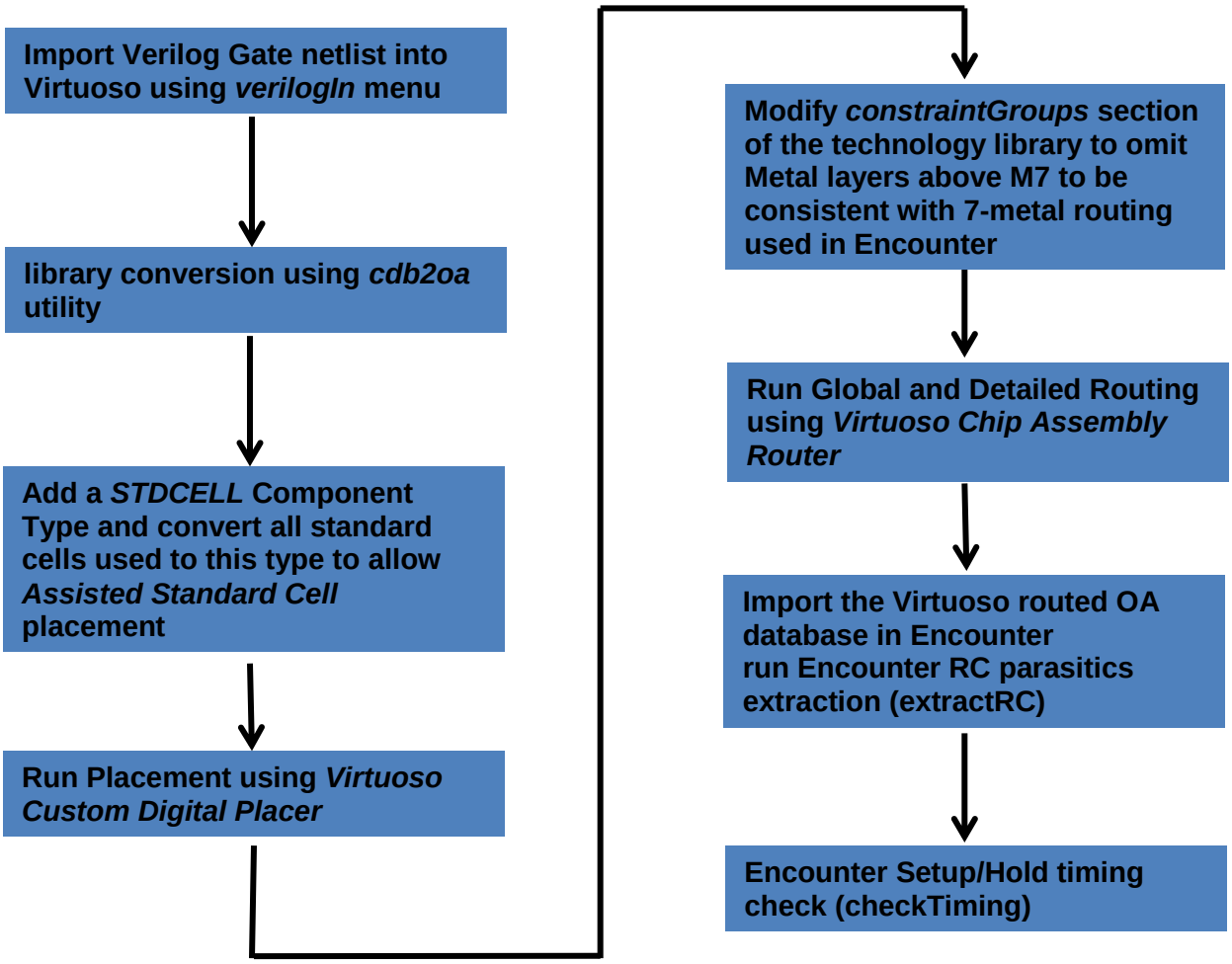


Fig 16. Virtuoso-GXL Place & Route flow

3.2.1 VeilogIn

The *VerologIn* menu (*File->Import->Verilog*) can be invoked from the main *Virtuoso* command window, for directly importing the gate-level netlist and standard cell libraries. The destination library to which the design should be imported can also specified.

3.2.2 CDB to Open Access Conversion (*cdb2oa*)

The cdb2oa utility can be used to migrate any PDK from Cadence version IC5.1.41 to IC6.1, to create a syntactically correct techfile [6]. Since the ST Microelectronics libraries were created using Cadence version IC5.1.41, and the Layout-GXL tool suite is only available as part of Cadence version IC6.1, the technology library, standard cell libraries and the design library all need to be converted to Open Access format to be used in IC6.1. This utility can be invoked as follows:

cdb2oa -cdslibpath <dir path of source library> -lib <source library name> -log <logfile>

Note that the technology library needs to be converted first before converting the standard cell and design libraries.

After the design was placed and routed within *Virtuoso-GXL*, the Open Access database is directly imported into Encounter using the *Design Import* (*File->Import Design*) form, as shown in **Figure 17**.

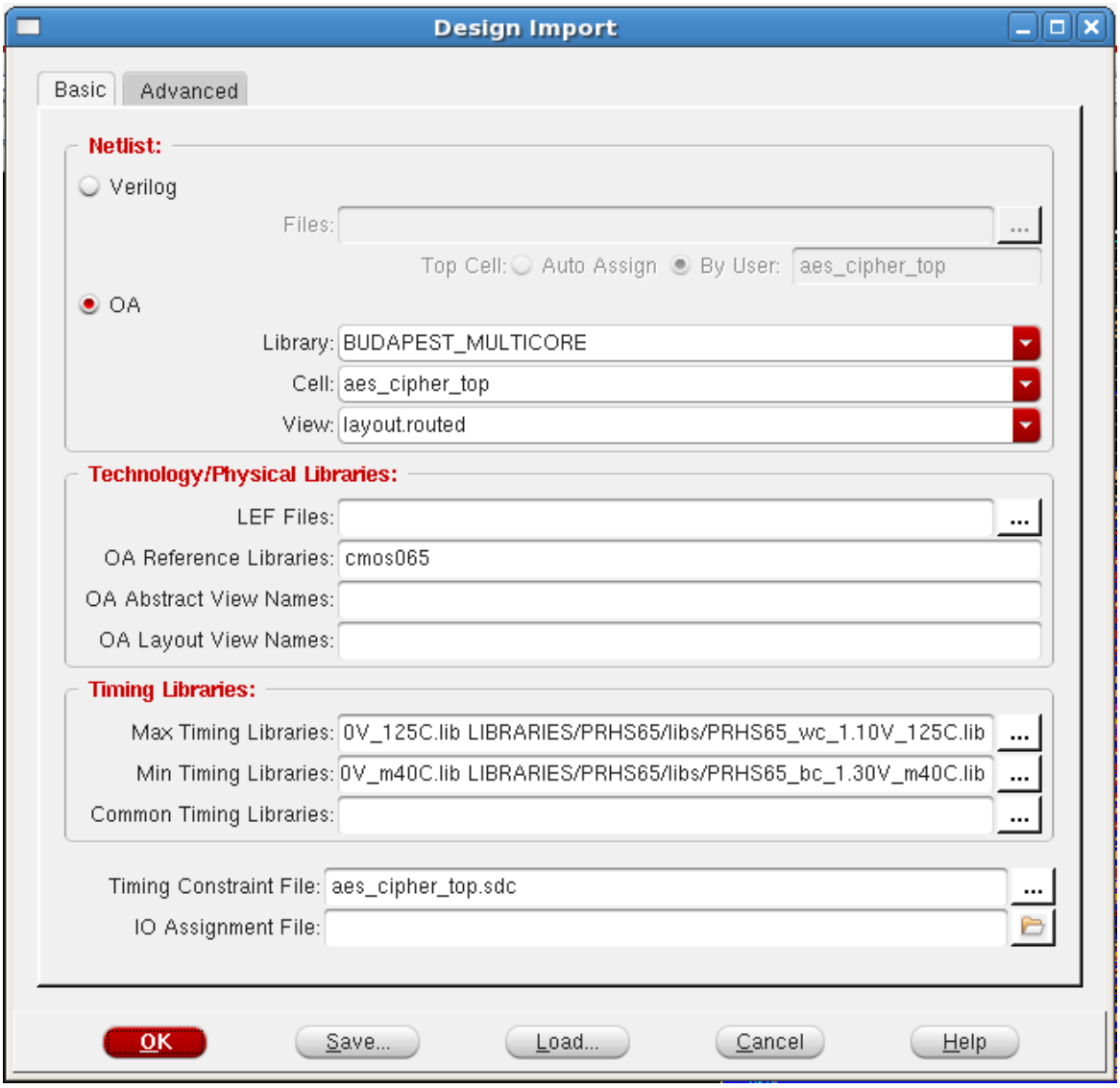


Fig 17. Encounter Open Access import from Virtuoso-GXL

Following this RC parasitics were extracted and static timing analysis using worst and best timing corners for setup and hold was performed within Encounter. However here the worst path violating setup was had a negative slack as large as -1.42ns The clock period was 2.5ns. Hold timing for the design was closed during this run. The following **Figure 18** shows timing snapshot of the worst setup and hold paths from this run.

```
#####################################################################
#  Generated by:      Cadence Encounter 09.11-s084_1
#  OS:                Linux x86_64(Host ID sody.ece.umn.edu)
#  Generated on:      Thu May  5 23:18:46 2011
#  Command:           report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 300 -net -summary
#####################################################################
```

Path No.	Pin	Cause	Slack	Arrival	Required	Phase	Other Phase
1	|u0|w_reg[2][24] /D ^	VIOLATED Setup Check with Pin |u0|w_reg[2][24] /CP	-1.420	3.848	2.428	clk(D)(P)	clk(C)(P)
2	|u0|w_reg[3][24] /D ^	VIOLATED Setup Check with Pin |u0|w_reg[3][24] /CP	-1.121	3.494	2.373	clk(D)(P)	clk(C)(P)
3	|sa21_reg[4] /D v	VIOLATED Setup Check with Pin |sa21_reg[4] /CP	-1.119	3.472	2.352	clk(D)(P)	clk(C)(P)
4	|u0|w_reg[3][25] /D ^	VIOLATED Setup Check with Pin |u0|w_reg[3][25] /CP	-1.097	3.530	2.433	clk(D)(P)	clk(C)(P)
5	|u0|w_reg[2][25] /D v	VIOLATED Setup Check with Pin |u0|w_reg[2][25] /CP	-1.082	3.498	2.416	clk(D)(P)	clk(C)(P)
6	|u0|w_reg[3][0] /D v	VIOLATED Setup Check with Pin |u0|w_reg[3][0] /CP	-1.080	3.496	2.416	clk(D)(P)	clk(C)(P)
7	|u0|w_reg[2][0] /D v	VIOLATED Setup Check with Pin |u0|w_reg[2][0] /CP	-1.026	3.443	2.417	clk(D)(P)	clk(C)(P)
8	|u0|w_reg[3][30] /D v	VIOLATED Setup Check with Pin |u0|w_reg[3][30] /CP	-1.014	3.429	2.415	clk(D)(P)	clk(C)(P)
9	|u0|w_reg[2][30] /D v	VIOLATED Setup Check with Pin |u0|w_reg[2][30] /CP	-0.987	3.403	2.416	clk(D)(P)	clk(C)(P)
10	|u0|w_reg[3][31] /D v	VIOLATED Setup Check with Pin |u0|w_reg[3][31] /CP	-0.982	3.396	2.414	clk(D)(P)	clk(C)(P)
11	|u0|w_reg[2][31] /D v	VIOLATED Setup Check with Pin |u0|w_reg[2][31] /CP	-0.961	3.377	2.416	clk(D)(P)	clk(C)(P)
12	|u0|w_reg[1][0] /D v	VIOLATED Setup Check with Pin |u0|w_reg[1][0] /CP	-0.887	3.302	2.415	clk(D)(P)	clk(C)(P)
13	|u0|w_reg[3][26] /D v	VIOLATED Setup Check with Pin |u0|w_reg[3][26] /CP	-0.886	3.302	2.416	clk(D)(P)	clk(C)(P)
14	|sa21_reg[1] /D v	VIOLATED Setup Check with Pin |sa21_reg[1] /CP	-0.883	3.251	2.368	clk(D)(P)	clk(C)(P)
15	|u0|w_reg[3][6] /D v	VIOLATED Setup Check with Pin |u0|w_reg[3][6] /CP	-0.876	3.291	2.416	clk(D)(P)	**clk(C)(P)**

Fig 18.a. Virtuoso-GXL Worst Setup Timing paths

```
#####################################################################
#  Generated by:      Cadence Encounter 09.11-s084_1
#  OS:                Linux x86_64(Host ID sody.ece.umn.edu)
#  Generated on:      Thu May  5 23:32:05 2011
#  Command:           report_timing -format {hpin arc cell delay arrival slew load} -early -max_points 100 -net -summary
#####################################################################
```

Path No.	Pin	Cause	Slack	Arrival	Required	Phase	Other Phase
1	|dcnt_reg[0] /D v	MET Hold Check with Pin |dcnt_reg[0] /CP	0.171	0.205	0.034	clk(D)(P)	clk(C)(P) *
2	|u0|r0|rcnt_reg[3] /D v	MET Hold Check with Pin |u0|r0|rcnt_reg[3] /CP	0.177	0.210	0.032	clk(D)(P)	clk(C)(P) *
3	|u0|r0|rcnt_reg[0] /D v	MET Hold Check with Pin |u0|r0|rcnt_reg[0] /CP	0.178	0.209	0.032	clk(D)(P)	clk(C)(P) *
4	|text_out_reg[114] /D v	MET Hold Check with Pin |text_out_reg[114] /CP	0.178	0.210	0.032	clk(D)(P)	clk(C)(P) *
5	|text_out_reg[119] /D v	MET Hold Check with Pin |text_out_reg[119] /CP	0.178	0.210	0.032	clk(D)(P)	clk(C)(P) *
6	|text_out_reg[85] /D v	MET Hold Check with Pin |text_out_reg[85] /CP	0.178	0.210	0.032	clk(D)(P)	clk(C)(P) *
7	|sa12_reg[2] /D v	MET Hold Check with Pin |sa12_reg[2] /CP	0.178	0.212	0.034	clk(D)(P)	clk(C)(P) *
8	|sa21_reg[6] /D v	MET Hold Check with Pin |sa21_reg[6] /CP	0.178	0.212	0.034	clk(D)(P)	clk(C)(P) *
9	|sa10_reg[7] /D v	MET Hold Check with Pin |sa10_reg[7] /CP	0.179	0.213	0.034	clk(D)(P)	clk(C)(P) *
10	|sa21_reg[3] /D v	MET Hold Check with Pin |sa21_reg[3] /CP	0.180	0.214	0.034	clk(D)(P)	clk(C)(P) *
11	|sa30_reg[6] /D v	MET Hold Check with Pin |sa30_reg[6] /CP	0.181	0.214	0.033	clk(D)(P)	clk(C)(P) *
12	|text_out_reg[88] /D v	MET Hold Check with Pin |text_out_reg[88] /CP	0.181	0.213	0.032	clk(D)(P)	clk(C)(P) *
13	|sa02_reg[6] /D v	MET Hold Check with Pin |sa02_reg[6] /CP	0.181	0.215	0.034	clk(D)(P)	clk(C)(P) *
14	|sa32_reg[4] /D v	MET Hold Check with Pin |sa32_reg[4] /CP	0.182	0.216	0.034	clk(D)(P)	clk(C)(P) *
15	|text_out_reg[107] /D v	MET Hold Check with Pin |text_out_reg[107] /CP	0.182	0.214	0.032	clk(D)(P)	clk(C)**(P) * |**

Fig 18.b. Virtuoso-GXL Worst Hold Timing paths

The following **Figure 19** gives slack profile of the number of paths violating setup timing, from the *Virtuoso-GXL* P&R run. A total 199 paths are violating setup timing.

Violating Slack	No. of Paths
1.2-1.4 ns	1
1.0-1.2 ns	7
0.8-1.0 ns	11
0.6-0.8 ns	11
0.4-0.6 ns	26
0.2-0.4 ns	64
<0.2ns	80

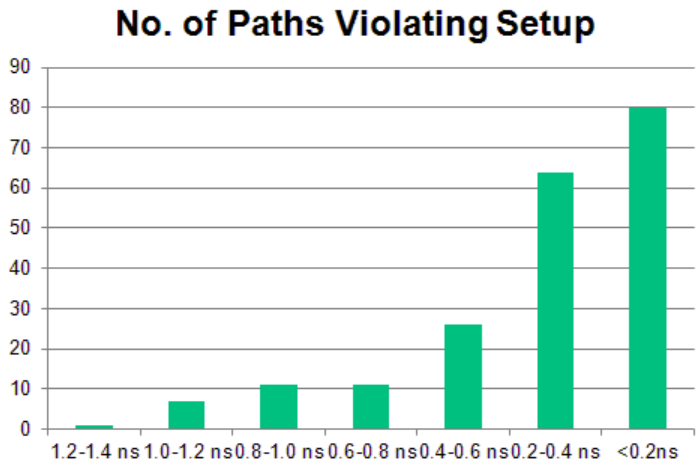
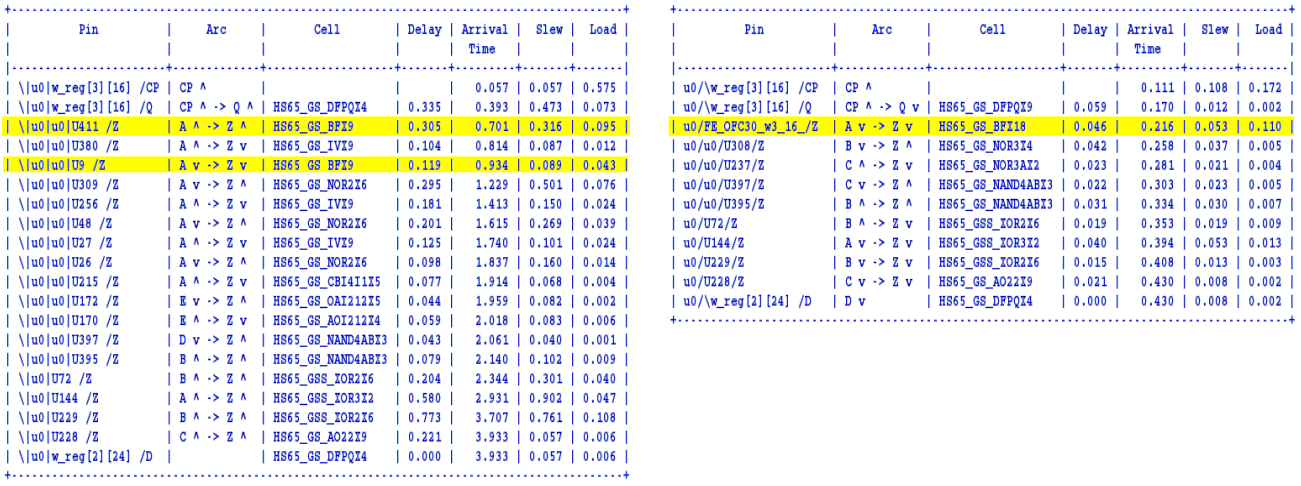


Fig 19. Virtuoso-GXL Setup Violation slack profile

After examination of the worst path between the 2 runs it was found that Encounter was optimizing 2 9X buffers to a single 18X buffer to optimize timing on this path as shown in **Figure 20** below. This replacement helps restrict the slew rate degradation long the path and causes the path to meet timing in the Encounter P&R run. Since the *Virtuoso-GXL* P&R was not run with timing constraints, this optimization did not occur. Constrained placement and routing in *Virtuoso-GXL* remains to be explored as part of future work.



Pin	Arc	Cell	Delay	Arrival Time	Slew	Load
|u0|w_reg[3][16] /CP	CP ^			0.057	0.057	0.575
|u0|w_reg[3][16] /Q	CP ^ -> Q ^	HS65_GS_DFPQX4	0.335	0.393	0.473	0.073
|u0|u0|U411 /Z	A ^ -> Z ^	HS65_GS_BFX9	0.305	0.701	0.316	0.095
|u0|u0|U380 /Z	A ^ -> Z v	HS65_GS_IVX9	0.104	0.814	0.087	0.012
|u0|u0|U9 /Z	A v -> Z v	HS65_GS_BFX9	0.119	0.934	0.089	0.043
|u0|u0|U309 /Z	A v -> Z ^	HS65_GS_NOR2X6	0.295	1.229	0.501	0.076
|u0|u0|U256 /Z	A ^ -> Z v	HS65_GS_IVX9	0.181	1.413	0.150	0.024
|u0|u0|U48 /Z	A v -> Z ^	HS65_GS_NOR2X6	0.201	1.615	0.269	0.039
|u0|u0|U27 /Z	A ^ -> Z v	HS65_GS_IVX9	0.125	1.740	0.101	0.024
|u0|u0|U26 /Z	A v -> Z ^	HS65_GS_NOR2X6	0.098	1.837	0.160	0.014
|u0|u0|U215 /Z	A ^ -> Z v	HS65_GS_CBI4I1X5	0.077	1.914	0.068	0.004
|u0|u0|U172 /Z	B v -> Z ^	HS65_GS_OAI212X5	0.044	1.959	0.082	0.002
|u0|u0|U170 /Z	B ^ -> Z v	HS65_GS_AOI212X4	0.059	2.018	0.083	0.006
|u0|u0|U397 /Z	D v -> Z ^	HS65_GS_NAND4ABX3	0.043	2.061	0.040	0.001
|u0|u0|U395 /Z	B ^ -> Z ^	HS65_GS_NAND4ABX3	0.079	2.140	0.102	0.009
|u0|U72 /Z	B ^ -> Z ^	HS65_GSS_XOR2X6	0.204	2.344	0.301	0.040
|u0|U144 /Z	A ^ -> Z ^	HS65_GSS_XOR3X2	0.580	2.931	0.902	0.047
|u0|U229 /Z	B ^ -> Z ^	HS65_GSS_XOR2X6	0.773	3.707	0.761	0.108
|u0|U228 /Z	C ^ -> Z ^	HS65_GS_AO22X9	0.221	3.933	0.057	0.006
|u0|w_reg[2][24] /D		HS65_GS_DFPQX4	0.000	3.933	0.057	0.006

Pin	Arc	Cell	Delay	Arrival Time	Slew	Load
u0/\w_reg[3][16] /CP	CP ^			0.111	0.108	0.172
u0/\w_reg[3][16] /Q	CP ^ -> Q v	HS65_GS_DFPQX9	0.059	0.170	0.012	0.002
u0/FE_OFC30_w3_16_/Z	A v -> Z v	HS65_GS_BFX18	0.046	0.216	0.053	0.110
u0/u0/U308/Z	B v -> Z ^	HS65_GS_NOR3X4	0.042	0.258	0.037	0.005
u0/u0/U237/Z	C ^ -> Z v	HS65_GS_NOR3AX2	0.023	0.281	0.021	0.004
u0/u0/U397/Z	C v -> Z ^	HS65_GS_NAND4ABX3	0.022	0.303	0.023	0.005
u0/u0/U395/Z	B ^ -> Z ^	HS65_GS_NAND4ABX3	0.031	0.334	0.030	0.007
u0/U72/Z	B ^ -> Z v	HS65_GSS_XOR2X6	0.019	0.353	0.019	0.009
u0/U144/Z	A v -> Z v	HS65_GSS_XOR3X2	0.040	0.394	0.053	0.013
u0/U229/Z	B v -> Z v	HS65_GSS_XOR2X6	0.015	0.408	0.013	0.003
u0/U228/Z	C v -> Z v	HS65_GS_AO22X9	0.021	0.430	0.008	0.002
u0/\w_reg[2][24] /D	D v	HS65_GS_DFPQX4	0.000	0.430	0.008	0.002

Fig 20. Comparison of Virtuoso-GXL worst setup timing path with Encounter P&R run

The following table shows a brief comparison of timing, area and power between the *Encounter* and *Virtuoso-GXL* P&R flows.

	Encounter P&R flow	**Virtuoso P&R flow**
Clock Period	~2.6ns (385Mhz)	~3.92ns (255Mhz)
Total Power (max corner)	31.04 mW	30.44 mW
Total Internal Power (max corner)	14.42mW (41.45%)	13.34mW (43.82%)
Total Switching Power(max corner)	19.85 mW (57.05%)	16.57 mW (54.44%)
Total Leakage Power (max corner)	0.5228 mW (1.502%)	0.528mW (1.734%)
Total Leakage Power (min corner)	1.116 mW	1.13 mW
Total Area	48532.08 um^2	57806.58 um^2
Runtime		
Placement	< 2min	1 hr
Routing	< 2 min	24 hrs (can be improved using abstract views for std cells)

Table 2. Comparison of Encounter & Virtuoso-GXL P&R flows

As can be seen from **Table 2** above there are some tradeoffs using *Virtuoso-GXL* P&R tools on a larger design as compared to a standard tool like *Encounter*, primarily in terms of timing, area and tool runtime. However the motivation for creating this flow is to integrate small sized blocks for testchip design and the tradeoffs are not so severe in that case.

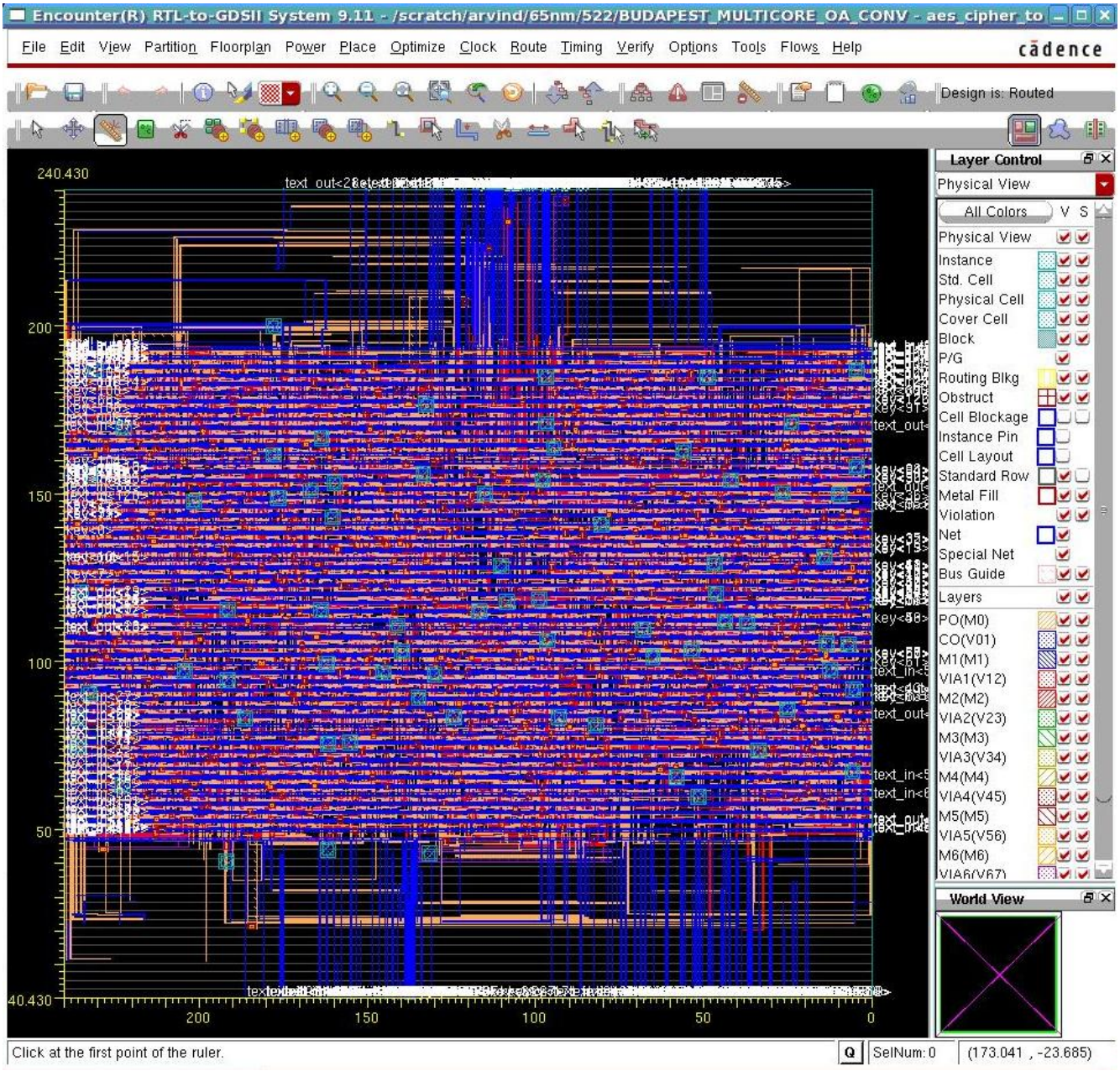


Fig 21. Virtuoso-GXL netlist imported into Encounter

Conclusion

This project attempted to provide an automated flow for placement and routing within the *Cadence Virtuoso* design environment. However, currently the flow is usable only for small to medium sized blocks. A method to run timing constrained placement and routing needs to be developed for larger designs in order to get better timing closure results on them at par with commercial P&R tools. Certain technology file modifications to guide the router have been effective in cutting down the number of DRC violations. However some violations still arise due to notches formed as a result of routing and the minimum number of via cuts for wide metal overlaps. Support needs to built into the tool to perform routing without these DRC rules.

References

[1] Cadence Design Systems, Inc, Virtuoso Custom Placer User Guide, *Product Version 6.1.3*

[2] Cadence Design Systems, Inc, Virtuoso Chip Assembly Router User Guide, *Product Version 6.1.3*

[3] Cadence Design Systems, Inc, Virtuoso Layout Suite GXL Reference, *Product Version 6.1.3*

[4] Cadence Design Systems, Inc, Encounter Digital Implementation System Reference, *Product Version 9.1.1*

[5] Open Access Constraints – http://vsevteme.ru/attachments/show?content=8292

[6] Challenges of PDK migration from IC5.1.41 to IC6.1 - http://www.cadence.com/rl/Resources/conference_papers/ctp_cdnlive2006_tran_pdkmigration.pdf

[7] Opencores.org - http://www.opencores.org

APPENDIX A: 10-bit counter DRC log

```
================================================================================
=====
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Fri May 13 12:18:10 2011
Calibre Version:           v2010.1_22.19    Tue Mar 9 14:04:08 PST 2010
Rule File Pathname:
/project/chriskim04/arvind/32nm/usrlib/drcRunDir/_soi32.drc.cal_
Rule File Title:
Layout System:             GDS
Layout Path(s):            COUNTER_10b.calibre.db
Layout Primary Cell:       COUNTER_10b
Current Directory:         /project/chriskim04/arvind/32nm/usrlib/drcRunDir
User Name:                 vinod001
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      COUNTER_10b.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       COUNTER_10b.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = NO  SKEW = NO  ANGLED = NO  OFFGRID = NO
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         YES
--------------------------------------------------------------------------------
-----
--------------------------------------------------------------------------------
-----
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
CELL pmos_7 ................... TOTAL Result Count = 1  (20)
    RULECHECK GR131BIc ........ TOTAL Result Count = 1  (20)
CELL nmos_4 ................... TOTAL Result Count = 1  (40)
    RULECHECK GR131BIc ........ TOTAL Result Count = 1  (40)
CELL pmos_8 ................... TOTAL Result Count = 1  (20)
    RULECHECK GR131BIc ........ TOTAL Result Count = 1  (20)
CELL nmos_2 ................... TOTAL Result Count = 1  (20)
    RULECHECK GR131BIc ........ TOTAL Result Count = 1  (20)
CELL sdff_1clk ................ TOTAL Result Count = 12 (120)
    RULECHECK GR131BIc ........ TOTAL Result Count = 12 (120)
CELL INV_MVT_1X ............... TOTAL Result Count = 2  (46)
    RULECHECK GR131BIc ........ TOTAL Result Count = 2  (46)
CELL COUNTER_10b .............. TOTAL Result Count = 6  (6)
    RULECHECK GR131BIc ........ TOTAL Result Count = 2  (2)
    RULECHECK GR999S_BI ....... TOTAL Result Count = 1  (1)
    RULECHECK GR999S_BP ....... TOTAL Result Count = 1  (1)
    RULECHECK GR999S_CABAR .... TOTAL Result Count = 1  (1)
    RULECHECK GR999S_MB ....... TOTAL Result Count = 1  (1)
```

```
--------------------------------------------------------------------------------
-----
--- SUMMARY
---
TOTAL CPU Time:                  6
TOTAL REAL Time:                 9
TOTAL Original Layer Geometries: 896 (8806)
TOTAL DRC RuleChecks Executed:   5822
TOTAL DRC Results Generated:     24 (272)
TOTAL DFM RDB Results Generated: 0 (0)
```

APPENDIX B:10-bit counter LVS log

```
                ################################################
                ##                                            ##
                ##         C A L I B R E    S Y S T E M       ##
                ##                                            ##
                ##             L V S   R E P O R T            ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         COUNTER_10b.lvs.report
LAYOUT NAME:              /project/chriskim04/arvind/32nm/usrlib/lvsRunDir/COUNTER_10b.sp
('COUNTER_10b')
SOURCE NAME:              /project/chriskim04/arvind/32nm/usrlib/lvsRunDir/COUNTER_10b.src.net
('COUNTER_10b')
RULE FILE:                /project/chriskim04/arvind/32nm/usrlib/lvsRunDir/_cmos32soi.lvs.cal_
CREATION TIME:            Wed May 11 01:11:16 2011
CURRENT DIRECTORY:        /project/chriskim04/arvind/32nm/usrlib/lvsRunDir
USER NAME:                vinod001
CALIBRE VERSION:          v2010.1_22.19    Tue Mar 9 14:04:08 PST 2010


                          OVERALL COMPARISON RESULTS


                       #       ###################       _   _
                     #         #                 #       *   *
                   #   #       #     CORRECT     #         |
                    # #        #                 #       \___/
                     #         ###################


  Warning:  Ambiguity points were found and resolved arbitrarily.

*************************************************************************************************
*************
                                    CELL  SUMMARY
*************************************************************************************************
*************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        COUNTER_10b                 COUNTER_10b


*************************************************************************************************
*************
                                    LVS PARAMETERS
*************************************************************************************************
*************


o LVS Setup:

   LVS COMPONENT TYPE PROPERTY           element
   LVS COMPONENT SUBTYPE PROPERTY        model
   LVS PIN NAME PROPERTY                 phy_pin
   // LVS POWER NAME
```

```
// LVS GROUND NAME
LVS CELL SUPPLY                         NO
LVS RECOGNIZE GATES                     ALL
LVS IGNORE PORTS                        YES
LVS CHECK PORT NAMES                    YES
LVS IGNORE TRIVIAL NAMED PORTS          NO
LVS BUILTIN DEVICE PIN SWAP             NO
LVS ALL CAPACITOR PINS SWAPPABLE        NO
LVS DISCARD PINS BY DEVICE              NO
LVS SOFT SUBSTRATE PINS                 NO
LVS INJECT LOGIC                        YES
LVS EXPAND UNBALANCED CELLS             YES
LVS EXPAND SEED PROMOTIONS              NO
LVS PRESERVE PARAMETERIZED CELLS        NO
LVS GLOBALS ARE PORTS                   YES
LVS REVERSE WL                          NO
LVS SPICE PREFER PINS                   NO
LVS SPICE SLASH IS SPACE                YES
LVS SPICE ALLOW FLOATING PINS           YES
// LVS SPICE ALLOW INLINE PARAMETERS
LVS SPICE ALLOW UNQUOTED STRINGS        NO
LVS SPICE CONDITIONAL LDD               NO
LVS SPICE CULL PRIMITIVE SUBCIRCUITS    NO
LVS SPICE IMPLIED MOS AREA              NO
// LVS SPICE MULTIPLIER NAME
LVS SPICE OVERRIDE GLOBALS              NO
LVS SPICE REDEFINE PARAM                NO
LVS SPICE REPLICATE DEVICES             NO
LVS SPICE SCALE X PARAMETERS            NO
LVS SPICE STRICT WL                     YES
// LVS SPICE OPTION
LVS STRICT SUBTYPES                     NO
LVS EXACT SUBTYPES                      NO
LAYOUT CASE                             YES
SOURCE CASE                             YES
LVS COMPARE CASE                        NO
LVS DOWNCASE DEVICE                     NO
LVS REPORT MAXIMUM                      50
LVS PROPERTY RESOLUTION MAXIMUM         ALL
// LVS SIGNATURE MAXIMUM
// LVS FILTER UNUSED OPTION
// LVS REPORT OPTION
LVS REPORT UNITS                        YES
// LVS NON USER NAME PORT
// LVS NON USER NAME NET
// LVS NON USER NAME INSTANCE

// Reduction

LVS REDUCE SERIES MOS                   NO
LVS REDUCE PARALLEL MOS                 NO
LVS REDUCE SEMI SERIES MOS              NO
LVS REDUCE SPLIT GATES                  NO
LVS REDUCE PARALLEL BIPOLAR             NO
LVS REDUCE SERIES CAPACITORS            NO
LVS REDUCE PARALLEL CAPACITORS          NO
LVS REDUCE SERIES RESISTORS             NO
LVS REDUCE PARALLEL RESISTORS           NO
LVS REDUCE PARALLEL DIODES              NO

LVS REDUCE  R(lvsres)  PARALLEL
LVS REDUCE  R(lvsres)  SERIES POS NEG
LVS REDUCE  efuse  PARALLEL NO
LVS REDUCE  MD(d_rvtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_rvtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_mvtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_mvtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_hvtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
```

```
LVS REDUCE  MD(d_hvtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_svtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_svtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_uvtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_uvtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_avtnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_avtpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  d_avtnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtdnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtdpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avthvdnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avthvdpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtmnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtmpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtlnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_avtlpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  MD(d_tonfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_topfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  d_tonfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_topfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tomnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tompfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tolnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tolpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tomlnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tomlpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_toxlnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_toxlpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tohvdnfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  d_tohvdpfet_bc  PARALLEL [ TOLERANCE l 0 w 0 nf 0 gcon 0 ]
LVS REDUCE  MD(d_tohvdnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_tohvdpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpubpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdbnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgbnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpucpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdcnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgcnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpudpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpddnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgdnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpuepfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdenfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgenfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpufpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdfnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgfnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpuhpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdhnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpghnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpujpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdjnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgjnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpukpfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpdknfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srpgknfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srxuknfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  MD(d_srxmknfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  R(resist)  PARALLEL [ TOLERANCE pl 0 pw 0 plevel 0 ]
LVS REDUCE  R(brres)  PARALLEL [ TOLERANCE W 0 L 0 s 0 pbar 0 m1pb 0 ]
LVS REDUCE  C(ugncap)  PARALLEL [ TOLERANCE pl 0 pw 0 nf 0 ]
LVS REDUCE  C(egncap)  PARALLEL [ TOLERANCE pl 0 pw 0 nf 0 ]
LVS REDUCE  C(vncap)  PARALLEL [ TOLERANCE l 0 w 0 botlev 0 toplev 0 ]
LVS REDUCE  Q(esdnsh)  PARALLEL [ TOLERANCE lesd 0 wesd 0 esdoxide 0 ]
LVS REDUCE  esdscr_sblk  PARALLEL [ TOLERANCE perimpdt 0 areapdt 0 dac 0 nf 0 ]
LVS REDUCE  esddiode  PARALLEL [ TOLERANCE perimpd 0 plpc 0 nf 0 nfc 0 w 0 ]
LVS REDUCE  esddiode_sblk  PARALLEL [ TOLERANCE perimpd 0 plpc 0 nf 0 nfc 0 nsblk 0 w 0 ]
```

```
LVS REDUCE  C(dtcellcap)  PARALLEL
LVS REDUCE  C(dtdcap)  PARALLEL [ TOLERANCE nrows 0 ncols 0 ]
LVS REDUCE  MD(dramnfet)  PARALLEL [ TOLERANCE l 0 w 0 gcon 0 pla 0 ]
LVS REDUCE  R(rmimhk)  PARALLEL [ TOLERANCE l 0 w 0 ]
LVS REDUCE  R(rmimhksh)  PARALLEL [ TOLERANCE l 0 w 0 ]
LVS REDUCTION PRIORITY                PARALLEL

// Filter

LVS FILTER  R(RP)  SHORT

// Trace Property

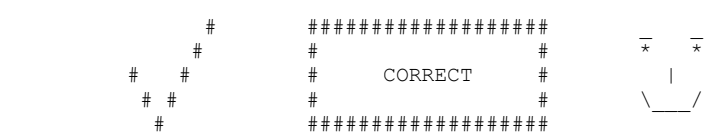
TRACE PROPERTY  d_avtnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtdnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtdnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtdpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtdpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtdpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avthvdnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avthvdnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avthvdpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avthvdpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avthvdpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtmnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtmnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtmpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtmpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtmpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtlnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtlnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtlpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_avtlpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_avtlpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tonfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tonfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tonfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tonfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tonfet_bc  nf nf 0.5 ABSOLUTE
```

```
TRACE PROPERTY  d_topfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_topfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_topfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_topfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_topfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tomnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tomnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tomnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tompfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tompfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tompfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tompfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tompfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tolnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tolnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tolnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tolnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tolnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tolpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tolpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tolpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tolpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tolpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomlnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomlnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomlpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tomlpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tomlpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_toxlnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_toxlnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_toxlpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_toxlpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_toxlpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdnfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tohvdnfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tohvdnfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdnfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdnfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdpfet_bc  l l 5e-10 ABSOLUTE
TRACE PROPERTY  d_tohvdpfet_bc  w w 5e-10 ABSOLUTE
TRACE PROPERTY  d_tohvdpfet_bc  m m 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdpfet_bc  gcon gcon 0.5 ABSOLUTE
TRACE PROPERTY  d_tohvdpfet_bc  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  fbdiode  perimpd perimpd 5e-10 ABSOLUTE
TRACE PROPERTY  fbdiode  ndiodes ndiodes 0.5 ABSOLUTE
TRACE PROPERTY  fbdiode  m m 0.5 ABSOLUTE
TRACE PROPERTY  r(resist)  pl pl 5e-10 ABSOLUTE
TRACE PROPERTY  r(resist)  plevel plevel 0.5 ABSOLUTE
TRACE PROPERTY  r(resist)  pw pw 5e-10 ABSOLUTE
TRACE PROPERTY  r(resist)  m m 0.5 ABSOLUTE
TRACE PROPERTY  r(brres)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  r(brres)  pbar pbar 0.5 ABSOLUTE
TRACE PROPERTY  r(brres)  s s 0.5 ABSOLUTE
TRACE PROPERTY  r(brres)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  r(brres)  m m 0.5 ABSOLUTE
TRACE PROPERTY  r(brres)  m1pb m1pb 0.5 ABSOLUTE
```

```
TRACE PROPERTY  c(vncap)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  c(vncap)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  c(vncap)  m m 0.5 ABSOLUTE
TRACE PROPERTY  c(vncap)  botlev botlev 0.5 ABSOLUTE
TRACE PROPERTY  c(vncap)  toplev toplev 0.5 ABSOLUTE
TRACE PROPERTY  r(sblkndres)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  r(sblkndres)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  r(sblkpdres)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  r(sblkpdres)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  lesd lesd 5e-10 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  wesd wesd 5e-10 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  esdoxide esdoxide 0.5 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  ldop ldop 5e-10 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  lsop lsop 5e-10 ABSOLUTE
TRACE PROPERTY  q(esdnsh)  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  esdscr_sblk  areapdt areapdt 1e-15 ABSOLUTE
TRACE PROPERTY  esdscr_sblk  perimpdt perimpdt 5e-10 ABSOLUTE
TRACE PROPERTY  esdscr_sblk  dac dac 5e-10 ABSOLUTE
TRACE PROPERTY  esdscr_sblk  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  esdscr_sblk  m m 0.5 ABSOLUTE
TRACE PROPERTY  esddiode  perimpd perimpd 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode  plpc plpc 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  esddiode  nfc nfc 0.5 ABSOLUTE
TRACE PROPERTY  esddiode  w w 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode  m m 0.5 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  perimpd perimpd 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  plpc plpc 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  nf nf 0.5 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  nfc nfc 0.5 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  w w 5e-10 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  nsblk nsblk 0.5 ABSOLUTE
TRACE PROPERTY  esddiode_sblk  m m 0.5 ABSOLUTE
TRACE PROPERTY  singlecpw  s s 5e-10 ABSOLUTE
TRACE PROPERTY  singlecpw  w w 5e-10 ABSOLUTE
TRACE PROPERTY  singlecpw  l l 5e-10 ABSOLUTE
TRACE PROPERTY  singlecpw  plane plane 0.5 ABSOLUTE
TRACE PROPERTY  singlecpw  layer_sig layer_sig 0.5 ABSOLUTE
TRACE PROPERTY  singlecpw  layer_top layer_top 0.5 ABSOLUTE
TRACE PROPERTY  singlecpw  layer_bot layer_bot 0.5 ABSOLUTE
TRACE PROPERTY  coupledcpw  d d 5e-10 ABSOLUTE
TRACE PROPERTY  coupledcpw  s s 5e-10 ABSOLUTE
TRACE PROPERTY  coupledcpw  w w 5e-10 ABSOLUTE
TRACE PROPERTY  coupledcpw  l l 5e-10 ABSOLUTE
TRACE PROPERTY  coupledcpw  plane plane 0.5 ABSOLUTE
TRACE PROPERTY  coupledcpw  layer_sig layer_sig 0.5 ABSOLUTE
TRACE PROPERTY  coupledcpw  layer_top layer_top 0.5 ABSOLUTE
TRACE PROPERTY  coupledcpw  layer_bot layer_bot 0.5 ABSOLUTE
TRACE PROPERTY  c(dtcellcap)  narray narray 0.5 ABSOLUTE
TRACE PROPERTY  c(dtdcap)  nrows nrows 0.5 ABSOLUTE
TRACE PROPERTY  c(dtdcap)  ncols ncols 0.5 ABSOLUTE
TRACE PROPERTY  c(dtdcap)  m m 0.5 ABSOLUTE
TRACE PROPERTY  r(rmimhk)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  r(rmimhk)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  r(rmimhk)  m m 0.5 ABSOLUTE
TRACE PROPERTY  r(rmimhksh)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  r(rmimhksh)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  r(rmimhksh)  m m 0.5 ABSOLUTE
TRACE PROPERTY  c(cmimhk)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  c(cmimhk)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  c(cmimhk)  m m 0.5 ABSOLUTE
TRACE PROPERTY  c(cmimhkhq)  l l 5e-10 ABSOLUTE
TRACE PROPERTY  c(cmimhkhq)  w w 5e-10 ABSOLUTE
TRACE PROPERTY  c(cmimhkhq)  m m 0.5 ABSOLUTE
TRACE PROPERTY  inds  w w 5e-10 ABSOLUTE
TRACE PROPERTY  inds  od od 5e-10 ABSOLUTE
TRACE PROPERTY  inds  turnspc turnspc 5e-10 ABSOLUTE
TRACE PROPERTY  inds  n n 0.5 ABSOLUTE
```

```
   TRACE PROPERTY  inds  bp bp 0.5 ABSOLUTE
   TRACE PROPERTY  symindp  w w 5e-10 ABSOLUTE
   TRACE PROPERTY  symindp  od od 5e-10 ABSOLUTE
   TRACE PROPERTY  symindp  wu wu 5e-10 ABSOLUTE
   TRACE PROPERTY  symindp  turnspc turnspc 5e-10 ABSOLUTE
   TRACE PROPERTY  symindp  n n 0.5 ABSOLUTE
   TRACE PROPERTY  symindp  tleval tleval 0.5 ABSOLUTE
   TRACE PROPERTY  symindp  tlevthkcu tlevthkcu 0.5 ABSOLUTE
   TRACE PROPERTY  symindp  bp bp 0.5 ABSOLUTE
```

CELL COMPARISON RESULTS (TOP LEVEL)



Warning: Ambiguity points were found and resolved arbitrarily.

LAYOUT CELL NAME: COUNTER_10b
SOURCE CELL NAME: COUNTER_10b

INITIAL NUMBERS OF OBJECTS

	Layout	Source		Component Type
Nets:	201	201		
Instances:	390	370	*	MD (4 pins)
Total Inst:	390	370		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Nets:	120	120	
Instances:	218	218	MD (4 pins)
	61	61	SMD2 (4 pins)
	10	10	SMD3 (5 pins)
Total Inst:	289	289	

* = Number of objects in layout different from number in source.

```
*****************************************************************************************************
*************
                                INFORMATION AND WARNINGS
*****************************************************************************************************
*************
```

	Matched Layout	Matched Source	Unmatched Layout	Unmatched Source	Component Type
Nets:	120	120	0	0	
Instances:	113	113	0	0	MD(d_mvtnfet)
	105	105	0	0	MD(d_mvtpfet)
	61	61	0	0	SMD2
	10	10	0	0	SMD3
Total Inst:	289	289	0	0	

o Statistics:

40 layout mos transistors were reduced to 20.
20 mos transistors were deleted by parallel reduction.

1 net was matched arbitrarily.

o Initial Correspondence Points:

Nets: vdd! gnd!

o Ambiguity Resolution Points:

(Each one of the following objects belongs to a group of indistinguishable objects.
The listed objects were matched arbitrarily by the Ambiguity Resolution feature of LVS.
Arbitrary matching may be prevented by assigning names to these objects or to adjacent nets).

Layout		Source
	Nets	
18		CLK_KILL

```
*****************************************************************************************************
*************
                                      SUMMARY
*****************************************************************************************************
*************

Total CPU Time:      1 sec
Total Elapsed Time:  1 sec
```

APPENDIX C:Encounter P&R log

```
Checking out Encounter license ...
Encounter_Digital_Impl_Sys_XL 9.1 license checkout succeeded.
You can run 2 CPU jobs with the base license that is currently checked out.
If required, use the setMultiCpuUsage command to enable multi-CPU processing.
This Encounter release has been compiled with OA version 22.04-p058.
****************************************************************
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*                    2655 Seely Avenue                           *
*                  San Jose, CA 95134,  USA                      *
*                                                                *
*                                                                *
****************************************************************

@(#)CDS: Encounter v09.11-s084_1 (32bit) 04/26/2010 12:41 (Linux 2.6)
@(#)CDS: NanoRoute v09.11-s008 NR100226-1806/USR63-UB (database version 2.30,
93.1.1) {superthreading v1.14}
@(#)CDS: CeltIC v09.11-s011_1 (32bit) 03/04/2010 09:23:40 (Linux 2.6.9-
78.0.25.ELsmp)
@(#)CDS: CTE 09.11-s016_1 (32bit) Apr  8 2010 03:34:50 (Linux 2.6.9-
78.0.25.ELsmp)
@(#)CDS: CPE v09.11-s023
--- Starting "Encounter v09.11-s084_1" on Mon May  2 11:21:51 2011
(mem=46.5M) ---
--- Running on sody.ece.umn.edu (x86_64 w/Linux 2.6.18-194.26.1.el5) ---
This version was compiled on Mon Apr 26 12:41:13 PDT 2010.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000
<CMD> loadConfig cmd/encounter/aes_cipher_top.conf
Reading config file - cmd/encounter/aes_cipher_top.conf
**WARN: (ENCEXT-1085):  Option 'rda_Input(ui_res_scale)' used in
configuration file 'cmd/encounter/aes_cipher_top.conf' is obsolete. The name
will be converted into new format automatically if design is saved and then
restored. Alternatively, update the configuration file to use names
'rda_Input(ui_preRoute_res)' and/or 'rda_Input(ui_postRoute_res)' for
resistance scale factors to be used at preRoute/postRoute stages of the
design . The obsolete name works in this release. But to avoid this warning
and to ensure compatibility with future releases, update this option name.
```

```
Loading Lef file cds.lef...
Set DBUPerIGU to M2 pitch 200.
Initializing default via types and wire widths ...
**WARN: (ENCLF-45):     Macro 'HS65_GSS1_FA1X21' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS1_FA1X35' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS1_FA1X9' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS1_HA1X8' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS2_FA1X18' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQNX18' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQNX27' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQNX35' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQX18' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQX27' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
```

```
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPHQX35' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQNX18' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQNX27' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQNX35' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQX18' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQX27' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPQX35' has no SITE statement and it
is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPRQNX18' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPRQNX27' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (ENCLF-45):     Macro 'HS65_GSS_DFPRQNX35' has no SITE statement and
it is a class
CORE macro that requires a SITE statement. The SITE CORE is
chosen because it is a core site with height 2.6000 that matches the macro
SIZE height.
**WARN: (EMS-62): Message <ENCLF-45> has exceeded the default message display
limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
```

```
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
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A layer must be defined before it can be referenced.
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A layer must be defined before it can be referenced.
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A layer must be defined before it can be referenced.
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A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
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**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**ERROR: (ENCLF-53):    The layer 'DCO' is not found in the database.
A layer must be defined before it can be referenced.
**WARN: (EMS-62): Message <ENCLF-53> has exceeded the default message display
limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LS_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
```

```
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LS_ANTPROT1' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LL_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LL_ANTPROT1' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LH_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_LH_ANTPROT1' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_GS_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_GL_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'MINUS' in macro 'HS65_GH_ANTPROT3' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'A' in macro 'CLOCKTREE' has no ANTENNAGATEAREA
attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'Z' in macro 'CLOCKTREE' has no ANTENNADIFFAREA
attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'A' in macro 'HS65_GS_XOR3X9' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'B' in macro 'HS65_GS_XOR3X9' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'C' in macro 'HS65_GS_XOR3X9' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
```

```
**WARN: (ENCLF-200):    Pin 'Z' in macro 'HS65_GS_XOR3X9' has no
ANTENNADIFFAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'A' in macro 'HS65_GS_XOR3X4' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'B' in macro 'HS65_GS_XOR3X4' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'C' in macro 'HS65_GS_XOR3X4' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'Z' in macro 'HS65_GS_XOR3X4' has no
ANTENNADIFFAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (ENCLF-200):    Pin 'A' in macro 'HS65_GS_XOR3X27' has no
ANTENNAGATEAREA attribute defined.
For any non-power/ground input or inout pin, The attribute should be
defined if any area ratio antenna attribute is defined on any layer.
**WARN: (EMS-62): Message <ENCLF-200> has exceeded the default message
display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.

Power Planner/ViaGen version 8.1.46 promoted on 02/17/2009.
viaInitial starts at Mon May  2 11:22:00 2011
viaInitial ends at Mon May  2 11:22:00 2011
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'src/netlist/aes_cipher_top.gates.v'
Inserting temporary buffers to remove assignment statements.

*** Memory Usage v0.159.2.6.2.1 (Current mem = 267.355M, initial mem =
46.480M) ***
*** End netlist parsing (cpu=0:00:00.1, real=0:00:00.0, mem=267.4M) ***
Set top cell to aes_cipher_top.
Reading max timing library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib' ...
 read 866 cells in library 'CORE65GPSVT'
Reading max timing library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib' ...
 read 110 cells in library 'CLOCK65GPSVT'
Reading max timing library 'LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib'
...
 read 10 cells in library 'PRHS65'
```

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Reading min timing library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_bc_1.10V_m40C.lib' ...
 read 866 cells in library 'CORE65GPSVT'
Reading min timing library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_bc_1.10V_m40C.lib' ...
 read 110 cells in library 'CLOCK65GPSVT'
Reading min timing library 'LIBRARIES/PRHS65/libs/PRHS65_bc_1.30V_m40C.lib'
...
 read 10 cells in library 'PRHS65'
Reading max timing library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.00, 25.00) of timing library
'CORE65GPSVT' does not match with previously read timing library of same name
with nominal PVT (1.20, 0.90, 125.00). To read this library change the
library name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' failed
Reading max timing library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.00, 25.00) of timing library
'CLOCK65GPSVT' does not match with previously read timing library of same
name with nominal PVT (1.20, 0.90, 125.00). To read this library change the
library name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' failed
Reading max timing library 'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib'
...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.20, 25.00) of timing library
'PRHS65' does not match with previously read timing library of same name with
nominal PVT (1.20, 1.10, 125.00). To read this library change the library
name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib' failed
Reading min timing library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.00, 25.00) of timing library
'CORE65GPSVT' does not match with previously read timing library of same name
with nominal PVT (0.80, 1.10, -40.00). To read this library change the
library name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' failed
Reading min timing library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.00, 25.00) of timing library
'CLOCK65GPSVT' does not match with previously read timing library of same
name with nominal PVT (0.80, 1.10, -40.00). To read this library change the
library name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' failed
Reading min timing library 'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib'
...
**ERROR: (ENCTS-296):   The nominal PVT (1.00, 1.20, 25.00) of timing library
'PRHS65' does not match with previously read timing library of same name with
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nominal PVT (0.80, 1.30, -40.00). To read this library change the library
name.
**ERROR: (TECHLIB-281): Attempt to read .lib library
'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib' failed
*** End library_loading (cpu=0.36min, mem=167.5M, fe_cpu=0.44min,
fe_mem=434.9M) ***
Starting recursive module instantiation check.
No recursion found.
Building hierarchical netlist for Cell aes_cipher_top ...
*** Netlist is unique.
** info: there are 2167 modules.
** info: there are 9809 stdCell insts.

*** Memory Usage v0.159.2.6.2.1 (Current mem = 435.117M, initial mem =
46.480M) ***
*info - Done with setDoAssign with 184 assigns removed and 0 assigns could
not be removed.
CTE reading timing constraint file 'src/sdc/aes_cipher_top.sdc' ...
aes_cipher_top
INFO (CTE): constraints read successfully
*** Read timing constraints (cpu=0:00:00.1 mem=439.4M) ***
Total number of combinational cells: 719
Total number of sequential cells: 255
Total number of tristate cells: 10
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: HS65_GS_CNBFX10 HS65_GS_CNBFX103 HS65_GS_CNBFX124
HS65_GS_CNBFX14 HS65_GS_CNBFX21 HS65_GS_CNBFX17 HS65_GS_CNBFX27
HS65_GS_CNBFX24 HS65_GS_CNBFX34 HS65_GS_CNBFX31 HS65_GS_CNBFX38
HS65_GS_CNBFX41 HS65_GS_CNBFX48 HS65_GS_CNBFX45 HS65_GS_CNBFX55
HS65_GS_CNBFX52 HS65_GS_CNBFX62 HS65_GS_CNBFX58 HS65_GS_CNBFX82
HS65_GS_DLYIC2X4 HS65_GS_DLYIC2X9 HS65_GS_DLYIC2X7 HS65_GS_BFX13
HS65_GS_BFX106 HS65_GS_BFX142 HS65_GS_BFX2 HS65_GS_BFX18 HS65_GS_BFX213
HS65_GS_BFX27 HS65_GS_BFX22 HS65_GS_BFX284 HS65_GS_BFX31 HS65_GS_BFX4
HS65_GS_BFX35 HS65_GS_BFX44 HS65_GS_BFX40 HS65_GS_BFX53 HS65_GS_BFX49
HS65_GS_BFX62 HS65_GS_BFX9 HS65_GS_BFX7 HS65_GS_BFX71
Total number of usable buffers: 42
List of unusable buffers: CLOCKTREE
Total number of unusable buffers: 1
List of usable inverters: HS65_GS_CNIVX10 HS65_GS_CNIVX103 HS65_GS_CNIVX124
HS65_GS_CNIVX14 HS65_GS_CNIVX21 HS65_GS_CNIVX17 HS65_GS_CNIVX24
HS65_GS_CNIVX3 HS65_GS_CNIVX27 HS65_GS_CNIVX34 HS65_GS_CNIVX31
HS65_GS_CNIVX41 HS65_GS_CNIVX38 HS65_GS_CNIVX48 HS65_GS_CNIVX45
HS65_GS_CNIVX55 HS65_GS_CNIVX52 HS65_GS_CNIVX58 HS65_GS_CNIVX7
HS65_GS_CNIVX62 HS65_GS_CNIVX82 HS65_GS_IVX13 HS65_GS_IVX106 HS65_GS_IVX142
HS65_GS_IVX2 HS65_GS_IVX18 HS65_GS_IVX213 HS65_GS_IVX27 HS65_GS_IVX22
HS65_GS_IVX284 HS65_GS_IVX31 HS65_GS_IVX4 HS65_GS_IVX35 HS65_GS_IVX44
HS65_GS_IVX40 HS65_GS_IVX53 HS65_GS_IVX49 HS65_GS_IVX62 HS65_GS_IVX9
HS65_GS_IVX7 HS65_GS_IVX71
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Total number of usable inverters: 41
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells: HS65_GS_DLYIC4X4 HS65_GS_DLYIC4X9
HS65_GS_DLYIC4X7 HS65_GS_DLYIC6X4 HS65_GS_DLYIC6X7 HS65_GS_DLYIC6X9
Total number of identified usable delay cells: 6
List of identified unusable delay cells: HS65_GS_CNBFX38_0 HS65_GS_CNBFX38_1
HS65_GS_CNBFX38_10 HS65_GS_CNBFX38_11 HS65_GS_CNBFX38_12 HS65_GS_CNBFX38_13
HS65_GS_CNBFX38_14 HS65_GS_CNBFX38_15 HS65_GS_CNBFX38_16 HS65_GS_CNBFX38_17
HS65_GS_CNBFX38_18 HS65_GS_CNBFX38_19 HS65_GS_CNBFX38_2 HS65_GS_CNBFX38_20
HS65_GS_CNBFX38_21 HS65_GS_CNBFX38_22 HS65_GS_CNBFX38_23 HS65_GS_CNBFX38_3
HS65_GS_CNBFX38_4 HS65_GS_CNBFX38_5 HS65_GS_CNBFX38_6 HS65_GS_CNBFX38_7
HS65_GS_CNBFX38_8 HS65_GS_CNBFX38_9
Total number of identified unusable delay cells: 24
*info: set bottom ioPad orient R0
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Set Input Pin Transition Delay as 0.1 ps.
PreRoute Cap Scale Factor :        1.00
PreRoute Res Scale Factor :        1.00
PostRoute Cap Scale Factor :       1.00
PostRoute Res Scale Factor :       1.00
PostRoute XCap Scale Factor :      1.00

PreRoute Clock Cap Scale Factor :  1.00   [Derived from postRoute_cap
(effortLevel low)]
PreRoute Clock Res Scale Factor :  1.00   [Derived from postRoute_res
(effortLevel low)]
PostRoute Clock Cap Scale Factor : 1.00   [Derived from postRoute_cap
(effortLevel low)]
PostRoute Clock Res Scale Factor : 1.00   [Derived from postRoute_res
(effortLevel low)]
**WARN: (ENCOPT-3465):  The buffer cells were automatically identified. The
command setBufFootPrint is ignored. If you want to force the tool to honor
this setting, you have to load a footprint file through the loadFootPrint
command.
**WARN: (ENCOPT-3466):  The inverter cells were automatically identified. The
command setInvFootPrint is ignored. If you want to force the tool to honor
this setting, you have to load a footprint file through the loadFootPrint
command.
**WARN: (ENCOPT-3467):  The delay cells were automatically identified. The
command setDelayFootPrint is ignored. If you want to force the tool to honor
this setting, you have to load a footprint file through the loadFootPrint
command.
<CMD> commitConfig
**WARN: (ENCSYT-3034):  commitConfig can only be run once per session.
 This command is skipped since it's already run by user or by loadConfig
command implicitly.
<CMD_INTERNAL> setCteReport
<CMD> setAnalysisMode -setup -async -skew -autoDetectClockTree
**WARN: (ENCTCM-70):    Option "-setup" for command setAnalysisMode is
obsolete and has been replaced by "-checkType setup". The obsolete option
still works in this release, but to avoid this warning and to ensure
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compatibility with future releases, update your script to use "-checkType
setup".
**WARN: (ENCTCM-70):    Option "-async" for command setAnalysisMode is
obsolete and has been replaced by "-asyncChecks async". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-asyncChecks
async".
**WARN: (ENCTCM-70):    Option "-skew" for command setAnalysisMode is
obsolete and has been replaced by "-skew true". The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use "-skew true".
**WARN: (ENCTCM-70):    Option "-autoDetectClockTree" for command
setAnalysisMode is obsolete and has been replaced by "-clockPropagation
autoDetectClockTree". The obsolete option still works in this release, but to
avoid this warning and to ensure compatibility with future releases, update
your script to use "-clockPropagation autoDetectClockTree".
**WARN: (ENCSYC-1870):  setAnalysisMode -clockPropagation autoDetectClockTree
not supported in CTE timing mode, mapping it to setAnalysisMode -
clockPropagation sdcControl
{DETAILMESSAGE}<CMD> buildTimingGraph -ignoreNetLoad
<CMD> check_timing -verbose > $rpt_dir/check_timing
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 453.4M)
Number of Loop : 0
Start delay calculation (mem=453.398M)...
Delay calculation completed. (cpu=0:00:01.1 real=0:00:01.0 mem=458.566M 0)
*** CDM Built up (cpu=0:00:01.8  real=0:00:02.0  mem= 458.6M) ***
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary > $rpt_dir/report_timing.initial.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net > $rpt_dir/report_timing.initial.slack
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
net  > $rpt_dir/report_timing.initial.crit_path
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary > $rpt_dir/report_timing.initial.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> floorPlan -s 200 200 10.12 10.25 10 10
Adjusting Core to Left to: 10.2000. Core to Bottom to: 10.4000.
<CMD> deselectAll
<CMD> addRing -width_left 2 -width_bottom 2 -width_top 2 -width_right 2 -
spacing_bottom 2 -spacing_top 2 -spacing_left 2 -spacing_right 2 -
layer_bottom M5 -layer_top M5 -layer_right M6 -layer_left M6 -nets {VDD VSS}


The power planner created 8 wires.
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<CMD> addRing -width_left 2 -width_bottom 2 -width_top 2 -width_right 2 -
spacing_bottom 2 -spacing_top 2 -spacing_left 2 -spacing_right 2 -
layer_bottom M5 -layer_top M5 -layer_right M6 -layer_left M6 -nets {VDD VSS}
-around each_block -type block_rings



<CMD> addStripe -width 1 -set_to_set_distance 50 -layer M2 -spacing 0.5 -nets
{VDD VSS}
**WARN: (ENCPP-2008):   AddStripe option -remove_floating_stripe_over_block
is ON so all fragmented stripes within a block will be removed.
  To turn OFF, setAddStripeOption -remove_floating_stripe_over_block 0.

Starting stripe generation ...
Stripe generation is complete.

The power planner created 8 wires.

<CMD> placeDesign -inPlaceOpt
*** Starting placeDesign concurrent flow ***
*** Start deleteBufferTree ***
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 458.9M)
Number of Loop : 0
Start delay calculation (mem=458.910M)...
Delay calculation completed. (cpu=0:00:01.2 real=0:00:02.0 mem=459.082M 0)
*** CDM Built up (cpu=0:00:01.9  real=0:00:02.0  mem= 459.1M) ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist
*summary: 312 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:02.2) ***
Extracting standard cell pins and blockage ......
Pin and blockage extraction finished
Extracting macro/IO cell pins and blockage ......
Pin and blockage extraction finished
*** Starting "NanoPlace(TM) placement v0.892.2.8.2.1 (mem=459.2M)" ...
*** Build Buffered Sizing Timing Model (Used Compact Buffer Set)
...(cpu=0:00:06.4 mem=515.0M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:09.9 mem=544.7M) ***
Options: timingDriven ignoreScan ignoreSpare pinGuide gpeffort=medium
**WARN: (ENCDB-2082):   Scan chains were not defined, -ignoreScan option will
be ignored.
Please first define the scan chains before using this option.
#std cell=9497 #block=0 (0 floating + 0 preplaced) #ioInst=0 #net=9756
#term=39950 #term/net=4.09, #fixedIo=0, #floatIo=0, #fixedPin=0,
#floatPin=388
stdCell: 9497 single + 0 double + 0 multi
Total standard cell length = 13.0892 (mm), area = 0.0340 (mm^2)
Average module density = 0.908.
Density for the design = 0.908.
       = stdcell_area 65446 (34032 um^2) / alloc_area 72048 (37465 um^2).
Pin Density = 0.610.
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           = total # of pins 39950 / total Instance area 65446.
Iteration  1: Total net bbox = 1.365e-09 (1.04e-09 3.24e-10)
               Est.  stn bbox = 1.365e-09 (1.04e-09 3.24e-10)
               cpu = 0:00:00.0 real = 0:00:00.0 mem = 550.0M
Iteration  2: Total net bbox = 1.365e-09 (1.04e-09 3.24e-10)
               Est.  stn bbox = 1.365e-09 (1.04e-09 3.24e-10)
               cpu = 0:00:00.0 real = 0:00:00.0 mem = 550.0M
Iteration  3: Total net bbox = 4.430e+02 (4.43e+02 7.38e-10)
               Est.  stn bbox = 4.430e+02 (4.43e+02 7.38e-10)
               cpu = 0:00:00.2 real = 0:00:00.0 mem = 550.0M
Iteration  4: Total net bbox = 5.537e+04 (2.71e+04 2.83e+04)
               Est.  stn bbox = 5.537e+04 (2.71e+04 2.83e+04)
               cpu = 0:00:05.9 real = 0:00:06.0 mem = 550.0M
Iteration  5: Total net bbox = 5.060e+04 (2.50e+04 2.56e+04)
               Est.  stn bbox = 5.060e+04 (2.50e+04 2.56e+04)
               cpu = 0:00:02.5 real = 0:00:02.0 mem = 550.0M
Iteration  6: Total net bbox = 1.285e+05 (6.78e+04 6.07e+04)
               Est.  stn bbox = 1.285e+05 (6.78e+04 6.07e+04)
               cpu = 0:00:02.8 real = 0:00:03.0 mem = 550.1M
Iteration  7: Total net bbox = 1.552e+05 (8.06e+04 7.46e+04)
               Est.  stn bbox = 1.891e+05 (9.92e+04 8.99e+04)
               cpu = 0:00:12.2 real = 0:00:12.0 mem = 549.2M
Iteration  8: Total net bbox = 1.552e+05 (8.06e+04 7.46e+04)
               Est.  stn bbox = 1.891e+05 (9.92e+04 8.99e+04)
               cpu = 0:00:05.2 real = 0:00:05.0 mem = 549.2M
Iteration  9: Total net bbox = 1.802e+05 (9.10e+04 8.92e+04)
               Est.  stn bbox = 2.234e+05 (1.14e+05 1.09e+05)
               cpu = 0:00:03.2 real = 0:00:03.0 mem = 550.3M
Iteration 10: Total net bbox = 1.802e+05 (9.10e+04 8.92e+04)
               Est.  stn bbox = 2.234e+05 (1.14e+05 1.09e+05)
               cpu = 0:00:05.2 real = 0:00:05.0 mem = 550.3M
Iteration 11: Total net bbox = 1.833e+05 (8.85e+04 9.48e+04)
               Est.  stn bbox = 2.274e+05 (1.11e+05 1.16e+05)
               cpu = 0:00:04.0 real = 0:00:04.0 mem = 550.6M
Iteration 12: Total net bbox = 1.880e+05 (9.18e+04 9.62e+04)
               Est.  stn bbox = 2.328e+05 (1.15e+05 1.18e+05)
               cpu = 0:00:00.0 real = 0:00:01.0 mem = 550.6M
*** cost = 1.880e+05 (9.18e+04 9.62e+04) (cpu for global=0:00:29.9)
real=0:00:30.0***
Core Placement runtime cpu: 0:00:19.2 real: 0:00:19.0
Starting refinePlace ...
move report: placeLevelShifters moves 0 insts, mean move: 0.00 um, max move:
0.00 um
  Spread Effort: high, pre-route mode. (cpu=0:00:03.7, real=0:00:03.0)
move report: preRPlace moves 8424 insts, mean move: 1.14 um, max move: 10.00
um
      max move on inst (us00/U96): (31.40, 10.40) --> (26.60, 15.60)
Placement tweakage begins.
wire length = 1.933e+05 = 9.607e+04 H + 9.728e+04 V
wire length = 1.888e+05 = 9.282e+04 H + 9.601e+04 V
Placement tweakage ends.
move report: wireLenOpt moves 5034 insts, mean move: 2.74 um, max move: 37.40
um
      max move on inst (us20/U6): (78.00, 200.20) --> (84.20, 169.00)
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move report: rPlace moves 8840 insts, mean move: 2.33 um, max move: 38.60 um
      max move on inst (us00/U298): (57.00, 31.20) --> (74.80, 10.40)
Statistics of distance of Instance movement in detailed placement:
  maximum (X+Y) =        38.60 um
  inst (us00/U298) with max move: (57, 31.2) -> (74.8, 10.4)
  mean    (X+Y) =         2.33 um
Total instances moved : 8840
*** cpu=0:00:04.7   mem=552.9M  mem(used)=2.3M***
Total net length = 1.910e+05 (9.429e+04 9.667e+04) (ext = 2.151e+04)
*** End of Placement (cpu=0:00:46.4, real=0:00:46.0, mem=552.9M) ***
default core: bins with density >  0.75 = 93.8 % ( 60 / 64 )
*** Free Virtual Timing Model ...(mem=542.4M)
Starting IO pin assignment...
Completed IO pin assignment.
**WARN: (ENCSP-9025):   No scan chain specified/traced.
setAnalysisMode  -domain allClockDomain -checkType setup -skew true -
usefulSkew false -log true -warn true -caseAnalysis true -sequentialConstProp
false -moduleIOCstr true -clockPropagation forcedIdeal -clkSrcPath false -
timingSelfLoopsNoSkew false -asyncChecks async -useOutputPinCap true -latch
true -latchDelayCalIteration 2 -timeBorrowing true -latchFullDelayCal false -
clockGatingCheck true -enableMultipleDriveNet true -analysisType bcWc -cppr
false -clkNetsMarking beforeConstProp -honorVirtualPartition false -
honorClockDomains true
**optDesign ... cpu = 0:00:00, real = 0:00:00, mem = 542.4M **
Added -handlePreroute to trialRouteMode
*** optDesign -preCTS ***
DRC Margin: user margin 0.0; extra margin 0.2
Setup Target Slack: user slack 0.0; extra slack 0.1
Hold Target Slack: user slack 0.0
*info: Setting setup target slack to 0.100
*info: Hold target slack is 0.000
*** CTE mode ***
*** Starting trialRoute (mem=542.4M) ***

There are 0 pin guide points passed to trialRoute.
Options:  -handlePreroute -noPinGuide

Nr of prerouted/Fixed nets = 0
routingBox: (0 0) (220200 220400)
coreBox:    (10200 10400) (210200 210400)

Phase 1a route (0:00:00.1 542.4M):
Est net length = 2.409e+05um = 1.191e+05H + 1.218e+05V
Usage: (26.6%H 38.9%V) = (1.345e+05um 2.130e+05um) = (133865 82260)
Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
Overflow: 31 = 0 (0.00% H) + 31 (0.17% V)

Phase 1b route (0:00:00.1 542.4M):
Usage: (26.6%H 38.9%V) = (1.342e+05um 2.130e+05um) = (133501 82260)
Overflow: 17 = 0 (0.00% H) + 17 (0.09% V)

Phase 1c route (0:00:00.1 542.4M):
Usage: (26.5%H 39.0%V) = (1.339e+05um 2.134e+05um) = (133194 82404)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)
```

```
Phase 1d route (0:00:00.1 542.4M):
Usage: (26.5%H 39.0%V) = (1.339e+05um 2.134e+05um) = (133200 82408)
Overflow: 7 = 0 (0.00% H) + 7 (0.04% V)

Phase 1e route (0:00:00.0 542.4M):
Usage: (26.5%H 39.0%V) = (1.338e+05um 2.134e+05um) = (133182 82413)
Overflow: 5 = 0 (0.00% H) + 5 (0.03% V)

Phase 1f route (0:00:00.0 542.4M):
Usage: (26.5%H 39.0%V) = (1.338e+05um 2.134e+05um) = (133181 82421)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Congestion distribution:

Remain      cntH        cntV
------------------------------------
------------------------------------
  0:  0      0.00%      70     0.38%
  1:  0      0.00%      366    2.00%
  2:  24     0.13%      895    4.89%
  3:  0      0.00%      1693   9.25%
  4:  2      0.01%      2566  14.02%
  5:  6      0.03%      2242  12.25%
  6:  7      0.04%      2371  12.95%
  7:  31     0.17%      1854  10.13%
  8:  31     0.17%      1267   6.92%
  9:  56     0.31%      1110   6.06%
 10:  700    3.82%      855    4.67%
 11:  172    0.94%      1776   9.70%
 12:  696    3.80%      535    2.92%
 13:  389    2.13%      0      0.00%
 14:  595    3.25%      0      0.00%
 15:  782    4.27%      0      0.00%
 16:  1270   6.94%      0      0.00%
 17:  971    5.30%      0      0.00%
 18:  1535   8.39%      0      0.00%
 19:  1286   7.03%      0      0.00%
 20:  9751  53.27%      704    3.85%


Global route (cpu=0.4s real=0.0s 542.4M)
Phase 1l route (0:00:00.6 542.4M):


*** After '-updateRemainTrks' operation:

Usage: (28.1%H 43.3%V) = (1.421e+05um 2.370e+05um) = (141235 91532)
Overflow: 115 = 0 (0.00% H) + 115 (0.63% V)

Congestion distribution:

Remain      cntH        cntV
------------------------------------
```

```
 -2:  0      0.00%      11     0.06%
 -1:  0      0.00%      99     0.54%
---------------------------------------
  0:  0      0.00%      442    2.41%
  1:  0      0.00%      904    4.94%
  2:  24     0.13%      1509   8.24%
  3:  1      0.01%      2000  10.93%
  4:  3      0.02%      2098  11.46%
  5:  11     0.06%      1803   9.85%
  6:  19     0.10%      2002  10.94%
  7:  43     0.23%      1510   8.25%
  8:  54     0.30%      1096   5.99%
  9:  99     0.54%      1026   5.61%
 10:  763    4.17%      872    4.76%
 11:  266    1.45%      1714   9.36%
 12:  758    4.14%      514    2.81%
 13:  523    2.86%      0      0.00%
 14:  708    3.87%      0      0.00%
 15:  844    4.61%      0      0.00%
 16:  1354   7.40%      0      0.00%
 17:  1033   5.64%      0      0.00%
 18:  1481   8.09%      0      0.00%
 19:  1276   6.97%      0      0.00%
 20:  9044  49.41%      704    3.85%


*** Completed Phase 1 route (0:00:01.1 542.4M) ***


Total length: 2.639e+05um, number of vias: 97526
M1(H) length: 5.145e+03um, number of vias: 39562
M2(V) length: 6.714e+04um, number of vias: 37786
M3(H) length: 9.416e+04um, number of vias: 15813
M4(V) length: 6.860e+04um, number of vias: 3714
M5(H) length: 2.550e+04um, number of vias: 636
M6(V) length: 3.296e+03um, number of vias: 15
M7(H) length: 7.000e+00um
*** Completed Phase 2 route (0:00:00.9 542.4M) ***

*** Finished all Phases (cpu=0:00:02.1 mem=542.4M) ***
Peak Memory Usage was 542.4M
*** Finished trialRoute (cpu=0:00:02.1 mem=542.4M) ***

Extraction called for design 'aes_cipher_top' of instances=9497 and nets=9942
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
```

```
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.1  Real Time: 0:00:00.0  MEM:
542.414M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 542.4M)
Number of Loop : 0
Start delay calculation (mem=542.414M)...
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via1_HV' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via2' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via3' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via4' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via5' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
**WARN: (ENCEXT-2882):  Unable to find resistance for via 'CDS_via6' in
capacitance table or LEF files. Check the capacitance table and LEF files.
Assigning default value of 4.0 ohms.
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=542.414M 0)
*** CDM Built up (cpu=0:00:02.4  real=0:00:03.0  mem= 542.4M) ***
Info: 1 clock net  excluded from IPO operation.

Netlist preparation processing...
Removed 0 instance
*info: Marking 0 isolation instances dont touch
*info: Marking 0 level shifter instances dont touch
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
*** Starting delays update (0:01:25 mem=542.4M) ***
*** Finished delays update (0:01:28 mem=542.4M) ***
**optDesign ... cpu = 0:00:09, real = 0:00:09, mem = 542.4M **
************ Recovering area ***************
Info: 1 clock net  excluded from IPO operation.
*** Starting Area Reclaim ***
** Density before area reclaim = 90.077% **
```

```
*** starting 1-st reclaim pass: 8695 instances
*** starting 2-nd reclaim pass: 8695 instances


** Area Reclaim Summary: Buffer Deletion = 0 Declone = 0 Downsize = 0 **
** Density Change = 0.000% **
** Density after area reclaim = 90.077% **
*** Finished Area Reclaim (0:00:01.4) ***
*** Starting sequential cell resizing ***
density before resizing = 90.077%
*summary:      0 instances changed cell type
density after resizing = 90.077%
*** Finish sequential cell resizing (cpu=0:00:00.6 mem=542.4M) ***
Re-routed 0 nets
Extraction called for design 'aes_cipher_top' of instances=9497 and nets=9942
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0  MEM:
542.414M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 542.4M)
Number of Loop : 0
Start delay calculation (mem=542.414M)...
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=542.414M 0)
*** CDM Built up (cpu=0:00:02.5  real=0:00:03.0  mem= 542.4M) ***
**optDesign ... cpu = 0:00:14, real = 0:00:14, mem = 542.4M **
*info: Start fixing DRV (Mem = 542.41M) ...
*info: Options = -maxCap -maxTran -noMaxFanout -sensitivity -backward -
reduceBuffer -maxIter 1
*info: Start fixing DRV iteration 1 ...
*** Starting dpFixDRCViolation (542.4M)
*info: 1 clock net excluded
*info: 2 special nets excluded.
*info: 186 no-driver nets excluded.
*** Starting multi-driver net buffering ***
*summary: 0 non-ignored multi-driver nets.
*** Finished buffering multi-driver nets (CPU=0:00:00.3, MEM=542.4M) ***
*info: There are 20 candidate Buffer cells
*info: There are 20 candidate Inverter cells
Initializing placement sections/sites ...
```

```
Density before buffering = 0.900765
Start fixing design rules ... (0:00:00.3 542.4M)
Done fixing design rule (0:00:06.3 542.4M)

Summary:
2 buffers added on 2 nets (with 231 drivers resized)

Density after buffering = 0.904316
*** Completed dpFixDRCViolation (0:00:06.6 542.4M)

Re-routed 233 nets
Extraction called for design 'aes_cipher_top' of instances=9499 and nets=9944
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0  MEM:
542.414M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 542.4M)
Number of Loop : 0
Start delay calculation (mem=542.414M)...
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=542.414M 0)
*** CDM Built up (cpu=0:00:02.4  real=0:00:03.0  mem= 542.4M) ***
*info: DRV Fixing Iteration 1.
*info: Remaining violations:
*info:   Max cap violations:    0
*info:   Max tran violations:   0
*info:   Prev Max cap violations:    81
*info:   Prev Max tran violations:   1939
*info:
*info: Completed fixing DRV (CPU Time = 0:00:10, Mem = 542.41M).
**optDesign ... cpu = 0:00:24, real = 0:00:24, mem = 542.4M **
*** Starting optFanout (542.4M)
*info: 1 clock net excluded
*info: 2 special nets excluded.
*info: 186 no-driver nets excluded.
*** Starting multi-driver net buffering ***
*summary: 0 non-ignored multi-driver nets.
*** Finished buffering multi-driver nets (CPU=0:00:00.3, MEM=542.4M) ***
Start fixing timing ... (0:00:00.3 542.4M)
```

```
Start clock batches slack = -0.073ns
End batches slack = 0.100ns
*info: Buffered 0 large fanout net (> 100 terms)
Done fixing timing (0:00:02.2 542.4M)

Summary:
43 buffers added on 43 nets (with 7 drivers resized)

Density after buffering = 0.912409
*** Completed optFanout (0:00:02.5 542.4M)

Re-routed 0 nets
Extraction called for design 'aes_cipher_top' of instances=9542 and nets=9987
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0  MEM:
542.414M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 542.4M)
Number of Loop : 0
Start delay calculation (mem=542.414M)...
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=542.414M 0)
*** CDM Built up (cpu=0:00:02.4  real=0:00:02.0  mem= 542.4M) ***
**optDesign ... cpu = 0:00:29, real = 0:00:29, mem = 542.4M **
*** Timing Is met
*** Check timing (0:00:00.3)
************ Recovering area ***************
Info: 1 clock net  excluded from IPO operation.
*** Starting Area Reclaim ***
** Density before area reclaim = 91.241% **

*** starting 1-st reclaim pass: 9012 instances
*** starting 2-nd reclaim pass: 9012 instances
*** starting 3-rd reclaim pass: 3112 instances
*** starting 4-th reclaim pass: 675 instances
*** starting 5-th reclaim pass: 25 instances


** Area Reclaim Summary: Buffer Deletion = 0 Declone = 0 Downsize = 157 **
** Density Change = 0.736% **
```

```
** Density after area reclaim = 90.505% **
*** Finished Area Reclaim (0:00:05.3) ***
*** Starting trialRoute (mem=542.4M) ***

There are 0 pin guide points passed to trialRoute.
Options:  -handlePreroute -keepMarkedOptRoutes -noPinGuide

Nr of prerouted/Fixed nets = 0
routingBox: (0 0) (220200 220400)
coreBox:    (10200 10400) (210200 210400)

Phase 1a route (0:00:00.1 542.4M):
Est net length = 2.409e+05um = 1.191e+05H + 1.218e+05V
Usage: (26.6%H 39.0%V) = (1.345e+05um 2.133e+05um) = (133834 82370)
Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
Overflow: 29 = 0 (0.00% H) + 29 (0.16% V)

Phase 1b route (0:00:00.1 542.4M):
Usage: (26.6%H 39.0%V) = (1.341e+05um 2.133e+05um) = (133467 82370)
Overflow: 23 = 0 (0.00% H) + 23 (0.12% V)

Phase 1c route (0:00:00.1 542.4M):
Usage: (26.5%H 39.0%V) = (1.338e+05um 2.137e+05um) = (133173 82530)
Overflow: 18 = 0 (0.00% H) + 18 (0.10% V)

Phase 1d route (0:00:00.1 542.4M):
Usage: (26.5%H 39.0%V) = (1.338e+05um 2.137e+05um) = (133181 82535)
Overflow: 6 = 0 (0.00% H) + 6 (0.03% V)

Phase 1e route (0:00:00.0 542.4M):
Usage: (26.5%H 39.1%V) = (1.338e+05um 2.138e+05um) = (133131 82556)
Overflow: 3 = 0 (0.00% H) + 3 (0.02% V)

Phase 1f route (0:00:00.1 542.4M):
Usage: (26.5%H 39.1%V) = (1.338e+05um 2.138e+05um) = (133136 82557)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Congestion distribution:

Remain      cntH        cntV
-----------------------------------------
-----------------------------------------
  0:  0      0.00%      79     0.43%
  1:  0      0.00%      365    1.99%
  2:  24     0.13%      888    4.85%
  3:  0      0.00%      1718   9.39%
  4:  4      0.02%      2560  13.99%
  5:  3      0.02%      2230  12.18%
  6:  11     0.06%      2389  13.05%
  7:  29     0.16%      1828   9.99%
  8:  32     0.17%      1301   7.11%
  9:  54     0.30%      1078   5.89%
 10:  689    3.76%      854    4.67%
 11:  148    0.81%      1776   9.70%
```

```
 12:  697    3.81%      534    2.92%
 13:  402    2.20%      0      0.00%
 14:  625    3.41%      0      0.00%
 15:  769    4.20%      0      0.00%
 16:  1305   7.13%      0      0.00%
 17:  974    5.32%      0      0.00%
 18:  1509   8.24%      0      0.00%
 19:  1251   6.83%      0      0.00%
 20:  9778  53.42%      704    3.85%


Global route (cpu=0.4s real=0.0s 542.4M)
Phase 1l route (0:00:00.8 542.4M):


*** After '-updateRemainTrks' operation:

Usage: (28.1%H 43.4%V) = (1.421e+05um 2.375e+05um) = (141254 91704)
Overflow: 129 = 0 (0.00% H) + 129 (0.71% V)

Congestion distribution:

Remain      cntH        cntV
-------------------------------------
 -3:  0      0.00%      1      0.01%
 -2:  0      0.00%      9      0.05%
 -1:  0      0.00%      115    0.63%
-------------------------------------
  0:  0      0.00%      414    2.26%
  1:  0      0.00%      927    5.06%
  2:  24     0.13%      1535   8.39%
  3:  1      0.01%      1976  10.80%
  4:  8      0.04%      2091  11.42%
  5:  9      0.05%      1824   9.97%
  6:  19     0.10%      2000  10.93%
  7:  40     0.22%      1516   8.28%
  8:  52     0.28%      1089   5.95%
  9:  84     0.46%      1009   5.51%
 10:  762    4.16%      864    4.72%
 11:  256    1.40%      1717   9.38%
 12:  747    4.08%      513    2.80%
 13:  552    3.02%      0      0.00%
 14:  760    4.15%      0      0.00%
 15:  825    4.51%      0      0.00%
 16:  1367   7.47%      0      0.00%
 17:  1028   5.62%      0      0.00%
 18:  1436   7.85%      0      0.00%
 19:  1246   6.81%      0      0.00%
 20:  9088  49.65%      704    3.85%


*** Completed Phase 1 route (0:00:01.2 542.4M) ***
```

```
Total length: 2.639e+05um, number of vias: 97800
M1(H) length: 5.161e+03um, number of vias: 39652
M2(V) length: 6.689e+04um, number of vias: 37846
M3(H) length: 9.382e+04um, number of vias: 15863
M4(V) length: 6.883e+04um, number of vias: 3805
M5(H) length: 2.577e+04um, number of vias: 619
M6(V) length: 3.444e+03um, number of vias: 15
M7(H) length: 7.000e+00um
*** Completed Phase 2 route (0:00:00.9 542.4M) ***

*** Finished all Phases (cpu=0:00:02.2 mem=542.4M) ***
Peak Memory Usage was 542.4M
*** Finished trialRoute (cpu=0:00:02.3 mem=542.4M) ***

Extraction called for design 'aes_cipher_top' of instances=9542 and nets=9987
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.1  Real Time: 0:00:01.0  MEM:
542.414M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 542.4M)
Number of Loop : 0
Start delay calculation (mem=542.414M)...
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=542.414M 0)
*** CDM Built up (cpu=0:00:02.4  real=0:00:02.0  mem= 542.4M) ***
**optDesign ... cpu = 0:00:40, real = 0:00:40, mem = 542.4M **
*** Timing NOT met, worst failing slack is 0.025
*** Check timing (0:00:00.3)
**optDesign ... cpu = 0:00:41, real = 0:00:40, mem = 542.4M **
setClockDomains -fromType register -toType register
**WARN: (ENCCTE-318):   Paths not in the reg2reg domain will be added 1000ns
slack adjustment
*** Timing Is met
*** Check timing (0:00:00.7)
**optDesign ... cpu = 0:00:42, real = 0:00:42, mem = 542.4M **
*** Finished optDesign ***
*** Starting "NanoPlace(TM) placement v0.892.2.8.2.1 (mem=542.4M)" ...
*** Build Buffered Sizing Timing Model (Used Compact Buffer Set)
...(cpu=0:00:06.3 mem=542.4M) ***
```

```
*** Build Virtual Sizing Timing Model
(cpu=0:00:09.8 mem=542.4M) ***
Options: timingDriven ignoreSpare pinGuide gpeffort=medium
#std cell=9542 #block=0 (0 floating + 0 preplaced) #ioInst=0 #net=9801
#term=40040 #term/net=4.09, #fixedIo=0, #floatIo=0, #fixedPin=0,
#floatPin=388
stdCell: 9542 single + 0 double + 0 multi
Total standard cell length = 13.1514 (mm), area = 0.0342 (mm^2)
Average module density = 0.913.
Density for the design = 0.913.
       = stdcell_area 65757 (34194 um^2) / alloc_area 72048 (37465 um^2).
Pin Density = 0.609.
            = total # of pins 40040 / total Instance area 65757.
Iteration 12: Total net bbox = 1.900e+05 (9.49e+04 9.51e+04)
              Est.  stn bbox = 2.358e+05 (1.19e+05 1.17e+05)
              cpu = 0:00:05.3 real = 0:00:05.0 mem = 555.3M
Iteration 13: Total net bbox = 1.834e+05 (8.86e+04 9.48e+04)
              Est.  stn bbox = 2.278e+05 (1.12e+05 1.16e+05)
              cpu = 0:00:02.8 real = 0:00:03.0 mem = 556.7M
Iteration 14: Total net bbox = 1.914e+05 (9.55e+04 9.59e+04)
              Est.  stn bbox = 2.364e+05 (1.19e+05 1.17e+05)
              cpu = 0:00:00.3 real = 0:00:00.0 mem = 555.4M
*** cost = 1.914e+05 (9.55e+04 9.59e+04) (cpu for global=0:00:08.4)
real=0:00:08.0***
Core Placement runtime cpu: 0:00:02.8 real: 0:00:03.0
Starting refinePlace ...
move report: placeLevelShifters moves 0 insts, mean move: 0.00 um, max move:
0.00 um
  Spread Effort: high, pre-route mode. (cpu=0:00:04.4, real=0:00:05.0)
move report: preRPlace moves 8266 insts, mean move: 1.50 um, max move: 11.60
um
      max move on inst (sa01_reg[5]): (103.80, 46.80) --> (112.80, 49.40)
Placement tweakage begins.
wire length = 1.983e+05 = 1.003e+05 H + 9.797e+04 V
wire length = 1.905e+05 = 9.416e+04 H + 9.634e+04 V
Placement tweakage ends.
move report: wireLenOpt moves 6574 insts, mean move: 3.10 um, max move: 44.80
um
      max move on inst (us01/U233): (126.20, 46.80) --> (137.20, 13.00)
move report: rPlace moves 8971 insts, mean move: 3.18 um, max move: 44.20 um
      max move on inst (us33/U174): (204.00, 13.00) --> (209.20, 52.00)
Statistics of distance of Instance movement in detailed placement:
  maximum (X+Y) =        44.20 um
  inst (us33/U174) with max move: (204, 13) -> (209.2, 52)
  mean    (X+Y) =         3.18 um
Total instances moved : 8971
*** cpu=0:00:05.4   mem=555.6M  mem(used)=0.2M***
Total net length = 1.938e+05 (9.622e+04 9.759e+04) (ext = 2.136e+04)
*** End of Placement (cpu=0:00:28.9, real=0:00:29.0, mem=555.6M) ***
default core: bins with density >  0.75 = 93.8 % ( 60 / 64 )
*** Free Virtual Timing Model ...(mem=544.9M)
Starting IO pin assignment...
Completed IO pin assignment.
**WARN: (ENCSP-9025):   No scan chain specified/traced.
```

```
*** Finishing placeDesign concurrent flow ***
**placeDesign ... cpu = 0: 2: 1, real = 0: 2: 2, mem = 544.9M **
**WARN: (ENCEXT-3493):  Extraction mode changed by calling extraction setup
command 'setExtractRCMode'. Therefore, parasitic data in the tool generated
as per previous mode is deleted. Call of extractRC/spefIn will generate/bring
parasitic data in the tool as per current mode.
<CMD> checkPlace
Begin checking placement ...
*info: Placed = 9542
*info: Unplaced = 0
Placement Density:90.50%(34194/37781)
<CMD> setAnalysisMode -setup -async -skew -autoDetectClockTree
**WARN: (ENCTCM-70):    Option "-setup" for command setAnalysisMode is
obsolete and has been replaced by "-checkType setup". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-checkType
setup".
**WARN: (ENCTCM-70):    Option "-async" for command setAnalysisMode is
obsolete and has been replaced by "-asyncChecks async". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-asyncChecks
async".
**WARN: (ENCTCM-70):    Option "-skew" for command setAnalysisMode is
obsolete and has been replaced by "-skew true". The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use "-skew true".
**WARN: (ENCTCM-70):    Option "-autoDetectClockTree" for command
setAnalysisMode is obsolete and has been replaced by "-clockPropagation
autoDetectClockTree". The obsolete option still works in this release, but to
avoid this warning and to ensure compatibility with future releases, update
your script to use "-clockPropagation autoDetectClockTree".
**WARN: (ENCSYC-1870):  setAnalysisMode -clockPropagation autoDetectClockTree
not supported in CTE timing mode, mapping it to setAnalysisMode -
clockPropagation sdcControl
{DETAILMESSAGE}<CMD> buildTimingGraph
<CMD_INTERNAL> setCteReport
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary > $rpt_dir/report_timing.placed.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
*** Starting trialRoute (mem=544.9M) ***

There are 0 pin guide points passed to trialRoute.
Options:  -handlePreroute -keepMarkedOptRoutes -noPinGuide

Nr of prerouted/Fixed nets = 0
routingBox: (0 0) (220200 220400)
coreBox:    (10200 10400) (210200 210400)

Phase 1a route (0:00:00.1 544.9M):
Est net length = 2.436e+05um = 1.204e+05H + 1.232e+05V
Usage: (26.9%H 39.3%V) = (1.359e+05um 2.151e+05um) = (135227 83081)
```

```
Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
Overflow: 39 = 0 (0.00% H) + 39 (0.21% V)

Phase 1b route (0:00:00.1 544.9M):
Usage: (26.8%H 39.3%V) = (1.355e+05um 2.151e+05um) = (134879 83081)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)

Phase 1c route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.353e+05um 2.155e+05um) = (134621 83234)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)

Phase 1d route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.353e+05um 2.155e+05um) = (134630 83242)
Overflow: 4 = 0 (0.00% H) + 4 (0.02% V)

Phase 1e route (0:00:00.0 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134593 83251)
Overflow: 3 = 0 (0.00% H) + 3 (0.02% V)

Phase 1f route (0:00:00.0 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134592 83253)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Congestion distribution:

Remain      cntH        cntV
----------------------------------------
----------------------------------------
  0:  0      0.00%      91     0.50%
  1:  0      0.00%      362    1.98%
  2:  24     0.13%      883    4.82%
  3:  0      0.00%      1708   9.33%
  4:  2      0.01%      2465  13.47%
  5:  4      0.02%      2391  13.06%
  6:  5      0.03%      2414  13.19%
  7:  26     0.14%      1835  10.03%
  8:  27     0.15%      1412   7.71%
  9:  59     0.32%      1017   5.56%
 10:  723    3.95%      865    4.73%
 11:  183    1.00%      1666   9.10%
 12:  685    3.74%      491    2.68%
 13:  436    2.38%      0      0.00%
 14:  607    3.32%      0      0.00%
 15:  757    4.14%      0      0.00%
 16:  1283   7.01%      0      0.00%
 17:  1049   5.73%      0      0.00%
 18:  1514   8.27%      0      0.00%
 19:  1225   6.69%      0      0.00%
 20:  9695  52.97%      704    3.85%


Global route (cpu=0.4s real=0.0s 544.9M)
Phase 1l route (0:00:00.7 544.9M):
```

```
*** After '-updateRemainTrks' operation:

Usage: (28.4%H 43.7%V) = (1.435e+05um 2.394e+05um) = (142750 92448)
Overflow: 134 = 0 (0.00% H) + 134 (0.73% V)

Congestion distribution:

Remain      cntH        cntV
------------------------------------
 -3:  0      0.00%      1      0.01%
 -2:  0      0.00%      18     0.10%
 -1:  0      0.00%      107    0.58%
------------------------------------
  0:  0      0.00%      475    2.60%
  1:  0      0.00%      893    4.88%
  2:  24     0.13%      1504   8.22%
  3:  1      0.01%      1931  10.55%
  4:  4      0.02%      2079  11.36%
  5:  12     0.07%      1908  10.42%
  6:  6      0.03%      2075  11.34%
  7:  39     0.21%      1516   8.28%
  8:  58     0.32%      1186   6.48%
  9:  117    0.64%      966    5.28%
 10:  755    4.12%      864    4.72%
 11:  291    1.59%      1606   8.77%
 12:  790    4.32%      471    2.57%
 13:  539    2.94%      0      0.00%
 14:  732    4.00%      0      0.00%
 15:  848    4.63%      0      0.00%
 16:  1358   7.42%      0      0.00%
 17:  1066   5.82%      0      0.00%
 18:  1443   7.88%      0      0.00%
 19:  1190   6.50%      0      0.00%
 20:  9031  49.34%      704    3.85%



*** Completed Phase 1 route (0:00:01.2 544.9M) ***


Total length: 2.667e+05um, number of vias: 98115
M1(H) length: 5.161e+03um, number of vias: 39652
M2(V) length: 6.787e+04um, number of vias: 38006
M3(H) length: 9.495e+04um, number of vias: 15893
M4(V) length: 6.941e+04um, number of vias: 3878
M5(H) length: 2.591e+04um, number of vias: 673
M6(V) length: 3.433e+03um, number of vias: 13
M7(H) length: 6.000e+00um
*** Completed Phase 2 route (0:00:00.9 544.9M) ***

*** Finished all Phases (cpu=0:00:02.1 mem=544.9M) ***
Peak Memory Usage was 544.9M
*** Finished trialRoute (cpu=0:00:02.2 mem=544.9M) ***
```

```
Extraction called for design 'aes_cipher_top' of instances=9542 and nets=9987
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.1  Real Time: 0:00:00.0  MEM:
544.930M)
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 544.9M)
Number of Loop : 0
Start delay calculation (mem=544.930M)...
Delay calculation completed. (cpu=0:00:01.6 real=0:00:01.0 mem=544.930M 0)
*** CDM Built up (cpu=0:00:04.6  real=0:00:04.0  mem= 544.9M) ***
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net  > $rpt_dir/report_timing.placed.slack
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
net  > $rpt_dir/report_timing.placed.crit_path
<CMD> trialRoute -highEffort
*** Starting trialRoute (mem=544.9M) ***

There are 0 pin guide points passed to trialRoute.
Options:  -highEffort -handlePreroute -keepMarkedOptRoutes -noPinGuide

Nr of prerouted/Fixed nets = 0
routingBox: (0 0) (220200 220400)
coreBox:    (10200 10400) (210200 210400)

Phase 1a route (0:00:00.1 544.9M):
Est net length = 2.436e+05um = 1.204e+05H + 1.232e+05V
Usage: (26.9%H 39.3%V) = (1.359e+05um 2.151e+05um) = (135227 83081)
Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
Overflow: 39 = 0 (0.00% H) + 39 (0.21% V)

Phase 1b route (0:00:00.1 544.9M):
Usage: (26.8%H 39.3%V) = (1.355e+05um 2.151e+05um) = (134879 83081)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)

Phase 1c route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.353e+05um 2.155e+05um) = (134621 83234)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)
```

```
Phase 1d route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.353e+05um 2.155e+05um) = (134630 83242)
Overflow: 4 = 0 (0.00% H) + 4 (0.02% V)

Phase 1e route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134593 83251)
Overflow: 3 = 0 (0.00% H) + 3 (0.02% V)

Phase 1f route (0:00:00.0 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134592 83253)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Phase 1g route (0:00:00.1 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134592 83253)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Phase 1h route (0:00:00.0 544.9M):
Usage: (26.8%H 39.4%V) = (1.352e+05um 2.156e+05um) = (134592 83253)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Congestion distribution:

Remain      cntH        cntV
------------------------------------
------------------------------------
  0:  0      0.00%      91     0.50%
  1:  0      0.00%      362    1.98%
  2:  24     0.13%      883    4.82%
  3:  0      0.00%      1708   9.33%
  4:  2      0.01%      2465  13.47%
  5:  4      0.02%      2391  13.06%
  6:  5      0.03%      2414  13.19%
  7:  26     0.14%      1835  10.03%
  8:  27     0.15%      1412   7.71%
  9:  59     0.32%      1017   5.56%
 10:  723    3.95%      865    4.73%
 11:  182    0.99%      1666   9.10%
 12:  685    3.74%      491    2.68%
 13:  437    2.39%      0      0.00%
 14:  608    3.32%      0      0.00%
 15:  756    4.13%      0      0.00%
 16:  1283   7.01%      0      0.00%
 17:  1049   5.73%      0      0.00%
 18:  1515   8.28%      0      0.00%
 19:  1224   6.69%      0      0.00%
 20:  9695  52.97%      704    3.85%


Global route (cpu=0.5s real=1.0s 544.9M)
Phase 1l route (0:00:00.8 544.9M):


*** After '-updateRemainTrks' operation:
```

```
Usage: (28.4%H 43.7%V) = (1.435e+05um 2.393e+05um) = (142730 92427)
Overflow: 130 = 0 (0.00% H) + 130 (0.71% V)

Congestion distribution:

Remain      cntH        cntV
------------------------------------
 -3:  0      0.00%      1      0.01%
 -2:  0      0.00%      17     0.09%
 -1:  0      0.00%      104    0.57%
------------------------------------
  0:  0      0.00%      471    2.57%
  1:  0      0.00%      892    4.87%
  2:  24     0.13%      1513   8.27%
  3:  1      0.01%      1933  10.56%
  4:  4      0.02%      2079  11.36%
  5:  12     0.07%      1904  10.40%
  6:  6      0.03%      2078  11.35%
  7:  38     0.21%      1514   8.27%
  8:  59     0.32%      1188   6.49%
  9:  115    0.63%      961    5.25%
 10:  756    4.13%      870    4.75%
 11:  287    1.57%      1604   8.76%
 12:  788    4.31%      471    2.57%
 13:  544    2.97%      0      0.00%
 14:  734    4.01%      0      0.00%
 15:  848    4.63%      0      0.00%
 16:  1357   7.41%      0      0.00%
 17:  1069   5.84%      0      0.00%
 18:  1435   7.84%      0      0.00%
 19:  1198   6.55%      0      0.00%
 20:  9029  49.33%      704    3.85%


*** Completed Phase 1 route (0:00:01.5 544.9M) ***


Total length: 2.667e+05um, number of vias: 98074
M1(H) length: 5.161e+03um, number of vias: 39652
M2(V) length: 6.789e+04um, number of vias: 38010
M3(H) length: 9.498e+04um, number of vias: 15882
M4(V) length: 6.943e+04um, number of vias: 3857
M5(H) length: 2.587e+04um, number of vias: 660
M6(V) length: 3.361e+03um, number of vias: 13
M7(H) length: 6.000e+00um
*** Completed Phase 2 route (0:00:01.0 544.9M) ***

*** Finished all Phases (cpu=0:00:02.5 mem=544.9M) ***
Peak Memory Usage was 544.9M
*** Finished trialRoute (cpu=0:00:02.7 mem=544.9M) ***

<CMD> extractRC
```

```
Extraction called for design 'aes_cipher_top' of instances=9542 and nets=9987
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.1  Real Time: 0:00:00.0  MEM:
544.926M)
<CMD> buildTimingGraph
<CMD> specifyClockTree -clkfile Clock.ctstch
Checking spec file integrity...
**WARN: (ENCCK-3217):   'specifyClockTree -clkfile' is obsolete. The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use
'specifyClockTree -file'.

Reading clock tree spec file 'Clock.ctstch' ...

RouteType               : FE_CTS_DEFAULT
PreferredExtraSpace     : 1
Shield                  : NONE
PreferLayer             : M3 M4
Est. Cap                : 0.232642(V=0.232642 H=0.232642) (ff/um)
[0.000232642]
Est. Res                : 0.76(V=0.76 H=0.76)(ohm/um) [0.00076]
Est. Via Res            : 4(ohm) [8]
Est. Via Cap            : 0.1233(ff)
M1(H) w=0.1(um) s=0.09(um) p=0.2(um) es=0.3(um) cap=0.236(ff/um)
res=0.76(ohm/um) viaRes=0(ohm) viaCap=0(ff)
M2(V) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.0868599(ff)
M3(H) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M4(V) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M5(H) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.44(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M6(V) w=0.4(um) s=0.4(um) p=0.8(um) es=1.2(um) cap=0.162(ff/um)
res=0.19(ohm/um) viaRes=4(ohm) viaCap=0.205046(ff)
M7(H) w=0.4(um) s=0.4(um) p=0.8(um) es=1.2(um) cap=0.164(ff/um)
res=0.19(ohm/um) viaRes=4(ohm) viaCap=0.241521(ff)

RouteType               : FE_CTS_DEFAULT_LEAF
```

```
PreferredExtraSpace     : 1
Shield                  : NONE
PreferLayer             : M3 M4
Est. Cap                : 0.232642(V=0.232642 H=0.232642) (ff/um)
[0.000232642]
Est. Res                : 0.76(V=0.76 H=0.76)(ohm/um) [0.00076]
Est. Via Res            : 4(ohm) [8]
Est. Via Cap            : 0.1233(ff)
M1(H) w=0.1(um) s=0.09(um) p=0.2(um) es=0.3(um) cap=0.236(ff/um)
res=0.76(ohm/um) viaRes=0(ohm) viaCap=0(ff)
M2(V) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.0868599(ff)
M3(H) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M4(V) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.76(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M5(H) w=0.1(um) s=0.1(um) p=0.2(um) es=0.3(um) cap=0.233(ff/um)
res=0.44(ohm/um) viaRes=4(ohm) viaCap=0.1233(ff)
M6(V) w=0.4(um) s=0.4(um) p=0.8(um) es=1.2(um) cap=0.162(ff/um)
res=0.19(ohm/um) viaRes=4(ohm) viaCap=0.205046(ff)
M7(H) w=0.4(um) s=0.4(um) p=0.8(um) es=1.2(um) cap=0.164(ff/um)
res=0.19(ohm/um) viaRes=4(ohm) viaCap=0.241521(ff)


****** AutoClockRootPin ******
AutoClockRootPin 1: clk
# NoGating         NO
# SetDPinAsSync    NO
# SetIoPinAsSync   NO
# SetAsyncSRPinAsSync   NO
# SetTriStEnPinAsSync   NO
# SetBBoxPinAsSync   NO
# RouteClkNet      NO
# PostOpt          YES
# RouteType        FE_CTS_DEFAULT
# LeafRouteType    FE_CTS_DEFAULT_LEAF

***** !! NOTE !! *****

CTS treats D-pins and I/O pins as non-synchronous pins by default.
If you want to change the behavior, you need to use the SetDPinAsSync
or SetIoPinAsSync statement in the clock tree specification file,
or use the setCTSMode -traceDPinAsLeaf {true|false} command,
or use the setCTSMode -traceIoPinAsLeaf {true|false} command
before specifyClockTree command.

*** End specifyClockTree (cpu=0:00:00.0, real=0:00:00.0, mem=544.9M) ***
<CMD> checkUnique
<CMD> ckSynthesis -rguide ./run/encounter_5/aes_cipher_top.rguide -report
./run/encounter_5/aes_cipher_top.ctsrpt -macromodel
./run/encounter_5/aes_cipher_top.ctsmdl -fix_added_buffers
Redoing specifyClockTree ...
Checking spec file integrity...
```

```
ckSynthesis Option :  -rguide ./run/encounter_5/aes_cipher_top.rguide -report
./run/encounter_5/aes_cipher_top.ctsrpt -macromodel
./run/encounter_5/aes_cipher_top.ctsmdl -fix_added_buffers
***** Allocate Placement Memory Finished (MEM: 544.926M)

Start to trace clock trees ...
*** Begin Tracer (mem=544.9M) ***
Tracing Clock clk ...
*** End Tracer (mem=544.9M) ***
***** Allocate Obstruction Memory  Finished (MEM: 544.926M)

****** Clock Tree (clk) Structure
Max. Skew           : 300(ps)
Max. Sink Transition: 400(ps)
Max. Buf Transition : 400(ps)
Max. Delay          : 3600(ps)
Min. Delay          : 0(ps)
Buffer              : (HS65_GS_CNBFX10) (HS65_GS_CNBFX14) (HS65_GS_CNBFX21)
Nr. Subtrees                    : 1
Nr. Sinks                       : 530
Nr.          Rising  Sync Pins  : 530
Nr. Inverter Rising  Sync Pins  : 0
Nr.          Falling Sync Pins  : 0
Nr. Inverter Falling Sync Pins  : 0
************************************************************
SubTree No: 0

Input_Pin:  (NULL)
Output_Pin: (clk)
Output_Net: (clk)
**** CK_START: TopDown Tree Construction for clk (530-leaf) (mem=544.9M)

Find 0 route_obs, 0 place_obs, 0 cut_obs  1 fence channel(s),
 1 channel(s).
Total 2 topdown clustering.
Trig. Edge Skew=55[230,285] N530 B7 G1 A8(8.2) L[3,3] score=2736
cpu=0:00:06.0 mem=545M

**** CK_END: TopDown Tree Construction for clk (cpu=0:00:07.0,
real=0:00:07.0, mem=544.9M)



**** CK_START: Update Database (mem=544.9M)
7 Clock Buffers/Inverters inserted.
**** CK_END: Update Database (cpu=0:00:00.0, real=0:00:00.0, mem=544.9M)
***** Start Refine Placement.....
Starting refinePlace ...
move report: placeLevelShifters moves 0 insts, mean move: 0.00 um, max move:
0.00 um
  Spread Effort: high, pre-route mode. (cpu=0:00:03.4, real=0:00:03.0)
move report: preRPlace moves 6527 insts, mean move: 0.74 um, max move: 8.20
um
```

```
      max move on inst (u0/U186): (98.40, 88.40) --> (101.40, 93.60)
move report: rPlace moves 6591 insts, mean move: 1.29 um, max move: 34.60 um
      max move on inst (us33/U41): (206.40, 10.40) --> (207.20, 44.20)
Statistics of distance of Instance movement in detailed placement:
  maximum (X+Y) =        34.60 um
  inst (us33/U41) with max move: (206.4, 10.4) -> (207.2, 44.2)
  mean    (X+Y) =         1.29 um
Total instances moved : 6591
*** cpu=0:00:03.4   mem=544.9M  mem(used)=0.0M***
***** Refine Placement Finished (CPU Time: 0:00:03.7  MEM: 544.930M)

#
# Mode                : Setup
# Library Name        : CLOCK65GPSVT(max)
# Operating Condition : CLOCK65GPSVT/%NOM_PVT
# Process             : 1.2
# Voltage             : 0.9
# Temperature         : 125
#
********** Clock clk Pre-Route Timing Analysis **********
Nr. of Subtrees                : 1
Nr. of Sinks                   : 530
Nr. of Buffer                  : 7
Nr. of Level (including gates) : 2
Root Rise Input Tran           : 0.1(ps)
Root Fall Input Tran           : 0.1(ps)
Max trig. edge delay at sink(R): sa11_reg[7]/CP 286.3(ps)
Min trig. edge delay at sink(R): sa13_reg[6]/CP 230.6(ps)


                                 (Actual)               (Required)
Rise Phase Delay               : 230.6~286.3(ps)        0~3600(ps)
Fall Phase Delay               : 222.5~273.6(ps)        0~3600(ps)
Trig. Edge Skew                : 55.7(ps)               300(ps)
Rise Skew                      : 55.7(ps)
Fall Skew                      : 51.1(ps)
Max. Rise Buffer Tran.         : 100.7(ps)              400(ps)
Max. Fall Buffer Tran.         : 81.5(ps)               400(ps)
Max. Rise Sink Tran.           : 235(ps)                400(ps)
Max. Fall Sink Tran.           : 188.4(ps)              400(ps)
Min. Rise Buffer Tran.         : 100.7(ps)              0(ps)
Min. Fall Buffer Tran.         : 81.4(ps)               0(ps)
Min. Rise Sink Tran.           : 156.2(ps)              0(ps)
Min. Fall Sink Tran.           : 125.6(ps)              0(ps)


Clock Analysis (CPU Time 0:00:00.0)



#
# Mode                : Setup
# Library Name        : CLOCK65GPSVT(max)
# Operating Condition : CLOCK65GPSVT/%NOM_PVT
```

```
# Process             : 1.2
# Voltage             : 0.9
# Temperature         : 125
#
********** Clock clk Pre-Route Timing Analysis **********
Nr. of Subtrees                : 1
Nr. of Sinks                   : 530
Nr. of Buffer                  : 7
Nr. of Level (including gates) : 2
Root Rise Input Tran           : 0.1(ps)
Root Fall Input Tran           : 0.1(ps)
Max trig. edge delay at sink(R): sa11_reg[7]/CP 286.3(ps)
Min trig. edge delay at sink(R): sa13_reg[6]/CP 230.6(ps)


                                  (Actual)               (Required)
Rise Phase Delay               : 230.6~286.3(ps)        0~3600(ps)
Fall Phase Delay               : 222.5~273.6(ps)        0~3600(ps)
Trig. Edge Skew                : 55.7(ps)               300(ps)
Rise Skew                      : 55.7(ps)
Fall Skew                      : 51.1(ps)
Max. Rise Buffer Tran.         : 100.7(ps)              400(ps)
Max. Fall Buffer Tran.         : 81.5(ps)               400(ps)
Max. Rise Sink Tran.           : 235(ps)                400(ps)
Max. Fall Sink Tran.           : 188.4(ps)              400(ps)
Min. Rise Buffer Tran.         : 100.7(ps)              0(ps)
Min. Fall Buffer Tran.         : 81.4(ps)               0(ps)
Min. Rise Sink Tran.           : 156.2(ps)              0(ps)
Min. Fall Sink Tran.           : 125.6(ps)              0(ps)


Clock Analysis (CPU Time 0:00:00.0)


Optimizing clock tree 'clk' ...

Calculating pre-route downstream delay for clock tree 'clk'...
*** Look For Reconvergent Clock Component ***
The clock tree clk has no reconvergent cell.
*** Look For PreservePin And Optimized CrossOver Root Pin ***
resized 0 standard cell(s).
inserted 0 standard cell(s).
*** Non-Gated Clock Tree Optimization (cpu=0:00:00.1 real=0:00:00.0
mem=544.9M) ***
*** Finished Clock Tree Skew Optimization (cpu=0:00:00.1 real=0:00:00.0
mem=544.9M) ***

None of the clock tree buffers/gates are modified by the skew optimization.


*** None of the buffer chains at roots are modified by the fine-tune process.


#
```

```
# Mode                 : Setup
# Library Name         : CLOCK65GPSVT(max)
# Operating Condition  : CLOCK65GPSVT/%NOM_PVT
# Process              : 1.2
# Voltage              : 0.9
# Temperature          : 125
#
********** Clock clk Pre-Route Timing Analysis **********
Nr. of Subtrees                : 1
Nr. of Sinks                   : 530
Nr. of Buffer                  : 7
Nr. of Level (including gates) : 2
Root Rise Input Tran           : 0.1(ps)
Root Fall Input Tran           : 0.1(ps)
Max trig. edge delay at sink(R): sa11_reg[7]/CP 286.3(ps)
Min trig. edge delay at sink(R): sa13_reg[6]/CP 230.6(ps)


                                  (Actual)               (Required)
Rise Phase Delay               : 230.6~286.3(ps)        0~3600(ps)
Fall Phase Delay               : 222.5~273.6(ps)        0~3600(ps)
Trig. Edge Skew                : 55.7(ps)               300(ps)
Rise Skew                      : 55.7(ps)
Fall Skew                      : 51.1(ps)
Max. Rise Buffer Tran.         : 100.7(ps)              400(ps)
Max. Fall Buffer Tran.         : 81.5(ps)               400(ps)
Max. Rise Sink Tran.           : 235(ps)                400(ps)
Max. Fall Sink Tran.           : 188.4(ps)              400(ps)
Min. Rise Buffer Tran.         : 100.7(ps)              0(ps)
Min. Fall Buffer Tran.         : 81.4(ps)               0(ps)
Min. Rise Sink Tran.           : 156.2(ps)              0(ps)
Min. Fall Sink Tran.           : 125.6(ps)              0(ps)


Generating Clock Analysis Report ./run/encounter_5/aes_cipher_top.ctsrpt ....
Generating Clock Routing Guide ./run/encounter_5/aes_cipher_top.rguide ....
Clock Analysis (CPU Time 0:00:00.1)


*** End ckSynthesis (cpu=0:00:11.8, real=0:00:12.0, mem=544.9M) ***
<CMD> saveClockNets -output ./run/encounter_5/clock_nets.ctsntf
Redoing specifyClockTree ...
Checking spec file integrity...
<CMD> trialRoute -highEffort -guide ./run/encounter_5/aes_cipher_top.rguide
*** Starting trialRoute (mem=544.9M) ***

There are 0 pin guide points passed to trialRoute.
Options:  -highEffort -handlePreroute -keepMarkedOptRoutes -guide
./run/encounter_5/aes_cipher_top.rguide -noPinGuide

Nr of prerouted/Fixed nets = 0
There are 8 nets with 1 extra space.
routingBox: (0 0) (220200 220400)
coreBox:    (10200 10400) (210200 210400)
```

```
Phase 0 route (using Routing Guide) (0:00:00.0 544.9M):

Phase 1a route (0:00:00.1 544.9M):
Est net length = 2.500e+05um = 1.243e+05H + 1.257e+05V
Usage: (28.0%H 40.3%V) = (1.412e+05um 2.208e+05um) = (140588 85252)
Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
Overflow: 38 = 0 (0.00% H) + 38 (0.21% V)

Phase 1b route (0:00:00.1 544.9M):
Usage: (27.9%H 40.3%V) = (1.409e+05um 2.208e+05um) = (140222 85251)
Overflow: 16 = 0 (0.00% H) + 16 (0.09% V)

Phase 1c route (0:00:00.1 544.9M):
Usage: (27.9%H 40.4%V) = (1.406e+05um 2.212e+05um) = (139979 85420)
Overflow: 15 = 0 (0.00% H) + 15 (0.08% V)

Phase 1d route (0:00:00.1 544.9M):
Usage: (27.9%H 40.4%V) = (1.406e+05um 2.212e+05um) = (139987 85425)
Overflow: 1 = 0 (0.00% H) + 1 (0.01% V)

Phase 1e route (0:00:00.0 544.9M):
Usage: (27.8%H 40.4%V) = (1.406e+05um 2.213e+05um) = (139923 85451)
Overflow: 1 = 0 (0.00% H) + 1 (0.01% V)

Phase 1f route (0:00:00.1 544.9M):
Usage: (27.8%H 40.4%V) = (1.406e+05um 2.213e+05um) = (139921 85454)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Phase 1g route (0:00:00.0 544.9M):
Usage: (27.8%H 40.4%V) = (1.406e+05um 2.213e+05um) = (139921 85454)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Phase 1h route (0:00:00.1 544.9M):
Usage: (27.8%H 40.4%V) = (1.406e+05um 2.213e+05um) = (139921 85454)
Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)

Congestion distribution:

Remain      cntH        cntV
---------------------------------------
---------------------------------------
  0:  0      0.00%      101    0.55%
  1:  0      0.00%      465    2.54%
  2:  24     0.13%      902    4.93%
  3:  1      0.01%      1684   9.20%
  4:  1      0.01%      2695  14.72%
  5:  4      0.02%      2334  12.75%
  6:  10     0.05%      2478  13.54%
  7:  42     0.23%      1880  10.27%
  8:  39     0.21%      1298   7.09%
  9:  69     0.38%      900    4.92%
 10:  711    3.88%      753    4.11%
 11:  206    1.13%      1621   8.86%
```

```
 12:  724    3.96%      489    2.67%
 13:  483    2.64%      0      0.00%
 14:  655    3.58%      0      0.00%
 15:  851    4.65%      0      0.00%
 16:  1375   7.51%      0      0.00%
 17:  1092   5.97%      0      0.00%
 18:  1521   8.31%      0      0.00%
 19:  1268   6.93%      0      0.00%
 20:  9228  50.42%      704    3.85%


Global route (cpu=0.5s real=0.0s 544.9M)
Phase 1l route (0:00:00.8 544.9M):


*** After '-updateRemainTrks' operation:

Usage: (29.6%H 45.3%V) = (1.497e+05um 2.480e+05um) = (148893 95765)
Overflow: 186 = 0 (0.00% H) + 186 (1.02% V)

Congestion distribution:

Remain      cntH        cntV
-------------------------------------
 -2:  0      0.00%      27     0.15%
 -1:  0      0.00%      148    0.81%
-------------------------------------
  0:  0      0.00%      545    2.98%
  1:  0      0.00%      1048   5.73%
  2:  24     0.13%      1462   7.99%
  3:  1      0.01%      2046  11.18%
  4:  6      0.03%      2214  12.10%
  5:  10     0.05%      1883  10.29%
  6:  24     0.13%      2043  11.16%
  7:  62     0.34%      1537   8.40%
  8:  73     0.40%      1022   5.58%
  9:  101    0.55%      835    4.56%
 10:  794    4.34%      762    4.16%
 11:  309    1.69%      1557   8.51%
 12:  838    4.58%      471    2.57%
 13:  619    3.38%      0      0.00%
 14:  793    4.33%      0      0.00%
 15:  918    5.02%      0      0.00%
 16:  1449   7.92%      0      0.00%
 17:  1041   5.69%      0      0.00%
 18:  1477   8.07%      0      0.00%
 19:  1212   6.62%      0      0.00%
 20:  8553  46.73%      704    3.85%


*** Completed Phase 1 route (0:00:01.4 544.9M) ***
```

```
Total length: 2.734e+05um, number of vias: 99858
M1(H) length: 5.162e+03um, number of vias: 39666
M2(V) length: 6.812e+04um, number of vias: 38312
M3(H) length: 9.669e+04um, number of vias: 16817
M4(V) length: 7.073e+04um, number of vias: 4310
M5(H) length: 2.829e+04um, number of vias: 738
M6(V) length: 4.354e+03um, number of vias: 15
M7(H) length: 8.400e+00um
*** Completed Phase 2 route (0:00:00.9 544.9M) ***

*** Finished all Phases (cpu=0:00:02.4 mem=544.9M) ***
Peak Memory Usage was 544.9M
*** Finished trialRoute (cpu=0:00:02.5 mem=544.9M) ***

<CMD> extractRC
Extraction called for design 'aes_cipher_top' of instances=9549 and nets=9994
using extraction engine 'preRoute' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Default RC Extraction called for design aes_cipher_top.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
RCMode: Default
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res Scaling Factor     : 1.00000
Shrink Factor                : 1.00000
Default RC extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Default RC Extraction DONE (CPU Time: 0:00:00.1  Real Time: 0:00:00.0  MEM:
544.934M)
<CMD> reportClockTree -postRoute -localSkew -report
./run/encounter_5/aes_cipher_top.post_troute_local.ctsrpt
Redoing specifyClockTree ...
Checking spec file integrity...


reportClockTree Option :  -postRoute -localSkew -report
./run/encounter_5/aes_cipher_top.post_troute_local.ctsrpt
*** Look For Reconvergent Clock Component ***
The clock tree clk has no reconvergent cell.

Searching for sequentially adjacent registers for clock tree 'clk' ...

Total number of adjacent register pair is 7069.

#
# Mode                : Setup
# Library Name        : CLOCK65GPSVT(max)
# Operating Condition : CLOCK65GPSVT/%NOM_PVT
# Process             : 1.2
```

```
# Voltage             : 0.9
# Temperature         : 125
#
********** Clock clk Post-Route Timing Analysis **********
Nr. of Subtrees                : 1
Nr. of Sinks                   : 530
Nr. of Buffer                  : 7
Nr. of Level (including gates) : 2
Root Rise Input Tran           : 0.1(ps)
Root Fall Input Tran           : 0.1(ps)
Max trig. edge delay at sink(R): text_in_r_reg[121]/CP 257.3(ps)
Min trig. edge delay at sink(R): sa13_reg[6]/CP 206.5(ps)


                                  (Actual)               (Required)
Rise Phase Delay               : 206.5~257.3(ps)        0~3600(ps)
Fall Phase Delay               : 200.6~245.6(ps)        0~3600(ps)
Trig. Edge Skew                : 50.8(ps)               300(ps)
Rise Skew                      : 50.8(ps)
Fall Skew                      : 45(ps)
Max. Rise Buffer Tran.         : 88.2(ps)               400(ps)
Max. Fall Buffer Tran.         : 71.6(ps)               400(ps)
Max. Rise Sink Tran.           : 255.2(ps)              400(ps)
Max. Fall Sink Tran.           : 220.6(ps)              400(ps)
Min. Rise Buffer Tran.         : 88.2(ps)               0(ps)
Min. Fall Buffer Tran.         : 71.6(ps)               0(ps)
Min. Rise Sink Tran.           : 147.3(ps)              0(ps)
Min. Fall Sink Tran.           : 118.5(ps)              0(ps)


**** Local Skew Report ****
Total number of adjacent register pair : 7069

Max. Local Skew                : 34.8(ps)
  sa13_reg[6]/CP(R)->
  text_out_reg[50]/CP(R)


Generating Clock Analysis Report
./run/encounter_5/aes_cipher_top.post_troute_local.ctsrpt ....
Clock Analysis (CPU Time 0:00:01.0)


*** End reportClockTree (cpu=0:00:01.1, real=0:00:01.0, mem=544.9M) ***
<CMD> reportClockTree -postRoute -report
./run/encounter_5/aes_cipher_top.post_troute.ctsrpt
Redoing specifyClockTree ...
Checking spec file integrity...


reportClockTree Option :  -postRoute -report
./run/encounter_5/aes_cipher_top.post_troute.ctsrpt
*** Look For Reconvergent Clock Component ***
The clock tree clk has no reconvergent cell.
```

```
#
# Mode                 : Setup
# Library Name         : CLOCK65GPSVT(max)
# Operating Condition  : CLOCK65GPSVT/%NOM_PVT
# Process              : 1.2
# Voltage              : 0.9
# Temperature          : 125
#
********** Clock clk Post-Route Timing Analysis **********
Nr. of Subtrees                : 1
Nr. of Sinks                   : 530
Nr. of Buffer                  : 7
Nr. of Level (including gates) : 2
Root Rise Input Tran           : 0.1(ps)
Root Fall Input Tran           : 0.1(ps)
Max trig. edge delay at sink(R): text_in_r_reg[121]/CP 257.3(ps)
Min trig. edge delay at sink(R): sa13_reg[6]/CP 206.5(ps)


                                 (Actual)               (Required)
Rise Phase Delay               : 206.5~257.3(ps)        0~3600(ps)
Fall Phase Delay               : 200.6~245.6(ps)        0~3600(ps)
Trig. Edge Skew                : 50.8(ps)               300(ps)
Rise Skew                      : 50.8(ps)
Fall Skew                      : 45(ps)
Max. Rise Buffer Tran.         : 88.2(ps)               400(ps)
Max. Fall Buffer Tran.         : 71.6(ps)               400(ps)
Max. Rise Sink Tran.           : 255.2(ps)              400(ps)
Max. Fall Sink Tran.           : 220.6(ps)              400(ps)
Min. Rise Buffer Tran.         : 88.2(ps)               0(ps)
Min. Fall Buffer Tran.         : 71.6(ps)               0(ps)
Min. Rise Sink Tran.           : 147.3(ps)              0(ps)
Min. Fall Sink Tran.           : 118.5(ps)              0(ps)


Generating Clock Analysis Report
./run/encounter_5/aes_cipher_top.post_troute.ctsrpt ....
Clock Analysis (CPU Time 0:00:00.0)


*** End reportClockTree (cpu=0:00:00.0, real=0:00:01.0, mem=544.9M) ***
<CMD> setAnalysisMode -setup -async -skew -autoDetectClockTree
**WARN: (ENCTCM-70):    Option "-setup" for command setAnalysisMode is
obsolete and has been replaced by "-checkType setup". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-checkType
setup".
**WARN: (ENCTCM-70):    Option "-async" for command setAnalysisMode is
obsolete and has been replaced by "-asyncChecks async". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-asyncChecks
async".
```

```
**WARN: (ENCTCM-70):    Option "-skew" for command setAnalysisMode is
obsolete and has been replaced by "-skew true". The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use "-skew true".
**WARN: (ENCTCM-70):    Option "-autoDetectClockTree" for command
setAnalysisMode is obsolete and has been replaced by "-clockPropagation
autoDetectClockTree". The obsolete option still works in this release, but to
avoid this warning and to ensure compatibility with future releases, update
your script to use "-clockPropagation autoDetectClockTree".
**WARN: (ENCSYC-1870):  setAnalysisMode -clockPropagation autoDetectClockTree
not supported in CTE timing mode, mapping it to setAnalysisMode -
clockPropagation sdcControl
{DETAILMESSAGE}<CMD> buildTimingGraph
<CMD_INTERNAL> setCteReport
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary > $rpt_dir/report_timing.cts.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 544.9M)
Number of Loop : 0
Start delay calculation (mem=544.938M)...
Delay calculation completed. (cpu=0:00:01.6 real=0:00:01.0 mem=544.938M 0)
*** CDM Built up (cpu=0:00:01.8  real=0:00:01.0  mem= 544.9M) ***
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net > $rpt_dir/report_timing.cts.slack
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 10 -net -summary > $rpt_dir/report_timing.cts.hold.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 544.9M)
Number of Loop : 0
Start delay calculation (mem=544.938M)...
Delay calculation completed. (cpu=0:00:01.6 real=0:00:02.0 mem=544.938M 0)
*** CDM Built up (cpu=0:00:02.3  real=0:00:03.0  mem= 544.9M) ***
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 10 -net > $rpt_dir/report_timing.cts.hold.slack
<CMD> fit
<CMD> man globalDetailRoute
<CMD> man setNanoRouteMode
<CMD> man setNanoRouteMode
<CMD> man setNanoRouteMode
<CMD> man setNanoRouteMode
<CMD> man setNanoRouteMode
<CMD> setLayerPreference page2/2 -isVisible 0
<CMD> setLayerPreference allM7 -isVisible 1
<CMD> setLayerPreference allM7 -isVisible 0
<CMD> setLayerPreference allM7 -isVisible 1
<CMD> setLayerPreference allM7 -isVisible 0
```

```
<CMD> setLayerPreference allM7Cont -isVisible 1
<CMD> setLayerPreference allM7Cont -isVisible 0
<CMD> setLayerPreference allM7Cont -isVisible 1
<CMD> setLayerPreference allM7Cont -isVisible 0
<CMD> setLayerPreference allM6 -isVisible 1
<CMD> setLayerPreference allM5 -isVisible 1
<CMD> man setNanoRouteMode
<CMD> man setNanoRouteMode
<CMD> man setAttribute
<CMD> man set_propagated_clock
<CMD> set_propagated_clock clk
<CMD> setAttribute -net @clock -weight 100
setAttribute -net @clock -weight 100
<CMD> setAttribute -net @clock -avoid_detour true
setAttribute -net @clock -avoid_detour true
<CMD> setAttribute -net @clock -bottom_preferred_routing_layer 4
setAttribute -net @clock -bottom_preferred_routing_layer 4
<CMD> setAttribute -net @clock -top_preferred_routing_layer 6
setAttribute -net @clock -top_preferred_routing_layer 6
<CMD> setNanoRouteMode -quiet routeWithTimingDriven true
**WARN: (ENCTCM-59):    Option "routeWithTimingDriven" for command
setNanoRouteMode is obsolete and has been replaced by "-
routeWithTimingDriven". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
routeWithTimingDriven".
<CMD> setNanoRouteMode -quiet routeWithTimingOpt false
**WARN: (ENCTCM-59):    Option "routeWithTimingOpt" for command
setNanoRouteMode is obsolete and has been replaced by "-routeWithTimingOpt".
All options will now require "-". The obsolete option still works in this
release, but to avoid this warning and to ensure compatibility with future
releases, update your script to use "-routeWithTimingOpt".
**WARN: (ENCTCM-77):    Option "-routeWithTimingOpt" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeFixSetupTime true
**WARN: (ENCTCM-59):    Option "optimizeFixSetupTime" for command
setNanoRouteMode is obsolete and has been replaced by "-
optimizeFixSetupTime". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
optimizeFixSetupTime".
**WARN: (ENCTCM-77):    Option "-optimizeFixSetupTime" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeTargetSetupSlack 0.000000
**WARN: (ENCTCM-59):    Option "optimizeTargetSetupSlack" for command
setNanoRouteMode is obsolete and has been replaced by "-
optimizeTargetSetupSlack". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
```

```
compatibility with future releases, update your script to use "-
optimizeTargetSetupSlack".
**WARN: (ENCTCM-77):    Option "-optimizeTargetSetupSlack" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeFixMaxCap false
**WARN: (ENCTCM-59):    Option "optimizeFixMaxCap" for command
setNanoRouteMode is obsolete and has been replaced by "-optimizeFixMaxCap".
All options will now require "-". The obsolete option still works in this
release, but to avoid this warning and to ensure compatibility with future
releases, update your script to use "-optimizeFixMaxCap".
**WARN: (ENCTCM-77):    Option "-optimizeFixMaxCap" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeFixHoldTime false
**WARN: (ENCTCM-59):    Option "optimizeFixHoldTime" for command
setNanoRouteMode is obsolete and has been replaced by "-optimizeFixHoldTime".
All options will now require "-". The obsolete option still works in this
release, but to avoid this warning and to ensure compatibility with future
releases, update your script to use "-optimizeFixHoldTime".
**WARN: (ENCTCM-77):    Option "-optimizeFixHoldTime" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeTargetHoldSlack 0.000000
**WARN: (ENCTCM-59):    Option "optimizeTargetHoldSlack" for command
setNanoRouteMode is obsolete and has been replaced by "-
optimizeTargetHoldSlack". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
optimizeTargetHoldSlack".
**WARN: (ENCTCM-77):    Option "-optimizeTargetHoldSlack" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeFixMaxTran false
**WARN: (ENCTCM-59):    Option "optimizeFixMaxTran" for command
setNanoRouteMode is obsolete and has been replaced by "-optimizeFixMaxTran".
All options will now require "-". The obsolete option still works in this
release, but to avoid this warning and to ensure compatibility with future
releases, update your script to use "-optimizeFixMaxTran".
**WARN: (ENCTCM-77):    Option "-optimizeFixMaxTran" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet optimizeDontUseCellFile default
```

```
**WARN: (ENCTCM-59):    Option "optimizeDontUseCellFile" for command
setNanoRouteMode is obsolete and has been replaced by "-
optimizeDontUseCellFile". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
optimizeDontUseCellFile".
**WARN: (ENCTCM-77):    Option "-optimizeDontUseCellFile" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet routeWithSiDriven true
**WARN: (ENCTCM-59):    Option "routeWithSiDriven" for command
setNanoRouteMode is obsolete and has been replaced by "-routeWithSiDriven".
All options will now require "-". The obsolete option still works in this
release, but to avoid this warning and to ensure compatibility with future
releases, update your script to use "-routeWithSiDriven".
<CMD> setNanoRouteMode -quiet routeSiEffort normal
**WARN: (ENCTCM-59):    Option "routeSiEffort" for command setNanoRouteMode
is obsolete and has been replaced by "-routeSiEffort". All options will now
require "-". The obsolete option still works in this release, but to avoid
this warning and to ensure compatibility with future releases, update your
script to use "-routeSiEffort".
<CMD> setNanoRouteMode -quiet siNoiseCTotalThreshold 0.050000
**WARN: (ENCTCM-59):    Option "siNoiseCTotalThreshold" for command
setNanoRouteMode is obsolete and has been replaced by "-
siNoiseCTotalThreshold". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
siNoiseCTotalThreshold".
**WARN: (ENCTCM-77):    Option "-siNoiseCTotalThreshold" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet siNoiseCouplingCapThreshold 0.005000
**WARN: (ENCTCM-59):    Option "siNoiseCouplingCapThreshold" for command
setNanoRouteMode is obsolete and has been replaced by "-
siNoiseCouplingCapThreshold". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
siNoiseCouplingCapThreshold".
**WARN: (ENCTCM-77):    Option "-siNoiseCouplingCapThreshold" for command
setNanoRouteMode is obsolete and will be removed in future release. The
obsolete option still works in this release, but to avoid this warning and to
ensure compatibility with future releases, remove the obsolete option from
your script.
<CMD> setNanoRouteMode -quiet routeWithSiPostRouteFix false
**WARN: (ENCTCM-59):    Option "routeWithSiPostRouteFix" for command
setNanoRouteMode is obsolete and has been replaced by "-
routeWithSiPostRouteFix". All options will now require "-". The obsolete
option still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
routeWithSiPostRouteFix".
```

```
<CMD> setNanoRouteMode -quiet drouteAutoStop true
**WARN: (ENCTCM-59):    Option "drouteAutoStop" for command setNanoRouteMode
is obsolete and has been replaced by "-drouteAutoStop". All options will now
require "-". The obsolete option still works in this release, but to avoid
this warning and to ensure compatibility with future releases, update your
script to use "-drouteAutoStop".
<CMD> setNanoRouteMode -quiet routeSelectedNetOnly false
**WARN: (ENCTCM-59):    Option "routeSelectedNetOnly" for command
setNanoRouteMode is obsolete and has been replaced by "-
routeSelectedNetOnly". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
routeSelectedNetOnly".
<CMD> setNanoRouteMode -quiet drouteStartIteration default
**WARN: (ENCTCM-59):    Option "drouteStartIteration" for command
setNanoRouteMode is obsolete and has been replaced by "-
drouteStartIteration". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
drouteStartIteration".
<CMD> setNanoRouteMode -quiet routeTopRoutingLayer M7
**WARN: (ENCTCM-59):    Option "routeTopRoutingLayer" for command
setNanoRouteMode is obsolete and has been replaced by "-
routeTopRoutingLayer". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
routeTopRoutingLayer".

Usage: setNanoRouteMode [-help] [-reset] [-dbCheckRule {true|false}]
                        [-dbReportWireExtraction <value>]
                        [-dbReportWireExtractionEcoOnly {true|false}]
                        [-dbSkipAnalog {true|false}]
                        [-drouteAntennaEcoListFile <value>]
                        [-drouteAutoCreateShield {true|false}]
                        [-drouteAutoStop {true|false}]
                        [-drouteCheckMinstepOnTopLevelPin {true|false}]
                        [-drouteElapsedTimeLimit <value>]
                        [-drouteEndIteration <value>]
                        [-drouteFixAntenna {true|false}]
                        [-drouteMinLengthForWireSpreading <value>]
                        [-drouteMinLengthForWireWidening <value>]
                        [-drouteMinSlackForWireOptimization <value>]
                        [-drouteNoTaperInLayers <value>]
                        [-drouteNoTaperOnOutputPin {true|false}]
                        [-drouteOnGridOnly <value>]
                        [-droutePostRouteLithoRepair {true|false}]
                        [-droutePostRouteMinimizeViaCount {true|false}]
                        [-droutePostRouteSpreadWire {true|false}]
                        [-droutePostRouteSwapVia <value>]
                        [-droutePostRouteWidenWire <value>]
                        [-droutePostRouteWidenWireRule <value>]
                        [-drouteSearchAndRepair {true|false}]
                        [-drouteStartIteration <value>]
                        [-drouteUseBiggerOverhangViaFirst {true|false}]
```

```
[-drouteUseMultiCutViaEffort <value>]
[-envAdvancedIntegration {true|false}]
[-envDontUseLicsForThreadings <value>]
[-envNumberFailLimit <value>]
[-envNumberProcessor <value>]
[-envNumberWarningLimit <value>]
[-grouteExpansionRatioFile <value>]
[-hfrouteNumReserveLayer <value>]
[-hfrouteShieldTrimLength <value>]
[-routeAllowPowerGroundPin {true|false}]
[-routeAntennaCellName <value>]
[-routeAntennaPinLimit <value>]
[-routeAutoGgrid {true|false}]
[-routeBottomRoutingLayer <value>]
[-routeBottomShieldLayer <value>]
[-routeConcurrentMinimizeViaCountEffort <value>]
[-routeDeferredShield {true|false}]
[-routeDeleteAntennaReroute {true|false}]
[-routeDesignFixClockNets {true|false}]
[-routeDesignNoCheckPlace {true|false}]
[-routeDesignRouteClockNetsFirst {true|false}]
[-routeEcoOnlyInLayers <value>]
[-routeExtraSpaceUseDefaultSpacing {true|false}]
[-routeExtraViaEnclosure <value>]
[-routeFixTopLayerAntenna {true|false}]
[-routeHonorPartition {true|false}]
[-routeHonorPowerDomain {true|false}]
[-routeIgnoreAntennaTopCellPin {true|false}]
[-routeIgnoreUnplacedInsts {true|false}]
[-routeInsertAntennaDiode {true|false}]
[-routeInsertAntennaInVerticalRow {true|false}]
[-routeInsertDiodeForClockNets {true|false}]
[-routeMergeSpecialWire <value>]
[-routeMinShieldViaSpan <value>]
[-routeReserveSpaceForMultiCut {true|false}]
[-routeReverseDirection <value>]
[-routeSelectedNetOnly {true|false}]
[-routeShieldingReportFileName <value>]
[-routeSiEffort <value>]
[-routeStrictlyHonorNonDefaultRule <value>]
[-routeStripeLayerRange <value>]
[-routeTdrEffort <value>]
[-routeTopRoutingLayer <value>]
[-routeTrunkWithClusterTargetSize <value>]
[-routeUseBlockageForAutoGgrid {true|false}]
[-routeWithEco {true|false}]
[-routeWithLithoDriven {true|false}]
[-routeWithSiDriven {true|false}]
[-routeWithSiPostRouteFix {true|false}]
[-routeWithTimingDriven {true|false}]
[-routeWithViaInPin <value>]
[-routeWithViaOnlyForStandardCellPin <value>]
[-timingEngine <value>]
```

```
**ERROR: (ENCTCM-4):    "M7" is not a valid int value for option
"routeTopRoutingLayer".
<CMD> man setNanoRouteMode
<CMD> getTrialRouteMode -maxRouteLayer -quiet
<CMD> setNanoRouteMode -quiet routeTopRoutingLayer 7
**WARN: (ENCTCM-59):    Option "routeTopRoutingLayer" for command
setNanoRouteMode is obsolete and has been replaced by "-
routeTopRoutingLayer". All options will now require "-". The obsolete option
still works in this release, but to avoid this warning and to ensure
compatibility with future releases, update your script to use "-
routeTopRoutingLayer".
<CMD> setNanoRouteMode -routeTopRoutingLayer 7
<CMD> getTrialRouteMode -maxRouteLayer -quiet
<CMD> setNanoRouteMode -routeTopRoutingLayer default
<CMD> getTrialRouteMode -maxRouteLayer -quiet
<CMD> globalDetailRoute

globalDetailRoute

#Start globalDetailRoute on Mon May  2 12:45:47 2011
#
#Generating timing graph information, please wait...
#9808 total nets, 0 already routed, 0 will ignore in trialRoute
#Dump tif for version 2.1
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
**WARN: (ENCEXT-6166):  Using capacitance table file without EXTENDED section
is not recommended and will result in lower accuracy for clock nets in
preRoute extraction and for all nets when using postRoute extraction -
effortLevel low. Regeneration of full capacitance table is recommended.
#Write timing file took: cpu time = 00:00:04, elapsed time = 00:00:05, memory
= 538.00 (Mb)
#Done generating timing graph information.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 538.00 (Mb)
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC6X9 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC6X7 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC6X4 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC4X9 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC4X7 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC4X4 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC2X9 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC2X7 does not have antenna
diff area.
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_DLYIC2X4 does not have antenna
diff area.
```

```
#WARNING (NRDB-728) PIN A in CELL_VIEW HS65_GS_CNXOR2X38 does not have
antenna diff area.
#WARNING (NRDB-728) PIN CP in CELL_VIEW HS65_GS_CNSDFPSQTX16 does not have
antenna diff area.
#WARNING (NRDB-728) PIN D in CELL_VIEW HS65_GS_CNSDFPSQTX16 does not have
antenna diff area.
#WARNING (NRDB-728) PIN SN in CELL_VIEW HS65_GS_CNSDFPSQTX16 does not have
antenna diff area.
#WARNING (NRDB-728) PIN TE in CELL_VIEW HS65_GS_CNSDFPSQTX16 does not have
antenna diff area.
#WARNING (NRDB-728) PIN TI in CELL_VIEW HS65_GS_CNSDFPSQTX16 does not have
antenna diff area.
#WARNING (NRDB-728) PIN CP in CELL_VIEW HS65_GS_CNSDFPRQTX15 does not have
antenna diff area.
#WARNING (NRDB-728) PIN D in CELL_VIEW HS65_GS_CNSDFPRQTX15 does not have
antenna diff area.
#WARNING (NRDB-728) PIN RN in CELL_VIEW HS65_GS_CNSDFPRQTX15 does not have
antenna diff area.
#WARNING (NRDB-728) PIN TE in CELL_VIEW HS65_GS_CNSDFPRQTX15 does not have
antenna diff area.
#WARNING (NRDB-728 Repeated 20 times. Will be suppressed.) PIN TI in
CELL_VIEW HS65_GS_CNSDFPRQTX15 does not have antenna diff area.
#WARNING (EMS-27) Message (NRDB-728) has exceeded the current message display
limit of 20.
#To increase the message display limit, refer to the product command
reference manual.
#WARNING (NRDB-2005) SPECIAL_NET VDD has special wires but no definition for
instance-pin connection. This will cause routability problems later.
#WARNING (NRDB-2005) SPECIAL_NET VSS has special wires but no definition for
instance-pin connection. This will cause routability problems later.
#Start reading timing information from file .timing_file.tif ...
#
#The worst setup slack read in is -0.162
#
#No hold time constraints read in
#Read in timing information for 388 ports, 9549 instances from timing file
.timing_file.tif.
#NanoRoute Version v09.11-s008 NR100226-1806/USR63-UB
#WARNING (NREX-28) The height of the first routing layer M1 is 0.000000. It
should be larger than 0.000000
#WARNING (NREX-29) The metal thickness of routing layer M1 is 0.000000. It
should be larger than 0.0. Add this to the technology information for better
accuracy.
#WARNING (NREX-30) Please also check the height and metal thickness values
for the routing layers heigher than routing layer M1
#WARNING (NREX-4) No Extended Cap Table was imported. Not enough process
information was provided either and default Extended Cap Table database will
be used.
#Merging special wires...
#Using S.M.A.R.T. routing technology.
#Number of eco nets is 0
#
#Start data preparation...
#Auto generating G-grids with size=15 tracks, using layer M2's pitch = 0.200.
```

```
#Using automatically generated G-grids.
#
#Data preparation is done on Mon May  2 12:45:57 2011
#
#Analyzing routing resource...
#Routing resource analysis is done on Mon May  2 12:45:57 2011
#
#  Resource Analysis:
#
#               Routing  #Total     %Gcell
#  Layer      Direction   Gcell     Blocked
#  ----------------------------------------
#  Metal 1        H        5329      42.86%
#  Metal 2        V        5329       0.00%
#  Metal 3        H        5329       0.00%
#  Metal 4        V        5329       0.00%
#  Metal 5        H        5329       0.00%
#  Metal 6        V        5329       1.33%
#  Metal 7        H        5329       0.00%
#  ----------------------------------------
#  Total                  37303       6.31%
#
#  8 nets (0.08%) with 1 preferred extra spacing.
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.00 (Mb)
#
#start global routing iteration 1...
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.00 (Mb)
#
#start global routing iteration 2...
#
#setting timing driven routing constraints ...
#
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 549.00 (Mb)
#
#start global routing iteration 3...
#cpu time = 00:00:03, elapsed time = 00:00:03, memory = 561.00 (Mb)
#
#start global routing iteration 4...
#cpu time = 00:00:04, elapsed time = 00:00:04, memory = 562.00 (Mb)
#
#start global routing iteration 5...
#cpu time = 00:00:04, elapsed time = 00:00:04, memory = 563.00 (Mb)
#
#start global routing iteration 6...
#cpu time = 00:00:04, elapsed time = 00:00:04, memory = 563.00 (Mb)
#
#
#  Congestion Analysis: (blocked Gcells are excluded)
#
#                 OverCon       OverCon       OverCon
#                  #Gcell        #Gcell        #Gcell    %Gcell
#     Layer         (1-2)         (3-4)         (5-6)   OverCon
```

```
#  ---------------------------------------------------------------
#   Metal 1    122(2.66%)      1(0.02%)      0(0.00%)   (2.68%)
#   Metal 2    320(6.00%)     37(0.69%)      0(0.00%)   (6.70%)
#   Metal 3     34(0.64%)      1(0.02%)      1(0.02%)   (0.68%)
#   Metal 4      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
#   Metal 5      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
#   Metal 6      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
#   Metal 7      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
#  ---------------------------------------------------------------
#     Total    476(1.30%)     39(0.11%)      1(0.00%)   (1.41%)
#
#  The worst congested Gcell overcon (routing demand over resource in number
of tracks) = 6
#
#Complete Global Routing.
#Total wire length = 310452 um.
#Total half perimeter of net bounding box = 209631 um.
#Total wire length on LAYER M1 = 6292 um.
#Total wire length on LAYER M2 = 72773 um.
#Total wire length on LAYER M3 = 87790 um.
#Total wire length on LAYER M4 = 73275 um.
#Total wire length on LAYER M5 = 45258 um.
#Total wire length on LAYER M6 = 13744 um.
#Total wire length on LAYER M7 = 11319 um.
#Total number of vias = 86652
#Up-Via Summary (total 86652):
#
#-----------------------
#  Metal 1        36237
#  Metal 2        28550
#  Metal 3        12341
#  Metal 4         7209
#  Metal 5         1510
#  Metal 6          805
#-----------------------
#                 86652
#
#Max overcon = 6 tracks.
#Total overcon = 1.41%.
#Worst layer Gcell overcon rate = 6.70%.
#Cpu time = 00:00:17
#Elapsed time = 00:00:17
#Increased memory = 15.00 (Mb)
#Total memory = 563.00 (Mb)
#Peak memory = 581.00 (Mb)
#Worst slack with path group effect -0.161700
#Using S.M.A.R.T. routing technology.
#routeSiEffort set to normal
#
#Start Detail Routing.
#start initial detail routing ...
#    number of violations = 610
#cpu time = 00:01:30, elapsed time = 00:01:30, memory = 581.00 (Mb)
#start 1st optimization iteration ...
```

```
#    number of violations = 94
#cpu time = 00:00:18, elapsed time = 00:00:18, memory = 580.00 (Mb)
#start 2nd optimization iteration ...
#    number of violations = 22
#cpu time = 00:00:05, elapsed time = 00:00:05, memory = 580.00 (Mb)
#start 3rd optimization iteration ...
#    number of violations = 8
#cpu time = 00:00:02, elapsed time = 00:00:02, memory = 580.00 (Mb)
#start 4th optimization iteration ...
#    number of violations = 0
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 580.00 (Mb)
#Complete Detail Routing.
#Total wire length = 295228 um.
#Total half perimeter of net bounding box = 209631 um.
#Total wire length on LAYER M1 = 7213 um.
#Total wire length on LAYER M2 = 65870 um.
#Total wire length on LAYER M3 = 78304 um.
#Total wire length on LAYER M4 = 71705 um.
#Total wire length on LAYER M5 = 51494 um.
#Total wire length on LAYER M6 = 12089 um.
#Total wire length on LAYER M7 = 8554 um.
#Total number of vias = 133728
#Total number of multi-cut vias = 429 (  0.3%)
#Total number of single cut vias = 133299 ( 99.7%)
#Up-Via Summary (total 133728):
#                   single-cut          multi-cut      Total
#-----------------------------------------------------------
#  Metal 1       43787 ( 99.8%)        77 (  0.2%)      43864
#  Metal 2       46764 (100.0%)         0 (  0.0%)      46764
#  Metal 3       25042 (100.0%)         0 (  0.0%)      25042
#  Metal 4       15078 ( 97.7%)       352 (  2.3%)      15430
#  Metal 5        1712 (100.0%)         0 (  0.0%)       1712
#  Metal 6         916 (100.0%)         0 (  0.0%)        916
#-----------------------------------------------------------
#               133299 ( 99.7%)       429 (  0.3%)     133728
#
#Total number of DRC violations = 0
#Total number of violations on LAYER M1 = 0
#Total number of violations on LAYER M2 = 0
#Total number of violations on LAYER M3 = 0
#Total number of violations on LAYER M4 = 0
#Total number of violations on LAYER M5 = 0
#Total number of violations on LAYER M6 = 0
#Total number of violations on LAYER M7 = 0
#
#start routing for process antenna violation fix ...
#Worst slack with path group effect -0.161700
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 590.00 (Mb)
#
#Total wire length = 295228 um.
#Total half perimeter of net bounding box = 209631 um.
#Total wire length on LAYER M1 = 7213 um.
#Total wire length on LAYER M2 = 65870 um.
#Total wire length on LAYER M3 = 78304 um.
```

```
#Total wire length on LAYER M4 = 71705 um.
#Total wire length on LAYER M5 = 51494 um.
#Total wire length on LAYER M6 = 12089 um.
#Total wire length on LAYER M7 = 8554 um.
#Total number of vias = 133728
#Total number of multi-cut vias = 429 (  0.3%)
#Total number of single cut vias = 133299 ( 99.7%)
#Up-Via Summary (total 133728):
#                   single-cut          multi-cut      Total
#-----------------------------------------------------------
#  Metal 1       43787 ( 99.8%)        77 (  0.2%)      43864
#  Metal 2       46764 (100.0%)         0 (  0.0%)      46764
#  Metal 3       25042 (100.0%)         0 (  0.0%)      25042
#  Metal 4       15078 ( 97.7%)       352 (  2.3%)      15430
#  Metal 5        1712 (100.0%)         0 (  0.0%)       1712
#  Metal 6         916 (100.0%)         0 (  0.0%)        916
#-----------------------------------------------------------
#               133299 ( 99.7%)       429 (  0.3%)     133728
#
#Total number of DRC violations = 0
#Total number of net violated process antenna rule = 0
#Total number of violations on LAYER M1 = 0
#Total number of violations on LAYER M2 = 0
#Total number of violations on LAYER M3 = 0
#Total number of violations on LAYER M4 = 0
#Total number of violations on LAYER M5 = 0
#Total number of violations on LAYER M6 = 0
#Total number of violations on LAYER M7 = 0
#
#detailRoute Statistics:
#Cpu time = 00:01:57
#Elapsed time = 00:01:58
#Increased memory = 27.00 (Mb)
#Total memory = 590.00 (Mb)
#Peak memory = 593.00 (Mb)
#
#globalDetailRoute statistics:
#Cpu time = 00:02:23
#Elapsed time = 00:02:24
#Increased memory = 49.00 (Mb)
#Total memory = 587.00 (Mb)
#Peak memory = 593.00 (Mb)
#Number of warnings = 27
#Total number of warnings = 27
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Mon May  2 12:48:11 2011
#
<CMD> readCapTable -typical
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable -best
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Best.captable -worst
```

```
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable
**WARN: (ENCEXT-3497):  Options '-best/-worst/-typical' of 'readCapTable' are
obsolete. For single mode two corner analysis and optimization, use MMMC
setup instead of reading multiple captables through command 'readCapTable'.
The obsolete options still works in this release, but to avoid this warning
and to ensure compatibility with future releases, update your script and
configuration file to use MMMC.
Reading Three Cap Table files:  -typical
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable -best
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Best.captable -worst
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable  ...
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMAX.
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMIN.
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMAX.
Reading EXTENDED_CAP_TABLE section completed.
Allocated an empty WireEdgeEnlargement table [0][6]
Allocated an empty WireEdgeEnlargement table [1][6]
Allocated an empty WireEdgeEnlargement table [2][6]
Allocated an empty WireEdgeEnlargement table [0][7]
Allocated an empty WireEdgeEnlargement table [1][7]
Allocated an empty WireEdgeEnlargement table [2][7]
Three process corner capacitance table is used.
<CMD> setExtractRCMode -engine postRoute -force true
<CMD> extractRC
Extraction called for design 'aes_cipher_top' of instances=9549 and nets=9994
using extraction engine 'postRoute' at effort level 'low' .
**WARN: (ENCEXT-3530):  Use of command 'setDesignMode -process
<process_node>' prior to extraction is recommended for maximum accuracy and
optimal automatic threshold setting.
Detail RC Extraction called for design aes_cipher_top.
Process corner(s) are loaded.
Loading corner...  Typical_Case :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable
Loading corner...  Best_Case    :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Best.captable
Loading corner...  Worst_Case   :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7
m4x0y2z_4.2/TECH/cmos065_7m4x0y2z_Worst.captable
extractDetailRC Option : -outfile ./aes_cipher_top_mEmTxU_5637.rcdb.d  -
3Corners
RC Mode: Detail [Extended CapTable, RC Table Resistances, 3 Process Corners]
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Coupling Cap. Scaling Factor : 1.00000
Clock Cap. Scaling Factor    : 1.00000
```

```
Clock Res. Scaling Factor    : 1.00000
Shrink Factor                : 1.00000
Width-based sheet resistance table (silicon width) is used ...
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 587.4M)
Creating parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'
for storing RC.
Extracted 10.0015% (CPU Time= 0:00:00.6  MEM= 587.5M)
Extracted 20.0013% (CPU Time= 0:00:00.7  MEM= 587.5M)
Extracted 30.001% (CPU Time= 0:00:00.9  MEM= 587.5M)
Extracted 40.0016% (CPU Time= 0:00:01.1  MEM= 587.5M)
Extracted 50.0013% (CPU Time= 0:00:01.3  MEM= 587.5M)
Extracted 60.0011% (CPU Time= 0:00:01.6  MEM= 587.5M)
Extracted 70.0017% (CPU Time= 0:00:01.9  MEM= 587.5M)
Extracted 80.0014% (CPU Time= 0:00:02.3  MEM= 587.5M)
Extracted 90.0012% (CPU Time= 0:00:02.7  MEM= 587.5M)
Extracted 100% (CPU Time= 0:00:03.6  MEM= 587.5M)
Nr. Extracted Resistors     : 245601
Nr. Extracted Ground Cap.   : 255403
Nr. Extracted Coupling Cap. : 531536
Opening parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'
for reading.
Filtering XCap in 'relativeOnly' mode using values relative_c_threshold=0.03
and total_c_threshold=5fF.
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 587.5M)
Creating parasitic data file
'./aes_cipher_top_mEmTxU_5637.rcdb_Filter.rcdb.d/header.seq' for storing RC.
Closing parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'.
9808 times net's RC data read were performed.
Opening parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'
for reading.
Detail RC Extraction DONE (CPU Time: 0:00:04.5  Real Time: 0:00:08.0  MEM:
587.441M)
<CMD> rcOut -spef signoff.spef
Opening parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'
for reading.
Dumping Spef file.....
RC Out has the following PVT Info:
   RC-worst
Printing D_NET...
Detail RC Out Completed (CPU Time= 0:00:00.9  MEM= 587.5M)
Closing parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'.
9808 times net's RC data read were performed.
<CMD> setAnalysisMode -analysisType single -checkType setup -skew true -
clockPropagation sdccontrol
<CMD> report_timing -summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 587.4M)
Number of Loop : 0
Start delay calculation (mem=587.441M)...
delayCal using detail RC...
```

```
Opening parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'
for reading.
RC Database In Completed (CPU Time= 0:00:00.2  MEM= 587.5M)
Width-based sheet resistance table (silicon width) is used ...
Closing parasitic data file './aes_cipher_top_mEmTxU_5637.rcdb.d/header.seq'.
9808 times net's RC data read were performed.
Delay calculation completed. (cpu=0:00:01.7 real=0:00:02.0 mem=587.441M 0)
*** CDM Built up (cpu=0:00:02.4  real=0:00:03.0  mem= 587.4M) ***
     +--------------------------------------------------------------------------
-------------------------------------------------------------------+
     |  Path |                      Pin | Cause
|  Slack | Arrival | Required |     Phase | Other Phase |
     |   No. |                          |
|        |         |          |           |             |
     |-------+-------------------------+-----------------------------------
-------------+--------+---------+----------+-----------+-------------|
     |     1 |        \sa32_reg[4] /D ^ | VIOLATED Setup Check with Pin
\sa32_reg[4] /CP   | -0.036 |   2.705 |    2.669 | clk(D)(P) | clk(C)(P) * |
     |     2 |        \sa31_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa31_reg[1] /CP   | -0.032 |   2.739 |    2.708 | clk(D)(P) | clk(C)(P) * |
     |     3 |        \sa20_reg[7] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[7] /CP   | -0.025 |   2.722 |    2.697 | clk(D)(P) | clk(C)(P) * |
     |     4 |        \sa20_reg[3] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[3] /CP   | -0.022 |   2.721 |    2.699 | clk(D)(P) | clk(C)(P) * |
     |     5 |        \sa00_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa00_reg[1] /CP   | -0.020 |   2.769 |    2.749 | clk(D)(P) | clk(C)(P) * |
     |     6 |        \sa23_reg[3] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[3] /CP   | -0.019 |   2.715 |    2.696 | clk(D)(P) | clk(C)(P) * |
     |     7 |        \sa23_reg[6] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[6] /CP   | -0.007 |   2.700 |    2.693 | clk(D)(P) | clk(C)(P) * |
     |     8 |        \sa23_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[1] /CP   | -0.004 |   2.703 |    2.699 | clk(D)(P) | clk(C)(P) * |
     |     9 |        \sa20_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[1] /CP   | -0.002 |   2.704 |    2.702 | clk(D)(P) | clk(C)(P) * |
     |    10 |        \sa32_reg[1] /D ^ | MET Setup Check with Pin
\sa32_reg[1] /CP     |  0.001 |   2.678 |    2.679 | clk(D)(P) | clk(C)(P)
* |
     |    11 |        \sa00_reg[3] /D ^ | MET Setup Check with Pin
\sa00_reg[3] /CP     |  0.002 |   2.750 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    12 |        \sa20_reg[4] /D ^ | MET Setup Check with Pin
\sa20_reg[4] /CP     |  0.003 |   2.698 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    13 |        \sa23_reg[4] /D ^ | MET Setup Check with Pin
\sa23_reg[4] /CP     |  0.003 |   2.697 |    2.700 | clk(D)(P) | clk(C)(P)
* |
     |    14 |        \sa00_reg[4] /D ^ | MET Setup Check with Pin
\sa00_reg[4] /CP     |  0.004 |   2.748 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    15 |        \sa31_reg[4] /D ^ | MET Setup Check with Pin
\sa31_reg[4] /CP     |  0.005 |   2.701 |    2.705 | clk(D)(P) | clk(C)(P)
* |
```

```
     |    16 |        \sa01_reg[1] /D ^ | MET Setup Check with Pin
\sa01_reg[1] /CP        |  0.008 |   2.708 |    2.715 | clk(D)(P) | clk(C)(P)
* |
     |    17 |        \sa21_reg[4] /D ^ | MET Setup Check with Pin
\sa21_reg[4] /CP        |  0.009 |   2.693 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    18 |        \sa11_reg[3] /D ^ | MET Setup Check with Pin
\sa11_reg[3] /CP        |  0.010 |   2.720 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |    19 |        \sa33_reg[1] /D ^ | MET Setup Check with Pin
\sa33_reg[1] /CP        |  0.015 |   2.686 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    20 |        \sa32_reg[3] /D ^ | MET Setup Check with Pin
\sa32_reg[3] /CP        |  0.020 |   2.653 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    21 |        \sa20_reg[0] /D ^ | MET Setup Check with Pin
\sa20_reg[0] /CP        |  0.022 |   2.679 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    22 |    u0/\w_reg[3][25] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][25] /CP    |  0.034 |   2.712 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |    23 |        \sa10_reg[0] /D ^ | MET Setup Check with Pin
\sa10_reg[0] /CP        |  0.040 |   2.660 |    2.700 | clk(D)(P) | clk(C)(P)
* |
     |    24 |        \sa33_reg[5] /D ^ | MET Setup Check with Pin
\sa33_reg[5] /CP        |  0.045 |   2.642 |    2.686 | clk(D)(P) | clk(C)(P)
* |
     |    25 |        \sa33_reg[4] /D ^ | MET Setup Check with Pin
\sa33_reg[4] /CP        |  0.047 |   2.641 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    26 |        \sa20_reg[5] /D ^ | MET Setup Check with Pin
\sa20_reg[5] /CP        |  0.050 |   2.652 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    27 |        \sa10_reg[7] /D ^ | MET Setup Check with Pin
\sa10_reg[7] /CP        |  0.053 |   2.625 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |    28 |        \sa12_reg[1] /D ^ | MET Setup Check with Pin
\sa12_reg[1] /CP        |  0.054 |   2.653 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    29 |        \sa20_reg[2] /D ^ | MET Setup Check with Pin
\sa20_reg[2] /CP        |  0.056 |   2.647 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |    30 |        \sa23_reg[2] /D ^ | MET Setup Check with Pin
\sa23_reg[2] /CP        |  0.060 |   2.626 |    2.686 | clk(D)(P) | clk(C)(P)
* |
     |    31 |        \sa03_reg[1] /D ^ | MET Setup Check with Pin
\sa03_reg[1] /CP        |  0.061 |   2.643 |    2.704 | clk(D)(P) | clk(C)(P)
* |
     |    32 |        \sa21_reg[7] /D ^ | MET Setup Check with Pin
\sa21_reg[7] /CP        |  0.064 |   2.640 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |    33 |        \sa10_reg[5] /D ^ | MET Setup Check with Pin
\sa10_reg[5] /CP        |  0.066 |   2.622 |    2.689 | clk(D)(P) | clk(C)(P)
* |
```

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     |    34 |    u0/\w_reg[3][27] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][27] /CP    |  0.067 |   2.669 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |    35 |        \sa13_reg[7] /D ^ | MET Setup Check with Pin
\sa13_reg[7] /CP        |  0.067 |   2.607 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |    36 |        \sa03_reg[4] /D ^ | MET Setup Check with Pin
\sa03_reg[4] /CP        |  0.068 |   2.638 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    37 |        \sa03_reg[3] /D ^ | MET Setup Check with Pin
\sa03_reg[3] /CP        |  0.071 |   2.636 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    38 |        \sa31_reg[2] /D ^ | MET Setup Check with Pin
\sa31_reg[2] /CP        |  0.072 |   2.627 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |    39 |        \sa21_reg[3] /D ^ | MET Setup Check with Pin
\sa21_reg[3] /CP        |  0.076 |   2.638 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    40 |        \sa13_reg[1] /D ^ | MET Setup Check with Pin
\sa13_reg[1] /CP        |  0.076 |   2.597 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    41 |     u0/\w_reg[3][7] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][7] /CP     |  0.076 |   2.675 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    42 |        \sa21_reg[1] /D ^ | MET Setup Check with Pin
\sa21_reg[1] /CP        |  0.078 |   2.636 |    2.713 | clk(D)(P) | clk(C)(P)
* |
     |    43 |        \sa31_reg[7] /D ^ | MET Setup Check with Pin
\sa31_reg[7] /CP        |  0.078 |   2.631 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |    44 |        \sa12_reg[3] /D ^ | MET Setup Check with Pin
\sa12_reg[3] /CP        |  0.079 |   2.635 |    2.713 | clk(D)(P) | clk(C)(P)
* |
     |    45 |        \sa13_reg[6] /D ^ | MET Setup Check with Pin
\sa13_reg[6] /CP        |  0.081 |   2.600 |    2.681 | clk(D)(P) | clk(C)(P)
* |
     |    46 |        \sa20_reg[6] /D ^ | MET Setup Check with Pin
\sa20_reg[6] /CP        |  0.081 |   2.624 |    2.705 | clk(D)(P) | clk(C)(P)
* |
     |    47 |        \sa01_reg[4] /D ^ | MET Setup Check with Pin
\sa01_reg[4] /CP        |  0.082 |   2.681 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |    48 |        \sa10_reg[2] /D ^ | MET Setup Check with Pin
\sa10_reg[2] /CP        |  0.082 |   2.620 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    49 |        \sa31_reg[3] /D ^ | MET Setup Check with Pin
\sa31_reg[3] /CP        |  0.083 |   2.615 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    50 |        \sa23_reg[0] /D ^ | MET Setup Check with Pin
\sa23_reg[0] /CP        |  0.083 |   2.615 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    51 |        \sa01_reg[3] /D ^ | MET Setup Check with Pin
\sa01_reg[3] /CP        |  0.084 |   2.681 |    2.765 | clk(D)(P) | clk(C)(P)
* |
```

```
     |    52 |        \sa30_reg[7] /D ^ | MET Setup Check with Pin
\sa30_reg[7] /CP        |  0.087 |   2.671 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |    53 |        \sa32_reg[7] /D ^ | MET Setup Check with Pin
\sa32_reg[7] /CP        |  0.090 |   2.586 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |    54 |        \sa21_reg[2] /D ^ | MET Setup Check with Pin
\sa21_reg[2] /CP        |  0.091 |   2.621 |    2.712 | clk(D)(P) | clk(C)(P)
* |
     |    55 |        \sa32_reg[6] /D v | MET Setup Check with Pin
\sa32_reg[6] /CP        |  0.092 |   2.600 |    2.692 | clk(D)(P) | clk(C)(P)
* |
     |    56 |    u0/\w_reg[2][25] /D v | MET Setup Check with Pin
u0/\w_reg[2][25] /CP    |  0.093 |   2.661 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |    57 |        \sa22_reg[4] /D ^ | MET Setup Check with Pin
\sa22_reg[4] /CP        |  0.095 |   2.621 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    58 |        \sa21_reg[5] /D ^ | MET Setup Check with Pin
\sa21_reg[5] /CP        |  0.097 |   2.613 |    2.710 | clk(D)(P) | clk(C)(P)
* |
     |    59 |        \sa10_reg[1] /D ^ | MET Setup Check with Pin
\sa10_reg[1] /CP        |  0.098 |   2.605 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    60 |        \sa11_reg[1] /D ^ | MET Setup Check with Pin
\sa11_reg[1] /CP        |  0.102 |   2.626 |    2.729 | clk(D)(P) | clk(C)(P)
* |
     |    61 |        \sa31_reg[6] /D ^ | MET Setup Check with Pin
\sa31_reg[6] /CP        |  0.103 |   2.615 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |    62 |        \sa00_reg[0] /D ^ | MET Setup Check with Pin
\sa00_reg[0] /CP        |  0.104 |   2.649 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    63 |    u0/\w_reg[3][31] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][31] /CP    |  0.104 |   2.638 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |    64 |        \sa22_reg[3] /D ^ | MET Setup Check with Pin
\sa22_reg[3] /CP        |  0.104 |   2.612 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    65 |        \sa23_reg[7] /D ^ | MET Setup Check with Pin
\sa23_reg[7] /CP        |  0.106 |   2.595 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    66 |        \sa11_reg[2] /D ^ | MET Setup Check with Pin
\sa11_reg[2] /CP        |  0.109 |   2.606 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    67 |        \sa33_reg[7] /D ^ | MET Setup Check with Pin
\sa33_reg[7] /CP        |  0.110 |   2.587 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |    68 |        \sa03_reg[7] /D ^ | MET Setup Check with Pin
\sa03_reg[7] /CP        |  0.112 |   2.594 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    69 |        \sa01_reg[2] /D ^ | MET Setup Check with Pin
\sa01_reg[2] /CP        |  0.114 |   2.602 |    2.717 | clk(D)(P) | clk(C)(P)
* |
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     |    70 |    u0/\w_reg[3][13] /D v | MET Setup Check with Pin
u0/\w_reg[3][13] /CP    |  0.115 |   2.638 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    71 |    u0/\w_reg[3][30] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][30] /CP    |  0.117 |   2.627 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |    72 |        \sa13_reg[3] /D ^ | MET Setup Check with Pin
\sa13_reg[3] /CP        |  0.118 |   2.556 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |    73 |        \sa13_reg[4] /D ^ | MET Setup Check with Pin
\sa13_reg[4] /CP        |  0.118 |   2.560 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |    74 |    u0/\w_reg[3][26] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][26] /CP    |  0.119 |   2.618 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |    75 |        \sa03_reg[5] /D ^ | MET Setup Check with Pin
\sa03_reg[5] /CP        |  0.120 |   2.586 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    76 |        \sa13_reg[2] /D ^ | MET Setup Check with Pin
\sa13_reg[2] /CP        |  0.121 |   2.547 |    2.668 | clk(D)(P) | clk(C)(P)
* |
     |    77 |        \sa10_reg[3] /D ^ | MET Setup Check with Pin
\sa10_reg[3] /CP        |  0.122 |   2.582 |    2.704 | clk(D)(P) | clk(C)(P)
* |
     |    78 |        \sa31_reg[5] /D ^ | MET Setup Check with Pin
\sa31_reg[5] /CP        |  0.126 |   2.583 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |    79 |        \sa21_reg[6] /D ^ | MET Setup Check with Pin
\sa21_reg[6] /CP        |  0.127 |   2.588 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    80 |    u0/\w_reg[3][28] /D v | MET Setup Check with Pin
u0/\w_reg[3][28] /CP    |  0.127 |   2.628 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |    81 |        \sa30_reg[1] /D ^ | MET Setup Check with Pin
\sa30_reg[1] /CP        |  0.128 |   2.630 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |    82 |    u0/\w_reg[3][14] /D v | MET Setup Check with Pin
u0/\w_reg[3][14] /CP    |  0.128 |   2.624 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    83 |        \sa13_reg[5] /D ^ | MET Setup Check with Pin
\sa13_reg[5] /CP        |  0.129 |   2.550 |    2.679 | clk(D)(P) | clk(C)(P)
* |
     |    84 |        \sa02_reg[4] /D ^ | MET Setup Check with Pin
\sa02_reg[4] /CP        |  0.129 |   2.604 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |    85 |    u0/\w_reg[3][24] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][24] /CP    |  0.131 |   2.614 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |    86 |        \sa33_reg[3] /D ^ | MET Setup Check with Pin
\sa33_reg[3] /CP        |  0.133 |   2.566 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    87 |    u0/\w_reg[2][27] /D v | MET Setup Check with Pin
u0/\w_reg[2][27] /CP    |  0.134 |   2.618 |    2.752 | clk(D)(P) | clk(C)(P)
* |
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     |    88 |    u0/\w_reg[3][21] /D v | MET Setup Check with Pin
u0/\w_reg[3][21] /CP    |  0.135 |   2.612 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |    89 |        \sa10_reg[6] /D ^ | MET Setup Check with Pin
\sa10_reg[6] /CP        |  0.135 |   2.552 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    90 |        \sa22_reg[1] /D ^ | MET Setup Check with Pin
\sa22_reg[1] /CP        |  0.137 |   2.577 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    91 |        \sa33_reg[6] /D ^ | MET Setup Check with Pin
\sa33_reg[6] /CP        |  0.137 |   2.551 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    92 |        \sa13_reg[0] /D ^ | MET Setup Check with Pin
\sa13_reg[0] /CP        |  0.139 |   2.535 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    93 |     u0/\w_reg[3][8] /D v | MET Setup Check with Pin
u0/\w_reg[3][8] /CP     |  0.144 |   2.620 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |    94 |        \sa22_reg[0] /D ^ | MET Setup Check with Pin
\sa22_reg[0] /CP        |  0.144 |   2.562 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    95 |        \sa12_reg[0] /D ^ | MET Setup Check with Pin
\sa12_reg[0] /CP        |  0.146 |   2.562 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |    96 |     u0/\w_reg[3][2] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][2] /CP     |  0.147 |   2.603 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |    97 |        \sa02_reg[1] /D ^ | MET Setup Check with Pin
\sa02_reg[1] /CP        |  0.147 |   2.588 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |    98 |        \sa11_reg[5] /D ^ | MET Setup Check with Pin
\sa11_reg[5] /CP        |  0.148 |   2.586 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |    99 |        \sa23_reg[5] /D ^ | MET Setup Check with Pin
\sa23_reg[5] /CP        |  0.150 |   2.544 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   100 |    u0/\w_reg[3][10] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][10] /CP    |  0.151 |   2.597 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   101 |        \sa30_reg[3] /D ^ | MET Setup Check with Pin
\sa30_reg[3] /CP        |  0.151 |   2.608 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   102 |     u0/\w_reg[3][6] /D v | MET Setup Check with Pin
u0/\w_reg[3][6] /CP     |  0.152 |   2.615 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   103 |        \sa10_reg[4] /D ^ | MET Setup Check with Pin
\sa10_reg[4] /CP        |  0.156 |   2.546 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |   104 |     u0/\w_reg[2][7] /D v | MET Setup Check with Pin
u0/\w_reg[2][7] /CP     |  0.156 |   2.606 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   105 |        \sa32_reg[5] /D v | MET Setup Check with Pin
\sa32_reg[5] /CP        |  0.157 |   2.531 |    2.688 | clk(D)(P) | clk(C)(P)
* |
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     |   106 |        \sa12_reg[2] /D ^ | MET Setup Check with Pin
\sa12_reg[2] /CP        |  0.160 |   2.534 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   107 |     u0/\w_reg[3][5] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][5] /CP     |  0.161 |   2.588 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   108 |        \sa21_reg[0] /D ^ | MET Setup Check with Pin
\sa21_reg[0] /CP        |  0.163 |   2.552 |    2.715 | clk(D)(P) | clk(C)(P)
* |
     |   109 |        \sa00_reg[7] /D ^ | MET Setup Check with Pin
\sa00_reg[7] /CP        |  0.164 |   2.585 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   110 |        \sa30_reg[6] /D ^ | MET Setup Check with Pin
\sa30_reg[6] /CP        |  0.165 |   2.591 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   111 |        \sa03_reg[0] /D ^ | MET Setup Check with Pin
\sa03_reg[0] /CP        |  0.166 |   2.540 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   112 |        \sa11_reg[7] /D ^ | MET Setup Check with Pin
\sa11_reg[7] /CP        |  0.166 |   2.570 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   113 |        \sa32_reg[0] /D ^ | MET Setup Check with Pin
\sa32_reg[0] /CP        |  0.168 |   2.509 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |   114 |        \sa01_reg[5] /D ^ | MET Setup Check with Pin
\sa01_reg[5] /CP        |  0.169 |   2.586 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   115 |        \sa01_reg[0] /D ^ | MET Setup Check with Pin
\sa01_reg[0] /CP        |  0.170 |   2.595 |    2.765 | clk(D)(P) | clk(C)(P)
* |
     |   116 |    u0/\w_reg[2][31] /D v | MET Setup Check with Pin
u0/\w_reg[2][31] /CP    |  0.172 |   2.578 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   117 |        \sa30_reg[4] /D ^ | MET Setup Check with Pin
\sa30_reg[4] /CP        |  0.173 |   2.584 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   118 |        \sa11_reg[4] /D ^ | MET Setup Check with Pin
\sa11_reg[4] /CP        |  0.174 |   2.560 |    2.735 | clk(D)(P) | clk(C)(P)
* |
     |   119 |        \sa32_reg[2] /D ^ | MET Setup Check with Pin
\sa32_reg[2] /CP        |  0.175 |   2.499 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |   120 |        \sa01_reg[7] /D ^ | MET Setup Check with Pin
\sa01_reg[7] /CP        |  0.176 |   2.585 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   121 |        \sa11_reg[6] /D ^ | MET Setup Check with Pin
\sa11_reg[6] /CP        |  0.177 |   2.560 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   122 |        \sa12_reg[7] /D ^ | MET Setup Check with Pin
\sa12_reg[7] /CP        |  0.179 |   2.541 |    2.720 | clk(D)(P) | clk(C)(P)
* |
     |   123 |        \sa12_reg[4] /D ^ | MET Setup Check with Pin
\sa12_reg[4] /CP        |  0.180 |   2.536 |    2.716 | clk(D)(P) | clk(C)(P)
* |
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```
     |   124 |        \sa31_reg[0] /D ^ | MET Setup Check with Pin
\sa31_reg[0] /CP        |  0.181 |   2.522 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   125 |    u0/\w_reg[3][29] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][29] /CP    |  0.182 |   2.555 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   126 |        \sa03_reg[2] /D ^ | MET Setup Check with Pin
\sa03_reg[2] /CP        |  0.183 |   2.519 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   127 |    u0/\w_reg[2][30] /D v | MET Setup Check with Pin
u0/\w_reg[2][30] /CP    |  0.183 |   2.567 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   128 |        \sa30_reg[2] /D ^ | MET Setup Check with Pin
\sa30_reg[2] /CP        |  0.185 |   2.574 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   129 |    u0/\w_reg[2][26] /D v | MET Setup Check with Pin
u0/\w_reg[2][26] /CP    |  0.186 |   2.563 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   130 |        \sa11_reg[0] /D ^ | MET Setup Check with Pin
\sa11_reg[0] /CP        |  0.189 |   2.547 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   131 |        \sa02_reg[2] /D ^ | MET Setup Check with Pin
\sa02_reg[2] /CP        |  0.191 |   2.541 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   132 |     u0/\w_reg[3][9] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][9] /CP     |  0.191 |   2.546 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   133 |        \sa33_reg[2] /D ^ | MET Setup Check with Pin
\sa33_reg[2] /CP        |  0.192 |   2.502 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   134 |        \sa03_reg[6] /D ^ | MET Setup Check with Pin
\sa03_reg[6] /CP        |  0.193 |   2.508 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   135 |        \sa01_reg[6] /D ^ | MET Setup Check with Pin
\sa01_reg[6] /CP        |  0.195 |   2.563 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   136 |        \sa02_reg[7] /D ^ | MET Setup Check with Pin
\sa02_reg[7] /CP        |  0.199 |   2.535 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   137 |    u0/\w_reg[2][13] /D v | MET Setup Check with Pin
u0/\w_reg[2][13] /CP    |  0.200 |   2.548 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   138 |     u0/\w_reg[3][1] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][1] /CP     |  0.201 |   2.549 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   139 |    u0/\w_reg[2][28] /D v | MET Setup Check with Pin
u0/\w_reg[2][28] /CP    |  0.203 |   2.552 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |   140 |    u0/\w_reg[2][24] /D v | MET Setup Check with Pin
u0/\w_reg[2][24] /CP    |  0.206 |   2.547 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   141 |    u0/\w_reg[2][21] /D v | MET Setup Check with Pin
u0/\w_reg[2][21] /CP    |  0.208 |   2.537 |    2.744 | clk(D)(P) | clk(C)(P)
* |
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```
     |   142 |        \sa00_reg[5] /D ^ | MET Setup Check with Pin
\sa00_reg[5] /CP        |  0.209 |   2.542 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   143 |        \sa12_reg[5] /D ^ | MET Setup Check with Pin
\sa12_reg[5] /CP        |  0.209 |   2.508 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   144 |        \sa30_reg[0] /D ^ | MET Setup Check with Pin
\sa30_reg[0] /CP        |  0.210 |   2.547 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   145 |        \sa02_reg[5] /D ^ | MET Setup Check with Pin
\sa02_reg[5] /CP        |  0.211 |   2.520 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   146 |    u0/\w_reg[3][15] /D v | MET Setup Check with Pin
u0/\w_reg[3][15] /CP    |  0.214 |   2.539 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   147 |    u0/\w_reg[2][14] /D v | MET Setup Check with Pin
u0/\w_reg[2][14] /CP    |  0.214 |   2.533 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   148 |        \sa00_reg[6] /D ^ | MET Setup Check with Pin
\sa00_reg[6] /CP        |  0.216 |   2.539 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |   149 |     u0/\w_reg[3][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][0] /CP     |  0.216 |   2.533 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   150 |        \sa22_reg[2] /D ^ | MET Setup Check with Pin
\sa22_reg[2] /CP        |  0.219 |   2.492 |    2.711 | clk(D)(P) | clk(C)(P)
* |
     |   151 |        \sa22_reg[6] /D ^ | MET Setup Check with Pin
\sa22_reg[6] /CP        |  0.219 |   2.507 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   152 |    u0/\w_reg[3][12] /D v | MET Setup Check with Pin
u0/\w_reg[3][12] /CP    |  0.221 |   2.528 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   153 |    u0/\w_reg[3][22] /D v | MET Setup Check with Pin
u0/\w_reg[3][22] /CP    |  0.222 |   2.524 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   154 |        \sa02_reg[3] /D ^ | MET Setup Check with Pin
\sa02_reg[3] /CP        |  0.222 |   2.510 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   155 |     u0/\w_reg[2][2] /D v | MET Setup Check with Pin
u0/\w_reg[2][2] /CP     |  0.222 |   2.535 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   156 |    u0/\w_reg[3][18] /D v | MET Setup Check with Pin
u0/\w_reg[3][18] /CP    |  0.223 |   2.531 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   157 |        \sa22_reg[7] /D ^ | MET Setup Check with Pin
\sa22_reg[7] /CP        |  0.223 |   2.503 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   158 |     u0/\w_reg[3][3] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][3] /CP     |  0.223 |   2.514 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   159 |    u0/\w_reg[2][10] /D v | MET Setup Check with Pin
u0/\w_reg[2][10] /CP    |  0.226 |   2.534 |    2.759 | clk(D)(P) | clk(C)(P)
* |
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```
     |   160 |     u0/\w_reg[2][6] /D v | MET Setup Check with Pin
u0/\w_reg[2][6] /CP     |  0.227 |   2.537 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   161 |     u0/\w_reg[2][5] /D v | MET Setup Check with Pin
u0/\w_reg[2][5] /CP     |  0.227 |   2.536 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   162 |    u0/\w_reg[3][11] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][11] /CP    |  0.229 |   2.510 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   163 |    u0/\w_reg[3][23] /D v | MET Setup Check with Pin
u0/\w_reg[3][23] /CP    |  0.230 |   2.531 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   164 |        \sa22_reg[5] /D ^ | MET Setup Check with Pin
\sa22_reg[5] /CP        |  0.231 |   2.488 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   165 |     u0/\w_reg[2][8] /D v | MET Setup Check with Pin
u0/\w_reg[2][8] /CP     |  0.232 |   2.528 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   166 |        \sa02_reg[0] /D ^ | MET Setup Check with Pin
\sa02_reg[0] /CP        |  0.233 |   2.500 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   167 |        \sa33_reg[0] /D ^ | MET Setup Check with Pin
\sa33_reg[0] /CP        |  0.239 |   2.452 |    2.691 | clk(D)(P) | clk(C)(P)
* |
     |   168 |        \sa30_reg[5] /D ^ | MET Setup Check with Pin
\sa30_reg[5] /CP        |  0.243 |   2.517 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   169 |    u0/\w_reg[1][25] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][25] /CP    |  0.245 |   2.519 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   170 |        \sa02_reg[6] /D ^ | MET Setup Check with Pin
\sa02_reg[6] /CP        |  0.247 |   2.483 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   171 |    u0/\w_reg[2][29] /D v | MET Setup Check with Pin
u0/\w_reg[2][29] /CP    |  0.249 |   2.500 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   172 |     u0/\w_reg[3][4] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][4] /CP     |  0.252 |   2.496 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   173 |        \sa00_reg[2] /D ^ | MET Setup Check with Pin
\sa00_reg[2] /CP        |  0.254 |   2.497 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   174 |     u0/\w_reg[2][9] /D v | MET Setup Check with Pin
u0/\w_reg[2][9] /CP     |  0.269 |   2.477 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   175 |     u0/\w_reg[2][1] /D v | MET Setup Check with Pin
u0/\w_reg[2][1] /CP     |  0.273 |   2.489 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   176 |    u0/\w_reg[3][20] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][20] /CP    |  0.279 |   2.459 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   177 |    u0/\w_reg[3][16] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][16] /CP    |  0.283 |   2.457 |    2.740 | clk(D)(P) | clk(C)(P)
* |
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     |   178 |     u0/\w_reg[1][7] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][7] /CP     |  0.283 |   2.479 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   179 |    u0/\w_reg[2][15] /D v | MET Setup Check with Pin
u0/\w_reg[2][15] /CP    |  0.288 |   2.459 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   180 |        \sa12_reg[6] /D ^ | MET Setup Check with Pin
\sa12_reg[6] /CP        |  0.289 |   2.432 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   181 |    u0/\w_reg[2][18] /D v | MET Setup Check with Pin
u0/\w_reg[2][18] /CP    |  0.291 |   2.457 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   182 |     u0/\w_reg[2][0] /D v | MET Setup Check with Pin
u0/\w_reg[2][0] /CP     |  0.291 |   2.469 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   183 |    u0/\w_reg[2][22] /D v | MET Setup Check with Pin
u0/\w_reg[2][22] /CP    |  0.295 |   2.449 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   184 |    u0/\w_reg[1][27] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][27] /CP    |  0.296 |   2.468 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   185 |    u0/\w_reg[2][12] /D v | MET Setup Check with Pin
u0/\w_reg[2][12] /CP    |  0.299 |   2.450 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   186 |    u0/\w_reg[3][17] /D v | MET Setup Check with Pin
u0/\w_reg[3][17] /CP    |  0.306 |   2.448 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   187 |     u0/\w_reg[2][3] /D v | MET Setup Check with Pin
u0/\w_reg[2][3] /CP     |  0.307 |   2.449 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   188 |    u0/\w_reg[1][30] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][30] /CP    |  0.309 |   2.437 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   189 |    u0/\w_reg[2][23] /D v | MET Setup Check with Pin
u0/\w_reg[2][23] /CP    |  0.311 |   2.444 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |   190 |    u0/\w_reg[1][10] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][10] /CP    |  0.313 |   2.421 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |   191 |    u0/\w_reg[1][31] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][31] /CP    |  0.316 |   2.447 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   192 |    u0/\w_reg[3][19] /D v | MET Setup Check with Pin
u0/\w_reg[3][19] /CP    |  0.321 |   2.427 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   193 |    u0/\w_reg[2][11] /D v | MET Setup Check with Pin
u0/\w_reg[2][11] /CP    |  0.324 |   2.434 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   194 |     u0/\w_reg[2][4] /D v | MET Setup Check with Pin
u0/\w_reg[2][4] /CP     |  0.324 |   2.433 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   195 |    u0/\w_reg[1][13] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][13] /CP    |  0.325 |   2.439 |    2.763 | clk(D)(P) | clk(C)(P)
* |
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```
     |   196 |    u0/\w_reg[1][26] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][26] /CP    |  0.339 |   2.425 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   197 |    u0/\w_reg[1][21] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][21] /CP    |  0.339 |   2.421 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   198 |    u0/\w_reg[1][14] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][14] /CP    |  0.340 |   2.424 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   199 |    u0/\w_reg[1][28] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][28] /CP    |  0.343 |   2.421 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   200 |     u0/\w_reg[1][8] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][8] /CP     |  0.346 |   2.418 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   201 |     u0/\w_reg[1][2] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][2] /CP     |  0.346 |   2.416 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   202 |     u0/\w_reg[1][6] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][6] /CP     |  0.349 |   2.413 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   203 |    u0/\w_reg[1][24] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][24] /CP    |  0.349 |   2.409 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   204 |     u0/\w_reg[1][5] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][5] /CP     |  0.355 |   2.407 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   205 |    u0/\w_reg[2][20] /D v | MET Setup Check with Pin
u0/\w_reg[2][20] /CP    |  0.355 |   2.392 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   206 |    u0/\w_reg[2][16] /D v | MET Setup Check with Pin
u0/\w_reg[2][16] /CP    |  0.365 |   2.383 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   207 |     u0/\w_reg[1][9] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][9] /CP     |  0.372 |   2.367 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   208 |   \text_out_reg[13] /D v | MET Setup Check with Pin
\text_out_reg[13] /CP   |  0.376 |   2.356 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   209 |    u0/\w_reg[1][29] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][29] /CP    |  0.379 |   2.367 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   210 |    u0/\w_reg[2][17] /D v | MET Setup Check with Pin
u0/\w_reg[2][17] /CP    |  0.381 |   2.368 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   211 |     u0/\w_reg[1][1] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][1] /CP     |  0.394 |   2.368 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   212 |    u0/\w_reg[2][19] /D v | MET Setup Check with Pin
u0/\w_reg[2][19] /CP    |  0.398 |   2.350 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   213 |    u0/\w_reg[1][11] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][11] /CP    |  0.411 |   2.324 |    2.735 | clk(D)(P) | clk(C)(P)
* |
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     |   214 |    u0/\w_reg[1][15] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][15] /CP    |  0.418 |   2.346 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   215 |     u0/\w_reg[1][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][0] /CP     |  0.421 |   2.340 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   216 |    u0/\w_reg[1][18] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][18] /CP    |  0.421 |   2.342 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   217 |    u0/\w_reg[1][12] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][12] /CP    |  0.426 |   2.338 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   218 |    u0/\w_reg[1][23] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][23] /CP    |  0.428 |   2.336 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   219 |    u0/\w_reg[1][22] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][22] /CP    |  0.428 |   2.332 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   220 |  \text_out_reg[120] /D v | MET Setup Check with Pin
\text_out_reg[120] /CP  |  0.429 |   2.337 |    2.766 | clk(D)(P) | clk(C)(P)
* |
     |   221 |     u0/\w_reg[1][3] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][3] /CP     |  0.429 |   2.333 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   222 |  \text_out_reg[121] /D v | MET Setup Check with Pin
\text_out_reg[121] /CP  |  0.444 |   2.323 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   223 |    u0/\w_reg[0][25] /D v | MET Setup Check with Pin
u0/\w_reg[0][25] /CP    |  0.446 |   2.335 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   224 |     u0/\w_reg[1][4] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][4] /CP     |  0.449 |   2.312 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   225 |    u0/\w_reg[0][30] /D v | MET Setup Check with Pin
u0/\w_reg[0][30] /CP    |  0.449 |   2.307 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   226 |   \text_out_reg[14] /D ^ | MET Setup Check with Pin
\text_out_reg[14] /CP   |  0.453 |   2.255 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   227 |    u0/\w_reg[0][13] /D v | MET Setup Check with Pin
u0/\w_reg[0][13] /CP    |  0.453 |   2.327 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   228 |  \text_out_reg[122] /D v | MET Setup Check with Pin
\text_out_reg[122] /CP  |  0.458 |   2.305 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   229 |    \text_out_reg[0] /D v | MET Setup Check with Pin
\text_out_reg[0] /CP    |  0.459 |   2.237 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   230 |   \text_out_reg[65] /D v | MET Setup Check with Pin
\text_out_reg[65] /CP   |  0.463 |   2.320 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   231 |    \text_out_reg[9] /D ^ | MET Setup Check with Pin
\text_out_reg[9] /CP    |  0.465 |   2.258 |    2.723 | clk(D)(P) | clk(C)(P)
* |
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     |   232 |   \text_out_reg[82] /D v | MET Setup Check with Pin
\text_out_reg[82] /CP   |  0.467 |   2.252 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   233 |   \text_out_reg[32] /D v | MET Setup Check with Pin
\text_out_reg[32] /CP   |  0.472 |   2.263 |    2.735 | clk(D)(P) | clk(C)(P)
* |
     |   234 |  \text_out_reg[127] /D v | MET Setup Check with Pin
\text_out_reg[127] /CP  |  0.473 |   2.294 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   235 |  \text_out_reg[125] /D ^ | MET Setup Check with Pin
\text_out_reg[125] /CP  |  0.473 |   2.281 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |   236 |    u0/\w_reg[0][31] /D v | MET Setup Check with Pin
u0/\w_reg[0][31] /CP    |  0.480 |   2.301 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   237 |    u0/\w_reg[0][14] /D v | MET Setup Check with Pin
u0/\w_reg[0][14] /CP    |  0.481 |   2.300 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   238 |   \text_out_reg[93] /D v | MET Setup Check with Pin
\text_out_reg[93] /CP   |  0.485 |   2.302 |    2.786 | clk(D)(P) | clk(C)(P)
* |
     |   239 |    u0/\w_reg[1][20] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][20] /CP    |  0.485 |   2.278 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   240 |    \text_out_reg[5] /D v | MET Setup Check with Pin
\text_out_reg[5] /CP    |  0.489 |   2.208 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |   241 |    u0/\w_reg[1][16] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][16] /CP    |  0.491 |   2.273 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   242 |   \text_out_reg[87] /D ^ | MET Setup Check with Pin
\text_out_reg[87] /CP   |  0.493 |   2.246 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   243 |     u0/\w_reg[0][8] /D v | MET Setup Check with Pin
u0/\w_reg[0][8] /CP     |  0.494 |   2.287 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   244 |   \text_out_reg[64] /D v | MET Setup Check with Pin
\text_out_reg[64] /CP   |  0.496 |   2.256 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |   245 |     u0/\w_reg[0][7] /D v | MET Setup Check with Pin
u0/\w_reg[0][7] /CP     |  0.496 |   2.277 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   246 |   \text_out_reg[56] /D v | MET Setup Check with Pin
\text_out_reg[56] /CP   |  0.497 |   2.242 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   247 |   \text_out_reg[29] /D v | MET Setup Check with Pin
\text_out_reg[29] /CP   |  0.498 |   2.221 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   248 |    u0/\w_reg[0][10] /D v | MET Setup Check with Pin
u0/\w_reg[0][10] /CP    |  0.499 |   2.282 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   249 |  \text_out_reg[101] /D ^ | MET Setup Check with Pin
\text_out_reg[101] /CP  |  0.501 |   2.240 |    2.741 | clk(D)(P) | clk(C)(P)
* |
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     |   250 |   \text_out_reg[97] /D ^ | MET Setup Check with Pin
\text_out_reg[97] /CP   |  0.504 |   2.241 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   251 |    u0/\w_reg[0][28] /D v | MET Setup Check with Pin
u0/\w_reg[0][28] /CP    |  0.504 |   2.278 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   252 |   \text_out_reg[69] /D v | MET Setup Check with Pin
\text_out_reg[69] /CP   |  0.506 |   2.276 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   253 |   \text_out_reg[26] /D v | MET Setup Check with Pin
\text_out_reg[26] /CP   |  0.509 |   2.200 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   254 |   \text_out_reg[70] /D v | MET Setup Check with Pin
\text_out_reg[70] /CP   |  0.509 |   2.270 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   255 |   \text_out_reg[15] /D v | MET Setup Check with Pin
\text_out_reg[15] /CP   |  0.512 |   2.225 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   256 |  \text_out_reg[117] /D ^ | MET Setup Check with Pin
\text_out_reg[117] /CP  |  0.512 |   2.232 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   257 |   \text_out_reg[54] /D v | MET Setup Check with Pin
\text_out_reg[54] /CP   |  0.512 |   2.223 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   258 |   \text_out_reg[89] /D v | MET Setup Check with Pin
\text_out_reg[89] /CP   |  0.513 |   2.273 |    2.786 | clk(D)(P) | clk(C)(P)
* |
     |   259 |   \text_out_reg[17] /D v | MET Setup Check with Pin
\text_out_reg[17] /CP   |  0.514 |   2.214 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   260 |    u0/\w_reg[1][17] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][17] /CP    |  0.514 |   2.249 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   261 |   \text_out_reg[81] /D v | MET Setup Check with Pin
\text_out_reg[81] /CP   |  0.517 |   2.265 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   262 |   \text_out_reg[23] /D v | MET Setup Check with Pin
\text_out_reg[23] /CP   |  0.517 |   2.215 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   263 |    u0/\w_reg[0][21] /D v | MET Setup Check with Pin
u0/\w_reg[0][21] /CP    |  0.521 |   2.257 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   264 |   \text_out_reg[37] /D v | MET Setup Check with Pin
\text_out_reg[37] /CP   |  0.521 |   2.224 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   265 |    u0/\w_reg[0][27] /D v | MET Setup Check with Pin
u0/\w_reg[0][27] /CP    |  0.523 |   2.259 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   266 |   \text_out_reg[52] /D ^ | MET Setup Check with Pin
\text_out_reg[52] /CP   |  0.523 |   2.196 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   267 |   \text_out_reg[90] /D ^ | MET Setup Check with Pin
\text_out_reg[90] /CP   |  0.526 |   2.220 |    2.745 | clk(D)(P) | clk(C)(P)
* |
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     |   268 |    u0/\w_reg[1][19] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][19] /CP    |  0.526 |   2.237 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   269 |   \text_out_reg[88] /D v | MET Setup Check with Pin
\text_out_reg[88] /CP   |  0.526 |   2.255 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   270 |     u0/\w_reg[0][2] /D v | MET Setup Check with Pin
u0/\w_reg[0][2] /CP     |  0.528 |   2.251 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   271 |  \text_out_reg[109] /D v | MET Setup Check with Pin
\text_out_reg[109] /CP  |  0.528 |   2.232 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   272 |  \text_out_reg[103] /D ^ | MET Setup Check with Pin
\text_out_reg[103] /CP  |  0.528 |   2.220 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   273 |    u0/\w_reg[0][26] /D v | MET Setup Check with Pin
u0/\w_reg[0][26] /CP    |  0.530 |   2.252 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   274 |   \text_out_reg[49] /D v | MET Setup Check with Pin
\text_out_reg[49] /CP   |  0.533 |   2.210 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   275 |   \text_out_reg[57] /D v | MET Setup Check with Pin
\text_out_reg[57] /CP   |  0.534 |   2.209 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   276 |    u0/\w_reg[0][29] /D v | MET Setup Check with Pin
u0/\w_reg[0][29] /CP    |  0.537 |   2.219 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   277 |     u0/\w_reg[0][9] /D v | MET Setup Check with Pin
u0/\w_reg[0][9] /CP     |  0.538 |   2.244 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   278 |   \text_out_reg[25] /D v | MET Setup Check with Pin
\text_out_reg[25] /CP   |  0.539 |   2.179 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   279 |   \text_out_reg[79] /D v | MET Setup Check with Pin
\text_out_reg[79] /CP   |  0.540 |   2.182 |    2.722 | clk(D)(P) | clk(C)(P)
* |
     |   280 |    \text_out_reg[2] /D v | MET Setup Check with Pin
\text_out_reg[2] /CP    |  0.542 |   2.151 |    2.693 | clk(D)(P) | clk(C)(P)
* |
     |   281 |    u0/\w_reg[0][12] /D v | MET Setup Check with Pin
u0/\w_reg[0][12] /CP    |  0.542 |   2.238 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   282 |     u0/\w_reg[0][6] /D ^ | MET Setup Check with Pin
u0/\w_reg[0][6] /CP     |  0.543 |   2.216 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   283 |   \text_out_reg[30] /D v | MET Setup Check with Pin
\text_out_reg[30] /CP   |  0.544 |   2.164 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   284 |    u0/\w_reg[0][24] /D v | MET Setup Check with Pin
u0/\w_reg[0][24] /CP    |  0.544 |   2.238 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   285 |     u0/\w_reg[0][5] /D v | MET Setup Check with Pin
u0/\w_reg[0][5] /CP     |  0.544 |   2.232 |    2.776 | clk(D)(P) | clk(C)(P)
* |
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     |   286 |   \text_out_reg[66] /D v | MET Setup Check with Pin
\text_out_reg[66] /CP   |  0.547 |   2.238 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   287 |    u0/\w_reg[0][15] /D v | MET Setup Check with Pin
u0/\w_reg[0][15] /CP    |  0.547 |   2.232 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   288 |    u0/\w_reg[0][23] /D v | MET Setup Check with Pin
u0/\w_reg[0][23] /CP    |  0.548 |   2.234 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   289 |   \text_out_reg[12] /D v | MET Setup Check with Pin
\text_out_reg[12] /CP   |  0.548 |   2.189 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   290 |  \text_out_reg[102] /D ^ | MET Setup Check with Pin
\text_out_reg[102] /CP  |  0.549 |   2.194 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   291 |   \text_out_reg[94] /D v | MET Setup Check with Pin
\text_out_reg[94] /CP   |  0.551 |   2.232 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   292 |   \text_out_reg[33] /D v | MET Setup Check with Pin
\text_out_reg[33] /CP   |  0.552 |   2.185 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   293 |    u0/\w_reg[0][18] /D v | MET Setup Check with Pin
u0/\w_reg[0][18] /CP    |  0.552 |   2.192 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   294 |  \text_out_reg[119] /D v | MET Setup Check with Pin
\text_out_reg[119] /CP  |  0.556 |   2.211 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   295 |   \text_out_reg[72] /D v | MET Setup Check with Pin
\text_out_reg[72] /CP   |  0.557 |   2.167 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   296 |   \text_out_reg[84] /D v | MET Setup Check with Pin
\text_out_reg[84] /CP   |  0.558 |   2.221 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   297 |   \text_out_reg[77] /D v | MET Setup Check with Pin
\text_out_reg[77] /CP   |  0.561 |   2.167 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   298 |   \text_out_reg[85] /D v | MET Setup Check with Pin
\text_out_reg[85] /CP   |  0.564 |   2.221 |    2.784 | clk(D)(P) | clk(C)(P)
* |
     |   299 |   \text_out_reg[34] /D v | MET Setup Check with Pin
\text_out_reg[34] /CP   |  0.565 |   2.171 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   300 |   \text_out_reg[48] /D ^ | MET Setup Check with Pin
\text_out_reg[48] /CP   |  0.567 |   2.152 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   301 |    \text_out_reg[8] /D ^ | MET Setup Check with Pin
\text_out_reg[8] /CP    |  0.569 |   2.142 |    2.711 | clk(D)(P) | clk(C)(P)
* |
     |   302 |  \text_out_reg[126] /D v | MET Setup Check with Pin
\text_out_reg[126] /CP  |  0.570 |   2.204 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   303 |  \text_out_reg[118] /D ^ | MET Setup Check with Pin
\text_out_reg[118] /CP  |  0.572 |   2.165 |    2.738 | clk(D)(P) | clk(C)(P)
* |
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```
     |   304 |   \text_out_reg[96] /D ^ | MET Setup Check with Pin
\text_out_reg[96] /CP   |  0.573 |   2.176 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   305 |    \text_out_reg[7] /D v | MET Setup Check with Pin
\text_out_reg[7] /CP    |  0.573 |   2.126 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   306 |   \text_out_reg[73] /D v | MET Setup Check with Pin
\text_out_reg[73] /CP   |  0.575 |   2.150 |    2.725 | clk(D)(P) | clk(C)(P)
* |
     |   307 |  \text_out_reg[123] /D v | MET Setup Check with Pin
\text_out_reg[123] /CP  |  0.578 |   2.192 |    2.769 | clk(D)(P) | clk(C)(P)
* |
     |   308 |  \text_out_reg[100] /D v | MET Setup Check with Pin
\text_out_reg[100] /CP  |  0.579 |   2.200 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   309 |   \text_out_reg[92] /D v | MET Setup Check with Pin
\text_out_reg[92] /CP   |  0.580 |   2.203 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   310 |  \text_out_reg[124] /D v | MET Setup Check with Pin
\text_out_reg[124] /CP  |  0.582 |   2.192 |    2.774 | clk(D)(P) | clk(C)(P)
* |
     |   311 |   \text_out_reg[39] /D v | MET Setup Check with Pin
\text_out_reg[39] /CP   |  0.583 |   2.159 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   312 |   \text_out_reg[24] /D v | MET Setup Check with Pin
\text_out_reg[24] /CP   |  0.583 |   2.128 |    2.712 | clk(D)(P) | clk(C)(P)
* |
     |   313 |   \text_out_reg[95] /D ^ | MET Setup Check with Pin
\text_out_reg[95] /CP   |  0.584 |   2.177 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   314 |   \text_out_reg[21] /D v | MET Setup Check with Pin
\text_out_reg[21] /CP   |  0.588 |   2.155 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   315 |     u0/\w_reg[0][1] /D v | MET Setup Check with Pin
u0/\w_reg[0][1] /CP     |  0.592 |   2.186 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   316 |    u0/\w_reg[0][11] /D v | MET Setup Check with Pin
u0/\w_reg[0][11] /CP    |  0.593 |   2.188 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   317 |   \text_out_reg[98] /D v | MET Setup Check with Pin
\text_out_reg[98] /CP   |  0.593 |   2.180 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   318 |  \text_out_reg[110] /D v | MET Setup Check with Pin
\text_out_reg[110] /CP  |  0.593 |   2.164 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   319 |   \text_out_reg[62] /D ^ | MET Setup Check with Pin
\text_out_reg[62] /CP   |  0.595 |   2.135 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |   320 |   \text_out_reg[61] /D ^ | MET Setup Check with Pin
\text_out_reg[61] /CP   |  0.596 |   2.134 |    2.729 | clk(D)(P) | clk(C)(P)
* |
     |   321 |   \text_out_reg[53] /D ^ | MET Setup Check with Pin
\text_out_reg[53] /CP   |  0.596 |   2.134 |    2.730 | clk(D)(P) | clk(C)(P)
* |
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```
     |   322 |     u0/\w_reg[0][3] /D v | MET Setup Check with Pin
u0/\w_reg[0][3] /CP     |  0.597 |   2.181 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   323 |   \text_out_reg[28] /D v | MET Setup Check with Pin
\text_out_reg[28] /CP   |  0.598 |   2.111 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   324 |   \text_out_reg[71] /D v | MET Setup Check with Pin
\text_out_reg[71] /CP   |  0.601 |   2.184 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   325 |    u0/\w_reg[0][22] /D v | MET Setup Check with Pin
u0/\w_reg[0][22] /CP    |  0.604 |   2.173 |    2.777 | clk(D)(P) | clk(C)(P)
* |
     |   326 |    \text_out_reg[6] /D v | MET Setup Check with Pin
\text_out_reg[6] /CP    |  0.605 |   2.094 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   327 |   \text_out_reg[76] /D v | MET Setup Check with Pin
\text_out_reg[76] /CP   |  0.608 |   2.114 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   328 |   \text_out_reg[20] /D v | MET Setup Check with Pin
\text_out_reg[20] /CP   |  0.609 |   2.128 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   329 |   \text_out_reg[74] /D v | MET Setup Check with Pin
\text_out_reg[74] /CP   |  0.609 |   2.119 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   330 |   \text_out_reg[50] /D v | MET Setup Check with Pin
\text_out_reg[50] /CP   |  0.610 |   2.131 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   331 |   \text_out_reg[31] /D v | MET Setup Check with Pin
\text_out_reg[31] /CP   |  0.610 |   2.096 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   332 |   \text_out_reg[38] /D v | MET Setup Check with Pin
\text_out_reg[38] /CP   |  0.612 |   2.132 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   333 |   \text_out_reg[68] /D ^ | MET Setup Check with Pin
\text_out_reg[68] /CP   |  0.612 |   2.155 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   334 |   \text_out_reg[63] /D v | MET Setup Check with Pin
\text_out_reg[63] /CP   |  0.612 |   2.132 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   335 |    \text_out_reg[4] /D v | MET Setup Check with Pin
\text_out_reg[4] /CP    |  0.614 |   2.077 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   336 |    \text_out_reg[3] /D v | MET Setup Check with Pin
\text_out_reg[3] /CP    |  0.614 |   2.087 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   337 |   \text_out_reg[60] /D v | MET Setup Check with Pin
\text_out_reg[60] /CP   |  0.615 |   2.131 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   338 |   \text_out_reg[10] /D v | MET Setup Check with Pin
\text_out_reg[10] /CP   |  0.618 |   2.121 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   339 |  \text_out_reg[113] /D v | MET Setup Check with Pin
\text_out_reg[113] /CP  |  0.618 |   2.151 |    2.769 | clk(D)(P) | clk(C)(P)
* |
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     |   340 |   \text_out_reg[67] /D v | MET Setup Check with Pin
\text_out_reg[67] /CP   |  0.620 |   2.165 |    2.784 | clk(D)(P) | clk(C)(P)
* |
     |   341 |  \text_out_reg[116] /D ^ | MET Setup Check with Pin
\text_out_reg[116] /CP  |  0.621 |   2.116 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   342 |   \text_out_reg[75] /D v | MET Setup Check with Pin
\text_out_reg[75] /CP   |  0.624 |   2.102 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   343 |    u0/\w_reg[0][16] /D v | MET Setup Check with Pin
u0/\w_reg[0][16] /CP    |  0.626 |   2.155 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   344 |   \text_out_reg[11] /D v | MET Setup Check with Pin
\text_out_reg[11] /CP   |  0.626 |   2.111 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   345 |   \text_out_reg[86] /D ^ | MET Setup Check with Pin
\text_out_reg[86] /CP   |  0.628 |   2.132 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   346 |   \text_out_reg[78] /D v | MET Setup Check with Pin
\text_out_reg[78] /CP   |  0.633 |   2.152 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   347 |   \text_out_reg[45] /D v | MET Setup Check with Pin
\text_out_reg[45] /CP   |  0.636 |   2.109 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   348 |  \text_out_reg[105] /D v | MET Setup Check with Pin
\text_out_reg[105] /CP  |  0.636 |   2.130 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   349 |    \text_out_reg[1] /D v | MET Setup Check with Pin
\text_out_reg[1] /CP    |  0.640 |   2.069 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   350 |     u0/\w_reg[0][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[0][0] /CP     |  0.641 |   2.119 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   351 |   \text_out_reg[99] /D v | MET Setup Check with Pin
\text_out_reg[99] /CP   |  0.641 |   2.132 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   352 |     u0/\w_reg[0][4] /D v | MET Setup Check with Pin
u0/\w_reg[0][4] /CP     |  0.641 |   2.137 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   353 |   \text_out_reg[51] /D v | MET Setup Check with Pin
\text_out_reg[51] /CP   |  0.645 |   2.098 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   354 |   \text_out_reg[40] /D v | MET Setup Check with Pin
\text_out_reg[40] /CP   |  0.645 |   2.102 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   355 |  \text_out_reg[114] /D v | MET Setup Check with Pin
\text_out_reg[114] /CP  |  0.648 |   2.117 |    2.765 | clk(D)(P) | clk(C)(P)
* |
     |   356 |    u0/\w_reg[0][20] /D v | MET Setup Check with Pin
u0/\w_reg[0][20] /CP    |  0.651 |   2.129 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   357 |   \text_out_reg[18] /D v | MET Setup Check with Pin
\text_out_reg[18] /CP   |  0.651 |   2.061 |    2.713 | clk(D)(P) | clk(C)(P)
* |
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     |   358 |   \text_out_reg[42] /D v | MET Setup Check with Pin
\text_out_reg[42] /CP   |  0.653 |   2.095 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   359 |    u0/\w_reg[0][17] /D v | MET Setup Check with Pin
u0/\w_reg[0][17] /CP    |  0.653 |   2.127 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   360 |   \text_out_reg[59] /D v | MET Setup Check with Pin
\text_out_reg[59] /CP   |  0.654 |   2.088 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   361 |   \text_out_reg[91] /D ^ | MET Setup Check with Pin
\text_out_reg[91] /CP   |  0.655 |   2.092 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   362 |   \text_out_reg[35] /D v | MET Setup Check with Pin
\text_out_reg[35] /CP   |  0.665 |   2.072 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   363 |   \text_out_reg[47] /D v | MET Setup Check with Pin
\text_out_reg[47] /CP   |  0.666 |   2.078 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   364 |   \text_out_reg[36] /D v | MET Setup Check with Pin
\text_out_reg[36] /CP   |  0.669 |   2.068 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   365 |    u0/\w_reg[0][19] /D v | MET Setup Check with Pin
u0/\w_reg[0][19] /CP    |  0.670 |   2.111 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   366 |   \text_out_reg[80] /D v | MET Setup Check with Pin
\text_out_reg[80] /CP   |  0.670 |   2.091 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   367 |   \text_out_reg[22] /D v | MET Setup Check with Pin
\text_out_reg[22] /CP   |  0.675 |   2.067 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   368 |  \text_out_reg[112] /D v | MET Setup Check with Pin
\text_out_reg[112] /CP  |  0.679 |   2.089 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   369 |   \text_out_reg[27] /D v | MET Setup Check with Pin
\text_out_reg[27] /CP   |  0.679 |   2.032 |    2.711 | clk(D)(P) | clk(C)(P)
* |
     |   370 |  \text_out_reg[111] /D v | MET Setup Check with Pin
\text_out_reg[111] /CP  |  0.680 |   2.080 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   371 |   \text_out_reg[55] /D ^ | MET Setup Check with Pin
\text_out_reg[55] /CP   |  0.680 |   2.053 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   372 |   \text_out_reg[19] /D v | MET Setup Check with Pin
\text_out_reg[19] /CP   |  0.702 |   2.029 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   373 |   \text_out_reg[41] /D ^ | MET Setup Check with Pin
\text_out_reg[41] /CP   |  0.708 |   2.020 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   374 |   \text_out_reg[16] /D v | MET Setup Check with Pin
\text_out_reg[16] /CP   |  0.709 |   2.029 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   375 |   \text_out_reg[58] /D v | MET Setup Check with Pin
\text_out_reg[58] /CP   |  0.717 |   2.035 |    2.752 | clk(D)(P) | clk(C)(P)
* |
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     |   376 |   \text_out_reg[46] /D v | MET Setup Check with Pin
\text_out_reg[46] /CP   |  0.729 |   2.016 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   377 |   \text_out_reg[83] /D v | MET Setup Check with Pin
\text_out_reg[83] /CP   |  0.729 |   2.050 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   378 |  \text_out_reg[106] /D v | MET Setup Check with Pin
\text_out_reg[106] /CP  |  0.730 |   2.033 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   379 |  \text_out_reg[115] /D v | MET Setup Check with Pin
\text_out_reg[115] /CP  |  0.735 |   2.033 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   380 |  \text_out_reg[108] /D v | MET Setup Check with Pin
\text_out_reg[108] /CP  |  0.738 |   2.025 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   381 |  \text_out_reg[104] /D v | MET Setup Check with Pin
\text_out_reg[104] /CP  |  0.741 |   2.020 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   382 |   \text_out_reg[44] /D v | MET Setup Check with Pin
\text_out_reg[44] /CP   |  0.765 |   1.978 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   383 |   \text_out_reg[43] /D v | MET Setup Check with Pin
\text_out_reg[43] /CP   |  0.789 |   1.958 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   384 |  \text_out_reg[107] /D v | MET Setup Check with Pin
\text_out_reg[107] /CP  |  0.835 |   1.930 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   385 |  u0/r0/\out_reg[31] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[31] /CP  |  0.927 |   1.797 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   386 |  u0/r0/\out_reg[30] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[30] /CP  |  0.950 |   1.792 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   387 |  u0/r0/\out_reg[27] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[27] /CP  |  0.952 |   1.792 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   388 |  u0/r0/\out_reg[28] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[28] /CP  |  0.957 |   1.793 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   389 |  u0/r0/\out_reg[26] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[26] /CP  |  0.958 |   1.795 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   390 |  u0/r0/\out_reg[25] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[25] /CP  |  0.968 |   1.775 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   391 |  u0/r0/\rcnt_reg[3] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[3] /CP  |  0.971 |   1.780 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   392 |  u0/r0/\out_reg[29] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[29] /CP  |  0.981 |   1.758 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   393 |  u0/r0/\rcnt_reg[1] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[1] /CP  |  1.057 |   1.673 |    2.731 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   394 |  u0/r0/\rcnt_reg[2] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[2] /CP  |  1.061 |   1.671 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   395 |  u0/r0/\out_reg[24] /D v | MET Setup Check with Pin
u0/r0/\out_reg[24] /CP  |  1.066 |   1.709 |    2.775 | clk(D)(P) | clk(C)(P)
* |
     |   396 |  u0/r0/\rcnt_reg[0] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[0] /CP  |  1.069 |   1.664 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |   397 |           text_out[74] ^ | MET Late External Delay Assertion
|  1.415 |   0.685 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   398 |        \dcnt_reg[1] /D v | MET Setup Check with Pin
\dcnt_reg[1] /CP        |  1.435 |   1.307 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   399 |           text_out[73] ^ | MET Late External Delay Assertion
|  1.457 |   0.643 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   400 |              done_reg/D ^ | MET Setup Check with Pin
done_reg/CP             |  1.467 |   1.250 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   401 |           text_out[81] ^ | MET Late External Delay Assertion
|  1.472 |   0.628 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   402 |           text_out[72] ^ | MET Late External Delay Assertion
|  1.489 |   0.611 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   403 |        \dcnt_reg[3] /D v | MET Setup Check with Pin
\dcnt_reg[3] /CP        |  1.491 |   1.255 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   404 |          text_out[109] ^ | MET Late External Delay Assertion
|  1.494 |   0.606 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   405 |           text_out[84] ^ | MET Late External Delay Assertion
|  1.518 |   0.582 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   406 |  \text_in_r_reg[52] /E v | MET Setup Check with Pin
\text_in_r_reg[52] /CP  |  1.522 |   1.091 |    2.613 | clk(D)(P) | clk(C)(P)
* |
     |   407 |          text_out[106] ^ | MET Late External Delay Assertion
|  1.524 |   0.576 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   408 |           text_out[65] ^ | MET Late External Delay Assertion
|  1.524 |   0.576 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   409 |           text_out[71] ^ | MET Late External Delay Assertion
|  1.525 |   0.575 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   410 |  \text_in_r_reg[54] /E v | MET Setup Check with Pin
\text_in_r_reg[54] /CP  |  1.530 |   1.091 |    2.621 | clk(D)(P) | clk(C)(P)
* |
     |   411 |  \text_in_r_reg[55] /E v | MET Setup Check with Pin
\text_in_r_reg[55] /CP  |  1.530 |   1.091 |    2.621 | clk(D)(P) | clk(C)(P)
* |
     |   412 |           text_out[93] ^ | MET Late External Delay Assertion
|  1.530 |   0.570 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   413 |          text_out[112] ^ | MET Late External Delay Assertion
|  1.530 |   0.569 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   414 |  \text_in_r_reg[53] /E v | MET Setup Check with Pin
\text_in_r_reg[53] /CP  |  1.534 |   1.093 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   415 |           text_out[70] ^ | MET Late External Delay Assertion
|  1.536 |   0.564 |    2.100 | clk(D)(P) | clk(C)(P) * |
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```
     |   416 |           text_out[80] ^ | MET Late External Delay Assertion
|  1.536 |   0.564 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   417 |  \text_in_r_reg[59] /E v | MET Setup Check with Pin
\text_in_r_reg[59] /CP  |  1.536 |   1.095 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   418 |  \text_in_r_reg[60] /E v | MET Setup Check with Pin
\text_in_r_reg[60] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   419 |  \text_in_r_reg[62] /E v | MET Setup Check with Pin
\text_in_r_reg[62] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   420 |  \text_in_r_reg[61] /E v | MET Setup Check with Pin
\text_in_r_reg[61] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   421 |  \text_in_r_reg[63] /E v | MET Setup Check with Pin
\text_in_r_reg[63] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   422 |  \text_in_r_reg[56] /E v | MET Setup Check with Pin
\text_in_r_reg[56] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   423 |  \text_in_r_reg[57] /E v | MET Setup Check with Pin
\text_in_r_reg[57] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   424 |  \text_in_r_reg[58] /E v | MET Setup Check with Pin
\text_in_r_reg[58] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   425 |           text_out[68] ^ | MET Late External Delay Assertion
|  1.538 |   0.562 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   426 |        \dcnt_reg[0] /D v | MET Setup Check with Pin
\dcnt_reg[0] /CP        |  1.540 |   1.200 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   427 |           text_out[89] ^ | MET Late External Delay Assertion
|  1.544 |   0.556 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   428 |  \text_in_r_reg[97] /E v | MET Setup Check with Pin
\text_in_r_reg[97] /CP  |  1.545 |   1.083 |    2.628 | clk(D)(P) | clk(C)(P)
* |
     |   429 |  \text_in_r_reg[67] /E v | MET Setup Check with Pin
\text_in_r_reg[67] /CP  |  1.545 |   1.083 |    2.628 | clk(D)(P) | clk(C)(P)
* |
     |   430 |           text_out[64] ^ | MET Late External Delay Assertion
|  1.547 |   0.553 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   431 |           text_out[85] ^ | MET Late External Delay Assertion
|  1.548 |   0.552 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   432 |  \text_in_r_reg[70] /E v | MET Setup Check with Pin
\text_in_r_reg[70] /CP  |  1.553 |   1.085 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   433 |  \text_in_r_reg[69] /E v | MET Setup Check with Pin
\text_in_r_reg[69] /CP  |  1.553 |   1.084 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   434 |  \text_in_r_reg[79] /E v | MET Setup Check with Pin
\text_in_r_reg[79] /CP  |  1.554 |   1.066 |    2.620 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   435 |  \text_in_r_reg[76] /E v | MET Setup Check with Pin
\text_in_r_reg[76] /CP  |  1.554 |   1.066 |    2.620 | clk(D)(P) | clk(C)(P)
* |
     |   436 |  \text_in_r_reg[68] /E v | MET Setup Check with Pin
\text_in_r_reg[68] /CP  |  1.556 |   1.082 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   437 |           text_out[92] ^ | MET Late External Delay Assertion
|  1.556 |   0.544 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   438 |  \text_in_r_reg[72] /E v | MET Setup Check with Pin
\text_in_r_reg[72] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   439 |  \text_in_r_reg[78] /E v | MET Setup Check with Pin
\text_in_r_reg[78] /CP  |  1.557 |   1.066 |    2.623 | clk(D)(P) | clk(C)(P)
* |
     |   440 |  \text_in_r_reg[65] /E v | MET Setup Check with Pin
\text_in_r_reg[65] /CP  |  1.557 |   1.081 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   441 |  \text_in_r_reg[74] /E v | MET Setup Check with Pin
\text_in_r_reg[74] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   442 |  \text_in_r_reg[82] /E v | MET Setup Check with Pin
\text_in_r_reg[82] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   443 |  \text_in_r_reg[75] /E v | MET Setup Check with Pin
\text_in_r_reg[75] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   444 |  \text_in_r_reg[77] /E v | MET Setup Check with Pin
\text_in_r_reg[77] /CP  |  1.557 |   1.066 |    2.623 | clk(D)(P) | clk(C)(P)
* |
     |   445 |  \text_in_r_reg[64] /E v | MET Setup Check with Pin
\text_in_r_reg[64] /CP  |  1.559 |   1.079 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   446 | \text_in_r_reg[109] /E v | MET Setup Check with Pin
\text_in_r_reg[109] /CP |  1.559 |   1.079 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   447 |  \text_in_r_reg[66] /E v | MET Setup Check with Pin
\text_in_r_reg[66] /CP  |  1.559 |   1.081 |    2.640 | clk(D)(P) | clk(C)(P)
* |
     |   448 |          text_out[107] ^ | MET Late External Delay Assertion
|  1.559 |   0.540 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   449 |          text_out[115] ^ | MET Late External Delay Assertion
|  1.560 |   0.540 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   450 | \text_in_r_reg[107] /E v | MET Setup Check with Pin
\text_in_r_reg[107] /CP |  1.560 |   1.079 |    2.639 | clk(D)(P) | clk(C)(P)
* |
     |   451 | \text_in_r_reg[110] /E v | MET Setup Check with Pin
\text_in_r_reg[110] /CP |  1.561 |   1.079 |    2.640 | clk(D)(P) | clk(C)(P)
* |
     |   452 | \text_in_r_reg[115] /E v | MET Setup Check with Pin
\text_in_r_reg[115] /CP |  1.561 |   1.074 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   453 |  \text_in_r_reg[30] /E v | MET Setup Check with Pin
\text_in_r_reg[30] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   454 | \text_in_r_reg[105] /E v | MET Setup Check with Pin
\text_in_r_reg[105] /CP |  1.562 |   1.079 |    2.641 | clk(D)(P) | clk(C)(P)
* |
     |   455 | \text_in_r_reg[111] /E v | MET Setup Check with Pin
\text_in_r_reg[111] /CP |  1.562 |   1.081 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   456 |  \text_in_r_reg[24] /E v | MET Setup Check with Pin
\text_in_r_reg[24] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   457 |  \text_in_r_reg[26] /E v | MET Setup Check with Pin
\text_in_r_reg[26] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   458 |  \text_in_r_reg[28] /E v | MET Setup Check with Pin
\text_in_r_reg[28] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   459 |  \text_in_r_reg[27] /E v | MET Setup Check with Pin
\text_in_r_reg[27] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   460 |  \text_in_r_reg[31] /E v | MET Setup Check with Pin
\text_in_r_reg[31] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   461 |  \text_in_r_reg[29] /E v | MET Setup Check with Pin
\text_in_r_reg[29] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   462 | \text_in_r_reg[104] /E v | MET Setup Check with Pin
\text_in_r_reg[104] /CP |  1.563 |   1.079 |    2.642 | clk(D)(P) | clk(C)(P)
* |
     |   463 | \text_in_r_reg[108] /E v | MET Setup Check with Pin
\text_in_r_reg[108] /CP |  1.563 |   1.079 |    2.642 | clk(D)(P) | clk(C)(P)
* |
     |   464 |  \text_in_r_reg[23] /E v | MET Setup Check with Pin
\text_in_r_reg[23] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   465 |  \text_in_r_reg[18] /E v | MET Setup Check with Pin
\text_in_r_reg[18] /CP  |  1.563 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   466 |  \text_in_r_reg[19] /E v | MET Setup Check with Pin
\text_in_r_reg[19] /CP  |  1.564 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   467 |  \text_in_r_reg[25] /E v | MET Setup Check with Pin
\text_in_r_reg[25] /CP  |  1.564 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   468 | \text_in_r_reg[106] /E v | MET Setup Check with Pin
\text_in_r_reg[106] /CP |  1.564 |   1.079 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   469 | \text_in_r_reg[114] /E v | MET Setup Check with Pin
\text_in_r_reg[114] /CP |  1.564 |   1.074 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   470 |           text_out[69] ^ | MET Late External Delay Assertion
|  1.565 |   0.535 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   471 | \text_in_r_reg[113] /E v | MET Setup Check with Pin
\text_in_r_reg[113] /CP |  1.565 |   1.073 |    2.638 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   472 |  \text_in_r_reg[20] /E v | MET Setup Check with Pin
\text_in_r_reg[20] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   473 |  \text_in_r_reg[21] /E v | MET Setup Check with Pin
\text_in_r_reg[21] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   474 |  \text_in_r_reg[22] /E v | MET Setup Check with Pin
\text_in_r_reg[22] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   475 |  \text_in_r_reg[16] /E v | MET Setup Check with Pin
\text_in_r_reg[16] /CP  |  1.567 |   1.052 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   476 |  \text_in_r_reg[17] /E v | MET Setup Check with Pin
\text_in_r_reg[17] /CP  |  1.567 |   1.052 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   477 | \text_in_r_reg[102] /E v | MET Setup Check with Pin
\text_in_r_reg[102] /CP |  1.567 |   1.085 |    2.652 | clk(D)(P) | clk(C)(P)
* |
     |   478 | \text_in_r_reg[103] /E v | MET Setup Check with Pin
\text_in_r_reg[103] /CP |  1.567 |   1.085 |    2.652 | clk(D)(P) | clk(C)(P)
* |
     |   479 | \text_in_r_reg[100] /E v | MET Setup Check with Pin
\text_in_r_reg[100] /CP |  1.567 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   480 | \text_in_r_reg[101] /E v | MET Setup Check with Pin
\text_in_r_reg[101] /CP |  1.567 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   481 | \text_in_r_reg[123] /E v | MET Setup Check with Pin
\text_in_r_reg[123] /CP |  1.567 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   482 | \text_in_r_reg[122] /E v | MET Setup Check with Pin
\text_in_r_reg[122] /CP |  1.567 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   483 |        \dcnt_reg[2] /D ^ | MET Setup Check with Pin
\dcnt_reg[2] /CP        |  1.567 |   1.152 |    2.720 | clk(D)(P) | clk(C)(P)
* |
     |   484 |  \text_in_r_reg[98] /E v | MET Setup Check with Pin
\text_in_r_reg[98] /CP  |  1.568 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   485 | \text_in_r_reg[127] /E v | MET Setup Check with Pin
\text_in_r_reg[127] /CP |  1.568 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   486 | \text_in_r_reg[121] /E v | MET Setup Check with Pin
\text_in_r_reg[121] /CP |  1.568 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   487 |  \text_in_r_reg[96] /E v | MET Setup Check with Pin
\text_in_r_reg[96] /CP  |  1.568 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   488 |  \text_in_r_reg[99] /E v | MET Setup Check with Pin
\text_in_r_reg[99] /CP  |  1.568 |   1.086 |    2.654 | clk(D)(P) | clk(C)(P)
* |
     |   489 |           text_out[78] ^ | MET Late External Delay Assertion
|  1.569 |   0.531 |    2.100 | clk(D)(P) | clk(C)(P) * |
```

```
     |   490 |  \text_in_r_reg[51] /E v | MET Setup Check with Pin
\text_in_r_reg[51] /CP  |  1.569 |   1.058 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   491 |  \text_in_r_reg[49] /E v | MET Setup Check with Pin
\text_in_r_reg[49] /CP  |  1.570 |   1.058 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   492 | \text_in_r_reg[126] /E v | MET Setup Check with Pin
\text_in_r_reg[126] /CP |  1.571 |   1.079 |    2.650 | clk(D)(P) | clk(C)(P)
* |
     |   493 |  \text_in_r_reg[45] /E v | MET Setup Check with Pin
\text_in_r_reg[45] /CP  |  1.571 |   1.058 |    2.629 | clk(D)(P) | clk(C)(P)
* |
     |   494 | \text_in_r_reg[120] /E v | MET Setup Check with Pin
\text_in_r_reg[120] /CP |  1.572 |   1.079 |    2.651 | clk(D)(P) | clk(C)(P)
* |
     |   495 |  \text_in_r_reg[95] /E v | MET Setup Check with Pin
\text_in_r_reg[95] /CP  |  1.572 |   1.083 |    2.655 | clk(D)(P) | clk(C)(P)
* |
     |   496 | \text_in_r_reg[116] /E v | MET Setup Check with Pin
\text_in_r_reg[116] /CP |  1.572 |   1.075 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   497 | \text_in_r_reg[124] /E v | MET Setup Check with Pin
\text_in_r_reg[124] /CP |  1.572 |   1.079 |    2.651 | clk(D)(P) | clk(C)(P)
* |
     |   498 | \text_in_r_reg[112] /E v | MET Setup Check with Pin
\text_in_r_reg[112] /CP |  1.572 |   1.074 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   499 |  \text_in_r_reg[94] /E v | MET Setup Check with Pin
\text_in_r_reg[94] /CP  |  1.573 |   1.083 |    2.656 | clk(D)(P) | clk(C)(P)
* |
     |   500 |  \text_in_r_reg[93] /E v | MET Setup Check with Pin
\text_in_r_reg[93] /CP  |  1.574 |   1.083 |    2.657 | clk(D)(P) | clk(C)(P)
* |
     |   501 |  \text_in_r_reg[44] /E v | MET Setup Check with Pin
\text_in_r_reg[44] /CP  |  1.575 |   1.058 |    2.633 | clk(D)(P) | clk(C)(P)
* |
     |   502 |  \text_in_r_reg[92] /E v | MET Setup Check with Pin
\text_in_r_reg[92] /CP  |  1.576 |   1.082 |    2.658 | clk(D)(P) | clk(C)(P)
* |
     |   503 |  \text_in_r_reg[43] /E v | MET Setup Check with Pin
\text_in_r_reg[43] /CP  |  1.576 |   1.058 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   504 |          text_out[123] ^ | MET Late External Delay Assertion
|  1.576 |   0.524 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   505 |  \text_in_r_reg[47] /E v | MET Setup Check with Pin
\text_in_r_reg[47] /CP  |  1.577 |   1.058 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   506 |  \text_in_r_reg[91] /E v | MET Setup Check with Pin
\text_in_r_reg[91] /CP  |  1.577 |   1.082 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   507 | \text_in_r_reg[125] /E v | MET Setup Check with Pin
\text_in_r_reg[125] /CP |  1.577 |   1.078 |    2.655 | clk(D)(P) | clk(C)(P)
* |
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     |   508 |  \text_in_r_reg[46] /E v | MET Setup Check with Pin
\text_in_r_reg[46] /CP  |  1.577 |   1.058 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   509 |  \text_in_r_reg[48] /E v | MET Setup Check with Pin
\text_in_r_reg[48] /CP  |  1.577 |   1.057 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   510 | \text_in_r_reg[119] /E v | MET Setup Check with Pin
\text_in_r_reg[119] /CP |  1.578 |   1.078 |    2.656 | clk(D)(P) | clk(C)(P)
* |
     |   511 |           text_out[86] ^ | MET Late External Delay Assertion
|  1.579 |   0.521 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   512 |  \text_in_r_reg[71] /E v | MET Setup Check with Pin
\text_in_r_reg[71] /CP  |  1.580 |   1.068 |    2.648 | clk(D)(P) | clk(C)(P)
* |
     |   513 |  \text_in_r_reg[80] /E v | MET Setup Check with Pin
\text_in_r_reg[80] /CP  |  1.580 |   1.068 |    2.648 | clk(D)(P) | clk(C)(P)
* |
     |   514 |  \text_in_r_reg[15] /E v | MET Setup Check with Pin
\text_in_r_reg[15] /CP  |  1.580 |   1.054 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   515 |  \text_in_r_reg[12] /E v | MET Setup Check with Pin
\text_in_r_reg[12] /CP  |  1.580 |   1.054 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   516 |           text_out[36] ^ | MET Late External Delay Assertion
|  1.580 |   0.520 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   517 |           text_out[95] v | MET Late External Delay Assertion
|  1.582 |   0.518 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   518 | \text_in_r_reg[118] /E v | MET Setup Check with Pin
\text_in_r_reg[118] /CP |  1.582 |   1.077 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   519 |          text_out[120] ^ | MET Late External Delay Assertion
|  1.583 |   0.517 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   520 | \text_in_r_reg[117] /E v | MET Setup Check with Pin
\text_in_r_reg[117] /CP |  1.583 |   1.077 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   521 |          text_out[110] ^ | MET Late External Delay Assertion
|  1.583 |   0.517 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   522 |  \text_in_r_reg[36] /E v | MET Setup Check with Pin
\text_in_r_reg[36] /CP  |  1.584 |   1.059 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   523 |  \text_in_r_reg[13] /E v | MET Setup Check with Pin
\text_in_r_reg[13] /CP  |  1.584 |   1.051 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   524 |  \text_in_r_reg[14] /E v | MET Setup Check with Pin
\text_in_r_reg[14] /CP  |  1.584 |   1.051 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   525 |  \text_in_r_reg[39] /E v | MET Setup Check with Pin
\text_in_r_reg[39] /CP  |  1.584 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   526 |  \text_in_r_reg[32] /E v | MET Setup Check with Pin
\text_in_r_reg[32] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
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     |   527 |  \text_in_r_reg[37] /E v | MET Setup Check with Pin
\text_in_r_reg[37] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   528 |  \text_in_r_reg[33] /E v | MET Setup Check with Pin
\text_in_r_reg[33] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   529 |  \text_in_r_reg[41] /E v | MET Setup Check with Pin
\text_in_r_reg[41] /CP  |  1.584 |   1.059 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   530 |  \text_in_r_reg[34] /E v | MET Setup Check with Pin
\text_in_r_reg[34] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   531 |  \text_in_r_reg[38] /E v | MET Setup Check with Pin
\text_in_r_reg[38] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   532 |  \text_in_r_reg[35] /E v | MET Setup Check with Pin
\text_in_r_reg[35] /CP  |  1.584 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   533 |  \text_in_r_reg[40] /E v | MET Setup Check with Pin
\text_in_r_reg[40] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   534 |  \text_in_r_reg[42] /E v | MET Setup Check with Pin
\text_in_r_reg[42] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   535 |  \text_in_r_reg[50] /E v | MET Setup Check with Pin
\text_in_r_reg[50] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   536 |          text_out[105] ^ | MET Late External Delay Assertion
|  1.585 |   0.515 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   537 |          text_out[122] ^ | MET Late External Delay Assertion
|  1.585 |   0.515 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   538 |          text_out[113] ^ | MET Late External Delay Assertion
|  1.586 |   0.514 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   539 |          text_out[114] ^ | MET Late External Delay Assertion
|  1.587 |   0.513 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   540 |  \text_in_r_reg[73] /E v | MET Setup Check with Pin
\text_in_r_reg[73] /CP  |  1.587 |   1.063 |    2.650 | clk(D)(P) | clk(C)(P)
* |
     |   541 |          text_out[104] ^ | MET Late External Delay Assertion
|  1.591 |   0.508 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   542 |           text_out[88] v | MET Late External Delay Assertion
|  1.592 |   0.508 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   543 |           text_out[67] v | MET Late External Delay Assertion
|  1.593 |   0.507 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   544 |           text_out[83] v | MET Late External Delay Assertion
|  1.593 |   0.507 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   545 |           text_out[53] ^ | MET Late External Delay Assertion
|  1.594 |   0.506 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   546 |           text_out[54] ^ | MET Late External Delay Assertion
|  1.595 |   0.505 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   547 |          text_out[111] v | MET Late External Delay Assertion
|  1.595 |   0.505 |    2.100 | clk(D)(P) | clk(C)(P) * |
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     |   548 |  \text_in_r_reg[85] /E v | MET Setup Check with Pin
\text_in_r_reg[85] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   549 |  \text_in_r_reg[86] /E v | MET Setup Check with Pin
\text_in_r_reg[86] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   550 |  \text_in_r_reg[87] /E v | MET Setup Check with Pin
\text_in_r_reg[87] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   551 |  \text_in_r_reg[84] /E v | MET Setup Check with Pin
\text_in_r_reg[84] /CP  |  1.598 |   1.068 |    2.665 | clk(D)(P) | clk(C)(P)
* |
     |   552 |  \text_in_r_reg[83] /E v | MET Setup Check with Pin
\text_in_r_reg[83] /CP  |  1.599 |   1.067 |    2.666 | clk(D)(P) | clk(C)(P)
* |
     |   553 |          text_out[108] v | MET Late External Delay Assertion
|  1.600 |   0.500 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   554 |  \text_in_r_reg[90] /E v | MET Setup Check with Pin
\text_in_r_reg[90] /CP  |  1.600 |   1.067 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   555 |  \text_in_r_reg[88] /E v | MET Setup Check with Pin
\text_in_r_reg[88] /CP  |  1.600 |   1.067 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   556 |  \text_in_r_reg[81] /E v | MET Setup Check with Pin
\text_in_r_reg[81] /CP  |  1.601 |   1.066 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   557 |  \text_in_r_reg[89] /E v | MET Setup Check with Pin
\text_in_r_reg[89] /CP  |  1.601 |   1.066 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   558 |          text_out[119] v | MET Late External Delay Assertion
|  1.603 |   0.497 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   559 |                   done ^ | MET Late External Delay Assertion
|  1.603 |   0.497 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   560 |          text_out[127] v | MET Late External Delay Assertion
|  1.605 |   0.495 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   561 |           text_out[44] ^ | MET Late External Delay Assertion
|  1.606 |   0.494 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   562 |          text_out[116] v | MET Late External Delay Assertion
|  1.606 |   0.494 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   563 |           text_out[66] v | MET Late External Delay Assertion
|  1.607 |   0.493 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   564 |           text_out[34] ^ | MET Late External Delay Assertion
|  1.608 |   0.492 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   565 |           text_out[94] v | MET Late External Delay Assertion
|  1.608 |   0.492 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   566 |          text_out[121] v | MET Late External Delay Assertion
|  1.610 |   0.490 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   567 |           text_out[35] ^ | MET Late External Delay Assertion
|  1.611 |   0.489 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   568 |          text_out[125] v | MET Late External Delay Assertion
|  1.611 |   0.489 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   569 |           text_out[43] ^ | MET Late External Delay Assertion
|  1.615 |   0.485 |    2.100 | clk(D)(P) | clk(C)(P) * |
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     |   570 |          text_out[126] v | MET Late External Delay Assertion
|  1.616 |   0.484 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   571 |          text_out[124] v | MET Late External Delay Assertion
|  1.619 |   0.481 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   572 |           text_out[75] ^ | MET Late External Delay Assertion
|  1.626 |   0.474 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   573 |          text_out[100] v | MET Late External Delay Assertion
|  1.628 |   0.472 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   574 |           text_out[98] v | MET Late External Delay Assertion
|  1.629 |   0.470 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   575 |           text_out[47] v | MET Late External Delay Assertion
|  1.631 |   0.469 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   576 |           text_out[82] v | MET Late External Delay Assertion
|  1.632 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   577 |           text_out[21] v | MET Late External Delay Assertion
|  1.633 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   578 |           text_out[99] v | MET Late External Delay Assertion
|  1.633 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   579 |           text_out[77] ^ | MET Late External Delay Assertion
|  1.634 |   0.466 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   580 |           text_out[46] v | MET Late External Delay Assertion
|  1.635 |   0.465 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   581 |           text_out[39] v | MET Late External Delay Assertion
|  1.635 |   0.465 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   582 |          text_out[118] v | MET Late External Delay Assertion
|  1.636 |   0.464 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   583 |           text_out[20] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   584 |          text_out[102] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   585 |           text_out[76] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   586 |           text_out[37] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   587 |          text_out[101] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   588 |           text_out[96] v | MET Late External Delay Assertion
|  1.638 |   0.462 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   589 |           text_out[87] v | MET Late External Delay Assertion
|  1.638 |   0.462 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   590 |           text_out[90] v | MET Late External Delay Assertion
|  1.639 |   0.461 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   591 |           text_out[91] v | MET Late External Delay Assertion
|  1.639 |   0.461 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   592 |           text_out[79] v | MET Late External Delay Assertion
|  1.640 |   0.460 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   593 |          text_out[103] v | MET Late External Delay Assertion
|  1.642 |   0.458 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   594 |           text_out[45] v | MET Late External Delay Assertion
|  1.643 |   0.457 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   595 |          text_out[117] v | MET Late External Delay Assertion
|  1.643 |   0.457 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   596 |           text_out[97] v | MET Late External Delay Assertion
|  1.643 |   0.457 |    2.100 | clk(D)(P) | clk(C)(P) * |
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| 597 | text_out[22] v | MET Late External Delay Assertion
| 1.645 | 0.455 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 598 | text_out[42] v | MET Late External Delay Assertion
| 1.658 | 0.442 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 599 | text_out[40] v | MET Late External Delay Assertion
| 1.662 | 0.438 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 600 | text_out[48] v | MET Late External Delay Assertion
| 1.663 | 0.437 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 601 | text_out[41] v | MET Late External Delay Assertion
| 1.663 | 0.436 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 602 | text_out[57] v | MET Late External Delay Assertion
| 1.664 | 0.436 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 603 | text_out[49] v | MET Late External Delay Assertion
| 1.664 | 0.436 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 604 | text_out[52] v | MET Late External Delay Assertion
| 1.664 | 0.436 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 605 | text_out[63] v | MET Late External Delay Assertion
| 1.665 | 0.435 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 606 | text_out[12] v | MET Late External Delay Assertion
| 1.665 | 0.435 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 607 | text_out[23] v | MET Late External Delay Assertion
| 1.666 | 0.434 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 608 | text_out[33] v | MET Late External Delay Assertion
| 1.666 | 0.434 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 609 | text_out[56] v | MET Late External Delay Assertion
| 1.668 | 0.432 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 610 | text_out[62] v | MET Late External Delay Assertion
| 1.668 | 0.432 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 611 | text_out[50] v | MET Late External Delay Assertion
| 1.669 | 0.431 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 612 | text_out[59] v | MET Late External Delay Assertion
| 1.669 | 0.431 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 613 | text_out[61] v | MET Late External Delay Assertion
| 1.669 | 0.431 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 614 | text_out[32] v | MET Late External Delay Assertion
| 1.669 | 0.431 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 615 | text_out[58] v | MET Late External Delay Assertion
| 1.670 | 0.430 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 616 | text_out[51] v | MET Late External Delay Assertion
| 1.670 | 0.430 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 617 | text_out[55] v | MET Late External Delay Assertion
| 1.670 | 0.430 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 618 | text_out[38] v | MET Late External Delay Assertion
| 1.671 | 0.429 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 619 | text_out[60] v | MET Late External Delay Assertion
| 1.671 | 0.429 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 620 | text_out[15] v | MET Late External Delay Assertion
| 1.673 | 0.427 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 621 | text_out[16] v | MET Late External Delay Assertion
| 1.675 | 0.425 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 622 | text_out[10] v | MET Late External Delay Assertion
| 1.675 | 0.425 | 2.100 | clk(D)(P) | clk(C)(P) * |
| 623 | text_out[29] v | MET Late External Delay Assertion
| 1.675 | 0.425 | 2.100 | clk(D)(P) | clk(C)(P) * |

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     |   624 |           text_out[19] v | MET Late External Delay Assertion
|  1.679 |   0.421 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   625 |           text_out[13] v | MET Late External Delay Assertion
|  1.681 |   0.419 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   626 |           text_out[17] v | MET Late External Delay Assertion
|  1.681 |   0.419 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   627 |           text_out[14] v | MET Late External Delay Assertion
|  1.682 |   0.418 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   628 |           text_out[11] v | MET Late External Delay Assertion
|  1.682 |   0.418 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   629 |            text_out[8] v | MET Late External Delay Assertion
|  1.684 |   0.416 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   630 |            text_out[9] v | MET Late External Delay Assertion
|  1.684 |   0.416 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   631 |           text_out[28] v | MET Late External Delay Assertion
|  1.687 |   0.413 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   632 |            text_out[4] v | MET Late External Delay Assertion
|  1.690 |   0.410 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   633 |            text_out[5] v | MET Late External Delay Assertion
|  1.691 |   0.409 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   634 |           text_out[18] v | MET Late External Delay Assertion
|  1.697 |   0.403 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   635 |            text_out[6] v | MET Late External Delay Assertion
|  1.699 |   0.401 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   636 |           text_out[25] v | MET Late External Delay Assertion
|  1.706 |   0.394 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   637 |           text_out[31] v | MET Late External Delay Assertion
|  1.706 |   0.394 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   638 |           text_out[24] v | MET Late External Delay Assertion
|  1.707 |   0.393 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   639 |           text_out[30] v | MET Late External Delay Assertion
|  1.707 |   0.393 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   640 |           text_out[26] v | MET Late External Delay Assertion
|  1.707 |   0.393 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   641 |           text_out[27] v | MET Late External Delay Assertion
|  1.708 |   0.392 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   642 |            text_out[0] v | MET Late External Delay Assertion
|  1.709 |   0.391 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   643 |            text_out[3] v | MET Late External Delay Assertion
|  1.709 |   0.391 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   644 |            text_out[7] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   645 |            text_out[1] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   646 |            text_out[2] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   647 |   \text_in_r_reg[4] /E v | MET Setup Check with Pin
\text_in_r_reg[4] /CP   |  1.921 |   0.757 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |   648 |   \text_in_r_reg[2] /E v | MET Setup Check with Pin
\text_in_r_reg[2] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
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     |   649 |   \text_in_r_reg[6] /E v | MET Setup Check with Pin
\text_in_r_reg[6] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   650 |   \text_in_r_reg[3] /E v | MET Setup Check with Pin
\text_in_r_reg[3] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   651 |   \text_in_r_reg[1] /E v | MET Setup Check with Pin
\text_in_r_reg[1] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   652 |   \text_in_r_reg[5] /E v | MET Setup Check with Pin
\text_in_r_reg[5] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   653 |   \text_in_r_reg[0] /E v | MET Setup Check with Pin
\text_in_r_reg[0] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   654 |  \text_in_r_reg[78] /D ^ | MET Setup Check with Pin
\text_in_r_reg[78] /CP  |  1.930 |   0.765 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   655 |  \text_in_r_reg[77] /D ^ | MET Setup Check with Pin
\text_in_r_reg[77] /CP  |  1.931 |   0.764 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   656 |  \text_in_r_reg[74] /D ^ | MET Setup Check with Pin
\text_in_r_reg[74] /CP  |  1.931 |   0.764 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   657 |  \text_in_r_reg[22] /D ^ | MET Setup Check with Pin
\text_in_r_reg[22] /CP  |  1.937 |   0.753 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   658 |  \text_in_r_reg[21] /D ^ | MET Setup Check with Pin
\text_in_r_reg[21] /CP  |  1.938 |   0.753 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   659 |  \text_in_r_reg[30] /D ^ | MET Setup Check with Pin
\text_in_r_reg[30] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   660 |  \text_in_r_reg[24] /D ^ | MET Setup Check with Pin
\text_in_r_reg[24] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   661 |  \text_in_r_reg[26] /D ^ | MET Setup Check with Pin
\text_in_r_reg[26] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   662 |   \text_in_r_reg[8] /E v | MET Setup Check with Pin
\text_in_r_reg[8] /CP   |  1.938 |   0.756 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   663 |  \text_in_r_reg[31] /D ^ | MET Setup Check with Pin
\text_in_r_reg[31] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   664 |  \text_in_r_reg[28] /D ^ | MET Setup Check with Pin
\text_in_r_reg[28] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   665 |  \text_in_r_reg[20] /D ^ | MET Setup Check with Pin
\text_in_r_reg[20] /CP  |  1.938 |   0.752 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   666 |  \text_in_r_reg[27] /D ^ | MET Setup Check with Pin
\text_in_r_reg[27] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
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     |   667 |  \text_in_r_reg[16] /D ^ | MET Setup Check with Pin
\text_in_r_reg[16] /CP  |  1.938 |   0.752 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   668 |   \text_in_r_reg[4] /D ^ | MET Setup Check with Pin
\text_in_r_reg[4] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   669 |   \text_in_r_reg[9] /E v | MET Setup Check with Pin
\text_in_r_reg[9] /CP   |  1.938 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   670 |   \text_in_r_reg[2] /D ^ | MET Setup Check with Pin
\text_in_r_reg[2] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   671 |   \text_in_r_reg[3] /D ^ | MET Setup Check with Pin
\text_in_r_reg[3] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   672 |  \text_in_r_reg[18] /D ^ | MET Setup Check with Pin
\text_in_r_reg[18] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   673 |  \text_in_r_reg[23] /D ^ | MET Setup Check with Pin
\text_in_r_reg[23] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   674 |   \text_in_r_reg[7] /E v | MET Setup Check with Pin
\text_in_r_reg[7] /CP   |  1.938 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   675 |   \text_in_r_reg[6] /D ^ | MET Setup Check with Pin
\text_in_r_reg[6] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   676 |  \text_in_r_reg[29] /D ^ | MET Setup Check with Pin
\text_in_r_reg[29] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   677 |  \text_in_r_reg[10] /E v | MET Setup Check with Pin
\text_in_r_reg[10] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   678 |   \text_in_r_reg[1] /D ^ | MET Setup Check with Pin
\text_in_r_reg[1] /CP   |  1.939 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   679 |  \text_in_r_reg[11] /E v | MET Setup Check with Pin
\text_in_r_reg[11] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   680 |   \text_in_r_reg[0] /D ^ | MET Setup Check with Pin
\text_in_r_reg[0] /CP   |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   681 |  \text_in_r_reg[17] /D ^ | MET Setup Check with Pin
\text_in_r_reg[17] /CP  |  1.939 |   0.751 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   682 |  \text_in_r_reg[25] /D ^ | MET Setup Check with Pin
\text_in_r_reg[25] /CP  |  1.939 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   683 |  \text_in_r_reg[79] /D ^ | MET Setup Check with Pin
\text_in_r_reg[79] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   684 |   \text_in_r_reg[5] /D ^ | MET Setup Check with Pin
\text_in_r_reg[5] /CP   |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
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     |   685 |  \text_in_r_reg[19] /D ^ | MET Setup Check with Pin
\text_in_r_reg[19] /CP  |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   686 |  \text_in_r_reg[76] /D ^ | MET Setup Check with Pin
\text_in_r_reg[76] /CP  |  1.941 |   0.754 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   687 |  \text_in_r_reg[54] /D ^ | MET Setup Check with Pin
\text_in_r_reg[54] /CP  |  1.943 |   0.760 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   688 |  \text_in_r_reg[82] /D ^ | MET Setup Check with Pin
\text_in_r_reg[82] /CP  |  1.943 |   0.754 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |   689 |  \text_in_r_reg[55] /D ^ | MET Setup Check with Pin
\text_in_r_reg[55] /CP  |  1.943 |   0.760 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   690 |  \text_in_r_reg[75] /D ^ | MET Setup Check with Pin
\text_in_r_reg[75] /CP  |  1.944 |   0.754 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |   691 |  \text_in_r_reg[72] /D ^ | MET Setup Check with Pin
\text_in_r_reg[72] /CP  |  1.944 |   0.753 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |   692 |  \text_in_r_reg[49] /D ^ | MET Setup Check with Pin
\text_in_r_reg[49] /CP  |  1.944 |   0.755 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   693 |  \text_in_r_reg[52] /D ^ | MET Setup Check with Pin
\text_in_r_reg[52] /CP  |  1.945 |   0.753 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |   694 |  \text_in_r_reg[51] /D ^ | MET Setup Check with Pin
\text_in_r_reg[51] /CP  |  1.946 |   0.754 |    2.700 | clk(D)(P) | clk(C)(P)
* |
     |   695 |  \text_in_r_reg[45] /D ^ | MET Setup Check with Pin
\text_in_r_reg[45] /CP  |  1.949 |   0.753 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |   696 |  \text_in_r_reg[43] /D ^ | MET Setup Check with Pin
\text_in_r_reg[43] /CP  |  1.951 |   0.756 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   697 |  \text_in_r_reg[48] /D ^ | MET Setup Check with Pin
\text_in_r_reg[48] /CP  |  1.952 |   0.755 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   698 |  \text_in_r_reg[44] /D ^ | MET Setup Check with Pin
\text_in_r_reg[44] /CP  |  1.954 |   0.753 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   699 |  \text_in_r_reg[46] /D ^ | MET Setup Check with Pin
\text_in_r_reg[46] /CP  |  1.954 |   0.754 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   700 |  \text_in_r_reg[13] /D ^ | MET Setup Check with Pin
\text_in_r_reg[13] /CP  |  1.955 |   0.752 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   701 |  \text_in_r_reg[47] /D ^ | MET Setup Check with Pin
\text_in_r_reg[47] /CP  |  1.955 |   0.753 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   702 |  \text_in_r_reg[14] /D ^ | MET Setup Check with Pin
\text_in_r_reg[14] /CP  |  1.955 |   0.752 |    2.707 | clk(D)(P) | clk(C)(P)
* |
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     |   703 |   \text_in_r_reg[8] /D ^ | MET Setup Check with Pin
\text_in_r_reg[8] /CP   |  1.955 |   0.750 |    2.705 | clk(D)(P) | clk(C)(P)
* |
     |   704 |  \text_in_r_reg[12] /D ^ | MET Setup Check with Pin
\text_in_r_reg[12] /CP  |  1.955 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   705 |   \text_in_r_reg[9] /D ^ | MET Setup Check with Pin
\text_in_r_reg[9] /CP   |  1.955 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   706 |   \text_in_r_reg[7] /D ^ | MET Setup Check with Pin
\text_in_r_reg[7] /CP   |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   707 |  \text_in_r_reg[11] /D ^ | MET Setup Check with Pin
\text_in_r_reg[11] /CP  |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   708 |  \text_in_r_reg[15] /D ^ | MET Setup Check with Pin
\text_in_r_reg[15] /CP  |  1.956 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   709 |  \text_in_r_reg[10] /D ^ | MET Setup Check with Pin
\text_in_r_reg[10] /CP  |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   710 |  \text_in_r_reg[67] /D ^ | MET Setup Check with Pin
\text_in_r_reg[67] /CP  |  1.957 |   0.757 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |   711 |  \text_in_r_reg[97] /D ^ | MET Setup Check with Pin
\text_in_r_reg[97] /CP  |  1.958 |   0.755 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |   712 | \text_in_r_reg[115] /D ^ | MET Setup Check with Pin
\text_in_r_reg[115] /CP |  1.959 |   0.757 |    2.715 | clk(D)(P) | clk(C)(P)
* |
     |   713 |  \text_in_r_reg[53] /D ^ | MET Setup Check with Pin
\text_in_r_reg[53] /CP  |  1.960 |   0.752 |    2.712 | clk(D)(P) | clk(C)(P)
* |
     |   714 | \text_in_r_reg[113] /D ^ | MET Setup Check with Pin
\text_in_r_reg[113] /CP |  1.961 |   0.757 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   715 |  \text_in_r_reg[73] /D ^ | MET Setup Check with Pin
\text_in_r_reg[73] /CP  |  1.961 |   0.763 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   716 |  \text_in_r_reg[70] /D ^ | MET Setup Check with Pin
\text_in_r_reg[70] /CP  |  1.962 |   0.761 |    2.722 | clk(D)(P) | clk(C)(P)
* |
     |   717 | \text_in_r_reg[109] /D ^ | MET Setup Check with Pin
\text_in_r_reg[109] /CP |  1.962 |   0.759 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   718 | \text_in_r_reg[114] /D ^ | MET Setup Check with Pin
\text_in_r_reg[114] /CP |  1.963 |   0.755 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   719 | \text_in_r_reg[107] /D ^ | MET Setup Check with Pin
\text_in_r_reg[107] /CP |  1.963 |   0.759 |    2.723 | clk(D)(P) | clk(C)(P)
* |
     |   720 |  \text_in_r_reg[69] /D ^ | MET Setup Check with Pin
\text_in_r_reg[69] /CP  |  1.964 |   0.759 |    2.723 | clk(D)(P) | clk(C)(P)
* |
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     |   721 |  \text_in_r_reg[65] /D ^ | MET Setup Check with Pin
\text_in_r_reg[65] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   722 |  \text_in_r_reg[80] /D ^ | MET Setup Check with Pin
\text_in_r_reg[80] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   723 |  \text_in_r_reg[59] /D ^ | MET Setup Check with Pin
\text_in_r_reg[59] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   724 |  \text_in_r_reg[61] /D ^ | MET Setup Check with Pin
\text_in_r_reg[61] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   725 |  \text_in_r_reg[41] /D ^ | MET Setup Check with Pin
\text_in_r_reg[41] /CP  |  1.965 |   0.752 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   726 |  \text_in_r_reg[36] /D ^ | MET Setup Check with Pin
\text_in_r_reg[36] /CP  |  1.965 |   0.752 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   727 |  \text_in_r_reg[66] /D ^ | MET Setup Check with Pin
\text_in_r_reg[66] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   728 |  \text_in_r_reg[62] /D ^ | MET Setup Check with Pin
\text_in_r_reg[62] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   729 |  \text_in_r_reg[60] /D ^ | MET Setup Check with Pin
\text_in_r_reg[60] /CP  |  1.966 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   730 |  \text_in_r_reg[35] /D ^ | MET Setup Check with Pin
\text_in_r_reg[35] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   731 |  \text_in_r_reg[68] /D ^ | MET Setup Check with Pin
\text_in_r_reg[68] /CP  |  1.966 |   0.758 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   732 |  \text_in_r_reg[37] /D ^ | MET Setup Check with Pin
\text_in_r_reg[37] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   733 |  \text_in_r_reg[32] /D ^ | MET Setup Check with Pin
\text_in_r_reg[32] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   734 |  \text_in_r_reg[42] /D ^ | MET Setup Check with Pin
\text_in_r_reg[42] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   735 |  \text_in_r_reg[58] /D ^ | MET Setup Check with Pin
\text_in_r_reg[58] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   736 |  \text_in_r_reg[63] /D ^ | MET Setup Check with Pin
\text_in_r_reg[63] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   737 |  \text_in_r_reg[39] /D ^ | MET Setup Check with Pin
\text_in_r_reg[39] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   738 |  \text_in_r_reg[56] /D ^ | MET Setup Check with Pin
\text_in_r_reg[56] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   739 |  \text_in_r_reg[57] /D ^ | MET Setup Check with Pin
\text_in_r_reg[57] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   740 |  \text_in_r_reg[40] /D ^ | MET Setup Check with Pin
\text_in_r_reg[40] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   741 |  \text_in_r_reg[34] /D ^ | MET Setup Check with Pin
\text_in_r_reg[34] /CP  |  1.967 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   742 |  \text_in_r_reg[50] /D ^ | MET Setup Check with Pin
\text_in_r_reg[50] /CP  |  1.967 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   743 |  \text_in_r_reg[33] /D ^ | MET Setup Check with Pin
\text_in_r_reg[33] /CP  |  1.967 |   0.750 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   744 | \text_in_r_reg[105] /D ^ | MET Setup Check with Pin
\text_in_r_reg[105] /CP |  1.967 |   0.758 |    2.725 | clk(D)(P) | clk(C)(P)
* |
     |   745 |  \text_in_r_reg[38] /D ^ | MET Setup Check with Pin
\text_in_r_reg[38] /CP  |  1.967 |   0.750 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   746 | \text_in_r_reg[108] /D ^ | MET Setup Check with Pin
\text_in_r_reg[108] /CP |  1.968 |   0.758 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   747 | \text_in_r_reg[106] /D ^ | MET Setup Check with Pin
\text_in_r_reg[106] /CP |  1.968 |   0.759 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   748 |  \text_in_r_reg[64] /D ^ | MET Setup Check with Pin
\text_in_r_reg[64] /CP  |  1.968 |   0.756 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   749 | \text_in_r_reg[112] /D ^ | MET Setup Check with Pin
\text_in_r_reg[112] /CP |  1.968 |   0.758 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   750 | \text_in_r_reg[104] /D ^ | MET Setup Check with Pin
\text_in_r_reg[104] /CP |  1.969 |   0.757 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   751 | \text_in_r_reg[110] /D ^ | MET Setup Check with Pin
\text_in_r_reg[110] /CP |  1.970 |   0.754 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   752 |  \text_in_r_reg[71] /D ^ | MET Setup Check with Pin
\text_in_r_reg[71] /CP  |  1.970 |   0.754 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   753 | \text_in_r_reg[111] /D ^ | MET Setup Check with Pin
\text_in_r_reg[111] /CP |  1.971 |   0.756 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   754 | \text_in_r_reg[116] /D ^ | MET Setup Check with Pin
\text_in_r_reg[116] /CP |  1.973 |   0.754 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   755 | \text_in_r_reg[127] /D ^ | MET Setup Check with Pin
\text_in_r_reg[127] /CP |  1.975 |   0.753 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   756 | \text_in_r_reg[121] /D ^ | MET Setup Check with Pin
\text_in_r_reg[121] /CP |  1.975 |   0.753 |    2.728 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   757 | \text_in_r_reg[123] /D ^ | MET Setup Check with Pin
\text_in_r_reg[123] /CP |  1.975 |   0.752 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   758 | \text_in_r_reg[122] /D ^ | MET Setup Check with Pin
\text_in_r_reg[122] /CP |  1.975 |   0.752 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   759 | \text_in_r_reg[126] /D ^ | MET Setup Check with Pin
\text_in_r_reg[126] /CP |  1.978 |   0.752 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |   760 | \text_in_r_reg[124] /D ^ | MET Setup Check with Pin
\text_in_r_reg[124] /CP |  1.980 |   0.752 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   761 |  \text_in_r_reg[88] /D ^ | MET Setup Check with Pin
\text_in_r_reg[88] /CP  |  1.980 |   0.762 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   762 | \text_in_r_reg[120] /D ^ | MET Setup Check with Pin
\text_in_r_reg[120] /CP |  1.980 |   0.752 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   763 |  \text_in_r_reg[91] /D ^ | MET Setup Check with Pin
\text_in_r_reg[91] /CP  |  1.981 |   0.761 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   764 |  \text_in_r_reg[90] /D ^ | MET Setup Check with Pin
\text_in_r_reg[90] /CP  |  1.982 |   0.760 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   765 |  \text_in_r_reg[83] /D ^ | MET Setup Check with Pin
\text_in_r_reg[83] /CP  |  1.982 |   0.760 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   766 | \text_in_r_reg[125] /D ^ | MET Setup Check with Pin
\text_in_r_reg[125] /CP |  1.984 |   0.752 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   767 |  \text_in_r_reg[85] /D ^ | MET Setup Check with Pin
\text_in_r_reg[85] /CP  |  1.985 |   0.756 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   768 |  \text_in_r_reg[89] /D ^ | MET Setup Check with Pin
\text_in_r_reg[89] /CP  |  1.985 |   0.759 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   769 | \text_in_r_reg[119] /D ^ | MET Setup Check with Pin
\text_in_r_reg[119] /CP |  1.985 |   0.752 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   770 |  \text_in_r_reg[84] /D ^ | MET Setup Check with Pin
\text_in_r_reg[84] /CP  |  1.986 |   0.757 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   771 |  \text_in_r_reg[86] /D ^ | MET Setup Check with Pin
\text_in_r_reg[86] /CP  |  1.986 |   0.756 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   772 | \text_in_r_reg[117] /D ^ | MET Setup Check with Pin
\text_in_r_reg[117] /CP |  1.986 |   0.754 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   773 | \text_in_r_reg[103] /D ^ | MET Setup Check with Pin
\text_in_r_reg[103] /CP |  1.986 |   0.751 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   774 |  \text_in_r_reg[95] /D ^ | MET Setup Check with Pin
\text_in_r_reg[95] /CP  |  1.986 |   0.754 |    2.740 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   775 | \text_in_r_reg[102] /D ^ | MET Setup Check with Pin
\text_in_r_reg[102] /CP |  1.986 |   0.751 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   776 |  \text_in_r_reg[93] /D ^ | MET Setup Check with Pin
\text_in_r_reg[93] /CP  |  1.987 |   0.755 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   777 |  \text_in_r_reg[87] /D ^ | MET Setup Check with Pin
\text_in_r_reg[87] /CP  |  1.987 |   0.754 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   778 | \text_in_r_reg[101] /D ^ | MET Setup Check with Pin
\text_in_r_reg[101] /CP |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   779 | \text_in_r_reg[100] /D ^ | MET Setup Check with Pin
\text_in_r_reg[100] /CP |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   780 |  \text_in_r_reg[94] /D ^ | MET Setup Check with Pin
\text_in_r_reg[94] /CP  |  1.987 |   0.753 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   781 |  \text_in_r_reg[98] /D ^ | MET Setup Check with Pin
\text_in_r_reg[98] /CP  |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   782 |  \text_in_r_reg[96] /D ^ | MET Setup Check with Pin
\text_in_r_reg[96] /CP  |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   783 | \text_in_r_reg[118] /D ^ | MET Setup Check with Pin
\text_in_r_reg[118] /CP |  1.987 |   0.753 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   784 |  \text_in_r_reg[99] /D ^ | MET Setup Check with Pin
\text_in_r_reg[99] /CP  |  1.988 |   0.751 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   785 |  \text_in_r_reg[92] /D ^ | MET Setup Check with Pin
\text_in_r_reg[92] /CP  |  1.991 |   0.752 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   786 |  \text_in_r_reg[81] /D ^ | MET Setup Check with Pin
\text_in_r_reg[81] /CP  |  1.992 |   0.752 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   787 |             ld_r_reg/D ^ | MET Setup Check with Pin
ld_r_reg/CP             |  1.999 |   0.757 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     +-------------------------------------------------------------------------
-------------------------------------------------------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary > $rpt_dir/report_timing.post_extract.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net > $rpt_dir/report_timing.post_extract.slack
<CMD> report_clocks
     +-------------------------------------------------------------------+
     |                        Clock Descriptions                         |
     |-------------------------------------------------------------------|
```

```
     |       |        |        |       |       |       Attributes       |
     |-------+--------+--------+-------+-------+------------------------|
     | Clock | Source | Period |  Lead | Trail | Generated | Propagated |
     |  Name |        |        |       |       |           |            |
     |-------+--------+--------+-------+-------+-----------+------------|
     |  clk  |  clk   |  2.500 | 0.000 | 1.800 |     n     |     y      |
     +-------------------------------------------------------------------+
<CMD> setAnalysisMode -analysisType single -checkType hold -skew true -
clockPropagation sdccontrol
<CMD> report_timing
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 587.4M)
Number of Loop : 0
Start delay calculation (mem=587.441M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:01.5 real=0:00:01.0 mem=587.441M 0)
*** CDM Built up (cpu=0:00:02.2  real=0:00:02.0  mem= 587.4M) ***
Path 1: MET Hold Check with Pin ld_r_reg/CP
Endpoint:   ld_r_reg/D (v) checked with  leading edge of 'clk'
Beginpoint: ld         (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.241
+ Hold                         0.045
+ Phase Shift                  0.000
= Required Time                0.286
  Arrival Time                 0.406
  Slack Time                   0.121
     Clock Rise Edge                      0.000
     + Input Delay                        0.400
     + Drive Adjustment                   0.004
     = Beginpoint Arrival Time            0.404
     +-------------------------------------------------------------------+
     | Instance |  Arc  |       Cell        | Delay | Arrival | Required |
     |          |       |                   |       |  Time   |   Time   |
     |----------+-------+-------------------+-------+---------+----------|
     |          | ld v  |                   |       |   0.404 |    0.284 |
     | ld_r_reg | D v   | HS65_GSS_DFPQNX27 | 0.002 |   0.406 |    0.286 |
     +-------------------------------------------------------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 10 -net -summary >
$rpt_dir/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 100 -net -summary >
$rpt_dir/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
```

```
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 10 -net -summary >
$rpt_dir/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 100 -net -summary >
$rpt_dir/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
max_points 100 -net > $rpt_dir/report_timing.post_extract.hold.slack
<CMD> fit
<CMD> setLayerPreference page2/2 -isVisible 1
<CMD> reportGateCount
Gate area 1.5600 um^2
[0] aes_cipher_top Gates=21935 Cells=9549 Area=34219.1 um^2
<CMD> setAnalysisMode -analysisType single -checkType setup -skew true -
clockPropagation sdccontrol
<CMD> report_timing -summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 587.4M)
Number of Loop : 0
Start delay calculation (mem=587.441M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:01.6 real=0:00:01.0 mem=587.441M 0)
*** CDM Built up (cpu=0:00:02.2  real=0:00:02.0  mem= 587.4M) ***
     +--------------------------------------------------------------------------
----------------------------------------------------------------------+
     |  Path |                       Pin | Cause
|  Slack | Arrival | Required |     Phase | Other Phase |
     |   No. |                           |
|        |         |          |           |             |
     |-------+-------------------------+-----------------------------------
--------------+--------+---------+----------+-----------+-------------|
     |     1 |        \sa32_reg[4] /D ^ | VIOLATED Setup Check with Pin
\sa32_reg[4] /CP   | -0.036 |   2.705 |    2.669 | clk(D)(P) | clk(C)(P) * |
     |     2 |        \sa31_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa31_reg[1] /CP   | -0.032 |   2.739 |    2.708 | clk(D)(P) | clk(C)(P) * |
     |     3 |        \sa20_reg[7] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[7] /CP   | -0.025 |   2.722 |    2.697 | clk(D)(P) | clk(C)(P) * |
     |     4 |        \sa20_reg[3] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[3] /CP   | -0.022 |   2.721 |    2.699 | clk(D)(P) | clk(C)(P) * |
     |     5 |        \sa00_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa00_reg[1] /CP   | -0.020 |   2.769 |    2.749 | clk(D)(P) | clk(C)(P) * |
```

```
     |     6 |        \sa23_reg[3] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[3] /CP   | -0.019 |   2.715 |    2.696 | clk(D)(P) | clk(C)(P) * |
     |     7 |        \sa23_reg[6] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[6] /CP   | -0.007 |   2.700 |    2.693 | clk(D)(P) | clk(C)(P) * |
     |     8 |        \sa23_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa23_reg[1] /CP   | -0.004 |   2.703 |    2.699 | clk(D)(P) | clk(C)(P) * |
     |     9 |        \sa20_reg[1] /D ^ | VIOLATED Setup Check with Pin
\sa20_reg[1] /CP   | -0.002 |   2.704 |    2.702 | clk(D)(P) | clk(C)(P) * |
     |    10 |        \sa32_reg[1] /D ^ | MET Setup Check with Pin
\sa32_reg[1] /CP     |  0.001 |   2.678 |    2.679 | clk(D)(P) | clk(C)(P)
* |
     |    11 |        \sa00_reg[3] /D ^ | MET Setup Check with Pin
\sa00_reg[3] /CP     |  0.002 |   2.750 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    12 |        \sa20_reg[4] /D ^ | MET Setup Check with Pin
\sa20_reg[4] /CP     |  0.003 |   2.698 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    13 |        \sa23_reg[4] /D ^ | MET Setup Check with Pin
\sa23_reg[4] /CP     |  0.003 |   2.697 |    2.700 | clk(D)(P) | clk(C)(P)
* |
     |    14 |        \sa00_reg[4] /D ^ | MET Setup Check with Pin
\sa00_reg[4] /CP     |  0.004 |   2.748 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    15 |        \sa31_reg[4] /D ^ | MET Setup Check with Pin
\sa31_reg[4] /CP     |  0.005 |   2.701 |    2.705 | clk(D)(P) | clk(C)(P)
* |
     |    16 |        \sa01_reg[1] /D ^ | MET Setup Check with Pin
\sa01_reg[1] /CP     |  0.008 |   2.708 |    2.715 | clk(D)(P) | clk(C)(P)
* |
     |    17 |        \sa21_reg[4] /D ^ | MET Setup Check with Pin
\sa21_reg[4] /CP     |  0.009 |   2.693 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    18 |        \sa11_reg[3] /D ^ | MET Setup Check with Pin
\sa11_reg[3] /CP     |  0.010 |   2.720 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |    19 |        \sa33_reg[1] /D ^ | MET Setup Check with Pin
\sa33_reg[1] /CP     |  0.015 |   2.686 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    20 |        \sa32_reg[3] /D ^ | MET Setup Check with Pin
\sa32_reg[3] /CP     |  0.020 |   2.653 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    21 |        \sa20_reg[0] /D ^ | MET Setup Check with Pin
\sa20_reg[0] /CP     |  0.022 |   2.679 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    22 |    u0/\w_reg[3][25] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][25] /CP    |  0.034 |   2.712 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |    23 |        \sa10_reg[0] /D ^ | MET Setup Check with Pin
\sa10_reg[0] /CP     |  0.040 |   2.660 |    2.700 | clk(D)(P) | clk(C)(P)
* |
     |    24 |        \sa33_reg[5] /D ^ | MET Setup Check with Pin
\sa33_reg[5] /CP     |  0.045 |   2.642 |    2.686 | clk(D)(P) | clk(C)(P)
* |
```

```
     |    25 |        \sa33_reg[4] /D ^ | MET Setup Check with Pin
\sa33_reg[4] /CP        |  0.047 |   2.641 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    26 |        \sa20_reg[5] /D ^ | MET Setup Check with Pin
\sa20_reg[5] /CP        |  0.050 |   2.652 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    27 |        \sa10_reg[7] /D ^ | MET Setup Check with Pin
\sa10_reg[7] /CP        |  0.053 |   2.625 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |    28 |        \sa12_reg[1] /D ^ | MET Setup Check with Pin
\sa12_reg[1] /CP        |  0.054 |   2.653 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    29 |        \sa20_reg[2] /D ^ | MET Setup Check with Pin
\sa20_reg[2] /CP        |  0.056 |   2.647 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |    30 |        \sa23_reg[2] /D ^ | MET Setup Check with Pin
\sa23_reg[2] /CP        |  0.060 |   2.626 |    2.686 | clk(D)(P) | clk(C)(P)
* |
     |    31 |        \sa03_reg[1] /D ^ | MET Setup Check with Pin
\sa03_reg[1] /CP        |  0.061 |   2.643 |    2.704 | clk(D)(P) | clk(C)(P)
* |
     |    32 |        \sa21_reg[7] /D ^ | MET Setup Check with Pin
\sa21_reg[7] /CP        |  0.064 |   2.640 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |    33 |        \sa10_reg[5] /D ^ | MET Setup Check with Pin
\sa10_reg[5] /CP        |  0.066 |   2.622 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |    34 |    u0/\w_reg[3][27] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][27] /CP    |  0.067 |   2.669 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |    35 |        \sa13_reg[7] /D ^ | MET Setup Check with Pin
\sa13_reg[7] /CP        |  0.067 |   2.607 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |    36 |        \sa03_reg[4] /D ^ | MET Setup Check with Pin
\sa03_reg[4] /CP        |  0.068 |   2.638 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    37 |        \sa03_reg[3] /D ^ | MET Setup Check with Pin
\sa03_reg[3] /CP        |  0.071 |   2.636 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    38 |        \sa31_reg[2] /D ^ | MET Setup Check with Pin
\sa31_reg[2] /CP        |  0.072 |   2.627 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |    39 |        \sa21_reg[3] /D ^ | MET Setup Check with Pin
\sa21_reg[3] /CP        |  0.076 |   2.638 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    40 |        \sa13_reg[1] /D ^ | MET Setup Check with Pin
\sa13_reg[1] /CP        |  0.076 |   2.597 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    41 |     u0/\w_reg[3][7] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][7] /CP     |  0.076 |   2.675 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    42 |        \sa21_reg[1] /D ^ | MET Setup Check with Pin
\sa21_reg[1] /CP        |  0.078 |   2.636 |    2.713 | clk(D)(P) | clk(C)(P)
* |
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     |    43 |        \sa31_reg[7] /D ^ | MET Setup Check with Pin
\sa31_reg[7] /CP        |  0.078 |   2.631 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |    44 |        \sa12_reg[3] /D ^ | MET Setup Check with Pin
\sa12_reg[3] /CP        |  0.079 |   2.635 |    2.713 | clk(D)(P) | clk(C)(P)
* |
     |    45 |        \sa13_reg[6] /D ^ | MET Setup Check with Pin
\sa13_reg[6] /CP        |  0.081 |   2.600 |    2.681 | clk(D)(P) | clk(C)(P)
* |
     |    46 |        \sa20_reg[6] /D ^ | MET Setup Check with Pin
\sa20_reg[6] /CP        |  0.081 |   2.624 |    2.705 | clk(D)(P) | clk(C)(P)
* |
     |    47 |        \sa01_reg[4] /D ^ | MET Setup Check with Pin
\sa01_reg[4] /CP        |  0.082 |   2.681 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |    48 |        \sa10_reg[2] /D ^ | MET Setup Check with Pin
\sa10_reg[2] /CP        |  0.082 |   2.620 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    49 |        \sa31_reg[3] /D ^ | MET Setup Check with Pin
\sa31_reg[3] /CP        |  0.083 |   2.615 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    50 |        \sa23_reg[0] /D ^ | MET Setup Check with Pin
\sa23_reg[0] /CP        |  0.083 |   2.615 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    51 |        \sa01_reg[3] /D ^ | MET Setup Check with Pin
\sa01_reg[3] /CP        |  0.084 |   2.681 |    2.765 | clk(D)(P) | clk(C)(P)
* |
     |    52 |        \sa30_reg[7] /D ^ | MET Setup Check with Pin
\sa30_reg[7] /CP        |  0.087 |   2.671 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |    53 |        \sa32_reg[7] /D ^ | MET Setup Check with Pin
\sa32_reg[7] /CP        |  0.090 |   2.586 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |    54 |        \sa21_reg[2] /D ^ | MET Setup Check with Pin
\sa21_reg[2] /CP        |  0.091 |   2.621 |    2.712 | clk(D)(P) | clk(C)(P)
* |
     |    55 |        \sa32_reg[6] /D v | MET Setup Check with Pin
\sa32_reg[6] /CP        |  0.092 |   2.600 |    2.692 | clk(D)(P) | clk(C)(P)
* |
     |    56 |    u0/\w_reg[2][25] /D v | MET Setup Check with Pin
u0/\w_reg[2][25] /CP    |  0.093 |   2.661 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |    57 |        \sa22_reg[4] /D ^ | MET Setup Check with Pin
\sa22_reg[4] /CP        |  0.095 |   2.621 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    58 |        \sa21_reg[5] /D ^ | MET Setup Check with Pin
\sa21_reg[5] /CP        |  0.097 |   2.613 |    2.710 | clk(D)(P) | clk(C)(P)
* |
     |    59 |        \sa10_reg[1] /D ^ | MET Setup Check with Pin
\sa10_reg[1] /CP        |  0.098 |   2.605 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |    60 |        \sa11_reg[1] /D ^ | MET Setup Check with Pin
\sa11_reg[1] /CP        |  0.102 |   2.626 |    2.729 | clk(D)(P) | clk(C)(P)
* |
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```
     |    61 |        \sa31_reg[6] /D ^ | MET Setup Check with Pin
\sa31_reg[6] /CP        |  0.103 |   2.615 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |    62 |        \sa00_reg[0] /D ^ | MET Setup Check with Pin
\sa00_reg[0] /CP        |  0.104 |   2.649 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    63 |    u0/\w_reg[3][31] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][31] /CP    |  0.104 |   2.638 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |    64 |        \sa22_reg[3] /D ^ | MET Setup Check with Pin
\sa22_reg[3] /CP        |  0.104 |   2.612 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    65 |        \sa23_reg[7] /D ^ | MET Setup Check with Pin
\sa23_reg[7] /CP        |  0.106 |   2.595 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |    66 |        \sa11_reg[2] /D ^ | MET Setup Check with Pin
\sa11_reg[2] /CP        |  0.109 |   2.606 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |    67 |        \sa33_reg[7] /D ^ | MET Setup Check with Pin
\sa33_reg[7] /CP        |  0.110 |   2.587 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |    68 |        \sa03_reg[7] /D ^ | MET Setup Check with Pin
\sa03_reg[7] /CP        |  0.112 |   2.594 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    69 |        \sa01_reg[2] /D ^ | MET Setup Check with Pin
\sa01_reg[2] /CP        |  0.114 |   2.602 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |    70 |    u0/\w_reg[3][13] /D v | MET Setup Check with Pin
u0/\w_reg[3][13] /CP    |  0.115 |   2.638 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    71 |    u0/\w_reg[3][30] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][30] /CP    |  0.117 |   2.627 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |    72 |        \sa13_reg[3] /D ^ | MET Setup Check with Pin
\sa13_reg[3] /CP        |  0.118 |   2.556 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |    73 |        \sa13_reg[4] /D ^ | MET Setup Check with Pin
\sa13_reg[4] /CP        |  0.118 |   2.560 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |    74 |    u0/\w_reg[3][26] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][26] /CP    |  0.119 |   2.618 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |    75 |        \sa03_reg[5] /D ^ | MET Setup Check with Pin
\sa03_reg[5] /CP        |  0.120 |   2.586 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |    76 |        \sa13_reg[2] /D ^ | MET Setup Check with Pin
\sa13_reg[2] /CP        |  0.121 |   2.547 |    2.668 | clk(D)(P) | clk(C)(P)
* |
     |    77 |        \sa10_reg[3] /D ^ | MET Setup Check with Pin
\sa10_reg[3] /CP        |  0.122 |   2.582 |    2.704 | clk(D)(P) | clk(C)(P)
* |
     |    78 |        \sa31_reg[5] /D ^ | MET Setup Check with Pin
\sa31_reg[5] /CP        |  0.126 |   2.583 |    2.708 | clk(D)(P) | clk(C)(P)
* |
```

```
     |    79 |        \sa21_reg[6] /D ^ | MET Setup Check with Pin
\sa21_reg[6] /CP        |  0.127 |   2.588 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    80 |    u0/\w_reg[3][28] /D v | MET Setup Check with Pin
u0/\w_reg[3][28] /CP    |  0.127 |   2.628 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |    81 |        \sa30_reg[1] /D ^ | MET Setup Check with Pin
\sa30_reg[1] /CP        |  0.128 |   2.630 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |    82 |    u0/\w_reg[3][14] /D v | MET Setup Check with Pin
u0/\w_reg[3][14] /CP    |  0.128 |   2.624 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |    83 |        \sa13_reg[5] /D ^ | MET Setup Check with Pin
\sa13_reg[5] /CP        |  0.129 |   2.550 |    2.679 | clk(D)(P) | clk(C)(P)
* |
     |    84 |        \sa02_reg[4] /D ^ | MET Setup Check with Pin
\sa02_reg[4] /CP        |  0.129 |   2.604 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |    85 |    u0/\w_reg[3][24] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][24] /CP    |  0.131 |   2.614 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |    86 |        \sa33_reg[3] /D ^ | MET Setup Check with Pin
\sa33_reg[3] /CP        |  0.133 |   2.566 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |    87 |    u0/\w_reg[2][27] /D v | MET Setup Check with Pin
u0/\w_reg[2][27] /CP    |  0.134 |   2.618 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |    88 |    u0/\w_reg[3][21] /D v | MET Setup Check with Pin
u0/\w_reg[3][21] /CP    |  0.135 |   2.612 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |    89 |        \sa10_reg[6] /D ^ | MET Setup Check with Pin
\sa10_reg[6] /CP        |  0.135 |   2.552 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    90 |        \sa22_reg[1] /D ^ | MET Setup Check with Pin
\sa22_reg[1] /CP        |  0.137 |   2.577 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |    91 |        \sa33_reg[6] /D ^ | MET Setup Check with Pin
\sa33_reg[6] /CP        |  0.137 |   2.551 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |    92 |        \sa13_reg[0] /D ^ | MET Setup Check with Pin
\sa13_reg[0] /CP        |  0.139 |   2.535 |    2.673 | clk(D)(P) | clk(C)(P)
* |
     |    93 |     u0/\w_reg[3][8] /D v | MET Setup Check with Pin
u0/\w_reg[3][8] /CP     |  0.144 |   2.620 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |    94 |        \sa22_reg[0] /D ^ | MET Setup Check with Pin
\sa22_reg[0] /CP        |  0.144 |   2.562 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |    95 |        \sa12_reg[0] /D ^ | MET Setup Check with Pin
\sa12_reg[0] /CP        |  0.146 |   2.562 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |    96 |     u0/\w_reg[3][2] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][2] /CP     |  0.147 |   2.603 |    2.749 | clk(D)(P) | clk(C)(P)
* |
```

```
     |    97 |        \sa02_reg[1] /D ^ | MET Setup Check with Pin
\sa02_reg[1] /CP        |  0.147 |   2.588 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |    98 |        \sa11_reg[5] /D ^ | MET Setup Check with Pin
\sa11_reg[5] /CP        |  0.148 |   2.586 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |    99 |        \sa23_reg[5] /D ^ | MET Setup Check with Pin
\sa23_reg[5] /CP        |  0.150 |   2.544 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   100 |    u0/\w_reg[3][10] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][10] /CP    |  0.151 |   2.597 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   101 |        \sa30_reg[3] /D ^ | MET Setup Check with Pin
\sa30_reg[3] /CP        |  0.151 |   2.608 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   102 |     u0/\w_reg[3][6] /D v | MET Setup Check with Pin
u0/\w_reg[3][6] /CP     |  0.152 |   2.615 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   103 |        \sa10_reg[4] /D ^ | MET Setup Check with Pin
\sa10_reg[4] /CP        |  0.156 |   2.546 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |   104 |     u0/\w_reg[2][7] /D v | MET Setup Check with Pin
u0/\w_reg[2][7] /CP     |  0.156 |   2.606 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   105 |        \sa32_reg[5] /D v | MET Setup Check with Pin
\sa32_reg[5] /CP        |  0.157 |   2.531 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   106 |        \sa12_reg[2] /D ^ | MET Setup Check with Pin
\sa12_reg[2] /CP        |  0.160 |   2.534 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   107 |     u0/\w_reg[3][5] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][5] /CP     |  0.161 |   2.588 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   108 |        \sa21_reg[0] /D ^ | MET Setup Check with Pin
\sa21_reg[0] /CP        |  0.163 |   2.552 |    2.715 | clk(D)(P) | clk(C)(P)
* |
     |   109 |        \sa00_reg[7] /D ^ | MET Setup Check with Pin
\sa00_reg[7] /CP        |  0.164 |   2.585 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   110 |        \sa30_reg[6] /D ^ | MET Setup Check with Pin
\sa30_reg[6] /CP        |  0.165 |   2.591 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   111 |        \sa03_reg[0] /D ^ | MET Setup Check with Pin
\sa03_reg[0] /CP        |  0.166 |   2.540 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   112 |        \sa11_reg[7] /D ^ | MET Setup Check with Pin
\sa11_reg[7] /CP        |  0.166 |   2.570 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   113 |        \sa32_reg[0] /D ^ | MET Setup Check with Pin
\sa32_reg[0] /CP        |  0.168 |   2.509 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |   114 |        \sa01_reg[5] /D ^ | MET Setup Check with Pin
\sa01_reg[5] /CP        |  0.169 |   2.586 |    2.756 | clk(D)(P) | clk(C)(P)
* |
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```
     |   115 |        \sa01_reg[0] /D ^ | MET Setup Check with Pin
\sa01_reg[0] /CP        |  0.170 |   2.595 |    2.765 | clk(D)(P) | clk(C)(P)
* |
     |   116 |    u0/\w_reg[2][31] /D v | MET Setup Check with Pin
u0/\w_reg[2][31] /CP    |  0.172 |   2.578 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   117 |        \sa30_reg[4] /D ^ | MET Setup Check with Pin
\sa30_reg[4] /CP        |  0.173 |   2.584 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   118 |        \sa11_reg[4] /D ^ | MET Setup Check with Pin
\sa11_reg[4] /CP        |  0.174 |   2.560 |    2.735 | clk(D)(P) | clk(C)(P)
* |
     |   119 |        \sa32_reg[2] /D ^ | MET Setup Check with Pin
\sa32_reg[2] /CP        |  0.175 |   2.499 |    2.674 | clk(D)(P) | clk(C)(P)
* |
     |   120 |        \sa01_reg[7] /D ^ | MET Setup Check with Pin
\sa01_reg[7] /CP        |  0.176 |   2.585 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   121 |        \sa11_reg[6] /D ^ | MET Setup Check with Pin
\sa11_reg[6] /CP        |  0.177 |   2.560 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   122 |        \sa12_reg[7] /D ^ | MET Setup Check with Pin
\sa12_reg[7] /CP        |  0.179 |   2.541 |    2.720 | clk(D)(P) | clk(C)(P)
* |
     |   123 |        \sa12_reg[4] /D ^ | MET Setup Check with Pin
\sa12_reg[4] /CP        |  0.180 |   2.536 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   124 |        \sa31_reg[0] /D ^ | MET Setup Check with Pin
\sa31_reg[0] /CP        |  0.181 |   2.522 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   125 |    u0/\w_reg[3][29] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][29] /CP    |  0.182 |   2.555 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   126 |        \sa03_reg[2] /D ^ | MET Setup Check with Pin
\sa03_reg[2] /CP        |  0.183 |   2.519 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   127 |    u0/\w_reg[2][30] /D v | MET Setup Check with Pin
u0/\w_reg[2][30] /CP    |  0.183 |   2.567 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   128 |        \sa30_reg[2] /D ^ | MET Setup Check with Pin
\sa30_reg[2] /CP        |  0.185 |   2.574 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   129 |    u0/\w_reg[2][26] /D v | MET Setup Check with Pin
u0/\w_reg[2][26] /CP    |  0.186 |   2.563 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   130 |        \sa11_reg[0] /D ^ | MET Setup Check with Pin
\sa11_reg[0] /CP        |  0.189 |   2.547 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   131 |        \sa02_reg[2] /D ^ | MET Setup Check with Pin
\sa02_reg[2] /CP        |  0.191 |   2.541 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   132 |     u0/\w_reg[3][9] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][9] /CP     |  0.191 |   2.546 |    2.738 | clk(D)(P) | clk(C)(P)
* |
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```
     |   133 |        \sa33_reg[2] /D ^ | MET Setup Check with Pin
\sa33_reg[2] /CP        |  0.192 |   2.502 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   134 |        \sa03_reg[6] /D ^ | MET Setup Check with Pin
\sa03_reg[6] /CP        |  0.193 |   2.508 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   135 |        \sa01_reg[6] /D ^ | MET Setup Check with Pin
\sa01_reg[6] /CP        |  0.195 |   2.563 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   136 |        \sa02_reg[7] /D ^ | MET Setup Check with Pin
\sa02_reg[7] /CP        |  0.199 |   2.535 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   137 |    u0/\w_reg[2][13] /D v | MET Setup Check with Pin
u0/\w_reg[2][13] /CP    |  0.200 |   2.548 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   138 |     u0/\w_reg[3][1] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][1] /CP     |  0.201 |   2.549 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   139 |    u0/\w_reg[2][28] /D v | MET Setup Check with Pin
u0/\w_reg[2][28] /CP    |  0.203 |   2.552 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |   140 |    u0/\w_reg[2][24] /D v | MET Setup Check with Pin
u0/\w_reg[2][24] /CP    |  0.206 |   2.547 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   141 |    u0/\w_reg[2][21] /D v | MET Setup Check with Pin
u0/\w_reg[2][21] /CP    |  0.208 |   2.537 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   142 |        \sa00_reg[5] /D ^ | MET Setup Check with Pin
\sa00_reg[5] /CP        |  0.209 |   2.542 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   143 |        \sa12_reg[5] /D ^ | MET Setup Check with Pin
\sa12_reg[5] /CP        |  0.209 |   2.508 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   144 |        \sa30_reg[0] /D ^ | MET Setup Check with Pin
\sa30_reg[0] /CP        |  0.210 |   2.547 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   145 |        \sa02_reg[5] /D ^ | MET Setup Check with Pin
\sa02_reg[5] /CP        |  0.211 |   2.520 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   146 |    u0/\w_reg[3][15] /D v | MET Setup Check with Pin
u0/\w_reg[3][15] /CP    |  0.214 |   2.539 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   147 |    u0/\w_reg[2][14] /D v | MET Setup Check with Pin
u0/\w_reg[2][14] /CP    |  0.214 |   2.533 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   148 |        \sa00_reg[6] /D ^ | MET Setup Check with Pin
\sa00_reg[6] /CP        |  0.216 |   2.539 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |   149 |     u0/\w_reg[3][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][0] /CP     |  0.216 |   2.533 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   150 |        \sa22_reg[2] /D ^ | MET Setup Check with Pin
\sa22_reg[2] /CP        |  0.219 |   2.492 |    2.711 | clk(D)(P) | clk(C)(P)
* |
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     |   151 |        \sa22_reg[6] /D ^ | MET Setup Check with Pin
\sa22_reg[6] /CP        |  0.219 |   2.507 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   152 |    u0/\w_reg[3][12] /D v | MET Setup Check with Pin
u0/\w_reg[3][12] /CP    |  0.221 |   2.528 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   153 |    u0/\w_reg[3][22] /D v | MET Setup Check with Pin
u0/\w_reg[3][22] /CP    |  0.222 |   2.524 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   154 |        \sa02_reg[3] /D ^ | MET Setup Check with Pin
\sa02_reg[3] /CP        |  0.222 |   2.510 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   155 |     u0/\w_reg[2][2] /D v | MET Setup Check with Pin
u0/\w_reg[2][2] /CP     |  0.222 |   2.535 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   156 |    u0/\w_reg[3][18] /D v | MET Setup Check with Pin
u0/\w_reg[3][18] /CP    |  0.223 |   2.531 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   157 |        \sa22_reg[7] /D ^ | MET Setup Check with Pin
\sa22_reg[7] /CP        |  0.223 |   2.503 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   158 |     u0/\w_reg[3][3] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][3] /CP     |  0.223 |   2.514 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   159 |    u0/\w_reg[2][10] /D v | MET Setup Check with Pin
u0/\w_reg[2][10] /CP    |  0.226 |   2.534 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   160 |     u0/\w_reg[2][6] /D v | MET Setup Check with Pin
u0/\w_reg[2][6] /CP     |  0.227 |   2.537 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   161 |     u0/\w_reg[2][5] /D v | MET Setup Check with Pin
u0/\w_reg[2][5] /CP     |  0.227 |   2.536 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   162 |    u0/\w_reg[3][11] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][11] /CP    |  0.229 |   2.510 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   163 |    u0/\w_reg[3][23] /D v | MET Setup Check with Pin
u0/\w_reg[3][23] /CP    |  0.230 |   2.531 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   164 |        \sa22_reg[5] /D ^ | MET Setup Check with Pin
\sa22_reg[5] /CP        |  0.231 |   2.488 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   165 |     u0/\w_reg[2][8] /D v | MET Setup Check with Pin
u0/\w_reg[2][8] /CP     |  0.232 |   2.528 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   166 |        \sa02_reg[0] /D ^ | MET Setup Check with Pin
\sa02_reg[0] /CP        |  0.233 |   2.500 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   167 |        \sa33_reg[0] /D ^ | MET Setup Check with Pin
\sa33_reg[0] /CP        |  0.239 |   2.452 |    2.691 | clk(D)(P) | clk(C)(P)
* |
     |   168 |        \sa30_reg[5] /D ^ | MET Setup Check with Pin
\sa30_reg[5] /CP        |  0.243 |   2.517 |    2.760 | clk(D)(P) | clk(C)(P)
* |
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     |   169 |    u0/\w_reg[1][25] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][25] /CP    |  0.245 |   2.519 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   170 |        \sa02_reg[6] /D ^ | MET Setup Check with Pin
\sa02_reg[6] /CP        |  0.247 |   2.483 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   171 |    u0/\w_reg[2][29] /D v | MET Setup Check with Pin
u0/\w_reg[2][29] /CP    |  0.249 |   2.500 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   172 |     u0/\w_reg[3][4] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][4] /CP     |  0.252 |   2.496 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   173 |        \sa00_reg[2] /D ^ | MET Setup Check with Pin
\sa00_reg[2] /CP        |  0.254 |   2.497 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   174 |     u0/\w_reg[2][9] /D v | MET Setup Check with Pin
u0/\w_reg[2][9] /CP     |  0.269 |   2.477 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   175 |     u0/\w_reg[2][1] /D v | MET Setup Check with Pin
u0/\w_reg[2][1] /CP     |  0.273 |   2.489 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   176 |    u0/\w_reg[3][20] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][20] /CP    |  0.279 |   2.459 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   177 |    u0/\w_reg[3][16] /D ^ | MET Setup Check with Pin
u0/\w_reg[3][16] /CP    |  0.283 |   2.457 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   178 |     u0/\w_reg[1][7] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][7] /CP     |  0.283 |   2.479 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   179 |    u0/\w_reg[2][15] /D v | MET Setup Check with Pin
u0/\w_reg[2][15] /CP    |  0.288 |   2.459 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   180 |        \sa12_reg[6] /D ^ | MET Setup Check with Pin
\sa12_reg[6] /CP        |  0.289 |   2.432 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   181 |    u0/\w_reg[2][18] /D v | MET Setup Check with Pin
u0/\w_reg[2][18] /CP    |  0.291 |   2.457 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   182 |     u0/\w_reg[2][0] /D v | MET Setup Check with Pin
u0/\w_reg[2][0] /CP     |  0.291 |   2.469 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   183 |    u0/\w_reg[2][22] /D v | MET Setup Check with Pin
u0/\w_reg[2][22] /CP    |  0.295 |   2.449 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   184 |    u0/\w_reg[1][27] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][27] /CP    |  0.296 |   2.468 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   185 |    u0/\w_reg[2][12] /D v | MET Setup Check with Pin
u0/\w_reg[2][12] /CP    |  0.299 |   2.450 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   186 |    u0/\w_reg[3][17] /D v | MET Setup Check with Pin
u0/\w_reg[3][17] /CP    |  0.306 |   2.448 |    2.753 | clk(D)(P) | clk(C)(P)
* |
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     |   187 |     u0/\w_reg[2][3] /D v | MET Setup Check with Pin
u0/\w_reg[2][3] /CP     |  0.307 |   2.449 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   188 |    u0/\w_reg[1][30] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][30] /CP    |  0.309 |   2.437 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   189 |    u0/\w_reg[2][23] /D v | MET Setup Check with Pin
u0/\w_reg[2][23] /CP    |  0.311 |   2.444 |    2.755 | clk(D)(P) | clk(C)(P)
* |
     |   190 |    u0/\w_reg[1][10] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][10] /CP    |  0.313 |   2.421 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |   191 |    u0/\w_reg[1][31] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][31] /CP    |  0.316 |   2.447 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   192 |    u0/\w_reg[3][19] /D v | MET Setup Check with Pin
u0/\w_reg[3][19] /CP    |  0.321 |   2.427 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   193 |    u0/\w_reg[2][11] /D v | MET Setup Check with Pin
u0/\w_reg[2][11] /CP    |  0.324 |   2.434 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   194 |     u0/\w_reg[2][4] /D v | MET Setup Check with Pin
u0/\w_reg[2][4] /CP     |  0.324 |   2.433 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   195 |    u0/\w_reg[1][13] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][13] /CP    |  0.325 |   2.439 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   196 |    u0/\w_reg[1][26] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][26] /CP    |  0.339 |   2.425 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   197 |    u0/\w_reg[1][21] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][21] /CP    |  0.339 |   2.421 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   198 |    u0/\w_reg[1][14] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][14] /CP    |  0.340 |   2.424 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   199 |    u0/\w_reg[1][28] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][28] /CP    |  0.343 |   2.421 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   200 |     u0/\w_reg[1][8] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][8] /CP     |  0.346 |   2.418 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   201 |     u0/\w_reg[1][2] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][2] /CP     |  0.346 |   2.416 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   202 |     u0/\w_reg[1][6] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][6] /CP     |  0.349 |   2.413 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   203 |    u0/\w_reg[1][24] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][24] /CP    |  0.349 |   2.409 |    2.758 | clk(D)(P) | clk(C)(P)
* |
     |   204 |     u0/\w_reg[1][5] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][5] /CP     |  0.355 |   2.407 |    2.761 | clk(D)(P) | clk(C)(P)
* |
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     |   205 |    u0/\w_reg[2][20] /D v | MET Setup Check with Pin
u0/\w_reg[2][20] /CP    |  0.355 |   2.392 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   206 |    u0/\w_reg[2][16] /D v | MET Setup Check with Pin
u0/\w_reg[2][16] /CP    |  0.365 |   2.383 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   207 |     u0/\w_reg[1][9] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][9] /CP     |  0.372 |   2.367 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   208 |   \text_out_reg[13] /D v | MET Setup Check with Pin
\text_out_reg[13] /CP   |  0.376 |   2.356 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   209 |    u0/\w_reg[1][29] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][29] /CP    |  0.379 |   2.367 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   210 |    u0/\w_reg[2][17] /D v | MET Setup Check with Pin
u0/\w_reg[2][17] /CP    |  0.381 |   2.368 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   211 |     u0/\w_reg[1][1] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][1] /CP     |  0.394 |   2.368 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   212 |    u0/\w_reg[2][19] /D v | MET Setup Check with Pin
u0/\w_reg[2][19] /CP    |  0.398 |   2.350 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   213 |    u0/\w_reg[1][11] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][11] /CP    |  0.411 |   2.324 |    2.735 | clk(D)(P) | clk(C)(P)
* |
     |   214 |    u0/\w_reg[1][15] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][15] /CP    |  0.418 |   2.346 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   215 |     u0/\w_reg[1][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][0] /CP     |  0.421 |   2.340 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   216 |    u0/\w_reg[1][18] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][18] /CP    |  0.421 |   2.342 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   217 |    u0/\w_reg[1][12] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][12] /CP    |  0.426 |   2.338 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   218 |    u0/\w_reg[1][23] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][23] /CP    |  0.428 |   2.336 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   219 |    u0/\w_reg[1][22] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][22] /CP    |  0.428 |   2.332 |    2.761 | clk(D)(P) | clk(C)(P)
* |
     |   220 |  \text_out_reg[120] /D v | MET Setup Check with Pin
\text_out_reg[120] /CP  |  0.429 |   2.337 |    2.766 | clk(D)(P) | clk(C)(P)
* |
     |   221 |     u0/\w_reg[1][3] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][3] /CP     |  0.429 |   2.333 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   222 |  \text_out_reg[121] /D v | MET Setup Check with Pin
\text_out_reg[121] /CP  |  0.444 |   2.323 |    2.767 | clk(D)(P) | clk(C)(P)
* |
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     |   223 |    u0/\w_reg[0][25] /D v | MET Setup Check with Pin
u0/\w_reg[0][25] /CP    |  0.446 |   2.335 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   224 |     u0/\w_reg[1][4] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][4] /CP     |  0.449 |   2.312 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   225 |    u0/\w_reg[0][30] /D v | MET Setup Check with Pin
u0/\w_reg[0][30] /CP    |  0.449 |   2.307 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     |   226 |   \text_out_reg[14] /D ^ | MET Setup Check with Pin
\text_out_reg[14] /CP   |  0.453 |   2.255 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   227 |    u0/\w_reg[0][13] /D v | MET Setup Check with Pin
u0/\w_reg[0][13] /CP    |  0.453 |   2.327 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   228 |  \text_out_reg[122] /D v | MET Setup Check with Pin
\text_out_reg[122] /CP  |  0.458 |   2.305 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   229 |    \text_out_reg[0] /D v | MET Setup Check with Pin
\text_out_reg[0] /CP    |  0.459 |   2.237 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   230 |   \text_out_reg[65] /D v | MET Setup Check with Pin
\text_out_reg[65] /CP   |  0.463 |   2.320 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   231 |    \text_out_reg[9] /D ^ | MET Setup Check with Pin
\text_out_reg[9] /CP    |  0.465 |   2.258 |    2.723 | clk(D)(P) | clk(C)(P)
* |
     |   232 |   \text_out_reg[82] /D v | MET Setup Check with Pin
\text_out_reg[82] /CP   |  0.467 |   2.252 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   233 |   \text_out_reg[32] /D v | MET Setup Check with Pin
\text_out_reg[32] /CP   |  0.472 |   2.263 |    2.735 | clk(D)(P) | clk(C)(P)
* |
     |   234 |  \text_out_reg[127] /D v | MET Setup Check with Pin
\text_out_reg[127] /CP  |  0.473 |   2.294 |    2.767 | clk(D)(P) | clk(C)(P)
* |
     |   235 |  \text_out_reg[125] /D ^ | MET Setup Check with Pin
\text_out_reg[125] /CP  |  0.473 |   2.281 |    2.754 | clk(D)(P) | clk(C)(P)
* |
     |   236 |    u0/\w_reg[0][31] /D v | MET Setup Check with Pin
u0/\w_reg[0][31] /CP    |  0.480 |   2.301 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   237 |    u0/\w_reg[0][14] /D v | MET Setup Check with Pin
u0/\w_reg[0][14] /CP    |  0.481 |   2.300 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   238 |   \text_out_reg[93] /D v | MET Setup Check with Pin
\text_out_reg[93] /CP   |  0.485 |   2.302 |    2.786 | clk(D)(P) | clk(C)(P)
* |
     |   239 |    u0/\w_reg[1][20] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][20] /CP    |  0.485 |   2.278 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   240 |    \text_out_reg[5] /D v | MET Setup Check with Pin
\text_out_reg[5] /CP    |  0.489 |   2.208 |    2.697 | clk(D)(P) | clk(C)(P)
* |
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```
     |   241 |    u0/\w_reg[1][16] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][16] /CP    |  0.491 |   2.273 |    2.764 | clk(D)(P) | clk(C)(P)
* |
     |   242 |   \text_out_reg[87] /D ^ | MET Setup Check with Pin
\text_out_reg[87] /CP   |  0.493 |   2.246 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   243 |     u0/\w_reg[0][8] /D v | MET Setup Check with Pin
u0/\w_reg[0][8] /CP     |  0.494 |   2.287 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   244 |   \text_out_reg[64] /D v | MET Setup Check with Pin
\text_out_reg[64] /CP   |  0.496 |   2.256 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |   245 |     u0/\w_reg[0][7] /D v | MET Setup Check with Pin
u0/\w_reg[0][7] /CP     |  0.496 |   2.277 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   246 |   \text_out_reg[56] /D v | MET Setup Check with Pin
\text_out_reg[56] /CP   |  0.497 |   2.242 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   247 |   \text_out_reg[29] /D v | MET Setup Check with Pin
\text_out_reg[29] /CP   |  0.498 |   2.221 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   248 |    u0/\w_reg[0][10] /D v | MET Setup Check with Pin
u0/\w_reg[0][10] /CP    |  0.499 |   2.282 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   249 |  \text_out_reg[101] /D ^ | MET Setup Check with Pin
\text_out_reg[101] /CP  |  0.501 |   2.240 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   250 |   \text_out_reg[97] /D ^ | MET Setup Check with Pin
\text_out_reg[97] /CP   |  0.504 |   2.241 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   251 |    u0/\w_reg[0][28] /D v | MET Setup Check with Pin
u0/\w_reg[0][28] /CP    |  0.504 |   2.278 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   252 |   \text_out_reg[69] /D v | MET Setup Check with Pin
\text_out_reg[69] /CP   |  0.506 |   2.276 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   253 |   \text_out_reg[26] /D v | MET Setup Check with Pin
\text_out_reg[26] /CP   |  0.509 |   2.200 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   254 |   \text_out_reg[70] /D v | MET Setup Check with Pin
\text_out_reg[70] /CP   |  0.509 |   2.270 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   255 |   \text_out_reg[15] /D v | MET Setup Check with Pin
\text_out_reg[15] /CP   |  0.512 |   2.225 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   256 |  \text_out_reg[117] /D ^ | MET Setup Check with Pin
\text_out_reg[117] /CP  |  0.512 |   2.232 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   257 |   \text_out_reg[54] /D v | MET Setup Check with Pin
\text_out_reg[54] /CP   |  0.512 |   2.223 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   258 |   \text_out_reg[89] /D v | MET Setup Check with Pin
\text_out_reg[89] /CP   |  0.513 |   2.273 |    2.786 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   259 |   \text_out_reg[17] /D v | MET Setup Check with Pin
\text_out_reg[17] /CP   |  0.514 |   2.214 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   260 |    u0/\w_reg[1][17] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][17] /CP    |  0.514 |   2.249 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   261 |   \text_out_reg[81] /D v | MET Setup Check with Pin
\text_out_reg[81] /CP   |  0.517 |   2.265 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   262 |   \text_out_reg[23] /D v | MET Setup Check with Pin
\text_out_reg[23] /CP   |  0.517 |   2.215 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   263 |    u0/\w_reg[0][21] /D v | MET Setup Check with Pin
u0/\w_reg[0][21] /CP    |  0.521 |   2.257 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   264 |   \text_out_reg[37] /D v | MET Setup Check with Pin
\text_out_reg[37] /CP   |  0.521 |   2.224 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   265 |    u0/\w_reg[0][27] /D v | MET Setup Check with Pin
u0/\w_reg[0][27] /CP    |  0.523 |   2.259 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   266 |   \text_out_reg[52] /D ^ | MET Setup Check with Pin
\text_out_reg[52] /CP   |  0.523 |   2.196 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   267 |   \text_out_reg[90] /D ^ | MET Setup Check with Pin
\text_out_reg[90] /CP   |  0.526 |   2.220 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   268 |    u0/\w_reg[1][19] /D ^ | MET Setup Check with Pin
u0/\w_reg[1][19] /CP    |  0.526 |   2.237 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   269 |   \text_out_reg[88] /D v | MET Setup Check with Pin
\text_out_reg[88] /CP   |  0.526 |   2.255 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   270 |     u0/\w_reg[0][2] /D v | MET Setup Check with Pin
u0/\w_reg[0][2] /CP     |  0.528 |   2.251 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   271 |  \text_out_reg[109] /D v | MET Setup Check with Pin
\text_out_reg[109] /CP  |  0.528 |   2.232 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   272 |  \text_out_reg[103] /D ^ | MET Setup Check with Pin
\text_out_reg[103] /CP  |  0.528 |   2.220 |    2.748 | clk(D)(P) | clk(C)(P)
* |
     |   273 |    u0/\w_reg[0][26] /D v | MET Setup Check with Pin
u0/\w_reg[0][26] /CP    |  0.530 |   2.252 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   274 |   \text_out_reg[49] /D v | MET Setup Check with Pin
\text_out_reg[49] /CP   |  0.533 |   2.210 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   275 |   \text_out_reg[57] /D v | MET Setup Check with Pin
\text_out_reg[57] /CP   |  0.534 |   2.209 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   276 |    u0/\w_reg[0][29] /D v | MET Setup Check with Pin
u0/\w_reg[0][29] /CP    |  0.537 |   2.219 |    2.756 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   277 |     u0/\w_reg[0][9] /D v | MET Setup Check with Pin
u0/\w_reg[0][9] /CP     |  0.538 |   2.244 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   278 |   \text_out_reg[25] /D v | MET Setup Check with Pin
\text_out_reg[25] /CP   |  0.539 |   2.179 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   279 |   \text_out_reg[79] /D v | MET Setup Check with Pin
\text_out_reg[79] /CP   |  0.540 |   2.182 |    2.722 | clk(D)(P) | clk(C)(P)
* |
     |   280 |    \text_out_reg[2] /D v | MET Setup Check with Pin
\text_out_reg[2] /CP    |  0.542 |   2.151 |    2.693 | clk(D)(P) | clk(C)(P)
* |
     |   281 |    u0/\w_reg[0][12] /D v | MET Setup Check with Pin
u0/\w_reg[0][12] /CP    |  0.542 |   2.238 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   282 |     u0/\w_reg[0][6] /D ^ | MET Setup Check with Pin
u0/\w_reg[0][6] /CP     |  0.543 |   2.216 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   283 |   \text_out_reg[30] /D v | MET Setup Check with Pin
\text_out_reg[30] /CP   |  0.544 |   2.164 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   284 |    u0/\w_reg[0][24] /D v | MET Setup Check with Pin
u0/\w_reg[0][24] /CP    |  0.544 |   2.238 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   285 |     u0/\w_reg[0][5] /D v | MET Setup Check with Pin
u0/\w_reg[0][5] /CP     |  0.544 |   2.232 |    2.776 | clk(D)(P) | clk(C)(P)
* |
     |   286 |   \text_out_reg[66] /D v | MET Setup Check with Pin
\text_out_reg[66] /CP   |  0.547 |   2.238 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   287 |    u0/\w_reg[0][15] /D v | MET Setup Check with Pin
u0/\w_reg[0][15] /CP    |  0.547 |   2.232 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   288 |    u0/\w_reg[0][23] /D v | MET Setup Check with Pin
u0/\w_reg[0][23] /CP    |  0.548 |   2.234 |    2.782 | clk(D)(P) | clk(C)(P)
* |
     |   289 |   \text_out_reg[12] /D v | MET Setup Check with Pin
\text_out_reg[12] /CP   |  0.548 |   2.189 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   290 |  \text_out_reg[102] /D ^ | MET Setup Check with Pin
\text_out_reg[102] /CP  |  0.549 |   2.194 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   291 |   \text_out_reg[94] /D v | MET Setup Check with Pin
\text_out_reg[94] /CP   |  0.551 |   2.232 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   292 |   \text_out_reg[33] /D v | MET Setup Check with Pin
\text_out_reg[33] /CP   |  0.552 |   2.185 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   293 |    u0/\w_reg[0][18] /D v | MET Setup Check with Pin
u0/\w_reg[0][18] /CP    |  0.552 |   2.192 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   294 |  \text_out_reg[119] /D v | MET Setup Check with Pin
\text_out_reg[119] /CP  |  0.556 |   2.211 |    2.768 | clk(D)(P) | clk(C)(P)
* |
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```
     |   295 |   \text_out_reg[72] /D v | MET Setup Check with Pin
\text_out_reg[72] /CP   |  0.557 |   2.167 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   296 |   \text_out_reg[84] /D v | MET Setup Check with Pin
\text_out_reg[84] /CP   |  0.558 |   2.221 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   297 |   \text_out_reg[77] /D v | MET Setup Check with Pin
\text_out_reg[77] /CP   |  0.561 |   2.167 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   298 |   \text_out_reg[85] /D v | MET Setup Check with Pin
\text_out_reg[85] /CP   |  0.564 |   2.221 |    2.784 | clk(D)(P) | clk(C)(P)
* |
     |   299 |   \text_out_reg[34] /D v | MET Setup Check with Pin
\text_out_reg[34] /CP   |  0.565 |   2.171 |    2.736 | clk(D)(P) | clk(C)(P)
* |
     |   300 |   \text_out_reg[48] /D ^ | MET Setup Check with Pin
\text_out_reg[48] /CP   |  0.567 |   2.152 |    2.719 | clk(D)(P) | clk(C)(P)
* |
     |   301 |    \text_out_reg[8] /D ^ | MET Setup Check with Pin
\text_out_reg[8] /CP    |  0.569 |   2.142 |    2.711 | clk(D)(P) | clk(C)(P)
* |
     |   302 |  \text_out_reg[126] /D v | MET Setup Check with Pin
\text_out_reg[126] /CP  |  0.570 |   2.204 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   303 |  \text_out_reg[118] /D ^ | MET Setup Check with Pin
\text_out_reg[118] /CP  |  0.572 |   2.165 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   304 |   \text_out_reg[96] /D ^ | MET Setup Check with Pin
\text_out_reg[96] /CP   |  0.573 |   2.176 |    2.749 | clk(D)(P) | clk(C)(P)
* |
     |   305 |    \text_out_reg[7] /D v | MET Setup Check with Pin
\text_out_reg[7] /CP    |  0.573 |   2.126 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   306 |   \text_out_reg[73] /D v | MET Setup Check with Pin
\text_out_reg[73] /CP   |  0.575 |   2.150 |    2.725 | clk(D)(P) | clk(C)(P)
* |
     |   307 |  \text_out_reg[123] /D v | MET Setup Check with Pin
\text_out_reg[123] /CP  |  0.578 |   2.192 |    2.769 | clk(D)(P) | clk(C)(P)
* |
     |   308 |  \text_out_reg[100] /D v | MET Setup Check with Pin
\text_out_reg[100] /CP  |  0.579 |   2.200 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   309 |   \text_out_reg[92] /D v | MET Setup Check with Pin
\text_out_reg[92] /CP   |  0.580 |   2.203 |    2.783 | clk(D)(P) | clk(C)(P)
* |
     |   310 |  \text_out_reg[124] /D v | MET Setup Check with Pin
\text_out_reg[124] /CP  |  0.582 |   2.192 |    2.774 | clk(D)(P) | clk(C)(P)
* |
     |   311 |   \text_out_reg[39] /D v | MET Setup Check with Pin
\text_out_reg[39] /CP   |  0.583 |   2.159 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   312 |   \text_out_reg[24] /D v | MET Setup Check with Pin
\text_out_reg[24] /CP   |  0.583 |   2.128 |    2.712 | clk(D)(P) | clk(C)(P)
* |
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```
     |   313 |   \text_out_reg[95] /D ^ | MET Setup Check with Pin
\text_out_reg[95] /CP   |  0.584 |   2.177 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   314 |   \text_out_reg[21] /D v | MET Setup Check with Pin
\text_out_reg[21] /CP   |  0.588 |   2.155 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   315 |     u0/\w_reg[0][1] /D v | MET Setup Check with Pin
u0/\w_reg[0][1] /CP     |  0.592 |   2.186 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   316 |    u0/\w_reg[0][11] /D v | MET Setup Check with Pin
u0/\w_reg[0][11] /CP    |  0.593 |   2.188 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   317 |   \text_out_reg[98] /D v | MET Setup Check with Pin
\text_out_reg[98] /CP   |  0.593 |   2.180 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   318 |  \text_out_reg[110] /D v | MET Setup Check with Pin
\text_out_reg[110] /CP  |  0.593 |   2.164 |    2.757 | clk(D)(P) | clk(C)(P)
* |
     |   319 |   \text_out_reg[62] /D ^ | MET Setup Check with Pin
\text_out_reg[62] /CP   |  0.595 |   2.135 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |   320 |   \text_out_reg[61] /D ^ | MET Setup Check with Pin
\text_out_reg[61] /CP   |  0.596 |   2.134 |    2.729 | clk(D)(P) | clk(C)(P)
* |
     |   321 |   \text_out_reg[53] /D ^ | MET Setup Check with Pin
\text_out_reg[53] /CP   |  0.596 |   2.134 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |   322 |     u0/\w_reg[0][3] /D v | MET Setup Check with Pin
u0/\w_reg[0][3] /CP     |  0.597 |   2.181 |    2.778 | clk(D)(P) | clk(C)(P)
* |
     |   323 |   \text_out_reg[28] /D v | MET Setup Check with Pin
\text_out_reg[28] /CP   |  0.598 |   2.111 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   324 |   \text_out_reg[71] /D v | MET Setup Check with Pin
\text_out_reg[71] /CP   |  0.601 |   2.184 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   325 |    u0/\w_reg[0][22] /D v | MET Setup Check with Pin
u0/\w_reg[0][22] /CP    |  0.604 |   2.173 |    2.777 | clk(D)(P) | clk(C)(P)
* |
     |   326 |    \text_out_reg[6] /D v | MET Setup Check with Pin
\text_out_reg[6] /CP    |  0.605 |   2.094 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   327 |   \text_out_reg[76] /D v | MET Setup Check with Pin
\text_out_reg[76] /CP   |  0.608 |   2.114 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   328 |   \text_out_reg[20] /D v | MET Setup Check with Pin
\text_out_reg[20] /CP   |  0.609 |   2.128 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   329 |   \text_out_reg[74] /D v | MET Setup Check with Pin
\text_out_reg[74] /CP   |  0.609 |   2.119 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   330 |   \text_out_reg[50] /D v | MET Setup Check with Pin
\text_out_reg[50] /CP   |  0.610 |   2.131 |    2.741 | clk(D)(P) | clk(C)(P)
* |
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```
     |   331 |   \text_out_reg[31] /D v | MET Setup Check with Pin
\text_out_reg[31] /CP   |  0.610 |   2.096 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   332 |   \text_out_reg[38] /D v | MET Setup Check with Pin
\text_out_reg[38] /CP   |  0.612 |   2.132 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   333 |   \text_out_reg[68] /D ^ | MET Setup Check with Pin
\text_out_reg[68] /CP   |  0.612 |   2.155 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   334 |   \text_out_reg[63] /D v | MET Setup Check with Pin
\text_out_reg[63] /CP   |  0.612 |   2.132 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   335 |    \text_out_reg[4] /D v | MET Setup Check with Pin
\text_out_reg[4] /CP    |  0.614 |   2.077 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   336 |    \text_out_reg[3] /D v | MET Setup Check with Pin
\text_out_reg[3] /CP    |  0.614 |   2.087 |    2.701 | clk(D)(P) | clk(C)(P)
* |
     |   337 |   \text_out_reg[60] /D v | MET Setup Check with Pin
\text_out_reg[60] /CP   |  0.615 |   2.131 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   338 |   \text_out_reg[10] /D v | MET Setup Check with Pin
\text_out_reg[10] /CP   |  0.618 |   2.121 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   339 |  \text_out_reg[113] /D v | MET Setup Check with Pin
\text_out_reg[113] /CP  |  0.618 |   2.151 |    2.769 | clk(D)(P) | clk(C)(P)
* |
     |   340 |   \text_out_reg[67] /D v | MET Setup Check with Pin
\text_out_reg[67] /CP   |  0.620 |   2.165 |    2.784 | clk(D)(P) | clk(C)(P)
* |
     |   341 |  \text_out_reg[116] /D ^ | MET Setup Check with Pin
\text_out_reg[116] /CP  |  0.621 |   2.116 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   342 |   \text_out_reg[75] /D v | MET Setup Check with Pin
\text_out_reg[75] /CP   |  0.624 |   2.102 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   343 |    u0/\w_reg[0][16] /D v | MET Setup Check with Pin
u0/\w_reg[0][16] /CP    |  0.626 |   2.155 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   344 |   \text_out_reg[11] /D v | MET Setup Check with Pin
\text_out_reg[11] /CP   |  0.626 |   2.111 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   345 |   \text_out_reg[86] /D ^ | MET Setup Check with Pin
\text_out_reg[86] /CP   |  0.628 |   2.132 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   346 |   \text_out_reg[78] /D v | MET Setup Check with Pin
\text_out_reg[78] /CP   |  0.633 |   2.152 |    2.785 | clk(D)(P) | clk(C)(P)
* |
     |   347 |   \text_out_reg[45] /D v | MET Setup Check with Pin
\text_out_reg[45] /CP   |  0.636 |   2.109 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   348 |  \text_out_reg[105] /D v | MET Setup Check with Pin
\text_out_reg[105] /CP  |  0.636 |   2.130 |    2.767 | clk(D)(P) | clk(C)(P)
* |
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```
     |   349 |    \text_out_reg[1] /D v | MET Setup Check with Pin
\text_out_reg[1] /CP    |  0.640 |   2.069 |    2.709 | clk(D)(P) | clk(C)(P)
* |
     |   350 |     u0/\w_reg[0][0] /D ^ | MET Setup Check with Pin
u0/\w_reg[0][0] /CP     |  0.641 |   2.119 |    2.759 | clk(D)(P) | clk(C)(P)
* |
     |   351 |   \text_out_reg[99] /D v | MET Setup Check with Pin
\text_out_reg[99] /CP   |  0.641 |   2.132 |    2.773 | clk(D)(P) | clk(C)(P)
* |
     |   352 |     u0/\w_reg[0][4] /D v | MET Setup Check with Pin
u0/\w_reg[0][4] /CP     |  0.641 |   2.137 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   353 |   \text_out_reg[51] /D v | MET Setup Check with Pin
\text_out_reg[51] /CP   |  0.645 |   2.098 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   354 |   \text_out_reg[40] /D v | MET Setup Check with Pin
\text_out_reg[40] /CP   |  0.645 |   2.102 |    2.746 | clk(D)(P) | clk(C)(P)
* |
     |   355 |  \text_out_reg[114] /D v | MET Setup Check with Pin
\text_out_reg[114] /CP  |  0.648 |   2.117 |    2.765 | clk(D)(P) | clk(C)(P)
* |
     |   356 |    u0/\w_reg[0][20] /D v | MET Setup Check with Pin
u0/\w_reg[0][20] /CP    |  0.651 |   2.129 |    2.780 | clk(D)(P) | clk(C)(P)
* |
     |   357 |   \text_out_reg[18] /D v | MET Setup Check with Pin
\text_out_reg[18] /CP   |  0.651 |   2.061 |    2.713 | clk(D)(P) | clk(C)(P)
* |
     |   358 |   \text_out_reg[42] /D v | MET Setup Check with Pin
\text_out_reg[42] /CP   |  0.653 |   2.095 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   359 |    u0/\w_reg[0][17] /D v | MET Setup Check with Pin
u0/\w_reg[0][17] /CP    |  0.653 |   2.127 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   360 |   \text_out_reg[59] /D v | MET Setup Check with Pin
\text_out_reg[59] /CP   |  0.654 |   2.088 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   361 |   \text_out_reg[91] /D ^ | MET Setup Check with Pin
\text_out_reg[91] /CP   |  0.655 |   2.092 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   362 |   \text_out_reg[35] /D v | MET Setup Check with Pin
\text_out_reg[35] /CP   |  0.665 |   2.072 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   363 |   \text_out_reg[47] /D v | MET Setup Check with Pin
\text_out_reg[47] /CP   |  0.666 |   2.078 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   364 |   \text_out_reg[36] /D v | MET Setup Check with Pin
\text_out_reg[36] /CP   |  0.669 |   2.068 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   365 |    u0/\w_reg[0][19] /D v | MET Setup Check with Pin
u0/\w_reg[0][19] /CP    |  0.670 |   2.111 |    2.781 | clk(D)(P) | clk(C)(P)
* |
     |   366 |   \text_out_reg[80] /D v | MET Setup Check with Pin
\text_out_reg[80] /CP   |  0.670 |   2.091 |    2.761 | clk(D)(P) | clk(C)(P)
* |
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     |   367 |   \text_out_reg[22] /D v | MET Setup Check with Pin
\text_out_reg[22] /CP   |  0.675 |   2.067 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   368 |  \text_out_reg[112] /D v | MET Setup Check with Pin
\text_out_reg[112] /CP  |  0.679 |   2.089 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   369 |   \text_out_reg[27] /D v | MET Setup Check with Pin
\text_out_reg[27] /CP   |  0.679 |   2.032 |    2.711 | clk(D)(P) | clk(C)(P)
* |
     |   370 |  \text_out_reg[111] /D v | MET Setup Check with Pin
\text_out_reg[111] /CP  |  0.680 |   2.080 |    2.760 | clk(D)(P) | clk(C)(P)
* |
     |   371 |   \text_out_reg[55] /D ^ | MET Setup Check with Pin
\text_out_reg[55] /CP   |  0.680 |   2.053 |    2.733 | clk(D)(P) | clk(C)(P)
* |
     |   372 |   \text_out_reg[19] /D v | MET Setup Check with Pin
\text_out_reg[19] /CP   |  0.702 |   2.029 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   373 |   \text_out_reg[41] /D ^ | MET Setup Check with Pin
\text_out_reg[41] /CP   |  0.708 |   2.020 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   374 |   \text_out_reg[16] /D v | MET Setup Check with Pin
\text_out_reg[16] /CP   |  0.709 |   2.029 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   375 |   \text_out_reg[58] /D v | MET Setup Check with Pin
\text_out_reg[58] /CP   |  0.717 |   2.035 |    2.752 | clk(D)(P) | clk(C)(P)
* |
     |   376 |   \text_out_reg[46] /D v | MET Setup Check with Pin
\text_out_reg[46] /CP   |  0.729 |   2.016 |    2.745 | clk(D)(P) | clk(C)(P)
* |
     |   377 |   \text_out_reg[83] /D v | MET Setup Check with Pin
\text_out_reg[83] /CP   |  0.729 |   2.050 |    2.779 | clk(D)(P) | clk(C)(P)
* |
     |   378 |  \text_out_reg[106] /D v | MET Setup Check with Pin
\text_out_reg[106] /CP  |  0.730 |   2.033 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   379 |  \text_out_reg[115] /D v | MET Setup Check with Pin
\text_out_reg[115] /CP  |  0.735 |   2.033 |    2.768 | clk(D)(P) | clk(C)(P)
* |
     |   380 |  \text_out_reg[108] /D v | MET Setup Check with Pin
\text_out_reg[108] /CP  |  0.738 |   2.025 |    2.763 | clk(D)(P) | clk(C)(P)
* |
     |   381 |  \text_out_reg[104] /D v | MET Setup Check with Pin
\text_out_reg[104] /CP  |  0.741 |   2.020 |    2.762 | clk(D)(P) | clk(C)(P)
* |
     |   382 |   \text_out_reg[44] /D v | MET Setup Check with Pin
\text_out_reg[44] /CP   |  0.765 |   1.978 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   383 |   \text_out_reg[43] /D v | MET Setup Check with Pin
\text_out_reg[43] /CP   |  0.789 |   1.958 |    2.747 | clk(D)(P) | clk(C)(P)
* |
     |   384 |  \text_out_reg[107] /D v | MET Setup Check with Pin
\text_out_reg[107] /CP  |  0.835 |   1.930 |    2.764 | clk(D)(P) | clk(C)(P)
* |
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     |   385 |  u0/r0/\out_reg[31] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[31] /CP  |  0.927 |   1.797 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   386 |  u0/r0/\out_reg[30] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[30] /CP  |  0.950 |   1.792 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   387 |  u0/r0/\out_reg[27] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[27] /CP  |  0.952 |   1.792 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   388 |  u0/r0/\out_reg[28] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[28] /CP  |  0.957 |   1.793 |    2.750 | clk(D)(P) | clk(C)(P)
* |
     |   389 |  u0/r0/\out_reg[26] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[26] /CP  |  0.958 |   1.795 |    2.753 | clk(D)(P) | clk(C)(P)
* |
     |   390 |  u0/r0/\out_reg[25] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[25] /CP  |  0.968 |   1.775 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   391 |  u0/r0/\rcnt_reg[3] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[3] /CP  |  0.971 |   1.780 |    2.751 | clk(D)(P) | clk(C)(P)
* |
     |   392 |  u0/r0/\out_reg[29] /D ^ | MET Setup Check with Pin
u0/r0/\out_reg[29] /CP  |  0.981 |   1.758 |    2.739 | clk(D)(P) | clk(C)(P)
* |
     |   393 |  u0/r0/\rcnt_reg[1] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[1] /CP  |  1.057 |   1.673 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   394 |  u0/r0/\rcnt_reg[2] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[2] /CP  |  1.061 |   1.671 |    2.731 | clk(D)(P) | clk(C)(P)
* |
     |   395 |  u0/r0/\out_reg[24] /D v | MET Setup Check with Pin
u0/r0/\out_reg[24] /CP  |  1.066 |   1.709 |    2.775 | clk(D)(P) | clk(C)(P)
* |
     |   396 |  u0/r0/\rcnt_reg[0] /D ^ | MET Setup Check with Pin
u0/r0/\rcnt_reg[0] /CP  |  1.069 |   1.664 |    2.734 | clk(D)(P) | clk(C)(P)
* |
     |   397 |           text_out[74] ^ | MET Late External Delay Assertion
|  1.415 |   0.685 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   398 |        \dcnt_reg[1] /D v | MET Setup Check with Pin
\dcnt_reg[1] /CP        |  1.435 |   1.307 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   399 |           text_out[73] ^ | MET Late External Delay Assertion
|  1.457 |   0.643 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   400 |              done_reg/D ^ | MET Setup Check with Pin
done_reg/CP             |  1.467 |   1.250 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   401 |           text_out[81] ^ | MET Late External Delay Assertion
|  1.472 |   0.628 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   402 |           text_out[72] ^ | MET Late External Delay Assertion
|  1.489 |   0.611 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   403 |        \dcnt_reg[3] /D v | MET Setup Check with Pin
\dcnt_reg[3] /CP        |  1.491 |   1.255 |    2.746 | clk(D)(P) | clk(C)(P)
* |
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     |   404 |          text_out[109] ^ | MET Late External Delay Assertion
|  1.494 |   0.606 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   405 |           text_out[84] ^ | MET Late External Delay Assertion
|  1.518 |   0.582 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   406 |  \text_in_r_reg[52] /E v | MET Setup Check with Pin
\text_in_r_reg[52] /CP  |  1.522 |   1.091 |    2.613 | clk(D)(P) | clk(C)(P)
* |
     |   407 |          text_out[106] ^ | MET Late External Delay Assertion
|  1.524 |   0.576 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   408 |           text_out[65] ^ | MET Late External Delay Assertion
|  1.524 |   0.576 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   409 |           text_out[71] ^ | MET Late External Delay Assertion
|  1.525 |   0.575 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   410 |  \text_in_r_reg[54] /E v | MET Setup Check with Pin
\text_in_r_reg[54] /CP  |  1.530 |   1.091 |    2.621 | clk(D)(P) | clk(C)(P)
* |
     |   411 |  \text_in_r_reg[55] /E v | MET Setup Check with Pin
\text_in_r_reg[55] /CP  |  1.530 |   1.091 |    2.621 | clk(D)(P) | clk(C)(P)
* |
     |   412 |           text_out[93] ^ | MET Late External Delay Assertion
|  1.530 |   0.570 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   413 |          text_out[112] ^ | MET Late External Delay Assertion
|  1.530 |   0.569 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   414 |  \text_in_r_reg[53] /E v | MET Setup Check with Pin
\text_in_r_reg[53] /CP  |  1.534 |   1.093 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   415 |           text_out[70] ^ | MET Late External Delay Assertion
|  1.536 |   0.564 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   416 |           text_out[80] ^ | MET Late External Delay Assertion
|  1.536 |   0.564 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   417 |  \text_in_r_reg[59] /E v | MET Setup Check with Pin
\text_in_r_reg[59] /CP  |  1.536 |   1.095 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   418 |  \text_in_r_reg[60] /E v | MET Setup Check with Pin
\text_in_r_reg[60] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   419 |  \text_in_r_reg[62] /E v | MET Setup Check with Pin
\text_in_r_reg[62] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   420 |  \text_in_r_reg[61] /E v | MET Setup Check with Pin
\text_in_r_reg[61] /CP  |  1.537 |   1.094 |    2.631 | clk(D)(P) | clk(C)(P)
* |
     |   421 |  \text_in_r_reg[63] /E v | MET Setup Check with Pin
\text_in_r_reg[63] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   422 |  \text_in_r_reg[56] /E v | MET Setup Check with Pin
\text_in_r_reg[56] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   423 |  \text_in_r_reg[57] /E v | MET Setup Check with Pin
\text_in_r_reg[57] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
     |   424 |  \text_in_r_reg[58] /E v | MET Setup Check with Pin
\text_in_r_reg[58] /CP  |  1.537 |   1.095 |    2.632 | clk(D)(P) | clk(C)(P)
* |
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     |   425 |           text_out[68] ^ | MET Late External Delay Assertion
|  1.538 |   0.562 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   426 |        \dcnt_reg[0] /D v | MET Setup Check with Pin
\dcnt_reg[0] /CP        |  1.540 |   1.200 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   427 |           text_out[89] ^ | MET Late External Delay Assertion
|  1.544 |   0.556 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   428 |  \text_in_r_reg[97] /E v | MET Setup Check with Pin
\text_in_r_reg[97] /CP  |  1.545 |   1.083 |    2.628 | clk(D)(P) | clk(C)(P)
* |
     |   429 |  \text_in_r_reg[67] /E v | MET Setup Check with Pin
\text_in_r_reg[67] /CP  |  1.545 |   1.083 |    2.628 | clk(D)(P) | clk(C)(P)
* |
     |   430 |           text_out[64] ^ | MET Late External Delay Assertion
|  1.547 |   0.553 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   431 |           text_out[85] ^ | MET Late External Delay Assertion
|  1.548 |   0.552 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   432 |  \text_in_r_reg[70] /E v | MET Setup Check with Pin
\text_in_r_reg[70] /CP  |  1.553 |   1.085 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   433 |  \text_in_r_reg[69] /E v | MET Setup Check with Pin
\text_in_r_reg[69] /CP  |  1.553 |   1.084 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   434 |  \text_in_r_reg[79] /E v | MET Setup Check with Pin
\text_in_r_reg[79] /CP  |  1.554 |   1.066 |    2.620 | clk(D)(P) | clk(C)(P)
* |
     |   435 |  \text_in_r_reg[76] /E v | MET Setup Check with Pin
\text_in_r_reg[76] /CP  |  1.554 |   1.066 |    2.620 | clk(D)(P) | clk(C)(P)
* |
     |   436 |  \text_in_r_reg[68] /E v | MET Setup Check with Pin
\text_in_r_reg[68] /CP  |  1.556 |   1.082 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   437 |           text_out[92] ^ | MET Late External Delay Assertion
|  1.556 |   0.544 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   438 |  \text_in_r_reg[72] /E v | MET Setup Check with Pin
\text_in_r_reg[72] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   439 |  \text_in_r_reg[78] /E v | MET Setup Check with Pin
\text_in_r_reg[78] /CP  |  1.557 |   1.066 |    2.623 | clk(D)(P) | clk(C)(P)
* |
     |   440 |  \text_in_r_reg[65] /E v | MET Setup Check with Pin
\text_in_r_reg[65] /CP  |  1.557 |   1.081 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   441 |  \text_in_r_reg[74] /E v | MET Setup Check with Pin
\text_in_r_reg[74] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   442 |  \text_in_r_reg[82] /E v | MET Setup Check with Pin
\text_in_r_reg[82] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
     |   443 |  \text_in_r_reg[75] /E v | MET Setup Check with Pin
\text_in_r_reg[75] /CP  |  1.557 |   1.066 |    2.622 | clk(D)(P) | clk(C)(P)
* |
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```
     |   444 |  \text_in_r_reg[77] /E v | MET Setup Check with Pin
\text_in_r_reg[77] /CP  |  1.557 |   1.066 |    2.623 | clk(D)(P) | clk(C)(P)
* |
     |   445 |  \text_in_r_reg[64] /E v | MET Setup Check with Pin
\text_in_r_reg[64] /CP  |  1.559 |   1.079 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   446 | \text_in_r_reg[109] /E v | MET Setup Check with Pin
\text_in_r_reg[109] /CP |  1.559 |   1.079 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   447 |  \text_in_r_reg[66] /E v | MET Setup Check with Pin
\text_in_r_reg[66] /CP  |  1.559 |   1.081 |    2.640 | clk(D)(P) | clk(C)(P)
* |
     |   448 |          text_out[107] ^ | MET Late External Delay Assertion
|  1.559 |   0.540 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   449 |          text_out[115] ^ | MET Late External Delay Assertion
|  1.560 |   0.540 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   450 | \text_in_r_reg[107] /E v | MET Setup Check with Pin
\text_in_r_reg[107] /CP |  1.560 |   1.079 |    2.639 | clk(D)(P) | clk(C)(P)
* |
     |   451 | \text_in_r_reg[110] /E v | MET Setup Check with Pin
\text_in_r_reg[110] /CP |  1.561 |   1.079 |    2.640 | clk(D)(P) | clk(C)(P)
* |
     |   452 | \text_in_r_reg[115] /E v | MET Setup Check with Pin
\text_in_r_reg[115] /CP |  1.561 |   1.074 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   453 |  \text_in_r_reg[30] /E v | MET Setup Check with Pin
\text_in_r_reg[30] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   454 | \text_in_r_reg[105] /E v | MET Setup Check with Pin
\text_in_r_reg[105] /CP |  1.562 |   1.079 |    2.641 | clk(D)(P) | clk(C)(P)
* |
     |   455 | \text_in_r_reg[111] /E v | MET Setup Check with Pin
\text_in_r_reg[111] /CP |  1.562 |   1.081 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   456 |  \text_in_r_reg[24] /E v | MET Setup Check with Pin
\text_in_r_reg[24] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   457 |  \text_in_r_reg[26] /E v | MET Setup Check with Pin
\text_in_r_reg[26] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   458 |  \text_in_r_reg[28] /E v | MET Setup Check with Pin
\text_in_r_reg[28] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   459 |  \text_in_r_reg[27] /E v | MET Setup Check with Pin
\text_in_r_reg[27] /CP  |  1.562 |   1.055 |    2.617 | clk(D)(P) | clk(C)(P)
* |
     |   460 |  \text_in_r_reg[31] /E v | MET Setup Check with Pin
\text_in_r_reg[31] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   461 |  \text_in_r_reg[29] /E v | MET Setup Check with Pin
\text_in_r_reg[29] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
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```
     |   462 | \text_in_r_reg[104] /E v | MET Setup Check with Pin
\text_in_r_reg[104] /CP |  1.563 |   1.079 |    2.642 | clk(D)(P) | clk(C)(P)
* |
     |   463 | \text_in_r_reg[108] /E v | MET Setup Check with Pin
\text_in_r_reg[108] /CP |  1.563 |   1.079 |    2.642 | clk(D)(P) | clk(C)(P)
* |
     |   464 |  \text_in_r_reg[23] /E v | MET Setup Check with Pin
\text_in_r_reg[23] /CP  |  1.563 |   1.055 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   465 |  \text_in_r_reg[18] /E v | MET Setup Check with Pin
\text_in_r_reg[18] /CP  |  1.563 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   466 |  \text_in_r_reg[19] /E v | MET Setup Check with Pin
\text_in_r_reg[19] /CP  |  1.564 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   467 |  \text_in_r_reg[25] /E v | MET Setup Check with Pin
\text_in_r_reg[25] /CP  |  1.564 |   1.054 |    2.618 | clk(D)(P) | clk(C)(P)
* |
     |   468 | \text_in_r_reg[106] /E v | MET Setup Check with Pin
\text_in_r_reg[106] /CP |  1.564 |   1.079 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   469 | \text_in_r_reg[114] /E v | MET Setup Check with Pin
\text_in_r_reg[114] /CP |  1.564 |   1.074 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   470 |           text_out[69] ^ | MET Late External Delay Assertion
|  1.565 |   0.535 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   471 | \text_in_r_reg[113] /E v | MET Setup Check with Pin
\text_in_r_reg[113] /CP |  1.565 |   1.073 |    2.638 | clk(D)(P) | clk(C)(P)
* |
     |   472 |  \text_in_r_reg[20] /E v | MET Setup Check with Pin
\text_in_r_reg[20] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   473 |  \text_in_r_reg[21] /E v | MET Setup Check with Pin
\text_in_r_reg[21] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   474 |  \text_in_r_reg[22] /E v | MET Setup Check with Pin
\text_in_r_reg[22] /CP  |  1.566 |   1.053 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   475 |  \text_in_r_reg[16] /E v | MET Setup Check with Pin
\text_in_r_reg[16] /CP  |  1.567 |   1.052 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   476 |  \text_in_r_reg[17] /E v | MET Setup Check with Pin
\text_in_r_reg[17] /CP  |  1.567 |   1.052 |    2.619 | clk(D)(P) | clk(C)(P)
* |
     |   477 | \text_in_r_reg[102] /E v | MET Setup Check with Pin
\text_in_r_reg[102] /CP |  1.567 |   1.085 |    2.652 | clk(D)(P) | clk(C)(P)
* |
     |   478 | \text_in_r_reg[103] /E v | MET Setup Check with Pin
\text_in_r_reg[103] /CP |  1.567 |   1.085 |    2.652 | clk(D)(P) | clk(C)(P)
* |
     |   479 | \text_in_r_reg[100] /E v | MET Setup Check with Pin
\text_in_r_reg[100] /CP |  1.567 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
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```
     |   480 | \text_in_r_reg[101] /E v | MET Setup Check with Pin
\text_in_r_reg[101] /CP |  1.567 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   481 | \text_in_r_reg[123] /E v | MET Setup Check with Pin
\text_in_r_reg[123] /CP |  1.567 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   482 | \text_in_r_reg[122] /E v | MET Setup Check with Pin
\text_in_r_reg[122] /CP |  1.567 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   483 |        \dcnt_reg[2] /D ^ | MET Setup Check with Pin
\dcnt_reg[2] /CP        |  1.567 |   1.152 |    2.720 | clk(D)(P) | clk(C)(P)
* |
     |   484 |  \text_in_r_reg[98] /E v | MET Setup Check with Pin
\text_in_r_reg[98] /CP  |  1.568 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   485 | \text_in_r_reg[127] /E v | MET Setup Check with Pin
\text_in_r_reg[127] /CP |  1.568 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   486 | \text_in_r_reg[121] /E v | MET Setup Check with Pin
\text_in_r_reg[121] /CP |  1.568 |   1.079 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   487 |  \text_in_r_reg[96] /E v | MET Setup Check with Pin
\text_in_r_reg[96] /CP  |  1.568 |   1.086 |    2.653 | clk(D)(P) | clk(C)(P)
* |
     |   488 |  \text_in_r_reg[99] /E v | MET Setup Check with Pin
\text_in_r_reg[99] /CP  |  1.568 |   1.086 |    2.654 | clk(D)(P) | clk(C)(P)
* |
     |   489 |           text_out[78] ^ | MET Late External Delay Assertion
|  1.569 |   0.531 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   490 |  \text_in_r_reg[51] /E v | MET Setup Check with Pin
\text_in_r_reg[51] /CP  |  1.569 |   1.058 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   491 |  \text_in_r_reg[49] /E v | MET Setup Check with Pin
\text_in_r_reg[49] /CP  |  1.570 |   1.058 |    2.627 | clk(D)(P) | clk(C)(P)
* |
     |   492 | \text_in_r_reg[126] /E v | MET Setup Check with Pin
\text_in_r_reg[126] /CP |  1.571 |   1.079 |    2.650 | clk(D)(P) | clk(C)(P)
* |
     |   493 |  \text_in_r_reg[45] /E v | MET Setup Check with Pin
\text_in_r_reg[45] /CP  |  1.571 |   1.058 |    2.629 | clk(D)(P) | clk(C)(P)
* |
     |   494 | \text_in_r_reg[120] /E v | MET Setup Check with Pin
\text_in_r_reg[120] /CP |  1.572 |   1.079 |    2.651 | clk(D)(P) | clk(C)(P)
* |
     |   495 |  \text_in_r_reg[95] /E v | MET Setup Check with Pin
\text_in_r_reg[95] /CP  |  1.572 |   1.083 |    2.655 | clk(D)(P) | clk(C)(P)
* |
     |   496 | \text_in_r_reg[116] /E v | MET Setup Check with Pin
\text_in_r_reg[116] /CP |  1.572 |   1.075 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   497 | \text_in_r_reg[124] /E v | MET Setup Check with Pin
\text_in_r_reg[124] /CP |  1.572 |   1.079 |    2.651 | clk(D)(P) | clk(C)(P)
* |
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     |   498 | \text_in_r_reg[112] /E v | MET Setup Check with Pin
\text_in_r_reg[112] /CP |  1.572 |   1.074 |    2.647 | clk(D)(P) | clk(C)(P)
* |
     |   499 |  \text_in_r_reg[94] /E v | MET Setup Check with Pin
\text_in_r_reg[94] /CP  |  1.573 |   1.083 |    2.656 | clk(D)(P) | clk(C)(P)
* |
     |   500 |  \text_in_r_reg[93] /E v | MET Setup Check with Pin
\text_in_r_reg[93] /CP  |  1.574 |   1.083 |    2.657 | clk(D)(P) | clk(C)(P)
* |
     |   501 |  \text_in_r_reg[44] /E v | MET Setup Check with Pin
\text_in_r_reg[44] /CP  |  1.575 |   1.058 |    2.633 | clk(D)(P) | clk(C)(P)
* |
     |   502 |  \text_in_r_reg[92] /E v | MET Setup Check with Pin
\text_in_r_reg[92] /CP  |  1.576 |   1.082 |    2.658 | clk(D)(P) | clk(C)(P)
* |
     |   503 |  \text_in_r_reg[43] /E v | MET Setup Check with Pin
\text_in_r_reg[43] /CP  |  1.576 |   1.058 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   504 |          text_out[123] ^ | MET Late External Delay Assertion
|  1.576 |   0.524 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   505 |  \text_in_r_reg[47] /E v | MET Setup Check with Pin
\text_in_r_reg[47] /CP  |  1.577 |   1.058 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   506 |  \text_in_r_reg[91] /E v | MET Setup Check with Pin
\text_in_r_reg[91] /CP  |  1.577 |   1.082 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   507 | \text_in_r_reg[125] /E v | MET Setup Check with Pin
\text_in_r_reg[125] /CP |  1.577 |   1.078 |    2.655 | clk(D)(P) | clk(C)(P)
* |
     |   508 |  \text_in_r_reg[46] /E v | MET Setup Check with Pin
\text_in_r_reg[46] /CP  |  1.577 |   1.058 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   509 |  \text_in_r_reg[48] /E v | MET Setup Check with Pin
\text_in_r_reg[48] /CP  |  1.577 |   1.057 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   510 | \text_in_r_reg[119] /E v | MET Setup Check with Pin
\text_in_r_reg[119] /CP |  1.578 |   1.078 |    2.656 | clk(D)(P) | clk(C)(P)
* |
     |   511 |           text_out[86] ^ | MET Late External Delay Assertion
|  1.579 |   0.521 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   512 |  \text_in_r_reg[71] /E v | MET Setup Check with Pin
\text_in_r_reg[71] /CP  |  1.580 |   1.068 |    2.648 | clk(D)(P) | clk(C)(P)
* |
     |   513 |  \text_in_r_reg[80] /E v | MET Setup Check with Pin
\text_in_r_reg[80] /CP  |  1.580 |   1.068 |    2.648 | clk(D)(P) | clk(C)(P)
* |
     |   514 |  \text_in_r_reg[15] /E v | MET Setup Check with Pin
\text_in_r_reg[15] /CP  |  1.580 |   1.054 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   515 |  \text_in_r_reg[12] /E v | MET Setup Check with Pin
\text_in_r_reg[12] /CP  |  1.580 |   1.054 |    2.634 | clk(D)(P) | clk(C)(P)
* |
     |   516 |           text_out[36] ^ | MET Late External Delay Assertion
|  1.580 |   0.520 |    2.100 | clk(D)(P) | clk(C)(P) * |
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     |   517 |           text_out[95] v | MET Late External Delay Assertion
|  1.582 |   0.518 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   518 | \text_in_r_reg[118] /E v | MET Setup Check with Pin
\text_in_r_reg[118] /CP |  1.582 |   1.077 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   519 |          text_out[120] ^ | MET Late External Delay Assertion
|  1.583 |   0.517 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   520 | \text_in_r_reg[117] /E v | MET Setup Check with Pin
\text_in_r_reg[117] /CP |  1.583 |   1.077 |    2.659 | clk(D)(P) | clk(C)(P)
* |
     |   521 |          text_out[110] ^ | MET Late External Delay Assertion
|  1.583 |   0.517 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   522 |  \text_in_r_reg[36] /E v | MET Setup Check with Pin
\text_in_r_reg[36] /CP  |  1.584 |   1.059 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   523 |  \text_in_r_reg[13] /E v | MET Setup Check with Pin
\text_in_r_reg[13] /CP  |  1.584 |   1.051 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   524 |  \text_in_r_reg[14] /E v | MET Setup Check with Pin
\text_in_r_reg[14] /CP  |  1.584 |   1.051 |    2.635 | clk(D)(P) | clk(C)(P)
* |
     |   525 |  \text_in_r_reg[39] /E v | MET Setup Check with Pin
\text_in_r_reg[39] /CP  |  1.584 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   526 |  \text_in_r_reg[32] /E v | MET Setup Check with Pin
\text_in_r_reg[32] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   527 |  \text_in_r_reg[37] /E v | MET Setup Check with Pin
\text_in_r_reg[37] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   528 |  \text_in_r_reg[33] /E v | MET Setup Check with Pin
\text_in_r_reg[33] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   529 |  \text_in_r_reg[41] /E v | MET Setup Check with Pin
\text_in_r_reg[41] /CP  |  1.584 |   1.059 |    2.643 | clk(D)(P) | clk(C)(P)
* |
     |   530 |  \text_in_r_reg[34] /E v | MET Setup Check with Pin
\text_in_r_reg[34] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   531 |  \text_in_r_reg[38] /E v | MET Setup Check with Pin
\text_in_r_reg[38] /CP  |  1.584 |   1.060 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   532 |  \text_in_r_reg[35] /E v | MET Setup Check with Pin
\text_in_r_reg[35] /CP  |  1.584 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   533 |  \text_in_r_reg[40] /E v | MET Setup Check with Pin
\text_in_r_reg[40] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   534 |  \text_in_r_reg[42] /E v | MET Setup Check with Pin
\text_in_r_reg[42] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
     |   535 |  \text_in_r_reg[50] /E v | MET Setup Check with Pin
\text_in_r_reg[50] /CP  |  1.585 |   1.059 |    2.644 | clk(D)(P) | clk(C)(P)
* |
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     |   536 |          text_out[105] ^ | MET Late External Delay Assertion
|  1.585 |   0.515 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   537 |          text_out[122] ^ | MET Late External Delay Assertion
|  1.585 |   0.515 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   538 |          text_out[113] ^ | MET Late External Delay Assertion
|  1.586 |   0.514 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   539 |          text_out[114] ^ | MET Late External Delay Assertion
|  1.587 |   0.513 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   540 |  \text_in_r_reg[73] /E v | MET Setup Check with Pin
\text_in_r_reg[73] /CP  |  1.587 |   1.063 |    2.650 | clk(D)(P) | clk(C)(P)
* |
     |   541 |          text_out[104] ^ | MET Late External Delay Assertion
|  1.591 |   0.508 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   542 |           text_out[88] v | MET Late External Delay Assertion
|  1.592 |   0.508 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   543 |           text_out[67] v | MET Late External Delay Assertion
|  1.593 |   0.507 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   544 |           text_out[83] v | MET Late External Delay Assertion
|  1.593 |   0.507 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   545 |           text_out[53] ^ | MET Late External Delay Assertion
|  1.594 |   0.506 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   546 |           text_out[54] ^ | MET Late External Delay Assertion
|  1.595 |   0.505 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   547 |          text_out[111] v | MET Late External Delay Assertion
|  1.595 |   0.505 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   548 |  \text_in_r_reg[85] /E v | MET Setup Check with Pin
\text_in_r_reg[85] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   549 |  \text_in_r_reg[86] /E v | MET Setup Check with Pin
\text_in_r_reg[86] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   550 |  \text_in_r_reg[87] /E v | MET Setup Check with Pin
\text_in_r_reg[87] /CP  |  1.596 |   1.068 |    2.664 | clk(D)(P) | clk(C)(P)
* |
     |   551 |  \text_in_r_reg[84] /E v | MET Setup Check with Pin
\text_in_r_reg[84] /CP  |  1.598 |   1.068 |    2.665 | clk(D)(P) | clk(C)(P)
* |
     |   552 |  \text_in_r_reg[83] /E v | MET Setup Check with Pin
\text_in_r_reg[83] /CP  |  1.599 |   1.067 |    2.666 | clk(D)(P) | clk(C)(P)
* |
     |   553 |          text_out[108] v | MET Late External Delay Assertion
|  1.600 |   0.500 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   554 |  \text_in_r_reg[90] /E v | MET Setup Check with Pin
\text_in_r_reg[90] /CP  |  1.600 |   1.067 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   555 |  \text_in_r_reg[88] /E v | MET Setup Check with Pin
\text_in_r_reg[88] /CP  |  1.600 |   1.067 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   556 |  \text_in_r_reg[81] /E v | MET Setup Check with Pin
\text_in_r_reg[81] /CP  |  1.601 |   1.066 |    2.667 | clk(D)(P) | clk(C)(P)
* |
     |   557 |  \text_in_r_reg[89] /E v | MET Setup Check with Pin
\text_in_r_reg[89] /CP  |  1.601 |   1.066 |    2.667 | clk(D)(P) | clk(C)(P)
* |
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     |   558 |          text_out[119] v | MET Late External Delay Assertion
|  1.603 |   0.497 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   559 |                   done ^ | MET Late External Delay Assertion
|  1.603 |   0.497 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   560 |          text_out[127] v | MET Late External Delay Assertion
|  1.605 |   0.495 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   561 |           text_out[44] ^ | MET Late External Delay Assertion
|  1.606 |   0.494 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   562 |          text_out[116] v | MET Late External Delay Assertion
|  1.606 |   0.494 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   563 |           text_out[66] v | MET Late External Delay Assertion
|  1.607 |   0.493 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   564 |           text_out[34] ^ | MET Late External Delay Assertion
|  1.608 |   0.492 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   565 |           text_out[94] v | MET Late External Delay Assertion
|  1.608 |   0.492 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   566 |          text_out[121] v | MET Late External Delay Assertion
|  1.610 |   0.490 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   567 |           text_out[35] ^ | MET Late External Delay Assertion
|  1.611 |   0.489 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   568 |          text_out[125] v | MET Late External Delay Assertion
|  1.611 |   0.489 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   569 |           text_out[43] ^ | MET Late External Delay Assertion
|  1.615 |   0.485 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   570 |          text_out[126] v | MET Late External Delay Assertion
|  1.616 |   0.484 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   571 |          text_out[124] v | MET Late External Delay Assertion
|  1.619 |   0.481 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   572 |           text_out[75] ^ | MET Late External Delay Assertion
|  1.626 |   0.474 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   573 |          text_out[100] v | MET Late External Delay Assertion
|  1.628 |   0.472 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   574 |           text_out[98] v | MET Late External Delay Assertion
|  1.629 |   0.470 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   575 |           text_out[47] v | MET Late External Delay Assertion
|  1.631 |   0.469 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   576 |           text_out[82] v | MET Late External Delay Assertion
|  1.632 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   577 |           text_out[21] v | MET Late External Delay Assertion
|  1.633 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   578 |           text_out[99] v | MET Late External Delay Assertion
|  1.633 |   0.467 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   579 |           text_out[77] ^ | MET Late External Delay Assertion
|  1.634 |   0.466 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   580 |           text_out[46] v | MET Late External Delay Assertion
|  1.635 |   0.465 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   581 |           text_out[39] v | MET Late External Delay Assertion
|  1.635 |   0.465 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   582 |          text_out[118] v | MET Late External Delay Assertion
|  1.636 |   0.464 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   583 |           text_out[20] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   584 |          text_out[102] v | MET Late External Delay Assertion
|  1.637 |   0.463 |    2.100 | clk(D)(P) | clk(C)(P) * |
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	585	text_out[76] v	MET Late External Delay Assertion
1.637	0.463	2.100	clk(D)(P)	clk(C)(P) *
	586	text_out[37] v	MET Late External Delay Assertion
1.637	0.463	2.100	clk(D)(P)	clk(C)(P) *
	587	text_out[101] v	MET Late External Delay Assertion
1.637	0.463	2.100	clk(D)(P)	clk(C)(P) *
	588	text_out[96] v	MET Late External Delay Assertion
1.638	0.462	2.100	clk(D)(P)	clk(C)(P) *
	589	text_out[87] v	MET Late External Delay Assertion
1.638	0.462	2.100	clk(D)(P)	clk(C)(P) *
	590	text_out[90] v	MET Late External Delay Assertion
1.639	0.461	2.100	clk(D)(P)	clk(C)(P) *
	591	text_out[91] v	MET Late External Delay Assertion
1.639	0.461	2.100	clk(D)(P)	clk(C)(P) *
	592	text_out[79] v	MET Late External Delay Assertion
1.640	0.460	2.100	clk(D)(P)	clk(C)(P) *
	593	text_out[103] v	MET Late External Delay Assertion
1.642	0.458	2.100	clk(D)(P)	clk(C)(P) *
	594	text_out[45] v	MET Late External Delay Assertion
1.643	0.457	2.100	clk(D)(P)	clk(C)(P) *
	595	text_out[117] v	MET Late External Delay Assertion
1.643	0.457	2.100	clk(D)(P)	clk(C)(P) *
	596	text_out[97] v	MET Late External Delay Assertion
1.643	0.457	2.100	clk(D)(P)	clk(C)(P) *
	597	text_out[22] v	MET Late External Delay Assertion
1.645	0.455	2.100	clk(D)(P)	clk(C)(P) *
	598	text_out[42] v	MET Late External Delay Assertion
1.658	0.442	2.100	clk(D)(P)	clk(C)(P) *
	599	text_out[40] v	MET Late External Delay Assertion
1.662	0.438	2.100	clk(D)(P)	clk(C)(P) *
	600	text_out[48] v	MET Late External Delay Assertion
1.663	0.437	2.100	clk(D)(P)	clk(C)(P) *
	601	text_out[41] v	MET Late External Delay Assertion
1.663	0.436	2.100	clk(D)(P)	clk(C)(P) *
	602	text_out[57] v	MET Late External Delay Assertion
1.664	0.436	2.100	clk(D)(P)	clk(C)(P) *
	603	text_out[49] v	MET Late External Delay Assertion
1.664	0.436	2.100	clk(D)(P)	clk(C)(P) *
	604	text_out[52] v	MET Late External Delay Assertion
1.664	0.436	2.100	clk(D)(P)	clk(C)(P) *
	605	text_out[63] v	MET Late External Delay Assertion
1.665	0.435	2.100	clk(D)(P)	clk(C)(P) *
	606	text_out[12] v	MET Late External Delay Assertion
1.665	0.435	2.100	clk(D)(P)	clk(C)(P) *
	607	text_out[23] v	MET Late External Delay Assertion
1.666	0.434	2.100	clk(D)(P)	clk(C)(P) *
	608	text_out[33] v	MET Late External Delay Assertion
1.666	0.434	2.100	clk(D)(P)	clk(C)(P) *
	609	text_out[56] v	MET Late External Delay Assertion
1.668	0.432	2.100	clk(D)(P)	clk(C)(P) *
	610	text_out[62] v	MET Late External Delay Assertion
1.668	0.432	2.100	clk(D)(P)	clk(C)(P) *
	611	text_out[50] v	MET Late External Delay Assertion
1.669	0.431	2.100	clk(D)(P)	clk(C)(P) *

	612	text_out[59] v	MET Late External Delay Assertion
1.669	0.431	2.100	clk(D)(P)	clk(C)(P) *
	613	text_out[61] v	MET Late External Delay Assertion
1.669	0.431	2.100	clk(D)(P)	clk(C)(P) *
	614	text_out[32] v	MET Late External Delay Assertion
1.669	0.431	2.100	clk(D)(P)	clk(C)(P) *
	615	text_out[58] v	MET Late External Delay Assertion
1.670	0.430	2.100	clk(D)(P)	clk(C)(P) *
	616	text_out[51] v	MET Late External Delay Assertion
1.670	0.430	2.100	clk(D)(P)	clk(C)(P) *
	617	text_out[55] v	MET Late External Delay Assertion
1.670	0.430	2.100	clk(D)(P)	clk(C)(P) *
	618	text_out[38] v	MET Late External Delay Assertion
1.671	0.429	2.100	clk(D)(P)	clk(C)(P) *
	619	text_out[60] v	MET Late External Delay Assertion
1.671	0.429	2.100	clk(D)(P)	clk(C)(P) *
	620	text_out[15] v	MET Late External Delay Assertion
1.673	0.427	2.100	clk(D)(P)	clk(C)(P) *
	621	text_out[16] v	MET Late External Delay Assertion
1.675	0.425	2.100	clk(D)(P)	clk(C)(P) *
	622	text_out[10] v	MET Late External Delay Assertion
1.675	0.425	2.100	clk(D)(P)	clk(C)(P) *
	623	text_out[29] v	MET Late External Delay Assertion
1.675	0.425	2.100	clk(D)(P)	clk(C)(P) *
	624	text_out[19] v	MET Late External Delay Assertion
1.679	0.421	2.100	clk(D)(P)	clk(C)(P) *
	625	text_out[13] v	MET Late External Delay Assertion
1.681	0.419	2.100	clk(D)(P)	clk(C)(P) *
	626	text_out[17] v	MET Late External Delay Assertion
1.681	0.419	2.100	clk(D)(P)	clk(C)(P) *
	627	text_out[14] v	MET Late External Delay Assertion
1.682	0.418	2.100	clk(D)(P)	clk(C)(P) *
	628	text_out[11] v	MET Late External Delay Assertion
1.682	0.418	2.100	clk(D)(P)	clk(C)(P) *
	629	text_out[8] v	MET Late External Delay Assertion
1.684	0.416	2.100	clk(D)(P)	clk(C)(P) *
	630	text_out[9] v	MET Late External Delay Assertion
1.684	0.416	2.100	clk(D)(P)	clk(C)(P) *
	631	text_out[28] v	MET Late External Delay Assertion
1.687	0.413	2.100	clk(D)(P)	clk(C)(P) *
	632	text_out[4] v	MET Late External Delay Assertion
1.690	0.410	2.100	clk(D)(P)	clk(C)(P) *
	633	text_out[5] v	MET Late External Delay Assertion
1.691	0.409	2.100	clk(D)(P)	clk(C)(P) *
	634	text_out[18] v	MET Late External Delay Assertion
1.697	0.403	2.100	clk(D)(P)	clk(C)(P) *
	635	text_out[6] v	MET Late External Delay Assertion
1.699	0.401	2.100	clk(D)(P)	clk(C)(P) *
	636	text_out[25] v	MET Late External Delay Assertion
1.706	0.394	2.100	clk(D)(P)	clk(C)(P) *
	637	text_out[31] v	MET Late External Delay Assertion
1.706	0.394	2.100	clk(D)(P)	clk(C)(P) *
	638	text_out[24] v	MET Late External Delay Assertion
1.707	0.393	2.100	clk(D)(P)	clk(C)(P) *

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     |   639 |           text_out[30] v | MET Late External Delay Assertion
|  1.707 |   0.393 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   640 |           text_out[26] v | MET Late External Delay Assertion
|  1.707 |   0.393 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   641 |           text_out[27] v | MET Late External Delay Assertion
|  1.708 |   0.392 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   642 |            text_out[0] v | MET Late External Delay Assertion
|  1.709 |   0.391 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   643 |            text_out[3] v | MET Late External Delay Assertion
|  1.709 |   0.391 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   644 |            text_out[7] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   645 |            text_out[1] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   646 |            text_out[2] v | MET Late External Delay Assertion
|  1.714 |   0.386 |    2.100 | clk(D)(P) | clk(C)(P) * |
     |   647 |   \text_in_r_reg[4] /E v | MET Setup Check with Pin
\text_in_r_reg[4] /CP   |  1.921 |   0.757 |    2.677 | clk(D)(P) | clk(C)(P)
* |
     |   648 |   \text_in_r_reg[2] /E v | MET Setup Check with Pin
\text_in_r_reg[2] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   649 |   \text_in_r_reg[6] /E v | MET Setup Check with Pin
\text_in_r_reg[6] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   650 |   \text_in_r_reg[3] /E v | MET Setup Check with Pin
\text_in_r_reg[3] /CP   |  1.921 |   0.757 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   651 |   \text_in_r_reg[1] /E v | MET Setup Check with Pin
\text_in_r_reg[1] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   652 |   \text_in_r_reg[5] /E v | MET Setup Check with Pin
\text_in_r_reg[5] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   653 |   \text_in_r_reg[0] /E v | MET Setup Check with Pin
\text_in_r_reg[0] /CP   |  1.922 |   0.756 |    2.678 | clk(D)(P) | clk(C)(P)
* |
     |   654 |  \text_in_r_reg[78] /D ^ | MET Setup Check with Pin
\text_in_r_reg[78] /CP  |  1.930 |   0.765 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   655 |  \text_in_r_reg[77] /D ^ | MET Setup Check with Pin
\text_in_r_reg[77] /CP  |  1.931 |   0.764 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   656 |  \text_in_r_reg[74] /D ^ | MET Setup Check with Pin
\text_in_r_reg[74] /CP  |  1.931 |   0.764 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   657 |  \text_in_r_reg[22] /D ^ | MET Setup Check with Pin
\text_in_r_reg[22] /CP  |  1.937 |   0.753 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   658 |  \text_in_r_reg[21] /D ^ | MET Setup Check with Pin
\text_in_r_reg[21] /CP  |  1.938 |   0.753 |    2.690 | clk(D)(P) | clk(C)(P)
* |
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     |   659 |  \text_in_r_reg[30] /D ^ | MET Setup Check with Pin
\text_in_r_reg[30] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   660 |  \text_in_r_reg[24] /D ^ | MET Setup Check with Pin
\text_in_r_reg[24] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   661 |  \text_in_r_reg[26] /D ^ | MET Setup Check with Pin
\text_in_r_reg[26] /CP  |  1.938 |   0.750 |    2.688 | clk(D)(P) | clk(C)(P)
* |
     |   662 |   \text_in_r_reg[8] /E v | MET Setup Check with Pin
\text_in_r_reg[8] /CP   |  1.938 |   0.756 |    2.694 | clk(D)(P) | clk(C)(P)
* |
     |   663 |  \text_in_r_reg[31] /D ^ | MET Setup Check with Pin
\text_in_r_reg[31] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   664 |  \text_in_r_reg[28] /D ^ | MET Setup Check with Pin
\text_in_r_reg[28] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   665 |  \text_in_r_reg[20] /D ^ | MET Setup Check with Pin
\text_in_r_reg[20] /CP  |  1.938 |   0.752 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   666 |  \text_in_r_reg[27] /D ^ | MET Setup Check with Pin
\text_in_r_reg[27] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   667 |  \text_in_r_reg[16] /D ^ | MET Setup Check with Pin
\text_in_r_reg[16] /CP  |  1.938 |   0.752 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   668 |   \text_in_r_reg[4] /D ^ | MET Setup Check with Pin
\text_in_r_reg[4] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   669 |   \text_in_r_reg[9] /E v | MET Setup Check with Pin
\text_in_r_reg[9] /CP   |  1.938 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   670 |   \text_in_r_reg[2] /D ^ | MET Setup Check with Pin
\text_in_r_reg[2] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   671 |   \text_in_r_reg[3] /D ^ | MET Setup Check with Pin
\text_in_r_reg[3] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   672 |  \text_in_r_reg[18] /D ^ | MET Setup Check with Pin
\text_in_r_reg[18] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   673 |  \text_in_r_reg[23] /D ^ | MET Setup Check with Pin
\text_in_r_reg[23] /CP  |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   674 |   \text_in_r_reg[7] /E v | MET Setup Check with Pin
\text_in_r_reg[7] /CP   |  1.938 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   675 |   \text_in_r_reg[6] /D ^ | MET Setup Check with Pin
\text_in_r_reg[6] /CP   |  1.938 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   676 |  \text_in_r_reg[29] /D ^ | MET Setup Check with Pin
\text_in_r_reg[29] /CP  |  1.938 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
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     |   677 |  \text_in_r_reg[10] /E v | MET Setup Check with Pin
\text_in_r_reg[10] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   678 |   \text_in_r_reg[1] /D ^ | MET Setup Check with Pin
\text_in_r_reg[1] /CP   |  1.939 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   679 |  \text_in_r_reg[11] /E v | MET Setup Check with Pin
\text_in_r_reg[11] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   680 |   \text_in_r_reg[0] /D ^ | MET Setup Check with Pin
\text_in_r_reg[0] /CP   |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   681 |  \text_in_r_reg[17] /D ^ | MET Setup Check with Pin
\text_in_r_reg[17] /CP  |  1.939 |   0.751 |    2.690 | clk(D)(P) | clk(C)(P)
* |
     |   682 |  \text_in_r_reg[25] /D ^ | MET Setup Check with Pin
\text_in_r_reg[25] /CP  |  1.939 |   0.751 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   683 |  \text_in_r_reg[79] /D ^ | MET Setup Check with Pin
\text_in_r_reg[79] /CP  |  1.939 |   0.756 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   684 |   \text_in_r_reg[5] /D ^ | MET Setup Check with Pin
\text_in_r_reg[5] /CP   |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   685 |  \text_in_r_reg[19] /D ^ | MET Setup Check with Pin
\text_in_r_reg[19] /CP  |  1.939 |   0.750 |    2.689 | clk(D)(P) | clk(C)(P)
* |
     |   686 |  \text_in_r_reg[76] /D ^ | MET Setup Check with Pin
\text_in_r_reg[76] /CP  |  1.941 |   0.754 |    2.695 | clk(D)(P) | clk(C)(P)
* |
     |   687 |  \text_in_r_reg[54] /D ^ | MET Setup Check with Pin
\text_in_r_reg[54] /CP  |  1.943 |   0.760 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   688 |  \text_in_r_reg[82] /D ^ | MET Setup Check with Pin
\text_in_r_reg[82] /CP  |  1.943 |   0.754 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |   689 |  \text_in_r_reg[55] /D ^ | MET Setup Check with Pin
\text_in_r_reg[55] /CP  |  1.943 |   0.760 |    2.703 | clk(D)(P) | clk(C)(P)
* |
     |   690 |  \text_in_r_reg[75] /D ^ | MET Setup Check with Pin
\text_in_r_reg[75] /CP  |  1.944 |   0.754 |    2.698 | clk(D)(P) | clk(C)(P)
* |
     |   691 |  \text_in_r_reg[72] /D ^ | MET Setup Check with Pin
\text_in_r_reg[72] /CP  |  1.944 |   0.753 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |   692 |  \text_in_r_reg[49] /D ^ | MET Setup Check with Pin
\text_in_r_reg[49] /CP  |  1.944 |   0.755 |    2.699 | clk(D)(P) | clk(C)(P)
* |
     |   693 |  \text_in_r_reg[52] /D ^ | MET Setup Check with Pin
\text_in_r_reg[52] /CP  |  1.945 |   0.753 |    2.697 | clk(D)(P) | clk(C)(P)
* |
     |   694 |  \text_in_r_reg[51] /D ^ | MET Setup Check with Pin
\text_in_r_reg[51] /CP  |  1.946 |   0.754 |    2.700 | clk(D)(P) | clk(C)(P)
* |
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     |   695 |  \text_in_r_reg[45] /D ^ | MET Setup Check with Pin
\text_in_r_reg[45] /CP  |  1.949 |   0.753 |    2.702 | clk(D)(P) | clk(C)(P)
* |
     |   696 |  \text_in_r_reg[43] /D ^ | MET Setup Check with Pin
\text_in_r_reg[43] /CP  |  1.951 |   0.756 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   697 |  \text_in_r_reg[48] /D ^ | MET Setup Check with Pin
\text_in_r_reg[48] /CP  |  1.952 |   0.755 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   698 |  \text_in_r_reg[44] /D ^ | MET Setup Check with Pin
\text_in_r_reg[44] /CP  |  1.954 |   0.753 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   699 |  \text_in_r_reg[46] /D ^ | MET Setup Check with Pin
\text_in_r_reg[46] /CP  |  1.954 |   0.754 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   700 |  \text_in_r_reg[13] /D ^ | MET Setup Check with Pin
\text_in_r_reg[13] /CP  |  1.955 |   0.752 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   701 |  \text_in_r_reg[47] /D ^ | MET Setup Check with Pin
\text_in_r_reg[47] /CP  |  1.955 |   0.753 |    2.708 | clk(D)(P) | clk(C)(P)
* |
     |   702 |  \text_in_r_reg[14] /D ^ | MET Setup Check with Pin
\text_in_r_reg[14] /CP  |  1.955 |   0.752 |    2.707 | clk(D)(P) | clk(C)(P)
* |
     |   703 |   \text_in_r_reg[8] /D ^ | MET Setup Check with Pin
\text_in_r_reg[8] /CP   |  1.955 |   0.750 |    2.705 | clk(D)(P) | clk(C)(P)
* |
     |   704 |  \text_in_r_reg[12] /D ^ | MET Setup Check with Pin
\text_in_r_reg[12] /CP  |  1.955 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   705 |   \text_in_r_reg[9] /D ^ | MET Setup Check with Pin
\text_in_r_reg[9] /CP   |  1.955 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   706 |   \text_in_r_reg[7] /D ^ | MET Setup Check with Pin
\text_in_r_reg[7] /CP   |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   707 |  \text_in_r_reg[11] /D ^ | MET Setup Check with Pin
\text_in_r_reg[11] /CP  |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   708 |  \text_in_r_reg[15] /D ^ | MET Setup Check with Pin
\text_in_r_reg[15] /CP  |  1.956 |   0.751 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   709 |  \text_in_r_reg[10] /D ^ | MET Setup Check with Pin
\text_in_r_reg[10] /CP  |  1.956 |   0.750 |    2.706 | clk(D)(P) | clk(C)(P)
* |
     |   710 |  \text_in_r_reg[67] /D ^ | MET Setup Check with Pin
\text_in_r_reg[67] /CP  |  1.957 |   0.757 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |   711 |  \text_in_r_reg[97] /D ^ | MET Setup Check with Pin
\text_in_r_reg[97] /CP  |  1.958 |   0.755 |    2.714 | clk(D)(P) | clk(C)(P)
* |
     |   712 | \text_in_r_reg[115] /D ^ | MET Setup Check with Pin
\text_in_r_reg[115] /CP |  1.959 |   0.757 |    2.715 | clk(D)(P) | clk(C)(P)
* |
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     |   713 |  \text_in_r_reg[53] /D ^ | MET Setup Check with Pin
\text_in_r_reg[53] /CP  |  1.960 |   0.752 |    2.712 | clk(D)(P) | clk(C)(P)
* |
     |   714 | \text_in_r_reg[113] /D ^ | MET Setup Check with Pin
\text_in_r_reg[113] /CP |  1.961 |   0.757 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   715 |  \text_in_r_reg[73] /D ^ | MET Setup Check with Pin
\text_in_r_reg[73] /CP  |  1.961 |   0.763 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   716 |  \text_in_r_reg[70] /D ^ | MET Setup Check with Pin
\text_in_r_reg[70] /CP  |  1.962 |   0.761 |    2.722 | clk(D)(P) | clk(C)(P)
* |
     |   717 | \text_in_r_reg[109] /D ^ | MET Setup Check with Pin
\text_in_r_reg[109] /CP |  1.962 |   0.759 |    2.721 | clk(D)(P) | clk(C)(P)
* |
     |   718 | \text_in_r_reg[114] /D ^ | MET Setup Check with Pin
\text_in_r_reg[114] /CP |  1.963 |   0.755 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   719 | \text_in_r_reg[107] /D ^ | MET Setup Check with Pin
\text_in_r_reg[107] /CP |  1.963 |   0.759 |    2.723 | clk(D)(P) | clk(C)(P)
* |
     |   720 |  \text_in_r_reg[69] /D ^ | MET Setup Check with Pin
\text_in_r_reg[69] /CP  |  1.964 |   0.759 |    2.723 | clk(D)(P) | clk(C)(P)
* |
     |   721 |  \text_in_r_reg[65] /D ^ | MET Setup Check with Pin
\text_in_r_reg[65] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   722 |  \text_in_r_reg[80] /D ^ | MET Setup Check with Pin
\text_in_r_reg[80] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   723 |  \text_in_r_reg[59] /D ^ | MET Setup Check with Pin
\text_in_r_reg[59] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   724 |  \text_in_r_reg[61] /D ^ | MET Setup Check with Pin
\text_in_r_reg[61] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   725 |  \text_in_r_reg[41] /D ^ | MET Setup Check with Pin
\text_in_r_reg[41] /CP  |  1.965 |   0.752 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   726 |  \text_in_r_reg[36] /D ^ | MET Setup Check with Pin
\text_in_r_reg[36] /CP  |  1.965 |   0.752 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   727 |  \text_in_r_reg[66] /D ^ | MET Setup Check with Pin
\text_in_r_reg[66] /CP  |  1.965 |   0.759 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   728 |  \text_in_r_reg[62] /D ^ | MET Setup Check with Pin
\text_in_r_reg[62] /CP  |  1.965 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   729 |  \text_in_r_reg[60] /D ^ | MET Setup Check with Pin
\text_in_r_reg[60] /CP  |  1.966 |   0.751 |    2.716 | clk(D)(P) | clk(C)(P)
* |
     |   730 |  \text_in_r_reg[35] /D ^ | MET Setup Check with Pin
\text_in_r_reg[35] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   731 |  \text_in_r_reg[68] /D ^ | MET Setup Check with Pin
\text_in_r_reg[68] /CP  |  1.966 |   0.758 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   732 |  \text_in_r_reg[37] /D ^ | MET Setup Check with Pin
\text_in_r_reg[37] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   733 |  \text_in_r_reg[32] /D ^ | MET Setup Check with Pin
\text_in_r_reg[32] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   734 |  \text_in_r_reg[42] /D ^ | MET Setup Check with Pin
\text_in_r_reg[42] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   735 |  \text_in_r_reg[58] /D ^ | MET Setup Check with Pin
\text_in_r_reg[58] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   736 |  \text_in_r_reg[63] /D ^ | MET Setup Check with Pin
\text_in_r_reg[63] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   737 |  \text_in_r_reg[39] /D ^ | MET Setup Check with Pin
\text_in_r_reg[39] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   738 |  \text_in_r_reg[56] /D ^ | MET Setup Check with Pin
\text_in_r_reg[56] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   739 |  \text_in_r_reg[57] /D ^ | MET Setup Check with Pin
\text_in_r_reg[57] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   740 |  \text_in_r_reg[40] /D ^ | MET Setup Check with Pin
\text_in_r_reg[40] /CP  |  1.966 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   741 |  \text_in_r_reg[34] /D ^ | MET Setup Check with Pin
\text_in_r_reg[34] /CP  |  1.967 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   742 |  \text_in_r_reg[50] /D ^ | MET Setup Check with Pin
\text_in_r_reg[50] /CP  |  1.967 |   0.751 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   743 |  \text_in_r_reg[33] /D ^ | MET Setup Check with Pin
\text_in_r_reg[33] /CP  |  1.967 |   0.750 |    2.717 | clk(D)(P) | clk(C)(P)
* |
     |   744 | \text_in_r_reg[105] /D ^ | MET Setup Check with Pin
\text_in_r_reg[105] /CP |  1.967 |   0.758 |    2.725 | clk(D)(P) | clk(C)(P)
* |
     |   745 |  \text_in_r_reg[38] /D ^ | MET Setup Check with Pin
\text_in_r_reg[38] /CP  |  1.967 |   0.750 |    2.718 | clk(D)(P) | clk(C)(P)
* |
     |   746 | \text_in_r_reg[108] /D ^ | MET Setup Check with Pin
\text_in_r_reg[108] /CP |  1.968 |   0.758 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   747 | \text_in_r_reg[106] /D ^ | MET Setup Check with Pin
\text_in_r_reg[106] /CP |  1.968 |   0.759 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   748 |  \text_in_r_reg[64] /D ^ | MET Setup Check with Pin
\text_in_r_reg[64] /CP  |  1.968 |   0.756 |    2.724 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   749 | \text_in_r_reg[112] /D ^ | MET Setup Check with Pin
\text_in_r_reg[112] /CP |  1.968 |   0.758 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   750 | \text_in_r_reg[104] /D ^ | MET Setup Check with Pin
\text_in_r_reg[104] /CP |  1.969 |   0.757 |    2.726 | clk(D)(P) | clk(C)(P)
* |
     |   751 | \text_in_r_reg[110] /D ^ | MET Setup Check with Pin
\text_in_r_reg[110] /CP |  1.970 |   0.754 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   752 |  \text_in_r_reg[71] /D ^ | MET Setup Check with Pin
\text_in_r_reg[71] /CP  |  1.970 |   0.754 |    2.724 | clk(D)(P) | clk(C)(P)
* |
     |   753 | \text_in_r_reg[111] /D ^ | MET Setup Check with Pin
\text_in_r_reg[111] /CP |  1.971 |   0.756 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   754 | \text_in_r_reg[116] /D ^ | MET Setup Check with Pin
\text_in_r_reg[116] /CP |  1.973 |   0.754 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   755 | \text_in_r_reg[127] /D ^ | MET Setup Check with Pin
\text_in_r_reg[127] /CP |  1.975 |   0.753 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   756 | \text_in_r_reg[121] /D ^ | MET Setup Check with Pin
\text_in_r_reg[121] /CP |  1.975 |   0.753 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   757 | \text_in_r_reg[123] /D ^ | MET Setup Check with Pin
\text_in_r_reg[123] /CP |  1.975 |   0.752 |    2.727 | clk(D)(P) | clk(C)(P)
* |
     |   758 | \text_in_r_reg[122] /D ^ | MET Setup Check with Pin
\text_in_r_reg[122] /CP |  1.975 |   0.752 |    2.728 | clk(D)(P) | clk(C)(P)
* |
     |   759 | \text_in_r_reg[126] /D ^ | MET Setup Check with Pin
\text_in_r_reg[126] /CP |  1.978 |   0.752 |    2.730 | clk(D)(P) | clk(C)(P)
* |
     |   760 | \text_in_r_reg[124] /D ^ | MET Setup Check with Pin
\text_in_r_reg[124] /CP |  1.980 |   0.752 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   761 |  \text_in_r_reg[88] /D ^ | MET Setup Check with Pin
\text_in_r_reg[88] /CP  |  1.980 |   0.762 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   762 | \text_in_r_reg[120] /D ^ | MET Setup Check with Pin
\text_in_r_reg[120] /CP |  1.980 |   0.752 |    2.732 | clk(D)(P) | clk(C)(P)
* |
     |   763 |  \text_in_r_reg[91] /D ^ | MET Setup Check with Pin
\text_in_r_reg[91] /CP  |  1.981 |   0.761 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   764 |  \text_in_r_reg[90] /D ^ | MET Setup Check with Pin
\text_in_r_reg[90] /CP  |  1.982 |   0.760 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   765 |  \text_in_r_reg[83] /D ^ | MET Setup Check with Pin
\text_in_r_reg[83] /CP  |  1.982 |   0.760 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   766 | \text_in_r_reg[125] /D ^ | MET Setup Check with Pin
\text_in_r_reg[125] /CP |  1.984 |   0.752 |    2.736 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   767 |  \text_in_r_reg[85] /D ^ | MET Setup Check with Pin
\text_in_r_reg[85] /CP  |  1.985 |   0.756 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   768 |  \text_in_r_reg[89] /D ^ | MET Setup Check with Pin
\text_in_r_reg[89] /CP  |  1.985 |   0.759 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   769 | \text_in_r_reg[119] /D ^ | MET Setup Check with Pin
\text_in_r_reg[119] /CP |  1.985 |   0.752 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   770 |  \text_in_r_reg[84] /D ^ | MET Setup Check with Pin
\text_in_r_reg[84] /CP  |  1.986 |   0.757 |    2.742 | clk(D)(P) | clk(C)(P)
* |
     |   771 |  \text_in_r_reg[86] /D ^ | MET Setup Check with Pin
\text_in_r_reg[86] /CP  |  1.986 |   0.756 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   772 | \text_in_r_reg[117] /D ^ | MET Setup Check with Pin
\text_in_r_reg[117] /CP |  1.986 |   0.754 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   773 | \text_in_r_reg[103] /D ^ | MET Setup Check with Pin
\text_in_r_reg[103] /CP |  1.986 |   0.751 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   774 |  \text_in_r_reg[95] /D ^ | MET Setup Check with Pin
\text_in_r_reg[95] /CP  |  1.986 |   0.754 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   775 | \text_in_r_reg[102] /D ^ | MET Setup Check with Pin
\text_in_r_reg[102] /CP |  1.986 |   0.751 |    2.737 | clk(D)(P) | clk(C)(P)
* |
     |   776 |  \text_in_r_reg[93] /D ^ | MET Setup Check with Pin
\text_in_r_reg[93] /CP  |  1.987 |   0.755 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   777 |  \text_in_r_reg[87] /D ^ | MET Setup Check with Pin
\text_in_r_reg[87] /CP  |  1.987 |   0.754 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   778 | \text_in_r_reg[101] /D ^ | MET Setup Check with Pin
\text_in_r_reg[101] /CP |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   779 | \text_in_r_reg[100] /D ^ | MET Setup Check with Pin
\text_in_r_reg[100] /CP |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   780 |  \text_in_r_reg[94] /D ^ | MET Setup Check with Pin
\text_in_r_reg[94] /CP  |  1.987 |   0.753 |    2.741 | clk(D)(P) | clk(C)(P)
* |
     |   781 |  \text_in_r_reg[98] /D ^ | MET Setup Check with Pin
\text_in_r_reg[98] /CP  |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   782 |  \text_in_r_reg[96] /D ^ | MET Setup Check with Pin
\text_in_r_reg[96] /CP  |  1.987 |   0.751 |    2.738 | clk(D)(P) | clk(C)(P)
* |
     |   783 | \text_in_r_reg[118] /D ^ | MET Setup Check with Pin
\text_in_r_reg[118] /CP |  1.987 |   0.753 |    2.740 | clk(D)(P) | clk(C)(P)
* |
     |   784 |  \text_in_r_reg[99] /D ^ | MET Setup Check with Pin
\text_in_r_reg[99] /CP  |  1.988 |   0.751 |    2.739 | clk(D)(P) | clk(C)(P)
* |
```

```
     |   785 |  \text_in_r_reg[92] /D ^ | MET Setup Check with Pin
\text_in_r_reg[92] /CP  |  1.991 |   0.752 |    2.743 | clk(D)(P) | clk(C)(P)
* |
     |   786 |  \text_in_r_reg[81] /D ^ | MET Setup Check with Pin
\text_in_r_reg[81] /CP  |  1.992 |   0.752 |    2.744 | clk(D)(P) | clk(C)(P)
* |
     |   787 |            ld_r_reg/D ^ | MET Setup Check with Pin
ld_r_reg/CP             |  1.999 |   0.757 |    2.756 | clk(D)(P) | clk(C)(P)
* |
     +--------------------------------------------------------------------------
-------------------------------------------------------------------+

<CMD> setAnalysisMode -analysisType bcwc -checkType setup -skew true -
clockPropagation sdccontrol
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -
max_points 100 -net -summary >
$rpt_dir/report_timing.post_extract.bcwc.summary
**WARN: (TCLCMD-566):   Option '-summary' for command 'report_timing' is
obsolete and has been replaced by '-path_type end'. The obsolete option still
works in this release, but to avoid this warning and to ensure compatibility
with future releases, update your script to use '-path_type end'.
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 587.4M)
Number of Loop : 0
Start delay calculation (mem=587.445M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:01.5 real=0:00:01.0 mem=587.445M 0)
*** CDM Built up (cpu=0:00:02.2  real=0:00:02.0  mem= 587.4M) ***
<CMD> report_power


Start force assigning power rail voltages for view default_view_setup
Finished assigning power rail voltages

CPE found ground net: VSS
CPE found power net: VDD  voltage: 0V

Warning:
  There are 2 power/gnd nets that are not connected
VSS VDD ...
Use 'globalNetConnect' to define rail connections.
[PowermeterNetlistLib::InfoMergingRails]
WARNING (POWER-2035): There are 2 power/gnd nets that are not connected
VSS VDD ...
Use 'globalNetConnect' to define rail connections.


INFO (POWER-1606): Found clock 'clk' with frequency 400MHz from SDC file.


Propagating signal activity...


Starting Levelizing
```

```
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT)
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 5%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 10%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 15%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 20%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 25%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 30%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 35%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 40%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 45%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 50%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 55%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 60%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 65%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 70%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 75%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 80%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 85%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 90%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 95%

Finished Levelizing
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT)

Starting Activity Propagation
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT)
INFO (POWER-1356):   No default input activity has been set.  Defaulting to
0.2.

2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 5%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 10%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 15%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 20%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 25%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 30%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 35%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 40%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 45%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 50%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 55%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 60%
2011-May-06 10:17:21 (2011-May-06 15:17:21 GMT): 65%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 70%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 75%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 80%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 85%

Finished Activity Propagation
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT)

Starting Calculating power
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT)

Calculating power dissipation...
```

```
 ... Calculating switching power
  Cannot locate supply power rail for net 'clk__L2_N5' of instance
clk__L2_I5
  Cannot locate supply power rail for net 'clk__L2_N4' of instance
clk__L2_I4
  Cannot locate supply power rail for net 'clk__L2_N3' of instance
clk__L2_I3
  Cannot locate supply power rail for net 'clk__L2_N2' of instance
clk__L2_I2
  Cannot locate supply power rail for net 'clk__L2_N1' of instance
clk__L2_I1
  only first five unconnected nets are listed...
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 5%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 10%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 15%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 20%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 25%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 30%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 35%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 40%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 45%
2011-May-06 10:17:22 (2011-May-06 15:17:22 GMT): 50%
 ... Calculating internal and leakage power
WARNING (POWER-2047): power_level vdds cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell
HS65_GS_CNBFX21.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell
HS65_GS_CNBFX21.
```

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2011-May-06 10:17:24 (2011-May-06 15:17:24 GMT): 55%
2011-May-06 10:17:26 (2011-May-06 15:17:26 GMT): 60%
2011-May-06 10:17:27 (2011-May-06 15:17:27 GMT): 65%
2011-May-06 10:17:30 (2011-May-06 15:17:30 GMT): 70%
2011-May-06 10:17:32 (2011-May-06 15:17:32 GMT): 75%
2011-May-06 10:17:34 (2011-May-06 15:17:34 GMT): 80%
2011-May-06 10:17:36 (2011-May-06 15:17:36 GMT): 85%
2011-May-06 10:17:39 (2011-May-06 15:17:39 GMT): 90%
2011-May-06 10:17:41 (2011-May-06 15:17:41 GMT): 95%

Finished Calculating power
2011-May-06 10:17:41 (2011-May-06 15:17:41 GMT)
*------------------------------------------------------------------------------
------------
*      -  - Version  32-bit
*
*
*     Date & Time:      2011-May-06 10:17:41 (2011-May-06 15:17:41 GMT)
*
*------------------------------------------------------------------------------
------------
*
*     Design: aes_cipher_top
*
*     Liberty Libraries used:
*             LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib
*             LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib
*             LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib
*             LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib
*             LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib
*             LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib
*
*     Power Domain used:
*
*     Power Units = 1mW
*
*     Time Units = 1e-09 secs
*
*       report_power
*
------------------------------------------------------------------------------
------------


Total Power
------------------------------------------------------------------------------
------------
Total Internal Power:        9.71      31.28%
Total Switching Power:       20.22      65.12%
Total Leakage Power:       1.116      3.596%
Total Power:       31.04
------------------------------------------------------------------------------
------------
```

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	2.889	2.536	0.1519	5.576	17.96
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	6.787	17.27	0.9624	25.02	80.6
Clock (Combinational)	0.03428	0.4105	0.001951	0.4468	1.439
Total	9.71	20.22	1.116	31.04	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Default	0.9	9.71	20.22	1.116	31.04	100

Clock	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
clk	0.03428	0.4105	0.001951	0.4468	1.439
Total	0.03428	0.4105	0.001951	0.4468	1.439

* Power Distribution Summary:

```
*           Highest Average Power:                clk__L2_I1
(HS65_GS_CNBFX21):         0.07982
*           Highest Leakage Power:                  ld_r_reg
(HS65_GSS_DFPQNX27):     0.0005514
*           Total Cap:  1.29069e-10 F
*           Total instances in design:  9549
*           Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*           Total Fillers and Decap:     0
------------------------------------------------------------------------
------------

report_power consumed time (real time) 00:00:26 : increased peak memory
(719M) by 0.
<CMD> reportGateCount
Gate area 1.5600 um^2
[0] aes_cipher_top Gates=21935 Cells=9549 Area=34219.1 um^2
<CMD> uiSetTool ruler
<CMD> zoomBox 212.768 9.419 228.176 -5.045
<CMD> zoomBox 219.487 0.358 221.250 -0.655
<CMD> zoomBox 220.143 0.068 220.282 -0.072
<CMD> fit
<CMD> zoomBox -3.888 224.188 8.061 212.239
<CMD> zoomBox -0.247 220.701 0.652 219.988
<CMD> fit
<CMD> report_timing -from \u0/w_reg[3][16]/Q -to \u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'Ã€/w_reg[3][16]/Q'
<CMD> report_timing -from \|u0/w_reg[3][16]/Q -to \|u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for '|u0/w_reg[3][16]/Q'
<CMD> report_timing -from \|u0|/w_reg[3][16]/Q -to \|u0|/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for '|u0|/w_reg[3][16]/Q'
<CMD> report_timing -from \sa31_reg[6]/Q -to \sa32_reg[4]/D
Path 1: VIOLATED Setup Check with Pin \sa32_reg[4] /CP
Endpoint:   \sa32_reg[4] /D (^) checked with  leading edge of 'clk'
Beginpoint: \sa31_reg[6] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.228
- Setup                         0.059
+ Phase Shift                   2.500
= Required Time                 2.669
- Arrival Time                  2.705
= Slack Time                   -0.036
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.262
     = Beginpoint Arrival Time       0.262
     +-------------------------------------------------------------------
--------------+
     |       Instance       |     Arc     |       Cell        | Delay |
Arrival | Required |
     |                      |             |                   |       |  Time
|   Time   |
     |----------------------+-------------+-------------------+-------+------
---+----------|
```

```
     | \sa31_reg[6]          | CP ^         |                    |       |
0.262 |    0.226 |
     | \sa31_reg[6]          | CP ^ -> Q v  | HS65_GS_DFPQX9     | 0.168 |
0.430 |    0.394 |
     | us31/FE_OFC8_sa31_6_  | A v -> Z v   | HS65_GS_BFX18      | 0.100 |
0.530 |    0.494 |
     | us31/U350             | A v -> Z ^   | HS65_GS_IVX9       | 0.185 |
0.715 |    0.679 |
     | us31/U63              | A ^ -> Z v   | HS65_GS_NOR2X6     | 0.141 |
0.856 |    0.820 |
     | us31/U37              | A v -> Z ^   | HS65_GS_IVX9       | 0.136 |
0.992 |    0.956 |
     | us31/U234             | A ^ -> Z v   | HS65_GS_NOR2X6     | 0.110 |
1.103 |    1.067 |
     | us31/U98              | A v -> Z ^   | HS65_GS_IVX9       | 0.111 |
1.214 |    1.178 |
     | us31/U34              | B ^ -> Z v   | HS65_GS_NOR2X6     | 0.059 |
1.273 |    1.237 |
     | us31/U266             | C v -> Z v   | HS65_GS_CB4I1X9    | 0.087 |
1.360 |    1.323 |
     | us31/U265             | F v -> Z ^   | HS65_GS_AOI312X4   | 0.079 |
1.438 |    1.402 |
     | us31/U264             | E ^ -> Z v   | HS65_GS_OAI212X5   | 0.072 |
1.511 |    1.474 |
     | us31/U334             | B v -> Z ^   | HS65_GS_AOI12X2    | 0.164 |
1.674 |    1.638 |
     | us31/U332             | E ^ -> Z v   | HS65_GS_OAI212X5   | 0.109 |
1.783 |    1.746 |
     | us31/U107             | A v -> Z v   | HS65_GS_NAND4ABX3  | 0.227 |
2.010 |    1.973 |
     | U818                  | B v -> Z ^   | HS65_GSS_XOR2X6    | 0.215 |
2.224 |    2.188 |
     | U1254                 | B ^ -> Z v   | HS65_GSS_XOR3X2    | 0.206 |
2.430 |    2.394 |
     | U1253                 | A v -> Z v   | HS65_GSS_XOR3X2    | 0.161 |
2.591 |    2.554 |
     | U1251                 | D v -> Z ^   | HS65_GS_OAI22X6    | 0.114 |
2.705 |    2.669 |
     | \sa32_reg[4]          | D ^          | HS65_GS_DFPQX9     | 0.000 |
2.705 |    2.669 |
     +-------------------------------------------------------------------------
--------------+

<CMD> report_timing -from \u0/w_reg[3][16]/Q -to \u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'Ã€/w_reg[3][16]/Q'
<CMD> report_timing -from u0/w_reg[3][16]/Q -to \u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'Ã€/w_reg[2][24]/D'
<CMD> report_timing -from u0/w_reg[3][16]/Q -to u0/w_reg[2][24]/D
Path 1: MET Setup Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.258
- Setup                         0.006
+ Phase Shift                   2.500
```

```
= Required Time                 2.753
- Arrival Time                  2.533
= Slack Time                    0.220
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.254
     = Beginpoint Arrival Time       0.254
     +--------------------------------------------------------------------
------------+
     |      Instance      |     Arc     |       Cell        | Delay | Arrival
| Required |
     |                    |             |                   |       |  Time
|   Time   |
     |--------------------+-------------+-------------------+-------+-------
-+----------|
     | u0/\w_reg[3][16]   | CP ^        |                   |       |   0.254
|    0.473 |
     | u0/\w_reg[3][16]   | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.164 |   0.418
|    0.637 |
     | u0/FE_OFC30_w3_16_ | A v -> Z v  | HS65_GS_BFX18     | 0.111 |   0.528
|    0.748 |
     | u0/u0/U380         | A v -> Z ^  | HS65_GS_IVX9      | 0.230 |   0.758
|    0.978 |
     | u0/u0/U309         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.197 |   0.955
|    1.174 |
     | u0/u0/U256         | A v -> Z ^  | HS65_GS_IVX9      | 0.158 |   1.112
|    1.332 |
     | u0/u0/U48          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.115 |   1.228
|    1.447 |
     | u0/u0/U27          | A v -> Z ^  | HS65_GS_IVX9      | 0.146 |   1.373
|    1.593 |
     | u0/u0/U26          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.078 |   1.452
|    1.671 |
     | u0/u0/U215         | A v -> Z ^  | HS65_GS_CBI4I1X5  | 0.069 |   1.521
|    1.741 |
     | u0/u0/U172         | E ^ -> Z v  | HS65_GS_OAI212X5  | 0.063 |   1.585
|    1.804 |
     | u0/u0/U170         | E v -> Z ^  | HS65_GS_AOI212X4  | 0.084 |   1.669
|    1.888 |
     | u0/u0/U397         | D ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.085 |   1.754
|    1.973 |
     | u0/u0/U395         | B v -> Z v  | HS65_GS_NAND4ABX3 | 0.150 |   1.903
|    2.123 |
     | u0/U72             | B v -> Z ^  | HS65_GSS_XOR2X6   | 0.125 |   2.028
|    2.248 |
     | u0/U144            | A ^ -> Z ^  | HS65_GSS_XOR3X2   | 0.234 |   2.262
|    2.482 |
     | u0/U229            | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.176 |   2.438
|    2.658 |
     | u0/U228            | C v -> Z v  | HS65_GS_AO22X9    | 0.095 |   2.533
|    2.753 |
     | u0/\w_reg[2][24]   | D v         | HS65_GS_DFPQX4    | 0.000 |   2.533
|    2.753 |
     +--------------------------------------------------------------------
------------+
```

```
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -to u0/w_reg[2][24]/D
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:00.1, MEM = 587.4M)
Number of Loop : 0
Start delay calculation (mem=587.441M)...
delayCal using detail RC...
Delay calculation completed. (cpu=0:00:01.5 real=0:00:01.0 mem=587.441M 0)
*** CDM Built up (cpu=0:00:02.3  real=0:00:02.0  mem= 587.4M) ***
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.430
  Slack Time                   0.302
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.111
     = Beginpoint Arrival Time           0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U308/Z         | B v -> Z ^  | HS65_GS_NOR3X4    | 0.042 |
0.258 | 0.037 | 0.005 |
     | u0/u0/U237/Z         | C ^ -> Z v  | HS65_GS_NOR3AX2   | 0.023 |
0.281 | 0.021 | 0.004 |
     | u0/u0/U397/Z         | C v -> Z ^  | HS65_GS_NAND4ABX3 | 0.022 |
0.303 | 0.023 | 0.005 |
     | u0/u0/U395/Z         | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.334 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.353 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.394 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.408 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.430 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.430 | 0.008 | 0.002 |
```

```
     +-------------------------------------------------------------------------
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<CMD> man report_timing
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -to u0/w_reg[2][24]/D  -all
    Usage:   report_timing  [-clock_from <clk_signame_list>
                                        [-edge_from {lead | trail}]]
                            [-clock_to <clk_signame_list>
                                        [-edge_to {lead | trail}]]
                            [-rise | -fall]
                            [-early | -late |
                             -check_type { setup | hold | pulse_width |
                                           clock_period |
                                           clock_gating_setup |
                                           clock_gating_hold |
                                           clock_gating_pulse_width |
                                           data_setup | data_hold |
                                           recovery | removal |
                                           clock_separation | skew |
                                           no_change_setup |
                                           no_change_hold }]
                            [-max_paths <integer> |
                             -max_points <integer> [-nworst <integer>] |
                             -begin_end_pair]
                            [{-from | -from_rise | -from_fall} <pin_list>]
                            [{-through | -through_rise | -through_fall}
                                 <pin_list>]
                            [{-not_through | -not_rise_through |
                           -not_fall_through}
                                 <object_list>]
                            [{-to | -to_rise | -to_fall} <pin_list>]
                            [-point_to_point]
                            [-check_clocks]
                            [-path_group <groupname_list>]
                            [-path_exceptions {applied | ignored | all}]
                            [-net]
                            [-unique_pins]
                            [-path_type {end | summary | full | full_clock |
                                       end_slack_only | summary_slack_only}]
                            [[-max_slack <float>] [-min_slack <float>]
                             | [-unconstrained [-delay_limit <float>]]]
                            [-view {viewName}]
                            [-format column_list]
                            [-collection]
                            [-retime {locv | path_slew_propagation | ssta}]
                            [-machine_readable | -tcl_list]
                            [-derate_summary]
                            [-worst_rc_corner]
                            [-sort_slack_by {ssta_yield | ssta_violation |
                                      ssta_NSigma | ssta_path_criticality}]
                            [-ssta_jpdf]
                            [-ssta_criticality <integer>]
                            [-ssta_percentile <float>]
```

```
                           [-ssta_sigma_multiplier <float>]
                           [{> | >>} filename[.gz]]
<CMD> man report_timing
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.472
  Slack Time                   0.345
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q ^ | HS65_GS_DFPQX9    | 0.057 |
0.168 | 0.009 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A ^ -> Z ^  | HS65_GS_BFX18     | 0.053 |
0.221 | 0.086 | 0.110 |
     | u0/u0/U380/Z         | A ^ -> Z v  | HS65_GS_IVX9      | 0.079 |
0.300 | 0.087 | 0.078 |
     | u0/u0/U265/Z         | B v -> Z ^  | HS65_GS_OAI21X3   | 0.045 |
0.345 | 0.016 | 0.001 |
     | u0/u0/U395/Z         | A ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.377 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.396 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.436 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.451 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.472 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.472 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
-------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
```

```
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                          0.012
+ Phase Shift                   0.000
= Required Time                 0.127
  Arrival Time                  0.430
  Slack Time                    0.302
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U308/Z         | B v -> Z ^  | HS65_GS_NOR3X4    | 0.042 |
0.258 | 0.037 | 0.005 |
     | u0/u0/U237/Z         | C ^ -> Z v  | HS65_GS_NOR3AX2   | 0.023 |
0.281 | 0.021 | 0.004 |
     | u0/u0/U397/Z         | C v -> Z ^  | HS65_GS_NAND4ABX3 | 0.022 |
0.303 | 0.023 | 0.005 |
     | u0/u0/U395/Z         | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.334 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.353 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.394 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.408 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.430 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.430 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
-------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                          0.012
+ Phase Shift                   0.000
= Required Time                 0.127
```

```
  Arrival Time                  0.472
  Slack Time                    0.345
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +--------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q ^ | HS65_GS_DFPQX9    | 0.057 |
0.168 | 0.009 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A ^ -> Z ^  | HS65_GS_BFX18     | 0.053 |
0.221 | 0.086 | 0.110 |
     | u0/u0/U380/Z         | A ^ -> Z v  | HS65_GS_IVX9      | 0.079 |
0.300 | 0.087 | 0.078 |
     | u0/u0/U265/Z         | B v -> Z ^  | HS65_GS_OAI21X3   | 0.045 |
0.345 | 0.016 | 0.001 |
     | u0/u0/U395/Z         | A ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.377 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.396 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.436 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.451 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.472 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.472 | 0.008 | 0.002 |
     +--------------------------------------------------------------------
-------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U170/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.495
  Slack Time                   0.368
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +--------------------------------------------------------------------
-------------------+
```

```
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U329/Z         | A v -> Z ^  | HS65_GS_NOR2X6    | 0.072 |
0.288 | 0.095 | 0.030 |
     | u0/u0/U239/Z         | C ^ -> Z v  | HS65_GS_NAND3X5   | 0.030 |
0.317 | 0.027 | 0.003 |
     | u0/u0/U171/Z         | D v -> Z ^  | HS65_GS_OAI311X5  | 0.022 |
0.339 | 0.019 | 0.009 |
     | u0/u0/U170/Z         | C ^ -> Z v  | HS65_GS_AOI212X4  | 0.012 |
0.351 | 0.010 | 0.002 |
     | u0/u0/U397/Z         | D v -> Z ^  | HS65_GS_NAND4ABX3 | 0.017 |
0.368 | 0.023 | 0.005 |
     | u0/u0/U395/Z         | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.399 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.419 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.459 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.474 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.495 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.495 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U170/Z   -through u0/u0/U170/Z -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.495
  Slack Time                   0.368
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
------------------+
```

```
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U329/Z         | A v -> Z ^  | HS65_GS_NOR2X6    | 0.072 |
0.288 | 0.095 | 0.030 |
     | u0/u0/U239/Z         | C ^ -> Z v  | HS65_GS_NAND3X5   | 0.030 |
0.317 | 0.027 | 0.003 |
     | u0/u0/U171/Z         | D v -> Z ^  | HS65_GS_OAI311X5  | 0.022 |
0.339 | 0.019 | 0.009 |
     | u0/u0/U170/Z         | C ^ -> Z v  | HS65_GS_AOI212X4  | 0.012 |
0.351 | 0.010 | 0.002 |
     | u0/u0/U397/Z         | D v -> Z ^  | HS65_GS_NAND4ABX3 | 0.017 |
0.368 | 0.023 | 0.005 |
     | u0/u0/U395/Z         | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.399 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.419 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.459 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.474 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.495 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.495 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U170/Z   -through u0/u0/U170/Z -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.495
  Slack Time                   0.368
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
------------------+
```

```
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U329/Z         | A v -> Z ^  | HS65_GS_NOR2X6    | 0.072 |
0.288 | 0.095 | 0.030 |
     | u0/u0/U239/Z         | C ^ -> Z v  | HS65_GS_NAND3X5   | 0.030 |
0.317 | 0.027 | 0.003 |
     | u0/u0/U171/Z         | D v -> Z ^  | HS65_GS_OAI311X5  | 0.022 |
0.339 | 0.019 | 0.009 |
     | u0/u0/U170/Z         | C ^ -> Z v  | HS65_GS_AOI212X4  | 0.012 |
0.351 | 0.010 | 0.002 |
     | u0/u0/U397/Z         | D v -> Z ^  | HS65_GS_NAND4ABX3 | 0.017 |
0.368 | 0.023 | 0.005 |
     | u0/u0/U395/Z         | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.399 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.419 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.459 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.474 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.495 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.495 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U380/Z   -through u0/u0/U170/Z -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.697
  Slack Time                   0.569
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
------------------+
```

```
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U380/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
     | u0/u0/U256/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U29/Z          | A v -> Z ^  | HS65_GS_NAND2X7   | 0.029 |
0.496 | 0.028 | 0.011 |
     | u0/u0/U172/Z         | D ^ -> Z v  | HS65_GS_OAI212X5  | 0.014 |
0.509 | 0.011 | 0.002 |
     | u0/u0/U170/Z         | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.525 | 0.018 | 0.002 |
     | u0/u0/U397/Z         | D ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.023 |
0.549 | 0.030 | 0.005 |
     | u0/u0/U395/Z         | B v -> Z v  | HS65_GS_NAND4ABX3 | 0.051 |
0.599 | 0.037 | 0.007 |
     | u0/U72/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.620 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.661 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.675 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.697 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.697 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U380/Z   -through u0/u0/U170/Z -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.697
```

```
  Slack Time                    0.569
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------
------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U380/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
     | u0/u0/U256/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U29/Z          | A v -> Z ^  | HS65_GS_NAND2X7   | 0.029 |
0.496 | 0.028 | 0.011 |
     | u0/u0/U172/Z         | D ^ -> Z v  | HS65_GS_OAI212X5  | 0.014 |
0.509 | 0.011 | 0.002 |
     | u0/u0/U170/Z         | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.525 | 0.018 | 0.002 |
     | u0/u0/U397/Z         | D ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.023 |
0.549 | 0.030 | 0.005 |
     | u0/u0/U395/Z         | B v -> Z v  | HS65_GS_NAND4ABX3 | 0.051 |
0.599 | 0.037 | 0.007 |
     | u0/U72/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.620 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.661 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.675 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.697 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.697 | 0.008 | 0.002 |
     +-------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U411/Z   -through   u0/u0/U380/Z   -
through   u0/u0/U9/Z   -through   u0/u0/U309/Z   -through   u0/u0/U256/Z   -
through   u0/u0/U48/Z   -through   u0/u0/U27/Z   -through   u0/u0/U26/Z   -
through   u0/u0/U215/Z   -through   u0/u0/U172/Z   -through   u0/u0/U170/Z
```

```
-through   u0/u0/U397/Z -through   u0/u0/U395/Z -through   u0/U72/Z -through
u0/U144/Z -through   u0/U229/Z -through   u0/U228/Z -to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U411/Z'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through   u0/u0/U380/Z   -through u0/u0/U411/Z -to
u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U411/Z'
<CMD> help write
Multiple commands found:
      writeAnnotatedTransition
      writeDesignTiming
      writeFlowTemplate
      writeHif
      writeSetLoad
      writeTimingCon
      write_anls_command_file
      write_category_summary
      write_global_slack_report
      write_global_slack_worst_trigger_path_on_clocks
      write_model_timing
      write_power_constraints
      write_sdf
      write_tcf
      write_text_timing_report
      write_timing_windows

<CMD> man writeDesignTiming
<CMD> help dump
Multiple commands found:
      dumpCongestArea
      dumpNanoCongestArea
      dumpNetsInCongestedArea
      dumpToGIF
      dump_unannotated_nets

<CMD> help netlist
Multiple commands found:
      checkNetlist
      ecoCompareNetlist
      loadBlackBlobNetlist
      loadBlackBoxNetlist
      netlistClustering
      netlistUnclustering
      runRcNetlistRestruct
      saveNetlist
      timing_disable_netlist_constants
      uniquifyNetlist

<CMD> help saveNetlist
Usage: saveNetlist
    saveNetlist
    <fileName>
    [-excludeLeafCell  | -onlyLeafCell  | -onlyStdCell  | -onlyMacro
     | -module <moduleName>]
```

```
    [-flat]
    [-ilm]
    [-phys]
    [-includePowerGround]
    [-includePhysicalInst]
    [-excludeTopCellPGPort <portName>]
    [-includeBumpCell]
    [-includePhysicalCell <cellName>]
    [-excludeLogicalCell <cellName> | -excludeCellInst <cellName>]
    [-lineLength <characters_per_line>]
    [-omitFloatingPort]

<CMD> saveNetlist aes_cipher_top.timing.v
Writing Netlist "aes_cipher_top.timing.v" ...
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z -
through u0/u0/U170/Z -through u0/u0/U172/Z -through u0/u0/U215/Z -through
u0/u0/U26/Z -through u0/u0/U27/Z -through u0/u0/U48/Z -through u0/u0/U256/Z -
through u0/u0/U309/Z -through u0/u0/U9/Z -through u0/u0/U380/Z -through
u0/u0/U411/Z -to u0/w_reg[3][16]/Q
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U9/Z'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z -
through u0/u0/U170/Z -through u0/u0/U172/Z -through u0/u0/U215/Z -through
u0/u0/U26/Z -through u0/u0/U27/Z -through u0/u0/U48/Z -through u0/u0/U256/Z -
through u0/u0/U309/Z -through u0/u0/U380/Z -through u0/u0/U411/Z -to
u0/w_reg[3][16]/Q
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U411/Z'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z -
through u0/u0/U170/Z -through u0/u0/U172/Z -through u0/u0/U215/Z -through
u0/u0/U26/Z -through u0/u0/U27/Z -through u0/u0/U48/Z -through u0/u0/U256/Z -
through u0/u0/U309/Z -through u0/u0/U380/Z -to u0/w_reg[3][16]/Q
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z -
through u0/u0/U170/Z -through u0/u0/U172/Z -through u0/u0/U215/Z -through
u0/u0/U26/Z -through u0/u0/U27/Z -through u0/u0/U48/Z -through u0/u0/U256/Z -
through u0/u0/U309/Z -through u0/u0/U380/Z -to u0/w_reg[3][16]/Q -
unconstrained
No unconstrained timing paths with given description found.
Paths may be constrained or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z -
through u0/u0/U170/Z  -through u0/u0/U215/Z -through u0/u0/U26/Z -through
```

```
u0/u0/U27/Z -through u0/u0/U48/Z -through u0/u0/U256/Z -through u0/u0/U309/Z
-through u0/u0/U380/Z -to u0/w_reg[3][16]/Q
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z  -
through u0/u0/U215/Z -through u0/u0/U26/Z -through u0/u0/U27/Z -through
u0/u0/U48/Z -through u0/u0/U256/Z -through u0/u0/U309/Z -through u0/u0/U380/Z
-to u0/w_reg[3][16]/Q
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[2][24]/D -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z -through u0/U72/Z -through u0/u0/U395/Z -through u0/u0/U397/Z  -
through u0/u0/U26/Z -through u0/u0/U27/Z -through u0/u0/U48/Z -through
u0/u0/U256/Z -through u0/u0/U309/Z -through u0/u0/U380/Z -to
u0/w_reg[3][16]/Q
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/U228/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                          0.012
+ Phase Shift                   0.000
= Required Time                 0.127
  Arrival Time                  0.430
  Slack Time                    0.302
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.111
     = Beginpoint Arrival Time           0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U308/Z         | B v -> Z ^  | HS65_GS_NOR3X4    | 0.042 |
0.258 | 0.037 | 0.005 |
```

```
     | u0/u0/U237/Z          | C ^ -> Z v  | HS65_GS_NOR3AX2   | 0.023 |
0.281 | 0.021 | 0.004 |
     | u0/u0/U397/Z          | C v -> Z ^  | HS65_GS_NAND4ABX3 | 0.022 |
0.303 | 0.023 | 0.005 |
     | u0/u0/U395/Z          | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.334 | 0.030 | 0.007 |
     | u0/U72/Z              | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.353 | 0.019 | 0.009 |
     | u0/U144/Z             | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.394 | 0.053 | 0.013 |
     | u0/U229/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.408 | 0.013 | 0.003 |
     | u0/U228/Z             | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.430 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D   | D v         | HS65_GS_DFPQX4    | 0.000 |
0.430 | 0.008 | 0.002 |
     +--------------------------------------------------------------------
-------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/U228/Z -through u0/U229/Z -through
u0/U144/Z  -to u0/w_reg[2][24]/D
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U411/Z -to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U411/Z'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.472
  Slack Time                   0.345
     Clock Rise Edge                0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +--------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q ^ | HS65_GS_DFPQX9    | 0.057 |
0.168 | 0.009 | 0.002 |
```

```
     | u0/FE_OFC30_w3_16_/Z | A ^ -> Z ^  | HS65_GS_BFX18     | 0.053 |
0.221 | 0.086 | 0.110 |
     | u0/u0/U380/Z         | A ^ -> Z v  | HS65_GS_IVX9      | 0.079 |
0.300 | 0.087 | 0.078 |
     | u0/u0/U265/Z         | B v -> Z ^  | HS65_GS_OAI21X3   | 0.045 |
0.345 | 0.016 | 0.001 |
     | u0/u0/U395/Z         | A ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.031 |
0.377 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.396 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.436 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.451 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.472 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.472 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
-------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U9/Z -to
u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U9/Z'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z  -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.537
  Slack Time                   0.410
     Clock Rise Edge                  0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q ^ | HS65_GS_DFPQX9    | 0.057 |
0.168 | 0.009 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A ^ -> Z ^  | HS65_GS_BFX18     | 0.053 |
0.221 | 0.086 | 0.110 |
```

```
     | u0/u0/U380/Z         | A ^ -> Z v  | HS65_GS_IVX9      | 0.079 |
0.300 | 0.087 | 0.078 |
     | u0/u0/U309/Z         | A v -> Z ^  | HS65_GS_NOR2X6    | 0.092 |
0.392 | 0.119 | 0.037 |
     | u0/u0/U396/Z         | A ^ -> Z v  | HS65_GS_AOI212X4  | 0.028 |
0.420 | 0.012 | 0.002 |
     | u0/u0/U395/Z         | C v -> Z ^  | HS65_GS_NAND4ABX3 | 0.021 |
0.441 | 0.030 | 0.007 |
     | u0/U72/Z             | B ^ -> Z v  | HS65_GSS_XOR2X6   | 0.019 |
0.461 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.501 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.516 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.537 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.537 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.689
  Slack Time                   0.562
     Clock Rise Edge                    0.000
     + Clock Network Latency (Prop)     0.111
     = Beginpoint Arrival Time          0.111
     +-------------------------------------------------------------------------
------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U380/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
```

```
     | u0/u0/U256/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U27/Z          | A v -> Z ^  | HS65_GS_IVX9      | 0.054 |
0.521 | 0.070 | 0.041 |
     | u0/u0/U106/Z         | A ^ -> Z v  | HS65_GS_OAI21X3   | 0.026 |
0.547 | 0.012 | 0.003 |
     | u0/u0/U396/Z         | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.563 | 0.018 | 0.002 |
     | u0/u0/U395/Z         | C ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.028 |
0.592 | 0.037 | 0.007 |
     | u0/U72/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.613 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.653 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.668 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.689 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.689 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.689
  Slack Time                   0.562
     Clock Rise Edge                    0.000
     + Clock Network Latency (Prop)     0.111
     = Beginpoint Arrival Time          0.111
     +-------------------------------------------------------------------------
------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
```

```
     | u0/u0/U380/Z          | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
     | u0/u0/U256/Z          | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z           | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U27/Z           | A v -> Z ^  | HS65_GS_IVX9      | 0.054 |
0.521 | 0.070 | 0.041 |
     | u0/u0/U106/Z          | A ^ -> Z v  | HS65_GS_OAI21X3   | 0.026 |
0.547 | 0.012 | 0.003 |
     | u0/u0/U396/Z          | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.563 | 0.018 | 0.002 |
     | u0/u0/U395/Z          | C ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.028 |
0.592 | 0.037 | 0.007 |
     | u0/U72/Z              | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.613 | 0.019 | 0.009 |
     | u0/U144/Z             | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.653 | 0.053 | 0.013 |
     | u0/U229/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.668 | 0.013 | 0.003 |
     | u0/U228/Z             | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.689 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D   | D v         | HS65_GS_DFPQX4    | 0.000 |
0.689 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z-through u0/u0/U380/Z
-through u0/u0/U309/Z -through u0/u0/U256/Z -through u0/u0/U48/Z  -through
u0/u0/U27/Z -through u0/u0/U26/Z -to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U27/Z-through'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z -through u0/u0/U380/Z
-through u0/u0/U309/Z -through u0/u0/U256/Z -through u0/u0/U48/Z  -through
u0/u0/U27/Z -through u0/u0/U26/Z -to u0/w_reg[2][24]/D
No constrained timing paths with given description found.
Paths may be unconstrained (try '-unconstrained' option) or may not exist.

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z-through u0/u0/U380/Z
-through u0/u0/U309/Z -through u0/u0/U256/Z -through u0/u0/U48/Z  -through
u0/u0/U27/Z -through u0/u0/U26/Z -to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U27/Z-through'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z -to u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
```

```
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                          0.012
+ Phase Shift                   0.000
= Required Time                 0.127
  Arrival Time                  0.689
  Slack Time                    0.562
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------------
-------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U380/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
     | u0/u0/U256/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U27/Z          | A v -> Z ^  | HS65_GS_IVX9      | 0.054 |
0.521 | 0.070 | 0.041 |
     | u0/u0/U106/Z         | A ^ -> Z v  | HS65_GS_OAI21X3   | 0.026 |
0.547 | 0.012 | 0.003 |
     | u0/u0/U396/Z         | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.563 | 0.018 | 0.002 |
     | u0/u0/U395/Z         | C ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.028 |
0.592 | 0.037 | 0.007 |
     | u0/U72/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.613 | 0.019 | 0.009 |
     | u0/U144/Z            | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.653 | 0.053 | 0.013 |
     | u0/U229/Z            | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.668 | 0.013 | 0.003 |
     | u0/U228/Z            | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.689 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D  | D v         | HS65_GS_DFPQX4    | 0.000 |
0.689 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
-------------------+
```

```
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Qreport_timing -format {hpin arc cell delay arrival slew
load} -early -from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through
u0/u0/U309/Z -through u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z
-to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for
'u0/w_reg[3][16]/Qreport_timing'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z-through u0/u0/U380/Z
-through u0/u0/U309/Z -through u0/u0/U256/Z -through u0/u0/U48/Z  -through
u0/u0/U27/Z -to u0/w_reg[2][24]/D-to u0/w_reg[2][24]/D
**WARN: (TCLCMD-513):   No matching object found for 'u0/u0/U27/Z-through'
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z   -to
u0/w_reg[2][24]/D
Path 1: MET Hold Check with Pin u0/\w_reg[2][24] /CP
Endpoint:   u0/\w_reg[2][24] /D (v) checked with  leading edge of 'clk'
Beginpoint: u0/\w_reg[3][16] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.115
+ Hold                         0.012
+ Phase Shift                  0.000
= Required Time                0.127
  Arrival Time                 0.689
  Slack Time                   0.562
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.111
     = Beginpoint Arrival Time       0.111
     +-------------------------------------------------------------------
------------------+
     |         Pin          |     Arc     |       Cell        | Delay |
Arrival |  Slew |  Load |
     |                      |             |                   |       |  Time
|       |       |
     |----------------------+-------------+-------------------+-------+------
---+-------+-------|
     | u0/\w_reg[3][16] /CP | CP ^        |                   |       |
0.111 | 0.108 | 0.172 |
     | u0/\w_reg[3][16] /Q  | CP ^ -> Q v | HS65_GS_DFPQX9    | 0.059 |
0.170 | 0.012 | 0.002 |
     | u0/FE_OFC30_w3_16_/Z | A v -> Z v  | HS65_GS_BFX18     | 0.046 |
0.216 | 0.053 | 0.110 |
     | u0/u0/U380/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.093 |
0.309 | 0.127 | 0.078 |
     | u0/u0/U309/Z         | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.065 |
0.373 | 0.070 | 0.037 |
     | u0/u0/U256/Z         | A v -> Z ^  | HS65_GS_IVX9      | 0.056 |
0.429 | 0.060 | 0.030 |
     | u0/u0/U48/Z          | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |
0.467 | 0.041 | 0.024 |
     | u0/u0/U27/Z          | A v -> Z ^  | HS65_GS_IVX9      | 0.054 |
0.521 | 0.070 | 0.041 |
```

```
     | u0/u0/U106/Z          | A ^ -> Z v  | HS65_GS_OAI21X3   | 0.026 |
0.547 | 0.012 | 0.003 |
     | u0/u0/U396/Z          | E v -> Z ^  | HS65_GS_AOI212X4  | 0.016 |
0.563 | 0.018 | 0.002 |
     | u0/u0/U395/Z          | C ^ -> Z v  | HS65_GS_NAND4ABX3 | 0.028 |
0.592 | 0.037 | 0.007 |
     | u0/U72/Z              | B v -> Z v  | HS65_GSS_XOR2X6   | 0.021 |
0.613 | 0.019 | 0.009 |
     | u0/U144/Z             | A v -> Z v  | HS65_GSS_XOR3X2   | 0.040 |
0.653 | 0.053 | 0.013 |
     | u0/U229/Z             | B v -> Z v  | HS65_GSS_XOR2X6   | 0.015 |
0.668 | 0.013 | 0.003 |
     | u0/U228/Z             | C v -> Z v  | HS65_GS_AO22X9    | 0.021 |
0.689 | 0.008 | 0.002 |
     | u0/\w_reg[2][24] /D   | D v         | HS65_GS_DFPQX4    | 0.000 |
0.689 | 0.008 | 0.002 |
     +-------------------------------------------------------------------------
------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -
from u0/w_reg[3][16]/Q  -through u0/u0/U380/Z -through u0/u0/U309/Z -through
u0/u0/U256/Z -through u0/u0/U48/Z  -through u0/u0/U27/Z -through u0/u0/U26/Z
-to u0/w_reg[2][24]/D
```

APPENDIX D: Virtuoso P&R Encounter Import log

```
Checking out Encounter license ...
Encounter_Digital_Impl_Sys_XL 9.1 license checkout succeeded.
You can run 2 CPU jobs with the base license that is currently checked out.
If required, use the setMultiCpuUsage command to enable multi-CPU processing.
This Encounter release has been compiled with OA version 22.04-p058.
*****************************************************************
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*****************************************************************

@(#)CDS: Encounter v09.11-s084_1 (32bit) 04/26/2010 12:41 (Linux 2.6)
@(#)CDS: NanoRoute v09.11-s008 NR100226-1806/USR63-UB (database version 2.30, 93.1.1)
{superthreading v1.14}
@(#)CDS: CeltIC v09.11-s011_1 (32bit) 03/04/2010 09:23:40 (Linux 2.6.9-78.0.25.ELsmp)
@(#)CDS: CTE 09.11-s016_1 (32bit) Apr  8 2010 03:34:50 (Linux 2.6.9-78.0.25.ELsmp)
@(#)CDS: CPE v09.11-s023
--- Starting "Encounter v09.11-s084_1" on Thu May  5 10:45:24 2011 (mem=46.5M) ---
--- Running on sody.ece.umn.edu (x86_64 w/Linux 2.6.18-194.26.1.el5) ---
This version was compiled on Mon Apr 26 12:41:13 PDT 2010.
Set DBUPerIGU to 1000.
Set net toggle Scale Factor to 1.00
Set Shrink Factor to 1.00000
*** Memory pool thread-safe mode activated.
<CMD> loadConfig OA_load.conf 0
Reading config file - OA_load.conf
<CMD> commitConfig
Reading tech data from OA Library 'BUDAPEST_MULTICORE' ...
**WARN: (ENCOAX-793):  Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
FE units: 0.001 microns/dbu, OA units: 0.001 microns/dbu, Conversion factor: 1
**WARN: (ENCOAX-775):  Layer 'overlap' has already been defined in Encounter database, the
contents will be skipped.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_M5X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_M4X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_M3X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_M2X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_M1'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M7Z_PO'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725):  More than 3 layers defined for via 'M6Z_M4X'. This via can not be read in
Encounter. Check the via information in OA database.
```

```
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M6Z_M3X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M6Z_M2X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M6Z_M1'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M6Z_PO'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M5X_M3X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M5X_M2X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M5X_M1'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M5X_PO'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M4X_M2X'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M4X_M1'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M4X_PO'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M3X_M1'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (ENCOAX-725): More than 3 layers defined for via 'M3X_PO'. This via can not be read in
Encounter. Check the via information in OA database.
**WARN: (EMS-62):     Message <ENCOAX-725> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (ENCOAX-735): Could not find top metal layer for cut layer 'CB'. Check the Layer
information in OA database.
Reading OA reference Library 'cmos065' ...
**WARN: (ENCOAX-793): Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
**WARN: (ENCOAX-735): Could not find top metal layer for cut layer 'CB'. Check the Layer
information in OA database.
**WARN: (ENCOAX-793): Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
Reading OA reference Library 'BUDAPEST_MULTICORE' ...
**WARN: (ENCOAX-793): Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
**WARN: (ENCOAX-735): Could not find top metal layer for cut layer 'CB'. Check the Layer
information in OA database.
**WARN: (ENCOAX-793): Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
Reading OA reference Library 'CORE65GPSVT' ...
**WARN: (ENCOAX-793): Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
Set DBUPerIGU to M1 pitch 200.
```

```
**WARN: (ENCSPR-101): No metal layer defined after cut layer CB, FE will ignore this cut layer.
Initializing default via types and wire widths ...
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GSS_XOR3X2'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-756): Macro 'HS65_GSS_XOR3X2' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is created and used for this macro using
height 2.6000 that matches the macro SIZE height, and width 0.2000 that matches the m2 routing
pitch.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GSS_XOR3X2' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GSS_XOR2X6'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GSS_XOR2X6' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GSS_XOR2X6' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI212X3'. Check if the macro in
OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_OAI212X3' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI212X3' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_DFPQX4'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_DFPQX4' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_DFPQX4' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_CBI4I6X5'. Check if the macro in
OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_CBI4I6X5' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_CBI4I6X5' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GSS_XNOR3X2'. Check if the macro in
OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GSS_XNOR3X2' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GSS_XNOR3X2' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_BFX9'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_BFX9' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_BFX9' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
```

**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_AO22X9'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_AO22X9' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_AO22X9' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI212X5'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_OAI212X5' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI212X5' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_NOR4ABX2'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_NOR4ABX2' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_NOR4ABX2' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI22X6'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_OAI22X6' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI22X6' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OA212X4'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_OA212X4' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OA212X4' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_AOI13X5'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_AOI13X5' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_AOI13X5' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_NAND2X7'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_NAND2X7' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_NAND2X7' in Encounter database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731): Invalid layer number 236 received for the layers specified in OA technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI311X5'. Check if the macro in OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755): Macro 'HS65_GS_OAI311X5' has no SITE statement and it is a class CORE macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with height 2.6000 that matches the macro SIZE height.

```
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI311X5' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731):  Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI211X5'. Check if the macro in
OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_OAI211X5' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI211X5' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731):  Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_NAND4ABX3'. Check if the macro in
OA database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_NAND4ABX3' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_NAND4ABX3' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731):  Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_IVX9'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_IVX9' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_IVX9' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731):  Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_AOI32X5'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_AOI32X5' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_AOI32X5' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (ENCOAX-731):  Invalid layer number 236 received for the layers specified in OA
technology data. Check the layer information in OA database.
**ERROR: (ENCOAX-750): Undefined site 'CORE' in macro 'HS65_GS_OAI21X3'. Check if the macro in OA
database has correct site information and if the site is defined in OA technology database.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_OAI21X3' has no SITE statement and it is a class CORE macro
that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site with
height 2.6000 that matches the macro SIZE height.
**ERROR: (ENCOAX-757): Can not find sitePattern 'CORE' for macro 'HS65_GS_OAI21X3' in Encounter
database. Check if the site is defined correctly in OA technology database.
**WARN: (EMS-62):      Message <ENCOAX-731> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (EMS-62):      Message <ENCOAX-750> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (ENCOAX-755):  Macro 'HS65_GS_AOI222X2' has no SITE statement and it is a class CORE
macro that requires a SITE statement. The SITE ENC_CORE_0 is chosen because it is a core site
with height 2.6000 that matches the macro SIZE height.
**WARN: (EMS-62):      Message <ENCOAX-757> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
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a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (EMS-62):      Message <ENCOAX-755> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
**WARN: (ENCOAX-735):  Could not find top metal layer for cut layer 'CB'. Check the Layer
information in OA database.

There were 52 layout cells that used automatic abstract creation. See aes_cipher_top.oaread.rpt
for a list of all the cells.

**WARN: (ENCOAX-1037): There were 52 cells with a total of 257 pins that were missing process
antenna data. Process antenna violations will not be detected for any routing attached to these
pins. You should add process antenna data to your OA cells to avoid this problem. See
aes_cipher_top.oaread.rpt for more details.


Power Planner/ViaGen version 8.1.46 promoted on 02/17/2009.
viaInitial starts at Thu May  5 10:46:08 2011
**WARN: (ENCPP-549):   VIARULE 'M7Z_M6Z_V' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA6' SAMENET SPACING (edge-2-edge) 0.540.
**WARN: (ENCPP-549):   VIARULE 'M7Z__M6Z_H' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA6' SAMENET SPACING (edge-2-edge) 0.540.
**WARN: (ENCPP-549):   VIARULE 'M7Z__M6Z' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA6' SAMENET SPACING (edge-2-edge) 0.540.
**WARN: (ENCPP-549):   VIARULE 'M6Z_M5X_V' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA5' SAMENET SPACING (edge-2-edge) 0.540.
**WARN: (ENCPP-549):   VIARULE 'M6Z__M5X_H' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA5' SAMENET SPACING (edge-2-edge) 0.540.
**WARN: (ENCPP-549):   VIARULE 'M6Z__M5X' SPACING (center-2-center) 0.700 is smaller than cut
layer 'VIA5' SAMENET SPACING (edge-2-edge) 0.540.
viaInitial ends at Thu May  5 10:46:08 2011
**WARN: (ENCOAX-1142): Current Encounter hierarchy has cds.lib plug-in installed and both cds.lib
& lib.defs files are present in the current directory. The cds.lib file will be used. The
lib.defs file will be ignored and it will not be updated.
**WARN: (ENCOAX-793):  Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
Reading EMH from OA ...
Backslashed names will retain backslash and a trailing blank character.

*** Memory Usage v0.159.2.6.2.1 (Current mem = 304.809M, initial mem = 46.480M) ***
Set top cell to aes_cipher_top.
Reading max timing library 'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib' ...
**WARN: (ENCTS-124):   Timing library description of pin 'vdd!' is missing from cell
'HS65_GSS_XNOR2X6' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'gnd!' is missing from cell
'HS65_GSS_XNOR2X6' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'vdd!' is missing from cell
'HS65_GSS_XNOR3X2' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'gnd!' is missing from cell
'HS65_GSS_XNOR3X2' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'vdd!' is missing from cell
'HS65_GSS_XOR2X6' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'gnd!' is missing from cell
'HS65_GSS_XOR2X6' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'vdd!' is missing from cell
'HS65_GSS_XOR3X2' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):   Timing library description of pin 'gnd!' is missing from cell
'HS65_GSS_XOR3X2' in timing library 'CORE65GPSVT'.
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**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AO112X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AO112X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AO12X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AO12X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AO22X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AO22X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AO312X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AO312X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AO31X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AO31X9' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'vdd!' is missing from cell
'HS65_GS_AOI12X2' in timing library 'CORE65GPSVT'.
**WARN: (ENCTS-124):  Timing library description of pin 'gnd!' is missing from cell
'HS65_GS_AOI12X2' in timing library 'CORE65GPSVT'.
**WARN: (EMS-62):     Message <ENCTS-124> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
 read 52 cells in library 'CORE65GPSVT'
ignored 814 cells in library 'CORE65GPSVT' because they are not defined in the LEF file, and they
are not used in the verilog netlist.
Reading max timing library 'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib' ...
 read 0 cells in library 'CLOCK65GPSVT'
ignored 110 cells in library 'CLOCK65GPSVT' because they are not defined in the LEF file, and
they are not used in the verilog netlist.
Reading max timing library 'LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib' ...
 read 0 cells in library 'PRHS65'
ignored 10 cells in library 'PRHS65' because they are not defined in the LEF file, and they are
not used in the verilog netlist.
Reading min timing library 'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_bc_1.10V_m40C.lib' ...
 read 52 cells in library 'CORE65GPSVT'
ignored 814 cells in library 'CORE65GPSVT' because they are not defined in the LEF file, and they
are not used in the verilog netlist.
Reading min timing library 'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_bc_1.10V_m40C.lib' ...
 read 0 cells in library 'CLOCK65GPSVT'
ignored 110 cells in library 'CLOCK65GPSVT' because they are not defined in the LEF file, and
they are not used in the verilog netlist.
Reading min timing library 'LIBRARIES/PRHS65/libs/PRHS65_bc_1.30V_m40C.lib' ...
 read 0 cells in library 'PRHS65'
ignored 10 cells in library 'PRHS65' because they are not defined in the LEF file, and they are
not used in the verilog netlist.
Reading max timing library 'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.00, 25.00) of timing library 'CORE65GPSVT' does
not match with previously read timing library of same name with nominal PVT (1.20, 0.90, 125.00).
To read this library change the library name.
**ERROR: (TECHLIB-281):       Attempt to read .lib library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' failed
Reading max timing library 'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.00, 25.00) of timing library 'CLOCK65GPSVT' does
not match with previously read timing library of same name with nominal PVT (1.20, 0.90, 125.00).
To read this library change the library name.
 read 0 cells in library 'CLOCK65GPSVT'
ignored 110 cells in library 'CLOCK65GPSVT' because they are not defined in the LEF file, and
they are not used in the verilog netlist.
Reading max timing library 'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib' ...
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**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.20, 25.00) of timing library 'PRHS65' does not
match with previously read timing library of same name with nominal PVT (1.20, 1.10, 125.00). To
read this library change the library name.
 read 0 cells in library 'PRHS65'
ignored 10 cells in library 'PRHS65' because they are not defined in the LEF file, and they are
not used in the verilog netlist.
Reading min timing library 'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.00, 25.00) of timing library 'CORE65GPSVT' does
not match with previously read timing library of same name with nominal PVT (0.80, 1.10, -40.00).
To read this library change the library name.
**ERROR: (TECHLIB-281):       Attempt to read .lib library
'LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib' failed
Reading min timing library 'LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib' ...
**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.00, 25.00) of timing library 'CLOCK65GPSVT' does
not match with previously read timing library of same name with nominal PVT (0.80, 1.10, -40.00).
To read this library change the library name.
 read 0 cells in library 'CLOCK65GPSVT'
ignored 110 cells in library 'CLOCK65GPSVT' because they are not defined in the LEF file, and
they are not used in the verilog netlist.
Reading min timing library 'LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib' ...
**ERROR: (ENCTS-296): The nominal PVT (1.00, 1.20, 25.00) of timing library 'PRHS65' does not
match with previously read timing library of same name with nominal PVT (0.80, 1.30, -40.00). To
read this library change the library name.
 read 0 cells in library 'PRHS65'
ignored 10 cells in library 'PRHS65' because they are not defined in the LEF file, and they are
not used in the verilog netlist.
*** End library_loading (cpu=0.09min, mem=14.9M, fe_cpu=0.17min, fe_mem=319.7M) ***
Starting recursive module instantiation check.
No recursion found.
Building hierarchical netlist for Cell aes_cipher_top ...
**WARN: (ENCDB-2077): Net \vdd!  exceeded maximum number of output terminals (8191)
**WARN: (ENCDB-2077): Net \gnd!  exceeded maximum number of output terminals (8191)
*** Netlist is unique.
** info: there are 105 modules.
** info: there are 9809 stdCell insts.

*** Memory Usage v0.159.2.6.2.1 (Current mem = 325.492M, initial mem = 46.480M) ***
CTE reading timing constraint file 'aes_cipher_top.sdc' ...
aes_cipher_top
INFO (CTE): constraints read successfully
*** Read timing constraints (cpu=0:00:00.1 mem=330.4M) ***
Total number of combinational cells: 0
Total number of sequential cells: 3
Total number of tristate cells: 0
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers:
Total number of usable buffers: 0
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters:
Total number of usable inverters: 0
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells:
Total number of identified usable delay cells: 0
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0
No delay cells were detected in the set of buffers. Buffers will be used to fix hold violations.
*info: set bottom ioPad orient R0
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
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Set Input Pin Transition Delay as 0.1 ps.
PreRoute Cap Scale Factor :        1.00
PreRoute Res Scale Factor :        1.00
PostRoute Cap Scale Factor :       1.00
PostRoute Res Scale Factor :       1.00
PostRoute XCap Scale Factor :      1.00

PreRoute Clock Cap Scale Factor :  1.00      [Derived from postRoute_cap (effortLevel low)]
PreRoute Clock Res Scale Factor :  1.00      [Derived from postRoute_res (effortLevel low)]
PostRoute Clock Cap Scale Factor : 1.00      [Derived from postRoute_cap (effortLevel low)]
PostRoute Clock Res Scale Factor : 1.00      [Derived from postRoute_res (effortLevel low)]
**WARN: (ENCOAX-793):  Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
----- oaIn -----------
Restoring OA database: Lib BUDAPEST_MULTICORE, Cell aes_cipher_top, View layout.routed
**WARN: (ENCOAX-1142): Current Encounter hierarchy has cds.lib plug-in installed and both cds.lib
& lib.defs files are present in the current directory. The cds.lib file will be used. The
lib.defs file will be ignored and it will not be updated.
**WARN: (ENCOAX-793):  Problem reading library definition file
/scratch/arvind/65nm/522/cmos065_golden/techlib_for_encounter_2/encounter/cds.lib : Unable to
open library functional at path
/home/apps/common/cadence/Linux/edi_91/tools.lnx86/dfII/etc/cdslib/artist/functional: Invalid Lib
Path.
FE units: 0.001 microns/dbu, OA units: 0.001 microns/dbu, Conversion factor: 1
**WARN: (ENCOAX-571):  Property 'lxInternal' from OA is of type 'HierProp' which is not supported
in Encounter. This property can not be translated and will be ignored.
No new Ext DEF rule to be processed.
**WARN: (ENCOAX-269):  IO box attributes are not specified in the OA database. IO box co-
ordinates will be calculated from Floorplan data.
New IO box co-ordinates are : LowerLeft = (0,0), UpperRight = (240430,240430).
**WARN: (ENCOAX-790):  Core box attributes are not specified in the OA database. Core box co-
ordinates will be calculated from Floorplan data by using ui_core_to_* settings from the
configuration file.
New Core box co-ordinates are : LowerLeft = (0,0), UpperRight = (240430,240430).
Set FPlanBox to (0 0 240430 240430)
2 Power/Ground nets were created.
Extracting standard cell pins and blockage ......
Pin and blockage extraction finished
Extracting macro/IO cell pins and blockage ......
Pin and blockage extraction finished
**WARN: (ENCOAX-787):  Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M5X_M4X_H_via' was found with 'W' orientation. A
new via cell 'M5X_M4X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787):  Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
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**WARN: (ENCOAX-787): Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M2X_M1_H_via' was found with 'W' orientation. A
new via cell 'M2X_M1_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M4X_M3X_H_via' was found with 'W' orientation. A
new via cell 'M4X_M3X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (ENCOAX-787): Via instance of via cell 'M3X_M2X_H_via' was found with 'W' orientation. A
new via cell 'M3X_M2X_H_via' will be created by rotating the original via geometries and
instantiated with R0 orientation.
**WARN: (EMS-62):     Message <ENCOAX-787> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
Read 275824 Routes.
Special routes: 382 routes, 0 vias.
**WARN: (ENCDB-2074): Escape fterm name for cell (aes_cipher_top) from (GND!) to (\GND! ).
**WARN: (ENCDB-2074): Escape fterm name for cell (aes_cipher_top) from (gnd!) to (\gnd! ).
**WARN: (ENCDB-2074): Escape fterm name for cell (aes_cipher_top) from (vdd!) to (\vdd! ).
**WARN: (ENCOAX-516): There are 1000 unreadable OA marker objects (violation markers) created by
tools other than Encounter that will be ignored. Only violations created and written by Encounter
into an OpenAccess database can be read back from OpenAccess.
TIMER: Purge OA from memory: 0h 0m  0.02s cpu {0h 0m 0s elapsed} Memory = -2.6
TIMER: oaIn total process: 0h 0m  1.94s cpu {0h 0m 2s elapsed} Memory = 16.1
<CMD> fit
<CMD> setDrawView fplan
<CMD> readCapTable -typical
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable -best
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Best.captable -worst
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable
**WARN: (ENCEXT-3497): Options '-best/-worst/-typical' of 'readCapTable' are obsolete. For single
mode two corner analysis and optimization, use MMMC setup instead of reading multiple captables
through command 'readCapTable'. The obsolete options still works in this release, but to avoid
this warning and to ensure compatibility with future releases, update your script and
configuration file to use MMMC.
```

```
Reading Three Cap Table files:  -typical
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable -best
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Best.captable -worst
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable  ...
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMAX.
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMIN.
Cap Table was created using Encounter 04.20-s447_1.
Process name: cmos065_7m4x0y2z_GL_RCMAX.
Reading EXTENDED_CAP_TABLE section completed.
Allocated an empty WireEdgeEnlargement table [0][6]
Allocated an empty WireEdgeEnlargement table [1][6]
Allocated an empty WireEdgeEnlargement table [2][6]
Allocated an empty WireEdgeEnlargement table [0][7]
Allocated an empty WireEdgeEnlargement table [1][7]
Allocated an empty WireEdgeEnlargement table [2][7]
Three process corner capacitance table is used.
<CMD> setExtractRCMode -engine postRoute -force true
<CMD> extractRC
Extraction called for design 'aes_cipher_top' of instances=9809 and nets=10071 using extraction
engine 'postRoute' at effort level 'low' .
**WARN: (ENCEXT-3530): Use of command 'setDesignMode -process <process_node>' prior to extraction
is recommended for maximum accuracy and optimal automatic threshold setting.
Detail RC Extraction called for design aes_cipher_top.
Process corner(s) are loaded.
Loading corner...  Typical_Case :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable
Loading corner...  Best_Case    :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Best.captable
Loading corner...  Worst_Case   :
/project/chriskim02/tools/cadence/st65nm_421/adv_EncounterTechnoKit_cmos065_7m4x0y2z_4.2/TECH/cmo
s065_7m4x0y2z_Worst.captable
extractDetailRC Option : -outfile ./aes_cipher_top_I62BUW_28067.rcdb.d  -3Corners
RC Mode: Detail [Extended CapTable, RC Table Resistances, 3 Process Corners]
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor    : 1.00000
Coupling Cap. Scaling Factor : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res. Scaling Factor    : 1.00000
Shrink Factor                : 1.00000
Width-based sheet resistance table (silicon width) is used ...
**WARN: (ENCEXT-3082): 3523 nets will be ignored in Native Extraction. The name of nets are saved
in aes_cipher_top.opennet. Run extraction with '-specialNet' option if the design contains
special routes. If '-specialNet' option has been used, these nets are either open, or have
polygons or other shapes which are not supported by Native Extraction engine. You can use QRC
extraction to extract parasitics of these nets. Use 'verifyConnectivity' command to determine the
physical openness of these nets.
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 347.6M)
Creating parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq' for storing RC.
Extracted 10.0015% (CPU Time= 0:00:00.3  MEM= 354.5M)
Extracted 20.0015% (CPU Time= 0:00:00.4  MEM= 358.2M)
Extracted 30.0015% (CPU Time= 0:00:00.5  MEM= 358.9M)
Extracted 40.0015% (CPU Time= 0:00:00.6  MEM= 360.5M)
Extracted 50.0015% (CPU Time= 0:00:00.8  MEM= 361.6M)
Extracted 60.0015% (CPU Time= 0:00:00.9  MEM= 362.7M)
Extracted 70.0015% (CPU Time= 0:00:01.2  MEM= 364.5M)
Extracted 80.0015% (CPU Time= 0:00:01.4  MEM= 365.5M)
Extracted 90.0015% (CPU Time= 0:00:01.7  MEM= 367.2M)
Extracted 100% (CPU Time= 0:00:02.6  MEM= 367.2M)
Nr. Extracted Resistors     : 225546
Nr. Extracted Ground Cap.   : 231781
Nr. Extracted Coupling Cap. : 322800
```

```
Opening parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq' for reading.
Filtering XCap in 'relativeOnly' mode using values relative_c_threshold=0.03 and
total_c_threshold=5fF.
**WARN: (ENCEXT-3082): 3523 nets will be ignored in Native Extraction. The name of nets are saved
in aes_cipher_top.opennet. Run extraction with '-specialNet' option if the design contains
special routes. If '-specialNet' option has been used, these nets are either open, or have
polygons or other shapes which are not supported by Native Extraction engine. You can use QRC
extraction to extract parasitics of these nets. Use 'verifyConnectivity' command to determine the
physical openness of these nets.
Checking LVS Completed (CPU Time= 0:00:00.1  MEM= 347.6M)
Creating parasitic data file './aes_cipher_top_I62BUW_28067.rcdb_Filter.rcdb.d/header.seq' for
storing RC.
Closing parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq'. 6547 times net's
RC data read were performed.
Opening parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq' for reading.
Detail RC Extraction DONE (CPU Time: 0:00:03.3  Real Time: 0:00:05.0  MEM: 347.621M)
<CMD> rcOut -spef signoff.spef
Opening parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq' for reading.
Dumping Spef file.....
RC Out has the following PVT Info:
   RC-worst
Printing D_NET...
Detail RC Out Completed (CPU Time= 0:00:00.9  MEM= 347.6M)
Closing parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq'. 6547 times net's
RC data read were performed.
<CMD> setAnalysisMode -analysisType single -checkType setup -skew true -clockPropagation
sdccontrol
<CMD> report_timing -summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:01.7, MEM = 354.7M)
Number of Loop : 0
Start delay calculation (mem=354.680M)...
delayCal using detail RC...
Opening parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq' for reading.
RC Database In Completed (CPU Time= 0:00:00.2  MEM= 368.7M)
Width-based sheet resistance table (silicon width) is used ...
Closing parasitic data file './aes_cipher_top_I62BUW_28067.rcdb.d/header.seq'. 6547 times net's
RC data read were performed.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[124] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
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```
**WARN: (ENCDC-348):   The output pin \|text_out_reg[124] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[120] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[120] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[57] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[57] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[58] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[58] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (EMS-62):     Message <ENCDC-348> has exceeded the default message display limit of 20.
To avoid this warning, increase the display limit per unique message
by using the set_message_limit <number> command. The message limit can
be removed by using the unset_message_limit command. Note that setting
a very large number using the set_message_limit command or removing the
message limit using the unset_message_limit command can significantly
increase the log file size.
Delay calculation completed. (cpu=0:00:02.0 real=0:00:03.0 mem=373.676M 0)
*** CDM Built up (cpu=0:00:05.3  real=0:00:06.0  mem= 373.7M) ***
     +-------------------------------------------------------------------------------------------------
-------------------------------------------------+
     |  Path |                          Pin | Cause                                                  |
Slack | Arrival | Required |     Phase |     Other |
     |   No. |                              |                                                        |
|         |          |           |     Phase |
     |-------+--------------------------+--------------------------------------------------------+--
------+---------+----------+-----------+-----------|
     |     1 |    \|u0|w_reg[2][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[2][24] /C | -
1.420 |   3.848 |    2.428 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |     2 |    \|u0|w_reg[3][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][24] /C | -
1.121 |   3.494 |    2.373 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |     3 |       \|sa21_reg[4] /D v | VIOLATED Setup Check with Pin \|sa21_reg[4] /CP    | -
1.119 |   3.472 |    2.352 | clk(D)(P) | clk(C)(P) |
     |     4 |    \|u0|w_reg[3][25] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][25] /C | -
1.097 |   3.530 |    2.433 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |     5 |    \|u0|w_reg[2][25] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][25] /C | -
1.082 |   3.498 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |     6 |     \|u0|w_reg[3][0] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][0] /CP | -
1.080 |   3.496 |    2.416 | clk(D)(P) | clk(C)(P) |
     |     7 |     \|u0|w_reg[2][0] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][0] /CP | -
1.026 |   3.443 |    2.417 | clk(D)(P) | clk(C)(P) |
     |     8 |    \|u0|w_reg[3][30] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][30] /C | -
1.014 |   3.429 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |     9 |    \|u0|w_reg[2][30] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][30] /C | -
0.987 |   3.403 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |    10 |    \|u0|w_reg[3][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][31] /C | -
0.982 |   3.396 |    2.414 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                      |
|         |          |           |           |
     |    11 |    \|u0|w_reg[2][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][31] /C | -
0.961 |   3.377 |    2.416 | clk(D)(P) | clk(C)(P) |
```

```
    |       |                           | P                                             |
|       |         |           |          |
    |    12 |     \|u0|w_reg[1][0] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][0] /CP | -
0.887 |   3.302 |    2.415 | clk(D)(P) | clk(C)(P) |
    |    13 |    \|u0|w_reg[3][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][26] /C | -
0.886 |   3.302 |    2.416 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    14 |       \|sa21_reg[1] /D v | VIOLATED Setup Check with Pin \|sa21_reg[1] /CP    | -
0.883 |   3.251 |    2.368 | clk(D)(P) | clk(C)(P) |
    |    15 |     \|u0|w_reg[3][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][6] /CP | -
0.876 |   3.291 |    2.416 | clk(D)(P) | clk(C)(P) |
    |    16 |       \|sa10_reg[4] /D v | VIOLATED Setup Check with Pin \|sa10_reg[4] /CP    | -
0.862 |   3.214 |    2.351 | clk(D)(P) | clk(C)(P) |
    |    17 |     \|u0|w_reg[3][7] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][7] /CP | -
0.846 |   3.263 |    2.416 | clk(D)(P) | clk(C)(P) |
    |    18 |    \|u0|w_reg[2][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][26] /C | -
0.828 |   3.239 |    2.411 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    19 |    \|u0|w_reg[1][25] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][25] /C | -
0.793 |   3.220 |    2.428 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    20 |     \|u0|w_reg[2][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][6] /CP | -
0.784 |   3.199 |    2.414 | clk(D)(P) | clk(C)(P) |
    |    21 |       \|sa31_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[1] /CP    | -
0.752 |   3.168 |    2.416 | clk(D)(P) | clk(C)(P) |
    |    22 |    \|u0|w_reg[1][30] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][30] /C | -
0.752 |   3.184 |    2.432 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    23 |     \|u0|w_reg[2][7] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][7] /CP | -
0.737 |   3.153 |    2.416 | clk(D)(P) | clk(C)(P) |
    |    24 |    \|u0|w_reg[1][31] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][31] /C | -
0.696 |   3.123 |    2.428 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    25 |     \|u0|w_reg[1][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][6] /CP | -
0.680 |   3.094 |    2.415 | clk(D)(P) | clk(C)(P) |
    |    26 |    \|u0|w_reg[1][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][24] /C | -
0.657 |   3.087 |    2.430 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    27 |     \|u0|w_reg[3][3] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][3] /CP | -
0.650 |   3.065 |    2.415 | clk(D)(P) | clk(C)(P) |
    |    28 |     \|u0|w_reg[0][0] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][0] /CP | -
0.618 |   3.049 |    2.431 | clk(D)(P) | clk(C)(P) |
    |    29 |    \|u0|w_reg[3][21] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][21] /C | -
0.601 |   3.017 |    2.416 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    30 |    \|u0|w_reg[3][27] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][27] /C | -
0.600 |   3.009 |    2.409 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    31 |     \|u0|w_reg[1][7] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][7] /CP | -
0.591 |   3.007 |    2.415 | clk(D)(P) | clk(C)(P) |
    |    32 |    \|u0|w_reg[1][26] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][26] /C | -
0.586 |   3.020 |    2.434 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    33 |    \|u0|w_reg[3][29] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][29] /C | -
0.570 |   2.986 |    2.416 | clk(D)(P) | clk(C)(P) |
    |       |                           | P                                             |
|       |         |           |          |
    |    34 |     \|u0|w_reg[2][3] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][3] /CP | -
0.554 |   2.967 |    2.413 | clk(D)(P) | clk(C)(P) |
```

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     |    35 |     \|u0|w_reg[3][5] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][5] /CP | -
0.543 |   2.958 |    2.416 | clk(D)(P) | clk(C)(P) |
     |    36 |     \|u0|w_reg[3][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][4] /CP | -
0.542 |   2.958 |    2.415 | clk(D)(P) | clk(C)(P) |
     |    37 |    \|u0|w_reg[2][21] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][21] /C | -
0.539 |   2.955 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    38 |       \|sa20_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[1] /CP    | -
0.534 |   2.939 |    2.405 | clk(D)(P) | clk(C)(P) |
     |    39 |    \|u0|w_reg[2][27] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][27] /C | -
0.524 |   2.936 |    2.412 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    40 |    \|u0|w_reg[2][29] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][29] /C | -
0.505 |   2.922 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    41 |       \|sa10_reg[0] /D v | VIOLATED Setup Check with Pin \|sa10_reg[0] /CP    | -
0.485 |   2.886 |    2.401 | clk(D)(P) | clk(C)(P) |
     |    42 |    \|u0|w_reg[3][28] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][28] /C | -
0.473 |   2.888 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    43 |    \|u0|w_reg[3][23] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][23] /C | -
0.469 |   2.855 |    2.387 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    44 |       \|sa30_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[1] /CP    | -
0.468 |   2.878 |    2.410 | clk(D)(P) | clk(C)(P) |
     |    45 |     \|u0|w_reg[2][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][4] /CP | -
0.465 |   2.882 |    2.417 | clk(D)(P) | clk(C)(P) |
     |    46 |     \|u0|w_reg[0][6] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][6] /CP | -
0.463 |   2.893 |    2.430 | clk(D)(P) | clk(C)(P) |
     |    47 |       \|sa20_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[0] /CP    | -
0.453 |   2.869 |    2.416 | clk(D)(P) | clk(C)(P) |
     |    48 |       \|sa13_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[4] /CP    | -
0.453 |   2.824 |    2.372 | clk(D)(P) | clk(C)(P) |
     |    49 |     \|u0|w_reg[2][5] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][5] /CP | -
0.437 |   2.854 |    2.417 | clk(D)(P) | clk(C)(P) |
     |    50 |       \|sa01_reg[5] /D v | VIOLATED Setup Check with Pin \|sa01_reg[5] /CP    | -
0.429 |   2.817 |    2.388 | clk(D)(P) | clk(C)(P) |
     |    51 |    \|u0|w_reg[3][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][20] /C | -
0.417 |   2.833 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    52 |     \|u0|w_reg[3][2] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][2] /CP | -
0.409 |   2.825 |    2.416 | clk(D)(P) | clk(C)(P) |
     |    53 |       \|sa20_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[4] /CP    | -
0.408 |   2.822 |    2.413 | clk(D)(P) | clk(C)(P) |
     |    54 |       \|sa31_reg[4] /D v | VIOLATED Setup Check with Pin \|sa31_reg[4] /CP    | -
0.407 |   2.783 |    2.376 | clk(D)(P) | clk(C)(P) |
     |    55 |       \|sa31_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[5] /CP    | -
0.404 |   2.812 |    2.407 | clk(D)(P) | clk(C)(P) |
     |    56 |       \|sa20_reg[3] /D v | VIOLATED Setup Check with Pin \|sa20_reg[3] /CP    | -
0.394 |   2.800 |    2.405 | clk(D)(P) | clk(C)(P) |
     |    57 |       \|sa21_reg[3] /D v | VIOLATED Setup Check with Pin \|sa21_reg[3] /CP    | -
0.387 |   2.775 |    2.388 | clk(D)(P) | clk(C)(P) |
     |    58 |    \|u0|w_reg[2][28] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][28] /C | -
0.380 |   2.796 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |    59 |       \|sa11_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[6] /CP    | -
0.379 |   2.793 |    2.414 | clk(D)(P) | clk(C)(P) |
     |    60 |       \|sa11_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[3] /CP    | -
0.373 |   2.784 |    2.411 | clk(D)(P) | clk(C)(P) |
     |    61 |       \|sa23_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[4] /CP    | -
0.372 |   2.773 |    2.401 | clk(D)(P) | clk(C)(P) |
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     |    62 |        \|sa11_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[4] /CP    | -
0.364 |   2.778 |    2.414 | clk(D)(P) | clk(C)(P) |
     |    63 |     \|u0|w_reg[1][3] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][3] /CP | -
0.364 |   2.800 |    2.436 | clk(D)(P) | clk(C)(P) |
     |    64 |        \|sa11_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[1] /CP    | -
0.362 |   2.776 |    2.414 | clk(D)(P) | clk(C)(P) |
     |    65 |    \|u0|w_reg[1][21] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][21] /C | -
0.355 |   2.789 |    2.435 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    66 |    \|u0|w_reg[3][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][15] /C | -
0.351 |   2.765 |    2.414 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    67 |        \|sa30_reg[7] /D v | VIOLATED Setup Check with Pin \|sa30_reg[7] /CP    | -
0.348 |   2.723 |    2.375 | clk(D)(P) | clk(C)(P) |
     |    68 |     \|u0|w_reg[2][2] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][2] /CP | -
0.346 |   2.758 |    2.412 | clk(D)(P) | clk(C)(P) |
     |    69 |        \|sa00_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[1] /CP    | -
0.345 |   2.753 |    2.409 | clk(D)(P) | clk(C)(P) |
     |    70 |        \|sa20_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[7] /CP    | -
0.343 |   2.765 |    2.422 | clk(D)(P) | clk(C)(P) |
     |    71 |     \|u0|w_reg[0][7] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][7] /CP | -
0.342 |   2.777 |    2.435 | clk(D)(P) | clk(C)(P) |
     |    72 |        \|sa11_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[0] /CP    | -
0.341 |   2.757 |    2.415 | clk(D)(P) | clk(C)(P) |
     |    73 |        \|sa30_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[0] /CP    | -
0.336 |   2.710 |    2.375 | clk(D)(P) | clk(C)(P) |
     |    74 |        \|sa00_reg[0] /D v | VIOLATED Setup Check with Pin \|sa00_reg[0] /CP    | -
0.335 |   2.732 |    2.397 | clk(D)(P) | clk(C)(P) |
     |    75 |    \|u0|w_reg[2][23] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][23] /C | -
0.334 |   2.751 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    76 |        \|sa01_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[1] /CP    | -
0.328 |   2.743 |    2.414 | clk(D)(P) | clk(C)(P) |
     |    77 |        \|sa01_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[7] /CP    | -
0.328 |   2.740 |    2.412 | clk(D)(P) | clk(C)(P) |
     |    78 |     \|u0|w_reg[1][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][4] /CP | -
0.323 |   2.740 |    2.417 | clk(D)(P) | clk(C)(P) |
     |    79 |        \|sa33_reg[4] /D v | VIOLATED Setup Check with Pin \|sa33_reg[4] /CP    | -
0.317 |   2.698 |    2.381 | clk(D)(P) | clk(C)(P) |
     |    80 |    \|u0|w_reg[2][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][20] /C | -
0.316 |   2.732 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    81 |        \|sa00_reg[7] /D v | VIOLATED Setup Check with Pin \|sa00_reg[7] /CP    | -
0.315 |   2.697 |    2.382 | clk(D)(P) | clk(C)(P) |
     |    82 |        \|sa21_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[0] /CP    | -
0.310 |   2.721 |    2.410 | clk(D)(P) | clk(C)(P) |
     |    83 |        \|sa10_reg[7] /D v | VIOLATED Setup Check with Pin \|sa10_reg[7] /CP    | -
0.307 |   2.704 |    2.397 | clk(D)(P) | clk(C)(P) |
     |    84 |        \|sa30_reg[4] /D v | VIOLATED Setup Check with Pin \|sa30_reg[4] /CP    | -
0.306 |   2.683 |    2.377 | clk(D)(P) | clk(C)(P) |
     |    85 |    \|u0|w_reg[1][27] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][27] /C | -
0.305 |   2.739 |    2.434 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    86 |        \|sa23_reg[3] /D v | VIOLATED Setup Check with Pin \|sa23_reg[3] /CP    | -
0.301 |   2.678 |    2.378 | clk(D)(P) | clk(C)(P) |
     |    87 |    \|u0|w_reg[0][30] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][30] /C | -
0.300 |   2.712 |    2.411 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    88 |    \|u0|w_reg[1][29] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][29] /C | -
0.299 |   2.732 |    2.434 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
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     |    89 |        \|sa01_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[6] /CP    | -
0.298 |   2.714 |    2.415 | clk(D)(P) | clk(C)(P) |
     |    90 |        \|sa11_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[7] /CP    | -
0.297 |   2.713 |    2.415 | clk(D)(P) | clk(C)(P) |
     |    91 |        \|sa30_reg[3] /D v | VIOLATED Setup Check with Pin \|sa30_reg[3] /CP    | -
0.295 |   2.675 |    2.380 | clk(D)(P) | clk(C)(P) |
     |    92 |        \|sa33_reg[5] /D v | VIOLATED Setup Check with Pin \|sa33_reg[5] /CP    | -
0.286 |   2.670 |    2.384 | clk(D)(P) | clk(C)(P) |
     |    93 |     \|u0|w_reg[3][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][1] /CP | -
0.283 |   2.699 |    2.416 | clk(D)(P) | clk(C)(P) |
     |    94 |     \|u0|w_reg[1][5] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][5] /CP | -
0.282 |   2.718 |    2.436 | clk(D)(P) | clk(C)(P) |
     |    95 |    \|u0|w_reg[0][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][26] /C | -
0.281 |   2.695 |    2.414 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |    96 |        \|sa21_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[2] /CP    | -
0.279 |   2.692 |    2.413 | clk(D)(P) | clk(C)(P) |
     |    97 |        \|sa30_reg[6] /D v | VIOLATED Setup Check with Pin \|sa30_reg[6] /CP    | -
0.266 |   2.653 |    2.387 | clk(D)(P) | clk(C)(P) |
     |    98 |        \|sa10_reg[1] /D v | VIOLATED Setup Check with Pin \|sa10_reg[1] /CP    | -
0.265 |   2.653 |    2.388 | clk(D)(P) | clk(C)(P) |
     |    99 |        \|sa23_reg[1] /D v | VIOLATED Setup Check with Pin \|sa23_reg[1] /CP    | -
0.262 |   2.637 |    2.375 | clk(D)(P) | clk(C)(P) |
     |   100 |        \|sa20_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[2] /CP    | -
0.262 |   2.684 |    2.422 | clk(D)(P) | clk(C)(P) |
     |   101 |        \|sa31_reg[3] /D v | VIOLATED Setup Check with Pin \|sa31_reg[3] /CP    | -
0.259 |   2.652 |    2.393 | clk(D)(P) | clk(C)(P) |
     |   102 |     \|u0|w_reg[3][9] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][9] /CP | -
0.241 |   2.655 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   103 |        \|sa32_reg[1] /D v | VIOLATED Setup Check with Pin \|sa32_reg[1] /CP    | -
0.234 |   2.618 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   104 |        \|sa00_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[4] /CP    | -
0.234 |   2.649 |    2.415 | clk(D)(P) | clk(C)(P) |
     |   105 |    \|u0|w_reg[3][10] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][10] /C | -
0.233 |   2.649 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   106 |        \|sa20_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[5] /CP    | -
0.231 |   2.651 |    2.420 | clk(D)(P) | clk(C)(P) |
     |   107 |        \|sa20_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[6] /CP    | -
0.230 |   2.655 |    2.425 | clk(D)(P) | clk(C)(P) |
     |   108 |        \|sa31_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[6] /CP    | -
0.225 |   2.640 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   109 |        \|sa30_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[5] /CP    | -
0.225 |   2.634 |    2.409 | clk(D)(P) | clk(C)(P) |
     |   110 |        \|sa10_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[6] /CP    | -
0.224 |   2.642 |    2.418 | clk(D)(P) | clk(C)(P) |
     |   111 |    \|u0|w_reg[3][22] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][22] /C | -
0.222 |   2.638 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   112 |    \|u0|w_reg[2][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][15] /C | -
0.218 |   2.634 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   113 |        \|sa22_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[4] /CP    | -
0.218 |   2.626 |    2.408 | clk(D)(P) | clk(C)(P) |
     |   114 |     \|u0|w_reg[3][8] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][8] /CP | -
0.215 |   2.632 |    2.416 | clk(D)(P) | clk(C)(P) |
     |   115 |        \|sa30_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[2] /CP    | -
0.211 |   2.631 |    2.420 | clk(D)(P) | clk(C)(P) |
     |   116 |    \|u0|w_reg[1][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][20] /C | -
0.204 |   2.620 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   117 |        \|sa32_reg[4] /D v | VIOLATED Setup Check with Pin \|sa32_reg[4] /CP    | -
0.200 |   2.605 |    2.405 | clk(D)(P) | clk(C)(P) |
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     |   118 |        \|sa03_reg[5] /D v | VIOLATED Setup Check with Pin \|sa03_reg[5] /CP    | -
0.199 |   2.580 |    2.380 | clk(D)(P) | clk(C)(P) |
     |   119 |        \|sa00_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[3] /CP    | -
0.196 |   2.614 |    2.418 | clk(D)(P) | clk(C)(P) |
     |   120 |     \|u0|w_reg[2][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][1] /CP | -
0.196 |   2.611 |    2.415 | clk(D)(P) | clk(C)(P) |
     |   121 |    \|u0|w_reg[3][18] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][18] /C | -
0.194 |   2.609 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   122 |    \|u0|w_reg[1][28] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][28] /C | -
0.186 |   2.617 |    2.431 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   123 |        \|sa21_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[5] /CP    | -
0.185 |   2.599 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   124 |   \|text_out_reg[96] /D v | VIOLATED Setup Check with Pin \|text_out_reg[96] / | -
0.183 |   2.549 |    2.366 | clk(D)(P) | clk(C)(P) |
     |       |                          | CP                                                 |
|         |          |          |          |
     |   125 |        \|sa02_reg[4] /D v | VIOLATED Setup Check with Pin \|sa02_reg[4] /CP    | -
0.177 |   2.568 |    2.391 | clk(D)(P) | clk(C)(P) |
     |   126 |    \|u0|w_reg[3][13] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][13] /C | -
0.170 |   2.585 |    2.414 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   127 |        \|sa32_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[7] /CP    | -
0.169 |   2.559 |    2.390 | clk(D)(P) | clk(C)(P) |
     |   128 |        \|sa03_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa03_reg[7] /CP    | -
0.168 |   2.583 |    2.416 | clk(D)(P) | clk(C)(P) |
     |   129 |        \|sa22_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[3] /CP    | -
0.161 |   2.583 |    2.423 | clk(D)(P) | clk(C)(P) |
     |   130 |    \|u0|w_reg[3][12] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][12] /C | -
0.159 |   2.574 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   131 |        \|sa00_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[6] /CP    | -
0.158 |   2.570 |    2.412 | clk(D)(P) | clk(C)(P) |
     |   132 |        \|sa22_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[1] /CP    | -
0.156 |   2.559 |    2.402 | clk(D)(P) | clk(C)(P) |
     |   133 |        \|sa22_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[0] /CP    | -
0.155 |   2.565 |    2.410 | clk(D)(P) | clk(C)(P) |
     |   134 |        \|sa13_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[7] /CP    | -
0.154 |   2.571 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   135 |        \|sa31_reg[7] /D v | VIOLATED Setup Check with Pin \|sa31_reg[7] /CP    | -
0.153 |   2.545 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   136 |        \|sa10_reg[2] /D v | VIOLATED Setup Check with Pin \|sa10_reg[2] /CP    | -
0.150 |   2.555 |    2.405 | clk(D)(P) | clk(C)(P) |
     |   137 |    \|u0|w_reg[2][18] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][18] /C | -
0.148 |   2.564 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   138 |        \|sa01_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[3] /CP    | -
0.143 |   2.558 |    2.415 | clk(D)(P) | clk(C)(P) |
     |   139 |        \|sa01_reg[4] /D v | VIOLATED Setup Check with Pin \|sa01_reg[4] /CP    | -
0.143 |   2.531 |    2.389 | clk(D)(P) | clk(C)(P) |
     |   140 |        \|sa23_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[0] /CP    | -
0.138 |   2.556 |    2.418 | clk(D)(P) | clk(C)(P) |
     |   141 |        \|sa21_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[7] /CP    | -
0.137 |   2.543 |    2.406 | clk(D)(P) | clk(C)(P) |
     |   142 |     \|u0|w_reg[2][8] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][8] /CP | -
0.136 |   2.553 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   143 |    \|u0|w_reg[2][10] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][10] /C | -
0.135 |   2.550 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |          |          |
     |   144 |    \|u0|w_reg[0][24] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][24] /C | -
0.132 |   2.549 |    2.417 | clk(D)(P) | clk(C)(P) |
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     |       |                            | P                                                     |
|         |          |           |           |
     |   145 |     \|u0|w_reg[1][2] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][2] /CP | -
0.130 |   2.566 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   146 |        \|sa03_reg[6] /D v | VIOLATED Setup Check with Pin \|sa03_reg[6] /CP    | -
0.130 |   2.511 |    2.382 | clk(D)(P) | clk(C)(P) |
     |   147 |        \|sa10_reg[3] /D v | VIOLATED Setup Check with Pin \|sa10_reg[3] /CP    | -
0.125 |   2.533 |    2.408 | clk(D)(P) | clk(C)(P) |
     |   148 |        \|sa12_reg[1] /D v | VIOLATED Setup Check with Pin \|sa12_reg[1] /CP    | -
0.116 |   2.521 |    2.406 | clk(D)(P) | clk(C)(P) |
     |   149 |        \|sa13_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[1] /CP    | -
0.114 |   2.518 |    2.403 | clk(D)(P) | clk(C)(P) |
     |   150 |        \|sa00_reg[5] /D v | VIOLATED Setup Check with Pin \|sa00_reg[5] /CP    | -
0.114 |   2.511 |    2.397 | clk(D)(P) | clk(C)(P) |
     |   151 |    \|u0|w_reg[1][23] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][23] /C | -
0.111 |   2.547 |    2.436 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   152 |        \|sa13_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[5] /CP    | -
0.110 |   2.500 |    2.390 | clk(D)(P) | clk(C)(P) |
     |   153 |    \|u0|w_reg[2][22] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][22] /C | -
0.109 |   2.526 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   154 |    \|u0|w_reg[3][14] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][14] /C | -
0.098 |   2.513 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   155 |        \|sa22_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[7] /CP    | -
0.098 |   2.510 |    2.412 | clk(D)(P) | clk(C)(P) |
     |   156 |        \|sa02_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[7] /CP    | -
0.095 |   2.511 |    2.416 | clk(D)(P) | clk(C)(P) |
     |   157 |        \|sa32_reg[0] /D v | VIOLATED Setup Check with Pin \|sa32_reg[0] /CP    | -
0.094 |   2.497 |    2.402 | clk(D)(P) | clk(C)(P) |
     |   158 |     \|u0|w_reg[1][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][1] /CP | -
0.091 |   2.504 |    2.412 | clk(D)(P) | clk(C)(P) |
     |   159 |     \|u0|w_reg[0][4] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][4] /CP | -
0.091 |   2.527 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   160 |    \|u0|w_reg[0][21] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][21] /C | -
0.090 |   2.522 |    2.432 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   161 |    \|u0|w_reg[0][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][31] /C | -
0.089 |   2.506 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   162 |    \|u0|w_reg[2][14] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][14] /C | -
0.082 |   2.499 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
     |   163 |        \|sa12_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa12_reg[7] /CP    | -
0.082 |   2.503 |    2.421 | clk(D)(P) | clk(C)(P) |
     |   164 |     \|u0|w_reg[0][3] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][3] /CP | -
0.082 |   2.517 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   165 |  \|text_out_reg[126] /D ^ | VIOLATED Setup Check with Pin \|text_out_reg[126]  | -
0.080 |   2.447 |    2.367 | clk(D)(P) | clk(C)(P) |
     |       |                            | /CP                                                   |
|         |          |           |           |
     |   166 |        \|sa01_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[2] /CP    | -
0.078 |   2.486 |    2.409 | clk(D)(P) | clk(C)(P) |
     |   167 |        \|sa23_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[5] /CP    | -
0.074 |   2.466 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   168 |        \|sa02_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[3] /CP    | -
0.074 |   2.487 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   169 |    \|u0|w_reg[3][19] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][19] /C | -
0.073 |   2.489 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                            | P                                                     |
|         |          |           |           |
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     |   170 |        \|sa00_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[2] /CP    | -
0.072 |   2.490 |    2.418 | clk(D)(P) | clk(C)(P) |
     |   171 |        \|sa11_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[5] /CP    | -
0.067 |   2.482 |    2.415 | clk(D)(P) | clk(C)(P) |
     |   172 |    \|u0|w_reg[1][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][15] /C | -
0.066 |   2.482 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   173 |        \|sa32_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[5] /CP    | -
0.064 |   2.442 |    2.378 | clk(D)(P) | clk(C)(P) |
     |   174 |        \|sa02_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[0] /CP    | -
0.063 |   2.484 |    2.421 | clk(D)(P) | clk(C)(P) |
     |   175 |        \|sa02_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[1] /CP    | -
0.060 |   2.482 |    2.422 | clk(D)(P) | clk(C)(P) |
     |   176 |        \|sa32_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[3] /CP    | -
0.055 |   2.475 |    2.420 | clk(D)(P) | clk(C)(P) |
     |   177 |        \|sa03_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa03_reg[1] /CP    | -
0.055 |   2.473 |    2.418 | clk(D)(P) | clk(C)(P) |
     |   178 |        \|sa33_reg[3] /D v | VIOLATED Setup Check with Pin \|sa33_reg[3] /CP    | -
0.054 |   2.430 |    2.375 | clk(D)(P) | clk(C)(P) |
     |   179 |        \|sa23_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[6] /CP    | -
0.053 |   2.475 |    2.422 | clk(D)(P) | clk(C)(P) |
     |   180 |        \|sa23_reg[2] /D v | VIOLATED Setup Check with Pin \|sa23_reg[2] /CP    | -
0.051 |   2.428 |    2.377 | clk(D)(P) | clk(C)(P) |
     |   181 |     \|u0|w_reg[2][9] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][9] /CP | -
0.051 |   2.468 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   182 |    \|u0|w_reg[2][19] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][19] /C | -
0.050 |   2.465 |    2.415 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   183 |        \|sa01_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[0] /CP    | -
0.049 |   2.462 |    2.413 | clk(D)(P) | clk(C)(P) |
     |   184 |        \|sa13_reg[6] /D v | VIOLATED Setup Check with Pin \|sa13_reg[6] /CP    | -
0.046 |   2.445 |    2.398 | clk(D)(P) | clk(C)(P) |
     |   185 |    \|u0|w_reg[2][13] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][13] /C | -
0.045 |   2.462 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   186 |        \|sa23_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[7] /CP    | -
0.042 |   2.465 |    2.422 | clk(D)(P) | clk(C)(P) |
     |   187 |        \|sa13_reg[3] /D v | VIOLATED Setup Check with Pin \|sa13_reg[3] /CP    | -
0.042 |   2.439 |    2.397 | clk(D)(P) | clk(C)(P) |
     |   188 |   \|text_out_reg[85] /D v | VIOLATED Setup Check with Pin \|text_out_reg[85] / | -
0.040 |   2.407 |    2.366 | clk(D)(P) | clk(C)(P) |
     |       |                          | CP                                                 |
|         |          |           |          |
     |   189 |   \|text_out_reg[28] /D v | VIOLATED Setup Check with Pin \|text_out_reg[28] / | -
0.040 |   2.411 |    2.371 | clk(D)(P) | clk(C)(P) |
     |       |                          | CP                                                 |
|         |          |           |          |
     |   190 |    \|u0|w_reg[0][25] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][25] /C | -
0.039 |   2.456 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   191 |    \|u0|w_reg[2][12] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][12] /C | -
0.037 |   2.454 |    2.417 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   192 |    \|u0|w_reg[3][17] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][17] /C | -
0.032 |   2.447 |    2.416 | clk(D)(P) | clk(C)(P) |
     |       |                          | P                                                  |
|         |          |           |          |
     |   193 |     \|u0|w_reg[0][5] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][5] /CP | -
0.031 |   2.467 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   194 |        \|sa33_reg[1] /D v | VIOLATED Setup Check with Pin \|sa33_reg[1] /CP    | -
0.030 |   2.414 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   195 |        \|sa33_reg[0] /D v | VIOLATED Setup Check with Pin \|sa33_reg[0] /CP    | -
0.028 |   2.407 |    2.379 | clk(D)(P) | clk(C)(P) |
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     |   196 |        \|sa03_reg[3] /D v | VIOLATED Setup Check with Pin \|sa03_reg[3] /CP    | -
0.027 |   2.421 |    2.394 | clk(D)(P) | clk(C)(P) |
     |   197 |        \|sa10_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[5] /CP    | -
0.013 |   2.438 |    2.425 | clk(D)(P) | clk(C)(P) |
     |   198 |   \|text_out_reg[78] /D v | VIOLATED Setup Check with Pin \|text_out_reg[78] / | -
0.011 |   2.354 |    2.343 | clk(D)(P) | clk(C)(P) |
     |       |                           | CP                                                 |
|         |         |          |          |
     |   199 |  \|text_out_reg[103] /D v | VIOLATED Setup Check with Pin \|text_out_reg[103]  | -
0.008 |   2.393 |    2.385 | clk(D)(P) | clk(C)(P) |
     |       |                           | /CP                                                |
|         |         |          |          |
     |   200 |  \|text_out_reg[122] /D ^ | VIOLATED Setup Check with Pin \|text_out_reg[122]  |
0.000 |   2.348 |    2.348 | clk(D)(P) | clk(C)(P) |
     |       |                           | /CP                                                |
|         |         |          |          |
     |   201 |   \|text_out_reg[97] /D v | MET Setup Check with Pin \|text_out_reg[97] /CP    |
0.003 |   2.381 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   202 |        \|sa13_reg[2] /D ^ | MET Setup Check with Pin \|sa13_reg[2] /CP         |
0.003 |   2.382 |    2.385 | clk(D)(P) | clk(C)(P) |
     |   203 |  \|text_out_reg[100] /D ^ | MET Setup Check with Pin \|text_out_reg[100] /CP   |
0.006 |   2.386 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   204 |        \|sa33_reg[6] /D v | MET Setup Check with Pin \|sa33_reg[6] /CP         |
0.008 |   2.376 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   205 |    \|u0|w_reg[0][20] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][20] /CP     |
0.011 |   2.420 |    2.430 | clk(D)(P) | clk(C)(P) |
     |   206 |   \|text_out_reg[79] /D v | MET Setup Check with Pin \|text_out_reg[79] /CP    |
0.011 |   2.358 |    2.368 | clk(D)(P) | clk(C)(P) |
     |   207 |        \|sa02_reg[6] /D v | MET Setup Check with Pin \|sa02_reg[6] /CP         |
0.014 |   2.374 |    2.388 | clk(D)(P) | clk(C)(P) |
     |   208 |        \|sa03_reg[2] /D v | MET Setup Check with Pin \|sa03_reg[2] /CP         |
0.017 |   2.360 |    2.377 | clk(D)(P) | clk(C)(P) |
     |   209 |     \|u0|w_reg[1][8] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][8] /CP      |
0.018 |   2.417 |    2.434 | clk(D)(P) | clk(C)(P) |
     |   210 |    \|u0|w_reg[0][27] /D v | MET Setup Check with Pin \|u0|w_reg[0][27] /CP     |
0.019 |   2.398 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   211 |   \|text_out_reg[75] /D ^ | MET Setup Check with Pin \|text_out_reg[75] /CP    |
0.021 |   2.298 |    2.319 | clk(D)(P) | clk(C)(P) |
     |   212 |        \|sa33_reg[2] /D v | MET Setup Check with Pin \|sa33_reg[2] /CP         |
0.021 |   2.354 |    2.375 | clk(D)(P) | clk(C)(P) |
     |   213 |        \|sa31_reg[2] /D ^ | MET Setup Check with Pin \|sa31_reg[2] /CP         |
0.025 |   2.376 |    2.401 | clk(D)(P) | clk(C)(P) |
     |   214 |    \|u0|w_reg[0][29] /D v | MET Setup Check with Pin \|u0|w_reg[0][29] /CP     |
0.028 |   2.378 |    2.405 | clk(D)(P) | clk(C)(P) |
     |   215 |        \|sa12_reg[4] /D v | MET Setup Check with Pin \|sa12_reg[4] /CP         |
0.033 |   2.373 |    2.406 | clk(D)(P) | clk(C)(P) |
     |   216 |        \|sa02_reg[5] /D ^ | MET Setup Check with Pin \|sa02_reg[5] /CP         |
0.033 |   2.375 |    2.408 | clk(D)(P) | clk(C)(P) |
     |   217 |        \|sa11_reg[2] /D ^ | MET Setup Check with Pin \|sa11_reg[2] /CP         |
0.038 |   2.375 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   218 |    \|u0|w_reg[0][28] /D v | MET Setup Check with Pin \|u0|w_reg[0][28] /CP     |
0.041 |   2.376 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   219 |        \|sa21_reg[6] /D ^ | MET Setup Check with Pin \|sa21_reg[6] /CP         |
0.047 |   2.369 |    2.416 | clk(D)(P) | clk(C)(P) |
     |   220 |    \|u0|w_reg[1][10] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][10] /CP     |
0.050 |   2.385 |    2.435 | clk(D)(P) | clk(C)(P) |
     |   221 |    \|u0|w_reg[2][17] /D v | MET Setup Check with Pin \|u0|w_reg[2][17] /CP     |
0.052 |   2.366 |    2.417 | clk(D)(P) | clk(C)(P) |
     |   222 |        \|sa32_reg[2] /D v | MET Setup Check with Pin \|sa32_reg[2] /CP         |
0.053 |   2.323 |    2.376 | clk(D)(P) | clk(C)(P) |
     |   223 |    \|u0|w_reg[1][22] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][22] /CP     |
0.057 |   2.379 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   224 |        \|sa12_reg[6] /D ^ | MET Setup Check with Pin \|sa12_reg[6] /CP         |
0.059 |   2.351 |    2.410 | clk(D)(P) | clk(C)(P) |
     |   225 |        \|sa03_reg[4] /D ^ | MET Setup Check with Pin \|sa03_reg[4] /CP         |
0.059 |   2.363 |    2.422 | clk(D)(P) | clk(C)(P) |
     |   226 |   \|text_out_reg[99] /D v | MET Setup Check with Pin \|text_out_reg[99] /CP    |
0.062 |   2.318 |    2.381 | clk(D)(P) | clk(C)(P) |
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| 227 | \|u0|w_reg[1][18] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][18] /CP |
0.064 | 2.373 | 2.437 | clk(D)(P) | clk(C)(P) |
| 228 | \|u0|w_reg[0][2] /D v | MET Setup Check with Pin \|u0|w_reg[0][2] /CP |
0.064 | 2.351 | 2.415 | clk(D)(P) | clk(C)(P) |
| 229 | \|u0|w_reg[1][9] /D v | MET Setup Check with Pin \|u0|w_reg[1][9] /CP |
0.068 | 2.348 | 2.416 | clk(D)(P) | clk(C)(P) |
| 230 | \|sa33_reg[7] /D v | MET Setup Check with Pin \|sa33_reg[7] /CP |
0.074 | 2.309 | 2.384 | clk(D)(P) | clk(C)(P) |
| 231 | \|u0|w_reg[3][11] /D v | MET Setup Check with Pin \|u0|w_reg[3][11] /CP |
0.080 | 2.336 | 2.416 | clk(D)(P) | clk(C)(P) |
| 232 | \|sa32_reg[6] /D ^ | MET Setup Check with Pin \|sa32_reg[6] /CP |
0.085 | 2.296 | 2.380 | clk(D)(P) | clk(C)(P) |
| 233 | \|u0|w_reg[3][16] /D v | MET Setup Check with Pin \|u0|w_reg[3][16] /CP |
0.085 | 2.331 | 2.416 | clk(D)(P) | clk(C)(P) |
| 234 | \|u0|w_reg[0][15] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][15] /CP |
0.106 | 2.322 | 2.428 | clk(D)(P) | clk(C)(P) |
| 235 | \|u0|w_reg[2][11] /D ^ | MET Setup Check with Pin \|u0|w_reg[2][11] /CP |
0.109 | 2.325 | 2.434 | clk(D)(P) | clk(C)(P) |
| 236 | \|u0|w_reg[1][12] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][12] /CP |
0.112 | 2.322 | 2.435 | clk(D)(P) | clk(C)(P) |
| 237 | \|sa12_reg[3] /D ^ | MET Setup Check with Pin \|sa12_reg[3] /CP |
0.113 | 2.306 | 2.420 | clk(D)(P) | clk(C)(P) |
| 238 | \|sa03_reg[0] /D ^ | MET Setup Check with Pin \|sa03_reg[0] /CP |
0.114 | 2.304 | 2.419 | clk(D)(P) | clk(C)(P) |
| 239 | \|sa02_reg[2] /D ^ | MET Setup Check with Pin \|sa02_reg[2] /CP |
0.115 | 2.300 | 2.416 | clk(D)(P) | clk(C)(P) |
| 240 | \|sa31_reg[0] /D v | MET Setup Check with Pin \|sa31_reg[0] /CP |
0.119 | 2.268 | 2.386 | clk(D)(P) | clk(C)(P) |
| 241 | \|u0|w_reg[1][14] /D v | MET Setup Check with Pin \|u0|w_reg[1][14] /CP |
0.122 | 2.294 | 2.417 | clk(D)(P) | clk(C)(P) |
| 242 | \|u0|w_reg[0][1] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][1] /CP |
0.129 | 2.307 | 2.435 | clk(D)(P) | clk(C)(P) |
| 243 | \|text_out_reg[76] /D v | MET Setup Check with Pin \|text_out_reg[76] /CP |
0.129 | 2.217 | 2.346 | clk(D)(P) | clk(C)(P) |
| 244 | \|u0|w_reg[1][13] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][13] /CP |
0.135 | 2.301 | 2.436 | clk(D)(P) | clk(C)(P) |
| 245 | \|sa22_reg[6] /D ^ | MET Setup Check with Pin \|sa22_reg[6] /CP |
0.140 | 2.266 | 2.406 | clk(D)(P) | clk(C)(P) |
| 246 | \|text_out_reg[101] /D ^ | MET Setup Check with Pin \|text_out_reg[101] /CP |
0.142 | 2.244 | 2.385 | clk(D)(P) | clk(C)(P) |
| 247 | \|text_out_reg[29] /D ^ | MET Setup Check with Pin \|text_out_reg[29] /CP |
0.152 | 2.214 | 2.366 | clk(D)(P) | clk(C)(P) |
| 248 | \|u0|w_reg[1][17] /D v | MET Setup Check with Pin \|u0|w_reg[1][17] /CP |
0.157 | 2.260 | 2.416 | clk(D)(P) | clk(C)(P) |
| 249 | \|u0|w_reg[2][16] /D v | MET Setup Check with Pin \|u0|w_reg[2][16] /CP |
0.160 | 2.257 | 2.417 | clk(D)(P) | clk(C)(P) |
| 250 | \|text_out_reg[7] /D ^ | MET Setup Check with Pin \|text_out_reg[7] /CP |
0.165 | 2.207 | 2.372 | clk(D)(P) | clk(C)(P) |
| 251 | \|text_out_reg[102] /D v | MET Setup Check with Pin \|text_out_reg[102] /CP |
0.166 | 2.234 | 2.400 | clk(D)(P) | clk(C)(P) |
| 252 | \|text_out_reg[65] /D ^ | MET Setup Check with Pin \|text_out_reg[65] /CP |
0.195 | 2.168 | 2.362 | clk(D)(P) | clk(C)(P) |
| 253 | \|sa12_reg[2] /D ^ | MET Setup Check with Pin \|sa12_reg[2] /CP |
0.198 | 2.224 | 2.423 | clk(D)(P) | clk(C)(P) |
| 254 | \|sa22_reg[5] /D ^ | MET Setup Check with Pin \|sa22_reg[5] /CP |
0.205 | 2.218 | 2.423 | clk(D)(P) | clk(C)(P) |
| 255 | \|text_out_reg[125] /D ^ | MET Setup Check with Pin \|text_out_reg[125] /CP |
0.206 | 2.165 | 2.372 | clk(D)(P) | clk(C)(P) |
| 256 | \|u0|w_reg[1][19] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][19] /CP |
0.210 | 2.224 | 2.434 | clk(D)(P) | clk(C)(P) |
| 257 | \|sa13_reg[0] /D ^ | MET Setup Check with Pin \|sa13_reg[0] /CP |
0.211 | 2.211 | 2.422 | clk(D)(P) | clk(C)(P) |
| 258 | \|u0|w_reg[0][9] /D v | MET Setup Check with Pin \|u0|w_reg[0][9] /CP |
0.217 | 2.199 | 2.416 | clk(D)(P) | clk(C)(P) |
| 259 | \|text_out_reg[87] /D v | MET Setup Check with Pin \|text_out_reg[87] /CP |
0.222 | 2.148 | 2.369 | clk(D)(P) | clk(C)(P) |
| 260 | \|text_out_reg[121] /D ^ | MET Setup Check with Pin \|text_out_reg[121] /CP |
0.227 | 2.149 | 2.375 | clk(D)(P) | clk(C)(P) |

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      |   261 |   \|text_out_reg[81] /D v | MET Setup Check with Pin \|text_out_reg[81] /CP    |
0.227 |   2.146 |    2.373 | clk(D)(P) | clk(C)(P) |
      |   262 |    \|text_out_reg[1] /D v | MET Setup Check with Pin \|text_out_reg[1] /CP     |
0.228 |   2.160 |    2.388 | clk(D)(P) | clk(C)(P) |
      |   263 |   \|text_out_reg[60] /D v | MET Setup Check with Pin \|text_out_reg[60] /CP    |
0.235 |   2.110 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   264 |   \|text_out_reg[39] /D v | MET Setup Check with Pin \|text_out_reg[39] /CP    |
0.244 |   2.152 |    2.396 | clk(D)(P) | clk(C)(P) |
      |   265 |   \|text_out_reg[63] /D v | MET Setup Check with Pin \|text_out_reg[63] /CP    |
0.247 |   2.118 |    2.365 | clk(D)(P) | clk(C)(P) |
      |   266 |    \|text_out_reg[5] /D v | MET Setup Check with Pin \|text_out_reg[5] /CP     |
0.250 |   2.131 |    2.382 | clk(D)(P) | clk(C)(P) |
      |   267 |   \|text_out_reg[57] /D ^ | MET Setup Check with Pin \|text_out_reg[57] /CP    |
0.254 |   2.123 |    2.376 | clk(D)(P) | clk(C)(P) |
      |   268 |    \|u0|w_reg[0][23] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][23] /CP     |
0.259 |   2.178 |    2.437 | clk(D)(P) | clk(C)(P) |
      |   269 |        \|sa12_reg[5] /D ^ | MET Setup Check with Pin \|sa12_reg[5] /CP         |
0.260 |   2.163 |    2.423 | clk(D)(P) | clk(C)(P) |
      |   270 |        \|sa12_reg[0] /D ^ | MET Setup Check with Pin \|sa12_reg[0] /CP         |
0.263 |   2.154 |    2.417 | clk(D)(P) | clk(C)(P) |
      |   271 |  \|text_out_reg[112] /D v | MET Setup Check with Pin \|text_out_reg[112] /CP   |
0.265 |   2.113 |    2.378 | clk(D)(P) | clk(C)(P) |
      |   272 |        \|sa22_reg[2] /D ^ | MET Setup Check with Pin \|sa22_reg[2] /CP         |
0.265 |   2.149 |    2.414 | clk(D)(P) | clk(C)(P) |
      |   273 |     \|u0|w_reg[0][8] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][8] /CP      |
0.276 |   2.156 |    2.431 | clk(D)(P) | clk(C)(P) |
      |   274 |   \|text_out_reg[86] /D v | MET Setup Check with Pin \|text_out_reg[86] /CP    |
0.285 |   2.088 |    2.373 | clk(D)(P) | clk(C)(P) |
      |   275 |    \|text_out_reg[6] /D v | MET Setup Check with Pin \|text_out_reg[6] /CP     |
0.285 |   2.098 |    2.383 | clk(D)(P) | clk(C)(P) |
      |   276 |  \|text_out_reg[117] /D v | MET Setup Check with Pin \|text_out_reg[117] /CP   |
0.286 |   2.102 |    2.388 | clk(D)(P) | clk(C)(P) |
      |   277 |    \|u0|w_reg[0][10] /D v | MET Setup Check with Pin \|u0|w_reg[0][10] /CP     |
0.289 |   2.127 |    2.416 | clk(D)(P) | clk(C)(P) |
      |   278 |  \|text_out_reg[124] /D v | MET Setup Check with Pin \|text_out_reg[124] /CP   |
0.291 |   2.102 |    2.392 | clk(D)(P) | clk(C)(P) |
      |   279 |   \|text_out_reg[92] /D v | MET Setup Check with Pin \|text_out_reg[92] /CP    |
0.294 |   2.107 |    2.401 | clk(D)(P) | clk(C)(P) |
      |   280 |  \|text_out_reg[116] /D ^ | MET Setup Check with Pin \|text_out_reg[116] /CP   |
0.296 |   2.086 |    2.382 | clk(D)(P) | clk(C)(P) |
      |   281 |   \|text_out_reg[66] /D v | MET Setup Check with Pin \|text_out_reg[66] /CP    |
0.298 |   2.098 |    2.396 | clk(D)(P) | clk(C)(P) |
      |   282 |   \|text_out_reg[74] /D v | MET Setup Check with Pin \|text_out_reg[74] /CP    |
0.306 |   2.056 |    2.363 | clk(D)(P) | clk(C)(P) |
      |   283 |    \|u0|w_reg[1][16] /D v | MET Setup Check with Pin \|u0|w_reg[1][16] /CP     |
0.309 |   2.108 |    2.417 | clk(D)(P) | clk(C)(P) |
      |   284 |  \|text_out_reg[113] /D v | MET Setup Check with Pin \|text_out_reg[113] /CP   |
0.310 |   2.086 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   285 |    \|u0|w_reg[0][18] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][18] /CP     |
0.313 |   2.107 |    2.420 | clk(D)(P) | clk(C)(P) |
      |   286 |    \|text_out_reg[2] /D v | MET Setup Check with Pin \|text_out_reg[2] /CP     |
0.316 |   2.067 |    2.383 | clk(D)(P) | clk(C)(P) |
      |   287 |  \|text_out_reg[104] /D v | MET Setup Check with Pin \|text_out_reg[104] /CP   |
0.319 |   2.067 |    2.386 | clk(D)(P) | clk(C)(P) |
      |   288 |   \|text_out_reg[89] /D v | MET Setup Check with Pin \|text_out_reg[89] /CP    |
0.325 |   2.069 |    2.394 | clk(D)(P) | clk(C)(P) |
      |   289 |   \|text_out_reg[88] /D v | MET Setup Check with Pin \|text_out_reg[88] /CP    |
0.328 |   2.068 |    2.396 | clk(D)(P) | clk(C)(P) |
      |   290 |  \|text_out_reg[115] /D v | MET Setup Check with Pin \|text_out_reg[115] /CP   |
0.328 |   2.061 |    2.389 | clk(D)(P) | clk(C)(P) |
      |   291 |   \|text_out_reg[53] /D v | MET Setup Check with Pin \|text_out_reg[53] /CP    |
0.329 |   2.072 |    2.401 | clk(D)(P) | clk(C)(P) |
      |   292 |    \|u0|w_reg[0][14] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][14] /CP     |
0.332 |   2.104 |    2.436 | clk(D)(P) | clk(C)(P) |
      |   293 |    \|u0|w_reg[1][11] /D v | MET Setup Check with Pin \|u0|w_reg[1][11] /CP     |
0.339 |   2.078 |    2.417 | clk(D)(P) | clk(C)(P) |
      |   294 |    \|u0|w_reg[0][17] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][17] /CP     |
0.341 |   2.092 |    2.434 | clk(D)(P) | clk(C)(P) |
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     |   295 |   \|text_out_reg[64] /D v | MET Setup Check with Pin \|text_out_reg[64] /CP    |
0.344 |   2.026 |    2.371 | clk(D)(P) | clk(C)(P) |
     |   296 |   \|text_out_reg[67] /D v | MET Setup Check with Pin \|text_out_reg[67] /CP    |
0.349 |   2.031 |    2.381 | clk(D)(P) | clk(C)(P) |
     |   297 |    \|u0|w_reg[0][12] /D v | MET Setup Check with Pin \|u0|w_reg[0][12] /CP     |
0.350 |   2.065 |    2.415 | clk(D)(P) | clk(C)(P) |
     |   298 |    \|u0|w_reg[0][13] /D v | MET Setup Check with Pin \|u0|w_reg[0][13] /CP     |
0.350 |   2.064 |    2.414 | clk(D)(P) | clk(C)(P) |
     |   299 |  \|text_out_reg[118] /D v | MET Setup Check with Pin \|text_out_reg[118] /CP   |
0.356 |   2.034 |    2.390 | clk(D)(P) | clk(C)(P) |
     |   300 |   \|text_out_reg[95] /D v | MET Setup Check with Pin \|text_out_reg[95] /CP    |
0.361 |   2.034 |    2.395 | clk(D)(P) | clk(C)(P) |
     |   301 |   \|text_out_reg[94] /D v | MET Setup Check with Pin \|text_out_reg[94] /CP    |
0.368 |   2.033 |    2.401 | clk(D)(P) | clk(C)(P) |
     |   302 |   \|text_out_reg[68] /D ^ | MET Setup Check with Pin \|text_out_reg[68] /CP    |
0.369 |   1.996 |    2.365 | clk(D)(P) | clk(C)(P) |
     |   303 |   \|text_out_reg[72] /D ^ | MET Setup Check with Pin \|text_out_reg[72] /CP    |
0.373 |   1.989 |    2.362 | clk(D)(P) | clk(C)(P) |
     |   304 |   \|text_out_reg[16] /D v | MET Setup Check with Pin \|text_out_reg[16] /CP    |
0.378 |   1.996 |    2.374 | clk(D)(P) | clk(C)(P) |
     |   305 |   \|text_out_reg[47] /D ^ | MET Setup Check with Pin \|text_out_reg[47] /CP    |
0.378 |   1.982 |    2.360 | clk(D)(P) | clk(C)(P) |
     |   306 |   \|text_out_reg[35] /D v | MET Setup Check with Pin \|text_out_reg[35] /CP    |
0.384 |   2.000 |    2.385 | clk(D)(P) | clk(C)(P) |
     |   307 |   \|text_out_reg[30] /D v | MET Setup Check with Pin \|text_out_reg[30] /CP    |
0.387 |   2.011 |    2.398 | clk(D)(P) | clk(C)(P) |
     |   308 |  \|text_out_reg[123] /D v | MET Setup Check with Pin \|text_out_reg[123] /CP   |
0.394 |   1.971 |    2.365 | clk(D)(P) | clk(C)(P) |
     |   309 |   \|text_out_reg[83] /D ^ | MET Setup Check with Pin \|text_out_reg[83] /CP    |
0.394 |   1.959 |    2.354 | clk(D)(P) | clk(C)(P) |
     |   310 |  \|text_out_reg[109] /D ^ | MET Setup Check with Pin \|text_out_reg[109] /CP   |
0.397 |   1.972 |    2.368 | clk(D)(P) | clk(C)(P) |
     |   311 |   \|text_out_reg[82] /D v | MET Setup Check with Pin \|text_out_reg[82] /CP    |
0.398 |   1.969 |    2.367 | clk(D)(P) | clk(C)(P) |
     |   312 |   \|text_out_reg[93] /D v | MET Setup Check with Pin \|text_out_reg[93] /CP    |
0.399 |   2.012 |    2.411 | clk(D)(P) | clk(C)(P) |
     |   313 |    \|u0|w_reg[0][22] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][22] /CP     |
0.401 |   2.030 |    2.431 | clk(D)(P) | clk(C)(P) |
     |   314 |   \|text_out_reg[24] /D v | MET Setup Check with Pin \|text_out_reg[24] /CP    |
0.401 |   1.967 |    2.368 | clk(D)(P) | clk(C)(P) |
     |   315 |   \|text_out_reg[98] /D ^ | MET Setup Check with Pin \|text_out_reg[98] /CP    |
0.406 |   1.981 |    2.387 | clk(D)(P) | clk(C)(P) |
     |   316 |   \|text_out_reg[55] /D ^ | MET Setup Check with Pin \|text_out_reg[55] /CP    |
0.406 |   1.965 |    2.372 | clk(D)(P) | clk(C)(P) |
     |   317 |   \|text_out_reg[27] /D ^ | MET Setup Check with Pin \|text_out_reg[27] /CP    |
0.409 |   1.947 |    2.357 | clk(D)(P) | clk(C)(P) |
     |   318 |   \|text_out_reg[91] /D v | MET Setup Check with Pin \|text_out_reg[91] /CP    |
0.411 |   1.980 |    2.391 | clk(D)(P) | clk(C)(P) |
     |   319 |   \|text_out_reg[49] /D v | MET Setup Check with Pin \|text_out_reg[49] /CP    |
0.412 |   1.988 |    2.401 | clk(D)(P) | clk(C)(P) |
     |   320 |   \|text_out_reg[59] /D v | MET Setup Check with Pin \|text_out_reg[59] /CP    |
0.416 |   1.977 |    2.393 | clk(D)(P) | clk(C)(P) |
     |   321 |   \|text_out_reg[62] /D v | MET Setup Check with Pin \|text_out_reg[62] /CP    |
0.417 |   1.973 |    2.391 | clk(D)(P) | clk(C)(P) |
     |   322 |   \|text_out_reg[58] /D ^ | MET Setup Check with Pin \|text_out_reg[58] /CP    |
0.427 |   1.947 |    2.373 | clk(D)(P) | clk(C)(P) |
     |   323 |    \|u0|w_reg[0][11] /D v | MET Setup Check with Pin \|u0|w_reg[0][11] /CP     |
0.429 |   1.982 |    2.411 | clk(D)(P) | clk(C)(P) |
     |   324 |  \|text_out_reg[110] /D ^ | MET Setup Check with Pin \|text_out_reg[110] /CP   |
0.433 |   1.939 |    2.372 | clk(D)(P) | clk(C)(P) |
     |   325 |   \|text_out_reg[40] /D ^ | MET Setup Check with Pin \|text_out_reg[40] /CP    |
0.437 |   1.946 |    2.382 | clk(D)(P) | clk(C)(P) |
     |   326 |   \|text_out_reg[56] /D ^ | MET Setup Check with Pin \|text_out_reg[56] /CP    |
0.440 |   1.942 |    2.382 | clk(D)(P) | clk(C)(P) |
     |   327 |   \|text_out_reg[61] /D v | MET Setup Check with Pin \|text_out_reg[61] /CP    |
0.459 |   1.932 |    2.390 | clk(D)(P) | clk(C)(P) |
     |   328 |   \|text_out_reg[37] /D v | MET Setup Check with Pin \|text_out_reg[37] /CP    |
0.461 |   1.929 |    2.390 | clk(D)(P) | clk(C)(P) |
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     |   329 |   \|text_out_reg[36] /D v | MET Setup Check with Pin \|text_out_reg[36] /CP    |
0.464 |   1.935 |    2.398 | clk(D)(P) | clk(C)(P) |
     |   330 |   \|text_out_reg[21] /D v | MET Setup Check with Pin \|text_out_reg[21] /CP    |
0.465 |   1.931 |    2.395 | clk(D)(P) | clk(C)(P) |
     |   331 |    \|text_out_reg[4] /D v | MET Setup Check with Pin \|text_out_reg[4] /CP     |
0.468 |   1.926 |    2.394 | clk(D)(P) | clk(C)(P) |
     |   332 |  \|text_out_reg[120] /D ^ | MET Setup Check with Pin \|text_out_reg[120] /CP   |
0.473 |   1.912 |    2.385 | clk(D)(P) | clk(C)(P) |
     |   333 |  \|text_out_reg[119] /D v | MET Setup Check with Pin \|text_out_reg[119] /CP   |
0.474 |   1.934 |    2.408 | clk(D)(P) | clk(C)(P) |
     |   334 |   \|text_out_reg[15] /D ^ | MET Setup Check with Pin \|text_out_reg[15] /CP    |
0.475 |   1.892 |    2.367 | clk(D)(P) | clk(C)(P) |
     |   335 |  \|text_out_reg[111] /D v | MET Setup Check with Pin \|text_out_reg[111] /CP   |
0.483 |   1.895 |    2.378 | clk(D)(P) | clk(C)(P) |
     |   336 |   \|text_out_reg[52] /D v | MET Setup Check with Pin \|text_out_reg[52] /CP    |
0.485 |   1.905 |    2.390 | clk(D)(P) | clk(C)(P) |
     |   337 |  \|text_out_reg[106] /D v | MET Setup Check with Pin \|text_out_reg[106] /CP   |
0.492 |   1.905 |    2.397 | clk(D)(P) | clk(C)(P) |
     |   338 |   \|text_out_reg[31] /D v | MET Setup Check with Pin \|text_out_reg[31] /CP    |
0.495 |   1.881 |    2.376 | clk(D)(P) | clk(C)(P) |
     |   339 |   \|text_out_reg[45] /D v | MET Setup Check with Pin \|text_out_reg[45] /CP    |
0.501 |   1.883 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   340 |    \|u0|w_reg[0][16] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][16] /CP     |
0.508 |   1.927 |    2.435 | clk(D)(P) | clk(C)(P) |
     |   341 |    \|text_out_reg[3] /D v | MET Setup Check with Pin \|text_out_reg[3] /CP     |
0.509 |   1.883 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   342 |   \|text_out_reg[20] /D v | MET Setup Check with Pin \|text_out_reg[20] /CP    |
0.513 |   1.869 |    2.382 | clk(D)(P) | clk(C)(P) |
     |   343 |   \|text_out_reg[25] /D v | MET Setup Check with Pin \|text_out_reg[25] /CP    |
0.513 |   1.894 |    2.408 | clk(D)(P) | clk(C)(P) |
     |   344 |   \|text_out_reg[34] /D v | MET Setup Check with Pin \|text_out_reg[34] /CP    |
0.516 |   1.862 |    2.378 | clk(D)(P) | clk(C)(P) |
     |   345 |    \|text_out_reg[8] /D ^ | MET Setup Check with Pin \|text_out_reg[8] /CP     |
0.517 |   1.859 |    2.376 | clk(D)(P) | clk(C)(P) |
     |   346 |    \|u0|w_reg[0][19] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][19] /CP     |
0.518 |   1.918 |    2.436 | clk(D)(P) | clk(C)(P) |
     |   347 |   \|text_out_reg[50] /D v | MET Setup Check with Pin \|text_out_reg[50] /CP    |
0.529 |   1.870 |    2.399 | clk(D)(P) | clk(C)(P) |
     |   348 |   \|text_out_reg[23] /D v | MET Setup Check with Pin \|text_out_reg[23] /CP    |
0.531 |   1.861 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   349 |   \|text_out_reg[22] /D v | MET Setup Check with Pin \|text_out_reg[22] /CP    |
0.536 |   1.847 |    2.384 | clk(D)(P) | clk(C)(P) |
     |   350 |  \|text_out_reg[114] /D v | MET Setup Check with Pin \|text_out_reg[114] /CP   |
0.543 |   1.852 |    2.396 | clk(D)(P) | clk(C)(P) |
     |   351 |   \|text_out_reg[54] /D v | MET Setup Check with Pin \|text_out_reg[54] /CP    |
0.545 |   1.849 |    2.394 | clk(D)(P) | clk(C)(P) |
     |   352 |   \|text_out_reg[70] /D v | MET Setup Check with Pin \|text_out_reg[70] /CP    |
0.546 |   1.842 |    2.388 | clk(D)(P) | clk(C)(P) |
     |   353 |  \|text_out_reg[127] /D v | MET Setup Check with Pin \|text_out_reg[127] /CP   |
0.551 |   1.844 |    2.395 | clk(D)(P) | clk(C)(P) |
     |   354 |   \|text_out_reg[32] /D v | MET Setup Check with Pin \|text_out_reg[32] /CP    |
0.552 |   1.854 |    2.406 | clk(D)(P) | clk(C)(P) |
     |   355 |   \|text_out_reg[33] /D v | MET Setup Check with Pin \|text_out_reg[33] /CP    |
0.561 |   1.831 |    2.392 | clk(D)(P) | clk(C)(P) |
     |   356 |  \|u0|r0|rcnt_reg[3] /D v | MET Setup Check with Pin \|u0|r0|rcnt_reg[3] /CP   |
0.564 |   1.845 |    2.409 | clk(D)(P) | clk(C)(P) |
     |   357 |   \|text_out_reg[14] /D v | MET Setup Check with Pin \|text_out_reg[14] /CP    |
0.566 |   1.830 |    2.397 | clk(D)(P) | clk(C)(P) |
     |   358 |   \|text_out_reg[90] /D ^ | MET Setup Check with Pin \|text_out_reg[90] /CP    |
0.568 |   1.819 |    2.387 | clk(D)(P) | clk(C)(P) |
     |   359 |   \|text_out_reg[38] /D v | MET Setup Check with Pin \|text_out_reg[38] /CP    |
0.570 |   1.831 |    2.401 | clk(D)(P) | clk(C)(P) |
     |   360 |   \|text_out_reg[18] /D v | MET Setup Check with Pin \|text_out_reg[18] /CP    |
0.574 |   1.824 |    2.398 | clk(D)(P) | clk(C)(P) |
     |   361 |   \|text_out_reg[17] /D v | MET Setup Check with Pin \|text_out_reg[17] /CP    |
0.574 |   1.815 |    2.389 | clk(D)(P) | clk(C)(P) |
     |   362 |   \|text_out_reg[48] /D v | MET Setup Check with Pin \|text_out_reg[48] /CP    |
0.575 |   1.811 |    2.386 | clk(D)(P) | clk(C)(P) |
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      |   363 |   \|text_out_reg[46] /D v | MET Setup Check with Pin \|text_out_reg[46] /CP    |
0.575 |   1.822 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   364 |  \|u0|r0|out_reg[28] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[28] /CP   |
0.579 |   1.844 |    2.424 | clk(D)(P) | clk(C)(P) |
      |   365 |   \|text_out_reg[51] /D v | MET Setup Check with Pin \|text_out_reg[51] /CP    |
0.582 |   1.820 |    2.402 | clk(D)(P) | clk(C)(P) |
      |   366 |  \|text_out_reg[105] /D v | MET Setup Check with Pin \|text_out_reg[105] /CP   |
0.586 |   1.806 |    2.392 | clk(D)(P) | clk(C)(P) |
      |   367 |   \|text_out_reg[71] /D v | MET Setup Check with Pin \|text_out_reg[71] /CP    |
0.594 |   1.803 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   368 |  \|u0|r0|out_reg[31] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[31] /CP   |
0.596 |   1.826 |    2.423 | clk(D)(P) | clk(C)(P) |
      |   369 |   \|text_out_reg[77] /D v | MET Setup Check with Pin \|text_out_reg[77] /CP    |
0.599 |   1.783 |    2.381 | clk(D)(P) | clk(C)(P) |
      |   370 |   \|text_out_reg[69] /D v | MET Setup Check with Pin \|text_out_reg[69] /CP    |
0.599 |   1.798 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   371 |  \|u0|r0|out_reg[30] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[30] /CP   |
0.600 |   1.835 |    2.434 | clk(D)(P) | clk(C)(P) |
      |   372 |   \|text_out_reg[11] /D v | MET Setup Check with Pin \|text_out_reg[11] /CP    |
0.602 |   1.789 |    2.391 | clk(D)(P) | clk(C)(P) |
      |   373 |  \|u0|r0|out_reg[24] /D v | MET Setup Check with Pin \|u0|r0|out_reg[24] /CP   |
0.604 |   1.792 |    2.396 | clk(D)(P) | clk(C)(P) |
      |   374 |  \|u0|r0|out_reg[27] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[27] /CP   |
0.610 |   1.801 |    2.411 | clk(D)(P) | clk(C)(P) |
      |   375 |  \|text_out_reg[108] /D v | MET Setup Check with Pin \|text_out_reg[108] /CP   |
0.617 |   1.785 |    2.401 | clk(D)(P) | clk(C)(P) |
      |   376 |  \|u0|r0|out_reg[25] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[25] /CP   |
0.619 |   1.801 |    2.420 | clk(D)(P) | clk(C)(P) |
      |   377 |   \|text_out_reg[41] /D v | MET Setup Check with Pin \|text_out_reg[41] /CP    |
0.632 |   1.765 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   378 |   \|text_out_reg[44] /D v | MET Setup Check with Pin \|text_out_reg[44] /CP    |
0.634 |   1.766 |    2.399 | clk(D)(P) | clk(C)(P) |
      |   379 |   \|text_out_reg[84] /D v | MET Setup Check with Pin \|text_out_reg[84] /CP    |
0.634 |   1.767 |    2.401 | clk(D)(P) | clk(C)(P) |
      |   380 |  \|u0|r0|out_reg[26] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[26] /CP   |
0.637 |   1.789 |    2.426 | clk(D)(P) | clk(C)(P) |
      |   381 |   \|text_out_reg[26] /D v | MET Setup Check with Pin \|text_out_reg[26] /CP    |
0.638 |   1.759 |    2.397 | clk(D)(P) | clk(C)(P) |
      |   382 |    \|text_out_reg[0] /D v | MET Setup Check with Pin \|text_out_reg[0] /CP     |
0.647 |   1.755 |    2.402 | clk(D)(P) | clk(C)(P) |
      |   383 |   \|text_out_reg[80] /D v | MET Setup Check with Pin \|text_out_reg[80] /CP    |
0.654 |   1.740 |    2.394 | clk(D)(P) | clk(C)(P) |
      |   384 |   \|text_out_reg[42] /D v | MET Setup Check with Pin \|text_out_reg[42] /CP    |
0.656 |   1.728 |    2.385 | clk(D)(P) | clk(C)(P) |
      |   385 |  \|u0|r0|out_reg[29] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[29] /CP   |
0.661 |   1.770 |    2.431 | clk(D)(P) | clk(C)(P) |
      |   386 |  \|text_out_reg[107] /D v | MET Setup Check with Pin \|text_out_reg[107] /CP   |
0.665 |   1.738 |    2.403 | clk(D)(P) | clk(C)(P) |
      |   387 |   \|text_out_reg[19] /D v | MET Setup Check with Pin \|text_out_reg[19] /CP    |
0.665 |   1.722 |    2.387 | clk(D)(P) | clk(C)(P) |
      |   388 |   \|text_out_reg[73] /D v | MET Setup Check with Pin \|text_out_reg[73] /CP    |
0.671 |   1.720 |    2.391 | clk(D)(P) | clk(C)(P) |
      |   389 |   \|text_out_reg[13] /D v | MET Setup Check with Pin \|text_out_reg[13] /CP    |
0.684 |   1.714 |    2.398 | clk(D)(P) | clk(C)(P) |
      |   390 |   \|text_out_reg[12] /D v | MET Setup Check with Pin \|text_out_reg[12] /CP    |
0.692 |   1.709 |    2.401 | clk(D)(P) | clk(C)(P) |
      |   391 |  \|u0|r0|rcnt_reg[2] /D ^ | MET Setup Check with Pin \|u0|r0|rcnt_reg[2] /CP   |
0.703 |   1.717 |    2.420 | clk(D)(P) | clk(C)(P) |
      |   392 |    \|text_out_reg[9] /D v | MET Setup Check with Pin \|text_out_reg[9] /CP     |
0.706 |   1.705 |    2.411 | clk(D)(P) | clk(C)(P) |
      |   393 |  \|u0|r0|rcnt_reg[0] /D v | MET Setup Check with Pin \|u0|r0|rcnt_reg[0] /CP   |
0.725 |   1.685 |    2.411 | clk(D)(P) | clk(C)(P) |
      |   394 |  \|u0|r0|rcnt_reg[1] /D v | MET Setup Check with Pin \|u0|r0|rcnt_reg[1] /CP   |
0.733 |   1.679 |    2.412 | clk(D)(P) | clk(C)(P) |
      |   395 |   \|text_out_reg[10] /D v | MET Setup Check with Pin \|text_out_reg[10] /CP    |
0.733 |   1.669 |    2.403 | clk(D)(P) | clk(C)(P) |
      |   396 |   \|text_out_reg[43] /D v | MET Setup Check with Pin \|text_out_reg[43] /CP    |
0.751 |   1.641 |    2.391 | clk(D)(P) | clk(C)(P) |
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      |   397 |        \|dcnt_reg[1] /D v | MET Setup Check with Pin \|dcnt_reg[1] /CP         |
0.861 |   1.553 |    2.414 | clk(D)(P) | clk(C)(P) |
      |   398 |        \|dcnt_reg[3] /D v | MET Setup Check with Pin \|dcnt_reg[3] /CP         |
0.914 |   1.504 |    2.418 | clk(D)(P) | clk(C)(P) |
      |   399 |           \|done_reg /D ^ | MET Setup Check with Pin \|done_reg /CP            |
0.924 |   1.500 |    2.424 | clk(D)(P) | clk(C)(P) |
      |   400 |        \|dcnt_reg[0] /D v | MET Setup Check with Pin \|dcnt_reg[0] /CP         |
0.964 |   1.446 |    2.410 | clk(D)(P) | clk(C)(P) |
      |   401 |  \|text_in_r_reg[67] /E v | MET Setup Check with Pin \|text_in_r_reg[67] /CP   |
0.979 |   1.280 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   402 |  \|text_in_r_reg[70] /E v | MET Setup Check with Pin \|text_in_r_reg[70] /CP   |
0.980 |   1.279 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   403 |  \|text_in_r_reg[69] /E v | MET Setup Check with Pin \|text_in_r_reg[69] /CP   |
0.980 |   1.279 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   404 |  \|text_in_r_reg[66] /E v | MET Setup Check with Pin \|text_in_r_reg[66] /CP   |
0.980 |   1.279 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   405 |  \|text_in_r_reg[65] /E v | MET Setup Check with Pin \|text_in_r_reg[65] /CP   |
0.981 |   1.278 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   406 |  \|text_in_r_reg[68] /E v | MET Setup Check with Pin \|text_in_r_reg[68] /CP   |
0.983 |   1.276 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   407 |  \|text_in_r_reg[64] /E v | MET Setup Check with Pin \|text_in_r_reg[64] /CP   |
0.983 |   1.276 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   408 | \|text_in_r_reg[127] /E v | MET Setup Check with Pin \|text_in_r_reg[127] /CP  |
0.988 |   1.276 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   409 | \|text_in_r_reg[125] /E v | MET Setup Check with Pin \|text_in_r_reg[125] /CP  |
0.988 |   1.276 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   410 |  \|text_in_r_reg[53] /E v | MET Setup Check with Pin \|text_in_r_reg[53] /CP   |
0.988 |   1.271 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   411 |  \|text_in_r_reg[63] /E v | MET Setup Check with Pin \|text_in_r_reg[63] /CP   |
0.992 |   1.267 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   412 |  \|text_in_r_reg[60] /E v | MET Setup Check with Pin \|text_in_r_reg[60] /CP   |
0.992 |   1.267 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   413 |  \|text_in_r_reg[59] /E v | MET Setup Check with Pin \|text_in_r_reg[59] /CP   |
0.992 |   1.267 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   414 |  \|text_in_r_reg[56] /E v | MET Setup Check with Pin \|text_in_r_reg[56] /CP   |
0.992 |   1.267 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   415 |  \|text_in_r_reg[61] /E v | MET Setup Check with Pin \|text_in_r_reg[61] /CP   |
0.993 |   1.266 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   416 |  \|text_in_r_reg[58] /E v | MET Setup Check with Pin \|text_in_r_reg[58] /CP   |
0.993 |   1.266 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   417 |  \|text_in_r_reg[57] /E v | MET Setup Check with Pin \|text_in_r_reg[57] /CP   |
0.993 |   1.266 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   418 |  \|text_in_r_reg[55] /E v | MET Setup Check with Pin \|text_in_r_reg[55] /CP   |
0.993 |   1.266 |    2.259 | clk(D)(P) | clk(C)(P) |
      |   419 | \|text_in_r_reg[123] /E v | MET Setup Check with Pin \|text_in_r_reg[123] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   420 | \|text_in_r_reg[121] /E v | MET Setup Check with Pin \|text_in_r_reg[121] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   421 | \|text_in_r_reg[113] /E v | MET Setup Check with Pin \|text_in_r_reg[113] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   422 | \|text_in_r_reg[115] /E v | MET Setup Check with Pin \|text_in_r_reg[115] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   423 | \|text_in_r_reg[118] /E v | MET Setup Check with Pin \|text_in_r_reg[118] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   424 | \|text_in_r_reg[116] /E v | MET Setup Check with Pin \|text_in_r_reg[116] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   425 | \|text_in_r_reg[117] /E v | MET Setup Check with Pin \|text_in_r_reg[117] /CP  |
0.998 |   1.266 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   426 |  \|text_in_r_reg[97] /E v | MET Setup Check with Pin \|text_in_r_reg[97] /CP   |
0.999 |   1.261 |    2.260 | clk(D)(P) | clk(C)(P) |
      |   427 | \|text_in_r_reg[112] /E v | MET Setup Check with Pin \|text_in_r_reg[112] /CP  |
0.999 |   1.265 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   428 | \|text_in_r_reg[114] /E v | MET Setup Check with Pin \|text_in_r_reg[114] /CP  |
0.999 |   1.265 |    2.264 | clk(D)(P) | clk(C)(P) |
      |   429 |  \|text_in_r_reg[52] /E v | MET Setup Check with Pin \|text_in_r_reg[52] /CP   |
1.008 |   1.252 |    2.260 | clk(D)(P) | clk(C)(P) |
      |   430 |  \|text_in_r_reg[54] /E v | MET Setup Check with Pin \|text_in_r_reg[54] /CP   |
1.009 |   1.251 |    2.260 | clk(D)(P) | clk(C)(P) |
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     |   431 |  \|text_in_r_reg[62] /E v | MET Setup Check with Pin \|text_in_r_reg[62] /CP   |
1.011 |   1.249 |    2.260 | clk(D)(P) | clk(C)(P) |
     |   432 | \|text_in_r_reg[126] /E v | MET Setup Check with Pin \|text_in_r_reg[126] /CP  |
1.022 |   1.242 |    2.264 | clk(D)(P) | clk(C)(P) |
     |   433 | \|text_in_r_reg[124] /E v | MET Setup Check with Pin \|text_in_r_reg[124] /CP  |
1.022 |   1.242 |    2.264 | clk(D)(P) | clk(C)(P) |
     |   434 | \|text_in_r_reg[122] /E v | MET Setup Check with Pin \|text_in_r_reg[122] /CP  |
1.022 |   1.242 |    2.264 | clk(D)(P) | clk(C)(P) |
     |   435 | \|text_in_r_reg[120] /E v | MET Setup Check with Pin \|text_in_r_reg[120] /CP  |
1.028 |   1.236 |    2.265 | clk(D)(P) | clk(C)(P) |
     |   436 | \|text_in_r_reg[119] /E v | MET Setup Check with Pin \|text_in_r_reg[119] /CP  |
1.036 |   1.229 |    2.265 | clk(D)(P) | clk(C)(P) |
     |   437 |       \|dcnt_reg[2] /D ^ | MET Setup Check with Pin \|dcnt_reg[2] /CP         |
1.259 |   1.165 |    2.425 | clk(D)(P) | clk(C)(P) |
     |   438 |  \|text_in_r_reg[90] /E v | MET Setup Check with Pin \|text_in_r_reg[90] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   439 |  \|text_in_r_reg[89] /E v | MET Setup Check with Pin \|text_in_r_reg[89] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   440 |  \|text_in_r_reg[88] /E v | MET Setup Check with Pin \|text_in_r_reg[88] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   441 |  \|text_in_r_reg[87] /E v | MET Setup Check with Pin \|text_in_r_reg[87] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   442 |  \|text_in_r_reg[86] /E v | MET Setup Check with Pin \|text_in_r_reg[86] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   443 |  \|text_in_r_reg[85] /E v | MET Setup Check with Pin \|text_in_r_reg[85] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   444 |  \|text_in_r_reg[84] /E v | MET Setup Check with Pin \|text_in_r_reg[84] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   445 |  \|text_in_r_reg[83] /E v | MET Setup Check with Pin \|text_in_r_reg[83] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   446 |  \|text_in_r_reg[82] /E v | MET Setup Check with Pin \|text_in_r_reg[82] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   447 |  \|text_in_r_reg[81] /E v | MET Setup Check with Pin \|text_in_r_reg[81] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   448 |  \|text_in_r_reg[80] /E v | MET Setup Check with Pin \|text_in_r_reg[80] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   449 |  \|text_in_r_reg[79] /E v | MET Setup Check with Pin \|text_in_r_reg[79] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   450 |  \|text_in_r_reg[78] /E v | MET Setup Check with Pin \|text_in_r_reg[78] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   451 |  \|text_in_r_reg[77] /E v | MET Setup Check with Pin \|text_in_r_reg[77] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   452 |  \|text_in_r_reg[76] /E v | MET Setup Check with Pin \|text_in_r_reg[76] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   453 |  \|text_in_r_reg[75] /E v | MET Setup Check with Pin \|text_in_r_reg[75] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   454 |  \|text_in_r_reg[74] /E v | MET Setup Check with Pin \|text_in_r_reg[74] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   455 |  \|text_in_r_reg[73] /E v | MET Setup Check with Pin \|text_in_r_reg[73] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   456 |  \|text_in_r_reg[72] /E v | MET Setup Check with Pin \|text_in_r_reg[72] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   457 |  \|text_in_r_reg[71] /E v | MET Setup Check with Pin \|text_in_r_reg[71] /CP   |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   458 | \|text_in_r_reg[111] /E v | MET Setup Check with Pin \|text_in_r_reg[111] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   459 | \|text_in_r_reg[110] /E v | MET Setup Check with Pin \|text_in_r_reg[110] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   460 | \|text_in_r_reg[109] /E v | MET Setup Check with Pin \|text_in_r_reg[109] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   461 | \|text_in_r_reg[108] /E v | MET Setup Check with Pin \|text_in_r_reg[108] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   462 | \|text_in_r_reg[107] /E v | MET Setup Check with Pin \|text_in_r_reg[107] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   463 | \|text_in_r_reg[106] /E v | MET Setup Check with Pin \|text_in_r_reg[106] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
     |   464 | \|text_in_r_reg[105] /E v | MET Setup Check with Pin \|text_in_r_reg[105] /CP  |
1.277 |   1.069 |    2.346 | clk(D)(P) | clk(C)(P) |
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| 465 | \|text_in_r_reg[104] /E v | MET Setup Check with Pin \|text_in_r_reg[104] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 466 | \|text_in_r_reg[103] /E v | MET Setup Check with Pin \|text_in_r_reg[103] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 467 | \|text_in_r_reg[102] /E v | MET Setup Check with Pin \|text_in_r_reg[102] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 468 | \|text_in_r_reg[101] /E v | MET Setup Check with Pin \|text_in_r_reg[101] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 469 | \|text_in_r_reg[100] /E v | MET Setup Check with Pin \|text_in_r_reg[100] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 470 | \|text_in_r_reg[99] /E v | MET Setup Check with Pin \|text_in_r_reg[99] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 471 | \|text_in_r_reg[98] /E v | MET Setup Check with Pin \|text_in_r_reg[98] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 472 | \|text_in_r_reg[96] /E v | MET Setup Check with Pin \|text_in_r_reg[96] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 473 | \|text_in_r_reg[95] /E v | MET Setup Check with Pin \|text_in_r_reg[95] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 474 | \|text_in_r_reg[94] /E v | MET Setup Check with Pin \|text_in_r_reg[94] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 475 | \|text_in_r_reg[93] /E v | MET Setup Check with Pin \|text_in_r_reg[93] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 476 | \|text_in_r_reg[92] /E v | MET Setup Check with Pin \|text_in_r_reg[92] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 477 | \|text_in_r_reg[91] /E v | MET Setup Check with Pin \|text_in_r_reg[91] /CP |
1.277 | 1.069 | 2.346 | clk(D)(P) | clk(C)(P) |
| 478 | \|text_in_r_reg[51] /E v | MET Setup Check with Pin \|text_in_r_reg[51] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 479 | \|text_in_r_reg[50] /E v | MET Setup Check with Pin \|text_in_r_reg[50] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 480 | \|text_in_r_reg[49] /E v | MET Setup Check with Pin \|text_in_r_reg[49] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 481 | \|text_in_r_reg[48] /E v | MET Setup Check with Pin \|text_in_r_reg[48] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 482 | \|text_in_r_reg[47] /E v | MET Setup Check with Pin \|text_in_r_reg[47] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 483 | \|text_in_r_reg[46] /E v | MET Setup Check with Pin \|text_in_r_reg[46] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 484 | \|text_in_r_reg[45] /E v | MET Setup Check with Pin \|text_in_r_reg[45] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 485 | \|text_in_r_reg[44] /E v | MET Setup Check with Pin \|text_in_r_reg[44] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 486 | \|text_in_r_reg[43] /E v | MET Setup Check with Pin \|text_in_r_reg[43] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 487 | \|text_in_r_reg[42] /E v | MET Setup Check with Pin \|text_in_r_reg[42] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 488 | \|text_in_r_reg[41] /E v | MET Setup Check with Pin \|text_in_r_reg[41] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 489 | \|text_in_r_reg[40] /E v | MET Setup Check with Pin \|text_in_r_reg[40] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 490 | \|text_in_r_reg[39] /E v | MET Setup Check with Pin \|text_in_r_reg[39] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 491 | \|text_in_r_reg[38] /E v | MET Setup Check with Pin \|text_in_r_reg[38] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 492 | \|text_in_r_reg[37] /E v | MET Setup Check with Pin \|text_in_r_reg[37] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 493 | \|text_in_r_reg[36] /E v | MET Setup Check with Pin \|text_in_r_reg[36] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 494 | \|text_in_r_reg[35] /E v | MET Setup Check with Pin \|text_in_r_reg[35] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 495 | \|text_in_r_reg[34] /E v | MET Setup Check with Pin \|text_in_r_reg[34] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 496 | \|text_in_r_reg[33] /E v | MET Setup Check with Pin \|text_in_r_reg[33] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 497 | \|text_in_r_reg[32] /E v | MET Setup Check with Pin \|text_in_r_reg[32] /CP |
1.278 | 1.067 | 2.346 | clk(D)(P) | clk(C)(P) |
| 498 | \|text_in_r_reg[31] /E v | MET Setup Check with Pin \|text_in_r_reg[31] /CP |
1.287 | 1.059 | 2.346 | clk(D)(P) | clk(C)(P) |

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      |   499 |  \|text_in_r_reg[30] /E v | MET Setup Check with Pin \|text_in_r_reg[30] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   500 |  \|text_in_r_reg[29] /E v | MET Setup Check with Pin \|text_in_r_reg[29] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   501 |  \|text_in_r_reg[28] /E v | MET Setup Check with Pin \|text_in_r_reg[28] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   502 |  \|text_in_r_reg[27] /E v | MET Setup Check with Pin \|text_in_r_reg[27] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   503 |  \|text_in_r_reg[26] /E v | MET Setup Check with Pin \|text_in_r_reg[26] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   504 |  \|text_in_r_reg[25] /E v | MET Setup Check with Pin \|text_in_r_reg[25] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   505 |  \|text_in_r_reg[24] /E v | MET Setup Check with Pin \|text_in_r_reg[24] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   506 |  \|text_in_r_reg[23] /E v | MET Setup Check with Pin \|text_in_r_reg[23] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   507 |  \|text_in_r_reg[22] /E v | MET Setup Check with Pin \|text_in_r_reg[22] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   508 |  \|text_in_r_reg[21] /E v | MET Setup Check with Pin \|text_in_r_reg[21] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   509 |  \|text_in_r_reg[20] /E v | MET Setup Check with Pin \|text_in_r_reg[20] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   510 |  \|text_in_r_reg[19] /E v | MET Setup Check with Pin \|text_in_r_reg[19] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   511 |  \|text_in_r_reg[18] /E v | MET Setup Check with Pin \|text_in_r_reg[18] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   512 |  \|text_in_r_reg[17] /E v | MET Setup Check with Pin \|text_in_r_reg[17] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   513 |  \|text_in_r_reg[16] /E v | MET Setup Check with Pin \|text_in_r_reg[16] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   514 |  \|text_in_r_reg[15] /E v | MET Setup Check with Pin \|text_in_r_reg[15] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   515 |  \|text_in_r_reg[14] /E v | MET Setup Check with Pin \|text_in_r_reg[14] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   516 |  \|text_in_r_reg[13] /E v | MET Setup Check with Pin \|text_in_r_reg[13] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   517 |  \|text_in_r_reg[12] /E v | MET Setup Check with Pin \|text_in_r_reg[12] /CP   |
1.287 |   1.059 |    2.346 | clk(D)(P) | clk(C)(P) |
      |   518 | \|text_in_r_reg[102] /D v | MET Setup Check with Pin \|text_in_r_reg[102] /CP  |
1.606 |   0.760 |    2.367 | clk(D)(P) | clk(C)(P) |
      |   519 | \|text_in_r_reg[121] /D v | MET Setup Check with Pin \|text_in_r_reg[121] /CP  |
1.607 |   0.760 |    2.367 | clk(D)(P) | clk(C)(P) |
      |   520 | \|text_in_r_reg[105] /D v | MET Setup Check with Pin \|text_in_r_reg[105] /CP  |
1.610 |   0.758 |    2.368 | clk(D)(P) | clk(C)(P) |
      |   521 |  \|text_in_r_reg[71] /D v | MET Setup Check with Pin \|text_in_r_reg[71] /CP   |
1.610 |   0.759 |    2.368 | clk(D)(P) | clk(C)(P) |
      |   522 |  \|text_in_r_reg[11] /E ^ | MET Setup Check with Pin \|text_in_r_reg[11] /CP   |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   523 |  \|text_in_r_reg[10] /E ^ | MET Setup Check with Pin \|text_in_r_reg[10] /CP   |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   524 |   \|text_in_r_reg[9] /E ^ | MET Setup Check with Pin \|text_in_r_reg[9] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   525 |   \|text_in_r_reg[8] /E ^ | MET Setup Check with Pin \|text_in_r_reg[8] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   526 |   \|text_in_r_reg[7] /E ^ | MET Setup Check with Pin \|text_in_r_reg[7] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   527 |   \|text_in_r_reg[6] /E ^ | MET Setup Check with Pin \|text_in_r_reg[6] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   528 |   \|text_in_r_reg[5] /E ^ | MET Setup Check with Pin \|text_in_r_reg[5] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   529 |   \|text_in_r_reg[4] /E ^ | MET Setup Check with Pin \|text_in_r_reg[4] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   530 |   \|text_in_r_reg[3] /E ^ | MET Setup Check with Pin \|text_in_r_reg[3] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   531 |   \|text_in_r_reg[2] /E ^ | MET Setup Check with Pin \|text_in_r_reg[2] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
      |   532 |   \|text_in_r_reg[1] /E ^ | MET Setup Check with Pin \|text_in_r_reg[1] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
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     |   533 |   \|text_in_r_reg[0] /E ^ | MET Setup Check with Pin \|text_in_r_reg[0] /CP    |
1.611 |   0.753 |    2.364 | clk(D)(P) | clk(C)(P) |
     |   534 | \|text_in_r_reg[123] /D v | MET Setup Check with Pin \|text_in_r_reg[123] /CP  |
1.612 |   0.757 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   535 |  \|text_in_r_reg[67] /D v | MET Setup Check with Pin \|text_in_r_reg[67] /CP   |
1.612 |   0.756 |    2.368 | clk(D)(P) | clk(C)(P) |
     |   536 | \|text_in_r_reg[116] /D v | MET Setup Check with Pin \|text_in_r_reg[116] /CP  |
1.613 |   0.756 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   537 |  \|text_in_r_reg[96] /D v | MET Setup Check with Pin \|text_in_r_reg[96] /CP   |
1.614 |   0.755 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   538 | \|text_in_r_reg[117] /D v | MET Setup Check with Pin \|text_in_r_reg[117] /CP  |
1.614 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   539 | \|text_in_r_reg[127] /D v | MET Setup Check with Pin \|text_in_r_reg[127] /CP  |
1.615 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   540 | \|text_in_r_reg[109] /D v | MET Setup Check with Pin \|text_in_r_reg[109] /CP  |
1.615 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   541 |  \|text_in_r_reg[97] /D v | MET Setup Check with Pin \|text_in_r_reg[97] /CP   |
1.615 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   542 | \|text_in_r_reg[125] /D v | MET Setup Check with Pin \|text_in_r_reg[125] /CP  |
1.615 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   543 | \|text_in_r_reg[118] /D v | MET Setup Check with Pin \|text_in_r_reg[118] /CP  |
1.615 |   0.754 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   544 |  \|text_in_r_reg[99] /D v | MET Setup Check with Pin \|text_in_r_reg[99] /CP   |
1.615 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   545 | \|text_in_r_reg[119] /D v | MET Setup Check with Pin \|text_in_r_reg[119] /CP  |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   546 |  \|text_in_r_reg[11] /D v | MET Setup Check with Pin \|text_in_r_reg[11] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   547 | \|text_in_r_reg[115] /D v | MET Setup Check with Pin \|text_in_r_reg[115] /CP  |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   548 |  \|text_in_r_reg[78] /D v | MET Setup Check with Pin \|text_in_r_reg[78] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   549 |  \|text_in_r_reg[84] /D v | MET Setup Check with Pin \|text_in_r_reg[84] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   550 |  \|text_in_r_reg[30] /D v | MET Setup Check with Pin \|text_in_r_reg[30] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   551 |  \|text_in_r_reg[29] /D v | MET Setup Check with Pin \|text_in_r_reg[29] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   552 | \|text_in_r_reg[113] /D v | MET Setup Check with Pin \|text_in_r_reg[113] /CP  |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   553 |  \|text_in_r_reg[18] /D v | MET Setup Check with Pin \|text_in_r_reg[18] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   554 |  \|text_in_r_reg[79] /D v | MET Setup Check with Pin \|text_in_r_reg[79] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   555 |  \|text_in_r_reg[54] /D v | MET Setup Check with Pin \|text_in_r_reg[54] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   556 |  \|text_in_r_reg[16] /D v | MET Setup Check with Pin \|text_in_r_reg[16] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   557 |  \|text_in_r_reg[13] /D v | MET Setup Check with Pin \|text_in_r_reg[13] /CP   |
1.616 |   0.753 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   558 |  \|text_in_r_reg[43] /D v | MET Setup Check with Pin \|text_in_r_reg[43] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   559 |  \|text_in_r_reg[22] /D v | MET Setup Check with Pin \|text_in_r_reg[22] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   560 |  \|text_in_r_reg[81] /D v | MET Setup Check with Pin \|text_in_r_reg[81] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   561 |  \|text_in_r_reg[62] /D v | MET Setup Check with Pin \|text_in_r_reg[62] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   562 |  \|text_in_r_reg[49] /D v | MET Setup Check with Pin \|text_in_r_reg[49] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   563 | \|text_in_r_reg[120] /D v | MET Setup Check with Pin \|text_in_r_reg[120] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   564 | \|text_in_r_reg[104] /D v | MET Setup Check with Pin \|text_in_r_reg[104] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   565 |  \|text_in_r_reg[82] /D v | MET Setup Check with Pin \|text_in_r_reg[82] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   566 |  \|text_in_r_reg[51] /D v | MET Setup Check with Pin \|text_in_r_reg[51] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
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     |   567 |  \|text_in_r_reg[15] /D v | MET Setup Check with Pin \|text_in_r_reg[15] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   568 | \|text_in_r_reg[114] /D v | MET Setup Check with Pin \|text_in_r_reg[114] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   569 |  \|text_in_r_reg[19] /D v | MET Setup Check with Pin \|text_in_r_reg[19] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   570 |   \|text_in_r_reg[9] /D v | MET Setup Check with Pin \|text_in_r_reg[9] /CP    |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   571 | \|text_in_r_reg[126] /D v | MET Setup Check with Pin \|text_in_r_reg[126] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   572 |  \|text_in_r_reg[55] /D v | MET Setup Check with Pin \|text_in_r_reg[55] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   573 |  \|text_in_r_reg[52] /D v | MET Setup Check with Pin \|text_in_r_reg[52] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   574 | \|text_in_r_reg[110] /D v | MET Setup Check with Pin \|text_in_r_reg[110] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   575 |  \|text_in_r_reg[75] /D v | MET Setup Check with Pin \|text_in_r_reg[75] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   576 |  \|text_in_r_reg[63] /D v | MET Setup Check with Pin \|text_in_r_reg[63] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   577 |  \|text_in_r_reg[58] /D v | MET Setup Check with Pin \|text_in_r_reg[58] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   578 |  \|text_in_r_reg[41] /D v | MET Setup Check with Pin \|text_in_r_reg[41] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   579 |   \|text_in_r_reg[7] /D v | MET Setup Check with Pin \|text_in_r_reg[7] /CP    |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   580 |   \|text_in_r_reg[0] /D v | MET Setup Check with Pin \|text_in_r_reg[0] /CP    |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   581 | \|text_in_r_reg[111] /D v | MET Setup Check with Pin \|text_in_r_reg[111] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   582 |  \|text_in_r_reg[83] /D v | MET Setup Check with Pin \|text_in_r_reg[83] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   583 |  \|text_in_r_reg[74] /D v | MET Setup Check with Pin \|text_in_r_reg[74] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   584 |  \|text_in_r_reg[61] /D v | MET Setup Check with Pin \|text_in_r_reg[61] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   585 |  \|text_in_r_reg[57] /D v | MET Setup Check with Pin \|text_in_r_reg[57] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   586 | \|text_in_r_reg[108] /D v | MET Setup Check with Pin \|text_in_r_reg[108] /CP  |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   587 |  \|text_in_r_reg[76] /D v | MET Setup Check with Pin \|text_in_r_reg[76] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   588 |  \|text_in_r_reg[73] /D v | MET Setup Check with Pin \|text_in_r_reg[73] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   589 |  \|text_in_r_reg[40] /D v | MET Setup Check with Pin \|text_in_r_reg[40] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   590 |  \|text_in_r_reg[24] /D v | MET Setup Check with Pin \|text_in_r_reg[24] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   591 |  \|text_in_r_reg[23] /D v | MET Setup Check with Pin \|text_in_r_reg[23] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   592 |   \|text_in_r_reg[8] /D v | MET Setup Check with Pin \|text_in_r_reg[8] /CP    |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   593 |  \|text_in_r_reg[86] /D v | MET Setup Check with Pin \|text_in_r_reg[86] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   594 |  \|text_in_r_reg[80] /D v | MET Setup Check with Pin \|text_in_r_reg[80] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   595 |  \|text_in_r_reg[38] /D v | MET Setup Check with Pin \|text_in_r_reg[38] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   596 |  \|text_in_r_reg[34] /D v | MET Setup Check with Pin \|text_in_r_reg[34] /CP   |
1.617 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   597 | \|text_in_r_reg[122] /D v | MET Setup Check with Pin \|text_in_r_reg[122] /CP  |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   598 |  \|text_in_r_reg[72] /D v | MET Setup Check with Pin \|text_in_r_reg[72] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   599 |  \|text_in_r_reg[44] /D v | MET Setup Check with Pin \|text_in_r_reg[44] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   600 |  \|text_in_r_reg[42] /D v | MET Setup Check with Pin \|text_in_r_reg[42] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
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      |   601 |  \|text_in_r_reg[36] /D v | MET Setup Check with Pin \|text_in_r_reg[36] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   602 |  \|text_in_r_reg[35] /D v | MET Setup Check with Pin \|text_in_r_reg[35] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   603 | \|text_in_r_reg[124] /D v | MET Setup Check with Pin \|text_in_r_reg[124] /CP  |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   604 | \|text_in_r_reg[112] /D v | MET Setup Check with Pin \|text_in_r_reg[112] /CP  |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   605 |  \|text_in_r_reg[88] /D v | MET Setup Check with Pin \|text_in_r_reg[88] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   606 |  \|text_in_r_reg[69] /D v | MET Setup Check with Pin \|text_in_r_reg[69] /CP   |
1.618 |   0.752 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   607 | \|text_in_r_reg[106] /D v | MET Setup Check with Pin \|text_in_r_reg[106] /CP  |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   608 |  \|text_in_r_reg[77] /D v | MET Setup Check with Pin \|text_in_r_reg[77] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   609 |  \|text_in_r_reg[50] /D v | MET Setup Check with Pin \|text_in_r_reg[50] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   610 |  \|text_in_r_reg[48] /D v | MET Setup Check with Pin \|text_in_r_reg[48] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   611 |  \|text_in_r_reg[45] /D v | MET Setup Check with Pin \|text_in_r_reg[45] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   612 |  \|text_in_r_reg[39] /D v | MET Setup Check with Pin \|text_in_r_reg[39] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   613 |  \|text_in_r_reg[33] /D v | MET Setup Check with Pin \|text_in_r_reg[33] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   614 |  \|text_in_r_reg[26] /D v | MET Setup Check with Pin \|text_in_r_reg[26] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   615 |  \|text_in_r_reg[20] /D v | MET Setup Check with Pin \|text_in_r_reg[20] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   616 |  \|text_in_r_reg[87] /D v | MET Setup Check with Pin \|text_in_r_reg[87] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   617 |  \|text_in_r_reg[85] /D v | MET Setup Check with Pin \|text_in_r_reg[85] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   618 |  \|text_in_r_reg[47] /D v | MET Setup Check with Pin \|text_in_r_reg[47] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   619 |  \|text_in_r_reg[46] /D v | MET Setup Check with Pin \|text_in_r_reg[46] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   620 |  \|text_in_r_reg[37] /D v | MET Setup Check with Pin \|text_in_r_reg[37] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   621 |  \|text_in_r_reg[32] /D v | MET Setup Check with Pin \|text_in_r_reg[32] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   622 | \|text_in_r_reg[101] /D v | MET Setup Check with Pin \|text_in_r_reg[101] /CP  |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   623 |  \|text_in_r_reg[98] /D v | MET Setup Check with Pin \|text_in_r_reg[98] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   624 |  \|text_in_r_reg[66] /D v | MET Setup Check with Pin \|text_in_r_reg[66] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   625 |   \|text_in_r_reg[4] /D v | MET Setup Check with Pin \|text_in_r_reg[4] /CP    |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   626 |   \|text_in_r_reg[2] /D v | MET Setup Check with Pin \|text_in_r_reg[2] /CP    |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   627 | \|text_in_r_reg[100] /D v | MET Setup Check with Pin \|text_in_r_reg[100] /CP  |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   628 |  \|text_in_r_reg[68] /D v | MET Setup Check with Pin \|text_in_r_reg[68] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   629 |  \|text_in_r_reg[89] /D v | MET Setup Check with Pin \|text_in_r_reg[89] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   630 |  \|text_in_r_reg[90] /D v | MET Setup Check with Pin \|text_in_r_reg[90] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   631 | \|text_in_r_reg[107] /D v | MET Setup Check with Pin \|text_in_r_reg[107] /CP  |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   632 |  \|text_in_r_reg[70] /D v | MET Setup Check with Pin \|text_in_r_reg[70] /CP   |
1.618 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   633 |  \|text_in_r_reg[10] /D v | MET Setup Check with Pin \|text_in_r_reg[10] /CP   |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
      |   634 |   \|text_in_r_reg[6] /D v | MET Setup Check with Pin \|text_in_r_reg[6] /CP    |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
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     |   635 | \|text_in_r_reg[103] /D v | MET Setup Check with Pin \|text_in_r_reg[103] /CP  |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   636 |  \|text_in_r_reg[95] /D v | MET Setup Check with Pin \|text_in_r_reg[95] /CP   |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   637 |  \|text_in_r_reg[93] /D v | MET Setup Check with Pin \|text_in_r_reg[93] /CP   |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   638 |  \|text_in_r_reg[25] /D v | MET Setup Check with Pin \|text_in_r_reg[25] /CP   |
1.619 |   0.751 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   639 |  \|text_in_r_reg[27] /D v | MET Setup Check with Pin \|text_in_r_reg[27] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   640 |  \|text_in_r_reg[21] /D v | MET Setup Check with Pin \|text_in_r_reg[21] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   641 |  \|text_in_r_reg[14] /D v | MET Setup Check with Pin \|text_in_r_reg[14] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   642 |  \|text_in_r_reg[92] /D v | MET Setup Check with Pin \|text_in_r_reg[92] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   643 |   \|text_in_r_reg[5] /D v | MET Setup Check with Pin \|text_in_r_reg[5] /CP    |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   644 |   \|text_in_r_reg[3] /D v | MET Setup Check with Pin \|text_in_r_reg[3] /CP    |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   645 |  \|text_in_r_reg[91] /D v | MET Setup Check with Pin \|text_in_r_reg[91] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   646 |  \|text_in_r_reg[53] /D v | MET Setup Check with Pin \|text_in_r_reg[53] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   647 |  \|text_in_r_reg[94] /D v | MET Setup Check with Pin \|text_in_r_reg[94] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   648 |  \|text_in_r_reg[64] /D v | MET Setup Check with Pin \|text_in_r_reg[64] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   649 |  \|text_in_r_reg[60] /D v | MET Setup Check with Pin \|text_in_r_reg[60] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   650 |  \|text_in_r_reg[59] /D v | MET Setup Check with Pin \|text_in_r_reg[59] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   651 |  \|text_in_r_reg[28] /D v | MET Setup Check with Pin \|text_in_r_reg[28] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   652 |  \|text_in_r_reg[12] /D v | MET Setup Check with Pin \|text_in_r_reg[12] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   653 |   \|text_in_r_reg[1] /D v | MET Setup Check with Pin \|text_in_r_reg[1] /CP    |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   654 |  \|text_in_r_reg[65] /D v | MET Setup Check with Pin \|text_in_r_reg[65] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   655 |  \|text_in_r_reg[56] /D v | MET Setup Check with Pin \|text_in_r_reg[56] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   656 |  \|text_in_r_reg[31] /D v | MET Setup Check with Pin \|text_in_r_reg[31] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   657 |  \|text_in_r_reg[17] /D v | MET Setup Check with Pin \|text_in_r_reg[17] /CP   |
1.619 |   0.750 |    2.369 | clk(D)(P) | clk(C)(P) |
     |   658 |          \|ld_r_reg /D v | MET Setup Check with Pin \|ld_r_reg /CP            |
1.671 |   0.753 |    2.424 | clk(D)(P) | clk(C)(P) |
     |   659 |           text_out[12] v | MET Late External Delay Assertion                  |
1.952 |   0.148 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   660 |            text_out[0] v | MET Late External Delay Assertion                  |
1.953 |   0.146 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   661 |           text_out[24] v | MET Late External Delay Assertion                  |
1.956 |   0.144 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   662 |           text_out[96] v | MET Late External Delay Assertion                  |
1.956 |   0.143 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   663 |           text_out[39] v | MET Late External Delay Assertion                  |
1.957 |   0.143 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   664 |          text_out[114] v | MET Late External Delay Assertion                  |
1.958 |   0.142 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   665 |          text_out[123] v | MET Late External Delay Assertion                  |
1.960 |   0.140 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   666 |          text_out[113] v | MET Late External Delay Assertion                  |
1.960 |   0.140 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   667 |           text_out[29] v | MET Late External Delay Assertion                  |
1.961 |   0.139 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   668 |          text_out[108] v | MET Late External Delay Assertion                  |
1.963 |   0.137 |    2.100 | clk(D)(P) | clk(C)(P) |
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669	text_out[32] v	MET Late External Delay Assertion
1.964	0.136	2.100	clk(D)(P)	clk(C)(P)
670	text_out[81] v	MET Late External Delay Assertion
1.966	0.134	2.100	clk(D)(P)	clk(C)(P)
671	text_out[118] v	MET Late External Delay Assertion
1.966	0.134	2.100	clk(D)(P)	clk(C)(P)
672	text_out[41] v	MET Late External Delay Assertion
1.967	0.132	2.100	clk(D)(P)	clk(C)(P)
673	text_out[2] v	MET Late External Delay Assertion
1.968	0.132	2.100	clk(D)(P)	clk(C)(P)
674	text_out[77] v	MET Late External Delay Assertion
1.968	0.132	2.100	clk(D)(P)	clk(C)(P)
675	text_out[80] v	MET Late External Delay Assertion
1.968	0.132	2.100	clk(D)(P)	clk(C)(P)
676	text_out[15] v	MET Late External Delay Assertion
1.969	0.131	2.100	clk(D)(P)	clk(C)(P)
677	text_out[43] v	MET Late External Delay Assertion
1.970	0.130	2.100	clk(D)(P)	clk(C)(P)
678	text_out[34] v	MET Late External Delay Assertion
1.971	0.129	2.100	clk(D)(P)	clk(C)(P)
679	text_out[49] v	MET Late External Delay Assertion
1.971	0.129	2.100	clk(D)(P)	clk(C)(P)
680	text_out[102] v	MET Late External Delay Assertion
1.971	0.129	2.100	clk(D)(P)	clk(C)(P)
681	text_out[66] v	MET Late External Delay Assertion
1.972	0.128	2.100	clk(D)(P)	clk(C)(P)
682	text_out[50] v	MET Late External Delay Assertion
1.972	0.128	2.100	clk(D)(P)	clk(C)(P)
683	text_out[33] v	MET Late External Delay Assertion
1.974	0.125	2.100	clk(D)(P)	clk(C)(P)
684	text_out[54] v	MET Late External Delay Assertion
1.975	0.125	2.100	clk(D)(P)	clk(C)(P)
685	text_out[76] v	MET Late External Delay Assertion
1.975	0.125	2.100	clk(D)(P)	clk(C)(P)
686	text_out[112] v	MET Late External Delay Assertion
1.976	0.124	2.100	clk(D)(P)	clk(C)(P)
687	text_out[86] v	MET Late External Delay Assertion
1.976	0.124	2.100	clk(D)(P)	clk(C)(P)
688	text_out[101] v	MET Late External Delay Assertion
1.977	0.123	2.100	clk(D)(P)	clk(C)(P)
689	text_out[35] v	MET Late External Delay Assertion
1.978	0.122	2.100	clk(D)(P)	clk(C)(P)
690	text_out[74] v	MET Late External Delay Assertion
1.978	0.122	2.100	clk(D)(P)	clk(C)(P)
691	text_out[105] v	MET Late External Delay Assertion
1.978	0.122	2.100	clk(D)(P)	clk(C)(P)
692	text_out[106] v	MET Late External Delay Assertion
1.979	0.121	2.100	clk(D)(P)	clk(C)(P)
693	text_out[48] v	MET Late External Delay Assertion
1.979	0.121	2.100	clk(D)(P)	clk(C)(P)
694	text_out[115] v	MET Late External Delay Assertion
1.979	0.121	2.100	clk(D)(P)	clk(C)(P)
695	text_out[92] v	MET Late External Delay Assertion
1.979	0.120	2.100	clk(D)(P)	clk(C)(P)
696	text_out[104] v	MET Late External Delay Assertion
1.980	0.120	2.100	clk(D)(P)	clk(C)(P)
697	text_out[31] v	MET Late External Delay Assertion
1.981	0.119	2.100	clk(D)(P)	clk(C)(P)
698	text_out[107] v	MET Late External Delay Assertion
1.981	0.119	2.100	clk(D)(P)	clk(C)(P)
699	text_out[98] v	MET Late External Delay Assertion
1.981	0.119	2.100	clk(D)(P)	clk(C)(P)
700	text_out[7] v	MET Late External Delay Assertion
1.982	0.118	2.100	clk(D)(P)	clk(C)(P)
701	text_out[8] v	MET Late External Delay Assertion
1.982	0.118	2.100	clk(D)(P)	clk(C)(P)
702	text_out[6] v	MET Late External Delay Assertion
1.982	0.118	2.100	clk(D)(P)	clk(C)(P)

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      |   703 |           text_out[110] v | MET Late External Delay Assertion                |
1.982 |   0.118 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   704 |           text_out[111] v | MET Late External Delay Assertion                |
1.982 |   0.118 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   705 |            text_out[45] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   706 |            text_out[13] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   707 |            text_out[51] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   708 |            text_out[97] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   709 |            text_out[36] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   710 |            text_out[37] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   711 |            text_out[78] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   712 |            text_out[60] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   713 |           text_out[109] v | MET Late External Delay Assertion                |
1.983 |   0.117 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   714 |            text_out[47] v | MET Late External Delay Assertion                |
1.984 |   0.116 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   715 |            text_out[99] v | MET Late External Delay Assertion                |
1.984 |   0.115 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   716 |            text_out[53] v | MET Late External Delay Assertion                |
1.985 |   0.115 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   717 |            text_out[72] v | MET Late External Delay Assertion                |
1.985 |   0.115 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   718 |           text_out[125] v | MET Late External Delay Assertion                |
1.985 |   0.115 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   719 |           text_out[126] v | MET Late External Delay Assertion                |
1.985 |   0.115 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   720 |            text_out[52] v | MET Late External Delay Assertion                |
1.986 |   0.114 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   721 |             text_out[5] v | MET Late External Delay Assertion                |
1.986 |   0.114 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   722 |           text_out[117] v | MET Late External Delay Assertion                |
1.986 |   0.114 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   723 |           text_out[100] v | MET Late External Delay Assertion                |
1.986 |   0.114 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   724 |            text_out[23] v | MET Late External Delay Assertion                |
1.986 |   0.114 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   725 |            text_out[42] v | MET Late External Delay Assertion                |
1.987 |   0.113 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   726 |            text_out[20] v | MET Late External Delay Assertion                |
1.987 |   0.113 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   727 |           text_out[103] v | MET Late External Delay Assertion                |
1.987 |   0.113 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   728 |            text_out[44] v | MET Late External Delay Assertion                |
1.987 |   0.112 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   729 |            text_out[19] v | MET Late External Delay Assertion                |
1.988 |   0.112 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   730 |            text_out[16] v | MET Late External Delay Assertion                |
1.988 |   0.112 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   731 |            text_out[70] v | MET Late External Delay Assertion                |
1.988 |   0.112 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   732 |            text_out[26] v | MET Late External Delay Assertion                |
1.988 |   0.112 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   733 |            text_out[25] v | MET Late External Delay Assertion                |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   734 |           text_out[120] v | MET Late External Delay Assertion                |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   735 |           text_out[119] v | MET Late External Delay Assertion                |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   736 |           text_out[124] v | MET Late External Delay Assertion                |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
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      |   737 |           text_out[28] v | MET Late External Delay Assertion                 |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   738 |          text_out[121] v | MET Late External Delay Assertion                 |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   739 |           text_out[22] v | MET Late External Delay Assertion                 |
1.989 |   0.111 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   740 |          text_out[116] v | MET Late External Delay Assertion                 |
1.990 |   0.110 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   741 |           text_out[10] v | MET Late External Delay Assertion                 |
1.990 |   0.110 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   742 |           text_out[21] v | MET Late External Delay Assertion                 |
1.990 |   0.110 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   743 |           text_out[14] v | MET Late External Delay Assertion                 |
1.990 |   0.110 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   744 |           text_out[64] v | MET Late External Delay Assertion                 |
1.990 |   0.110 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   745 |           text_out[30] v | MET Late External Delay Assertion                 |
1.992 |   0.108 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   746 |           text_out[82] v | MET Late External Delay Assertion                 |
1.992 |   0.107 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   747 |           text_out[11] v | MET Late External Delay Assertion                 |
1.993 |   0.107 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   748 |            text_out[1] v | MET Late External Delay Assertion                 |
1.997 |   0.102 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   749 |           text_out[93] v | MET Late External Delay Assertion                 |
1.998 |   0.102 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   750 |          text_out[127] v | MET Late External Delay Assertion                 |
1.999 |   0.101 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   751 |           text_out[87] v | MET Late External Delay Assertion                 |
2.003 |   0.097 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   752 |           text_out[84] v | MET Late External Delay Assertion                 |
2.003 |   0.097 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   753 |           text_out[73] v | MET Late External Delay Assertion                 |
2.003 |   0.097 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   754 |           text_out[89] v | MET Late External Delay Assertion                 |
2.007 |   0.093 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   755 |           text_out[71] v | MET Late External Delay Assertion                 |
2.010 |   0.090 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   756 |          text_out[122] v | MET Late External Delay Assertion                 |
2.010 |   0.090 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   757 |                  done v | MET Late External Delay Assertion                 |
2.012 |   0.088 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   758 |            text_out[9] v | MET Late External Delay Assertion                 |
2.014 |   0.086 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   759 |           text_out[79] v | MET Late External Delay Assertion                 |
2.014 |   0.086 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   760 |           text_out[83] v | MET Late External Delay Assertion                 |
2.015 |   0.085 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   761 |           text_out[68] v | MET Late External Delay Assertion                 |
2.015 |   0.085 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   762 |           text_out[69] v | MET Late External Delay Assertion                 |
2.016 |   0.084 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   763 |           text_out[75] v | MET Late External Delay Assertion                 |
2.016 |   0.084 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   764 |           text_out[65] v | MET Late External Delay Assertion                 |
2.016 |   0.083 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   765 |           text_out[40] v | MET Late External Delay Assertion                 |
2.017 |   0.083 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   766 |           text_out[88] v | MET Late External Delay Assertion                 |
2.017 |   0.083 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   767 |           text_out[55] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   768 |           text_out[27] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   769 |           text_out[17] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
      |   770 |           text_out[63] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
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     |   771 |            text_out[90] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   772 |            text_out[56] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   773 |            text_out[46] v | MET Late External Delay Assertion                 |
2.018 |   0.082 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   774 |            text_out[91] v | MET Late External Delay Assertion                 |
2.020 |   0.080 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   775 |            text_out[85] v | MET Late External Delay Assertion                 |
2.020 |   0.080 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   776 |             text_out[3] v | MET Late External Delay Assertion                 |
2.020 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   777 |            text_out[95] v | MET Late External Delay Assertion                 |
2.020 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   778 |            text_out[18] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   779 |            text_out[94] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   780 |            text_out[38] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   781 |            text_out[57] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   782 |            text_out[58] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   783 |            text_out[59] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   784 |            text_out[61] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   785 |            text_out[62] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   786 |            text_out[67] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     |   787 |             text_out[4] v | MET Late External Delay Assertion                 |
2.021 |   0.079 |    2.100 | clk(D)(P) | clk(C)(P) |
     +-------------------------------------------------------------------------------------------
-------------------------------------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 100 -net -
summary > timing_reports/report_timing.post_extract.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 100 -net >
timing_reports/report_timing.post_extract.slack
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 300 -net -
summary > timing_reports/report_timing.post_extract.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
<CMD> set_propagated_clock clk
<CMD> setAnalysisMode -analysisType single -checkType hold -skew true -clockPropagation
sdccontrol
<CMD> report_timing
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:01.7, MEM = 374.9M)
Number of Loop : 0
Start delay calculation (mem=374.859M)...
delayCal using detail RC...
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
```

```
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[124] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[124] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[120] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[120] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[57] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[57] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[58] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[58] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
Delay calculation completed. (cpu=0:00:01.8 real=0:00:02.0 mem=374.859M 0)
*** CDM Built up (cpu=0:00:05.0  real=0:00:05.0  mem= 374.9M) ***
Path 1: MET Hold Check with Pin \|dcnt_reg[0] /CP
Endpoint:   \|dcnt_reg[0] /D (v) checked with  leading edge of 'clk'
Beginpoint: \|dcnt_reg[0] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.045
+ Hold                         -0.011
+ Phase Shift                   0.000
= Required Time                 0.034
  Arrival Time                  0.205
  Slack Time                    0.171
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.045
     = Beginpoint Arrival Time       0.045
     +-------------------------------------------------------------------------------+
     |   Instance    |     Arc     |      Cell       | Delay | Arrival | Required |
     |               |             |                 |       |  Time   |   Time   |
     |---------------+-------------+-----------------+-------+---------+----------|
     | \|dcnt_reg[0] | CP ^        |                 |       |   0.045 |   -0.127 |
     | \|dcnt_reg[0] | CP ^ -> Q ^ | HS65_GS_DFPQX4  | 0.117 |   0.162 |   -0.009 |
     | \|U1565       | A ^ -> Z v  | HS65_GS_OAI21X3 | 0.043 |   0.205 |    0.034 |
     | \|dcnt_reg[0] | D v         | HS65_GS_DFPQX4  | 0.000 |   0.205 |    0.034 |
     +-------------------------------------------------------------------------------+

<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -max_points 10 -net -
summary > timing_reports/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -early -max_points 100 -net -
summary > timing_reports/report_timing.post_extract.hold.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
```

```
<CMD> setAnalysisMode -analysisType single -checkType setup -skew true -clockPropagation
sdccontrol
<CMD> report_timing -summary
**WARN: (TCLCMD-566):  Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
Calculate delays in Single mode...
Topological Sorting (CPU = 0:00:01.7, MEM = 374.9M)
Number of Loop : 0
Start delay calculation (mem=374.859M)...
delayCal using detail RC...
**WARN: (ENCDC-348):   The output pin \|text_out_reg[121] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[121] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[123] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[123] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[125] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[125] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[126] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[126] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[127] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[127] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[122] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[122] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[124] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[124] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[120] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[120] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[57] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[57] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[58] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):   The output pin \|text_out_reg[58] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
Delay calculation completed. (cpu=0:00:01.8 real=0:00:01.0 mem=374.859M 0)
*** CDM Built up (cpu=0:00:05.0  real=0:00:05.0  mem= 374.9M) ***
     +-------------------------------------------------------------------------------------------
-------------------------------------------------+
     |  Path |                       Pin | Cause                                                |
Slack | Arrival | Required |     Phase | Other Phase |
     |   No. |                           |                                                      |
|         |          |           |             |
     |-------+--------------------------+------------------------------------------------------+--
------+---------+----------+-----------+-------------|
     |     1 |    \|u0|w_reg[2][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[2][24] /C | -
1.431 |   3.933 |    2.502 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                    |
|         |          |           |             |
     |     2 |    \|u0|w_reg[3][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][24] /C | -
1.128 |   3.578 |    2.450 | clk(D)(P) | clk(C)(P) * |
```

```
     |       |                           | P                                                                                |
|         |          |                |           |
     |     3 |       \|sa21_reg[4] /D v | VIOLATED Setup Check with Pin \|sa21_reg[4] /CP    | -
1.121 |   3.555 |    2.434 | clk(D)(P) | clk(C)(P) * |
     |     4 |    \|u0|w_reg[3][25] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][25] /C | -
1.108 |   3.615 |    2.507 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |     5 |    \|u0|w_reg[2][25] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][25] /C | -
1.085 |   3.582 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |     6 |     \|u0|w_reg[3][0] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][0] /CP | -
1.084 |   3.582 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |     7 |     \|u0|w_reg[2][0] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][0] /CP | -
1.031 |   3.529 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |     8 |    \|u0|w_reg[3][30] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][30] /C | -
1.023 |   3.531 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |     9 |    \|u0|w_reg[2][30] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][30] /C | -
0.990 |   3.487 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    10 |    \|u0|w_reg[3][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][31] /C | -
0.985 |   3.481 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    11 |    \|u0|w_reg[2][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][31] /C | -
0.964 |   3.461 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    12 |     \|u0|w_reg[1][0] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][0] /CP | -
0.895 |   3.405 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |    13 |    \|u0|w_reg[3][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][26] /C | -
0.889 |   3.387 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    14 |       \|sa21_reg[1] /D v | VIOLATED Setup Check with Pin \|sa21_reg[1] /CP    | -
0.886 |   3.334 |    2.448 | clk(D)(P) | clk(C)(P) * |
     |    15 |     \|u0|w_reg[3][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][6] /CP | -
0.880 |   3.378 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |    16 |       \|sa10_reg[4] /D v | VIOLATED Setup Check with Pin \|sa10_reg[4] /CP    | -
0.864 |   3.297 |    2.433 | clk(D)(P) | clk(C)(P) * |
     |    17 |     \|u0|w_reg[3][7] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][7] /CP | -
0.851 |   3.349 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    18 |    \|u0|w_reg[2][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][26] /C | -
0.832 |   3.323 |    2.492 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    19 |    \|u0|w_reg[1][25] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][25] /C | -
0.804 |   3.305 |    2.501 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    20 |     \|u0|w_reg[2][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][6] /CP | -
0.790 |   3.285 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |    21 |       \|sa31_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[1] /CP    | -
0.764 |   3.252 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |    22 |    \|u0|w_reg[1][30] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][30] /C | -
0.763 |   3.269 |    2.506 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
     |    23 |     \|u0|w_reg[2][7] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][7] /CP | -
0.742 |   3.240 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    24 |    \|u0|w_reg[1][31] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][31] /C | -
0.707 |   3.208 |    2.501 | clk(D)(P) | clk(C)(P) * |
     |       |                           | P                                                                                |
|         |          |                |           |
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     |    25 |     \|u0|w_reg[1][6] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][6] /CP | -
0.685 |   3.181 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |    26 |    \|u0|w_reg[1][24] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][24] /C | -
0.668 |   3.172 |    2.504 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    27 |     \|u0|w_reg[3][3] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][3] /CP | -
0.653 |   3.149 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |    28 |     \|u0|w_reg[0][0] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][0] /CP | -
0.630 |   3.135 |    2.505 | clk(D)(P) | clk(C)(P) * |
     |    29 |    \|u0|w_reg[3][21] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][21] /C | -
0.604 |   3.101 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    30 |    \|u0|w_reg[3][27] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][27] /C | -
0.603 |   3.093 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    31 |     \|u0|w_reg[1][7] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][7] /CP | -
0.599 |   3.107 |    2.509 | clk(D)(P) | clk(C)(P) * |
     |    32 |    \|u0|w_reg[1][26] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][26] /C | -
0.596 |   3.104 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    33 |    \|u0|w_reg[3][29] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][29] /C | -
0.573 |   3.070 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    34 |     \|u0|w_reg[2][3] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][3] /CP | -
0.557 |   3.052 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |    35 |     \|u0|w_reg[3][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][4] /CP | -
0.547 |   3.044 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |    36 |     \|u0|w_reg[3][5] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][5] /CP | -
0.546 |   3.043 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |    37 |       \|sa20_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[1] /CP    | -
0.545 |   3.023 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |    38 |    \|u0|w_reg[2][21] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][21] /C | -
0.541 |   3.039 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    39 |    \|u0|w_reg[2][27] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][27] /C | -
0.527 |   3.020 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    40 |    \|u0|w_reg[2][29] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][29] /C | -
0.508 |   3.006 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    41 |       \|sa10_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[0] /CP    | -
0.488 |   2.984 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |    42 |       \|sa30_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[1] /CP    | -
0.480 |   2.962 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |    43 |    \|u0|w_reg[3][23] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][23] /C | -
0.478 |   2.940 |    2.462 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    44 |    \|u0|w_reg[3][28] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][28] /C | -
0.476 |   2.973 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |    45 |     \|u0|w_reg[0][6] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][6] /CP | -
0.476 |   2.980 |    2.504 | clk(D)(P) | clk(C)(P) * |
     |    46 |     \|u0|w_reg[2][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][4] /CP | -
0.470 |   2.968 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    47 |       \|sa20_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[0] /CP    | -
0.464 |   2.953 |    2.489 | clk(D)(P) | clk(C)(P) * |
     |    48 |       \|sa13_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[4] /CP    | -
0.461 |   2.909 |    2.448 | clk(D)(P) | clk(C)(P) * |
```

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     |    49 |        \|sa01_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[5] /CP    | -
0.440 |   2.928 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |    50 |     \|u0|w_reg[2][5] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][5] /CP | -
0.440 |   2.938 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    51 |        \|sa20_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[4] /CP    | -
0.420 |   2.906 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |    52 |    \|u0|w_reg[3][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][20] /C | -
0.420 |   2.917 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |    53 |        \|sa31_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[5] /CP    | -
0.416 |   2.896 |    2.480 | clk(D)(P) | clk(C)(P) * |
     |    54 |     \|u0|w_reg[3][2] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][2] /CP | -
0.412 |   2.910 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |    55 |        \|sa31_reg[4] /D v | VIOLATED Setup Check with Pin \|sa31_reg[4] /CP    | -
0.411 |   2.866 |    2.456 | clk(D)(P) | clk(C)(P) * |
     |    56 |        \|sa20_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[3] /CP    | -
0.402 |   2.898 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |    57 |        \|sa11_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[6] /CP    | -
0.391 |   2.878 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |    58 |        \|sa21_reg[3] /D v | VIOLATED Setup Check with Pin \|sa21_reg[3] /CP    | -
0.391 |   2.859 |    2.468 | clk(D)(P) | clk(C)(P) * |
     |    59 |        \|sa11_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[3] /CP    | -
0.384 |   2.868 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |    60 |        \|sa23_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[4] /CP    | -
0.383 |   2.857 |    2.474 | clk(D)(P) | clk(C)(P) * |
     |    61 |    \|u0|w_reg[2][28] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][28] /C | -
0.383 |   2.880 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |    62 |        \|sa11_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[4] /CP    | -
0.375 |   2.861 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |    63 |     \|u0|w_reg[1][3] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][3] /CP | -
0.374 |   2.884 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |    64 |        \|sa11_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[1] /CP    | -
0.373 |   2.859 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |    65 |    \|u0|w_reg[1][21] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][21] /C | -
0.365 |   2.874 |    2.509 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |    66 |        \|sa00_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[1] /CP    | -
0.356 |   2.837 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |    67 |    \|u0|w_reg[3][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][15] /C | -
0.355 |   2.850 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |    68 |     \|u0|w_reg[0][7] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][7] /CP | -
0.354 |   2.863 |    2.509 | clk(D)(P) | clk(C)(P) * |
     |    69 |        \|sa20_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[7] /CP    | -
0.354 |   2.849 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |    70 |        \|sa11_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[0] /CP    | -
0.352 |   2.840 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |    71 |        \|sa30_reg[7] /D v | VIOLATED Setup Check with Pin \|sa30_reg[7] /CP    | -
0.352 |   2.807 |    2.455 | clk(D)(P) | clk(C)(P) * |
     |    72 |     \|u0|w_reg[2][2] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][2] /CP | -
0.349 |   2.842 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |    73 |        \|sa30_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[0] /CP    | -
0.343 |   2.794 |    2.452 | clk(D)(P) | clk(C)(P) * |
     |    74 |        \|sa01_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[1] /CP    | -
0.340 |   2.827 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |    75 |        \|sa00_reg[0] /D v | VIOLATED Setup Check with Pin \|sa00_reg[0] /CP    | -
0.339 |   2.816 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |    76 |        \|sa01_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[7] /CP    | -
0.339 |   2.823 |    2.484 | clk(D)(P) | clk(C)(P) * |
     |    77 |    \|u0|w_reg[2][23] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][23] /C | -
0.337 |   2.835 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
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     |    78 |     \|u0|w_reg[1][4] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][4] /CP | -
0.328 |   2.826 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    79 |       \|sa00_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[7] /CP    | -
0.323 |   2.812 |    2.489 | clk(D)(P) | clk(C)(P) * |
     |    80 |       \|sa33_reg[4] /D v | VIOLATED Setup Check with Pin \|sa33_reg[4] /CP    | -
0.322 |   2.782 |    2.460 | clk(D)(P) | clk(C)(P) * |
     |    81 |       \|sa21_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[0] /CP    | -
0.321 |   2.804 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |    82 |    \|u0|w_reg[2][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][20] /C | -
0.319 |   2.816 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |    83 |       \|sa10_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[7] /CP    | -
0.316 |   2.807 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |    84 |    \|u0|w_reg[1][27] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][27] /C | -
0.315 |   2.823 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |    85 |       \|sa30_reg[4] /D v | VIOLATED Setup Check with Pin \|sa30_reg[4] /CP    | -
0.310 |   2.767 |    2.457 | clk(D)(P) | clk(C)(P) * |
     |    86 |       \|sa01_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[6] /CP    | -
0.310 |   2.798 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |    87 |    \|u0|w_reg[1][29] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][29] /C | -
0.309 |   2.817 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |    88 |       \|sa11_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[7] /CP    | -
0.308 |   2.796 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |    89 |       \|sa23_reg[3] /D v | VIOLATED Setup Check with Pin \|sa23_reg[3] /CP    | -
0.304 |   2.762 |    2.457 | clk(D)(P) | clk(C)(P) * |
     |    90 |    \|u0|w_reg[0][30] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][30] /C | -
0.303 |   2.796 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |    91 |       \|sa30_reg[3] /D v | VIOLATED Setup Check with Pin \|sa30_reg[3] /CP    | -
0.299 |   2.759 |    2.460 | clk(D)(P) | clk(C)(P) * |
     |    92 |       \|sa33_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa33_reg[5] /CP    | -
0.296 |   2.786 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |    93 |     \|u0|w_reg[1][5] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][5] /CP | -
0.292 |   2.802 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |    94 |       \|sa21_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[2] /CP    | -
0.292 |   2.777 |    2.485 | clk(D)(P) | clk(C)(P) * |
     |    95 |     \|u0|w_reg[3][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][1] /CP | -
0.288 |   2.786 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |    96 |    \|u0|w_reg[0][26] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][26] /C | -
0.284 |   2.780 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |    97 |       \|sa20_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[2] /CP    | -
0.273 |   2.768 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |    98 |       \|sa30_reg[6] /D v | VIOLATED Setup Check with Pin \|sa30_reg[6] /CP    | -
0.270 |   2.737 |    2.467 | clk(D)(P) | clk(C)(P) * |
     |    99 |       \|sa10_reg[1] /D v | VIOLATED Setup Check with Pin \|sa10_reg[1] /CP    | -
0.268 |   2.736 |    2.468 | clk(D)(P) | clk(C)(P) * |
     |   100 |       \|sa23_reg[1] /D v | VIOLATED Setup Check with Pin \|sa23_reg[1] /CP    | -
0.265 |   2.720 |    2.455 | clk(D)(P) | clk(C)(P) * |
     |   101 |       \|sa31_reg[3] /D v | VIOLATED Setup Check with Pin \|sa31_reg[3] /CP    | -
0.263 |   2.735 |    2.473 | clk(D)(P) | clk(C)(P) * |
     |   102 |     \|u0|w_reg[3][9] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[3][9] /CP | -
0.250 |   2.756 |    2.507 | clk(D)(P) | clk(C)(P) * |
     |   103 |       \|sa00_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[4] /CP    | -
0.245 |   2.733 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   104 |       \|sa20_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[5] /CP    | -
0.242 |   2.734 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   105 |       \|sa20_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa20_reg[6] /CP    | -
0.241 |   2.739 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   106 |       \|sa32_reg[1] /D v | VIOLATED Setup Check with Pin \|sa32_reg[1] /CP    | -
0.239 |   2.702 |    2.463 | clk(D)(P) | clk(C)(P) * |
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     |   107 |    \|u0|w_reg[3][10] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][10] /C | -
0.237 |   2.735 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   108 |       \|sa31_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa31_reg[6] /CP    | -
0.236 |   2.723 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |   109 |       \|sa30_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[5] /CP    | -
0.236 |   2.717 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |   110 |       \|sa10_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[6] /CP    | -
0.235 |   2.726 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |   111 |       \|sa22_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[4] /CP    | -
0.229 |   2.710 |    2.480 | clk(D)(P) | clk(C)(P) * |
     |   112 |    \|u0|w_reg[3][22] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][22] /C | -
0.225 |   2.722 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   113 |    \|u0|w_reg[2][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][15] /C | -
0.222 |   2.719 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   114 |       \|sa30_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa30_reg[2] /CP    | -
0.221 |   2.714 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   115 |     \|u0|w_reg[3][8] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][8] /CP | -
0.219 |   2.717 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   116 |       \|sa32_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[4] /CP    | -
0.211 |   2.710 |    2.500 | clk(D)(P) | clk(C)(P) * |
     |   117 |       \|sa00_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[3] /CP    | -
0.207 |   2.698 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |   118 |    \|u0|w_reg[1][20] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][20] /C | -
0.207 |   2.704 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   119 |       \|sa03_reg[5] /D v | VIOLATED Setup Check with Pin \|sa03_reg[5] /CP    | -
0.204 |   2.664 |    2.460 | clk(D)(P) | clk(C)(P) * |
     |   120 |     \|u0|w_reg[2][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][1] /CP | -
0.201 |   2.698 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |   121 |    \|u0|w_reg[3][18] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][18] /C | -
0.197 |   2.693 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   122 |    \|u0|w_reg[1][28] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][28] /C | -
0.197 |   2.701 |    2.505 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   123 |       \|sa21_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[5] /CP    | -
0.196 |   2.682 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |   124 |       \|sa02_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[4] /CP    | -
0.189 |   2.674 |    2.485 | clk(D)(P) | clk(C)(P) * |
     |   125 |   \|text_out_reg[96] /D v | VIOLATED Setup Check with Pin \|text_out_reg[96] / | -
0.186 |   2.633 |    2.446 | clk(D)(P) | clk(C)(P) * |
     |       |                          | CP                                                 |
|         |         |          |           |
     |   126 |       \|sa03_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa03_reg[7] /CP    | -
0.178 |   2.667 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   127 |       \|sa32_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[7] /CP    | -
0.178 |   2.643 |    2.464 | clk(D)(P) | clk(C)(P) * |
     |   128 |    \|u0|w_reg[3][13] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][13] /C | -
0.173 |   2.669 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |
     |   129 |       \|sa22_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[3] /CP    | -
0.172 |   2.668 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |   130 |       \|sa00_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[6] /CP    | -
0.169 |   2.653 |    2.484 | clk(D)(P) | clk(C)(P) * |
     |   131 |       \|sa22_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[0] /CP    | -
0.167 |   2.649 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   132 |       \|sa22_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[1] /CP    | -
0.167 |   2.643 |    2.475 | clk(D)(P) | clk(C)(P) * |
```

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     |   133 |        \|sa13_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[7] /CP    | -
0.165 |   2.654 |    2.489 | clk(D)(P) | clk(C)(P) * |
     |   134 |    \|u0|w_reg[3][12] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][12] /C | -
0.163 |   2.659 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   135 |        \|sa31_reg[7] /D v | VIOLATED Setup Check with Pin \|sa31_reg[7] /CP    | -
0.156 |   2.628 |    2.472 | clk(D)(P) | clk(C)(P) * |
     |   136 |        \|sa01_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[3] /CP    | -
0.154 |   2.641 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   137 |        \|sa10_reg[2] /D v | VIOLATED Setup Check with Pin \|sa10_reg[2] /CP    | -
0.153 |   2.638 |    2.485 | clk(D)(P) | clk(C)(P) * |
     |   138 |        \|sa01_reg[4] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[4] /CP    | -
0.153 |   2.641 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   139 |    \|u0|w_reg[2][18] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][18] /C | -
0.151 |   2.648 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   140 |        \|sa23_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[0] /CP    | -
0.149 |   2.639 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |   141 |        \|sa21_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa21_reg[7] /CP    | -
0.148 |   2.626 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   142 |     \|u0|w_reg[1][2] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][2] /CP | -
0.140 |   2.650 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   143 |     \|u0|w_reg[2][8] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][8] /CP | -
0.140 |   2.639 |    2.499 | clk(D)(P) | clk(C)(P) * |
     |   144 |    \|u0|w_reg[2][10] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][10] /C | -
0.139 |   2.635 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   145 |    \|u0|w_reg[0][24] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][24] /C | -
0.135 |   2.633 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   146 |        \|sa03_reg[6] /D v | VIOLATED Setup Check with Pin \|sa03_reg[6] /CP    | -
0.134 |   2.595 |    2.461 | clk(D)(P) | clk(C)(P) * |
     |   147 |        \|sa10_reg[3] /D v | VIOLATED Setup Check with Pin \|sa10_reg[3] /CP    | -
0.128 |   2.617 |    2.489 | clk(D)(P) | clk(C)(P) * |
     |   148 |        \|sa13_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[1] /CP    | -
0.126 |   2.602 |    2.476 | clk(D)(P) | clk(C)(P) * |
     |   149 |    \|u0|w_reg[1][23] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[1][23] /C | -
0.122 |   2.631 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   150 |        \|sa13_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[5] /CP    | -
0.120 |   2.585 |    2.465 | clk(D)(P) | clk(C)(P) * |
     |   151 |        \|sa12_reg[1] /D v | VIOLATED Setup Check with Pin \|sa12_reg[1] /CP    | -
0.119 |   2.605 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |   152 |        \|sa00_reg[5] /D v | VIOLATED Setup Check with Pin \|sa00_reg[5] /CP    | -
0.117 |   2.594 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   153 |    \|u0|w_reg[2][22] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][22] /C | -
0.112 |   2.610 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   154 |        \|sa22_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa22_reg[7] /CP    | -
0.109 |   2.594 |    2.485 | clk(D)(P) | clk(C)(P) * |
     |   155 |        \|sa02_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[7] /CP    | -
0.106 |   2.595 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   156 |     \|u0|w_reg[0][4] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][4] /CP | -
0.104 |   2.613 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   157 |    \|u0|w_reg[3][14] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][14] /C | -
0.103 |   2.599 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
     |   158 |    \|u0|w_reg[0][21] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][21] /C | -
0.100 |   2.606 |    2.506 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |          |           |           |
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     |   159 |        \|sa32_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[0] /CP    | -
0.099 |   2.594 |    2.494 | clk(D)(P) | clk(C)(P) * |
     |   160 |     \|u0|w_reg[1][1] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][1] /CP | -
0.096 |   2.590 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   161 |        \|sa12_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa12_reg[7] /CP    | -
0.093 |   2.587 |    2.494 | clk(D)(P) | clk(C)(P) * |
     |   162 |     \|u0|w_reg[0][3] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][3] /CP | -
0.092 |   2.602 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   163 |    \|u0|w_reg[0][31] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][31] /C | -
0.092 |   2.590 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |   164 |        \|sa01_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[2] /CP    | -
0.090 |   2.570 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |   165 |  \|text_out_reg[126] /D ^ | VIOLATED Setup Check with Pin \|text_out_reg[126]  | -
0.087 |   2.531 |    2.443 | clk(D)(P) | clk(C)(P) * |
     |       |                          | /CP                                                |
|         |         |          |           |          |
     |   166 |    \|u0|w_reg[2][14] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][14] /C | -
0.086 |   2.584 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |   167 |        \|sa02_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[3] /CP    | -
0.085 |   2.571 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |   168 |        \|sa23_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[5] /CP    | -
0.084 |   2.551 |    2.467 | clk(D)(P) | clk(C)(P) * |
     |   169 |        \|sa00_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa00_reg[2] /CP    | -
0.083 |   2.574 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |   170 |        \|sa11_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa11_reg[5] /CP    | -
0.077 |   2.565 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   171 |    \|u0|w_reg[3][19] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][19] /C | -
0.076 |   2.574 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |   172 |        \|sa02_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[0] /CP    | -
0.073 |   2.568 |    2.494 | clk(D)(P) | clk(C)(P) * |
     |   173 |        \|sa32_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[5] /CP    | -
0.071 |   2.525 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   174 |        \|sa02_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa02_reg[1] /CP    | -
0.071 |   2.566 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |   175 |    \|u0|w_reg[1][15] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[1][15] /C | -
0.070 |   2.568 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |   176 |        \|sa32_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa32_reg[3] /CP    | -
0.067 |   2.559 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   177 |        \|sa03_reg[1] /D ^ | VIOLATED Setup Check with Pin \|sa03_reg[1] /CP    | -
0.066 |   2.556 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |   178 |        \|sa23_reg[6] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[6] /CP    | -
0.063 |   2.558 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |   179 |        \|sa01_reg[0] /D ^ | VIOLATED Setup Check with Pin \|sa01_reg[0] /CP    | -
0.060 |   2.545 |    2.485 | clk(D)(P) | clk(C)(P) * |
     |   180 |        \|sa33_reg[3] /D v | VIOLATED Setup Check with Pin \|sa33_reg[3] /CP    | -
0.058 |   2.513 |    2.456 | clk(D)(P) | clk(C)(P) * |
     |   181 |        \|sa23_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[2] /CP    | -
0.056 |   2.539 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |   182 |     \|u0|w_reg[2][9] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][9] /CP | -
0.053 |   2.552 |    2.499 | clk(D)(P) | clk(C)(P) * |
     |   183 |        \|sa23_reg[7] /D ^ | VIOLATED Setup Check with Pin \|sa23_reg[7] /CP    | -
0.053 |   2.548 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |   184 |    \|u0|w_reg[2][19] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][19] /C | -
0.052 |   2.549 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                          | P                                                  |
|         |         |          |           |          |
     |   185 |        \|sa13_reg[6] /D v | VIOLATED Setup Check with Pin \|sa13_reg[6] /CP    | -
0.050 |   2.528 |    2.479 | clk(D)(P) | clk(C)(P) * |
     |   186 |    \|u0|w_reg[2][13] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][13] /C | -
0.048 |   2.546 |    2.498 | clk(D)(P) | clk(C)(P) * |
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     |       |                              | P                                                                                  |
|         |          |             |              |
     |   187 |        \|sa13_reg[3] /D v | VIOLATED Setup Check with Pin \|sa13_reg[3] /CP    | -
0.045 |   2.522 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   188 |   \|text_out_reg[85] /D v | VIOLATED Setup Check with Pin \|text_out_reg[85] / | -
0.044 |   2.491 |    2.447 | clk(D)(P) | clk(C)(P) * |
     |       |                              | CP                                                                                 |
|         |          |             |              |
     |   189 |   \|text_out_reg[28] /D v | VIOLATED Setup Check with Pin \|text_out_reg[28] / | -
0.044 |   2.495 |    2.452 | clk(D)(P) | clk(C)(P) * |
     |       |                              | CP                                                                                 |
|         |          |             |              |
     |   190 |    \|u0|w_reg[0][25] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[0][25] /C | -
0.042 |   2.541 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                              | P                                                                                  |
|         |          |             |              |
     |   191 |     \|u0|w_reg[0][5] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][5] /CP | -
0.042 |   2.552 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   192 |    \|u0|w_reg[2][12] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[2][12] /C | -
0.041 |   2.539 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |       |                              | P                                                                                  |
|         |          |             |              |
     |   193 |        \|sa03_reg[3] /D ^ | VIOLATED Setup Check with Pin \|sa03_reg[3] /CP    | -
0.039 |   2.517 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   194 |    \|u0|w_reg[3][17] /D v | VIOLATED Setup Check with Pin \|u0|w_reg[3][17] /C | -
0.035 |   2.532 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |       |                              | P                                                                                  |
|         |          |             |              |
     |   195 |        \|sa33_reg[1] /D v | VIOLATED Setup Check with Pin \|sa33_reg[1] /CP    | -
0.034 |   2.497 |    2.463 | clk(D)(P) | clk(C)(P) * |
     |   196 |        \|sa33_reg[0] /D v | VIOLATED Setup Check with Pin \|sa33_reg[0] /CP    | -
0.031 |   2.490 |    2.459 | clk(D)(P) | clk(C)(P) * |
     |   197 |        \|sa10_reg[5] /D ^ | VIOLATED Setup Check with Pin \|sa10_reg[5] /CP    | -
0.023 |   2.522 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   198 |   \|text_out_reg[78] /D v | VIOLATED Setup Check with Pin \|text_out_reg[78] / | -
0.012 |   2.437 |    2.425 | clk(D)(P) | clk(C)(P) * |
     |       |                              | CP                                                                                 |
|         |          |             |              |
     |   199 |  \|text_out_reg[103] /D v | VIOLATED Setup Check with Pin \|text_out_reg[103]  | -
0.012 |   2.477 |    2.465 | clk(D)(P) | clk(C)(P) * |
     |       |                              | /CP                                                                                |
|         |          |             |              |
     |   200 |  \|text_out_reg[122] /D ^ | VIOLATED Setup Check with Pin \|text_out_reg[122]  | -
0.009 |   2.432 |    2.423 | clk(D)(P) | clk(C)(P) * |
     |       |                              | /CP                                                                                |
|         |          |             |              |
     |   201 |        \|sa13_reg[2] /D ^ | VIOLATED Setup Check with Pin \|sa13_reg[2] /CP    | -
0.005 |   2.465 |    2.460 | clk(D)(P) | clk(C)(P) * |
     |   202 |  \|text_out_reg[100] /D ^ | VIOLATED Setup Check with Pin \|text_out_reg[100]  | -
0.003 |   2.469 |    2.466 | clk(D)(P) | clk(C)(P) * |
     |       |                              | /CP                                                                                |
|         |          |             |              |
     |   203 |   \|text_out_reg[97] /D v | VIOLATED Setup Check with Pin \|text_out_reg[97] / | -
0.001 |   2.465 |    2.464 | clk(D)(P) | clk(C)(P) * |
     |       |                              | CP                                                                                 |
|         |          |             |              |
     |   204 |    \|u0|w_reg[0][20] /D ^ | VIOLATED Setup Check with Pin \|u0|w_reg[0][20] /C |
0.000 |   2.504 |    2.504 | clk(D)(P) | clk(C)(P) * |
     |       |                              | P                                                                                  |
|         |          |             |              |
     |   205 |        \|sa33_reg[6] /D ^ | MET Setup Check with Pin \|sa33_reg[6] /CP         |
0.002 |   2.488 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |   206 |     \|u0|w_reg[1][8] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][8] /CP       |
0.006 |   2.502 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |   207 |   \|text_out_reg[79] /D v | MET Setup Check with Pin \|text_out_reg[79] /CP    |
0.008 |   2.441 |    2.449 | clk(D)(P) | clk(C)(P) * |
     |   208 |        \|sa03_reg[2] /D ^ | MET Setup Check with Pin \|sa03_reg[2] /CP         |
0.008 |   2.475 |    2.483 | clk(D)(P) | clk(C)(P) * |
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     |   209 |   \|text_out_reg[75] /D ^ | MET Setup Check with Pin \|text_out_reg[75] /CP    |
0.009 |   2.382 |    2.391 | clk(D)(P) | clk(C)(P) * |
     |   210 |       \|sa02_reg[6] /D v | MET Setup Check with Pin \|sa02_reg[6] /CP         |
0.009 |   2.459 |    2.468 | clk(D)(P) | clk(C)(P) * |
     |   211 |       \|sa33_reg[2] /D ^ | MET Setup Check with Pin \|sa33_reg[2] /CP         |
0.014 |   2.467 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |   212 |       \|sa31_reg[2] /D ^ | MET Setup Check with Pin \|sa31_reg[2] /CP         |
0.015 |   2.459 |    2.474 | clk(D)(P) | clk(C)(P) * |
     |   213 |    \|u0|w_reg[0][27] /D v | MET Setup Check with Pin \|u0|w_reg[0][27] /CP     |
0.017 |   2.482 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   214 |       \|sa02_reg[5] /D ^ | MET Setup Check with Pin \|sa02_reg[5] /CP         |
0.021 |   2.460 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |   215 |    \|u0|w_reg[0][29] /D v | MET Setup Check with Pin \|u0|w_reg[0][29] /CP     |
0.024 |   2.462 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |   216 |       \|sa11_reg[2] /D ^ | MET Setup Check with Pin \|sa11_reg[2] /CP         |
0.026 |   2.459 |    2.486 | clk(D)(P) | clk(C)(P) * |
     |   217 |       \|sa12_reg[4] /D v | MET Setup Check with Pin \|sa12_reg[4] /CP         |
0.030 |   2.456 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |   218 |       \|sa21_reg[6] /D ^ | MET Setup Check with Pin \|sa21_reg[6] /CP         |
0.036 |   2.452 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   219 |    \|u0|w_reg[0][28] /D v | MET Setup Check with Pin \|u0|w_reg[0][28] /CP     |
0.037 |   2.461 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   220 |    \|u0|w_reg[1][10] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][10] /CP     |
0.038 |   2.470 |    2.509 | clk(D)(P) | clk(C)(P) * |
     |   221 |       \|sa32_reg[2] /D ^ | MET Setup Check with Pin \|sa32_reg[2] /CP         |
0.043 |   2.439 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   222 |       \|sa12_reg[6] /D ^ | MET Setup Check with Pin \|sa12_reg[6] /CP         |
0.046 |   2.436 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   223 |    \|u0|w_reg[1][22] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][22] /CP     |
0.046 |   2.464 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   224 |       \|sa03_reg[4] /D ^ | MET Setup Check with Pin \|sa03_reg[4] /CP         |
0.048 |   2.447 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |   225 |    \|u0|w_reg[2][17] /D v | MET Setup Check with Pin \|u0|w_reg[2][17] /CP     |
0.049 |   2.450 |    2.499 | clk(D)(P) | clk(C)(P) * |
     |   226 |    \|u0|w_reg[1][18] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][18] /CP     |
0.054 |   2.457 |    2.511 | clk(D)(P) | clk(C)(P) * |
     |   227 |   \|text_out_reg[99] /D v | MET Setup Check with Pin \|text_out_reg[99] /CP    |
0.059 |   2.402 |    2.460 | clk(D)(P) | clk(C)(P) * |
     |   228 |     \|u0|w_reg[0][2] /D v | MET Setup Check with Pin \|u0|w_reg[0][2] /CP      |
0.061 |   2.435 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |   229 |     \|u0|w_reg[1][9] /D v | MET Setup Check with Pin \|u0|w_reg[1][9] /CP      |
0.066 |   2.432 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   230 |       \|sa33_reg[7] /D ^ | MET Setup Check with Pin \|sa33_reg[7] /CP         |
0.067 |   2.424 |    2.490 | clk(D)(P) | clk(C)(P) * |
     |   231 |    \|u0|w_reg[3][11] /D v | MET Setup Check with Pin \|u0|w_reg[3][11] /CP     |
0.076 |   2.422 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   232 |       \|sa32_reg[6] /D ^ | MET Setup Check with Pin \|sa32_reg[6] /CP         |
0.077 |   2.379 |    2.457 | clk(D)(P) | clk(C)(P) * |
     |   233 |    \|u0|w_reg[3][16] /D v | MET Setup Check with Pin \|u0|w_reg[3][16] /CP     |
0.082 |   2.416 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |   234 |    \|u0|w_reg[0][15] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][15] /CP     |
0.094 |   2.407 |    2.502 | clk(D)(P) | clk(C)(P) * |
     |   235 |    \|u0|w_reg[2][11] /D ^ | MET Setup Check with Pin \|u0|w_reg[2][11] /CP     |
0.097 |   2.411 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |   236 |    \|u0|w_reg[1][12] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][12] /CP     |
0.101 |   2.408 |    2.509 | clk(D)(P) | clk(C)(P) * |
     |   237 |       \|sa12_reg[3] /D ^ | MET Setup Check with Pin \|sa12_reg[3] /CP         |
0.102 |   2.390 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   238 |       \|sa03_reg[0] /D ^ | MET Setup Check with Pin \|sa03_reg[0] /CP         |
0.103 |   2.388 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |   239 |       \|sa02_reg[2] /D ^ | MET Setup Check with Pin \|sa02_reg[2] /CP         |
0.103 |   2.385 |    2.488 | clk(D)(P) | clk(C)(P) * |
     |   240 |       \|sa31_reg[0] /D v | MET Setup Check with Pin \|sa31_reg[0] /CP         |
0.115 |   2.351 |    2.466 | clk(D)(P) | clk(C)(P) * |
     |   241 |    \|u0|w_reg[1][14] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][14] /CP     |
0.115 |   2.395 |    2.510 | clk(D)(P) | clk(C)(P) * |
     |   242 |     \|u0|w_reg[0][1] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][1] /CP      |
0.116 |   2.393 |    2.509 | clk(D)(P) | clk(C)(P) * |
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| 243 | \|u0|w_reg[1][13] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][13] /CP |
0.125 | 2.385 | 2.510 | clk(D)(P) | clk(C)(P) * |
| 244 | \|text_out_reg[76] /D v | MET Setup Check with Pin \|text_out_reg[76] /CP |
0.128 | 2.300 | 2.428 | clk(D)(P) | clk(C)(P) * |
| 245 | \|sa22_reg[6] /D ^ | MET Setup Check with Pin \|sa22_reg[6] /CP |
0.130 | 2.349 | 2.479 | clk(D)(P) | clk(C)(P) * |
| 246 | \|text_out_reg[101] /D ^ | MET Setup Check with Pin \|text_out_reg[101] /CP |
0.134 | 2.327 | 2.461 | clk(D)(P) | clk(C)(P) * |
| 247 | \|text_out_reg[29] /D ^ | MET Setup Check with Pin \|text_out_reg[29] /CP |
0.144 | 2.299 | 2.443 | clk(D)(P) | clk(C)(P) * |
| 248 | \|u0|w_reg[1][17] /D v | MET Setup Check with Pin \|u0|w_reg[1][17] /CP |
0.154 | 2.344 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 249 | \|u0|w_reg[2][16] /D v | MET Setup Check with Pin \|u0|w_reg[2][16] /CP |
0.157 | 2.341 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 250 | \|text_out_reg[7] /D ^ | MET Setup Check with Pin \|text_out_reg[7] /CP |
0.158 | 2.291 | 2.449 | clk(D)(P) | clk(C)(P) * |
| 251 | \|text_out_reg[102] /D v | MET Setup Check with Pin \|text_out_reg[102] /CP |
0.163 | 2.317 | 2.480 | clk(D)(P) | clk(C)(P) * |
| 252 | \|text_out_reg[65] /D ^ | MET Setup Check with Pin \|text_out_reg[65] /CP |
0.186 | 2.252 | 2.438 | clk(D)(P) | clk(C)(P) * |
| 253 | \|sa12_reg[2] /D ^ | MET Setup Check with Pin \|sa12_reg[2] /CP |
0.187 | 2.309 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 254 | \|sa22_reg[5] /D ^ | MET Setup Check with Pin \|sa22_reg[5] /CP |
0.194 | 2.302 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 255 | \|text_out_reg[125] /D ^ | MET Setup Check with Pin \|text_out_reg[125] /CP |
0.199 | 2.249 | 2.448 | clk(D)(P) | clk(C)(P) * |
| 256 | \|u0|w_reg[1][19] /D ^ | MET Setup Check with Pin \|u0|w_reg[1][19] /CP |
0.200 | 2.309 | 2.508 | clk(D)(P) | clk(C)(P) * |
| 257 | \|sa13_reg[0] /D ^ | MET Setup Check with Pin \|sa13_reg[0] /CP |
0.201 | 2.294 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 258 | \|u0|w_reg[0][9] /D v | MET Setup Check with Pin \|u0|w_reg[0][9] /CP |
0.215 | 2.283 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 259 | \|text_out_reg[87] /D v | MET Setup Check with Pin \|text_out_reg[87] /CP |
0.219 | 2.231 | 2.450 | clk(D)(P) | clk(C)(P) * |
| 260 | \|text_out_reg[121] /D ^ | MET Setup Check with Pin \|text_out_reg[121] /CP |
0.219 | 2.233 | 2.452 | clk(D)(P) | clk(C)(P) * |
| 261 | \|text_out_reg[81] /D v | MET Setup Check with Pin \|text_out_reg[81] /CP |
0.223 | 2.231 | 2.454 | clk(D)(P) | clk(C)(P) * |
| 262 | \|text_out_reg[1] /D v | MET Setup Check with Pin \|text_out_reg[1] /CP |
0.224 | 2.244 | 2.468 | clk(D)(P) | clk(C)(P) * |
| 263 | \|text_out_reg[60] /D v | MET Setup Check with Pin \|text_out_reg[60] /CP |
0.234 | 2.194 | 2.428 | clk(D)(P) | clk(C)(P) * |
| 264 | \|text_out_reg[39] /D v | MET Setup Check with Pin \|text_out_reg[39] /CP |
0.240 | 2.236 | 2.476 | clk(D)(P) | clk(C)(P) * |
| 265 | \|text_out_reg[63] /D v | MET Setup Check with Pin \|text_out_reg[63] /CP |
0.243 | 2.202 | 2.446 | clk(D)(P) | clk(C)(P) * |
| 266 | \|text_out_reg[5] /D v | MET Setup Check with Pin \|text_out_reg[5] /CP |
0.247 | 2.214 | 2.461 | clk(D)(P) | clk(C)(P) * |
| 267 | \|text_out_reg[57] /D ^ | MET Setup Check with Pin \|text_out_reg[57] /CP |
0.247 | 2.206 | 2.453 | clk(D)(P) | clk(C)(P) * |
| 268 | \|u0|w_reg[0][23] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][23] /CP |
0.248 | 2.262 | 2.511 | clk(D)(P) | clk(C)(P) * |
| 269 | \|sa12_reg[5] /D ^ | MET Setup Check with Pin \|sa12_reg[5] /CP |
0.250 | 2.246 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 270 | \|sa12_reg[0] /D ^ | MET Setup Check with Pin \|sa12_reg[0] /CP |
0.252 | 2.237 | 2.489 | clk(D)(P) | clk(C)(P) * |
| 271 | \|sa22_reg[2] /D ^ | MET Setup Check with Pin \|sa22_reg[2] /CP |
0.254 | 2.232 | 2.487 | clk(D)(P) | clk(C)(P) * |
| 272 | \|text_out_reg[112] /D v | MET Setup Check with Pin \|text_out_reg[112] /CP |
0.261 | 2.197 | 2.458 | clk(D)(P) | clk(C)(P) * |
| 273 | \|u0|w_reg[0][8] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][8] /CP |
0.264 | 2.241 | 2.505 | clk(D)(P) | clk(C)(P) * |
| 274 | \|text_out_reg[86] /D v | MET Setup Check with Pin \|text_out_reg[86] /CP |
0.281 | 2.172 | 2.453 | clk(D)(P) | clk(C)(P) * |
| 275 | \|text_out_reg[6] /D v | MET Setup Check with Pin \|text_out_reg[6] /CP |
0.281 | 2.181 | 2.463 | clk(D)(P) | clk(C)(P) * |
| 276 | \|text_out_reg[117] /D v | MET Setup Check with Pin \|text_out_reg[117] /CP |
0.282 | 2.186 | 2.467 | clk(D)(P) | clk(C)(P) * |

| 277 | \|u0|w_reg[0][10] /D v | MET Setup Check with Pin \|u0|w_reg[0][10] /CP |
0.285 | 2.213 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 278 | \|text_out_reg[124] /D v | MET Setup Check with Pin \|text_out_reg[124] /CP |
0.287 | 2.186 | 2.472 | clk(D)(P) | clk(C)(P) * |
| 279 | \|text_out_reg[116] /D ^ | MET Setup Check with Pin \|text_out_reg[116] /CP |
0.288 | 2.169 | 2.458 | clk(D)(P) | clk(C)(P) * |
| 280 | \|text_out_reg[92] /D v | MET Setup Check with Pin \|text_out_reg[92] /CP |
0.291 | 2.190 | 2.481 | clk(D)(P) | clk(C)(P) * |
| 281 | \|text_out_reg[66] /D v | MET Setup Check with Pin \|text_out_reg[66] /CP |
0.294 | 2.182 | 2.476 | clk(D)(P) | clk(C)(P) * |
| 282 | \|u0|w_reg[0][18] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][18] /CP |
0.301 | 2.191 | 2.492 | clk(D)(P) | clk(C)(P) * |
| 283 | \|text_out_reg[74] /D v | MET Setup Check with Pin \|text_out_reg[74] /CP |
0.304 | 2.140 | 2.444 | clk(D)(P) | clk(C)(P) * |
| 284 | \|u0|w_reg[1][16] /D v | MET Setup Check with Pin \|u0|w_reg[1][16] /CP |
0.306 | 2.192 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 285 | \|text_out_reg[113] /D v | MET Setup Check with Pin \|text_out_reg[113] /CP |
0.307 | 2.170 | 2.477 | clk(D)(P) | clk(C)(P) * |
| 286 | \|text_out_reg[2] /D v | MET Setup Check with Pin \|text_out_reg[2] /CP |
0.312 | 2.150 | 2.463 | clk(D)(P) | clk(C)(P) * |
| 287 | \|text_out_reg[104] /D v | MET Setup Check with Pin \|text_out_reg[104] /CP |
0.315 | 2.151 | 2.465 | clk(D)(P) | clk(C)(P) * |
| 288 | \|u0|w_reg[0][14] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][14] /CP |
0.320 | 2.189 | 2.510 | clk(D)(P) | clk(C)(P) * |
| 289 | \|text_out_reg[89] /D v | MET Setup Check with Pin \|text_out_reg[89] /CP |
0.321 | 2.152 | 2.474 | clk(D)(P) | clk(C)(P) * |
| 290 | \|text_out_reg[115] /D v | MET Setup Check with Pin \|text_out_reg[115] /CP |
0.325 | 2.144 | 2.469 | clk(D)(P) | clk(C)(P) * |
| 291 | \|text_out_reg[53] /D v | MET Setup Check with Pin \|text_out_reg[53] /CP |
0.325 | 2.157 | 2.481 | clk(D)(P) | clk(C)(P) * |
| 292 | \|text_out_reg[88] /D v | MET Setup Check with Pin \|text_out_reg[88] /CP |
0.325 | 2.151 | 2.476 | clk(D)(P) | clk(C)(P) * |
| 293 | \|u0|w_reg[0][17] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][17] /CP |
0.331 | 2.177 | 2.508 | clk(D)(P) | clk(C)(P) * |
| 294 | \|u0|w_reg[1][11] /D v | MET Setup Check with Pin \|u0|w_reg[1][11] /CP |
0.335 | 2.163 | 2.498 | clk(D)(P) | clk(C)(P) * |
| 295 | \|text_out_reg[64] /D v | MET Setup Check with Pin \|text_out_reg[64] /CP |
0.341 | 2.110 | 2.451 | clk(D)(P) | clk(C)(P) * |
| 296 | \|text_out_reg[67] /D v | MET Setup Check with Pin \|text_out_reg[67] /CP |
0.345 | 2.115 | 2.460 | clk(D)(P) | clk(C)(P) * |
| 297 | \|u0|w_reg[0][12] /D v | MET Setup Check with Pin \|u0|w_reg[0][12] /CP |
0.346 | 2.150 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 298 | \|u0|w_reg[0][13] /D v | MET Setup Check with Pin \|u0|w_reg[0][13] /CP |
0.348 | 2.148 | 2.496 | clk(D)(P) | clk(C)(P) * |
| 299 | \|text_out_reg[118] /D v | MET Setup Check with Pin \|text_out_reg[118] /CP |
0.352 | 2.117 | 2.470 | clk(D)(P) | clk(C)(P) * |
| 300 | \|text_out_reg[95] /D v | MET Setup Check with Pin \|text_out_reg[95] /CP |
0.358 | 2.117 | 2.475 | clk(D)(P) | clk(C)(P) * |
| 301 | \|text_out_reg[68] /D ^ | MET Setup Check with Pin \|text_out_reg[68] /CP |
0.361 | 2.081 | 2.442 | clk(D)(P) | clk(C)(P) * |
| 302 | \|text_out_reg[72] /D ^ | MET Setup Check with Pin \|text_out_reg[72] /CP |
0.365 | 2.073 | 2.438 | clk(D)(P) | clk(C)(P) * |
| 303 | \|text_out_reg[94] /D v | MET Setup Check with Pin \|text_out_reg[94] /CP |
0.365 | 2.117 | 2.482 | clk(D)(P) | clk(C)(P) * |
| 304 | \|text_out_reg[47] /D ^ | MET Setup Check with Pin \|text_out_reg[47] /CP |
0.371 | 2.065 | 2.436 | clk(D)(P) | clk(C)(P) * |
| 305 | \|text_out_reg[16] /D v | MET Setup Check with Pin \|text_out_reg[16] /CP |
0.374 | 2.080 | 2.454 | clk(D)(P) | clk(C)(P) * |
| 306 | \|text_out_reg[35] /D v | MET Setup Check with Pin \|text_out_reg[35] /CP |
0.380 | 2.084 | 2.464 | clk(D)(P) | clk(C)(P) * |
| 307 | \|text_out_reg[30] /D v | MET Setup Check with Pin \|text_out_reg[30] /CP |
0.384 | 2.094 | 2.478 | clk(D)(P) | clk(C)(P) * |
| 308 | \|text_out_reg[83] /D ^ | MET Setup Check with Pin \|text_out_reg[83] /CP |
0.386 | 2.042 | 2.429 | clk(D)(P) | clk(C)(P) * |
| 309 | \|text_out_reg[109] /D ^ | MET Setup Check with Pin \|text_out_reg[109] /CP |
0.390 | 2.055 | 2.445 | clk(D)(P) | clk(C)(P) * |
| 310 | \|u0|w_reg[0][22] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][22] /CP |
0.390 | 2.114 | 2.504 | clk(D)(P) | clk(C)(P) * |

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      |   311 |  \|text_out_reg[123] /D v | MET Setup Check with Pin \|text_out_reg[123] /CP   |
0.391 |   2.055 |    2.446 | clk(D)(P) | clk(C)(P) * |
      |   312 |   \|text_out_reg[82] /D v | MET Setup Check with Pin \|text_out_reg[82] /CP    |
0.396 |   2.052 |    2.448 | clk(D)(P) | clk(C)(P) * |
      |   313 |   \|text_out_reg[93] /D v | MET Setup Check with Pin \|text_out_reg[93] /CP    |
0.397 |   2.095 |    2.493 | clk(D)(P) | clk(C)(P) * |
      |   314 |   \|text_out_reg[98] /D ^ | MET Setup Check with Pin \|text_out_reg[98] /CP    |
0.398 |   2.064 |    2.462 | clk(D)(P) | clk(C)(P) * |
      |   315 |   \|text_out_reg[55] /D ^ | MET Setup Check with Pin \|text_out_reg[55] /CP    |
0.398 |   2.050 |    2.448 | clk(D)(P) | clk(C)(P) * |
      |   316 |   \|text_out_reg[24] /D v | MET Setup Check with Pin \|text_out_reg[24] /CP    |
0.399 |   2.050 |    2.448 | clk(D)(P) | clk(C)(P) * |
      |   317 |   \|text_out_reg[27] /D ^ | MET Setup Check with Pin \|text_out_reg[27] /CP    |
0.400 |   2.032 |    2.432 | clk(D)(P) | clk(C)(P) * |
      |   318 |   \|text_out_reg[91] /D v | MET Setup Check with Pin \|text_out_reg[91] /CP    |
0.408 |   2.064 |    2.471 | clk(D)(P) | clk(C)(P) * |
      |   319 |   \|text_out_reg[49] /D v | MET Setup Check with Pin \|text_out_reg[49] /CP    |
0.408 |   2.073 |    2.481 | clk(D)(P) | clk(C)(P) * |
      |   320 |   \|text_out_reg[59] /D v | MET Setup Check with Pin \|text_out_reg[59] /CP    |
0.412 |   2.061 |    2.473 | clk(D)(P) | clk(C)(P) * |
      |   321 |   \|text_out_reg[62] /D ^ | MET Setup Check with Pin \|text_out_reg[62] /CP    |
0.413 |   2.058 |    2.472 | clk(D)(P) | clk(C)(P) * |
      |   322 |   \|text_out_reg[58] /D ^ | MET Setup Check with Pin \|text_out_reg[58] /CP    |
0.420 |   2.030 |    2.450 | clk(D)(P) | clk(C)(P) * |
      |   323 |    \|u0|w_reg[0][11] /D v | MET Setup Check with Pin \|u0|w_reg[0][11] /CP     |
0.424 |   2.067 |    2.492 | clk(D)(P) | clk(C)(P) * |
      |   324 |  \|text_out_reg[110] /D ^ | MET Setup Check with Pin \|text_out_reg[110] /CP   |
0.426 |   2.023 |    2.449 | clk(D)(P) | clk(C)(P) * |
      |   325 |   \|text_out_reg[40] /D ^ | MET Setup Check with Pin \|text_out_reg[40] /CP    |
0.429 |   2.029 |    2.458 | clk(D)(P) | clk(C)(P) * |
      |   326 |   \|text_out_reg[56] /D ^ | MET Setup Check with Pin \|text_out_reg[56] /CP    |
0.433 |   2.025 |    2.458 | clk(D)(P) | clk(C)(P) * |
      |   327 |   \|text_out_reg[61] /D v | MET Setup Check with Pin \|text_out_reg[61] /CP    |
0.455 |   2.015 |    2.470 | clk(D)(P) | clk(C)(P) * |
      |   328 |   \|text_out_reg[37] /D v | MET Setup Check with Pin \|text_out_reg[37] /CP    |
0.456 |   2.013 |    2.469 | clk(D)(P) | clk(C)(P) * |
      |   329 |   \|text_out_reg[36] /D v | MET Setup Check with Pin \|text_out_reg[36] /CP    |
0.460 |   2.019 |    2.479 | clk(D)(P) | clk(C)(P) * |
      |   330 |   \|text_out_reg[21] /D v | MET Setup Check with Pin \|text_out_reg[21] /CP    |
0.461 |   2.015 |    2.476 | clk(D)(P) | clk(C)(P) * |
      |   331 |  \|text_out_reg[120] /D ^ | MET Setup Check with Pin \|text_out_reg[120] /CP   |
0.465 |   1.996 |    2.460 | clk(D)(P) | clk(C)(P) * |
      |   332 |    \|text_out_reg[4] /D v | MET Setup Check with Pin \|text_out_reg[4] /CP     |
0.465 |   2.010 |    2.474 | clk(D)(P) | clk(C)(P) * |
      |   333 |   \|text_out_reg[15] /D ^ | MET Setup Check with Pin \|text_out_reg[15] /CP    |
0.468 |   1.976 |    2.444 | clk(D)(P) | clk(C)(P) * |
      |   334 |  \|text_out_reg[119] /D v | MET Setup Check with Pin \|text_out_reg[119] /CP   |
0.472 |   2.018 |    2.489 | clk(D)(P) | clk(C)(P) * |
      |   335 |  \|text_out_reg[111] /D ^ | MET Setup Check with Pin \|text_out_reg[111] /CP   |
0.479 |   1.982 |    2.461 | clk(D)(P) | clk(C)(P) * |
      |   336 |   \|text_out_reg[52] /D v | MET Setup Check with Pin \|text_out_reg[52] /CP    |
0.482 |   1.988 |    2.470 | clk(D)(P) | clk(C)(P) * |
      |   337 |  \|text_out_reg[106] /D v | MET Setup Check with Pin \|text_out_reg[106] /CP   |
0.488 |   1.989 |    2.477 | clk(D)(P) | clk(C)(P) * |
      |   338 |   \|text_out_reg[31] /D v | MET Setup Check with Pin \|text_out_reg[31] /CP    |
0.491 |   1.965 |    2.456 | clk(D)(P) | clk(C)(P) * |
      |   339 |   \|text_out_reg[45] /D v | MET Setup Check with Pin \|text_out_reg[45] /CP    |
0.497 |   1.966 |    2.463 | clk(D)(P) | clk(C)(P) * |
      |   340 |    \|u0|w_reg[0][16] /D ^ | MET Setup Check with Pin \|u0|w_reg[0][16] /CP     |
0.498 |   2.011 |    2.509 | clk(D)(P) | clk(C)(P) * |
      |   341 |    \|text_out_reg[3] /D v | MET Setup Check with Pin \|text_out_reg[3] /CP     |
0.506 |   1.966 |    2.472 | clk(D)(P) | clk(C)(P) * |
      |   342 |   \|text_out_reg[20] /D v | MET Setup Check with Pin \|text_out_reg[20] /CP    |
0.508 |   1.954 |    2.462 | clk(D)(P) | clk(C)(P) * |
      |   343 |   \|text_out_reg[25] /D v | MET Setup Check with Pin \|text_out_reg[25] /CP    |
0.510 |   1.979 |    2.488 | clk(D)(P) | clk(C)(P) * |
      |   344 |    \|text_out_reg[8] /D ^ | MET Setup Check with Pin \|text_out_reg[8] /CP     |
0.511 |   1.942 |    2.453 | clk(D)(P) | clk(C)(P) * |
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     |   345 |   \|text_out_reg[34] /D v | MET Setup Check with Pin \|text_out_reg[34] /CP    |
0.513 |   1.945 |    2.458 | clk(D)(P) | clk(C)(P) * |
     |   346 |   \|text_out_reg[50] /D v | MET Setup Check with Pin \|text_out_reg[50] /CP    |
0.526 |   1.954 |    2.479 | clk(D)(P) | clk(C)(P) * |
     |   347 |   \|text_out_reg[23] /D v | MET Setup Check with Pin \|text_out_reg[23] /CP    |
0.527 |   1.945 |    2.472 | clk(D)(P) | clk(C)(P) * |
     |   348 |   \|text_out_reg[22] /D v | MET Setup Check with Pin \|text_out_reg[22] /CP    |
0.532 |   1.931 |    2.463 | clk(D)(P) | clk(C)(P) * |
     |   349 |  \|text_out_reg[114] /D v | MET Setup Check with Pin \|text_out_reg[114] /CP   |
0.540 |   1.936 |    2.476 | clk(D)(P) | clk(C)(P) * |
     |   350 |   \|text_out_reg[70] /D v | MET Setup Check with Pin \|text_out_reg[70] /CP    |
0.541 |   1.926 |    2.468 | clk(D)(P) | clk(C)(P) * |
     |   351 |   \|text_out_reg[54] /D v | MET Setup Check with Pin \|text_out_reg[54] /CP    |
0.543 |   1.931 |    2.474 | clk(D)(P) | clk(C)(P) * |
     |   352 |  \|text_out_reg[127] /D v | MET Setup Check with Pin \|text_out_reg[127] /CP   |
0.547 |   1.928 |    2.475 | clk(D)(P) | clk(C)(P) * |
     |   353 |   \|text_out_reg[32] /D v | MET Setup Check with Pin \|text_out_reg[32] /CP    |
0.550 |   1.937 |    2.487 | clk(D)(P) | clk(C)(P) * |
     |   354 |   \|text_out_reg[33] /D v | MET Setup Check with Pin \|text_out_reg[33] /CP    |
0.557 |   1.915 |    2.472 | clk(D)(P) | clk(C)(P) * |
     |   355 |   \|text_out_reg[90] /D ^ | MET Setup Check with Pin \|text_out_reg[90] /CP    |
0.560 |   1.902 |    2.462 | clk(D)(P) | clk(C)(P) * |
     |   356 |   \|text_out_reg[14] /D v | MET Setup Check with Pin \|text_out_reg[14] /CP    |
0.563 |   1.914 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   357 |   \|text_out_reg[38] /D v | MET Setup Check with Pin \|text_out_reg[38] /CP    |
0.566 |   1.915 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   358 |   \|text_out_reg[17] /D v | MET Setup Check with Pin \|text_out_reg[17] /CP    |
0.570 |   1.899 |    2.469 | clk(D)(P) | clk(C)(P) * |
     |   359 |   \|text_out_reg[18] /D v | MET Setup Check with Pin \|text_out_reg[18] /CP    |
0.570 |   1.908 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   360 |   \|text_out_reg[48] /D v | MET Setup Check with Pin \|text_out_reg[48] /CP    |
0.571 |   1.895 |    2.466 | clk(D)(P) | clk(C)(P) * |
     |   361 |   \|text_out_reg[46] /D v | MET Setup Check with Pin \|text_out_reg[46] /CP    |
0.572 |   1.905 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   362 |   \|text_out_reg[51] /D v | MET Setup Check with Pin \|text_out_reg[51] /CP    |
0.578 |   1.904 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |   363 |  \|text_out_reg[105] /D v | MET Setup Check with Pin \|text_out_reg[105] /CP   |
0.582 |   1.890 |    2.472 | clk(D)(P) | clk(C)(P) * |
     |   364 |    \|u0|w_reg[0][19] /D v | MET Setup Check with Pin \|u0|w_reg[0][19] /CP     |
0.589 |   1.909 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   365 |   \|text_out_reg[71] /D v | MET Setup Check with Pin \|text_out_reg[71] /CP    |
0.591 |   1.886 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   366 |   \|text_out_reg[77] /D v | MET Setup Check with Pin \|text_out_reg[77] /CP    |
0.595 |   1.866 |    2.461 | clk(D)(P) | clk(C)(P) * |
     |   367 |   \|text_out_reg[69] /D v | MET Setup Check with Pin \|text_out_reg[69] /CP    |
0.595 |   1.882 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   368 |   \|text_out_reg[11] /D v | MET Setup Check with Pin \|text_out_reg[11] /CP    |
0.598 |   1.873 |    2.471 | clk(D)(P) | clk(C)(P) * |
     |   369 |  \|text_out_reg[108] /D v | MET Setup Check with Pin \|text_out_reg[108] /CP   |
0.614 |   1.868 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   370 |   \|text_out_reg[41] /D v | MET Setup Check with Pin \|text_out_reg[41] /CP    |
0.627 |   1.850 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   371 |   \|text_out_reg[44] /D v | MET Setup Check with Pin \|text_out_reg[44] /CP    |
0.629 |   1.851 |    2.480 | clk(D)(P) | clk(C)(P) * |
     |   372 |   \|text_out_reg[84] /D v | MET Setup Check with Pin \|text_out_reg[84] /CP    |
0.630 |   1.851 |    2.481 | clk(D)(P) | clk(C)(P) * |
     |   373 |   \|text_out_reg[26] /D v | MET Setup Check with Pin \|text_out_reg[26] /CP    |
0.634 |   1.843 |    2.477 | clk(D)(P) | clk(C)(P) * |
     |   374 |  \|u0|r0|rcnt_reg[3] /D ^ | MET Setup Check with Pin \|u0|r0|rcnt_reg[3] /CP   |
0.640 |   1.858 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   375 |    \|text_out_reg[0] /D v | MET Setup Check with Pin \|text_out_reg[0] /CP     |
0.644 |   1.839 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |   376 |   \|text_out_reg[80] /D ^ | MET Setup Check with Pin \|text_out_reg[80] /CP    |
0.648 |   1.828 |    2.475 | clk(D)(P) | clk(C)(P) * |
     |   377 |  \|u0|r0|out_reg[28] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[28] /CP   |
0.652 |   1.844 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |   378 |   \|text_out_reg[42] /D v | MET Setup Check with Pin \|text_out_reg[42] /CP    |
0.653 |   1.811 |    2.464 | clk(D)(P) | clk(C)(P) * |
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     |   379 |   \|text_out_reg[19] /D v | MET Setup Check with Pin \|text_out_reg[19] /CP    |
0.661 |   1.805 |    2.467 | clk(D)(P) | clk(C)(P) * |
     |   380 |  \|text_out_reg[107] /D v | MET Setup Check with Pin \|text_out_reg[107] /CP   |
0.662 |   1.821 |    2.484 | clk(D)(P) | clk(C)(P) * |
     |   381 |   \|text_out_reg[73] /D v | MET Setup Check with Pin \|text_out_reg[73] /CP    |
0.666 |   1.804 |    2.471 | clk(D)(P) | clk(C)(P) * |
     |   382 |  \|u0|r0|out_reg[31] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[31] /CP   |
0.670 |   1.826 |    2.496 | clk(D)(P) | clk(C)(P) * |
     |   383 |  \|u0|r0|out_reg[30] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[30] /CP   |
0.674 |   1.835 |    2.508 | clk(D)(P) | clk(C)(P) * |
     |   384 |   \|text_out_reg[13] /D v | MET Setup Check with Pin \|text_out_reg[13] /CP    |
0.680 |   1.798 |    2.478 | clk(D)(P) | clk(C)(P) * |
     |   385 |  \|u0|r0|out_reg[27] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[27] /CP   |
0.683 |   1.801 |    2.484 | clk(D)(P) | clk(C)(P) * |
     |   386 |  \|u0|r0|out_reg[24] /D v | MET Setup Check with Pin \|u0|r0|out_reg[24] /CP   |
0.684 |   1.792 |    2.476 | clk(D)(P) | clk(C)(P) * |
     |   387 |   \|text_out_reg[12] /D v | MET Setup Check with Pin \|text_out_reg[12] /CP    |
0.689 |   1.793 |    2.482 | clk(D)(P) | clk(C)(P) * |
     |   388 |  \|u0|r0|out_reg[25] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[25] /CP   |
0.692 |   1.801 |    2.492 | clk(D)(P) | clk(C)(P) * |
     |   389 |    \|text_out_reg[9] /D v | MET Setup Check with Pin \|text_out_reg[9] /CP     |
0.703 |   1.789 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   390 |  \|u0|r0|out_reg[26] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[26] /CP   |
0.710 |   1.789 |    2.500 | clk(D)(P) | clk(C)(P) * |
     |   391 |   \|text_out_reg[10] /D v | MET Setup Check with Pin \|text_out_reg[10] /CP    |
0.730 |   1.753 |    2.483 | clk(D)(P) | clk(C)(P) * |
     |   392 |  \|u0|r0|out_reg[29] /D ^ | MET Setup Check with Pin \|u0|r0|out_reg[29] /CP   |
0.735 |   1.770 |    2.504 | clk(D)(P) | clk(C)(P) * |
     |   393 |   \|text_out_reg[43] /D v | MET Setup Check with Pin \|text_out_reg[43] /CP    |
0.746 |   1.726 |    2.471 | clk(D)(P) | clk(C)(P) * |
     |   394 |  \|u0|r0|rcnt_reg[2] /D ^ | MET Setup Check with Pin \|u0|r0|rcnt_reg[2] /CP   |
0.776 |   1.717 |    2.493 | clk(D)(P) | clk(C)(P) * |
     |   395 |  \|u0|r0|rcnt_reg[0] /D ^ | MET Setup Check with Pin \|u0|r0|rcnt_reg[0] /CP   |
0.806 |   1.697 |    2.503 | clk(D)(P) | clk(C)(P) * |
     |   396 |  \|u0|r0|rcnt_reg[1] /D ^ | MET Setup Check with Pin \|u0|r0|rcnt_reg[1] /CP   |
0.808 |   1.695 |    2.503 | clk(D)(P) | clk(C)(P) * |
     |   397 |        \|dcnt_reg[1] /D v | MET Setup Check with Pin \|dcnt_reg[1] /CP         |
0.943 |   1.553 |    2.495 | clk(D)(P) | clk(C)(P) * |
     |   398 |        \|dcnt_reg[3] /D v | MET Setup Check with Pin \|dcnt_reg[3] /CP         |
0.996 |   1.504 |    2.499 | clk(D)(P) | clk(C)(P) * |
     |   399 |           \|done_reg /D ^ | MET Setup Check with Pin \|done_reg /CP            |
0.997 |   1.500 |    2.497 | clk(D)(P) | clk(C)(P) * |
     |   400 |        \|dcnt_reg[0] /D v | MET Setup Check with Pin \|dcnt_reg[0] /CP         |
1.045 |   1.446 |    2.491 | clk(D)(P) | clk(C)(P) * |
     |   401 |  \|text_in_r_reg[67] /E v | MET Setup Check with Pin \|text_in_r_reg[67] /CP   |
1.049 |   1.280 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   402 |  \|text_in_r_reg[70] /E v | MET Setup Check with Pin \|text_in_r_reg[70] /CP   |
1.050 |   1.279 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   403 |  \|text_in_r_reg[69] /E v | MET Setup Check with Pin \|text_in_r_reg[69] /CP   |
1.050 |   1.279 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   404 |  \|text_in_r_reg[66] /E v | MET Setup Check with Pin \|text_in_r_reg[66] /CP   |
1.050 |   1.279 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   405 |  \|text_in_r_reg[65] /E v | MET Setup Check with Pin \|text_in_r_reg[65] /CP   |
1.051 |   1.278 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   406 |  \|text_in_r_reg[68] /E v | MET Setup Check with Pin \|text_in_r_reg[68] /CP   |
1.053 |   1.276 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   407 |  \|text_in_r_reg[64] /E v | MET Setup Check with Pin \|text_in_r_reg[64] /CP   |
1.053 |   1.276 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   408 | \|text_in_r_reg[127] /E v | MET Setup Check with Pin \|text_in_r_reg[127] /CP  |
1.058 |   1.276 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   409 | \|text_in_r_reg[125] /E v | MET Setup Check with Pin \|text_in_r_reg[125] /CP  |
1.058 |   1.276 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   410 |  \|text_in_r_reg[53] /E v | MET Setup Check with Pin \|text_in_r_reg[53] /CP   |
1.058 |   1.271 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   411 |  \|text_in_r_reg[63] /E v | MET Setup Check with Pin \|text_in_r_reg[63] /CP   |
1.062 |   1.267 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   412 |  \|text_in_r_reg[60] /E v | MET Setup Check with Pin \|text_in_r_reg[60] /CP   |
1.062 |   1.267 |    2.329 | clk(D)(P) | clk(C)(P) * |
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     |   413 |  \|text_in_r_reg[59] /E v | MET Setup Check with Pin \|text_in_r_reg[59] /CP   |
1.062 |   1.267 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   414 |  \|text_in_r_reg[56] /E v | MET Setup Check with Pin \|text_in_r_reg[56] /CP   |
1.062 |   1.267 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   415 |  \|text_in_r_reg[61] /E v | MET Setup Check with Pin \|text_in_r_reg[61] /CP   |
1.063 |   1.266 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   416 |  \|text_in_r_reg[58] /E v | MET Setup Check with Pin \|text_in_r_reg[58] /CP   |
1.063 |   1.266 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   417 |  \|text_in_r_reg[57] /E v | MET Setup Check with Pin \|text_in_r_reg[57] /CP   |
1.063 |   1.266 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   418 |  \|text_in_r_reg[55] /E v | MET Setup Check with Pin \|text_in_r_reg[55] /CP   |
1.063 |   1.266 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   419 | \|text_in_r_reg[123] /E v | MET Setup Check with Pin \|text_in_r_reg[123] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   420 | \|text_in_r_reg[121] /E v | MET Setup Check with Pin \|text_in_r_reg[121] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   421 | \|text_in_r_reg[113] /E v | MET Setup Check with Pin \|text_in_r_reg[113] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   422 | \|text_in_r_reg[115] /E v | MET Setup Check with Pin \|text_in_r_reg[115] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   423 | \|text_in_r_reg[118] /E v | MET Setup Check with Pin \|text_in_r_reg[118] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   424 | \|text_in_r_reg[116] /E v | MET Setup Check with Pin \|text_in_r_reg[116] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   425 | \|text_in_r_reg[117] /E v | MET Setup Check with Pin \|text_in_r_reg[117] /CP  |
1.068 |   1.266 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   426 |  \|text_in_r_reg[97] /E v | MET Setup Check with Pin \|text_in_r_reg[97] /CP   |
1.069 |   1.261 |    2.329 | clk(D)(P) | clk(C)(P) * |
     |   427 | \|text_in_r_reg[112] /E v | MET Setup Check with Pin \|text_in_r_reg[112] /CP  |
1.069 |   1.265 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   428 | \|text_in_r_reg[114] /E v | MET Setup Check with Pin \|text_in_r_reg[114] /CP  |
1.069 |   1.265 |    2.334 | clk(D)(P) | clk(C)(P) * |
     |   429 |  \|text_in_r_reg[52] /E v | MET Setup Check with Pin \|text_in_r_reg[52] /CP   |
1.078 |   1.252 |    2.330 | clk(D)(P) | clk(C)(P) * |
     |   430 |  \|text_in_r_reg[54] /E v | MET Setup Check with Pin \|text_in_r_reg[54] /CP   |
1.079 |   1.251 |    2.330 | clk(D)(P) | clk(C)(P) * |
     |   431 |  \|text_in_r_reg[62] /E v | MET Setup Check with Pin \|text_in_r_reg[62] /CP   |
1.081 |   1.249 |    2.330 | clk(D)(P) | clk(C)(P) * |
     |   432 | \|text_in_r_reg[126] /E v | MET Setup Check with Pin \|text_in_r_reg[126] /CP  |
1.093 |   1.242 |    2.335 | clk(D)(P) | clk(C)(P) * |
     |   433 | \|text_in_r_reg[124] /E v | MET Setup Check with Pin \|text_in_r_reg[124] /CP  |
1.093 |   1.242 |    2.335 | clk(D)(P) | clk(C)(P) * |
     |   434 | \|text_in_r_reg[122] /E v | MET Setup Check with Pin \|text_in_r_reg[122] /CP  |
1.093 |   1.242 |    2.335 | clk(D)(P) | clk(C)(P) * |
     |   435 | \|text_in_r_reg[120] /E v | MET Setup Check with Pin \|text_in_r_reg[120] /CP  |
1.099 |   1.236 |    2.335 | clk(D)(P) | clk(C)(P) * |
     |   436 | \|text_in_r_reg[119] /E v | MET Setup Check with Pin \|text_in_r_reg[119] /CP  |
1.107 |   1.229 |    2.335 | clk(D)(P) | clk(C)(P) * |
     |   437 |       \|dcnt_reg[2] /D ^ | MET Setup Check with Pin \|dcnt_reg[2] /CP         |
1.333 |   1.165 |    2.498 | clk(D)(P) | clk(C)(P) * |
     |   438 |  \|text_in_r_reg[90] /E v | MET Setup Check with Pin \|text_in_r_reg[90] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   439 |  \|text_in_r_reg[89] /E v | MET Setup Check with Pin \|text_in_r_reg[89] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   440 |  \|text_in_r_reg[88] /E v | MET Setup Check with Pin \|text_in_r_reg[88] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   441 |  \|text_in_r_reg[87] /E v | MET Setup Check with Pin \|text_in_r_reg[87] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   442 |  \|text_in_r_reg[86] /E v | MET Setup Check with Pin \|text_in_r_reg[86] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   443 |  \|text_in_r_reg[85] /E v | MET Setup Check with Pin \|text_in_r_reg[85] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   444 |  \|text_in_r_reg[84] /E v | MET Setup Check with Pin \|text_in_r_reg[84] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   445 |  \|text_in_r_reg[83] /E v | MET Setup Check with Pin \|text_in_r_reg[83] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   446 |  \|text_in_r_reg[82] /E v | MET Setup Check with Pin \|text_in_r_reg[82] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
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     |   447 |  \|text_in_r_reg[81] /E v | MET Setup Check with Pin \|text_in_r_reg[81] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   448 |  \|text_in_r_reg[80] /E v | MET Setup Check with Pin \|text_in_r_reg[80] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   449 |  \|text_in_r_reg[79] /E v | MET Setup Check with Pin \|text_in_r_reg[79] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   450 |  \|text_in_r_reg[78] /E v | MET Setup Check with Pin \|text_in_r_reg[78] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   451 |  \|text_in_r_reg[77] /E v | MET Setup Check with Pin \|text_in_r_reg[77] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   452 |  \|text_in_r_reg[76] /E v | MET Setup Check with Pin \|text_in_r_reg[76] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   453 |  \|text_in_r_reg[75] /E v | MET Setup Check with Pin \|text_in_r_reg[75] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   454 |  \|text_in_r_reg[74] /E v | MET Setup Check with Pin \|text_in_r_reg[74] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   455 |  \|text_in_r_reg[73] /E v | MET Setup Check with Pin \|text_in_r_reg[73] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   456 |  \|text_in_r_reg[72] /E v | MET Setup Check with Pin \|text_in_r_reg[72] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   457 |  \|text_in_r_reg[71] /E v | MET Setup Check with Pin \|text_in_r_reg[71] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   458 | \|text_in_r_reg[111] /E v | MET Setup Check with Pin \|text_in_r_reg[111] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   459 | \|text_in_r_reg[110] /E v | MET Setup Check with Pin \|text_in_r_reg[110] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   460 | \|text_in_r_reg[109] /E v | MET Setup Check with Pin \|text_in_r_reg[109] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   461 | \|text_in_r_reg[108] /E v | MET Setup Check with Pin \|text_in_r_reg[108] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   462 | \|text_in_r_reg[107] /E v | MET Setup Check with Pin \|text_in_r_reg[107] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   463 | \|text_in_r_reg[106] /E v | MET Setup Check with Pin \|text_in_r_reg[106] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   464 | \|text_in_r_reg[105] /E v | MET Setup Check with Pin \|text_in_r_reg[105] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   465 | \|text_in_r_reg[104] /E v | MET Setup Check with Pin \|text_in_r_reg[104] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   466 | \|text_in_r_reg[103] /E v | MET Setup Check with Pin \|text_in_r_reg[103] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   467 | \|text_in_r_reg[102] /E v | MET Setup Check with Pin \|text_in_r_reg[102] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   468 | \|text_in_r_reg[101] /E v | MET Setup Check with Pin \|text_in_r_reg[101] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   469 | \|text_in_r_reg[100] /E v | MET Setup Check with Pin \|text_in_r_reg[100] /CP  |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   470 |  \|text_in_r_reg[99] /E v | MET Setup Check with Pin \|text_in_r_reg[99] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   471 |  \|text_in_r_reg[98] /E v | MET Setup Check with Pin \|text_in_r_reg[98] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   472 |  \|text_in_r_reg[96] /E v | MET Setup Check with Pin \|text_in_r_reg[96] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   473 |  \|text_in_r_reg[95] /E v | MET Setup Check with Pin \|text_in_r_reg[95] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   474 |  \|text_in_r_reg[94] /E v | MET Setup Check with Pin \|text_in_r_reg[94] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   475 |  \|text_in_r_reg[93] /E v | MET Setup Check with Pin \|text_in_r_reg[93] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   476 |  \|text_in_r_reg[92] /E v | MET Setup Check with Pin \|text_in_r_reg[92] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   477 |  \|text_in_r_reg[91] /E v | MET Setup Check with Pin \|text_in_r_reg[91] /CP   |
1.349 |   1.069 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   478 |  \|text_in_r_reg[51] /E v | MET Setup Check with Pin \|text_in_r_reg[51] /CP   |
1.350 |   1.067 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   479 |  \|text_in_r_reg[50] /E v | MET Setup Check with Pin \|text_in_r_reg[50] /CP   |
1.350 |   1.067 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   480 |  \|text_in_r_reg[49] /E v | MET Setup Check with Pin \|text_in_r_reg[49] /CP   |
1.350 |   1.067 |    2.418 | clk(D)(P) | clk(C)(P) * |
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| 481 | \|text_in_r_reg[48] /E v | MET Setup Check with Pin \|text_in_r_reg[48] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 482 | \|text_in_r_reg[47] /E v | MET Setup Check with Pin \|text_in_r_reg[47] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 483 | \|text_in_r_reg[46] /E v | MET Setup Check with Pin \|text_in_r_reg[46] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 484 | \|text_in_r_reg[45] /E v | MET Setup Check with Pin \|text_in_r_reg[45] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 485 | \|text_in_r_reg[44] /E v | MET Setup Check with Pin \|text_in_r_reg[44] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 486 | \|text_in_r_reg[43] /E v | MET Setup Check with Pin \|text_in_r_reg[43] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 487 | \|text_in_r_reg[42] /E v | MET Setup Check with Pin \|text_in_r_reg[42] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 488 | \|text_in_r_reg[41] /E v | MET Setup Check with Pin \|text_in_r_reg[41] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 489 | \|text_in_r_reg[40] /E v | MET Setup Check with Pin \|text_in_r_reg[40] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 490 | \|text_in_r_reg[39] /E v | MET Setup Check with Pin \|text_in_r_reg[39] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 491 | \|text_in_r_reg[38] /E v | MET Setup Check with Pin \|text_in_r_reg[38] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 492 | \|text_in_r_reg[37] /E v | MET Setup Check with Pin \|text_in_r_reg[37] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 493 | \|text_in_r_reg[36] /E v | MET Setup Check with Pin \|text_in_r_reg[36] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 494 | \|text_in_r_reg[35] /E v | MET Setup Check with Pin \|text_in_r_reg[35] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 495 | \|text_in_r_reg[34] /E v | MET Setup Check with Pin \|text_in_r_reg[34] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 496 | \|text_in_r_reg[33] /E v | MET Setup Check with Pin \|text_in_r_reg[33] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 497 | \|text_in_r_reg[32] /E v | MET Setup Check with Pin \|text_in_r_reg[32] /CP |
1.350 | 1.067 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 498 | \|text_in_r_reg[31] /E v | MET Setup Check with Pin \|text_in_r_reg[31] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 499 | \|text_in_r_reg[30] /E v | MET Setup Check with Pin \|text_in_r_reg[30] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 500 | \|text_in_r_reg[29] /E v | MET Setup Check with Pin \|text_in_r_reg[29] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 501 | \|text_in_r_reg[28] /E v | MET Setup Check with Pin \|text_in_r_reg[28] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 502 | \|text_in_r_reg[27] /E v | MET Setup Check with Pin \|text_in_r_reg[27] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 503 | \|text_in_r_reg[26] /E v | MET Setup Check with Pin \|text_in_r_reg[26] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 504 | \|text_in_r_reg[25] /E v | MET Setup Check with Pin \|text_in_r_reg[25] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 505 | \|text_in_r_reg[24] /E v | MET Setup Check with Pin \|text_in_r_reg[24] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 506 | \|text_in_r_reg[23] /E v | MET Setup Check with Pin \|text_in_r_reg[23] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 507 | \|text_in_r_reg[22] /E v | MET Setup Check with Pin \|text_in_r_reg[22] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 508 | \|text_in_r_reg[21] /E v | MET Setup Check with Pin \|text_in_r_reg[21] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 509 | \|text_in_r_reg[20] /E v | MET Setup Check with Pin \|text_in_r_reg[20] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 510 | \|text_in_r_reg[19] /E v | MET Setup Check with Pin \|text_in_r_reg[19] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 511 | \|text_in_r_reg[18] /E v | MET Setup Check with Pin \|text_in_r_reg[18] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 512 | \|text_in_r_reg[17] /E v | MET Setup Check with Pin \|text_in_r_reg[17] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 513 | \|text_in_r_reg[16] /E v | MET Setup Check with Pin \|text_in_r_reg[16] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |
| 514 | \|text_in_r_reg[15] /E v | MET Setup Check with Pin \|text_in_r_reg[15] /CP |
1.359 | 1.059 | 2.418 | clk(D)(P) | clk(C)(P) * |

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     |   515 |  \|text_in_r_reg[14] /E v | MET Setup Check with Pin \|text_in_r_reg[14] /CP   |
1.359 |   1.059 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   516 |  \|text_in_r_reg[13] /E v | MET Setup Check with Pin \|text_in_r_reg[13] /CP   |
1.359 |   1.059 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   517 |  \|text_in_r_reg[12] /E v | MET Setup Check with Pin \|text_in_r_reg[12] /CP   |
1.359 |   1.059 |    2.418 | clk(D)(P) | clk(C)(P) * |
     |   518 | \|text_in_r_reg[102] /D v | MET Setup Check with Pin \|text_in_r_reg[102] /CP  |
1.691 |   0.760 |    2.451 | clk(D)(P) | clk(C)(P) * |
     |   519 | \|text_in_r_reg[121] /D v | MET Setup Check with Pin \|text_in_r_reg[121] /CP  |
1.692 |   0.760 |    2.451 | clk(D)(P) | clk(C)(P) * |
     |   520 | \|text_in_r_reg[105] /D v | MET Setup Check with Pin \|text_in_r_reg[105] /CP  |
1.694 |   0.758 |    2.452 | clk(D)(P) | clk(C)(P) * |
     |   521 |  \|text_in_r_reg[71] /D v | MET Setup Check with Pin \|text_in_r_reg[71] /CP   |
1.694 |   0.759 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   522 | \|text_in_r_reg[123] /D v | MET Setup Check with Pin \|text_in_r_reg[123] /CP  |
1.696 |   0.757 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   523 |  \|text_in_r_reg[67] /D v | MET Setup Check with Pin \|text_in_r_reg[67] /CP   |
1.696 |   0.756 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   524 | \|text_in_r_reg[116] /D v | MET Setup Check with Pin \|text_in_r_reg[116] /CP  |
1.697 |   0.756 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   525 |  \|text_in_r_reg[11] /E ^ | MET Setup Check with Pin \|text_in_r_reg[11] /CP   |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   526 |  \|text_in_r_reg[10] /E ^ | MET Setup Check with Pin \|text_in_r_reg[10] /CP   |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   527 |   \|text_in_r_reg[9] /E ^ | MET Setup Check with Pin \|text_in_r_reg[9] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   528 |   \|text_in_r_reg[8] /E ^ | MET Setup Check with Pin \|text_in_r_reg[8] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   529 |   \|text_in_r_reg[7] /E ^ | MET Setup Check with Pin \|text_in_r_reg[7] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   530 |   \|text_in_r_reg[6] /E ^ | MET Setup Check with Pin \|text_in_r_reg[6] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   531 |   \|text_in_r_reg[5] /E ^ | MET Setup Check with Pin \|text_in_r_reg[5] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   532 |   \|text_in_r_reg[4] /E ^ | MET Setup Check with Pin \|text_in_r_reg[4] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   533 |   \|text_in_r_reg[3] /E ^ | MET Setup Check with Pin \|text_in_r_reg[3] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   534 |   \|text_in_r_reg[2] /E ^ | MET Setup Check with Pin \|text_in_r_reg[2] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   535 |   \|text_in_r_reg[1] /E ^ | MET Setup Check with Pin \|text_in_r_reg[1] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   536 |   \|text_in_r_reg[0] /E ^ | MET Setup Check with Pin \|text_in_r_reg[0] /CP    |
1.698 |   0.753 |    2.450 | clk(D)(P) | clk(C)(P) * |
     |   537 |  \|text_in_r_reg[96] /D v | MET Setup Check with Pin \|text_in_r_reg[96] /CP   |
1.698 |   0.755 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   538 | \|text_in_r_reg[117] /D v | MET Setup Check with Pin \|text_in_r_reg[117] /CP  |
1.699 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   539 | \|text_in_r_reg[109] /D v | MET Setup Check with Pin \|text_in_r_reg[109] /CP  |
1.699 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   540 | \|text_in_r_reg[127] /D v | MET Setup Check with Pin \|text_in_r_reg[127] /CP  |
1.699 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   541 | \|text_in_r_reg[125] /D v | MET Setup Check with Pin \|text_in_r_reg[125] /CP  |
1.700 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   542 |  \|text_in_r_reg[97] /D v | MET Setup Check with Pin \|text_in_r_reg[97] /CP   |
1.700 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   543 | \|text_in_r_reg[118] /D v | MET Setup Check with Pin \|text_in_r_reg[118] /CP  |
1.700 |   0.754 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   544 |  \|text_in_r_reg[99] /D v | MET Setup Check with Pin \|text_in_r_reg[99] /CP   |
1.700 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   545 | \|text_in_r_reg[119] /D v | MET Setup Check with Pin \|text_in_r_reg[119] /CP  |
1.700 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   546 |  \|text_in_r_reg[11] /D v | MET Setup Check with Pin \|text_in_r_reg[11] /CP   |
1.700 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   547 | \|text_in_r_reg[115] /D v | MET Setup Check with Pin \|text_in_r_reg[115] /CP  |
1.700 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
     |   548 |  \|text_in_r_reg[78] /D v | MET Setup Check with Pin \|text_in_r_reg[78] /CP   |
1.700 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
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      |   549 |  \|text_in_r_reg[84] /D v | MET Setup Check with Pin \|text_in_r_reg[84] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   550 |  \|text_in_r_reg[30] /D v | MET Setup Check with Pin \|text_in_r_reg[30] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   551 |  \|text_in_r_reg[29] /D v | MET Setup Check with Pin \|text_in_r_reg[29] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   552 | \|text_in_r_reg[113] /D v | MET Setup Check with Pin \|text_in_r_reg[113] /CP  |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   553 |  \|text_in_r_reg[18] /D v | MET Setup Check with Pin \|text_in_r_reg[18] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   554 |  \|text_in_r_reg[79] /D v | MET Setup Check with Pin \|text_in_r_reg[79] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   555 |  \|text_in_r_reg[54] /D v | MET Setup Check with Pin \|text_in_r_reg[54] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   556 |  \|text_in_r_reg[16] /D v | MET Setup Check with Pin \|text_in_r_reg[16] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   557 |  \|text_in_r_reg[13] /D v | MET Setup Check with Pin \|text_in_r_reg[13] /CP   |
1.701 |   0.753 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   558 |  \|text_in_r_reg[43] /D v | MET Setup Check with Pin \|text_in_r_reg[43] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   559 |  \|text_in_r_reg[22] /D v | MET Setup Check with Pin \|text_in_r_reg[22] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   560 |  \|text_in_r_reg[62] /D v | MET Setup Check with Pin \|text_in_r_reg[62] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   561 | \|text_in_r_reg[120] /D v | MET Setup Check with Pin \|text_in_r_reg[120] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   562 | \|text_in_r_reg[104] /D v | MET Setup Check with Pin \|text_in_r_reg[104] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   563 |  \|text_in_r_reg[82] /D v | MET Setup Check with Pin \|text_in_r_reg[82] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   564 |  \|text_in_r_reg[81] /D v | MET Setup Check with Pin \|text_in_r_reg[81] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   565 |  \|text_in_r_reg[51] /D v | MET Setup Check with Pin \|text_in_r_reg[51] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   566 |  \|text_in_r_reg[49] /D v | MET Setup Check with Pin \|text_in_r_reg[49] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   567 |  \|text_in_r_reg[15] /D v | MET Setup Check with Pin \|text_in_r_reg[15] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   568 | \|text_in_r_reg[114] /D v | MET Setup Check with Pin \|text_in_r_reg[114] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   569 |  \|text_in_r_reg[19] /D v | MET Setup Check with Pin \|text_in_r_reg[19] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   570 |   \|text_in_r_reg[9] /D v | MET Setup Check with Pin \|text_in_r_reg[9] /CP    |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   571 | \|text_in_r_reg[126] /D v | MET Setup Check with Pin \|text_in_r_reg[126] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   572 |  \|text_in_r_reg[55] /D v | MET Setup Check with Pin \|text_in_r_reg[55] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   573 |  \|text_in_r_reg[52] /D v | MET Setup Check with Pin \|text_in_r_reg[52] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   574 | \|text_in_r_reg[110] /D v | MET Setup Check with Pin \|text_in_r_reg[110] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   575 |  \|text_in_r_reg[63] /D v | MET Setup Check with Pin \|text_in_r_reg[63] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   576 |  \|text_in_r_reg[41] /D v | MET Setup Check with Pin \|text_in_r_reg[41] /CP   |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   577 | \|text_in_r_reg[111] /D v | MET Setup Check with Pin \|text_in_r_reg[111] /CP  |
1.701 |   0.752 |    2.453 | clk(D)(P) | clk(C)(P) * |
      |   578 |  \|text_in_r_reg[75] /D v | MET Setup Check with Pin \|text_in_r_reg[75] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   579 |  \|text_in_r_reg[58] /D v | MET Setup Check with Pin \|text_in_r_reg[58] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   580 |   \|text_in_r_reg[7] /D v | MET Setup Check with Pin \|text_in_r_reg[7] /CP    |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   581 |   \|text_in_r_reg[0] /D v | MET Setup Check with Pin \|text_in_r_reg[0] /CP    |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   582 |  \|text_in_r_reg[83] /D v | MET Setup Check with Pin \|text_in_r_reg[83] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
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     |   583 |  \|text_in_r_reg[74] /D v | MET Setup Check with Pin \|text_in_r_reg[74] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   584 |  \|text_in_r_reg[61] /D v | MET Setup Check with Pin \|text_in_r_reg[61] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   585 |  \|text_in_r_reg[57] /D v | MET Setup Check with Pin \|text_in_r_reg[57] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   586 | \|text_in_r_reg[108] /D v | MET Setup Check with Pin \|text_in_r_reg[108] /CP  |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   587 |  \|text_in_r_reg[76] /D v | MET Setup Check with Pin \|text_in_r_reg[76] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   588 |  \|text_in_r_reg[73] /D v | MET Setup Check with Pin \|text_in_r_reg[73] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   589 |  \|text_in_r_reg[40] /D v | MET Setup Check with Pin \|text_in_r_reg[40] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   590 |  \|text_in_r_reg[24] /D v | MET Setup Check with Pin \|text_in_r_reg[24] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   591 |  \|text_in_r_reg[23] /D v | MET Setup Check with Pin \|text_in_r_reg[23] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   592 |   \|text_in_r_reg[8] /D v | MET Setup Check with Pin \|text_in_r_reg[8] /CP    |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   593 |  \|text_in_r_reg[86] /D v | MET Setup Check with Pin \|text_in_r_reg[86] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   594 |  \|text_in_r_reg[80] /D v | MET Setup Check with Pin \|text_in_r_reg[80] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   595 |  \|text_in_r_reg[38] /D v | MET Setup Check with Pin \|text_in_r_reg[38] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   596 |  \|text_in_r_reg[34] /D v | MET Setup Check with Pin \|text_in_r_reg[34] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   597 | \|text_in_r_reg[122] /D v | MET Setup Check with Pin \|text_in_r_reg[122] /CP  |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   598 |  \|text_in_r_reg[72] /D v | MET Setup Check with Pin \|text_in_r_reg[72] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   599 |  \|text_in_r_reg[44] /D v | MET Setup Check with Pin \|text_in_r_reg[44] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   600 |  \|text_in_r_reg[42] /D v | MET Setup Check with Pin \|text_in_r_reg[42] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   601 |  \|text_in_r_reg[36] /D v | MET Setup Check with Pin \|text_in_r_reg[36] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   602 |  \|text_in_r_reg[35] /D v | MET Setup Check with Pin \|text_in_r_reg[35] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   603 | \|text_in_r_reg[124] /D v | MET Setup Check with Pin \|text_in_r_reg[124] /CP  |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   604 | \|text_in_r_reg[112] /D v | MET Setup Check with Pin \|text_in_r_reg[112] /CP  |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   605 |  \|text_in_r_reg[88] /D v | MET Setup Check with Pin \|text_in_r_reg[88] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   606 |  \|text_in_r_reg[69] /D v | MET Setup Check with Pin \|text_in_r_reg[69] /CP   |
1.702 |   0.752 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   607 | \|text_in_r_reg[106] /D v | MET Setup Check with Pin \|text_in_r_reg[106] /CP  |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   608 |  \|text_in_r_reg[77] /D v | MET Setup Check with Pin \|text_in_r_reg[77] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   609 |  \|text_in_r_reg[50] /D v | MET Setup Check with Pin \|text_in_r_reg[50] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   610 |  \|text_in_r_reg[48] /D v | MET Setup Check with Pin \|text_in_r_reg[48] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   611 |  \|text_in_r_reg[45] /D v | MET Setup Check with Pin \|text_in_r_reg[45] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   612 |  \|text_in_r_reg[39] /D v | MET Setup Check with Pin \|text_in_r_reg[39] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   613 |  \|text_in_r_reg[33] /D v | MET Setup Check with Pin \|text_in_r_reg[33] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   614 |  \|text_in_r_reg[26] /D v | MET Setup Check with Pin \|text_in_r_reg[26] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   615 |  \|text_in_r_reg[20] /D v | MET Setup Check with Pin \|text_in_r_reg[20] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
     |   616 |  \|text_in_r_reg[87] /D v | MET Setup Check with Pin \|text_in_r_reg[87] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
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      |   617 |  \|text_in_r_reg[85] /D v | MET Setup Check with Pin \|text_in_r_reg[85] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   618 |  \|text_in_r_reg[47] /D v | MET Setup Check with Pin \|text_in_r_reg[47] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   619 |  \|text_in_r_reg[46] /D v | MET Setup Check with Pin \|text_in_r_reg[46] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   620 |  \|text_in_r_reg[37] /D v | MET Setup Check with Pin \|text_in_r_reg[37] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   621 |  \|text_in_r_reg[32] /D v | MET Setup Check with Pin \|text_in_r_reg[32] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   622 | \|text_in_r_reg[101] /D v | MET Setup Check with Pin \|text_in_r_reg[101] /CP  |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   623 |  \|text_in_r_reg[98] /D v | MET Setup Check with Pin \|text_in_r_reg[98] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   624 |  \|text_in_r_reg[66] /D v | MET Setup Check with Pin \|text_in_r_reg[66] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   625 |   \|text_in_r_reg[4] /D v | MET Setup Check with Pin \|text_in_r_reg[4] /CP    |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   626 |   \|text_in_r_reg[2] /D v | MET Setup Check with Pin \|text_in_r_reg[2] /CP    |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   627 | \|text_in_r_reg[100] /D v | MET Setup Check with Pin \|text_in_r_reg[100] /CP  |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   628 |  \|text_in_r_reg[68] /D v | MET Setup Check with Pin \|text_in_r_reg[68] /CP   |
1.702 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   629 |  \|text_in_r_reg[89] /D v | MET Setup Check with Pin \|text_in_r_reg[89] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   630 |  \|text_in_r_reg[90] /D v | MET Setup Check with Pin \|text_in_r_reg[90] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   631 | \|text_in_r_reg[107] /D v | MET Setup Check with Pin \|text_in_r_reg[107] /CP  |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   632 |  \|text_in_r_reg[70] /D v | MET Setup Check with Pin \|text_in_r_reg[70] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   633 |  \|text_in_r_reg[10] /D v | MET Setup Check with Pin \|text_in_r_reg[10] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   634 |   \|text_in_r_reg[6] /D v | MET Setup Check with Pin \|text_in_r_reg[6] /CP    |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   635 | \|text_in_r_reg[103] /D v | MET Setup Check with Pin \|text_in_r_reg[103] /CP  |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   636 |  \|text_in_r_reg[95] /D v | MET Setup Check with Pin \|text_in_r_reg[95] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   637 |  \|text_in_r_reg[93] /D v | MET Setup Check with Pin \|text_in_r_reg[93] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   638 |  \|text_in_r_reg[25] /D v | MET Setup Check with Pin \|text_in_r_reg[25] /CP   |
1.703 |   0.751 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   639 |  \|text_in_r_reg[27] /D v | MET Setup Check with Pin \|text_in_r_reg[27] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   640 |  \|text_in_r_reg[21] /D v | MET Setup Check with Pin \|text_in_r_reg[21] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   641 |  \|text_in_r_reg[14] /D v | MET Setup Check with Pin \|text_in_r_reg[14] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   642 |  \|text_in_r_reg[92] /D v | MET Setup Check with Pin \|text_in_r_reg[92] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   643 |   \|text_in_r_reg[5] /D v | MET Setup Check with Pin \|text_in_r_reg[5] /CP    |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   644 |   \|text_in_r_reg[3] /D v | MET Setup Check with Pin \|text_in_r_reg[3] /CP    |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   645 |  \|text_in_r_reg[91] /D v | MET Setup Check with Pin \|text_in_r_reg[91] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   646 |  \|text_in_r_reg[53] /D v | MET Setup Check with Pin \|text_in_r_reg[53] /CP   |
1.703 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   647 |  \|text_in_r_reg[94] /D v | MET Setup Check with Pin \|text_in_r_reg[94] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   648 |  \|text_in_r_reg[64] /D v | MET Setup Check with Pin \|text_in_r_reg[64] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   649 |  \|text_in_r_reg[60] /D v | MET Setup Check with Pin \|text_in_r_reg[60] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   650 |  \|text_in_r_reg[59] /D v | MET Setup Check with Pin \|text_in_r_reg[59] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
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      |   651 |  \|text_in_r_reg[28] /D v | MET Setup Check with Pin \|text_in_r_reg[28] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   652 |  \|text_in_r_reg[12] /D v | MET Setup Check with Pin \|text_in_r_reg[12] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   653 |   \|text_in_r_reg[1] /D v | MET Setup Check with Pin \|text_in_r_reg[1] /CP    |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   654 |  \|text_in_r_reg[65] /D v | MET Setup Check with Pin \|text_in_r_reg[65] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   655 |  \|text_in_r_reg[56] /D v | MET Setup Check with Pin \|text_in_r_reg[56] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   656 |  \|text_in_r_reg[31] /D v | MET Setup Check with Pin \|text_in_r_reg[31] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   657 |  \|text_in_r_reg[17] /D v | MET Setup Check with Pin \|text_in_r_reg[17] /CP   |
1.704 |   0.750 |    2.454 | clk(D)(P) | clk(C)(P) * |
      |   658 |           \|ld_r_reg /D v | MET Setup Check with Pin \|ld_r_reg /CP            |
1.751 |   0.753 |    2.503 | clk(D)(P) | clk(C)(P) * |
      |   659 |           text_out[12] v | MET Late External Delay Assertion                  |
1.869 |   0.231 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   660 |            text_out[0] v | MET Late External Delay Assertion                  |
1.870 |   0.230 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   661 |           text_out[24] v | MET Late External Delay Assertion                  |
1.873 |   0.227 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   662 |           text_out[96] v | MET Late External Delay Assertion                  |
1.873 |   0.227 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   663 |           text_out[39] v | MET Late External Delay Assertion                  |
1.874 |   0.226 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   664 |          text_out[114] v | MET Late External Delay Assertion                  |
1.875 |   0.225 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   665 |          text_out[123] v | MET Late External Delay Assertion                  |
1.876 |   0.224 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   666 |          text_out[113] v | MET Late External Delay Assertion                  |
1.877 |   0.223 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   667 |           text_out[29] v | MET Late External Delay Assertion                  |
1.878 |   0.222 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   668 |          text_out[108] v | MET Late External Delay Assertion                  |
1.879 |   0.221 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   669 |           text_out[32] v | MET Late External Delay Assertion                  |
1.881 |   0.219 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   670 |           text_out[81] v | MET Late External Delay Assertion                  |
1.882 |   0.218 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   671 |          text_out[118] v | MET Late External Delay Assertion                  |
1.883 |   0.217 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   672 |           text_out[41] v | MET Late External Delay Assertion                  |
1.884 |   0.216 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   673 |            text_out[2] v | MET Late External Delay Assertion                  |
1.884 |   0.216 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   674 |           text_out[77] v | MET Late External Delay Assertion                  |
1.885 |   0.215 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   675 |           text_out[80] v | MET Late External Delay Assertion                  |
1.885 |   0.215 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   676 |           text_out[15] v | MET Late External Delay Assertion                  |
1.885 |   0.214 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   677 |           text_out[43] v | MET Late External Delay Assertion                  |
1.887 |   0.213 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   678 |           text_out[34] v | MET Late External Delay Assertion                  |
1.888 |   0.212 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   679 |           text_out[49] v | MET Late External Delay Assertion                  |
1.888 |   0.212 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   680 |          text_out[102] v | MET Late External Delay Assertion                  |
1.888 |   0.212 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   681 |           text_out[66] v | MET Late External Delay Assertion                  |
1.888 |   0.212 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   682 |           text_out[50] v | MET Late External Delay Assertion                  |
1.889 |   0.211 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   683 |           text_out[33] v | MET Late External Delay Assertion                  |
1.891 |   0.209 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   684 |           text_out[54] v | MET Late External Delay Assertion                  |
1.892 |   0.208 |    2.100 | clk(D)(P) | clk(C)(P) * |
```

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      |   685 |           text_out[76] v | MET Late External Delay Assertion                |
1.892 |   0.208 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   686 |          text_out[112] v | MET Late External Delay Assertion                |
1.893 |   0.207 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   687 |           text_out[86] v | MET Late External Delay Assertion                |
1.893 |   0.207 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   688 |          text_out[101] v | MET Late External Delay Assertion                |
1.894 |   0.206 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   689 |           text_out[35] v | MET Late External Delay Assertion                |
1.894 |   0.206 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   690 |           text_out[74] v | MET Late External Delay Assertion                |
1.895 |   0.205 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   691 |          text_out[105] v | MET Late External Delay Assertion                |
1.895 |   0.205 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   692 |          text_out[106] v | MET Late External Delay Assertion                |
1.896 |   0.204 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   693 |           text_out[48] v | MET Late External Delay Assertion                |
1.896 |   0.204 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   694 |          text_out[115] v | MET Late External Delay Assertion                |
1.896 |   0.204 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   695 |           text_out[92] v | MET Late External Delay Assertion                |
1.896 |   0.204 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   696 |          text_out[104] v | MET Late External Delay Assertion                |
1.897 |   0.203 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   697 |           text_out[31] v | MET Late External Delay Assertion                |
1.897 |   0.202 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   698 |           text_out[98] v | MET Late External Delay Assertion                |
1.898 |   0.202 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   699 |          text_out[107] v | MET Late External Delay Assertion                |
1.898 |   0.202 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   700 |            text_out[7] v | MET Late External Delay Assertion                |
1.898 |   0.202 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   701 |            text_out[8] v | MET Late External Delay Assertion                |
1.898 |   0.202 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   702 |            text_out[6] v | MET Late External Delay Assertion                |
1.899 |   0.201 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   703 |          text_out[111] v | MET Late External Delay Assertion                |
1.899 |   0.201 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   704 |          text_out[110] v | MET Late External Delay Assertion                |
1.899 |   0.201 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   705 |           text_out[45] v | MET Late External Delay Assertion                |
1.899 |   0.201 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   706 |           text_out[13] v | MET Late External Delay Assertion                |
1.899 |   0.201 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   707 |           text_out[36] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   708 |           text_out[51] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   709 |           text_out[97] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   710 |           text_out[37] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   711 |           text_out[78] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   712 |           text_out[60] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   713 |          text_out[109] v | MET Late External Delay Assertion                |
1.900 |   0.200 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   714 |           text_out[47] v | MET Late External Delay Assertion                |
1.901 |   0.199 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   715 |           text_out[99] v | MET Late External Delay Assertion                |
1.901 |   0.199 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   716 |           text_out[53] v | MET Late External Delay Assertion                |
1.901 |   0.199 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   717 |           text_out[72] v | MET Late External Delay Assertion                |
1.901 |   0.199 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   718 |          text_out[125] v | MET Late External Delay Assertion                |
1.901 |   0.199 |    2.100 | clk(D)(P) | clk(C)(P) * |
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719	text_out[126] v	MET Late External Delay Assertion
1.902	0.198	2.100	clk(D)(P)	clk(C)(P) *
720	text_out[52] v	MET Late External Delay Assertion
1.902	0.198	2.100	clk(D)(P)	clk(C)(P) *
721	text_out[5] v	MET Late External Delay Assertion
1.903	0.197	2.100	clk(D)(P)	clk(C)(P) *
722	text_out[117] v	MET Late External Delay Assertion
1.903	0.197	2.100	clk(D)(P)	clk(C)(P) *
723	text_out[100] v	MET Late External Delay Assertion
1.903	0.197	2.100	clk(D)(P)	clk(C)(P) *
724	text_out[23] v	MET Late External Delay Assertion
1.903	0.197	2.100	clk(D)(P)	clk(C)(P) *
725	text_out[42] v	MET Late External Delay Assertion
1.903	0.197	2.100	clk(D)(P)	clk(C)(P) *
726	text_out[20] v	MET Late External Delay Assertion
1.904	0.196	2.100	clk(D)(P)	clk(C)(P) *
727	text_out[103] v	MET Late External Delay Assertion
1.904	0.196	2.100	clk(D)(P)	clk(C)(P) *
728	text_out[44] v	MET Late External Delay Assertion
1.904	0.196	2.100	clk(D)(P)	clk(C)(P) *
729	text_out[19] v	MET Late External Delay Assertion
1.905	0.195	2.100	clk(D)(P)	clk(C)(P) *
730	text_out[16] v	MET Late External Delay Assertion
1.905	0.195	2.100	clk(D)(P)	clk(C)(P) *
731	text_out[70] v	MET Late External Delay Assertion
1.905	0.195	2.100	clk(D)(P)	clk(C)(P) *
732	text_out[26] v	MET Late External Delay Assertion
1.905	0.195	2.100	clk(D)(P)	clk(C)(P) *
733	text_out[25] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
734	text_out[120] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
735	text_out[119] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
736	text_out[124] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
737	text_out[28] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
738	text_out[121] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
739	text_out[22] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
740	text_out[116] v	MET Late External Delay Assertion
1.906	0.194	2.100	clk(D)(P)	clk(C)(P) *
741	text_out[10] v	MET Late External Delay Assertion
1.907	0.193	2.100	clk(D)(P)	clk(C)(P) *
742	text_out[21] v	MET Late External Delay Assertion
1.907	0.193	2.100	clk(D)(P)	clk(C)(P) *
743	text_out[14] v	MET Late External Delay Assertion
1.907	0.193	2.100	clk(D)(P)	clk(C)(P) *
744	text_out[64] v	MET Late External Delay Assertion
1.907	0.193	2.100	clk(D)(P)	clk(C)(P) *
745	text_out[30] v	MET Late External Delay Assertion
1.909	0.191	2.100	clk(D)(P)	clk(C)(P) *
746	text_out[82] v	MET Late External Delay Assertion
1.909	0.191	2.100	clk(D)(P)	clk(C)(P) *
747	text_out[11] v	MET Late External Delay Assertion
1.910	0.190	2.100	clk(D)(P)	clk(C)(P) *
748	text_out[1] v	MET Late External Delay Assertion
1.914	0.186	2.100	clk(D)(P)	clk(C)(P) *
749	text_out[93] v	MET Late External Delay Assertion
1.915	0.185	2.100	clk(D)(P)	clk(C)(P) *
750	text_out[127] v	MET Late External Delay Assertion
1.915	0.185	2.100	clk(D)(P)	clk(C)(P) *
751	text_out[87] v	MET Late External Delay Assertion
1.919	0.181	2.100	clk(D)(P)	clk(C)(P) *
752	text_out[84] v	MET Late External Delay Assertion
1.919	0.181	2.100	clk(D)(P)	clk(C)(P) *

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      |   753 |           text_out[73] v | MET Late External Delay Assertion                |
1.920 |   0.180 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   754 |           text_out[89] v | MET Late External Delay Assertion                |
1.923 |   0.177 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   755 |           text_out[71] v | MET Late External Delay Assertion                |
1.926 |   0.174 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   756 |          text_out[122] v | MET Late External Delay Assertion                |
1.927 |   0.173 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   757 |                 done v | MET Late External Delay Assertion                |
1.929 |   0.171 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   758 |           text_out[9] v | MET Late External Delay Assertion                |
1.931 |   0.169 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   759 |           text_out[79] v | MET Late External Delay Assertion                |
1.931 |   0.169 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   760 |           text_out[83] v | MET Late External Delay Assertion                |
1.932 |   0.168 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   761 |           text_out[68] v | MET Late External Delay Assertion                |
1.932 |   0.168 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   762 |           text_out[75] v | MET Late External Delay Assertion                |
1.932 |   0.168 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   763 |           text_out[69] v | MET Late External Delay Assertion                |
1.932 |   0.168 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   764 |           text_out[65] v | MET Late External Delay Assertion                |
1.933 |   0.167 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   765 |           text_out[40] v | MET Late External Delay Assertion                |
1.934 |   0.166 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   766 |           text_out[88] v | MET Late External Delay Assertion                |
1.934 |   0.166 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   767 |           text_out[55] v | MET Late External Delay Assertion                |
1.934 |   0.166 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   768 |           text_out[27] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   769 |           text_out[17] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   770 |           text_out[63] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   771 |           text_out[90] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   772 |           text_out[56] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   773 |           text_out[46] v | MET Late External Delay Assertion                |
1.935 |   0.165 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   774 |           text_out[91] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   775 |           text_out[85] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   776 |            text_out[3] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   777 |           text_out[95] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   778 |           text_out[18] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   779 |           text_out[94] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   780 |           text_out[38] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   781 |           text_out[59] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   782 |           text_out[57] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   783 |           text_out[58] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   784 |           text_out[61] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   785 |           text_out[62] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
      |   786 |           text_out[67] v | MET Late External Delay Assertion                |
1.937 |   0.163 |    2.100 | clk(D)(P) | clk(C)(P) * |
```

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     |   787 |             text_out[4] v | MET Late External Delay Assertion                  |
1.938 |   0.162 |    2.100 | clk(D)(P) | clk(C)(P) * |
     +-------------------------------------------------------------------------------------------
-----------------------------------------------------+

<CMD> checkDesign

Usage: checkDesign [-help] {[-all [-danglingNet [highlight]]] | [[-io ] [-netlist [-danglingNet
[highlight]]] [-physicalLibrary ] [-timingLibrary ] [-powerGround ] [-tieHiLo ] [-floorplan ] [-
place ] ]} [[[-noText ] [-outdir <string>] [-browser ]] | [-noHtml [-outfile <string>]]]

**ERROR: (ENCTCM-32): Wrong number of arguments specified for command "checkDesign".
<CMD> checkDesign -physicalLibrary
Creating directory checkDesign.
Design check done.
Report saved in file checkDesign/aes_cipher_top.main.htm.ascii.
<CMD> report_power


Start force assigning power rail voltages for view default_view_setup
Finished assigning power rail voltages

CPE found ground net: gnd!
CPE found power net: vdd!  voltage: 0.9V
INFO (POWER-1606): Found clock 'clk' with frequency 400MHz from SDC file.


Propagating signal activity...


Starting Levelizing
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT)
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 5%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 10%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 15%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 20%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 25%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 30%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 35%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 40%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 45%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 50%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 55%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 60%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 65%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 70%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 75%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 80%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 85%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 90%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 95%

Finished Levelizing
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT)

Starting Activity Propagation
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT)
INFO (POWER-1356):   No default input activity has been set.  Defaulting to 0.2.

2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 5%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 10%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 15%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 20%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 25%
2011-May-06 00:04:53 (2011-May-06 05:04:53 GMT): 30%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 35%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 40%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 45%
```

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2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 50%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 55%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 60%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 65%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 70%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 75%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 80%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 85%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 90%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 95%

Finished Activity Propagation
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT)

Starting Calculating power
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT)

Calculating power dissipation...

 ... Calculating switching power
  Cannot locate supply power rail for net 'text_out[127]' of instance
|text_out_reg[127]
  Cannot locate supply power rail for net 'text_out[126]' of instance
|text_out_reg[126]
  Cannot locate supply power rail for net 'text_out[125]' of instance
|text_out_reg[125]
  Cannot locate supply power rail for net 'text_out[124]' of instance
|text_out_reg[124]
  Cannot locate supply power rail for net 'text_out[123]' of instance
|text_out_reg[123]
  only first five unconnected nets are listed...
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 5%
2011-May-06 00:04:54 (2011-May-06 05:04:54 GMT): 10%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 15%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 20%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 25%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 30%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 35%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 40%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 45%
2011-May-06 00:04:55 (2011-May-06 05:04:55 GMT): 50%
 ... Calculating internal and leakage power
WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdd cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

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WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

WARNING (POWER-2047): power_level vdds cannot be mapped for cell HS65_GSS_XOR3X2.

2011-May-06 00:04:58 (2011-May-06 05:04:58 GMT): 55%
2011-May-06 00:05:01 (2011-May-06 05:05:01 GMT): 60%
2011-May-06 00:05:03 (2011-May-06 05:05:03 GMT): 65%
2011-May-06 00:05:06 (2011-May-06 05:05:06 GMT): 70%
2011-May-06 00:05:09 (2011-May-06 05:05:09 GMT): 75%
2011-May-06 00:05:12 (2011-May-06 05:05:12 GMT): 80%
```

```
2011-May-06 00:05:15 (2011-May-06 05:05:15 GMT): 85%
2011-May-06 00:05:18 (2011-May-06 05:05:18 GMT): 90%
2011-May-06 00:05:21 (2011-May-06 05:05:21 GMT): 95%

Finished Calculating power
2011-May-06 00:05:23 (2011-May-06 05:05:23 GMT)
*-------------------------------------------------------------------------------------------
*       -  - Version  32-bit
*
*
*       Date & Time:   2011-May-06 00:05:23 (2011-May-06 05:05:23 GMT)
*
*-------------------------------------------------------------------------------------------
*
*       Design: aes_cipher_top
*
*       Liberty Libraries used:
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib
*
*       Power Domain used:
*              Rail:       vdd!      Voltage:        0.9
*
*       Power Units = 1mW
*
*       Time Units = 1e-09 secs
*
*       report_power
*
-------------------------------------------------------------------------------------------


Total Power
-------------------------------------------------------------------------------------------
Total Internal Power:       9.113      30.12%
Total Switching Power:       20.01      66.14%
Total Leakage Power:        1.13      3.737%
Total Power:       30.25
-------------------------------------------------------------------------------------------


Group                            Internal   Switching     Leakage       Total  Percentage
                                 Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------------
Sequential                          2.412        1.34      0.1459       3.899       12.89
Macro                                   0           0           0           0           0
IO                                      0           0           0           0           0
Combinational                       6.701       18.67      0.9845       26.35       87.11
Clock (Combinational)                   0           0           0           0           0
-------------------------------------------------------------------------------------------
Total                               9.113       20.01        1.13       30.25         100
-------------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------------
vdd!                      0.9         0           0           0           0           0
Default                   0.9     9.113       20.01        1.13       30.25         100


-------------------------------------------------------------------------------------------
*       Power Distribution Summary:
```

```
*              Highest Average Power:                  |u0|U229 (HS65_GSS_XOR2X6):
0.03724
*              Highest Leakage Power:        |text_in_r_reg[11] (HS65_GS_DFPHQX9):
0.0003203
*              Total Cap:     1.29583e-10 F
*              Total instances in design:  9809
*              Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*              Total Fillers and Decap:     0
-------------------------------------------------------------------------------------

report_power consumed time (real time) 00:00:36 : increased peak memory
(511M) by 5.
<CMD> reportCritNet
Marking critical nets with default slack = 0ps
critical nets number = 3753
<CMD> reportCapTable

Three process corners
TYPICAL_CASE:
M1
Width(um) Space(um) Ca(fF/um)      Cf(fF/um)      Cc(fF/um)
-----------------------------------------------------------------
0.09      0.072     0.0758         0.0304         0.1477
0.09      0.09      0.0668         0.0331         0.1159
0.09      0.27      0.0483         0.056          0.0313
0.09      0.45      0.0458         0.07           0.0117
0.09      0.63      0.0451         0.0764         0.0046
0.09      0.81      0.0449         0.0792         0.0018
0.09      0.99      0.0448         0.0804         0.0007
0.09      1.17      0.0448         0.0807         0.0002
0.27      0.072     0.1785         0.0251         0.1497
0.27      0.09      0.1673         0.0288         0.1174
0.27      0.27      0.1409         0.0557         0.0316
0.27      0.45      0.1364         0.0707         0.0118
0.27      0.63      0.135          0.0775         0.0046
0.27      0.81      0.1346         0.0804         0.0018
0.27      0.99      0.1344         0.0816         0.0007
0.27      1.17      0.1343         0.0821         0.0002
1         0.072     0.5493         0.0239         0.1499
1         0.09      0.5374         0.028          0.1175
1         0.27      0.5069         0.0568         0.0316
1         0.45      0.5006         0.0728         0.0118
1         0.63      0.4984         0.0801         0.0046
1         0.81      0.4976         0.0831         0.0018
1         0.99      0.4973         0.0844         0.0007
1         1.17      0.4972         0.0848         0.0002
9         0.072     4.53           0.052          0.1499
9         0.09      4.5179         0.0561         0.1175
9         0.27      4.4861         0.0858         0.0316
9         0.45      4.4788         0.1021         0.0118
9         0.63      4.4762         0.1096         0.0046
9         0.81      4.4752         0.1127         0.0018
9         0.99      4.4748         0.1141         0.0007
9         1.17      4.4746         0.1146         0.0002


M2
Width(um) Space(um) Ca(fF/um)      Cf(fF/um)      Cc(fF/um)
-----------------------------------------------------------------
0.1       0.08      0.0831         0.034          0.1232
0.1       0.1       0.0761         0.0373         0.0978
0.1       0.3       0.06           0.0649         0.0219
0.1       0.5       0.0581         0.0776         0.0064
0.1       0.7       0.0576         0.082          0.002
0.1       0.9       0.0575         0.0834         0.0006
0.1       1.1       0.0574         0.0839         0.0002
```

0.1	1.3	0.0574	0.084	0
0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M3

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0831	0.034	0.1232
0.1	0.1	0.0761	0.0373	0.0978
0.1	0.3	0.06	0.0649	0.0219
0.1	0.5	0.0581	0.0776	0.0064
0.1	0.7	0.0576	0.082	0.002
0.1	0.9	0.0575	0.0834	0.0006
0.1	1.1	0.0574	0.0839	0.0002
0.1	1.3	0.0574	0.084	0
0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M4

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0831	0.034	0.1232

0.1	0.1	0.0761	0.0373	0.0978
0.1	0.3	0.06	0.0649	0.0219
0.1	0.5	0.0581	0.0776	0.0064
0.1	0.7	0.0576	0.082	0.002
0.1	0.9	0.0575	0.0834	0.0006
0.1	1.1	0.0574	0.0839	0.0002
0.1	1.3	0.0574	0.084	0
0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M5

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0644	0.0291	0.1326
0.1	0.1	0.0577	0.0309	0.1077
0.1	0.3	0.0418	0.0484	0.0329
0.1	0.5	0.0394	0.0598	0.0149
0.1	0.7	0.0386	0.0661	0.0073
0.1	0.9	0.0383	0.0694	0.0037
0.1	1.1	0.0382	0.0713	0.0019
0.1	1.3	0.0381	0.0722	0.001
0.3	0.08	0.1527	0.0258	0.1368
0.3	0.1	0.1443	0.0282	0.1113
0.3	0.3	0.1212	0.0488	0.0343
0.3	0.5	0.1169	0.0613	0.0155
0.3	0.7	0.1154	0.0682	0.0077
0.3	0.9	0.1147	0.072	0.0039
0.3	1.1	0.1144	0.0739	0.002
0.3	1.3	0.1142	0.075	0.001
1	0.08	0.4264	0.0267	0.138
1	0.1	0.4173	0.0294	0.1124
1	0.3	0.3904	0.0518	0.0347
1	0.5	0.3845	0.065	0.0158
1	0.7	0.3822	0.0725	0.0078
1	0.9	0.3811	0.0764	0.004
1	1.1	0.3806	0.0785	0.002
1	1.3	0.3803	0.0797	0.001
9	0.08	3.4707	0.0733	0.138
9	0.1	3.4614	0.076	0.1124
9	0.3	3.4331	0.0991	0.0347
9	0.5	3.4262	0.1129	0.0158
9	0.7	3.4234	0.1205	0.0078
9	0.9	3.4221	0.1247	0.004
9	1.1	3.4214	0.1267	0.002
9	1.3	3.421	0.1279	0.001

M6

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.1121	0.0411	0.1691
0.4	0.4	0.102	0.0456	0.1341
0.4	1.2	0.079	0.082	0.0304
0.4	2	0.0762	0.0992	0.0092
0.4	2.8	0.0755	0.1053	0.0029
0.4	3.6	0.0753	0.1074	0.0009
0.4	4.4	0.0753	0.108	0.0002
0.4	5.2	0.0753	0.1083	0.0001
1.2	0.32	0.2774	0.034	0.1696
1.2	0.4	0.265	0.0396	0.1344
1.2	1.2	0.2326	0.0806	0.0304
1.2	2	0.2277	0.0989	0.0092
1.2	2.8	0.2264	0.1055	0.0029
1.2	3.6	0.226	0.1075	0.0009
1.2	4.4	0.2259	0.1083	0.0002
1.2	5.2	0.2259	0.1084	0.0001
2	0.32	0.4324	0.0317	0.1696
2	0.4	0.4196	0.0375	0.1344
2	1.2	0.3846	0.0798	0.0304
2	2	0.3788	0.0987	0.0092
2	2.8	0.3772	0.1053	0.0029
2	3.6	0.3767	0.1075	0.0009
2	4.4	0.3765	0.1081	0.0002
2	5.2	0.3765	0.1084	0.0001
9	0.32	1.756	0.0281	0.1696
9	0.4	1.7428	0.0341	0.1344
9	1.2	1.7044	0.0781	0.0304
9	2	1.6969	0.0977	0.0092
9	2.8	1.6948	0.1046	0.0029
9	3.6	1.6941	0.1069	0.0009
9	4.4	1.6939	0.1076	0.0002
9	5.2	1.6939	0.1078	0.0001

M7

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.076	0.0284	0.1748
0.4	0.4	0.0663	0.03	0.1417
0.4	1.2	0.0438	0.0467	0.0466
0.4	2	0.0406	0.0581	0.0249
0.4	2.8	0.0395	0.066	0.0151
0.4	3.6	0.0389	0.0714	0.0095
0.4	4.4	0.0386	0.0751	0.0061
0.4	5.2	0.0384	0.0776	0.004
1	0.32	0.1479	0.0223	0.18
1	0.4	0.1361	0.025	0.1466
1	1.2	0.1056	0.0453	0.0491
1	2	0.1002	0.0581	0.0263
1	2.8	0.0981	0.0666	0.016
1	3.6	0.0971	0.0724	0.0101
1	4.4	0.0965	0.0764	0.0065
1	5.2	0.0962	0.0792	0.0042
9	0.32	0.9343	0.035	0.2123
9	0.4	0.9164	0.0383	0.1628
9	1.2	0.8751	0.0618	0.0467
9	2	0.8683	0.0757	0.0271
9	2.8	0.8646	0.0854	0.016
9	3.6	0.8626	0.0918	0.0098
9	4.4	0.8615	0.0962	0.0061
9	5.2	0.8608	0.099	0.0039

BEST_CASE:
M1

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.09	0.072	0.0055	0.0024	0.1023
0.09	0.09	0.0102	0.0055	0.0814
0.09	0.27	0.0205	0.0249	0.0234
0.09	0.45	0.0219	0.0351	0.009
0.09	0.63	0.0224	0.0397	0.0036
0.09	0.81	0.0225	0.0417	0.0014
0.09	0.99	0.0226	0.0426	0.0006
0.09	1.17	0.0226	0.0429	0.0002
0.27	0.072	0.0429	0.0068	0.1051
0.27	0.09	0.0489	0.0093	0.0835
0.27	0.27	0.0639	0.0268	0.0239
0.27	0.45	0.0666	0.0365	0.0092
0.27	0.63	0.0674	0.041	0.0037
0.27	0.81	0.0677	0.043	0.0015
0.27	0.99	0.0679	0.0438	0.0006
0.27	1.17	0.0679	0.0442	0.0002
1	0.072	0.2216	0.0115	0.1053
1	0.09	0.2281	0.0138	0.0837
1	0.27	0.2455	0.0301	0.024
1	0.45	0.2494	0.0393	0.0092
1	0.63	0.2507	0.0436	0.0037
1	0.81	0.2512	0.0454	0.0015
1	0.99	0.2514	0.0462	0.0006
1	1.17	0.2515	0.0466	0.0002
9	0.072	2.2322	0.0381	0.1053
9	0.09	2.2388	0.0402	0.0837
9	0.27	2.257	0.0562	0.024
9	0.45	2.2614	0.065	0.0092
9	0.63	2.263	0.0692	0.0037
9	0.81	2.2637	0.071	0.0015
9	0.99	2.2639	0.0717	0.0006
9	1.17	2.2641	0.0721	0.0002

M2

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.014	0.0057	0.0805
0.1	0.1	0.0177	0.0086	0.0646
0.1	0.3	0.0265	0.0289	0.0149
0.1	0.5	0.0276	0.0373	0.0044
0.1	0.7	0.0278	0.0401	0.0013
0.1	0.9	0.0279	0.041	0.0004
0.1	1.1	0.0279	0.0413	0.0001
0.1	1.3	0.0279	0.0413	0
0.3	0.08	0.064	0.0093	0.0814
0.3	0.1	0.0686	0.0117	0.0653
0.3	0.3	0.0811	0.0305	0.0151
0.3	0.5	0.0831	0.0384	0.0045
0.3	0.7	0.0836	0.0411	0.0013
0.3	0.9	0.0838	0.0419	0.0004
0.3	1.1	0.0838	0.0422	0.0001
0.3	1.3	0.0839	0.0423	0
1	0.08	0.2563	0.0132	0.0814
1	0.1	0.2612	0.0156	0.0653
1	0.3	0.2757	0.0333	0.0151
1	0.5	0.2784	0.0409	0.0045
1	0.7	0.2792	0.0435	0.0013
1	0.9	0.2794	0.0443	0.0004
1	1.1	0.2795	0.0445	0.0001
1	1.3	0.2795	0.0445	0
9	0.08	2.4906	0.0401	0.0814
9	0.1	2.4955	0.0425	0.0653

9	0.3	2.5108	0.0597	0.0151
9	0.5	2.514	0.0671	0.0045
9	0.7	2.5149	0.0696	0.0013
9	0.9	2.5152	0.0704	0.0004
9	1.1	2.5153	0.0706	0.0001
9	1.3	2.5153	0.0707	0

M3

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.014	0.0057	0.0805
0.1	0.1	0.0177	0.0086	0.0646
0.1	0.3	0.0265	0.0289	0.0149
0.1	0.5	0.0276	0.0373	0.0044
0.1	0.7	0.0278	0.0401	0.0013
0.1	0.9	0.0279	0.041	0.0004
0.1	1.1	0.0279	0.0413	0.0001
0.1	1.3	0.0279	0.0413	0
0.3	0.08	0.064	0.0093	0.0814
0.3	0.1	0.0686	0.0117	0.0653
0.3	0.3	0.0811	0.0305	0.0151
0.3	0.5	0.0831	0.0384	0.0045
0.3	0.7	0.0836	0.0411	0.0013
0.3	0.9	0.0838	0.0419	0.0004
0.3	1.1	0.0838	0.0422	0.0001
0.3	1.3	0.0839	0.0423	0
1	0.08	0.2563	0.0132	0.0814
1	0.1	0.2612	0.0156	0.0653
1	0.3	0.2757	0.0333	0.0151
1	0.5	0.2784	0.0409	0.0045
1	0.7	0.2792	0.0435	0.0013
1	0.9	0.2794	0.0443	0.0004
1	1.1	0.2795	0.0445	0.0001
1	1.3	0.2795	0.0445	0
9	0.08	2.4906	0.0401	0.0814
9	0.1	2.4955	0.0425	0.0653
9	0.3	2.5108	0.0597	0.0151
9	0.5	2.514	0.0671	0.0045
9	0.7	2.5149	0.0696	0.0013
9	0.9	2.5152	0.0704	0.0004
9	1.1	2.5153	0.0706	0.0001
9	1.3	2.5153	0.0707	0

M4

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.014	0.0057	0.0805
0.1	0.1	0.0177	0.0086	0.0646
0.1	0.3	0.0265	0.0289	0.0149
0.1	0.5	0.0276	0.0373	0.0044
0.1	0.7	0.0278	0.0401	0.0013
0.1	0.9	0.0279	0.041	0.0004
0.1	1.1	0.0279	0.0413	0.0001
0.1	1.3	0.0279	0.0413	0
0.3	0.08	0.064	0.0093	0.0814
0.3	0.1	0.0686	0.0117	0.0653
0.3	0.3	0.0811	0.0305	0.0151
0.3	0.5	0.0831	0.0384	0.0045
0.3	0.7	0.0836	0.0411	0.0013
0.3	0.9	0.0838	0.0419	0.0004
0.3	1.1	0.0838	0.0422	0.0001
0.3	1.3	0.0839	0.0423	0
1	0.08	0.2563	0.0132	0.0814
1	0.1	0.2612	0.0156	0.0653
1	0.3	0.2757	0.0333	0.0151
1	0.5	0.2784	0.0409	0.0045

1	0.7	0.2792	0.0435	0.0013
1	0.9	0.2794	0.0443	0.0004
1	1.1	0.2795	0.0445	0.0001
1	1.3	0.2795	0.0445	0
9	0.08	2.4906	0.0401	0.0814
9	0.1	2.4955	0.0425	0.0653
9	0.3	2.5108	0.0597	0.0151
9	0.5	2.514	0.0671	0.0045
9	0.7	2.5149	0.0696	0.0013
9	0.9	2.5152	0.0704	0.0004
9	1.1	2.5153	0.0706	0.0001
9	1.3	2.5153	0.0707	0

M5

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0053	0.0026	0.0866
0.1	0.1	0.0086	0.005	0.0711
0.1	0.3	0.0168	0.0207	0.0231
0.1	0.5	0.0181	0.0287	0.0109
0.1	0.7	0.0185	0.0331	0.0056
0.1	0.9	0.0187	0.0355	0.003
0.1	1.1	0.0188	0.0368	0.0016
0.1	1.3	0.0189	0.0375	0.0009
0.3	0.08	0.036	0.0069	0.0909
0.3	0.1	0.0403	0.0088	0.075
0.3	0.3	0.0525	0.0228	0.0247
0.3	0.5	0.0549	0.0307	0.0117
0.3	0.7	0.0558	0.0351	0.0061
0.3	0.9	0.0562	0.0375	0.0033
0.3	1.1	0.0564	0.0389	0.0017
0.3	1.3	0.0566	0.0396	0.0009
1	0.08	0.1636	0.012	0.0925
1	0.1	0.1683	0.0137	0.0765
1	0.3	0.1828	0.0265	0.0254
1	0.5	0.1862	0.0341	0.0121
1	0.7	0.1875	0.0384	0.0063
1	0.9	0.1882	0.0409	0.0034
1	1.1	0.1885	0.0421	0.0018
1	1.3	0.1887	0.0429	0.001
9	0.08	1.6725	0.0435	0.0925
9	0.1	1.6774	0.0451	0.0765
9	0.3	1.6926	0.0576	0.0255
9	0.5	1.6966	0.0649	0.0121
9	0.7	1.6983	0.0691	0.0063
9	0.9	1.6992	0.0713	0.0034
9	1.1	1.6996	0.0726	0.0018
9	1.3	1.6998	0.0733	0.001

M6

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.0176	0.0066	0.125
0.4	0.4	0.0236	0.0108	0.0999
0.4	1.2	0.0377	0.0406	0.0232
0.4	2	0.0394	0.0532	0.0069
0.4	2.8	0.0398	0.0576	0.0021
0.4	3.6	0.0399	0.059	0.0006
0.4	4.4	0.04	0.0594	0.0002
0.4	5.2	0.04	0.0596	0
1.2	0.32	0.0884	0.011	0.1259
1.2	0.4	0.0959	0.0146	0.1006
1.2	1.2	0.1158	0.0417	0.0233
1.2	2	0.1189	0.0537	0.0069
1.2	2.8	0.1197	0.0579	0.0021
1.2	3.6	0.12	0.0592	0.0006

1.2	4.4	0.12	0.0597	0.0002
1.2	5.2	0.12	0.0598	0.0001
2	0.32	0.1657	0.0123	0.126
2	0.4	0.1734	0.0158	0.1006
2	1.2	0.195	0.0421	0.0233
2	2	0.1987	0.0537	0.0069
2	2.8	0.1997	0.0578	0.0021
2	3.6	0.2	0.0591	0.0006
2	4.4	0.2001	0.0596	0.0002
2	5.2	0.2001	0.0597	0.0001
9	0.32	0.8624	0.0137	0.1259
9	0.4	0.8703	0.017	0.1006
9	1.2	0.894	0.0422	0.0233
9	2	0.8987	0.0534	0.0069
9	2.8	0.9001	0.0572	0.0021
9	3.6	0.9005	0.0586	0.0006
9	4.4	0.9006	0.0589	0.0002
9	5.2	0.9006	0.059	0.0001

M7

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.0237	0	0.1126
0.4	0.4	0.0035	0.0016	0.103
0.4	1.2	0.017	0.0189	0.0345
0.4	2	0.0189	0.0285	0.0186
0.4	2.8	0.0196	0.0346	0.0114
0.4	3.6	0.0199	0.0388	0.0073
0.4	4.4	0.0201	0.0416	0.0049
0.4	5.2	0.0202	0.0435	0.0032
1	0.32	0.0195	0.003	0.1311
1	0.4	0.0264	0.005	0.1074
1	1.2	0.0448	0.0201	0.0369
1	2	0.0481	0.0296	0.0201
1	2.8	0.0493	0.0358	0.0123
1	3.6	0.05	0.0401	0.008
1	4.4	0.0503	0.0431	0.0052
1	5.2	0.0505	0.0451	0.0035
9	0.32	0.4141	0.0263	0.1585
9	0.4	0.4244	0.0289	0.1225
9	1.2	0.4487	0.045	0.0364
9	2	0.4527	0.0541	0.0217
9	2.8	0.4549	0.0605	0.0132
9	3.6	0.4562	0.065	0.0083
9	4.4	0.457	0.0679	0.0052
9	5.2	0.4574	0.07	0.0035

WORST_CASE:

M1

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.09	0.072	0.0758	0.0304	0.1477
0.09	0.09	0.0668	0.0331	0.1159
0.09	0.27	0.0483	0.056	0.0313
0.09	0.45	0.0458	0.07	0.0117
0.09	0.63	0.0451	0.0764	0.0046
0.09	0.81	0.0449	0.0792	0.0018
0.09	0.99	0.0448	0.0804	0.0007
0.09	1.17	0.0448	0.0807	0.0002
0.27	0.072	0.1785	0.0251	0.1497
0.27	0.09	0.1673	0.0288	0.1174
0.27	0.27	0.1409	0.0557	0.0316
0.27	0.45	0.1364	0.0707	0.0118
0.27	0.63	0.135	0.0775	0.0046
0.27	0.81	0.1346	0.0804	0.0018

0.27	0.99	0.1344	0.0816	0.0007
0.27	1.17	0.1343	0.0821	0.0002
1	0.072	0.5493	0.0239	0.1499
1	0.09	0.5374	0.028	0.1175
1	0.27	0.5069	0.0568	0.0316
1	0.45	0.5006	0.0728	0.0118
1	0.63	0.4984	0.0801	0.0046
1	0.81	0.4976	0.0831	0.0018
1	0.99	0.4973	0.0844	0.0007
1	1.17	0.4972	0.0848	0.0002
9	0.072	4.53	0.052	0.1499
9	0.09	4.5179	0.0561	0.1175
9	0.27	4.4861	0.0858	0.0316
9	0.45	4.4788	0.1021	0.0118
9	0.63	4.4762	0.1096	0.0046
9	0.81	4.4752	0.1127	0.0018
9	0.99	4.4748	0.1141	0.0007
9	1.17	4.4746	0.1146	0.0002

M2

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0831	0.034	0.1232
0.1	0.1	0.0761	0.0373	0.0978
0.1	0.3	0.06	0.0649	0.0219
0.1	0.5	0.0581	0.0776	0.0064
0.1	0.7	0.0576	0.082	0.002
0.1	0.9	0.0575	0.0834	0.0006
0.1	1.1	0.0574	0.0839	0.0002
0.1	1.3	0.0574	0.084	0
0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M3

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0831	0.034	0.1232
0.1	0.1	0.0761	0.0373	0.0978
0.1	0.3	0.06	0.0649	0.0219
0.1	0.5	0.0581	0.0776	0.0064
0.1	0.7	0.0576	0.082	0.002
0.1	0.9	0.0575	0.0834	0.0006
0.1	1.1	0.0574	0.0839	0.0002
0.1	1.3	0.0574	0.084	0

0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M4

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0831	0.034	0.1232
0.1	0.1	0.0761	0.0373	0.0978
0.1	0.3	0.06	0.0649	0.0219
0.1	0.5	0.0581	0.0776	0.0064
0.1	0.7	0.0576	0.082	0.002
0.1	0.9	0.0575	0.0834	0.0006
0.1	1.1	0.0574	0.0839	0.0002
0.1	1.3	0.0574	0.084	0
0.3	0.08	0.2083	0.0316	0.1238
0.3	0.1	0.1998	0.0358	0.0982
0.3	0.3	0.1771	0.0666	0.022
0.3	0.5	0.1737	0.08	0.0064
0.3	0.7	0.1728	0.0848	0.002
0.3	0.9	0.1725	0.0862	0.0006
0.3	1.1	0.1724	0.0866	0.0002
0.3	1.3	0.1724	0.0867	0
1	0.08	0.6165	0.0377	0.1238
1	0.1	0.6074	0.042	0.0982
1	0.3	0.5813	0.0746	0.022
1	0.5	0.5766	0.0887	0.0064
1	0.7	0.5753	0.0935	0.002
1	0.9	0.5749	0.0951	0.0006
1	1.1	0.5748	0.0956	0.0002
1	1.3	0.5747	0.0957	0
9	0.08	5.2173	0.1385	0.1238
9	0.1	5.2081	0.143	0.0982
9	0.3	5.1806	0.1762	0.022
9	0.5	5.1751	0.1907	0.0064
9	0.7	5.1735	0.1957	0.002
9	0.9	5.173	0.1972	0.0006
9	1.1	5.1729	0.1977	0.0002
9	1.3	5.1728	0.1979	0

M5

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.1	0.08	0.0644	0.0291	0.1326
0.1	0.1	0.0577	0.0309	0.1077

0.1	0.3	0.0418	0.0484	0.0329
0.1	0.5	0.0394	0.0598	0.0149
0.1	0.7	0.0386	0.0661	0.0073
0.1	0.9	0.0383	0.0694	0.0037
0.1	1.1	0.0382	0.0713	0.0019
0.1	1.3	0.0381	0.0722	0.001
0.3	0.08	0.1527	0.0258	0.1368
0.3	0.1	0.1443	0.0282	0.1113
0.3	0.3	0.1212	0.0488	0.0343
0.3	0.5	0.1169	0.0613	0.0155
0.3	0.7	0.1154	0.0682	0.0077
0.3	0.9	0.1147	0.072	0.0039
0.3	1.1	0.1144	0.0739	0.002
0.3	1.3	0.1142	0.075	0.001
1	0.08	0.4264	0.0267	0.138
1	0.1	0.4173	0.0294	0.1124
1	0.3	0.3904	0.0518	0.0347
1	0.5	0.3845	0.065	0.0158
1	0.7	0.3822	0.0725	0.0078
1	0.9	0.3811	0.0764	0.004
1	1.1	0.3806	0.0785	0.002
1	1.3	0.3803	0.0797	0.001
9	0.08	3.4707	0.0733	0.138
9	0.1	3.4614	0.076	0.1124
9	0.3	3.4331	0.0991	0.0347
9	0.5	3.4262	0.1129	0.0158
9	0.7	3.4234	0.1205	0.0078
9	0.9	3.4221	0.1247	0.004
9	1.1	3.4214	0.1267	0.002
9	1.3	3.421	0.1279	0.001

M6

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.1121	0.0411	0.1691
0.4	0.4	0.102	0.0456	0.1341
0.4	1.2	0.079	0.082	0.0304
0.4	2	0.0762	0.0992	0.0092
0.4	2.8	0.0755	0.1053	0.0029
0.4	3.6	0.0753	0.1074	0.0009
0.4	4.4	0.0753	0.108	0.0002
0.4	5.2	0.0753	0.1083	0.0001
1.2	0.32	0.2774	0.034	0.1696
1.2	0.4	0.265	0.0396	0.1344
1.2	1.2	0.2326	0.0806	0.0304
1.2	2	0.2277	0.0989	0.0092
1.2	2.8	0.2264	0.1055	0.0029
1.2	3.6	0.226	0.1075	0.0009
1.2	4.4	0.2259	0.1083	0.0002
1.2	5.2	0.2259	0.1084	0.0001
2	0.32	0.4324	0.0317	0.1696
2	0.4	0.4196	0.0375	0.1344
2	1.2	0.3846	0.0798	0.0304
2	2	0.3788	0.0987	0.0092
2	2.8	0.3772	0.1053	0.0029
2	3.6	0.3767	0.1075	0.0009
2	4.4	0.3765	0.1081	0.0002
2	5.2	0.3765	0.1084	0.0001
9	0.32	1.756	0.0281	0.1696
9	0.4	1.7428	0.0341	0.1344
9	1.2	1.7044	0.0781	0.0304
9	2	1.6969	0.0977	0.0092
9	2.8	1.6948	0.1046	0.0029
9	3.6	1.6941	0.1069	0.0009
9	4.4	1.6939	0.1076	0.0002
9	5.2	1.6939	0.1078	0.0001

M7

Width(um)	Space(um)	Ca(fF/um)	Cf(fF/um)	Cc(fF/um)
0.4	0.32	0.076	0.0284	0.1748
0.4	0.4	0.0663	0.03	0.1417
0.4	1.2	0.0438	0.0467	0.0466
0.4	2	0.0406	0.0581	0.0249
0.4	2.8	0.0395	0.066	0.0151
0.4	3.6	0.0389	0.0714	0.0095
0.4	4.4	0.0386	0.0751	0.0061
0.4	5.2	0.0384	0.0776	0.004
1	0.32	0.1479	0.0223	0.18
1	0.4	0.1361	0.025	0.1466
1	1.2	0.1056	0.0453	0.0491
1	2	0.1002	0.0581	0.0263
1	2.8	0.0981	0.0666	0.016
1	3.6	0.0971	0.0724	0.0101
1	4.4	0.0965	0.0764	0.0065
1	5.2	0.0962	0.0792	0.0042
9	0.32	0.9343	0.035	0.2123
9	0.4	0.9164	0.0383	0.1628
9	1.2	0.8751	0.0618	0.0467
9	2	0.8683	0.0757	0.0271
9	2.8	0.8646	0.0854	0.016
9	3.6	0.8626	0.0918	0.0098
9	4.4	0.8615	0.0962	0.0061
9	5.2	0.8608	0.099	0.0039

<CMD> report_ports

				Early		Late	
Pin Name	Dir	Assertion	Clock Name	Rise	Fall	Rise	Fall
clk	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
clk	IN	clock_root	clk(C)(P)				
key[0]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[0]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[100]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[100]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[101]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[101]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[102]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[102]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[103]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[103]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[104]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[104]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[105]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[105]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[106]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[106]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[107]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[107]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[108]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[108]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[109]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[109]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[10]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[10]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[110]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[110]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[111]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[111]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[112]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750

key[112]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[113]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[113]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[114]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[114]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[115]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[115]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[116]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[116]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[117]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[117]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[118]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[118]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[119]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[119]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[11]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[11]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[120]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[120]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[121]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[121]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[122]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[122]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[123]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[123]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[124]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[124]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[125]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[125]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[126]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[126]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[127]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[127]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[12]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[12]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[13]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[13]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[14]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[14]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[15]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[15]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[16]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[16]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[17]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[17]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[18]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[18]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[19]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[19]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[1]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[1]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[20]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[20]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[21]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[21]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[22]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[22]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[23]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[23]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[24]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[24]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[25]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[25]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[26]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[26]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[27]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[27]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[28]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750

key[28]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[29]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[29]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[2]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[2]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[30]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[30]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[31]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[31]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[32]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[32]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[33]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[33]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[34]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[34]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[35]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[35]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[36]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[36]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[37]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[37]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[38]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[38]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[39]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[39]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[3]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[3]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[40]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[40]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[41]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[41]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[42]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[42]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[43]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[43]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[44]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[44]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[45]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[45]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[46]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[46]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[47]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[47]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[48]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[48]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[49]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[49]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[4]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[4]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[50]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[50]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[51]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[51]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[52]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[52]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[53]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[53]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[54]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[54]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[55]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[55]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[56]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[56]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[57]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[57]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[58]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[58]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[59]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750

key[59]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[5]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[5]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[60]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[60]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[61]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[61]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[62]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[62]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[63]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[63]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[64]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[64]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[65]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[65]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[66]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[66]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[67]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[67]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[68]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[68]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[69]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[69]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[6]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[6]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[70]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[70]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[71]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[71]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[72]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[72]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[73]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[73]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[74]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[74]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[75]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[75]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[76]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[76]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[77]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[77]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[78]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[78]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[79]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[79]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[7]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[7]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[80]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[80]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[81]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[81]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[82]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[82]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[83]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[83]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[84]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[84]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[85]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[85]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[86]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[86]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[87]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[87]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[88]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[88]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[89]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[89]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[8]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100

key[8]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[90]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[90]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[91]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[91]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[92]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[92]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[93]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[93]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[94]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[94]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[95]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[95]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[96]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[96]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[97]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[97]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[98]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[98]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[99]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[99]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
key[9]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
key[9]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
ld	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
ld	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
rst	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
rst	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[0]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[0]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[100]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[100]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[101]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[101]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[102]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[102]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[103]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[103]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[104]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[104]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[105]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[105]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[106]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[106]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[107]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[107]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[108]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[108]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[109]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[109]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[10]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[10]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[110]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[110]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[111]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[111]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[112]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[112]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[113]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[113]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[114]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[114]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[115]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[115]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[116]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[116]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[117]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[117]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[118]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750

text_in[118]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[119]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[119]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[11]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[11]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[120]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[120]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[121]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[121]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[122]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[122]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[123]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[123]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[124]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[124]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[125]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[125]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[126]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[126]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[127]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[127]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[12]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[12]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[13]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[13]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[14]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[14]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[15]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[15]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[16]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[16]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[17]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[17]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[18]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[18]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[19]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[19]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[1]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[1]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[20]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[20]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[21]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[21]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[22]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[22]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[23]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[23]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[24]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[24]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[25]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[25]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[26]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[26]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[27]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[27]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[28]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[28]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[29]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[29]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[2]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[2]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[30]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[30]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[31]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[31]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[32]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[32]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[33]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100

text_in[33]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[34]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[34]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[35]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[35]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[36]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[36]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[37]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[37]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[38]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[38]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[39]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[39]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[3]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[3]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[40]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[40]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[41]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[41]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[42]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[42]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[43]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[43]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[44]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[44]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[45]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[45]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[46]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[46]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[47]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[47]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[48]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[48]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[49]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[49]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[4]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[4]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[50]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[50]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[51]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[51]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[52]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[52]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[53]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[53]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[54]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[54]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[55]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[55]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[56]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[56]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[57]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[57]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[58]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[58]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[59]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[59]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[5]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[5]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[60]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[60]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[61]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[61]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[62]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[62]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[63]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[63]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[64]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100

text_in[64]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[65]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[65]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[66]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[66]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[67]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[67]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[68]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[68]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[69]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[69]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[6]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[6]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[70]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[70]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[71]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[71]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[72]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[72]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[73]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[73]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[74]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[74]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[75]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[75]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[76]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[76]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[77]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[77]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[78]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[78]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[79]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[79]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[7]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[7]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[80]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[80]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[81]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[81]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[82]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[82]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[83]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[83]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[84]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[84]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[85]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[85]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[86]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[86]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[87]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[87]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[88]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[88]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[89]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[89]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[8]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[8]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[90]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[90]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[91]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[91]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[92]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[92]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[93]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[93]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[94]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[94]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[95]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100

text_in[95]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[96]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[96]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[97]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[97]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[98]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[98]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[99]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[99]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
text_in[9]	IN	input	clk(D)(P)	0.400	0.400	0.750	0.750
text_in[9]	IN	drive_resistance	*(D)(P)	0.100	0.100	0.100	0.100
done	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[0]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[100]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[101]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[102]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[103]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[104]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[105]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[106]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[107]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[108]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[109]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[10]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[110]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[111]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[112]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[113]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[114]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[115]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[116]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[117]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[118]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[119]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[11]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[120]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[121]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[122]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[123]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[124]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[125]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[126]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[127]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[12]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[13]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[14]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[15]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[16]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[17]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[18]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[19]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[1]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[20]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[21]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[22]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[23]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[24]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[25]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[26]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[27]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[28]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[29]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[2]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[30]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[31]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[32]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[33]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[34]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400

text_out[35]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[36]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[37]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[38]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[39]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[3]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[40]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[41]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[42]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[43]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[44]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[45]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[46]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[47]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[48]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[49]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[4]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[50]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[51]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[52]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[53]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[54]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[55]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[56]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[57]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[58]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[59]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[5]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[60]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[61]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[62]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[63]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[64]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[65]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[66]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[67]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[68]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[69]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[6]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[70]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[71]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[72]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[73]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[74]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[75]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[76]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[77]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[78]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[79]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[7]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[80]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[81]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[82]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[83]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[84]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[85]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[86]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[87]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[88]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[89]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[8]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[90]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[91]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[92]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[93]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[94]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[95]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[96]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400

text_out[97]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[98]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[99]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400
text_out[9]	OUT	external	clk(C)(P)	0.400	0.400	0.400	0.400

Pin Name	Dir	Assertion	Value
key[127]	IN	slew_limit	(: 1.500)
key[127]	IN	port_cap_limit	(: 1.706)
key[126]	IN	slew_limit	(: 1.500)
key[126]	IN	port_cap_limit	(: 1.706)
key[125]	IN	slew_limit	(: 1.500)
key[125]	IN	port_cap_limit	(: 1.706)
key[124]	IN	slew_limit	(: 1.500)
key[124]	IN	port_cap_limit	(: 1.706)
key[123]	IN	slew_limit	(: 1.500)
key[123]	IN	port_cap_limit	(: 1.706)
key[122]	IN	slew_limit	(: 1.500)
key[122]	IN	port_cap_limit	(: 1.706)
key[121]	IN	slew_limit	(: 1.500)
key[121]	IN	port_cap_limit	(: 1.706)
key[120]	IN	slew_limit	(: 1.500)
key[120]	IN	port_cap_limit	(: 1.706)
key[119]	IN	slew_limit	(: 1.500)
key[119]	IN	port_cap_limit	(: 1.706)
key[118]	IN	slew_limit	(: 1.500)
key[118]	IN	port_cap_limit	(: 1.706)
key[117]	IN	slew_limit	(: 1.500)
key[117]	IN	port_cap_limit	(: 1.706)
key[116]	IN	slew_limit	(: 1.500)
key[116]	IN	port_cap_limit	(: 1.706)
key[115]	IN	slew_limit	(: 1.500)
key[115]	IN	port_cap_limit	(: 1.706)
key[114]	IN	slew_limit	(: 1.500)
key[114]	IN	port_cap_limit	(: 1.706)
key[113]	IN	slew_limit	(: 1.500)
key[113]	IN	port_cap_limit	(: 1.706)
key[112]	IN	slew_limit	(: 1.500)
key[112]	IN	port_cap_limit	(: 1.706)
key[111]	IN	slew_limit	(: 1.500)
key[111]	IN	port_cap_limit	(: 1.706)
key[110]	IN	slew_limit	(: 1.500)
key[110]	IN	port_cap_limit	(: 1.706)
key[109]	IN	slew_limit	(: 1.500)
key[109]	IN	port_cap_limit	(: 1.706)
key[108]	IN	slew_limit	(: 1.500)
key[108]	IN	port_cap_limit	(: 1.706)
key[107]	IN	slew_limit	(: 1.500)
key[107]	IN	port_cap_limit	(: 1.706)
key[106]	IN	slew_limit	(: 1.500)
key[106]	IN	port_cap_limit	(: 1.706)
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text_in[34]	IN	slew_limit	(: 1.500)
text_in[34]	IN	port_cap_limit	(: 1.706)
text_in[33]	IN	slew_limit	(: 1.500)
text_in[33]	IN	port_cap_limit	(: 1.706)
text_in[32]	IN	slew_limit	(: 1.500)
text_in[32]	IN	port_cap_limit	(: 1.706)
text_in[31]	IN	slew_limit	(: 1.500)
text_in[31]	IN	port_cap_limit	(: 1.706)
text_in[30]	IN	slew_limit	(: 1.500)
text_in[30]	IN	port_cap_limit	(: 1.706)
text_in[29]	IN	slew_limit	(: 1.500)
text_in[29]	IN	port_cap_limit	(: 1.706)
text_in[28]	IN	slew_limit	(: 1.500)
text_in[28]	IN	port_cap_limit	(: 1.706)
text_in[27]	IN	slew_limit	(: 1.500)
text_in[27]	IN	port_cap_limit	(: 1.706)
text_in[26]	IN	slew_limit	(: 1.500)
text_in[26]	IN	port_cap_limit	(: 1.706)
text_in[25]	IN	slew_limit	(: 1.500)
text_in[25]	IN	port_cap_limit	(: 1.706)
text_in[24]	IN	slew_limit	(: 1.500)
text_in[24]	IN	port_cap_limit	(: 1.706)
text_in[23]	IN	slew_limit	(: 1.500)
text_in[23]	IN	port_cap_limit	(: 1.706)
text_in[22]	IN	slew_limit	(: 1.500)
text_in[22]	IN	port_cap_limit	(: 1.706)

```
|  text_in[21] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[21] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[20] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[20] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[19] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[19] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[18] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[18] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[17] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[17] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[16] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[16] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[15] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[15] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[14] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[14] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[13] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[13] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[12] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[12] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[11] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[11] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[10] |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[10] |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[9]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[9]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[8]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[8]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[7]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[7]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[6]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[6]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[5]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[5]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[4]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[4]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[3]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[3]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[2]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[2]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[1]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[1]  |  IN   | port_cap_limit | (  : 1.706 ) |
|  text_in[0]  |  IN   |   slew_limit   | (  : 1.500 ) |
|  text_in[0]  |  IN   | port_cap_limit | (  : 1.706 ) |
|     clk      |  IN   |   slew_limit   | (  : 1.500 ) |
|     clk      |  IN   | port_cap_limit | (  : 1.706 ) |
|     rst      |  IN   |   slew_limit   | (  : 1.500 ) |
|     rst      |  IN   | port_cap_limit | (  : 1.706 ) |
|      ld      |  IN   |   slew_limit   | (  : 1.500 ) |
|      ld      |  IN   | port_cap_limit | (  : 1.706 ) |
+--------------------<CMD> man get_nets
<CMD> man get_nets */CP
**WARN: (TCLCMD-513): No matching object found for '*/CP'
**ERROR: (TCLCMD-917): Cannot find 'nets' that match '*/CP'
\|sa11_reg[1] /CP \|sa10_reg[1] /CP \|sa32_reg[7] /CP \|sa13_reg[4] /CP \|sa13_reg[5] /CP
\|sa01_reg[2] /CP \|dcnt_reg[1] /CP \|done_reg /CP \|dcnt_reg[2] /CP \|dcnt_reg[3] /CP
\|dcnt_reg[0] /CP \|text_in_r_reg[12] /CP \|text_in_r_reg[13] /CP \|text_in_r_reg[14] /CP
\|text_in_r_reg[15] /CP \|text_in_r_reg[16] /CP \|text_in_r_reg[17] /CP \|text_in_r_reg[18] /CP
\|text_in_r_reg[19] /CP \|text_in_r_reg[20] /CP \|text_in_r_reg[21] /CP \|text_in_r_reg[22] /CP
\|text_in_r_reg[23] /CP \|text_in_r_reg[24] /CP \|text_in_r_reg[25] /CP \|text_in_r_reg[26] /CP
\|text_in_r_reg[27] /CP \|text_in_r_reg[28] /CP \|text_in_r_reg[29] /CP \|text_in_r_reg[30] /CP
\|text_in_r_reg[31] /CP \|text_in_r_reg[32] /CP \|text_in_r_reg[33] /CP \|text_in_r_reg[34] /CP
\|text_in_r_reg[35] /CP \|text_in_r_reg[36] /CP \|text_in_r_reg[37] /CP \|text_in_r_reg[38] /CP
\|text_in_r_reg[39] /CP \|text_in_r_reg[40] /CP \|text_in_r_reg[41] /CP \|text_in_r_reg[42] /CP
\|text_in_r_reg[43] /CP \|text_in_r_reg[44] /CP \|text_in_r_reg[45] /CP \|text_in_r_reg[46] /CP
\|text_in_r_reg[47] /CP \|text_in_r_reg[48] /CP \|text_in_r_reg[49] /CP \|text_in_r_reg[50] /CP
\|text_in_r_reg[51] /CP \|text_in_r_reg[52] /CP \|text_in_r_reg[53] /CP \|text_in_r_reg[54] /CP
\|text_in_r_reg[55] /CP \|text_in_r_reg[56] /CP \|text_in_r_reg[57] /CP \|text_in_r_reg[58] /CP
```

\|text_in_r_reg[59] /CP \|text_in_r_reg[60] /CP \|text_in_r_reg[61] /CP \|text_in_r_reg[62] /CP
\|text_in_r_reg[63] /CP \|text_in_r_reg[64] /CP \|text_in_r_reg[65] /CP \|text_in_r_reg[66] /CP
\|text_in_r_reg[67] /CP \|text_in_r_reg[68] /CP \|text_in_r_reg[69] /CP \|text_in_r_reg[70] /CP
\|text_in_r_reg[97] /CP \|text_in_r_reg[71] /CP \|text_in_r_reg[72] /CP \|text_in_r_reg[73] /CP
\|text_in_r_reg[74] /CP \|text_in_r_reg[75] /CP \|text_in_r_reg[76] /CP \|text_in_r_reg[77] /CP
\|text_in_r_reg[78] /CP \|text_in_r_reg[79] /CP \|text_in_r_reg[80] /CP \|text_in_r_reg[81] /CP
\|text_in_r_reg[82] /CP \|text_in_r_reg[83] /CP \|text_in_r_reg[84] /CP \|text_in_r_reg[85] /CP
\|text_in_r_reg[86] /CP \|text_in_r_reg[87] /CP \|text_in_r_reg[88] /CP \|text_in_r_reg[89] /CP
\|text_in_r_reg[90] /CP \|text_in_r_reg[91] /CP \|text_in_r_reg[92] /CP \|text_in_r_reg[93] /CP
\|text_in_r_reg[94] /CP \|text_in_r_reg[95] /CP \|text_in_r_reg[96] /CP \|text_in_r_reg[98] /CP
\|text_in_r_reg[99] /CP \|text_in_r_reg[100] /CP \|text_in_r_reg[101] /CP \|text_in_r_reg[102]
/CP \|text_in_r_reg[103] /CP \|text_in_r_reg[104] /CP \|text_in_r_reg[105] /CP
\|text_in_r_reg[106] /CP \|text_in_r_reg[107] /CP \|text_in_r_reg[108] /CP \|text_in_r_reg[109]
/CP \|text_in_r_reg[110] /CP \|text_in_r_reg[111] /CP \|text_in_r_reg[112] /CP
\|text_in_r_reg[113] /CP \|text_in_r_reg[114] /CP \|text_in_r_reg[115] /CP \|text_in_r_reg[116]
/CP \|text_in_r_reg[117] /CP \|text_in_r_reg[118] /CP \|text_in_r_reg[119] /CP
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/CP \|text_in_r_reg[124] /CP \|text_in_r_reg[125] /CP \|text_in_r_reg[126] /CP
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\|u0|w_reg[3][27] /CP \|u0|w_reg[1][27] /CP \|u0|w_reg[3][26] /CP \|u0|w_reg[1][26] /CP
\|u0|w_reg[3][25] /CP \|u0|w_reg[1][25] /CP \|u0|w_reg[3][20] /CP \|u0|w_reg[2][20] /CP
\|u0|w_reg[3][19] /CP \|u0|w_reg[1][19] /CP \|u0|w_reg[3][17] /CP \|u0|w_reg[2][17] /CP
\|u0|w_reg[3][12] /CP \|u0|w_reg[1][12] /CP \|u0|w_reg[3][11] /CP \|u0|w_reg[1][11] /CP
\|u0|w_reg[3][10] /CP \|u0|w_reg[1][10] /CP \|u0|w_reg[3][4] /CP \|u0|w_reg[2][4] /CP
\|u0|w_reg[3][3] /CP \|u0|w_reg[1][3] /CP \|u0|w_reg[3][1] /CP \|u0|w_reg[2][1] /CP
\|u0|w_reg[3][18] /CP \|u0|w_reg[2][18] /CP \|u0|w_reg[3][2] /CP \|u0|w_reg[2][2] /CP
\|u0|w_reg[2][28] /CP \|u0|w_reg[1][28] /CP \|u0|w_reg[1][20] /CP \|u0|w_reg[0][20] /CP
\|u0|w_reg[1][17] /CP \|u0|w_reg[0][17] /CP \|u0|w_reg[1][4] /CP \|u0|w_reg[0][4] /CP
\|u0|w_reg[1][1] /CP \|u0|w_reg[0][1] /CP \|u0|w_reg[1][18] /CP \|u0|w_reg[0][18] /CP
\|u0|w_reg[1][2] /CP \|u0|w_reg[0][2] /CP \|u0|w_reg[3][14] /CP \|u0|w_reg[2][14] /CP
\|u0|w_reg[2][10] /CP \|u0|w_reg[2][12] /CP \|u0|w_reg[2][9] /CP \|u0|w_reg[2][11] /CP
\|u0|w_reg[2][13] /CP \|u0|w_reg[3][13] /CP \|u0|w_reg[2][19] /CP \|u0|w_reg[2][3] /CP
\|u0|w_reg[2][8] /CP \|u0|w_reg[3][8] /CP \|u0|w_reg[3][16] /CP \|u0|w_reg[2][16] /CP
\|u0|w_reg[3][0] /CP \|u0|w_reg[2][0] /CP \|u0|w_reg[3][21] /CP \|u0|w_reg[2][21] /CP
\|u0|w_reg[3][22] /CP \|u0|w_reg[2][22] /CP \|u0|w_reg[3][5] /CP \|u0|w_reg[2][5] /CP
\|u0|w_reg[3][6] /CP \|u0|w_reg[2][6] /CP \|u0|r0|out_reg[29] /CP \|u0|r0|out_reg[27] /CP
\|u0|r0|out_reg[26] /CP \|u0|r0|out_reg[31] /CP \|u0|r0|out_reg[28] /CP \|u0|r0|out_reg[30] /CP
\|u0|r0|rcnt_reg[3] /CP \|u0|r0|out_reg[25] /CP \|u0|r0|rcnt_reg[0] /CP \|u0|r0|rcnt_reg[2] /CP
\|u0|r0|rcnt_reg[1] /CP \|u0|r0|out_reg[24] /CP \|u0|w_reg[0][10] /CP \|u0|w_reg[0][12] /CP
\|u0|w_reg[0][9] /CP \|u0|w_reg[0][11] /CP \|u0|w_reg[0][13] /CP \|u0|w_reg[1][13] /CP
\|u0|w_reg[1][14] /CP \|u0|w_reg[0][14] /CP \|u0|w_reg[0][19] /CP \|u0|w_reg[0][3] /CP
\|u0|w_reg[0][8] /CP \|u0|w_reg[1][8] /CP \|u0|w_reg[0][16] /CP \|u0|w_reg[1][16] /CP
\|u0|w_reg[0][0] /CP \|u0|w_reg[1][0] /CP \|u0|w_reg[0][21] /CP \|u0|w_reg[1][21] /CP
\|u0|w_reg[0][22] /CP \|u0|w_reg[1][22] /CP \|u0|w_reg[0][5] /CP \|u0|w_reg[1][5] /CP
\|u0|w_reg[0][6] /CP \|u0|w_reg[1][6] /CP \|u0|w_reg[3][24] /CP \|u0|w_reg[2][24] /CP
\|u0|w_reg[0][24] /CP \|u0|w_reg[0][27] /CP \|u0|w_reg[2][27] /CP \|u0|w_reg[0][29] /CP
\|u0|w_reg[2][29] /CP \|u0|w_reg[3][29] /CP \|u0|w_reg[0][30] /CP \|u0|w_reg[3][30] /CP
\|u0|w_reg[2][30] /CP \|u0|w_reg[2][7] /CP \|u0|w_reg[3][7] /CP \|u0|w_reg[2][31] /CP
\|u0|w_reg[2][23] /CP \|u0|w_reg[2][15] /CP \|u0|w_reg[3][15] /CP \|u0|w_reg[3][23] /CP
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\|u0|w_reg[2][25] /CP \|u0|w_reg[2][26] /CP \|u0|w_reg[1][24] /CP \|u0|w_reg[0][28] /CP
\|u0|w_reg[1][29] /CP \|u0|w_reg[1][30] /CP \|u0|w_reg[0][15] /CP \|u0|w_reg[0][7] /CP
\|u0|w_reg[1][15] /CP \|u0|w_reg[1][7] /CP \|u0|w_reg[1][31] /CP \|u0|w_reg[1][23] /CP
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\|text_in_r_reg[11] /CP \|ld_r_reg /CP \|sa33_reg[1] /CP \|sa20_reg[2] /CP \|sa00_reg[2] /CP
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\|sa21_reg[4] /CP \|sa11_reg[7] /CP \|sa01_reg[4] /CP \|sa20_reg[4] /CP \|sa00_reg[4] /CP
\|sa23_reg[4] /CP \|sa23_reg[3] /CP \|sa23_reg[1] /CP \|sa01_reg[1] /CP \|sa01_reg[3] /CP
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\|sa01_reg[0] /CP \|sa30_reg[3] /CP \|sa30_reg[4] /CP \|sa20_reg[3] /CP \|sa20_reg[5] /CP

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\|sa00_reg[5] /CP \|sa10_reg[5] /CP \|sa20_reg[6] /CP \|sa00_reg[6] /CP \|sa30_reg[6] /CP
\|sa10_reg[7] /CP \|sa10_reg[6] /CP \|sa30_reg[5] /CP \|sa00_reg[7] /CP \|sa00_reg[3] /CP
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\|sa02_reg[2] /CP \|sa12_reg[1] /CP \|sa22_reg[1] /CP \|sa12_reg[3] /CP \|sa32_reg[2] /CP
\|sa22_reg[0] /CP \|sa12_reg[0] /CP \|sa02_reg[3] /CP \|sa22_reg[2] /CP \|sa12_reg[2] /CP
\|sa12_reg[4] /CP \|sa02_reg[0] /CP \|sa32_reg[0] /CP \|sa32_reg[3] /CP \|sa02_reg[6] /CP
\|sa32_reg[5] /CP \|sa22_reg[3] /CP \|sa22_reg[4] /CP \|sa02_reg[7] /CP \|sa12_reg[7] /CP
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\|sa13_reg[6] /CP \|sa13_reg[7] /CP \|sa23_reg[0] /CP \|sa23_reg[7] /CP \|text_out_reg[31] /CP
\|text_out_reg[30] /CP \|text_out_reg[29] /CP \|text_out_reg[15] /CP \|text_out_reg[14] /CP
\|text_out_reg[13] /CP \|text_out_reg[24] /CP \|text_out_reg[22] /CP \|text_out_reg[21] /CP
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\|text_out_reg[76] /CP \|text_out_reg[74] /CP \|text_out_reg[79] /CP \|text_out_reg[78] /CP
\|text_out_reg[77] /CP \|text_out_reg[75] /CP \|text_out_reg[73] /CP \|text_out_reg[92] /CP
\|text_out_reg[90] /CP \|text_out_reg[95] /CP \|text_out_reg[94] /CP \|text_out_reg[93] /CP
\|text_out_reg[91] /CP \|text_out_reg[89] /CP \|text_out_reg[88] /CP \|text_out_reg[104] /CP
\|text_out_reg[108] /CP \|text_out_reg[106] /CP \|text_out_reg[111] /CP \|text_out_reg[110] /CP
\|text_out_reg[109] /CP \|text_out_reg[107] /CP \|text_out_reg[105] /CP \|text_out_reg[48] /CP
\|text_out_reg[52] /CP \|text_out_reg[51] /CP \|text_out_reg[49] /CP \|text_out_reg[55] /CP
\|text_out_reg[54] /CP \|text_out_reg[53] /CP \|text_out_reg[50] /CP \|text_out_reg[80] /CP
\|text_out_reg[84] /CP \|text_out_reg[83] /CP \|text_out_reg[81] /CP \|text_out_reg[87] /CP
\|text_out_reg[86] /CP \|text_out_reg[85] /CP \|text_out_reg[82] /CP \|text_out_reg[112] /CP
\|text_out_reg[116] /CP \|text_out_reg[115] /CP \|text_out_reg[113] /CP \|text_out_reg[119] /CP
\|text_out_reg[118] /CP \|text_out_reg[117] /CP \|text_out_reg[114] /CP \|text_out_reg[56] /CP
\|text_out_reg[61] /CP \|text_out_reg[63] /CP \|text_out_reg[62] /CP \|text_out_reg[60] /CP
\|text_out_reg[59] /CP \|text_out_reg[58] /CP \|text_out_reg[57] /CP \|text_out_reg[120] /CP
\|text_out_reg[124] /CP \|text_out_reg[122] /CP \|text_out_reg[127] /CP \|text_out_reg[126] /CP
\|text_out_reg[125] /CP \|text_out_reg[123] /CP \|text_out_reg[121] /CP
<CMD> report_timing -from \|sa31_reg[6] /Q  -to \|sa32_reg[4] /D
**ERROR: (TCLCMD-981): Unsupported extra argument '/Q' in command 'report_timing'.
<CMD> report_timing -from \|sa31_reg[6]/Q  -to \|sa32_reg[4]/D
Path 1: MET Setup Check with Pin \|sa32_reg[4] /CP
Endpoint:   \|sa32_reg[4] /D (^) checked with  leading edge of 'clk'
Beginpoint: \|sa31_reg[6] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.057
- Setup                         0.058
+ Phase Shift                   2.500
= Required Time                 2.500
- Arrival Time                  2.341
= Slack Time                    0.159
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.057
     = Beginpoint Arrival Time       0.057
     +-------------------------------------------------------------------------------+
     |   Instance    |     Arc     |       Cell        | Delay | Arrival | Required |
     |               |             |                   |       |  Time   |   Time   |
     |---------------+-------------+-------------------+-------+---------+----------|
     | \|sa31_reg[6] | CP ^        |                   |       |   0.057 |    0.216 |
     | \|sa31_reg[6] | CP ^ -> Q v | HS65_GS_DFPQX4    | 0.143 |   0.200 |    0.359 |
     | \|us31|U12    | A v -> Z v  | HS65_GS_BFX9      | 0.140 |   0.340 |    0.499 |
     | \|us31|U350   | A v -> Z ^  | HS65_GS_IVX9      | 0.156 |   0.496 |    0.655 |
```

```
| \|us31|U63     | A ^ -> Z v  | HS65_GS_NOR2X6     | 0.118 |   0.614 |    0.773 |
| \|us31|U37     | A v -> Z ^  | HS65_GS_IVX9       | 0.172 |   0.786 |    0.945 |
| \|us31|U234    | A ^ -> Z v  | HS65_GS_NOR2X6     | 0.155 |   0.941 |    1.100 |
| \|us31|U98     | A v -> Z ^  | HS65_GS_IVX9       | 0.081 |   1.021 |    1.180 |
| \|us31|U34     | B ^ -> Z v  | HS65_GS_NOR2X6     | 0.038 |   1.059 |    1.218 |
| \|us31|U266    | C v -> Z v  | HS65_GS_CB4I1X9    | 0.074 |   1.133 |    1.292 |
| \|us31|U265    | F v -> Z ^  | HS65_GS_AOI312X4   | 0.099 |   1.232 |    1.391 |
| \|us31|U264    | E ^ -> Z v  | HS65_GS_OAI212X5   | 0.077 |   1.309 |    1.468 |
| \|us31|U334    | B v -> Z ^  | HS65_GS_AOI12X2    | 0.086 |   1.394 |    1.553 |
| \|us31|U332    | E ^ -> Z v  | HS65_GS_OAI212X5   | 0.067 |   1.461 |    1.620 |
| \|us31|U107    | A v -> Z v  | HS65_GS_NAND4ABX3  | 0.240 |   1.701 |    1.860 |
| \|U818         | B v -> Z ^  | HS65_GSS_XOR2X6    | 0.231 |   1.932 |    2.091 |
| \|U1254        | B ^ -> Z v  | HS65_GSS_XOR3X2    | 0.221 |   2.153 |    2.312 |
| \|U1253        | A v -> Z v  | HS65_GSS_XOR3X2    | 0.142 |   2.296 |    2.454 |
| \|U1251        | D v -> Z ^  | HS65_GS_OAI22X6    | 0.045 |   2.341 |    2.500 |
| \|sa32_reg[4]  | D ^         | HS65_GS_DFPQX4     | 0.000 |   2.341 |    2.500 |
+-------------------------------------------------------------------------------+

<CMD> setAnalysisMode -analysisType bcwc -checkType setup -skew true -clockPropagation sdccontrol
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 100 -net -
summary > timing_reports/report_timing.post_extract.bcwc.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
Calculate delays in BcWc mode...
Topological Sorting (CPU = 0:00:01.7, MEM = 380.3M)
Number of Loop : 0
Start delay calculation (mem=380.320M)...
delayCal using detail RC...
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[121] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[123] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[125] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[126] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[127] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[122] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[124] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[124] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[120] /\vdd!  is connected to power/ground
net \vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[120] /\gnd!  is connected to power/ground
net \gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[57] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[57] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
**WARN: (ENCDC-348):  The output pin \|text_out_reg[58] /\vdd!  is connected to power/ground net
\vdd! . This can compromise the delay calculation. Fix the netlist and re-run.
```

```
**WARN: (ENCDC-348):  The output pin \|text_out_reg[58] /\gnd!  is connected to power/ground net
\gnd! . This can compromise the delay calculation. Fix the netlist and re-run.
Delay calculation completed. (cpu=0:00:01.8 real=0:00:02.0 mem=380.320M 0)
*** CDM Built up (cpu=0:00:05.1  real=0:00:06.0  mem= 380.3M) ***
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 200 -net -
summary > timing_reports/report_timing.post_extract.bcwc.summary
**WARN: (TCLCMD-566): Option '-summary' for command 'report_timing' is obsolete and has been
replaced by '-path_type end'. The obsolete option still works in this release, but to avoid this
warning and to ensure compatibility with future releases, update your script to use '-path_type
end'.
<CMD> report_power


Start force assigning power rail voltages for view default_view_setup
Finished assigning power rail voltages

CPE found ground net: gnd!
CPE found power net: vdd!  voltage: 0.9V

Propagating signal activity...


Starting Activity Propagation
2011-May-06 10:15:09 (2011-May-06 15:15:09 GMT)
2011-May-06 10:15:09 (2011-May-06 15:15:09 GMT): 5%
2011-May-06 10:15:09 (2011-May-06 15:15:09 GMT): 10%
2011-May-06 10:15:09 (2011-May-06 15:15:09 GMT): 15%
2011-May-06 10:15:09 (2011-May-06 15:15:09 GMT): 20%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 25%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 30%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 35%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 40%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 45%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 50%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 55%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 60%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 65%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 70%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 75%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 80%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 85%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 90%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 95%

Finished Activity Propagation
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT)

Starting Calculating power
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT)

Calculating power dissipation...

 ... Calculating switching power
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 5%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 10%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 15%
2011-May-06 10:15:10 (2011-May-06 15:15:10 GMT): 20%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 25%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 30%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 35%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 40%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 45%
2011-May-06 10:15:11 (2011-May-06 15:15:11 GMT): 50%
 ... Calculating internal and leakage power
2011-May-06 10:15:13 (2011-May-06 15:15:13 GMT): 55%
2011-May-06 10:15:16 (2011-May-06 15:15:16 GMT): 60%
2011-May-06 10:15:19 (2011-May-06 15:15:19 GMT): 65%
2011-May-06 10:15:22 (2011-May-06 15:15:22 GMT): 70%
```

```
2011-May-06 10:15:25 (2011-May-06 15:15:25 GMT): 75%
2011-May-06 10:15:28 (2011-May-06 15:15:28 GMT): 80%
2011-May-06 10:15:31 (2011-May-06 15:15:31 GMT): 85%
2011-May-06 10:15:34 (2011-May-06 15:15:34 GMT): 90%
2011-May-06 10:15:37 (2011-May-06 15:15:37 GMT): 95%

Finished Calculating power
2011-May-06 10:15:38 (2011-May-06 15:15:38 GMT)
*-------------------------------------------------------------------------------------------
*        -  - Version  32-bit
*
*
*       Date & Time:   2011-May-06 10:15:38 (2011-May-06 15:15:38 GMT)
*
*-------------------------------------------------------------------------------------------
*
*       Design: aes_cipher_top
*
*       Liberty Libraries used:
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib
*
*       Power Domain used:
*              Rail:       vdd!      Voltage:        0.9
*
*       Power Units = 1mW
*
*       Time Units = 1e-09 secs
*
*       report_power
*
-------------------------------------------------------------------------------------------


Total Power
-------------------------------------------------------------------------------------------
Total Internal Power:       9.113      30.12%
Total Switching Power:       20.01      66.14%
Total Leakage Power:        1.13      3.737%
Total Power:       30.25
-------------------------------------------------------------------------------------------


Group                            Internal   Switching     Leakage       Total  Percentage
                                 Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------------
Sequential                          2.412        1.34      0.1459       3.899       12.89
Macro                                   0           0           0           0           0
IO                                      0           0           0           0           0
Combinational                       6.701       18.67      0.9845       26.35       87.11
Clock (Combinational)                   0           0           0           0           0
-------------------------------------------------------------------------------------------
Total                               9.113       20.01        1.13       30.25         100
-------------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-------------------------------------------------------------------------------------------
vdd!                      0.9          0           0           0           0           0
Default                   0.9      9.113       20.01        1.13       30.25         100


-------------------------------------------------------------------------------------------
```

```
*       Power Distribution Summary:
*              Highest Average Power:                  |u0|U229 (HS65_GSS_XOR2X6):
0.03724
*              Highest Leakage Power:        |text_in_r_reg[11] (HS65_GS_DFPHQX9):
0.0003203
*              Total Cap:     1.29583e-10 F
*              Total instances in design:  9809
*              Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*              Total Fillers and Decap:     0
--------------------------------------------------------------------------------

report_power consumed time (real time) 00:00:32 : increased peak memory
(517M) by 0.
<CMD> reportGateCount
Gate area 1.5600 um^2
[0] aes_cipher_top Gates=22231 Cells=9809 Area=34680.9 um^2
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points  -net
**ERROR: (TCLCMD-164): Number of end points not specified
<CMD> report_timing -format {hpin arc cell delay arrival slew load} -late -max_points 1 -net
Path 1: VIOLATED Setup Check with Pin \|u0|w_reg[2][24] /CP
Endpoint:   \|u0|w_reg[2][24] /D (^) checked with  leading edge of 'clk'
Beginpoint: \|u0|w_reg[3][16] /Q (^) triggered by  leading edge of 'clk'
Other End Arrival Time          0.057
- Setup                         0.056
+ Phase Shift                   2.500
= Required Time                 2.502
- Arrival Time                  3.933
= Slack Time                   -1.431
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.057
     = Beginpoint Arrival Time           0.057
     +-------------------------------------------------------------------------------------------------
+
     |          Pin          |     Arc     |       Cell        | Delay | Arrival |  Slew |  Load
|
     |                       |             |                   |       |  Time   |       |
|
     |-----------------------+-------------+-------------------+-------+---------+-------+-------
|
     | \|u0|w_reg[3][16] /CP | CP ^        |                   |       |   0.057 | 0.057 | 0.575
|
     | \|u0|w_reg[3][16] /Q  | CP ^ -> Q ^ | HS65_GS_DFPQX4    | 0.335 |   0.393 | 0.473 | 0.073
|
     | \|u0|u0|U411 /A       |             | HS65_GS_BFX9      | 0.003 |   0.396 | 0.473 | 0.073
|
     | \|u0|u0|U411 /Z       | A ^ -> Z ^  | HS65_GS_BFX9      | 0.305 |   0.701 | 0.316 | 0.095
|
     | \|u0|u0|U380 /A       |             | HS65_GS_IVX9      | 0.010 |   0.711 | 0.316 | 0.095
|
     | \|u0|u0|U380 /Z       | A ^ -> Z v  | HS65_GS_IVX9      | 0.104 |   0.814 | 0.087 | 0.012
|
     | \|u0|u0|U9 /A         |             | HS65_GS_BFX9      | 0.000 |   0.815 | 0.087 | 0.012
|
     | \|u0|u0|U9 /Z         | A v -> Z v  | HS65_GS_BFX9      | 0.119 |   0.934 | 0.089 | 0.043
|
     | \|u0|u0|U309 /A       |             | HS65_GS_NOR2X6    | 0.000 |   0.934 | 0.089 | 0.043
|
     | \|u0|u0|U309 /Z       | A v -> Z ^  | HS65_GS_NOR2X6    | 0.295 |   1.229 | 0.501 | 0.076
|
     | \|u0|u0|U256 /A       |             | HS65_GS_IVX9      | 0.003 |   1.233 | 0.501 | 0.076
|
     | \|u0|u0|U256 /Z       | A ^ -> Z v  | HS65_GS_IVX9      | 0.181 |   1.413 | 0.150 | 0.024
|
     | \|u0|u0|U48 /A        |             | HS65_GS_NOR2X6    | 0.000 |   1.413 | 0.150 | 0.024
|
```

```
     | \|u0|u0|U48 /Z        | A v -> Z ^  | HS65_GS_NOR2X6    | 0.201 |   1.615 | 0.269 | 0.039
|
     | \|u0|u0|U27 /A        |             | HS65_GS_IVX9      | 0.000 |   1.615 | 0.269 | 0.039
|
     | \|u0|u0|U27 /Z        | A ^ -> Z v  | HS65_GS_IVX9      | 0.125 |   1.740 | 0.101 | 0.024
|
     | \|u0|u0|U26 /A        |             | HS65_GS_NOR2X6    | 0.000 |   1.740 | 0.101 | 0.024
|
     | \|u0|u0|U26 /Z        | A v -> Z ^  | HS65_GS_NOR2X6    | 0.098 |   1.837 | 0.160 | 0.014
|
     | \|u0|u0|U215 /A       |             | HS65_GS_CBI4I1X5  | 0.000 |   1.837 | 0.160 | 0.014
|
     | \|u0|u0|U215 /Z       | A ^ -> Z v  | HS65_GS_CBI4I1X5  | 0.077 |   1.914 | 0.068 | 0.004
|
     | \|u0|u0|U172 /E       |             | HS65_GS_OAI212X5  | 0.000 |   1.914 | 0.068 | 0.004
|
     | \|u0|u0|U172 /Z       | E v -> Z ^  | HS65_GS_OAI212X5  | 0.044 |   1.959 | 0.082 | 0.002
|
     | \|u0|u0|U170 /E       |             | HS65_GS_AOI212X4  | 0.000 |   1.959 | 0.082 | 0.002
|
     | \|u0|u0|U170 /Z       | E ^ -> Z v  | HS65_GS_AOI212X4  | 0.059 |   2.018 | 0.083 | 0.006
|
     | \|u0|u0|U397 /D       |             | HS65_GS_NAND4ABX3 | 0.000 |   2.018 | 0.083 | 0.006
|
     | \|u0|u0|U397 /Z       | D v -> Z ^  | HS65_GS_NAND4ABX3 | 0.043 |   2.061 | 0.040 | 0.001
|
     | \|u0|u0|U395 /B       |             | HS65_GS_NAND4ABX3 | 0.000 |   2.061 | 0.040 | 0.001
|
     | \|u0|u0|U395 /Z       | B ^ -> Z ^  | HS65_GS_NAND4ABX3 | 0.079 |   2.140 | 0.102 | 0.009
|
     | \|u0|U72 /B           |             | HS65_GSS_XOR2X6   | 0.000 |   2.140 | 0.102 | 0.009
|
     | \|u0|U72 /Z           | B ^ -> Z ^  | HS65_GSS_XOR2X6   | 0.204 |   2.344 | 0.301 | 0.040
|
     | \|u0|U144 /A          |             | HS65_GSS_XOR3X2   | 0.007 |   2.351 | 0.301 | 0.040
|
     | \|u0|U144 /Z          | A ^ -> Z ^  | HS65_GSS_XOR3X2   | 0.580 |   2.931 | 0.902 | 0.047
|
     | \|u0|U229 /B          |             | HS65_GSS_XOR2X6   | 0.002 |   2.933 | 0.902 | 0.047
|
     | \|u0|U229 /Z          | B ^ -> Z ^  | HS65_GSS_XOR2X6   | 0.773 |   3.707 | 0.761 | 0.108
|
     | \|u0|U228 /C          |             | HS65_GS_AO22X9    | 0.005 |   3.712 | 0.761 | 0.108
|
     | \|u0|U228 /Z          | C ^ -> Z ^  | HS65_GS_AO22X9    | 0.221 |   3.933 | 0.057 | 0.006
|
     | \|u0|w_reg[2][24] /D  |             | HS65_GS_DFPQX4    | 0.000 |   3.933 | 0.057 | 0.006
|
     +-------------------------------------------------------------------------------------------
+

<CMD> report_timing -from \|sa31_reg[6]/Q  -to
\|sa32_reg[4]/D/scratch/arvind/65nm/522/techlib_for_encounter
**WARN: (TCLCMD-513):  No matching object found for
'|sa32_reg[4]/D/scratch/arvind/65nm/522/techlib_for_encounter'
<CMD> report_timing -from \|sa31_reg[6]/Q  -to \|sa32_reg[4]/D
Path 1: MET Setup Check with Pin \|sa32_reg[4] /CP
Endpoint:   \|sa32_reg[4] /D (^) checked with  leading edge of 'clk'
Beginpoint: \|sa31_reg[6] /Q (v) triggered by  leading edge of 'clk'
Other End Arrival Time          0.057
- Setup                         0.058
+ Phase Shift                   2.500
= Required Time                 2.500
- Arrival Time                  2.341
= Slack Time                    0.159
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  0.057
     = Beginpoint Arrival Time       0.057
```

```
+-------------------------------------------------------------------------------+
|   Instance    |     Arc     |       Cell        | Delay | Arrival | Required |
|               |             |                   |       |  Time   |   Time   |
|---------------+-------------+-------------------+-------+---------+----------|
| \|sa31_reg[6] | CP ^        |                   |       |   0.057 |    0.216 |
| \|sa31_reg[6] | CP ^ -> Q v | HS65_GS_DFPQX4    | 0.143 |   0.200 |    0.359 |
| \|us31|U12    | A v -> Z v  | HS65_GS_BFX9      | 0.140 |   0.340 |    0.499 |
| \|us31|U350   | A v -> Z ^  | HS65_GS_IVX9      | 0.156 |   0.496 |    0.655 |
| \|us31|U63    | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.118 |   0.614 |    0.773 |
| \|us31|U37    | A v -> Z ^  | HS65_GS_IVX9      | 0.172 |   0.786 |    0.945 |
| \|us31|U234   | A ^ -> Z v  | HS65_GS_NOR2X6    | 0.155 |   0.941 |    1.100 |
| \|us31|U98    | A v -> Z ^  | HS65_GS_IVX9      | 0.081 |   1.021 |    1.180 |
| \|us31|U34    | B ^ -> Z v  | HS65_GS_NOR2X6    | 0.038 |   1.059 |    1.218 |
| \|us31|U266   | C v -> Z v  | HS65_GS_CB4I1X9   | 0.074 |   1.133 |    1.292 |
| \|us31|U265   | F v -> Z ^  | HS65_GS_AOI312X4  | 0.099 |   1.232 |    1.391 |
| \|us31|U264   | E ^ -> Z v  | HS65_GS_OAI212X5  | 0.077 |   1.309 |    1.468 |
| \|us31|U334   | B v -> Z ^  | HS65_GS_AOI12X2   | 0.086 |   1.394 |    1.553 |
| \|us31|U332   | E ^ -> Z v  | HS65_GS_OAI212X5  | 0.067 |   1.461 |    1.620 |
| \|us31|U107   | A v -> Z v  | HS65_GS_NAND4ABX3 | 0.240 |   1.701 |    1.860 |
| \|U818        | B v -> Z ^  | HS65_GSS_XOR2X6   | 0.231 |   1.932 |    2.091 |
| \|U1254       | B ^ -> Z v  | HS65_GSS_XOR3X2   | 0.221 |   2.153 |    2.312 |
| \|U1253       | A v -> Z v  | HS65_GSS_XOR3X2   | 0.142 |   2.296 |    2.454 |
| \|U1251       | D v -> Z ^  | HS65_GS_OAI22X6   | 0.045 |   2.341 |    2.500 |
| \|sa32_reg[4] | D ^         | HS65_GS_DFPQX4    | 0.000 |   2.341 |    2.500 |
+-------------------------------------------------------------------------------+

<CMD> report_power


*-----------------------------------------------------------------------------------------
*        -  - Version  32-bit
*
*
*       Date & Time:   2011-May-12 18:30:21 (2011-May-12 23:30:21 GMT)
*
*-----------------------------------------------------------------------------------------
*
*       Design: aes_cipher_top
*
*       Liberty Libraries used:
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_wc_0.90V_125C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_wc_1.10V_125C.lib
*               LIBRARIES/CORE65GPSVT/libs/CORE65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/CLOCK65GPSVT/libs/CLOCK65GPSVT_nom_1.00V_25C.lib
*               LIBRARIES/PRHS65/libs/PRHS65_nom_1.20V_25C.lib
*
*       Power Domain used:
*              Rail:       vdd!      Voltage:        0.9
*
*       Power Units = 1mW
*
*       Time Units = 1e-09 secs
*
*        report_power
*
-----------------------------------------------------------------------------------------


Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:       9.113      30.12%
Total Switching Power:       20.01      66.14%
Total Leakage Power:        1.13      3.737%
Total Power:       30.25
-----------------------------------------------------------------------------------------
```

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	2.412	1.34	0.1459	3.899	12.89
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	6.701	18.67	0.9845	26.35	87.11
Clock (Combinational)	0	0	0	0	0
Total	9.113	20.01	1.13	30.25	100

Rail	Voltage	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
vdd!	0.9	0	0	0	0	0
Default	0.9	9.113	20.01	1.13	30.25	100

```
*       Power Distribution Summary:
*              Highest Average Power:                  |u0|U229 (HS65_GSS_XOR2X6):
0.03724
*              Highest Leakage Power:        |text_in_r_reg[11] (HS65_GS_DFPHQX9):
0.0003203
*              Total Cap:     1.29583e-10 F
*              Total instances in design:  9809
*              Total instances in design with no power:     0
*                Total instances in design with no activty:     0

*              Total Fillers and Decap:     0
```